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Dissertation

A Control Concept for Highly-dynamic Operation of DC Converters Driving Nonlinear Loads

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von

Dipl.-Ing. Michael Zauner
[redacted]

Wien, am 12. Mai 2022

Meiner Familie und Freunden

Danksagung

Leider lässt sich eine wahrhafte Dankbarkeit mit Worten nicht ausdrücken.

Johann Wolfgang von Goethe (1749-1832)

Eidesstattliche Erklärung

Ich erkläre an Eides statt, dass die vorliegende Arbeit nach den anerkannten Grundsätzen für wissenschaftliche Abhandlungen von mir selbstständig erstellt wurde. Alle verwendeten Hilfsmittel, insbesondere die zugrunde gelegte Literatur, sind in dieser Arbeit genannt und aufgelistet. Die aus den Quellen wörtlich entnommenen Stellen, sind als solche kenntlich gemacht. Das Thema dieser Arbeit wurde von mir bisher weder im In- noch Ausland einer Beurteilerin/einem Beurteiler zur Begutachtung in irgendeiner Form als Prüfungsarbeit vorgelegt. Diese Arbeit stimmt mit der von den Begutachterinnen/Begutachtern beurteilten Arbeit überein. Ich nehme zur Kenntnis, dass die vorgelegte Arbeit mit geeigneten und dem derzeitigen Stand der Technik entsprechenden Mitteln (Plagiat-Erkennungssoftware) elektronisch-technisch überprüft wird. Dies stellt einerseits sicher, dass bei der Erstellung der vorgelegten Arbeit die hohen Qualitätsvorgaben im Rahmen der geltenden Regeln zur Sicherung guter wissenschaftlicher Praxis „Code of Conduct“ an der TU Wien eingehalten wurden. Zum anderen werden durch einen Abgleich mit anderen studentischen Abschlussarbeiten Verletzungen meines persönlichen Urheberrechts vermieden.

Wien, am 12. Mai 2022 — Michael Zauner

Ich nehme zur Kenntnis, dass ich zur Drucklegung meiner Arbeit unter der Bezeichnung Dissertation nur mit Bewilligung der Prüfungskommission berechtigt bin.

Kurzfassung

Diese Dissertation präsentiert die gesammelten Ergebnisse, welche im Rahmen einer Forschungskooperation zwischen dem Christian Doppler Labor für innovative Regelung und Überwachung von Antriebssystemen an der TU Wien und der AVL List GmbH in Graz entstanden sind.
Das zentrale Thema dieser Arbeit ist die Entwicklung eines hochdynamischen Regelungskonzeptes für DC-Konverter mit nichtlinearen Lasten. Zur Veranschaulichung wird das neuentwickelte Regelungskonzept auf einem DC-Konverter angewendet, welcher in einem Batterie-Emulator für Hardware-in-the-loop (HIL) Prüfstände zum Einsatz kommt. Für die nichtlineare Last wird ein Prüfling mit konstanter Leistungsaufnahme angenommen, was eine zusätzliche Herausforderung darstellt da dies zu Stabilitätsproblemen am DC-Bus führt. Der DC-Konverter in derartigen Emulatoren soll eine möglichst dynamische Ausgangsspannung haben, um die Impedanz einer Batterie genau abbilden zu können. Außerdem sollte diese hohe Ausgangsdynamik über einen möglichst großen Betriebsbereich verfügbar sein, was bei Lasten mit konstanter Leistungsaufnahme aufgrund der Nichtlinearität eine besondere Herausforderung darstellt. Weiters müssen sicherheitsrelevante Komponentenlimits eingehalten werden, um einen problemlosen Betrieb zu gewährleisten.
In der Fachliteratur werden mehrere Regelungskonzepte für DC-Konverter beschrieben, jedoch gehen diese meist von einem einzigen stationären Betriebspunkt aus. Diese Annahme ist ausreichend für den Großteil der Einsatzgebiete, jedoch ist sie nicht zielführend für die Realisierung von hochdynamischen Sollwertänderungen über einen großen Spannungsbereich, welche z.B. bei Batterieemulatoren gefordert werden.
Um die hochdynamischen Anforderungen über einen großen Betriebsbereich zu erfüllen, wurde ein flachheits-basiertes Regelungskonzept entwickelt, welches Rückkopplungsäquivalenz zwischen einem nichtlinearen Systemmodell und einem linearisierten Modell herstellt. Hierbei wird das lineare Modell für die Synthese eines Reglers verwendet, welcher dank der Rückkopplungsäquivalenz in ein nichtlineares Regelgesetzt transformiert werden kann. Dadurch wird der resultierende Regler über einen großen Betriebsbereich anwendbar, was mittels einer Stabilitätsanalyse belegt wird. Das Regelungskonzept wurde weiters auf einem Prototyp einer Hardwareplatine implementiert und mittels Echtzeittests validiert. Zur Einhaltung der sicherheitsrelevanten Limits wird ein modifizierter Referenz-Governor vorgestellt, welcher zusätzlich auftretende Oszillationen während einer Sollwertänderung reduziert.

Abstract

This dissertation presents the collected results of a research project within the Christian Doppler Laboratory for Innovative Control and Monitoring of Automotive Powertrain Systems at TU Wien in cooperation with AVL List GmbH in Graz.
The central topic of this work is the development of a highly-dynamic control concept for DC converters driving nonlinear loads. The newly developed concept is exemplified by applying it to a DC converter used in a battery emulator on a hardware in the loop (HIL) testbed. In this particular setup, a unit under test (UUT) with a constant power draw is assumed as the nonlinear load, which introduces stability issues on the DC bus. The DC converter in such a battery emulator should have a highly dynamic output voltage to accurately emulate the dynamic impedance of a battery. Additionally, there exists a requirement for a large operating region, which is especially challenging for UUTs that behave like a constant power load due to the introduced nonlinearity. Additionally, safety-critical constraints have to be satisfied to ensure proper operation and protection of components.
While the literature describes several specialized control concepts for DC converters, they usually assume a single stationary operating point. This assumption is sufficient for the majority of applications, but it is not suitable for the realization of highly dynamic setpoint changes over a wide voltage range, which are, for example, required for battery emulators.
In order to meet the highly dynamic requirements over a large operating range, a flatness-based control concept was developed, which establishes feedback equivalence between a nonlinear system description and a linearized one. The linearized system is used to synthesize a control law that meets the dynamical requirements, which, thanks to the established feedback equivalence, can be transformed into a nonlinear control law. As a result, the controller becomes applicable over a wide operating range, verified through a stability analysis. The control concept was implemented on a prototype hardware board and validated via real-time tests. In order to meet the safety-critical limits, a modified reference governor is presented that allows for smooth setpoint changes.

Contents

List of Terms and Acronyms

List of Abbreviations

ADC	analog-to-digital converter
BCF	Brunovsky canonical form
C-HIL	control-HIL
CPL	constant power load
DAC	digital-to-analog converter
DC	direct current
DSP	digital signal processor
FPGA	field programmable gate array
HEV	hybrid electric vehicle
HIL	hardware in the loop
ICE	internal combustion engine
IGBT	insulated-gate bipolar transistor
LQR	linear quadratic regulator
MPC	model predicive control
P-HIL	power-HIL
PT1-RG	reference governor with PT1-element
PWM	pulse width modulated
RG	reference governor
ROA	region of attraction
S+H	sample and hold
UUT	unit under test
ZOH	zero order hold

List of Latin Symbols

$\boldsymbol{A}_b$	System matrix of the system in BCF
$\boldsymbol{A}_{cl}$	System matrix of the linear closed-loop system
$\boldsymbol{A}_d$	System matrix of the linear discrete-time system
$\boldsymbol{A}_l$	System matrix of the linear system
$\boldsymbol{B}_b$	Input matrix of the system in BCF
$\boldsymbol{B}_{cl}$	Input matrix of the linear closed-loop system
$\boldsymbol{B}_d$	Input matrix of the linear discrete-time system
$\boldsymbol{B}_l$	Input matrix of the linear system
b_s	Binary variable describing the switch state
c	Bounding level set of Lyapunov function
C_1	Capacitance of converter filter
C_2	Capacitance of output filter
$\boldsymbol{C}_b$	Output matrix of the system in BCF
$\boldsymbol{C}_{cl}$	Output matrix of the linear closed-loop system
$\boldsymbol{C}_d$	Output matrix of the linear discrete-time system
$\boldsymbol{C}_l$	Output matrix of the linear system
$\tilde{\boldsymbol{C}}$	Output matrix for the constraint output
$\mathcal{D}$	Stable region
d_{PWM}	Duty cycle of the PWM signal
$\tilde{\boldsymbol{D}}$	Output matrix for the constraint output
$\boldsymbol{E}_{cl}$	Disturbance matrix of the linear closed-loop system
$\boldsymbol{E}_d$	Disturbance matrix of the linear discrete-time system
$\boldsymbol{E}_l$	Disturbance matrix of the linear system
$\boldsymbol{f}$	Nonlinear system dynamics
f_{PWM}	Frequency of the PWM signal
$\boldsymbol{g}$	Nonlinear input dynamics
$\boldsymbol{h}$	Nonlinear output dynamics
$\tilde{\boldsymbol{h}}$	Function for the constraint output of the closed-loop system
$\tilde{\boldsymbol{h}}_l$	Function for the constraint output of the linear system
i_1	Converter stage current

$i_{1,a}$	Current in Leg a
$i_{1,a,\max}$	Maximal reachable current reference
$i_{1,a,\min}$	Minimal reachable current reference
$i_{1,a,\text{approx}}$	Approximation for the current in Leg a
$i_{1,b}$	Current in Leg b
$i_{1,c}$	Current in Leg c
$i_{1,d}$	Current in Leg d
$i_{1,\text{limit}}$	Converter stage current limit
i_2	Current in cable
$i_{2,\text{limit}}$	Output stage current limit
i_p	Load current
$i_{p,0}$	Load current in the linearization point
J	Cost function for LQR synthesis
k	Discrete index
K_P	Disturbance feedback gain
K_v	Reference feedback gain
$\boldsymbol{K}_x$	State vector feedback gain
L_1	Inductance of each leg
L_2	Inductance of the cable
P	Power draw of the original system
P_0	Power draw in the linearization point
P_l	Power draw of the linear system
$\boldsymbol{Q}$	State weighting matrix of the cost function for LQR synthesis
R	Input weighting matrix of the cost function for LQR synthesis
r	External voltage reference
R_1	Resistance of each leg
$\boldsymbol{S}$	Solution of the discrete-time algebraic Riccati equation
$\boldsymbol{t}$	Nonlinear state vector transformation $\boldsymbol{x} \rightarrow \boldsymbol{z}$
t	Continuous time
t_{on}	Time where the PWM signal is turned on
$\boldsymbol{T}_P$	Part of the state vector transformation $\boldsymbol{x}_l \rightarrow \boldsymbol{z}_l$
T_s	Sampling time

$\boldsymbol{T}_x$	Part of the state vector transformation $\boldsymbol{x}_l \to \boldsymbol{z}_l$
u	Input of the original system
u^*	Ideal input for Σ_{nl}
u_0	Input in the linearization point
u_l	Input of the linear system
u_l^*	Ideal input for Σ_l
u_{limit}	PWM duty cycle limits
V	Lyapunov function candidate for the nonlinear system
v	Internal voltage reference
v_2	Output filter voltage
$v_{2,0}$	Output voltage in the linearization point
v_c	Converter filter voltage
V_{cc}	DC-link voltage
V_l	Lyapunov function candidate for the linear system
$\tilde{v}$	Predicted internal reference voltage
$\mathcal{W}$	Assumed set for input state distortion
$\boldsymbol{w}$	State disturbance of the nonlinear system
$\boldsymbol{w}_l$	State distortion of the linear system due to the input distortion
$\boldsymbol{x}$	State vector of the original system
$\boldsymbol{x}_0$	State vector in the linearization point
$\hat{\boldsymbol{x}}$	Target state given for the nonlinear system
$\hat{\boldsymbol{x}}_l$	Target state given for the linear system
$\boldsymbol{x}_l$	State vector of the linear system
$\boldsymbol{x}_l^*$	State vector of the linear system without a input distortion
$\check{\boldsymbol{x}}_l$	Shifted state vector
$\tilde{\boldsymbol{x}}_l$	Predicted state vector
$\mathcal{Y}$	Convex compact set for constraint output
y	Output of the original system
y_0	Output in the linearization point
y_l	Output of the linear system
$\tilde{\boldsymbol{y}}$	Constraint output of the nonlinear system
$\boldsymbol{z}$	State vector of the original system in BCF
$\boldsymbol{z}_l$	State vector of the linear system in BCF
$\boldsymbol{z}_{l,0}$	State vector of the linear system in BCF in the linearization point

List of Greek Symbols

α	Part of the input transformation $u_l \to u$
β	Part of the input transformation $u_l \to u$
δu_l	Input distortion of Σ_l caused by the ZOH element
Δv_2	Allowable output voltage deviation
ΔV_l^*	Nominal Lyapunov function change with a LQR
κ	Low-pass filter time constant
κ^*	Optimal low-pass filter time constant
Ω	Positive invariant set
$\boldsymbol{\Phi}$	Nonlinear state vector transformation $\boldsymbol{x} \to \boldsymbol{x}_l$
Σ_b	System in BCF
Σ_{cl}	Linear closed-loop system
Σ_d	Linear discrete-time system
Σ_l	Linear system
Σ_{nl}	Nonlinear system
τ	Generic time variable

Chapter 1

Introduction

Over the last decade, the world's energy consumption has steadily increased. One of the fastest-growing sectors in that regard is the transportation sector, which is also one of the leading sources of greenhouse gas emissions due to its dependency on fossil fuels [1]. In an attempt to achieve ambitious climate protection goals [2], all major car manufacturers are investing in new technologies to improve vehicle efficiency. One of the most promising technologies for achieving those goals is the electrification of the powertrain and vehicle subsystems [3]. While many electric, hybrid, and fuel cell vehicles are already commercially available today, there are still barriers to overcome to achieve significant market shares [4]. Therefore, the development of new powertrain solutions is an ongoing topic. In order to reduce costs and speed up the development process of powertrain components, they are commonly tested in hardware in the loop (HIL) environments [5]. In a HIL environment, some physical components of a testbed are replaced with highly dynamic actuators that are controlled such that they behave like the replaced components. Consequently, HIL setups allow individual components to be tested long before a complete prototype vehicle is available, enabling an efficient parallel development strategy. In order to provide a realistic testing environment for the unit under test (UUT) on a HIL testbed, the actuators connected to the UUT have to be accurate and tightly controlled. Furthermore, profound mathematical models that describe the interactions between the actuators and the UUT are required. With a sophisticated HIL setup, results can be obtained that are comparable to test results from an actual vehicle on the road. In Fig. 1.1 an example of a HIL setup is illustrated where the UUTs are an electric motor and inverter: On the left, the powertrain components connected to the UUTs in a hybrid electric vehicle (HEV) with an internal combustion engine (ICE) are shown. On the right, a HIL testbed is illustrated where actuators (a dynamometer and a battery emulator in this case) replace the ICE and the onboard battery.

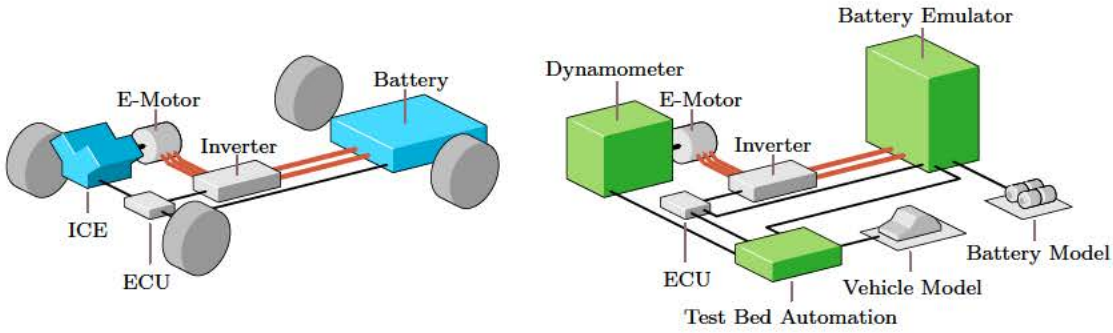

Figure 1.1: Left: Powertrain components in a HEV with an ICE and an onboard battery. Right: HIL testbed for the electric motor and inverter where the ICE and onboard battery are replaced with a dynamometer and a battery emulator respectively.

1.1 Motivation and Overview

Especially in automotive testbeds for electric vehicles and HEV, replacing the physical battery with a battery emulator is highly beneficial. The usage of physical batteries in HIL tests is not only cumbersome (they must be pre-charged and pre-conditioned to achieve the required initial conditions), it is also dangerous, as a faulty UUT can lead to short circuits and fires. Furthermore, a functional battery prototype might not be readily available at earlier points of the development progress. A safer, more efficient, and environmentally friendly solution for HIL testbeds is to use an emulated battery to perform tests in a power-HIL (P-HIL) testing environment [6]. During P-HIL tests, the power components of the UUT are supplied with the same power levels as in the final product, allowing for validation and testing at the UUT's typical operating conditions. As electrical powertrain components became more and more performant, demand for battery emulators capable of higher power levels arose. Typically, such a high-performance battery emulator is realized as a controllable bidirectional DC power supply driven by a real-time-capable battery model that generates a reference trajectory for the output voltage [7]. Obviously, this reference trajectory should be tracked as fast as possible for the most accurate testing results. To achieve fast and accurate tracking of the reference, the controller for the DC power supply should have a high bandwidth while also ensuring that the physical constraints of the system are met. Since a battery emulator represents a significant investment for any company, there exists an incentive to use one device for a wide range of different battery topologies. Consequently, a large viable operating region over a broad range of voltages is desired. However, this requirement is particularly challenging to meet when the connected UUT behaves like a constant power load (CPL). While the instantaneous input impedance of such a CPL

is positive, the incremental input impedance is negative [8]. This discrepancy causes stability issues on the DC bus feeding the CPL [9]. Additionally, the CPL also introduces a nonlinear characteristic into the system [10]. An example of a UUT that draws constant power from its input would be a tightly controlled inverter connected to an electric motor [11].

In this thesis, a highly-dynamic control concept for DC converters with nonlinear loads is proposed and exemplified on a prototype of a battery emulator driving a CPL. The battery emulator prototype was developed by AVL and should feature a large viable operating range for UUTs that behave like CPLs. The controllable DC power supply for this battery emulator is realized as a bidirectional DC-DC converter. Usually, the switches in the converter are driven by pulse width modulated (PWM) signals, with the controlled variable being the duty cycle. However, to ensure signal integrity, the duty cycle can only be changed at the start of each PWM period and has to remain constant throughout the remainder of it. With this limitation, a discrete-time component is introduced into the continuous-time system, effectively turning it into a hybrid system [12]. If only slow system dynamics are desired, one can use state-space averaging methods [13] to avoid the difficulties arising from a hybrid system formulation [14]. With state-space averaging, a continuous-time model can be found that accurately captures the slow dynamics of the system. As state-space averaging is based on the assumption that the PWM period is by far smaller than the time constants of the resulting closed-loop dynamics [15], it quickly reaches its limits when faster dynamics are required. Therefore, in order to avoid a hybrid system representation and achieve the fastest possible dynamics, a new controlled variable in the shape of a piecewise constant time-derivative of the inverter stage current is introduced. A control variable with such a shape could be easily computed via a discrete-time control law, for which a discrete-time representation of the system would be required. However, due to the nonlinearity introduced by the CPL, an analytical solution of the differential equations describing the system cannot be found. In order to solve this problem, the presented control concept establishes feedback equivalence between the nonlinear system description of the plant and a linearized description. It is hypothesized that if both descriptions have similar dynamics and follow the same output trajectory, the required control inputs will be similar in shape. The control concept is investigated in terms of achievable control performance, and the feasibility of a real-time implementation is shown. In addition, a stability analysis is performed to investigate whether the hypothesis mentioned above holds in a large enough operating region. Finally, a modified reference governor with an internal PT1-element is added to the overall control concept to handle constraints in the battery emulator. This reference governor manipulates the internal voltage reference of the controller to avoid state-space regions where safety-critical constraints would be violated.

This dissertation is organized as follows: In the following Section 1.2, the main con-

tributions of this work are collected, and the relevant own scientific publications are listed. Chapter 2 describes the model of the battery emulator in detail and motivates the advantages of using a piecewise constant change in current as a control input. In Chapter 3, the flatness-based control concept is presented which establishes feedback equivalence between a nonlinear and linear model. Additional, simulation results and experimental results are provided in this chapter. In Chapter 4, a stability analysis is carried out to investigate whether the abovementioned hypothesis holds over a sufficiently large operating region. Chapter 5 introduces the reference governor with an internal PT1-element to the control concept and shows why a constraint management scheme is necessary. Finally, conclusions are drawn in Chapter 6, and an outlook is given.

1.2 Contribution

The main contribution of this work is a novel concept for the highly dynamic and safe control of DC converters with nonlinear loads. The new concept is shown in this work by applying it to a DC-DC converter used as a battery emulator in an automotive P-HIL testbed, where the nonlinear load is given by a UUT that draws constant power from the DC bus. The primary focus of the developed method is to provide the fastest possible output dynamics over a large operating region, which is especially challenging due to the nonlinear characteristic of the connected load. In order to ensure the feasibility of the concept on commonly utilized embedded processors, a relatively low computational complexity has to be maintained. The concept is able to meet the requirements for fast output dynamics and a low online computational burden by synthesizing a suitable nonlinear control law via a *flatness-based approach*. The controller performance was validated in high-fidelity simulations, and applicability was tested in real-time control-HIL (C-HIL) tests. Furthermore, an analytical stability analysis was carried out via computation of the *region of attraction* around all feasible operating points. This analysis also provides a sufficient condition that guarantees stability when transitioning between two operating points. However, the results of this analysis are only valid as long as no constraints are violated. Therefore, a *reference governor with an internal PT1-element* is employed that ensures constraints satisfaction. The novelty of the reference governor is that it implicitly includes a PT1 element, which results in a smoother trajectory generation and fewer current oscillations in the circuit.

During the multi-year-long research cooperation between AVL List GmbH and the Christian Doppler Laboratory for Innovative Control and Monitoring of Automotive Powertrain Systems, some of the most significant milestones of this work have already been published in scientific journals and presented at conferences. Additionally, a patent covering a constraint satisfaction approach via the presented reference governor has been filed. The following publications substantiate the scientific quality of this dissertation:

Journal Papers

The main difficulties in the development of highly dynamic controllers for DC-DC converters in battery emulators and a suitable flatness-based approach for controller synthesis were published in:

> [16] Michael Zauner, Philipp Mandl, Oliver König, Christoph Hametner and Stefan Jakubek. Flatness-Based Discrete-Time Control of a Battery Emulator Driving a Constant Power Load *IEEE Journal of Emerging and Selected Topics in Power Electronics*, Vol. 9 (2021), Issue 6, pages 6864-6874.

Results from the stability analysis of the proposed controller via computation of the region of attraction, as detailed in Chapter 4, were published in:

> [17] Michael Zauner, Philipp Mandl, Oliver König, Christoph Hametner and Stefan Jakubek. Stability Analysis of a Flatness-Based Controller Driving a Battery Emulator with Constant Power Load *at - Automatisierungstechnik*, Vol. 69 (2021), Issue 2, pages 142-154

The reference governor with an internal PT1-element for handling the system constraints, presented in Chapter 5, was submitted as:

> [18] Michael Zauner, Oliver König, Christoph Hametner and Stefan Jakubek. A Control Concept for Battery Emulators using a Reference Governor with a Variable PT1-element for Constraint Handling *IEEE Open Journal of Industry Applications*, submitted on 21st of April 2022

Conference Papers

The general idea for combining a nonlinear model description with its linearization via a flatness-based approach was first presented at the following (German-language) conference:

> [19] Michael Zauner, Oliver König, Christoph Hametner and Stefan Jakubek. Flachheitsbasierte diskrete Regelung eines Batterieemulators für Lasten mit konstanter Leistungsaufnahme *54. Regelungstechnisches Kolloquium 2020*, Boppard, Germany; 4.-6. March 2020

The separation of a DC-DC buck converter circuit into two coupled subsystems, as well as the advantages of using a piecewise-constant change in the converter stage current as the controlled variable, were presented at the following international conference:

> [20] Michael Zauner, Philipp Mandl, Oliver König, Christoph Hametner and Stefan Jakubek. Flatness based Control of DC-DC Converters with Constant Power Loads. *PCIM Europe digital days 2021* (held virtually); 3.-7. May 2021

Patents

The following patent, dealing with the developed reference governor concept for constraints satisfaction, presented in Chapter 5, was filed:

> Michael Zauner, Oliver König, and Christoph Hametner. *Verfahren zur Regelung eines technischen Systems.* Patent pending (ÖPA application number: A50277/2022)

Chapter 2

Battery Emulator Model

This work deals with a novel concept for the highly-dynamic control of DC converters with nonlinear loads. One of the most challenging applications for DC converters is in battery emulators on P-HIL testbeds, as there exist requirements for fast output voltage responses over a large operating region while handling substantial bidirectional power transfer. In order to demonstrate the capabilities of the developed control concept, it is exemplified with a battery emulator in a P-HIL testbed driving a nonlinear load in the shape of a CPL. Such a battery emulator usually consists of a controllable DC voltage source and a computer running a real-time-capable battery model. In the testbed, the battery emulator is connected to a UUT, where it provides the necessary power for the tests. With measurements of the current drawn by the UUT, the battery model calculates the appropriate voltage response based on the characterization of the physical battery being emulated. The controllable DC source then applies the computed voltage response to the input terminals of the UUT. With this setup, the UUT can be tested without having a physical battery present at the testbed, which increases safety (batteries are a fire hazard) while also eliminating the time-consuming pre-conditioning of the battery. For achieving accurate test results with a battery emulator, it is required that the battery model is sufficiently detailed and the DC source is tightly controlled. In order to emulate both the charging and discharging of a battery, the DC voltage source must be capable of bidirectional energy transfer. Therefore, a common choice for a DC source is a bidirectional multiphase DC-DC step-down converter, as they are highly efficient and able to handle large currents. The electrical circuit of such a DC converter connected to a UUT is depicted in Fig. 2.1. The multiphase buck converter is connected to an upstream DC link voltage V_{cc} and produces a downstream DC link voltage v_c. A cable (modeled as parasitic inductance L_2) connects the converter to the UUT, consisting of the capacitance C_2 and CPL. Note that the output voltage v_2 at the input terminals of the UUT is the controlled output of the battery emulator. As illustrated in Fig. 2.1, this circuit can be separated into two subsystems: the converter stage and the output stage. In the following sections, both subsystems are described in more detail, suitable mathematical models are derived, and the physical limitations of the system are shown.

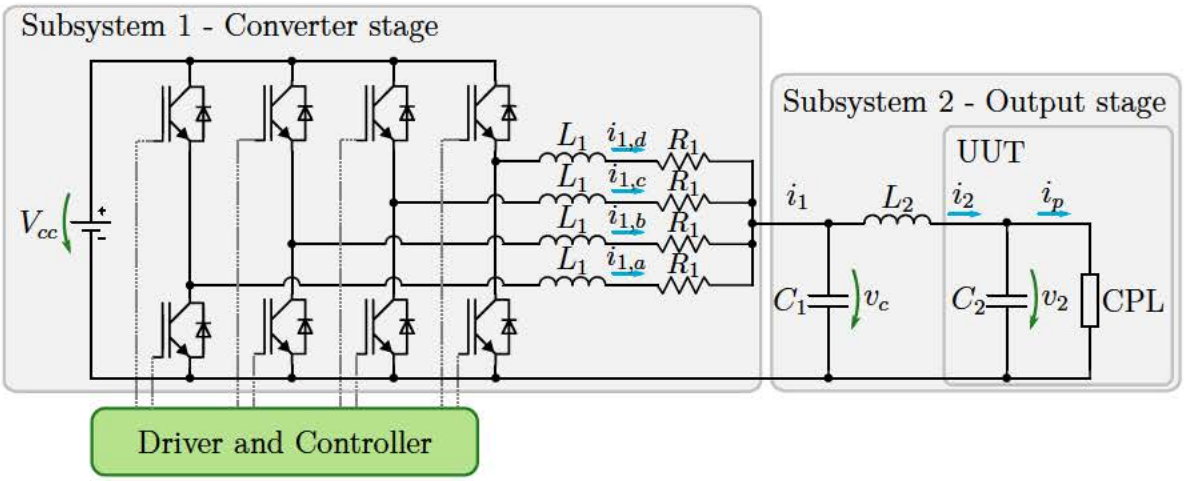

Figure 2.1: The electrical circuit diagram of a bidirectional multiphase DC-DC step-down converter driving a UUT.

2.1 Converter Stage

The converter stage contains four half-bridges with phase inductors L_1 connected in parallel. Each phase inductor is also modeled with a parasitic resistance R_1 in mind. There are two insulated-gate bipolar transistors (IGBTs) in every half-bridge which act as switches and either connect L_1 to V_{cc} or the ground. The dynamics of the upstream DC link voltage are assumed to be negligible, allowing it to be modeled as a constant voltage source. Similarly, the IGBTs are assumed to have sufficiently fast dynamics, along with an insignificant forward voltage drop, allowing them to be modeled as ideal switches. The main difficulty in modeling the converter stage is finding a suitable model that accurately captures the discontinuity caused by the binary switching characteristics.

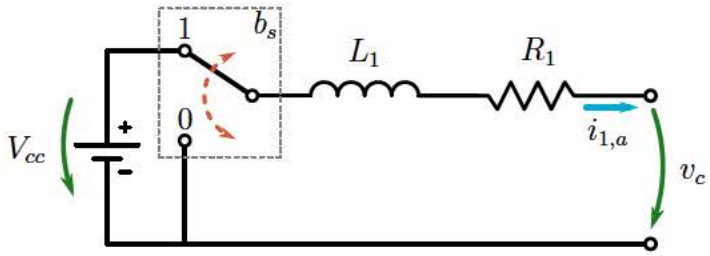

Figure 2.2: The equivalent circuit model for one phase in the converter stage.

As shown in Fig. 2.2, an equivalent circuit for one phase (exemplified by phase a) can be formed by combining both switches into one. The differential equation describing

the current $i_{1,a}$ is then given by

$$L_1 \frac{\mathrm{d}i_{1,a}(t)}{\mathrm{d}t} = V_{cc} b_s(t) - v_c(t) - R_1 i_{1,a}(t)\,, \tag{2.1}$$

where $b_s \in \{0, 1\}$ is a binary variable describing the switch state. The solution of this equation is given by

$$i_{1,a}(t) = e^{\frac{-R_1}{L_1}t} \left[\frac{1}{L_1} \int_0^t e^{\frac{R_1}{L_1}\tau} \left(V_{cc} b_s(\tau) - v_c(\tau) \right) \mathrm{d}\tau + i_{1,a}(0) \right] . \tag{2.2}$$

For short time periods t and small values of R_1, such that $\frac{R_1}{L_1} t \ll 1$ holds, the above equation can be simplified to

$$L_1 (i_{1,a}(t) - i_{1,a}(0)) = \int_0^t V_{cc} b_s(\tau) - v_c(\tau)) \,\mathrm{d}\tau\,. \tag{2.3}$$

Usually, the switches in the converter stage are driven by PWM signals. The total period of the PWM signal has a duration of $T_s = 1/f_{\mathrm{PWM}}$, where f_{PWM} is the frequency of the PWM carrier. The duty cycle of the signal is defined as $d_{\mathrm{PWM}} = t_{\mathrm{on}}/T_s$, $d_{\mathrm{PWM}} \in [0, 1]$, where t_{on} is the duration where $b_s = 1$. Choosing symmetrical PWM signals with triangular carriers reduces steady-state errors in conventional control schemes [21] and is beneficial for interleaving multiple phases. Note that in a symmetrical PWM signal, $b_s = 1$ for equal-length durations at the start and the end of a PWM period, see Fig. 2.3. Therefore, one can separate the integral in (2.3) into three parts:

$$L_1 (i_{1,a}(T_s) - i_{1,a}(0)) = \int_0^{t_1} V_{cc} - v_c(\tau)\,\mathrm{d}\tau + \int_{t_1}^{t_2} 0 - v_c(\tau)\,\mathrm{d}\tau + \int_{t_2}^{T_s} V_{cc} - v_c(\tau)\,\mathrm{d}\tau\,, \tag{2.4}$$

with $t_1 = t_{\mathrm{on}}/2$ and $t_2 = T_s - t_{\mathrm{on}}/2$. It is justified to assume that v_c is constant over T_s, as a low output voltage ripple is a design target of the filter given by L_1 and C_1. Consequently, (2.4) can be simplified into

$$L_1 (i_{1,a}(T_s) - i_{1,a}(0)) = V_{cc} t_{\mathrm{on}} - v_c T_s \tag{2.5}$$

or equivalently into

$$\frac{i_{1,a}(T_s) - i_{1,a}(0)}{T_s} = \frac{V_{cc} d_{\mathrm{PWM}} - v_c}{L_1} \tag{2.6}$$

From this equation, it is evident that there exists a direct relationship between the duty cycle d_{PWM} of the PWM signal and the discrete-time representation of $\frac{\mathrm{d}}{\mathrm{d}t} i_{1,a}$ with a sampling time of T_s. Furthermore, one can use the above equation to approximate the current waveform of $i_{1,a}$ over one PWM period. As shown in Fig. 2.3, a constant $\frac{\mathrm{d}}{\mathrm{d}t} i_{1,a,\mathrm{approx}}$ starting at $i_{1,a}(0)$ can be used to approximate the actual current $i_{1,a}$ over $\tau \in [0, T_s]$. Note that the integral of the error between the approximation and the exact waveform vanishes over τ. This approximation yields even better results if the

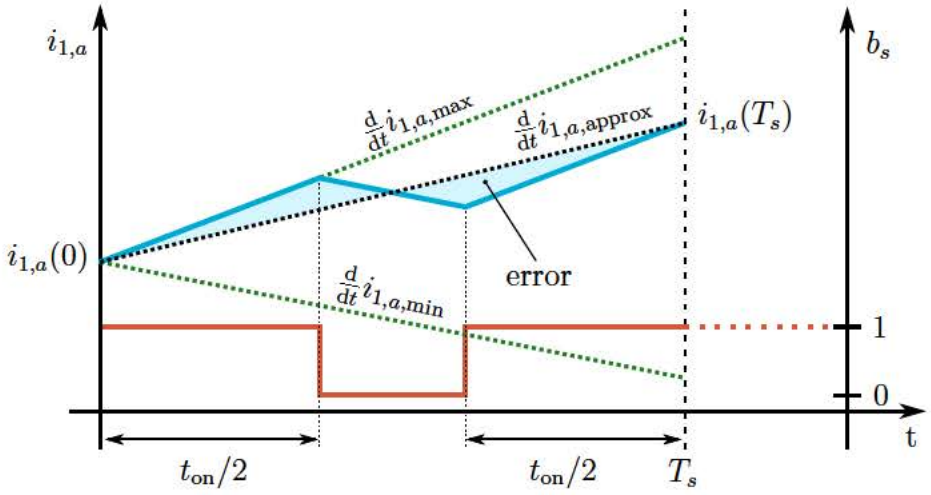

Figure 2.3: Output of the equivalent circuit model with a PWM signal (shown in red) driving the switch and the approximation given by $i_{1,a,\text{approx}}$. The shaded area highlights the difference between the approximation and the exact waveform. Note the minimal and maximal reachable currents for $i_{1,a}$ given by a duty cycle of 0 % and 100 % respectively (shown as green dotted lines).

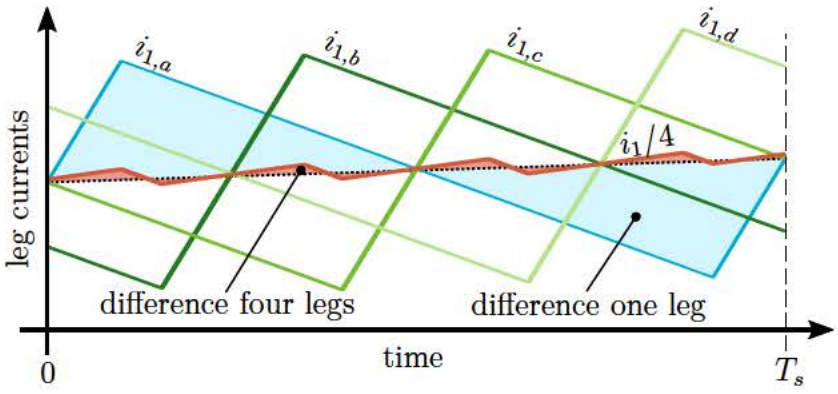

Figure 2.4: Difference between the approximation and the exact current waveform for one phase (blue shaded area) and four phases (red shaded area). Note that the sum $i_{1,a} + \cdots + i_{1,d} = i_1$ was scaled by 1/4.

sum of multiple interleaved phase currents is considered, as the absolute error decreases drastically compared to the case with just one phase, see Fig. 2.4 for a comparison. With (2.6), one can easily compute the required duty cycle necessary to achieve a desired constant change in current. Computing the duty cycle this way is especially practical, as the duty cycle can only be changed at the start of each PWM period and has to remain constant for the remainder of it. This restriction is due to technical limitations and to ensure signal integrity. Therefore, a convenient and reasonable approximation of the combined converter stage output current i_1 is given by

$$\frac{\mathrm{d}i_1}{\mathrm{d}t} = u\,, \tag{2.7}$$

where the value of u has to be constant over one PWM period. With the dynamics given by (2.7), a suitable model for the converter stage without any binary states for the switches is found. Comparing the right-hand sides of (2.6) and (2.7), one can see that there exists a direct relationship between u and the average duty cycle in the converter stage.

2.2 Output Stage

The output stage contains the filter capacitance C_1, a cable (modeled as parasitic inductance L_2), and the UUT, as shown in Fig. 2.1. In the presented setting, the UUT includes another capacitance C_2 and the CPL. An example of such an UUT would be a highly efficient inverter driving a motor or a power-electronics converter with a tightly-controlled output voltage, as both frequently draw constant power from their inputs [22]. While the instantaneous input impedance of such a CPL is positive, the incremental input impedance is negative [8], which causes stability issues on the DC bus feeding the CPL [9]. Note that the power draw $P = P(t)$ of the CPL can be time-varying. However, the value of P is assumed to change with sufficiently low frequency so that it can be modeled as constant over multiple PWM periods. Furthermore, it is also assumed that the power draw is independent of the output voltage v_2, although it is worth mentioning that the load current $i_p = \frac{P}{v_2}$ is nonlinear with respect to v_2. Finally, the input current i_1 of the output stage is the sum of all phase currents $i_{1,a} + \cdots + i_{1,d}$ of the converter stage. The following system of differential equations can be derived to describe the behavior of the output stage:

$$\begin{aligned}
\frac{\mathrm{d}v_2}{\mathrm{d}t} &= \frac{1}{C_2}(i_2 - i_p) = \frac{1}{C_2}\left(i_2 - \frac{P}{v_2}\right)\,,\\
\frac{\mathrm{d}i_2}{\mathrm{d}t} &= \frac{1}{L_2}(v_c - v_2)\,,\\
\frac{\mathrm{d}v_c}{\mathrm{d}t} &= \frac{1}{C_1}(i_1 - i_2)\,.
\end{aligned} \tag{2.8}$$

Due to the nonlinearity caused by the CPL, even if P is assumed to be constant, the analytical solution of (2.8) cannot be found. Therefore, the exact set of difference equations describing a discrete-time model of the output stage cannot be derived.

2.3 System Constraints

In order to ensure proper and safe operation of the battery emulator, it is necessary for the control concept to respect the physical limits of the system. Violation of the constraints given by the physical limits could lead to an unstable system or even damage the internal components of the battery emulator. The first set of constraints in the presented system is that the PWM signals in the converter stage can only have duty cycles between 0 % and 100 %, see Fig. 2.3. Violation of this constraint would lead to input saturation, which can cause stability issues in the system. Instead of considering this constraint for each phase individually, it is relaxed a bit by considering only the average duty cycle of all phases. This relaxation is justified as phase balancing (having similar averaged currents in all phases) is a secondary control goal of the underlying control scheme. Therefore, all duty cycles can be expected to be similar in value. Consequently, the restriction on the duty cycle is expressed via the following inequalities

$$\frac{-4v_c}{L_1} \leq u \leq \frac{4V_{cc} - 4v_c}{L_1}\,, \tag{2.9}$$

where u is defined in (2.7). Further constraints are given by the maximal ratings of the components being used. For example, the maximum current flowing through the switches in the converter stage has to be limited. If those limits are not satisfied at all times, component damage is imminent. Similar to before, this constraint is not formulated for each phase individually but rather for the entire converter stage as

$$-i_{1,\text{limit}} \leq i_1 \leq i_{1,\text{limit}}\,. \tag{2.10}$$

The next constraint is a result of the maximum measuring range of the current sensor for i_2 and is given by

$$-i_{2,\text{limit}} \leq i_2 \leq i_{2,\text{limit}}\,. \tag{2.11}$$

While violation of (2.9) is physically not possible, violation of (2.10) or (2.11) would trip the fail-safe in the device, resulting in an emergency shutdown to prevent component damage. Although the emergency shutdown protects the battery emulator from destruction, it still interrupts the test in progress. Therefore, the developed control concept should be able to reliably satisfy the constraints.

Chapter 3

Flatness-Based Control Concept

The performance specifications for a DC-DC converter used in a battery emulator differ from the typical specifications for most converters. For once the battery emulator's output voltage should be highly dynamic as it should follow the reference trajectory computed by a real-time capable battery model as fast as possible. This highly dynamic output is needed to accurately emulate a battery's almost instantaneous voltage response to sudden changes in load current. Furthermore, there are cost and space-saving incentives to use one battery emulator for various battery types with different output voltages. Consequently, the battery emulator should have a large operating region, covering different voltage and current ranges. Therefore, it is evident that the utilized control concept should allow for fast dynamics while also having a large viable operating region. Especially the large operating region is an unusual requirement for DC converters, as they are typically designed for a single stationary operating point [23]. One also has to keep in mind that the algorithms used in the control concept have to be real-time capable on the utilized embedded hardware. Therefore, additional requirements exist regarding computational complexity for the control concept. In this chapter, the challenges for designing a suitable control law are illustrated, and a flatness-based control concept is presented that is able to meet the requirements for fast output dynamics, a large operating range, and low computational effort. The presented concept was published in [16] and [17].

3.1 State of the Art

One of the most commonly used methods for controlling DC converters is PI control [24]. In the simplest implementation of this controller, the duty cycle values are directly computed based on the output voltage error. However, the characteristics of a nonlinear load, like a CPL, and the requirement for a large operating range make classical linear control methods (like PI control) unsuitable for the system [25]. Nevertheless, the widespread usage of linear control methods is explained by the fact that, usually, DC converters are used in a single operating point. One method to compensate for the

instability introduced by the CPL over a larger operating region is to insert passive elements into the circuit [26]. Alternatively, one could also use active damping [27], which uses a nonlinear control law to introduce virtual passive elements into the loop. Conceptually similar is a passivity-based control method [28], where stabilizing damping is assigned to the system. Another widespread control concept utilized in DC converters is feedback-linearization [22, 29, 30], where the original (nonlinear) system is transformed into a simpler (linear) form. A control law is then synthesized in this simpler form and transformed to make it applicable to the original system. DC converters are well suited for feedback-linearization as they are known to be flat systems [22]. Control concepts that have been successfully deployed to DC converters used in battery emulators are sliding mode control [23] and model predicive control (MPC) [31, 32]. While sliding mode control is well-known for its robust behavior over a large-signal range, it can lead to an unpredictable switching frequency in power converters which can lead to chattering issues [22]. On the other hand, MPC is based on an optimization problem, solved in a receding horizon fashion. Therefore, a (usually) quadratic optimization problem has to be solved at every time step. This leads to a rather significant online computational effort, which limits the practical implementation of the MPC.

3.2 Problem Description

Designing a suitable control law for the battery emulator capable of providing a highly dynamic output voltage over a large operating range is not a trivial task. By combining the equations describing the converter stage, see (2.7), and the output stage, see (2.8), the complete nonlinear system model for the battery emulator is derived as

$$\begin{aligned} \frac{\mathrm{d}v_2}{\mathrm{d}t} &= \frac{1}{C_2}\left(i_2 - \frac{P}{v_2}\right), \\ \frac{\mathrm{d}i_2}{\mathrm{d}t} &= \frac{1}{L_2}(v_c - v_2), \\ \frac{\mathrm{d}v_c}{\mathrm{d}t} &= \frac{1}{C_1}(i_1 - i_2), \\ \frac{\mathrm{d}i_1}{\mathrm{d}t} &= u, \end{aligned} \tag{3.1}$$

or equivalently with the state-vector $\boldsymbol{x} = [v_2, i_2, v_c, i_1]^T$ as the nonlinear state-space model given by

$$\sum_{nl}: \begin{cases} \dot{\boldsymbol{x}} = \boldsymbol{f}(\boldsymbol{x}, P) + \boldsymbol{g}u, & (3.2) \\ y = \boldsymbol{h}(\boldsymbol{x}) = v_2. & (3.3) \end{cases}$$

Recall that the input u must be held constant for the duration of one PWM period in order to use the approximation of the converter stage presented in Section 2.1. Such a piecewise constant input could be achieved via a discrete-time control law with a zero

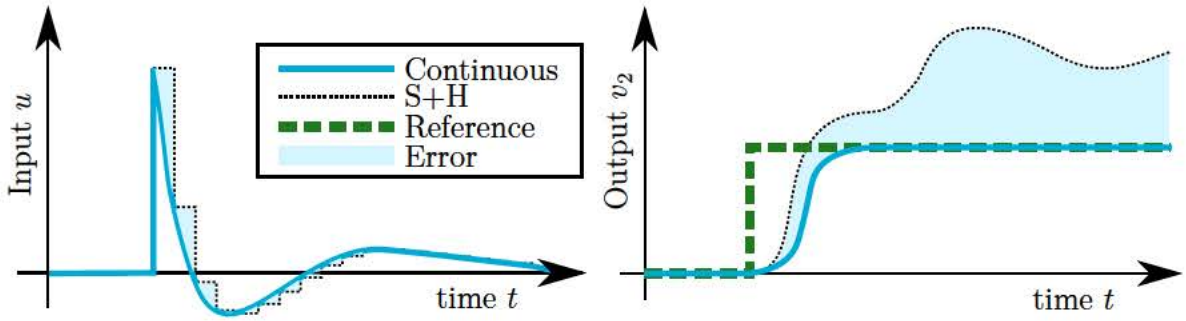

Figure 3.1: Left: The computed input of a continuous-time controller (solid line) and the applied input with a S+H element (dotted line). Right: The resulting outputs for a reference change; If the computed input was directly applied to the system (solid line) and the actual applied input (dotted line).

order hold (ZOH) element and a sampling time of $T_s = f_{\mathrm{PWM}}^{-1}$. However, synthesizing such a controller would also require a discrete-time model of the plant. Due to the nonlinearity introduced by the CPL, an exact discretization of Σ_{nl} with a ZOH element on the input is not possible. If only slow closed-loop dynamics are required, one could design a continuous-time controller and utilize a sample and hold (S+H) element to arrive at a piecewise constant input u. Such a continuous-time controller is only applicable if the computed input varies slowly over one period such that the difference caused by the applied S+H is neglectable. With faster dynamics, the difference between computed and applied input increases. This difference leads to error accumulation that can destabilize the system, as illustrated in Fig. 3.1. However, in order to achieve the most accurate testing results with the battery emulator, the fastest possible dynamics are desired. Consequently, a continuous-time controller with a S+H element is unsuitable for this setup. Therefore, a discrete-time representation of the nonlinear plant has to be found to synthesize a discrete-time controller. Commonly, this is achieved by applying an approximative discretization method. When choosing a suitable approximation method, one has to consider a trade-off between maximal step size, accuracy, and computational effort. Simple methods like forward Euler integration [30] provide easily computable and reasonable approximations for sufficiently small step sizes. However, for the given step size of T_s, its accuracy was unsatisfactory. More sophisticated methods, like classical Runge-Kutta [33], would be accurate enough, but they quickly exceed the allowable computational complexity. Another commonly used approach for arriving at a discrete-time representation of a nonlinear system is based on linearizing it around a stationary linearization point. The resulting linear system Σ_l, generally expressed as

$$\Sigma_l: \begin{cases} \dot{\boldsymbol{x}}_l = \boldsymbol{A}_l \boldsymbol{x}_l + \boldsymbol{B}_l u_l + \boldsymbol{E}_l P_l \,, & (3.4) \\ y_l = \boldsymbol{C}_l \boldsymbol{x}_l \,, & (3.5) \end{cases}$$

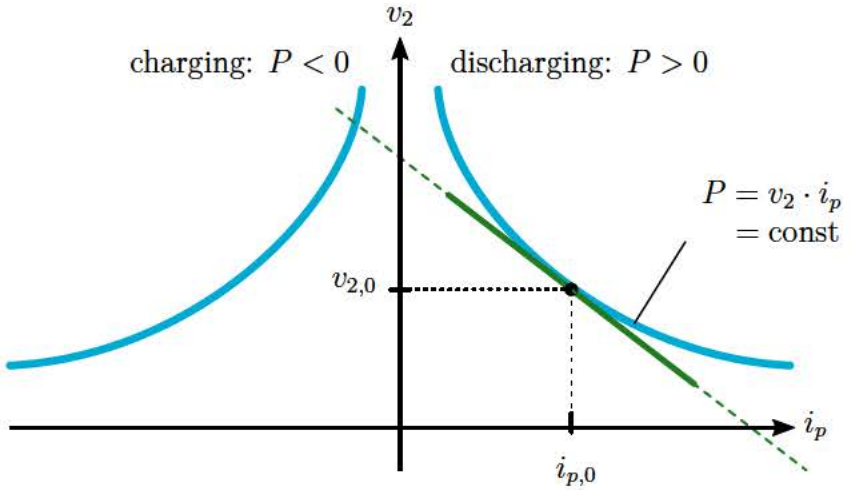

Figure 3.2: Nonlinear characteristics of the CPL (blue line) and linear approximation (green line) at the point $v_{2,0}$ and $i_{p,0} = P_0/v_{2,0}$.

where $\boldsymbol{x}_l$, u_l, and y_l are the deviations of $\boldsymbol{x}$, u, and y to the linearization point respectively. Σ_l can then be discretized exactly with a ZOH element on the input and used for controller synthesis. However, looking at the nonlinear characteristics of the CPL in Fig. 3.2, it is clear that this approach only produces accurate results in the vicinity of the linearization point. Since a large operating range is required, this linear approximation would quickly lead to errors and destabilize the system.

3.3 Establishing Feedback-Equivalence

The previous section introduced the nonlinear system Σ_{nl} and its linearization Σ_l. Both Σ_{nl} and Σ_l have their own set of advantages and disadvantages, which influence their usability for controller synthesis: On the one hand, Σ_{nl} captures the nonlinear characteristics of the CPL well, but it cannot be discretized exactly. On the other hand, Σ_l can be discretized exactly, although it is only accurate in the vicinity of the linearization point. It is assumed that a combination of Σ_{nl} and Σ_l could reduce their respective disadvantages while retaining most of their advantages. Based on this idea, a flatness-based control concept is proposed that establishes feedback equivalence [34] between Σ_{nl} and Σ_l. For that purpose, a diffeomorphism $\boldsymbol{\Phi} : \boldsymbol{x} \rightarrow \boldsymbol{x}_l$ is introduced alongside a nonlinear feedback law $u = \alpha(\boldsymbol{x}, P) + \beta(\boldsymbol{x})u_l$. The smooth functions $\boldsymbol{\Phi}$, α, and β map Σ_{nl} into Σ_l, thus establishing feedback-equivalence between them. Instead of deriving the required diffeomorphism directly, one can exploit the differential flatness property [35] of the system for a more systematic approach. It is well known that the combination of two diffeomorphisms result again in a diffeomorphism [36]. Therefore, one could combine two separate diffeomorphisms into a common system, e.g., mapping

Σ_{nl} into Σ_b and Σ_b into Σ_l, and join them together to find the mapping Σ_{nl} into Σ_l. As Σ_{nl} and Σ_l are both flat systems with a full relative degree (the flatness-properties are derived in Appendix A), a logical choice for the common system Σ_b would be a system in Brunovsky canonical form (BCF).

3.3.1 Mapping Σ_{nl} into Σ_b

In a first step, the mapping of Σ_{nl} into Σ_b is derived. If Σ_b is chosen to be in BCF, this can be carried out by writing down the transformation of Σ_{nl} into input-output normal form [35]. The so-called Lie derivatives are used for a more compact notation, e.g.,

$$L_f h(\boldsymbol{x}, P) := \frac{\partial h(\boldsymbol{x})}{\partial \boldsymbol{x}} \boldsymbol{f}(\boldsymbol{x}, P)\,. \tag{3.6}$$

With this, the output y and its time-derivatives of the nonlinear system Σ_{nl} can be written as

$$z_1 = y = h(\boldsymbol{x})\,, \tag{3.7}$$

$$z_2 = \dot{y} = \dot{z}_1 = L_f h(\boldsymbol{x}, P) + \underbrace{L_g h(\boldsymbol{x})}_{=0} u\,, \tag{3.8}$$

$$\vdots$$

$$z_4 = y^{(3)} = \dot{z}_3 = L_f^3 h(\boldsymbol{x}, P) + \underbrace{L_g L_f^2 h(\boldsymbol{x})}_{=0} u\,, \tag{3.9}$$

$$y^{(4)} = \dot{z}_4 = L_f^4 h(\boldsymbol{x}, P) + \underbrace{L_g L_f^3 h(\boldsymbol{x})}_{\neq 0} u\,. \tag{3.10}$$

With $\boldsymbol{z} = [z_1, z_2, z_3, z_4]^T$, one can collect (3.7)-(3.9) into

$$\boldsymbol{z} = \boldsymbol{t}(\boldsymbol{x}, P)\,, \tag{3.11}$$

where $\boldsymbol{t}(\cdot)$ is continuously differentiable and the inverse $\boldsymbol{x} = \boldsymbol{t}^{-1}(\boldsymbol{z}, P)$ exists. The resulting system dynamics in input-output normal form are given as

$$\Sigma_b\colon \begin{cases} \dot{\boldsymbol{z}} = \boldsymbol{A}_b \boldsymbol{z} + \boldsymbol{B}_b y^{(4)}\,, & (3.12) \\ y = \boldsymbol{C}_b \boldsymbol{z}\,, & (3.13) \end{cases}$$

where

$$\boldsymbol{A}_b = \begin{bmatrix} 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 \end{bmatrix}, \boldsymbol{B}_b = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 1 \end{bmatrix}, \boldsymbol{C}_b = \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \end{bmatrix}^T . \tag{3.14}$$

Evidently, Σ_b is in BCF, meaning that the diffeomorphism given by (3.11) transforms the nonlinear system dynamics into a simple chain of integrators, where the states are the system's output and its time-derivatives.

3.3.2 Mapping Σ_b into Σ_l

Similar to before, the mapping between Σ_b and Σ_l can be derived. Let the triplet $(\boldsymbol{x}_0, u_0, P_0)$ be a valid linearization point for Σ_{nl}, such that $\mathbf{0} = \boldsymbol{f}(\boldsymbol{x}_0, P_0) + \boldsymbol{g}u_0$ holds. The linear system Σ_l can then be written as

$$\Sigma_l\colon \begin{cases} \dot{\boldsymbol{x}}_{\boldsymbol{l}} = \boldsymbol{A}_l\boldsymbol{x}_l + \boldsymbol{B}_l u_l + \boldsymbol{E}_l P_l\,, & (3.15)\\ y_l = \boldsymbol{C}_l\boldsymbol{x}_l + y_0\,, & (3.16)\end{cases}$$

where $\boldsymbol{x}_l = (\boldsymbol{x} - \boldsymbol{x}_0)$, $u_l = (u - u_0)$, $P_l = (P - P_0)$, and $y_0 = \boldsymbol{h}(\boldsymbol{x}_0)$. Note that the output of Σ_{nl} in (3.3) and Σ_l in (3.16) are identical as $y_l = y$ holds. The transformation into input-output normal form can be again found by writing down the output y_l and its time-derivatives:

$$\begin{aligned}
z_{l,1} = y_l &= \boldsymbol{C}_l\boldsymbol{x}_l + y_0\,, && (3.17)\\
z_{l,2} = \dot{y}_l &= \boldsymbol{C}_l\boldsymbol{A}_l\boldsymbol{x}_l + \underbrace{\boldsymbol{C}_l\boldsymbol{E}_l}_{\neq 0} P_l + \underbrace{\boldsymbol{C}_l\boldsymbol{B}_l}_{=0} u_l\,, && (3.18)\\
&\vdots\\
z_{l,4} = y_l^{(3)} &= \boldsymbol{C}_l\boldsymbol{A}_l^3\boldsymbol{x}_l + \underbrace{\boldsymbol{C}_l\boldsymbol{A}_l^2\boldsymbol{E}_l}_{\neq 0} P_l + \underbrace{\boldsymbol{C}_l\boldsymbol{A}_l^2\boldsymbol{B}_l}_{=0} u_l\,, && (3.19)\\
y_l^{(4)} &= \boldsymbol{C}_l\boldsymbol{A}_l^4\boldsymbol{x}_l + \underbrace{\boldsymbol{C}_l\boldsymbol{A}_l^3\boldsymbol{E}_l}_{\neq 0} P_l + \underbrace{\boldsymbol{C}_l\boldsymbol{A}_l^3\boldsymbol{B}_l}_{\neq 0} u_l\,. && (3.20)
\end{aligned}$$

Similarly, with $\boldsymbol{z}_l = [z_{l,1}, z_{l,2}, z_{l,3}, z_{l,4}]^T$ the transformation into input-output normal form is given as

$$\boldsymbol{z}_l = \underbrace{\begin{bmatrix}\boldsymbol{C}_l\\ \boldsymbol{C}_l\boldsymbol{A}_l\\ \boldsymbol{C}_l\boldsymbol{A}_l^2\\ \boldsymbol{C}_l\boldsymbol{A}_l^3\end{bmatrix}}_{\boldsymbol{T}_x}\boldsymbol{x}_l + \underbrace{\begin{bmatrix}\mathbf{0}\\ \boldsymbol{C}_l\boldsymbol{E}_l\\ \boldsymbol{C}_l\boldsymbol{A}_l\boldsymbol{E}_l\\ \boldsymbol{C}_l\boldsymbol{A}_l^2\boldsymbol{E}_l\end{bmatrix}}_{\boldsymbol{T}_P} P_l + \underbrace{\begin{bmatrix}y_0\\ 0\\ 0\\ 0\end{bmatrix}}_{\boldsymbol{z}_{l,0}}, \tag{3.21}$$

where $\boldsymbol{T}_x$ is square with $\det(\boldsymbol{T}_x) \neq 0$. Consequently, the inverse

$$\boldsymbol{x}_l = \boldsymbol{T}_x^{-1}(\boldsymbol{z}_l - \boldsymbol{T}_P P_l - \boldsymbol{z}_{l,0}) \tag{3.22}$$

exists. The resulting system dynamics in input-output normal form are given as

$$\begin{aligned}
\dot{\boldsymbol{z}}_{\boldsymbol{l}} &= \boldsymbol{A}_b\boldsymbol{z}_l + \boldsymbol{B}_b y_l^{(4)}\,, && (3.23)\\
y_l &= \boldsymbol{C}_b\boldsymbol{z}_l\,, && (3.24)
\end{aligned}$$

where $\boldsymbol{A}_b$, $\boldsymbol{B}_b$, and $\boldsymbol{C}_b$ have already been defined in (3.14). Since $y_l = y$ holds, their time-derivatives are also identical, resulting in $\boldsymbol{z}_l = \boldsymbol{z}$ and $y_l^{(4)} = y^{(4)}$. Therefore, (3.23)-(3.24) is the same system as Σ_b in (3.12)-(3.13).

3.3.3 Mapping Σ_{nl} into Σ_l

In the previous two subsections, the mappings of Σ_{nl} into Σ_b and Σ_b into Σ_l have been derived. Combining (3.11) and (3.22), one can find the required diffeomorphism $\boldsymbol{\Phi} : \boldsymbol{x} \to \boldsymbol{x}_l$ to map Σ_{nl} directly into Σ_l as

$$\boldsymbol{x}_l = \underbrace{\boldsymbol{T}_x^{-1}(\boldsymbol{t}(\boldsymbol{x}, P) - \boldsymbol{T}_P P_l - \boldsymbol{z}_{l,0})}_{\boldsymbol{\Phi}(\boldsymbol{x},P)} . \tag{3.25}$$

A geometric interpretation of this diffeomorphism can also be given: The states $\boldsymbol{x}_l$ are chosen so that Σ_l has the same output trajectory (up to the 3rd time-derivative) as Σ_{nl} with the states $\boldsymbol{x}$. In order to fully establish feedback equivalence between Σ_{nl} and Σ_l, a nonlinear feedback law has to be derived. Combining (3.10) and (3.20), one can find the feedback law $u = \alpha(\boldsymbol{x}, P) + \beta(\boldsymbol{x})u_l$ as

$$u = \underbrace{\frac{\boldsymbol{C}_l \boldsymbol{A}_l^4 \boldsymbol{x}_l + \boldsymbol{C}_l \boldsymbol{A}_l^3 \boldsymbol{E}_l P_l - L_f^4 h(\boldsymbol{x}, P)}{L_g L_f^3 h(\boldsymbol{x})}}_{\alpha(\boldsymbol{x},P)} + \underbrace{\frac{\boldsymbol{C}_l \boldsymbol{A}_l^3 \boldsymbol{B}_l}{L_g L_f^3 h(\boldsymbol{x})}}_{\beta(\boldsymbol{x})} u_l . \tag{3.26}$$

Likewise, a geometric interpretation for this feedback law can also be given: The input u is chosen so that y of Σ_{nl} has the same 4th time-derivative as y_l of Σ_l with u_l. The first term $\alpha(\boldsymbol{x}, P)$ can be interpreted as a state-dependent nonlinear distortion term, while $\beta(\boldsymbol{x})$ is used as a scaling factor. In the presented system, the terms $L_g L_f^3 h(\boldsymbol{x})$ and $\boldsymbol{C}_l \boldsymbol{A}_l^3 \boldsymbol{B}_l$ are independent of $\boldsymbol{x}$ and equal ($L_g L_f^3 h(\boldsymbol{x}) = \boldsymbol{C}_l \boldsymbol{A}_l^3 \boldsymbol{B}_l = (C_1 C_2 L_2)^{-1}$). Therefore, $\beta(\boldsymbol{x})$ simplifies to $\beta = 1$.

3.4 Controller Design

The idea behind establishing feedback equivalence between Σ_{nl} and Σ_l is that it is hypothesized that if both systems have similar dynamics and follow the same trajectory, the required control inputs will be similar in shape. Consequently, the linear system Σ_l can be initialized with the trajectory of the nonlinear system Σ_{nl} at every time step and used to compute a stabilizing piecewise constant control input u_l^*. This input then determines the future trajectory of Σ_l. Finally, the control input u^* for Σ_{nl} can be found, such that it follows the same stable trajectory as Σ_l. If the hypothesis holds, the input u^* will be (almost) piecewise constant. The required steps for this control concept are illustrated in Fig. 3.3 and described in more detail below:
One can take measurements of the plant to determine the states $\boldsymbol{x}$ of Σ_{nl} and use (3.25) to find $\boldsymbol{x}_l$. By initializing Σ_l with $\boldsymbol{x}_l$, the linear system will have the same output trajectory as Σ_{nl} up to the 3rd time-derivative. Note that this trajectory is independent of the input u, as Σ_{nl} and Σ_l have a full relative degree. As Σ_l is a linear system, it can be discretized exactly and used to design a stabilizing discrete-time controller that

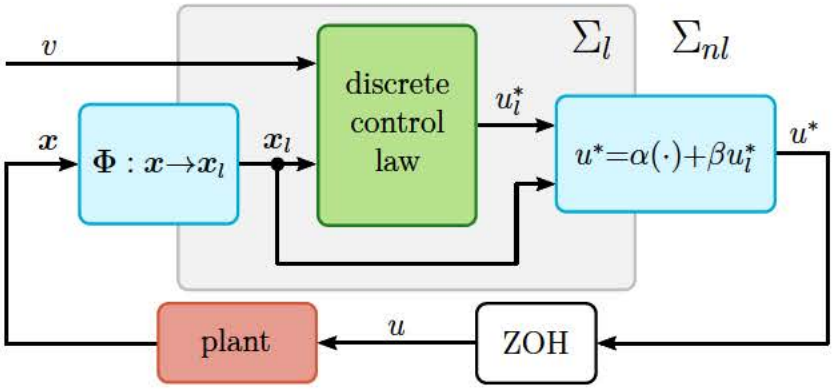

Figure 3.3: Overview of the proposed control concept with the reference voltage v. For ease of illustration, the influence of P is not shown.

computes a piecewise constant control input u_l^*. The combination of u_l^* and $\boldsymbol{x}_l$ specifies the trajectory of Σ_l up to the 4th time-derivative. One can now use (3.26) to fully establish feedback equivalence between Σ_l and Σ_{nl} by computing the control input u^* for Σ_{nl}. If this u^* is directly applied to Σ_{nl}, it will follow the same stabilizing trajectory as Σ_l. However, as α is state-dependent (and consequently time-dependent), the input u^* will no longer be exactly piecewise constant. Therefore, a ZOH element must be included to ensure a piecewise constant input u that can be applied to the plant.

3.4.1 Discrete-Time Control Law

The discrete-time system used for controller synthesis is found by discretizing Σ_l exactly with a ZOH on the input and a sampling time of T_s, yielding

$$\Sigma_d: \begin{cases} \boldsymbol{x}_l[k+1] = \boldsymbol{A}_d \boldsymbol{x}_l[k] + \boldsymbol{B}_d u_l[k] + \boldsymbol{E}_d P_l[k]\,, & (3.27) \\ y_l[k] = \boldsymbol{C}_d \boldsymbol{x}_l[k] + y_0\,, & (3.28) \end{cases}$$

where $\boldsymbol{x}_l[k]$ and $\boldsymbol{x}_l[k+1]$ are shorthand notations for $\boldsymbol{x}(kT_s)$ and $\boldsymbol{x}((k+1)T_s)$ with $k \in \mathbb{N}$ respectively, which also applies to other variables. While any linear controller synthesis method can be used for arriving at a control law that satisfies the dynamical requirements for a highly dynamic output voltage, the resulting control law is generally written as:

$$u_l^*[k] = -\boldsymbol{K}_x \boldsymbol{x}_l[k] + K_v v[k] + K_P P_l[k]\,, \tag{3.29}$$

where v is the reference output voltage and $\boldsymbol{K}_x$, K_v, and K_P are the state-feedback gain, the pre-filter gain, and the disturbance gain respectively. Examples of different synthesis methods that have been used in this framework are pole-placement design [20], linear quadratic regulator (LQR) [17], and exact feedback linearization [16]. The resulting nonlinear control law is found by inserting u_l^* into (3.26), resulting in

$$u^* = \alpha(\boldsymbol{x}, P) + \beta u_l^*\,. \tag{3.30}$$

Table 3.1: Nominal parameters of the model

Description	Notation	Value
DC-link voltage	V_{cc}	820 V
Resistance of each leg	R_1	0 mΩ/1 mΩ*
Inductance of each leg	L_1	300 µH
Inductance of the cable	L_2	25 µH
Capacitance of converter filter	C_1	425 µF
Capacitance of the UUT	C_2	2.3 mF
Maximum converter stage current	$i_{1,\text{limit}}$	±700 A
Steady state point for linearization	$\boldsymbol{x}_0$	$[410, 40, 410, 40]^T$
Input for linearization	u_0	0 A s^{-1}
Power draw for linearization	P_0	16.4 kW

*Nominal value for controller synthesis was 0 mΩ, while the value used for simulation was 1 mΩ.

However, as shown in Fig. 3.3, the applied control input u is actually given by

$$u[k] := u(\tau) = u^*(kT_s),\ \{\tau \in \mathbb{R}^+ \,|\, kT_s \leq \tau < (k{+}1)T_s\}\,, \tag{3.31}$$

as there exists a ZOH element to ensure a piecewise constant input.

3.5 Performance Analysis

This section aims to showcase the performance of the presented flatness-based control concept via numerical simulations. Furthermore, a comparison to other state-of-the-art control concepts is presented. More details and supplementary results can be found in [16], where, for example, the need for a discrete-time control concept is examined by illustrating the problems with a continuous-time controller implementation.

3.5.1 Simulation Setup

For accurate simulations, a high fidelity model of the battery emulator has been implemented in Simulink/Simscape, which includes the nonlinear characteristics of the IGBTs and equivalent series resistance components not shown in Fig. 2.1. The model has been validated with measurements from existing battery emulator devices. In order to ensure accurate test results with the battery emulator, there exists a dynamical requirement that the controller should achieve a closed-loop rise-time of 1 ms on the output if no constraints are violated. This requirement should be met in a large operating region, as the investigated battery emulator is designed to have a stable output

voltage between 48 V and 800 V for UUTs that behave like CPLs. For those kinds of UUTs, the converter is rated for a maximum continuous power draw of 250 kW. However, there also exists a constraint on the maximum current delivered by the output stage, limiting the allowable output power at lower voltages. Note that the constraint limiting the maximum output stage current is ignored in the presented results of this chapter, as it cannot be trivially satisfied. The leg inductances L_1 are chosen for a 10 % current ripple in each leg, while the capacitance C_1 was chosen for a resonance frequency well below the switching frequency. The parasitic resistance R_1 was neglected for controller synthesis; however, the simulations were carried out with the nominal value of 1 mΩ. Another parasitic component in the circuit is the self-inductance L_2 in the DC cables. The value of $L_2 = 25\,\mu\text{H}$ corresponds to the parasitic inductance of typical cable lengths in usual testbed layouts. An overview of the nominal parameter values for all simulations is given in Tab. 3.1. The PWM generators are simulated with the same properties and limitations as PWM generators found in the utilized digital signal processor (DSP). The duty cycles values of the PWM signals are computed according to (2.6) and applied to each half-bridge with an active-high complimentary signal with rising-edge delays and falling-edge delays to avoid short-circuits.

3.5.2 Comparison to other Concepts

In order to compare the performance of the presented flatness-based concept to other concepts, two state-of-the-art methods for arriving at a suitable discrete-time model for controller synthesis were also implemented. All the controllers are tuned to have the same closed-loop dynamics at the output.

Concept A: Forward Euler Integration

The first state-of-the-art concept uses an approximative method to directly arrive at a discrete-time model from the nonlinear description Σ_{nl}. While the forward Euler integration is the most fundamental explicit method for numerical integration, it is widely used due to its simplicity [33]. The resulting discrete-time model of Σ_{nl} with forward Euler integration is given by

$$\boldsymbol{x}[k+1] \approx \boldsymbol{x}[k] + T_s(\boldsymbol{f}(\boldsymbol{x}[k], P[k]) + \boldsymbol{g}u[k])\,. \tag{3.32}$$

This nonlinear model is then used for later controller synthesis.

Concept B: Linearization and Discretization

The second concept linearizes Σ_{nl} around a single linearization point, also resulting in Σ_l. This linear model is then discretized exactly with a ZOH on the input, yielding Σ_d, which is then used as a basis for controller synthesis. The difference to the proposed concept is that no feedback equivalence is established between Σ_{nl} and Σ_l. The states of

Table 3.2: Sampling times for the different simulation cases

Description	Notation	Value
Case I: Switching frequency	f_{PWM}	12 kHz
Case II: Switching frequency	f_{PWM}	8 kHz
Case III: Switching frequency	f_{PWM}	4 kHz

Σ_l are measured directly from the plant, and the control signal is also applied directly to it. Note that this concept represents a special case of the presented concept, where $\boldsymbol{\Phi} = \boldsymbol{x} - \boldsymbol{x}_0$, $\alpha = 0$, and $\beta = 1$.

3.5.3 Simulation Results

The proposed concept is compared to the two state-of-the-art concepts described previously in three simulation settings of increasing difficulty. While the reference voltage trajectory $v(t)$ and power draw $P(t) = P_0$ are the same for each simulation, the switching frequency f_{PWM} is reduced, which consequently increases the sampling time T_s. This increase in sampling time has the same effect on the discrete-time controller as increasing the dynamics of the plant while also increasing the desired closed-loop dynamics. The different switching frequencies for Cases I-III are given in Tab. 3.2.

Case I

In Case I, the switching frequency is set to 12 kHz, resulting in a sampling time of 83.33 µs. The results of this simulation are shown in Fig. 3.4: In the upper plot, the desired reference voltage v and the output voltages v_2 of each concept are shown. From this, one can see that all concepts manage to stabilize the plant. The first reference step at $t = 2$ ms is carried out in less than 1 ms, satisfying the requirement for a fast rise-time. However, during the larger second reference step at $t = 5$ ms, the rise-time is increased to 2 ms as the system encounters the current limit of the converter stage. This current limit constraint can be seen later in Fig. 3.9. In the lower plot of Fig. 3.4, the controlled variable u is shown. Notice that concept A is caught in a limit cycle as the input is oscillating. Concept B performs similarly to the proposed concept in terms of output voltage and input variable, with the only difference being at 100 V, where concept B has a steady-state error of 19 V. This error is caused by the nonlinearity of the CPL and the great distance to the linearization point at 410 V.

Case II

With Case II, the switching frequency is reduced to 8 kHz, resulting in a sampling time of 125 µs. From the simulation results given in Fig. 3.5, one can see that concept A can no longer track the desired reference value. However, both concept B and the proposed

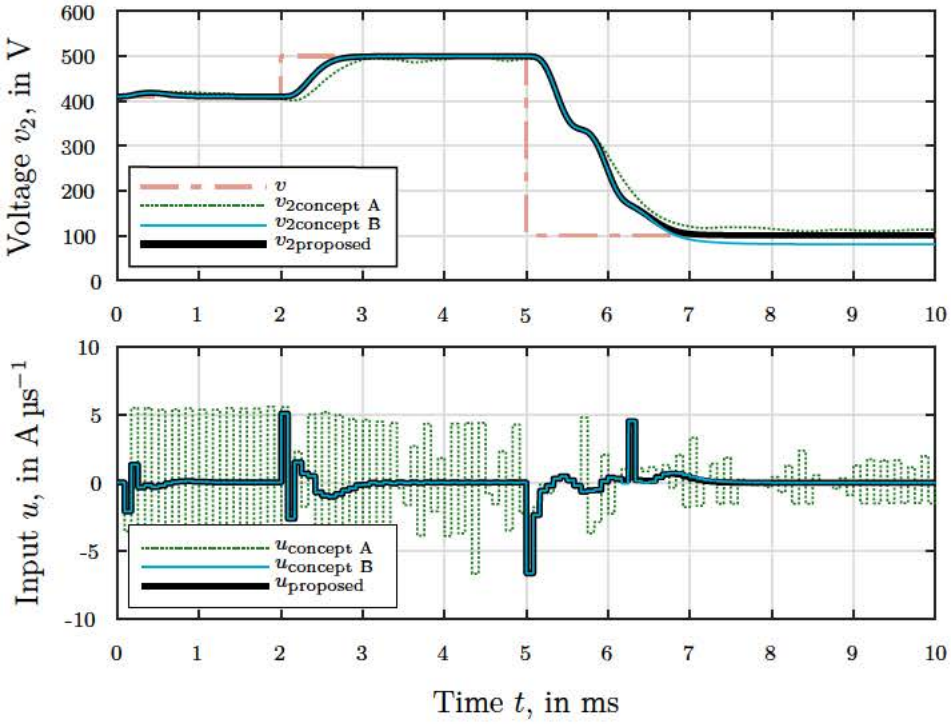

Figure 3.4: Case I: Switching frequency $f_{\text{PWM}} = T_s^{-1} = 12\,\text{kHz}$.

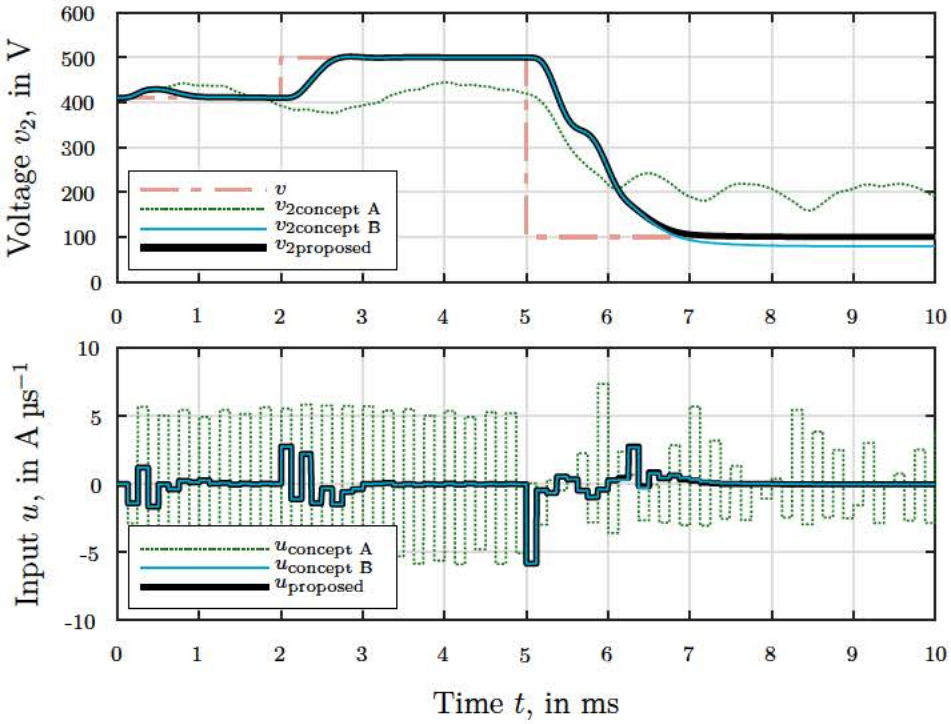

Figure 3.5: Case II: Switching frequency $f_{\text{PWM}} = T_s^{-1} = 8\,\text{kHz}$.

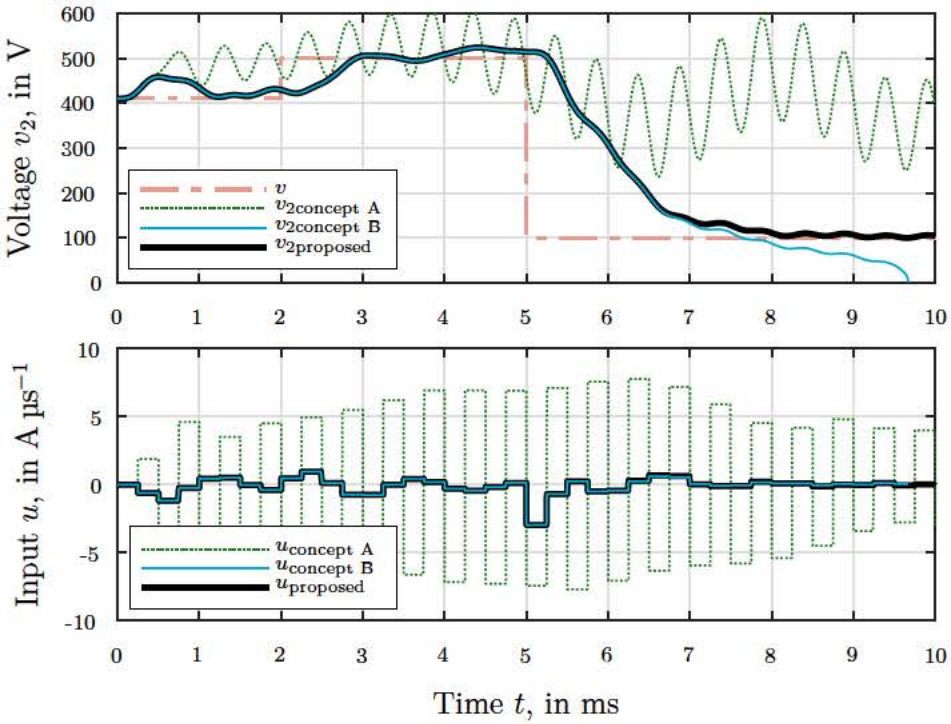

Figure 3.6: Case III: Switching frequency $f_{\text{PWM}} = T_s^{-1} = 4\,\text{kHz}$.

concept continue to perform up to the specifications. The only difference from the previous case is that concept B now has a more noticeable offset of 21 V at the lower voltage.

Case III

In Case III, the switching frequency is reduced to 4 kHz, increasing the sampling time to 250 µs. As seen in Fig. 3.6, concept A is caught in a limit cycle from the start. On the other hand, concept B remains similar in performance to the proposed concept if it is close to its linearization point. However, concept B can no longer stabilize the plant at lower voltages, as the nonlinear characteristic of the CPL causes an offset big enough to destabilize the system. Only the proposed concept remains stable throughout the investigated operating region.

3.6 HIL Experiments

In addition to the numerical simulation in Section 3.5, experiments were also conducted in a control-HIL (C-HIL) setup. In a C-HIL setup, the controller is implemented on a DSP and tested in real-time while the rest of the system is emulated. Moreover, high-

precision digital-to-analog converters (DACs) are used to drive the analog-to-digital converters (ADCs) of the DSP to achieve a realistic measurement noise.

3.6.1 HIL Setup

The controller is deployed to a prototype board intended to be used in a future generation of battery emulators. On this board, the utilized DSP is a Texas Instruments C2000, while a Typhoon HIL 602 [37] device is used to emulate the converter stage, the cable, and the UUT, see Fig. 3.7. The model of the converter stage was validated with measurement data from real systems. Further details on the model and its accuracy are given in [38] and [39].

Figure 3.7: The C-HIL test setup with a TYPHOON HIL 602 and a Texas Instruments C2000 DSP.

3.6.2 HIL Results

The converter stage was emulated with a switching frequency f_{PWM} of 12 kHz, resulting in a sampling time T_s of 83.33 µs. In order to be real-time capable, the controller has to compute the required duty cycles in less than 83.33 µs on the utilized DSP. As low computational complexity was one of the design criteria for the proposed concept, this capability is met. The reference voltage trajectory v and the power draw P are the same as in Section 3.5. Figure 3.8 shows the results captured on the C-HIL testbed. The measurements from channels 1, 2, and 3 show the voltage v_2, the current i_2, and the voltage v_c, respectively. As there exists no measurement device for the current i_1, the leg-current $i_{1,a}$ is displayed instead. The same results are also illustrated in Fig. 3.9, where they are compared to the simulation results of Case I. One can see the good agreement between numerical simulations and C-HIL results. The only noteworthy difference is a slight offset in output voltage at 100 V for the C-HIL results. This offset is caused by gain errors in sensor measurements, causing skewed ADC readings of $i_1 = i_{1,a} + \cdots + i_{1,d}$ and i_2, which results in a steady-state error of 2.6 V. Similar to the numerical results, the first reference step at $t = 2\,\mathrm{ms}$ has a rise-time of 1 ms,

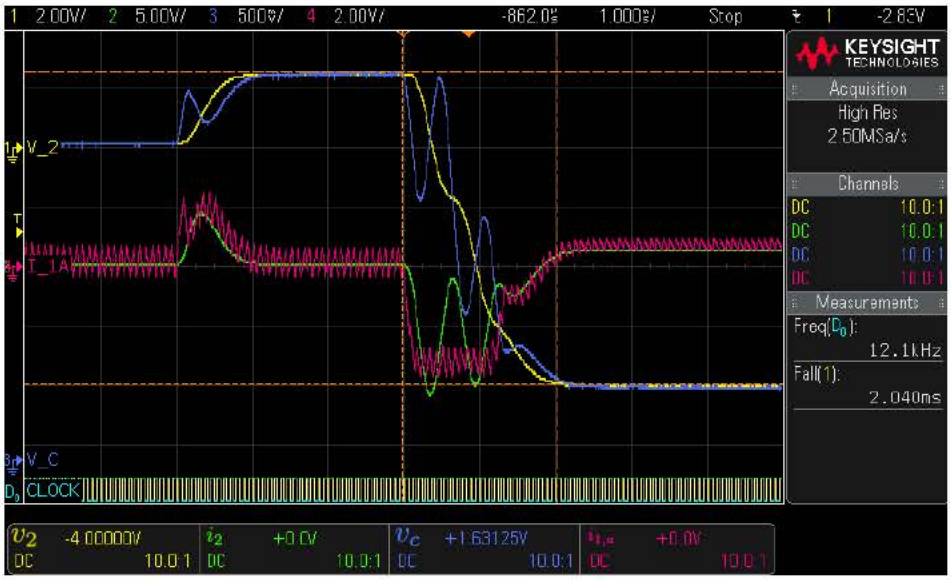

Figure 3.8: Proposed control concept on the C-HIL test bed with a switching frequency $f_{\mathrm{PWM}} = T_s^{-1} = 12\,\mathrm{kHz}$. Channel 1, 2, 3, shows the voltage v_2, the current i_2, and the voltage v_c respectively. Representative for all leg currents, the current $i_{1,a}$ is shown on channel 4.

satisfying the requirement for fast closed-loop dynamics. During the second reference step at $t = 5\,\mathrm{ms}$, a slower rise-time of 2.04 ms was achieved as the controller was limited by the maximum converter stage current of $\pm 700\,\mathrm{A}$. While this constraint was active, oscillations occurred on the voltage v_c and the current i_2. However, the controller suppressed those oscillations when the constraint was no longer active.

3.7 Aspects of the Flatness-Based Controller

This chapter proposes a flatness-based control concept for a bidirectional multiphase DC-DC converter driving a CPL. As the converter is used in a battery emulator for automotive testbeds, there are requirements to achieve fast closed-loop dynamics over a large operating range. A nonlinear control law satisfying those requirements is found by establishing feedback-equivalence between the nonlinear plant model and a linearized model. Numerical simulations show that compared to two other state-of-the-art concepts, the flatness-based concept is able to stabilize the plant at lower switching frequencies. The same simulations show that the proposed concept stabilizes the system over a wide voltage range. Providing a stable system output is especially challenging at lower voltages, where the nonlinearity of the CPL is more pronounced. In Chapter 4, the influence of the power draw and voltage setpoint on the stability is investigated in more detail via a stability analysis. Compared to MPC, another control concept used in bat-

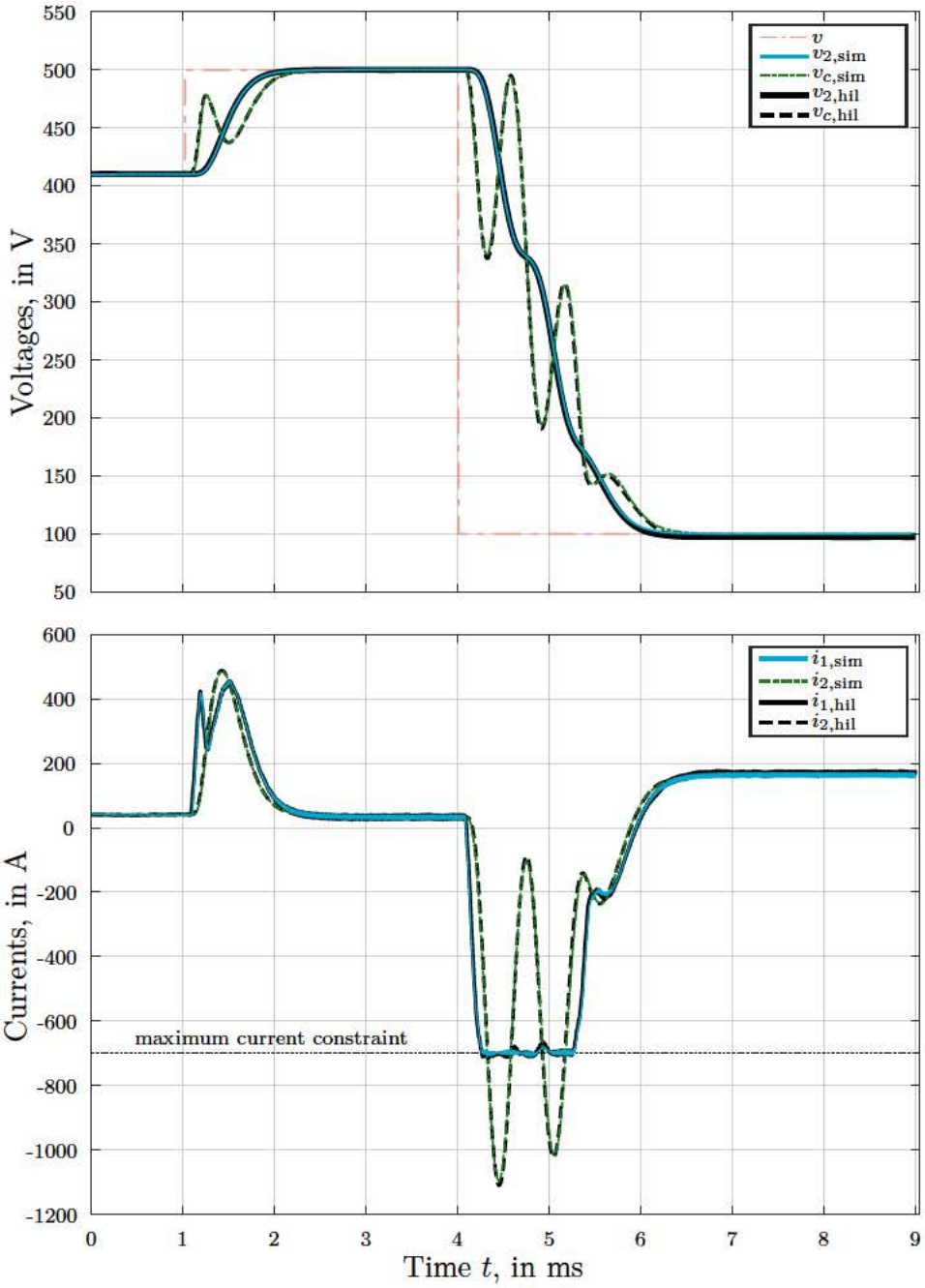

Figure 3.9: Comparison of the simulation and C-HIL results. The upper plot compares the simulated voltages $v_{2,\mathrm{sim}}$ and $v_{c,\mathrm{sim}}$ to the C-HIL voltages $v_{2,\mathrm{hil}}$ and $v_{c,\mathrm{hil}}$. In the lower plot the simulated currents $i_{2,\mathrm{sim}}$ and $i_{1,\mathrm{sim}}$ are compared to the C-HIL currents $i_{2,\mathrm{hil}}$ and $i_{1,\mathrm{hil}}$.

tery emulators, the closed-loop performance of the proposed concept is similar [7, 32]. Note that the online computational burden is significantly lower for the proposed concept, as no optimization problem has to be solved at each time step. Thanks to the low computational complexity of the concept, it was able to run on a C2000 DSP in real-time and tested in a C-HIL setup. However, in contrast to MPC, which can natively consider constraints and reliable meet them, the proposed concept requires additional algorithms to guarantee constraint satisfaction. An example of such an algorithm for the proposed concept is presented in Chapter 5.

Chapter 4

Stability Analysis

An essential contribution of this work is that the stability of the complete system has also been studied analytically. The proposed control concept introduced in Chapter 3 establishes feedback equivalence between a nonlinear system description Σ_{nl} and a linearized description Σ_l. The reason for establishing feedback equivalence between the two descriptions is that while Σ_{nl} describes the dynamics of the plant well over the entire operating range, it cannot be discretized exactly. On the other hand, Σ_l can be discretized exactly and, therefore, utilized for designing a highly dynamic discrete-time state-feedback controller. However, the dynamics of the plant can change significantly over the operating region and will only match the dynamics of Σ_l if close to the linearization point. By establishing feedback equivalence, a nonlinear control law is synthesized that is able to provide a highly dynamic output voltage while being applicable over a wider operating region. In order to investigate the extent where this controller is applicable, a stability analysis is carried out in this chapter.
The main reason for a (possibly) limited operating region is owed to the restriction that only piecewise constant control inputs can be applied to the plant. While the discrete-time control law for Σ_l computes an exactly piecewise-constant input u_l^*, it is generally no longer exactly piecewise constant after the transformation into u^* for Σ_{nl}. In order to still arrive at an applicable input u for Σ_{nl}, a ZOH element is added, which introduces additional dynamics into the system by distorting the input. In the following sections, the influence of this input distortion on the system states and the value of a Lyapunov function candidate are investigated. Furthermore, a sufficient criterion for stability is formulated by providing a lower bound estimation of the region of attraction (ROA). Finally, the estimation of the ROA is computed over the entire operating range and discussed. The presented results were also published in [17].

4.1 Input Distortion

This section aims to illustrate and quantify the influence of the input distortion on the system states caused by the ZOH element. In order to establish feedback equivalence

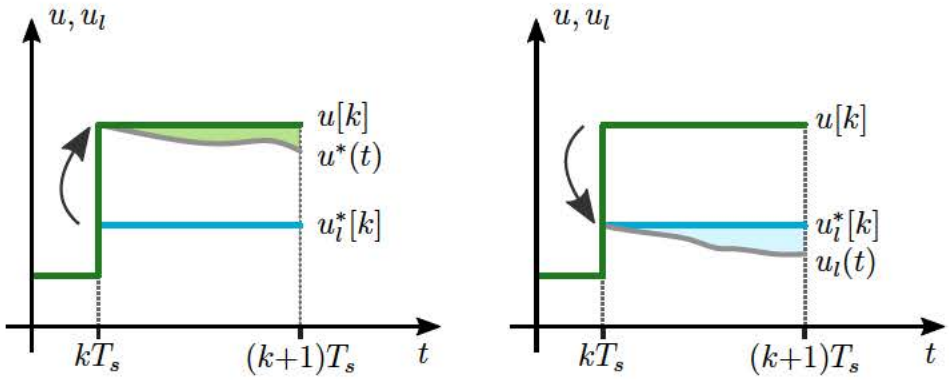

Figure 4.1: Influence of the ZOH element on the inputs of Σ_{nl} and Σ_l.
Left: The difference between $u^*(t)$ and the applied $u[k]$ for a given $u_l^*[k]$.
Right: The necessary distortion of the input $u_l(t)$ for a given $u[k]$ for both systems to remain feedback equivalent.

between Σ_{nl} and Σ_l, a diffeomorphism $\boldsymbol{x}_l = \boldsymbol{\Phi}(\boldsymbol{x}, P)$ was introduced alongside a nonlinear feedback law $u = \alpha(\boldsymbol{x}, P) + \beta u_l$. A discrete-time controller produces an exact piecewise-constant input $u_l^*[k]$ that is valid for Σ_l and only changes its value at times $t = kT_s$, $k \in \mathbb{N}$. However, after the transformation into

$$u^*(t) = \alpha(\boldsymbol{x}(t), P) + \beta u_l^*[k]\,, \tag{4.1}$$

the input is generally no longer constant over T_s, as α is state-dependent and, consequently, time-dependent. To still arrive at an exactly piecewise-constant input $u[k]$, which can be applied to the plant, a ZOH element is introduced, as seen in Fig. 3.3. This ZOH element samples the value of $u^*(t)$ every kT_s and outputs a constant value

$$u[k] := u(\tau) = u^*(kT_s),\ \{\tau \in \mathbb{R}^+ \,|\, kT_s \leq \tau < (k+1)T_s\}\,, \tag{4.2}$$

as seen on the left part of Fig. 4.1. The differences between $u[k]$ and $u^*(t)$ result in additionally introduced dynamics that can potentially destabilize the closed-loop system. For Σ_l to remain feedback equivalent to Σ_{nl} with $u[k]$ applied to its input, one has to introduce additional dynamics into Σ_l as well, as seen on the right part of Fig. 4.1. This can be done by adding a time-varying input distortion term $\delta u_l(t)$ to the input of Σ_l such that

$$u_l(t) = u_l^*[k] + \delta u_l(t)\,. \tag{4.3}$$

The relationship between an applied $u[k]$ and the $u_l(t)$ required to remain feedback equivalent is given by

$$u[k] = \alpha(\boldsymbol{x}(t), P) + \beta u_l(t)\,, \tag{4.4}$$

which can be solved with (4.3) for the distortion $\delta u_l(t)$, yielding

$$\delta u_l(t) = \frac{u[k] - \alpha(\boldsymbol{x}(t), P)}{\beta} - u_l^*[k]\,. \tag{4.5}$$

Furthermore, with the value of $u[k]$ found at time $t = kT_s$ given as

$$u[k] = \alpha(\boldsymbol{x}[k], P) + \beta u_l^*[k]\,, \tag{4.6}$$

one can simplify (4.5) into

$$\delta u_l(t) = \frac{\alpha(\boldsymbol{x}[k], P) - \alpha(\boldsymbol{x}(t), P)}{\beta}\,. \tag{4.7}$$

Obviously, $\delta u_l(t) = 0$ at every $t = kT_s$, as seen in Fig. 4.1. The input distortion δu_l influences the future trajectory of Σ_l. Without the input distortion, the states of Σ_l at the next time step would be given by

$$\boldsymbol{x}_l^*[k{+}1] = \boldsymbol{A}_d \boldsymbol{x}_l[k] + \boldsymbol{B}_d u_l^*[k] + \boldsymbol{E}_d P_l[k]\,, \tag{4.8}$$

where $\boldsymbol{A}_d$, $\boldsymbol{B}_d$, and $\boldsymbol{E}_d$ were introduced in (3.27). However, by including the input distortion, the states of Σ_l at the next time step are actually given by

$$\boldsymbol{x}_l[k{+}1] = \boldsymbol{A}_d \boldsymbol{x}_l[k] + \int_{\tau=kT_s}^{(k+1)T_s} \mathrm{e}^{\boldsymbol{A}_l((k+1)T_s-\tau)} \boldsymbol{B}_l u_l(\tau)\,\mathrm{d}\tau + \boldsymbol{E}_d P_l[k]\,. \tag{4.9}$$

With (4.3) inserted in the equation above, one arrives at

$$\boldsymbol{x}_l[k{+}1] = \underbrace{\boldsymbol{A}_d \boldsymbol{x}_l[k] + \boldsymbol{B}_d u_l^*[k] + \boldsymbol{E}_d P_l[k]}_{\boldsymbol{x}_l^*[k+1]} + \underbrace{\int_{\tau=kT_s}^{(k+1)T_s} \mathrm{e}^{\boldsymbol{A}_l((k+1)T_s-\tau)} \boldsymbol{B}_l \delta u_l(\tau)\,\mathrm{d}\tau}_{\boldsymbol{w}_l[k]}\,, \tag{4.10}$$

where $\boldsymbol{w}_l[k]$ is the resulting state distortion of Σ_l caused by the ZOH element. Looking at (4.10), it is evident that the closed-loop system will only follow the trajectory computed by the controller if $\boldsymbol{w}_l = 0$, which is generally not the case. Consequently, the influence of $\boldsymbol{w}_l$ can lead to stability issues.

4.2 Lyapunov Function Candidate

Finding a suitable Lyapunov function candidate is an essential step for analyzing the stability of the proposed concept. Although it was described in Section 3.4 that any linear controller synthesis method could be used for the proposed concept, the choice of an LQR is advantageous for further analysis. Therefore, the state-feedback gain $\boldsymbol{K}_x$ in (3.29) is chosen to minimize the quadratic cost function

$$J = \sum_{k=0}^{\infty} (\boldsymbol{x}_l[k] - \hat{\boldsymbol{x}}_l)^T \boldsymbol{Q} (\boldsymbol{x}_l[k] - \hat{\boldsymbol{x}}_l) + u_l^*[k]^T R u_l^*[k]\,, \tag{4.11}$$

where $\boldsymbol{Q} \succ 0$, and $R > 0$. The target state $\hat{\boldsymbol{x}}_l = \hat{\boldsymbol{x}}_l(v, P)$ in this cost function is dependent on the voltage reference v and the current power draw P via

$$\hat{\boldsymbol{x}}_l(v, P) = \{\hat{\boldsymbol{x}}_l : \hat{\boldsymbol{x}}_l = \boldsymbol{A}_d\hat{\boldsymbol{x}}_l + \boldsymbol{E}_d(P - P_0),\ v = \boldsymbol{C}_d\hat{\boldsymbol{x}}_l + y_0\}\ . \tag{4.12}$$

The state-feedback gain $\boldsymbol{K}_x$ of the LQR can then be expressed as

$$\boldsymbol{K}_x = (\boldsymbol{B}_d^T\boldsymbol{S}\boldsymbol{B}_d + R)^{-1}\boldsymbol{B}_d^T\boldsymbol{S}\boldsymbol{A}_d\,, \tag{4.13}$$

where $\boldsymbol{S} \succ 0$ is the solution of the associated discrete-time Ricatti equation

$$\boldsymbol{A}_d^T\boldsymbol{S}\boldsymbol{A}_d - \boldsymbol{S} - \boldsymbol{A}_d^T\boldsymbol{S}\boldsymbol{B}_d(\boldsymbol{B}_d^T\boldsymbol{S}\boldsymbol{B}_d + R)^{-1}\boldsymbol{B}_d^T\boldsymbol{S}\boldsymbol{A}_d + \boldsymbol{Q} = \boldsymbol{0}\,, \tag{4.14}$$

see, e.g., [40] for more details. One can now define a Lyapunov function for Σ_l as

$$V_l(\boldsymbol{x}_l) = \frac{1}{2}(\boldsymbol{x}_l - \hat{\boldsymbol{x}}_l)^T\boldsymbol{S}(\boldsymbol{x}_l - \hat{\boldsymbol{x}}_l)\,. \tag{4.15}$$

Furthermore, with the diffeomorphism $\boldsymbol{\Phi}$ one can find a nonlinear function

$$V(\boldsymbol{x}) = \frac{1}{2}(\boldsymbol{\Phi}(\boldsymbol{x}, P) - \hat{\boldsymbol{x}}_l)^T\boldsymbol{S}(\boldsymbol{\Phi}(\boldsymbol{x}, P) - \hat{\boldsymbol{x}}_l)\,, \tag{4.16}$$

which is continuously differentiable w.r.t. $\boldsymbol{x}$ with the properties $V(\boldsymbol{x}) > 0$, $\forall\, \boldsymbol{x} \neq \hat{\boldsymbol{x}}$ and $V(\hat{\boldsymbol{x}}) = 0$, where the target state $\hat{\boldsymbol{x}}$ for Σ_{nl} is defined as

$$\hat{\boldsymbol{x}}(v, P) = \{\hat{\boldsymbol{x}} : \boldsymbol{0} = \boldsymbol{f}(\hat{\boldsymbol{x}}, P),\ v = \boldsymbol{h}(\hat{\boldsymbol{x}})\}\ . \tag{4.17}$$

Therefore, V_l is also a valid Lyapunov function candidate for the nonlinear system Σ_{nl}.

4.3 Stability Criteria

After the state distortion $\boldsymbol{w}_l$ caused by the ZOH element has been derived and a suitable Lyapunov function candidate V_l has been found, the closed-loop stability of the proposed control concept can be investigated. In order to quantify the closed-loop stability, it is examined by means of Lyapunov's second method for stability [41]: A sufficient condition for stability on the subspace $\mathcal{D} \subset \mathbb{R}^4$ for a given target state $\hat{\boldsymbol{x}}_l$ is that $V_l(\hat{\boldsymbol{x}}_l) = 0$ holds and the Lyapunov function decreases over one sampling interval T_s, i.e.,

$$V_l(\boldsymbol{x}_l[k+1]) - V_l(\boldsymbol{x}_l[k]) < 0,\ \forall\, \boldsymbol{x}_l \in \mathcal{D} \setminus \hat{\boldsymbol{x}}_l\,. \tag{4.18}$$

If the state distortion was non-existent, the stable subset $\mathcal{D}$ would (theoretically) span the entirety of $\mathbb{R}^4$, as the LQR control law produces a negative definite Lyapunov function change everywhere, see Theorem 4.1

Theorem 4.1. *Given an undisturbed linear discrete-time system (e.g., Σ_d), the positive-definite solution $\boldsymbol{S}$ of the Riccati equation (shown in (4.14)), and a state-feedback gain $\boldsymbol{K}_x$ according to (4.13), then the closed-loop system with the control law $u_l^* = -\boldsymbol{K}_x \boldsymbol{x}_l$ is stable $\forall\, \boldsymbol{x}_l \in \mathbb{R}$.*

Proof. Without loss of generality, one can introduce the shifted state vector $\check{\boldsymbol{x}}_l = \boldsymbol{x}_l - \hat{\boldsymbol{x}}_l$, simplifying the Lyapunov function to

$$V_l(\check{\boldsymbol{x}}_l[k]) = \frac{1}{2}\|\check{\boldsymbol{x}}_l\|^2_{\boldsymbol{S}}\,, \tag{4.19}$$

where $\|\check{\boldsymbol{x}}_l\|^2_{\boldsymbol{S}}$ is a short-hand notation for $\check{\boldsymbol{x}}_l^T \boldsymbol{S} \check{\boldsymbol{x}}_l$. Furthermore, a power draw $P_l = 0$ is assumed for simplicity. The value of the Lyapunov function at the next time step $[k{+}1]$ is then given by

$$V_l(\check{\boldsymbol{x}}_l[k{+}1]) = \frac{1}{2}\|\boldsymbol{A}_d \check{\boldsymbol{x}}_l[k] + \boldsymbol{B}_d u_l^*[k]\|^2_{\boldsymbol{S}}\,. \tag{4.20}$$

The *nominal Lyapunov function change* is defined as

$$\Delta V_l^*[k] := V_l(\check{\boldsymbol{x}}_l[k{+}1]) - V_l(\check{\boldsymbol{x}}_l[k])\,. \tag{4.21}$$

With $u_l^* = -\boldsymbol{K}_x \check{\boldsymbol{x}}_l$ inserted in (4.21), one arrives at

$$\Delta V_l^*[k] = \frac{1}{2}\|(\boldsymbol{A}_d - \boldsymbol{B}_d \boldsymbol{K}_x)\check{\boldsymbol{x}}_l[k]\|^2_{\boldsymbol{S}} - \frac{1}{2}\|\check{\boldsymbol{x}}_l\|^2_{\boldsymbol{S}}\,, \tag{4.22}$$

which can be expanded into

$$\Delta V_l^*[k] = \frac{1}{2}\check{\boldsymbol{x}}_l[k]^T(\boldsymbol{A}_d^T \boldsymbol{S} \boldsymbol{A}_d - \boldsymbol{S} - \boldsymbol{A}_d^T \boldsymbol{S} \boldsymbol{B}_d \boldsymbol{K}_x - \boldsymbol{K}_x^T \boldsymbol{B}_d^T \boldsymbol{S} \boldsymbol{A}_d + \boldsymbol{K}_x^T \boldsymbol{B}_d^T \boldsymbol{S} \boldsymbol{B}_d \boldsymbol{K}_x)\check{\boldsymbol{x}}_l[k]\,. \tag{4.23}$$

Finally, with $\boldsymbol{K}_x$ according to (4.13) inserted into the Riccati equation, one can see that the first 3 terms of (4.23) can be simplified with (4.14) to $-\boldsymbol{Q}$. Furthermore, the last two terms can be rewritten into $-\boldsymbol{K}_x^T R \boldsymbol{K}_x$. Consequently, the nominal Lyapunov function change can be written as

$$\Delta V_l^*[k] = -\frac{1}{2}\check{\boldsymbol{x}}_l[k]^T(\boldsymbol{Q} + \boldsymbol{K}_x^T R \boldsymbol{K}_x)\check{\boldsymbol{x}}_l[k]\,, \tag{4.24}$$

which is negative definite. Therefore, the Lyapunov function decreases for any $\check{\boldsymbol{x}}_l \in \mathbb{R}$, resulting in a stable subset $\mathcal{D} \equiv \mathbb{R}^4$. □

Following the results of Theorem 4.1, one can see that the distortion-free state at the next time step $\boldsymbol{x}_l^*[k{+}1]$, introduced in (4.8), result in a Lyapunov function decrease:

$$V_l(\boldsymbol{x}_l^*[k{+}1]) - V_l(\boldsymbol{x}_l[k]) = \Delta V_l^*[k] < 0\,. \tag{4.25}$$

By inserting (4.25) into (4.18), one can rewrite the stability condition for a non-vanishing state distortion $\boldsymbol{w}_l \neq \mathbf{0}$, into

$$V_l(\boldsymbol{x}_l[k+1]) - V_l(\boldsymbol{x}_l^*[k+1]) + \Delta V_l^* < 0\,, \tag{4.26}$$

or by expanding it, a sufficient, but not necessary condition for stability is given as

$$\begin{aligned} &\underbrace{\frac{1}{2}(\boldsymbol{w}_l[k] + \boldsymbol{x}_l^*[k+1] - \hat{\boldsymbol{x}}_l)^T \boldsymbol{S}(\boldsymbol{w}_l[k] + \boldsymbol{x}_l^*[k+1] - \hat{\boldsymbol{x}}_l)}_{\geq 0} \\ &\underbrace{-\frac{1}{2}(\boldsymbol{x}_l^*[k+1] - \hat{\boldsymbol{x}}_l)^T \boldsymbol{S}(\boldsymbol{x}_l^*[k+1] - \hat{\boldsymbol{x}}_l)}_{<0} + \underbrace{\Delta V_l^* k}_{<0} < 0\,. \end{aligned} \tag{4.27}$$

While the latter two terms of the equation above are negative definite, the first term is positive semi-definite and can potentially cause stability issues. Recall that the value of $\boldsymbol{w}_l$ depends on the input distortion term δu_l caused by the ZOH element. If no input distortion acted on the system, $\boldsymbol{w}_l$ would be zero, and consequently, the first two terms would cancel each other out, leading to an unconditionally stable system. While (4.27) provides a condition for determining $\mathcal{D}$, which ensures stability in the current sampling interval, it does not guarantee that the system will remain within $\mathcal{D}$ in subsequent sampling intervals. Therefore, of more practical use in analyzing the stability of a controlled system is the positive invariant subset of $\mathcal{D}$ in which the controlled system will remain for all times. Determination of such a set is carried out in the next section.

4.4 Region of Attraction

The region of attraction (ROA) is defined as the region around a stable equilibrium point $\hat{\boldsymbol{x}}_l$ to which the system will return when perturbed [42]. Alternatively formulated, the ROA is the positive invariant subspace $\Omega \subset \mathcal{D}$ around $\hat{\boldsymbol{x}}_l$ in which all state trajectories will converge to $\hat{\boldsymbol{x}}_l$. From Lyapunov theory, one can arrive at a lower bound estimation of the ROA by computing a bounding surface c of V_l such that the entire state-space contained in $V_l < c$ is part of $\mathcal{D}$. The bounding surface can be found by solving the optimization problem

$$c = \min_{\boldsymbol{x}_l \notin \mathcal{D}} V_l(\boldsymbol{x}_l)\,, \tag{4.28}$$

which returns the minimum Lyapunov function value that is no longer in $\mathcal{D}$. If the system starts inside the bounding level surface c, its Lyapunov function value will decrease at the next time step. As the entire state-space inside the ROA is also part of $\mathcal{D}$, all subsequent time steps will decrease the Lyapunov function value. Consequently, the Lyapunov function V_l eventually converges to zero, and the state trajectory converges to the target state $\hat{\boldsymbol{x}}_l$. Practically speaking, the ROA also provides a condition for stability during the transition between two setpoints, provided the initial setpoint is contained inside the ROA of the final setpoint.

Table 4.1: Nominal parameters of the model

Description	Notation	Value
DC-link voltage	V_{cc}	820 V
Inductance of the cable	L_2	25 µH
Capacitance of converter filter	C_1	425 µF
Capacitance of the UUT	C_2	2.3 mF
Steady state point for linearization	$\boldsymbol{x}_0$	$[150, 333, 150, 333]^T$
Input for linearization	u_0	0 A s^{-1}
Power draw for linearization	P_0	50 kW
Sampling time	T_s	100 µs

4.5 Results

This section aims to illustrate the ROA of the flatness-based control concept introduced in Chapter 3. In addition, a practical application of the ROA is shown where it is used to ensure stability during the transition between two steady-state setpoints. Finally, the extent of ROA over all feasible stationary points is illustrated.

4.5.1 Setup

The following stability analysis is carried out with the nonlinear model Σ_{nl} and the parameters given in Table 4.1. According to the flatness-based control concept, a linear system Σ_l is computed by linearizing Σ_{nl} around a single linearization point, also found in Table 4.1. This linear system is then discretized with a sampling time $T_s = 100\,\mu s$ and used to derive a linear control law, where an LQR was used for synthesis. As shown in Section 3.3, the final nonlinear control law is found by establishing feedback-equivalence between Σ_{nl} and Σ_l. For simplicity, no constraints on the states or the input are considered.

4.5.2 Single ROA Example

In order to analyze the region around the linearization point, a lower-bound estimation of its ROA is computed. The main difficulty in investigating the ROA for the given system lies in visualizing the 4-dimensional space Ω. However, by finding the intersection of Ω with the plane containing all steady-state points given by reference voltage v and the power draw P, the ROA can be illustrated as shown in Fig. 4.2. Since Ω is a positive invariant set, the target state $\hat{\boldsymbol{x}}_l(150\,\text{V}, 50\,\text{kW})$ can be reached from any steady-state combination of output voltage and power draw located within the shaded area. Fig. 4.2 further illustrates the allowable voltage deviation Δv_2 of 25 V from the target state for a given constant power draw of 50 kW. Therefore, the system

can start from any steady-state point given by $\hat{\boldsymbol{x}}_l(\delta, 50\,\mathrm{kW})$ with $\delta \in [125\,\mathrm{V}, 175\,\mathrm{V}]$, and the system trajectories are guaranteed to converge to $\hat{\boldsymbol{x}}_l(150\,\mathrm{V}, 50\,\mathrm{kW})$. In order to demonstrate that all system trajectories starting within $\hat{\boldsymbol{x}}_l(\delta, 50\,\mathrm{kW})$ are stable, the output trajectories corresponding to the limits of δ are shown in Fig. 4.3.

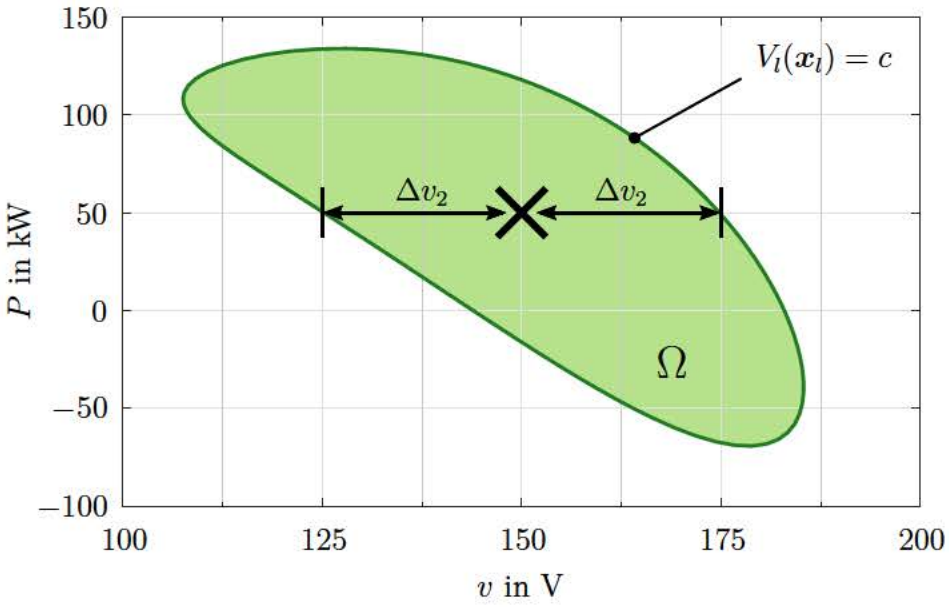

Figure 4.2: Intersection of the estimated ROA for the target point $\hat{\boldsymbol{x}}_l(150\,\mathrm{V}, 50\,\mathrm{kW})$ with the plane containing all steady-states. The cross marks the target point and Δv_2 illustrates the allowable voltage deviation for the given power draw.

4.5.3 ROA Estimation Over Entire Operating Range

While the previous section investigated the allowable voltage deviation Δv_2 for a single target state, one can define Δv_2 more generally as $\Delta v_2 = \Delta v_2(v, P)$ via

$$\begin{aligned} \Delta v_2(v, P) := \max_{\zeta \in \mathbb{R}^+} \ & \zeta\,, \\ \text{s.t.} \quad & \hat{\boldsymbol{x}}_l(\delta, P) \in \Omega,\ \forall\, \delta \in [v - \zeta, v + \zeta]\,. \end{aligned} \tag{4.29}$$

By computing the ROA over the entire operating range, the value of Δv_2 can be illustrated depending on v and P, as shown in Fig. 4.4. From these results, it is evident that the ROA increases with higher voltages. Contrary to this, the ROA decreases with a higher absolute power draw. Consequently, the corner cases with high power draw and low voltages have the smallest ROA, which was expected given the nature of the CPL. However, most of those corner cases are outside the technically feasible operating

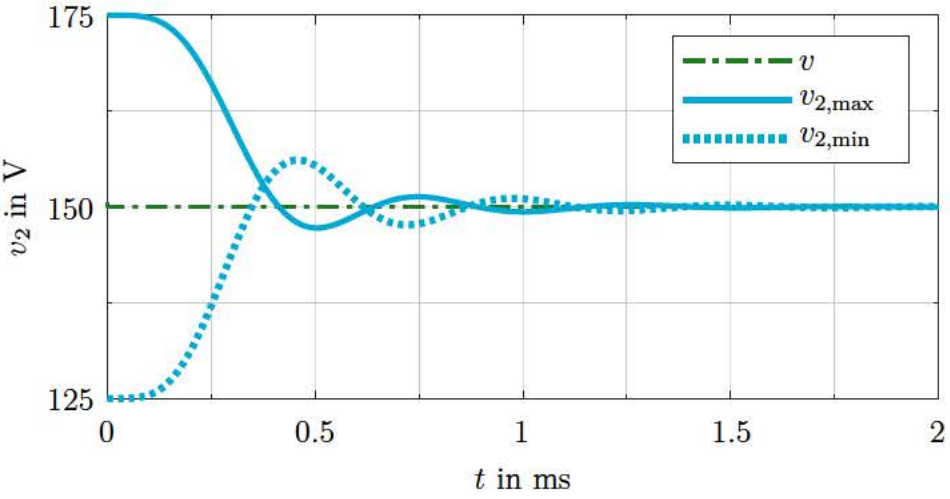

Figure 4.3: Trajectories of the output voltage v_2 converging to $v = 150\,\mathrm{V}$ at $P = 50\,\mathrm{kW}$ when starting inside the ROA shown in Fig. 4.2 with a starting voltage deviation of $v + \Delta v_2$ (shown as $v_{2,\max}$) and $v - \Delta v_2$ (shown as $v_{2,\min}$).

range, shown by the shaded area. For the power draw $P = 0$, the system Σ_{nl} becomes linear, which results in a rapidly increasing ROA. An example of a guaranteed stable output trajectory over a larger range is given in Fig. 4.5. There, multiple reference steps are carried out, where each step size was chosen according to the local value of Δv_2. The presented control concept stabilizes the system throughout the entire simulation while also providing consistently fast rise-times of 0.4 ms with a settling time of 1 ms. For comparison, the output of another control concept is also illustrated in Fig. 4.5. This other concept uses the same linear control law as the presented concept; however, it does not establish feedback equivalence between Σ_{nl} and Σ_l (for more details, see concept B in Section 3.5.2). Both concepts behave similarly in the vicinity of the linearization point at 150 V. If the system states move away from this linearization point, the linear controller introduces an offset that increases at some point enough to destabilize the system. As all values of Δv_2 in Fig. 4.4 are greater than 0, the proposed control concept can stabilize all technically feasible steady-state points. Therefore, the requirement for a large operating range for the battery emulator is met. Furthermore, the results in Fig. 4.5 also imply that every feasible steady-state point is also reachable from any other, as multiple smaller reference steps could be requested according to the local value of Δv_2.

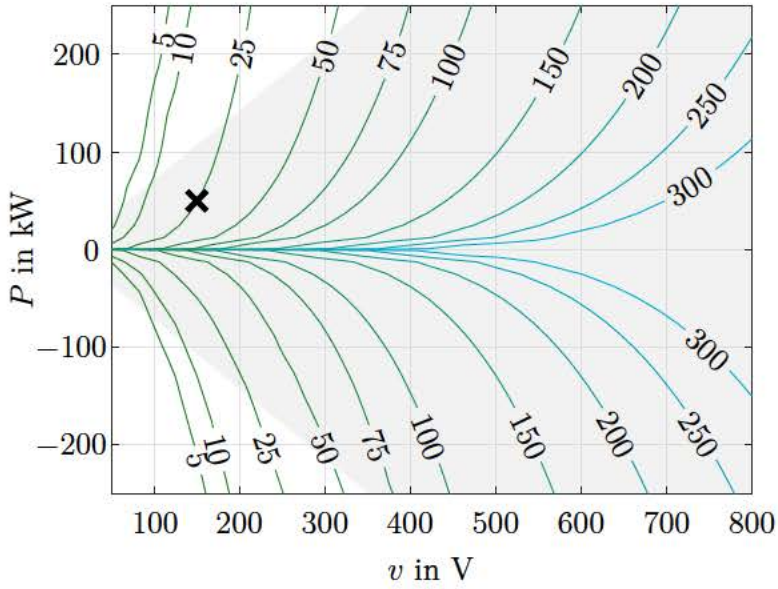

Figure 4.4: Allowable voltage deviation Δv_2 in V to stay inside the estimated ROA. The technically feasible operating range is highlighted. The cross marks the target point shown in Fig. 4.2.

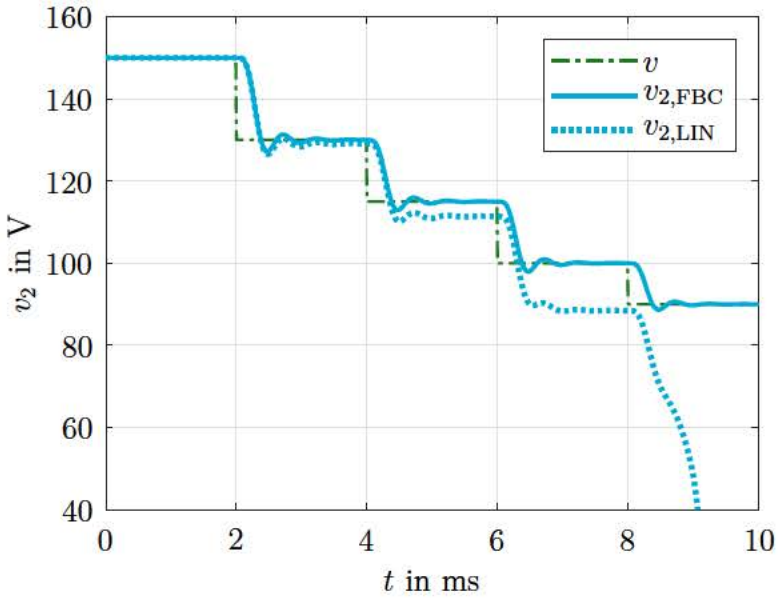

Figure 4.5: Comparison of the output trajectories for the flatness-based control concept (shown as $v_{2,\mathrm{FBC}}$) and a linear controller (shown as $v_{2,\mathrm{LIN}}$) when following a reference trajectory (shown as v) at $P = 50\,\mathrm{kW}$.

4.6 Summary

This chapter investigates the stability of the proposed flatness-based control concept. The main source of potential stability issues lies in the input distortion and subsequent state distortion caused by the included ZOH element, which is required to arrive at a piecewise-constant input. In order to quantify the influence of the ZOH element, a suitable Lyapunov function candidate was found and used to describe a stable region around a given target point. Furthermore, a positive invariant subset of this stable region was examined and used as a lower bound estimation of the ROA. The presented results show an example of such an estimate of the ROA for a given target state. It is also illustrated that there exists an allowable voltage deviation from the target state in which stability is still guaranteed. By investigating this allowable voltage deviation over the entire technically feasible operating range, it is demonstrated that the control concept meets the requirement for a large operating range. The investigated ROA also provides a condition to guarantee stability during the transition between two target states, which was also illustrated. However, the stability analysis carried out in this chapter does not consider system constraints. Therefore, it only applies to state-space regions where no constraints are violated. It is worth mentioning that even if two target states are feasible (i.e., no constraints are violated), the transition between those states is not guaranteed to be feasible, as the controller could steer the state-trajectory into regions where constraints would be violated. In order to ensure that the controller stays away from those regions, an additional algorithm can be introduced, as shown in Chapter 5, which guarantees a stable overall system.

Chapter 5

Constraints Handling

In the previous chapters a control concept for a battery emulator was motivated and investigated. It has been shown that the proposed concept achieves the required highly dynamic output voltage while also being able to stabilize the system over a large operating region. However, before implementing the concept on physical hardware, it is necessary to ensure that safety-critical constraints are satisfied at any time during operation. As with every physical system, the DC-DC converter in the battery emulator is subject to constraints due to physical limits [43]. If those constraints are not satisfied at all times, component damage is imminent. While a stability analysis was performed for the control scheme in Chapter 4, the influence of constraints on stability was not investigated. Consequently, the results are only applicable if no constraint violation occurs. However, the utilized controller does not guarantee that the constraints are satisfied. Therefore, a novel reference governor with PT1-element (PT1-RG) is proposed in this chapter to add constraint handling capabilities to the control concept. By including a PT1-element (also known as a first-order lag element) in this novel scheme, a smooth and safe transition between setpoints can be achieved by avoiding regions where constraints would be violated. Additionally, the PT1-RG reduces oscillations during the setpoint change compared to a traditional approach without the PT1-element. The contents of this chapter are widely based on the material submitted for publication in [18].

5.1 State of the Art

A well-known method for constraint handling is limiting the input action. The underlying control scheme in this method is generally not designed with this input saturation in mind, which can lead to stability issues or integrator windup phenomena [43]. Furthermore, this method cannot be easily expanded to enforce constraints on the states. On the other hand, a control scheme designed with the constraints in mind is model predicive control (MPC). In an MPC scheme, future input trajectories are computed by solving a constraint optimization problem at each time step. However, solving such

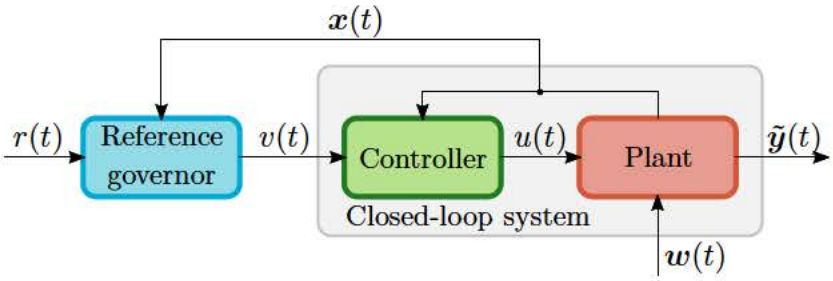

Figure 5.1: Principle of a reference governor applied to a closed-loop system. The external reference r is modified, resulting in the internal reference v, such that the constraints are met, i.e., $\tilde{\boldsymbol{y}} \in \mathcal{Y}$.

an optimization problem is computationally expensive. This is particularly problematic in systems where high sampling frequencies are desired, such as in the presented battery emulator [32]. Considering that future power electronics converters will have even higher switching frequencies (and consequently sampling frequencies), it becomes clear that even modern processors will be pushed to their limits. Another method is modifying the reference variable for the controller to avoid steering the closed-loop system into constraint regions. As seen in Fig. 5.1, this so-called reference governor (RG) is an add-on to an existing control concept and can be used to satisfy pointwise-in-time state and control constraints [44]. Partially contributing to its success, an RG has attractive properties like recursive feasibility and finite-time convergence while also having manageable online computational requirements [45]. Multiple modifications to the original RG introduced by [46] have been proposed throughout the years. The reader is encouraged to check out [44] for an excellent overview of different RG schemes. RGs have been applied (in their original and modified forms) in numerous fields like automotive applications [47], battery management [48], or DC-DC converters [49].

5.2 Problem Description

Until now, the constraints in the battery emulator have not received a lot of attention. However, it is safety-critical to satisfy them during operation. As introduced in Section 2.3, there exist constraints on the maximum converter stage current i_1, the maximum UUT current i_2, and the duty cycle of the PWM signal. As those constraints are linear in $\boldsymbol{x}$ and u, one can extend the nonlinear state-space system Σ_{nl} into

$$\Sigma_{nl}: \begin{cases} \dot{\boldsymbol{x}} = \boldsymbol{f}(\boldsymbol{x}, P) + \boldsymbol{g}u\,, & (5.1) \\ y = \boldsymbol{h}(\boldsymbol{x})\,, & (5.2) \\ \tilde{\boldsymbol{y}} = \tilde{\boldsymbol{C}}\boldsymbol{x} + \tilde{\boldsymbol{D}}u\,, \quad \tilde{\boldsymbol{y}} \in \mathcal{Y} & (5.3) \end{cases}$$

where the added line on the bottom describes a so-called constrained output. All constraints are satisfied if the constraint output $\tilde{\boldsymbol{y}}$ lies in the compact convex set $\mathcal{Y}$.

After applying the diffeomorphism $\boldsymbol{\Phi} : \boldsymbol{x} \rightarrow \boldsymbol{x}_l$, such that the nonlinear dynamics of Σ_{nl} are rendered linear, the extended linear system Σ_l is given by

$$\sum_l: \begin{cases} \dot{\boldsymbol{x}}_{\boldsymbol{l}} = \boldsymbol{A}_l \boldsymbol{x}_l + \boldsymbol{B}_l u_l + \boldsymbol{E}_l P_l \,, & (5.4) \\ y_l = \boldsymbol{C}_l \boldsymbol{x}_l + y_0 \,, & (5.5) \\ \tilde{\boldsymbol{y}} = \tilde{\boldsymbol{h}}_l(\boldsymbol{x}_l, u_l, P_l) \quad \tilde{\boldsymbol{y}} \in \mathcal{Y} \,. & (5.6) \end{cases}$$

After this transformation, the linear description of the constraints (5.3) become nonlinear in (5.6). By discretizing Σ_l and synthesizing a linear discrete-time control law, as shown in Section 3.4, the closed-loop system Σ_{cl} can be written as

$$\sum_{cl}: \begin{cases} \boldsymbol{x}_l[k{+}1] = \boldsymbol{A}_{cl} \boldsymbol{x}_l[k] + \boldsymbol{B}_{cl} v[k] + \boldsymbol{E}_{cl} P_l[k] + \boldsymbol{w}_l[k] \,, & (5.7) \\ y_l[k] = \boldsymbol{C}_{cl} \boldsymbol{x}_l[k] + y_0 \,, & (5.8) \\ \tilde{\boldsymbol{y}}[k] = \tilde{\boldsymbol{h}}(\boldsymbol{x}_l[k], v[k], P_l[k]) \quad \tilde{\boldsymbol{y}} \in \mathcal{Y} \,, & (5.9) \end{cases}$$

where v is the internal reference voltage and $\boldsymbol{w}_l$ is the state distortion caused by the ZOH element as described in Section 4.1. A similar case of input disturbance was investigated in [43], where a safety margin for constraint satisfaction was computed. For simplicity, in the presented case it is assumed that $\boldsymbol{w}_l[k] \in \mathcal{W} \,, \forall k \in \mathbb{Z}^+$, with the compact convex set $\mathcal{W} \subset \mathbb{R}^4$ containing the origin $\mathbf{0} \in \mathcal{W}$. Furthermore, the following assumptions are also considered:

Assumption 5.1. *The unconstrained ($\tilde{\boldsymbol{y}} \in \mathcal{Y}$), disturbance-free ($\boldsymbol{w}_l = 0$), closed-loop system Σ_{cl} is asymptotically stable, i.e., all eigenvalues of $\boldsymbol{A}_{cl}$ are strictly inside the unit circle.*

Assumption 5.2. *For $\lim_{k\to\infty}$ the closed-loop system output $y_l[k] \equiv v[k]$ for any $P[k]$, if $\tilde{\boldsymbol{y}}[k] \in \mathcal{Y}$.*

Remark 5.1. *While assumption 5.1 only guarantees stability for the disturbance-free case, stability can also be shown for the system with the disturbance $\boldsymbol{w}_l$ given by* (4.10)*, see the results of Chapter 4.*

Assumptions 5.1-5.2 are reasonable for controlled closed-loop systems in regions where the constraints $\tilde{\boldsymbol{y}} \in \mathcal{Y}$ are easily satisfied. However, the controller does not ensure that the closed-loop system will always stay in those regions. Especially during setpoint changes, the controller can lead to trajectories where $\tilde{\boldsymbol{y}} \notin \mathcal{Y}$. In order to ensure that the system will only be operated in regions where $\tilde{\boldsymbol{y}} \in \mathcal{Y}$, a RG scheme is proposed.

5.3 PT1 Reference Governor

In order to handle constraints in the shape of $\tilde{\boldsymbol{y}} \in \mathcal{Y}$ in the discrete-time closed-loop system Σ_{cl}, an RG scheme was added to the control concept as seen in Fig. 5.2. The

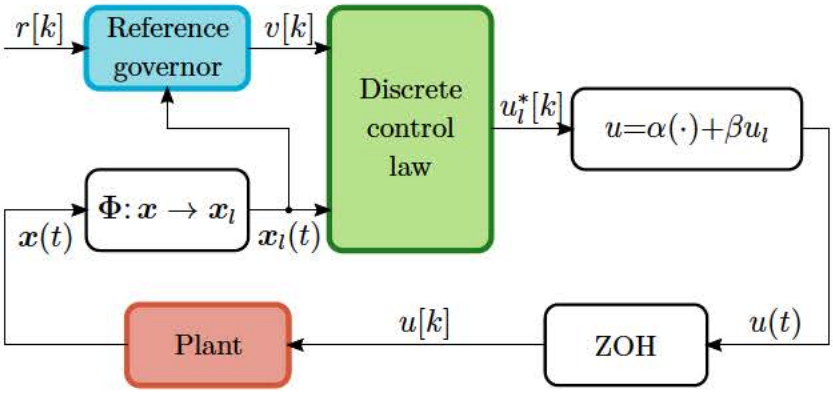

Figure 5.2: Overview of the flatness-based control concept with a reference governor. For ease of illustration, the influence of P is not shown.

basic idea of an RG is to low-pass filter the external reference r, creating the internal reference v, which ensures constraints satisfaction in the closed-loop. The low-pass filter is realized in the presented RG scheme as a variable PT1-element, also known as first-order lag element, with a fixed static gain of 1. By changing the time constant of the PT1-element, the time evolution of the internal reference v can be modified. With the inclusion of the PT1-element the RG achieves a smoother transition between setpoints in the presented setting. A discrete-time PT1-element with unit gain can be expressed via

$$v[k] = v[k-1] + \kappa(r[k] - v[k-1]), \tag{5.10}$$

where $\kappa \in [0, 1]$ is related to the time constant, see Fig. 5.3. One can see that a $\kappa = 0$ leads to a rejection of any external reference changes. Instead, the previous value of v will be continued. On the other hand, a $\kappa = 1$ results in a $v \equiv r$, meaning that the internal reference follows the external one exactly. In order to achieve the fastest possible tracking behavior, the PT1-RG is tasked to find the maximal value of κ, termed κ^*, which does not lead to constraint violation. The resulting optimization problem for $\kappa^* = \kappa^*(r[k], v[k-1], \boldsymbol{x}_l[k], P_l[k])$ is given by:

$$\begin{aligned}
\kappa^* = \quad & \max_{\kappa \in [0,1]} \kappa && \text{(5.11a)}\\
\text{s.t.} \quad & \tilde{\boldsymbol{x}}_l[n+1] = \boldsymbol{A}_{cl}\tilde{\boldsymbol{x}}_l[n] + \boldsymbol{B}_{cl}\tilde{v}[n] + \boldsymbol{E}_{cl}P_l[k] + \boldsymbol{w}_l, && \text{(5.11b)}\\
& \tilde{v}[n] = \tilde{v}[n-1] + \kappa(r[k] - \tilde{v}[n-1]), && \text{(5.11c)}\\
& \tilde{\boldsymbol{x}}_l[0] = \boldsymbol{x}_l[k], && \text{(5.11d)}\\
& \tilde{v}[-1] = v[k-1], && \text{(5.11e)}\\
& \tilde{\boldsymbol{h}}(\tilde{\boldsymbol{x}}_l[k], \tilde{v}[k], P_l[k]) \in \mathcal{Y},\ \forall\, \boldsymbol{w}_l \in \mathcal{W},\ \forall\, n = 0, \dots, n^*\,, && \text{(5.11f)}
\end{aligned}$$

where n is the prediction index used to compute the future values of $\tilde{\boldsymbol{x}}_l$ with $\tilde{v}$. The initial values for the predictions are initialized in (5.11d)-(5.11e) with $\boldsymbol{x}_l[k]$ and $v[k-1]$

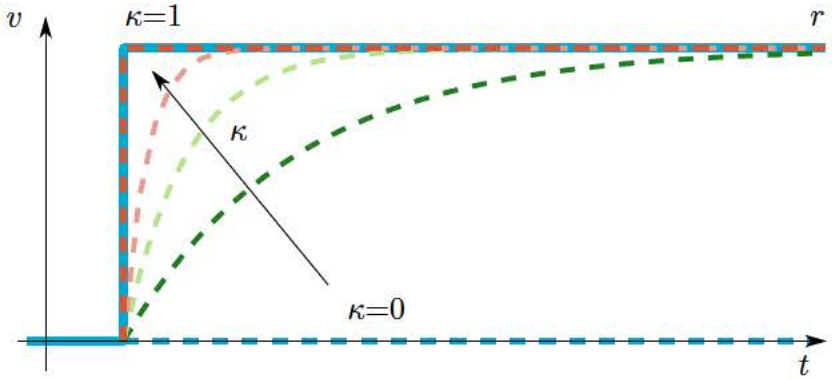

Figure 5.3: Time evolution of the internal reference v generated by the PT1-element for the PT1-RG with different values of κ (dashed lines) when following an external reference r (solid line).

respectively. The value of the prediction horizon n^* has to be chosen so that prediction steps $n > n^*$ no longer contribute to the constraints. It can be shown that (5.11) has a so-called finite determination property [50], meaning that there exists a finite value for n^*. Computation of n^* can be carried out offline, although any upper bound for n^* can also be used instead. An algorithm for solving (5.11) via bisections is given in [51].

5.3.1 Comparison to Classical Reference Governor

This section aims to briefly describe the differences between the PT1-RG and a *classical* RG design, as seen, e.g., in [45]. Similar to before, a low-pass filter is used to generate the internal reference v with a classical RG. However, the predicted future reference values $\tilde{v}$ do not follow any internal dynamics; rather, they are kept constant:

$$\tilde{v}[\infty] = \cdots = \tilde{v}[k+1] = \tilde{v}[k] = v[k-1] + \kappa(r[k] - v[k-1]), \tag{5.12}$$

where κ is again $\in [0,1]$, as seen in Fig. 5.4. The resulting optimization problem for $\kappa^* = \kappa^*(r[k], v[k-1], \boldsymbol{x}_l[k], P_l[k])$ is then given by:

$$\begin{aligned}
\kappa^* = \quad & \max_{\kappa \in [0,1]} \kappa && \text{(5.13a)}\\
\text{s.t.} \quad & \tilde{\boldsymbol{x}}_l[n+1] = \boldsymbol{A}_{cl}\tilde{\boldsymbol{x}}_l[n] + \boldsymbol{B}_{cl}\tilde{v}[n] + \boldsymbol{E}_{cl}P_l[k] + \boldsymbol{w}_l, && \text{(5.13b)}\\
& \tilde{v}[n] = v[n-1] + \kappa(r[k] - \tilde{v}[n-1]), && \text{(5.13c)}\\
& \tilde{\boldsymbol{x}}_l[0] = \boldsymbol{x}_l[k], && \text{(5.13d)}\\
& \tilde{\boldsymbol{h}}(\tilde{\boldsymbol{x}}_l[k], \tilde{v}[k], P_l[k]) \in \mathcal{Y},\ \forall\, \boldsymbol{w}_l \in \mathcal{W},\ \forall\, n = 0, \ldots, n^*\,. && \text{(5.13e)}
\end{aligned}$$

In the case of linear constraints, choosing a $\tilde{v}$ according to (5.12) allows for a greatly reduced computational burden. However, when dealing with nonlinear constraints, as in (5.13e), one has to use bisection for solving (5.13) anyways, see [51]. In that case,

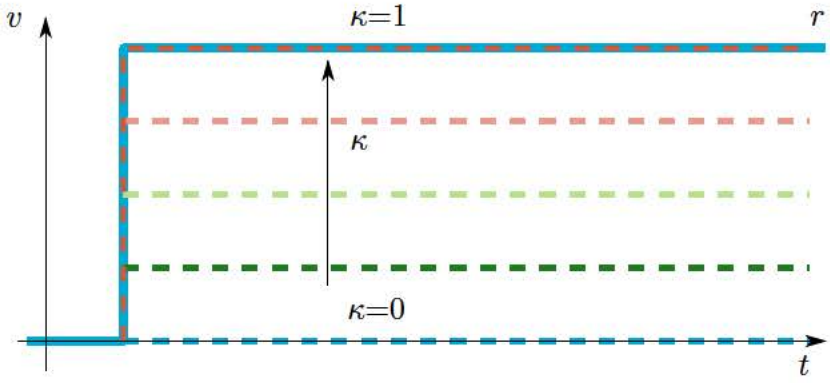

Figure 5.4: Time evolution of the internal reference v for a classical RG with different values of κ (dashed lines) when following an external reference r (solid line).

the difference in computational burden between (5.11) and (5.13) becomes neglectable.

5.4 Simulation Results

A series of simulations were performed to showcase the necessity and advantages of the PT1-RG scheme. All simulations were implemented in MATLAB Simulink/Simscape utilizing validated high-fidelity models, including nonlinear switching characteristics and equivalent series resistance components for the capacitors, similar to the setup described in Section 3.5. It has been shown in Section 3.6 and earlier works (e.g., [16, 38, 39]), that the simulations agree well with results from C-HIL tests. The simulated battery emulator is rated for a maximum of 250 kW. However, for low voltages the maximum current ratings are decisive: the converter stage can deliver a maximum continuous output current of 700 A, while the output stage can briefly handle 800 A. Additional constraints exist for the input variable, as the duty cycle of the PWM signal has to lie between 0 % and 100 %. The controller is designed to dynamically stabilize the output voltage in the range from 48 V to 800 V for UUTs that behave like a CPL while also delivering a fast rise time of 1 ms for unconstrained setpoint changes. The nominal values given in Table 5.1 were utilized for all simulations. Note that a nominal resistance value of $R_1 = 0\,\mathrm{m\Omega}$ was used for controller synthesis; however, the simulations were carried out with a value of $R_1 = 1\,\mathrm{m\Omega}$.

5.4.1 Single Setpoint Change

In the first set of simulations, a single setpoint change is investigated. These simulations aim to illustrate the need for a constraint management concept by showcasing the peak

Table 5.1: Nominal parameters of the model

Description	Notation	Value
DC-link voltage	V_{cc}	820 V
Resistance of each leg	R_1	0 mΩ/1 mΩ*
Inductance of each leg	L_1	300 µH
Inductance of the cable	L_2	25 µH
Capacitance of converter filter	C_1	425 µF
Capacitance of the UUT	C_2	2.3 mF
Maximum converter stage current	$i_{1,\text{limit}}$	±700 A
Maximum output stage current	$i_{2,\text{limit}}$	±800 A
Sampling time	T_s	83.33 µs
Switching frequency	f_{PWM}	12 kHz

*Nominal value for controller synthesis was 0 mΩ, while the value used for simulation was 1 mΩ.

currents demanded by the controller during large setpoint changes. The simulations are carried out with the UUT turned off ($P = 0\,\text{kW}$), illustrating that this issue is not just limited to CPL-like UUTs. Three cases are investigated: The first one without any constraints management scheme, the second one with the proposed PT1-RG, and the third one with a classical RG scheme.

Case 1: Without a Constraints Management Scheme

In the first simulation, no constraint management scheme is used ($\kappa^* \equiv 1$). The results of this simulation can be seen in Fig. 5.5, where the upper plot shows the output voltage $y = v_2$, as well as the internal and external references v and r. As no RG is utilized, $v \equiv r$. The middle plot shows the controlled variable $u = \frac{\mathrm{d}}{\mathrm{d}t} i_1$, and the limits given by 0 % and 100 % duty cycle respectively. In the lower plot, the currents i_1 and i_2 are illustrated, as well as their respective limits. As expected, the resulting rise time of the output voltage is approximately 1 ms [1]. However, the peak converter stage current demanded by the controller is 1250 A, which also results in a peak current in the output stage of more than 1700 A. Such high currents would trip the fail-safe in the device, resulting in an emergency shutdown to prevent component damage. Furthermore, the requested u would have required a duty cycle of more than 100 %, which is physically impossible.

[1] The rise time is measured from requesting the setpoint change to achieving 90 % of the step-height.

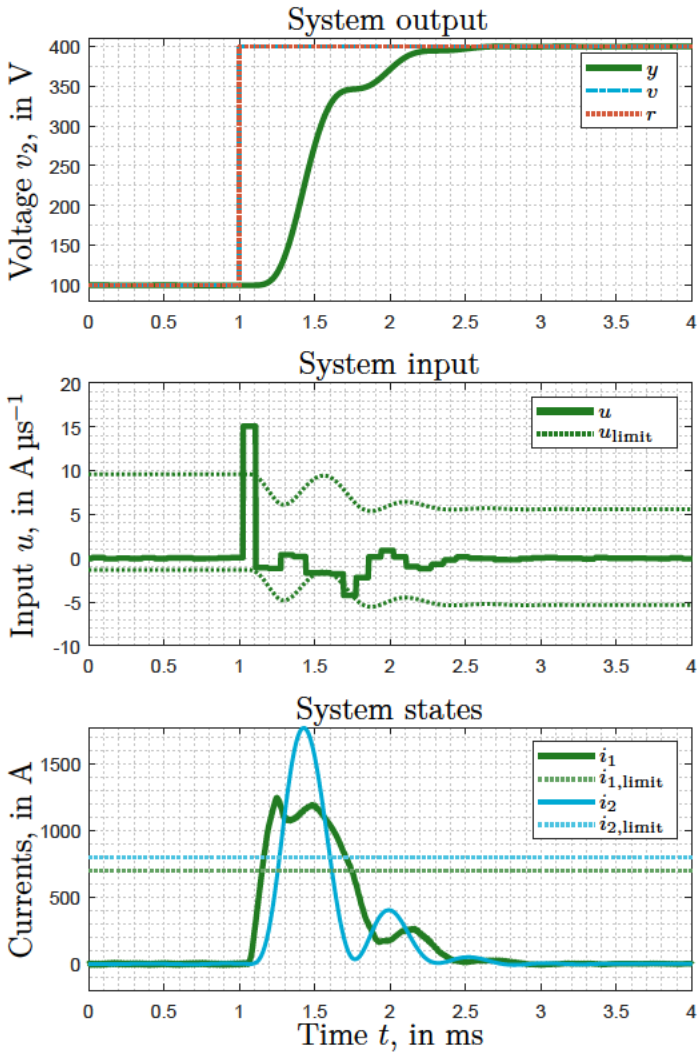

Figure 5.5: Simulation results without constraints management, performing a single setpoint change with $P = 0\,\text{kW}$.

Case 2: Using the Proposed PT1 Reference Governor

The PT1-RG was implemented to handle the constraints in the second simulation. The simulation results are illustrated in Fig. 5.6. Looking at the upper plot, one can see that the PT1-RG manipulated the internal reference v according to (5.11). This modification resulted in a slower rise time of 1.5 ms. However, the constraints were satisfied during the setpoint change: All the currents were within their limits, as well as the requested controlled input u.

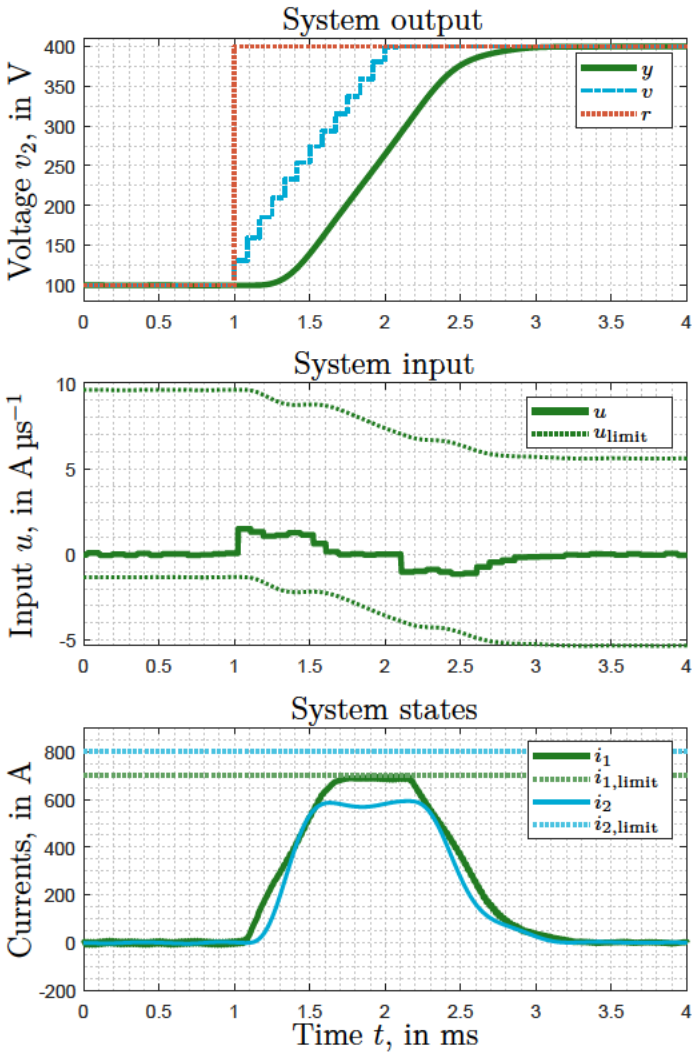

Figure 5.6: Simulation results with the proposed PT1-RG, performing a single setpoint change with $P = 0\,\text{kW}$.

Case 3: Using a Classical Reference Governor

Finally, a classical RG was used in the next simulation, shown in Fig. 5.7. As expected, all constraints were satisfied as well in this simulation. The rise time is also comparable to the one achieved with the PT1-RG. However, the current i_2, as seen in the lower plot of Fig. 5.7, shows an undesired oscillation. The requested u is also greater in magnitude with the classical RG compared to the PT1-RG.

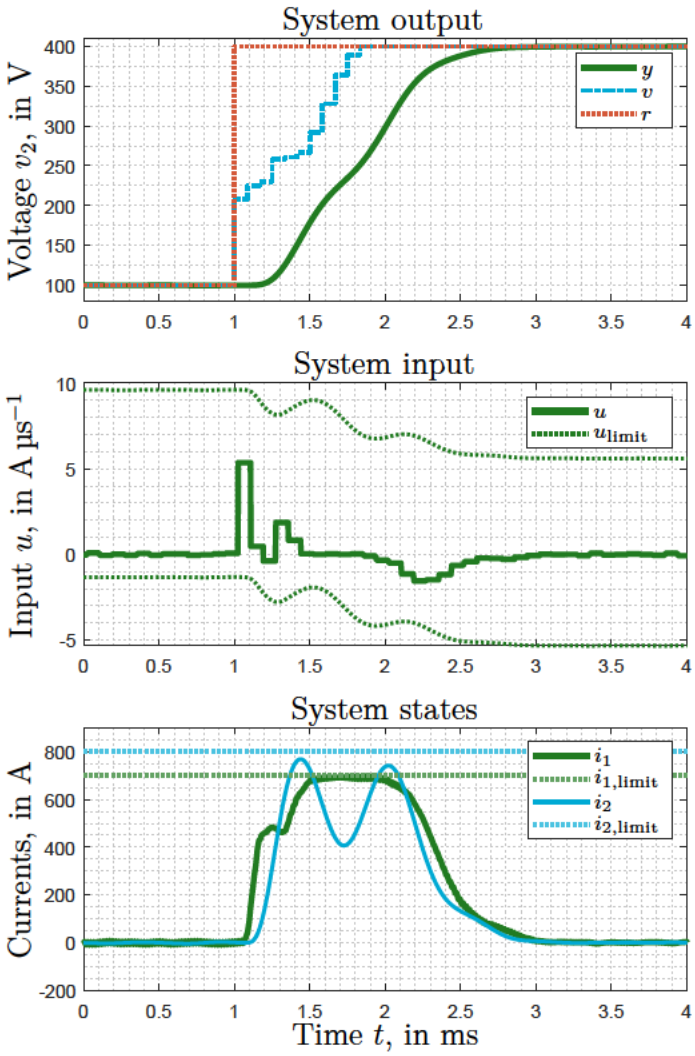

Figure 5.7: Simulation results with a classical RG, performing a single setpoint change with $P = 0\,\text{kW}$.

Comparing the results in Fig. 5.6 and Fig. 5.7 it is evident that both the PT1-RG and the classical RG are able to satisfy the constraints. However, the controller effort was significantly reduced when using the PT1-RG scheme compared to the classical RG. Additionally, no oscillations on the current i_2 occurred when using the PT1-RG. This is partially caused by the fact that the internal reference v in Fig. 5.6 has a constant slope, while in Fig. 5.7, it is composed of multiple steps with different heights.

5.4.2 Multiple Setpoint Changes

Another simulation was carried out to showcase the performance of the developed PT1-RG concept for different setpoint changes. The UUT was turned on for this simulation, drawing a constant power of $P = 50\,\mathrm{kW}$. First, a series of smaller setpoint changes were carried out in the region of 100 V to 400 V, see Fig. 5.8. After that, a large setpoint change from 100 V to 700 V is carried out, followed by another setpoint change from 700 V down to 100 V. In the upper plot of Fig. 5.8, one can see how the PT1-RG manipulated the internal reference v depending on the voltage level and height of the step. The controlled variable u stays in the feasible region throughout the simulation, as illustrated in the middle plot. Also, the currents i_1 and i_2 stay within their respective limits, as can be seen in the lower plot of Fig. 5.8. As per design, the RG computed an internal reference $v \neq r$ only when violations of the constraints were imminent (e.g., during the initial step or the larger steps). During non-critical setpoint changes, the internal reference followed the external one, resulting in fast rise times. Additionally, there were no oscillations in the currents during constraint operation.

5.5 Design Considerations and Discussion

In this chapter, a PT1-RG for handling constraints in a battery emulator is presented. Simulations show that the PT1-RG is able to modify the voltage setpoint trajectory for the controller such that potentially dangerous over-current situations are avoided. Furthermore, the PT1-RG is also able to handle constraints regarding the input variable, ensuring that the duty cycle of the PWM signal is always feasible. Both the nonlinear state and the input constraints are consistently met over the entire operating range of the battery emulator with the presented RG scheme. By implicitly including a PT1-element with a variable time constant into the prediction model of the RG, the PT1-RG resulted in a smoother transition between setpoints with fewer oscillations in the states compared to a classical RG design without PT1-element. Additionally, the required control effort is also reduced for the PT1-RG compared to a classical RG, while both achieve comparable rise times. Also, the computational effort for the PT1-RG and the classical RG are comparable as the nonlinear constraints mandate a bisection algorithm to solve the underlying optimization problem. However, for applications with linear constraints (and linear system dynamics), the classical RG scheme allows for a significantly reduced computational complexity as one can compute a so-called maximal output admissible set [52], which simplifies the online optimization problem considerably. Common to most RG schemes, the proposed PT1-RG modifies the external reference only if constraints would be violated [47]. If no constraint violations are imminent, the RG preserves the closed-loop dynamics given by the plant and the controller. In either case, a setpoint is provided to the controller, which does not lead to constraint violations. Therefore, the results of the stability analysis for the

proposed controller concerning unconstraint setpoint changes shown in Chapter 4 are also applicable if an RG scheme is used. Consequently, the inclusion of the PT1-RG to the overall control concept enables a safe operation of the battery emulator over the entire operating range as dangerous over-current situations are prevented during large setpoint changes without negatively impacting the stability of the closed-loop system.

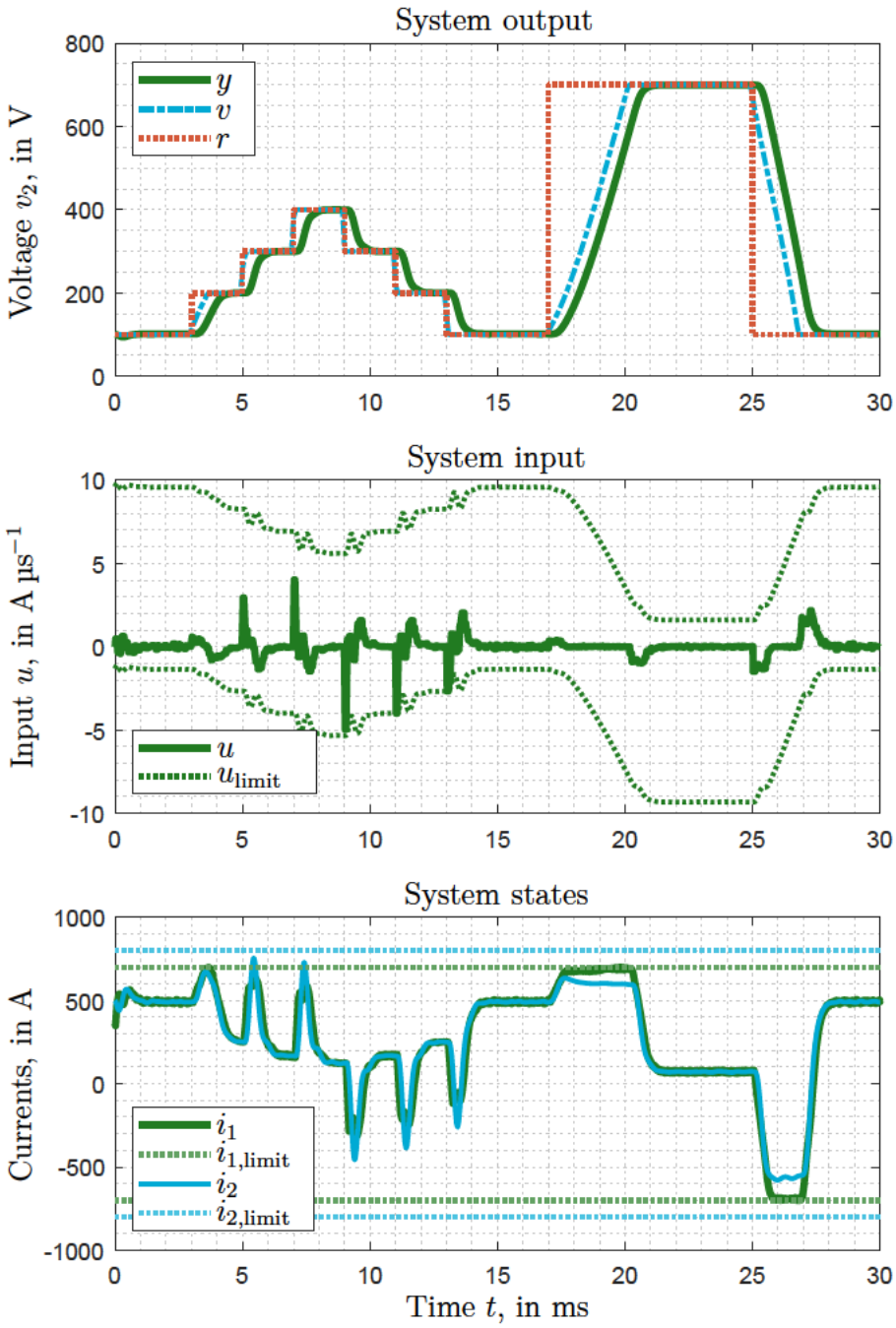

Figure 5.8: Simulation results with a PT1-RG, performing multiple setpoint changes with $P = 50\,\text{kW}$.

Chapter 6

Conclusion and Outlook

This dissertation summarizes the most important research results of my work at TU Wien in cooperation with AVL List GmbH. The research focus of this project was the development of a suitable control concept for DC converters connected to nonlinear loads. The control concept's primary design objectives are a highly dynamic output voltage and an extensive stable operating range. The latter objective is especially challenging if the load behaves like a CPL, which renders the system not just nonlinear but also unstable. Furthermore, the control concept should also be able to fulfill safety-critical constraints, such as avoiding overcurrent situations to ensure the protection of its components. However, during the design process, one must also take into account the limited computing resources available on the hardware, which limits the allowable complexity of the control law. The developed concept is exemplified in this work by a DC-DC converter used as a battery emulator in automotive testbeds. In a battery emulator setup, a real-time-capable battery model computes the appropriate voltage response based on the characterization of the physical battery being emulated and the measured current draw of the UUT. A highly dynamic output voltage of the battery emulator is required to follow the computed voltage response as fast as possible in order to achieve the most accurate emulation results possible. Additionally, a large operating region is desired to make the emulator applicable for a variety of battery topologies.
Chapter 2 describes the DC-DC converter used as a controllable DC power supply in the battery emulator in detail and provides a mathematical description of its dynamic behavior. Via first principles, the system equations for the converter stage with binary switching characteristics are derived, and a simplified model for the converter stage is motivated. In this simplified model, the current waveform over one PWM period is approximated via a constant change in current. With this approximation, a relationship between the duty cycle of the PWM signal to a piecewise constant control variable is established. Furthermore, the nonlinear equations describing the output stage, including the UUT in the shape of a CPL, are presented in this chapter. Safety-critical limits of the physical components in the battery emulator are also provided, next to limitations on the control variable.
In order to meet the requirements for a highly dynamic output voltage and a large sta-

ble operating region, a flatness-based control concept has been developed, as described in Chapter 3. When developing a control concept for the presented system, the main problem is that a piecewise constant control input is required to use the approximation of the converter stage dynamics motivated in Chapter 2. However, in order to design a discrete-time control concept that provides such a piecewise constant control input, a discrete-time description of the plant is required. Due to the nonlinearity introduced by the CPL, the differential equations describing the system cannot be solved exactly. Therefore, an exact discrete-time representation of the system could not be found. In order to solve this problem, the developed concept establishes feedback equivalence between the nonlinear system description of the plant and a linearized description. It is hypothesized that if both descriptions have similar dynamics and follow the same output trajectory, the required control inputs are similar in shape. Based on this hypothesis, the linearized system description is used to derive a discrete-time model, which is consequently used to synthesize a discrete-time control law. Due to the established feedback equivalence, this control law can be transformed to be applicable to the nonlinear system over a large operating region. Chapter 3 also includes simulation results comparing the proposed concept with other state-of-the-art concepts. Furthermore, the developed concept was deployed to a prototype board and tested in real-time on a C-HIL setup.
In Chapter 4, a stability analysis is performed in order to investigate whether the above-mentioned hypothesis is valid over a sufficiently large operating range. The primary cause for potential stability issues can be expressed as an input distortion, leading to additional dynamics in the system. A sufficient stability criterion is formulated to examine the additional dynamics by defining a suitable Lyapunov function candidate and using Lyapunov's second method for stability. Based on this criterion, a lower bound estimate of the ROA is computed. The positive invariant set given by the ROA can be used to guarantee stability during the transition between setpoints. The ROA is also used to define an allowable voltage deviation around a target point to which any steady-state starting point with a lower voltage deviation will converge. Furthermore, by examining the ROA over the entire technically feasible operating range, it is demonstrated that the developed concept is able to stabilize the output voltage over the required operating range.
While the stability analysis presented in Chapter 4 can be used to guarantee stable transitions between setpoints, it is only valid if no constraints are violated. As with every physical system, the DC-DC converter in the battery emulator is also subject to constraints due to physical limits. Meeting those constraints is safety-critical, as they protect components from overcurrent situations that could potentially damage them. To ensure that the constraints are met, a modified reference governor with PT1-element (PT1-RG) was proposed in Chapter 5. This RG is an add-on to the developed control concept, which manipulates the internal reference voltage for the controller. By including the PT1-element, the modified reference governor can provide safe and smooth transitions between setpoints by avoiding regions where constraints would be violated. Simulations showcase the need for constraint management and illustrate the

capabilities of the PT1-RG. Furthermore, a comparison to a classical RG (without the PT1-element) is also given, showing the ability of the PT1-RG to reduce state oscillations.
Overall, a highly dynamic control concept for DC converters is presented in this work and exemplified by a DC-DC converter used in a battery emulator. It was shown that the concept meets the requirement for a highly dynamic output voltage and is able to stabilize the system over a large operating range. Furthermore, the concept can meet safety-critical constraints and perform smooth setpoint changes over large voltages. The development of the control concept is not finished yet, but the contents of this dissertation describe the necessary elements for an industrial application of the concept. Due to the prototype status of the hardware, it was not possible to deploy the concept to a physical system yet. However, it is planned to continue the development of the proposed control concept at AVL and use it in the next generation of battery emulators.
Possible enhancements for the presented concept are, for example, the development of a nonlinear observer for the power draw of the UUT. This work assumed that the load current i_p was measured, and consequently, it was easy to obtain the power consumption via $P = i_p \cdot v_2$, where v_2 is the also measured output voltage. However, the load-current i_p might not be available as a measurement for all UUTs.
While the parameter values in the converter stage are well known, the value of the cable's parasitic inductance and the UUT's capacitance can change from setup to setup. However, accurate knowledge of all parameter values is essential to establishing feedback equivalence. Therefore, it is also interesting to investigate the possible addition of an automatic parameter identification procedure to arrive at the correct values.
While IGBTs are used as switching devices in the converter stage in the presented configuration, advances in semiconductor technology might change that. Particularly SiC MOSFETs are a viable alternative as they offer higher switching frequencies while having comparable voltage ratings. In order to keep up with those higher switching frequencies (and consequently shorter sampling times), the usage of field programmable gate arrays (FPGAs) should be considered. The main advantage of FPGAs, as opposed to DSPs, is the parallel execution of simple logic, which the presented control concept could take advantage of due to its modular nature.

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Appendix A

Flatness Properties

An important prerequisite for the control concept developed in this work is the so-called *flatness property*. The flatness property extends the idea of controllability from linear systems to nonlinear systems. If the system possesses the flatness property, it is said to be a *flat system* and a (usually fictious) *flat output* can be found. All state and input variables of a flat system can be completely described in terms of this flat output and a finite number of its time derivatives. With the presented nonlinear system Σ_{nl} the flat output coincides with the system output y. The output y of Σ_{nl} and its time-derivatives are given by the following equations:

$$y = v_2 \tag{A.1}$$

$$\dot{y} = \frac{i_2}{C_2} - \frac{P}{C_2\, v_2} \tag{A.2}$$

$$\ddot{y} = \frac{P\left(\frac{i_2}{C_2} - \frac{P}{C_2\, v_2}\right)}{C_2\, {v_2}^2} - \frac{\frac{v_2}{L_2} - \frac{v_c}{L_2}}{C_2} \tag{A.3}$$

$$\begin{aligned} y^{(3)} = &\left(-\frac{P}{{C_2}^2\, {v_2}^2}\right)\left(\frac{v_2}{L_2} - \frac{v_c}{L_2}\right) \\ &- \left(\frac{i_2}{C_2} - \frac{P}{C_2\, v_2}\right)\left(\frac{1}{C_2\, L_2} - \frac{P^2}{{C_2}^2\, {v_2}^4} + \frac{2\,P\left(\frac{i_2}{C_2} - \frac{P}{C_2\, v_2}\right)}{C_2\, {v_2}^3}\right) + \frac{\frac{i_1}{C_1} - \frac{i_2}{C_1}}{C_2\, L_2} \end{aligned} \tag{A.4}$$

$$
\begin{aligned}
y^{(4)} = &\left(\frac{v_2}{L_2} - \frac{v_c}{L_2}\right)\left(\frac{\frac{1}{C_2\,L_2} - \frac{P^2}{{C_2}^2\,{v_2}^4} + \frac{2\,P\left(\frac{i_2}{C_2} - \frac{P}{C_2\,v_2}\right)}{C_2\,{v_2}^3}}{C_2} + \frac{1}{C_1\,C_2\,L_2} + \frac{2\,P\left(\frac{i_2}{C_2} - \frac{P}{C_2\,v_2}\right)}{{C_2}^2\,{v_2}^3}\right) \\
&- \left(\frac{i_2}{C_2} - \frac{P}{C_2\,v_2}\right)\left(\left(\frac{6\,P^2}{{C_2}^2\,{v_2}^5} - \frac{6\,P\left(\frac{i_2}{C_2} - \frac{P}{C_2\,v_2}\right)}{C_2\,{v_2}^4}\right)\left(\frac{i_2}{C_2} - \frac{P}{C_2\,v_2}\right) - \frac{-\frac{P}{{C_2}^2\,{v_2}^2}}{L_2}\right. \\
&\left. - \frac{2\,P\left(\frac{v_2}{L_2} - \frac{v_c}{L_2}\right)}{{C_2}^2\,{v_2}^3} + \frac{P\left(\frac{1}{C_2\,L_2} - \frac{P^2}{{C_2}^2\,{v_2}^4} + \frac{2\,P\left(\frac{i_2}{C_2} - \frac{P}{C_2\,v_2}\right)}{C_2\,{v_2}^3}\right)}{C_2\,{v_2}^2}\right) \\
&- \frac{\left(\frac{i_1}{C_1} - \frac{i_2}{C_1}\right)\left(-\frac{P}{{C_2}^2\,{v_2}^2}\right)}{L_2} + \underbrace{\frac{1}{C_1\,C_2\,L_2}}_{L_g L_f^3 h(\boldsymbol{x})}\,u
\end{aligned}
\tag{A.5}
$$

From the above equations, one can see that for a $v_2 \neq 0$ the output and its time-derivatives are continuously differentiable with respect to $\boldsymbol{x}$ and u. Note that, $y = y(v_2)$ is linear in v_2, that $\dot{y} = \dot{y}(v_2, i_2)$ is linear in i_2, that $\ddot{y} = \ddot{y}(v_2, i_2, v_c)$ is linear in v_c, and so on. Therefore, the states $\boldsymbol{x} = [v_2, i_2, v_c, i_1]^T$ and the input u can be uniquely represented as functions of the output and the first 4 time-derivatives: $\boldsymbol{x} = \boldsymbol{\Phi}^{-1}(y, \dot{y}, \ddot{y}, y^{(3)})$ and $u = \phi(y, \dot{y}, \ldots, y^{(4)})$. As the system is further square, meaning that it has the same number of inputs as outputs, all the conditions for *flatness* are met [53]. Note as the input u only appears in the 4th time-derivative of y, the system is said to have a *relative degree* of 4. As Σ_{nl} is of order 4 ($\dim(\boldsymbol{x}) = 4$), it is further said to have *full relative degree*.

Remark A.1. *The singularity at $v2 = 0$ is not restrictive for the presented use-case. That is because the UUT would not be turned on below a certain threshold voltage. Therefore, the UUT would either draw a constant current or no current below this threshold voltage. In either case, the resulting system dynamics would be linear.*

The flatness property of Σ_l can be shown easier: As Σ_l is linear, it is flat if and only if it is controllable [35]. For real and positive values of C_1, C_2, and L_2 the controllability matrix of Σ_l has full rank. Therefore, it is controllable and by extension also flat.

Curriculum Vitae

Personal Information

Name	Dipl.-Ing. Michael Zauner
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Education

03/2018 -	TU Wien Doctoral studies in Mechanical Engineering
10/2011 - 03/2018	TU Wien Diploma studies in Mechanical Engineering Specialization in Control and Process Automation Final examination passed with distinction on March 6th, 2018
09/2005 - 06/2010	HTBLuVA, Mödling (secondary school) Institute for Wood Technology Final examinations passed with high distinction in June, 2010

Diploma Thesis

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Professional Work Experience

03/2018 -	Project assistant at TU Wien Institute of Mechanics and Mechatronics Division of Control and Process Automation
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IT Skills

Operation systems	Windows, Linux
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