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High-Temperature Reorganization Behavior of Single-Crystalline Porous 4H-SiC Thin Foils

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Abstract. This work reports on the high-temperature reorganization behavior of single-crystalline porous 4H-silicon carbide (4H-SiC) thin foils. Porous 4H-SiC thin foils are realized via state-of-the-art photoelectrochemical etching in hydrofluoric (HF) acid solution enabling for the first time a released foil with a diameter of 2 inches. Subsequent annealing under inert gas atmosphere and comparison between samples suggests that a temperature of 1500 °C allows for various degrees of compactification across the foil surface, whereas at 1600 °C single crystallinity can be preserved.

Introduction

In modern semiconductor industry SiC plays an ever-growing role as alternative to silicon, specifically in the field of power devices, thanks to its superior properties including, but not limited to, a wide band gap, a high electrical breakdown field, thermal stability and chemical inertness [1].

In this context, epitaxial processes are one of the key techniques to harness SiC desirable properties for device fabrication, but a major drawback for such processes is that they are quite cost intensive [2]. To increase the market share of SiC power devices, however, the overall costs of substrate and epitaxial processes need to be reduced substantially. As a consequence, the use of advanced substrate concepts is envisaged.

A promising approach to tackle this challenge would consist in bonding a monocrystalline SiC foil released from a standard SiC wafer to an alternative, less cost-intensive substrate. However, since techniques such as controlled spalling or smart-cut are not yet established in industry for SiC substrate manufacturing as in silicon, novel technologies are required to address this need.

Recent developments in photoelectrochemical etching proved the possibility to release 1-inch porous SiC foils with a thickness ranging in the order of a few µm from standard 4H-SiC wafers by using an HF acid-based electrolyte [3, 4]. This process can be summarized as follows: to start, metal-assisted photo chemical etching (MAPCE) is applied, where a first superficial layer is porosified on the wafer. A subsequent photo electro-chemical etching (PECE) step is performed to propagate the pore front in a controlled way into depth. Finally, the release of a porous thin foil from the original

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wafer is achieved by applying a short voltage pulse. Further improvement of this process allowed to scale-up the released foil diameter to a previously unreported size of 2 inches.

Controlled reorganization of such porous thin foils, however, is a vital pre-requisite to exploit the full potential of this promising technology for industrial applications in analogy to what has been already established in silicon [5]. Hence, the effect of high-temperature annealing in helium gas atmosphere on the reorganization process of porous SiC is investigated, advancing knowledge on SiC in this field.

In this study we therefore report on first results that the goal of producing monocrystalline SiC foils released from a standard SiC wafer can be reached through a combination of photo electro-chemical etching as well as high-temperature annealing in an inert gas atmosphere.

Methods

Photochemical etching. For the etching procedure a 4-inch wafer of n-type 4H-SiC (001) with a 4° off-axis cut first undergoes a MAPCE step for pore initiation on its C-face. The wafer is then placed in an etching chamber from AMMT GmbH for the PECE step. In this configuration, a 2-inch circular portion of the wafer surface is in direct contact with an HF etching solution as well as exposed to a custom built UV source consisting of an 18 W UV-C low pressure mercury vapor lamp through a sapphire window, as depicted in Fig. 1a. This latter combination allows to generate a well-controlled porous structure into the 4H-SiC wafer, where the size and the shape of the developing pores are substantially influenced by the voltage profile applied between both cell electrodes, as shown in Fig. 1b. With a tailored voltage characteristic over time, the pore morphology at the bottom of the etched layer can be designed such that the release from the original wafer is possible using a high voltage pulse at the end of the PECE process.

High-temperature annealing. Following the release from the original wafer, a smaller portion of the thin foil, with an approximate size of 5×5 mm^2, was annealed in a helium gas atmosphere in a Netzsch STA 449 F1 Jupiter high-temperature Differential Scanning Calorimeter using two different procedures. First, the heating process has been carried out until a peak temperature of 1500 °C is reached and held for 30 min. after applying a heating rate of 20 °C/min. Next, the sample has been cooled down to room temperature applying a cooling rate of 20 °C/min. For the second sample, the annealing process has been carried out at a temperature of 1600 °C applying a heating rate of 10 °C/min. After reaching the peak temperature, the sample has been cooled down to room temperature applying a cooling rate of 10 °C/min.

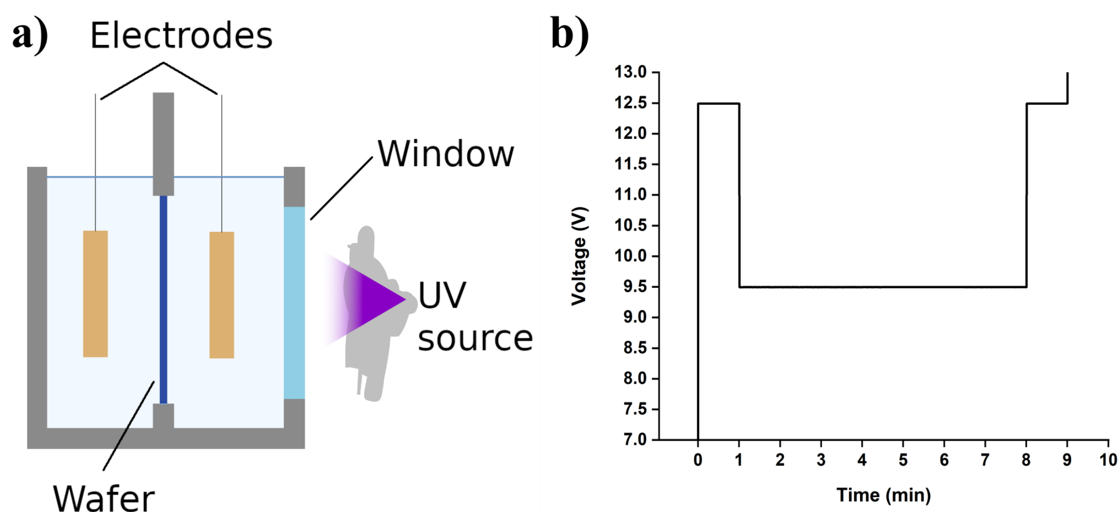

Fig. 1. (a) Schematic representation of the photoelectrochemical etching chamber and (b) voltage profile as a function of time applied between the electrodes during PECE.

Thin foils characterization. For the thin foils prior and after annealing at 1500 °C, cross-sectional and top-down analyses have been performed with a Hitachi SU8030 scanning electron microscope (SEM) using an acceleration voltage of 2 kV. For the thin foils prior and after annealing at 1600 °C, samples have been prepared via focused ion beam (FIB) and successive high-resolution imaging and selected area electron diffraction (SAED) patterns have been done with a FEI TECNAI F20 transmission electron microscope (TEM) at an acceleration voltage of 200 kV.

Results and Discussion

In Fig. 2a, an optical micrograph of a 4-inch 4H-SiC wafer is shown, from which after applying a local photoelectrochemical etching process a thin foil is released, demonstrated by the same wafer missing the circular portion in the middle (see Fig. 2b and 2c). The thickness of the released foil can be adjusted by the etching time during the photochemical etching process. In this study the released foils ranged from 25 to 30 µm in thickness.

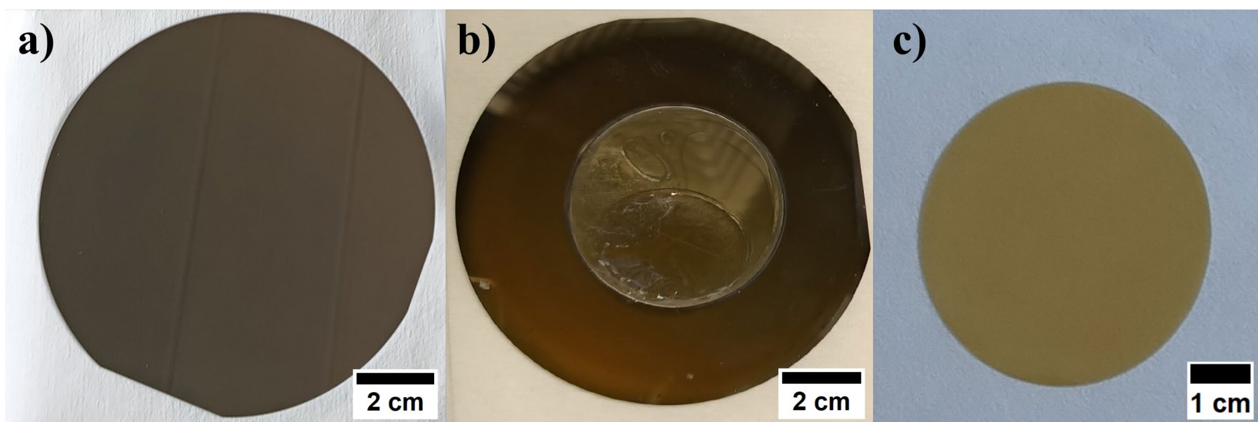

Fig. 2. Example of 4-inch wafer (a) before and (b) after etching process and (c) resulting in a 2-inch released thin foil.

A striking feature of this procedure is that multiple thin foils can be released sequentially from the same wafer and each foil can have an individually customized pore profile related to the voltage profile applied during the PECE step. The explanation for this feature is that MAPCE is currently needed only for the very first surface-near initiation of pores on a clean wafer because after the first foil release the newly exposed surface already possesses a sufficient superficial porosity to allow an immediate PECE step to successfully release a new foil without intermediate steps.

Characterization of pores morphology. The cross-sectional SEM analysis of thin foils before and after annealing at 1500 °C (see Fig. 3) shows that both samples, with a thickness of around 27 µm, exhibit two separated regions having different pore size, which are related to the first one-minute section at 12.5 V and the subsequent seven minutes section at 9.5 V of the etching procedure (see Fig. 1b). The last one-minute section at 12.5 V is, however, too thin to be visible at this magnification.

A more in-depth analysis is shown in Fig. 4 for three different regions consisting of the top (C-face of the foil), the voltage transition area and the bottom (Si-face of the foil). A comparison between the left and right column suggests that high-temperature annealing in helium atmosphere allowed for a partial reorganization of the originally elongated pores being now arranged and segmented in isolated tracks. The region associated with the transition from 12.5 V to 9.5 V (see Fig. 4c and Fig. 4d) shows the effect of sudden voltage change on pores size, where the average pore width decreases from values estimated to be just above 20 nm at 12.5 V to typical width values between 10 nm and 20 nm at 9.5 V. Another relevant feature is the presence of protrusions (indicated by black lines on Fig. 4a and Fig. 4e) on both the Si and C-face sample surfaces before annealing. Taking into account that this thin foil is the fifth one released from the original wafer, these protrusions are understood as high porosity regions due to the last one minute step at 12.5 V during PECE (see Fig. 1b) from the

previous release, on the C-face (see Fig. 4a), and from the current release, on the Si-face (see Fig. 4e). When comparing both samples after annealing a remarkable conclusion is that high-temperature reorganization allows for a noticeable decrease in surface roughness for both SiC faces.

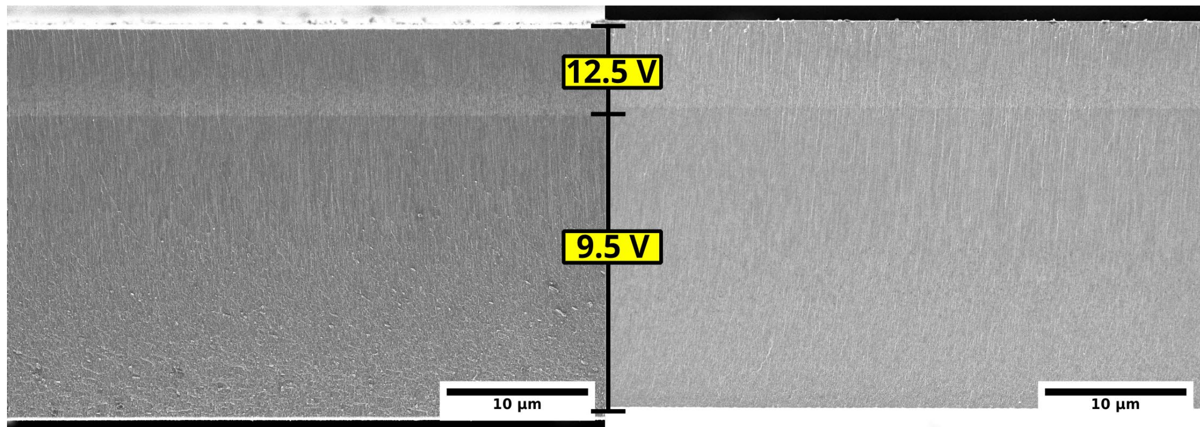

Fig. 3. Cross-sectional SEM image of the porous thin foil before (left) and after annealing (right) in helium atmosphere at 1500 °C. The vertical line indicates the two main regions separated by the rapid voltage transition applied during PECE.

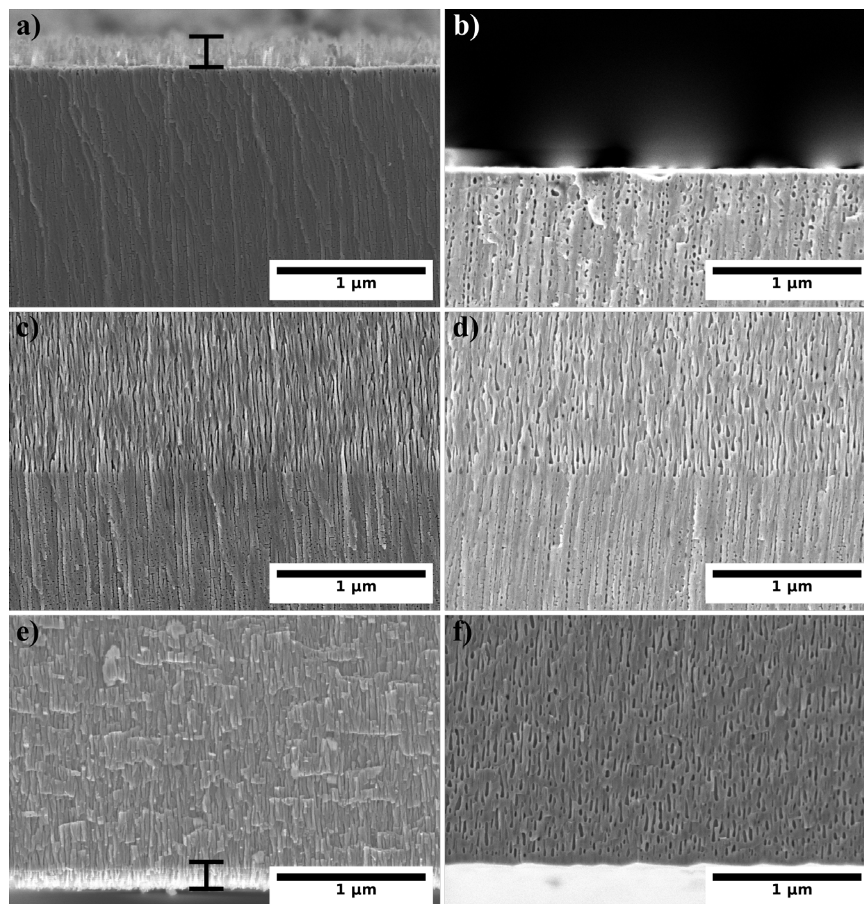

Fig. 4. Cross-sectional SEM images of the porous thin foil before (left column) and after annealing (right column) in helium atmosphere at 1500 °C for: (a) and (b) top C-face, (c) and (d) voltage transition area, (e) and (f) bottom Si-face. The black lines in (a) and (e) indicate the protrusions extension from the corresponding surfaces.

Additionally, comparison between selected surface areas, as shown in Fig. 5, confirms that reorganization during annealing in helium greatly affects the surface morphology eliminating protrusions and allowing various degrees of compactification. In particular, reorganization on the Si-

face can lead to a complete closing of the previously open porous surface, forming terraces that can be ascribed to the off-axis tilting of the original wafer [6].

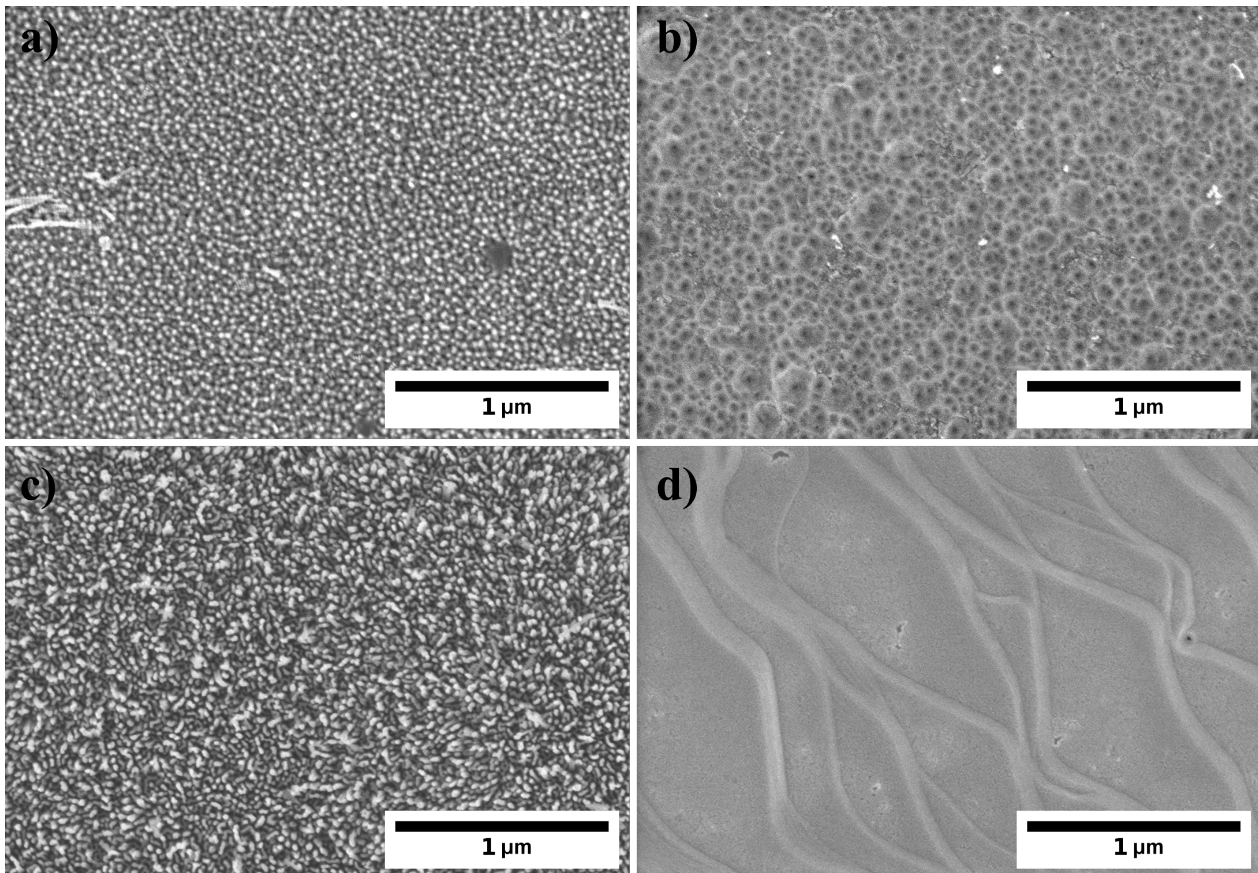

Fig. 5. SEM images in top view on the porous thin foil surface: C-face (a) before and (b) after annealing, Si-face (c) before and (d) after annealing in helium atmosphere at 1500 °C.

Assessment of crystal structure. After the assessment of material reorganization after annealing, the crystallographic structure of the closed pores surface is investigated. To demonstrate the modifications, cross-sectional HRTEM images were recorded at voltage transition areas together with SAED patterns, over a larger portion of the same, before and after annealing at 1600 °C (see Fig. 6). Comparison between Fig. 6a and Fig. 6b together with the related SAED in Fig. 6c and Fig. 6d shows that, while the structure of the pores boundary experiences substantial change, the overall single crystalline structure of 4H-SiC is preserved after etching and after subsequent annealing up to 1600 °C in helium atmosphere. A more detailed analysis of the diffraction patterns confirms this statement through a direct comparison of diffraction spots distances for a set of indexes selected from reference [7]. Fig. 6c and 6d depict the reciprocal lattice indexes of choice and Table 1 shows the results which are collected by measuring, for each index, the distance across several spots and then dividing such distance for the number of crossed spots, proving quantitative consistency between the two crystal structures.

As presented in Fig. 6b, it is worth mentioning that the boundary between reorganized 4H-SiC (lower part in dark gray) and internal pore wall (upper part in light gray) is clearly distinguishable. Careful examination suggests that the superficial layer on the inner pore wall may not follow the same ordered crystalline structure as expected from the bulk material. This observation may find some support from the results in a recent work focusing on the effects of graphene growth in porous SiC in an ultra-high-vacuum UHV environment [8]. Such results show that after annealing at temperatures well below 1500 °C carbon formations may grow on internal pore walls of SiC, thus hinting to a clear direction for future studies on this topic.

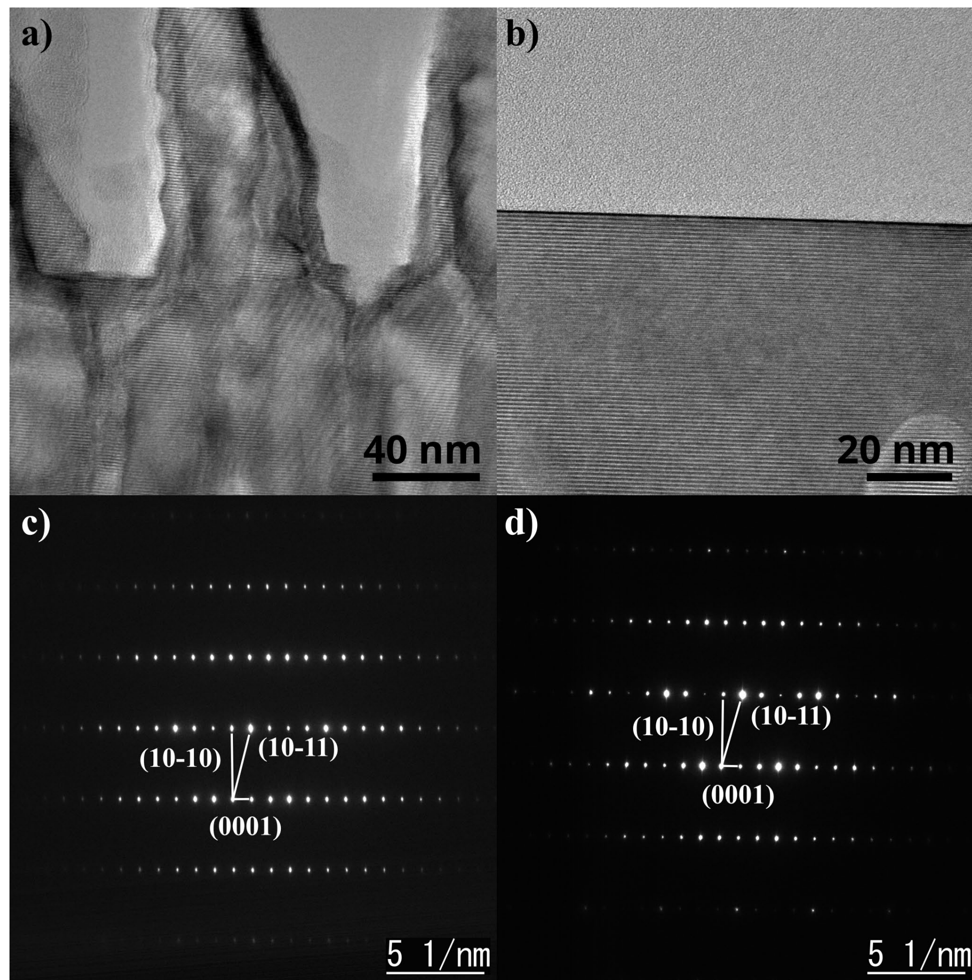

Fig. 6. Cross-sectional HRTEM image and related selected area diffraction pattern of the porous foils in the voltage transition area (a and c) before and (b and d) after annealing in helium atmosphere at 1600 °C. In (a) and (b) dark gray portions represent bulk SiC, while light gray portions represent porous regions.

Table 1. Comparison of reciprocal lattice distances.

Sample	Indexes for the reciprocal lattice planes		
	(0001) [1/nm]	(10-10) [1/nm]	(10-11) [1/nm]
Before annealing	0.95	3.58	3.69
After annealing	0.96	3.62	3.77

Summary

We presented, in comparison to already existing literature, a successful upscaling from 1-inch to 2-inch diameter wide foil release of porous 4H-SiC from a 4-inch wafer via photoelectrochemical etching. We believe that this promising result is an essential milestone on the way to fabricate low cost alternative SiC substrates in wafer dimensions currently used in semiconductor industry.

Furthermore, we showed how a single crystalline porous structure reorganizes after a high-temperature annealing process in an inert gas atmosphere. Evidence of surface compactification coupled with proof of preserved single crystallinity suggest that proper fine-tuning can lead to controlled compactification across the entire foil surface without sacrificing the 4H-SiC structure. A natural continuation of this topic should address the effect of different gas atmospheres to determine either possible similarities, as could be expected from another noble gas such as argon, or differences, perhaps in the case of nitrogen which may not be inert towards SiC at such high temperatures.

All in all, these results demonstrate the outstanding prospects for the cost-effective realization of 4H-SiC thin foils as potential platform for advanced SiC substrate concepts when bonding these compactified single-crystalline foils to alternative substrates.

Acknowledgements

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