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Faithful dynamic timing analysis of digital circuits using continuous thresholded mode-switched ODEs☆

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ABSTRACT

Thresholded hybrid systems are restricted dynamical systems, where the current mode, and hence the ODE system describing its behavior, is solely determined by externally supplied digital input signals and where the only output signals are digital ones generated by comparing an internal state variable to a threshold value. An attractive feature of such systems is easy composition, which is facilitated by their purely digital interface. A particularly promising application domain of thresholded hybrid systems is digital integrated circuits: Modern digital circuit design considers them as a composition of Millions and even Billions of elementary logic gates, like inverters, OR and AND. Since every such logic gate is eventually implemented as an electronic circuit, however, which exhibits a behavior that is governed by some ODE system, thresholded hybrid systems are ideally suited for making the transition from the analog to the digital world rigorous.

In this paper, we prove that the mapping from digital input signals to digital output signals is continuous for a large class of thresholded hybrid systems. Moreover, we show that, under some mild conditions regarding causality, this continuity also continues to hold for arbitrary compositions, which in turn guarantees that the composition faithfully captures the analog reality. By applying our generic results to some recently developed thresholded hybrid gate models, both for single-input single-output gates like inverters and for a two-input CMOS NOR gate, we show that they are continuous. Moreover, we provide a novel thresholded hybrid model for the two-input NOR gate, which is not only continuous but also, unlike the existing one, faithfully models all multi-input switching effects.

1. Introduction

The behavior of *thresholded hybrid systems* is governed by the dynamics of a continuous process, described by some system of *ordinary differential equations* (ODEs), which is selected according to externally supplied digital mode switch signals from a set of

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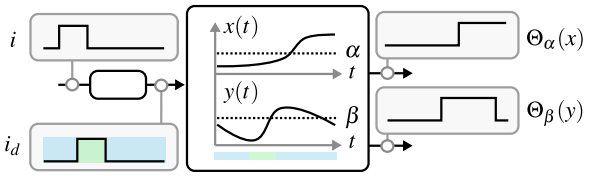


Fig. 1. Thresholded mode-switched ODE with a single mode input i, the delayed input i_d, two continuous states x, y, and two thresholded outputs $\Theta_\alpha(x)$ and $\Theta_\beta(y)$.

candidates, and controls some digital outputs based on whether some internal signals are above or below a threshold, see Fig. 1 for an illustration. Thresholded hybrid systems can be found in various application areas, including digitally controlled thermodynamic processes, hydrodynamic systems, and, in particular, digital integrated circuits. Consider a simple digitally controlled heating system, for example: The continuous dynamics of the room temperature would be governed by some ODE for the case when the heating is switched on, and another ODE for the case where the heating is switched off. A binary mode switch input signal tells whether the heating is switched on or off. Two binary output signal, low resp. high, report on whether the current room temperature is below 20 degrees resp. above 23 degrees. A simple digital bang–bang controller could be used to switch the heating on when low makes a transition from 0 to 1, and to switch it off when high makes such a transition.

In this paper, we will study properties of such thresholded hybrid systems, and systems built from those via arbitrary composition, i.e., where the digital output signal of one component drives a mode switch signal of one or more other components, possibly forming some feedback loops. First and foremost, we will give conditions that ensure the continuity of the outputs of such systems with respect to their external inputs. This continuity property guarantees that small timing variations of the digital input signals lead to small variations of the digital output signals only. Moreover, we will show that, under some mild constraints regarding causality, any finite composition of continuous thresholded hybrid systems is continuous, and faithfully models the analog reality.

Whereas our continuity results are independent of the particular application area, we will tailor our presentation primary to digital integrated circuits. Indeed, digital circuits are a particularly important class of systems composed of thresholded hybrid systems, modeling elementary logic gates like inverters, OR, and AND, which will be called *digitized hybrid gates* in the sequel. The application of our generic results will reveal that thresholded hybrid systems are indeed ideally suited for making the transition from the analog implementation to the digital abstraction in modern digital circuit design rigorous.

Digital circuit modeling basics. Modern digital integrated circuits consist of Millions and sometimes Billions of transistors, which are analog electronic devices and thus process and generate analog signals. Modern digital circuit design, on the other hand, considers a circuit as a composition of elementary digital logic gates, and leaves it to (quite complex) tools to compile a design down to its analog implementation.

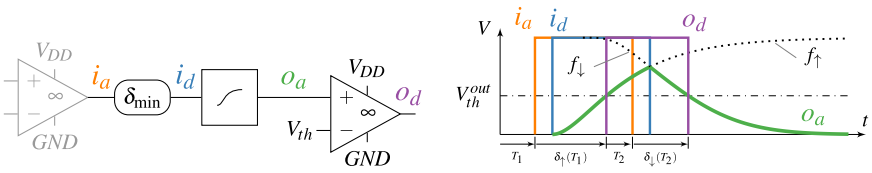
In view of the very short design cycles nowadays, developers cannot afford to repeatedly downcompile a design to verify its correctness and performance. Fast *digital* functional verification and timing analysis techniques and tools are hence key elements of modern circuit design. In particular, thanks to the elaborate static timing analysis techniques available today, like CCSM [1] and ECSM [2], worst-case critical path delays can be determined very accurately and very quickly, even for very large circuits. Whereas such corner-case delay estimates are sufficient for synchronous circuit designs, which are still the vast majority nowadays, analyzing the behavior of specific asynchronous circuits, like the one described in [3], or inter-neuron links using time-based encoding in hardware-implemented spiking neural networks [4], require more elaborate timing analysis techniques.

More specifically, consider the token-passing ring studied by Winstanley et al. in [3], which is composed of stages consisting of a 2-input Muller C gate with its inputs connected to the preceding and succeeding stages. The authors demonstrated that this ring implements an oscillator, which exhibits two distinct modes of operation: burst behavior and evenly spaced output transitions, which can alternate over time in an unpredictable (chaotic) fashion. In order to predict the actual behavior of this circuit, it is essential to track the timing relationships of *individual* transitions across the entire ring. Since static timing analysis techniques cannot accomplish this, *dynamic* timing analysis techniques need to be resorted to.

The golden standard for dynamic timing analysis are analog simulations, e.g., using SPICE [5], applied to a (usually manufacturer-supplied) ODE model of the entire circuit. Since such numerical analog simulations are prohibitively time-consuming even for small circuits and short signal traces, *digital* dynamic timing analysis techniques have been invented as a less accurate but much faster alternative. They rest on fast and efficiently computable *gate delay models* like pure or inertial delays [6], which provide input-to-output delay estimations for every gate. The resulting dynamic timing analysis techniques enable efficient correctness validation of large circuits, as well as precise performance and power estimations, even during early design stages [7].

The simplest non-trivial[1] digital delay models suitable for accurate dynamic timing analysis are *single-history delay models*. In fact, since the delay for a given signal transition of a real gate is also dependent on the previous transition(s), in particular, when they are close, single-history delay models like [8–10] assume that the input-to-output delay $\delta(T)$ of a gate also depends on the previous-output-to-input delay T.

[1] In our context, the widely known pure and inertial delay models [6], which exhibit little to no history dependency, must be considered trivial.



(a) Thresholded hybrid model (b) Sample execution

Fig. 2. A digitized hybrid gate model (for a non-inverting buffer) satisfying the involution property and a sample execution. *Source:* Adapted from [10].

It has been proved by Függer et al. [8,10] that *continuity* is mandatory for any single-history model of a gate to faithfully represent the analog reality. Continuity ensures, for example, that a constant-low input signal and an arbitrarily short low-high-low pulse lead to very similar gate output signals. Note that this continuity property also implies continuity of the output signal power w.r.t. the input signal power, since the square of a signal is proportional to its power. Consequently, continuous delay models are the most promising candidates for the timing and power-accurate simulation of digital circuits [7].

So far, the only delay model that is known to ensure continuity is the *involution delay model* (IDM) [10], which consists of zero-time Boolean gates interconnected by single-input single-output involution delay channels. An IDM channel is characterized by a delay function δ that is a negative involution, i.e., $-\delta(-\delta(T)) = T$. In its generalized version, different delay functions $\delta_\uparrow$ resp. $\delta_\downarrow$ are assumed for rising resp. falling transitions, requiring $-\delta_\uparrow(-\delta_\downarrow(T)) = T$.

It has been shown already in [10] that involution delay functions arise naturally in the 2-state thresholded hybrid model illustrated in Fig. 2, which consists of a pure delay component, a slew-rate limiter with a rising and falling switching waveform, and an ideal comparator: The binary-valued input i_a is delayed by some $\delta_{\min} > 0$, which assures causality, i.e., $\delta_{\uparrow/\downarrow}(0) > 0$. At every transition of i_d, the slew-rate limiter switches to the corresponding waveform ($f_\downarrow/f_\uparrow$ for a falling/rising transition), thereby ensuring that the resulting analog output voltage o_a is a *continuous* (but not necessarily smooth) function of time. Finally, the comparator generates the output o_d by digitizing o_a w.r.t. the discretization threshold voltage V_{th}.

It is hence probably not too surprising that the involution property itself guarantees continuity also at the level of digital signals, which in turn is the key to proving that the IDM allows to solve the canonical *short-pulse filtration problem* (see Section 4.2) exactly as it is possible with real circuits. Note that the IDM also allows to incorporate substantial delay noise, PVT variations, and aging without compromising faithfulness [11,12].

The IDM also comes with a publicly available simulation framework, the *Involution Tool* [13], which allows to simulate circuits composed of gates for with an IDM model has been provided. It also facilitates the evaluation of the accuracy of IDM delay predictions against SPICE-generated data and other delay models. Whereas the accuracy of IDM predictions for single-input, single-output circuits like inverter chains or clock trees turned out to be very good [13], this is less so for circuits involving multi-input gates. It has been revealed by Ferdowsi et al. [14] that this is primarily due to the IDM's inherent inability to properly cover output delay variations caused by *multiple input switching* (MIS) effects, also known as *Charlie effects*, where different inputs switch in close temporal proximity [15]: compared to the *single input switching* (SIS) case, output transitions may be sped up/slowed down with decreasing transition separation time on different inputs. Since circuit models based on single-input, single-output delay channels like IDM inherently cannot model MIS effects, generalized delay models like the ones presented in Section 5 are needed for the accurate digital modeling of multi-input gates.

Detailed contributions.

(1) We show that any thresholded hybrid model, where mode m is governed by a system of first-order ODEs $\frac{dx}{dt} = F_m(t, x)$, leads to a continuous digital delay model, provided all the F_m are continuous in t and Lipschitz continuous in x, with a common Lipschitz constant for every $t > 0$ and m.
(2) We carry over our general continuity property to digitized hybrid gates.
(3) We prove that the parallel composition of finitely many digitized hybrid gates in a circuit result in a unique and Zeno-free execution, under some mild conditions regarding causality. Moreover, we prove that the resulting model is faithful w.r.t. solving the canonical short-pulse filtration problem, provided all involved digitized hybrid gates are continuous.
(4) We introduce the intricacies caused by MIS effects in multi-input gates, and show that the digitized hybrid model for CMOS NOR gates proposed in [14] is continuous.
(5) We revisit the advanced digitized hybrid model for CMOS NOR gates presented in [16], which covers all MIS effects. We prove that it is continuous, and derive an accurate approximation of its delay function based on explicit solutions of the underlying ODEs.[2]

[2] Note that the present paper actually combines and extends both the HSCC'23 paper [17] (where we presented our continuity proof) and the ICCAD'23 paper [16] (where we presented our advanced model for the NOR gate), with the important difference that we replace the complicated approximation of the ODE solutions used in [16] by the recently found explicit solutions, which results in much simpler and more accurate delay formulas and an explicit model parametrization procedure that avoids any fitting.

Paper organization. In Section 2, we instantiate our general continuity result (Theorem 6). Section 3 presents our main continuity results for digitized hybrid gates (Theorems 7 and 8), and Section 4 deals with circuit composition and faithfulness of composed models. In Section 5, we introduce MIS effects in multi-input gates and apply our continuity and faithfulness results to existing digitized hybrid models [10,14]. In Section 6, we provide our novel analysis of the advanced model introduced in [16]. Some conclusions are provided in Section 7.

2. Thresholded mode-switched ODEs

In this section, we provide a generic proof that every hybrid model that adheres to some mild conditions on its ODEs leads to a continuous digital delay model. We start with proving continuity in the analog domain and then establish continuity of the digitized signal obtained by feeding a continuous real-valued signal into a threshold voltage comparator. Combining those results will allow us to assert the continuity of digital delay channels like the one shown in Fig. 2.

2.1. Continuity of ODE mode switching

For a vector $x \in \mathbb{R}^n$, denote by $\|x\|$ its Euclidean norm. For a piecewise continuous function $f : [a,b] \to \mathbb{R}^n$, we write $\|f\|_1 = \int_a^b \|f(t)\|\,dt$ for its 1-norm and $\|f\|_\infty = \sup_{t\in[a,b]} \|f(t)\|$ for its supremum norm. The projection function of a vector in $\mathbb{R}^n$ onto its kth component, for $1 \le k \le n$, is denoted by $\pi_k : \mathbb{R}^n \to \mathbb{R}$.

In this section, we will consider non-autonomous first-order ODEs of the form $\frac{d}{dt}\,x(t) = f(t, x(t))$, where the non-negative $t \in \mathbb{R}_+$ represents the time parameter, $x(t) \in U$ for some arbitrary open set $U \subseteq \mathbb{R}^n$, $x_0 \in U$ is some initial value, and $f : \mathbb{R}_+ \times U \to \mathbb{R}^n$ is chosen from a set F of bounded functions that are continuous for $(t,x) \in [0,T] \times U$, where $0 < T < \infty$, and Lipschitz continuous in U with a common Lipschitz constant for all $t \in [0,T]$ and all choices of $f \in F$. It is well-known that every such ODE has a unique solution $x(t)$ with $x(0) = x_0$ that satisfies $x(t) \in U$ for $t \in [0,T]$, is continuous in $[0,T]$, and differentiable in $(0,T)$.

The following lemma shows the continuous dependence of the solutions of such ODEs on their initial values. To be more explicit, the exponential dependence of the Lipschitz constant on the time parameter allows temporal composition of the bound. The proof can be found in standard textbooks on ODEs [18, Theorem 2.8].

Lemma 1. *Let $U \subseteq \mathbb{R}^n$ be an open set and let $f : \mathbb{R} \times U \to \mathbb{R}^n$ be Lipschitz continuous with Lipschitz constant K for $t \in [0,T]$ with $T > 0$, and let $x, y : [0,T] \to U$ be continuous functions that are differentiable on $(0,T)$ such that $\frac{d}{dt}\,x(t) = f(t,x(t))$ and $\frac{d}{dt}\,y(t) = f(t,y(t))$ for all $t \in (0,T)$. Then, $\|x(t) - y(t)\| \le e^{tK}\|x(0) - y(0)\|$ for all $t \in [0,T]$.*

A *step function* $s : \mathbb{R}_+ \to \{0,1\}$ is a right-continuous function with left limits, i.e., $\lim_{t\to t_0^+} s(t) = s(t_0)$ and $\lim_{t\to t_0^-} s(t)$ exists for all $t_0 \in \mathbb{R}_+$. A *binary signal* s is a step function $s : [0,T] \to \{0,1\}$, a *mode-switch signal* a is a step function $a : [0,T] \to F$, $t \mapsto a_t$.

Given a mode-switch signal a, a *matching output signal* for a is a function $x_a : [0,T] \to U$ that satisfies

(i) $x_a(0) = x_0$,
(ii) the function x_a is continuous,
(iii) for all $t \in (0,T)$, if a is continuous at t, then x_a is differentiable at t and $\frac{d}{dt}\,x_a(t) = a_t(t, x_a(t))$.

For (iii), recall that the codomain of a is F.

Using an inductive argument, the following lemma establishes that, for any given mode-switch signal, there is a unique matching output signal, given as a continuous and differentiable function.

Lemma 2 (*Existence and Uniqueness of Matching Output Signal*)**.** *Given a mode-switch signal a, the matching output signal x_a for a exists and is unique.*

Proof. x_a can be constructed inductively, by pasting together the solutions x_{t_j} of $\frac{d}{dt}\,x_{t_j}(t) = a_{t_j}(t, x_{t_j}(t))$, where $t_0 = 0$ and $t_1 < t_2 < \dots$ are a's switching times in S_a: For the induction basis $j = 0$, we define $x_a(t) := x_{t_0}(t)$ with initial value $x_{t_0} = x_{t_0}(t_0) := x_0$ for $t \in [0,t_1]$. Obviously, (i) holds by construction, and the continuity and differentiability of $x_{t_0}(t)$ at other times ensures (ii) and (iii).

For the induction step $j \to j+1$, we assume that we have constructed $x_a(t)$ already for $0 \le t \le t_j$. For $t \in [t_j, t_{j+1}]$, we define $x_a(t) := x_{t_{j+1}}(t)$ with initial value $x_{t_{j+1}} = x_{t_{j+1}} := x_a(t_j) = x_{t_j}(t_j)$. Continuity of $x_a(t)$ at $t = t_j$ follows by construction, and the continuity and differentiability of $x_{t_{j+1}}(t)$ again ensures (ii) and (iii).

Finally, the uniqueness of x_a follows directly from the uniqueness of the solution of the underlying first-order Lipschitz-continuous ODE system $\frac{dx}{dt} = f(t,x)$ with the given initial condition. □

Given two mode-switch signals a, b, we define their distance as

$$d_T(a,b) = \lambda\big(\{t \in [0,T] \mid a_t \neq b_t\}\big) \tag{1}$$

where λ is the Lebesgue measure on $\mathbb{R}$. Obviously, the distance function d_T is a metric on the set of mode-switch signals.

The following Theorem 3 shows that the mapping $a \mapsto x_a$ is continuous. Note that it requires all the functions in F to satisfy a common Lipschitz constant. Albeit this clearly limits the applicability of our theorem, the examples in Sections 5 and 6 reveal that it is not an overly conservative assumption.

Theorem 3. *Let $K \geq 1$ be a common Lipschitz constant for all functions in F and let M be a real number such that $\|f(t, x(t))\| \leq M$ for all $f \in F$, all $x \in U$, and all $t \in [0, T]$. Then, for all mode-switch signals a and b, if x_a is the output signal for a and x_b is the output signal for b, then $\|x_a - x_b\|_\infty \leq 2Me^{TK} d_T(a, b)$. Consequently, the mapping $a \mapsto x_a$ is continuous.*

Proof. Let $S = \{t \in (0, T) \mid a \text{ or } b \text{ is discontinuous at } t\} \cup \{0, T\}$ be the set of switching times of a and b. The set S must be finite, since both a and b are right-continuous on a compact interval. Let $0 = s_0 < s_1 < s_2 < \cdots < s_m = T$ be the increasing enumeration of S.

We show by induction on k that

$$\forall t \in [0, s_k]: \quad \|x_a(t) - x_b(t)\| \leq 2Me^{tK} d_t(a, b) \tag{2}$$

for all $k \in \{0, 1, 2, \ldots, m\}$. The base case $k = 0$ is trivial. For the induction step $k \mapsto k + 1$, we distinguish the two cases $a_{s_k} = b_{s_k}$ and $a_{s_k} \neq b_{s_k}$.

If $a_{s_k} = b_{s_k}$, then we have $a_t = b_t$ for all $t \in [s_k, s_{k+1})$ and hence $d_t(a, b) = d_{s_k}(a, b)$ for all $t \in [s_k, s_{k+1}]$. Moreover, we can apply Lemma 1 and obtain

$$\forall t \in [s_k, s_{k+1}]: \quad \|x_a(t) - x_b(t)\| \leq e^{(t-s_k)K} \|x_a(s_k) - x_b(s_k)\| \ . \tag{3}$$

Plugging in (2) for $t = s_k$ reveals that (2) holds for all $t \in [s_k, s_{k+1}]$ as well.

If $a_{s_k} \neq b_{s_k}$, then x_a and x_b follow different differential equations in the interval $t \in [s_k, s_{k+1}]$. We can, however, use the mean-value theorem for vector-valued functions [19, Theorem 5.19] to obtain

$$\forall t \in [s_k, s_{k+1}]: \quad \|x_a(t) - x_a(s_k)\| \leq M(t - s_k) \text{ and} \tag{4}$$

$$\forall t \in [s_k, s_{k+1}]: \quad \|x_b(t) - x_b(s_k)\| \leq M(t - s_k). \tag{5}$$

This, combined with the induction hypothesis, the equality $d_t(a, b) = d_{s_k}(a, b) + (t - s_k)$, and the inequalities $1 \leq e^{tK}$ and $e^{s_k K} \leq e^{tK}$, implies

$$\begin{aligned}
\|x_a(t) - x_b(t)\| &\leq \|x_a(t) - x_a(s_k) + \|x_a(s_k) - x_b(s_k)\| + \|x_b(s_k) - x_b(t)\| \\
&\leq 2M(t - s_k) + 2Me^{s_k K} d_{s_k}(a, b) \\
&\leq 2Me^{tK}(t - s_k) + 2Me^{tK} d_{s_k}(a, b) \\
&= 2Me^{tK}\left(d_t(a, b) - d_{s_k}(a, b)\right) + 2Me^{tK} d_{s_k}(a, b) \\
&= 2Me^{tK} d_t(a, b)
\end{aligned}$$

for all $t \in [s_k, s_{k+1}]$. This concludes the proof. □

We remark that the (proof of the) continuity property of Theorem 3 is very different from the standard (proof of the) continuity property of controlled variables in closed thresholded hybrid systems. Mode switches in such systems are caused by the time evolution of the system itself, e.g., when some controlled variable exceeds some value. Consequently, such systems can be described by means of a *single* ODE system with discontinuous righthand side [20].

By contrast, in our hybrid systems, the mode switches are solely caused by changes of digital inputs that are *externally* controlled: For every possible pattern of the digital inputs, there is a dedicated ODE system that controls the analog output. Consequently, the time evolution of the output now also depends on the time evolution of the inputs. Proving the continuity of the (discretized) output w.r.t. different (but close, w.r.t. some metric) digital input signals require relating the output of *different* ODE systems. Therefore, our setting *cannot* be modeled as a single ODE system with discontinuous righthand side.

2.2. Continuity of thresholding

For a real number $\xi \in \mathbb{R}$ and a function $x : [a, b] \to \mathbb{R}$, denote by $\Theta_\xi(x)$ the thresholded version of x defined by

$$\Theta_\xi(x) : [a, b] \to \{0, 1\}, \quad \Theta_\xi(x)(t) = \begin{cases} 0 & \text{if } x(t) \leq \xi, \\ 1 & \text{if } x(t) > \xi. \end{cases} \tag{6}$$

In what follows, we prove that, under some mild conditions, the mapping $x \mapsto \Theta_\xi(x)$ is continuous.

Lemma 4. *Let $\xi \in \mathbb{R}$ and let $x : [a, b] \to \mathbb{R}$ be a continuous strictly monotonic function with $x(b) = \xi$. Then, for every $\varepsilon > 0$, there exists a $\delta > 0$ such that, for every continuous function $y : [a, b] \to \mathbb{R}$, the condition $\|x - y\|_\infty < \delta$ implies $\|\Theta_\xi(x) - \Theta_\xi(y)\|_1 < \varepsilon$.*

Proof. We show the lemma for the case that x is strictly increasing. The proof for strictly decreasing x is analogous.

Set $\chi = x(a)$. Since x is bijective onto the interval $[\chi, \xi]$, it has an inverse function $x^{-1} : [\chi, \xi] \to [a, b]$. The inverse function x^{-1} is continuous because the domain $[a, b]$ is compact [19, Theorem 4.17].

The relation $t \leq x^{-1}(\xi - \delta)$ implies $x(t) + \delta \leq \xi$. Hence, if $\|x - y\|_\infty < \delta$, then $y(t) \leq x(t) + \delta \leq \xi$ for all $t \leq x^{-1}(\xi - \delta)$. This means that $\Theta_\xi(y)(t) = 0$ for all $t \leq x^{-1}(\xi - \delta)$, so $t > x^{-1}(\xi - \delta)$ for every $t \in [a, b]$ where $\Theta_\xi(y)(t) = 1$.

By assumption, we have $\Theta_\xi(x)(t) = 0$ for all $t \in [a, b]$. Thus,

$$\|\Theta_\xi(x) - \Theta_\xi(y)\|_1 = \lambda\big(\{t \in [0,T] \mid \Theta_\xi(y) = 1\}\big) = \lambda\big(\{t \in [0,T] \mid y(t) > \xi\}\big) \le b - x^{-1}(\xi - \delta). \tag{7}$$

Note that continuity of y is sufficient to ensure that the set $\{t \in [0,T] \mid y(t) > \xi\}$ in Eq. (7) is measurable. Since x^{-1} is continuous, we have $x^{-1}(\xi - \delta) \to x^{-1}(\xi) = b$ as $\delta \to 0$. In particular, for every $\varepsilon > 0$, there exists a $\delta > 0$ such that $b - x^{-1}(\xi - \delta) < \varepsilon$. This concludes the proof. □

The following Lemma 5 shows that we can drop the assumption $x(b) = \xi$ in Lemma 4:

Lemma 5. *Let $\xi \in \mathbb{R}$ and let $x, y : [a, b] \to \mathbb{R}$ be two continuous functions where x is strictly monotonic. Then, for every $\varepsilon > 0$, there exists a $\delta > 0$ such that $\|x - y\|_\infty < \delta$ implies $\|\Theta_\xi(x) - \Theta_\xi(y)\|_1 < \varepsilon$. Moreover, if $\max\{x(a), x(b)\} \le \xi$ or $\min\{x(a), x(b)\} > \xi$, then $\|\Theta_\xi(x) - \Theta_\xi(y)\|_1 = 0$.*

Proof. We again show the lemma for the case that x is strictly increasing. The proof for strictly decreasing x is analogous.

Let $\varepsilon > 0$. We distinguish three cases:

(i) If $x(b) < \xi$, then we have $\Theta_\xi(x)(t) = 0$ for all $t \in [a, b]$. Choosing $\delta = \xi - x(b)$, we deduce $y(t) < x(t) + \delta \le x(b) + \xi - x(b) = \xi$ for all $t \in [a, b]$ whenever $\|x - y\|_\infty < \delta$. Hence, we get $\Theta_\xi(y)(t) = 0$ for all $t \in [a, b]$ and thus $\|\Theta_\xi(x) - \Theta_\xi(y)\|_1 = 0 < \varepsilon$.

(ii) If $x(a) > \xi$, then we can choose $\delta = x(a) - \xi$ and get $\Theta_\xi(y)(t) = \Theta_\xi(x)(t) = 1$ for all $t \in [a, b]$ whenever $\|x - y\|_\infty < \delta$. In particular, $\|\Theta_\xi(x) - \Theta_\xi(y)\|_1 = 0 < \varepsilon$.

(iii) If $x(a) \le \xi \le x(b)$, then there exists a unique $c \in [a, b]$ with $x(c) = \xi$. Applying Lemma 4 on the restriction of x on the interval $[a, c]$, we get the existence of a $\delta_1 > 0$ such that $\|x - y\|_{[a,c],\infty} < \delta_1$ implies $\|\Theta_\xi(x) - \Theta_\xi(y)\|_{[a,c],1} < \varepsilon/2$; herein, $\|\cdot\|_{[a,c],\infty}$ and $\|\cdot\|_{[a,c],1}$ denote the supremum-norm and the 1-norm on the interval $[a, c]$, respectively. Applying Lemma 4 on the restriction of x on the interval $[c, b]$ after the coordinate transformation $t \mapsto -t$ yields the existence of a $\delta_2 > 0$ such that $\|x - y\|_{[c,b],\infty} < \delta_2$ implies $\|\Theta_\xi(x) - \Theta_\xi(y)\|_{[c,b],1} < \varepsilon/2$. Setting $\delta = \min\{\delta_1, \delta_2\}$, we thus get $\|\Theta_\xi(x) - \Theta_\xi(y)\|_{[a,b],1} = \|\Theta_\xi(x) - \Theta_\xi(y)\|_{[a,c],1} + \|\Theta_\xi(x) - \Theta_\xi(y)\|_{[c,b],1} < \varepsilon/2 + \varepsilon/2 = \varepsilon$ whenever $\|x - y\|_{[a,b],\infty} < \delta$. □

The following Theorem 6 shows that the mapping $x \mapsto \Theta_\xi(x)$ is continuous for a given function x, provided that x has only finitely many alternating critical points, i.e., local optima that alternate between lying above and below ξ. Formally, these are times $t_0, t_1, \dots, t_M$ where $x'(t_j) = 0$ for all $0 \le j \le M$ and $\operatorname{sgn}\big(x(t_i) - \xi\big) = -\operatorname{sgn}\big(x(t_{i+1}) - \xi\big)$, for all $0 \le i \le M - 1$. Note carefully that we require M to be fixed and hence, in particular, independent of the choice of T here.

Theorem 6. *Let $\xi \in \mathbb{R}$ and let $x, y : [0,T] \to \mathbb{R}$ be two differentiable functions. Assume that x has at most $M < \infty$ alternating critical points, where M is independent of T. Then, for every $\varepsilon > 0$, there exists a $\delta > 0$ such that $\|x - y\|_\infty < \delta$ implies $\|\Theta_\xi(x) - \Theta_\xi(y)\|_1 < \varepsilon$. Consequently, the mapping $x \mapsto \Theta_\xi(x)$ is continuous.*

Proof. Let $\mathcal{N} = \{t \in [0,T] \mid x \text{ has a critical point at } t\} \cup \{0, T\}$, which contains only $m \le M$ alternating critical points by assumption, and $t_0 < t_1 < t_2 < \cdots < t_m$ be the increasing enumeration of $\mathcal{N}$. By the mean-value theorem, the function x is strictly monotonic in every interval $[t_k, t_{k+1}]$ for every $k \in \{0, 1, 2, \dots, m\}$.

Let $\varepsilon > 0$. Applying Lemma 5 to the restriction of x on each of the intervals $[t_k, t_{k+1}]$, we distinguish two cases: (i) if t_k, t_{k+1} are non-alternating critical points, then $\|\Theta_\xi(x) - \Theta_\xi(y)\|_{[t_k,t_{k+1}],1} = 0$. Otherwise, we are assured of the existence of some $\delta_k > 0$ such that $\|x - y\|_{[t_k,t_{k+1}],\infty} < \delta_k$ implies $\|\Theta_\xi(x) - \Theta_\xi(y)\|_{[t_k,t_{k+1}],1} < \varepsilon/m$. Setting $\delta = \min\{\delta_{k_0}, \delta_{k_1}, \delta_{k_2}, \dots, \delta_{k_{m-1}}\}$, we thus obtain

$$\|\Theta_\xi(x) - \Theta_\xi(y)\|_{[0,T],1} = \sum_{k=0}^{m-1} \|\Theta_\xi(x) - \Theta_\xi(y)\|_{[t_k,t_{k+1}],1} < \sum_{k=0}^{m-1} \varepsilon/m = \varepsilon, \tag{8}$$

whenever $\|x - y\|_{[0,T],\infty} < \delta$. □

3. Continuity of digitized hybrid gates

To prepare for our general result about the continuity of hybrid gate models (Theorem 8), we will first (re)prove the continuity of IDM channels as shown in Fig. 2, which has been established by a (somewhat tedious) direct proof in [10]. In our notation, an IDM channel consists of:

- A nonnegative minimum delay $\delta_{\min} \ge 0$ and a delay function $\Delta_{\delta_{\min}}(s)$ that maps the binary input signal i_a, augmented with the left-sided limit $i_a(0-)$ as the *initial value*[3] that can be different from $i_a(0)$, to the binary signal $i_d = \Delta_{\delta_{\min}}(i_a)$, defined by

$$\Delta_{\delta_{\min}}(i_a)(t) = \begin{cases} i_a(0-) & \text{if } t < \delta_{\min} \\ i_a(t - \delta_{\min}) & \text{if } t \ge \delta_{\min} \end{cases}. \tag{9}$$

[3] In [10], this initial value of a signal was encoded by extending the time domain to the whole $\mathbb{R}$ and using $i_a(-\infty)$.

- An open set $U \subseteq \mathbb{R}^n$, where $\pi_1[U]$ represents the analog output signal and $\pi_k[U]$, $k = \{2, 3, \dots, n\}$, specifies the internal state variables of the model. In this fashion,[4] we presume that $\pi_1[U] = (0, 1)$, i.e., the range of output signals is contained in the interval $(0, 1)$.
- Two bounded functions $F_\uparrow, F_\downarrow : \mathbb{R} \times U \to \mathbb{R}^n$ with the following properties:
  - $F_\uparrow, F_\downarrow$ are continuous for $(t, x) \in [0, T] \times U$, for any $0 < T < \infty$, and Lipschitz continuous in U, which entails that every trajectory x of the ODEs $\frac{d}{dt}\, x(t) = F_\uparrow(t, x(t))$ and $\frac{d}{dt}\, x(t) = F_\downarrow(t, x(t))$ with any initial value $x(0) \in U$ satisfies $x(t) \in U$ for all $t \in [0, T]$, recall Section 2.1.
  - for no trajectory x of the ODEs $\frac{d}{dt}\, x(t) = F_\uparrow(t, x(t))$ and $\frac{d}{dt}\, x(t) = F_\downarrow(t, x(t))$ with initial value $x(0) \in U$ does $\pi_1[x]$ have infinitely many alternating critical points $t_0, t_1, \dots$ with $\pi_1[x]'(t) = 0$ and $\operatorname{sgn}\big(\pi_1[x](t_i) - \xi\big) = -\operatorname{sgn}\big(\pi_1[x](t_{i+1}) - \xi\big)$, for all $i \geq 0$.
- An initial value $x_0 \in U$, with $x_0 = F_\uparrow$ if $i_a(0-) = 1$ and $x_0 = F_\downarrow$ if $i_a(0-) = 0$.
- A mode-switch signal $b : [0, T] \to \{F_\uparrow, F_\downarrow\}$ defined by setting $b(t) = F_\uparrow$ if $i_d(t) = 1$ and $b(t) = F_\downarrow$ if $i_d(t) = 0$.
- The analog output signal $o_a = \pi_1[x_b]$, i.e., the output signal for b and initial value x_0.
- A threshold voltage $\xi = V_{th} \in (0, 1)$ for the comparator that finally produces the binary output signal $o_d = \Theta_\xi(o_a)$.

By combining the results from Sections 2.1 and 2.2, we obtain the continuity of the channel function in a hybrid system mapping input signals to output signals stated in Theorem 7. It implies that small changes in the input signal lead to proportionally small changes in the output signal.

Theorem 7. *The channel function of an IDM channel, which maps from the input signal i_a to the output signal o_d, is continuous with respect to the 1-norm on the interval $[0, T]$.*

Proof. The mapping from i_a to o_d is continuous as the concatenation of continuous mappings:

- The mapping from $i_a \mapsto i_d$ is continuous since $\Delta_{\delta_{\min}}$ is trivially continuous for input and output binary signals with the 1-norm.
- The mapping $i_d \mapsto b$ is a continuous mapping from the set of signals equipped with the 1-norm to the set of mode-switch signals equipped with the metric d_T, since the points of discontinuity of b are the points where i_d is discontinuous.
- By Theorem 3, the mapping $b \mapsto x_b$ is a continuous mapping from the set of mode-switch signals equipped with the metric d_T to the set of piecewise differentiable functions $[0, T] \to U$ equipped with the supremum-norm.
- The mapping $x_b \mapsto \pi_1 \circ x_b$ is a continuous mapping from the set of piecewise differentiable functions $[0, T] \to U$ equipped with the supremum-norm to the set of piecewise differentiable functions $[0, T] \to (0, 1)$ equipped with the supremum-norm. Since $\|(x_1, \dots, x_n)\|_1 = \|x_1\|_1 + \cdots + \|x_n\|_1$ for every $x \in U$, this follows from $\|\pi_1[x]\|_1 \leq \|x\|_1$.
- By Theorem 6, the mapping $\pi_1 \circ x_b \mapsto \Theta_\xi(\pi_1 \circ x_b)$ is a continuous mapping from the set of piecewise differentiable functions $[0, T] \to (0, 1)$ equipped with the supremum-norm to the set of binary signals equipped with the 1-norm. □

Whereas the condition that no trajectory of any of the ODEs may have infinitely many alternating critical points is difficult to check in general, it is always guaranteed for every switching waveform $f(t)$ typically found in elementary[5] digitized hybrid gates. More specifically, as any f is meant to represent a digital signal here, it must satisfy either $\lim_{t\to\infty} f(t) = 0$ or $\lim_{t\to\infty} f(t) = 1$. Moreover, since real circuits cannot produce waveforms with arbitrary steep slopes, $|f'(t)|$ must be bounded. From the former, it follows that, for every $\varepsilon > 0$, there is some $t(\varepsilon)$ such that either $f(t) < \varepsilon$ or else $f(t) > 1 - \varepsilon$ for every $t \geq t(\varepsilon)$. Consequently, choosing $\varepsilon = \min\{V_{th}, 1 - V_{th}\}$ reveals that no alternating critical point $t \geq t(\varepsilon)$ can exist. Infinitely many alternating critical points for $t < t(\varepsilon)$ are prohibited by $|f'(t)|$ being bounded.

With these preparations, we can now deal with the general case: General digitized hybrid gates have $c \geq 1$ binary input signals $i_a = (i_a^1, \dots, i_a^c)$, augmented with *initial values* $(i_a^1(0-), \dots, i_a^c(0-))$, and a single binary output signal o_d, and are specified as follows:

Definition 1 (*Digitized Hybrid Gate*)**.** A digitized hybrid gate with c inputs consists of:

- c delay functions $\Delta_{\delta_j}(s)$ with $\delta_j \geq 0$, $1 \leq j \leq c$, that map the binary input signal i_a^j with initial value $i_a^j(0-)$ to the binary signal $i_d^j = \Delta_{\delta_j}(i_a^j)$, defined by
$$\Delta_{\delta_j}(i_a^j)(t) = \begin{cases} i_a^j(0-) & \text{if } t < \delta_j \\ i_a^j(t - \delta_j) & \text{if } t \geq \delta_j \end{cases}. \tag{10}$$
- An open set $U \subseteq \mathbb{R}^n$, where $\pi_1[U]$ represents the analog output signal and $\pi_k[U]$, $k = \{2, 3, \dots, n\}$, specifies the internal state variables of the model.

[4] In real circuits, the interval $(0, 1)$ typically needs to be replaced by $(0, V_{DD})$.

[5] This is true for all combinational gates like inverters, NOR, NAND etc. Excluded are gates with an internal state, like a storage element, which may exhibit *metastable behavior* [21,22].

- A set F of bounded functions $F^\ell : \mathbb{R} \times U \to \mathbb{R}^n$, with the following properties:
  - F^ℓ is continuous for $(t, x) \in [0, T] \times U$, for any $0 < T < \infty$, and Lipschitz continuous in U, with a common Lipschitz constant, which entails that every trajectory x of the ODE $\frac{d}{dt} x(t) = F^\ell(t, x(t))$ with any initial value $x(0) \in U$ satisfies $x(t) \in U$ for all $t \in [0, T]$.
  - for no trajectory x of the ODEs $\frac{d}{dt} x(t) = F^\ell(t, x(t))$ with initial value $x(0) \in U$ does $\pi_1[x]$ have infinitely many alternating critical points $t_0, t_1, \ldots$ with $\pi_1[x]'(t) = 0$ and $\operatorname{sgn}\big(\pi_1[x](t_i) - \xi\big) = -\operatorname{sgn}\big(\pi_1[x](t_{i+1}) - \xi\big)$, for all $i \geq 0$.
- A mode-switch signal $b : [0, T] \to F$, which obtained by a continuous choice function b_c acting on $i_d^1(t), \ldots, i_d^c(t)$, i.e., $b(t) = b_c(i_d^1(t), \ldots, i_d^c(t))$.
- An initial value $x_0 \in U$, which must correspond to the mode selected by $b_c(i_a^1(0-), \ldots, i_a^c(0-))$.
- The analog output signal $o_a = \pi_1[x_b]$, i.e., the output signal for b and initial value x_0.
- A threshold voltage $\xi = V_{th} \in (0, 1)$ for the comparator that finally produces the binary output signal $o_d = \Theta_\xi(o_a)$.

By essentially the same proof as for Theorem 7, we obtain:

Theorem 8. *The gate function of a digitized hybrid gate with c inputs according to Definition 1, which maps from the vector of input signals $i_a = (i_a^1, \ldots, i_a^c)$ to the output signal o_d, is continuous with respect to the 1-norm on the interval $[0, T]$.*

4. Composing gates in circuits

In this section, we will first compose digital circuits from digitized hybrid gates and reason about their executions. More specifically, it will turn out that, under certain conditions ensuring the causality of every composed gate, the resulting circuit will exhibit a unique execution for any given execution of its inputs. This uniqueness is mandatory for building digital dynamic timing simulation tools.

Moreover, we will adapt the proof that no circuit with IDM channels can solve the bounded SPF problem utilized in [10] to our setting: Using the continuity result of Theorem 8, we prove that no circuit with digitized hybrid gates can solve bounded SPF. Since unbounded SPF can be solved with IDM channels, which are simple instances of digitized hybrid gate models, faithfulness w.r.t. solving the SPF problem follows.

4.1. Executions of circuits

Circuits. Circuits are obtained by interconnecting a set of input ports and a set of output ports, forming the external interface of a circuit, and a finite set of digitized hybrid gates. We constrain the way components are interconnected in a natural way, by requiring that any gate input, channel input and output port is attached to only one input port, gate output or channel output, respectively. Formally, a *circuit* is described by a directed graph where:

(C1) A vertex Γ can be either a *circuit input port*, a *circuit output port*, or a digitized hybrid *gate*.
(C2) The *edge* (Γ, I, Γ') represents a 0-delay connection from the output of Γ to a fixed input I of Γ'.
(C3) Circuit input ports have no incoming edges.
(C4) Circuit output ports have exactly one incoming edge and no outgoing one.
(C5) A c-ary gate G has a single output and c inputs $I_1, \ldots, I_c$, in a fixed order, fed by incoming edges from exactly one gate output or input port.

Executions. An *execution* of a circuit C is a collection of binary signals s_Γ defined on $[0, \infty)$ for all vertices Γ of C that respects all the gate functions and input port signals. Formally, the following properties must hold:

(E1) If i is a circuit input port, there are no restrictions on s_i.
(E2) If o is a circuit output port, then $s_o = s_G$, where G is the unique gate output connected to o.
(E3) If vertex G is a gate with c inputs $I_1, \ldots, I_c$, ordered according to the fixed order condition C5), and gate function f_G, then $s_G = f_G(s_{\Gamma_1}, \ldots, s_{\Gamma_c})$, where $\Gamma_1, \ldots, \Gamma_c$ are the vertices the inputs $I_1, \ldots, I_c$ of C are connected to via edges $(\Gamma_1, I_1, G), \cdots, (\Gamma_d, I_c, G)$.

The above definition of an execution of a circuit is "existential", in the sense that it only allows checking for a given collection of signals whether it is an execution or not: For every hybrid gate in the circuit, it specifies the gate output signal, given a *fixed* vector of input signals, all defined on the time domain $t \in [0, \infty)$. A priori, this does not give an algorithm to construct executions of circuits, in particular, when they contain feedback loops. Indeed, the parallel composition of general hybrid automata may lead to non-unique executions and bizarre timing behaviors known as *Zeno*, where an infinite number of transitions may occur in finite time [23].

To avoid such behaviors in our setting, we require all digitized hybrid gates in a circuit to be *strictly causal*:

Definition 2 (*Strict Causality*)**.** A digitized hybrid gate G with c inputs is strictly causal, if the pure delays δ_j for every $1 \leq j \leq c$ are positive. Let $\delta_{\min}^C > 0$ be the minimal pure delay of any input of any gate in circuit C.

We proceed with defining input–output causality for gates, which is based on signal transitions. Every binary signal can equivalently be described by a sequence of transitions: A *falling transition* at time t is the pair $(t, 0)$, a *rising transition* at time t is the pair $(t, 1)$.

Definition 3 (*Input–output Causality*)**.** The output transition $(t, .) \in s_G$ of a gate G *is caused* by the transition $(t', .) \in s_G^j$ on input I_j of G, if $(t, .)$ occurs in the mode $a_c(i_d^1(t^+), \ldots, i_d^c(t^+))$, where $i_d^j(t^+)$ is the pure-delay shifted input signal at input I_j at the last mode switching time $t^+ \le t$ (see Eq. 1) and $(t', .)$ is the last transition in s_G^j before or at time $t^+ - \delta_j$, i.e., $\nexists (t'', .) \in s_G^j$ for $t' < t'' \le t^+ - \delta_j$.

We also assume that the output transition $(t, .) \in s_G$ *causally depends* on every transition in s_G^j before or at time $t^+ - \delta_j$.

Strictly causal gates satisfy the following obvious property:

Lemma 9. *If some output transition $(t, .) \in s_G$ of a strictly causal digitized hybrid gate G in a circuit C causally depends on its input transition $(t', .) \in s_G^j$, then $t - t' \ge \delta_j$.*

The following Theorem 4.1 shows that every circuit made up of strictly causal gates has a unique execution, defined for $t \in [0, \infty)$.

Theorem 4.1 (*Unique Execution*)**.** *Every circuit C made up of finitely many strictly causal digitized hybrid gates has a unique execution, which either consists of finitely many transitions only or else requires $[0, \infty)$ as its time domain.*

Proof. We will inductively construct this unique execution by a sequence of iterations $\ell \ge 1$ of a simple deterministic simulation algorithm, which determines the prefix of the sought execution up to time t_ℓ. Iteration ℓ deals with transitions occurring at time t_ℓ, starting with $t_1 = 0$. To every transition e generated throughout its iterations, we also assign a *causal depth* $d(e)$ that gives the maximum causal distance to an input port: $d(e) = 0$ if e is a transition at some input port, and $d(e)$ is the maximum of $1 + d(e^j)$, $1 \le j \le c$, for every transition added at the output of a c-ary gate caused by transitions e^j at its inputs.

Induction basis $\ell = 1$: At the beginning of iteration 1, which deals with all transitions occurring at time $t_1 = 0$, all gates are in their initial mode, which is determined by the initial values of their inputs. They are either connected to input ports, in which case $s_i(0-)$ is used, or to the output port of some gate G, in which case $s_G(0)$ (determined by the initial mode of G) is used. Depending on whether $s_i(0-) = s_i(0)$ or not, there is also an input transition $(0, s_i(0)) \in s_i$ or not. All transitions in the so generated execution prefix $[0, t_1] = [0, 0]$ have a causal depth of 0.

Still, the transitions that have happened by time t_1 may cause additional *potential future transitions*. They are called future transitions, because they occur only after t_1, and potential because they need not occur in the final execution. In particular, if there is an input transition $(0, s_i(0)) \in s_i$, it may cause a mode switch of every gate G that is connected to the input port i. Due to Lemma 9, however, such a mode switch, and hence each of the output transitions e that may occur during that new mode (which all are assigned a causal depth $d(e) = 1$), of G can only happen at or after time $t_1 + \delta_{\min}^C$. In addition, the initial mode of any gate G that is not mode switched may also cause output transitions e at arbitrary times $t > 0$, which are assigned a causal depth $d(e) = 0$. Since at most finitely many critical points may exist for every mode's trajectory, it follows that at most *finitely* many such future potential transitions could be generated in each of the finitely many gates in the circuit. Let $t_2 > t_1$ denote the time of the closest transition among all input port transitions and all the potential future transitions just introduced.

Induction step $\ell \to \ell + 1$: Assume that the execution prefix for $[0, t_\ell]$ has already been constructed in iterations $1, \ldots, \ell$, with at most finitely many potential future transitions occurring after t_ℓ. If the latter set is empty, then the execution of the circuit has already been determined completely. Otherwise, let $t_{\ell+1} > t_\ell$ be the closest future transition time.

During iteration $\ell+1$, all transitions occurring at time $t_{\ell+1}$ are dealt with, exactly as in the base case: Any transition e, with causal depth $d(e)$, happening at $t_{\ell+1}$ at a gate output or at some input port may cause a mode switch of every gate G that is connected to it. Due to Lemma 9, such a mode switch, and hence each of the at most finitely many output transitions e' occurring during that new mode (which all are assigned a causal depth $d(e') = d(e) + 1$), of G can only happen at or after time $t_{\ell+1} + \delta_{\min}^C$. In addition, the at most finitely many potential future transitions w.r.t. t_ℓ of all gates that have not been mode-switched and actually occur at times greater than $t_{\ell+1}$ are retained, along with their assigned causal depth, as potential future transitions w.r.t. $t_{\ell+1}$. Overall, we again end up with at most finitely many potential future transitions, which completes the induction step.

To complete our proof, we only need to argue that $\lim_{\ell \to \infty} t_\ell = \infty$ for the case where the iterations do not stop at some finite ℓ. This follows immediately from the fact that, for every $k \ge 1$, there must be some iteration $\ell \ge 1$ such that $t_\ell \ge k\delta_{\min}^C$. If this was not the case, there must be some iteration after which no further mode switch of any gate takes place. This would cause the set of potential future transitions to shrink in every subsequent iteration, however, and thus the simulation algorithm to stop, which provides the required contradiction. □

From the execution construction, we also immediately get:

Lemma 10. *For all $\ell \ge 1$, (a) the simulation algorithm never assigns a causal depth larger than ℓ to a transition generated in iteration ℓ, and (b) at the end of iteration ℓ the sequence of causal depths of transitions in s_Γ for $t \in [0, t_\ell]$ is nondecreasing for all components Γ.*

4.2. Impossibility of short-pulse filtration

The results of the previous subsection allow us to adapt the impossibility proof of [10] to our setting. We start with the definition of the SPF problem:

Short-Pulse Filtration. A signal *contains a pulse* of length Δ at time T_0, if it contains a rising transition at time T_0, a falling transition at time $T_0 + \Delta$, and no transition in between. The *zero signal* has the initial value 0 and does not contain any transition. A circuit *solves Short-Pulse Filtration (SPF)*, if it fulfills all of:

(F1) The circuit has exactly one input port and exactly one output port. *(Well-formedness)*
(F2) If the input signal is the zero signal, then so is the output signal. *(No generation)*
(F3) There exists an input pulse such that the output signal is not the zero signal. *(Nontriviality)*
(F4) There exists an $\varepsilon > 0$ such that for every input pulse the output signal never contains a pulse of length less than or equal to ε. *(No short pulses)*

We allow the circuit to behave arbitrarily if the input signal is not a single pulse or the zero signal.

A circuit *solves bounded SPF* if additionally:

(F5) There exists a $K > 0$ such that for every input pulse the last output transition is before time $T_0 + \Delta + K$, where T_0 is the time of the first input transition. *(Bounded stabilization time)*

A circuit is called a *forward circuit* if its graph is acyclic. Forward circuits are exactly those circuits that do not contain feedback loops. Equipped with the continuity of digitized hybrid gates and the fact that the composition of continuous functions is continuous, it is not too difficult to prove that the inherently discontinuous SPF problem cannot be solved with forward circuits.

Theorem 4.2. *No forward circuit solves bounded SPF.*

Proof. Suppose that there exists a forward circuit that solves bounded SPF with stabilization time bound K. Denote by s_Δ its output signal when feeding it a Δ-pulse at time 0 as the input. Because s_Δ in forward circuits is a finite composition of continuous functions by Theorem 8, $\|s_\Delta\|_{[0,T],1}$ depends continuously on Δ, for any T.

By the nontriviality condition (F3) of the SPF problem, there exists some Δ_0 such that s_{Δ_0} is not the zero signal. Set $T = 2\Delta_0 + K$.

Let $\varepsilon > 0$ be smaller than both Δ_0 and $\|s_{\Delta_0}\|_{[0,T],1}$. We show a contradiction by finding some Δ such that s_Δ either contains a pulse of length less than ε (contradiction to the no short pulses condition (F4)) or contains a transition after time $\Delta + K$ (contradicting the bounded stabilization time condition (F5)).

Since $\|s_\Delta\|_{[0,T],1} \to 0$ as $\Delta \to 0$ by the no generation condition (F2) of SPF, there exists a $\Delta_1 < \Delta_0$ such that $\|s_{\Delta_1}\|_{[0,T],1} = \varepsilon$ by the intermediate value property of continuity. By the bounded stabilization time condition (F5), there are no transitions in s_{Δ_1} after time $\Delta_1 + K$. Hence, s_{Δ_1} is 0 after this time because otherwise it is 1 for the remaining duration $T - (\Delta_1 + K) > \Delta_0 > \varepsilon$, which would mean that $\|s_{\Delta_1}\|_{[0,T],1} > \varepsilon$. Consequently, there exists a pulse in s_{Δ_1} before time $\Delta_1 + K$. But any such pulse is of length at most ε because $\|s_{\Delta_1}\|_{[0,\Delta_1+K],1} \leq \|s_{\Delta_1}\|_{[0,T],1} = \varepsilon$. This is a contradiction to the no short pulses condition (F4). □

We next show how to simulate (part of) an execution of an arbitrary circuit C by a forward circuit C' generated from C by the unrolling of feedback loops. Intuitively, the deeper the unrolling, the longer the time C' behaves as C.

Definition 4. Let C be a circuit, V a vertex of C, and $k \geq 0$. We define the *k-unrolling of C from V*, denoted by $C_k(V)$, to be a directed acyclic graph with a single sink, constructed as follows:

The unrolling $C_k(I)$ from input port I is just a copy of that input port. The unrolling $C_k(O)$ from output port O with incoming channel C and predecessor V comprises a copy of the output port $O^{(k)}$ and the unrolled circuit $C_k(V)$ with its sink connected to $O^{(k)}$ by an edge.

The 0-unrolling $C_0(B)$ from hybrid gate B is a trivial Boolean gate X_v without inputs and the constant output value v equal to B's initial digitized output value. For $k > 0$, the k-unrolling $C_k(B)$ from gate B comprises an exact copy of that gate $B^{(k)}$. Additionally, for every incoming edge of B from V in C, it contains the circuit $C_{k-1}(V)$ with its sink connected to $B^{(k)}$. Note that all copies of the same input port are considered to be the same.

To each component Γ in $C_k(V)$, we assign a value $z(\Gamma) \in \mathbb{N}_0 \cup \{\infty\}$ as follows: $z(\Gamma) = \infty$ if Γ has no predecessor (in particular, is an input port) and $\Gamma \notin \{X_0, X_1\}$. Moreover, $z(X_0) = z(X_1) = 0$, $z(V) = z(U)$ if V is an output port connected by an edge to U, and $z(B) = \min_{c \in E^B}\{1 + z(c)\}$ if B is a gate with its inputs connected to the components in the set E^B. Fig. 3 shows an example of a circuit and an unrolled circuit with its z values.

Noting that, for every component Γ in $C_k(V)$, $z(\Gamma)$ is the number of gates on the shortest path from an X_v node to Γ, or $z(\Gamma) = \infty$ if no such path exists, we immediately get:

Lemma 11. *The z-value assigned to the sink vertex $V^{(k)}$ of a k-unrolling $C_k(V)$ of C from V satisfies $z(V^{(k)}) \geq k$.*

Recalling the causal depths assigned to transitions during the execution construction in Theorem 4.1, we are now in the position to prove the result for a circuit simulated by an unrolled circuit.

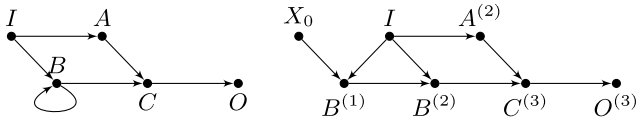


Fig. 3. Circuit C (left) and $C_3(O)$ (right) under the assumption that the gate B has initial value 0. It is $z(X_0) = 0$, $z(I) = z(A^{(2)}) = \infty$, $z(B^{(1)}) = 1$, $z(B^{(2)}) = 2$, $z(C^{(3)}) = 3$, and $z(O^{(3)}) = 3$.

Theorem 4.3. *Let C be a circuit with input port I and output port O that solves bounded SPF. Let $C_k(O)$ be an unrolling of C, Γ a component in C, and Γ' a copy of Γ in $C_k(O)$. For all input signals s_I on I, if a transition e is generated for Γ by the execution construction algorithm run on circuit C with input signal s_I and $d(e) \le z(\Gamma')$, then e is also generated for Γ' by the algorithm run on circuit $C_k(O)$ with input signal s_I; and vice versa.*

Proof. Assume that e is the first transition violating the theorem. The input signal is the same for both circuits, and the initial digitized values of gates in C and both their copies in $C_k(O)$ and the X_v gates resulting from their 0-unrolling are equal as well. Hence, e cannot be any such transition (added in iteration 1 only).

If e was added to the output of a gate B in either circuit, the transition e' resp. e'' at one of its inputs that caused e in C resp. $C_k(V)$ must have been different. These transitions e' resp. e'' must come from the output of some other gate B_1, and causally precede e. Hence, by Definition 3, $d(e) = d(e')+1$, and by Lemma 10, $d(e) \ge d(e'')$. Also by definition, $z(B) = z(B_1)+1$ in $C_k(O)$. Since $d(e) \le z(B)$ by assumption, we find $d(e') \le z(B_1)$ and $d(e'') \le z(B)$, so applying our theorem to e' and e'' yields a contradiction to e being the first violating transition. □

We can finally prove that bounded SPF is not solvable, even with non-forward circuits.

Theorem 4.4. *No circuit solves bounded SPF.*

Proof. We first note that the impossibility of bounded SPF also implies the impossibility of bounded SPF when restricting pulse lengths to be at most some $\Delta_0 > 0$.

Since all transitions generated in the execution construction Theorem 4.1 up to any bounded time t_ℓ have bounded causal depth, let ζ be an upper bound on the causal depth of transitions up to the SPF stabilization time bound $\Delta_0 + K$. Then, by Theorem 4.3 and Lemma 11, the ζ-unrolled circuit $C_\zeta(O)$ has the same output transitions as the original circuit C up to time $\Delta_0 + K$, and hence, by definition of bounded SPF, the same transitions for all times. But since $C_\zeta(O)$ is a forward circuit, it cannot solve bounded SPF by Theorem 4.2, i.e., neither can C. □

5. Digitized hybrid models for multi-input gates

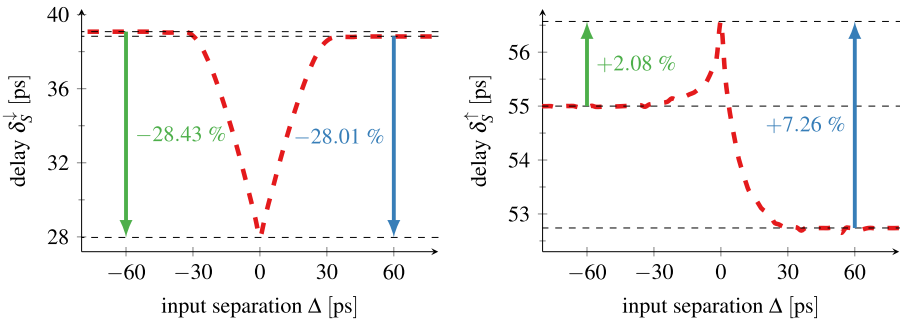
In this section, we will apply the results obtained in the previous section to circuits composed of digitized hybrid gates. For a warm-up, we will effortlessly re-prove the already known fact that every digitized hybrid gate model obtained by appending resp. prepending an IDM *exp-channel* with pure delay $\delta_{\min} > 0$ at the output of resp. at every input of any zero-time Boolean gate is continuous and strictly causal. Consequently, according to Section 4, the resulting IDM circuit model is faithful w.r.t. solving the SPF problem.

An exp-channel, as introduced in [10], is just the two-state digitized hybrid model illustrated in Fig. 2 instantiated with exponential switching waveforms $f_\downarrow(t) = 1 - f_\uparrow(t) = e^{-t/\tau}$ for some time constant $\tau > 0$. Obviously, these are the trajectories of a simple first-order RC low-pass filter. The ODEs governing $y = f_\downarrow(t)$ resp. $y = f_\uparrow$ are $y' + y/\tau = 0$ resp. $y' + y/\tau = 1/\tau$, so $F_\downarrow(t, y) = -y/\tau$ resp. $F_\uparrow(t, y) = (1-y)/\tau$ is of course Lipschitz-continuous. An exp-channel hence satisfies the conditions of Theorem 7 and is hence continuous and, due to the assumption $\delta_{\min} > 0$, also strictly causal according to Definition 2. Since zero-time Boolean gates that alternate with IDM channels can neither affect continuity nor causality of the latter, this completes our proof.

5.1. Modeling multi-input switching effects

As already mentioned in Section 1, experiments in [13] showed that the prediction accuracy of the above IDM circuit model for multi-input gates is below expectations. As revealed by Ferdowsi et al. [14], this is primarily due to the fact that a model of a multi-input gate that combines single-input single-output IDM channels with zero-time Boolean gates cannot properly capture output delay variations caused by *multiple input switching* (MIS) effects: output transitions may be sped up/slowed down when different inputs switch in close temporal proximity [15].

Consider the CMOS implementation of a NOR gate shown in Fig. 6(a), for example, which consists of two serial pMOS (T_1 and T_2) for charging the load capacitance C (producing a rising output transition), and two parallel nMOS transistors (T_3 and T_4) for discharging it (producing a falling one). When an input experiences a rising transition, the corresponding nMOS transistor closes while the corresponding pMOS transistor opens, so C will be discharged. If both inputs A and B experience a rising transition at



(a) Rising input delay (b) Falling input delay

Fig. 4. MIS effects in the measured delay of a 15 nm technology CMOS NOR gate.

the same time, C is discharged twice as fast. Since the gate delay depends on the discharging speed, it follows that the delay $\delta_S^{\downarrow}(\Delta)$ increases (by almost 30% in the example shown in Fig. 4(a)) when the *input separation time* $\Delta = t_B - t_A$ increases from 0 to ∞ or decreases from 0 to $-\infty$. For falling input transitions, the behavior of the NOR gate is quite different: Fig. 4(b) shows that the MIS effects lead to a moderate decrease of $\delta_S^{\uparrow}(\Delta)$ when $|\Delta|$ goes from 0 to ∞, which is primarily caused by capacitive coupling.

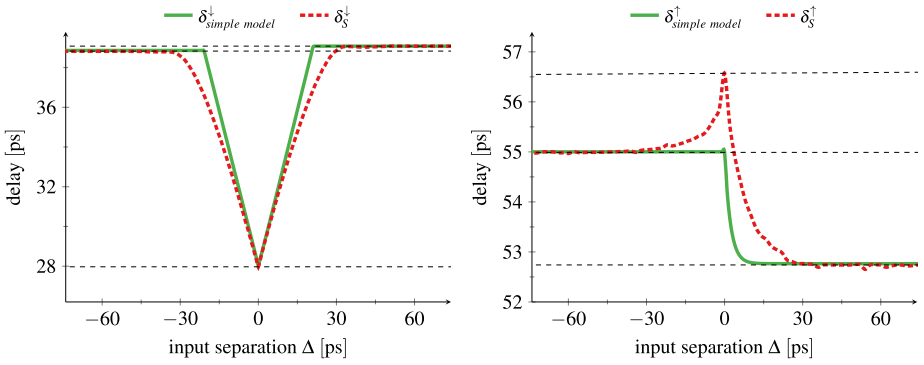
MIS effects have of course been studied in the digital circuit modeling literature in the past, with approaches ranging from linear [24] or quadratic [25] fitting over higher-dimensional macromodels [26] and model representations [27] to recent machine learning methods [28]. However, the resulting models are either empirical or statistical and, hence, have not been analyzed w.r.t. continuity. Whether they admit a faithful digital circuit model or not is hence unknown.

5.2. A simple digitized hybrid model for a CMOS NOR gate

To the best of our knowledge, the first attempt to develop a delay model that captures MIS effects and can be analyzed w.r.t. continuity has been provided in [14]. It is a 4-state digitized hybrid model for a CMOS NOR gate, with one mode per possible digital state of the inputs $(A, B) \in \{(0,0),(0,1),(1,0),(1,1)\}$, which has been obtained by replacing the four transistors in Fig. 6(a) by ideal zero-time switches with non-zero resistance, and adding another capacitance C_N to the node N between the two pMOS transistors T_1 and T_2. In each mode, the voltage of the output signal O and the internal node N are governed by a system of constant-coefficient first-order ODEs as follows:

- System $(1,1)$: $V_A = 1$, $V_B = 1$: If inputs A and B are 1, both nMOS transistors are conducting and thus replaced by resistors, causing the output O to be discharged in parallel. By contrast, N is completely isolated and keeps its value. This leads to the following ODEs:
$$\begin{pmatrix} \frac{\mathrm{d}}{\mathrm{d}t} V_{int}(t) \\ \frac{\mathrm{d}}{\mathrm{d}t} V_{out}(t) \end{pmatrix} = \begin{pmatrix} F_1(V_{int}(t), V_{out}(t)) \\ F_2(V_{int}(t), V_{out}(t)) \end{pmatrix} = \begin{pmatrix} 0 \\ -\left(\frac{1}{CR_3} + \frac{1}{CR_4}\right) V_{out}(t) \end{pmatrix}$$
- System $(1,0)$: $V_A = 1$, $V_B = 0$: Since T_1 and T_4 are open, node N is connected to O, and O to GND. Both capacitors have to be discharged over resistor R_3, resulting in less current that is available for discharging C. One obtains:
$$\begin{pmatrix} \frac{\mathrm{d}}{\mathrm{d}t} V_{int}(t) \\ \frac{\mathrm{d}}{\mathrm{d}t} V_{out}(t) \end{pmatrix} = \begin{pmatrix} F_3(V_{int}(t), V_{out}(t)) \\ F_4(V_{int}(t), V_{out}(t)) \end{pmatrix} = \begin{pmatrix} -\frac{V_{int}(t)}{C_{int} R_2} + \frac{V_{out}(t)}{C_{int} R_2} \\ \frac{V_{int}(t)}{CR_2} - \left(\frac{1}{CR_2} + \frac{1}{CR_3}\right) V_{out}(t) \end{pmatrix}$$
- System $(0,1)$: $V_A = 0$, $V_B = 1$: Opening transistors T_2 and T_3 again decouples the nodes N and O. We thus get
$$\begin{pmatrix} \frac{\mathrm{d}}{\mathrm{d}t} V_{int}(t) \\ \frac{\mathrm{d}}{\mathrm{d}t} V_{out}(t) \end{pmatrix} = \begin{pmatrix} F_5(V_{int}(t), V_{out}(t)) \\ F_6(V_{int}(t), V_{out}(t)) \end{pmatrix} = \begin{pmatrix} -\frac{V_{int}(t)}{C_{int} R_1} + \frac{V_{DD}}{C_{int} R_1} \\ -\frac{V_{out}(t)}{CR_4} \end{pmatrix}$$
- System $(0,0)$: $V_A = 0$, $V_B = 0$: Closing both pMOS transistors causes both capacitors to be charged over the same resistor R_1, similarly to system $(1,0)$. Thus
$$\begin{pmatrix} \frac{\mathrm{d}}{\mathrm{d}t} V_{int}(t) \\ \frac{\mathrm{d}}{\mathrm{d}t} V_{out}(t) \end{pmatrix} = \begin{pmatrix} F_7(V_{int}(t), V_{out}(t)) \\ F_8(V_{int}(t), V_{out}(t)) \end{pmatrix} = \begin{pmatrix} -\left(\frac{1}{C_{int}(t) R_1} + \frac{1}{C_{int}(t) R_2}\right) V_{int} + \frac{V_{out}(t)}{C_{int} R_2} + \frac{V_{DD}}{C_{int} R_1} \\ \frac{V_{int}(t)}{CR_2} - \frac{V_{out}(t)}{CR_2} \end{pmatrix}$$

Every F_i, $i \in \{1, \ldots, 8\}$, is a mapping from $U = (0,1)^2 \subseteq \mathbb{R}^2$ to $\mathbb{R}$, whereat U is the vector of the voltages at the nodes N and O. Solving the above ODEs provides analytic expressions for these voltage trajectories, which can even be inverted to obtain the relevant gate delays. As it turned out in [14], although the model perfectly covers the MIS effects in the case of rising input



(a) Rising input transition (b) Falling input transition

Fig. 5. Comparison of the measured delay $\delta_S^{\downarrow/\uparrow}(\Delta)$ of a real 15 nm CMOS NOR gate (red dashed line) and the delay prediction of the simple digitized hybrid model (green line) from [14]. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

transitions (Fig. 5(a)) , it unfortunately fails to do so for falling input (= rising output) transitions (Fig. 5(b)).

Nevertheless, using Theorem 8, we can show that the model of [14] is continuous:

Theorem 5.1. *For any $i \in \{1, \ldots, 8\}$, F_i of the simple digitized hybrid model is Lipschitz continuous.*

Proof. Since the proof is straightforward, we elaborate it only for F_7; similar arguments apply to the other cases. Let $K = max\{(\frac{1}{C_{int}R_1} + \frac{1}{C_{int}R_2}), \frac{1}{C_{int}R_2}\}$. For any voltages V^1_{int}, V^2_{int}, V^1_{out}, and V^2_{out} in $(0, 1)$, we find

$$\left|F_7(V^1_{int}, V^1_{out}) - F_7(V^2_{int}, V^2_{out})\right| = \left| -\left(\frac{1}{C_{int}R_1} + \frac{1}{C_{int}R_2}\right)(V^1_{int} - V^2_{int}) + \frac{1}{C_{int}R_2}\left(V^1_{out} - V^2_{out}\right)\right| \tag{11}$$

$$\leq K\left|(V^1_{int} - V^2_{int}) + (V^1_{out} - V^2_{out})\right|. \quad \square \tag{12}$$

Consequently, we can instantiate Definition 1 with

$$b_c(i^A_d, i^B_d) = \begin{cases} \begin{pmatrix} F_1(V_{int}(t), V_{out}(t)) \\ F_2(V_{int}(t), V_{out}(t)) \end{pmatrix} & (i^A_d, i^B_d) = (1,1) \\ \begin{pmatrix} F_3(V_{int}(t), V_{out}(t)) \\ F_4(V_{int}(t), V_{out}(t)) \end{pmatrix} & (i^A_d, i^B_d) = (1,0) \\ \begin{pmatrix} F_5(V_{int}(t), V_{out}(t)) \\ F_6(V_{int}(t), V_{out}(t)) \end{pmatrix} & (i^A_d, i^B_d) = (0,1) \\ \begin{pmatrix} F_7(V_{int}(t), V_{out}(t)) \\ F_8(V_{int}(t), V_{out}(t)) \end{pmatrix} & (i^A_d, i^B_d) = (0,0) \end{cases}$$

such that the model is continuous by Theorem 8.

6. An advanced digitized hybrid model for a CMOS NOR gate

In an attempt to mitigate the inability of the simple digitized hybrid model for a CMOR NOR gate proposed in [14] to cover the MIS effect for falling input (= rising output) transitions (recall Fig. 5(b)), Ferdowsi, Schmid, and Salzmann developed an advanced model originally presented in [16]. Whereas this model indeed accomplishes its purpose, its analysis is based on a complicated piecewise approximation (in terms of Δ) of both the ODE solutions and, in particular, the corresponding delay formulas. This not only impairs the utility of the results for determining delays of compound circuits, both for simulation-based and analytical studies, but also caused the model parametrization, which is based on fitting, to partially compensate for the approximation error by obtaining inexact parameters.

In this section, we will provide an entirely novel analysis of the digitized hybrid model proposed in [16], which has been enabled by the recent discovery of an explicit expression for the ODE solution. It not only leads to more accurate delay formulas, but also to an explicit model parametrization procedure that avoids any fitting.

The advanced digitized hybrid model for a 2-input CMOS NOR gate introduced in [16] is built upon replacing the transistors in Fig. 6(a) by time-varying resistors: The values $R_i(t)$, $i \in \{1, \ldots, 4\}$ in the resulting Fig. 6(b) vary between some fixed on-resistance R_i and the off-resistance ∞ according to some laws, which we will introduce below. The law to be used is determined by the state of the particular input signal that drives the gate of the corresponding transistor. This construction results in a hybrid model with

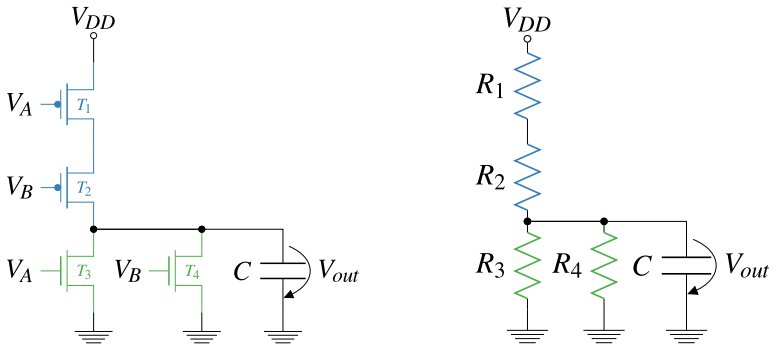


Fig. 6. Schematics and resistor model of a CMOS NOR gate.

Table 1
State transitions and modes. ↑ and ↑↑ (resp. ↓ and ↓↓) represent the first and the second rising (resp. falling) input transitions. + and − specify the sign of the switching time difference $\Delta = t_B - t_A$.

Mode	Transition	t_A	t_B	R_1	R_2	R_3	R_4
$T_-^{\uparrow}$	$(0,0) \to (1,0)$	0	$-\infty$	$on \to off$	on	$off \to on$	off
$T_+^{\uparrow\uparrow}$	$(1,0) \to (1,1)$	$-\lvert\Delta\rvert$	0	off	$on \to off$	on	$off \to on$
$T_+^{\uparrow}$	$(0,0) \to (0,1)$	$-\infty$	0	on	$on \to off$	off	$off \to on$
$T_-^{\uparrow\uparrow}$	$(0,1) \to (1,1)$	0	$-\lvert\Delta\rvert$	$on \to off$	off	$off \to on$	on
$T_-^{\downarrow}$	$(1,1) \to (0,1)$	0	$-\infty$	$off \to on$	off	$on \to off$	on
$T_+^{\downarrow\downarrow}$	$(0,1) \to (0,0)$	$-\lvert\Delta\rvert$	0	on	$off \to on$	off	$on \to off$
$T_+^{\downarrow}$	$(1,1) \to (1,0)$	$-\infty$	0	off	$off \to on$	on	$on \to off$
$T_-^{\downarrow\downarrow}$	$(1,0) \to (0,0)$	0	$-\lvert\Delta\rvert$	$off \to on$	on	$on \to off$	off

4 different modes, which correspond to the 4 possible input states $(A, B) \in \{(0,0), (0,1), (1,0), (1,1)\}$.

Table 1 shows all possible input state transitions and the corresponding resistor time evolution mode switches. Double arrows in the mode switch names indicate MIS-relevant modes, whereas + and − indicate whether input A switched before B or the other way round. For instance, assume the system is in state $(0,0)$ initially, i.e., that both A and B were set to 0 at time $t_A = t_B = -\infty$. This causes R_1 and R_2 to be in the *on-mode*, whereas R_3 and R_4 are in the *off-mode*. Now assume that at time $t_A = 0$, A is switched to 1. This switches R_1 resp. R_3 to the *off-mode* resp. *on-mode* at time $t_1^{off} = t_3^{on} = t_A = 0$. The corresponding mode switch is $T_-^{\uparrow}$ and reaches state $(1,0)$. Now assume that B is also switched to 1, at some time $t_B = \Delta > 0$. This causes R_2 resp. R_4 to switch to *off-mode* resp. *on-mode* at time $t_2^{off} = t_4^{on} = t_B = \Delta$. The corresponding mode switch is $T_+^{\uparrow\uparrow}$ and reaches state $(1,1)$; note carefully that the delay is Δ-dependent and hence MIS-relevant.

Crucial for the model is choosing a suitable law for the time evolution of $R_i(t)$ in the *on-* and *off-mode*, which should facilitate an analytic solution of the resulting ODE systems (15) while being reasonably close to the physical behavior of a transistor. The simple Shichman–Hodges transistor model [29] is used here, which states a quadratic dependence of the output current on the input voltage. Approximating the latter by $d\sqrt{t - t_0}$ in the operation range close to the threshold voltage V_{th}, with d and t_0 some fitting parameters, leads to the *continuous resistance model*

$$R_j^{on}(t) = \frac{\alpha_j}{t - t^{on}} + R_j;\ t \geq t^{on}, \tag{13}$$

$$R_j^{off}(t) = \beta_j(t - t^{off}) + R_j;\ t \geq t^{off}, \tag{14}$$

for some constant slope parameters α_j [Ω s], β_j [Ω/s], and on-resistance R_j [Ω]. t^{on} resp. t^{off} represent the time when the respective transistor is switched on resp. off.

Actually, it was found in [16] that continuously changing resistors, according to (13), are only required for switching-on the pMOS transistors in Fig. 6(a). All other resistors can be immediately switched on/off (in zero-time), as already employed in [14]. Note that immediate switching is obtained by setting $\alpha_j = 0$ and $\beta_j = \infty$ in (13) and (14). Subsequently, we will use the notation $R_1 = R_{p_A}$, $R_2 = R_{p_B}$ with the abbreviation $2R = R_{p_A} + R_{p_B}$ for the two pMOS transistors T_1 and T_2, and $R_3 = R_{n_A}$, $R_4 = R_{n_B}$ for the two nMOS transistors T_3 and T_4.

Another pivotal question is how to incorporate $R_1(t), \ldots, R_4(t)$ in the ODEs of the modes. The arguably most intuitive idea is to incorporate those in the state of the ODE of every mode, and switch between them continuously upon a mode switch. This "full-state model" would lead to ODE systems with a 5-dimensional state (output voltage V_{out} and the 4 resistors), however, which rules out finding analytic solutions.

Therefore, in [16], these resistors were incorporated in the *coefficients* of a simple first-order ODE obtained by applying Kirchhoff's rules to Fig. 6(b). Doing this results in the non-autonomous, non-homogeneous ordinary differential equation (ODE)

Table 2
$F(t, V_{out}(t))$ for each state transition.

State transition	$F(t, V_{out}(t))$
$(0,0) \to (1,0)$	$F_1(t, V_{out}(t)) \doteq \frac{-V_{out}(t)}{C R_{n_A}}$
$(1,1) \to (1,0)$	$F_1(t, V_{out}(t)) \doteq \frac{-V_{out}(t)}{C R_{n_A}}$
$(0,1) \to (1,0)$	$F_1(t, V_{out}(t)) \doteq \frac{-V_{out}(t)}{C R_{n_A}}$
$(0,0) \to (0,1)$	$F_2(t, V_{out}(t)) \doteq \frac{-V_{out}(t)}{C R_{n_B}}$
$(1,1) \to (0,1)$	$F_2(t, V_{out}(t)) \doteq \frac{-V_{out}(t)}{C R_{n_B}}$
$(1,0) \to (0,1)$	$F_2(t, V_{out}(t)) \doteq \frac{-V_{out}(t)}{C R_{n_B}}$
$(1,0) \to (0,0)$	$F_3(t, V_{out}(t)) \doteq \frac{\left(-V_{out}(t)+V_{DD}\right)}{C(\frac{\alpha_1}{t}+\frac{\alpha_2}{t+\Delta}+2R)}$
$(0,1) \to (0,0)$	$F_4(t, V_{out}(t)) \doteq \frac{\left(-V_{out}(t)+V_{DD}\right)}{C(\frac{\alpha_1}{t+\Delta}+\frac{\alpha_2}{t}+2R)}$
$(1,1) \to (0,0)$	$F_5(t, V_{out}(t)) \doteq \frac{\left(-V_{out}(t)+V_{DD}\right)t}{C(2Rt+\alpha_1+\alpha_2)}$
$(1,0) \to (1,1)$	$F_6(t, V_{out}(t)) \doteq \frac{-V_{out}(t)}{C}(\frac{1}{R_{n_A}}+\frac{1}{R_{n_B}})$
$(0,1) \to (1,1)$	$F_6(t, V_{out}(t)) \doteq \frac{-V_{out}(t)}{C}(\frac{1}{R_{n_A}}+\frac{1}{R_{n_B}})$
$(0,0) \to (1,1)$	$F_6(t, V_{out}(t)) \doteq \frac{-V_{out}(t)}{C}(\frac{1}{R_{n_A}}+\frac{1}{R_{n_B}})$

with non-constant coefficients $C\frac{\mathrm{d}V_{out}}{\mathrm{d}t} = \frac{V_{DD}-V_{out}}{R_1(t)+R_2(t)} - \frac{V_{out}}{R_3(t) \parallel R_4(t)}$, which can be transformed into

$$\frac{\mathrm{d}V_{out}}{\mathrm{d}t} = F(t, V_{out}(t)) = -\frac{V_{out}}{C\, R_g(t)} + U(t), \tag{15}$$

where $\frac{1}{R_g(t)} = \frac{1}{R_1(t)+R_2(t)} + \frac{1}{R_3(t)} + \frac{1}{R_4(t)}$ and $U(t) = \frac{V_{DD}}{C(R_1(t)+R_2(t))}$. Note that the entire voltage divider in Fig. 6(b) is equivalent to an ideal voltage source $U_0 = V_{DD}\frac{R_3(t)\|R_4(t)}{R_1(t)+R_2(t)+R_3(t)\|R_4(t)}$ and a serial resistor $R_g(t)$ sourcing C. Consequently, $CU(t) = U_0/R_g(t)$ in (15) is the short-circuit current, and $CU(t) - V_{out}/R_g(t)$ the current actually sourced into C.

6.1. Continuity of the model

In order to prove the continuity of the resulting digitized hybrid model, via Theorem 8, we need to verify some properties of the functions $F(t, V_{out}(t))$ arising in the ODE (15). Note carefully that, depending the current mode, different expressions for $R_g(t)$, $U(t)$ determine the function F governing this mode. In fact, F may even depend on the actual mode switch, i.e., also the previous mode. Table 2 summarizes the functions $F_1, \dots, F_6$ associated with each possible input transition; unlike in Table 1, we also consider state transitions where both inputs are changed simultaneously. Due to some symmetry, we end up with only six different functions.

For instance, to determine F_5 corresponding to the transition $(1,1) \to (0,0)$, we assume that the system is in mode $(1,1)$ initially (i.e., at time $t = -\infty$) and transitions to $(0,0)$ at time $t = 0$. Consequently, R_1 and R_2, previously in the *off-mode*, switch to the *on-mode*, while R_3 and R_4 switch from *on-mode* to *off-mode*. Formally, this transition results in $R_{p_A}(t) = \frac{\alpha_1}{t} + R_1$, $R_{p_B}(t) = \frac{\alpha_2}{t} + R_2$, and $R_{n_A}(t) = R_{n_B}(t) = \infty$, collectively leading to $1/R_g(t) = t/(2Rt + \alpha_1 + \alpha_2)$ since $R_1 + R_2 = 2R$. As a result, we obtain $F_5(t, V_{out}(t)) = -\frac{V_{out}}{C\, R_g(t)} + U(t) = \frac{(-V_{out}(t)+V_{DD})t}{C(2Rt+\alpha_1+\alpha_2)}$. The other cases can be obtained similarly.

The following theorem paves the way for verifying the continuity property of the model, by guaranteeing the properties required in Definition 1:

Theorem 6.1. *Let $F = \{F_1, \dots, F_6 : \mathbb{R} \times (0,1) \to \mathbb{R}\}$ be the set of all functions described in Table 2. Every $F_i \in F$, where $i \in \{1, \dots, 6\}$, is continuous for $t \in [0,T]$, $0 < T < \infty$, $V_{out} \in (0,1)$, and Lipschitz continuous w.r.t. V_{out}.*

Proof. The statement is immediate for functions F_1, F_2, and F_6. For F_5, let $g(t) = \frac{t}{C(2Rt+\alpha_1+\alpha_2)}$. Since $t \in [0,T]$, $g(t)$ takes its supremum value in the interval, which we denote by K (i.e., $sup_{t\in[0,T]} g(t) = K$). We observe

$$\left|F_5(t, V^1_{out}) - F_5(t, V^2_{out})\right| = \left|\frac{(-V^1_{out}+V_{DD})t}{C(2Rt+\alpha_1+\alpha_2)} - \frac{(-V^2_{out}+V_{DD})t}{C(2Rt+\alpha_1+\alpha_2)}\right|$$
$$= \left|\frac{-t}{C(2Rt+\alpha_1+\alpha_2)} \cdot (V^1_{out} - V^2_{out})\right| \le |K|\left|V^1_{out} - V^2_{out}\right|,$$

which concludes the proof for F_5. The proof for F_3 and F_4 follows the same route; we only sketch the proof for F_3: We observe

$$\left|F_3(t, V^1_{out}) - F_3(t, V^2_{out})\right| = \left|\frac{-(V^1_{out} - V^2_{out})}{\frac{\alpha_1}{t+\Delta} + \frac{\alpha_2}{t} + 2R}\right|.$$

Since we can safely assume that both t and $t + \Delta$ belong to the closed interval $[0,T]$, by choosing T appropriately, we obviously get some Lipschitz constant L that is independent of t. Consequently,

$$\left|F_3(t, V^1_{out}) - F_3(t, V^2_{out})\right| \le L \cdot \left|\left(V^1_{out} - V^2_{out}\right)\right|,$$

which completes the proof. □

Table 3
Integrals $I_1(t)$, $I_2(t)$, $I_3(t)$ and the function $U(t)$ for every possible mode switch; $\Delta = t_B - t_A$, and $2R = R_{p_A} + R_{p_B}$.

Mode	$I_1(t) = \int_0^t \frac{\mathrm{d}s}{R_1(s)+R_2(s)}$	$I_2(t) = \int_0^t \frac{\mathrm{d}s}{R_3(s)}$	$I_3(t) = \int_0^t \frac{\mathrm{d}s}{R_4(s)}$	$U(t) = \frac{V_{DD}}{C(R_1(t)+R_2(t))}$
$T_-^{\uparrow}$	0	$\int_0^t (1/R_{n_A})\mathrm{d}s$	0	0
$T_+^{\uparrow\uparrow}$	0	$\int_0^t (1/R_{n_A})\mathrm{d}s$	$\int_0^t (1/R_{n_B})\mathrm{d}s$	0
$T_+^{\uparrow}$	0	0	$\int_0^t (1/(R_{n_B})\mathrm{d}s$	0
$T_-^{\uparrow\uparrow}$	0	$\int_0^t (1/R_{n_A})\mathrm{d}s$	$\int_0^t (1/R_{n_B})\mathrm{d}s$	0
$T_-^{\downarrow}$	0	0	$\int_0^t (1/R_{n_B})\mathrm{d}s$	0
$T_+^{\downarrow\downarrow}$	$\int_0^t (1/(\frac{\alpha_1}{s+\Delta} + \frac{\alpha_2}{s} + 2R))\mathrm{d}s$	0	0	$\frac{V_{DD}t(t+\Delta)}{C(2Rt^2+(\alpha_1+\alpha_2+2\Delta R)t+\alpha_2\Delta)}$
$T_+^{\downarrow}$	0	$\int_0^t (1/(R_{n_A})\mathrm{d}s$	0	0
$T_-^{\downarrow\downarrow}$	$\int_0^t (1/(\frac{\alpha_1}{s} + \frac{\alpha_2}{s+\lvert\Delta\rvert} + 2R))\mathrm{d}s$	0	0	$\frac{V_{DD}t(t+\lvert\Delta\rvert)}{C(2Rt^2+(\alpha_1+\alpha_2+2\lvert\Delta\rvert R)t+\alpha_1\lvert\Delta\rvert)}$

According to Theorem 6.1, by defining $s(t) = (i_d^A(t^+), i_d^B(t^+))$ and $s_p(t) = (i_d^A(t), i_d^B(t))$, we can instantiate Definition 1 by the choice function

$$b_c(s(t)) = \begin{cases} F_1(t, V_{out}(t)) & s(t) = (1,0) \\ F_2(t, V_{out}(t)) & s(t) = (0,1) \\ F_3(t, V_{out}(t)) & s(t) = (0,0), s_p(t) = (1,0) \\ F_4(t, V_{out}(t)) & s(t) = (0,0), s_p(t) = (0,1) \\ F_5(t, V_{out}(t)) & s(t) = (0,0), s_p(t) = (1,1) \\ F_6(t, V_{out}(t)) & s(t) = (1,1) \end{cases}$$

which, according to (15) and Table 2, results in

$$\frac{dV_{out}(t)}{dt} = \begin{cases} \frac{-V_{out}(t)}{CR_{n_A}} & s(t) = (1,0) \\ \frac{-V_{out}(t)}{CR_{n_B}} & s(t) = (0,1) \\ \frac{\left(-V_{out}(t)+V_{DD}\right)t(t+\Delta)}{C\left(2Rt^2+(\alpha_1+\alpha_2+2\Delta R)t+\alpha_1\Delta\right)} & s(t) = (0,0), s_p(t) = (1,0) \\ \frac{\left(-V_{out}(t)+V_{DD}\right)t(t+\Delta)}{C\left(2Rt^2+(\alpha_1+\alpha_2+2\Delta R)t+\alpha_2\Delta\right)} & s(t) = (0,0), s_p(t) = (0,1) \\ \frac{\left(-V_{out}(t)+V_{DD}\right)t}{C(2Rt+\alpha_1+\alpha_2)} & s(t) = (0,0), s_p(t) = (1,1) \\ \frac{-V_{out}(t)}{C}\left(\frac{1}{R_{n_A}} + \frac{1}{R_{n_B}}\right) & s(t) = (1,1). \end{cases}$$

Since all the conditions in Definition 1 are satisfied, Theorem 8 indeed guarantees continuity of the model.

6.2. Analytic solutions for the output voltage trajectories

We now turn our attention to the ability of our model to cover all MIS effects illustrated in Fig. 4. Since gate delays are just the time it takes for the output voltage trajectory to reach the threshold voltage, this subsection is devoted to determining explicit analytic expressions for $V_{out}^{MS}(t)$ for each mode switch MS listed in Table 1.

It is well-known that the general solution of (15) is

$$V_{out}(t) = V_0\, e^{-G(t)} + \int_0^t U(s)\, e^{G(s)-G(t)}\mathrm{d}s, \tag{16}$$

where $V_0 = V_{out}(0)$ denotes the initial condition and $G(t) = \int_0^t (C\, R_g(s))^{-1}\mathrm{d}s$.

As already mentioned, $R_g(t)$ and $U(t)$ depend on the particular mode, recall Table 2. It turns out that computing $G(t)$ for each mode requires the solution of three different integrals $I_1 = \int_0^t \frac{\mathrm{d}s}{R_1(s)+R_2(s)}$, $I_2 = \int_0^t \frac{\mathrm{d}s}{R_3(s)}$, and $I_3(t) = \int_0^t \frac{\mathrm{d}s}{R_4(s)}$. Table 3 lists these integrals as well as the value $U(t)$ for each mode.

Fortunately, a closer look at Table 1 and Table 3 shows a certain symmetry between the pairs of modes $(T_-^{\uparrow}, T_+^{\uparrow})$, $(T_+^{\uparrow\uparrow}, T_-^{\uparrow\uparrow})$, $(T_-^{\downarrow}, T_+^{\downarrow})$, and $(T_+^{\downarrow\downarrow}, T_-^{\downarrow\downarrow})$. Therefore, it is sufficient to derive analytic expressions for the case $\Delta \geq 0$ only. The corresponding formulas for $\Delta < 0$ can be obtained from those by exchanging α_1 and α_2, as well as R_{n_A} and R_{n_B}.

To proceed, we split the discussions into two parts, one devoted to rising input transitions (= falling output transitions) and one to falling input transitions (= rising output transitions). We start with the (simpler) former one.

6.2.1. Rising input transitions

In this part, we analyze the output voltage trajectories related to rising input transitions. The following theorem elaborates on this.

Theorem 6.2 (*Output Trajectories for Rising Input Transitions*). *For any $0 \leq |\Delta| \leq \infty$, the voltage output trajectory functions of our model for rising input transitions are given by:*

$$V_{out}^{T_-^{\uparrow}}(t) = V_{out}^{T_-^{\uparrow}}(0)e^{\frac{-t}{CR_{n_A}}} \tag{17}$$

$$V_{out}^{T_+^{\uparrow}}(t) = V_{out}^{T_+^{\uparrow}}(0)e^{\frac{-t}{CR_{n_B}}} \tag{18}$$

$$V_{out}^{T_+^{\uparrow\uparrow}}(t) = V_{out}^{T_-^{\uparrow}}(\Delta)e^{-\left(\frac{1}{CR_{n_A}}+\frac{1}{CR_{n_B}}\right)t} \tag{19}$$

$$V_{out}^{T_-^{\uparrow\uparrow}}(t) = V_{out}^{T_+^{\uparrow}}(\Delta)e^{-\left(\frac{1}{CR_{n_A}}+\frac{1}{CR_{n_B}}\right)t} \tag{20}$$

Proof. In order to compute $V_{out}^{T_-^{\uparrow}}(t)$, consider the corresponding integrals $I_1(t)$, $I_2(t)$, and $I_3(t)$, as well as $U(t)$ in the first line of Table 3. Since we assumed immediate resistor switching here, we have $\beta_1 = \beta_2 = \infty$ and $\alpha_3 = \alpha_4 = 0$, so that

$$I_1(t) = I_3(t) = U(t) = 0, \qquad I_2(t) = \frac{t}{R_{n_A}}.$$

Since $G(t) = (I_1(t) + I_2(t) + I_3(t))/C$, we get $e^{\pm G(t)} = e^{\frac{\pm t}{CR_{n_A}}}$ and $\int_0^t e^{G(s)}U(s)ds = 0$. With $V_0^{\uparrow} = V_{out}^{T_-^{\uparrow}}(0)$ as our initial value, (16) finally provides

$$V_{out}^{T_-^{\uparrow}}(t) = V_{out}^{T_-^{\uparrow}}(0)e^{\frac{-t}{CR_{nA}}}.$$

Similarly, for the mode $T_+^{\uparrow\uparrow}$, we obtain

$$I_1(t) = U(t) = 0, \qquad I_2(t) = \frac{t}{R_{n_A}}, \qquad I_3(t) = \frac{t}{R_{n_B}},$$

such that $e^{\pm G(t)} = e^{\pm(\frac{1}{CR_{n_A}}+\frac{1}{CR_{n_B}})t}$ and $\int_0^t e^{G(s)}U(s)ds = 0$. Consequently, we obtain

$$V_{out}^{T_+^{\uparrow\uparrow}}(t) = V_{out}^{T_-^{\uparrow}}(\Delta)e^{-\left(\frac{1}{CR_{n_A}}+\frac{1}{CR_{n_B}}\right)t},$$

where the initial value $V_{out}^{T_-^{\uparrow}}(\Delta)$ can be computed via (17).

Due to our symmetry argument, exchanging R_{n_A} and R_{n_B} immediately provides the trajectories (20) and (18) for negative Δ. □

6.2.2. *Falling input transitions*

In this case, we first need to compute $V_{out}^{T_-^{\downarrow}}(t)$. Again plugging the immediate switching parameters $\beta_1 = \beta_2 = \infty$ and $\alpha_3 = \alpha_4 = 0$ in the corresponding expressions in Table 3 provides $I_1(t) = I_2(t) = U(t) = 0$ and $I_3(t) = \frac{t}{R_{n_B}}$. With $V_0^{\downarrow} = V_{out}^{T_-^{\downarrow}}(0)$ as our initial condition, (16) yields

$$V_{out}^{T_-^{\downarrow}}(t) = V_{out}^{T_-^{\downarrow}}(0)e^{\frac{-t}{CR_{n_B}}}. \tag{21}$$

Turning our attention to $V_{out}^{T_+^{\downarrow\downarrow}}(t)$ in Table 3, we are confronted with a more intricate case: Whereas $I_2(t) = I_3(t) = 0$ again, evaluating $I_1(t)$ requires us to study the function $f(s) = \frac{1}{\frac{\alpha_1}{s+\Delta}+\frac{\alpha_2}{s}+2R}$, as

$$I_1(t) = \int_0^t f(s)ds, \qquad G(t) = I_1(t)/C, \tag{22}$$

$$\int_0^t e^{G(s)}U(s)ds = \frac{V_{DD}}{C}\int_0^t e^{\frac{I_1(s)}{C}}f(s)ds. \tag{23}$$

It is not difficult to check that $\frac{V_{DD}}{C}\int_0^t e^{\frac{I_1(s)}{C}}f(s)ds = V_{DD}(e^{\frac{I_1(t)}{C}} - 1)$, which according to (16) leads to

$$V_{out}^{T_+^{\downarrow\downarrow}}(t) = (V_{out}^{T_-^{\downarrow}}(\Delta) - V_{DD})e^{-I_1(t)/C} + V_{DD}, \tag{24}$$

where $V_{out}^{T_-^{\downarrow}}(\Delta)$ gives the initial value.

In order to compute an explicit formula for the voltage trajectory from (24), we need to evaluate $e^{-I_1(t)/C}$. To simplify our derivations, we write $f(s) = \frac{1-g(s)}{2R}$, where $g(s) = \frac{as+c'}{s^2+ds+c'}$ and

$$a = \frac{\alpha_1 + \alpha_2}{2R}, \tag{25}$$

$$d = a + \Delta, \tag{26}$$

$$c' = \frac{\alpha_2\Delta}{2R}, \tag{27}$$

$$\chi = d^2 - 4c' = (a+\Delta)^2 - \frac{2\alpha_2\Delta}{R}. \tag{28}$$

With this, $I_1(t) = \frac{1}{2R}(t - \int_0^t g(s)ds)$. The following lemma reveals that the denominator of g possesses two rational zeros, which will make it easy to compute $\int_0^t g(s)ds$ after a simple partial fraction decomposition.

Lemma 12. *$s^2+ds+c' = 0$ has two rational roots $s_1 = \frac{-d+\sqrt{\chi}}{2}$ and $s_2 = \frac{-d-\sqrt{\chi}}{2}$, which satisfy $s_1 s_2 = c'$, $s_1+s_2 = -d$, and $s_2 - s_1 = -\sqrt{\chi}$.*

Proof. It is apparent that $s_{1,2} = \frac{-d\pm\sqrt{\chi}}{2} = \frac{a+\Delta}{2}(-1 + \sqrt{1 - \frac{4b\Delta}{(a+\Delta)^2}})$, where $b = \alpha_2/(2R)$, are the two zeros of $s^2 + ds + c' = 0$. These zeros are rational if and only if $1 - \frac{4b\Delta}{(a+\Delta)^2} \geq 0$, i.e., if and only if

$$\Delta^2 + (2a - 4b)\Delta + a^2 \geq 0. \tag{29}$$

Clearly, (29) has two complex zeros $\Delta_{1,2} = \frac{(\alpha_2-\alpha_1)\pm\sqrt{-4\alpha_1\alpha_2}}{2R}$ since α_1, α_2, and R are all positive. Therefore, (29) cannot become negative for any Δ, since it is positive for $\Delta = 0$. Consequently, s_1 and s_2 are rational, and satisfy $s_1 s_2 = c'$ and $s_1 + s_2 = -d$ by Vieta's theorem. □

The following theorem provides the sought explicit expression for $I_1(t) = \frac{1}{2R}\left(t - \int_0^t g(s)ds\right)$:

Lemma 13. *Let s_1 and s_2 denote the two rational zeros of $s^2 + ds + c' = 0$, and define*

$$A = \frac{-as_1 - c'}{s_2 - s_1} = \frac{a\frac{d-\sqrt{\chi}}{2} - \frac{\alpha_2\Delta}{2R}}{-\sqrt{\chi}}. \tag{30}$$

Then,

$$I_1(t) = \frac{1}{2R}\left[t + (A-a)\cdot\log\left(1 + \frac{2t}{d+\sqrt{\chi}}\right) - A\cdot\log\left(1 + \frac{2t}{d-\sqrt{\chi}}\right)\right]. \tag{31}$$

Proof. Utilizing partial fraction decomposition and recalling $s_1 s_2 = c'$ and $s_1 + s_2 = -d$ from Lemma 12 gives us $g(s) = \frac{as+c'}{s^2+ds+c'} = \frac{A}{(s-s_1)} + \frac{a-A}{(s-s_2)}$, for A as defined in Eq. (30), which leads to

$$\begin{aligned}
\int g(s)ds &= A\int \frac{ds}{s-s_1} + (a-A)\int \frac{ds}{s-s_2} \\
&= A\cdot\log(s-s_1) + (a-A)\cdot\log(s-s_2) + K \\
&= A\cdot\log\left(s - \frac{-d+\sqrt{\chi}}{2}\right) + (a-A)\cdot\log\left(s - \frac{-d-\sqrt{\chi}}{2}\right) + K \\
&= (a-A)\cdot\log\left(s + \frac{d+\sqrt{\chi}}{2}\right) + A\cdot\log\left(s + \frac{d-\sqrt{\chi}}{2}\right) + K,
\end{aligned}$$

where K is some constant. Plugging in the boundaries, elementary calculations finally yield

$$\begin{aligned}
&I_1(t) = \int_0^t f(s)ds = \int_0^t \frac{1-g(s)}{2R}ds = \\
&\frac{1}{2R}\left[t + (A-a)\cdot\log\left(1 + \frac{2t}{d+\sqrt{\chi}}\right) - A\cdot\log\left(1 + \frac{2t}{d-\sqrt{\chi}}\right)\right]
\end{aligned} \tag{32}$$

as asserted. □

With these preparations, we are now ready to state the major theorem of this subsection:

Theorem 6.3 (*Output Trajectories for Falling Input Transitions*). *For any $0 \leq |\Delta| \leq \infty$, the voltage output trajectory functions of our model for input falling transitions are given by:*

$$V_{out}^{T_-^{\downarrow}}(t) = V_{out}^{T_-^{\downarrow}}(0)e^{\frac{-t}{CR_{n_B}}} \tag{33}$$

$$V_{out}^{T_+^{\downarrow}}(t) = V_{out}^{T_+^{\downarrow}}(0)e^{\frac{-t}{CR_{n_A}}} \tag{34}$$

$$\begin{aligned}
V_{out}^{T_+^{\downarrow\downarrow}}(t) &= V_{DD} \\
&+ \left(V_{out}^{T_-^{\downarrow}}(\Delta) - V_{DD}\right)\left[e^{\frac{-t}{2RC}}\left(1 + \frac{2t}{d+\sqrt{\chi}}\right)^{\frac{-A+a}{2RC}}\left(1 + \frac{2t}{d-\sqrt{\chi}}\right)^{\frac{A}{2RC}}\right]
\end{aligned} \tag{35}$$

$$\begin{aligned}
V_{out}^{T_-^{\downarrow\downarrow}}(t) &= V_{DD} \\
&+ \left(V_{out}^{T_+^{\downarrow}}(|\Delta|) - V_{DD}\right)\left[e^{\frac{-t}{2RC}}\left(1 + \frac{2t}{d+\sqrt{\chi}}\right)^{\frac{-A+a}{2RC}}\left(1 + \frac{2t}{d-\sqrt{\chi}}\right)^{\frac{A}{2RC}}\right]
\end{aligned} \tag{36}$$

Proof. The trajectory Eq. (33) has been established in Eq. (21) already, Eq. (34) follows from our symmetry argument by exchanging R_{n_B} with R_{n_A}.

Plugging in $I_1(t)$ in (32) into (24), we immediately obtain the expression for the output trajectory $V_{out}^{T_+^{\downarrow\downarrow}}(t)$ starting from the initial value $V_{out}^{T_-^{\downarrow}}(\Delta)$ given in Eq. (21). Due to our symmetry, the trajectory formula (36) for negative values of Δ is obtained by exchanging α_1 with α_2 in χ and A, and $V_{out}^{T_-^{\downarrow}}(\Delta)$ with $V_{out}^{T_+^{\downarrow}}(|\Delta|)$ in (35). □

6.3. Delay formulas

With the explicit output trajectories available, we can now determine formulas for the MIS gate delays of our model, which are functions of the input separation time $\Delta = t_B - t_A$. We use the following general procedure, which we exemplify for the case $\Delta \geq 0$; the case $\Delta < 0$ follows by invoking our symmetry argument again.

- For rising input transitions (= falling output transitions), we compute $V_{out}^{T_-^{\uparrow}}(\Delta)$, and use it as the initial value for $V_{out}^{T_+^{\uparrow\uparrow}}(t)$. The sought MIS gate delay $\delta_{M,+}^{\downarrow}(\Delta)$ is the time until the latter crosses the threshold voltage $V_{DD}/2$.
- For falling input transitions (= rising output transitions), we compute $V_{out}^{T_-^{\downarrow}}(\Delta)$, and use it as the initial value for $V_{out}^{T_+^{\downarrow\downarrow}}(t)$. The sought MIS gate delay $\delta_{M,+}^{\uparrow}(\Delta)$ is the time until the latter crosses the threshold voltage $V_{DD}/2$.

6.3.1. Rising input transitions

We again start with the simpler rising input transition scenario:

Theorem 6.4 (*MIS Delay Functions for Rising Input Transitions*)**.** *For any $0 \leq |\Delta| \leq \infty$, the MIS gate delay functions of our model for rising input transitions with pure delay $\delta_{min} \geq 0$[6] are given by:*

$$\delta_{M,+}^{\downarrow}(\Delta) = \begin{cases} \frac{\log(2)CR_{n_A}R_{n_B} - \Delta R_{n_B}}{R_{n_A}+R_{n_B}} + \Delta + \delta_{min} & 0 \leq \Delta < \log(2)CR_{n_A} \\ \log(2)CR_{n_A} + \delta_{min} & \Delta \geq \log(2)CR_{n_A} \end{cases}$$

$$\delta_{M,-}^{\downarrow}(\Delta) = \begin{cases} \frac{\log(2)CR_{n_A}R_{n_B} + |\Delta| R_{n_A}}{R_{n_A}+R_{n_B}} + |\Delta| + \delta_{min} & |\Delta| < \log(2)CR_{n_B} \\ \log(2)CR_{n_B} + \delta_{min} & |\Delta| \geq \log(2)CR_{n_B} \end{cases}$$

Proof. We sketch how $\delta_{M,+}^{\downarrow}(\Delta)$ is computed; the expression for $\delta_{M,-}^{\downarrow}(\Delta)$ is obtained analogously by our usual symmetry argument. Consider the trajectory $V_{out}^{T_+^{\uparrow\uparrow}}(t)$ in (19) starting from the initial value $V_{out}^{T_-^{\uparrow}}(\Delta)$, where the latter in turn is started from the initial value $V_{out}^{T_-^{\uparrow}}(0) = V_{DD}$. The objective is to compute the time $\delta_{M,+}^{\downarrow}(\Delta)$ when $V_{DD}/2$ is hit by either (i) already the preceding trajectory $V_{out}^{T_-^{\uparrow}}(t)$, or else (ii) $V_{out}^{T_+^{\uparrow\uparrow}}(t)$ itself (which is started at time Δ). Note that this reflects the fact that already the first rising input (happening at time 0) alone causes the output to eventually go to 0. Since all these trajectories only involve a single exponential function, they are easy to invert: It is apparent from (17) that case (i) occurs for values $\Delta \geq -\log(0.5)CR_{n_A}$, whereas (19) governs case (ii) for smaller values of Δ. □

6.3.2. Falling input transitions

In order to compute the MIS gate delay $\delta_{M,+}^{\uparrow}(\Delta)$, we need to study the time the voltage trajectory $V_{out}^{T_+^{\downarrow\downarrow}}(t)$ given in (35) needs to hit the threshold voltage $V_{DD}/2$ when starting from $V_{out}^{T_-^{\downarrow}}(\Delta) = 0$. After all, a NOR gate, where both inputs were initialized to V_{DD} at time $-\infty$, and where only one input experiences a falling transition at time 0 keeps its output at 0. Consequently, at time $t = \Delta$, when the second falling input transition occurs, the output voltage $V_{out}^{T_-^{\downarrow}}(\Delta)$ is still 0.

Therefore, $t = \delta_{M,+}^{\uparrow}(\Delta)$ must be a solution of the functional equation

$$I(t,\Delta) = e^{\frac{-t}{2RC}}\left(1 + \frac{2t}{d+\sqrt{\chi}}\right)^{\frac{-A+a}{2RC}}\left(1 + \frac{2t}{d-\sqrt{\chi}}\right)^{\frac{A}{2RC}} - \frac{1}{2} = 0. \tag{37}$$

[6] A pure delay term $\delta_{min} \geq 0$, already foreseen in the original IDM model [11], is essential for guaranteeing causality, and also for model parametrization introduced in Section 6.4.

In view of the complicated shape of (37), it is immediately apparent that there is not much hope to obtain an explicit solution $\delta^{\uparrow}_{M,+}(\Delta)$ satisfying $I\big(\delta^{\uparrow}_{M,+}(\Delta),\Delta\big)=0$, for every Δ. Even worse, since $\lim_{\Delta\to 0}A=0$ (recall Eq. (30)) and also $\lim_{\Delta\to 0}(d-\sqrt{\chi})=0$ (recall Eq. (26) and Eq. (28)), it is apparent that we cannot even determine a local solution of (37) in a neighborhood of $(0,0)$ via the implicit function theorem, as $(0,0)$ is a singular point (a cusp, as already suggested by Fig. 4(b)). Fortunately, however, the bootstrapping method from asymptotic analysis [30] eventually allowed us to develop accurate asymptotic expansions, in particular, for $\Delta\to 0$.

In a nutshell, bootstrapping (sometimes) allows to improve the accuracy of an a priori known asymptotic expansion of the sought solution of $I(t,\Delta)=0$, by rewriting $I(t,\Delta)=0$ into a suitable equivalent form $t=J(t,\Delta)$, and plugging the known expansion into the right-hand side only. In particular, relying on the fact that $\delta^{\uparrow}_{M,+}(\Delta)=\delta_0=O(1)$ for $\Delta\to 0$ as established in Lemma 15 below, one can easily derive the more accurate expansion $\delta^{\uparrow}_{M,+}(\Delta)=\delta_0+O(\Delta)$ for $\Delta\to 0$, where $\delta_0=\delta^{\uparrow}_{M,+}(0)$ is independent of Δ.

The following two technical lemmas provides asymptotic expansions of the basic ingredients in (37):

Lemma 14. *For $\Delta\to 0$, we have the following asymptotic expansions:*

$$\sqrt{\chi}=(a+\Delta)\sqrt{1-\frac{2\alpha_2\Delta}{R(a+\Delta)^2}}=\frac{\alpha_1+\alpha_2}{2R}+\frac{\alpha_1-\alpha_2}{\alpha_1+\alpha_2}\Delta+O(\Delta^2), \tag{38}$$

$$d+\sqrt{\chi}=a+\Delta+\sqrt{\chi}=\frac{\alpha_1+\alpha_2}{R}+\frac{2\alpha_1}{\alpha_1+\alpha_2}\Delta+O(\Delta^2), \tag{39}$$

$$d-\sqrt{\chi}=a+\Delta-\sqrt{\chi}=\frac{2\alpha_2}{\alpha_1+\alpha_2}\Delta+O(\Delta^2), \tag{40}$$

$$\frac{A}{2RC}=\frac{1}{2RC}\cdot\frac{-as_1-c'}{s_2-s_1}=\frac{-1}{2RC}\cdot\frac{a\frac{d-\sqrt{\chi}}{2}-\frac{\alpha_2\Delta}{2R}}{\sqrt{\chi}}=O(\Delta^2). \tag{41}$$

Proof. For (38), recalling definition Eq. (28) of χ and using the well-known expansions $\sqrt{1+x}=1+x/2+O(x^2)$ and $1/(1+x)^2=1-2x+O(x^2)$ for $x\to 0$, we obtain

$$\sqrt{1-\frac{2\alpha_2\Delta}{R(a+\Delta)^2}}=1-\frac{2\alpha_2\Delta}{2a^2R(1+\Delta/a)^2}+O(\Delta^2)=1-\frac{\alpha_2\Delta}{a^2R}+O(\Delta^2).$$

Plugging this into the first equality in (38) and recalling $a=\frac{\alpha_1+\alpha_2}{2R}$, the claimed asymptotic expansion follows by simple algebra. (39), (40) and (41) follow easily from their definitions Eq. (26) and Eq. (30) by plugging in the asymptotic expansion of $\sqrt{\chi}$ given in (38). □

Lemma 15. *For $\Delta\to\infty$, we have the following asymptotic expansions:*

$$\sqrt{\chi}=(a+\Delta)\sqrt{1-\frac{2\alpha_2\Delta}{R(a+\Delta)^2}}=\Delta+\frac{\alpha_1-\alpha_2}{2R}+O(\Delta^{-1}), \tag{42}$$

$$d+\sqrt{\chi}=a+\Delta+\sqrt{\chi}=2\Delta+\frac{\alpha_1}{R}+O(\Delta^{-1}), \tag{43}$$

$$d-\sqrt{\chi}=a+\Delta-\sqrt{\chi}=\frac{\alpha_2}{R}+O(\Delta^{-1}), \tag{44}$$

$$\frac{A}{2RC}=\frac{1}{2RC}\cdot\frac{-as_1-c'}{s_2-s_1}=\frac{-1}{2RC}\cdot\frac{a\frac{d-\sqrt{\chi}}{2}-\frac{\alpha_2\Delta}{2R}}{\sqrt{\chi}}=\frac{\alpha_2}{4R^2C}+O(\Delta^{-1}). \tag{45}$$

Proof. For (42), recalling definition Eq. (28) of χ and again using the well-known expansions $\sqrt{1+x}=1+x/2+O(x^2)$ and $1/(1+x)^2=1-2x+O(x^2)$ for $x\to 0$, we obtain

$$\begin{aligned}\sqrt{1-\frac{2\alpha_2\Delta}{R(a+\Delta)^2}}&=\sqrt{1-\frac{2\alpha_2}{\Delta R(1+a/\Delta)^2}}\\&=1-\frac{\alpha_2}{\Delta R(1+a/\Delta)^2}+O(\Delta^{-2})\\&=1-\frac{\alpha_2}{\Delta R}+O(\Delta^{-2}).\end{aligned}$$

Plugging this into the first equality in (42) and recalling $a=\frac{\alpha_1+\alpha_2}{2R}$, the claimed asymptotic expansion follows by simple algebra. (43), (44) and (45) follow easily from their definitions Eq. (26) and Eq. (30) by plugging in the asymptotic expansion of $\sqrt{\chi}$ given in (42). □

As the basis for our first bootstrapping step, we will need the extremal delay values $\delta^{\uparrow}_{M,+}(0)$, $\delta^{\uparrow}_{M,+}(\infty)$ and $\delta^{\uparrow}_{M,+}(-\infty)$. The following Lemma 16 will provide solutions δ_0, δ_∞ and $\delta_{-\infty}$ of (37) for $\Delta=0$, $\Delta=\infty$ and $\Delta=-\infty$, respectively, which can be expressed in

terms of some branch of the multi-valued *Lambert W function* [31]. We note that $W(x)$ provides the inverse of the function $ye^y = x$, and has only two real-valued branches: the principal branch $y = W_0(x)$ where $y \geq -1$, and the branch $y = W_{-1}(x)$ where $y \leq -1$. Since we will also prove in Theorem 6.5 later on that (37) has a unique solution for $\Delta = 0$, $\Delta = \infty$ and $\Delta = -\infty$, it follows that indeed $\delta^{\uparrow}_{M,+}(0) = \delta_0$, $\delta^{\uparrow}_{M,+}(\infty) = \delta_\infty$ and $\delta^{\uparrow}_{M,+}(-\infty) = \delta_{-\infty}$.

Lemma 16 (*Extremal MIS dElay Values*)**.** *Given*[7] α_1, α_2, R, *and* C, *we find*

$$\delta_0 = -\frac{\alpha_1+\alpha_2}{2R}\Big[1 + W_{-1}\Big(\frac{-1}{e \cdot 2^{\frac{4R^2C}{\alpha_1+\alpha_2}}}\Big)\Big], \tag{46}$$

$$\delta_\infty = -\frac{\alpha_2}{2R}\Big[1 + W_{-1}\Big(\frac{-1}{e \cdot 2^{\frac{4R^2C}{\alpha_2}}}\Big)\Big], \tag{47}$$

$$\delta_{-\infty} = -\frac{\alpha_1}{2R}\Big[1 + W_{-1}\Big(\frac{-1}{e \cdot 2^{\frac{4R^2C}{\alpha_1}}}\Big)\Big]. \tag{48}$$

Proof. We start with the proof for δ_0. Plugging in $\Delta = 0$ in (37) leads to

$$e^{-\frac{\delta_0}{2RC}}\Big(1 + \frac{\delta_0}{a}\Big)^{\frac{a}{2RC}} = \frac{1}{2}, \tag{49}$$

since $d + \sqrt{\chi} = 2a$, $d - \sqrt{\chi} = 0$ by Eq. (26)–Eq. (28), and $A = 0$ by Eq. (30); note that the third factor in (37) collapses to 1 since $(1+\infty)^0 = 1$. Raising Eq. (49) to the power $2RC/a$, one obtains

$$e^{-\frac{\delta_0}{a}}\Big(1 + \frac{\delta_0}{a}\Big) = 2^{-\frac{2RC}{a}}. \tag{50}$$

Setting $y = -(1 + \frac{\delta_0}{a})$ and $\gamma = \frac{2^{-\frac{2RC}{a}}}{e}$, this translates to $e^y y = -\gamma$. Note carefully that $-\gamma > -\frac{1}{e}$ and $y < -1$. It hence follows that

$$y = W_{-1}\Big(\frac{-1}{e \cdot 2^{\frac{2RC}{a}}}\Big),$$

which is equivalent to Eq. (46) by recalling $y = -(1 + \frac{\delta_0}{a})$ and $a = \frac{\alpha_1+\alpha_2}{2R}$.

We next turn our attention to δ_∞. Recalling the asymptotic expansions in Lemma 15, it is not difficult to verify that plugging in $\Delta = \infty$ in (37) leads to

$$e^{-\frac{\delta_\infty}{2RC}}\Big(1 + \frac{\delta_\infty}{\frac{\alpha_2}{2R}}\Big)^{\frac{\alpha_2}{4R^2C}} = \frac{1}{2}; \tag{51}$$

note that it is the second factor in (37) that collapses to 1 here. Since Eq. (51) differs from Eq. (49) only in that $a = \frac{\alpha_1+\alpha_2}{2R}$ has been replaced by $\frac{\alpha_2}{2R}$, the above derivations can be literally used to also confirm Eq. (47), and, by our usual symmetry argument, Eq. (48). □

We are now ready for proving the main Theorem 6.5 of this section:

Theorem 6.5 (*MIS Delay Functions for Falling Input Transitions*)**.** *For any* $0 \leq |\Delta| \leq \infty$, *the MIS delay functions of our model for falling input transitions with pure delay* $\delta_{min} \geq 0$ *are given by*

$$\delta^{\uparrow}_{M,+}(\Delta) = \begin{cases} \delta_0 - \frac{\alpha_1}{\alpha_1+\alpha_2}\Delta + \delta_{min} & 0 \leq \Delta < \frac{(\alpha_1+\alpha_2)(\delta_0-\delta_\infty)}{\alpha_1} \\ \delta_\infty + \delta_{min} & \Delta \geq \frac{(\alpha_1+\alpha_2)(\delta_0-\delta_\infty)}{\alpha_1} \end{cases} \tag{52}$$

$$\delta^{\uparrow}_{M,-}(\Delta) = \begin{cases} \delta_0 - \frac{\alpha_2}{\alpha_1+\alpha_2}|\Delta| + \delta_{min} & 0 \leq |\Delta| < \frac{(\alpha_1+\alpha_2)(\delta_0-\delta_{-\infty})}{\alpha_2} \\ \delta_{-\infty} + \delta_{min} & |\Delta| \geq \frac{(\alpha_1+\alpha_2)(\delta_0-\delta_{-\infty})}{\alpha_2} \end{cases} \tag{53}$$

Proof. Since inverting (37) globally is hopeless, we will determine the linear asymptotic expansion of $\delta^{\uparrow}_{M,+}(\Delta)$ for $\Delta \to 0$ and the constant asymptotic expansions of $\delta^{\uparrow}_{M,+}(\Delta)$ for $\Delta \to \pm\infty$, and glue them together at their intersection point.

To simplify our derivations, we will employ the variable substitutions

$$y = \frac{t}{2RC} \quad \text{and} \quad x = \frac{\Delta}{2RC},$$

in (37). This leads to

$$e^{-y}\Big(1 + \frac{y}{p + p_1 x + O(x^2)}\Big)^{p+O(x^2)}\Big(1 + \frac{y}{mx + O(x^2)}\Big)^{O(x^2)} = \frac{1}{2}, \tag{54}$$

[7] In Section 6.4, we will explain how to determine these parameters from given delay values δ_0, δ_∞ and $\delta_{-\infty}$.

where the constants

$$p = \frac{\alpha_1 + \alpha_2}{4R^2C}, \quad p_1 = \frac{\alpha_1}{\alpha_1 + \alpha_2}, \quad m = \frac{\alpha_2}{\alpha_1 + \alpha_2}$$

follow from the expansions provided in Lemma 14.

Obviously, in accordance with Eq. (49), setting $x = 0$ in the logarithm of (54) results in the following equation for the solution(s) y_0:

$$y_0 = p \cdot \log(1 + \frac{y_0}{p}) + \log(2). \tag{55}$$

Using continuity and convexity arguments, we first show that Eq. (55) and hence (54) has a unique solution, which must hence be equal to $y_0 = \delta_0/(2RC) > 0$ according to Lemma 16. More specifically, given y_1 and y_2 with $0 < y_1 < y_0 < y_2$, we prove that (54) has a unique solution $y = y(x) \in [y_1, y_2]$ for sufficiently small x by using Banach's fixed point theorem [19]: By taking the logarithm, we can rewrite (54) as a fixed point equation

$$y = \big(p + O(x^2)\big) \log\Big(1 + \frac{y}{p + p_1 x + O(x^2)}\Big) + O(x^2) \log\Big(1 + \frac{y}{mx + O(x^2)}\Big) - \log\frac{1}{2}. \tag{56}$$

Since

$$\begin{aligned}\frac{\partial}{\partial y}\big(p + O(x^2)\big) \log\Big(1 + \frac{y}{p + p_1 x + O(x^2)}\Big) &= \frac{\frac{p+O(x^2)}{p+p_1x+O(x^2)}}{1 + \frac{y}{p+p_1x+O(x^2)}} \\ &\le \left(1 + \frac{y_1}{2p}\right)^{-1} < 1\end{aligned}$$

provided x is chosen sufficiently small, and

$$\frac{\partial}{\partial y}\left(O(x^2) \log\Big(1 + \frac{y}{mx + O(x^2)}\Big)\right) = O\left(\frac{x^2}{mx + O(x^2) + y}\right) = O(x^2),$$

it follows that (56) is a contraction. Banach's fixed point theorem thus shows that the solution $y(x)$ (and hence also the corresponding solution $t(\Delta)$ of (37)) is unique. Note that an analogous reasoning can be used to prove that the solutions for $\Delta \to \infty$ and $\Delta \to -\infty$ are unique, which also confirms the values δ_∞ and $\delta_{-\infty}$ given in Lemma 16.

For our bootstrapping step, we write

$$y = y_0 + z \tag{57}$$

with $z = z(x) \in [y_1 - y_0, y_2 - y_0]$ for $x \to 0$, and show next that actually $z = O(x)$. We again take the logarithm of (54) and split it up into three parts T_1, T_2, T_3. Furthermore, we set

$$U = \frac{z}{p + p_1 x + O(x^2)} - \frac{y_0 p_1}{p^2} x + O(x^2),$$

which can be made arbitrarily small by choosing y_1, y_2 appropriately, and obtain

$$z = U(p + p_1 x) + \frac{y_0 p_1}{p} x + O(x^2). \tag{58}$$

Using the relations $1/(1 + x) = 1 - x + O(x^2)$ and $\log(1 + x) = x + O(x^2)$ for $x \to 0$, we thus obtain

$$\begin{aligned}
T_1 &= \log\big(e^{-y}\big) = -y_0 - z = -y_0 - U(p + p_1 x) - \frac{y_0 p_1}{p} x + O(x^2), \\
T_2 &= \log\Big(1 + \frac{y}{p + p_1 x + O(x^2)}\Big)^{p + O(x^2)} \\
&= \big(p + O(x^2)\big) \log\Big(1 + \frac{y_0}{p + p_1 x + O(x^2)} + \frac{z}{p + p_1 x + O(x^2)}\Big) \\
&= \big(p + O(x^2)\big) \log\Big(1 + \frac{y_0}{p} \cdot \frac{1}{1 + \frac{p_1 x}{p} + O(x^2)} + U + \frac{y_0 p_1 x}{p^2} + O(x^2)\Big) \\
&= \big(p + O(x^2)\big) \log\Big(1 + \frac{y_0}{p} + O(x^2) + U\Big) \\
&= \big(p + O(x^2)\big) \log\Big(\big(1 + \frac{y_0}{p}\big)\big(1 + \frac{U}{1 + \frac{y_0}{p}}\big)\Big) \\
&= \big(p + O(x^2)\big) \log\big(1 + \frac{y_0}{p}\big) + \big(p + O(x^2)\big) \frac{U + O(U^2)}{1 + \frac{y_0}{p}} \\
T_3 &= \log\Big(1 + \frac{y}{mx + O(x^2)}\Big)^{O(x^2)} = \log\Big(\frac{y + mx + O(x^2)}{mx + O(x^2)}\Big)^{O(x^2)} \\
&= O(x^2) \cdot \log\big(y_0 + z + mx + O(x^2)\big) + O\big(x^2 \log(x)\big) \\
&= O(x^2) \cdot \log\left(y_0\Big(1 + \frac{z + mx + O(x^2)}{y_0}\Big)\right) + O\big(x^2 \log(x)\big) \\
&= O(x^2) \cdot \Big(\log(y_0) + \frac{z + mx + O(x^2)}{y_0}\Big) + O\big(x^2 \log(x)\big)
\end{aligned}$$

$$= O\big(x^2 \log(x)\big).$$

Thus, (54), which is equivalent to $T_1 + T_2 + T_3 = \log(1/2)$, is also equivalent to

$$-U\big(p + p_1 x\big) - \frac{y_0 p_1}{p} x + \big(p + O(x^2)\big) \frac{U\big(1 + O(U)\big)}{1 + \frac{y_0}{p}} + O(x^2 \log x) = 0, \tag{59}$$

where the terms involving y_0 canceled out due to relation Eq. (55). Extracting U and recalling that $O(U)$ can be made arbitrarily small by choosing y_1, y_2 appropriately finally reveals $U = O(x)$ and hence $z = z(x) = O(x)$ by Eq. (58) as claimed.

In an additional bootstrapping step, we can be slightly more precise w.r.t. T_2 and obtain

$$\begin{aligned}
T_2 &= \big(p + O(x^2)\big) \cdot \log\Big(1 + \frac{y}{p + p_1 x + O(x^2)}\Big) \\
&= \big(p + O(x^2)\big) \cdot \log\Big(1 + \frac{y_0 + z}{p}\big(1 - \frac{p_1}{p} x + O(x^2)\big)\Big) \\
&= \big(p + O(x^2)\big) \cdot \log\left(\big(1 + \frac{y_0}{p}\big)\Big(1 + \frac{\frac{z}{p} - \frac{y_0 p_1}{p^2} x + O(x^2)}{1 + \frac{y_0}{p}}\Big)\right) \\
&= \big(p + O(x^2)\big) \cdot \Big(\log\big(1 + \frac{y_0}{p}\big) + \frac{z}{y_0 + p} - \frac{y_0 p_1}{p(y_0 + p)} x + O(x^2)\Big) \\
&= \frac{p}{y_0 + p} z + p \log\big(1 + \frac{y_0}{p}\big) - \frac{y_0 p_1}{y_0 + p} x + O(x^2).
\end{aligned}$$

This leads to

$$-y_0 - z + \log(2) + \frac{p}{y_0 + p} z + p \log(1 + \frac{y_0}{p}) - \frac{y_0 p_1}{y_0 + p} x + O\big(x^2 \log(x)\big) = 0, \tag{60}$$

which, by virtue of Eq. (55), gives

$$z = -p_1 x + O\big(x^2 \log(x)\big) = -\frac{\alpha_1}{\alpha_1 + \alpha_2} x + O\big(x^2 \log(x)\big). \tag{61}$$

Recalling Eq. (57), we therefore arrive at the improved expansion

$$y = y_0 - \frac{\alpha_1}{\alpha_1 + \alpha_2} x + O\big(x^2 \log(x)\big) \tag{62}$$

and, after undoing our variable substitution,

$$\delta^{\uparrow}_{M,+}(\Delta) = \delta_0 - \frac{\alpha_1}{\alpha_1 + \alpha_2} \Delta + O(\Delta^2 \log(\Delta)). \tag{63}$$

Finally, it is easy to check that the crossing point of the linear part of (63) and δ_∞ is $\Delta = \frac{(\alpha_1 + \alpha_2)(\delta_0 - \delta_\infty)}{\alpha_1}$. By pasting them together at this crossing point, we obtain the delay formula (52) that is valid for all values of Δ.

Last but not least, $\delta^{\uparrow}_{M,-}(\Delta)$ is obtained by exchanging α_1 and α_2 and replacing δ_∞ by $\delta_{-\infty}$ as well as Δ by $|\Delta|$ in (52), according to our usual symmetry argument, which completes our proof. □

To conclude this section, we note that more accurate asymptotic expansions for the delay can be derived easily by further bootstrapping steps. It turns out, however, that improving the accuracy for Δ very close to 0 has its price in a rapid worsening of the accuracy for larger values of Δ. Consequently, just pasting together the expansions for $\Delta \to 0$ and $\Delta \to \pm\infty$ would no longer be sufficient to cover the whole range for Δ. Whereas bootstrapping could also be used to develop an asymptotic expansion at some intermediate point within this gap, the resulting improvement is not worth the effort.

6.4. Model parametrization and evaluation results

What is still needed to use our model, in particular, the delay formulas established in Theorems 6.4 and 6.5, is a practical procedure for model parametrization: Given some data that characterize the delays of a real gate, one needs to determine appropriate values for the model parameters α_1, α_2, C, R, R_{n_A}, and R_{n_B} and an appropriate pure delay $\delta_{\min}$ that align our model with these data.

As in [14,16], we will parameterize our model based on the characteristic MIS delay values $\delta^{\downarrow}_S(-\infty)$, $\delta^{\downarrow}_S(0)$, and $\delta^{\downarrow}_S(\infty)$ according to Fig. 4(a) and $\delta^{\uparrow}_S(-\infty)$, $\delta^{\uparrow}_S(0)$, and $\delta^{\uparrow}_S(\infty)$ according to Fig. 4(b). In sharp contrast to the parametrization procedure employed for the original model in [16], which was based on least-squares fitting, we can exploit our explicit trajectory formulas to get rid of any fitting. In fact, as already in Lemma 16, Lambert W functions will turn out to be instrumental also here.

Theorem 6.6 (*Gate Characterization*). *Let $\delta^{\downarrow}_S(-\infty)$, $\delta^{\downarrow}_S(0)$, $\delta^{\downarrow}_S(\infty)$ and $\delta^{\uparrow}_S(-\infty)$, $\delta^{\uparrow}_S(0)$, $\delta^{\uparrow}_S(\infty)$ be the MIS delay values of a real gate that shall be matched by our model, in the sense that $\delta^{\downarrow}_{M,-}(-\infty) = \delta^{\downarrow}_S(-\infty)$, $\delta^{\downarrow}_{M,-}(0) = \delta^{\downarrow}_{M,+}(0) = \delta^{\downarrow}_S(0)$, $\delta^{\downarrow}_{M,+}(\infty) = \delta^{\downarrow}_S(\infty)$ and $\delta^{\uparrow}_{M,-}(-\infty) = \delta^{\uparrow}_S(-\infty)$, $\delta^{\uparrow}_{M,-}(0) = \delta^{\uparrow}_{M,+}(0) = \delta^{\uparrow}_S(0)$, $\delta^{\uparrow}_{M,+}(\infty) = \delta^{\uparrow}_S(\infty)$.*

Given an arbitrarily chosen value C for the load capacitance, this matching is accomplished by choosing the model parameters as follows:

$$\delta_{\min} = \delta^{\downarrow}_S(0) - \sqrt{\big(\delta^{\downarrow}_S(\infty) - \delta^{\downarrow}_S(0)\big)\big(\delta^{\downarrow}_S(-\infty) - \delta^{\downarrow}_S(0)\big)} \tag{64}$$

$$R_{n_B} = \frac{\delta_S^{\downarrow}(-\infty) - \delta_{\min}}{C \cdot \log(2)} \tag{65}$$

$$R_{n_A} = \frac{\delta_S^{\downarrow}(\infty) - \delta_{\min}}{C \cdot \log(2)} \tag{66}$$

Furthermore, using the function

$$A(t, R, C) = \frac{-2R\big(t - 2RC \cdot \log(2)\big)}{W_{-1}\Big(\big(\frac{2RC \cdot \log(2)}{t} - 1\big)e^{\frac{2RC \cdot \log(2)}{t} - 1}\Big) + 1 - \frac{2RC \cdot \log(2)}{t}}, \tag{67}$$

determine R by numerically[8] *solving the equation*

$$A\big(\delta_S^{\uparrow}(0) - \delta_{\min}, R, C\big) - A\big(\delta_S^{\uparrow}(\infty) - \delta_{\min}, R, C\big) - A\big(\delta_S^{\uparrow}(-\infty) - \delta_{\min}, R, C\big) = 0, \tag{68}$$

and finally choose

$$\alpha_1 = A\big(\delta_S^{\uparrow}(-\infty) - \delta_{\min}, R, C\big), \tag{69}$$

$$\alpha_2 = A\big(\delta_S^{\uparrow}(\infty) - \delta_{\min}, R, C\big). \tag{70}$$

Proof. We first consider the parameters determined by the rising input transition case. To align the delay formulas in Theorem 6.4 with the given delay values, we just plug in $\delta_S^{\downarrow}(-\infty) - \delta_{\min}$, $\delta_S^{\downarrow}(0) - \delta_{\min}$, and $\delta_S^{\downarrow}(\infty) - \delta_{\min}$ in order to obtain the following system of equations for our sought parameters $\delta_{\min}$, R_{n_B} and R_{n_A}:

$$\delta_S^{\downarrow}(0) - \delta_{\min} - \frac{\log(2) \cdot C \cdot R_{n_A} R_{n_B}}{R_{n_A} + R_{n_B}} = 0$$

$$\delta_S^{\downarrow}(\infty) - \delta_{\min} - \log(2) \cdot C \cdot R_{n_A} = 0$$

$$\delta_S^{\downarrow}(-\infty) - \delta_{\min} - \log(2) \cdot C \cdot R_{n_B} = 0$$

Some straightforward algebra shows that this system is equivalent to the following one:

$$\frac{1}{R_{n_A}} + \frac{1}{R_{n_B}} = \frac{\log(2) \cdot C}{\delta_S^{\downarrow}(0) - \delta_{\min}}$$

$$\frac{1}{R_{n_A}} = \frac{\log(2) \cdot C}{\delta_S^{\downarrow}(\infty) - \delta_{\min}}$$

$$\frac{1}{R_{n_B}} = \frac{\log(2) \cdot C}{\delta_S^{\downarrow}(-\infty) - \delta_{\min}}$$

It follows that

$$\frac{1}{\delta_S^{\downarrow}(0) - \delta_{\min}} = \frac{1}{\delta_S^{\downarrow}(\infty) - \delta_{\min}} + \frac{1}{\delta_S^{\downarrow}(-\infty) - \delta_{\min}},$$

which can be rewritten into a quadratic equation for $\delta_{\min}$, namely,

$$\delta_{\min}^2 - 2\delta_S^{\downarrow}(0)\delta_{\min} + \delta_S^{\downarrow}(0)\delta_S^{\downarrow}(\infty) + \delta_S^{\downarrow}(0)\delta_S^{\downarrow}(-\infty) - \delta_S^{\downarrow}(\infty)\delta_S^{\downarrow}(-\infty) = 0.$$

It is easy to verify that it has the solution stated in Eq. (64). Note that we need to take the negative solution in order to ensure that $\delta_{\min} \leq \delta_S^{\downarrow}(0)$.

We now turn our attention to the parameters determined by the falling input transition case. We first justify Eq. (67) by considering $A\big(\delta_S^{\uparrow}(0) - \delta_{\min}, R, C\big)$, which corresponds to setting $t = \delta_0 = \delta_S^{\uparrow}(0) - \delta_{\min}$ as defined in Lemma 16. Abbreviating $\alpha = \alpha_1 + \alpha_2$ and noting that $\alpha = 2Ra$ according to Eq. (25), we start from Eq. (50) in the proof of Lemma 16, which states $e^{\frac{-2R\delta_0}{\alpha}}(1 + \frac{2R\delta_0}{\alpha}) = 2^{\frac{-4R^2C}{\alpha}}$. By raising both sides to the power of $\alpha/(2R)$, we get $1 < (1 + \frac{2R\delta_0}{\alpha})^{\frac{\alpha}{2R}} = 2^{-2RC}e^{\delta_0}$ that is equivalent to $(1 + \frac{\omega}{y})^y = \beta$ with $\omega = 2R\delta_0 > 0$, $y = \alpha > 0$, and $\beta = e^{2R(\delta_0 - 2RC\log(2))} > 1$. Once again, by the substitution $z = 1 + \frac{\omega}{y} > 1$, we get $e^{\frac{\omega}{z-1}\log(z)} = \beta$. Accordingly, by taking the natural logarithm on both sides, we arrive at

$$\log(z) = (z - 1)\gamma, \tag{71}$$

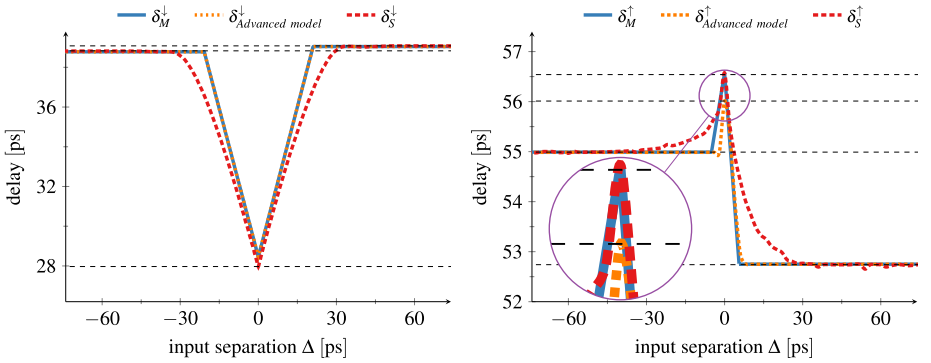
for $\gamma = \frac{\log(\beta)}{\omega} > 0$. We need to solve Eq. (71) for $z > 1$ so as to obtain $\alpha = y = \frac{\omega}{z}$. From Eq. (71), we get by exponentiation $ze^{-z\gamma} = e^{-\gamma}$, and multiplication by $-\gamma$ finally gives us $-z\gamma e^{-z\gamma} = -\gamma e^{-\gamma}$. We can solve this equation for $-z\gamma$ by means of the Lambert W function. Since $\gamma > 0$ and we need the solution to satisfy $z > 1$, we must take the branch W_{-1} here to compute

$$z = -\frac{W_{-1}(-\gamma e^{-\gamma})}{\gamma}.$$

[8] Whereas there might be a way to solve it analytically, we did not find it so far.

Table 4
Model parameter values for the 15 nm CMOS NOR gate used for producing Fig. 4(a) and Fig. 4(b). The chosen capacitance value is $C = 3.6331599443276\ fF$.

Parameters determined by falling output transitions		
$\delta_{\min} = 16.963423585525\ ps$	$R_{n_A} = 8.760489389736\ k\Omega$	$R_{n_B} = 8.658111065573\ k\Omega$
Parameters determined by rising output transitions		
$R = 6.539995525955\ k\Omega$	$\alpha_1 = 20.4461 \cdot 10^{-9}\ \Omega s$	$\alpha_2 = 9.3487 \cdot 10^{-9}\ \Omega s$



(a) Rising input transition (b) Falling input transition

Fig. 7. Our proposed computed ($\delta_M^{\downarrow/\uparrow}(\Delta)$), the measured ($\delta_S^{\downarrow/\uparrow}(\Delta)$), and those computed by the baseline model in [16] for the 15nm CMOS NOR gate from [14].

Plugging in the values of z and γ into $y = \frac{\omega}{z}$, we obtain

$$y = -\frac{-\log(\beta)}{W_{-1}(-\frac{\log(\beta)}{\omega}\beta^{\frac{-1}{\omega}}) + \frac{\log(\beta)}{\omega}}. \tag{72}$$

Finally, replacing ω resp. β by their "generic" value $2Rt$ resp. $e^{2R(t-2RC\log(2))}$ (where δ_0 is replaced by t) in Eq. (72) gives Eq. (67).

It only remains to justify Eq. (70) and Eq. (69), where we use the same argument as in the proof of Lemma 16: We can use literally the same derivations as above, except that we start from the variant of Eq. (50) where a is replaced by $\frac{\alpha_2}{2R}$ resp. $\frac{\alpha_1}{2R}$ for Eq. (70) resp. Eq. (69). This finally also explains why we can determine R by (numerically) solving Eq. (68). □

We are now ready to compare the delay predictions of our Theorems 6.4 and 6.5 with the ones provided in the original paper [16]. For that purpose, we employ our Theorem 6.6 for computing the parameters for the same 15 nm technology CMOS NOR gate used in [16], which are summarized in Table 4, and visualize the delay predictions of our model: Fig. 7 depicts our delays (blue curve) and compares it to the analog reality (dashed red curve), as well as to the predictions provided by the original model in [16] (dashed orange curve).

Since we are utilizing almost the same delay formulas and parameters as those used in [16] for the rising input transition case, we observe identical blue and orange curves, which closely match the gate's real MIS delays. There is a significant improvement in the delay predictions of our model over the one in [16] for the falling input transition case, however. In particular, according to Fig. 7(b), our model accurately predicts the real delays even for very small values of Δ, where [16] is considerably off.

7. Conclusions

We presented a general continuity proof for a broad class of first-order thresholded hybrid models, which arise naturally in digital integrated circuits. We showed that, under mild conditions regarding causality, digitized hybrid gates can be composed to form circuits with unique and well-behaved executions. We introduced the intricacies of multi-input switching effects in multi-input gates and proved the continuity of two state-of-the-art digitized hybrid models for CMOS NOR gates. Moreover, we revisited the currently best of these models and provided a completely new analysis of its MIS delay predictions, based on explicit solutions of the involved ODEs, which not only resulted in a much better accuracy but also in an explicit model parametrization procedure.

The main strength of our approach is its simplicity combined with a very reasonable delay prediction accuracy. In the context of digital integrated circuits, this enables analytic delay formulas and fast dynamic timing simulation with a surprisingly high accuracy. Consequently, the slow analog simulations of the large ODE systems describing a typical circuit can be replaced by a fast discrete event simulation that utilizes our delay formulas. Our implementation in the Involution Tool revealed that this reduces typical simulation times by several orders of magnitude. At the same time, the achievable delay prediction accuracy is also the main weakness of our approach, as our simple first-order thresholded hybrid gate models cannot capture all the intricacies of real circuit implementations.

CRediT authorship contribution statement

Arman Ferdowsi: Writing – review & editing, Writing – original draft, Validation, Methodology, Formal analysis. **Matthias Függer:** Writing – review & editing, Writing – original draft, Validation, Methodology, Formal analysis. **Thomas Nowak:** Writing – review & editing, Writing – original draft, Validation, Methodology, Formal analysis. **Ulrich Schmid:** Writing – review & editing, Writing – original draft, Validation, Methodology, Formal analysis. **Michael Drmota:** Methodology, Formal analysis.

Declaration of competing interest

The authors have no competing interests to declare that are relevant to the content of this article.

Data availability

Data will be made available on request.

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