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Si/$Ge_{1-x}Sn_x$/Si transistors with highly transparent Al contacts

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ABSTRACT

We study the monolithic quasi-ohmic contact formation with single-elementary Al to $Ge_{1-x}Sn_x$ channel devices with various Sn concentrations between 0.5 % and 4 %. Thereby we investigate the influence of increasing Sn content on the electrical transport properties in field-effect transistors for a wide temperature range between 77 K and 400 K. At low temperatures, the devices exhibit improved performance metrics, promising for cryo-CMOS applications. Compared to pure Ge control devices, the introduction of Sn into the channel leads to a 20 times increased on-current. In a multi-gate architecture, we analyze the decoupled influence of the carrier injection through the metal–semiconductor junction and the channel conduction.

1. Introduction

The introduction of GeSn as a channel material, with its modulated band structure and high carrier mobilities for both electrons and especially holes, is promising for optoelectronics, Beyond CMOS technologies with high on-state conductance as well as low power cryogenic applications [1–5]. Mobilities of up to 698 cm^2/Vs for electrons [6] and 509 cm^2/Vs for holes [7] have been recently reported. In field-effect transistors (FETs) the integration of Sn has already demonstrated performance enhancements, such as increased transconductance and operation frequencies, compared to equivalent Ge channel devices [1,8]. Importantly, as a group-IV semiconductor material, GeSn retains high compatibility with current Si CMOS technology. Furthermore, with Sn concentrations higher than ~8%, GeSn exhibits direct band gap transitions [9,10], making it highly promising for direct integration of optoelectronic applications into CMOS platforms [11]. For any integration of GeSn devices, high-quality, nanoscaled ohmic contacts are of utmost importance. Especially for cryo-CMOS applications, doping-free metal contacts to GeSn devices are of high interest, as their resistivity is even reducing with lower temperatures, in contrast to doped semiconductor contacts that suffer from carrier freeze-out, leading to an exponential increase in material resistivity [12]. On the other hand, the reproducibility of stochiometry and crystal quality in metallic compound materials, such as NiGeSn [3], PtGeSn [2] or Yb stanogermanide [13], can be challenging due to complex phase transitions, although providing good contact properties.

Recently, we have demonstrated monolithic and single elementary Al contact formation to top-down fabricated nanosheets composed of vertical Si-$Si_{1-x}Ge_x$-Si heterostructures [14], providing a versatile platform for various emerging device concepts [15]. In this work, we now demonstrate the contact formation to heterostructures encompassing $Ge_{1-x}Sn_x$ layers with Sn concentrations ranging from 0.5 % to 4 %. Thereby, we analyze the composition-dependent electrical transport properties in FET architectures.

2. Results and discussion

For GeSn device fabrication, we adapted recent growth strategies using ultra-low growth temperatures for the epitaxial deposition of Si/$Ge_{1-x}Sn_x$/Si heterostructures on SOI substrates [16], schematically shown in Fig. 1(a). The growth was carried out in a Riber SIVA 45 solid source molecular beam epitaxy (MBE) system on silicon on insulator (SOI) substrates, with a Si(001) device layer thickness of 20 nm on a 100 nm thick buried oxide (BOX). The samples underwent a standard Si substrate cleaning process [17], finalized by a dip in diluted hydrofluoric acid (HF 1 %) to remove the native oxide. All substrates were degassed at 923 K for 15 min, followed by a one-hour conditioning step at 723 K. In all cases, an 8 nm thick Si buffer was

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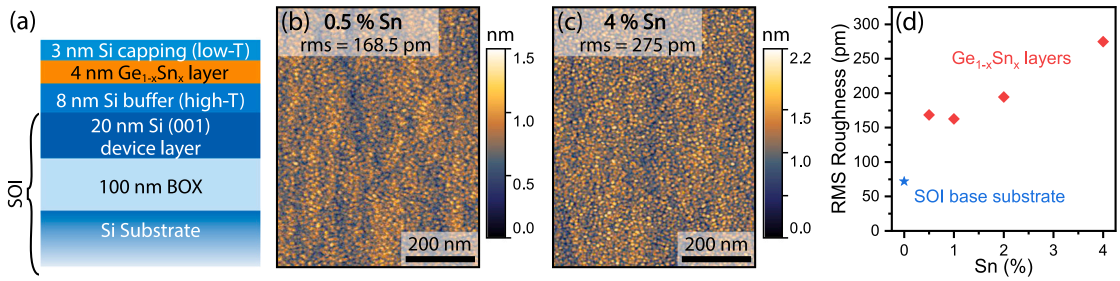

Fig. 1. (a) Schematic of the epitaxially grown Si/$Ge_{1-x}Sn_x$/Si heterostructure on SOI, with AFM surface topography of the substrate containing 0.5 % (b) and 4 % Sn (c). The rms surface roughness of four substrates with different Sn contents (0.5 %, 1 %, 2 %, 4 %) and the base SOI substrate are compared in (d).

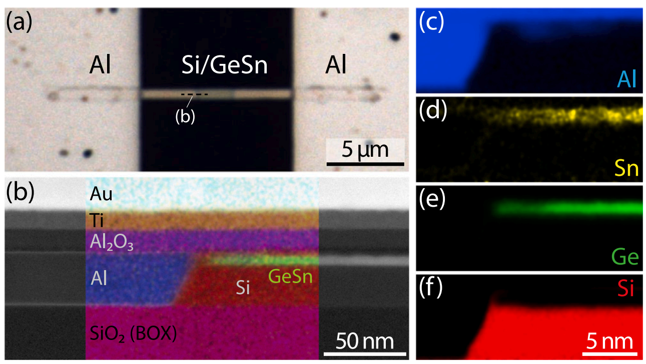

Fig. 2. (a) Microscope image of the formed Al-Si/$Ge_{0.99}Sn_{0.01}$ heterostructure after the thermally induced exchange reaction. (b) HAADF-STEM image with EDX overlay of the axial cut at the Al-Si/$Ge_{1-x}Sn_x$ interface, indicated in (a). (c)–(f) Single elementary EDX maps.

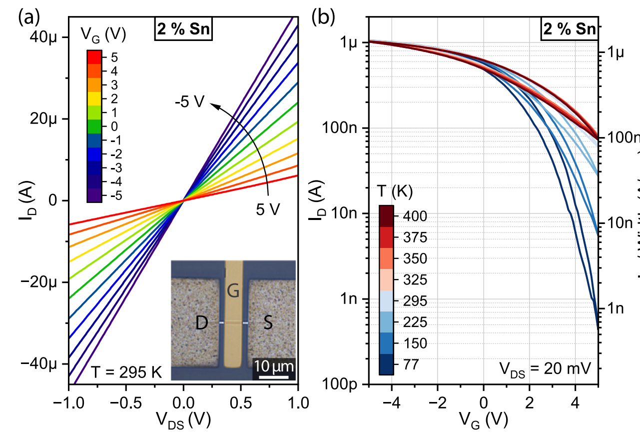

Fig. 3. (a) Linear gate-dependent I/V characteristic of a top-gated Al-$Ge_{0.98}Sn_{0.02}$ heterostructure shown in the inset. (b) Temperature-dependent transfer characteristic at V_{DS} = 20 mV.

deposited at a growth temperature of 923 K and a rate of 0.7 Å/s. Hereafter, a 4 nm thick $Ge_{1-x}Sn_x$ layer was deposited, followed by a 3 nm thick Si capping layer, both grown at 448 K. In total, four samples with different Sn contents x of 0.5 %, 1 %, 2 %, and 4 % were grown. In all cases, the low growth temperatures of the $Ge_{1-x}Sn_x$ layers suppress elastic and plastic relaxation [17]. This results in a low root-mean-square (rms) surface roughness < 0.28 nm for all substrates, as shown in the atomic force microscopy images in Figs. 1(b,c) taken immediately after sample growth. With increasing the Sn content in the strained $Ge_{1-x}Sn_x$ layer on Si, the strain energy in the film increases, promoting a strain relaxation-driven increase in the film's surface roughness (see Fig. 1(d)). However, the rms values are close to that of the pristine SOI substrate, indicating that the low growth temperature of the Si capping layers ensures efficient suppression of Ge [18] and Sn surface segregation.

From the vertical Si-$Ge_{1-x}Sn_x$-Si heterostructure sample, ~700 nm wide mesa structures are then patterned using laser lithography and SF_6-O_2 based dry etching techniques. An approximately 10.8 nm thick Al_2O_3 gate dielectric is grown by atomic layer deposition (ALD) and subsequently removed by BHF (7:1) etching at the drain (D) and source (S) contact areas of the nanosheets prior to sputtering 120 nm of Al. Using rapid thermal annealing (RTA) at 773 K in forming gas atmosphere a solid-state exchange reaction between Al and the Si/$Ge_{1-x}Sn_x$ layers is induced, where Al supplied by the contact pads is exchanging the semiconducting channel material [14]. A microscope image of the monolithically formed metal-semiconductor-metal heterostructure is shown in Fig. 2(a). The high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) image of the axial cut of this heterostructure in Fig. 2(b) reveals the formed abrupt Al-$Ge_{1-x}Sn_x$ junction. Interestingly, a nanometer-thin Si agglomeration between the Al and the $Ge_{1-x}Sn_x$ layer is evident, which is consistent with observations in exchange processes between Al and SiGe in similar structures [14]. The single elementary energy-dispersive X-ray spectroscopy (EDX) images in Fig. 2(c–d) show that during the exchange process at 773 K the vertical Si/$Ge_{1-x}Sn_x$/Si heterostructure stays intact, without any evident intermixing of the epitaxially grown layers. Furthermore, the intruded Al leads seem to be crystalline and single elementary (within the Sn detection limit), with only small Sn residuals detected close to the metal–semiconductor junction and surface. As no intermetallic phases with complex phase transitions occur during the thermally induced exchange process, several consecutive annealing steps can be applied to precisely control the remaining $Ge_{1-x}Sn_x$ channel length [14].

Integrated into a FET by adding a gate atop the whole Al-$Ge_{1-x}Sn_x$-Al heterostructure via laser lithography, Ti/Au (10 nm/100 nm) evaporation and lift-off, the electrical transport is investigated in Fig. 3 for a device with a Sn concentration of 2 %. The gate-dependent I/V characteristic thereby reveals linear behavior, suggesting highly transparent quasi-ohmic contacts attributed to the high Sn content in the Si interlayer. By decreasing the gate voltage (V_G) from −5 V to 5 V, the current can be increased by a factor of ~20. The transfer characteristic in Fig. 3(b) at a bias voltage V_{DS} of 20 mV further shows very p-type dominant conduction, which can be attributed to strong Fermi-level pinning near the valance band edge. Furthermore, as the 4 nm thin $Ge_{1-x}Sn_x$ layer is sandwiched vertically between two Si layers, we speculate that this results in an abrupt discontinuity of the energy band structure at the interfaces, potentially leading to a hole gas formation [14,19]. Temperature-dependent measurements in Fig. 3(b) between 77 K and 400 K indicate that at cryogenic temperatures, the $Ge_{1-x}Sn_x$ channel can be sufficiently depleted due to fewer thermally excited charge carriers at $V_G > 0$ V. This results in a drain current modulation over six orders of magnitude while the on-currents remain mostly temperature-independent, making the system especially interesting for

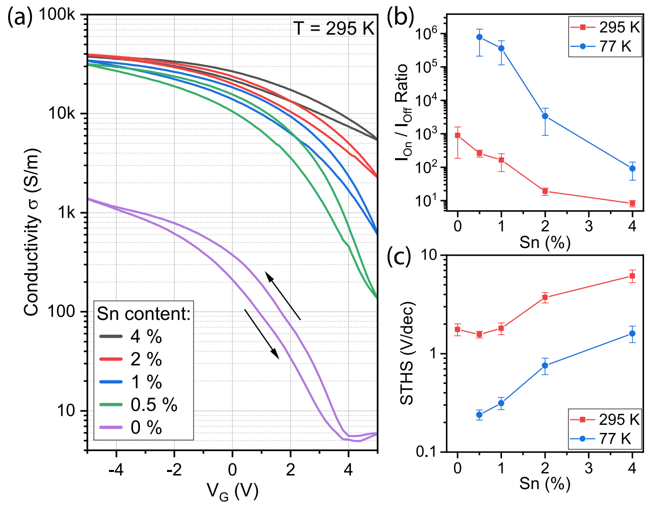

Fig. 4. (a) Comparison of the gate-dependent conductivity of samples with different Sn content, including a reference sample with a pure Ge layer, measured at V_{DS} = 20 mV. The arrows indicate the sweeping direction. (b) I_{on}/I_{off} ratio and (c) subthreshold slope vs. Sn content, at 295 K and 77 K. The values are averaged over three comparable devices.

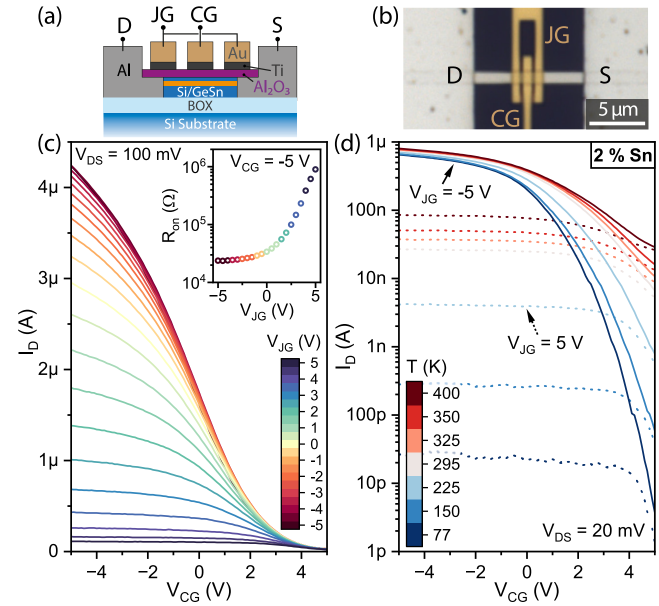

Fig. 5. (a) Schematic and (b) microscope image of a multi-gate structure with 2 % Sn. Junction gate (V_{JG}) dependent transfer characteristic, with the inset showing the change in on-state resistance (R_{on}). (b) Temperature dependent transfer characteristic for V_{JG} = −5 V (solid) and V_{JG} = 5 V (dotted line).

cryo-CMOS applications. At elevated temperatures above 325 K, there are almost no changes in the transfer characteristic.

The comparison of nanosheets with four different GeSn stoichiometries in an FET architecture is shown in Fig. 4, compared to a control sample with a pure Ge layer. The gate-dependent conductivity, normalized to the geometry of the remaining $Ge_{1-x}Sn_x$ channel, shows that an increased Sn content enhances the conductivity, over 20x higher compared to a pure Ge layer in agreement with an accumulation channel. However, the off-state is given by depletion implying a V_G-dependent overall gate capacitance accompanied by degraded I_{on}/I_{off} ratios and subthreshold slopes (STHS), as shown in Fig. 4(b,c). Scaling the width of the semiconducting channel down to the low nm range and improved gating architecture, such as FinFETs [20] or gate-all-around (GAA) FETs [2,5], should therefore significantly improve electrostatic gating, as a sufficient carrier depletion in the off-state cannot be achieved for such wide channels. At cryogenic temperatures, both the I_{on}/I_{off} ratio and the STHS for all Sn concentrations can be greatly improved, with a modulation up to 6 orders of magnitude and STHS of 240 mV/dec for 0.5 % Sn channel device at 77 K.

To decouple the influence of the carrier injection at the junction and the channel conduction, a multi-gate structure, featuring a dedicated junction gate (JG) atop the Al-$Ge_{1-x}Sn_x$ interfaces and a channel gate (CG) in the middle of the $Ge_{1-x}Sn_x$ channel, is investigated. A schematic cross section of this multi-gate transistor is depicted in Fig. 5(a), with an optical microscope image in (b). The JG-dependent transfer characteristic in Fig. 5(c) shows that the on-state current can be lowered with increased V_{JG}, as this leads to an increased injection barrier for holes. This results in a modulation of the on-state resistance by a factor of ∼40. In the transfer characteristic in Fig. 5(c), with V_{CG} swept from −5 V and 5 V, the on-state current can be modulated via the JG, as the injection barrier for holes is increased with increasing V_{JG}. Thereby, the on-state resistance can be tuned by a factor of ∼40. The off-state current is barely influenced by the JG, as this is defined by the depletion of the charge carriers within the channel. With the JG set to 5 V, the current can then only be modulated by a factor of 4.8. Temperature-dependent measurements in 5(d) show that reduced temperatures lead to improved channel depletion due to less thermally active carriers, resulting in increased I_{on}/I_{off} ratio over more than 5 orders of magnitude at 77 K for V_{JG} = −5 V. Furthermore, this leads to an increased influence of the JG, with an on-state resistance change of up to 2.5×10^4 at V_{CG} = −5 V. It can, therefore, be assumed that the main mechanism for controlling the device is modulation of the injection barrier, mainly by blocking the holes with positive V_{JG} by introducing an electrostatically tunable energy barrier at the junction.

3. Conclusion

We have systematically investigated the contact formation to nanosheets patterned from epitaxially grown vertical Si-$Ge_{1-x}Sn_x$-Si heterostructures with Sn contents between 0.5 % and 4 %. Using a thermally induced exchange reaction between Al and Si/GeSn at 773 K, single-elementary Al contacts with abrupt junctions to the $Ge_{1-x}Sn_x$ channel are formed, showing highly transparent quasi-ohmic behavior for holes. In FETs, the introduced Sn leads to a more than 20-fold increase in on-state conductivity compared to a Ge control sample. Temperature measurements down to 77 K reveal improved electrostatic tunability for all samples, up to 6 orders of magnitude for 0.5 % Sn, while on-state currents remain temperature invariant. In multi-gate structure, decoupling carrier injection and channel modulation, the on-state resistance can be modulated by a factor of ∼40 via a junction gate by changing the injection barrier of holes into the channel. This finding supports the highly transparent contacts for holes.

CRediT authorship contribution statement

Lukas Wind: Writing – original draft, Methodology, Investigation, Data curation. **Stefan Preiß:** Investigation, Data curation. **Daniele Nazzari:** Methodology, Investigation. **Johannes Aberl:** Resources, Methodology, Investigation. **Enrique Prado Navarrete:** Resources, Methodology, Investigation. **Moritz Brehm:** Writing – review & editing, Resources, Methodology, Funding acquisition. **Lilian Vogl:** Validation, Methodology, Investigation. **Andrew M. Minor:** Resources, Investigation. **Masiar Sistani:** Writing – review & editing, Supervision, Project administration, Investigation, Funding acquisition, Data curation, Conceptualization. **Walter M. Weber:** Writing – review & editing, Supervision, Resources, Project administration, Funding acquisition, Conceptualization.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Data availability

Data will be made available on request.

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