DISSERTATION

Si to SiGe Heterostructure Transistors for Reconfigurable Circuits and Functionality Enhancement via Ferroelectric Gating

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Dipl. Ing. Lukas Wind, BSc

Matr.-Nr. 01426229

unter der Leitung von

Univ.Prof. Dipl.Ing. Dr.-Ing. Walter Michael Weber

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Abstract

Adaptive computing presents a promising solution to meet the increasing computational demands of artificial intelligence (AI), while addressing the challenges of traditional hardware scaling. In this context, reconfigurable field-effect transistors (RFETs) can overcome the limitations of the static nature of CMOS technology by dynamically adapting the hardware to enable more resource-efficient computing and optimize device performance.

RFETs, a special form of Schottky barrier FETs, combine the functionality of n- and p-type transistors in a single device that can be electrostatically switched during operation. As a technology enabler, a novel thermal heterostructure formation technique between Al and Si nanosheets is presented in this work. Thereby, abrupt, single-elementary and single-crystalline Al-Si Schottky junctions are monolithically formed, showing symmetric injection of electrons and holes, ideal for the realization of RFETs with symmetric current-voltage operation modes. The Al contact formation is also conducted towards $Si_{1-x}Ge_x$ nanosheets, where similar structural properties without intermetallic phase formations are achieved. The transport properties are systematically investigated with respect to the stoichiometric $Si_{1-x}Ge_x$ composition, ranging from highly transparent contacts to distinct Schottky barriers, offering potential for a variety of emerging "More than Moore" applications.

The realized Al-Si heterostructure-based RFETs exhibited highly symmetric n- and p-mode operation with low device-to-device variability. This enabled the realization of RFET-based complementary and combinational logic gates, including inverter and runtime switchable NAND/NOR and XOR/XNOR gates. Compared to conventional circuits with static transistors, an increased functionality of the logic circuits is achieved while simultaneously reducing the transistor count. The reliable operation of the logic gates is demonstrated using only a single pair of symmetric supply rails, achieving full output swing and stable state current suppression. Finally, a fully operational 1-bit full adder based on only 8 physically identical RFETs is also demonstrated. By integrating a $Si_{0.67}Ge_{0.33}$ channel and high-κ dielectrics, or implementing multi-channel devices, performance enhancements of the individual RFETs are obtained without severely compromising device symmetry.

To achieve non-volatile programming of the operation state, ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ (HZO) layers are integrated into the RFET gate stack. By polarizing the HZO in the vicinity of the Schottky junction with short voltage pulses, time-stable switching between fully p-type conduction and n-dominant operation is achieved. The modulation strength of the HZO is strongly dependent on the pulse amplitude, allowing access to drive currents associated with multiple polarization states whose stability is verified by retention measurements. This functionality is highly promising for the realization of artificial synapses for neuromorphic computing paradigms. Finally, the combination of RFETs with non-volatile memory capabilities can be an ideal building block to enable versatile Logic-in-Memory hardware to overcome the limitations of "von Neumann" architectures.

Kurzfassung

Adaptives Computing stellt eine vielversprechende Lösung dar, um den steigenden Leistungsanforderungen von künstlicher Intelligenz gerecht zu werden und gleichzeitig die Herausforderungen der traditionellen Hardwareskalierung zu bewältigen. In diesem Zusammenhang können rekonfigurierbare Feldeffekttransistoren (RFETs) die Grenzen der statischen CMOS-Technologie überwinden, indem Hardware dynamisch angepasst wird, um ressourceneffizienteres Rechnen zu ermöglichen und die Geräteleistung zu optimieren. RFETs vereinen dabei die Funktionalität von n- und p-Typ Transistoren in einem einzigen Bauelement, dessen Polarität im Betrieb elektrostatisch umgeschaltet werden kann. Zur Fertigung dieser Transistoren wird hier eine neuartige Methode zur Bildung monolithischer Heterostrukturen präsentiert, die auf einer thermisch induzierten Austauschreaktion von Al und Si Nanostrukturen basiert. Dadurch entstehen abrupte, monoelementare und einkristalline Al-Si Schottky-Übergänge, die eine symmetrische Injektion von Elektronen und Löchern ermöglichen, ideal für die Realisierung von RFETs mit symmetrischen Betriebsmodi. Die thermische Austauschreaktion mit Al kann auch auf $Si_{1-x}Ge_x$ Nanostrukturen erweitert werden, mit ähnlichen Struktureigenschaften und ebenfalls ohne Bildung intermetallischer Phasen. Die elektrischen Transporteigenschaften in den dadurch hergestellten Al-$Si_{1-x}Ge_x$ Heterostrukturen werden systematisch in Bezug auf ihre stöchiometrische Zusammensetzung untersucht. Diese reichen von hochtransparenten Kontakten für Ge bis hin zu ausgeprägten Schottky-Barrieren für SiGe, mit Potenzial für eine Vielzahl neuartiger „More than Moore“-Anwendungen. Basierend auf Al-Si Heterostrukturen werden RFETs gefertigt, die einen hochsymmetrischen n- und p-Betrieb zeigen. Das ermöglicht die Realisierung von RFET-basierten komplementären und kombinatorischen Logikgattern, darunter Inverter-, und rekonfigurierbaren NAND/NOR- und XOR/XNOR-Gatter. Im Vergleich zu herkömmlichen Schaltungen mit statischen Transistoren wird damit eine erhöhte Funktionalität bei gleichzeitiger Reduzierung der Anzahl der Transistoren erreicht. Unter Verwendung einer symmetrischen Versorgungsspannung wird der zuverlässige Betrieb der Logikgatter unter voller Aussteuerung des Ausgangs und guter Stromunterdrückung im stationären Zustand gezeigt. Basierend auf nur 8 physisch identischen RFETs wird zudem ein voll funktionsfähiger 1-Bit Volladdierer demonstriert. Durch die Integration eines $Si_{0.67}Ge_{0.33}$-Kanals und high-κ Dielektrika, oder der Implementierung von Mehrkanal-Bauelementen wird die Leistungssteigerung der einzelnen RFETs angestrebt, ohne die Symmetrie der Bauelemente stark zu beeinträchtigen. Um eine nichtflüchtige Programmierung des Betriebszustands zu erreichen, wird eine ferroelektrische $Hf_{0,5}Zr_{0,5}O_2$ (HZO) Schicht in den Gate-Stapel integriert. Durch kurze Spannungsimpulse am Gate wird das HZO in der Nähe des Schottky-Übergangs polarisiert, wodurch zwischen p- und n-dominantem Betrieb umgeschaltet werden kann. Die Modulation des HZOs ist dabei stark von der Pulsamplitude abhängig und ermöglicht das Einstellen der Drainströme unter der Nutzung mehrerer Polarisationszustände, deren Stabilität durch Langzeitmessungen verifiziert wurde. Diese Funktionalität ist sehr vielversprechend für die Realisierung künstlicher Synapsen für neuromorphe Computerparadigmen. Weiters kann die Kombination von RFETs mit nichtflüchtigen Speicherfähigkeiten eine wertvolle Komponente für die Realisierung von adaptiver "Logic-in-Memory"-Hardware sein, um die Einschränkungen der "von Neumann"-Architekturen zu überwinden.

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List of Abbreviations

1T1C	One-Transistor, One-Capacitor
AI	Artificial Intelligence
Al	Aluminum
Al_2O_3	Aluminum Oxide
ALD	Atomic Layer Deposition
Ar	Argon
Au	Gold
B	Boron
Bi	Bismuth
BOX	Buried Oxide
BHF	Buffered Hydrofluoric Acid
c-Al	Crystalline Aluminum
CB	Conduction Band
CMOS	Complementary Metal-Oxide-Semiconductor
CVD	Chemical Vapor Deposition
C/V	Capacitance-Voltage
CVU	Capacitance-Voltage-Unit
DIBL	Drain-Induced Barrier Lowering
DOS	Density of States
DRAM	Dynamic Random Access Memory
EBL	Electron Beam Lithography
EDP	Energy-Delay Product
EDX	Energy Dispersive X-ray Analysis
Fcc	Face Centered Cubic
FDSOI	Fully Depleted Silicon On Insulator
FE	Field Emission
FE	Ferroelectric
FeFET	Ferroelectric Field Effect Transistor
FEOL	Front End of Line
FeRAM	Ferroelectric Random Access Memory
FeRFET	Ferroelectric Reconfigurable Field Effect Transistor

FeSBFET	Ferroelectric Schottky Barrier Field Effect Transistor
FG	Floating Gate
FTJ	Ferroelectric Tunnel Junction
FET	Field-Effect Transistor
FFT	Fast Fourier Transformation
FPGA	Field Programmable Gate Arrays
GAA	Gate-All-Around
GIDL	Gate-Induced Drain Leakage
GaAs	Gallium Arsenide
GaN	Gallium Nitride
Ge	Germanium
GeO	Germanium Monoxide
GeO_2	Germanium Dioxide
GeOI	Ge-on-Insulator
GNDU	Ground Unit
HAADF	High-Angle Annular Dark Field
H_2O	Water
H_2O_2	Hydrogen Peroxide
HCl	Hydrogen Chloride
HEMT	High Electron Mobility Transistor
HF	Hydrofluoric Acid
HfO_2	Hafnium Oxide
HRSTEM	High-Resolution Scanning Transmission Electron Microscopy
HZO	Hafnium Zirconium Oxide ($Hf_{0.5}Zr_{0.5}O_2$)
IL	Interface layer
I/V	Current-Voltage
LiM	Logic-in-Memory
JKU	Johannes Kepler Universität
MFIS	Metal-Ferroelectric-Insulator-Semiconductor
MFM	Metal-Ferroelectric-Metal
MFMIS	Metal-Ferroelectric-Metal-Insulator-Semiconductor
MIGFET	Multi-Independent Gate Field Effect Transistor
MIGS	Metal Induced Gap States
MLC	Multi-Level Cell
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MW	Memory Window
N	Nitrogen
Ni	Nickel
NDR	Negative Differential Resistance
NW	Nanowire
PDK	Process Design Kit
P/E	Polarization-Electric Field
PMMA	Polymethyl Methacrylat

PPD	Paired-Pulse Depression
PPF	Paired-Pulse Facilitation
Pt	Platinum
PZT	Lead Zirconate Titanate ($Pb(Zr,Ti)O_3$)
RCA	Radio Corporation of America (Standard Set of Wafer Cleaning Steps)
rms	root-mean-square
RTA	Rapid Thermal Annealing
SBFET	Schottky Barrier Field Effect Transistor
SBH	Schottky Barrier Height
SBT	Strontium Bismuth Tantalite ($SrBi_2Ta_2O_9$)
sccm	standard cubic centimeter per minute (atm cm^3/min)
SEM	Scanning Electron Microscopy
Si	Silicon
SiC	Silicon Carbide
SMU	Source Measure Unit
Sn	Tin
SOI	Silicon on Insulator
SPICE	Simulation Program with Integrated Circuit
STDP	Spike-Timing-Dependent Plasticity
STEM	Scanning Transmission Electron Microscopy
TaN	Tantal Nitride
TCAD	Technology Computer Aided Design
TE	Thermionic Emission
TEMAHf	Tetrakis(ethylmethylamino)hafnium
TEMAZr	Tetrakis(ethylmethylamino)zirconium
TER	Tunneling Electroresistance
TFE	Thermionic Field Emission
Ti	Titanium
TiN	Titanium Nitride
TiO_2	Titanium Oxide
TMA	Trimethylaluminum (TMA)
VB	Valence Band
VLS	Vapor-Liquid-Solid
VMU	Voltage Measurement Unit
VSU	Voltage Source Unit
Y	Yttrium
ZMNS	Center for Micro- and Nanostructures
ZrO_2	Zirconium Oxide

Chapter 1

Introduction

Over the past few decades, the demand for both computing power and energy consumption has experienced dramatic growth, driven by a variety of technological, economic, and societal factors. Especially the growing interest in the development of intelligent computing, with the rise of artificial intelligence (AI), machine learning and big data analytics, the demand for computing power has increased even more [1]. These fields require extremely high levels of computational power, consuming huge amounts of energy and causing an immense carbon footprint, especially for training large AI models and running complex simulations [2, 3].

The semiconductor industry has long relied on the scaling of traditional field-effect transistors (FETs) to improve the performance of integrated circuits, following Moore's law [4], which predicts a doubling of transistor density and performance every 18 to 24 months. However, as transistor dimensions approach their fundamental physical limits, the benefits from simple scaling are diminishing. Issues such as increased power consumption, leakage currents, and short-channel effects, along with the difficulty in maintaining reliable performance at smaller sizes, are pushing the boundaries of conventional FET technology [5–7]. These challenges underscore the need for innovative alternatives to traditional FET architectures to enhance circuit performance without solely depending on further miniaturization. In recent years, this has driven the semiconductor industry to a number of technological innovations, including the introduction of high-κ gate dielectrics [8], strain enhancement of mobility [9], and improved gating architectures [10]. In the near future, this will perspectively also include the integration of alternative high-mobility channel materials, a transition to gate-all-around (GAA) architectures and 3D integration schemes [11].

In conventional complementary metal-oxide-semiconductor (CMOS) technology, logic circuits are based on the combination of two opposing types of transistors, the n-type and p-type transistors for electron- and hole-induced conduction, respectively. These two types

of transistors are fundamentally different in terms of the selection of doping, geometric dimensions and used material combinations. All these differences result in increased technological complexity in the production of CMOS circuits. In addition, since the polarity of the individual transistors is predetermined during the fabrication process, the functionality of the circuit is also fixed and static. In view of the arising computational constraints for neuromorphic applications, hardware security and edge computing, novel device and circuit methods are being studied that would benefit from a functional diversification of the elementary switching unit, the FET.

Alternative FET designs, particularly reconfigurable FETs (RFETs), present promising solutions to address many of the limitations of rigid conventional CMOS technologies. This emerging device concept is capable of switching its polarity between n-type and p-type operation during runtime, therefore combining the functionality of two physically different FETs into one. The polarity of the multifunctional device can be selected by an electrical signal typically applied on an additional gate electrode, the so-called polarity or program gate (PG). In contrast to conventional MOSFETs with doped transistor channels and degenerately doped contacts, RFETs rely on the unique properties of Schottky junctions and do not require any doping [12]. With the PG controlling the Schottky barrier, the desired charge carrier type can be filtered, allowing either the flow of electrons or holes for n- or p-type conduction. The second gate, the control gate (CG), modulates the channel conductance to switch the transistor between the on and off states, similar to the gate of a conventional MOSFET [13]. The functional diversification at the device level is highly promising to increase the functional density on chip without further scaling of the individual components. Utilizing these RFETs in logic circuits, a "fine-grain" reconfigurability of circuits can be achieved, efficiently adapting its logic function during runtime. This is fundamentally different to the conventional "coarse grain" approach in field programmable gate arrays (FPGAs), where the signal is routed to predefined logic and memory blocks, resulting in an overall large routing delay, chip area and power consumption [14]. By changing the polarity of the RFETs in a pull-up and pull-down network, the polarity of the entire circuit can be inverted, thus switching between the functionality of two logic functions, e.g., NAND/NOR or XOR/XNOR, without increasing the number of transistors [15, 16]. As a consequence, many circuits can be designed more efficiently, which means that the number of transistors required can be significantly reduced, with positive effects on performance, chip area and energy efficiency [17–20]. In particular, RFETs allow the compact realization of XOR and MAJ rich logic circuits, which are very complex and inefficient to implement with conventional CMOS technology [21, 22].

The polymorphic RFET concept further shows high potential for a variety of applications beyond the general computing paradigm. Co-integrated into classical CMOS platforms, it can be utilized for emerging hardware security approaches to prevent theft of chip intellectual property [23]. Polymorphic gates can be used in camouflaging or logic locking schemes to obfuscate the circuitry from malicious entities [13,24,25]. Furthermore, RFETs have also gained increased attention in analog and mixed-signal circuit applications [26–28]

Another major point of interest is the transition to alternative channel materials, not only in RFETs but also for classic CMOS technology. Ge, with its higher electron and hole mobility compared to Si, coupled with a significantly lower band gap, can deliver higher on-state currents [29]. Therefore, it offers the potential for faster switching speeds and improved performance in high-frequency and low-power applications [5,30]. In this regard, $Si_{1-x}Ge_x$ layers are already integrated as channel material in PMOS to boost the mobility of the devices [11]. Ge also offers new possibilities for "More-than-Moore" paradigms to extend the Si platform [31]. These include direct integration of optoelectronic devices [32], negative differential resistance (NDR) devices [33, 34] or Josephson field-effect transistors [35]. However, many technological challenges are still present for the integration of Ge channel devices [31]. The instability of the Ge surface requires complex engineering of the interface towards high-κ gate dielectrics to ensure a low density of trap states [30]. Strong Fermi level pinning of metal/Ge interfaces [36] has also been a major limitation in achieving high n-type currents in NMOS devices as well as RFETs, where it leads to highly asymmetric on-state currents [37, 38].

To target the immense power consumption of deep learning algorithms and big data analytics, novel Logic-in-Memory (LiM) architectures and neuromorphic computing paradigms can be a possible solution [39]. In general, modern computing uses large amounts of resources to move data between the processing unit and memory elements. In these emerging but very data-intensive applications, this ultimately limits computing performance due to the "von Neumann" bottleneck [40]. LiM implementations however rely on computing units that can also locally store information, drastically reducing the data transfer [41–43]. Especially since the discovery of the ferroelectric phase in HfO_2-based layers [44], which are well scalable and integrable into CMOS processes [45], the use of ferroelectric-based memories and non-volatile FETs is very promising for LiM applications [42, 46] and neuromorphic devices [47–49]. Integrated into the gate stack of an RFET, it could be utilized for a non-volatile programming of the operation mode of the device. This hybrid concept, combining the non-volatile memory element with the RFET-based polymorphic logic gates, can lead to the realization of adaptive universal logic-in-memory cells [50].

1.1 Motivation and Scope

Reproducible contact formation towards $Si_{1-x}Ge_x$ nanosheets

For the fabrication of Schottky barrier FETs (SBFETs), a reliable and reproducible contact formation of the metal towards the nanoscaled semiconductor transistor channel is of utmost importance. In particular, well-defined Schottky junctions are key for the realization of RFETs that rely on the electrostatic tuning of the formed Schottky barrier.

The metal-silicide formation using e.g., Ni or Co [51–53] is a well established method in the semiconductor industry for forming electrical contacts to Si. However, due to the complex phase systems with intermetallic phases of various stoichiometric compositions, different phase stabilization techniques as well as precise process control of the thermal treatment are required to achieve reproducible contact properties [54, 55]. This especially holds true for the formation of metal germanides (e.g., with Ni, Co, or Cu), as these generally exhibit lower stability [51, 56, 57]. When transferring these processes to $Si_{1-x}Ge_x$ alloys, the complexity increases even further with the formation of different germano-silicides [58].

Al could therefore be an interesting alternative to form pure metal contacts towards the $Si_{1-x}Ge_x$ transistor channel. Although Al has been discarded by the semiconductor industry as a contact material to bulk Si due to reliability concerns regarding electromigration [59], void formation [60] or spiking [61], recent advances in contacting Ge nanowires (NW) [62, 63] and nanosheets [LW17] have been promising and have not shown the aforementioned issues. Moreover, ultra-scaled devices with abrupt metal-semiconductor interfaces have been achieved at reduced process complexity [64].

Analysis of the transport properties of Al-$Si_{1-x}Ge_x$ heterostructures of varying stoichiometric compositions

The integration of Ge as a transistor channel material can be advantageous for a variety of different applications, from boosting the performance in classical CMOS devices to various “More than Moore” applications. Analyzing $Si_{1-x}Ge_x$ of various compositions, it is of interest how the stoichiometric composition influences the contact formation as well as the electrical transport properties of the formed heterostructure.

Realization of RFETs with symmetric on-states for the integration in adaptive combinational logic

In recent years, the growing interest in RFETs has given rise to various device concepts and channel materials for their realization [65]. While first concepts were mainly based on carbon nanotubes [66] or Si NW-based channels [67–69], commonly in combination with Ni-silicide contacts, later implementations have already transitioned to top-down fabricated platforms for a more industry-related approach [14, 70–72]. Concepts using 2D channel materials, such as graphene [73], WSe_2 [74] or $MoTe_2$ [75] have also been successfully demonstrated [76]. RFETs based on Ge channels have also been realized, but suffer

from increased asymmetric on-states due to the strong Fermi-level pinning of the metal-Ge interface towards the valence band edge [37, 38]. In general, achieving symmetrical operation of n- and p-mode is a major challenge, which is one of the main requirements for practical use in RFET-based circuits [13]. In this regard, strain engineering was shown to be a viable approach to improve symmetry [77, 78].

Targeting circuit implementations based on RFETs, several research groups have demonstrated their potential in terms of increased functional density and improved critical path delay by utilizing simulations [17, 79–81]. However, actual physical on-chip implementations are rare, as fabricating symmetric RFETs with sufficient yield on a scalable top-down platform appears to be challenging. In this regard, a top-down fabrication scheme and aiming for high yield and reproducibility, the realization of RFET-based complementary and combinatorial logic gates is aimed at.

Ferroelectric layer integration into RFETs for non-volatile applications

To further enhance the SBFETs, and in particular the RFET, the integration of a ferroelectric layer into the gate stack is targeted. This is intended to achieve non-volatile programming of the operation mode, which is maintained even if no permanent voltage is applied to the PG. This can be an important building block for realizing reconfigurable logic cells for adaptive LiM computing. Based on charge trapping layers, non-volatile reconfigurable devices have already been demonstrated in poly-Si [49] and 2D WeS_2 channel devices [82]. However, a transition to ferroelectric-based devices should result in a reduction of the operation voltages and latencies, as well as an enhanced device endurance [83]. In addition, ferroelectric layers can enable gradual switching for multiple output states, which could lead to the development of artificial synapses for neuromorphic applications [47]. In this regard, ferroelectrically enhanced single gated FETs [84] or SBFETs [48, 85] have already shown promising results.

1.2 Outline

Chapter 2 provides the theoretical background for this work, including the state-of-the-art and ongoing research topics in the associated material and device fields for the thesis topic. Starting from the underlying materials for the transistor channel and gate dielectrics, the physics behind the heterostructure formation process and the carrier transport through metal-semiconductor junctions is elaborated. Subsequently, the different device concepts, including the general SBFET, as well as novel RFETs and ferroelectric FETs (FeFETs) are introduced.

Chapter 3 describes the experimental techniques for the fabrication of the different devices as well as the main methods for their electrical characterization and evaluation.

Chapter 4, as the first results chapter, starts with the investigation of a novel Al-Si heterostructure formation process, thereby analyzing the structural and electrical properties by their integration into an SBFET architecture. Furthermore, Al-Si-based RFETs are systematically investigated before they are integrated into complementary and combinational logic gates, such as inverters and reconfigurable NAND/NOR and XOR/XNOR gates. Finally, RFETs with multiple parallel transistor channels as well as Al as an alternative top gate material are presented.

Chapter 5 analyzes the contact formation of Al to $Si_{1-x}Ge_x$ nanosheet channels with varying stoichiometric composition. Furthermore, the electrical transport properties of the Al-$Si_{1-x}Ge_x$-Al-based SBFETs in respect to the Ge content are investigated. The integration of a Ge-rich nanosheet channel into the RFET architecture is then investigated using different gate dielectrics (SiO_2, HfO_2). In addition, the Si and $Si_{0.67}Ge_{0.33}$-based RFETs from this work are compared with state-of-the-art RFETs from the literature.

Chapter 6 first provides a short study using capacitive test structures to optimize the ferroelectric phase in $Hf_{0.5}Zr_{0.5}O_2$ (HZO) layers. Subsequently, the HZO film is employed in Si-channel SBFET and RFETs, where its non-volatile switching behavior is analyzed using variable pulse amplitude and retention measurements.

Chapter 7 finally summarizes the key findings of this work and provides an outlook on further research topics and improvements aiming to push the presented concepts towards a large-scale integration.

Chapter 2

Theoretical Background

This chapter discusses the theoretical background that serves as the basis for further discussion of the results, including the state-of-the-art research. The first part, Section 2.1, covers the properties of Si and Ge and their use as channel materials in transistors. Furthermore, the gate dielectric materials relevant for this work and their influence on the scalability of devices are discussed in Section 2.2. The latter also includes a detailed discussion of the ferroelectric effect and the fabrication of ferroelectric layers, with the main focus on hafnium zirconium oxide (HZO).

Section 2.3 covers the formation of metal-semiconductor heterostructures using diffusion and solid-state reactions. The electrical properties of the thereby obtained Schottky junctions are discussed, with special attention to the involved transport mechanism.

Based on this, Section 2.4 shows the state-of-the-art integration of such metal-semiconductor heterostructures into Schottky barrier field-effect transistors (SBFETs). The reconfigurable FET (RFET) as an emerging device concept based on the SBFET is introduced in Section 2.5, where its working principle, scaling prospects and circuit applications are discussed. Finally, Section 2.6 addresses the integration of ferroelectric layers for the realization of non-volatile ferroelectric FETs (FeFETs) and their potential fields of application.

2.1 Semiconductor Channel

The semiconductor industry has undergone significant advances, driven by the increasing demand for faster, smaller and more energy efficient electronic devices. Silicon (Si) has traditionally dominated this field due to its abundant availability and favorable as well as stable electronic properties. However, germanium (Ge) and Ge-rich silicon-germanium ($Si_{1-x}Ge_x$) alloys have gained attention for their potential to further enhance the performance of semiconductor devices [11].

Up-to-date, Si is the most commonly used semiconductor material in electronics, with Si-based devices occupying around 90 % of the worldwide market [86]. As a group-IV semiconductor with an indirect band gap of 1.12 eV at room temperature (see Figure 2.1(a)), it is well suited for a variety of applications, including transistors, diodes and solar cells. Bulk Si crystallizes in a face-centered cubic (fcc) diamond structure with a lattice constant of $a_{Si} = 0.5431\,\text{nm}$ [87]. A unique feature of Si among semiconductor materials is the formation of a stable, high-quality oxide (SiO_2). This oxide not only protects the surface from degradation but also provides a low surface state density at the Si-SiO_2 interface [88]. Combined with its excellent processability, this has enabled the high-density and large-volume fabrication of modern semiconductor devices [89].

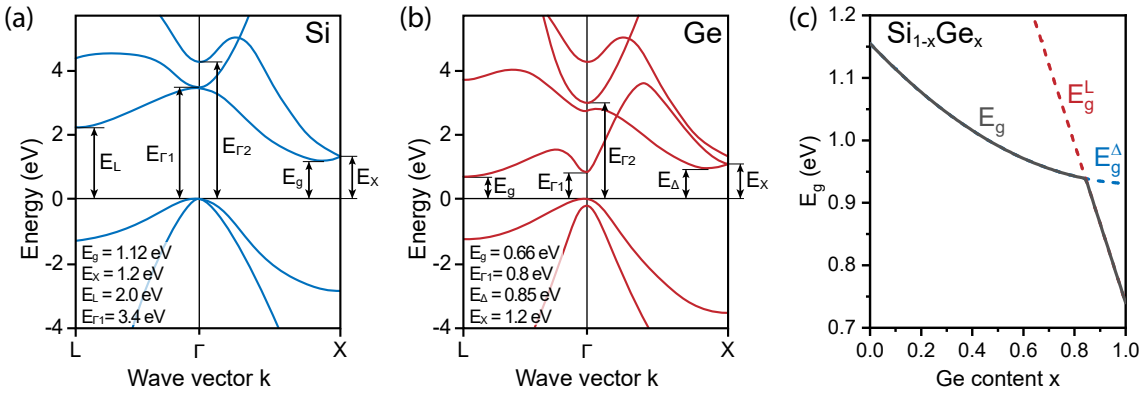

Figure 2.1: Energy band structure of different group-IV bulk semiconductors. (a) Energy band structure of Si, adapted from [90]. (b) Energy band structure of Ge, adapted from [91]. (c) Energy band gap E_g as a function of the Ge content [92].

Ge, the group-IV semiconductor material with the next higher nuclear mass, is also commonly used, sharing similar properties with Si and also crystallizing in a diamond lattice, with a larger lattice constant of $a_{Ge} = 0.5658\,\text{nm}$ [87]. For this work it is particularly interesting due to its lower indirect band gap of $E_g = 0.66\,\text{eV}$ and its exceptionally high electron and hole mobilities of $3900\,\text{cm}^2/(\text{Vs})$ and $1900\,\text{cm}^2/(\text{Vs})$ in $\langle 100 \rangle$ direction, respectively [30]. The carrier mobilities are therefore significantly higher compared to Si ($\mu_e = 1500\,\text{cm}^2/(\text{Vs})$, $\mu_h = 500\,\text{cm}^2/(\text{Vs})$ [30]), with the hole mobility even being the highest of all known bulk semiconductors at room temperature [29]. These properties can lead to enhanced performance metrics in electronic in terms of increased drive currents, as well as novel optoelectronic devices [11,93]. Table 2.1 provides an overview of the

	Si	Ge	SiC (4H)	GaN	GaAs
Band gap E_g (eV)	1.12	0.66	3.26	3.45	1.42
Electron affinity χ (eV)	4.0	4.05	3.1	4.1	4.07
Electron mobility μ_e ($cm^2/(Vs)$)	1500	3900	1000	1250	8500
Hole mobility μ_h ($cm^2/(Vs)$)	450	1900	115	850	400
Breakdown field E_{BD} (MV/cm)	0.3	0.1	2.2	2	0.06
Dielectric constant ε_r	11.9	16	10.1	9	13.1
Therm. conduct. λ (W/(K cm))	1.3	0.58	4.5	2.2	0.56
Lattice constant a (nm)	0.543	0.565	0.307	0.518	0.565

Table 2.1: Bulk properties of Si and Ge, compared to commonly used wide (SiC and GaN) and direct band gap materials (GaN, GaAs) at room temperature [30, 87, 94, 95].

most important properties of Si and Ge, compared to other commonly used semiconductor materials.

Despite these excellent electrical properties, and the fact that the very first bipolar transistor ever built, i.e., by Bell Labs in 1948 [96], was based on Ge, Si has nevertheless prevailed in applications. One of the main reasons for this is that, unlike Si, Ge lacks the formation of a stable native oxide. Instead, the native Ge oxide can be composed of various Ge_xO_y suboxides depending on the oxidation conditions, temperatures and pressure [97], with some suboxides being water soluble and thermally unstable. While GeO_2 would be the preferred oxidation state to reduce interface trap density (D_{it}), it reacts with the Ge interface at ~673 K and decomposes into GeO and other suboxides. This results in the formation of a high density of dangling bonds and oxide defects, which severely degrade device performance, e.g., increasing leakage currents and reducing charge carrier mobilities [29]. For Ge devices, the formation of high-quality (high-κ) dielectric layers with a low D_{it}, in the order of magnitude of state-of-the-art Si technology, is therefore of utmost importance [29].

Comparing the band structures of bulk Si and Ge in Figure 2.1, it can be seen that the conduction band (CB) minimum of Si is located off-centered and near the X point along the $\langle 100 \rangle$ directions (referred as the Δ minima), while Ge has its minima in the $\langle 111 \rangle$ directions (L valley) [98]. The valence band (VB) maxima for both elements is in the Γ point. Interestingly, for Ge, the minimum of the CB in the Γ point with $E_{\Gamma 1} = 0.8\,\text{eV}$ is only slightly higher than the one located at the L valley giving an indirect band gap ($E_g = 0.66\,\text{eV}$). Note that by applying high uniaxial tensile strain [99] in $\langle 111 \rangle$ direction or by incorporating Sn (>8 % Sn) into the Ge lattice [100, 101], it is possible to achieve direct band gap transitions in Ge, which is highly interesting for on-chip integration of optoelectronic devices into CMOS platforms [32]. In addition, the energy difference between the two lowest CBs with 0.19 eV is also very small. By applying sufficiently high electric fields, electrons can be transferred from the L-valley of the first CB to the X-valley of the second, which is leading to a change in effective mass. This effect is known as the Gunn effect [102], leading to device characteristics with negative differential resistance

(NDR), which can be utilized to enable novel device concepts, such as multi-value logic [33, 34, 103][LW5], enhanced photodetectors [104] or THz-oscillators [105].

Since high-quality Ge or Ge-on-Insulator (GeOI) wafers are scarce and expensive, a direct integration of ultra-thin Ge layers into the mainstream Si CMOS platform is favorable. However, the direct growth of Ge layers on Si is challenging due to the lattice mismatch of about 4 % [29]. Common heteroepitaxy growth techniques therefore are molecular beam epitaxy (MBE) [106–108] or chemical vapor deposition (CVD) [109, 110]. Typically, thick $Si_{1-x}Ge_x$ buffer layers are grown to accommodate the lattice mismatch. Furthermore, a precise control of the growth temperature and pressure is required to prevent segregation effects during the crystallization.

Due to the similar crystal properties of Si and Ge, the two materials can be mixed in arbitrary stoichiometric compositions to form $Si_{1-x}Ge_x$ alloys, where $0 \leq x \leq 1$. By changing the Ge concentration, important electrical properties of the material, such as the energy band gap or charge carrier mobilities, can be engineered. Since the conduction band minima of Si and Ge are localized differently, the band minimum of $Si_{1-x}Ge_x$ transitions from the Δ-band to the L-band at Ge concentrations higher than 85 % for unstrained layers. Weber et al. [92] used low temperature photo-luminescence measurements to analytically describe the $Si_{1-x}Ge_x$ band gap E_g depending on the Ge content x by

$$\begin{aligned} E_g^{\Delta}(x) &= 1.155 - 0.43x + 0.206x^2 \;\; eV \qquad && 0 \leq x \leq 0.85 \\ E_g^{L}(x) &= 2.01 - 1.27x \;\; eV && 0.85 < x \leq 1 \end{aligned} \tag{2.1}$$

including the transition from the Δ to the L band. The entire band structure, and thus the band gap E_g of $Si_{1-x}Ge_x$ however is significantly influenced by the strain of the material. In general, compressive in-plain strain of $Si_{1-x}Ge_x$ alloys pseudomorphically grown on an Si (100) substrate leads to a monotonic decrease of the indirect band gap [98] and thus an increase in carrier mobilities [111]. Therefore, the integration of Si-$Si_{1-x}Ge_x$ heterostructures is a common method to engineer the strain of Si (or $Si_{1-x}Ge_x$) layers and enhance carrier mobilities and thus the device performance [9, 93]. For p-type FETs in particular, the incorporation of $Si_{1-x}Ge_x$ layers to increase the otherwise low hole mobility of Si is highly relevant and is already used in current CMOS technology [9, 11].

When a thin $Si_{1-x}Ge_x$ layer is vertically confined, e.g., in vertical Si-Ge-Si heterostructures, the band structure of this layer is significantly modified compared to a bulk material. In addition to the strain-induced effects of the lattice mismatch between the different layers described above, band discontinuities occur at the Si-Ge interfaces. In the case of a compressively strained $Si_{1-x}Ge_x$ layer grown between two relaxed Si layers, with the $Si_{1-x}Ge_x$ layer thus having a smaller band gap than the Si layer above and below, this results in a type I band alignment and the formation of a quantum well for holes. On the other hand, a Si layer grown on a relaxed $Si_{1-x}Ge_x$ layer undergoes tensile strain, resulting in a type II band alignment and the formation of a quantum well for electrons [112, 113]. Moreover, quantum confinement in the thin Ge layer thus modifies the density

of states (DOS). While in bulk 3D semiconductors, the DOS continuously increases above (beyond) E_C (E_V), the DOS in 2D confined systems is split into discrete terraces of constant value. The spacing of these terraces increases with decreasing width of the quantum well (thickness of the sandwiched layer) [112, 114]. These heterostructure quantum wells can be used to engineer the band gap and carrier mobilities to realize, e.g., high electron mobility transistors (HEMTs) for high-frequency applications [98, 112]. In addition, SiGe quantum wells with periodically oscillating Ge content have recently been used to demonstrate quantum dot qubits [115].

By lowering the band gap, the source-drain leakage is increased, and therefore the on- to off-current ratio (I_{on}/I_{off}) in FETs generally decreases, which can be estimated with [116]

$$\frac{I_{on}}{I_{off}} \approx \frac{1}{4} \exp\left(\frac{E_g}{2k_B T}\right). \tag{2.2}$$

Consequently, Si channel FETs can achieve I_{on}/I_{off} ratios of around 6×10^9, while the modulation of Ge-based FETs is limited to less than 10^5 due to an exponential increase in off-currents. This estimation, which only considers the band gap energy E_g of a device, is in fact a very robust measure for devices that do not involve Schottky barriers [116]. However, for devices that inherit Schottky barriers and field modulation, these barriers must also be taken into account, as it will be shown in Equation 2.22 in Section 2.3.2.

2.2 Gate Dielectrics

High-quality dielectrics are crucial in MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors), as they directly influence the device's performance, reliability, and scalability. The gate dielectric layer serves as an insulator that separates the gate from the channel, enabling precise control of the channel's conductivity.

As already mentioned in the previous section, the use of SiO_2 as a gate dielectric in combination with Si as transistor channel material has dominated the semiconductor industry, as it basically fulfills all requirements for a high quality gate dielectric. As a high band gap material ($E_g \approx 9\,\text{eV}$) with appropriate offsets to the CB- and VB-edges of Si (see Figure 2.2(b)), and a high stability against electrical breakdown ($E_{BD} \approx 1 \times 10^3\,\text{MV/cm}$ [90]), it achieves excellent insulating properties. Furthermore, it provides a low interface state density, such that the oxide capacitance C_{ox} is much larger than the capacitance related to the interface traps C_{it} ($C_{ox} \gg C_{it}$), which is essential for a proper switching of MOSFETs [114]. As a native oxide of Si, its formation is also straightforward, fabricated by simple oxidation of the Si surface using dry thermal, hydrothermal or chemical processes. However, one of the main restrictions of using SiO_2 is its relatively low dielectric constant ($\varepsilon_r = 3.9$). According to Dennard's constant field scaling [117], as MOSFETs are scaled down to smaller dimensions, also the thickness of the gate oxide has to be thinned to maintain sufficient electrostatic control of the transistor channel. The required ultra-thin layer thicknesses t_{ox} for SiO_2 would thereby lead to significantly increasing gate leakage

currents, which become intolerable at $t_{ox} \lesssim 1.5\,\text{nm}$ [114]. To address these limitations, the semiconductor industry has turned to high-κ dielectrics, which have a higher dielectric constant, allowing for thicker insulating layers without sacrificing capacitance.

2.2.1 High-κ Dielectrics

Materials such as hafnium oxide (HfO_2) and zirconium oxide (ZrO_2) have emerged as promising candidates for high-κ dielectrics in scaled MOSFETs due to their significantly higher dielectric constants (typically in the range of 20 to 25 in an amorphous state) compared to SiO_2. Al_2O_3 is also worth mentioning, as it also achieves more than twice the permittivity of SiO_2 at a slightly smaller band gap. The electrical properties of SiO_2 and other commonly used high-κ materials are compared in Table 2.2. These materials offer better control over leakage currents and enable the continued scaling of transistors in advanced technology nodes. It is important to mention that the crystallinity of the insulator materials strongly influences the relative dielectric constant ε_r. For MOSFETs, mainly amorphous dielectrics are considered to avoid grain boundary leakage.

As MOSFETs are capacitively operated devices, their drain current in the ohmic and saturation regions is directly proportional to the gate capacitance. In a plate capacitor structure geometry, the geometrical oxide capacitance per area can be simply expressed by

$$C_{ox} = \frac{\varepsilon_0 \varepsilon_r}{t_{ox}}\,, \tag{2.3}$$

including the vacuum permittivity ε_0. When changing from a SiO_2 gate oxide to a high-κ dielectric, the same capacitance can be achieved with increased layer thickness $t_{\text{high-}\kappa}$. This is a highly effective approach to reduce the tunneling currents, as the probability of direct tunneling decreases exponentially with increasing insulator thickness. To facilitate a direct comparison of the used alternative gate dielectric to SiO_2, the *equivalent oxide thickness* (EOT) is introduced. Its value represents the thickness of a pure SiO_2 layer that would yield the same capacitance as the given high-k dielectric of the thickness $t_{\text{high-}\kappa}$, excluding interface charges and depletion capacitances, and is calculated by [121]

$$EOT = t_{\text{high-}\kappa} \cdot \frac{\varepsilon_{\text{high-}\kappa}}{\varepsilon_{SiO_2}}\,. \tag{2.4}$$

Note that a higher dielectric constant of the gate electric also positively influences the gating efficiency in terms of a reduced screening length λ, which will be discussed later in Section 2.4.

	SiO_2	GeO_2	Si_3N_4	Al_2O_3	HfO_2	ZrO_2	TiO_2
Dielectric constant ε_r	3.9	7	7	9	25	25	80
Band gap E_g (eV)	9	5.8	5.3	8.8	5.8	5.8	3.5
CB offset ΔE_C (eV)	3.5	-	2.4	2.8	1.5	1.4	0

Table 2.2: Properties of common gate dielectric materials in amorphous states, including the relative dielectric constants ε_r, band gaps E_g and the conduction band edge offsets ΔE_C towards Si [30, 118–120].

To maintain a strong electrostatic control over the channel while keeping gate leakage currents at acceptable levels, the dielectric material must have both a sufficiently high dielectric constant and low leakage characteristics. Therefore, a high band gap of the materials is a key factor to withstand the electric fields that develop across the dielectric and prevent the injection of electrons or holes from the gate into the semiconductor channel. However, as the dielectric constant of a material tends to vary with its band gap, with $E_g \sim \sqrt{1/\varepsilon_r}$, there is always a trade-off between these two parameters. This trade-off is also shown in Figure 2.2(a), with the band gap in relation to the dielectric constant for different dielectric materials [118].

The alignment of the dielectric band gap is not always centered towards the one of the semiconductor channel. Therefore, the injection barriers for electrons and holes can vary depending on the choice of the materials. The band alignment of different dielectrics towards Si is shown in Figure 2.2(b). To ensure a stable device operation, the injection barrier for both charge carrier types should be larger than 1 eV for Si. Since the conduction band offsets (ΔE_C) are generally lower than the ones for the valence bands (ΔE_V), the choice of materials is generally limited to those with $E_g > 5\,\text{eV}$ [118]. TiO_2, for example, would give excellent high-κ properties with $\varepsilon_r \sim 80$, but does not provide any barrier for electron injection.

Interestingly, the transition from SiO_2 to high-κ materials in semiconductor technology is also an opportunity for the integration of alternative channel materials such as Ge or III-V semiconductors, as the formation of the gate oxide no longer relies solely on the direct growth of SiO_2 on Si [30, 118].

The most common high-κ deposition methods are atomic layer deposition (ALD) or chemical vapor deposition (CVD), both capable of producing high qualitative and pin-hole free insulators at highly conformal coverage, even for complex geometries such as FinFETs

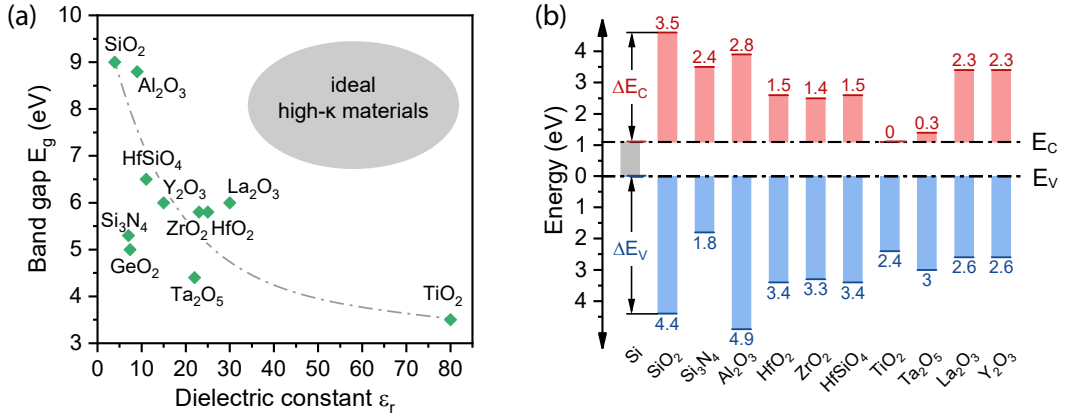

Figure 2.2: (a) Relation of the energy band gap E_g and the dielectric constant ε_r of common high-κ dielectric materials in amorphous states. (b) Band alignment of the dielectric materials towards the energy band gap of Si. Figure adapted from [118].

and gate-all-around (GAA) nanowire (NW) and nanosheet FETs. Despite the low growth rate, ALD with its cyclic growth process is usually the preferred method. As the individual cycles and involved half-reactions are self-limiting due to the surface chemistry, the deposited layer thickness can be precisely controlled, which also enables the fabrication of ultra-scaled layers. Furthermore, it produces the most conformal films, ideal for covering structures with high aspect ratios, such as deep trench capacitors [122, 123]. Sputter deposition of high-κ dielectrics is also possible, but the resulting films often suffer from bad conformal coverage [118].

The direct integration of high-k dielectrics into gate stacks also presents challenges in terms of material stability, interface quality, and compatibility with existing fabrication processes. Dielectrics deposited with high defect densities or poor interface quality can lead to increased gate leakage, reduced breakdown voltage, and degraded device performance. For instance, defects in the dielectric can create localized percolation paths for the current to flow, e.g., by Poole-Frenkel emission or trap-assisted tunneling [8], leading to higher power dissipation, performance degradation, and even device failure over time. Furthermore, the quality of the dielectric-semiconductor interface is crucial, as any roughness, traps, or other imperfections can undermine the reliability and the electrostatic integrity of the MOSFET gate control. In general, high-κ dielectrics have a significantly higher density of defect states compared to thermal SiO_2 or Si_3N_4.

For Ge channel MOSFETs, for example, the formation of stable interface layers is highly important to prevent the formation of unstable GeO_x, as well as interdiffusion with the deposited high-κ dielectric [30]. In this regard, the use of interface layers between Ge and the high-κ prior to the high-κ deposition is a common method to obtain a low interface density and maintain high carrier mobility. There are different passivation and interface layer approaches reported in the literature. Controlled thermal oxidation of the Ge surface can produce GeO_2/Ge interfaces with low D_{it} [124]. The nitridation of the Ge surface, e.g., forming Ge_3N_4 [125, 126] or GeO_xN_y [127] surfaces, is also a viable method to improve the interface stability and the EOT in Ge MOS capacitors. Another technique for Ge surface passivation is to grow a thin Si passivation layer in the range of a few monolayers, e.g., by SiH_4 annealing [128] or Si epitaxial growth [129], which is then typically oxidized to form a SiO_2 prior to the high-κ dielectric deposition [130].

But also for Si devices a (native) interface oxide layer is commonly formed between the semiconductor surface and the high-κ to stabilize the surface. This interface layer however increases the EOT and must be taken into account when trying to achieve ultra-low EOT values. A method to thin down the SiO_2 interfacial layer is the oxide scavenging process, where oxygen is "sucked out" of the interface layer and reacts with a scavenger metal such as Hf or Ti [118, 131].

2.2.2 Ferroelectric Materials

Ferroelectricity is a characteristic of certain materials, typically crystals, that exhibit spontaneous electrical polarization. This means that these materials have a natural dipole moment that can be reoriented by applying an external electric field. This phenomenon arises from a non-centrosymmetric arrangement of atoms within the crystal unit cell, leading to the formation of natural electric dipoles. As these materials are capable of preserving the dipole orientation even after removing the externally applied electric field, ferroelectric materials are highly interesting for memory applications [132, 133].

Ferroelectric materials are classified in one of the 21 different non-centrosymmetric crystal point groups, meaning they lack inversion symmetry. As they are characterized by permanent dipoles, ferroelectrics must also feature piezoelectricity (linear response of charge development on the applied mechanical stress) and pyroelectricity (charge development when changing the materials temperature). All other crystal point groups, including purely piezoelectric or pyroelectric crystals, do not feature a reorientable, permanent dipole moment [132]. In uniaxial ferroelectrics, the dipoles can be switched by 180°, allowing two polarization states. A region within the material of uniform and aligned polarization is called a ferroelectric domain. These domains form due to the inherent instability of the polarization state in the material, which can exist in different orientations. The presence of domains allows the material to minimize its overall energy by accommodating various polarization states that arise from external influences such as mechanical stress, temperature changes, or electric fields. Many ferroelectric materials are biaxial, allowing polarization along multiple crystallographically identical axes. In orthorhombic crystals, for example, the polarization vector forms along the <110> directions, allowing an angle difference between neighboring domains of 60°, 90° or 180° [132]. Figure 2.3(a) shows the dipole formation in an orthorhombic fluorite-type crystal (crystallographic space group $Pca2_1$) in two different polarization states.

In a classic dielectric material, the electrical polarization P is linearly proportional to the applied electric field E, given by

$$P = \varepsilon_0(\varepsilon_r - 1)E = \varepsilon_0\chi_e E \tag{2.5}$$

with the electrical susceptibility χ_e, related to the relative permittivity ε_r of the dielectric material with $\chi_e = \varepsilon_r - 1$. Since ferroelectric materials exhibit spontaneous electrical polarization with reorientable dipoles, their polarization also depends on the previously applied electric fields and their induced remnant polarization. This results in a characteristic hysteresis loop as shown in Figure 2.3(b).

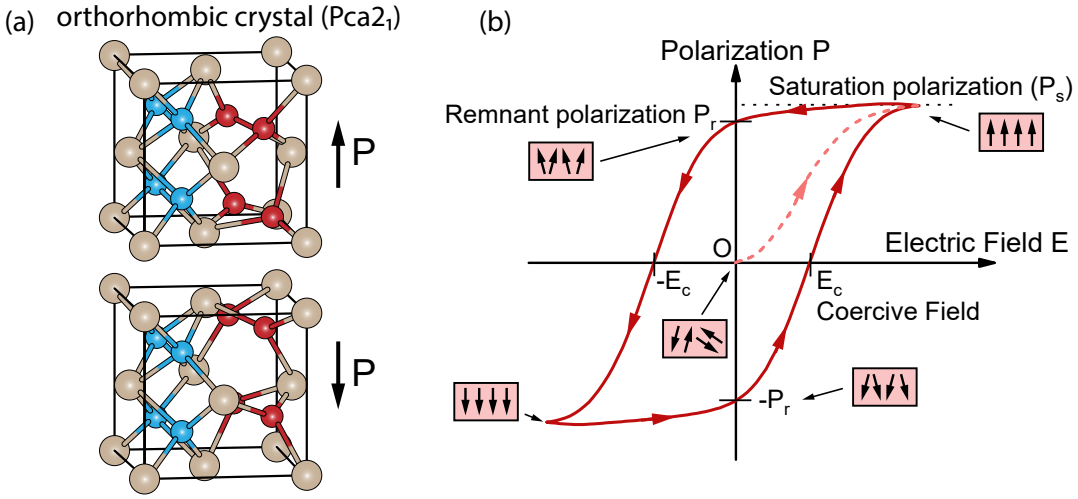

Figure 2.3: (a) Ferroelectric orthorhombic crystal lattice ($Pca2_1$) in two different states of polarization. In case of HZO, Hf/Zr atoms are represented in gray, O atoms in blue, and the shifting O atoms mainly responsible for the polarization in red. Image adapted from [134]. (b) Typical ferroelectric hysteresis curve. The dipole orientation is schematically shown for specific points in the hysteresis loop.

Initially in a non-polarized state, the ferroelectric domains are randomly oriented and cancel each other out throughout the material. As the electric field is increased, it first follows a linear relationship, but eventually saturates at a maximum polarization P_s, as all electric dipoles become fully aligned. Upon reducing the electric field, the polarization does not return to zero, but instead retains a remnant polarization P_r when the field is removed. When the field is reversed, the polarization decreases with the dipoles gradually changing their orientation until it reaches zero at a critical coercive field E_c. A decrease of the electric field beyond that point leads to an inverse polarization until the other saturation point at $-P_s$, and the negative remnant polarization $-P_r$ after removing the external electrical field. The area enclosed within the hysteresis loop represents the energy loss per cycle, attributable to mechanisms such as domain wall motion and dipole switching, which are crucial for the functionality of ferroelectric devices.

Perovskite-based ferroelectrics, such as $Pb(Zr,Ti)O_3$ (PZT) or $SrBi_2Ta_2O_9$ (SBT), are commonly used in state-of-the-art ferroelectric random access memories (FeRAMs) and ferroelectric FETs (FeFETs), but suffer from poor CMOS compatibility and limited scalability [133, 135]. The discovery of ferroelectricity in fluorite-structured, Si-doped HfO_2, in 2011 by Böscke et al. [44] was considered a breakthrough for the semiconductor industry, as they are physically compatible with Si and various metals [135]. Furthermore, HfO_2-based ferroelectric layers can be scaled down even below 5 nm, enabling the fabrication of high-density FeRAMs and FeFETs [45, 83, 133, 136]. In addition, its mature ALD capability with high control of film thickness is an additional advantage over perovskite-based ferroelectrics. Table 2.3 compares the key properties of fluorite-structured $Hf_{1-x}Zr_xO_2$ (HZO) with common perovskite-based ferroelectrics.

	$Hf_{1-x}Zr_xO_2$ [132, 137]	PZT [137–139]	SBT [137, 138, 140]
P_r ($\mu C/cm^2$)	1-45	20-40	<10
E_c (MV/cm)	1-2	~0.05	0.01-0.1
E_{BD} (MV/cm)	4-8	0.5-2	~2
E_c/E_{BD} (%)	12.5-50	2.5-10	0.5-5
Dielectric constant ε_r	~30	~400	150-250
Endurance (cycles)	$>10^{11}$	$>10^{15}$	$>10^{12}$
Film thickness (nm)	5-30	>70	>25
Annealing temperature (K)	723-1273	>873	>1023
ALD capability	mature	limited	limited
CMOS compatibility	stable	Pb, O_2 diffusion	Bi, O_2 diffusion

Table 2.3: Comparison of HZO with the most common perovskite ferroelectrics PZT and SBT, including remnant polarization P_r, coercive field E_c, breakdown field E_{BD} as well as scalability and process compatibility.

The extraordinarily high coercive field E_c of the fluorite-structured $Hf_{1-x}Zr_xO_2$ is a rather unique property, which is more than an order of magnitude higher than in other perovskite materials. This is a major advantage for the scalability of FeFETs, enabling shorter gate lengths. Furthermore, it provides greater resistance to internal depolarization effects, improving the retention of memory devices. The generally lower trap density and the lower permittivity of HfO_2-based ferroelectrics compared to PZT and SBT also help to alleviate retention losses [141]. However, as the high coercive field E_c required for its polarization switching is relatively close to the breakdown field E_{BD}, this could limit the reliability and endurance of the $Hf_{1-x}Zr_xO_2$ layers [137]. The high achieved remnant polarization P_r in the range of $1\,\mu C/cm^2$ to $45\,\mu C/cm^2$, e.g., depending on Zr content and fabrication methods, is in the range of PZT, promising for its integration into non-volatile devices with large memory windows.

The most common and stable crystal phase of HfO_2 is the monoclinic fluorite-type crystal structure (m-phase, crystallographic space group: $P2_1/c$), which is centrosymmetric and therefore non-ferroelectric. However, a phase transition to a non-centrosymmetric phase, the orthorhombic crystal structure of the crystallographic space group $Pca2_1$ (o-phase), is feasible. Sang et al. [142] confirmed via convergent electron beam diffraction that the orthorhombic phase is the origin of the ferroelectric properties. To stabilize this ferroelectric phase, the HfO_2 can be doped with different materials such as Si, Zr, Y or Al [44, 135, 143, 144], modifying the material's crystal structure. Furthermore, its crystallographic orientation and therefore its ferroelectric response heavily depend on the deposition methodology [135, 145], thermal treatments [146, 147] and film thickness [148, 149]. Moreover, strain engineering, through the application of mechanical stress via different top metal electrodes or substrate-induced strain, can also enhance the stability of the ferroelectric phase by favoring specific lattice distortions that promote dipole alignment [132, 150].

Especially the incorporation of Zr is highly interesting to stabilize the polar phase at room temperature [144]. Zr, similar to Si or Al dopants, tends to suppress the m-phase and favors the formation of the tetragonal (t-phase, space group: $P4_2/nmc$) or cubic phase (c-phase, $Fm\bar{3}m$), with the ferroelectric o-phase always present between its transitions [133]. In addition, as the ionic size of Zr^{4+} with 86 pm is almost identical to that of Hf^{4+} with 85 pm, as is their chemical valence, stable solid $Hf_{1-x}Zr_xO_2$ compositions can be formed over the entire range of x [133]. Mueller et al. [144] have shown that the properties of $Hf_{1-x}Zr_xO_2$ thin films heavily depend on the Zr concentration. This is illustrated in Figure 2.4, which shows the P/E and C/V characteristics for different $Hf_{1-x}Zr_xO_2$ compositions. Without the incorporation of Zr, the pure HfO_2 crystal remains in the centrosymmetric m-phase, showing an almost hysteresis-free paraelectric behavior. When increasing the Zr concentration, a transition to a dominant o-phase is observed, increasing its ferroelectric hysteresis. At a balanced concentration of Hf and Zr, i.e., $Hf_{0.5}Zr_{0.5}O_2$ or HZO for short, the remnant polarization P_r reaches its maximum and is therefore favored for many memory applications. As the Zr content is further increased, the proportion of the t-phase increases, thinning down the hysteresis loop at zero bias, eventually leading to an antiferroelectric-like behavior for pure ZrO_2 layers with no remnant polarization.

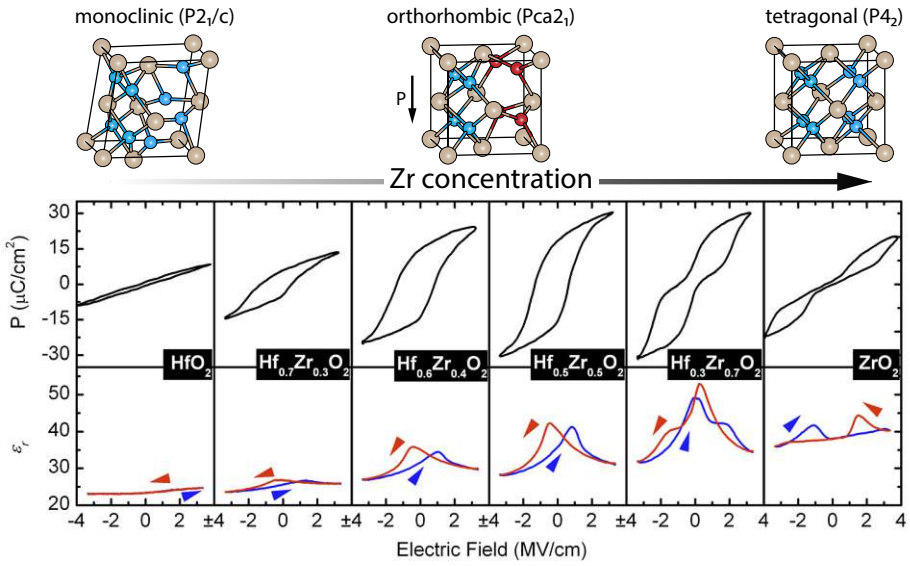

Figure 2.4: Polarization (P) and permittivity (ε_r) hysteresis in relation to the Zr concentration in $Hf_{1-x}Zr_xO_2$ thin films. With the increase of Zr, the main crystal phase changes from a paraelectric monoclinic phase to a ferroelectric orthorhombic phase and finally to an antiferroelectric tetragonal phase for pure ZrO_2. Adapted from [143].

The fabrication of ferroelectric HZO thin films involves several critical steps that influence their ferroelectric properties and overall performance. Most commonly, ALD is used for the deposition of HZO thin films [135]. Other deposition techniques such as pulsed laser deposition (PLD) [151], CVD [152] or sputtering [153] have also been demonstrated, with each method having a strong impact on film properties. ALD processes are particularly favored for their ability to produce uniform and conformal coatings, with a precise control

over film thickness and composition. Furthermore, it features significantly lower process temperatures compared to CVD or PLD processes, which is advantageous for its integration into CMOS fabrication process flows. The deposition parameters as well as the choice of precursors are also known to influence the properties of the ALD-grown HZO layers [145, 154].

Since the deposited films are mainly amorphous or in a random polycrystalline orientation, it is necessary to perform thermal post-deposition treatments to induce crystallization, usually by using rapid thermal annealing (RTA) processes. Therefore, mechanical stress on the layer is essential to stabilize the orthorhombic phase and at the same time suppress the formation of undesired phases. This mechanical stress is applied to the HZO layer via top and/or bottom electrodes. The choice of electrode material has a major influence on the properties of the ferroelectric layer, as it affects the orientation and grain size [132, 155]. Furthermore, the electric properties are also strongly affected by the electrodes due to different metal work functions or the quality of the interface [132, 150]. In this regard, TiN or TaN are the most commonly studied electrode materials, also due to their widespread use in CMOS technology. But also many other metal electrodes like Pt, Pd, W or Au have been shown to induce ferroelectric behavior in HZO films at different annealing temperatures [155].

The crystallization process of a thin HZO layer sandwiched between two metal electrodes is schematically illustrated in Figure 2.5, mainly following a two-step process. In the as-deposited amorphous layers, the crystallization starts from cubic or tetragonal nuclei, following Ostwald's rule [146]. With increasing temperature, these t-phase nuclei will act as crystallization seeds and start extending their size, eventually fully crystallizing the HZO layer. For HZO layers with TiN electrodes, annealing temperatures around 773 K are commonly used [155]. Park et al. [148] suggested that at this temperature, a phase

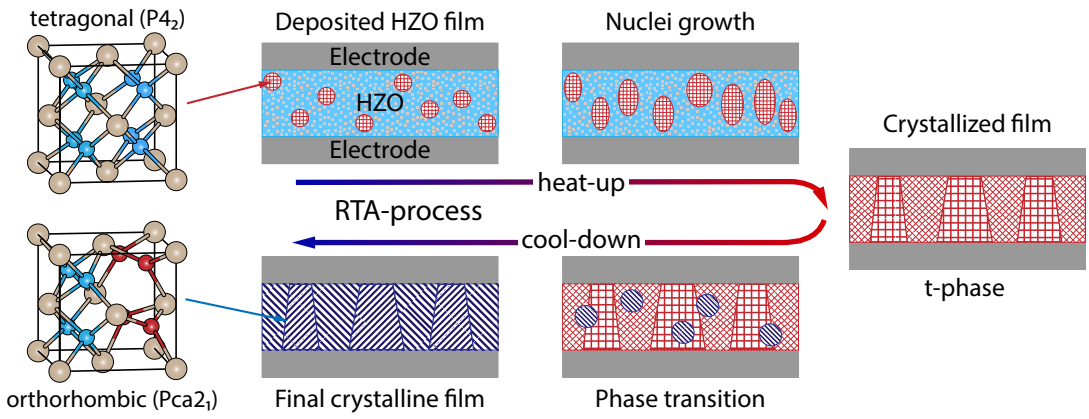

Figure 2.5: Schematic visualization of the crystallization and phase transition process via RTA. The as-deposited amorphous HZO layer with t-phase nanocrystallites fully crystallizes during the heat-up process and transitions to the ferroelectric o-phase during the cooling process. Image adapted from [148].

transition from the t-phase to the m-phase is, to some extent, kinetically hindered by its high activation barrier. Furthermore, it was shown that RTA of HZO with TiN electrodes at too high temperatures of >873 K significantly facilitates the formation of the m-phase, while that of the o- and t-phases decreases, leading to a reduced remnant polarization. During the following cool-down process, all the t-phase can be transformed into the o-phase crystal due to the very low kinetic transition barrier [148]. A high oxygen content within the layer including a large number of oxygen interstitials, can hinder this phase transition, as it increases the activation barriers and promotes the formation of the m-phase. In contrast, oxygen vacancies promote the formation of the ferroelectric phase [146,153]. It should be noted that any formed m-phase crystal cannot be transformed into another lattice structure, as this phase is highly stable [148].

After this crystallization process, the annealed film is polycrystalline with random orientation of the individual grains, frequently also including other crystallographic phases. This still remains a big challenge for a large-scale integration, as this can lead to a problematic device-to-device variation [47]. A strong preferential crystal orientation in ALD-grown HZO thin films has so far been limited to sub-3 nm layers [156].

For HZO layers exceeding a thickness of 20 nm, a significant degradation of the ferroelectricity is observed. This can be attributed to an increased formation of the monoclinic phase [148,149]. To counteract this degradation, 1 nm thin interlayers can be incorporated between thin HZO layers, enabling thicker ferroelectric stacks while reducing leakage currents [157].

When the ferroelectric layer is cycled between its two polarization states many times, a degeneration of its polarization response may occur. These degeneration effects are called ferroelectric fatigue. Thereby, an increase of the coercive field E_c and a decrease of the remnant polarization P_r are commonly observed [132]. In HZO, while high retention of the set polarization state over 10 years is consistently reached, fatigue is a well-known reliability issue, with the cycling endurance often limited to less than $>10^5$ cycles [135]. In HZO, Zhao et al. [158] verified that trapping of charges causes this fatigue, with the number of traps increasing during endurance cycling. These defects may also include oxygen vacancies that migrate towards the interfaces or domain walls, restricting the domain wall motion and therefore reducing the polarization response. Recent publications have demonstrated that by scaling the HZO layer thickness down to 4 nm and the thereby achieved reduction of operation voltages, the endurance of the ferroelectric could be enhanced to $>10^{14}$ cycles [159,160]. Moreover, the degradation of the polarization can mostly be recovered by annealing of the ferroelectric at elevated temperatures, presumably redistributing the defects initially causing the fatigue [132].

2.3 Metal-Semiconductor Heterostructures

All devices investigated in this work are based on metal-semiconductor-metal heterostructures, where two metal electrodes are in direct contact with the semiconductor channel, usually forming Schottky junctions. This is in contrast to conventional MOSFETs, where degenerately doped regions are used as source and drain (S/D) to form ohmic contacts with the semiconductor channel. Especially in recent years, metal-semiconductor heterostructures have regained interest as the transition to nanoscale dimensions makes it increasingly challenging to fabricate degenerately doped ohmic contacts with sharp doping profiles towards the channel and high reproducibility [57]. The metal-semiconductor interface is of key importance, as the resulting Schottky barrier determines the basic device characteristics. Low barrier heights result in ohmic behavior, characterized by linear I/V behavior and by moderate resistance to current flow in both directions. High barriers result in a rectifying behavior, with low resistance in one direction and high resistance in the other.

The focus of this section will be on Al as the metal contact material, and Si and Ge as the channel materials, since they are the key materials used in this work. It is important to note that the findings regarding the exchange reaction between Al and Si are results of this work, and its theoretical background is discussed here along with the Al-Ge exchange for simplicity [LW14].

2.3.1 Solid-State Diffusion for Contact Formation

For the fabrication of electrical devices based on metal-semiconductor heterostructures, reliable and reproducible contact formation is of utmost importance. Besides the properties of the two materials in contact, the quality and geometry of the interface play an important role and have a strong influence on the device characteristics. The majority of metal contacts is deposited via sputtering or evaporation techniques. Prior cleaning of the semiconductor surface, e.g., by chemical or sputter etching, is essential as the presence of interfacial oxides or other contaminants can significantly increase the contact resistance or degrade the electrical properties [161]. To further improve the contact properties after the metal deposition, thermally induced reaction or diffusion processes are commonly used to form metal-semiconductor interfaces, ideally resulting in well-defined and abrupt transitions with a defined Schottky barrier height, a low defect density and a controlled contact resistance.

Metal-Silicide and -Germanide Formation

For the contact formation to Si, metal-silicide solid-state reactions, e.g., forming Co_xSi_y [52], Pt_xSi_y [162], or Ni_xSi_y [163, 164], have been extensively studied in recent years. Especially the Ni_xSi_y system is well established in state-of-the-art CMOS processes [53]. It has also been successfully applied to novel electronic devices such as modern MOSFETs and reconfigurable field-effect transistors (RFETs) [67], where even a large-scale fabrication of fully integrated devices was demonstrated [72]. Starting from the deposited metal layer,

e.g., Ni, mostly the metal atoms diffuse to the Si interface, where it reacts to form a silicide. Over time, more and more of the Si in the semiconductor channel is converted, resulting in an increasing length of the silicide and a propagating silicide-Si interface [165]. During the silicidation process, different phases with varying stoichiometric compositions can be formed depending on the temperature [54, 55]. In addition, the silicide phases have different material properties, e.g., different sheet resistivity, built-in strain and Schottky barriers to the Si interface [166, 167]. As these properties have a strong influence on the device characteristics, good control of the silicide phase is essential. An improvement of the thermal stability of the Ni_xSi_y phase is commonly achieved by inserting additional metals (e.g., Pt, Pd, Ti) or impurity implantation (e.g., N_2, BF_2) to retard the formation of agglomerations [168, 169]. Furthermore, the control of the silicide length is challenging and can suffer from rather large statistical variability due to the complex reaction kinetics and phase transitions [163, 166]. A major advantage of this silicidation process is its use for the self-aligned fabrication of contacts, the so-called salicidation process, which is particularly important in scaled CMOS technology [53]. The metal (Ni) is deposited directly on the transistor structure without any additional lithography step. After thermal annealing, the metal reacts with the Si to form the silicide, and the unreacted metal is removed subsequently by selective chemical etching [90].

Similar to the silicide formation, germanide contact formation to Ge structures can be utilized using different materials, e.g., Ni [55], Cu [170] or Mn [171]. Again, different intermetallic phases can be formed, which can also cause significant process variations, possibly void formation and reliability problems [171, 172]. Furthermore, germanides generally show a lower stability compared to silicides [51, 56, 57]. Particularly in $Si_{1-x}Ge_x$ systems with a ternary phase diagram, the large number of different intermetallic phases leads to poor morphological stability [173]. Noticeable improvements have been achieved by further including, e.g., Pt, Al or Ti additives, however, increasing process complexity even further [58, 169, 174].

Al Contact Formation to Si and Ge Nanostructures

The use of Al as a contact material instead could be a highly promising alternative to these contact formation processes including intermetallic phases. In recent years, the highly reproducible contact formation to bottom-up grown Ge NWs [62, 175], $Si_{1-x}Ge_x$ NWs [63, 176] and top-down fabricated Ge nanosheets [LW17, LW16], [LWM1] has been extensively studied. Through a thermally induced exchange reaction between Ge and Al, self-aligned crystalline Al leads towards an atomically abrupt and single-elementary Al-Ge interface are achieved. The absence of intermetallic phases thereby has positive effects on variability and yield issues, as no complex phase transitions occur during the contact formation process. In addition, a lower resistance of the pure Al leads is achieved in comparison to the common silicide or germanide contacts [62].

A stable silicide or germanide formation as a compound material is prevented by the different chemical properties of Al and Si/Ge. This can also be seen in the binary phase

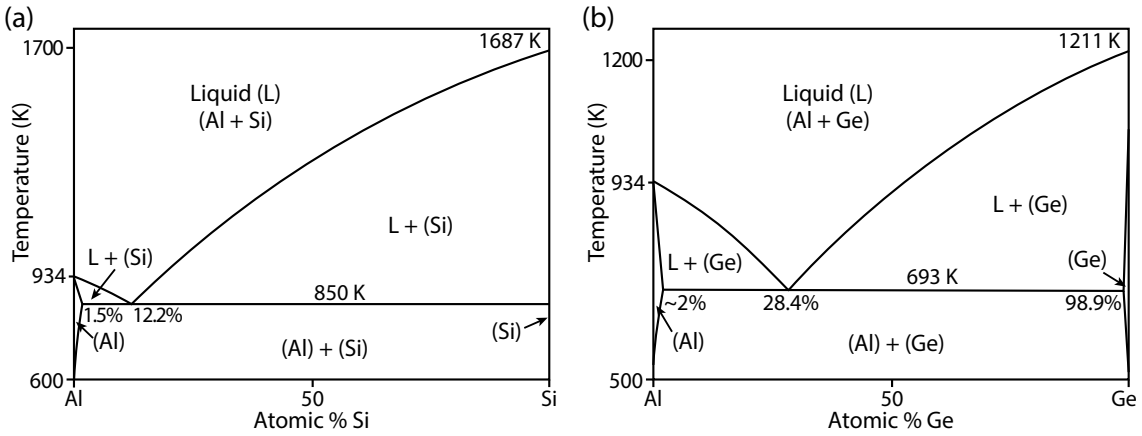

Figure 2.6: (a) Binary Al-Si phase diagram [177] and (b) Al-Ge phase diagram [178], both showing an eutectic system without intermetallic phases. The eutectic point of Al and Si is located at a composition of about 12.2 at% Si, with the solid-liquid transition at 850 K. For Al-Ge, the eutectic point is at 28.4 at% Si and 693 K.

diagrams for the Al-Si and the Al-Ge material system in Figure 2.6. Below the eutectic temperatures of 850 K for Al-Si and 693 K for Al-Ge, structures with local crystallites instead of intermetallic phases are formed. Furthermore, a miscibility gap is observed, leading to the segregation of Al and Si/Ge. The solubility in both systems is very low, with only ∼1.5 at% of Si [177] and ∼1.8 at% of Ge atoms [179] that can be dissolved in Al at the eutectic temperature, strongly decreasing for lower temperatures. Conversely, the solubility of Al in pure Si and Ge is even lower.

The contact formation processes of Si and Ge with Al are based on solid-state diffusion, where the overall movement of atoms is induced to compensate for concentration gradients. This flux of diffusing atoms $\vec{J}$ is described by Fick's first law

$$\vec{J} = -D\nabla C\,, \tag{2.6}$$

with the diffusion vector $\vec{J}$ directed towards the opposite direction of the concentration gradient ∇C. The diffusion coefficient is the tensor D, which is a proportional factor describing the diffusivity of a material. At higher temperatures, the diffusion of atoms is enhanced due to an increase of Brownian atomic movement. This temperature dependency of the diffusion is described by the Arrhenius formula [180]

$$D = D_0 \cdot \exp\left(-\frac{E_a}{k_B T}\right), \tag{2.7}$$

with D_0 as the diffusion constant and E_a as the activation energy. Since the number of diffusing particles must remain constant in an isolated system, Fick's first law can be combined with the continuity equation

$$\frac{\partial C}{\partial t} = -\nabla \cdot \vec{J} \tag{2.8}$$

resulting in a second-order differential equation, which is referred as Fick's second law:

$$\frac{\partial C}{\partial t} = \nabla \cdot (D \nabla C) \,. \tag{2.9}$$

The diffusion of particles in binary systems occurs between the two materials, known as inter-diffusion, but also within the same material, known as self-diffusion. Both elements can thereby have different intrinsic diffusion coefficients, which results in differences in the flux of particles. According to Fick's first law in Equation 2.6, the different flux of particles results in a movement of the interface between the two phases due to a net mass flow of the faster diffusing specimen [180].

Table 2.4 shows the inter- and self-diffusion coefficients D in of Al-Si-Ge system for a temperature of 773 K. Thereby, it is evident that the diffusion of Si and Ge in Al is more than 10 orders of magnitude stronger compared to the contrary diffusion of Al in Si and Ge. In Figure 2.7, this exchange effect is schematically illustrated for a Si/Ge nanosheet channel, contacted by large Al pads. In this Al-Si/Ge system with the highly asymmetric diffusion coefficients, this means that the channel material is rapidly diffusing into the Al contact pads, reducing the Si/Ge channel length due to a propagating metal-semiconductor interface. In contrast to the Kirkendall effect, where empty lattice sites are left behind as one material diffuses faster than the other one, thus leading to void formation, Al is effectively supplied via fast self-diffusion, compensating the out-diffusion of Si/Ge [62]. In addition, diffusion of Al into the semiconductor channel and consequent contamination is very unlikely due to the low diffusion parameters. A certain diffusion between Si and Ge, e.g., in vertical Si-Ge-Si heterostructures as used in this work, also has to be considered. However, since the diffusion coefficients of Si in Ge and vice versa are all very small, intermixing of the two layers is rather unlikely, at least for the used annealing temperatures of $T = 773\,\mathrm{K}$.

	Diffusing element		
(cm^2/s)	Al	Si	Ge
in Al	6.2×10^{-10}	4.4×10^{-8}	3×10^{-9}
in Si	1.9×10^{-22}	6.2×10^{-19}	2×10^{-22}
in Ge	3.2×10^{-20}	7.5×10^{-21}	8.3×10^{-20}

Table 2.4: Absolute values of the diffusion coefficients of the Al-Si-Ge material system at $T = 773\,\mathrm{K}$, calculated from the Arrhenius formula (Equation 2.7). Therefore, the parameter D_0 and E_0 are taken from the literature for the Al-Si [181, 182], Al-Ge [183, 184] and Si-Ge [185] systems excluding anisotropy effects. The given values imply that the elements in the columns diffuse into the elements in the rows.

The Al atoms replacing the out-diffusing Si/Ge are ordered in a single crystal manner. As Al crystallizes in an fcc crystal structure, with a lattice constant of $a = 0.405\,\mathrm{nm}$ [178], a significant lattice mismatch towards the diamond-structured Si (0.543 nm) and Ge channel

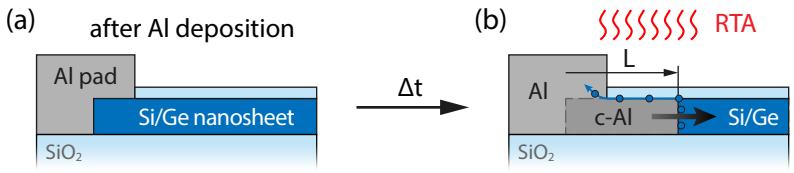

Figure 2.7: Schematic illustration of the thermal exchange process between Al and Si/Ge. (a) Structure after Al is deposited to directly contact the Si/Ge nanosheet. (b) Rapid thermal annealing (RTA) induces the Al-Si/Ge exchange reaction, where Si/Ge atoms are diffusing into the large Al reservoir, mainly along surface channels. Al is supplied via fast self-diffusion, forming crystalline Al-leads (c-Al).

(0.565 nm) is evident. To compensate for this lattice mismatch, the c-Al lattice is rotated towards the crystal structure of the semiconductor channel, enabling strain minimization and lattice relaxation [LW17]. In ⟨111⟩ oriented Ge NW, a mutual in-plane rotation of the two crystal lattices of 18° [64] is observed, while in Ge nanosheets patterned from (100) oriented GeOI a 6.5° rotation was measured [LW17]. The formed Al-semiconductor interface is thereby found to be flat and atomically abrupt, free of contamination (e.g., interface oxides) [64]. Similar to the silicide and germanide contact formation, a preferential {111} facet of the interface is obtained [63, 163][LW17]. It can be thus assumed that the Al atoms are ordered epitaxially to the Si/Ge lattice. Indeed the {111} is a preferential reaction interface in cubic systems.

The growth of the c-Al lead and thus the propagation of the Al-Si/Ge interface over the time t can be described by a parabolic behavior, which can be estimated by

$$L = \sqrt{2Dt}\,, \tag{2.10}$$

hinting towards diffusion limited reaction kinetics. Studies of Al-Ge exchange reactions in NWs and nanosheets have also shown the influence of diameter or sheet width, with increasing reaction rate for narrow structures, indicating a volume diffusion limited process [62, 186][LW17]. In addition, EDX scans have revealed an ∼2 nm thick germanium-rich shell around the c-Al core, formed by Al-Ge exchange in Ge NWs, which indicates that Ge out-diffusion occurs via surface channels [175]. Importantly, the Al reservoir for the exchange with Si or Ge has to be large compared to the volume of the exchanged material. Kral et al. [62] showed that the Al-Ge exchange reaction stops when the bulk solubility limit of Ge in the Al reservoir of around ∼1.8 at% is reached. In the Al-Si system, this bulk limit is estimated at ∼1.5 at% [177].

Due to the absence of intermetallic phases, several consecutive annealing steps can be conducted to precisely tune the desired length of the remaining semiconductor channel. Thereby, the channel lengths of the devices can be reduced towards the few nm region, without the limitation of lithographic processes. Luong et al. [64] demonstrated the fabrication of ultra-scaled Ge channels of 7 nm length embedded in an Al-Ge-Al heterostructure via an in-situ annealing process in a transmission electron microscope (TEM). Furthermore, this led to the demonstration of quantum ballistic transport at room temperature by

Sistani et al. [187]. Since Al becomes superconducting at a transition temperature of 1.2 K [87], Al-Ge-Al heterostructures with superconductor-semiconductor interfaces may also be very interesting for the use in Josephson FETs, which can be integrated into gate-tunable superconducting qubits [188, 189].

2.3.2 Schottky Barrier Junction

The Schottky barrier is a fundamental phenomenon observed at the interface between metals and semiconductors, characterized by a potential energy barrier that affects the charge carrier flow. This barrier forms due to the intrinsic differences in the work functions of the two materials, which leads to the redistribution of charge carriers [190].

In a metal, the work function $q\phi_m$ is defined as the difference between the Fermi level E_F^m and the vacuum level E_{vac} with $q\phi_m = E_{vac} - E_F^m$. This property basically describes the mean energy an electron needs to surpass to be emitted to the vacuum. Al, used in this work as the contact material towards the semiconductor channel, has a metal work function of $q\phi_m = 4.2\,\text{eV}$ [191]. Table 2.5 summarizes the work functions for different metals. An analogous property in semiconductors is the electron affinity χ, given by the energy difference between E_{vac} and the conduction band edge E_C with $q\chi = E_{vac} - E_C$. The work function of the semiconductor is thus given by $q\phi_s = q(\chi + \phi_n)$, with $q\phi_n$ as the energy difference between E_C and the Fermi level E_F^s.

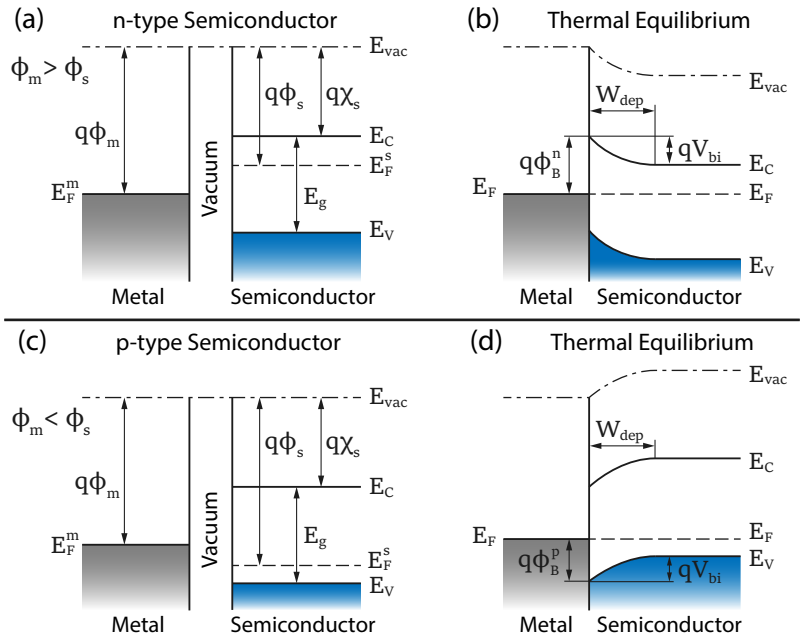

Figure 2.8: Schematic energy band diagrams of a metal-semiconductor junction, forming a Schottky barrier. (a) N-type semiconductor and a metal separated in vacuum ($\phi_m > \phi_s$) and (b) in contact at thermal equilibrium. (c) and (d) show the Schottky barrier formation for a p-type semiconductor with $\phi_m < \phi_s$.

Metal	Work function ϕ_m (eV)	Metal	Work function ϕ_m (eV)
Er	3	W	4.55
Hf	3.9	Cu	4.65
Ta	4.25	**Au**	**5.1**
Al	**4.28**	**Pd**	**5.12**
Ti	**4.33**	Ni	5.15
TiN	**4.3 - 4.65**	Pt	5.65

Table 2.5: Work functions ϕ_m for commonly used metals [191]. For TiN the work function strongly depends on the deposition methods and parameters [192]. The materials used in this work are highlighted.

Figure 2.8 shows the schematic illustration of the energy band diagram of a metal-semiconductor junction in the case of an n-doped (a,b) and p-doped semiconductor (c,d). At contact, the Fermi levels of both materials are aligned, with the other energy bands bending towards the metallurgical interface to reach thermal equilibrium. This causes a charge transfer between the two materials, creating a depletion region of the width W_{dep} within the semiconductor near the interface. This intrinsic band bending V_{bi}, commonly referred to as built-in bias, depends on the difference between the two thermionic work functions

$$V_{bi} = \phi_m - \phi_s. \tag{2.11}$$

An externally applied bias that compensates for this built-in bias, resulting in flat energy bands across the metal-semiconductor junction, is called the flat-band voltage $V_{FB} = V_{bi}$. If the work function of the metal is larger than that of the n-type semiconductor ($\phi_m > \phi_s$), the energy bands of the semiconductor bend upwards (see Figure 2.8(b)). This results in a depletion of the majority charge carriers (electrons) near the interface and thus to a rectifying behavior. In the case of the work function of the metal being lower than the one of the semiconductor ($\phi_m < \phi_s$), an accumulation layer with excess electrons near the interface is formed, without the formation of an energy barrier, resulting in an ohmic behavior. Between the Fermi level E_F and the conduction band edge E_C, the Schottky barrier for electrons is formed, which in an ideal case without surface state is given by

$$q\phi_B^n = q(\phi_m - \chi). \tag{2.12}$$

The equivalent behavior is given for p-doped semiconductors for $\phi_m > \phi_s$, resulting in a depletion of holes (see Figure 2.8(d)). Analogously, the Schottky barrier for electrons in a p-type semiconductor is formed between E_F and the valence band E_V, given by

$$q\phi_B^p = E_g - q(\phi_m - \chi), \tag{2.13}$$

including the energy band gap E_g.

In reality, however, the Schottky barriers estimated by Equations 2.12 and 2.13 can be substantially different. Experiments have shown a less sensitive influence of the metal

work functions on the Schottky barriers [161]. The differences are attributed to localized states at the metal-semiconductor interface that can accumulate charges and eventually generate dipoles [190]. Hence, these metal-induced gap states (MIGS) screen the work function of the metal. This effect is called Fermi level pinning. Figure 2.9(a) shows the Fermi level pinning in an n-doped semiconductor, where the Schottky barrier for electron injection $q\phi_B^e$ is strongly increased.

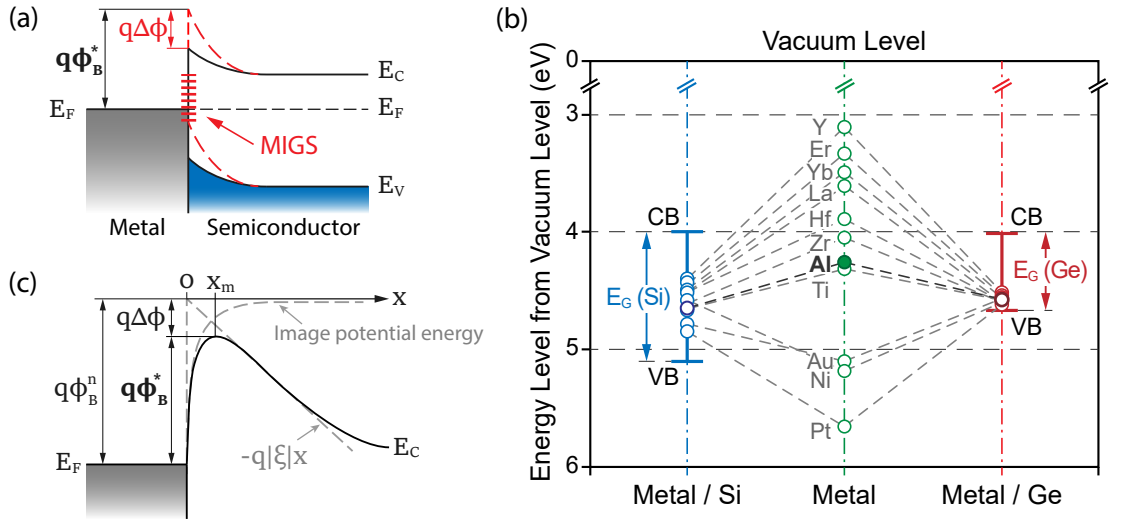

Figure 2.9: (a) Fermi level pinning at the metal-semiconductor interface due to metal-induced gap states (MIGS). (b) Schottky barrier heights for Si and Ge in contact with various different metals. In Si, most metals pin in the mid-gap region, while Ge exhibits strong pinning towards the VB. Figure adapted from [193]. (c) The barrier height $q\phi_B^n$ is reduced by $q\Delta\phi$ due to a combination of the applied field ξ at the interface and the image-force. Image adapted from [90].

The material screening in Figure 2.9(b) shows the pinning levels in Si and Ge for a large variety of metals [193]. In Si, most metals tend to pin toward the center of the band gap, but the Schottky barrier height can still be modified by the choice of contact material and doping level in the semiconductor. When Si is contacted with Al, the Fermi level is pinned very close to the center of the band, which should result in similar barriers for both holes and electrons. This property is highly desirable for the realization of RFETs [12]. For Ge, however, almost all metals, including Al, pin closer to the valence band edge. This leads to low injection barriers for holes and very high electron barriers, which typically results in strong p-type behavior of Ge-based Schottky devices [36, 194]. This strong Fermi level pinning becomes a serious challenge when trying to realize ambipolar or even n-type devices. A common method to target this is to deposit ultra-thin insulating interface layers between the metal and the semiconductor, such as SiN [195] and high-κ dielectrics, creating interface dipoles that counteract the Fermi level pinning [193]. Thin TiN and TaN interface layers can also be effectively used to lower the Schottky barrier to achieve ohmic contacts to n-doped Ge [196, 197]. Recently, also the use of Bi as contact material was reported to create almost pinning-free contacts for both Si and Ge [198].

Another important effect that lowers the potential barrier at the metal-semiconductor interface is the image-force lowering, known as the Schottky effect. As charge carriers approach the interface, its electrostatic attraction reduces the electric field at the interface, which results in a reduced effective barrier height [199]. This lowering is depicted in Figure 2.9(c) for an n-type barrier interacting with electrons. The effect of the image-force lowering can be estimated by

$$\Delta\phi = \sqrt{\frac{q\xi}{4\pi\varepsilon_s}}, \tag{2.14}$$

with the electric field ξ applied to the metal-semiconductor interface and the permittivity of the semiconductor ε_s. This means that an increasing electric field, e.g., at a larger reverse bias, results in a stronger decrease of the Schottky barrier height. Furthermore, the peak of the potential barrier is also shifted away from the interface into the semiconductor to the position x_m.

Transport Mechanisms through a Schottky Contact

When an external voltage V is applied to the metal-semiconductor interface, the energy bands within the semiconductor can be modulated. Depending on the direction of the bias voltage, the Schottky barrier for the injection of the majority charge carriers from the metal into the semiconductor can be either lowered (forward bias) or raised (reverse bias), resulting in a change in the current flow along the heterostructure. Figure 2.10 shows the carrier injection mechanism for a slightly n-doped semiconductor for electrons. At this junction, three different transport processes are considered (with the inverse processes under the reverse bias conditions), including:

1. Thermionic emission (TE)
2. Thermionic field emission (TFE)
3. Field emission (FE)

Note that electron-hole recombination could also occur within the space charge region, but this is not discussed here.

Under moderate bias conditions, i.e., not leading to extreme bending of the energy bands, thermionic emission (TE) is the main process responsible for the current transport in Schottky junctions in moderately doped semiconductors at room temperature [90]. Thereby, charge carriers are injected over the energy barrier from the metal into the semiconductor, enabled by the thermal energy distribution. Based on the thermionic emission theory, under the assumptions that $q\phi_B \gg k_B T$ and that the current flow does not affect

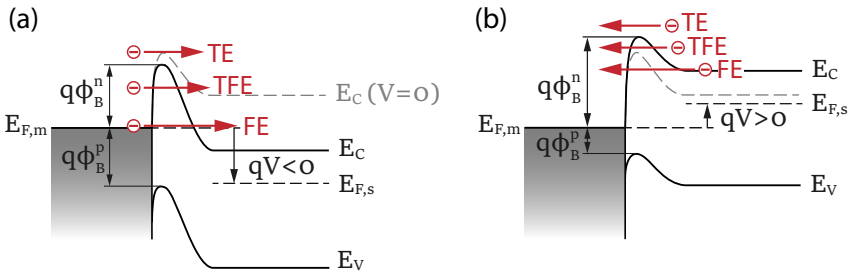

Figure 2.10: Transport mechanisms through a Schottky junction for an n-type semiconductor in (a) reverse bias and (b) forward bias direction. The transport mechanisms include thermionic emission (TE) over the Schottky barrier ($q\phi_B^n$), field emission (FE) with quantum-mechanical tunneling through the barrier, and thermionic field emission (TFE) with tunneling of thermally activated carriers.

the thermal equilibrium at the interface, the current flow can be estimated by

$$\begin{aligned} J &= A^* T^2 \exp\left(-\frac{q\phi_B^*}{k_B T}\right)\left[\exp\left(\frac{qV}{k_B T}\right) - 1\right] \\ &= J_{TE}\left[\exp\left(\frac{qV}{k_B T}\right) - 1\right]. \end{aligned} \tag{2.15}$$

This means that the current injection over the barrier is exponentially increasing with the bias voltage V applied to the metal-semiconductor junction. Note that this formula includes the effective Schottky barrier height $q\phi_B^* = q(\phi_B - \Delta\phi)$, also considering the effects of image-force lowering and Fermi level pinning. The constant A^* is called the effective Richardson constant for thermionic emission and includes material-related parameters. When neglecting the effects of optical phonon scattering and quantum mechanical reflections, it is given by

$$A^* = \frac{4\pi q m^* k^2}{h^3} = A \cdot \frac{m^*}{m_0}. \tag{2.16}$$

In this context, the Richardson constant $A = 120\,\mathrm{A/cm^2K^2}$ for free electrons ($m^* = m_0$) is commonly used, which can then be directly related to the effective mass of the majority charge carriers in the semiconductor channel with $A^*/A = m^*/m_0$ [161].

When lowering the voltage on the junction towards $V = 0\,\mathrm{V}$, reaching thermal equilibrium, the thermal emission current mainly depends on the effective Schottky barrier height $q\phi_B^*$ with [90]

$$J_{TE} = A^* T^2 \exp\left(-\frac{q\phi_B^*}{k_B T}\right). \tag{2.17}$$

Based on this equation, the effective Schottky barrier height in a Schottky barrier FET (SBFET) can be extracted, which is described in Section 3.2.4.

At increased band bending, e.g., higher voltage levels V applied to the Schottky junction, or at lower temperatures, carrier transport by tunneling is the main contributor to current flow. Thereby, charge carriers with energies below the height of the potential barrier at the

interface can pass this barrier by quantum-mechanical tunneling. Strong band bending can thereby decrease the thickness of the barriers, increasing their transmissibility for tunneling. In case of highly doped degenerative contacts to the semiconductor channel, this is also the main transport mechanism. Tunneling of charge carriers with energies near the Fermi level is called field emission (FE) or direct tunneling. Thermalized carriers with higher energies can also tunnel through the thinner part of the potential barrier towards the top, which is referred to as thermionic field emission (TFE) [57]. The relative contribution of these two depends on the temperature and the doping concentration in the semiconductor channel.

The tunneling current from the semiconductor to the metal (J_{s-m}) is proportional to the quantum transmission probability $\mathcal{T}(E)$ for an energy E, multiplied by the Fermi-Dirac distribution functions of the occupied states F_s of the semiconductor and the unoccupied states $(1 - F_m)$ at the metal side of the interface, and is given by [90]

$$J_{s-m} = \frac{A^* T}{k_B} \int_{E_{F,m}}^{q\phi_B^n} F_s \mathcal{T}(E)(1 - F_m) dE. \tag{2.18}$$

The transmission probability $\mathcal{T}(E)$ can be estimated by using the Wentzel–Kramers–Brillouin (WKB) approximation, under the consideration of a triangular potential shape at the interface, given by $V(x) = q\phi_B^n - q\xi x$, with the externally applied electric field ξ. This results in [199]

$$\mathcal{T}(E) = \exp\left(-4\frac{\sqrt{2m^*}}{3\hbar q\xi}(q\phi_B^n - E)^{3/2}\right), \tag{2.19}$$

including the effective mass m^* of the tunneling charge carrier and the reduced Planck's constant $\hbar$. For the tunneling currents in the opposite direction, from the metal into the semiconductor (J_{m-s}), a similar expression as in Equation 2.18 can be derived by interchanging the Fermi-Dirac statistics F_s and F_m. The resulting net tunneling current density is then given by the sum of the two currents. As further analytical expressions for the tunneling currents are rather complex, this equation can also be conveniently expressed by using the ideality factor n with

$$J = J_{s-m} + J_{m-s} = J_0 \left[\exp\left(\frac{qV}{nk_BT}\right) - 1\right], \tag{2.20}$$

including the saturation current density J_0 determined by the thermionic emission current J_{TE}. Values for the ideality factor n can either be extracted by numerical evaluation of the equations above or by experimental extraction from typical I/V characteristics of Schottky diodes. For high temperatures and low doping concentrations, the ideality factor n usually is close to 1, which relates to a dominating thermionic emission current. At low temperatures or at large doping concentrations resulting in thinner potential barriers, both n and J_0 are increasing due to an increasing contribution of the tunneling currents.

A characteristic parameter for tunneling is the tunneling energy E_{00}, as it is directly related to the tunneling probability by

$$\mathcal{T}(E) \sim \exp\left(-\frac{q\phi_B}{E_{00}}\right) \quad \text{with} \quad E_{00} = \frac{q\hbar}{2}\sqrt{\frac{N}{m^*\varepsilon_s}}, \tag{2.21}$$

with the doping concentration N. Therefore, this parameter can be used to estimate the contribution of the different transport mechanisms to the current flow. When $k_BT \ll E_{00}$, tunneling-related FE will be the dominating effect, while $k_BT \gg E_{00}$ results in a dominant TE. At $k_BT \approx E_{00}$, TFE is expected, with a combination of both mechanisms contributing to the total current flow [90].

2.4 Schottky Barrier Field-Effect Transistors

In a Schottky barrier field-effect transistor (SBFET), metal source and drain (S/D) electrodes are used to directly contact the semiconductor channel, which can be either highly-doped, moderately doped or even undoped. Compared to conventional MOSFETs, which use degenerately doped S/D regions to form ohmic contacts to a doped channel, the contacts in SBFETs have the advantages of abrupt interface formation and reduced series resistance of the metal electrodes. Especially when considering highly scaled devices, the reproducible fabrication of well-defined and abrupt doping profiles with low parasitic resistances becomes increasingly challenging. However, since a potential barrier is always present at the interface, SBFETs typically suffer from reduced on-state currents [57]. Nonetheless, high-speed operation of Si-based SBFETs has been demonstrated with transit frequencies up to 280 GHz, attributed to the low RC delays [200].

The integrated metal-semiconductor-metal heterostructure forms two back-to-back Schottky junctions that are biased in opposite directions (i.e., forward and reverse). The operation of the SBFET is therefore fundamentally based on the modulation of the Schottky barriers by the application of a gate voltage (V_G). This gate electrode is separated from the metal-semiconductor-metal heterostructure by an insulating dielectric layer and, importantly, also covers both metal-semiconductor junctions to allow electrostatic control of the Schottky barriers. A schematic of an SBFET based on an SOI substrate is shown in Figure 2.11(a). The typical transfer characteristic with separated electron and hole current contributions is shown in Figure 2.11(b). When no external voltage is applied to the device, the system is in thermal equilibrium with no net current flowing, with Schottky barriers formed for electrons ϕ_B^n and holes ϕ_B^p. A positive bias voltage between S/D ($V_{DS} > 0\,\text{V}$) would then allow a net current flow of holes from the drain contact to the source side. As long as $V_{GS} = 0\,\text{V}$ and a long-channel behavior is given, the increase of the drain potential only influences the potential barrier at the drain side, with an exponential increase of the current flow of holes for positive bias due to increasing tunneling probability into the VB at the drain. However, since the injection barriers for both carrier types are still relatively high at $V_{GS} = 0\,\text{V}$, only a low leakage current flow is enabled in this off-state.

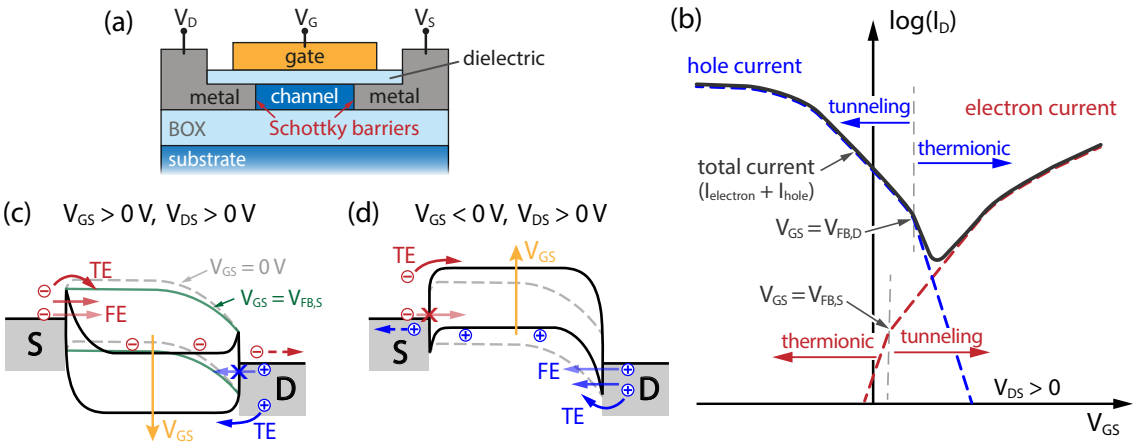

Figure 2.11: (a) Schematic of an SOI-based SBFET composed of a top-gated metal-semiconductor-metal heterostructure. (b) Transfer characteristic of a typical SBFET. The total current flow I_{DS} is the combination of the electron-induced (red) and hole-induced (blue) currents. The kinks in the characteristic mark the transition from the thermionic regime (TE) to the tunneling regime (FE and TFE). Figure based on [201]. Energy band diagrams at a positive bias voltage ($V_{DS} > 0\,\mathrm{V}$) for (c) positive gate voltages for electron-dominated current flow via FE, and (d) for negative gate voltages with hole-dominated currents. The dashed lines show the energy bands at $V_{GS} = 0\,\mathrm{V}$. The green lines in (c) mark the flat-band condition ($V_{GS} = V_{FB,S}$). The source is grounded.

With an increasing gate voltage ($V_{GS} > 0\,\mathrm{V}$), the energy bands in the semiconductor channel can be lowered, which is schematically shown in Figure 2.11(c). The transport is next discussed, separated between injection at the source- and drain-sided junction. At gate voltages below the here-called "flat-band" voltage at the source ($V_{GS} < V_{FB,S}$), the "natural", i.e., material-related, Schottky barrier at the source is not changed by the shifting potential. However, a potential barrier ϕ_s higher than ϕ_B^n adds up to the electrical Schottky barrier, resulting in a behavior similar to that of a conventional MOSFET, whose modulation is determined by thermionic emission. When the gate voltage exceeds the flat-band voltage ($V_{GS} > V_{FB,S}$), the Schottky barrier at the interface then becomes the highest barrier in the channel and determines the injection of electrons. The electron-induced current then further increases with increasing V_{GS} as the thickness of the barrier at the Schottky contact is reduced and tunneling takes place [114]. In the transfer characteristic (dashed red line) in Figure 2.11(b), the transition from TE to the tunneling regime with a reduced slope can be seen by a kink in the characteristic [121]. At the drain-side junction, however, increasing the gate voltage leads to a thicker barrier and a decrease in the tunneling probability to the VB. Eventually this will transition to thermionic emission when the flat-band voltage at the drain $V_{FB,D}$ is exceeded, causing an exponential decrease in hole currents (see dashed blue line in Figure 2.11(b)). The opposite behavior is obtained when the gate voltage is modulated in the opposite direction ($V_{GS} < 0\,\mathrm{V}$), which is shown in Figure 2.11(d). An increased hole-induced current flow from drain to source is enabled, while the flow of electrons is inhibited.

The sum of the electron and hole contributions gives the total current flow of the SBFET. As the current flow exponentially depends on the Schottky barrier height ϕ_B, the ratio between the potential barriers for electrons ϕ_B^n and holes ϕ_B^p will determine the dominant charge carrier type and thus its device characteristic [114]. For symmetric barriers, an ambipolar characteristic with symmetrical on-state currents can be expected. The off-state of an SBFET with symmetrical barriers then mainly depends on the effective Schottky barrier height $q\phi_B^*$ and can be estimated with [116]

$$I_{off} \approx 2 \cdot \frac{2e^2}{h} V_{DS} \cdot \exp\left(-\frac{q\phi_B^*}{k_B T}\right) \tag{2.22}$$

Ge-based SBFETs typically exhibit strong unipolar, p-type device behavior due to their strong Fermi level pinning close to the VB for most metals, resulting in large injection barriers for electrons [202].

Figure 2.12(a,b) shows the influence of a changing drain potential while keeping the source and gate voltages fixed. Since the potential distribution on the source side (with V_{GS}) remains constant, the injection mechanism for the electrons and thus the corresponding current branch is not changed. However, as the energy bands on the drain side are shifted downwards, increasing the bias voltage V_{DS} and consequently also the potential difference V_{GD}, the Schottky barrier for the hole injection is thinned, yielding increased p-type currents [114]. This results in a fanning of the subthreshold characteristic in the p-branch for varying V_D. The analog effect is observed for the n-branch when the source potential V_S is modulated at fixed V_D and V_G.

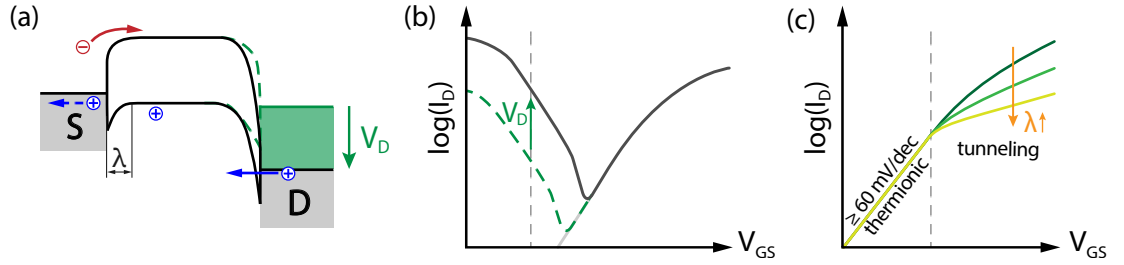

Figure 2.12: (a) Schematic band diagram and (b) transfer characteristic of an SBFET for two different drain voltages V_D. With V_{GS} kept constant, only the injection of holes at the drain is modulated. Figure adapted from [114]. (c) Influence of the screening length λ on the current slope in the tunneling regime (here for the n-branch current).

As already shown in Figure 2.11, the subthreshold slope of the SBFET characteristic clearly depends on the operation regime. In the thermionic region, e.g., $V_{GS} < V_{FB,S}$ for electron emission over the barrier, the current flow purely depends on the linear displacement of the maximum channel barrier. Similar to a conventional MOSFET, a minimum subthreshold slope (S_{th}) according to [57]

$$S_{th} = \left(\frac{d(log_{10}(I_D))}{dV_G}\right)^{-1} \simeq \left(1 + \frac{C_{dm}}{C_{ox}}\right) \ln 10 \cdot \frac{k_B T}{q} \tag{2.23}$$

can be reached, depending on the body effect coefficient ($1+C_{dm}/C_{ox}$) with the capacitance at the depletion width maximum C_{dm} and the oxide gate capacitance C_{ox}. Note that the D_{it} is not considered here for simplicity. To improve the steepness, it is desirable to minimize C_{dm}/C_{ox} by reducing the thickness of the active region of the channel and maximizing the gate capacitance, e.g., by using thin high-κ dielectrics (see Section 2.2.1). As for classical dielectrics, this body factor always remains above 1, the ideal slope is limited to ∼60 mV/dec at $T = 300\,\mathrm{K}$.

In the tunneling regime ($V_{FB,S} < V_{GS}$ for electrons), the current is limited by the fixed Schottky barrier height at the junction, where the thickness and transparency of the potential barrier are modulated by V_{GS}. Consequently, this results in a degraded subthreshold slope [121]. The natural screening length λ is an important parameter that relates the geometric properties of the semiconductor channel to the potential distribution within the channel. In this context, it specifically denotes the thickness of the Schottky barrier [116]. In ultra-thin body devices with a channel thickness below ∼20 nm, such as devices based on SOI platforms, the semiconductor channel can be considered to be fully depleted, depending on the doping concentration. For planar single-gated devices, the screening length can be calculated with [57, 203]

$$\lambda_{SOI} = \sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{ox}}\, t_{Si}\, t_{ox}}, \tag{2.24}$$

with the thickness t and dielectric constants ε for the Si channel and the gate oxide layer. In multi-gate structures, such as FinFETs or GAA architectures, the gating efficiency can be significantly improved, e.g., lowering λ up to a factor of $2^{-1/2}$ for double-gated structures [57]. A shorter λ therefore relates to a shorter tunneling distance and thus results in increased currents at a steeper slope within the tunneling dominated regime, with $\lambda \to 0$ as the ideal case approaching the thermal limit. Figure 2.12(c) shows the influence of the screening length λ on the n-type currents, given an already ideal S_{th}.

2.5 Reconfigurable Field-Effect Transistors

The reconfigurable field-effect transistor (RFET) is an emerging device concept based on an SBFET that combines the functionality of n- and p-type FETs in a single device. This is achieved by adding additional gates to the SBFET structure to electrostatically control the energy band landscape within the typically intrinsic or low-doped semiconductor channel and the Schottky junctions. As shown in the previous section, SBFETs with a single gate covering the entire metal-semiconductor-metal heterostructure exhibit ambipolar device behavior with, in the case of mid-gap pinning S/D contacts, symmetrical n- and p-type currents. Using an additional gate, the so-called polarity (or program) gate (PG), the undesired charge carrier type can be filtered out by introducing an injection barrier at the Schottky junction, allowing unipolar n- and p-type conduction with well-suppressed off-state currents. The current flow through the device is then modulated via the other gate electrode, the control gate (CG).

The first RFET devices were mainly demonstrated utilizing low-dimensional NW channel materials such as Si [68, 77, 204], Ge [33, 37], or carbon nanotubes [66, 205, 206], or 2D channels based on graphene [73], $MoTe_2$ [75] or WSe_2 [76, 82]. Over the past few years, RFETs with top-down fabricated channels, usually based on SOI, have shown greater promise for a large-scale production [25, 69, 71, 207, 208]. More recently, Sessi et al. [72] demonstrated the first full-scale wafer fabrication of RFETs on a 22 nm FDSOI (fully depleted SOI) platform. All devices rely on the same mechanism of modulating the energy band structure to enable a predominant charge carrier injection over Schottky junctions into the conduction or valence band [57].

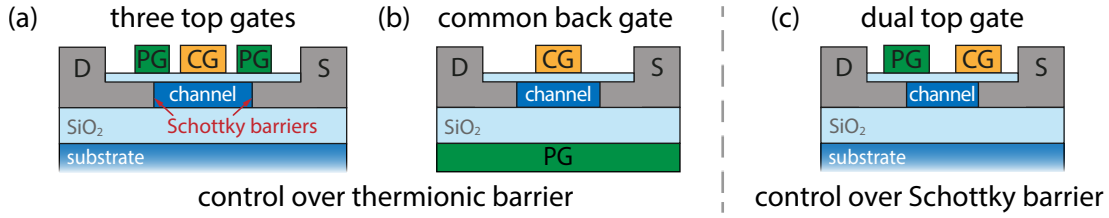

Figure 2.13: Schematic representation of common RFET architectures. (a) and (b) have the CG in the middle of the channel to control the current flow over a thermionic barrier. The Schottky barriers are controlled by the PG via additional top gate electrodes (a) or by a common back gate contact (b). (c) Dual top gate (DTG) architecture, with the CG controlling the source-sided and the PG controlling the drain-sided Schottky junction.

Figure 2.13 schematically shows three commonly used RFET architectures with different arrangements of the gate electrodes. These can be categorized according to the different transport mechanisms via the CG. For the devices in 2.13(a,b), the PG covers both Schottky junctions, thereby controlling both potential barriers for the carrier injection. The CG exclusively modulates only the thermionic channel barrier for the injected charge carriers in order to control the current flow. This concept is commonly referred to as electrostatic channel doping. The modulation of a thermionic channel barrier has the advantage that subthreshold slopes down to the thermal limit of 60 mV/dec can be achieved. The three top-gated (TTG) design in Figure 2.13(a) is the main device architecture in this work and allows independent control of the injection barrier and channel conduction. However, the placement of three top gates on the metal-semiconductor heterostructure leads to increased fabrication complexity and limited scalability of the channel. By using a common back gate contact for the PG (see Figure 2.13(b)) the lateral size of the RFET can be reduced as only one top gate electrode has to be placed atop the channel [72]. A drawback of this design is that the simultaneous application of the electric field from the CG and PG can compete with each other for control of the designated channel region. This, together with the potentially thicker back gate oxide, typically results in increased operating voltages compared to the TTG design [13].

In the dual top gate (DTG) RFET concept in 2.13(c) both the CG and the PG are placed directly atop each Schottky junction, allowing individual control of the injection barriers without an additional gating electrode in the middle of the channel. One gate can block the undesired charge carrier type at the injection barrier, setting the device polarity. The

other gate can tune the transparency of the other Schottky barrier to modulate the flow of the majority charge carriers [57]. As this modulation of the current flow relies on FE/TFE through a potential barrier, the subthreshold slopes and threshold voltages for the DTG architecture are significantly reduced compared to TTG devices. Hybrid implementations, e.g., TTG architectures with independently controlled PGs, allow both current modulation types and provide the functionality to switch between high-V_{th} and low-V_{th} operation [207].

2.5.1 Working Principle

The modulation of the band structure for a TTG RFET is shown schematically in Figure 2.14. The bias voltage V_{DS} is thereby set to be positive and constant for all the different scenarios. When a positive potential is applied to the PGs for the n-type operation, the energy bands of the semiconductor channel are lowered, allowing electrons to be injected into the CB and through the drain barrier via TE/TFE. Simultaneously, the potential barrier width and height for holes is increased, inhibiting its injection into the VB. With the CG also set to a positive potential (Figure 2.14(a)) the injected electrons can pass through the semiconductor channel, resulting in current flow. When a negative potential is applied to the CG (Figure 2.14(b)), the injected electrons are blocked at the channel barrier and current flow is suppressed, giving the off-state of the n-type operation. An equivalent behavior is obtained for the operation as a p-type transistor with inverted potentials at the gate electrodes. A negative potential at the PG shifts the energy bands towards higher energies, thinning the barriers for hole injection while blocking electrons. By modulating the CG voltage, the thermionic channel barrier is modulated, either blocking (Figure 2.14(c)) or enabling (d) the flow of the injected holes.

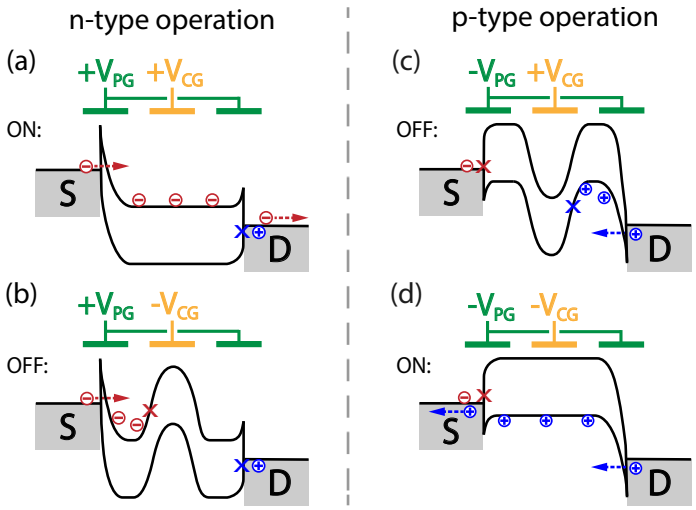

Figure 2.14: Schematic energy band diagrams for a three top-gated RFET at positive bias V_{DS}. The carrier injection for electrons and holes is indicated. The n-mode is set via positive V_{PG}, with the electron-induced current being modulated with the CG over a thermionic barrier between on-state (a) and off-state (b). P-mode for hole-dominated currents at negative V_{PG} in the off-state (c) and on-state operation (d).

The characteristic transfer curve of a TTG RFET is shown schematically in Figure 2.15. Depending on the constant PG voltage, the device thereby mimics the characteristic of an n-type FET ($V_{PG} > 0$) or a p-type FET ($V_{PG} < 0$). Low off-currents are typically achieved as the unintended carriers are well suppressed at the Schottky barriers and the intended carriers are suppressed by the channel barrier. In contrast to the TTG characteristic, DTG devices show a distinct kink when the "flat-band" condition at the injecting barrier is reached at $V_{CG} = V_{FB}$, indicating the transition from TE to TFE. This is due to the different current modulation mechanism, as the CG of the DTG device also controls the injection of charge carriers at the junctions, whereas the injection for the TTG device is fixed with the PG potential, as explained before in Section 3.1.2. Hence, this leads to shallower subthreshold slopes and increased threshold voltages. The on-state currents, however, are almost the same, as this is limited by the injection of the Schottky barriers for both RFET types.

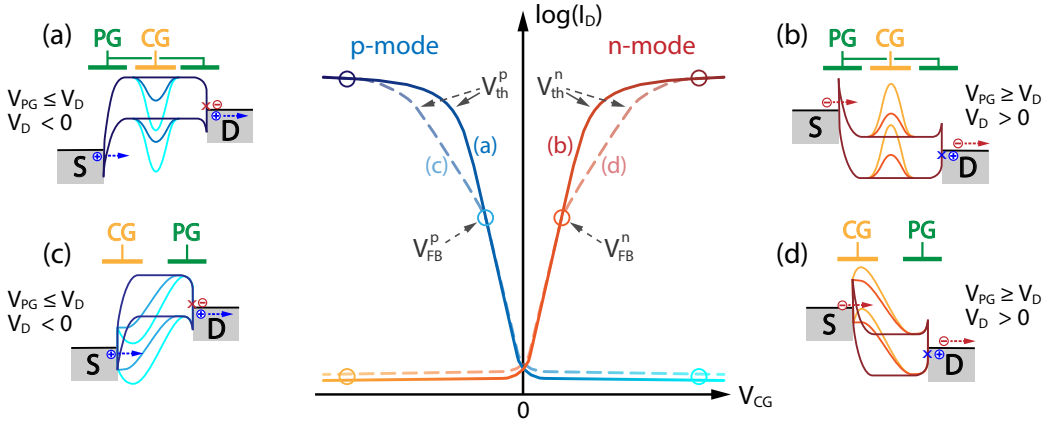

Figure 2.15: Schematic transfer characteristic of a three top-gated (solid lines) and a dual top-gated RFET (dashed lines), with the corresponding band diagrams for both operation modes. A distinct kink only in the DTG device characteristic is evident when reaching the flat-band condition. Figure adapted from [76].

A crucial aspect for the integration of RFETs into circuit applications is the symmetry of the two operation modes. Although many publications have already demonstrated the successful implementation of polarity switching devices, achieving symmetrical characteristics in terms of on-currents, threshold voltages and threshold slopes remains a challenge [71]. Therefore, the injection conditions for both carrier types play an important role. The formation of S/D contacts directly aligned with their Fermi level to the mid-gap energy of the channels is desirable, resulting in equal injection barriers for electrons and holes. In addition, differences in the tunneling effective masses of the two carriers also affect the tunneling probability (see Equation 2.19) and the channel mobility through the device channel, which can also induce asymmetric behavior [12]. In this respect, Heinzig et al. [77] utilized strain engineering of the Si NW-based channel to tune the tunneling transmission of charge carriers and achieve a higher degree of symmetry, with on-current ratios I^p_{on}/I^n_{on} up to 0.98. Simon et al. [71] used a similar approach in top-down fabricated RFETs with omega gating geometry to achieve on-state symmetries of 1.6. These

two publications are also the ones with the highest symmetries reported for Si channel RFETs, with both using intruded $NiSi_2$ contacts towards the channel as S/D contacts. The realization of Ge channel RFETs has also been reported for bottom-up NW [33, 37] and top-down nanosheet channels [38]. However, the strong Fermi level pinning towards the Ge VB has resulted in strongly asymmetric operating modes, with p-type currents at least 10 times higher than those for n-mode. Effective depinning or mid-gap repinning strategies are therefore inevitable for the integration of Ge in RFETs.

2.5.2 Scaling Prospects

Due to the additional gates required to reconfigure the device characteristics, the scalability of RFETs is limited. In this context, the critical tunneling barrier thickness d_T, at which two states can still be clearly distinguished, must be considered. In MOSFETs, where only a single potential barrier is introduced to tune the current flow, the ultimate scaling limit of the channel is $L_{ch} = d_T$. For RFETs with two independent top gates (DTG), the channel is limited to $L_{ch} > 2d_T$, while for TTG devices it further increases to $L_{ch} > 3d_T$. Moreover, potential build-up within the individually gated regions should be considered. Therefore, other aspects, such as drain-induced barrier lowering (DIBL)-like effects or band-to-band tunneling when applying high electric fields between two neighboring channel regions, may further reduce the scalability of the devices [12].

In this regard, Baldauf et al. [209] used TCAD simulations to analyze the scaling of DTG RFETs based on GAA Si NW channels, showing that the performance can be increased by reducing the cross-section of the devices. Considering the natural length λ, sufficiently high off-state currents and stable V_{th} can be achieved for channel lengths $L_{ch} > 8\lambda$. In addition, a small overlap of the gate contact to the channel is critical for proper device operation, while the overlap to the metal S/D region should be minimized to avoid large parasitic capacitances.

Cadareanu et al. [210] analyzed the scaling of TTG RFETs based on GAA NWs at the 10 nm node, also using TCAD simulations. When considering $Si_{0.7}Ge_{0.3}$ channels, drive currents comparable to 10 nm Si FinFET technology devices are thereby claimed to be achievable. Remarkably, Sessi et al. [72] realized wafer-scale fabrication of back-biased RFETs (similar to the device in Figure 2.13(b)) with a 22 nm technology.

2.5.3 RFET Circuit Implementations

In contrast to common CMOS devices, the ohmic and saturation regions are not given by drift but mainly by the injection properties at the junctions and diffusion across the channel [199]. Therefore, reasonably small ungated regions in an SBFET do not limit the transport properties and therefore the device operation, as the Schottky barriers mainly control the charge carrier transport [12, 211]. Since the on-state resistance is primarily determined by the resistance at the injection barriers and not by the channel length (up to a channel length of $\sim$1 µm) [212], it is feasible to extend the channel length of the

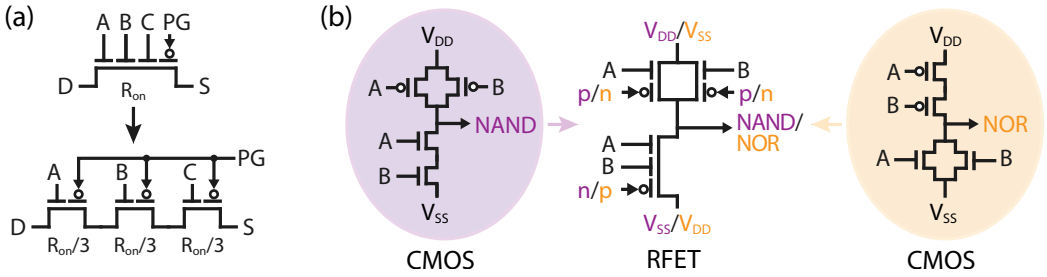

Figure 2.16: (a) MIGFET with three independent CGs for the realization of a wired-AND, combining three RFETs in series within one device. Up to a certain channel length, the effective resistance of each virtual device is only ∼1/3 of the internal resistance of the MIGFET, as no additional junctions are formed. (b) A simple RFET-based logic gate combining NAND and NOR functionality into one circuit while simultaneously reducing transistor count compared to a conventional CMOS implementation. By inverting the potential at the PGs and the supply voltages, the logic function can be switched between NAND and NOR.

device and incorporate additional gates on top of it, realizing a multi-independent gate FET (MIGFET) [17]. These additional channel/control gates can then be used as inputs to provide wired-AND functionality within a single device. In such a device, current flow is enabled only when all CGs are at the same potential as the PG, which defines the type of majority charge carrier. The MIGFET can therefore replace several transistors of the same polarity connected in series, effectively reducing the overall resistance. A schematic of a MIGFET replacing three RFETs is shown in Figure 2.16(a). Note that this is different to a NAND-memory design, as the S/D junctions are explicitly avoided in the MIGFET concept [213].

Utilizing the flexible properties of the RFETs and MIGFETs, with the runtime switchable polarity and its unipolar operability, highly efficient and adaptive logic circuits can be realized. In conventional CMOS technology, NAND and NOR logic gates are fundamental building blocks for implementing digital logic operations, where the former dominates design in memory and logic due to size constraints. Given the De Morgan's laws of binary logic, the two gates are related in a way that can be described as symmetrical in their topology, meaning that the roles of the p- and n-type transistors are reversed between the NAND and NOR gates. By replacing the conventional transistors, whose polarity is determined during the fabrication process, e.g., by doping the channel, with RFETs and reversing the cell bias rail voltage (see Figure 2.16(b)), a circuit can be realized that can switch between NAND and NOR at runtime [214, 215]. By also incorporating a MIGFET with two independent CGs to replace the two transistors in series, the RFET-based circuit not only gains functionality but also reduces the number of transistors compared to conventional implementations (see Figure 2.16(b)). In general, RFETs are ideal to merge symmetrical circuits with equivalent pull-up and pull-down networks [15]. Even more interesting is their use in XOR gates, as RFETs provide intrinsic XOR functionality. De Marchi et al. [21] demonstrated the realization of a complementary XOR gate based on only four physically identical RFETs. By inverting the polarity of this circuit, XNOR functionality as its symmetrical counterpart can be achieved within the same circuit. In

conventional CMOS technology, this function is very complex and inefficient to implement, as a two-input gate already requires 8 transistors for either XOR or XNOR functionality. The benefits of using RFETs in these logic gates increase significantly as the number of inputs is scaled, as the reduction in transistor count also reduces structural delays and energy consumption of the circuits [17].

In large-scale combinational circuit applications, various works have demonstrated that equal functionality at reduced chip area can be achieved despite the larger size of the individual devices [18, 20, 216–218]. It is worth to note that this depends on the actual function and technology design rules chosen for the physical synthesis. Gaillardon et al. [217, 219] proposed the integration of this fine-grain reconfigurability into novel ASIC and FPGA architectures, simulating an average reduction in chip area and delays by 43 % and 23 %, respectively, compared to FPGAs based on conventional 22 nm CMOS technology.

In addition to digital circuits, RFETs have gained interest for their use in analog circuit applications, ranging from differential amplifiers with adaptive gains [26] to three-to-one analog signal modulation [27]. RFETs are also considered an effective method to prevent know-how theft of circuit design intellectual property [24, 220]. In this regard, complex generic building blocks can be designed that are capable of hosting a variety of different functions. However, their actual function is mainly determined by the programming signal, e.g., by defining the individual components as NAND or NOR gates, which impedes reverse engineering of the logic block purely from the circuit layout. This layout camouflaging is combined with "delay obfuscation" features using delay-invariant logic gates. In contrast to CMOS implementations, where a significant propagation delay between equally sized NAND and NOR gates is always present, the delays in RFET-based gates can be tuned to be almost identical. Therefore, a readout of the circuit design from the observations of the delay traces is also inhibited [221]. Another interesting hardware security approach is the so-called logic locking. Thereby, RFET-based logic gates can be used to replace equivalent CMOS gates while maintaining their boolean function. A locking key can then enable the function of the whole circuit by setting the correct polarities of the devices [13, 23].

Despite the aforementioned benefits, RFETs may not be powerful enough to completely replace classic CMOS transistors, but they can be a highly valuable add-on technology that can be co-integrated into the CMOS platform to efficiently solve specific tasks.

2.6 Ferroelectric Field-Effect Transistors

Since the discovery of the ferroelectric properties in fluorite-structured Hf-based oxides, allowing the fabrication of nanometer-scaled ferroelectric layers, their integration into memory devices has been of great interest and the subject of numerous recent publications [135,222]. Various device architectures are available for the implementation of ferroelectric memories, such as ferroelectric random-access memories (FeRAMs), ferroelectric field-effect transistors (FeFETs) or ferroelectric tunnel junctions (FTJs).

FeRAM utilizes ferroelectric capacitors to achieve fast read and write operations, typically combined with an access transistor in a one-transistor one-capacitor (1T1C) structure. This technology is characterized by low power consumption, high endurance and fast access times, making it particularly useful in embedded memory applications. Sony [223] just recently demonstrated the large-scale and high-density implementation of 1T1C FeRAM arrays, achieving a high cycling endurance of $>10^{12}$ cycles at a retention of over 10 years. Micron [45] even demonstrated a 32 Gb stacked non-volatile FeRAM with low read/write latency and high endurance, approaching the performance of state-of-the-art dynamic random access memories (DRAMs). The read operation in 1T1C FeRAMs to extract the stored binary value ("0" or "1") is destructive, requiring an additional write-back operation. Their basic architecture and working principle are therefore quite similar to volatile DRAMs (with integrated linear dielectrics) that are used as main memory in modern computers, servers or mobile phones [133, 135].

Similar to the FeRAM, the ferroelectric layer in FTJ devices is integrated between two metal electrodes in a two-terminal device. The change of polarization leads to a significant modulation of the tunneling current and thus its tunneling electroresistance (TER), which can be detected non-destructively [132, 224]. Furthermore, they provide higher speeds and better scalability compared to FeRAMs. However, the degradation of the thin tunneling oxide and the low driving currents still remain issues that need to be targeted. Nevertheless, this device concept shows high potential for applications in memristive- and neuromorphic-computing [31, 224].

The integration of the ferroelectric layer into a traditional FET structure, realizing FeFETs, is also highly interesting for non-volatile applications. Thereby, the ferroelectric layer, e.g., HZO, is integrated into the gate stack atop the semiconductor channel and directly beneath the gate electrode, replacing the conventional linear dielectric layer (e.g., SiO_2, HfO_2) [31]. Utilizing the electrode, the ferroelectric can then be polarized, influencing the charge carrier flow even when the external electric potential on the gate is removed.

By applying a sufficiently high pulse voltage to the gate, with the voltage drop over the ferroelectric exceeding the required coercive field E_c, the polarization of the ferroelectric layer can be switched [132]. The remnant electric field induced by the ferroelectric dipoles can then either assist in inversion or accumulation of the channel, leading to a threshold voltage shift ΔV_{th} of the transfer characteristic. Figure 2.17(a) schematically shows this

polarization-induced shift in a FeFET based on an nMOS transistor. A positive pulse of V_G thereby results in a net positive charge close to the semiconductor channel, shifting the characteristic towards lower positive V_{th}, while a negative pulse results in net negative charges and thus a larger positive V_{th}. This threshold voltage shift ΔV_{th} between the programmed and erased state directly defines the memory window (MW), which is a key parameter for FeFETs. In general, the achievable MW can be estimated by

$$MW = 2\alpha \cdot E_c \cdot t_{Fe}, \tag{2.25}$$

with the thickness of the ferroelectric layer t_{Fe} and a FeFET ideality factor $\alpha < 1$, which depends on several material properties and second-order effects that contribute to the reduction of the ideal MW [225].

A non-destructive read-out operation of the stored information can then be conducted by sensing the drain-source current I_D at a specific gate voltage V_G. The successful implementation of FeFETs in state-of-the-art technology using Hf-based ferroelectric layers has already been demonstrated in various platforms, e.g., planar 22 nm FDSOI [226], 25 nm FinFET [227] or stacked GAA NWs [228]. Large MWs (~1.4 V) and ultra-fast polarization switching speeds <1 ns were thereby achieved [227], making FeFETs highly interesting for high-speed embedded memory applications. However, the cycling endurance is often limited to $<10^5$ cycles, mainly attributed to the degradation of the interface layer (IL) between the semiconductor channel and the ferroelectric layer [138, 227]. The importance of this interface layer will be discussed later. Compared to state-of-the-art eFLASH memories, FeFETs achieve comparable retention and structural density, with the potential for enhanced scalability, at significantly lowered energy consumption and enhanced switching speeds [225].

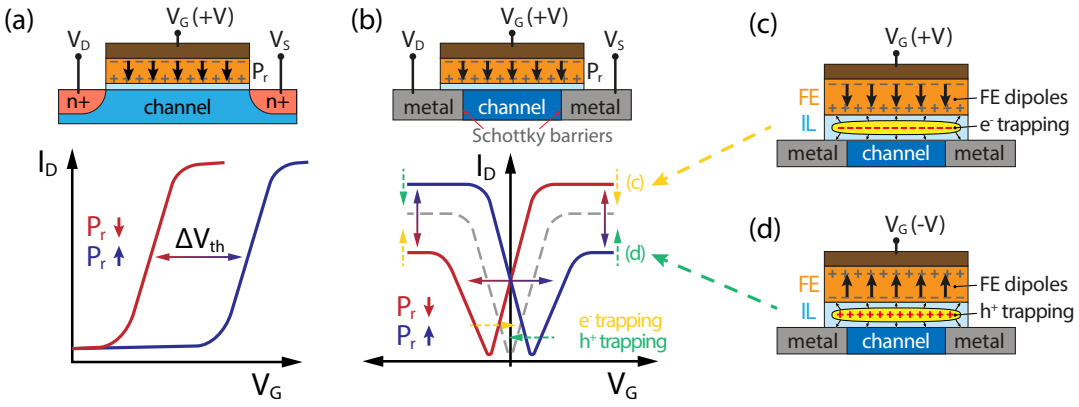

Figure 2.17: (a) Schematic FeFET characteristic for an nMOS device with a doped channel and S/D contacts. The ferroelectric polarization leads to a shift of the threshold voltage V_{th}. (b) Ferroelectric layer integrated into an SBFET architecture (FeSBFET) with an undoped semiconductor channel for an ambipolar transfer characteristic. The polarization of the ferroelectric leads to a modulation of the carrier injection barriers and thus to a change of the n- and p-branch current flow in addition to the V_{th}-shift. Potential electron (c) and hole (d) trapping in the interface layer can attenuate the electric field induced by the ferroelectric dipoles.

2.6.1 Ferroelectric Layer Integration into SBFETs

When integrating the ferroelectric layer into an SBFET architecture, covering the undoped semiconductor channel as well as both metal-semiconductor interfaces, the Schottky barriers are also modulated by the polarization state of the ferroelectric dipoles. Figure 2.17(b) schematically shows a FeFET based on a metal-semiconductor-metal heterostructure, realizing an FeSBFET. In the non-polarized state, with equal Schottky barrier heights for electrons and holes, a symmetrical ambipolar transfer characteristic is obtained, which is indicated by the gray dashed line. When switching to positive polarization with a sufficiently high gate pulse voltage, the electron injection barriers are lowered, increasing the electron-induced current while the hole injection is suppressed. This results in a non-volatile n-dominant device characteristic, indicated by the red curve in Figure 2.17(b). In addition, this effect is superimposed on the V_{th} shift towards lower V_G caused by the remnant electric field over the semiconductor channel. Switching to the reversed polarization by a negative pulse voltage induces the opposite behavior, with a positive V_{th} shift and increased hole-dominated currents, while electrons exhibit higher injection barriers. Besides the V_{th} shifts, this behavior is strongly reminiscent of polarity switching in RFETs by using fixed voltages on the PGs (see Section 2.5). This non-volatile polarity control is demonstrated for the first time in this work [LW1].

2.6.2 Influence of the Interface Layer and Charge Trapping Effects

Typically, a thin interface layer is used between the ferroelectric layer and the channel of the semiconductor device, usually based on SiO_2 or other linear dielectrics (e.g., Al_2O_3, ZrO_2, La_2O_3) [135, 229], leading to metal-ferroelectric-insulator-semiconductor (MFIS) structures. This is done to ensure a stable interface configuration with a low interface trap density, enabling a consistent ferroelectric response for a reliable device operation. Furthermore, it prevents inter-diffusion between the ferroelectric and the substrate underneath [30, 225]. A stable interface also helps to ensure a proper growth of the ferroelectric layer. Although the thickness of the IL is typically in the range of only 0.5 nm to 2 nm, it significantly affects the performance of the FeFETs, as it introduces a series capacitance and a depolarization field.

A major challenge for the integration of HZO and other Hf-based ferroelectric layers is the generation of charge traps. These can occur both in the ferroelectric layer, due to a relatively high defect density, as well as in the dielectric interface layer and its interfaces [229]. The defects in the HZO are mainly fixed trap states related to oxide vacancies with negative fixed charges, resulting in a constant threshold voltage shift of the device characteristic [230], strongly influencing the MW of the FeFET. The interface trap states are typically accessed during the pulsing operation, with high pulse voltages required to switch the polarization state. Figure 2.17(c,d) schematically shows the trapping effects in a top-gated SBFET architecture. Depending on the sign of the pulse voltage, either electrons (for $V_G > 0\,\mathrm{V}$) or holes ($V_G < 0\,\mathrm{V}$) are trapped in the gate stack, leading to a threshold voltage shift according to the density of trapped charges. Importantly, these shifts are in

the opposite direction of the ferroelectric effect, so a positive shift for electron traps and a negative shift for holes, degrading the MW (see Figure 2.17(b)). Furthermore, in the case of an FeSBFET, the electric field induced by the trap states also influences the Schottky barrier shape and thus the charge carrier injection, which can result in a degradation of the on- and off-states of the two polarized states, counteracting the ferroelectric effect. In extreme cases of high trap density, the ferroelectric effect can even be completely screened, resulting in a predominance of trap-induced shifts. The generation of interface/border traps can also lead to a degradation of the subthreshold slopes, which further contributes to the degradation of the MWs [231]. As these traps (partially) release charges over time after setting the polarization pulse, this can influence the read-after-write operation and thus limit the operation speed [229]. Subsequently, these charge trapping and interface trap formation effects can significantly limit the endurance of the device [231].

In general, a higher dielectric constant of the interlayer helps to increase the memory window while simultaneously reducing the electric field applied to the interlayer, thereby reducing its stress and potential breakdown [229]. This is evident when the capacitances of the entire gate stack are considered. The stack is composed of a series connection of the capacitances of the ferroelectric layer (C_{FE}), the interface layer (C_{IL}), and that of the semiconductor channel (C_{SC}), resulting in a total capacitance of

$$\frac{1}{C_{tot}} = \frac{1}{C_{FE}} + \frac{1}{C_{IL}} + \frac{1}{C_{SC}}. \tag{2.26}$$

The voltage drop at the IL subsequently leads to a reduced voltage at the ferroelectric through the voltage divider, described by [232]

$$V_{FE} = V_{tot}\,\frac{C_{tot}}{C_{FE}} = V_{tot}\,\frac{t_{FE}\,\varepsilon_{IL}}{t_{FE}\,\varepsilon_{IL} + t_{IL}\,\varepsilon_{FE}}. \tag{2.27}$$

Note that the capacitance of the semiconductor channel C_{SC} here can be neglected, as during the high polarization pulses the FeFET is either driven in strong inversion or strong accumulation, reducing its capacitive influence to a minimum [132]. In the case of a 1 nm thin SiO_2 IL ($\varepsilon_{SiO_2} = 3.9$) and a 10 nm HZO FE layer ($\varepsilon_{HZO} \approx 25$), this results in a voltage drop of ∼60 % of the total applied voltage in the HZO, while ∼40 % is applied to the thin IL. Due to the large voltage drop on the IL, a higher gate voltage V_{tot} is required to exceed the coercive voltage for polarization switching, but it also results in a high electric field in the IL. This high electric field in the IL enhances the charge injection from the device channel and thus accelerates the IL breakdown [229]. The voltage drop on the IL could be improved by reducing the interlayer thickness, but quickly reaches its limits due to the drastically increased tunnel currents. A better alternative is to increase the relative permittivity ε_{IL} by integrating high-κ dielectrics, thereby also reducing the total operation voltages required for switching the ferroelectric polarization. The use of high-κ dielectrics allows to use thicker IL layers, reducing tunneling leakage currents and electrical stress and thus enhancing the endurance of the ferroelectric devices. Furthermore, the larger dielectric constant of the high-κ results in improved coupling of the ferroelectric polarization to the semiconductor channel, enhancing the MW of the FeFETs.

An interesting effect that reduces the thickness of the dielectric (SiO_2) IL is the oxygen scavenging effect in gate stacks incorporating a Ti top electrode. During high-temperature annealing, the oxygen vacancies in the HZO layer become mobile and allow the migration of oxygen atoms from the SiO_2 layer to the Ti electrode, forming a thin TiO_x layer while reducing the SiO_2 IL thickness. The thereby obtained devices showed increased remnant polarization with more abrupt switching characteristics while reducing the operation voltages [131].

A certain amount of charge injection via tunneling is, however, crucial for the stabilization of the ferroelectric effect [233]. In particular, it has been recently demonstrated that the injection and subsequent trapping of charges in the vicinity of the ferroelectric layer is a fundamental prerequisite for switching the polarization state in FTJs [234] and FeFETs [235]. In addition, a certain level of charge trapping at the interface can even improve the retention by counteracting depolarization fields [233], but can also limit the achievable currents in FeFETs [236].

2.6.3 Optimized FeFET Device Architectures

Another way to improve the ferroelectric response in the devices and thus enable higher MWs is to optimize the structure of the FeFETs, i.e., the architecture of the gate stack. In addition to increasing the ratio of the dielectric constants $\varepsilon_{IL}/\varepsilon_{FE}$, the capacitor area ratio of the layers A_{IL}/A_{FE} can also be changed, resulting in an analogous effect and allows to reduce the interfacial field stress to the IL. This can be achieved by utilizing a metal-ferroelectric-metal-insulator-semiconductor (MFMIS) gate structure by integrating a floating gate (FG) electrode. In this way, the capacitor areas can be scaled individually in order to achieve an improved electric field distribution and the suppression of charge trapping, i.e., by scaling $A_{IL}/A_{FE} > 1$ [132].

Figure 2.18 schematically shows different device architectures to adapt the capacitances of the gate stack. In the planar approach of the MFMIS structure, the higher A_{IL}/A_{FE} ratio can be achieved by simply reducing the size of the top gate electrode. However,

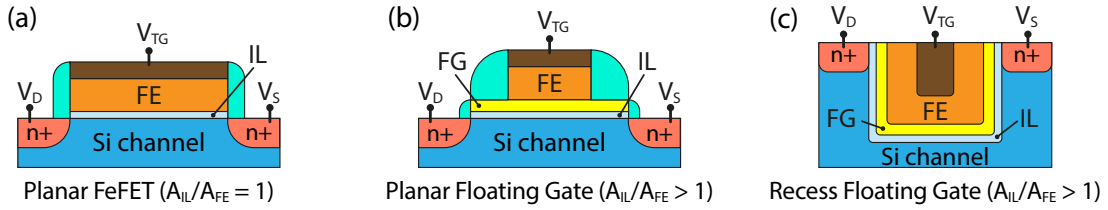

Figure 2.18: Schematic cross-sections of different approaches to adapt the A_{IL}/A_{FE} ratio to reduce the interfacial field stress and improve the FeFET device characteristics. (a) Conventional planar FeFET without adapting the A_{IL}/A_{FE} ratio. (b) Planar FeFET with integrated floating gate (FG) and a scaled top gate (TG) electrode, shrinking the area of the ferroelectric (FE) capacitor ($A_{IL}/A_{FE} > 1$). (c) Recess gate architecture with FG for improved scalability of the FeFET. Figure adapted from [132].

this approach limits the scalability of the device as the area ratio increases and introduces additional complexity to the gate stack. To achieve high area ratios while maintaining a low lateral device footprint, recessed gate architectures can be used (see Figure 2.18(c)). Thereby, the depth of the trench defines the area for the dielectric capacitor, while the buried gate contact defines the area for the ferroelectric capacitor. The achievable area ratio is technologically limited due to increased channel lengths, which lead to reduced on-currents [132]. Lee et al. [237] demonstrated FeFETs with recessed channels (without a floating gate electrode), significantly improving the MW, switching speed, retention and endurance of the devices compared to a planar structure due to a higher electric field across the ferroelectric layer. Also in FeRAMs, the recessed channel is a common method to improve the device performance while maintaining a small lateral footprint [123, 136, 223].

Another positive aspect of integrating a metal FG into the MFMIS gate structures is the improved electric field distribution of the polarized grains towards the transistor channel. Since the grains in the ferroelectric layer can have different polarization states or even different dielectric/ferroelectric crystal phases, the non-uniform field distribution can lead to the formation of unwanted current percolation paths. The introduction of the FG layer can equalize the non-uniform conductance of the FeFET channel, generally improving the MW as well as reducing device-to-device variability [238, 239].

2.6.4 Gradual Switching and Neuromorphic Application

When the channel length of the FeFET is considerably larger than the ferroelectric grain size, the polycrystalline ferroelectric layer will be in a multidomain configuration. This means that not all ferroelectric domains necessarily are oriented in the same direction but may be partially randomly oriented. This is caused by the polycrystalline nature of the ferroelectric film, where the polar axis is randomly oriented in space, resulting in a dispersion of the coercive voltage across the different domains [132]. A FeFET in a multidomain configuration is schematically illustrated in Figure 2.19(a).

Based on the classical nucleation theory, a statistical model for the switching of the ferroelectric domains can be derived, relating the switching time t_s to the applied gate voltage V_G of the FeFET by [225]

$$t_s = t_0 \cdot \exp\left(\frac{\alpha}{k_B T} \cdot \frac{1}{(V_G - V_0)^2}\right), \tag{2.28}$$

with the minimal switching time t_0, a voltage offset V_0 and an exponential constant α depending on intrinsic material properties such as polarization P, domain wall energy and geometry of the nucleating domains. The switching voltage is directly proportional to the coercive voltage V_C of the different domains. This means that the higher the pulsing amplitude V_G, the shorter the switching time.

Due to the dispersion of the coercive voltage within the polycrystalline film, the domains can gradually be switched by varying the pulsing amplitude V_G or the pulse duration t_p,

resulting in different values of the "global" polarization P_r and thus intermediate output states of the FeFET, e.g., different values of the threshold voltage V_{th} [240]. In FeSBFETs, this also results in a gradual modulation of the carrier injection barriers, strongly influencing the on- and off-state currents. When some domains in the layer are switched, this inherently changes the electric field distribution, which also affects the switching of the other domains [241]. Therefore, also a series of pulses of the same amplitude and pulse duration can gradually increase the global polarization of the ferroelectric layer and thus influence the output state [48]. The gradual shift of the transfer characteristic is schematically shown in Figure 2.19(a). Interestingly, in nanoscaled devices, a sharp transition only between two polarization states in an "all-or-nothing" characteristic is obtained after a certain number of polarization pulses due to an accumulation of electrical excitation, with the number of pulses decreasing with the pulse amplitude [242].

This gradual switching can be of particular interest for the realization of artificial neural networks. These bio-inspired neural networks hold great promise for overcoming the memory bottleneck of current "von Neumann" architectures, which suffer from limited scalability and high energy consumption [135]. These networks are based on vector-matrix multiplications, where the synaptic weight, i.e., the conductivity of the artificial synapse, can be adjusted via spiking neurons (voltage pulses), mimicking the topologies of biological brains. The currents are then summed according to Kirchoff's law [135]. According to neuroscientific terminology, increasing or decreasing channel conductance (as a result of the shifting threshold voltage) is commonly referred to as *potentiation* or *depression*, which is analogous to the increase and decrease of the synaptic conductivity [132] (see Figure 2.19(b)). F. Xi, et int., and Q. T. Zhao [48] experimentally demonstrated the realization

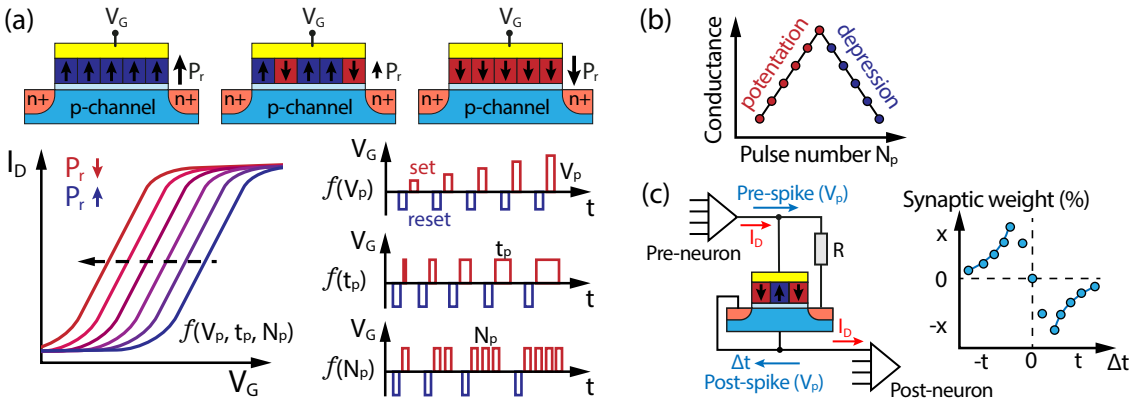

Figure 2.19: (a) Schematic of FeFET with gradually switching ferroelectric domains, resulting in multiple stable output states. These intermediate states can be reached by varying the pulsing amplitude (V_p), the pulse duration (t_p) or the number of consecutive pulses (N_p). (b) Change of conduction of an artificial synapse as a function of N_p, corresponding to the PPF/PPD method. Figure adapted from [83]. (c) FeFET used as an artificial synapse in the STDP method. Depending on the time difference Δt between the pre- and post-neuronal spike (V_p) the synaptic weight is modulated, resulting in different synaptic currents I_D in the read-out operation. Figure adapted from [132].

of artificial synapses utilizing FeSBFETs, with multiple different synaptic functions such as paired-pulse facilitation/depression (PPF/PPD) or spike-timing-dependent plasticity (STDP). In PPF/PPD, a series of repeated voltage pulses is used to modify the conductivity and thus the synaptic current, similar to the last pulsing scheme in Figure 2.19(a). In the STDP method, indicated in Figure 2.19(c), the synaptic current depends on the relative timing difference between a pre-synaptic spike and a post-synaptic spike [48]. Correlated pre- and post-neuronal activity, which leads to a change in the conductivity of the involved synapse, is believed to be a key mechanism in the biological brain that enables learning and memory [132].

Chapter 3

Experimental Techniques

This chapter describes the experimental techniques used to fabricate and characterize the devices from this work. The first part, Section 3.1, discusses the fabrication of the Al-$Si_{1-x}Ge_x$ heterostructure-based SBFETs utilizing a top-down fabrication scheme. The differences between the fabrication steps for the various device types are also addressed in more detail. Section 3.1.1 briefly discusses the growth of the $Si_{1-x}Ge_x$ substrates, which were provided by our project partners at the JKU Linz.

Section 3.2 covers the electrical characterization methods and evaluation techniques for extracting device performance parameters. This includes characterization methods for single SBFETs, logic circuits and non-volatile devices.

Finally, it has to be noted that additional physical analysis of the fabricated devices, including transmission electron microscopy (TEM) and energy dispersive X-ray analysis (EDX) was conducted by project partners at *EMPA* in Thun and the *University of California* at Berkeley.

3.1 Device Fabrication

The device fabrication is based on a top-down fabrication scheme, meaning that the transistor channel is patterned from a semiconductor substrate. The key component for all SBFETs in this work is the metal-semiconductor-metal heterostructure, monolithically formed by the thermally induced exchange reaction between the Al from the contact electrodes and the Si/Ge semiconductor channel. Although the general fabrication of the various devices in this work is fairly similar, individual process steps or the process flow differ depending on the materials or device architecture used, apart from the different mask designs for the lithography. Figure 3.1 provides an overview of the process flow including the key fabrication steps of the different device types.

Finally, it has to be mentioned that the complete device fabrication, except the growth of the SOI and $Si_{1-x}Ge_x$-Si heterostructure substrates, was carried out in the in-house cleanroom facilities of the *Center for Micro- and Nanostructures (ZMNS)* at the *TU Wien*.

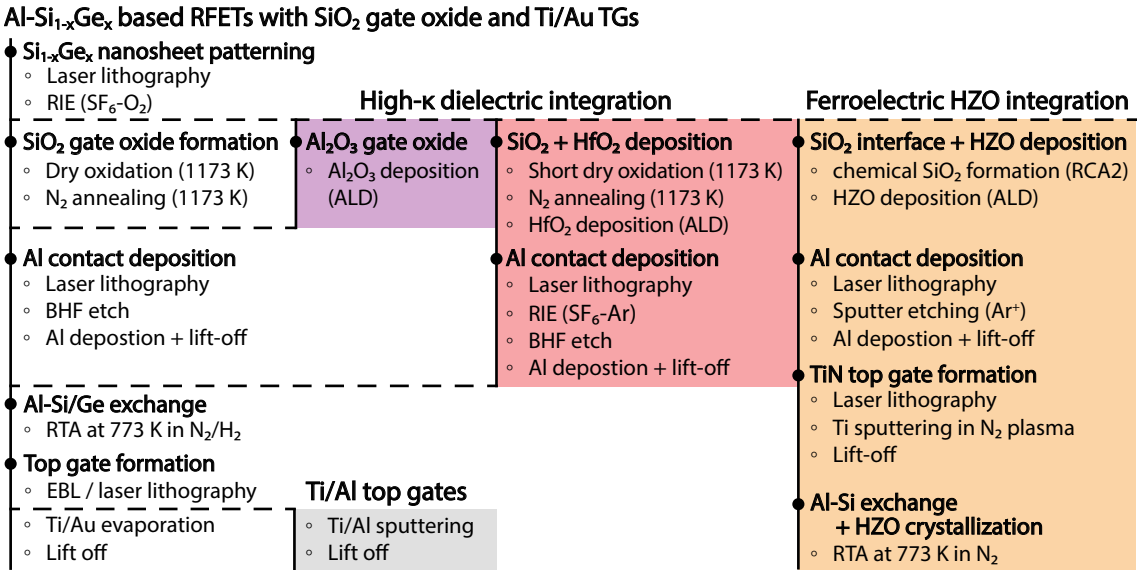

Figure 3.1: Process flow for the fabrication of the different device types. The standard process flow for the fabrication of Al-$Si_{1-x}Ge_x$-based RFETs with SiO_2 gate dielectric and Ti/Au top gates is shown in white. The integration of high-κ dielectrics, ferroelectric HZO or Ti/Al top gates requires a different process flow, indicated by alternative branches highlighted in different colors.

3.1.1 $Si_{1-x}Ge_x$ on Insulator Growth

The composition-dependent study of electrical transport mechanisms in vertical Si-$Si_{1-x}Ge_x$-Si heterostructures for various stoichiometric compositions, as well as the $Si_{0.67}Ge_{0.33}$ channel-based RFETs in Chapter 5 are based on SOI substrates with MBE-grown Ge-rich layers. These substrates were provided by the group of Moritz Brehm at the *Johannes Kepler Universität (JKU) Linz*.

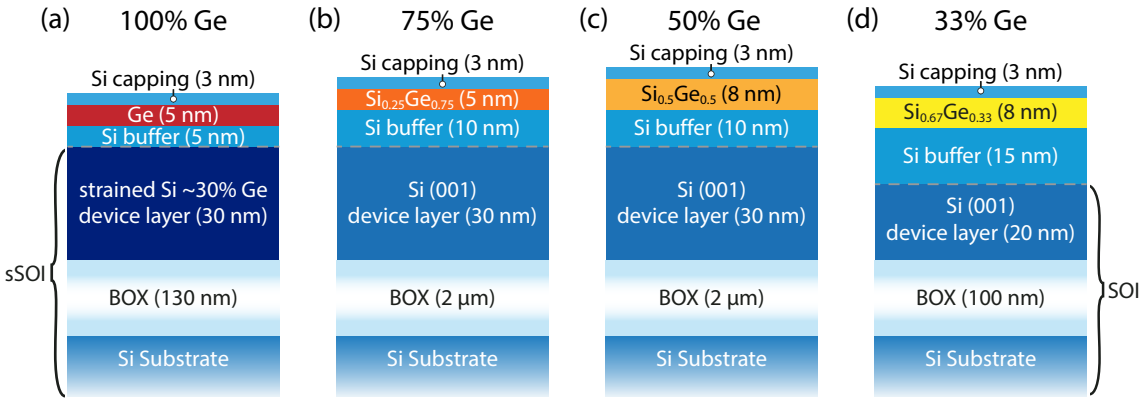

Figure 3.2: Schematic of the MBE-grown vertical Si-$Si_{1-x}Ge_x$-Si heterostructure substrates. (a) The sample with the pure Ge layer is grown on an sSOI substrate. The other samples, with (b) 75 % Ge, (c) 50 % Ge, and (c) 33 % Ge are grown on unstrained SOI. For each sample, a Si buffer layer was grown prior to the deposition of the Ge-rich layer. A 3 nm Si capping layer protects the Ge layer from degradation.

In this regard, recent growth strategies for the growth of Ge-rich but pseudomorphic 2D films with low surface roughness on strained SOI (sSOI) substrates were adapted [243]. The growth was carried out in a Riber SIVA-45 solid source MBE system on an sSOI base substrate for the pure Ge layer sample and on SOI substrates for lower Ge contents (33 %, 50 %, 75 %), both with a [100] Si device layer orientation. The thicknesses of the sSOI device layer and the buried oxide (BOX) are 30 nm and 130 nm, respectively, with the strained device layer having an in-plane lattice constant equal to that of a relaxed $Si_{0.7}Ge_{0.3}$ alloy. The SOI substrate for the $Si_{1-x}Ge_x$ samples with 50 % and 75 % Ge content has a 30 nm thick unstrained Si device layer on top of a 2 µm thick BOX. The $Si_{0.67}Ge_{0.33}$ samples use the same SOI base substrate as the pure Si channel devices in Chapter 4 and 6, with a 20 nm thin, lightly p-doped Si device layer (B, layer resistivity ρ = 9-15 Ω cm) on a 100 nm thick BOX. Figure 3.2 gives an overview of the four different MBE-grown Si-$Si_{1-x}Ge_x$-Si heterostructure substrates, including the thicknesses of the layers.

Prior to the introduction into the MBE chamber, the substrates were cleaned using a standard substrate cleaning process, including Piranha solution and RCA cleaning, followed by a dip in diluted hydrofluoric acid (HF 1 %) to remove the native oxide [244]. The substrates were then degassed at 923 K for 20 min. For the sample with the pure Ge layer, a 5 nm thick Si buffer layer was first grown on the sSOI substrate, followed by the 5 nm pure Ge layer and a 3 nm thick Si capping layer to prevent the Ge from degradation. All the layers for the pure Ge sample were grown at low growth temperature T_G of only 558 K to suppress elastic and plastic strain relaxation inherited from the lattice mismatch to the sSOI substrate [244]. For the substrates with 50 % and 75 % Ge layer content, a 10 nm thick Si buffer was grown on the SOI surface by ramping the growth temperature from 723 K to 823 K. The Ge-rich layers, with 5 nm of $Si_{0.25}Ge_{0.75}$ and 8 nm of $Si_{0.5}Ge_{0.5}$, respectively, were grown at 548 K, followed by the deposition of the 3 nm thin Si capping at

723 K. The $Si_{0.67}Ge_{0.33}$ sample grown on the SOI with the thinner device layer and BOX (20 nm/100 nm) uses a thicker buffer layer of 15 nm (T_G ramped from 723 K to 823 K) before the deposition of the 8 nm Ge-rich layer and the 3 nm Si capping layer, both at 623 K.

A scanning transmission electron microscopy (STEM) image combined with an elementary energy-dispersive X-ray spectroscopy (EDX) of the MBE-grown vertical Si-$Si_{0.67}Ge_{0.33}$-Si stack is shown in Figure 3.3(a). The high-quality growth of the thin films under optimized growth conditions, with ultra-low growth temperatures < 623 K for all Ge-rich layers, is confirmed by the good surface quality of the substrate [106]. The AFM image in Figure 3.3(b), taken immediately after the growth of the layers of the $Si_{0.67}Ge_{0.33}$ sample, shows the dislocation-free surface with an excellent root mean square (rms) roughness of 90.6 pm, which is not significantly higher than that of the SOI base substrate with 72 pm.

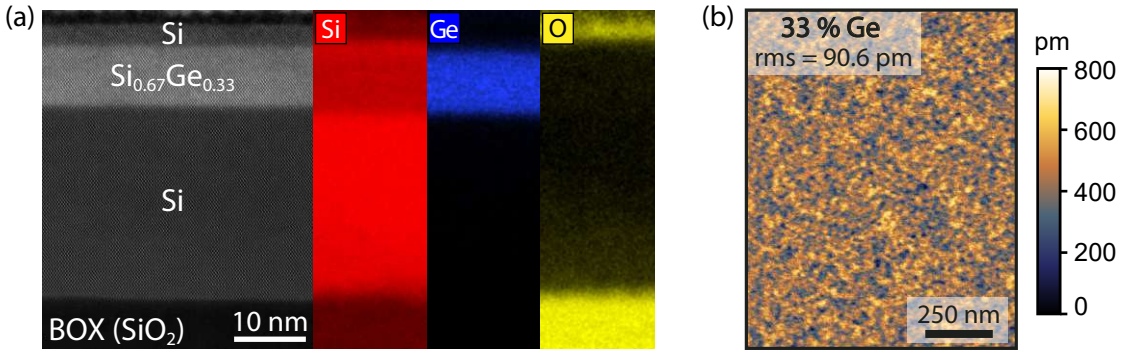

Figure 3.3: HRSTEM and elementary EDX image of the MBE-grown vertical Si-$Si_{0.67}Ge_{0.33}$-Si stack. (b) AFM image of the substrate surface of the $Si_{0.67}Ge_{0.33}$ sample showing the low rms surface roughness of 90.6 pm.

3.1.2 Fabrication of Schottky Barrier Field-Effect Transistors

The top-down fabrication process of SBFETs in this work, including the special variant with three top gates for the realization of RFETs, is largely independent of whether Si or $Si_{1-x}Ge_x$ is used as the transistor channel material, since Si and Ge can be processed very similarly. However, different gate dielectric materials may require a different process sequence (see Figure 3.1), which is discussed in more detail in Section 3.1.2.1. This section focuses on the basic SBFET fabrication scheme using an SiO_2 gate dielectric. A schematic illustration of the main RFET fabrication steps is shown in Figure 3.4.

Starting with the base substrate, either an SOI substrate for pure Si channels or the Si-$Si_{1-x}Ge_x$-Si heterostructure substrates (see Section 3.1.1), small nanosheets for the transistor channels are patterned, with a sheet width (W) of around 300 nm to 800 nm and a length (L) of ~20 µm. In this regard, after a basic substrate cleaning using acetone and isopropanol, the positive photoresist *AZ5214* is applied using spin coating and a softbake at 373 K for 60 s. The mask design is then exposed using the laser lithography system *HIMT MLA150* at a dose of 140 J/cm^2 and developed in *AZ726 MIF*. Despite the

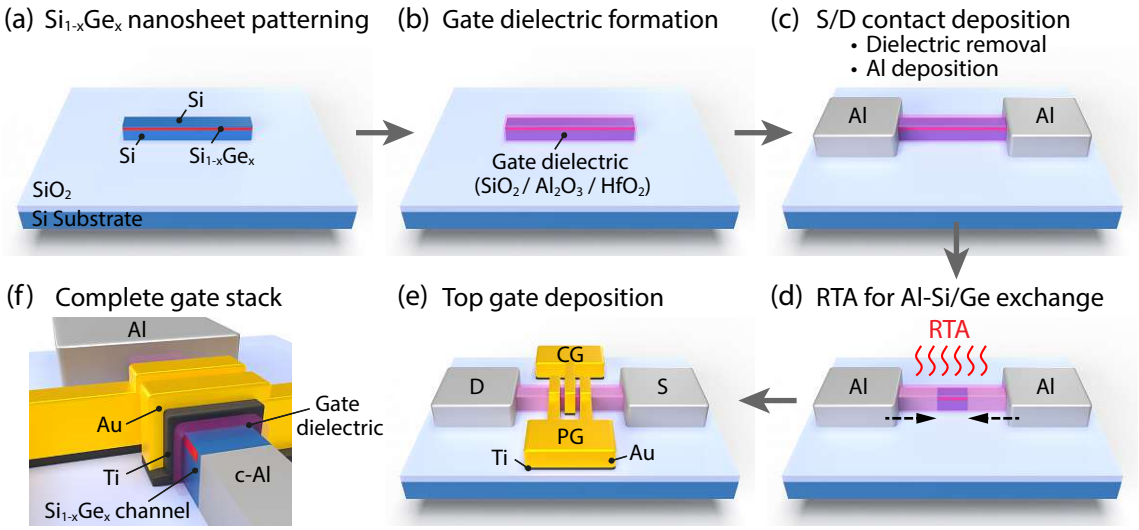

Figure 3.4: Top-down fabrication of a TTG RFET device based on Al-$Si_{1-x}Ge$-Al heterostructures. An SOI substrate with epitaxially grown Si-$Si_{1-x}Ge_x$-Si layers is used as the base material. The final gate stack, with a cut through the CG, is shown in (f).

nominal resolution limit of 0.6 µm of the laser lithography system, thinner sheet widths even below 300 nm could be achieved by a moderate overexposure, resulting in a lateral thinning of the resistive mask. SF_6-O_2-based reactive ion etching (RIE) for 50 s is then used to remove the Si/Ge regions that are not covered by the photoresist (see Figure 3.4). The dry etching is performed in an *Oxford Instruments PlasmaPro 100 Cobra ICP RIE* system with an SF_6/O_2 gas flow of 50 sccm/4 sccm, RF power of 15 W and a process temperature of 308 K. Due to the high selectivity between Si/Ge and SiO_2, the BOX provides a sufficient etch stop, making the process robust and minimizing the susceptibility to overetching and damage to the BOX. Furthermore, the low O_2 content provides a high anisotropy of the dry etching process, resulting in steep etching profiles of the nanosheets [245]. The resist is then stripped by plasma incineration (*Pink V10-G*) at 300 W for 5 min in O_2 plasma, followed by rinsing in acetone and isopropanol.

The SiO_2 gate oxide is formed using thermal dry oxidation at 1173 K at an O_2 flow of 50 sccm in the *ATV PEO-601* furnace. The oxide thickness t_{ox} is thereby controlled over the oxidation time, with a parabolic growth of the SiO_2 layer according to the Deal-Grove model [246]. During oxide formation, Si is consumed, resulting in a reduction of the SOI device layer. This Si consumption can be estimated by $t_{Si} \simeq 0.46 \cdot t_{ox}$, where t_{Si} is the decrease in Si thickness from the initial layer thickness [114]. The SiO_2 layer thickness and the remaining Si device layer thickness for different oxidation times for the furnace in our clean room facilities are extracted in Figure 3.5. The layer thicknesses are determined using ellipsometry. Subsequently to the growth of the thermal SiO_2, an in-situ post-oxidation annealing step in N_2 at the oxidation temperature for the same time duration is followed to reduce the density of interfacial defects [88, 247].

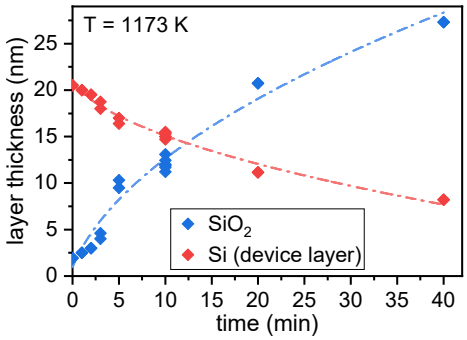

Figure 3.5: Oxidation of an SOI substrate at $T = 1173\,\mathrm{K}$ with measured data points for the SiO_2 and Si thickness versus the oxidation time. The dash-dotted lines show Deal-Grove model fits [246].

The next fabrication step is the patterning of the S/D contact pads (see Figure 3.4(c)). Therefore, laser lithography with the same resist and parameters as before is used to define the contact region. Before the sample is introduced into the sputter chamber (*Creavac Creamet 750 S10*) for the metal deposition, buffered hydrofluoric acid (BHF, 7:1) is used to remove the thermally grown SiO_2 layer from the contact area. To ensure a good contact of the Si/Ge nanosheet channel, Ar^+ sputtering at 100 W for 120 s is used to remove any oxide residuals from the semiconductor surface. 120 nm Al is then deposited in six sputtering cycles of 60 s each at 60 W, followed by the lift-off in acetone and mild ultrasonic treatment.

Subsequently, rapid thermal annealing (RTA) in the *Unitemp UTP-1100* system at 773 K in forming gas atmosphere (N_2:H_2, 10:1) is used to induce the thermal exchange reaction between Al and Si/Ge to form Al-$Si_{1-x}Ge_x$-Al heterostructures with abrupt metal-semiconductor interfaces (see Figure 3.4(d)). Due to the absence of intermetallic phases, several consecutive annealing steps can be conducted to precisely tune the length of the remaining $Si_{1-x}Ge_x$ channel. For the fabrication of TTG RFETs, channel lengths in the range of 1.5 µm to 2 µm are typically targeted to accommodate three independent top gates on this heterostructure. MIGFET devices with four or more top gate electrodes may require longer channels. For single top-gated SBFETs, the channel lengths can also be scaled down to the low nm range using this contact formation technique [187].

Electron beam lithography (EBL) with the *Raith e-LiNE* system is used to pattern the top gate electrodes for the RFETs due to its high structure resolution ($\leq 20\,\mathrm{nm}$) and alignment accuracy. This is required to achieve a small spacing between the individual top gates for improved electrostatic gating, as well as a precise placement of the PG atop the metal-semiconductor junctions to ensure a good control of the charge carrier injection barriers. For the EBL process, the positive polymethyl methacrylate (PMMA) resist (*AR-P 679.04*) is applied on the sample using spin-coating, and is developed after the exposure with a matching developer. Note that for sample designs only including single top-gated structures, with lower requirements for structural resolution and alignment accuracy of

the gate electrodes, laser lithography is used with the process steps described above, as this significantly reduces the complexity of the process.

The Ti/Au top gate electrodes are then deposited via electron-beam evaporation in the *Plassys MEB550SL* system. First, a 10 nm Ti layer is deposited on the gate dielectric, which mainly defines the work function of the gate electrode and also acts as an adhesion layer for the Au layer. The 100 nm thick Au layer deposited afterwards serves as a contact material to the electrical needle probes and as a bonding pad. After metal deposition, the excess metal is removed by lift-off in acetone and ultrasonics. The finished TTG RFET structure is shown in Figure 3.4(e), with a more detailed view of the gate stack in Figure 3.4(f). Figure 3.6 shows a fabricated SOI-based device with distinct RFETs and RFET-based logic gates.

As an alternative to the non-CMOS-compatible Au, sputtered Ti/Al layers have also been used as gate electrode material. The 10 nm thin Ti layer is thereby deposited in two cycles of 60 s at 60 W, followed by the sputtering of 105 nm Al in eight cycles of 60 s at 30 W. As a direct comparison to analyze the influence of the top metal layer on the gate stack, reference structures with a sputtered Ti/Au gate stack were fabricated, using the same parameters for the Ti layer and four cycles of 60 s at 30 W for the sputtering of 177 nm Au.

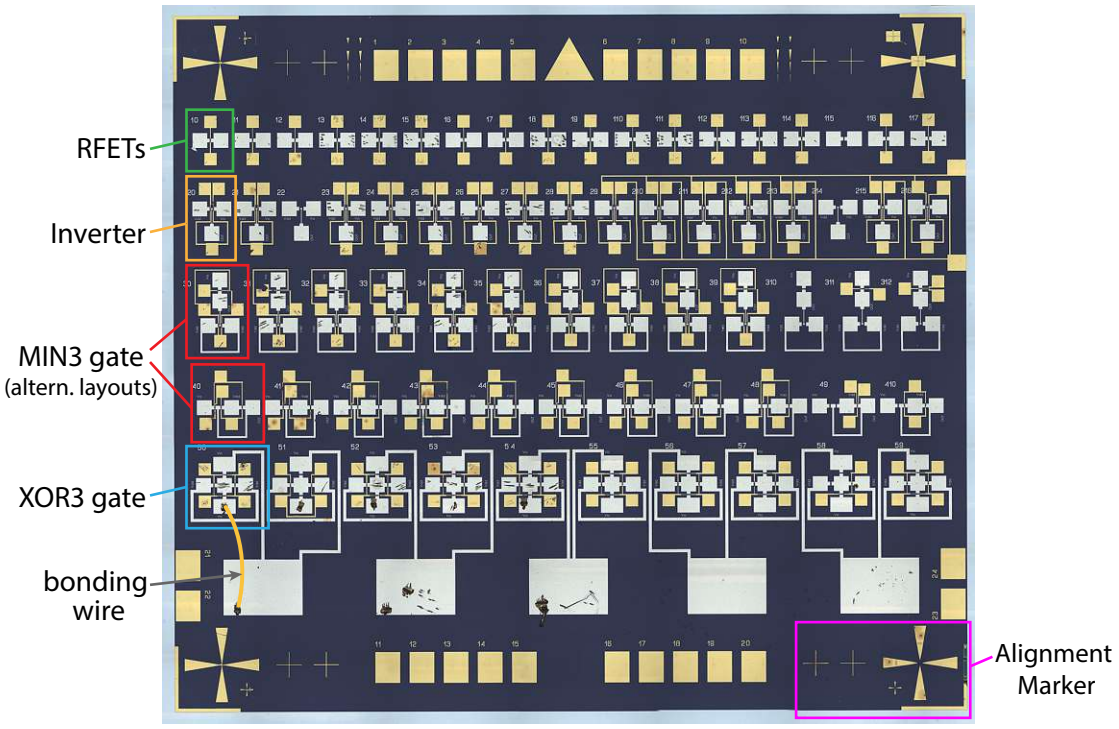

Figure 3.6: Microscope image of a fabricated sample based on an SOI substrate, including RFETs and RFET-based logic gates. For the XOR3 gate, a bonding wire is indicated connecting two pads of the same potential due to the lack of additional metal interconnection layers.

3.1.2.1 High-κ Gate Dielectric Integration via ALD

As an alternative to thermally grown SiO_2, high-κ dielectrics were also integrated into the gate stack of the fabricated devices. In the early stages of the study, when the transition-dependent transport in $Si_{1-x}Ge_x$ heterostructures was being investigated, Al_2O_3 was used and deposited directly on the native SiO_2 of the Si capping layer. In this regard, ALD is employed to coat the patterned nanosheets with 10.6 nm Al_2O_3 at a reactor temperature of 473 K using the trimethylaluminum (TMA) precursor and H_2O as the oxidant source. Since Al_2O_3 can be etched by BHF at a very similar rate as thermal SiO_2 ($\sim$1 nm/s), the fabrication of the devices can be proceeded in the same way as described in the previous section.

For the integration of HfO_2 into the RFET gate stack, more steps from the previously described process flow have to be adapted (see Figure 3.1) as it can be barely etched using BHF. The main purpose of its integration into the $Si_{0.67}Ge_{0.33}$-based RFETs in Section 5.3.1 is to effectively reduce the EOT and thus the electrostatic gating of the devices without increasing the leakage currents by physically reducing the gate oxide thickness. To ensure a good interface quality to the Si surface of the nanosheets, a short thermal oxidation of 1 min at 1173 K is conducted to grow a 2.5 nm thin SiO_2 interface layer. Ideally, the thickness of this SiO_2 interface should be further reduced, but this is difficult to achieve with the furnace available for the oxide growth. Chemical growth of the SiO_2 interface oxide (see Section 3.1.3) is also problematic, as the chemicals used would etch the Ge layer. Subsequently, the sample is loaded into the *Beneq TFS 200* ALD system to grow a 7.6 nm thick HfO_2 layer at 523 K using tetrakis-(ethylmethylamino)-hafnium (TEMAHf) and H_2O precursors, with N_2 as the carrier gas.

To etch through the deposited HfO_2 layer prior to the deposition of the Al for the S/D contacts, an SF_6/Ar-based RIE process was developed. At a process temperature of 293 K, an RF power of 50 W and an SF_6/Ar gas flow of 50 sccm/4 sccm, the HfO_2 is etched at a rate of $\sim$0.06 nm/s. Unfortunately, the underlying SiO_2 and Si/Ge layers do not act as an etch stop, with an even higher etch rate in Si, which means that the process timing must be precisely tuned. For a 7.6 nm thick HfO_2 layer, this results in an etch time of 125 s. The process is tuned to stop etching within the thermally grown SiO_2 layer. The remaining oxide layer is subsequently removed by standard wet chemical etching in BHF for 20 s, which naturally stops at the Si surface of the nanosheet.

3.1.3 Ferroelectric Gate Integration into SBFET

The SBFETs with the integrated ferroelectric gate stack for non-volatile applications are based on Si nanosheets patterned from an SOI substrate. As before, these are fabricated using laser lithography and SF_6-O_2-based RIE. For a reliable device operation with a strong ferroelectric response, a thin interface layer of high quality and a low interface state density is essential. In this regard, the substrate is first dipped in BHF to remove

the native oxide, followed by the growth of an ∼1 nm thin SiO_2 film chemically formed following the RCA-2 procedure (H_2O_2:HCl:H_2O (6:1:1) at $T = 343\,K$ for 10 min).

The 8.5 nm thick HZO layer is then grown utilizing the *Beneq TFS 200* ALD at a chamber temperature of 523 K using the TEMAHf and TEMAZr (tetrakis-(ethylmethylamino)-zirconium) precursors, H_2O as the oxidant source and N_2 as carrier gas. First, two ALD cycles of ZrO_2 are deposited on the SiO_2 surface as a seed layer for the HZO growth. The introduction of a ZrO_2 layer promotes the lateral growth of the HZO and diminishes island growth. Furthermore, the smaller lattice mismatch of the ZrO_2 seed layer towards the HZO compared to the SiO_2 could also decrease tensile strain effects, resulting in reduced grain sizes. These smaller grain sizes can effectively prohibit the transition of the tetragonal phase to the unwanted monoclinic crystal phase and therefore improve the ferroelectric properties [224]. The growth of the HZO is then performed by alternating single cycles for HfO_2 (TEMAHf, H_2O) and ZrO_2 (TEMAZr, H_2O) layers, with 58 of these so-called supercycles for a total HZO layer thickness of 8.5 nm.

The Al S/D contacts are then defined using the standard laser lithography procedure. Since HZO is even more stable against BHF etching, and the SF_6-Ar RIE process has also revealed various processing issues, the HZO layer in the contact region was etched purely physically using Ar^+ sputtering. At a power of 100 W, the sample is etched for 695 s with an extracted etch rate of the HZO of 0.86 nm/min, thereby also moderately etching into the Si device layer to ensure a good contact to the Si nanosheets. Subsequently, 120 nm Al is deposited in-situ at 60 W in six cycles of 60 s, followed by lift-off in acetone and ultrasonics.

For the fabrication of SBFETs with classical dielectrics, the RTA would now be applied to form the monolithic Al-Si-Al heterostructures. However, annealing the structures without top gates would here result in the HZO crystallizing in an undesired dielectric phase. In this regard, the top gate electrodes are structured first using standard laser lithography, as the single and dual top-gated FeFETs in this work do not require the high resolution of the EBL process. The deposition of the 50 nm thick TiN layer is conducted using reactive sputtering of Ti in N_2 plasma at 100 W at a N_2 flow of 6 sccm and a working pressure of 6×10^{-3} mbar, followed by lift-off. RTA at 773 K ($t > 2$ min) is then applied to induce the Al-Si exchange reaction as well as the crystallization of the HZO into the orthorhombic phase to achieve ferroelectric device behavior. Thereby, annealing in N_2 atmosphere is used, as forming gas is known to significantly degrade the ferroelectric properties of the HZO layer [132]. Again, several consecutive annealing steps can be carried out in order to adjust the length of the Si segment so that the Al-Si interfaces are located below the top gate electrodes, without destroying the orthorhombic phase.

3.2 Electrical Characterization and Evaluation

For the electrical characterization of the fabricated devices, different measurement setups and techniques are used. The main device characterization of the individual SBFETs is conducted in the *Lake Shore PS-100* cryo-probe station using a *Keysight B1500A* semiconductor analyzer. This setup features five needle probes connected to four source-measure-units (SMUs) and an additional ground unit (GNDU), ideal for characterizing three- or four-terminal devices such as STG SBFETs or TTG RFETs. The four SMUs are capable of applying voltage to the device while precisely measuring currents with high resolution down to 1 fA. In addition, the SMUs feature a pulsed operation mode, where the voltage level is applied only for a very short time, with a minimum pulse width of $t_p > 0.5$ ms. This allows to reduce charging and charge trapping effects of the devices during the characterization. The measurements are generally conducted in ambient air, shielded from ambient light. The sample stage can be heated up above 400 K for temperature-dependent characterization.

For the characterization of devices (MIGFETs) or circuits requiring more than four terminals, a needle probe station with up to seven electrical probes, in combination with the *HP 4156B* semiconductor analyzer is used (see Figure 3.7). The analyzer is equipped with four SMUs, also with a high resolution in the low fA-region, two voltage-measurement-units (VMUs) and two voltage-source-units (VSUs). The needle probe station is also placed in a dark box to minimize the influence of light irradiation during measurements. For transient measurements, this setup is combined with up to three dual-channel *Keysight EDU33212A* function generators to provide the signal inputs for characterizing the fabricated RFET-based logic gates. However, the operating speed for time-dependent measurements is limited by the low temporal resolution of the analyzer (> 10 ms) and the sample design with large planar contact pads for the needle probes, which induces large parasitic capacitances.

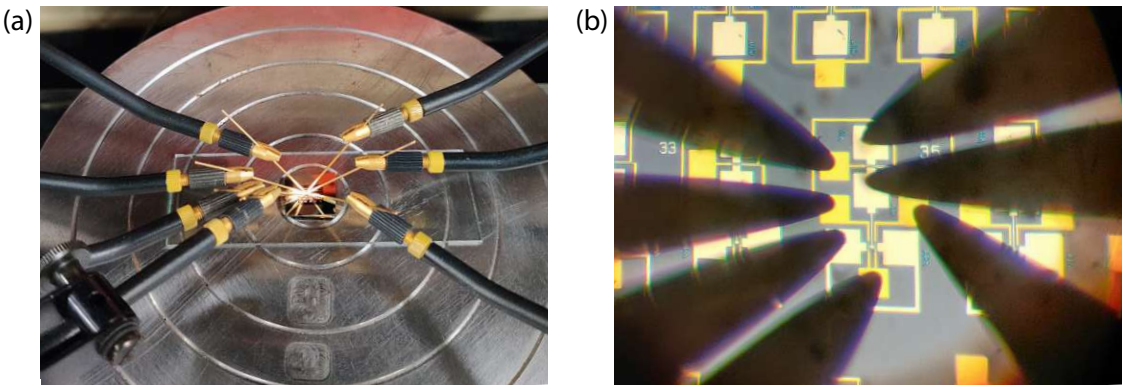

Figure 3.7: (a) Image of the measurement of an RFET-based logic circuit using 7 tungsten-carbide needles. The needle probes are positioned on the Au contact pads using micromanipulators and connect the device to the semiconductor analyzer. (b) Microscope image of the contacted MIN3 gate.

The C/V measurements for the characterization of capacitive test structures, as well as some additional four-terminal I/V measurements, are conducted using the *Keithley 4200-SCS* semiconductor analyzer and the *Cascade Microtech Summit 11000 AP* probe station. The built-in capacitance-voltage-unit (CVU) allows capacitance measurements in the range of fF to nF at frequencies from 1 kHz to 10 MHz. The four SMUs for the I/V measurements achieve comparable current resolution as the other two semiconductor analyzers.

3.2.1 Transfer Characteristics

The transfer characteristic of a transistor describes the relationship between the gate voltage (V_G) and the drain current (I_D) at a constant bias voltage (V_{DS}). This measurement is a standard analysis used to describe the electrical behavior of transistors in general and to extract important performance metrics. By plotting the characteristic in a semi-logarithmic representation, the switch-off behavior of the transistor is revealed, whereby important parameters such as on- and off-currents (I_{on}, I_{off}) and the subthreshold slope (S_{th}) can be extracted. To classify the measurement results, it is common to normalize the currents to the characteristic size of the transistor, which is typically the channel width W (in µA/µm) for top-down fabricated platforms. For NW-based transistor channels, currents are typically normalized to the NW diameter d_{NW}. This provides better comparability between differently scaled devices or device platforms, both within this work and with comparable devices from the literature.

For a multi-gate transistor, such as the RFET, only the CG for modulating the channel barrier is varied to measure the transfer characteristic. The PG is typically fixed to a specific voltage, which sets the polarity of the device to either n-type ($V_{PG} > 0\,\mathrm{V}$) or p-type conduction ($V_{PG} < 0\,\mathrm{V}$). An exemplary transfer characteristic of an RFET is shown in Figure 3.8(a), with the measured current flow I_D for both operation modes. In devices with multiple CGs (MIGFETs), only one CG is swept over the defined measurement range, while the other CGs and the PG are set to a constant potential. The bias voltage is set by the source-drain potential difference $V_{DS} = V_D - V_S$. For measurements where the bias is referred to as asymmetrical, the bias voltage is defined by the potential at the drain contact, with $V_{DS} = V_D$, while the source contact is grounded ($V_S = 0\,\mathrm{V}$). For symmetrical bias measurements, the source potential is set to the inverted drain potential ($V_D = -V_S$), resulting in a symmetrical modulation of the injection barriers at both Schottky junctions.

When determining transistor parameters, measurements are always made in a symmetrical range around the zero point, e.g., V_G swept between $\pm 5\,\mathrm{V}$. Especially for RFETs, only symmetrical operating voltages are used for n- and p-type operation to ensure a fair comparison, i.e., $V_{PG}^p = -V_{PG}^n$ and $V_{DS}^p = V_{DS}^n$.

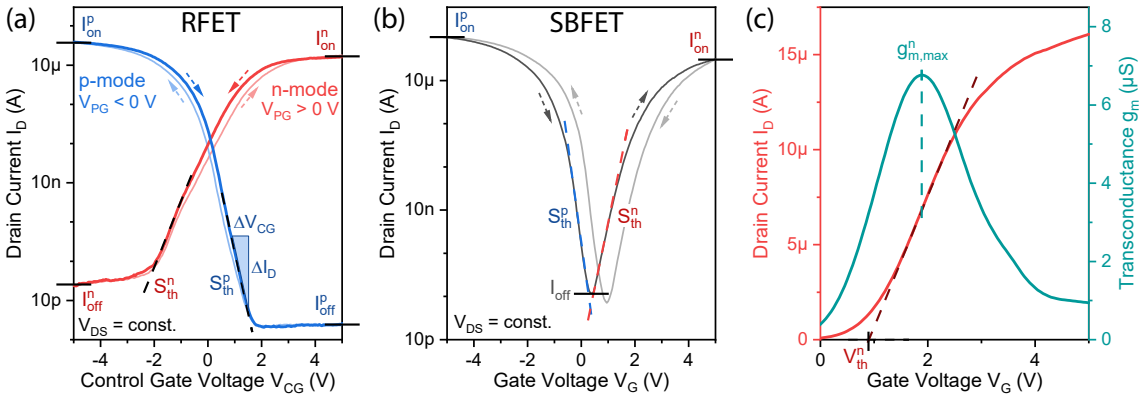

Figure 3.8: (a) Semi-logarithmic transfer characteristic of an RFET, for the extraction of the on-currents $I_{on}^{n,p}$, off-currents $I_{off}^{n,p}$ and subthreshold slopes $S_{th}^{n,p}$ for n-mode (red) and p-mode (blue) operation, respectively. (b) Semi-logarithmic transfer characteristic of an ambipolar SBFET. (c) Linear transfer characteristic and transconductance g_m for the extraction of the threshold voltage V_{th} of the n-mode.

On- and Off-State Currents

The on-state currents I_{on} are extracted as the maximum current values I_D above the threshold voltage at the on-state of the transistor, typically either at the maximum applied positive V_G for electron-induced currents (I_{on}^n) or negative V_G for hole-induced currents (I_{on}^p). The off-state current I_{off} is extracted from the minimum I_D value of the measured characteristic. In an ambipolar SBFET with both n- and p-type branches within a single device characteristic, on-state currents can be extracted for both carrier types, which is shown in Figure 3.8(b). In an RFET, the injection of one charge carrier type is blocked by the potential barrier introduced from the PG, resulting in a unipolar device characteristic with a distinct on-state and off-state current for the respective operation mode (Figure 3.8(a)). Note that the detection of the off-currents is limited to current levels of ∼10 fA due to the resolution limitations of the setup. The on/off current ratio (I_{on}/I_{off}) is an important device metric representing the transistor's capability of current modulation and is mostly independent of the device dimensions, making this parameter well suited for comparing devices of different technologies. For RFETs in particular, the on-state symmetry is an essential performance parameter, which is calculated from the ratio of the on-state currents for both operation modes I_{on}^p/I_{on}^n. For equivalent driving capabilities of the RFET in both configurations for logic circuits, this symmetry factor should ideally be close to 1.

Subthreshold Slope

The switch-off behavior of the transistor in the subthreshold region is characterized by the subthreshold slope S_{th}, which is defined by

$$S_{th} = \left(\frac{d(log_{10}(I_D))}{dV_G} \right)^{-1}. \tag{3.1}$$

The S_{th} is expressed in mV/dec and describes the gate voltage required to change the current by one order of magnitude (see Figure 3.8(a,b)). For logic operations, low S_{th} values are desirable as this corresponds to a steeper transition between the on- and off-states of the transistor. For thermionic emission in conventional transistor architectures, the slope is generally limited to $\geq 60\,\mathrm{mV/dec}$ at room temperature, which is further discussed in Section 2.4. By optimizing the electrostatic gate coupling, e.g., reducing the EOT or improving the gating architecture, the S_{th} can be optimized to approach this thermionic limit.

Threshold Voltage

The threshold voltage V_{th} of a transistor is identified as the voltage at which a FET turns on. In conventional MOSFETs, it is defined as the gate voltage where an inversion channel is formed at the silicon surface, enabling the flow of charge carriers [90]. However, the current transport in SBFETs with lowly doped or undoped semiconductor channels is different and is mainly defined by the modulation of the Schottky barriers. Therefore, a more general definition of the threshold voltage is applicable. For electron/hole conduction, V_{th}^n/V_{th}^p can be defined as the voltage level where the CB/VB band edge coincides with the source Fermi level, which is largely independent of the actual Schottky barrier height. In this regard, in an ambipolar SBFET, the difference between the threshold voltages for the n- and p-branches equals the band gap of the channel material, with $E_g = q(V_{th}^n - V_{th}^p)$ [248].

To extract the threshold voltage V_{th}, several different methods can be used, such as the constant-current method, transconductance method, or the linear extrapolation method, all resulting in slightly different values for V_{th} [249, 250]. In the constant-current method, the threshold voltage is defined as the gate voltage at which a predefined threshold drain current I_T is reached. The transconductance (g_m) method uses a linear extrapolation of the g_m/V_G characteristic at the maximum of its first derivative [249]. In this work, the linear extrapolation method is used for the extraction, which is also the most commonly used method. This extraction method is shown in Figure 3.8(c), using the transfer characteristic plotted in a linear scale. A tangent is drawn through the inflection point of the I_D curve. The value for the V_{th} is then extracted at the intersection of the tangent with the x-axis, at $I_D = 0\,\mathrm{A}$. The inflection point is found at the maximum point of the transconductance g_m, which is the first derivative of the I_D-V_G characteristic, calculated by

$$g_m = \frac{\partial I_D}{\partial V_D}. \tag{3.2}$$

The threshold voltage is commonly used as the basis for evaluating the on- and off-currents. Thereby, the current values are measured with a predefined offset towards the V_{th} [251]. However, in this work, it is not always feasible to extract the V_{th} for all the different devices with different channel materials, as the peak transconductance cannot be reached within the possible V_G-measurement range.

Hysteresis

To analyze the influence of the gate voltage sweeping direction, the transfer characteristic can be recorded using double sweeps. Thereby, the gate voltage is swept in opposite directions within the measurement range. In unipolar devices, such as the RFET set in either n- or p-type operation, measurements are typically conducted from off → on → off-state. In ambipolar SBFETs, the measurement is usually started from the negative V_G value. Figure 3.8(a,b) shows the double sweep measurements for both device types, with small arrows indicating the measurement direction. Different charge trapping effects can then result in differences in the obtained transfer characteristic depending on the sweeping direction. Strong charge trapping due to high interface trap densities, as often found in Ge devices with unstable GeO_x interfaces [38, 252], can cause large hysteresis effects, reducing the reproducibility of measurement results and thus limiting the ability to properly evaluate device properties. This hysteresis can be quantified by the difference of the threshold voltages from the two measurement directions ($\Delta V_{th} = V_{th,1} - V_{th,2}$). In general, the sweep rate affects the amount of charge trapping and therefore the hysteresis, with a faster sweep rate usually resulting in a reduced hysteresis [249]. Furthermore, also the V_G-measurement range can influence the hysteresis, as higher voltages can access deep-level trap states.

To minimize the influence of charge trapping effects on the characteristics of the devices, pulsed transfer measurements are conducted. This measurement technique was specifically important for the characterization of the $Si_{1-x}Ge_x$ devices with an Si/Al_2O_3 interface in Section 5.2 due to a large density of slow interface traps. For each data point, the gate voltage $V_G = V_{G,x}$ is only applied for a short time (the pulse duration t_{pulse}) during which the drain current $I_D(V_{G,x})$ is measured. For the rest of the pulse period, V_G is set back to the base level, usually 0 V, before being pulsed to the next voltage value $V_G = V_{G,x+1}$ to measure the next data point $I_D(V_{G,x+1})$. The shortest possible pulse duration t_{pulse} of 0.5 ms was used for the pulsed measurements, limited by the available measurement setup. However, due to the reduced integration times, the current resolution is severely limited to ≥100 pA in the used setup. As a result, with the pulsed measurements, it is often not possible to fully capture the subthreshold region of the transfer characteristic because it cannot adequately resolve low off-state currents.

Evaluation Remarks

For the evaluation of the device parameters, Python scripts were developed to allow faster and more efficient analysis of a larger number of devices, also at different temperatures or bias conditions. The extraction of the parameters was validated by the generation of verification plots and partial manual evaluation.

3.2.2 Polarity Gate-dependent Transfer Characteristic

In SBFETs the current flow is mainly defined by the charge carrier injection at the Schottky junctions. In TTG RFETs, this injection barrier can be independently controlled by the PG, increasing the transmissibility for tunneling for one charge carrier type while decreasing it for the other. To analyze the modulation of the Schottky barrier with the PG, the I_D/V_{CG} transfer characteristic is measured for multiple different V_{PG} values, typically within the same range of the CG-voltages. Starting from negative V_{PG} values, the transition from a hole-dominant p-type device characteristic to an electron-dominant n-type characteristic is observed. This measurement with two variable input voltages is often plotted in a 2D color map representation to better visualize the operation regimes. In addition, this graph is useful for determining the optimum operating conditions for symmetrical on-state currents.

3.2.3 Output Characteristics

The output characteristic describes the bias voltage (V_{DS})-dependent measurement of the drain current (I_D) while the gate potential (V_G or V_{CG}) is fixed. This I_D/V_{DS} measurement is then repeated for various (control) gate voltages to create a multitude of curves. It gives important insights into the saturation properties for a given bias voltage of the device, as well as the contact properties of the metal-semiconductor junction. In particular, a linear I_D/V_{DS} behavior indicates a (quasi-) ohmic contact, while a nonlinear behavior implies a distinct Schottky barrier for the injection of charge carriers. Plotted in a 2D semi-logarithmic color map representation, with V_{DS} and V_G on the x- and y-axis, it further provides insights into the different transport regimes (TE, TFE, FE) [253, 254]. The measurement of the temperature-dependent output characteristics further allows to extract the activation energies for the injection of carriers from the metal S/D contacts into the semiconductor channel. The temperature-dependent I_D/V_{DS} characteristic for two different gate voltages in an SBFET is shown in Figure 3.9(a).

3.2.4 Activation Energy Evaluation

The effective Schottky barrier height describes the minimum energy required for the injection of charge carriers into the semiconductor channel. As already described in Section 2.3.2, it is strongly influenced by Fermi level, band bending from the applied bias voltage and the temperature. In order to analyze the properties of the metal-semiconductor junction and to gain a deeper understanding of the underlying transport mechanisms, the extraction of the effective Schottky barrier is of great interest. There are several methods available for determining the Schottky barrier height of a metal-semiconductor junction-based device: current-voltage, current-temperature, capacitance-voltage, or photoelectric measurements [161, 249]. In this work, the extraction is carried out via temperature-dependent measurements of the V_{DS}/I_D output characteristic, based on the thermionic emission theory [90].

Since the current flow I_D in the SBFET is a combination of tunneling current and thermionic emission, the individual transport mechanisms (TE, TFE, FE) cannot be distinguished from the measured data. Furthermore, it must be taken into account that the investigated devices incorporate two metal-semiconductor junctions through which the charge carriers are transported. The term *Activation Energy* (E_a) is therefore used instead of the *effective Schottky barrier*, as this is more suitable for describing the total energy required to transport the charge carriers through the heterostructure.

Based on the thermionic emission theory, the drain current density $J_D = I_D/A$ (with A being the cross-sectional area of the semiconductor channel) can be described according to

$$J_D(T) = A^* T^2 \exp\left(\frac{-E_a}{k_B T}\right)\left[\exp\left(\frac{qV_{DS}}{k_B T}\right) - 1\right]. \tag{3.3}$$

The current is evaluated by measuring the output characteristic for five different temperatures from 295 K to 400 K, for low bias voltages V_{DS} between 0 mV to 100 mV. The measurement of the I_D/V_{DS} characteristic for different gate voltages V_G further allows a gate-dependent E_a evaluation. Figure 3.9(a) shows the temperature-dependent output characteristic for an exemplary $Si_{0.67}Ge_{0.33}$ SBFET for two different gate voltages.

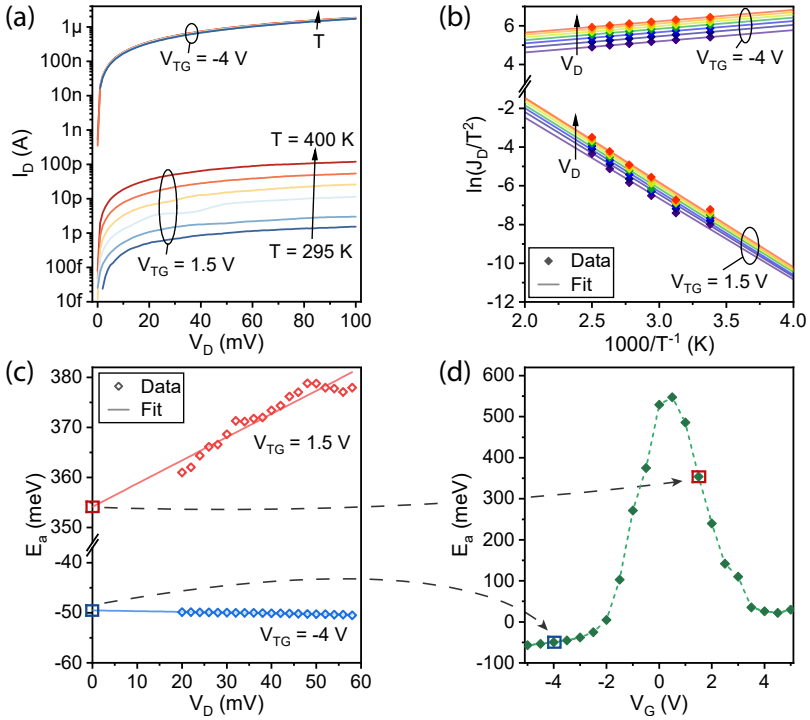

Figure 3.9: Evaluation of the activation energy E_a, based on the example of a $Si_{0.67}Ge_{0.33}$ SBFET. (a) Temperature-dependent output characteristic (T = 295 K to 400 K) shown for two different gate voltages ($V_{TG} = -4$ V and 1.5 V). (b) Arrhenius plot for the two corresponding gate voltages. (c) V_D-dependent activation energies E_a, with a linear fit for extracting the E_a value at $V_D = 0$ V. (d) V_G-dependent E_a plot with the extracted values from (c).

Considering $\exp\left(\frac{qV_{DS}}{k_BT}\right) \gg 1$ and applying the natural logarithm to Equation 3.3, the Arrhenius equation according to

$$\ln\left(\frac{J_D}{T^2}\right) = \frac{1}{T}\left(\frac{-E_a + qV_{DS}}{k_B}\right) + ln(A^*) \tag{3.4}$$

can be formed. The left-hand term shows a linear relationship to $1/T$, which is also shown accordingly in the Arrhenius plot in Figure 3.9(b). From this, the slope $k = 1/k_B \cdot (qV_{DS} - E_a)$ for each bias voltage V_{DS} can be determined. Finally, the expression for the activation energy can be found with

$$E_a = -k \cdot k_B + qV_{DS}. \tag{3.5}$$

Setting $V_{DS} = 0\,\mathrm{V}$, in particular by applying a linear fit through the derived data points in Figure 3.9(b), a distinct data point of the activation energy for the respective gate voltage is extracted. Repeating this extraction method for different gate voltages results in a V_G-dependent activation energy plot as shown in Figure 3.9(d).

In general, the activation energy is extracted at low bias voltages to reduce the influence of band bending. However, in order to get a more detailed insight into the device behavior in

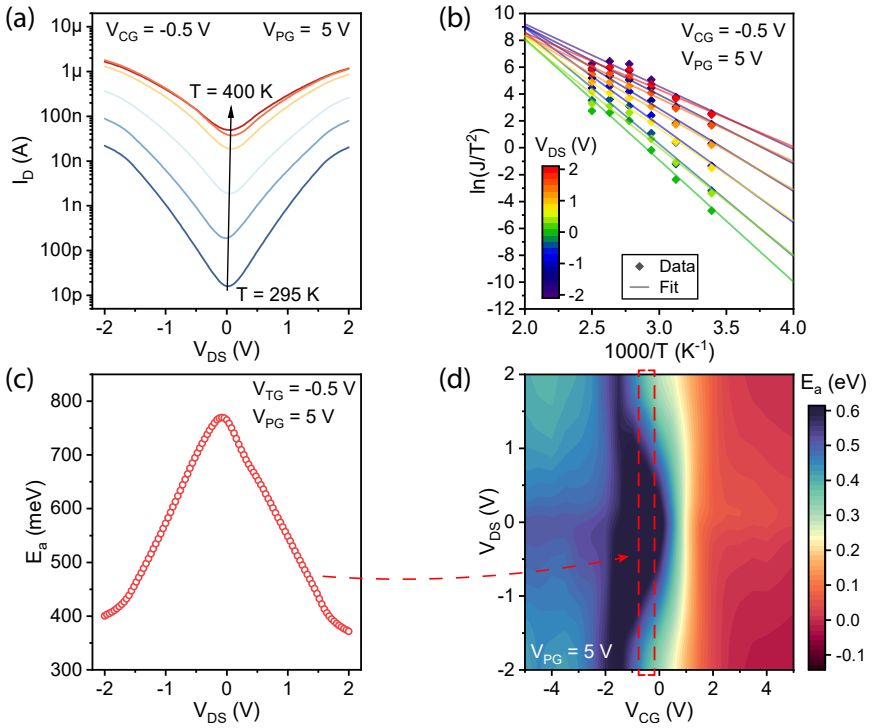

Figure 3.10: Evaluation of the activation energy E_a color maps, based on the example of a $Si_{0.67}Ge_{0.33}$ RFET. (a) Output characteristic measured for an extended bias range V_{DS}, plotted for the n-type operation ($V_{PG} = 5\,\mathrm{V}$) for $V_{CG} = -0.5\,\mathrm{V}$. (b) Arrhenius plot for V_{DS} between $-2\,\mathrm{V}$ to $2\,\mathrm{V}$. (c) The fitted slopes in (b) give the E_a values for the full bias range. (d) Extracted E_a as a function of V_{CG} and V_{DS} in a 2D color map representation.

its actual operating voltage regime, the extraction at higher bias voltages is of particular interest. In this regard, the temperature-dependent output characteristic is measured over a wider range, e.g., ±2 V as shown in Figure 3.10(a) for the measurement of an exemplary RFET in n-mode configuration. The further evaluation for the generation of the Arrhenius plot and the V_{DS}-dependent activation energies is then conducted analogously to before (see Figure 3.10(b,c)). However, instead of fitting the data with a linear fit towards $V_D = 0\,\mathrm{V}$, all E_a data points are plotted accordingly in a 2D color map as a function of V_{DS} and V_{CG} (see Figure 3.10(d)). This reveals the effective barriers under the respective operating conditions and when the dominant carrier type is effectively injected or blocked.

3.2.5 Noise Margins

The concept of noise margins is an important criterion to evaluate the stability of a digital logic circuit to resist the effects of noise and other input voltage variations while still maintaining correct logic levels. They are critical parameters that define how much noise a circuit can tolerate before it incorrectly switches its output [255].

For binary logic levels, the noise margins can be divided into a criterion for the high state (NM_H) and the low state (NM_L). The noise margin high (NM_H) refers to the amount of noise voltage that can be added to the output of a logic gate at a high logic level ("1") before it is interpreted as a low logic level ("0"). The noise margin low (NM_L) accordingly is the tolerance for noise in the logic low state. The two parameters can be evaluated according to

$$\begin{aligned} NM_H &= V_{OH} - V_{IH} \\ NM_L &= V_{IL} - V_{OL}. \end{aligned} \tag{3.6}$$

The voltage levels V_{IL} and V_{IH} thereby define the input threshold voltage when the respective output threshold levels V_{OH} or V_{OL} for the high and low states are reached. As illustrated in the inverter output transfer characteristic in Figure 3.11, by definition these

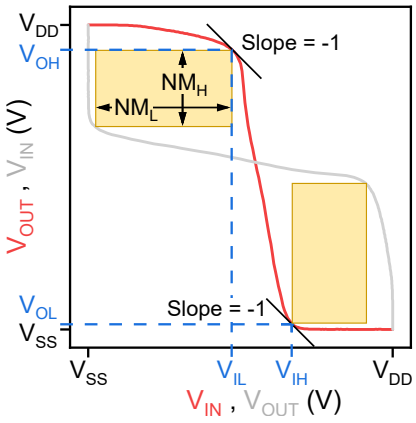

Figure 3.11: Evaluation of the activation noise margins NM_H and NM_L from an inverter output transfer characteristic. The red curve shows the output voltage V_{OUT} in relation to the input voltage V_{IN}. The gray curve shows the same data but with output and input axes reversed.

threshold voltages can be extracted at the points where the slope $= dV_{OUT}/dV_{IN} = -1$ [255]. An abrupt switching at $(V_{DD} - V_{SS})/2$ would thereby be the ideal case for the logic output, resulting in maximized noise margins. In general, CMOS logic gates achieve larger noise margins than comparable NMOS logic gates, as CMOS delivers rail-to-rail outputs, while the V_{OL} level in NMOS is restricted [256]. The gray curve in Figure 3.11 shows the same inverter characteristic as the red one, but with the input and output axes reversed. The intersections of the two curves thereby represent the stable states of a pair of two cross-coupled inverters [255].

To analytically compare the operation of the logic inverter in this work operated at different operation voltages, the noise margin levels NM_H and NM_L are normalized to the supply rail voltages V_{DD} and V_{SS}, according to

$$NM'_{H,L} = \frac{NM_{H,L}}{V_{DD} - V_{SS}}. \tag{3.7}$$

In this case, $NM'_H = NM'_L = 0.5$ would be ideal and represent a rectangular output curve switching at half the supply rail voltage difference $V_{DD} - V_{SS}$. If the output curve is strongly shifted towards V_{DD} or V_{SS} despite a steep switching slope, this results in strongly asymmetrical NMs, e.g., a high NM_L and a low NM_H, with a low stability for one output state.

3.2.6 C/V and P/E Characterization

To optimize the ferroelectric gate stack, in particular the HZO deposition and crystallization parameters as well as its layer thickness, capacitive metal-ferroelectric-metal (MFM) test structures are fabricated and characterized. The bottom metal electrode (e.g., TiN) is thereby sputtered on a highly n-doped Si substrate, followed by the deposition of the HZO layer (ALD) and the circular top gate electrodes with diameters in the range of 75 µm to 150 µm. Capacitive metal-ferroelectric-insulator-semiconductor (MFIS) test structures are fabricated to investigate different interface layers (IL) between the HZO and Si channel and different top gate electrode materials. Instead of depositing a bottom electrode contact, the IL is grown on the p-doped Si substrate, followed by deposition of the HZO and top gate electrode.

The capacitance-voltage (C/V) measurements are then conducted by sweeping a large DC voltage that is superimposed with a small AC signal in the mV range at a frequency of 1 kHz to 10 MHz. The measured current flow is then integrated over time to extract the electric charge Q of the capacitor, which thus results in the capacity of the structure according to

$$C = \frac{\Delta Q}{\Delta V} = \frac{\varepsilon_0 \varepsilon_r A}{t}. \tag{3.8}$$

From the vacuum permittivity ε_0 and the dimensions of the MFM structure, with the area of the circular top electrode A and the thickness of the HZO layer t, the relative

permittivity ε_r of the ferroelectric layer can be extracted. The relative permittivity can be further expressed in terms of the polarization P, according to

$$\varepsilon_r = \frac{\varepsilon_0 E + P}{\varepsilon_0 E} = 1 + \frac{1}{\varepsilon_0} \cdot \frac{P}{E}. \tag{3.9}$$

Due to the nonlinear polarization switching of the ferroelectric material, a nonlinear butterfly-shaped C/V characteristic with two distinct peaks is obtained. If the extracted C/V curve exhibits a counterclockwise hysteresis, as schematically indicated in Figure 3.12(a), this indicates ferroelectric behavior of the investigated structure. A clockwise hysteresis on the other hand would indicate dominant charge carrier trapping effects.

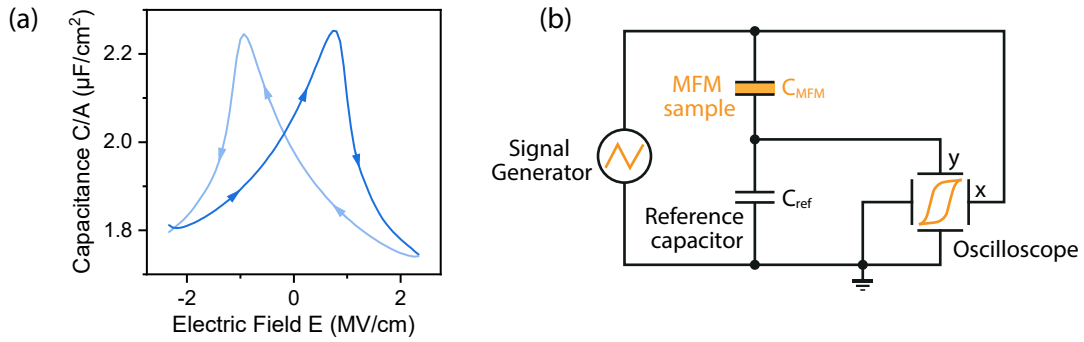

Figure 3.12: (a) C/V measurement of an MFM structure showing a butterfly-shaped curve with a counterclockwise hysteresis. (b) Sawyer-Tower circuit for measuring the P/E characteristic.

In MFIS capacitive structures, the capacitance of the semiconductor substrate and the insulating interface layer, both connected in series with the capacitance of the ferroelectric layer, also play an important role during the measurement. Due to the formation of depletion and accumulation regions near the semiconductor interface, the capacitance changes strongly depending on the applied voltage. In an n-doped semiconductor, when a positive voltage is applied to the metal, electrons are attracted to the surface, resulting in an accumulation of carriers near the interface and hence an increase in capacitance. At negative voltages, a depletion region is formed, resulting in a decrease in capacitance. Due to the large influence of the capacitance of the Si substrate in series with the IL and the HZO, the resulting C/V characteristic has a distinct S-shape. From the direction of the hysteresis, information about the ferroelectric polarization or trapping effects can be extracted. A clockwise hysteresis indicates a dominant trapping behavior due to high trap densities at the interfaces or in the deposited layers. A counterclockwise hysteresis indicates fixed charges induced by the ferroelectric polarization of the HZO.

For recording the P/E characteristic curve, with the polarity P depending on the applied electric field E, the Sawyer-Tower circuit is used [257, 258]. The schematic of this circuit is shown in Figure 3.12(b). A reference capacitor is connected in series with the MFM structure to sense the amount of charge across the ferroelectric in response to the triangular voltage signal [132]. Thereby, both capacitors have the same charge, and the ratio $V = Q/C$ results in different voltage drops proportional to the capacity. A reference capacitor with a nominal capacitance of $C_{ref} = 10\,\text{nF}$ is selected. This is significantly larger

than the capacity of the measured device to minimize the voltage drop across the reference [259]. The signals are typically fed directly into an xy-mode oscilloscope to directly visualize the polarization curve, where the x-axis is proportional to the input voltage and the y-axis is proportional to the measured electrical polarization. The polarization of the MFM capacitor can then be extracted by

$$P \approx \frac{Q}{A_{MFM}} = \frac{C_{ref} \cdot V_{ref}}{A_{MFM}}. \tag{3.10}$$

From this P/E characteristic, the remnant polarization P_r and the coercive field E_c can be extracted (see Figure 2.3(b)).

3.2.7 Polarization State Measurements of Ferroelectric Transistors

To characterize the transistors with the integrated HZO layer (FeSBFETs and FeRFETs) and analyze their ferroelectric switching behavior, pulsed measurements are used. Figure 3.13 schematically shows the measurement principle for the characterization of an FeRFET. Short pulses with a pulse width $t_{pulse} = 0.5\,\text{ms}$ of high amplitudes are thereby applied to the top gate electrode (TG) to switch the ferroelectric polarization state of the HZO layer and therefore the electrical characteristic of the device. During the pulsing sequence, all other device terminals (D, S, BG) are kept grounded. Each pulsing operation consists of three consecutive pulses of alternating polarity, with the amplitudes V_{set} and V_{reset}. The first two pulses, a set pulse followed by a reset pulse, are performed to reset the polarization state and reduce the influence of previous pulses or measurements. The last pulse of this sequence, with the same pulsing amplitude V_{set} as the starting pulse, switches the device into the desired polarization state for the measurement. A positive set pulse is thereby used to induce a polarization state with a net positive charge towards the semiconductor channel (and the metal-semiconductor interfaces). Negative V_{set} pulse amplitudes are used to flip the polarization state in the negative direction. After applying the pulse sequence, the transfer characteristic of the polarized FeSBFET is measured. In this work, this is typically done by sweeping the back gate electrode (V_{BG}) in both directions while measuring the drain current flow I_D. A constant bias voltage V_{DS} is thereby

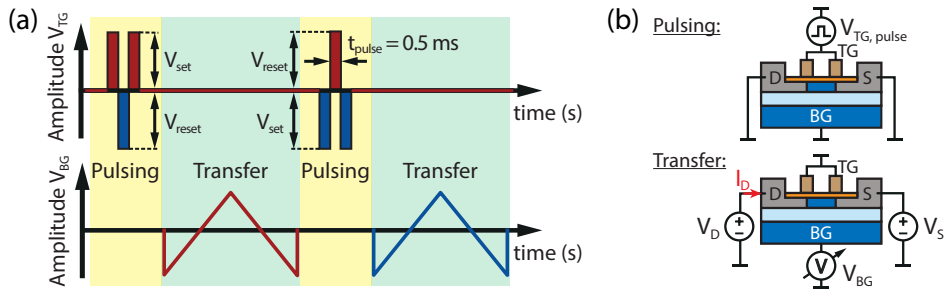

Figure 3.13: (a) Pulsing schematic for measuring the FeFET polarization states. (b) Configuration of the device during pulsing and transfer measurement. The pulsing sequence is applied via the TG electrode, while the drain, source and back-gate terminals are set to 0 V. For measuring the transfer characteristic, V_{BG} is swept in both directions while a constant V_{DS} is applied.

applied to the device, with the TG electrode being grounded. Therefore, only the electric field induced from the ferroelectric layer is gating the device from top. Note that large V_{BG} in the range of ±20 V needs to be applied to modulate the current flow due to the thick BOX (100 nm) between the BG contact and the semiconductor channel. In general, the device can also be modulated via the TG electrode, which is also used to polarize the HZO. However, the remanent polarization of the HZO is directly superimposed on the TG voltage, reducing the direct influence of the ferroelectric response.

Gradual Polarization Switching Measurements

To analyze the influence of the pulse amplitude on the polarization of the HZO layer and thus on the electrical behavior of the device, a measurement sequence according to Figure 3.14(a) is used. This measurement is of particular interest for the determination of intermediate polarization states from a gradual switching of the ferroelectric domains. In this regard, the amplitude for the set pulse V_{set} is gradually increased for each set pulsing sequence, and its electrical response is measured afterwards by modulating V_{BG}. Before each measurement with the variable set pulse amplitudes, the device is always reset to the same polarization state of opposite polarity by applying a reset sequence with a constant V_{reset} amplitude. This reset state is also measured accordingly to ensure that the device has been properly reset to the initial state.

Retention Measurements

The storage capability of a non-volatile device is one of the most important characteristics that indicates how long the stored information is retained. In this regard, the measurement sequence according to 3.14(b) is employed. After applying the pulsing sequence to set the device in the respective polarization state, several consecutive measurements are performed, each separated by a waiting time Δt. In between the measurements, the device remains connected to the probe station, with all terminals set to 0 V. By comparing the recorded transfer characteristics, the progression of, e.g., on-state currents over time can be analyzed and conclusions about depolarization effects can be drawn.

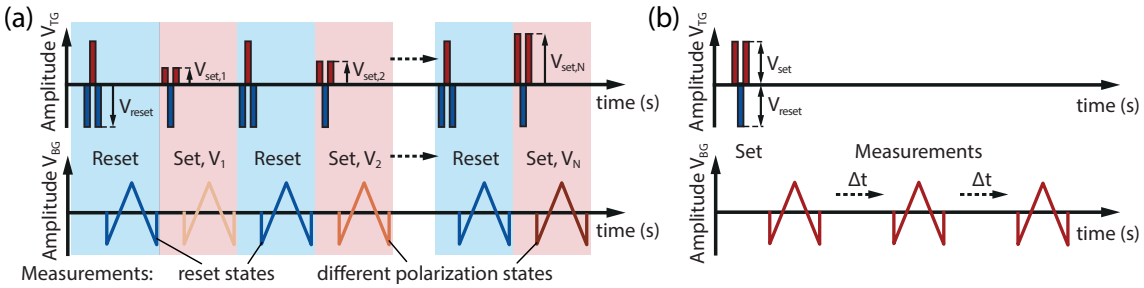

Figure 3.14: (a) Measurement sequence for analyzing the influence of variable pulsing amplitudes V_{set}. Before each set sequence, a reset sequence is applied to set the FeFET to a defined initial state of opposite polarization. (b) Schematic of the retention measurement. After setting the polarization state, several measurements are carried out, separated by a time interval Δt.

Results and Discussion

Chapter 4

Al-Si based Multi-Gate Transistors

The first part of this chapter focuses on the monolithic contact formation of Al to Si. The characteristics of this novel heterostructure formation process are studied, supported by detailed analysis of the formed interfaces and crystal structures, as well as electrical properties of the Al leads. This reproducible contact formation is thereby key for the realization of the devices throughout this work. Integrated into SBFETs the electrical transport characteristics of the Al-Si-Al heterostructures are investigated. Subsequently, a three top-gated (TTG) architecture is used to realize RFETs that can switch their device characteristics between n-type and p-type operation during runtime. This device concept is very promising to reduce the transistor count of symmetric functions in circuits, leading to increased functional density and energy efficiency [14, 18]. Furthermore, RFETs may enable new approaches for adaptive computing and hardware security [13, 25]. A detailed characterization and evaluation of the individual RFETs also addresses the high reproducibility of the manufacturing method, which is essential for large-scale integration in circuits.

The second part of this chapter then demonstrates the integration of RFETs into complementary and combinational logic gates, including inverters, reconfigurable NAND/NOR and XOR/XNOR gates, highlighting the potential of this flexible device concept. Ultimately, the first physical implementation of a full adder using only 8 physically identical RFETs is shown. Next, a multi-wire RFET is presented as a method for increasing the drive currents of the individual devices. Finally, in the last part of the chapter, the influence of replacing the CMOS-incompatible Au by Al in the gate stack is analyzed.

The following results and discussion from this chapter are based on the author's work in publications about Al-Si heterostructure formation [LW14], the realization of RFETs [LW10, LW12], and their integration in complementary logic gates [LW6, LW8][LWC4].

4.1 Structural Analysis of Al-Si-Al Heterostructures

Metal-semiconductor-metal heterostructures are the basis of all devices analyzed in this thesis. Al was chosen due to its mid-gap alignment in Si, however, reliable junction formation between the two materials had been missing prior to this work. Therefore, a reliable fabrication method leading to reproducible Al-Si junctions had to be developed here. As already discussed in more detail in Section 3.1.2, these heterostructures are formed by contacting Si mesa structures, patterned from an SOI substrate, with Al pads and then using RTA to form the Al-Si heterojunctions. In temperature series experiments, 773 K was found to be the optimal temperature, as controllable reaction rates could be observed. Below this temperature ($\leq$723 K) no reaction was visible.

A schematic of the Al-Si heterostructure formation process is shown in Figure 4.1(a). The microscope image in Figure 4.1(b) shows an Al-Si-Al heterostructure fabricated by this exchange process, with the Al leads extending from the lithographically defined Al contact pads into the mesa structure and monolithically connecting the ~3.6 µm long unreacted Si channel. Several consecutive annealing steps can be conducted to precisely tune the position of the Al-Si interface and therefore further reduce the Si channel length (see Figure 4.1(c)). Examination of Al-Si diffusion in 15 nm thick Si nanosheets with structural widths W ranging from 300 nm to 700 nm reveals an increased exchange rate for reduced cross-sections A, with exchange rates of (50.7 $\pm$ 3.8) nm/s for the narrowest structures. The data can be fitted to a $1/W$ function, which, for a constant height H of the nanosheets, is directly proportional to the inverse of their cross-sectional area (~$1/A$), indicating volume diffusion [186, 260]. Note that for the evaluation of the Al-Si exchange rates in Figure

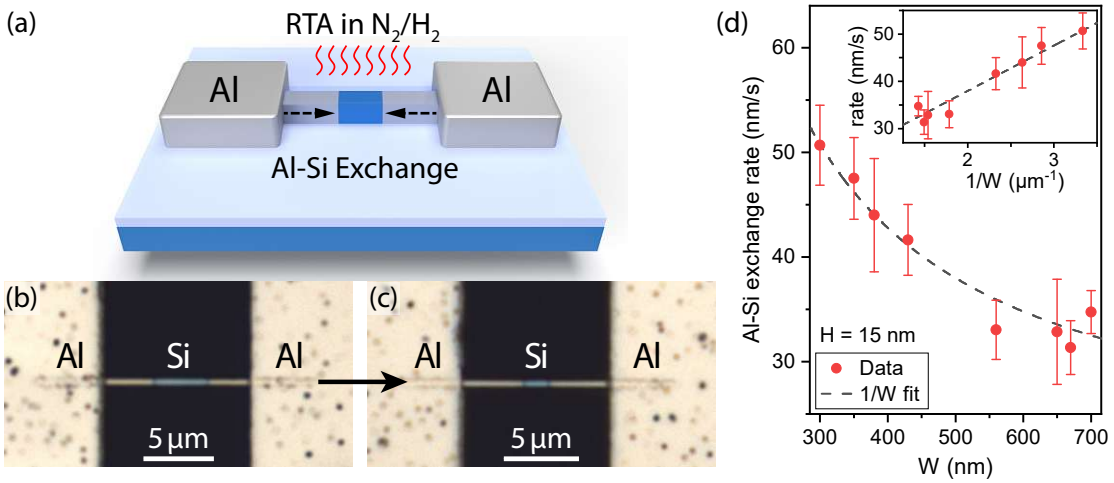

Figure 4.1: (a) Schematic illustration of the Al-Si-Al heterostructure formation. (b,c) Microscope images showing the annealing progress, where the Si channel length is reduced over time. (d) Al-Si exchange rate in relation to the width of the Si nanosheets. The data is fitted using a $1/W$ function, indicating volume diffusion. The inset shows the linear relation between the exchange rate and the inverse structure width $1/W$.

4.1(c), the structures were annealed for 26 s at 773 K, excluding an ∼12 s heat-up time of the furnace to reach the process temperature. With increasing annealing duration t it can be assumed that the reaction rate decreases proportional to $\sqrt{t}$, as observations in Ge nanostructures have shown [LW17][175] and as expected for a diffusion limited process. Furthermore, variations in the exchange rate are evident even for nanosheets of similar width. These can be partially attributed to variations in the Al-Si contact area, such as geometric differences and residual patchy oxide layers. Nevertheless, comparable rapid thermal contact formation processes reveal the significantly higher variability of Ni-silicide formation rates when employing $NiSi_2$ contacts [163].

To analyze the formed Al-Si-Al heterostructure in more detail, scanning transmission electron microscopy (STEM) and energy-dispersive X-ray spectroscopy (EDX) analysis were conducted by our project partners at EMPA. The high-angle annular dark-field (HAADF)-STEM image in 4.2(a) shows the cross-sectional cut across the Al-Si-Al heterostructure on top of the 100 nm thick BOX and the Si base substrate. The EDX image in Figure 4.2(b), with the line scan along one Al-Si interface in Figure 4.2(c), shows the elementary composition of the formed heterostructure. No Al contamination of the remaining Si segment can be detected within the EDX resolution limit (<1 %). The EDX image further shows that the thermally grown SiO_2 cap encapsulating the remaining Si-segment as well as the formed Al leads is still intact after the thermal exchange process. In the high-resolution (HR)STEM image in Figure 4.2(d), the abruptness of the Al-Si interface is revealed, ranging from a few nm up to the atomic level. It is clearly evident that the reacted Al lead is

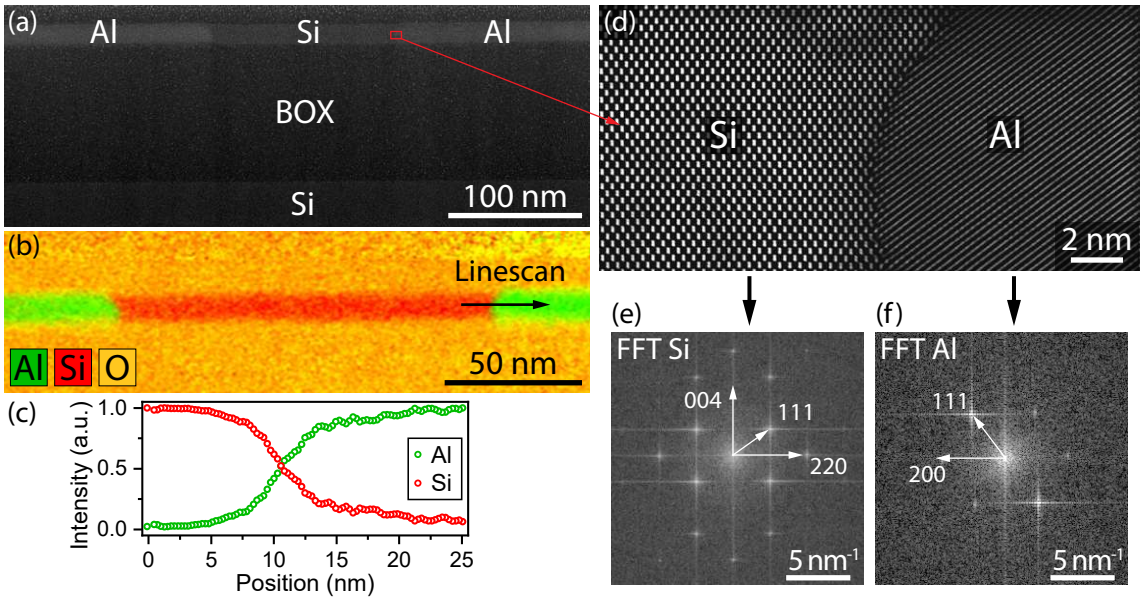

Figure 4.2: (a) HAADF-STEM image of the entire Al-Si-Al heterostructure atop the BOX and the Si base substrate. (b) EDX map of the heterostructure. A line scan across the Al-Si interface mapping the Al and Si content is shown in (c). (d) Close-up HRSTEM image of the Al-Si interface, with the FFT patterns of the Si and Al segments (zone axis [110]) in (e) and (f), respectively.

mono-crystalline, as it was also discovered in Al-Ge exchange reactions [62][LW17]. The Al and Si crystals are thereby different in lattice constants and crystal orientation. The local fast Fourier transform (FFT) patterns of the Al and Si segments in Figure 4.2(e) and (f), respectively, provide more information about the crystal structure. After the exchange reaction, the Si segment still remains in its initial diamond structure. The reacted Al segment is identified as a face-centered cubic (fcc) crystal. Both crystals are oriented in a [110] zone axis, with a mutual in-plane rotation to each other. This presumably leads to stress relaxation and compensation of the lattice mismatch of both materials.

Remarkably, no void formation or spiking was observed in the monolithically formed Al leads in any analyzed sample. This is in contrast to investigations in bulk and thin-film Al-Si reactions that show non-uniform interface formation, massive void creation and spiking, leading to high variability in the contact area and local field enhancement [60, 61]. Also there, grain boundaries can lead to severe electromigration problems [59]. These problems and the limited thermal budget have led to the abandonment of Al from front-end-of-line (FEOL) processes in current CMOS technology [261]. As the Al-Si exchange reaction here is taking place in nanoscaled Si structures, such as nanosheets or nanowires [LW14], flat, void-free and highly abrupt interfaces are observed. Within structures scaled down towards thicknesses beyond the typical grain sizes of bulk Al, single-crystal formation of Al is observed. It is also expected that electromigration should be sufficiently suppressed, as the weak reliability sites are typically located at the grain boundaries [59, 262]. Furthermore, the Al grows lattice oriented to the Si region, possibly guaranteeing a closed surface formation rather than energetically unfavorable voids.

It can be assumed that, at the annealing temperature of 773 K, Si atoms are diffusing into the bulk Al contact pads and are replaced by Al atoms. This exchange mechanism is caused by highly asymmetric diffusion coefficients of the Al-Si material system (see Table 2.4). Importantly, the diffusion of Si in Al is 14 orders of magnitude higher than vice versa, preventing the Al from diffusing into the Si segment and thus contaminating it. Furthermore, Al atoms are efficiently supplied via fast self-diffusion (Al in Al), compensating for the out-diffusion of Si atoms. As a result of the replacement of Si with Al, the Al-Si interface migrates successively along the pristine Si nanostructure, leading to a reduction in the Si channel length connected by monolithic Al leads.

After sufficient annealing time, the Si nanosheet can be completely exchanged with Al, resulting in pure and crystalline Al (c-Al) nanosheet, as it is shown in the microscope image in Figure 4.3(b). Similar to findings in the Al-Ge exchange in Ge nanosheets with nanoscaled sheet widths [LW17][LWM1], it is expected that they only feature a single grain boundary at the location where the diffusion fronts from both sides merge. The fact that no other inner grains seem to form within the Al metallization has positive effects for low resistivities of $\rho = 6.65 \times 10^{-8}\,\Omega\,\mathrm{m}$ at room temperature. Compared to commonly used Ni-silicides, with resistivities ranging from $10 \times 10^{-8}\,\Omega\,\mathrm{m}$ to $38 \times 10^{-8}\,\Omega\,\mathrm{m}$ depending on the silicide phase [164, 263], the resistivity of pure Al leads is significantly

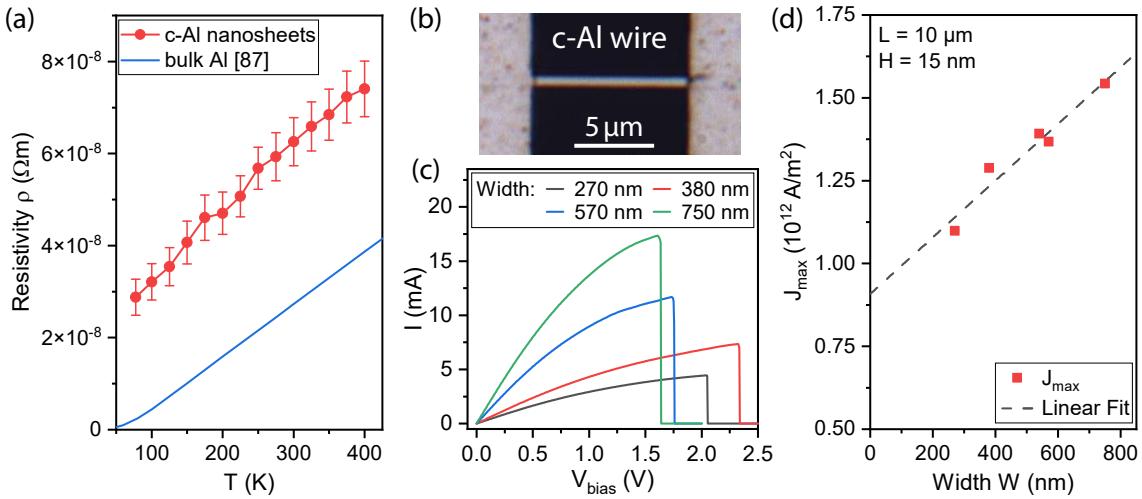

Figure 4.3: (a) Temperature-dependent resistivity ρ of fully exchanged c-Al nanosheets, compared to the resistivity of bulk Al from [87]. (b) Microscope image of a c-Al nanosheet with L = 10 µm, W = 750 nm and H = 15 nm connecting the two sputtered Al contact pads. (c) I/V data for different sheet widths W, with the bias voltage V_{bias} slowly increased until the failure point of the nanosheet to extract the peak current densities in (d).

lower. The temperature-dependent measurement in Figure 4.3(a) shows that the resistivity is decreasing with lowered temperature, down to $3.15 \times 10^{-8}\,\Omega\,\mathrm{m}$ at 77 K, following the trend of bulk Al [87]. This decrease in resistivity is attributed to the for metals typical decrease of phonon scattering [264]. The ∼2.5 times higher resistivity compared to bulk Al at room temperature can be explained by the increased influence of surface scattering in nanostructures [265]. Furthermore, these results cannot rule out that dissolved Si in the Al, despite its extremely low concentration, may also contribute to a slight increase in resistance [179]. At temperatures below 1.46 K, a transition of the c-Al leads to a superconducting state is expected [266], making it highly interesting for superconductor-semiconductor hybrid quantum systems, such as gate-tunable Josephson junctions and superconducting qubits [189].

To characterize the maximum current density in these c-Al nanosheets, the applied bias voltage is increased until the current limit is reached and the nanosheet breaks. Figure 4.3(c) shows this measurement for four Al nanosheets with different sheet widths, with the widest sheet having the lowest resistance and therefore also the highest transport currents. The rapid drop of the current indicates the breakdown point of the sheet due to the excessive current stress. Note that at high bias voltages, close to the breaking point of the nanosheets, the otherwise linear increase in current is distorted, probably as increased phonon scattering leads to self-heating of the Al lead, increasing its resistance and reducing the current flow. The peak values of the measured currents are then extracted to calculate the maximal current densities J_{max} of the nanosheets considering their cross-sections, shown in Figure 4.3(d). Very high current densities of up to $1.54 \times 10^{12}\,\mathrm{A/m^2}$ at room temperature are reached, which is in the range of Ni-silicides [263]. The high

current-carrying capabilities can also be attributed to the absence of grain boundaries. Interestingly, J_{max} is slightly lowered with decreasing sheet widths W. This is presumably due to poorer heat dissipation from the locally generated heat in the thin cross-section of the sheet to the large Al contact pads. However, in c-Al NWs with diameters below 100 nm, approaching the electron–phonon scattering length, an increase in the breakdown current was demonstrated due to reduced lattice heating [266].

4.2 Al-Si-Al Schottky Barrier Field-Effect Transistors

The Al-Si-Al heterostructures are then integrated in SBFETs to investigate their electrical properties. Therefore, a 12.5 nm thick SiO_2 gate oxide was thermally grown on the Si mesa structures prior to the Al contact formation, with a remaining Si channel thickness of 15.4 nm. Lastly, the Ti/Au top gate is deposited, covering both Al-Si interfaces. Figure 4.4(a) shows the false-color SEM image of the final single top-gated SBFET, with a channel width $W = 430$ nm and a Si channel length of $L_{Si} = 1$ µm. The entire gate stack is shown in the cross-sectional HRSTEM and EDX in Figure 4.4(b,c), with the Si channel on top of the 100 nm thick BOX and the Si substrate. The SiO_2 gate oxide and the Ti/Au top gate layers cover the Si nanosheet channel from three sides, resembling a tri-gate architecture [10]. Note that the contact formation was carried out in forming gas to passivate the Si/SiO_2 interface. The measured transfer characteristic in Figure 4.4(d) reveals ambipolar behavior with very symmetric on-state currents I_D for both electron ($V_G > 0$ V) and hole conduction ($V_G < -1$ V). This can be attributed to the near mid-gap Fermi level pinning of the Al contact to the Si channel [193]. The current flow can be electrostatically

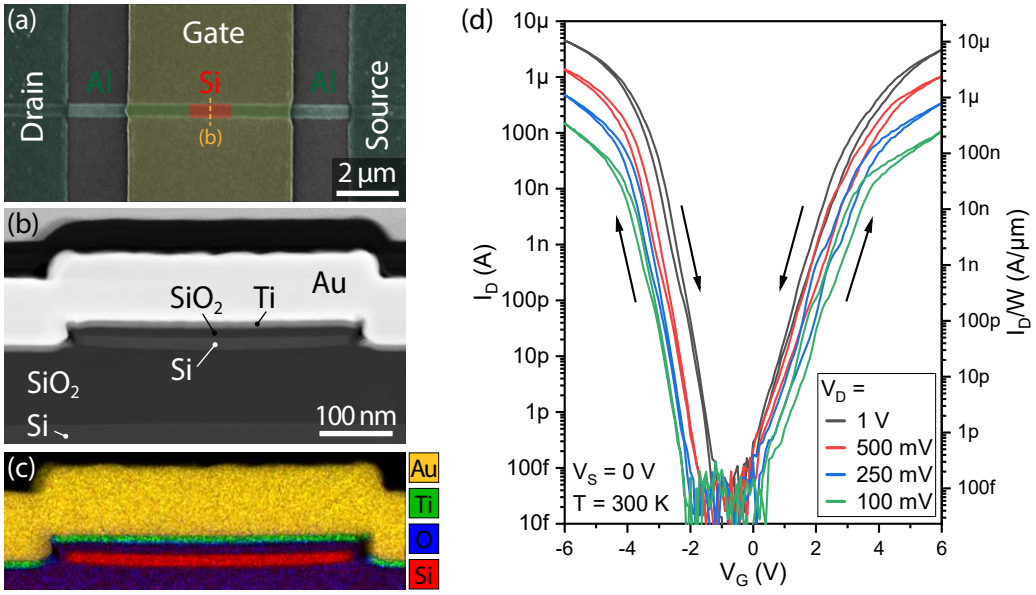

Figure 4.4: Al-Si SBFET on SOI. (a) Colored SEM image of a top-gated Al-Si-Al heterostructure. (b) Cross-sectional HRSTEM image and (c) EDX map showing the gate stack. (d) Transfer characteristic of the SBFET for different bias voltages V_D, at $V_S = 0$ V. $W = 430$ nm, $L_{Si} = 1$ µm.

modulated over more than seven orders of magnitude, with off-state currents below the resolution limit of the measurement setup. At $V_D = 1\,\mathrm{V}$, maximum currents I_D of 2.84 µA (6.6 µA/µm) for the n-branch and 4.45 µA (10.34 µA/µm) for the p-branch are reached, with subthreshold slopes (S_{th}) of 456 mV/dec and 268 mV/dec, respectively. Only a small dependency on the V_G sweeping direction is evident, with the I_D curves being slightly higher when changing from an on- to an off-state. The low hysteresis can be attributed to the good quality of the thermally grown SiO_2 gate oxide and its low interface state density to the Si channel.

The output characteristic in Figure 4.5 shows the bias-dependent current flow I_D, with V_G increasing to 6 V for electron-dominated (a) and to −6 V for hole-dominated conduction (b). The respective band diagrams of the SBFET are shown as insets. In both cases, the I/V characteristic shows an SBFET-typical, nonlinear increase with V_D, due to changes in the shape of the tunnel barrier at the Al-Si Schottky junction. As the bias voltage increases, the barrier width decreases, leading to an increased tunnel probability and thus an exponential increase in current. The full range output map in a semi-logarithmic scale is given in the color map in Figure 4.5(c), showing a steeper subthreshold current modulation with V_G for the p-branch.

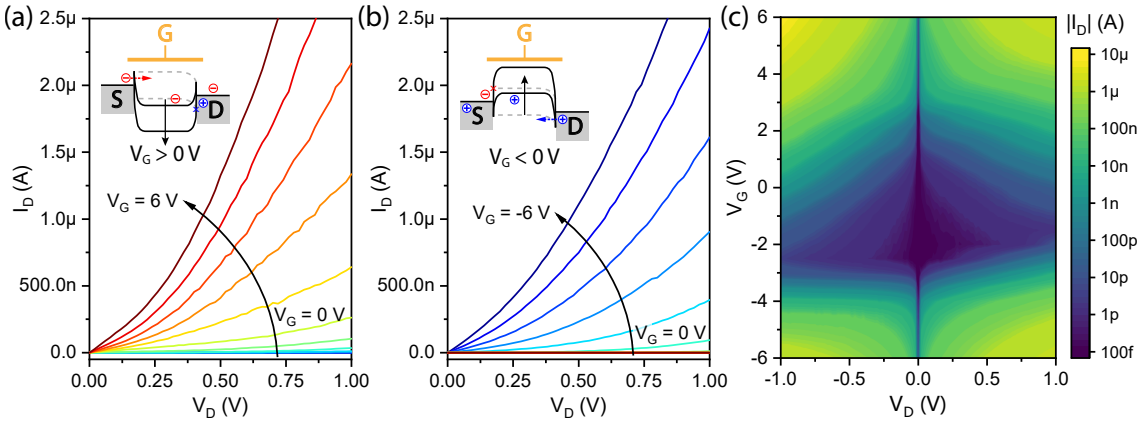

Figure 4.5: Output characteristic of the Al-Si SBFET of Figure 4.4. In (a) V_G is increased to positive voltages for preferred electron conduction, and in (b) to negative voltages for hole conduction. The schematic band diagrams for both conditions are shown as insets. (c) Color map representation of the complete output characteristic in log scale.

To test the thermal stability of the devices, the temperature-dependent transfer characteristic was measured in the range of 300 K to 400 K at $V_D = 1\,\mathrm{V}$, as shown in Figure 4.6(a). The characteristic was measured at $V_D = 1\,\mathrm{V}$ ($V_S = 0\,\mathrm{V}$) with V_G increased from −6 V to 6 V. A clear increase in current with temperature is evident throughout the transfer curve, with the off-currents around the intrinsic point being strongly temperature dependent, marking the thermionic emission regime. Compared to the off-currents, the on-currents increase only slightly, indicating a tunneling-dominated charge injection. This leads to a distortion of the I_{on}/I_{off} ratio at higher temperatures, although the curves remain well tunable over five orders of magnitude.

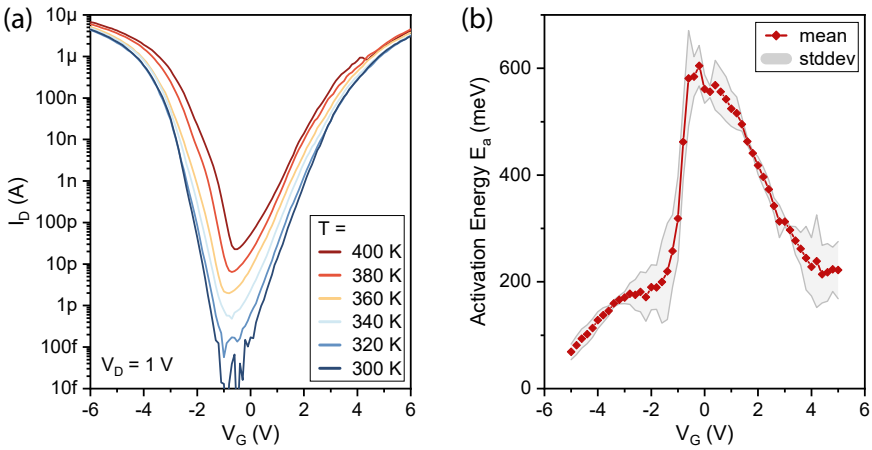

Figure 4.6: (a) Temperature-dependent transfer characteristic of the Al-Si SBFET from Figure 4.4 for $V_D = 1\,\mathrm{V}$. (b) Activation energy E_a as a function of V_G, evaluated for three comparable devices.

By measuring the output characteristic over temperature, the activation energy E_a can be extracted (see Section 3.2.4). Figure 4.6(b) shows E_a in relation to the applied gate voltage V_G, evaluated for three comparable devices. Distinct activation energies were extracted at both on-states, with slightly higher injection barriers for electrons with $E_a = 220\,\mathrm{eV}$ at $5\,\mathrm{V}$ than for the holes with $E_a = 69\,\mathrm{eV}$ at $-5\,\mathrm{V}$. This results in very symmetrical ambipolar behavior, with slightly higher on-currents and steeper subthreshold slopes for the p-type conduction. The highest barrier values were extracted at $V_G = -0.2\,\mathrm{V}$ with 605 eV, close to half the value of the energy band gap of Si. This leads to effective blocking of both carrier types, resulting in low off-currents.

4.3 Reconfigurable Si-based TTG FETs

Since the fabrication of Al-Si-Al heterostructures and their integration into single top-gated SBFETs has reproducibly yielded very symmetric ambipolar device characteristics, they are highly promising for their use in reconfigurable electronics. Therefore, instead of a single global top gate, three top gate electrodes are now placed atop the metal-semiconductor-metal heterostructure, allowing independent control of the carrier injection barrier and the channel conductance, significantly enhancing the device functionality compared to conventional transistors.
A three top-gated (TTG) RFET is shown in Figure 4.7(a,b), with the two connected PGs placed directly atop the two Al-Si junctions and the CG in the middle covering the Si channel. The RFETs were fabricated with the same gate stack as the single top-gated device from the previous section, with an estimated SiO_2 thickness of 12.5 nm and 15.4 nm Si channel height. By setting a positive voltage on the PG, with $V_{PG} = 7\,\mathrm{V}$, the device is operated in a p-type configuration. As schematically shown in 4.7(c), electrons are efficiently injected into the semiconductor channel, while holes are blocked by the introduced electrostatic barrier at the metal-semiconductor junction. The current flow is modulated

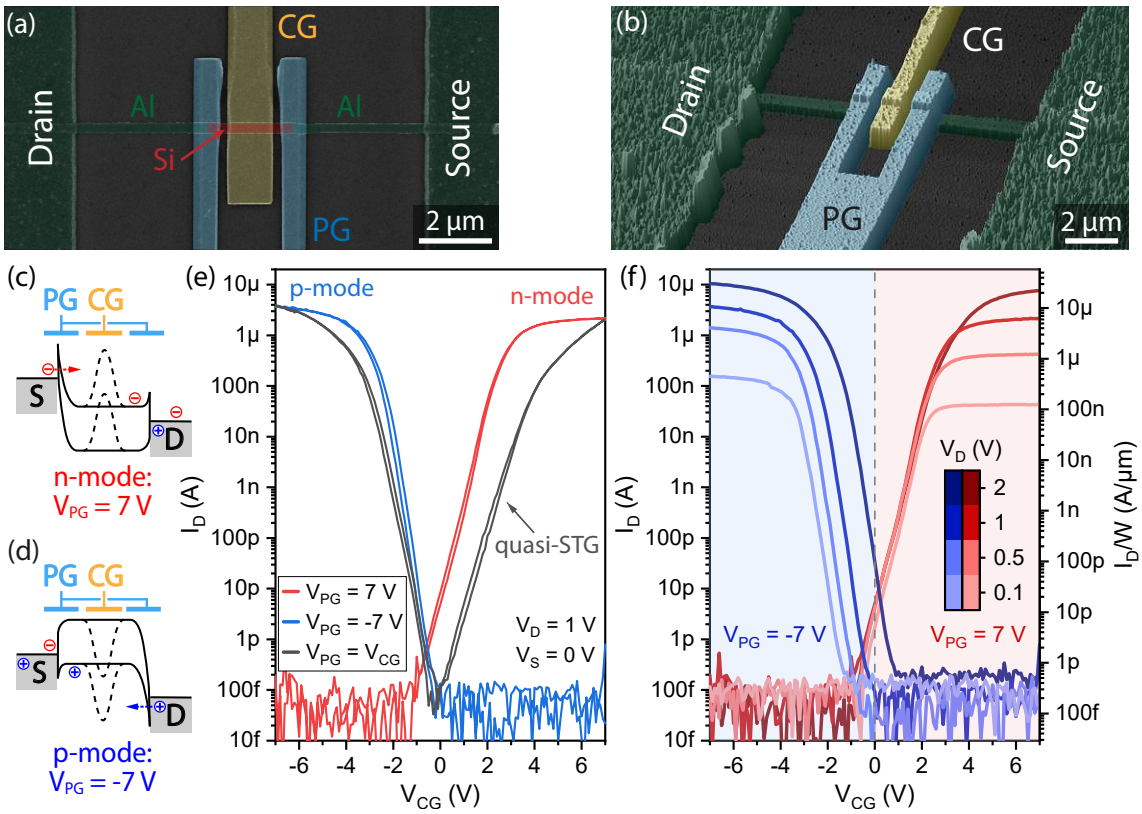

Figure 4.7: (a) Colored SEM and (b) AFM images of an Al-Si-Al heterostructure-based RFET, with a Si channel length $L_{Si} = 2.2\,\mu m$ and a sheet width $W = 350\,nm$. Schematic band diagrams for the n-type (c) and p-type operation (d) of the RFET. (e) Transfer characteristic showing symmetric n- (red) and p-type (blue) operation at $V_{PG} = \pm 7\,V$, at a drain voltage of $V_D = 1\,V$ ($V_S = 0\,V$). The black line shows the operation as a quasi-STG transistor, with $V_{CG} = V_{PG}$. Only a very small hysteresis is visible when changing the sweeping direction of V_{CG} for all configurations. (f) Transfer characteristic for different drain voltages in the range between 100 mV and 2 V, tuning the on-state symmetry.

by the CG atop the Si channel, reaching the on-state at $V_{CG} = V_{PG} = 7\,V$. With inverted voltages ($V_{PG} = -7\,V$, see Figure 4.7(d)), the RFET is set to p-mode conduction, with a hole-induced current flow and the electrons being blocked by the junction barriers. Figure 4.7(d) shows the transfer characteristic of an Al-Si-Al-based RFET for $V_D = 1\,V$, with the red curve showing the n-mode and the blue curve for the p-mode. With on-state currents of $I^n_{on} = 2.15\,\mu A$ ($6.23\,\mu A/\mu m$) and $I^p_{on} = 3.66\,\mu A$ ($10.56\,\mu A/\mu m$), highly symmetric operation is achieved. The off-current in both modes is found to be in the range or even below the noise floor of our measurement setup ($\sim$100 fA), indicating an excellent blocking of the undesired charge carrier type, as well as the suppression of gate-induced drain leakage (GIDL)-like effects [57][LW12]. This results in very high I_{on}/I_{off} ratios above 10^8, reached for both operation modes. Furthermore, as seen for the STG SBFETs in the previous section, there is hardly any dependence on the V_{CG} sweep direction due to the good quality of the thermally grown SiO_2 gate oxide and its interface to the Si channel.

By simultaneously tuning both the CG and the PG, with $V_{CG} = V_{PG}$ in a quasi-STG mode, the ambipolar characteristic of an STG SBFET can be replicated. The same on-state currents at $\pm 7\,\mathrm{V}$ are reached, as these states exactly match the conditions of the RFET on-states. However, S_{th} is smaller for the TTG operation as the quasi-STG, and the transition from the on- to the off-state and towards the other branch of the ambipolar characteristic is steeper than with fixed V_{PG}. This can be explained by the fact that, in addition to the changing channel barrier with V_{CG}, the tunnel barrier of the dominant carrier type increases with decreasing absolute values of V_{PG}, leading to a decrease in carrier injection and a more efficient decline in current flow.

By adapting the bias voltage, as shown in Figure 4.7(f) with V_D varied between 100 mV and 2 V, the on-states can further be tuned, reaching exceptional symmetry values I^p_{on}/I^n_{on} of up to 1.38 at $V_D = 2\,\mathrm{V}$. Since also other important transistor parameters, such as the threshold voltages ($V^n_{th} = 2.3\,\mathrm{V}$, $V^p_{th} = -2.8\,\mathrm{V}$) and the subthreshold slopes ($S^n_{th} = 440\,\mathrm{mV/dec}$, $S^p_{th} = 320\,\mathrm{mV/dec}$) at $V_D = 1\,\mathrm{V}$ are very symmetric for both modes, these Al-Si-based RFETs are already promising for an integration into reconfigurable logic circuits. The slightly higher on-state currents for the p-mode can thereby be attributed to the slightly lower Schottky barriers for the hole injection [121]. Figure 4.7(f) further shows a clear shift or fanning of the subthreshold region (and V_{th}) to higher V_{CG} with increased V_D for the p-mode due to the asymmetric bias condition, with V_S fixed to 0 V. This is a typical behavior of SBFETs caused by the influence of V_D on the energy band landscape in the device, which also changes the carrier injection [57]. A more detailed explanation of this effect is given in Section 2.4, Figure 2.12. Inverting the bias to negative V_D values would lead to a "fanning" of the n-mode, as the electron injection would then be more affected [LW12]. To avoid this asymmetric fanning of the transfer characteristic with increasing V_D due to asymmetric changes of the energy band landscape, the bias will later be set asymmetrically, i.e., with $V_D = -V_S$.

To measure the reproducibility of our Al-Si-based RFET fabrication process, 20 comparable devices were characterized and evaluated. The most characteristic RFET device parameters are plotted in Figure 4.8, with the on- and off-currents (I_{on}, I_{off}), on-current symmetry, V_{th} and S_{th}. Thereby, an overall low device-to-device variability for lab devices is obtained, which is highly important when integrating multiple transistors into circuits, indicating good reliability and reproducibility of the Al-Si contact formation process. All devices thereby show good on-currents $>1\,\mu\mathrm{A}/\mu\mathrm{m}$ (normalized to the channel width W) for both operation modes compared to most RFET works. Mean current values of $(6.2 \pm 2.4)\,\mu\mathrm{A}/\mu\mathrm{m}$ for the n-mode ($V_{PG} = 7\,\mathrm{V}$) and $(11.8 \pm 3.4)\,\mu\mathrm{A}/\mu\mathrm{m}$ for the p-mode ($V_{PG} = -7\,\mathrm{V}$) are reached, while the off-currents remain in the range of the measurement resolution limit. Almost all devices thereby show a slightly predominant p-mode, but still very high on-current symmetry ratios of 2.09 ± 0.9. Furthermore, a high degree of symmetry and stability is also obtained for V_{th}, with $V^n_{th} = (1.82 \pm 0.22)\,\mathrm{V}$ and $V^p_{th} = (-2.8 \pm 0.3)\,\mathrm{V}$. The extracted S_{th} show a slightly higher variability especially for the n-mode, reaching slopes of $S^n_{th} = (480 \pm 58)\,\mathrm{mV/dec}$ and $S^n_{th} = (336 \pm 34)\,\mathrm{mV/dec}$. By improving the efficiency of the electrostatic gating by scaling down the EOT and adapting

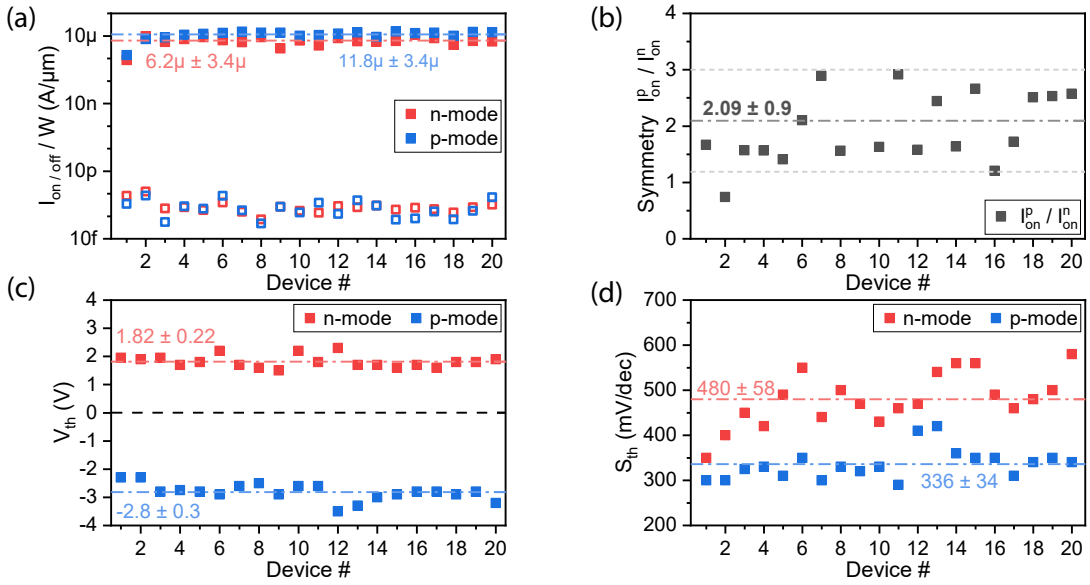

Figure 4.8: Extracted transistor parameters for 20 comparable Al-Si-based RFETs, measured at $V_D = 1\,\text{V}$, $V_S = 0\,\text{V}$ and $V_{PG} = \pm 7\,\text{V}$ for n- and p-mode. (a) On-currents (solid points) and off-currents I_D (empty square points), normalized to the sheet width W. (b) Current symmetry (I^p_{on}/I^n_{on}). (c) Threshold voltages (V_{th}). (d) Subthreshold slopes (S_{th}). The dash-dotted line marks the mean value of the extracted parameter.

the gating geometry, e.g., using a GAA-architecture, steeper slopes close to the thermal limit of 60 mV/dec at 300 K should be feasible [57, 69]. Finally, it should be noted that all analyzed devices show almost no hysteresis when recording the measurements. The extraction of the threshold voltages V_{th} for different V_{CG} sweeping directions resulted in hysteresis values of 71 mV and 110 mV for n- and p-mode, respectively.

Scaled Oxide Thickness for Reduced Operation Voltages

For the second generation of Al-Si-based RFETs, the gate thickness of the gate oxide was reduced to improve the electrostatic gating, leading to reduced operation voltages and steeper subthreshold characteristics. Therefore, the thermal oxidation time was reduced from 10 min to 5 min, resulting in a reduced SiO_2 gate oxide thickness of 10.3 nm, with a slightly thicker remaining Si channel thickness of 16.4 nm.

Figure 4.9(a) shows the schematic cross-section of the Al-Si-based RFET with reduced oxide thickness. The measured transfer characteristic in Figure 4.9(b) demonstrates that the new devices can be fully modulated using reduced gate voltages of ±4 V, while maintaining an almost hysteresis-free operation. Excellent symmetry is reached for the key transistor parameters, such as on- and off-state currents, threshold voltages and subthreshold slopes, especially for operation at higher bias conditions of $V_{DS} = 2\,\text{V}$. Note that, in contrast to previous investigations, the bias is now applied symmetrically, i.e., with $V_D = -V_S$ and $V_{DS} = V_D - V_S$. This now leads to a symmetric change of the injection barrier with the

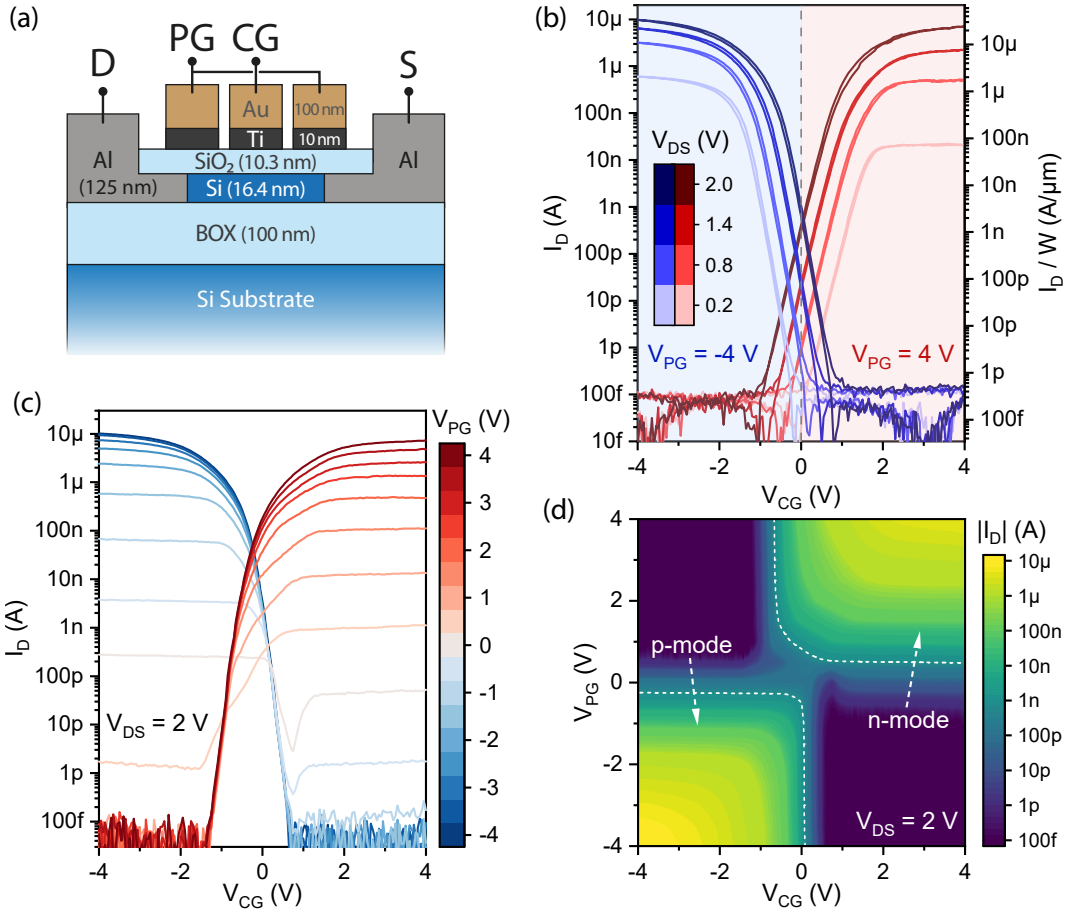

Figure 4.9: (a) Schematic cross-section of the Al-Si RFET with reduced SiO_2 gate oxide thickness of 10.3 nm. (b) Measured transfer characteristic showing n- (red) and p-type operation (blue) at $V_{PG} = \pm 4\,\mathrm{V}$ for V_{DS} between 0.2 V and 2 V, symmetrically applied with $V_D = -V_S$. (c) Subthreshold characteristic of the RFET for different PG voltages. By increasing V_{PG} from $-4\,\mathrm{V}$ to 4 V, the device switches from hole to electron conduction. (d) Semi-logarithmic conduction map showing the transition from p- to n-mode, indicated by the white dotted line at a current value of 1 nA. Device geometry: $L_{Si} = 3\,\mu\mathrm{m}$, $W = 290\,\mathrm{nm}$.

bias voltage V_{DS} for both operation modes. Figure 4.9(c,d) shows the transition of the RFET from p- to n-type operation with increasing V_{PG} for a constant bias condition of $V_{DS} = 2\,\mathrm{V}$. Stable switching behavior between the n- and p-mode is obtained, with two large and distinct on-state regimes (indicated in the conduction map for current values $I_D > 1\,\mathrm{nA}$) and well-suppressed off-states with currents below 100 fA. The color map representation thereby demonstrates the symmetric tunability of the energy barriers for both electrons and holes. Furthermore, these large operation regimes are essential for a reliable operation in circuit applications, making the RFETs resilient to input voltage variation. At $V_{PG} = 0\,\mathrm{V}$, the transfer curve favors weak p-type behavior, indicating that the Fermi level in the Al-Si junction pins slightly closer towards the VB, leading to slightly lower barriers for holes. Furthermore, for negative V_{PG} approaching $-4\,\mathrm{V}$, the transfer

curves are hardly affected by changes in V_{PG}, since the tunnel barrier for holes is already highly transparent and seems to no longer limit the carrier injection. For the n-mode, a larger influence of V_{PG} is visible, indicating that the injection barrier can still be further modulated.

For logic circuit applications, especially for symmetrical RFET circuits (see Section 2.5.3), it is advantageous to reduce the number of different voltage levels as much as possible in order to minimize the complexity of the circuit design. As the conduction map in Figure 4.9(d) has already indicated, it is possible to further reduce the voltages at the gates (V_{CG}, V_{PG}) while the switching of the polarities remains stable. Figure 4.10(a) shows the transfer characteristic of the same device as before, operated at reduced gate voltages of $\pm 2\,\mathrm{V}$, with the symmetrically applied bias voltage V_{DS} varied between $1\,\mathrm{V}$ and $4\,\mathrm{V}$. Note, that a bias voltage $V_{DS} = 4\,\mathrm{V}$ here refers to $V_D = -V_S = 2\,\mathrm{V}$, which means that only a single symmetrical voltage level of $\pm 2\,\mathrm{V}$ is sufficient at all RFET terminals to operate the device in both polarities. The transfer characteristic for $V_{PG} = \pm 4\,\mathrm{V}$ and $V_{DS} = \pm 2\,\mathrm{V}$ is indicated by dashed lines. At these lower operating voltages on the gates, especially on the PG, a stronger shift of V_{th} with increasing V_{DS} is obtained. At high bias voltages of $V_{DS} = 4\,\mathrm{V}$, the threshold voltage even shifts to low negative values for n-, and positive values for p-type operation, with $V_{th}^{n} = -0.2\,\mathrm{V}$ and $V_{th}^{p} = 0.33\,\mathrm{V}$, meaning the transistor is already weakly turned on at $V_{CG} = 0\,\mathrm{V}$. Nevertheless, operating the device at $V_{CG} = \pm 2\,\mathrm{V}$, the off-state currents can still be well suppressed. However, in p-mode, the channel cannot be completely depleted via the CG, resulting in increased

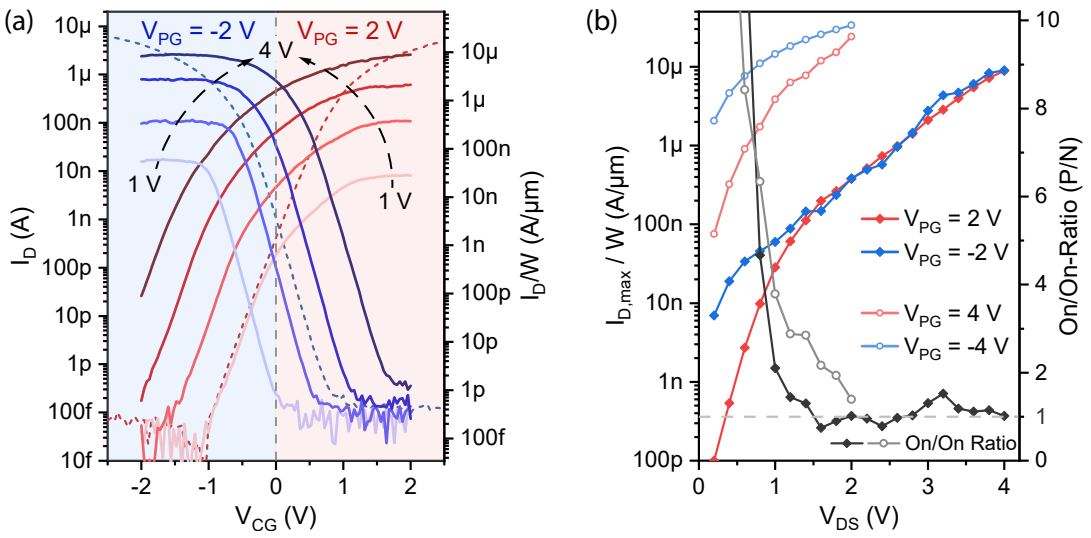

Figure 4.10: (a) Transfer characteristic of the RFET from Figure 4.9 at reduced gate voltages, using only $V_{PG} = \pm 2\,\mathrm{V}$ to switch between the operation modes. The symmetric bias voltage ($V_D = -V_S$) is increased from $V_{DS} = 1\,\mathrm{V}$ to $4\,\mathrm{V}$ in $1\,\mathrm{V}$ steps. The dashed lines indicate the transfer curves for $V_{PG} = \pm 4\,\mathrm{V}$, $V_{DS} = 2\,\mathrm{V}$. (b) On-currents $I_{on}^{p,n}$ (left axis) and on/on current ratio I_{on}^{p}/I_{on}^{n} (right axis) in relation to the bias voltage V_{DS} for gate voltages of $\pm 2\,\mathrm{V}$ (filled square points) and $\pm 4\,\mathrm{V}$ (empty dots).

off-state currents of about 20 pA and strongly reduced I_{on}/I_{off} ratios. In Figure 4.10(b), the on-state currents as well as the on/on ratio are plotted for the RFET operation at $V_{PG} = \pm 2\,\mathrm{V}$ and $\pm 4\,\mathrm{V}$, in relation to the bias voltage V_{DS}. Compared to the operation at $\pm 4\,\mathrm{V}$, the on-state currents are lower at $\pm 2\,\mathrm{V}$, as the injection barriers for both carrier types cannot be lowered that well, negatively influencing the tunneling probability and increasing on-state resistivities. However, at $V_{PG} = \pm 2\,\mathrm{V}$, the on-state currents for both p- and n-mode are almost identical for a large bias voltage range between 1.2 V to 4 V, with $I^p_{on}/I^n_{on} = 1.02$ at $V_{DS} = 4\,\mathrm{V}$. For $V_{PG} = \pm 4\,\mathrm{V}$, the optimal on-state symmetry of 1.39 is achieved at $V_{DS} = 2\,\mathrm{V}$, which is still a remarkably good value, as no strain engineering measures like in [77,78] have been applied. It should be noted that in the case of the 4 V-operation, it is not possible to increase the bias voltage V_{DS} up to 4 V, as this could result in a breakdown of the 10.3 nm thick SiO_2 gate oxide due to a high voltage difference at the Al-Si junction below the PG, with $V_D - V_{PG}$ of up to 8 V.

The temperature-dependent characterization in Figure 4.11 up to $T = 400\,\mathrm{K}$ at $V_{PG} = \pm 4\,\mathrm{V}$ shows that a stable and symmetrical operation of the devices is also possible at elevated temperatures. The on-currents for both operation modes slightly increase with the temperature, typical for Schottky junctions. With a slightly larger temperature dependency of the n-mode currents in and towards the on-state, which is attributed to a larger remaining effective Schottky barrier in the on-state, a slight asymmetry of the on-currents occurs, especially for temperatures $\geq$380 K (see Figure 4.11(b)). The p-type on-state seems to be dominated by the channel resistance, leading to a reversed behavior. For the off-currents, a stronger increase over temperature is evident due to the increase of thermally excited charge carriers, leading to a reduction of the on/off ratio of around one order of magnitude ($\sim 2 \times 10^7$) at 400 K (see Figure 4.11(c)). A shift of the threshold voltages V_{th} for

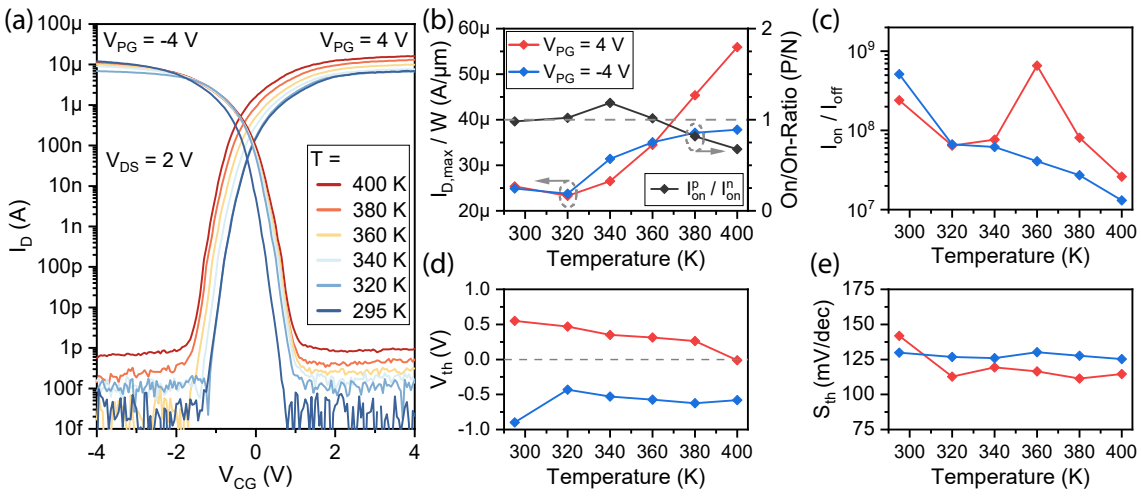

Figure 4.11: (a) Temperature-dependent transfer characteristic from $T = 295\,\mathrm{K}$ to 400 K at $V_{PG} = \pm 4\,\mathrm{V}$ and $V_{DS} = 2\,\mathrm{V}$ ($V_D = -V_S$) of the same RFET as in Figure 4.9. (b) On-currents and on/on current ratio I^p_{on}/I^n_{on}, (c) on/off current ratio, (d) threshold voltages V_{th}, and (e) subthreshold slopes S_{th} for n- (red) and p-type operation (blue) are evaluated over temperature.

both modes to lower absolute values is also clearly visible from the transfer curves and in Figure 4.11(d). In this TFE region, as the temperature rises, less voltage hub is required for higher-energy charge carriers to cross the barrier, allowing current to flow. This effect is again more pronounced for the n-type operation, with V_{th} approaching 0 V at 400 K. The subthreshold slopes in Figure 4.11(e) remain widely temperature independent and highly symmetric in the investigated range, with measured values of ∼115 mV/dec and ∼125 mV/dec for n- and p-mode, respectively.

Figure 4.12 shows the output characteristic of the Al-Si-based RFET for n- and p-type operation at room temperature (a,d) and 400 K (b,e). The devices were measured with symmetric bias conditions ($V_D = -V_S$). These color map representations illustrate the well-defined on- and off-states for both polarizations, demonstrating the stability of the device operation. The off-currents for both modes remain below 100 fA (in the range of the noise level of the measurement setup) for a wide V_{DS} and V_{CG} range due to the electrostatically high injection barrier from the PGs for the undesired charge carrier type. Furthermore, the measured data show high symmetry around the y-axis at $V_{DS} = 0$ V,

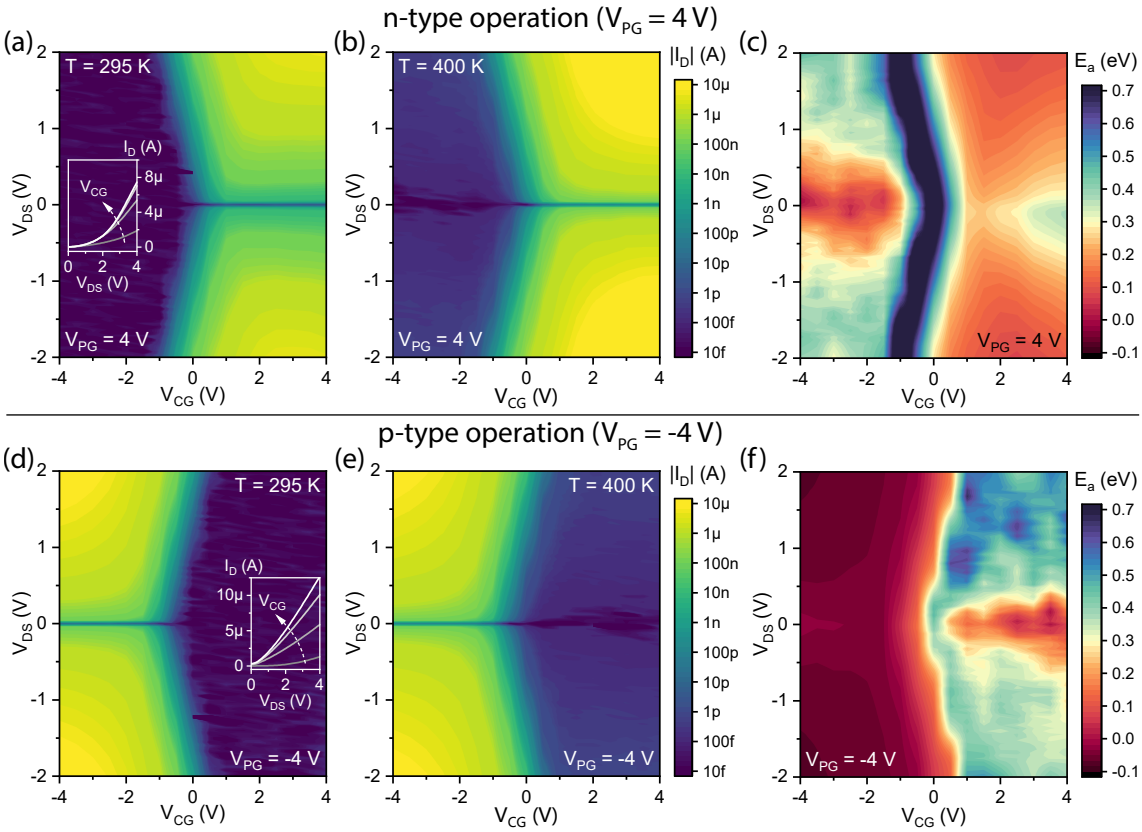

Figure 4.12: Semi-logarithmic output characteristic maps of the RFET from Figure 4.9 at room temperature (a,d) and 400 K (b,e) for n- and p-mode operation ($V_{PG} = \pm 4$ V, $V_D = -V_S$). The insets in the room temperature plots show the I/V characteristic in a linear scale, with V_{CG} increased from 1 V to 4 V (a) and −1 V to −4 V (d). (c,f) Extracted activation energy maps.

meaning that the I/V characteristic does not change when inverting the bias voltage. This ability provides an additional degree of freedom especially in adaptive circuits. A nonlinear increase of the drain current I_D with the bias voltage V_{DS} is obtained (see insets), similar to the output characteristic of the single top-gated SBFET in Figure 4.5. Note that within the given V_{DS} range, saturation could not be reached. The change of potential difference between V_{PG} and V_{DS} influences the tunneling probability, leading to an exponential increase of the current with increasing V_{DS}. Thus, V_{CG} can tune the contact resistivity ($\partial V_{DS}/\partial I_D$ for $V_{DS} \to 0$). For the p-mode at $V_{PG} = -4\,\mathrm{V}$, a linear I/V characteristic is obtained for $V_{CG} < 2\,\mathrm{V}$, as the activation energy E_a reaches negative values, indicating a transparent junction for holes with a quasi-ohmic behavior. At elevated temperatures of 400 K, the off-currents are clearly rising due to thermally excited charge carriers overcoming the blocking barrier. Furthermore, the smaller increase of the on-currents and also the V_{th} shift to lower V_{CG} voltage levels is well visible.

From the temperature-dependent output characteristics, V_{CG}/V_{DS}-dependent activation energy maps in Figure 4.12(c,f) can be derived (see Section 3.2.4), allowing a more detailed and resilient interpretation of the charge carrier transport mechanism in the RFET. The maps for both modes widely show positive values, indicating the contribution of the Schottky barriers. At the off-states of the RFETs ($V_{CG} < 0\,\mathrm{V}$ for n, $V_{CG} > 0\,\mathrm{V}$ for p), the activation energy reaches high values in the range of 0.3 eV to 0.7 eV, effectively blocking the majority charge carriers via the channel barrier using the CG. The injection of the undesired minority charge carriers into the semiconductor channel is already blocked via the PG, with $V_{PG} = 4\,\mathrm{V}$ and $-4\,\mathrm{V}$ for n- and p-mode, respectively. Note that the red/orange areas in the off-states are measurement artifacts, as the currents in this low-bias region are below the noise level of the measurement setup for all temperatures, making a correct estimation of E_a impossible. In the on-states (n: $V_{CG} > 0\,\mathrm{V}$, p: $V_{CG} < 0\,\mathrm{V}$), the barriers are electrostatically lowered via the gates, indicating an efficient injection of electrons (c) and holes (d) via FE or TFE. In the n-type operation, low positive E_a values of ∼0.1 eV to 0.2 eV are extracted. For the p-mode, the effective activation energy E_a even reaches small negative values for $V_{CG} < -1.5\,\mathrm{V}$, indicating transparent quasi-ohmic contacts for hole conduction, which results in linear I_D/V_{DS} characteristics. With higher V_{DS}, the low E_a region extends to lower $|V_{CG}|$ due to additional band bending of the bias voltage. The slight asymmetry observed in the extracted activation energy maps can be attributed to the Fermi level of the Al-Si junction being pinned slightly closer to the VB edge. This may also explain the overall slightly favored p-type conduction in all measured devices.

4.4 Multi Control-Gate Si RFETs

By adding additional CGs atop the semiconductor channel, wired-AND functionality within a single RFET can be realized. This multi-CG RFET structure (or MIGFET) can therefore replace several transistors (with the same polarization) in series. The equivalent circuit for a device with two CGs is schematically illustrated in Figure 4.13(a), with each of the virtually replaced single CG RFETs operating with only half the on-state re-

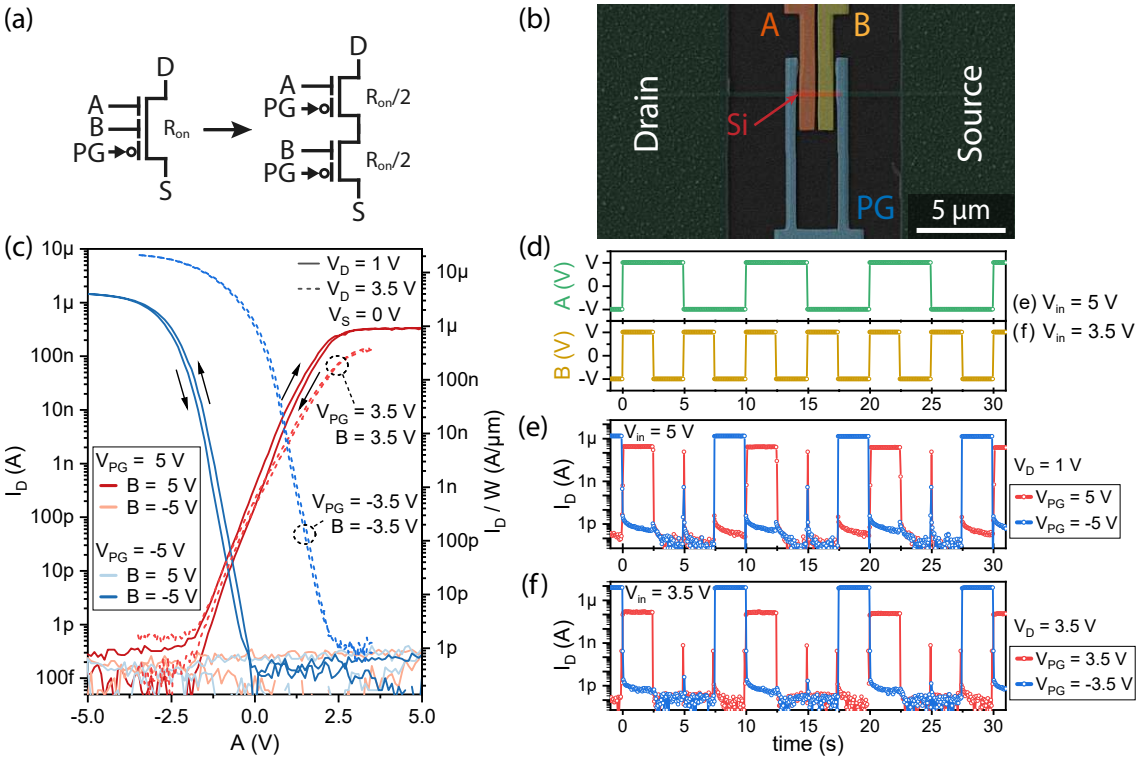

Figure 4.13: Si RFET with two CGs (4TG) for wired-AND functionality. (a) Equivalent circuit diagram of the multi-CG RFET, which replaces two single RFETs in series, each with a virtual channel resistance of $R_{on}/2$. (b) False-color SEM image of a 4TG RFET. (c) Transfer characteristic of the wired-AND RFET, with the input A swept in both directions, while the input B and the polarity with PG are fixed. The solid lines show the device operation at gate voltages V_G of $\pm 5\,\mathrm{V}$ and a drain bias V_D of 1 V, the dashed lines at $V_D = |V_G| = 3.5\,\mathrm{V}$. (d-f) Transient operation of the wired-AND gate, with the input signal sequence (d) and the resulting drain current I_D for input voltage levels of 5 V (e) and 3.5 V (f) for n- and p-type operation. $W = 360\,\mathrm{nm}$, $L_{Si} = 2.26\,\mu\mathrm{m}$.

sistance (R_{on}). As the internal resistance of the RFETs is dominated by the resistance at the charge injection barrier and not by the channel length or amount of individual top gates, the overall on-state resistance can be reduced by replacing several transistors with a single MIGFET structure. This holds true as long as the channel length is sufficiently short. For Si NW SBFETs with $NiSi_2$ contacts, the critical length was found to be $\sim$1 µm [212]. This can be exploited in combinational circuits, effectively reducing transistor count and critical path delays [17]. Figure 4.13(b) shows a false-color SEM image of an RFET with four top gates (4TG), including two individually controllable CGs (for the inputs A,B) in between the two physically connected PGs atop the Al-Si junction.

The function of this wired-AND gate with two inputs (A, B) is shown in the transfer characteristic in Figure 4.13(c). The current flow I_D is plotted depending on the voltage at the input A, while the potential on the other terminals, the input B, V_{PG} and V_{DS} are kept constant. Note that the measured device again has a thicker SiO_2 gate oxide

of 12.5 nm, requiring higher operation voltages. The Si channel of this device is 2.26 µm long and 360 nm in width. The solid lines show the operation at ±5 V on the gates, with an asymmetric bias of $V_{DS} = V_D = 1\,\text{V}$. When the device is set to n-type conduction, with $V_{PG} = 5\,\text{V}$, an electron-induced current of $I^n_{D,max} = 0.34\,\mu\text{A}$ (0.93 µA/µm) is flowing when both inputs are set to 5 V. The subthreshold characteristic, with B fixed at 5 V and A modulated between −5 V and 5 V, is almost identical to that of the previously shown RFETs with a single CG. At B = −5 V, the transistor remains in the off-state with currents of ∼100 fA due to the additional induced channel barrier from B, blocking the electron flow. By setting the PG to −5 V, the wired-AND gate operates in the p-mode, with a hole-induced current flowing when both inputs are set to −5 V. With B set to 5 V, the transistor remains off regardless of the voltage level at the input A. With an on-state current of $I^p_{D,max} = 1.46\,\mu\text{A}$ (4 µA/µm), the device exhibits a slightly favored p-type characteristic, with an I^p_{on}/I^n_{on} symmetry factor of 4.3. Also the subthreshold slope with $S^p_{th} = 280\,\text{mV/dec}$ is clearly steeper for the p-mode than for the n-mode with $S^n_{th} = 514\,\text{mV/dec}$, as previously seen in TTG devices.

As before, the operating voltages for the device can be adjusted to allow the same symmetric voltage level to be applied to both the gates and the drain. The dashed lines in Figure 4.13(c) show the characteristic of the same device operated at ±3.5 V on the gates and 3.5 V on the drain voltage. While a stable operation for both modes is still achieved, the characteristic thereby becomes even more asymmetric, with increased p-type and reduced n-type current ($I^p_{on}/I^n_{on} = 56$). The symmetry can presumably be improved by changing the source potential to $V_S = -V_D$ (instead of $V_S = 0\,\text{V}$), as this has already led to a more symmetrical operation in the TTG RFETs (see Figure 4.10).

The transient operation of the wired-AND gate is shown in Figure 4.13(d-f), with the input sequence on the two CGs A and B in (d) determining the output current I_D, depending on the defined polarization state at the PG. For both operation voltage configurations, with ±5 V on the gates in (e) and ±3.5 V in (f), the high-current state for I_D is reached when both inputs are set either to the positive (logical high) voltage level for the n-mode, or the negative (logical low) voltage level when the transistor is operating in the n-mode. For all other states, the current flow is well suppressed, obtaining an on/off current ratio of $>1 \times 10^6$ and $>5 \times 10^5$ for the ±5 V and ±3.5 V settings, respectively.

In Figure 4.14, one more CG is added to implement a 3-input wired-AND structure. For the fabrication of these 5TG structures, devices with a longer channel length were selected to accommodate the three CGs between the two connected PGs on the Al-Si junction. While the increase in the internal resistance R_{on} due to the longer semiconductor channel is only marginal, the virtual channel resistance of each replaced single-CG RFET is reduced ideally to $R_{on}/3$, leading to even larger improvements compared to classical implementations. The AFM scan in Figure 4.14(b) shows an RFET with three independent CGs on top of a 3.13 µm long and 290 nm wide Si channel. The device operation is demonstrated in the transfer characteristic in Figure 4.14(c), with the current I_D as a

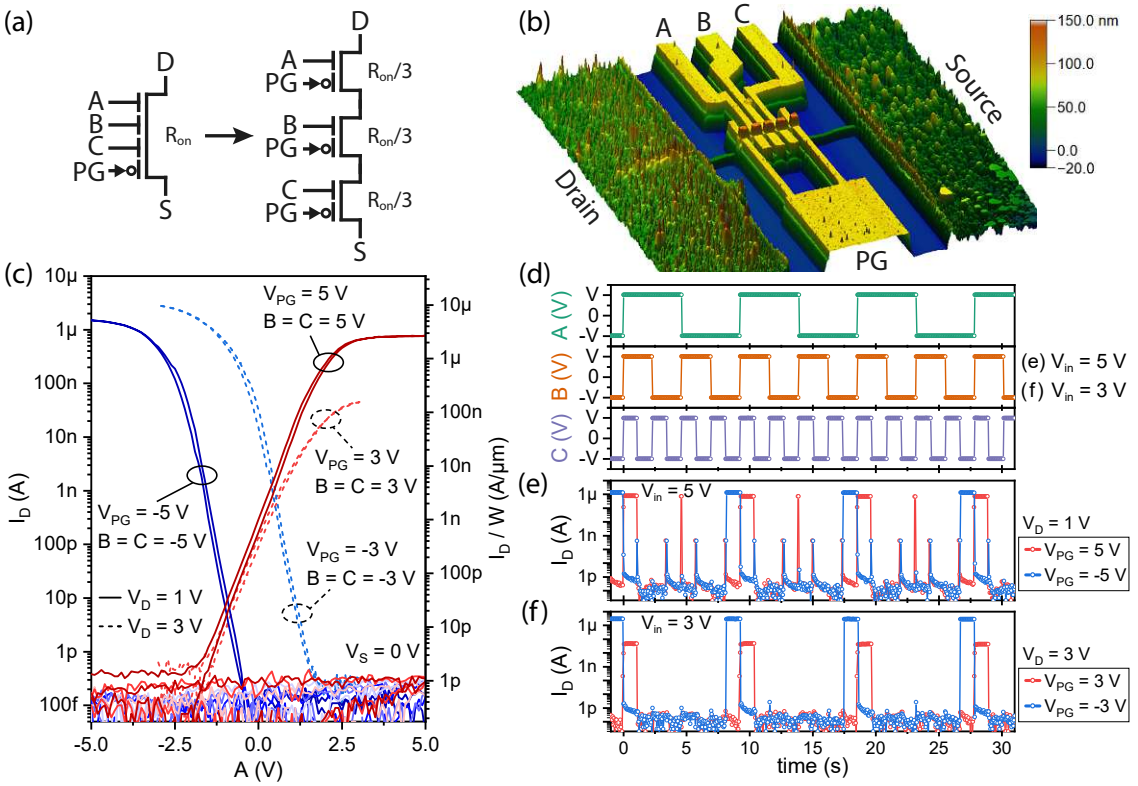

Figure 4.14: Si RFET with three CGs (5TG) for wired-AND functionality. (a) Equivalent circuit diagram of the multi-CG RFET, which replaces three single RFETs in series, each with a virtual channel resistance $R_{on}/3$. (b) AFM scan of a 5TG RFET. (c) Transfer characteristic of the three-input wired-AND RFET, with the channel A swept in both directions, while the inputs B, C and PG are fixed. The solid lines show the device operation at $V_G = \pm 5\,\mathrm{V}$ and V_D=1 V, the dashed lines at $V_D = |V_G| = 3\,\mathrm{V}$. (d-f) Transient operation of the wired-AND gate, with the input signal sequence (d) and the resulting drain current I_D for input voltage levels of 5 V (e) and 3 V (f) for n- and p-type operation. $W = 290\,\mathrm{nm}$, $L_{Si} = 3.13\,\mu\mathrm{m}$.

function of the input A, while all other terminals are kept at constant values. At the $\pm 5\,\mathrm{V}$ operation level, with $V_{DS} = V_D = 1\,\mathrm{V}$ (solid lines), a relatively symmetric characteristic is obtained, with on-state currents of $I^n_{D,max} = 0.77\,\mu\mathrm{A}$ and $I^p_{D,max} = 1.52\,\mu\mathrm{A}$ being reached when all gates (A, B, C, PG) are set to 5 V or -5 V for n- or p-type operation, respectively. The small hysteresis when changing the sweeping direction and the subthreshold slopes of $S^n_{th} = 550\,\mathrm{mV/dec}$ and $S^p_{th} = 277\,\mathrm{mV/dec}$ are comparable with previously measured RFETs with only one or two CGs (and the same gate oxide thickness). Therefore, no significant influence of the increased ungated region on the semiconductor channel due to the increased number of gaps between the individual gates was observed, which is consistent with the simulation results in [17, 211]. For all the other states, with one or more gate voltages set to the opposite polarity, the transistor remains in the off-state, with $I_D \sim 100\,\mathrm{fA}$.

When adapting the operation voltages again to a single symmetric voltage domain, with $V_D = |V_G| = 3\,\mathrm{V}$ (dashed lines in 4.14(c)), the device characteristic becomes strongly p-dominant, mainly due to the strongly decreasing n-mode current, increasing its asymmetry from $I^p_{on}/I^n_{on} = 1.97$ to 61.7. Apparently, the 3 V at the gates are not enough to fully lower the injection barrier for electrons, leaving a higher on-state resistance.

The transient behavior in Figure 4.14(d-f) further demonstrates the wired-AND functionality for three inputs (A, B, C). A current flow I_D is enabled when all inputs are set to the same potential as the PG. For all other states, the current flow is well suppressed, with off-state currents below 1 pA. As it was already expected from the transfer characteristic, higher currents are delivered in the p-mode, with a less symmetric operation at the symmetric 3 V settings in (f). Nevertheless, high on/off current ratios of $>1.5 \times 10^6$ for the 5 V (e) and $>2 \times 10^5$ for the 3 V operation (f) are reached.

4.5 RFET-based Complementary and Combinational Logic

The previously demonstrated RFETs based on Al-Si-Al heterostructures showed highly symmetric n- and p-type characteristics at a relatively low device-to-device variability, promising for their first integration into combinational logic gates. Furthermore, due to the good manufacturing yield, including the reliable Al-Si heterostructure formation process, the individual RFETs can be combined and interconnected directly during manufacturing on-chip, rather than by bonding selected devices.

4.5.1 Complementary Inverter

The simplest commonly used logic gate is the complementary inverter. In standard CMOS technology, this gate is based on two physically different transistors, a p- and n-channel MOSFET, connected in series, with the input signal applied to both gates defining the output level between the two transistors. The same circuit can also be implemented using two physically identical RFETs, electrostatically setting both transistors into opposite polarizations using the PG. Thereby, differently doped channels or doping wells are not required, reducing constraints in the layout design. Figure 4.15(a) shows the colored SEM image of a fabricated complementary inverter based on two RFETs. Exploiting the Al-Si exchange reaction, the inverter can be fabricated from a single long Si nanosheet (or nanowire [LW12]). With an Al contact pad for the inverter output (V_{OUT}) atop the middle of the Si nanosheet, two Al-Si-Al heterostructures can be formed toward the source/drain pads, which are then contacted by the top gates. During operation, the RFET on the V_{DD} side is set to the p-mode by applying a negative V_{PG}, acting as a pull-up transistor, while the V_{SS}-side RFET is used as a pull-down transistor in n-mode with positive V_{PG} (see Figure 4.15(b)). The input voltage V_{IN} is applied to the connected CGs of both RFETs, and the inverted output signal V_{OUT} is read at the common node connecting both RFET drain regions. As each RFET maintains its functionality at reversed bias condition, the whole circuit can be operated with inverted voltages without changing its characteristic, which would not be possible with conventional CMOS transistors.

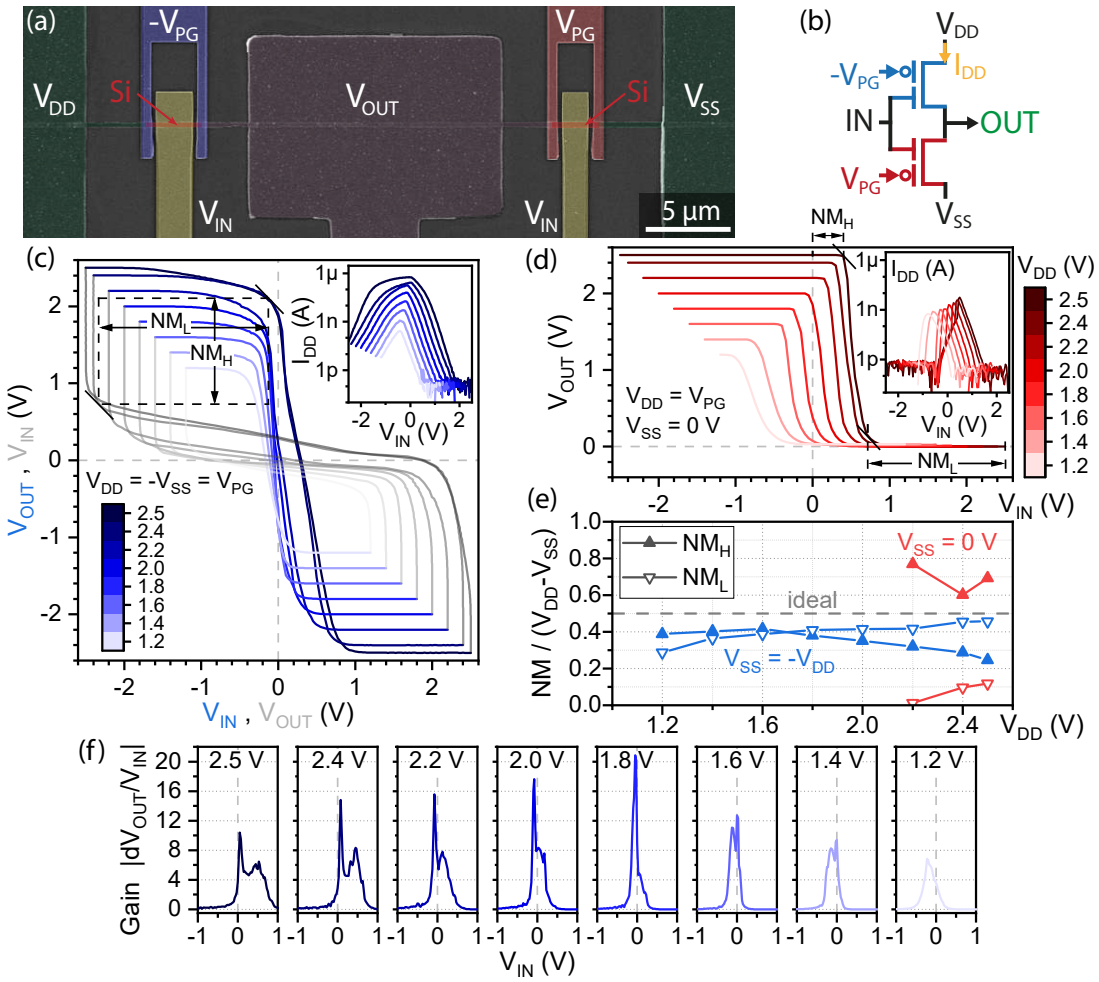

Figure 4.15: (a) Colored SEM image of the complementary inverter based on two Al-Si-Al heterostructure RFETs. (b) Schematic of the inverter, with the n- and p-type transistor set via the PGs. (c) Output transfer characteristic at different voltages in the range of 2.5 V to 1.2 V, with $V_{DD} = -V_{SS} = V_{PG}$. V_{IN} and V_{OUT} are plotted interchangeably to evaluate the noise margins NM_H and NM_L. The cross-current flow I_{DD} for the different operation voltages is shown in the inset. (d) Inverter operation at asymmetric bias, with $V_{SS} = 0$ V, resulting in output levels between V_{DD} and 0 V. (e) Extracted noise margins NM_H, NM_L normalized to the supply voltage $V_{DD} - V_{SS}$. The dashed line at 0.5 V marks the ideal noise margins for both parameters. (f) Inverter voltage gain (dV_{OUT}/dV_{IN}) for different symmetric bias voltage levels, extracted from (c).

Figure 4.15(c) shows the voltage transfer characteristic of the complementary inverter for different operation voltages. Fully symmetric supply voltages are thereby applied on all terminals, with $V_{DD} = -V_{SS} = V_{PG}$, with the V_{IN} and V_{OUT} varied between the positive and negative voltage level. With only two voltage levels (positive for logic "high" or "1", negative for logic "low" or "0") used in the circuit, there is no need to generate additional supply rail voltages, simplifying the circuit layout. Remarkably, a full-swing inverter characteristic is obtained for a wide range of operation voltages between ±2.5 V

down to ±1.2 V. Hence, the transitions between the two logical states are very steep and well centered around $V_{IN} = 0\,\text{V}$. This can be seen in Figure 4.15(f), showing high voltage gains (dV_{OUT}/dV_{IN}) of up to 20.8 for the $V_{DD} = 1.8\,\text{V}$ operation. The cross-circuit flow I_{DD} during the switching operation is shown in the inset. The current thereby scales with the used supply voltages. At the transition between steady states, short circuit current peaks up to 580 nA for the 2.5 V and 240 pA for the 1.2 V operation are reached. At the steady states, due to the complementary design, the currents are well suppressed, limiting the current flow below 62 pA and 6.2 pA. The higher steady state currents for V_{IN} at logic "low" (V_{OUT} = "high") can be explained by the fact that the RFET in n-type configuration is turned off in this state, but its off-currents are significantly higher than those of the p-mode transistor. These asymmetric off-currents are also seen in the 2 V transfer characteristics of the single RFET in Figure 4.10. To illustrate and evaluate the noise margins, the output curves are also plotted with interchanged axes. The extracted noise margins for both the logical high (NM_H) and logical low (NM_L) states, normalized to the supply voltage, are plotted in Figure 4.15(e). High and symmetrical noise margins are achieved, especially for operation voltages between ±1.4 V and ±2 V, with values from 0.35 to 0.42, allowing a very reliable and robust operation. Noise margin values of 0.5 would be ideal, i.e., a perfectly rectangular inverting behavior, with the switching point at 0 V (or in the middle of the two states).

By setting $V_{SS} = 0\,\text{V}$, the operation region is shifted, with an output voltage range of $0\,\text{V} \leq V_{OUT} \leq V_{DD}$ for the inverted input. Note that the negative voltage level $-V_{DD}$ is still required for the PG to set the pull-up RFET to the p-mode. This asymmetric operation is shown in Figure 4.15(d) for voltage levels from ±2.5 V to ±1.2 V. For input voltages between $\pm V_{DD}$, a full output swing between 0 V and V_{DD} is reached. However, if V_{IN} is only varied from 0 V to V_{DD}, which would be a more practical use case, both logic states are only reached up to operating voltages >2.2 V. Therefore, the extracted noise margins in Figure 4.15(e) are only measured for positive voltages on V_{IN}. Although the state transitions are still quite steep, i.e., having a large voltage gain, they are clearly shifted towards V_{IN} levels close to 0 V, resulting in asymmetric noise margins with high NM_L and low NM_H. This implies that the logic high level for the output is rather unstable. The cross-circuit currents again show the benefits of the complementary design, with short peaks at the state transitions and well-suppressed steady state currents. However, due to the shifted transitions, for $V_{DD} < 2.2\,\text{V}$, the currents at $V_{IN} = 0\,\text{V}$ are not well suppressed, as the high logic level cannot be reached, with at least one RFET not fully switching.

To further demonstrate the stable operation of the RFET-based complementary inverter, transient measurements were conducted. Figure 4.16 shows the operation of this circuit for ±2 V on all terminals, with a rectangular (a) and triangular (b) input signal V_{IN} generated from a function generator, and the inverted signal on the output V_{OUT}. For both signal forms, a full-swing operation is obtained. In general, the rail-to-rail cross-current flow is retained, with well-suppressed steady state currents (I_{DD} <20 pA) and only short current peaks of ∼100 pA measured when switching between the two states for the rectangular input signal in Figure 4.16(a). Note that the current peaks could be higher, as they are very

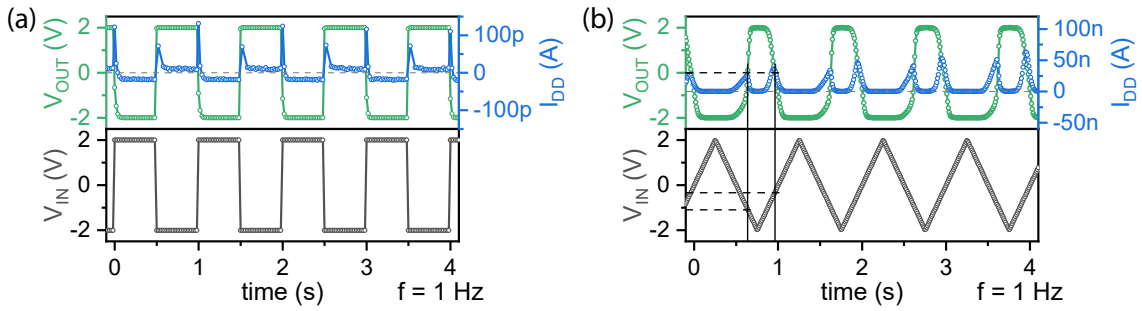

Figure 4.16: Transient measurements of the RFET-based complementary inverter in symmetric operation ($V_{DD} = -V_{SS} = V_{PG}$), with the output voltage V_{OUT} depending on (a) a rectangular and (b) a triangular input signal V_{IN}. The cross-current flow I_{DD} is shown in blue.

short and probably not accurately measured due to the rather poor time resolution of the semiconductor analyzer. This could partly explain why the values in the transient measurements are much lower than for the static measurements in Figure 4.15(a). The current flow for the triangular input signal in Figure 4.16(b) is generally higher, as this input results in a more continuous switching behavior. Furthermore, the logic "high" states in the rectified output signal are shorter than for the logic "low", indicating slight asymmetries in the switching behavior towards negative V_{IN}. The low operation frequency of 1 Hz was used due to limitations of the measurement setup and furthermore the lab-based contact technology. This features large and planar contact pads for contacting the probes on the same layer as the devices, resulting in large parasitic capacities and related high capacitive charging and discharging time constants. Nevertheless, mixed-mode TCAD simulations have already demonstrated feasible operation speeds of RFET-based logic circuits with proper back-end-of-line interconnect technology in the GHz regime [209].

4.5.2 Reconfigurable NAND/NOR Gate (Minority Gate)

In conventional CMOS technology, NAND and NOR gates basically share the same circuit topology, except that their polarity, including supply voltage polarity and transistor type (n-FET and p-FET), is inverted. Since RFETs provide unipolar operation with runtime switchable polarity, replacing classic transistors with RFETs provides the opportunity to combine both circuits. The thereby realized logic cell is then switchable between NAND and NOR operation by flipping the voltages on the supply rail (V_{DD}, V_{SS}) and the PGs on the RFETs.

Figure 4.17(a) shows the optical microscope image of this reconfigurable NAND/NOR gate, realized with only three RFETs. The bottom RFET is designed with two CGs, realizing a wired-AND gate to replace two transistors in series, further reducing the transistor count compared to conventional implementations (see Figure 4.17(b)). The contact C and its inverted signal $\overline{C} = -C$ are thereby connected to the supply voltages V_{DD} and V_{SS} and the PGs of the RFETs, defining the polarity of the circuit. The inputs A and B are applied on the CGs. With $C = -2\,\mathrm{V}$ (or logic "0"), the two parallel RFETs are set to p-mode and the 4TG RFET to n-mode, realizing the NAND functionality. For the NOR

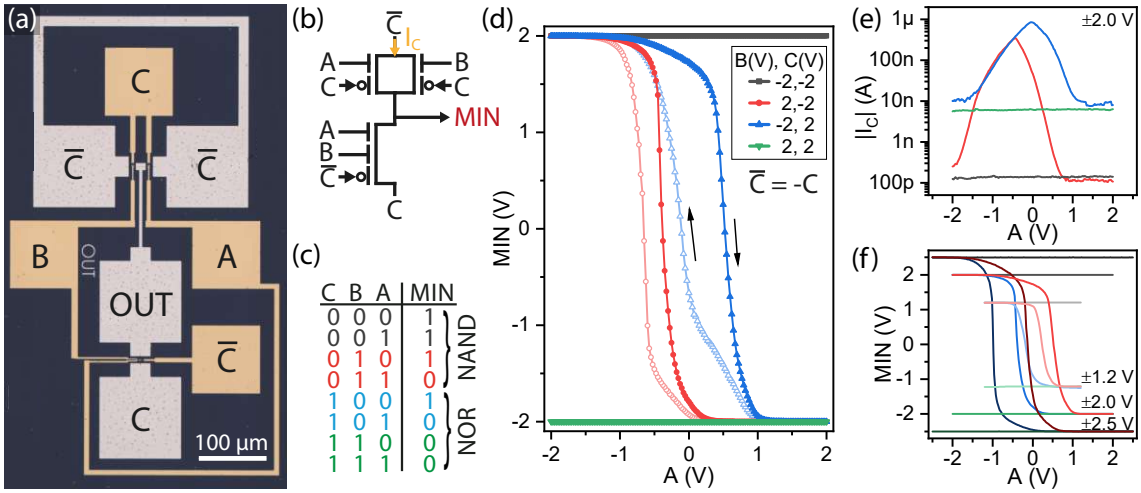

Figure 4.17: (a) Microscope image and (b) schematic of a reconfigurable NAND/NOR gate based on three RFETs. The polarity of the logic cell can be inverted with the input C, switching between NAND ($C = -2\,\mathrm{V}$) and NOR operation ($C = 2\,\mathrm{V}$), resembling a three-input minority gate (MIN). (c) Logic table of the MIN gate, where a logic "0" corresponds to a voltage level of $-2\,\mathrm{V}$ and a logic "1" corresponds to $2\,\mathrm{V}$. (d) Output transfer characteristic, where A is varied between $\pm 2\,\mathrm{V}$ in both directions, and the inputs B, C are fixed. (e) Rail-to-rail current flow I_C, with A increased from $-2\,\mathrm{V}$ to $2\,\mathrm{V}$. (f) MIN gate operation at different supply voltages of $\pm 2.5\,\mathrm{V}$, $\pm 2\,\mathrm{V}$ and $\pm 1.2\,\mathrm{V}$.

operation, C is set to $2\,\mathrm{V}$ (or logic "1"), with the parallel RFETs operating in n-type, and the 4TG RFET in p-type configuration. As this polarity switching is possible during runtime, C (and $\overline{C}$) can be used as logic input, realizing a three-input minority (MIN) in a transmission gate architecture. The logic table for the MIN gate is shown in Figure 4.17(c). This further demonstrates the advantages of this realized RFET-based logic gate over conventional implementations by using fewer transistors while significantly increasing functionality.

The voltage transfer characteristic in Figure 4.17(d) demonstrates the switching behavior of the realized MIN gate, with the output voltage depending on the varied input signal A. The inputs B and C are set to constant values of $\pm 2\,\mathrm{V}$ to switch between every logic state. Thereby, a full-swing operation with sharp state transitions is achieved for all output states while only showing a small hysteresis when changing the sweeping direction. The rail-to-rail current flow I_C in Figure 4.17(e) shows current peaks of up to 800 nA when the output level is switched between $2\,\mathrm{V}$ and $-2\,\mathrm{V}$. For the steady states, the complementary circuit design limits the current flow to values below 10 nA. If the output state remains at a constant level with a changing input A, i.e., at $B = C = -2\,\mathrm{V}$ and $B = C = 2\,\mathrm{V}$, the current also remains constant, with $I_C \approx 140\,\mathrm{pA}$ and $I_C \approx 6\,\mathrm{nA}$, respectively. The variation of the steady state currents depending on the output state can again be explained by the asymmetric off-state currents of the RFETs at the $\pm 2\,\mathrm{V}$ operation. Remarkably, a stable operation of this logic cell is possible for a wide range of operation levels, with voltages ranging from $\pm 2.5\,\mathrm{V}$ down to $\pm 1.2\,\mathrm{V}$ applied to all terminals, as shown in Figure 4.17(f).

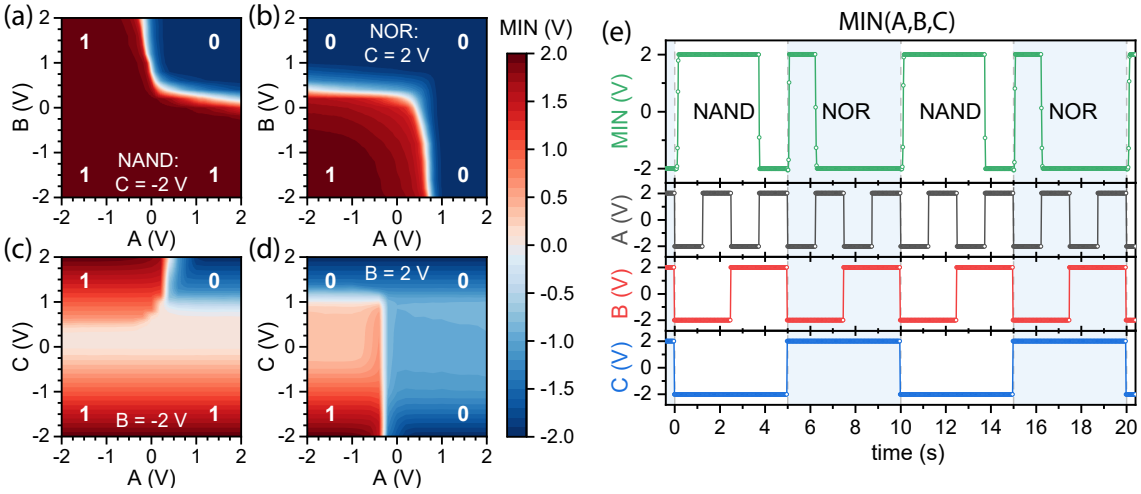

Figure 4.18: Output color maps of the MIN gate, showing the output voltage level depending on the inputs A and B, with C fixed at $\pm 2\,\mathrm{V}$ (a,b), and as a function of A and C, with B fixed at $\pm 2\,\mathrm{V}$ (c,d). (e) Transient measurement of the MIN gate.

To further demonstrate the stability of this RFET-based logic gate, 2D output maps are measured by varying two input voltages and measuring the resulting voltage at the output. The color maps in Figure 4.18(a,b), show the operation for constant values at the "select" input C, i.e., without changing the polarity of the circuit, representing the operation as dedicated NAND ($C = -2\,\mathrm{V}$) or NOR gates ($C = 2\,\mathrm{V}$). Thereby, large operation windows with constant output levels and steep transitions are obtained, which allows a robust operation of the circuit even at high input voltage fluctuations and noise levels. The output levels when varying C (and A) at fixed input levels $B = \pm 2\,\mathrm{V}$ in Figure 4.18(c,d) are not as stable as for constant C. Since C not only controls the voltage of the PGs, but also the supply voltage of the entire circuit, the output voltage is directly affected by changes of C. This means that the state transitions when varying C are gradual rather than abrupt.

In the time-dependent measurement in Figure 4.18(e), the logic operation of the reconfigurable logic cell is demonstrated, where the device reliably switches between NAND and NOR operation, thus realizing a MIN function. Full-swing operation is achieved for all output states for a sequence of input signals at A, B, and C at $\pm 2\,\mathrm{V}$.

4.5.3 Reconfigurable XOR/XNOR Gate (XOR3 Gate)

When implementing XOR circuits, the use of RFETs offers even greater potential for performance improvements over classic transistors than the previously shown logic gates. Exploiting the reconfigurable nature of the RFETs, an XOR gate can be realized using only 4 RFETs, as can be seen in the microscope image of Figure 4.19(a) and its corresponding schematic in (b). In conventional CMOS, this logic gate is rather complex to implement, as it already requires eight transistors (n-FET and p-FET) for only two inputs, twice

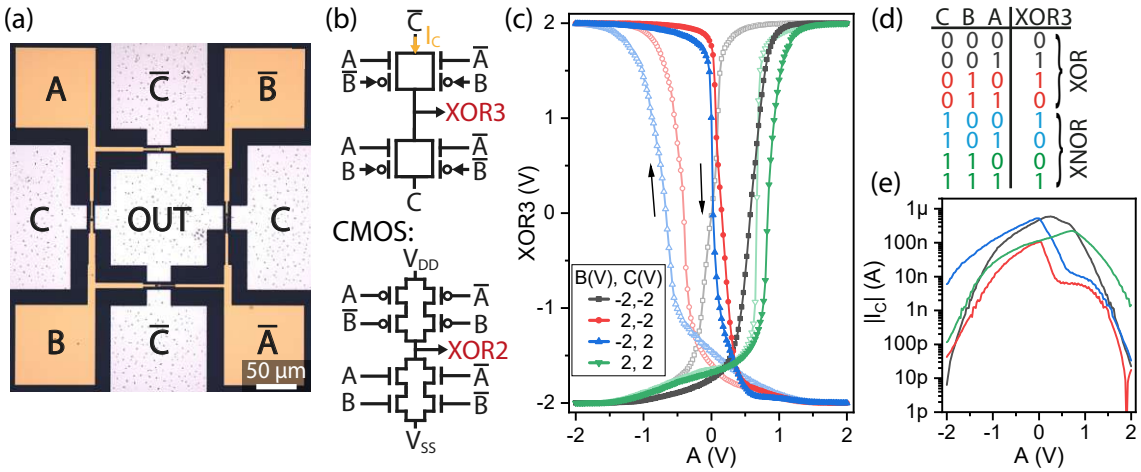

Figure 4.19: (a) Microscope image and (b) schematic of a reconfigurable XOR/XNOR gate based on four RFETs. A classical CMOS implementation of an XOR or XNOR gate requires eight transistors (NMOS and PMOS). The polarity of the circuit is inverted using C, switching between XOR ($C = -2\,\mathrm{V}$) or XNOR ($C = 2\,\mathrm{V}$) operation. Using C as input, the logic gate operates as a 3-input XOR (XOR3) transmission gate. (c) Transfer characteristic, with the output $XOR3$ depending on the input A (varied in both directions), B and C (fixed). (d) Logic table of the XOR3 gate. (e) Rail-to-rail current flow I_C, with A increased from $-2\,\mathrm{V}$ to $2\,\mathrm{V}$.

the transistor count as for RFETs. As the number of inputs n increases, the XOR gate becomes drastically more complex, with the intrinsic delay increasing with $g = n2^{n-1}$ [267]. This makes RFET implementations even more advantageous, with vastly decreased transistor count and circuit delays [17].

In this RFET-based XOR implementation, the input signal A and its inverted counterpart $\overline{A} = -A$ are thereby applied to the CGs of the four RFETs, while B and $\overline{B}$ are applied to the PGs. The inputs C and $\overline{C}$ act as the select signal. With $\overline{C} = V_{DD} = 2\,\mathrm{V}$ and $C = V_{SS} = -2\,\mathrm{V}$, the circuit operates as an XOR gate, equivalent to the depicted CMOS implementation. However, since the TTG RFETs offer bias-independent operability, the supply voltage can again be inverted via C, which transforms the circuit into an XNOR gate. Consequently, using C as logical input, the circuit is then transformed from a static to a pass-transistor design, performing the function of an XOR3 gate in a transmission gate architecture, still using only four RFETs. The corresponding truth table for the XOR3 gate is shown in Figure 4.19(d). Note that additional inverters for providing the inverted signals $(\overline{A}, \overline{B}, \overline{C})$ would still be required, increasing the actual transistor count for both for the RFET and the CMOS implementation. Nevertheless, such differential designs are often used in CMOS.

The voltage transfer characteristic of the RFET-based XOR3 gate in Figure 4.19(c) shows that for the operation at $\pm 2\,\mathrm{V}$ on all terminals, a full output swing with steep state transitions is achieved. A distinct hysteresis is evident, implying that the switching between two states is shifted to different voltages at A, depending on the switching direction. The

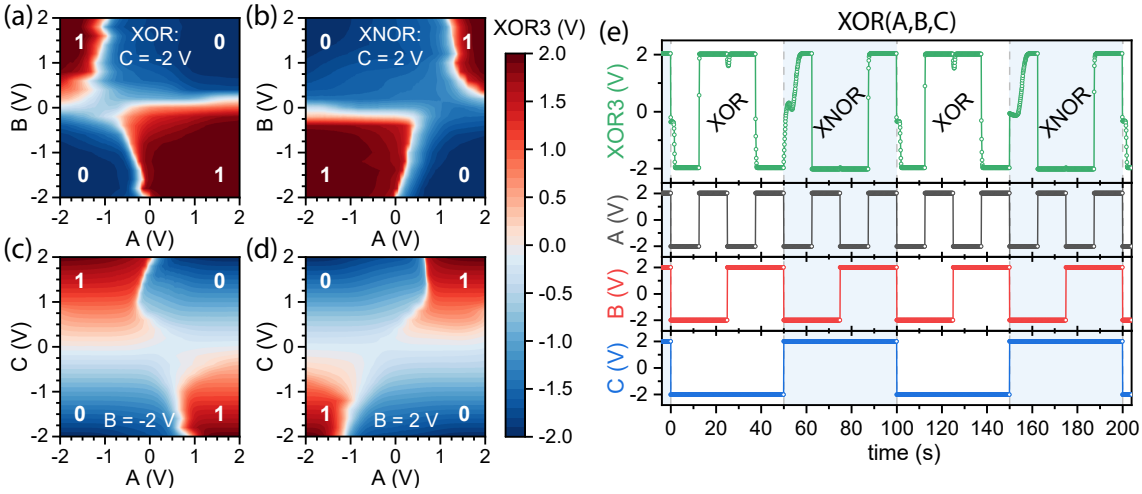

Figure 4.20: Output color maps of the three-input XOR gate, showing the output $XOR3$ depending on the inputs A, B (a,b), and A, C (c,d), with the other input fixed at $\pm 2\,\mathrm{V}$. (e) Time-dependent measurement of the XOR3 gate.

complementary circuit design, with either both upper or both lower RFETs turned off, again leads to suppressed currents I_C at the defined output states, which is shown in Figure 4.19(e). With steady state currents ranging from 6 nA to 6 pA and short-circuit currents up to 585 nA at the state transitions, similar values as for the MIN gate with three RFETs are obtained.

The output color maps in Figure 4.20 further demonstrate a stable operation of this XOR3 circuit. Although the operating windows in (a) for the state $(A, B, C) = (0, 1, 0)$ and in (b) for $(A, B, C) = (1, 1, 1)$ are rather small, a constant output level of 2 V for logic "1" can still be maintained for input voltage variations of at least 0.6 V before the output is flipped. The state transitions in Figure 4.20(c,d) when varying the input C are more blurred than the sharp transitions when switching A or B. Since the maximum output level is determined by the supply voltages in the circuit, which are set by the voltages at the inputs C and $\overline{C}$, even small changes in C directly affect the output voltage. Nevertheless, these changes to the output level are gradual and should not lead to an unwanted transition to another output state.

The transient response of the XOR3 circuit based on four physically identical RFETs in Figure 4.20(e) shows that a full swing operation is achieved for all eight output states. Slow state transitions with some logic degradation can be detected, especially when the polarity of the circuit is inverted with C, switching the gate between XOR and XNOR functionality. This can be explained by capacitive coupling and charge RC delays from the large planar contact pads on top of the SOI for contacting the probes, which severely limit the operating speed. This problem can be addressed by using a back-end-of-line interconnect technology that should allow the circuit to be operated in the GHz range [69]. According to TCAD simulations by Cadareanu et al. [19], the RFET-based XOR3

gate reaches approximately the same energy-delay product (EDP) as conventional CMOS implementations, where the increased capacitance per device from the additional TGs is compensated by the reduction in transistor count within the logic gate. Therefore, in circuits where the use of RFET can further reduce the transistor count, higher performance gains are expected.

4.5.4 Majority Gate

By slightly modifying the circuit of the XOR3 gate, i.e., changing the signals applied to the supply rails on the Al pads from $\overline{C}$ and C to C and A, a 3-input MAJ gate can be realized. The schematic and its corresponding truth table of this MAJ gate, also realized by interconnecting four physically identical TTG RFETs, are shown in Figure 4.21(a,b). Like the XOR function, the MAJ logic function is widely used in arithmetic circuits. Therefore, a more efficient implementation using RFETs with fewer physical resources can improve the performance of logic applications [79]. Again, an RFET-based MAJ gate can significantly reduce the transistor count, with the static CMOS implementation with 10 transistors employing 2.5x more devices [267].

Figure 4.21(c) shows the voltage transfer characteristic of the fabricated MAJ gate using $\pm 2\,\mathrm{V}$ on all input terminals. Thereby, some linear changes in the output voltage during the modulation of A can be seen for all state transitions. This is attributed to the circuit design, where the supply rail voltage is defined by the voltage difference between the two inputs A and C. With the output pulled down (or up) to one of the supply voltage nodes A or C, a change in that node results in a linear change in the output voltage. This is also the reason why for logic input level changes that would result in the same output state, e.g., from $(A, B, C) = (0, 0, 0)$ to $(1, 0, 0)$, the output voltage level is not kept constant at $-2\,\mathrm{V}$ during the transition of A from "0" to "1" ($-2\,\mathrm{V}$ to $2\,\mathrm{V}$). However, with all the inputs

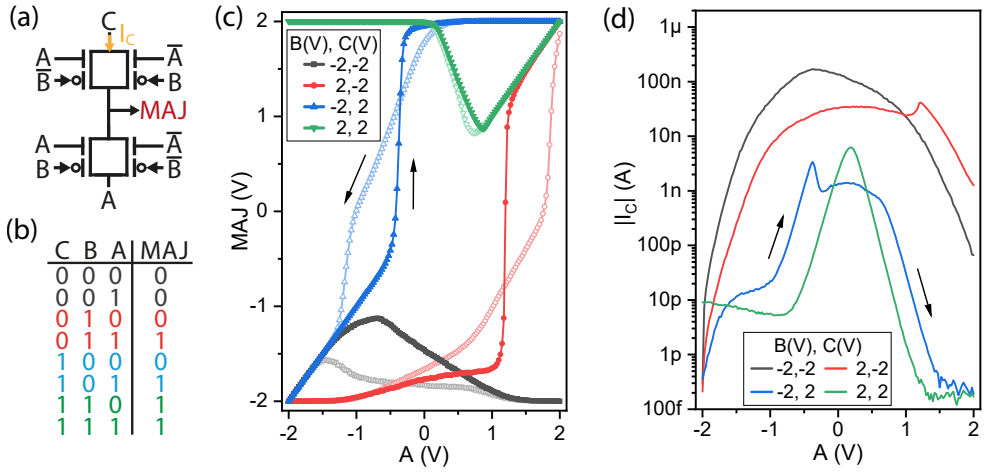

Figure 4.21: (a) Schematic of the MAJ gate based on four RFETs, with its corresponding truth table in (b). (c) Voltage transfer characteristic of the MAJ gate, with the input A swept in both directions. (d) Cross-current flow I_C, with A increased from $-2\,\mathrm{V}$ to $2\,\mathrm{V}$.

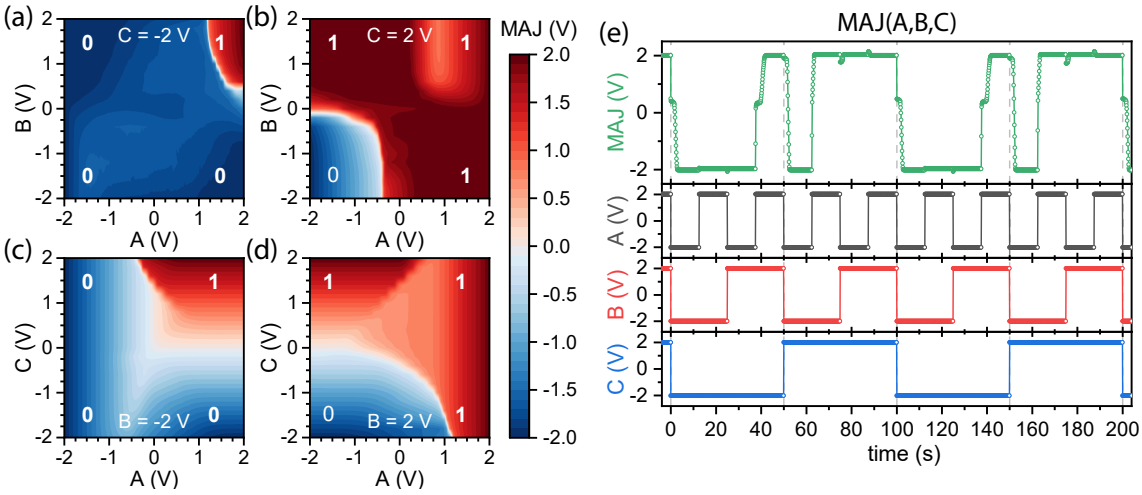

Figure 4.22: Output color maps for the MAJ gate, showing the output voltage depending on the inputs A, B (a,b), and A, C (c,d), with the other input fixed at $\pm 2\,\mathrm{V}$. (e) Transient measurement of the MAJ gate, showing its logic operation in response to the input signals A, B and C.

set to the maximum values of $\pm 2\,\mathrm{V}$, the output also reaches full swing operation. The cross-current flow in Figure 4.21(d) again shows the characteristic of the complementary design, with a current flow I_C <169 nA between the state transitions and steady state currents below 1.2 nA. In particular, for the steady states at $A = C$, no current flow above the noise level of the measurement setup (≈200 fA) can be measured, as there is no voltage difference at the supply nodes of the circuit.

The output color maps for the MAJ gate in Figure 4.22(a-d) show that the voltage level at the output is less constant than in the previously shown logical gates. This is caused by the direct coupling of inputs A and C to the supply rail voltages of the circuit and thus to the output voltage. This further leads to less sharp transitions between some logical states. Nevertheless, stable operation regimes for all output states are evident in the output maps, providing sufficient noise immunity. The transient measurement in Figure 4.22(e) shows the output response to the complete input sequence, with all logic states being correctly reached at a full output swing of $\pm 2\,\mathrm{V}$. Since the MAJ gate essentially shares the same circuit design as the XOR3 gate shown previously, with the large planar contact pads inducing large parasitic capacitances, the frequency for the input signal sequence in this demonstrator is also limited. This can result in slow transitions with some logic degradation.

4.5.5 1-bit Full Adder

Combining the two circuits for the XOR3 gate and the MAJ gate, a fully functional 1-bit full adder can be realized. Remarkably, this can be done with a total number of eight physically identical RFETs, excluding inverters for providing the inverted input signals. As shown in Figure 4.23, the XOR3 gate is thereby used for calculating the sum, while the MAJ gate is used to calculate the carry output C_{out}. The transient measurement

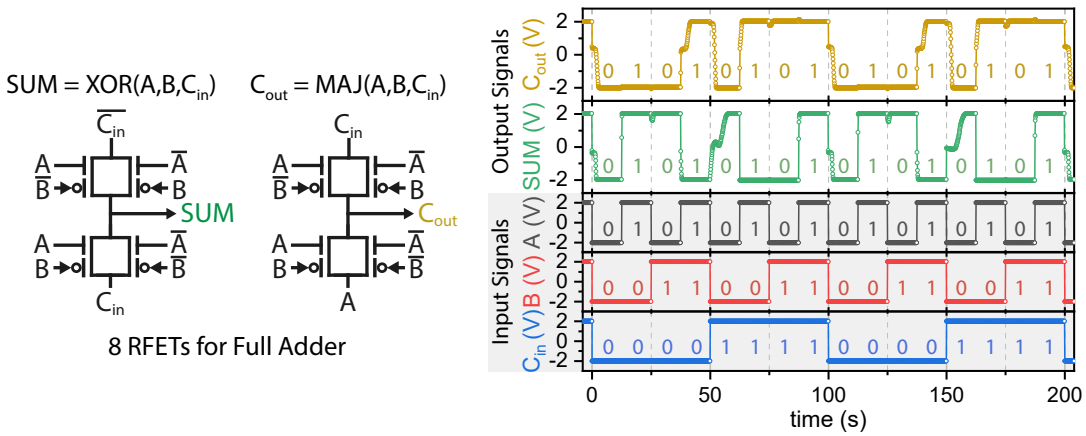

Figure 4.23: 1-bit full adder realized with eight RFETs, with the XOR3 gate for the sum operation and the MAJ gate for the carry output C_{out}. The transient measurement shows the correct operation of the circuit, with a full output swing provided for supply voltages of ±2 V.

demonstrates the fully functional 1-bit full adder, with the inputs A, B and C_{in} leading to the correctly calculated outputs SUM and C_{out}. As the two gates are operated in a transmission gate configuration, additional gates may be required to drive the gates, which may result in additional overhead depending on the targeted application and whether the circuit is co-integrated with CMOS or in a full transmission gate logic setup.

This work shows the first experimental realization of a reconfigurable full adder [LW6]. In standard CMOS technology, 28 transistors with differently doped channels (n-FET, p-FET) are required for a static [267], and 14 transistors for a transmission gate implementation [268]. Simulations by Gore et al. [20] using a predictive process design kit (PDK) showed that with the given reduced transistor count, despite the larger individual transistor sizes, an area reduction of 41 % for the 1-bit full adder and 26 % for XOR gates is achievable. In addition, Amaru et al. [79] demonstrated feasible switching speeds of the RFET-based full adder in the GHz range using HSPICE simulations based on a 22 nm technology node, even 3.8x faster than its conventional CMOS counterpart due to reduced propagation delays. These results are also supported by simulations by Cadareanu et al. [19] that show an 18 % reduction in EDP in the full adder circuit despite a 30 % increase in parasitic gate capacitance per RFET. Recently, Quijada et al. [81] predicted further performance improvements for the integration of Ge channel RFETs using TCAD simulations.

4.6 Multi-Wire RFETs

Although the preceding devices have already demonstrated very good electrical characteristics, especially with regard to their excellent symmetry and good turn-off behavior, their on-state currents are still quite limited with values in the low µA range. Therefore, fabricating devices with multiple parallel semiconductor channels is an effective strategy for scaling drive currents. The increased number of channels thereby increases the effective channel width of the devices while also maintaining good electrostatic control due to the tri-gate architecture of each individual channel [10, 269]. Additionally, as many parallel channels share individual S/D regions, the overall capacitance is lower compared to entire RFETs connected in parallel.

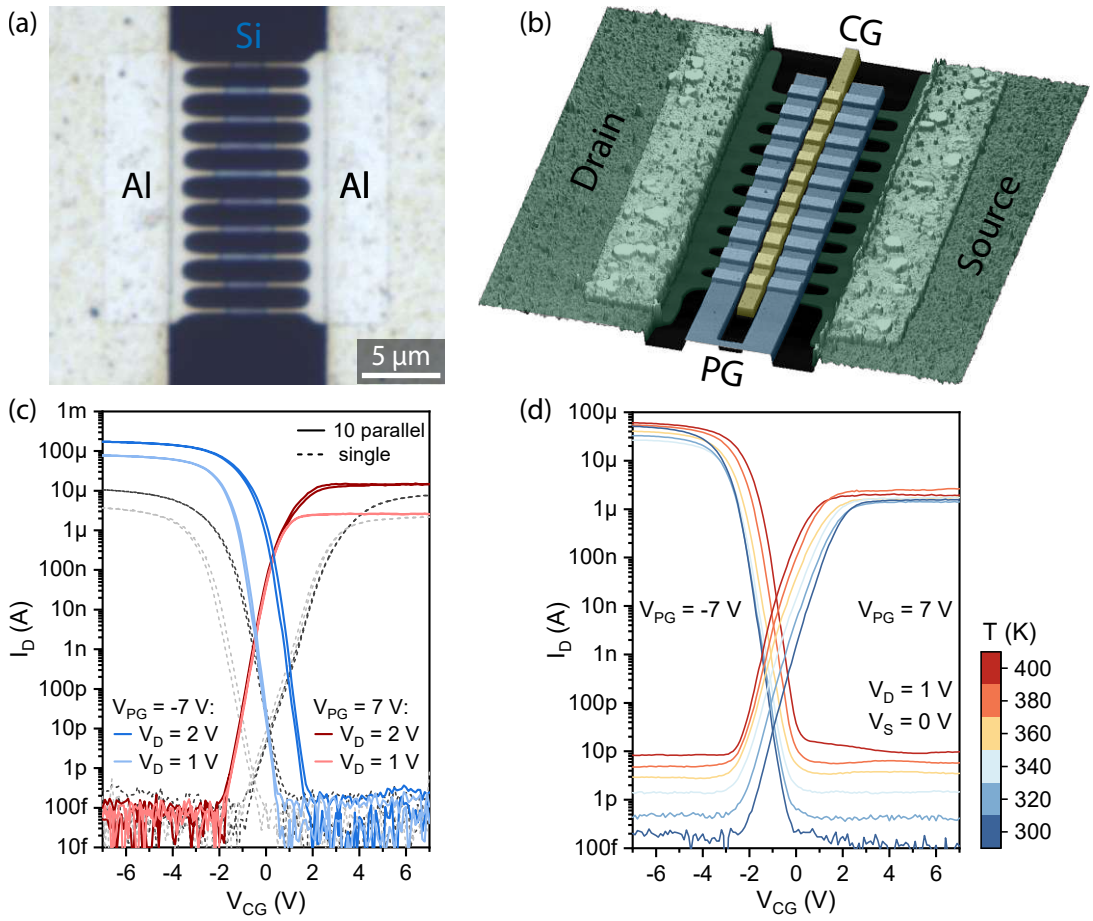

Figure 4.24: Multi-wire RFET based on ten parallel Si channels. (a) Microscope image of the parallel array of Al-Si-Al heterostructures, fabricated by the thermally induced Al-Si exchange reaction. (b) False-color AFM image of the multi-wire RFET. (d) Transfer characteristic at $V_D = 1\,\mathrm{V}$ and $2\,\mathrm{V}$ ($V_S = 0\,\mathrm{V}$) for the RFET with ten parallel Si channels (solid lines) compared to the single-channel RFET (dashed lines). V_{PG} is set to $7\,\mathrm{V}$ and $-7\,\mathrm{V}$ for n- and p-mode operation, respectively. (d) Temperature-dependent transfer characteristic for the multi-wire RFET between $300\,\mathrm{K}$ and $400\,\mathrm{K}$.

Figure 4.24 shows a fabricated RFET with ten parallel Al-Si-Al heterostructure channels. This is achieved by utilizing the reproducible Al-Si exchange process with the stable crystal phase of the Al leads, leading to significantly lower process variations compared to e.g., silicidation rates for common Ni_xSi_y lateral heterostructures [166]. In the optical microscope image after the heterostructure formation process in Figure 4.24(a), a slight but systematic variation of the Si channel within a single device is evident, with higher Al-Si exchange rates and therefore shorter channels towards the outer nanosheets. Interestingly, these experiments reveal the importance and spatial range of the Al-material supply at the contacts required for the exchange reactions. The nanosheets at the center exhibit a higher Al-material competition compared to the outer ones. However, it should be possible to reduce these variations by optimizing the lithography process for an improved uniformity of the channel width of the ten parallel wires,and by optimizing the structural design. A uniform channel length is crucial, as the PG has to be aligned atop all Al-Si interfaces of the structure for an effective electrostatic control of all injection barriers. In addition, low variation in diffusion rates allows the fabrication of devices with shorter channels. Figure 4.24(b) shows the false-color AFM scan of the complete multi-wire RFET structure, with rather wide PG electrodes to cover all metal-semiconductor interfaces. For the gate dielectric, a 13 nm thick SiO_2 layer was thermally grown on the Si structure.

The transfer characteristic in Figure 4.24(c) shows the device operation of the multi-wire RFET, with V_{PG} set to 7 V and −7 V to switch between n- and p-type operation. Note that the bias is applied asymmetrically, with $V_{DS} = V_D$ ($V_S = 0$ V), resulting in an asymmetrical fanning of the subthreshold characteristic. Compared to the device characteristic of a comparable single-channel RFET, the p-mode on-currents at $V_D = 2$ V have been significantly increased by a factor of ∼12, with $I^p_{on} = 172$ µA. Unexpectedly, the n-type current is only about twice as high ($I^p_{on} = 14.7$ µA), resulting in a decreased symmetry of the on-states ($I^p_{on}/I^n_{on} \approx 11.7$). Remarkably, no increase in off-state currents could be detected within the current resolution of the measurement setup. The hysteresis is also not significantly increased despite the larger surface area of the device, attributed to the good quality of the SiO_2 gate oxide. The subthreshold slope of the multi-wire RFET could even be improved, with extracted values of 294 mV/dec and 209 mV/dec for n- and p-mode operation, respectively, compared to the slopes of the single-channel device with the same gate oxide thickness (480 mV/dec, 320 mV/dec).

The temperature-dependent measurement in Figure 4.24(d) provides information about the thermal stability of the multi-wire RFET. Similar to observations in the single-wire devices in Figure 4.11, a pronounced increase in off-currents over temperature due to the increase of thermally activated carriers is evident. As the on-currents increase is smaller, this leads to a slight reduction of the on/off current ratio at elevated temperatures. However, stable operation with $I_{on}/I_{off} > 10^5$ is still maintained.

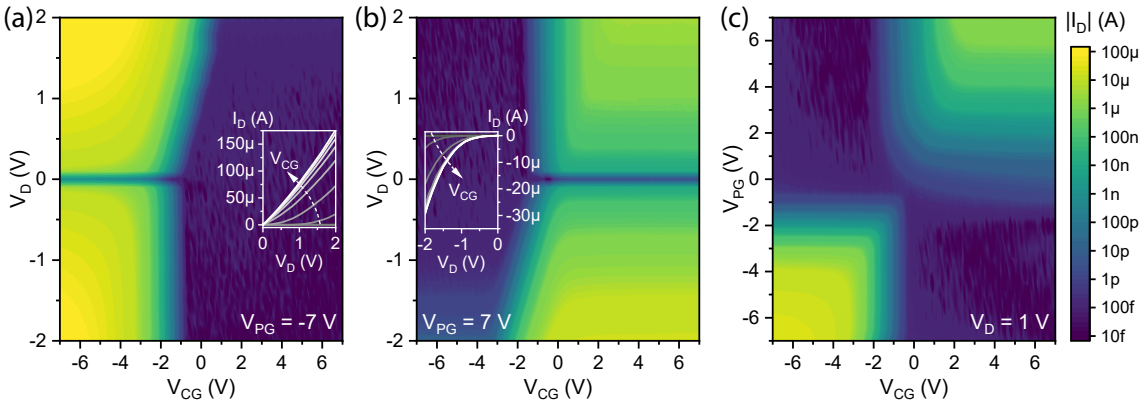

Figure 4.25: Output map of the multi-wire RFET from Figure 4.24 with 10 parallel Si channels for (a) p-type ($V_{PG} = -7\,\mathrm{V}$) and (b) n-type operation ($V_{PG} = 7\,\mathrm{V}$), measured with asymmetric bias conditions ($V_S = 0\,\mathrm{V}$). The insets show the linear I_D-V_D characteristic, with V_{CG} increased to $-7\,\mathrm{V}$ and $7\,\mathrm{V}$, respectively. (c) V_{PG}-dependent transfer characteristic at $V_D = 1\,\mathrm{V}$ ($V_S = 0\,\mathrm{V}$).

Figure 4.25(a,b) shows the output characteristic of the multi-wire RFET. Thereby, large on- and off-state regions are obtained, with its transition being slightly shifted towards negative V_{CG} values of around $-2\,\mathrm{V}$. Nevertheless, higher on-state currents for the p-mode conduction are reached, indicating lower injection barriers for holes. This is also reflected in the insets of the two color maps, showing the output characteristic in a linear scale. Thereby, an almost linear increase in current over the bias voltage V_D is obtained at high negative values of V_{CG}, indicating high transparency of the Al-Si junction for holes. For the n-type conduction, the exponential increase in the I/V characteristic indicates a higher, distinct Schottky barrier for the electron conduction. The PG-dependent characteristic in Figure 4.25(c) shows the stable transition between the n- and p-type operation by tuning the electrostatic injection barrier with V_{PG}, with large and distinct operation windows. Slight asymmetries are evident, with a less sharp transition to switch into the n-type operation with increasing V_{PG}, indicating a larger and less tunable electron injection barrier.

4.7 Al Top Gate SBFETs

The use of Au as a top gate material is avoided in the semiconductor industry, as it acts as deep-level trap and recombination center in Si, drastically reducing carrier lifetimes and therefore degrading the device performance [90]. Furthermore, its high diffusivity even at moderate temperatures can contaminate other device layers [270]. For the fabricated devices shown in the previous sections, the Au in the contact pads is mainly used because of its good properties for contacting with the needle probes or for bonding. The metal work function of the top gate should mainly be defined by the 10 nm thick Ti layer underneath the Au layer, which is in direct contact with the SiO_2 gate oxide. Therefore, it would be reasonable to replace the Au from the pads with other less critical material.

Since Al is already used for the S/D contact pads and thus for the formation of the Al-Si heterostructure, the use of Al as a top gate material is also a suitable way of reducing the number of different materials used. The electrical resistivity of Al with $2.65 \times 10^{-8}\,\Omega\,\mathrm{m}$ is also comparable to that of Au with $2.12 \times 10^{-8}\,\Omega\,\mathrm{m}$ (at 293 K) [87]. To study the influence of replacing Au with Al in the devices, comparable devices with two different top gate stacks, Ti/Au and Ti/Al (10 nm/100 nm layer thickness), were fabricated on the same chip. The deposition method for the metals was also changed from evaporation to sputtering because tests with Al evaporation (electron-beam method), especially on the EBL resist, have caused some lift-off problems. Also, sputtering is more common in the semiconductor industry. In addition, a rather short oxidation time of 3 min of the Si nanosheets was used to thermally grow a 6.4 nm thin SiO_2 gate oxide, reducing the operation voltages of the devices. Figure 4.26 shows the comparison of the two different Al-Si-Al-based SBFETs with different top gate stacks, with the microscope image and the device characteristic for the Ti/Au control device in (a-c) and the Ti/Al gated devices in (d-f). Both device types exhibit very similar ambipolar characteristics, with symmetric electron and hole-induced current levels at $V_G = \pm 3\,\mathrm{V}$. A slight shift of the characteristic to the left towards negative gate voltages can be seen for the structures with Ti/Al gates. This indicates that despite the 10 nm Ti layer, there is a slight influence on the work function of

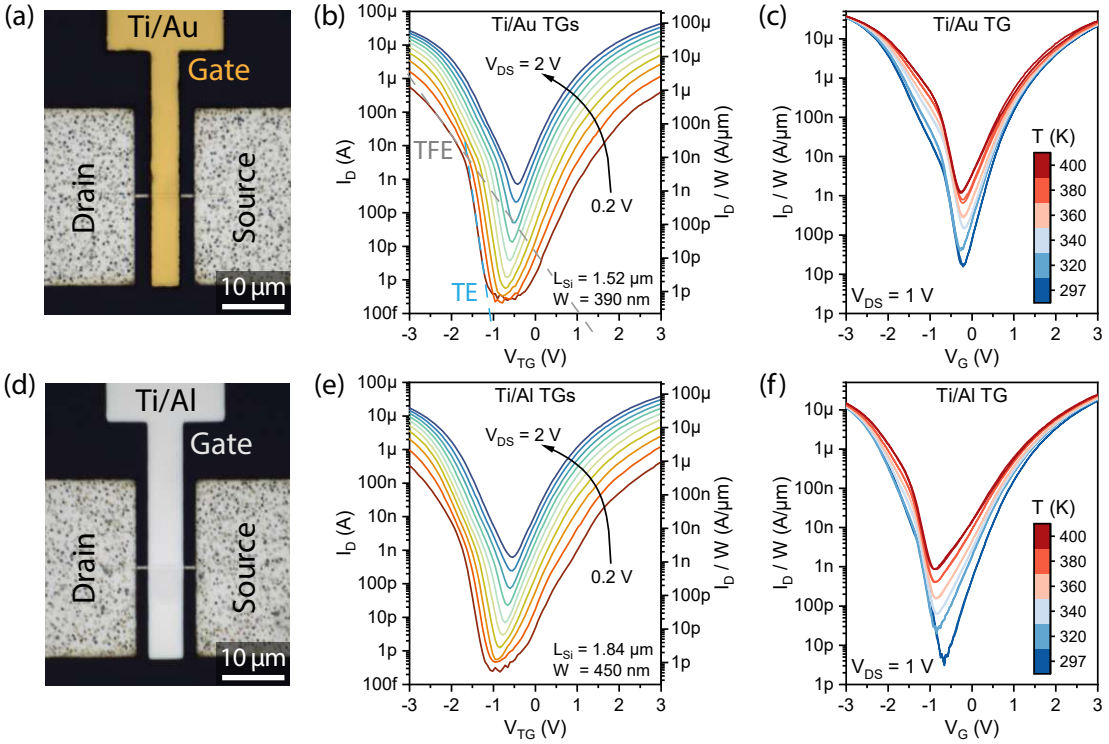

Figure 4.26: Comparison of Al-Si-based SBFETs with different top gate materials. (a) Microscope image, (b) bias-dependent, and (c) temperature-dependent transfer characteristic of an SBFET with a sputtered Ti/Au gate. (d-f) Microscope image and device characteristics for a Ti/Al top-gated SBFET. The transfer characteristics are measured with symmetrical bias $V_D = -V_S$.

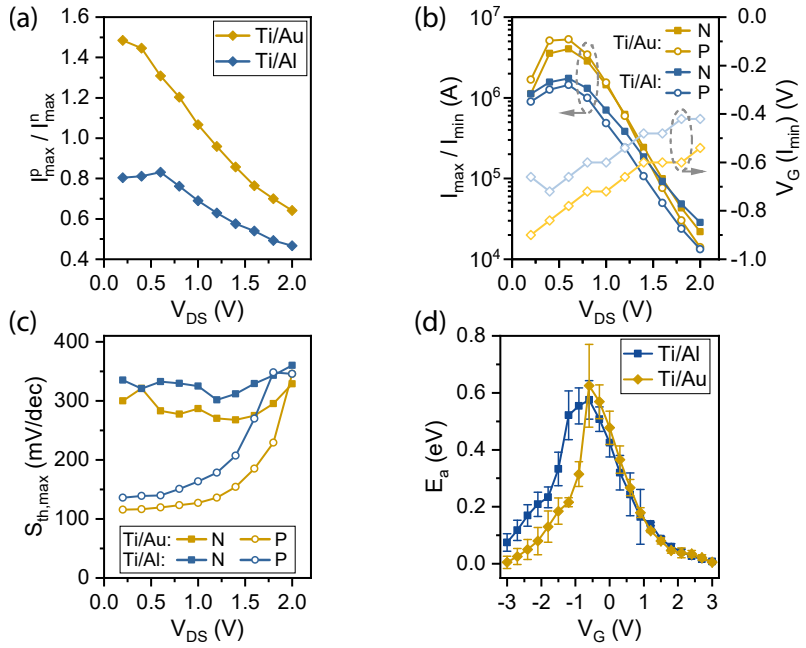

Figure 4.27: Transistor parameters of the Ti/Au and Ti/Al SBFETs, extracted from 4.26(b,d). (a) On-current symmetry I^p_{on}/I^n_{on}. (b) On/off ratio for both the n-branch measured at $V_G = 3\,\mathrm{V}$ and the p-branch at $V_G = -3\,\mathrm{V}$. The lighter lines for the right axis show the gate voltage V_G at the current minima $I_{D,min}$. (c) Bias-dependent subthreshold slopes $S^{n,p}_{th}$. (d) V_G-dependent activation energies E_a, extracted from the temperature-dependent output characteristics of three devices per device category. The error bars indicate the standard deviation.

the top metal layer. The significantly lower work function of Al (4.28 eV) compared to Au (5.1 eV) [191] therefore results in a small shift to the left. In the transfer characteristics, especially in the p-branch at lower bias conditions, a kink in the subthreshold region with two different slopes is evident (cf. Figure 4.26(b,e)). This clearly indicates the transition from the TFE/FE region with a shallow slope ($V_G < -1.6\,\mathrm{V}$) from a dominant charge carrier injection via tunneling to the steeper TE region ($V_G > -1.6\,\mathrm{V}$) mainly coming from carrier injection over the barrier. This transition between the two transport regimes was already described in simulations [209]. This kink is also clearly visible in the temperature-dependent transfer characteristics in Figure 4.26(c,f). Thereby, a stable operation for both device types at elevated temperatures up to 400 K is obtained, with a decreasing on/off ratio over temperature due to the stronger increase in off-currents.

The evaluation of the transistor parameter in Figure 4.27 shows the direct comparison of the two SBFETs with different TG metals. Overall, both devices reach a very high on-current symmetry within the V_{DS} measurement range, whereby the current of one branch remains below twice the value of the other branch. Consistently lower maximum p-type currents are obtained for the Ti/Al TG device, with $I^p_{max}/I^n_{max} < 1$, which can be attributed to the small left shift of the transfer characteristic due to the different work functions. Since the currents in the characteristic curve at $V_G = \pm 3\,\mathrm{V}$ are not saturated and

would still rise for higher gate voltages, a slight shift to negative V_G results in a decrease of I^p_{max} (and an increase of I^n_{max}). This consistent shift of the device characteristic is also shown in Figure 4.27(b), where V_G is extracted at the intrinsic point, the minimum current value I_{min}. While increasing the bias V_{DS} from 0.2 V to 2 V shifts the off-state point toward lower V_G, the shift due to the different gate materials remains fairly constant at about 0.12 V. The Ti/Au device achieves slightly higher on/off current ratios up to 5×10^7 at low bias voltages, but then approaches the values of the Ti/Al device at higher bias voltages $\geq$1.4 V. As in all the structures shown so far, the p-branch shows a clearly steeper subthreshold characteristic for both devices (see Figure 4.27(c)), with slightly lower S_{th} values for the Ti/Au gated structures. As V_{DS} is increased, the current in the transfer characteristic becomes more and more tunneling dominated (TFE/FE), with the kink and the steeper TE dominated region disappearing (cf. Figure 4.26(b,e)). This consequently results in an increase in the S_{th} for the p-type currents.

In Figure 4.27(d) the gate-dependent activation energies (E_a) from the temperature-dependent measurements are extracted. It can be seen that the lower metal work function from the Ti/Al gate stack results in higher activation energies in the p-branch. Therefore, a higher gate voltage is required to equally tune the hole injection barrier than for the Ti/Au device, resulting in a lower current flow for the same V_G. While the effective barrier for the Ti/Au device can be completely lowered to 0 eV at $V_G = -3$ V to achieve transparency for holes, a barrier of 75 meV remains for the Ti/Al device. The n-branch, however, does not seem to be affected by the change of top gate metals, reaching $E_a \approx 0$ eV for transparent Al-Si junctions for electrons, resulting in a quasi-ohmic behavior.

From the direct comparison of the two gate stacks, it can be concluded that the Ti/Au top gate devices have slightly better overall device characteristics. Nevertheless, it is feasible to replace the Au layer, with its undesirable properties in the semiconductor industry, with Al without significant loss of performance.

4.7.1 Ti/Al Top-Gated Si RFETs

Next, this sputtered Ti/Al gate stack is also used for the fabrication of TTG RFETs. Figure 4.28 shows the characteristics of a Ti/Al top-gated RFET, with a Si channel of $L_{Si} = 2.4$ µm, $W = 380$ nm and $H = 18$ nm, operated at $V_{PG} = \pm 3$ V to switch between the n- and p-mode. As expected from the previous results of the STG SBFETs, the subthreshold characteristic of the Ti/Al gated devices is slightly shifted to the left towards negative V_{CG}. This results in asymmetric threshold voltages V_{th} of 0.4 V for the n-type and -1.86 V for the p-type operation, derived from the room temperature characteristic in Figure 4.28(a) at $V_{DS} = 1$ V. Nevertheless, a high on-current symmetry of $I^p_{on}/I^n_{on} = 1.9$ to 0.93 within the bias range of 0.2 V to 1 V is obtained. For the low-bias curves, this is even an improvement compared to the Ti/Au-based RFETs in Section 4.3, where symmetry values below 2 are reached only for bias voltages >1 V. The subthreshold slopes with $S^n_{th} = 193$ mV/dec and $S^p_{th} = 160$ mV/dec are again slightly steeper for the p-type operation and comparable to the Ti/Au devices.

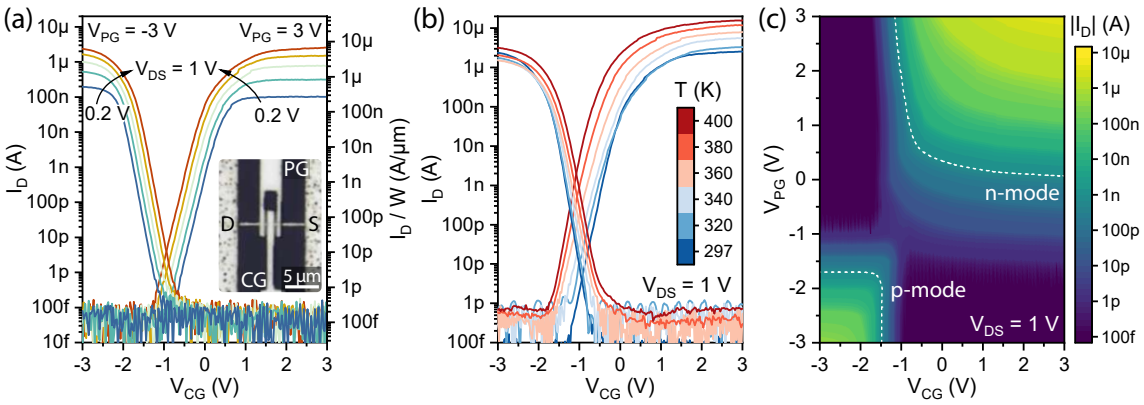

Figure 4.28: (a) Subthreshold transfer characteristic of an Al-Si RFET with Ti/Al top gates, with V_{PG} set to 3 V and −3 V to switch between n- and p-type operation, respectively. The bias voltage V_{DS} ($V_D = -V_S$) is increased from 0.2 V to 1 V in 0.2 V steps. The microscope image of a fabricated device is shown in the inset. (b) Temperature-dependent measurement from 297 K to 400 K at $V_{DS} = 1$ V. (c) Semi-logarithmic color map showing the V_{CG} and V_{PG}-dependent current flow I_D. The dashed lines at $I_D = 1$ nA indicate the two operation modes. Device dimensions: $L_{Si} = 2.4$ µm, $W = 380$ nm.

At elevated temperatures in Figure 4.28(b), a strong increase of the on-state currents for the n-mode is evident, significantly exceeding the temperature dependency of the p-mode. This leads to a considerably increased asymmetry up to $I^p_{on}/I^n_{on} = 0.2$ at 400 K. The off-currents remain remarkably low, still not significantly exceeding the noise level of the measurement setup. The conduction map in Figure 4.28(c) shows the transition between the n- and p-mode conduction by varying V_{PG} and V_{CG}. Although the maximum on-state currents for both modes reach similar values, a rather asymmetric size of the operation regimes is evident due to the shifted characteristics from the Ti/Al gate stack. Therefore, for p-type on-state currents exceeding 1 nA (marked by the dashed lines), V_{PG} voltages <-1.75 V are required, while the same currents for the n-mode are already reached at $V_{PG} > 0.25$ V. To compensate for the shift induced by the lowered metal work functions of the Ti/Al gate stack, a high-κ dielectric layer such as HfO_2 or ZrO_2 could be integrated into the gate stack. This would not only shift the device characteristics to the right towards positive gate voltages but also enable further scaling of the EOT, resulting in lowered operation voltages and steeper subthreshold characteristics [271, 272].

Chapter 5

Al-$Si_{1-x}Ge_x$-Al Heterostructures

The integration of Ge and $Si_{1-x}Ge_x$ compounds as channel materials is highly promising to further enhance the performance of modern CMOS and bipolar devices. Especially in RFETs, but also in SBFETs in general, the smaller Schottky barriers associated with the reduced band gap, as well as smaller effective tunneling masses of both electrons and holes, can increase the transmissibility of the injection barriers [209]. This can lead to enhanced on-currents and thus faster switching capabilities compared to Si devices [81][LW9]. Furthermore, Ge can promote the development of emerging "More than Moore" device architectures, such as negative differential resistance (NDR)-based electronics [33, 34, 254], optoelectronics [243, 273] and quantum computing paradigms [188, 274]. However, metal-$Si_{1-x}Ge_x$ junctions often suffer from reliability issues and strong Fermi-level pinning, hindering their large-scale implementation.

In the following chapter, the metal contact formation to $Si_{1-x}Ge_x$ nanosheets of different stoichiometries is discussed, and their composition-dependent transport properties are analyzed. In this regard, our project partners at the JKU Linz provided us substrates with vertical Si-$Si_{1-x}Ge_x$-Si layers epitaxially grown on top of SOI and sSOI substrates, with Ge layer concentrations of 33 %, 50 %, 75 % and 100 %. More details regarding the growth of these substrates can be found in the experimental part in Section 3.1.1. Based on the promising results, $Si_{0.67}Ge_{0.33}$ nanosheets are then integrated into a three top-gated architecture to fabricate RFETs with enhanced device properties. Furthermore, a high-κ HfO_2 dielectric layer is introduced into the gate stack of the $Si_{0.67}Ge_{0.33}$-based RFETs to improve the electrostatic gating. Finally, the various RFETs fabricated in this work are compared with other state-of-the-art devices found in the literature.

The results and discussions in this chapter are primarily based on the author's work in the publications on composition-dependent transport in $Si_{1-x}Ge_x$ nanosheets [LW13] and $Si_{0.67}Ge_{0.33}$-based RFETs [LW11]. Furthermore, the results have led to the conference contributions [LWC2, LWC11, LWC12, LWC17, LWC23].

5.1 Contact Formation to $Si_{1-x}Ge_x$ Heterostructures

Similar to the SOI-based devices from the previous chapter, small nanosheets are patterned from the $Si_{1-x}Ge_x$ heterostructure substrates using laser lithography and SF_6-O_2-based RIE processes. The MBE-grown vertical Si-$Si_{1-x}Ge_x$-Si heterostructure as the active region in the nanosheet devices is shown in the HRSTEM image in Figure 5.1(a). A 10.6 nm thick Al_2O_3 layer was then grown by ALD to passivate the mesa structures, which also serves as the gate dielectric for top-gated electrical characterization. To contact the $Si_{1-x}Ge_x$ heterostructure nanosheets, 125 nm thick Al pads are sputtered after removing the Al_2O_3 passivation in the contact area with a 15 s BHF etching step. As for the pure Si structures on the SOI substrate, a thermally induced exchange process can be observed by using RTA at 773 K in forming gas. Thereby, both Si and Ge are diffusing into the Al contacts, forming monolithic contacts to the vertical $Si_{1-x}Ge_x$ stack. The diffusion coefficients of both Si and Ge in Al, as well as the Al self-diffusion, are comparatively high, while the diffusion of the other species, i.e., Al in Si and Ge, is orders of magnitudes lower (see Table 2.4). This asymmetry leads to a fast out-diffusion of the Si and Ge atoms mainly into the large Al pads, while they are replaced by Al atoms via fast self-diffusion. The diffusion of Al into the $Si_{1-x}Ge_x$ channel, as well as an intermixing of the Si and Ge atoms from the heterostructure layers, should be negligible due to the low annealing temperatures of 773 K and short annealing times $\leq$5 min. Figure 5.1(b) shows the SEM image of an Al-$Si_{1-x}Ge_x$-Al heterostructure after the Al-Si/Ge exchange process, with a remaining $Si_{1-x}Ge_x$ channel length of $\sim$1 µm. An axial cut of the entire monolithically formed heterostructure, including the base SOI substrate, is shown in the STEM and EDX images in Figure 5.1(c,d). There it can be seen that the epitaxial Si-$Si_{1-x}Ge_x$-Si heterostructure remains intact over the entire channel of the device.

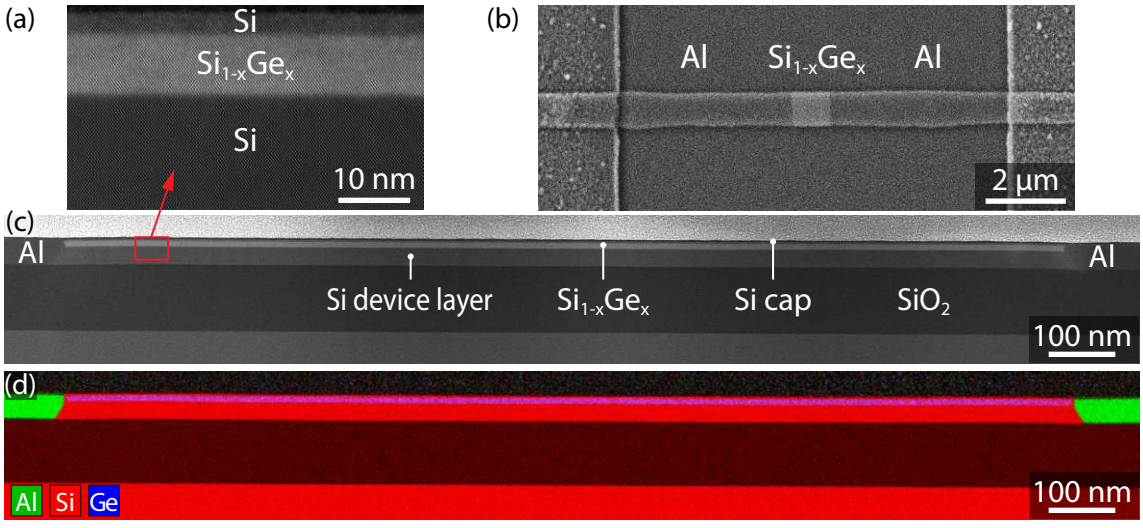

Figure 5.1: (a) HRSTEM image of the MBE-grown vertical Si-$Si_{1-x}Ge_x$-Si stack, here for $x = 0.33$. (b) SEM image of the Al-$Si_{1-x}Ge_x$-Al heterostructure formed by the thermally induced exchange reaction. (c) STEM and (d) EDX map of the entire monolithic Al-$Si_{1-x}Ge_x$-Al heterostructure.

A more detailed investigation of the monolithically formed metal-semiconductor interface is shown in Figure 5.2. Thereby, two samples with different stoichiometries, with 33 % Ge layer content in (a-d) and 75 % Ge in (e-h), are analyzed with HRSTEM and EDX scans. The samples with the other $Si_{1-x}Ge_x$ compositions were also examined and delivered consistent results. Thereby, for all investigated stoichiometries, a thin, Si-rich segment in-between the crystalline Al lead and the unreacted $Si_{1-x}Ge_x$ region was found. This can also be seen in the EDX line scans in Figure 5.2(c,g). Interestingly, a clear peak of the Si intensity arises in between the Al signal decay and the Ge signal increase to the nominal $Si_{1-x}Ge_x$ composition. These line scans, together with the elemental mapping (c,g) and the clear contrast region between the Al and the $Si_{1-x}Ge_x$ in the HRSTEM images (a,e) can be interpreted as a Si interlayer of a thickness of 3 nm to 4 nm. There, the Si region shows a single-crystal structure epitaxially aligned towards the $Si_{1-x}Ge_x$ layer, Si buffer and capping layer. Investigations in $Si_{0.67}Ge_{0.33}$ NWs have shown similar pile-up formations, but not as a closed layer [176]. Interestingly, the Si interlayer is also formed in structures with a pure Ge layer in this vertical Si-Ge-Si heterostructure, presumably diffusing from the two adjacent Si layers. This thin Si interlayer can play an important role in reducing the strong Fermi level pinning of the Al-Ge junction to achieve a more balanced injection of both carrier types into the semiconductor channel. The exact mechanism leading to this Si pile-up region is still unclear. More detailed investigations, such as in-situ TEM studies of the thermal exchange reaction, would be required. It can

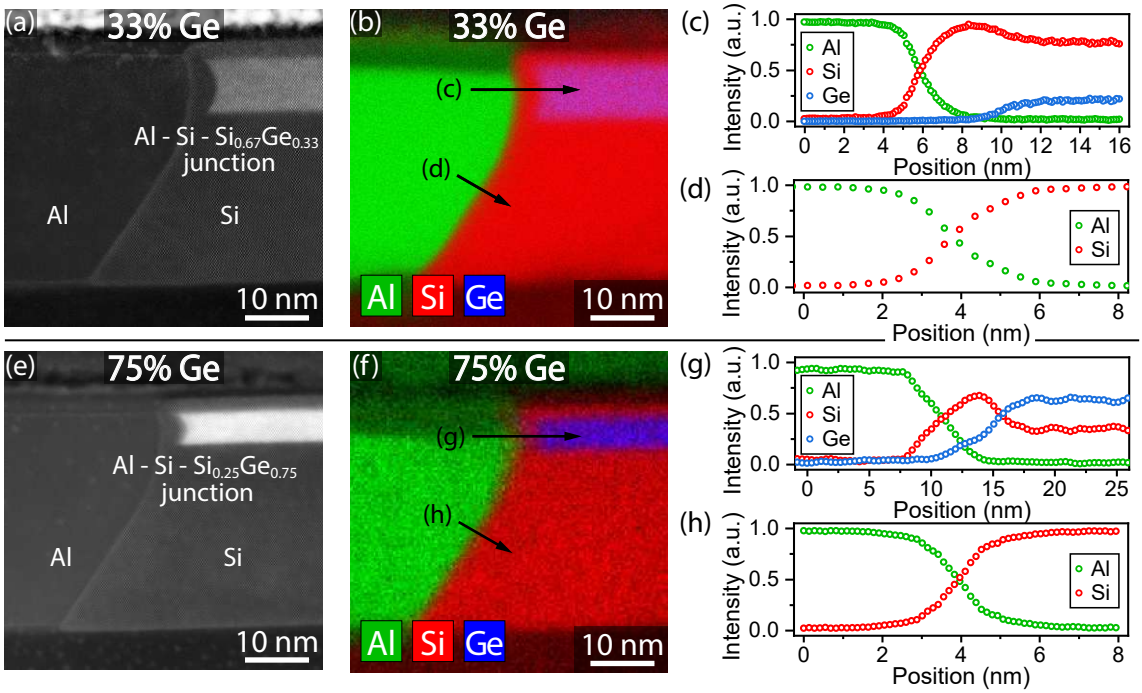

Figure 5.2: Close-up view of the formed metal-semiconductor interface for structures with a Ge layer content of (a-d) 33 % and (e-h) 75 %. (a,e) HRSTEM images and (b,f) EDX maps. (c,g) Line scans across the Al-Si-$Si_{1-x}Ge_x$ heterojunctions. (d,h) Line scans of the Al-Si interfaces.

be assumed that the significantly faster Ge diffusion compared to Si could promote the formation of the Si interlayer.

The line scans in Figure 5.2(d,f) show the abrupt, single-elementary Al-Si interface. It has to be noted that electron scattering actually broadens the local definition. As expected from previous investigations with exchange reactions between pure Si and Ge with Al [LW14, LW17][62, 63, 275] and the binary Al-Si and Al-Ge phase diagrams in Figure 2.6, no intermetallic phases are formed. Furthermore, no traces of Al in the unreacted Si and $Si_{1-x}Ge_x$ regions are detected within the EDX resolution limit (<1 %). The pure and crystalline Al leads were identified as a face-centered cubic structure, with the interface oriented in an {111} facet, bending towards an {110} facet close to the $Si_{1-x}Ge_x$ layer at the top of the vertical stack. The $Si_{1-x}Ge_x$ channel itself is terminated by two {111} facets towards the Si interlayer.

5.2 Composition-dependent Electrical Transport in Al-$Si_{1-x}Ge_x$-Al Heterostructures

To analyze the electrical properties of the fabricated Al-$Si_{1-x}Ge_x$-Al heterostructures with the different stoichiometries, Ti/Au top gates (10 nm/100 nm) were deposited atop the 10.6 nm thick ALD-grown Al_2O_3 gate dielectric (see Figure 5.3(a)). A direct comparison of the transfer characteristics of all fabricated samples with Ge layer contents of 33 %, 50 %, 75 % and 100 % is shown in Figure 5.3(b), with channel lengths from 1 µm to 4 µm. An SBFET with Al-Si-Al heterostructures based on an SOI substrate (20 nm Si device layer) with the same gate stack is also included as a reference. The transfer characteristics of all samples are measured under the same conditions, with $V_D = V_{DS} = 1\,\mathrm{V}$ and V_G swept from $-5\,\mathrm{V}$ to 5 V. To minimize the influence of slow charge carrier traps mainly coming from the Si/Al_2O_3 interface, pulsed V_G measurements were conducted. For a fair comparison of the different samples to compensate geometric variations, the conductivity is calculated from the measured current I_D and the dimension of the semiconductor channel, with $\sigma = I_D/V_D \cdot L/A$. For the cross-section A of the channel, the whole vertical Si-$Si_{1-x}Ge_x$-Si stack is considered. However, especially for the structures with high Ge content, it can be assumed that the current flow is mainly confined to the Ge-rich layer. Therefore, by reducing the Si device and buffer layer below the $Si_{1-x}Ge_x$ layer, the effective conductivity calculated from the entire vertical stack of nanosheets can presumably be further increased.

A clear increase of the on-state conductivity in the hole-dominant p-type region ($V_G < 0\,\mathrm{V}$) for the structures with higher Ge content is evident due to the lower band gap and thus smaller effective barriers and enhanced injection. Furthermore, the intrinsic point with the lowest conductivity is shifting towards higher positive gate voltages. The electron-dominated current flow and thus the n-type on-state conductivity ($V_G > 0\,\mathrm{V}$) decrease with increasing Ge concentration, resulting in a gradually decreasing ambipolar behavior. While the pure Si sample shows an ambipolar behavior with very symmetric on-states, the structures with the pure Ge layer show a strong p-type behavior without a significant

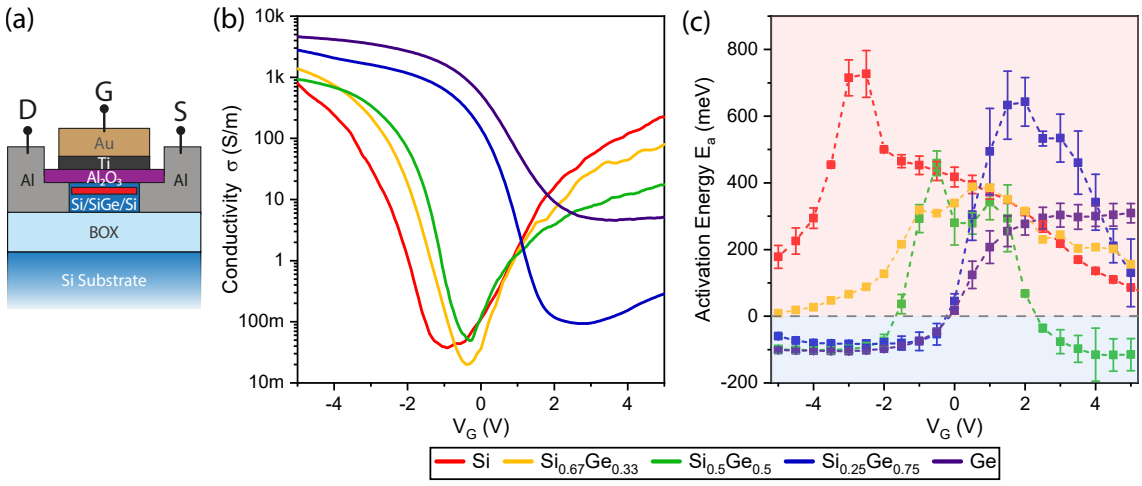

Figure 5.3: (a) Schematic of the SBFETs based on Al-$Si_{1-x}Ge_x$-Al heterostructures. (b) V_G-dependent conductivity measurement and (c) activation energy (E_a) extraction for $Si_{1-x}Ge_x$ SBFETs with different Ge layer concentrations. The negative E_a-region is marked in blue, indicating transparent carrier injection barriers.

increase in electron conductivity with increasing V_G. This behavior can be related to the fact that the Ge layer is vertically sandwiched between two Si layers. This creates an abrupt discontinuity in the valence band structure at the interfaces due to an expected band offset of ≈500 meV [113], causing a constant flow of holes from Si to Ge to maintain a constant chemical potential throughout the heterostructure [98]. The holes are thus confined within the Ge layer, resulting in the formation of a 2D hole gas [276].

Extracting the activation energies E_a in Figure 5.3(c) via the thermionic emission theory from temperature-dependent measurements between 295 K and 400 K gives more insights into the dominant carrier injection properties for the different Al-$Si_{1-x}Ge_x$-Al heterostructures. In good agreement with the transfer characteristic, the pure Si structures showed comparable, positive E_a, and thus comparable Schottky barriers for both electrons and holes. Interestingly, the heterostructures with 50 % Ge content show the contrary behavior, with negative E_a values for both carrier types, resulting in transparent, quasi-ohmic contacts. Thereby, we can assume that an injection into the $Si_{0.5}Ge_{0.5}$ is achieved. Although the pure Si structures feature higher extracted (thermionic) barriers for the electrons than the $Si_{0.5}Ge_{0.5}$ structures, a higher conductivity for the n-branch ($V_G > 0$ V) is evident. Therefore, it needs to be considered that despite the Si interlayer in the Al-Si-$Si_{1-x}Ge_x$ interface, the Fermi level still pins closer to the VB, favoring the p-type conduction and also affecting the n-type regime. Therefore, the pure Si samples have a thinner tunnel barrier for electrons compared to the $Si_{1-x}Ge_x$ structures, resulting in higher tunnel currents and thus higher conductivity in the n-branch. For higher Ge concentrations, the high transparency for the holes is retained, while the electron injection barrier increases up to ≈300 meV for the pure Ge layer sample. Changing the top gate voltage V_G therefore merely modulates the energy barrier for holes rather than enabling electron conduction.

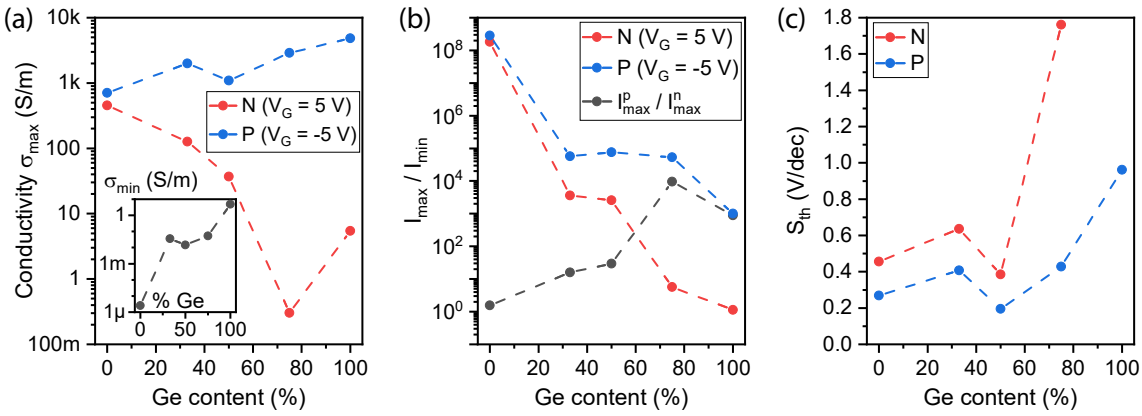

Figure 5.4: Si$_{1-x}$Ge$_x$ composition-dependent extraction of the SBFET properties. (a) On-state conductivity σ_{max} for the n- and p-branch at $V_G = 5\,\mathrm{V}$ and $-5\,\mathrm{V}$, respectively. The minimum conductivity σ_{min}, measured at the intrinsic point, is shown in the inset. (b) On/off current ratio and on-current symmetry I^p_{max}/I^n_{max}. (c) Subthreshold slope S_{th} depending on the Ge content.

Extracted from the transfer characteristics, the device performance parameters of the different top-gated Si$_{1-x}$Ge$_x$ SBFETs are plotted as a function of their Ge layer content in Figure 5.4. The p-type on-state conductivity σ^p_{max} is increasing from 708 S/m for the pure Si nanosheets up to 4825 S/m for the pure Ge layer structures. In contrast, the conductivity for the n-branch (σ^n_{max}) decreases for higher Ge concentrations, with Si reaching 452 S/m down to 0.3 S/m for 75 % Ge structures. Although the Ge structures do not show an electron-induced current flow, with $\sigma^n_{max} = \sigma_{min}$, the conductivity at $V_G = 5\,\mathrm{V}$ is still higher than that of the Si$_{0.25}$Ge$_{0.75}$ structures, possibly due to differences in the Schottky barrier height for electrons. As the minimum conductivity σ_{min} of the intrinsic point is strongly increasing with the Ge content by orders of magnitude (see inset in Figure 5.4(a)) due to the lower band gap and the increased carrier concentration, also the on/off current ratio in Figure 5.4(b) is strongly decreasing. The change from a symmetric ambipolar

Vertical stack	σ^p_{on} (S/m)	σ^n_{on} (S/m)	σ_{min} (S/m)	S^p_{th} (V/dec)	S^n_{th} (V/dec)
Si (SOI device layer)	708	452	2.5×10^{-6}	0.27	0.46
Si-Si$_{0.67}$Ge$_{0.33}$-Si	2000	126.6	0.035	0.41	0.64
Si-Si$_{0.5}$Ge$_{0.5}$-Si	1087	36.8	0.014	0.19	0.38
Si-Si$_{0.25}$Ge$_{0.75}$-Si	2885	0.3	0.053	0.43	1.76
Si-Ge-Si	4825	5.45	4.8	0.96	-
GeOI [38]	131	61	0.56	3.1	1.7
Ge NW [37]	752	0.4	71.8×10^{-3}	0.83	1.66
Ge/Si core/shell NW [277]	1.18×10^{5}	393	16	0.13	0.2

Table 5.1: Device performance metrics of different Si$_{1-x}$Ge$_x$ SBFETs. Additionally, devices fabricated from a GeOI substrate [38], as well as VLS-grown Ge NWs [37] and Si/Ge core/shell NWs [277] are compared. Note that [277] utilizes ultra-scaled 18 nm thick NWs with a 4 nm thick HfO_2 gate oxide.

behavior for the pure Si SBFETs to an increasingly strong p-type behavior by introducing Ge is also evident when comparing the on-current symmetries I^p_{max}/I^n_{max} in Figure 5.4(b). Generally steeper subthreshold slopes are extracted for the p-type conduction throughout all $Si_{1-x}Ge_x$ compositions (see Figure 5.4(c)), with 190 mV/dec to 410 mV/dec for the p-branch and 380 mV/dec to 640 mV/dec for the n-branch for samples incorporating $\leq$50 % Ge. While the $Si_{0.25}Ge_{0.75}$ structure with 430 mV/dec exhibits comparable slopes for the p-type conduction, a very shallow increase of the low electron-dominated conduction is evident. The SBFETs with the pure Ge layer only feature a p-type conduction with a relatively shallow slope of 960 mV/dec. By optimizing the gate stack, e.g., reducing interface charges and enhancing the body effect coefficient by introducing high-κ dielectric with a reduced EOT and scaled channel dimensions, the performance metrics of the devices can still be improved. The performance metrics of the fabricated SBFETs are summarized in Table 5.1, also including $Si_{1-x}Ge_x$-based devices found in literature.

To give more insights into the transport properties of the fabricated devices, the output characteristics of two exemplary devices, with 100 % and 33 % Ge layer concentrations, are shown in Figure 5.5. In (a,b), the device with the vertical Si-Ge-Si stack shows the pure p-type behavior, with a hole-induced current flow at negative gate voltages.

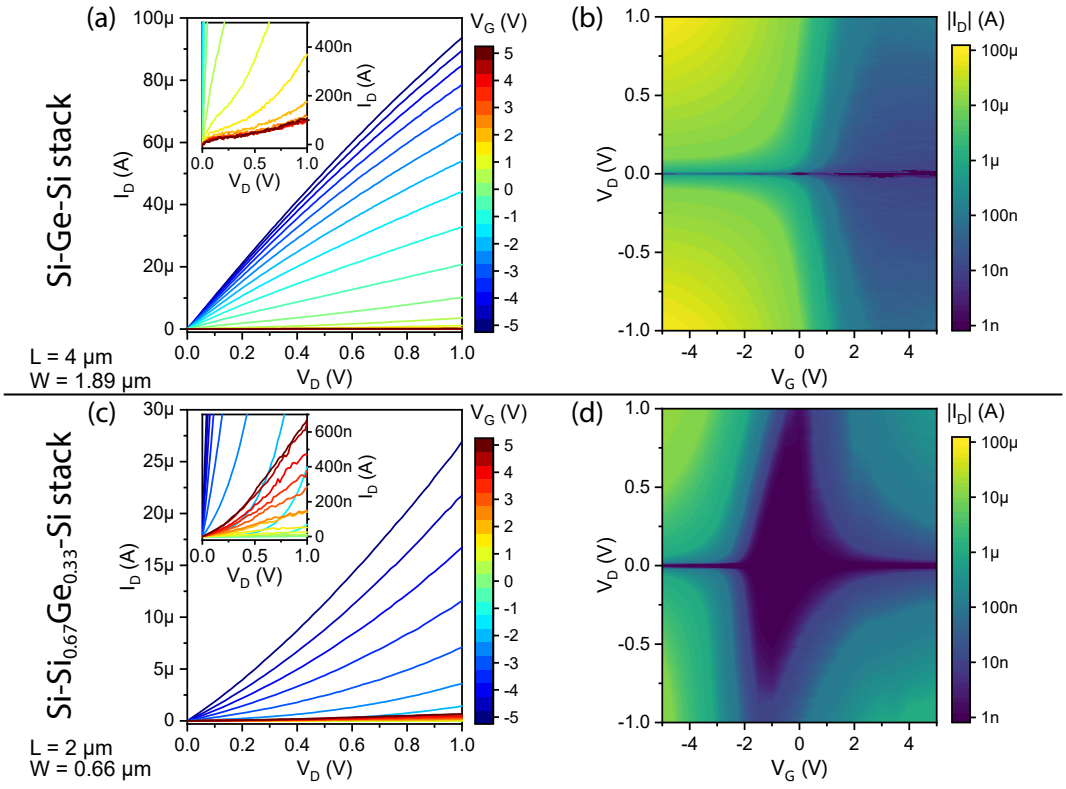

Figure 5.5: Output characteristics of SBFETs based on the vertical (a-b) Si-Ge-Si and (c-d) Si-$Si_{0.67}Ge_{0.33}$-Si heterostructures. (a,c) Linear I/V-characteristic, with the inset showing a zoomed view of the low current region for positive V_G. (b,d) Semi-logarithmic color map representation of the output characteristic.

Thereby a linear increase in current I_D over a wide measurement range is evident for $V_G < 0\,\mathrm{V}$, attributed to the highly transparent, quasi-ohmic contacts. In contrast to the Si SBFETs described before, a slight onset towards saturation can be observed. At positive V_G, a clear nonlinear increase in current with the bias voltage V_D is evident due to the distinct Schottky barriers (see inset). In contrast, the ambipolar $Si_{0.67}Ge_{0.33}$ heterostructure devices in Figure 5.5(c,d) show a nonlinear, exponential current increase over the full V_G measurement range of $\pm 5\,\mathrm{V}$. For both the electron- ($V_G > 0\,\mathrm{V}$) and hole-induced conduction ($V_G < 0\,\mathrm{V}$), charge carriers are injected through distinct Schottky barriers, whose thickness and thus its related tunnel transmissibility is changed by the bias voltage. The off-state region of the $Si_{0.67}Ge_{0.33}$ SBFETs is centered around $V_G = -1\,\mathrm{V}$ to $0\,\mathrm{V}$ at currents below $1\,\mathrm{nA}$, while the pure Ge layer SBFETs show rather gate-independent off-state currents of $\sim$100 nA for $V_G > 2.5\,\mathrm{V}$.

Finally, temperature-dependent transfer characteristics in the range of 300 K to 400 K are measured for the different $Si_{1-x}Ge_x$ compositions. Thereby, both the pure Si as well as the $Si_{0.67}Ge_{0.33}$ heterostructure devices showed a small increase in on-state current for both the n- and p-type branches in the ambipolar characteristic, indicating a tunneling-dominated charge carrier injection through distinct Schottky barriers. Remarkably, the opposite behavior can be seen for the $Si_{0.5}Ge_{0.5}$ structures, where the conductivity for

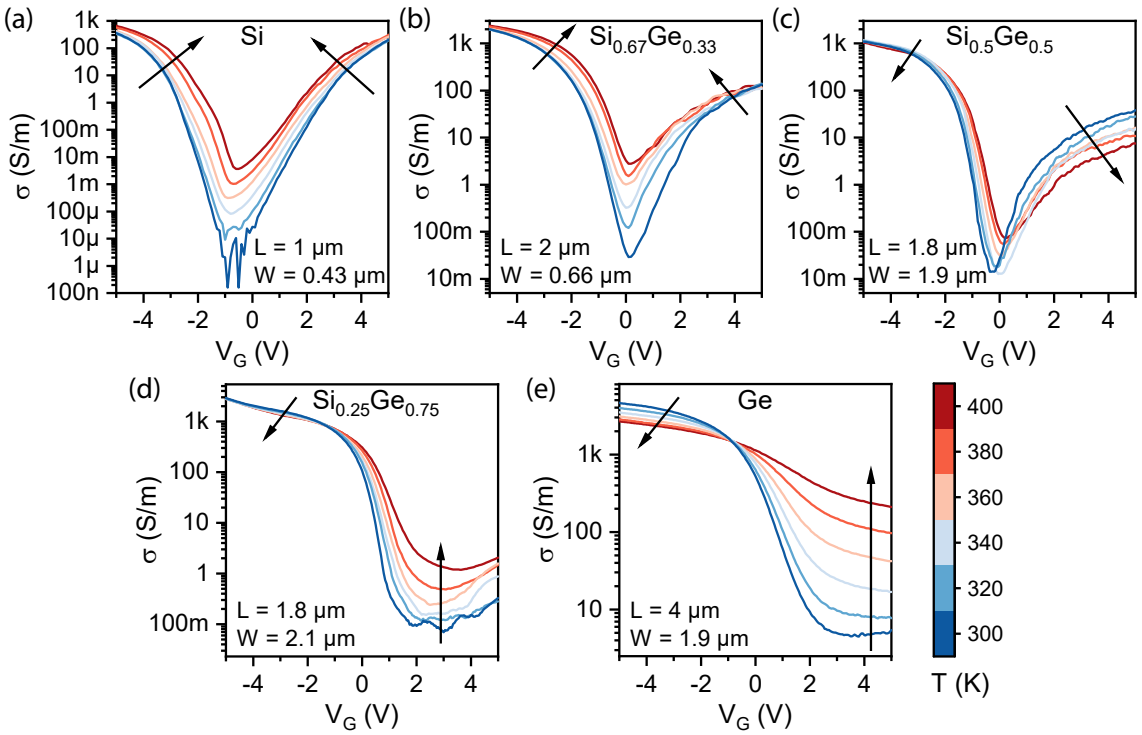

Figure 5.6: Temperature-dependent transfer characteristics of (a) Si, (b) $Si_{0.67}Ge_{0.33}$, (c) $Si_{0.5}Ge_{0.5}$, (d) $Si_{0.25}Ge_{0.75}$, and (e) Ge nanosheets embedded in Al-$Si_{1-x}Ge_x$-Al heterostructure SBFETs in the range of 295 K to 400 K, measured at $V_D = 1\,\mathrm{V}$. The arrows indicate the change in on-state conductivity with increasing temperature.

both hole and electron conduction is decreasing. This is in good agreement with the E_a extraction from Figure 5.3(c), where transparent junctions for both carrier types were derived. This negative variation of the currents with temperature is also observed for the p-type conduction in the devices with 75 % and 100 % Ge layer concentration. Therefore, it can be concluded that scattering is the main contribution to the resistance of the devices at elevated temperatures. Furthermore, this indicates that the transport is limited by tunneling through the thin barrier, rather than thermionic emission. Such highly transparent junctions to intrinsic or lowly doped semiconductors have only rarely been observed, e.g., in carbon nanotubes with Pd contacts [278] or in systems that employ efficient Fermi-level depinning techniques [198, 279–281]. As the sample with 75 % Ge content still features a band structure that is close to the one of Ge [282], but also shows a distinct electron-induced conduction for $V_G > 3\,\mathrm{V}$, this heterostructure system may be very interesting for the implementation of NDR devices based on the electron transfer effect [34, 254].

A clear increase in off-state currents is evident for all samples regardless of the Ge content. This can be attributed to the increase of the thermally activated carriers overcoming the Schottky barrier. The increase in off-currents, extracted from the temperature-dependent transfer measurements in Figure 5.6, is also shown in Figure 5.7. In this semi-logarithmic plot, the extracted off-currents follow a linear trend, meaning an exponential increase of the currents with the temperature. This is in agreement with the thermionic emission theory from Equation 3.3. The pure Si sample thereby shows the largest increase in off-currents at elevated temperatures, which can be related to the largest activation energies extracted at the off-state (see Figure 5.3). The large temperature dependency of the Al-$Si_{1-x}Ge_x$-Al SBFETs operated in the off-state regime could be very interesting for the implementation of bolometers [283].

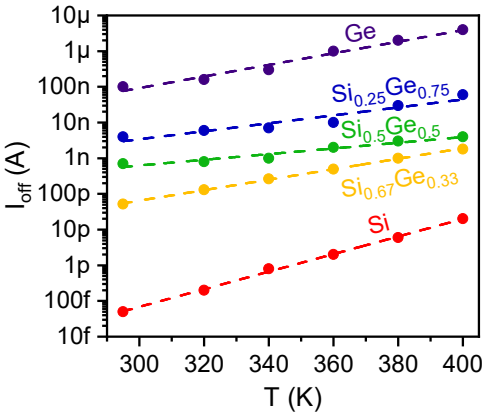

Figure 5.7: Temperature-dependent off-currents of the different Al-$Si_{1-x}Ge_x$-Al SBFETs, measured at $V_D = 1\,\mathrm{V}$. Values extracted from Figure 5.6.

5.3 $Si_{0.67}Ge_{0.33}$-based RFETs

The investigations of the transport properties of the $Si_{0.67}Ge_{0.33}$-based SBFETs have shown ambipolar characteristics with similar injection capabilities for both electrons and holes. Therefore, the integration of this vertical Si-$Si_{0.67}Ge_{0.33}$-Si heterostructure stack into RFETs may be promising to enhance the device performance by exploiting the advantages of Ge, resulting in higher on-state currents and increased switching speeds.

Since the direct integration of the Al_2O_3 dielectric layer on top of the Si capping layer in the previous samples, without the formation of a high-quality interface oxide, has led to reliability problems in the electrical measurements and introduced large hysteresis due to a high density of interface trap states, the gate stack was adapted. Therefore, after patterning the mesa structures, thermal dry oxidation at 1174 K for 3 min was used to transform the 3 nm Si capping layer of the Si-$Si_{0.67}Ge_{0.33}$-Si heterostructure into a high-quality ≈6 nm thick SiO_2 oxide. The subsequent fabrication steps are identical to those previously used for Si RFETs, with Al-$Si_{1-x}Ge_x$ contact formation and Ti/Au TG deposition after EBL patterning (see Section 3.1.2). Figure 5.8(a) shows the SEM image of a $Si_{0.67}Ge_{0.33}$-based RFET. The fabricated devices have a typical channel length L_{SiGe} of 1.6 µm to 2.1 µm, with channel widths W around 400 nm. The cross-sectional HRSTEM and EDX maps of the gate stack in Figure 5.8 show that the entire Si capping layer atop the $Si_{0.67}Ge_{0.33}$ layer is consumed, forming the ≈6 nm thick SiO_2 gate oxide. Remarkably, the oxide layer is encapsulating the entire mesa structure, also covering the sidewalls of the Ge-rich layer (see Figure 5.8(d)), possibly due to Si surface diffusion from the neighboring regions. This passivation with a high-quality thermal oxide should therefore prevent a degradation and oxidation of the Ge layer, resulting in nearly hysteresis-free I/V characteristics. Thus, it can be seen that the 8 nm thick Ge-rich layer remains intact without any signs of out-diffusion or intermixing with the other Si layers even after thermal treatments up to 1174 K.

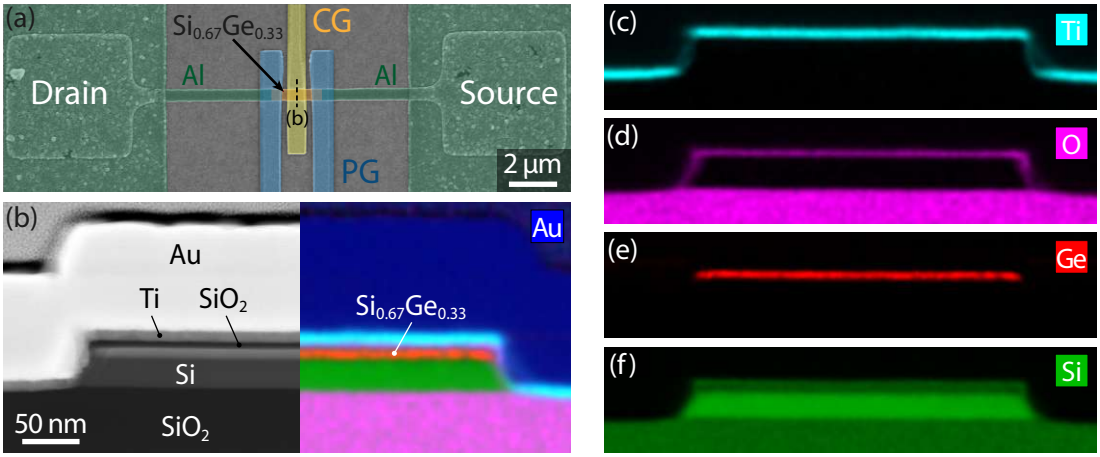

Figure 5.8: (a) Colored SEM image of a TTG RFET based on an Al-$Si_{0.67}Ge_{0.33}$-Al heterostructure. (b) Cross-sectional HRSTEM and EDX image of the gate stack. (c-f) Single elementary EDX maps.

The transfer characteristic of this TTG RFET with a $Si_{0.67}Ge_{0.33}$ channel ($L = 1.96\,\mu m$, $W = 460\,nm$) in Figure 5.9(a) shows a nearly hysteresis-free operation with highly symmetric on-states. At $V_{DS} = 2\,V$, high on-state currents of $I^n_{on} = 17.3\,\mu A$ (37.9 µA/µm) for the n-mode operation ($V_{PG} = 5\,V$) and $I^p_{on} = 33\,\mu A$ (72.2 µA/µm) in the p-mode ($V_{PG} = -5\,V$) are obtained. This results in a symmetry factor of $I^p_{on}/I^n_{on} = 1.9$, which is only a slightly higher asymmetry compared to the Si-based devices shown in Section 4.3. This device is therefore the first RFET containing diluted Ge in the channel, showing a hysteresis-free operation with a high level of symmetry and a strong S/D leakage suppression [LW11]. Compared to a reference SBFET with a single TG covering the entire Al-$Si_{0.67}Ge_{0.33}$-Al heterostructure, the on-state symmetry as well as the off-states could even be improved. The lowered off-state currents below 20 pA can be attributed to the electrostatic barrier

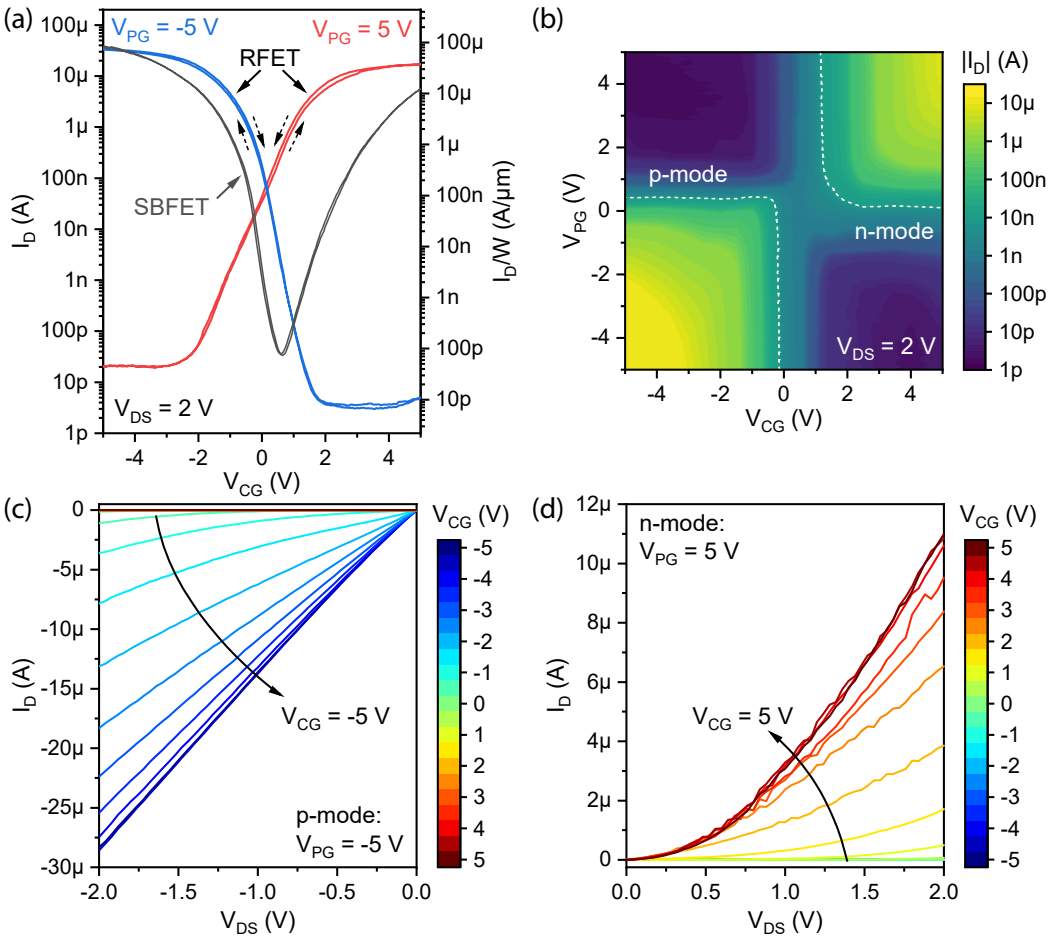

Figure 5.9: (a) Transfer characteristic of the TTG RFET with a $Si_{0.67}Ge_{0.33}$ channel and a 6 nm SiO_2 gate oxide, measured at $V_{DS} = 2\,V$ ($V_D = -V_S$). $L_{SiGe} = 1.96\,\mu m$, $W = 460\,nm$. The characteristic of a comparable SBFET with a single global TG is shown in gray. (b) Semi-logarithmic conduction map showing the current flow as a function of the gate voltages V_{PG} and V_{CG}. The dotted line at $I_D = 10\,nA$ indicates the n- and p-type operation windows. (c,d) Linear V_{CG}-dependent output characteristic for p- and n-mode at $V_{PG} = -5\,V$ and $5\,V$, respectively.

induced by the PGs, efficiently blocking the injection of undesired charge carriers. This results in high I_{on}/I_{off} current ratios of $\sim 1 \times 10^6$ and $\sim 2 \times 10^7$ for n- and p-mode, respectively. The extracted subthreshold slopes with $S_{th}^n = 510\,\mathrm{mV/dec}$ and $S_{th}^p = 235\,\mathrm{mV/dec}$, as well as the threshold voltages with $V_{th}^n = 0.96\,\mathrm{V}$ and $V_{th}^p = -0.4\,\mathrm{V}$, further show a slightly p-favored behavior, presumably due to slightly lower carrier injection barriers for holes. However, we speculate that the Al-Si-$Si_{0.67}Ge_{0.33}$ heterojunctions formed during the Al-Si/Ge exchange reaction for the S/D contact formation (see Figure 5.2) play an important role in reducing the Fermi level pinning towards the VB, which would otherwise presumably lead to very asymmetric device behavior as seen in other Ge-based RFETs [37, 38].

The conduction map in Figure 5.9(b) shows the polarity control of the fabricated $Si_{0.67}Ge_{0.33}$-RFET to derive the ideal operating parameters. By varying the voltage on the PG, the injection barriers are modulated, with a transition between n- and p-mode conduction. Thereby, two large operation regimes are evident that are slightly shifted towards positive gate voltages, meaning that higher PG voltages are required to achieve the same current values for n-mode. Nevertheless, this plot further demonstrates the stable and widely symmetric operability of the device. The slight asymmetry of the two operation modes is also evident in the output characteristics in Figure 5.9(c,d). For the p-mode at $V_{PG} = -5\,\mathrm{V}$, a linear behavior in the I/V characteristic is obtained for negative V_{CG} approaching $-5\,\mathrm{V}$, indicating a transparent, quasi-ohmic Al-Si-$Si_{0.67}Ge_{0.33}$ junction. In contrast, a lower current flow with a clear nonlinear increase with V_{DS} is obtained in the n-mode ($V_{PG} = 5\,\mathrm{V}$) for all values of V_{CG}, indicating a dedicated Schottky barrier for the injection of electrons.

In order to obtain more precise information about the transport properties of the structures, temperature-dependent measurements were performed. Figure 5.10(a) shows the stable device operation measured up to 400 K. In particular, the off-currents increase strongly with temperature, by more than two orders of magnitude for the n-mode. This is attributed to the large increase in thermionic emission, where thermally activated carriers are passing the blocking barrier. In addition, a temperature-dependent fanning of the subthreshold region is observed due to an increased rate of thermally assisted tunneling. The on-state currents are not that strongly affected by the temperature, leading to a general decrease in the I_{on}/I_{off} ratio, consistent with the thermionic emission theory [116]. While a slight increase in on-currents in the n-mode is evident, a slight but reproducible reduction of the p-mode currents is observed. This is another indication of a highly transparent junction for holes, where the on-state resistance is mainly defined by scattering rather than the injection through a barrier. The extraction of the activation energies E_a in Figure 5.10(b) also shows the high transparency of the holes in the on-region of the p-mode. Clearly negative and widely constant E_a values are obtained for $V_{CG} < 0\,\mathrm{V}$, allowing an efficient hole injection. This region is even extending towards $V_{CG} = 1\,\mathrm{V}$ for higher bias voltages V_{DS} due to a stronger energy band bending. The off-state region on the other side shows a clear Schottky barrier, with E_a values up to 0.5 eV, efficiently blocking the undesired charge carriers (electrons). For the n-mode in Figure 5.10(c), positive E_a val-

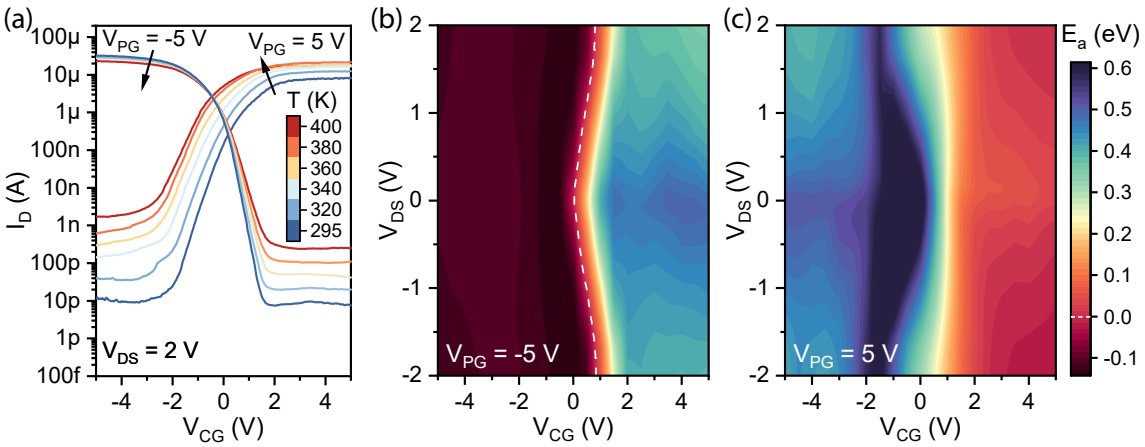

Figure 5.10: (a) Temperature-dependent transfer characteristic of the $Si_{0.67}Ge_{0.33}$-RFET from Figure 5.9, in the range from 295 K to 400 K at $V_{DS} = 2$ V. (b,c) Activation energy maps for p- and n-mode. The dashed line at $E_a = 0$ eV indicates the transition to a transparent junction.

ues close to 0 eV are reached in the on-state for $V_{CG} > 1$ V. However, in contrast to the p-mode, full transparency cannot be achieved, leaving a small remaining injection barrier, presumably due to slightly off-center Fermi level pinning. This leads to a weaker n-mode, with a nonlinear I_D/V_{DS} characteristic typical for SBFETs (see Figure 5.9(d)). Thus, the high symmetry of both activation energy maps with respect to the applied bias voltage V_{DS} indicates identical charge carrier injection from both source and drain contacts, highlighting the stability of the Al-Si-$Si_{0.67}Ge_{0.33}$ heterojunction.

5.3.1 HfO_2 Gate Dielectric Integration

To further improve the electrostatic gating of the $Si_{0.67}Ge_{0.33}$-based RFETs, a 7.6 nm thick ALD-grown HfO_2 layer is incorporated into the gate stack. At the same time, the SiO_2 interface layer below the HfO_2, thermally grown from the Si cap of the vertical Si-$Si_{0.67}Ge_{0.33}$-Si heterostructure, was reduced to 2.5 nm by shortening the oxidation time to 1 min at 1173 K. This unusually thick interfacial oxide was chosen to be on the safe side of interface stability and to prevent the intermixing of Hf with $Si_{1-x}Ge_x$. Figure 5.11(a) shows the EDX analysis of the fabricated gate stack, with the Si-$Si_{0.67}Ge_{0.33}$ channel being covered by the SiO_2 interface layer and the HfO_2 layer, and the Ti/Au (10 nm/100 nm) gate stack on top. Additionally, the HRSTEM image in Figure 5.11(b) shows a close-up image of the sidewall coverage of the dielectric layers. Note that due to the short oxidation time of 1 min, resulting in a Si interface oxide thickness of ~2.5 nm, the initial 3 nm thick Si capping layer of the vertical Si-$Si_{0.67}Ge_{0.33}$-Si heterostructure may not be fully consumed.

With an estimated permittivity value of $\varepsilon_{HfO_2} = 20$ measured from capacitive test structures [284], and $\varepsilon_{SiO_2} = 3.9$, this adapted dielectric stack results in an EOT of 4 nm according to Equation 2.4. In addition to enhanced electrostatic gating, lower gate leakage currents should be achieved due to reduced tunneling effects and oxide defects, while

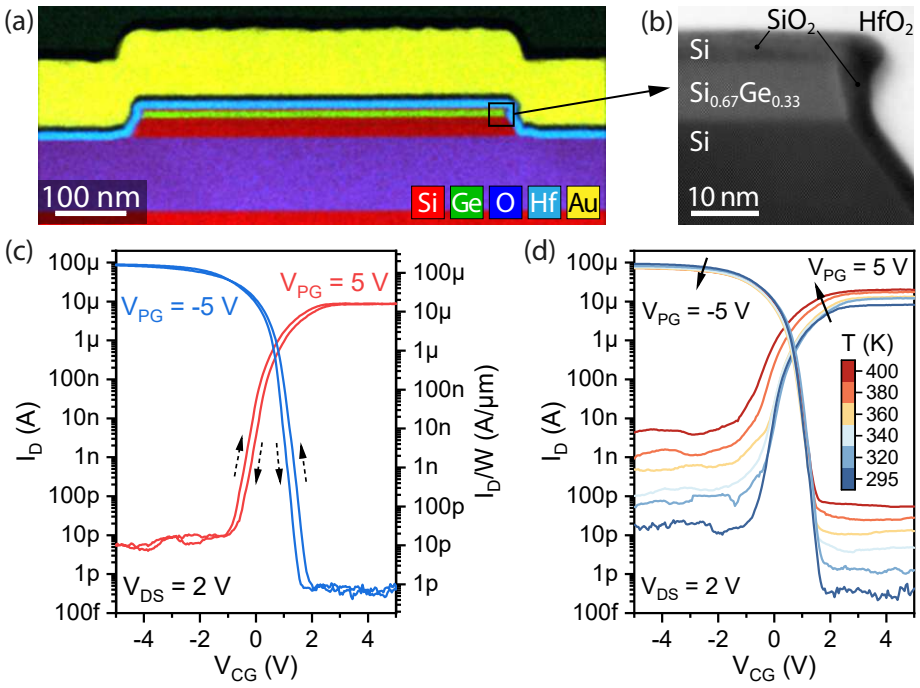

Figure 5.11: (a) EDX map showing the cut through the gate stack of the $Si_{0.67}Ge_{0.33}$ channel RFET with SiO_2 and HfO_2 gate dielectric. (b) Close-up HRSTEM image showing the sidewall of the vertical Si-$Si_{0.67}Ge_{0.33}$ channel passivated by the SiO_2 and HfO_2 layers. (c) Corresponding transfer characteristic of the RFET with $L_{SiGe} = 2.18\,\mu m$ and $W = 550\,nm$ at $V_{DS} = 2\,V$ ($V_D = -V_S$). V_{CG} is swept in both directions, with the arrows indicating the sweeping direction. (d) Temperature-dependent transfer characteristic between 295 K and 400 K. The arrows indicate the direction of the change in on-state current with temperature.

maintaining high stability against electrostatic breakdown [30, 90]. The resulting transfer characteristic of an RFET with a channel length $L_{SiGe} = 2.18\,\mu m$ and a width $W = 550\,nm$ in Figure 5.11(c) shows the stable operation for both operation modes at $V_{PG} = \pm 5\,V$. Thereby, most of the transistor properties could be improved with the adapted gate stack. Higher I_{on}/I_{off} current ratios (n: 3.4×10^6, p: 4.3×10^8) and steeper subthreshold slopes (n: 207 mV/dec, p: 115 mV/dec) for both modes are reached. Furthermore, the off-currents could be significantly reduced. However, an increased on-current asymmetry is induced, with I^p_{on}/I^n_{on} rising to 7.4. This can be explained by the fixed charges in the HfO_2 dielectric layer, inducing a shift of the transfer characteristic and thus the threshold voltages towards positive voltages [94, 285], with $V^n_{th} = 0.68\,V$ and $V^p_{th} = 0.15\,V$. These fixed charges also affect the electrostatic barriers at the metal-semiconductor junction below the PG, leading to more asymmetric charge carrier injection conditions. Furthermore, a slight increase in hysteresis can be observed compared to the SiO_2 sample. However, this is still comparatively small due to the good quality of the SiO_2 interfacial layer, which suppresses the formation of unstable Ge oxides or Ge indiffusion into the HfO_2 layer, which can otherwise lead to degradation and reliability issues [30, 129, 286].

The temperature-dependent transfer characteristic in 5.11(d) is comparable to the behavior of the devices with the SiO_2 gate dielectric, demonstrating that the adapted gate stack provides the same temperature stability. The on- and off-current changes are within the same range as before, again with a slight decrease of the p-mode on-state current at rising temperatures.

5.3.2 RFET Performance Comparison

To provide a better comparison of the non-volatile RFETs of this work, the transfer characteristics of an exemplary RFET of each of the different devices are shown in the same plot in Figure 5.12(a). Thereby, an SOI-based RFET with SiO_2 gate oxide is compared to the two different $Si_{0.67}Ge_{0.33}$ channel devices, with and without the integrated HfO_2 layer in the gate stack. The drain currents are thereby normalized to the channel width W of each device. It can be seen that the RFET with the pure Si channel reaches the best on-state symmetry, with $I^p_{on}/I^n_{on} \sim 1$. Incorporating Ge into the channel increases the on-state current in the p-mode, but reduces the current in the n-mode due to increased electron injection barriers caused by off-centered Fermi level pinning. This on-state asymmetry is even enhanced when integrating the HfO_2 layer into the dielectric gate stack due to fixed charges, which is also evident in the shift of the transfer characteristic towards positive gate voltages. Nevertheless, the HfO_2 RFET devices show significantly enhanced off-state

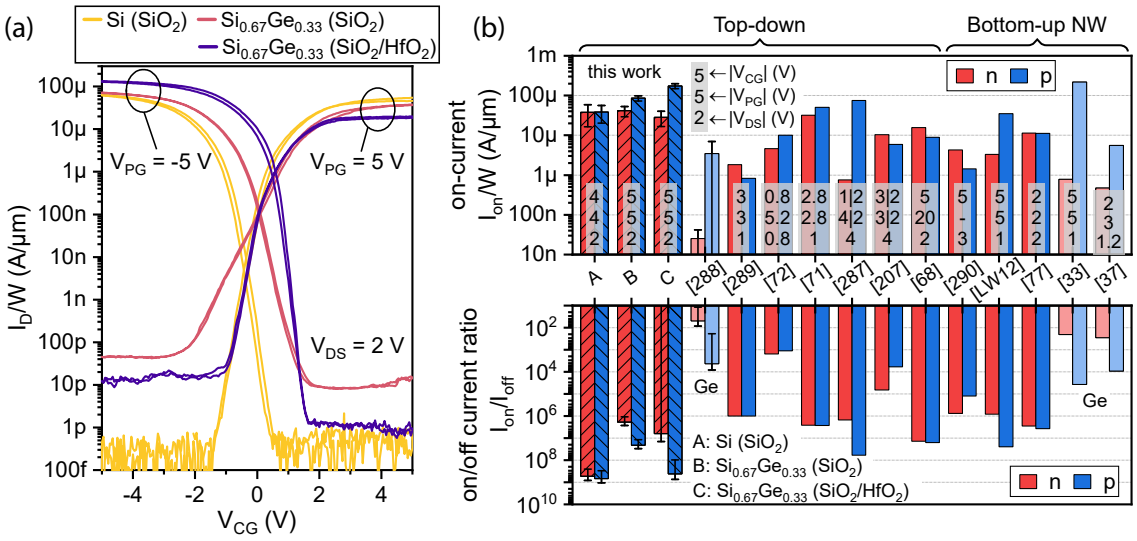

Figure 5.12: (a) Transfer characteristic comparison of the $Si_{0.67}Ge_{0.33}$-RFET with different gate stacks (SiO_2/HfO_2 (2.5 nm/7.6 nm) and SiO_2 (6 nm)) and the pure Si channel device with 10.3 nm SiO_2 gate oxide. All devices are measured under the same conditions, with $V_{DS} = 2\,V$ and $V_{PG} = \pm 5\,V$. (b) Comparison of the on-state currents I_{on}/W and on/off current ratios of the RFETs from this work (A-C) with RFETs from literature. The currents are normalized to the channel width W for top-down fabricated channel devices and to the channel diameter for bottom-up grown NW RFETs. The operation voltages of each device are indicated in the gray boxes. In [207, 287], different voltages are used for n- and p-mode operation. The RFETs in [33, 37, 288] use pure Ge as channel material.

currents, subthreshold slopes and threshold voltages for both operation modes compared to the $Si_{0.67}Ge_{0.33}$-channel device with the pure and thicker SiO_2 gate dielectric. This is due to the effective reduction of the EOT from 6 nm to 3.98 nm, leading to improved electrostatic control of the device. This also results in improved I_{on}/I_{off} ratios, with 6×10^6 and 4×10^8 for n- and p-type operation, respectively. However, the pure Si channel device reaches the highest on/off ratio, exceeding 5×10^8 for both modes. This is consistent with the thermionic emission theory, as the I_{on}/I_{off} ratio is generally expected to decrease for SBFETs with a smaller band gap channel material [116]. Interestingly, despite the thicker EOT of the Si RFETs, similar (or even steeper in p-mode) subthreshold slopes are achieved. This can be explained by the thinner device layer of the Si RFETs (16.4 nm instead of a total of 43 nm for the $Si_{0.67}Ge_{0.33}$ channel), which nevertheless significantly reduces the screening length λ (see Equation 2.24) and results in increased gating efficiency.

To put the results of this work into perspective, a comparison of the on-state currents as well as the on/off current ratios with other state-of-the-art RFETs from the literature is shown in Figure 5.12(b). Furthermore, an extended set of performance metrics for some selected Si, $Si_{1-x}Ge_x$ and Ge-based RFETs are summarized in Table 5.2. For the extraction of the performance parameters of the RFETs in this work, the mean values and standard deviation of ten comparable devices were evaluated. Among the compared RFETs, only the VLS-grown Si-NWs in a $NiSi_2$-Si platform by Heinzig et al. [77], with $I^p_{on}/I^n_{on} = 0.98\pm0.22$, achieve symmetry values comparable to the Al-Si-Al heterostructure-based RFETs. However, there a complex radially compressive stress of $\sim$1 % is required. In addition, the RFETs from this work exhibit exceptionally high on-currents I_{on}/W and the highest on/off ratios. The introduction of Ge as a channel material leads to enhanced on-currents, especially for the p-mode, with the highest p-type current reached by Sistani et al. [33] in Ge NW RFETs. There, the Ge channel even allows for an additional operation mode of the RFET by utilizing the NDR effect. However, these RFETs, as well as the other pure Ge channel devices, exhibit strongly asymmetric behavior due to strong Fermi level pinning, as well as significantly increased off-currents. In contrast, the RFETs based on the Al-Si-$Si_{0.67}Ge_{0.33}$ multi-heterojunction show a comparatively good symmetry. With a scaled semiconductor channel and an optimized omega-gate geometry, Simon et al. [71] showed improved Si RFETs with subthreshold slopes in the range of the Al-Si and Al-$Si_{0.67}Ge_{0.33}$-based (HfO_2) devices, although only utilizing a dual top gate approach. Zhang et al. [287] even achieved sub-60 mV/dec operation (down to 6 mV/dec) in FinFETs, utilizing special gating conditions in a three independent top gate architecture, impact ionization and positive feedback effects.

	Al-Si	Al-$Si_{0.67}Ge_{0.33}$	Al-$Si_{0.67}Ge_{0.33}$	Al-Ge [288]	$NiSi_2$-Si [71]	Al-Si [LW12]	$NiSi_2$-Si [77]	Al-Ge [33]	Ni_2Ge-Ge [37]
Platform	SOI	SiGe on SOI	SiGe on SOI	GeOI	SOI	Si NW	Si NW	Ge NW	Ge NW
Si|Ge layer (nm)	16.4	35 | 8	35 | 8	20	3.5	80	12	30	18
Oxide	SiO_2	SiO_2	SiO_2|HfO_2	Al_2O_3	SiO_2	SiO_2	SiO_2	Al_2O_3	GeO_x|Al_2O_3
Thickness (nm)	10.3	6	2.5 | 7.6	11	6.5	8.5-9.7	8	22	7
ε_r	3.9	3.9	3.9 | 20	9.31	3.9	3.9	3.9	9.31	≈ 9
EOT (nm)	10.3	6	3.98	4.6	6.5	8.5-9.7	8	9.2	3
I^n_{on}/W (µA/µm)	37.6	41.3	28.4	0.025	32.3	3.3	11.4	0.778	0.47
I^p_{on}/W (µA/µm)	38.4	85.7	174.4	3.48	50.2	35	11.17	216.8	5.56
I^n_{off}/W (µA/µm)	7.6×10^{-8}	2.4×10^{-5}	1×10^{-5}	5.5×10^{-4}	1.2×10^{-5}	4×10^{-6}	4×10^{-6}	3.8×10^{-3}	1.7×10^{-3}
I^p_{off}/W (µA/µm)	5.9×10^{-8}	4.4×10^{-6}	9.9×10^{-7}	7.6×10^{-4}	1.9×10^{-6}	1.4×10^{-6}	3×10^{-6}	5.9×10^{-3}	6×10^{-4}
$I^p_{on}/\ I^n_{on}$	1.054	2.2	6.66	125	1.56	10.6	0.98	279	11.8
$I^n_{on}/\ I^n_{off}$	5.4×10^{8}	1.9×10^{6}	6.2×10^{6}	48.6	2.6×10^{6}	8.3×10^{5}	2.86×10^{6}	210	280
$I^p_{on}/\ I^p_{off}$	6.8×10^{8}	2.1×10^{7}	4.2×10^{8}	4270	2.7×10^{6}	2.5×10^{7}	3.72×10^{6}	3.68×10^{4}	9300
V^n_{th} (V)	0.51	0.79	0.67	1.57		0.36	1.42	1	0.4
V^p_{th} (V)	-1.14	-0.36	-0.02	0.04		-0.72	-1.41	-1.4	-0.2
S^n_{th} (mV/dec)	144.3	436	207	1233	142	280	150	800	215
S^p_{th} (mV/dec)	142.6	245	121	835	128	289	150	700	150

Table 5.2: Characteristic RFET performance metrics of different RFETs. The SOI and $Si_{0.67}Ge_{0.33}$ channel RFETs from this work and are compared with state-of-the-art devices from literature.
Top-down nanosheet structures: currents normalized to sheet width W. Bottom-up NW structures: currents normalized to wire diameter.

Chapter 6

Non-Volatile Transistors based on Ferroelectric HZO Gate

In the previous chapters, the implementation of RFETs based on Al-Si-Al and Al-$Si_{0.67}Ge_{0.33}$-Al heterostructures was demonstrated, achieving highly symmetric and runtime reconfigurable n- and p-type characteristics that can be switched at runtime by applying a constant positive or negative potential to the PG. Their potential was further demonstrated by their integration into complementary, combinational logic gates with significantly reduced transistor count. For many circuit applications, however, it would be beneficial if the programming of this state could be stored over a longer period of time without the need to apply a permanent potential to the PGs. In particular, such a non-volatile, reconfigurable device could be an important building block for neuromorphic computing approaches [48, 83] and LiM architectures [42].

In this regard, $Hf_{0.5}Zr_{0.5}O_2$ (HZO) layers in their orthorhombic phase have already shown promising results regarding their ability to maintain their ferroelectric polarization with its induced electric field over long periods of time. Furthermore, it is highly scalable, reliable and CMOS compatible, making it promising for large-scale integration [138, 223].

Therefore, this chapter focuses on the integration of a ferroelectric HZO layer into the gate stack of the RFET, specifically localized below the PG contact, to allow non-volatile switching of the device between n- and p-type operation. To reduce the complexity, the devices are based on the simpler Al-Si-Al heterostructures patterned from SOI substrates from Chapter 4. The data and discussion in this chapter are primarily based on the author's work in [LW1][LWC5, LWC10].

6.1 Optimization of the Ferroelectric Gate Stack

Before integrating the HZO ferroelectric layer into transistor structures, circular capacitor test structures are fabricated to find the optimal deposition parameters and material combinations to maximize remnant polarization and device reliability. In Figure 6.1, the ferroelectric response of the HZO layers of different layer thicknesses is tested within a metal-ferroelectric-metal (MFM) capacitor structure. As top and bottom electrodes, a TiN layer is deposited by reactive Ti sputtering in N_2 plasma. The MFM structures were then annealed via RTA at 723 K in N_2 atmosphere for 2 min, where the stress induced by the TiN electrodes at the elevated temperature induces the targeted crystallization of the HZO. Capacitance-voltage (C/V) measurements on both test structures thereby show a clear counterclockwise hysteresis in Figure 6.1(a), indicating ferroelectric behavior. Annealing tests at lower temperatures (e.g., 673 K) have yielded significantly reduced or even a non-ferroelectric response. The increase of the layer thickness thereby results in decreased capacity values for the red curve, according to the capacitor Equation 3.8. The symmetrical shape of the butterfly loop, as well as the position of the peak capacitance values and the crossing points of the curves in the different measurement directions are largely identical. A slight shift of the characteristic towards negative voltages of about $-0.14\,\mathrm{MV/cm}$ is evident, resulting in a slightly asymmetric switching of the two polarization states. For the 8 nm HZO sample, the peak capacitance values of $4.8\,\mu\mathrm{F/cm^2}$ and $4.76\,\mu\mathrm{F/cm^2}$ are reached at electric fields of $0.75\,\mathrm{MV/cm}$ and $-0.88\,\mathrm{MV/cm}$, respectively. A minimum capacitance of $\sim 3.3\,\mu\mathrm{F/cm^2}$ at $E = \pm 3\,\mathrm{MV/cm}$ is extracted. According to Equation 3.8, the dielectric constant ε_r can be estimated, varying between 30 and 43, which is in the range of values found in the literature [137].

The polarization hysteresis curves in Figure 6.1(b), extracted from the Sawyer-Tower circuit measurements, provide further insights of the ferroelectric switching behavior. Thereby, a higher remnant polarization of $P_r = 21.4\,\mu\mathrm{C/cm^2}$ is achieved for the 8 nm

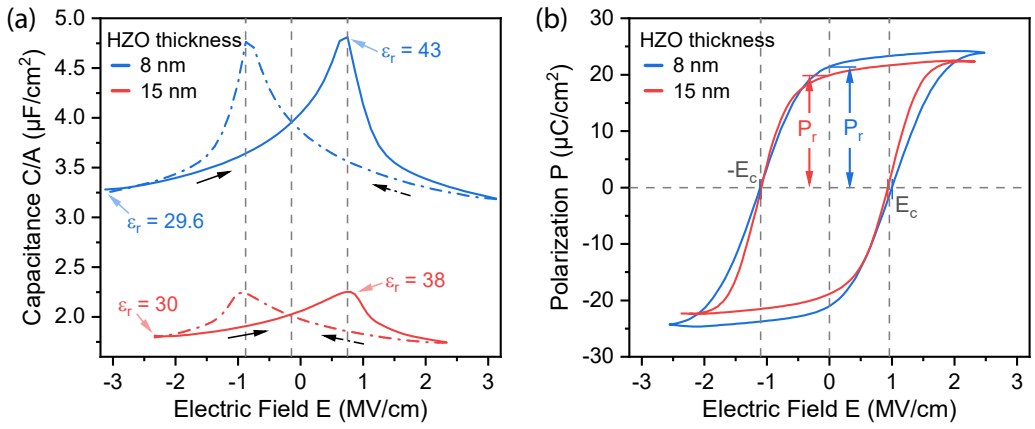

Figure 6.1: Comparison of the C/V characteristic (a) and the polarization curves (b) of two MFM structures with different HZO layer thicknesses of 8 nm and 15 nm. The HZO layer is embedded between two TiN electrodes in a circular capacitor structure.

thin HZO layer compared to 19.9 µC/cm^2 for the 15 nm layer. This is in accordance with results from literature, where it was also shown that for HZO layers thicker than 10 nm, the remnant polarization is reduced due to an increased fraction of the non-ferroelectric monoclinic phase[149,157,291]. The coercive field of both MFM structures is very similar, with $E_c \sim 0.96$ MV/cm and -1.1 MV/cm. The values obtained for residual polarization and coercive field of these MFM test structures are within the expected range or even slightly above average compared to the values found in the literature [135].

For device integration of the ferroelectric stack into an SBFET, it is of utmost importance to have a high-quality interface of the HZO layer to the Si channel with the low interface trap density. First of all, a high interface trap density could drastically degrade the device performance by reducing carrier mobilities and inducing unwanted hysteresis. Second, high voltage pulses used to switch the polarization states can access deep-level trap states, charging the device for a long period. Since the electric field induced by charge trapping always acts in the opposite direction to that induced by the ferroelectric, its effect on the underlying semiconductor channel can be reduced or even completely suppressed.

For this purpose, metal-ferroelectric-insulator-semiconductor (MFIS) capacitor structures with different interface layers (IL) were fabricated and compared. A highly n-doped Si substrate (P, $\sim 10^{21}$ cm^{-3}) is thereby used as the base substrate, where either a 2.5 nm thermally grown SiO_2, a 0.9 nm thin chemically grown SiO_2 (RCA2), or a 2 nm ALD-grown HfO_2 layer was deposited, followed by a 10 nm thick HZO layer and a Pd electrode on top. The Pd electrodes were used initially due to an unavailability of the TiN process. Both the thin chemical SiO_2 and the HfO_2 IL show a clear counterclockwise hysteresis indicating ferroelectricity. The thicker thermal oxide, on the other hand, shows clockwise hysteresis, a clear sign of trapping-induced behavior that completely obscures the ferroelectric polarization. As the thickness of the thermally grown SiO_2 IL is larger than for the chemically grown one, the total capacitance drops due to the thicker total insulator stack. Although the thickness of the HfO_2 layer with 2 nm is also increased, its higher permittivity ($\varepsilon_r = 20$ [284]) results in an EOT of only $\sim$0.4 nm, resulting in capacitance values similar to the chemical oxide. Furthermore, due to the voltage drop at the dielectric IL, the effective voltage applied to the HZO layer is reduced according to [232]

$$V_{HZO} = V_{tot}\,\frac{C_{tot}}{C_{HZO}} = V_{tot}\,\frac{t_{HZO}\,\varepsilon_{IL}}{t_{HZO}\,\varepsilon_{IL} + t_{IL}\,\varepsilon_{HZO}}. \tag{6.1}$$

While for HfO_2 and the chemical SiO_2 IL MFIS structures, 77 % and 59 % of the total voltage (V_{tot}) is applied to the HZO layer, less than 35 % of the voltage remains for the thermal SiO_2 layer. This is an important aspect that needs to be considered for the device operation and the switching between the polarity states. Furthermore, implemented in an SBFET, the larger voltage drop on the thicker IL would also reduce the influence of the remnant polarization of the HZO layer on the semiconductor channel or the metal-semiconductor interface below, significantly reducing the memory window [229]. An IL that is too thick can also strongly block charge tunneling. Since a moderate level of traps near the HZO are

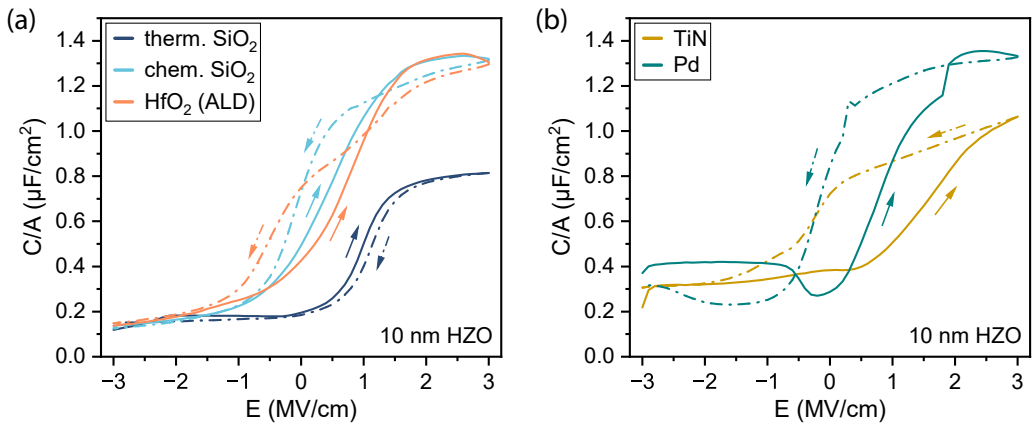

Figure 6.2: (a) C/V characterization of MFIS test structures measured at $f = 100\,\text{kHz}$ comparing different dielectric interface layers between the Si substrate and the 10 nm thick HZO layer with a Pd top electrode. The structures with the chemically grown SiO_2 (0.9 nm) and ALD-grown HfO_2 (2 nm) interface layers show a counterclockwise hysteresis indicating ferroelectric behavior, while the thermally grown SiO_2 (2.5 nm) shows a trap-dominated behavior. (b) Comparison of the MFIS structures with TiN and Pd top electrodes, with a chemically grown SiO_2 interface layer.

crucial for stabilizing the ferroelectric polarization, a low level of trapped charges can thus lead to poor switching behavior [233]. Note that also for the HfO_2-MFIS structure, a thin native SiO_x IL is expected to be present between the ALD-grown HfO_2 and the Si surface, effectively increasing the EOT of the sample. Although a slightly higher ferroelectric-induced hysteresis is achieved with the HfO_2 IL, the MFIS structures with the chemically grown SiO_2 layer exhibited a higher yield with more reproducible ferroelectric behavior. Furthermore, an improved interface to the Si channel is expected, which is why this stack was chosen for the first samples to integrate the HZO layer into SOI-based SBFETs.

As the choice of the top gate material can strongly influence the ferroelectric behavior as well as other electrical device properties, MFIS capacitor structures with commonly used TiN (sputtered) and Pd (evaporated) top metal contacts were examined. Both samples use the previously tested thin, chemically grown SiO_2 IL on the highly n-doped Si substrate. Both MFIS structures show a large counterclockwise hysteresis indicating ferroelectric behavior, with the TiN sample achieving a larger coercive field. Differences in the metal work functions of both Pd and TiN lead to shifted C/V characteristics [150]. The higher measured capacitance for the Pd MFIS sample relates to a higher permittivity ε_r of the HZO. This could indicate that a higher fraction of the HZO layer remained in the centrosymmetric tetragonal phase instead of the orthorhombic phase after the crystallization step, resulting in an overall weaker ferroelectric response [154]. The lower TiN capacitance could also be an indication for the formation of a thin TiO_xN_y layer between the TiN and the HZO surface. The existence of this serial capacitance would then also result in a reduction of the overall capacitance. Since TiN showed slightly better results and is a very common electrode material for HZO devices in literature, TiN was used for the integration in SBFETs.

6.2 HZO Integration in Al-Si SBFETs

Based on the previously shown Al-Si-Al heterostructures on SOI substrate, the classical gate dielectric is now replaced by an HZO-based stack to realize non-volatile transistors. This gate stack consists of a 0.9 nm thin chemical SiO_2 interface layer grown on the Si mesa structures, the 8.5 nm ALD-grown HZO and the 50 nm thick TiN top gate electrode. The fabrication process flow for the integration of the HZO had to be adapted, with the annealing process to induce the thermal Al-Si exchange reaction being carried out after the deposition of the top gate electrode (see Section 3.1.3). Simultaneously with the exchange, the HZO layer is crystallized to induce the ferroelectric, orthorhombic phase exclusively under the TiN gate region. The HZO region, which is not in contact with the TiN top gate electrode, remains in a non-ferroelectric phase, acting as a trivial linear dielectric. As the 50 nm thin TiN gate is semi-transparent, the underlying Al-Si-Al heterostructure with a Si channel length of ∼2.5 µm is well visible in the optical microscope image in Figure 6.3(a). The schematic of the Al-Si SBFET with the ferroelectric gate stack is shown in Figure 6.3(b).

When operating the device in a low V_{TG} range between −1 V and 1 V, without triggering the overall dominating remnant polarization of the HZO layer, an ambipolar transfer characteristic with a predominant p-type current ($I^p_{on}/I^n_{on} > 67$) is obtained (see Figure 6.3(c)). Furthermore, the whole characteristic is shifted towards positive V_{TG}. This may be an indication for fixed charges from the HZO layer integration, resulting also in asymmetric injection barriers for electrons and holes. A small clockwise hysteresis is evident when sweeping the TG voltage, indicating minor trap-based charging effects. Remarkably steep subthreshold slopes of 70 mV/dec for the p-branch (and up to 82 mV/dec for the n-branch)

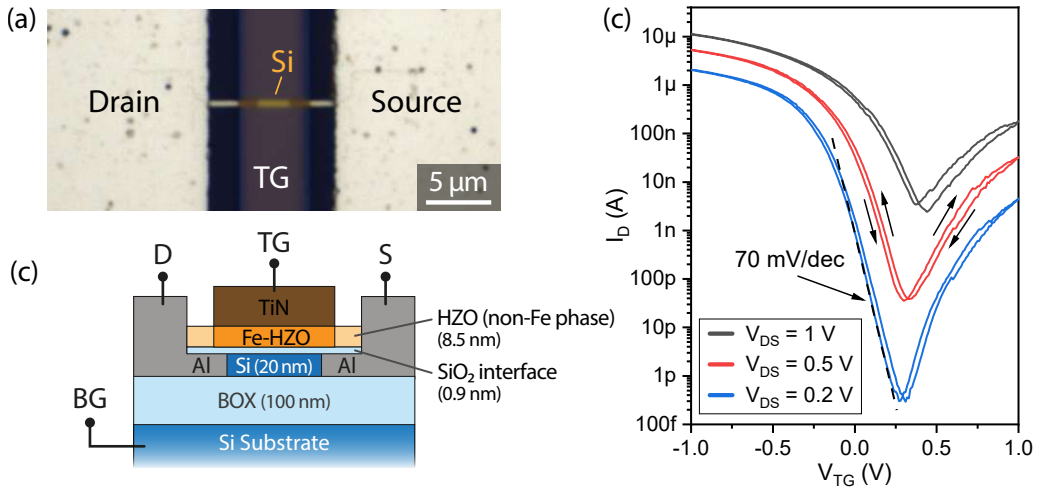

Figure 6.3: (a) Optical microscope image of the SBFET with integrated ferroelectric HZO gate stack. The fully covered Al-Si-Al heterostructure is visible underneath the semi-transparent TiN top gate. (b) Schematic gate stack of the FeSBFET. (c) Transfer characteristic of the device at different bias voltages V_{DS} ($V_D = -V_S$). Device dimensions: $L_{Si} = 2.65$ µm, $W = 450$ nm.

are achieved at low bias operation of $V_{DS} = 200\,\text{mV}$ over several orders of magnitude, approaching the conventional Boltzmann limit of 60 mV/dec at room temperature. This is much steeper than the other devices studied above. This is enabled by the low thickness of the chemical SiO_2 IL and the high permittivity of the HZO ($\varepsilon_{HZO} \geq 30$), resulting in an EOT of only $\sim$2 nm.

To exploit the non-volatile properties of this SBFET, high voltage pulses are applied to the top gate electrode to polarize the orthorhombically crystallized HZO. In Figure 6.4, the FeSBFET is operated in two different ways, with the operating sequence schematically shown above the corresponding transfer characteristic. The SET operation for aligning the ferroelectric domains and inducing ferroelectric polarization is the same for both methods. Thereby, an alternating pulse sequence, with two SET pulses (V_{set}) and a RESET pulse ($V_{reset} = -V_{set}$) in between, is applied on the TG, with a pulse duration of $t_{pulse} = 0.5\,\text{ms}$, while the other terminals (V_D, V_S, V_{BG}) are fixed at 0 V. A pulse voltage of $V_{set} = 4\,\text{V}$ and $-4\,\text{V}$ is used to switch between two polarization states of the HZO. For the READ operation in Figure 6.4(a), the TG voltage (V_{TG}) is swept between $\pm 1\,\text{V}$ while measuring the current flow through the device (I_D) at a bias voltage of $V_{DS} = 0.5\,\text{V}$. When a positive pulse of 4 V is applied for the SET pulse, the n-type current at $V_{TG} = 1\,\text{V}$ is increased

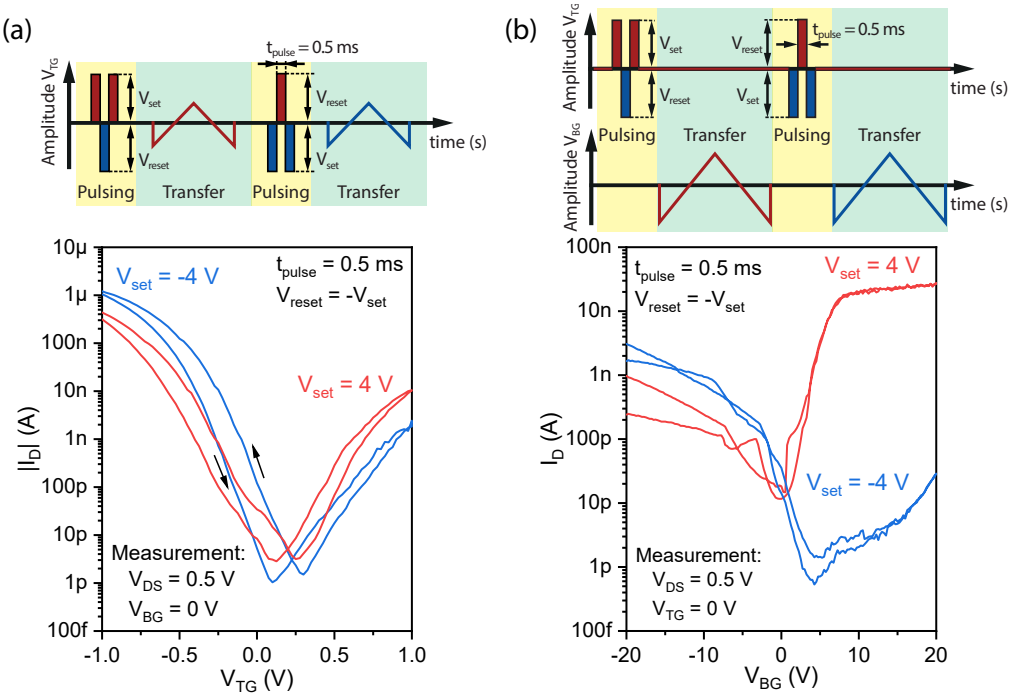

Figure 6.4: Pulsing scheme and transfer characteristic of the single gated FeSBFET from Figure 6.3. In (a), pulsing at $\pm 4\,\text{V}$ to set the ferroelectric polarization and modulation to measure the transfer characteristic (bidirectional between $\pm 1\,\text{V}$) is conducted via the TG. In (b) the current is modulated via the BG between $\pm 20\,\text{V}$. The same amplitude is used for the SET and RESET pulses, with $V_{set} = -V_{reset}$.

up to 10.4 nA, while the p-type current at $V_{TG} = 1\,\mathrm{V}$ is lowered to 400 nA. Switching to the opposite polarization via $V_{set} = -4\,\mathrm{V}$ causes the currents to change in the opposite direction, with a reduction in the n-mode (1.8 nA) and an increase in the p-type currents (1.2 µA). The change of the on-currents for both branches is relatively low and, with less than one order of magnitude. Furthermore, a slight shift of the subthreshold characteristic is evident, with a shift of the threshold voltages (V_{th}^{p}) of ∼110 mV. The direction of the shifts, both of the on-state currents as well as the threshold voltage shift, are a clear indication of predominant ferroelectric behavior rather than charge trapping-related effects. A positive SET pulse creates a dipole formation of the aligned ferroelectric domains with a net positive electric charge, especially close to the Al-Si Schottky barrier, lowering the injection barrier for electrons (and raising the barrier for holes). The negative SET pulse has the opposite effect, with a net negative charge towards the Al-Si-Al heterostructure, enhancing hole conduction and attenuating electron-induced currents. A residual electric field induced by charge trapping would result in changes in the reversed direction. However, a significant hysteresis is evident when changing the sweeping direction during the transfer measurement via the TG. This can be partly attributed to charged trap states, but also to a certain depolarization of the HZO layer due to the superposition of the gate potential during the characterization of the device. Due to this superposition of the electric field of the TG during the READ operation, and possible trapping effects screening the ferroelectrically induced field, the ferroelectric polarization shifts are rather weak.

A significantly increased ferroelectric response is achieved when the BG is used for the READ operation in Figure 6.4(b). The TG voltage is set to 0 V when measuring the transfer characteristic, whereby only the remnant electric field of the polarized HZO acts on the adjacent Al-Si-Al heterostructure from above. Thereby, a clear transition between a dominant n-type and p-type characteristic is evident when applying the pulsing sequence for $V_{set} = 4\,\mathrm{V}$ and $-4\,\mathrm{V}$, respectively. The ambipolar SBFET turns into a unipolar device, as programmed in a non-volatile manner by the TG pulse. Although the globally applied BG voltage affects the whole device, including the Al-Si interface region, its effect on the polarization of the HZO layer should be negligible due to the large thickness of the BOX of 100 nm. Therefore, the reduced influence of the BG on the HZO layer prevents its partial depolarization during the measurement, resulting in a significantly larger difference between the two states. While the current changes in the p-branch are still less than one order of magnitude, the on-currents in the n-branch (at $V_{BG} = 20\,\mathrm{V}$) increase by a factor of $\sim 10^3$ from 28.7 pA to 27.6 nA. Operating the FeSBFET in that regime could already be promising for memory applications. However, the current flow in both states is rather low. Presumably, the ferroelectric domains are aligned only in the vicinity of the Al lead and the Al-Si interface, where the electric field (from $V_{TG} - V_D$ or $V_{TG} - V_S$) is strongest, especially since the S/D contacts are metallic compared to conventional FeFETs. It can be speculated that, as the electric potential drops across the low-doped Si channel due to its high resistivity, the electric field applied to the HZO layer is reduced and eventually not strong enough to polarize the HZO. Therefore, there is no remnant electric field over large parts of the channel, which is only influenced by the 0 V from the TG during the measurement.

6.3 HZO-enhanced RFET

To further prove the non-volatile tunability of the injection junction, this approach of the ferroelectric gate stack is transferred to RFETs, thus realizing ferroelectric RFETs (FeRFETs). The structure of the TG electrode has been modified to cover only the area around the Al-Si junction, similar to the PG in previously shown RFET structures. Large parts of the Si channel thereby remain ungated from the top, only being modulated by the BG acting as the CG. The microscope image of an FeRFET is shown in Figure 6.5(a), with a close-up inset showing the Al-Si interfaces underneath the semi-transparent TiN PG. The HZO layer is only crystallized underneath the PG, where its remnant polarization in the vicinity of the Al-Si junction directly influences the injection barrier for electrons and holes. In the region between the two PG electrodes, which is used to modulate the current flow through the Si channel, the HZO remains in a linear dielectric phase, resulting in hysteresis-free current modulation independent of the measurement direction.

When operating the device with static PG voltages in Figure 6.5(b), a highly p-dominant characteristic is obtained, strongly shifted towards higher positive V_{BG}. Even at $V_{PG} = 0\,\mathrm{V}$, a high p-type current up to 376 nA at $V_{DS} = 0.5\,\mathrm{V}$ is reached, while almost no electron-induced current is measured. This dominant p-type behavior can be explained by the presence of negative fixed charges in the HZO layer, which is a well-known effect in high-κ/Si systems [118,292,293]. These fixed charges affect both the semiconductor channel, leading to a threshold voltage shift towards positive V_{BG}, and the Al-Si Schottky barriers, where upward band bending leads to preferential hole injection. In the case of Hf- and Zr-based oxides, most traps are associated with defects in the crystal structure, often caused by oxygen vacancies or interstitials [230, 294]. Since the trap levels due to oxygen vacancies are calculated to lie close to the Si VB edge, they may be the main source for charge trapping [295]. The oxygen interstitials, on the other hand, are located deep below the Si valence band edge and therefore do not act directly as carrier traps but could also act as a source of negative fixed charges [294, 295]. Setting V_{PG} to $-2\,\mathrm{V}$ further enhances the p-mode, increasing the on-currents to 7.8 µA and suppressing electron conduction for lowered off-currents <1 pA. At $V_{PG} = 2\,\mathrm{V}$, a distinct n-mode with well-suppressed off-currents in the low pA region is obtained, but the on-state currents at 27 nA are more than two orders of magnitude lower than for the p-mode.

To utilize the non-volatile properties of the ferroelectric gate stack, the same pulsing scheme as before for the globally gated FeSBFET (see Figure 6.4(b)) is applied to the TG (PG) to polarize the HZO underneath during the SET operation, with the BG (as the CG of the FeRFET) used to modulate the current flow during the READ operation. The voltages for the SET and RESET pulses were optimized to maximize the ferroelectric response, with the largest difference between the two polarized modes. The n-mode uses a V_{set} of 4.5 V and a V_{reset} of $-3\,\mathrm{V}$, the p-mode is set with $V_{set} = -4.25\,\mathrm{V}$ and $V_{reset} = 4.5\,\mathrm{V}$. Higher positive voltage pulses are used for SET and RESET operations due to the right-shifted polarization characteristics of the HZO. As indicated in the schematic in Figure 6.5(c), the ferroelectric dipoles in the HZO layer are aligned underneath the PG in the

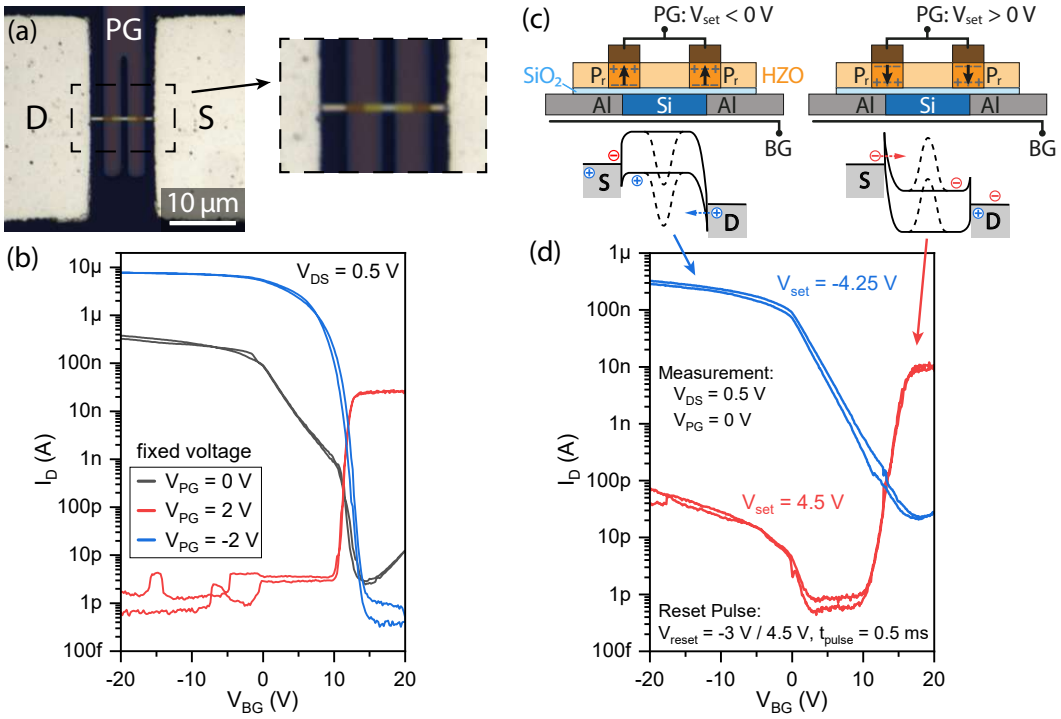

Figure 6.5: (a) Microscope image of the FeRFET, with the PG on top of the HZO covering the Al-Si interfaces, and the BG used as CG. (b) Transfer characteristic with constant potential applied to the PG, and the BG swept between ±20 V. (c) Schematic of the FeRFET with polarized HZO layer, including the energy band structure for both polarization states. (d) Transfer characteristic after applying the polarization sequence. For the n-mode (red), the PG is pulsed at $V_{set} = 4.5\,\text{V}$ and $V_{reset} = -3\,\text{V}$. The p-mode (blue) is set by $V_{set} = -4.25\,\text{V}$ and $V_{reset} = 4.5\,\text{V}$. Device dimensions: $L_{Si} = 4.1\,\mu\text{m}$, $W = 450\,\text{nm}$.

vicinity of the Al-Si junctions, directly influencing the Schottky barriers with their remnant electric field, explicitly excluding the middle of the channel region. Negative pulsing thereby results in a net negative charge close to the interface, locally raising the energy bands and enabling effective tunneling of holes into the semiconductor channel, while the injection of electrons is suppressed. Positive pulsing results in the opposite behavior, with a net positive charge locally lowering the injection barriers, enabling electron-induced currents while impeding hole injection. The resulting transfer characteristic is measured by sweeping the BG between ±20 V, while V_{PG} is set to 0 V.

The READ operation in Figure 6.5(d) shows the non-volatile reconfigurability of the FeRFET. Both operation modes are solely determined by the previously applied pulse sequence and the thereby induced remnant polarization in the HZO layer, as V_{PG} is set to 0 V during the measurements. Although a significant asymmetry with respect to the on-currents, with $I^p_{on}/I^n_{on} \sim 30$, and the threshold voltages is evident, both modes show good controllability with clear polarity control, no hysteresis and high on/off ratios, making the device the first non-volatile programmable RFET at all and the first FeRFET shown to the best of our knowledge [LW1]. In particular, compared to the previously shown structures

with the global TG, a significant improvement is achieved because possible charges in the ferroelectric no longer screens the Si channel from the BG potential during the measurement. The current of the p-mode is tunable from 324 nA down to 28 pA over four orders of magnitude. The n-mode shows a lower on-state current of 10.6 nA, indicating a higher remaining injection barrier for electrons. Furthermore, the increase in off-currents from a minimum of less than 1 pA up to 73 pA with increasing negative V_{BG} is an indication that the remnant electric field at the Al-Si junction is not sufficient to fully inhibit hole injection. Considering only the current values at −20 V and 20 V, remarkable non-volatile current changes with factors of 4×10^3 and 3.8×10^2 are achieved. The clearly distinguishable states are also stable over a long period of time, as it will be shown later in Section 6.3.2. In order to improve the electrostatic control of the Si channel and to lower the operation voltages, an additional TG electrode in the non-ferroelectric HZO area between the two PG electrodes, acting as CG, could be deposited perspectively after the HZO crystallization step via RTA.

6.3.1 Non-Volatile Multi-level Operation

Testing the FeRFET with different pulse voltages reveals that stable intermediate states are present in addition to the two extreme polarization states shown above. Figure 6.6 shows the response of the device to increasingly positive (a-c) and negative (d-f) pulse voltages V_{set} applied on the PG. The semi-logarithmic color map representation shows the changes of the current flow I_D as a function of V_{set} in a more immediate way. Furthermore, the on-currents I^n and I^p at $V_{BG} = 20$ V and -20 V, respectively, are extracted in Figure 6.6(c,f) to illustrate the change of the polarity of the FeRFET. After each applied positive (or negative) SET pulse sequence, the device is reset to its initial p-type (n-type) state by applying a reset sequence with $V_{set} = -3$ V and $V_{reset} = 4.5$ V ($V_{set} = 4.5$ V and $V_{reset} = -3$ V). This ensures that the next higher pulse voltage level is not influenced by the previous one.

When increasing V_{set} from 1.5 V to 5 V in Figure 6.6(a-c), a clear transition from the p- to the n-mode is evident. First changes in the device characteristic are thereby visible when the pulse voltage is increased to 2.5 V, as first ferroelectric domains in the HZO layer gradually start to flip in the opposite direction, increasing the probability for electron injection and the blocking of holes at the Al-Si junction. This results in a progressive increase in the n-type on-current I^n and a decreasing p-type current I^p. In addition, because a mixture of both carrier types is injected into the Si channel, the ability of the BG to efficiently block current flow is reduced. At $V_{set} = 3$ V the n-type on-current I^n already reaches its maximum, indicating that the barrier cannot be further lowered for electrons. The I^n current levels of ∼10 nA achieved by the non-volatile pulsing operation are also in a similar range as those achieved by operation with a fixed, static V_{PG} voltage. On the other hand, I^p still decreases for higher pulse voltages up to 5 V, indicating that more and more ferroelectric dipoles can be aligned parallel to each other, in the direction of the electric field. As evident in Figure 6.6(c), the increase and suppression of the current flow follows an exponential trend with the applied pulse voltage V_{set}. Furthermore, it must

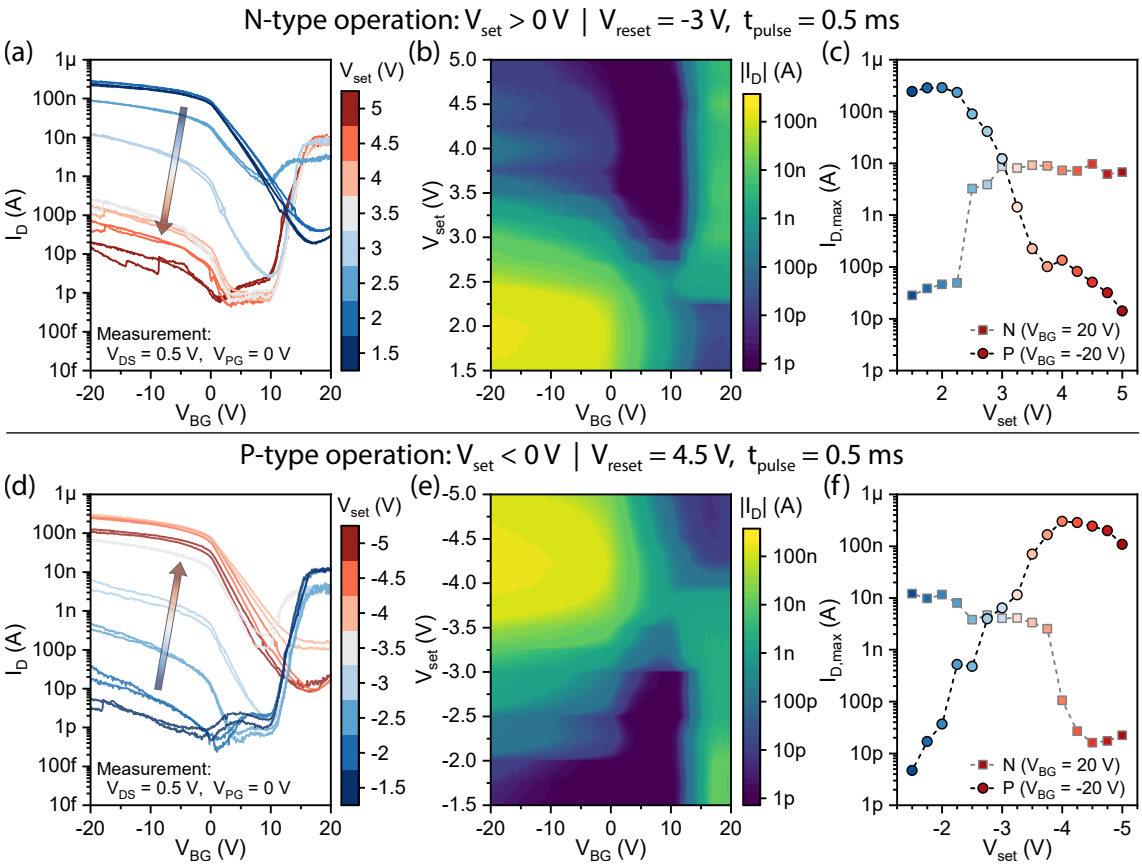

Figure 6.6: (a) Transfer characteristic of the FeFET from Figure 6.5 obtained after a variation of different positive pulse amplitudes between 1.5 V and 5 V for a transition to n-type operation. The reset pulse amplitude V_{reset} at −3 V is the same for all different V_{set} values. (b) Color map representation of the current flow depending on the pulse height V_{set} and the BG voltage. (c) Extracted n- and p-type currents measured at $V_{BG} = 20$ V and −20 V as a function of V_{set}. (d-f) Same type of plots for the transition to p-type operation, with the pulsing amplitude V_{set} increased from −1.5 V to −5 V and a constant V_{reset} of 4.5 V.

be noted that the pulsing at different voltage levels does not induce a significant horizontal shift of the characteristic, indicating only a local accumulation of the polarization charges in the vicinity of the Al-Si interface.

For the gradual transition from the n-mode to p-mode in Figure 6.6(d-f), the amplitude of the negative pulse voltage V_{set} is increased from −1.5 V to −5 V. The p-branch currents I^p are already exponentially increasing at low amplitudes from −2 V, reaching a maximum value of $I^p = 300$ nA at $V_{set} = -4$ V. Thereby, the ferroelectric polarization of the HZO cannot be further increased, as apparently a maximum number of domains are already aligned parallel to each other. As the pulse amplitude is further increased, I^p is clearly decreasing again. This can be explained by an accumulation of trap states due to strong band bending during the pulsing operation. Charge carriers can tunnel through the thin SiO_2 IL, occupying deep trap states at the high-κ interface and counteracting the ferroelectric

effect. Furthermore, large pulsing amplitudes can damage the oxide layer, increasing gate leakage and degrading the device characteristic. For the n-branch current, first significant changes are evident at $V_{set} \leq -2.25\,\mathrm{V}$, with a more rapid decrease after exceeding $-4\,\mathrm{V}$. There, the minimum value of $I^n = 16\,\mathrm{pA}$ is reached at $V_{set} = -4.5\,\mathrm{V}$, with a minor degradation at higher amplitudes. The weaker trapping effect for electrons can be attributed to the defects in the HZO acting as donors, favoring holes but repelling electrons.

Overall, it can be seen that the device characteristics of the FeRFET can be gradually controlled via the pulse amplitude so that clearly separated, non-volatile values of I^n and I^p can be obtained. These multiple stable output states can be highly interesting for the realization of multi-level cells (MLC), where more than one bit per data cell can be stored, increasing the bit density without decreasing the feature size [225]. Furthermore, this inherently tunable behavior is of great interest as it could be exploited to engineer devices compatible with a neuromorphic-like computation mechanism and mimicking the behavior of synapses [48].

6.3.2 Retention Measurements

The stability of the individual polarization states over time is an important characteristic for the non-volatile FeRFET. In this regard, retention measurements over ∼6 hours are conducted in Figure 6.7. Note that a different device was used here, as excessive testing at even higher pulse voltages led to some degradation of the device and would therefore not be representative of the fabricated structures. To measure the retention, after resetting the device to the opposite polarization, the individual states were programmed with the corresponding SET sequence, followed by repetitive transfer measurements every 10 min. Figure 6.7(a) shows the series of transfer measurements over time for an n-mode state set via $V_{set} = 5\,\mathrm{V}$. Thereby, a remarkably high temporal stability is achieved over the entire measurement range between $V_{BG} = \pm 20\,\mathrm{V}$ and the observation period. Only a minor decrease of both on-state currents (I^n, I^p) over time is evident, indicating that almost no depolarization of the HZO layer takes place, keeping its electrostatic influence on the injection barriers constant. The largest change occurs directly after the first measurement, presumably due to relaxation of charge trap states from the SET pulse. A similar temporal stability is achieved for the p-type dominant configurations, as shown in Figure 6.7(b) for the transfer measurements over time shown after programming the device with $V_{set} = -3.5\,\mathrm{V}$. Again, the largest changes in the characteristic are observed between the first and the second measurement. The slight increase of I^p and a decrease of I^n over time even improves the p-mode in terms of the I_{on}/I_{off} ratio (with $I_{off} \equiv I^n$). This is again an indication of positive trap states partially releasing over time at a faster rate than the depolarization of the HZO. A decay of the polarization would result in the opposite effect, lowering the injection barriers for electrons and weakening the dominant p-type behavior.

A more detailed analysis of on-current retention for different pulsed states is shown in Figure 6.7, with p-type currents I^p in (c) and n-type currents I^n in (d). Note that these drain current states are a different "state" approach than V_{th} shifts often used in, e.g., flash

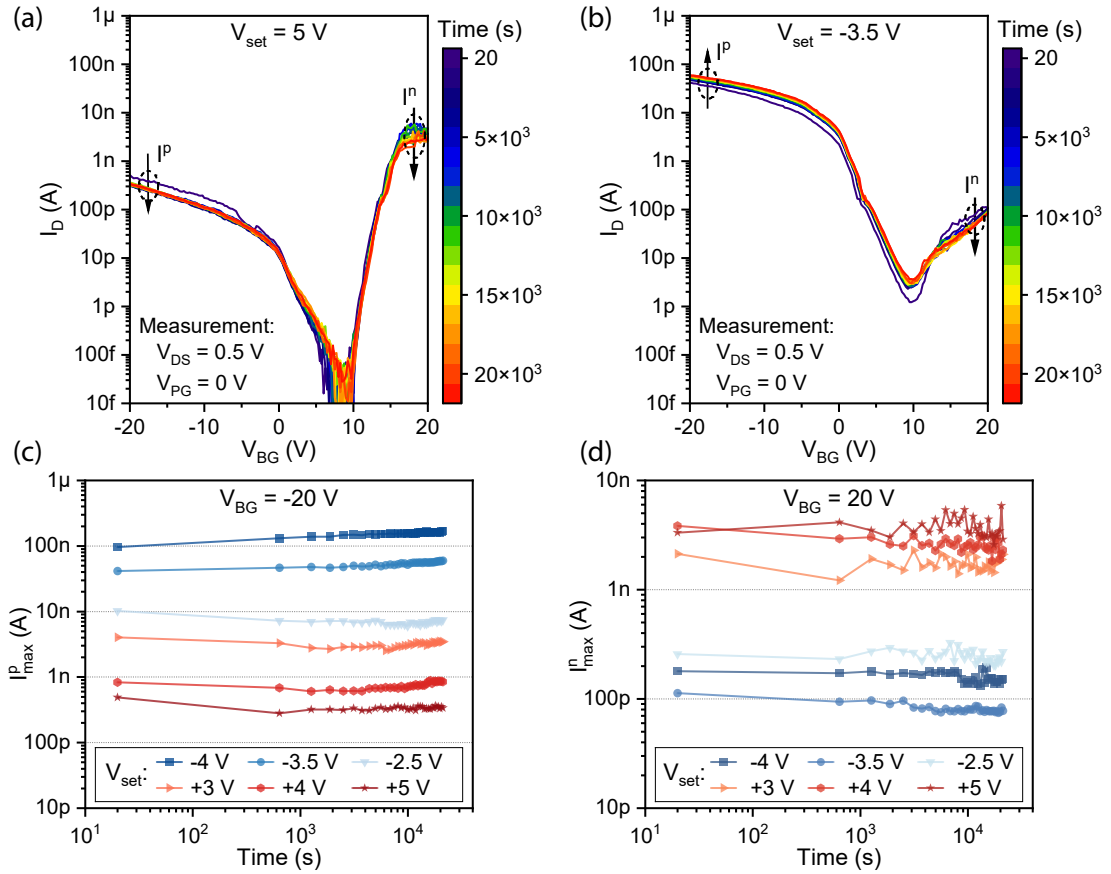

Figure 6.7: Repetitive transfer characteristic after an initial polarization pulsing with (a) $V_{set} = 5\,\mathrm{V}$ for the n-mode and (b) $-3.5\,\mathrm{V}$ for the p-mode, measured at intervals of 10 min at a bias voltage of $V_{DS} = 0.5\,\mathrm{V}$. (c) Time-dependency of the maximum p-branch currents I^p extracted at $V_{BG} = -20\,\mathrm{V}$ and (d) n-branch currents I^n at $V_{BG} = -20\,\mathrm{V}$ for different polarization pulse heights. Device dimensions: $L_{Si} = 2.9\,\mu\mathrm{m}$, $W = 600\,\mathrm{nm}$.

memories or conventional FeFETs. Over the observed period of ~6 hours ($>2 \times 10^4\,\mathrm{s}$), only minor changes are evident. In particular with regard to the p-type currents, the individual states remain clearly distinguishable. For example, the $-4\,\mathrm{V}$ state increases from 96 nA up to 168 nA, while the $-3.5\,\mathrm{V}$ state rises from 41.5 nA to 60 nA, always remaining well separated. Since the influence of the ferroelectric polarization on the n-type currents is generally smaller than in the p-branch (~2 orders of magnitude), a clear differentiation between some less separated states can be more difficult, although a similar temporal stability is achieved. Considering only the two main states of the FeRFET, n-mode and p-mode (e.g., set via a short pulse at 5 V and $-4\,\mathrm{V}$), operation in the respective device polarity is definitely stable over a long period of time, obviating the need for a constantly applied PG voltage in logic circuit applications. Finally, this non-volatile FeRFET could be a promising building block for next-generation LiM-applications and artificial neural networks [40, 42, 83].

Chapter 7

Summary and Outlook

This thesis provides a systematic summary, conclusion and prospect of the experimental work of Al-Si and Al-$Si_{1-x}Ge_x$ heterostructures integrated into SBFETs, further enabling the demonstration of highly on-state symmetric RFETs and RFET-based complementary logic circuits, as well as novel non-volatile FeRFETs. These emerging device concepts provide alternatives to the traditional IRDS roadmap with CMOS technology [11] and may enable novel computing paradigms such as neuromorphic computing or adaptive logic-in-memory.

Al-$Si_{1-x}Ge_x$ heterostructure formation

The fundamental process step for the fabrication of all the different devices in this work is the thermally induced exchange reaction between Al and $Si_{1-x}Ge_x$ in top-down patterned nanosheets. This novel heterostructure formation technique enables the monolithic integration of Si and $Si_{1-x}Ge_x$ channels with single-elementary and crystalline Al contacts.
In the first part of this work, the contact formation of Al to Si nanosheets was studied. The thereby formed Al-Si junctions revealed flat and highly abrupt interfaces with symmetric activation energies E_a for the injection of electrons and holes, ideal for the use in reconfigurable electronics. The quality and abruptness were confirmed by TEM and EDX measurements, revealing the crystalline and single-elementary Al lead. Importantly, no evidence of void formation, spiking or electromigration effects was observed in any sample analyzed, including structures after extensive electrical characterization. This is in stark contrast to the contact formation to bulk Si and can presumably be attributed to the absence of grain barriers in the nanoscaled devices. The absence of intermetallic phases further overcomes difficulties of complex growth kinetics of commonly used silicidation processes that require precise process control and additional phase stabilization measures. In addition, the pure and crystalline Al leads achieve significantly lower resistivities ($\rho = 6.65 \times 10^{-8}\,\Omega\,\mathrm{m}$ at room temperature) at similar breakdown current densities ($J_{max} > 1 \times 10^{12}\,\mathrm{A/m^2}$) compared to conventional metal silicides.

Without adaptations, this thermal annealing process can be transferred to the $Si_{1-x}Ge_x$ platform, where monolithic Al contact formation was demonstrated to nanosheets patterned from vertical Si-$Si_{1-x}Ge_x$-Si heterostructure substrates of different stoichiometric compositions. Similar structural properties and reproducibility of the formed structures are observed as for the exchange in pure Si nanosheets. Interestingly, a Si-rich agglomeration between the intruded Al and the $Si_{1-x}Ge_x$ layer is formed, resulting in an Al-Si-$Si_{1-x}Ge_x$ multi-heterojunction. This can effectively change the otherwise Fermi level pinning of the metal-Ge Schottky junction near the valence band, resulting in a more balanced injection of electrons and holes. To clarify the exact mechanisms for the formation of this Si agglomeration and how to control its thickness, further investigations are required. From an integration point of view, the reaction temperatures are higher than for Al-Ge formation, making the former compatible with mid-end-of-line CMOS processing.

Within the scope of this work, the Al-Si/Ge exchange process proved to be a reliable and reproducible method for the fabrication of the different device types. However, further analyses regarding a large-scale integration into state-of-the-art FEOL processes are necessary. In particular, the long-term stability of the monolithically formed Al-$Si_{1-x}Ge_x$ junctions needs to be investigated to provide sufficient data on stress-induced void formation and electromigration.

Composition-dependent transport investigation in Al-$Si_{1-x}Ge_x$ heterostructures

The electrical transport in Al-$Si_{1-x}Ge_x$-Al heterostructures integrated into SBFET architectures was investigated and compared regarding their stoichiometric layer composition. This includes the fabrication and temperature-dependent electrical characterization of five different compositions with Ge contents ranging from 0 % to 100 %. The different $Si_{1-x}Ge_x$ devices exhibited distinct device characteristics with widely varying carrier injection capabilities, which may be key building blocks for the realization of emerging nanoelectronic, optoelectronic and Josephson FET quantum devices.

A transition from a symmetric ambipolar transfer characteristic for pure Si channels towards a distinct p-type behavior for pure Ge layers is observed. Accordingly, the extraction of the activation energies E_a revealed distinct and comparable injection barriers for both electrons and holes for the Si device. Increasing the Ge content results in lowered E_a for hole injection, reaching negative E_a values for transparent, quasi-ohmic contacts for holes at Ge contents $\geq$ 50 %. Remarkably, the Al-$Si_{0.5}Ge_{0.5}$-Al heterostructures revealed transparent junctions for both electron and hole conduction, which may be promising for Josephson junction quantum devices with gate-tunable charge-carrier tunneling [296, 297]. The Ge-rich samples with Ge contents $\geq$ 75 % show strongly asymmetric barriers, with transparent junctions for holes and distinct Schottky barriers for electrons. The vertical confinement in the Si-Ge-Si heterostructures further leads to the formation of a hole gas, with a gate-tunable transparency of the Al-Ge junction, which could be utilized in Josephson junction devices to realize superconducting qubits [188, 274]. Furthermore, the

Ge-rich structures are capable of exhibiting NDR functionality, which has already been demonstrated in Al-Ge-Al NW heterostructures [33, 34]. Recently, we were also able to transfer this to the top-down fabricated Si-Ge-Si heterostructure substrate platform from this work, where it was possible to combine the gate-tunable NDR with the RFET functionality to enable reconfigurable NDR-based logic [LW5, LW4].

In follow-up investigations, based on the fabrication and analysis methods of the presented study, we recently demonstrated that the integration of Sn-rich layers in vertical Si-$Ge_{1-x}Sn_x$-Si heterostructures can also be achieved by utilizing the Al contact formation process [LW2]. A similarly dominant p-type behavior is thereby obtained due to the formation of a hole gas, with the Sn strongly increasing the on and off currents.

Realization of Si and $Si_{0.67}Ge_{0.33}$ RFETs with symmetric on-states

The potentially CMOS-compatible integration of RFETs based on Al-Si-Al heterostructures on the SOI platform was demonstrated. The three top-gated devices thereby showed highly symmetrical operation modes in terms of on-state currents (37.6 µA/µm, 38.4 µA/µm), threshold voltages (0.51 V, −1.14 V), and subthreshold slopes (144 mV/dec, 142 mV/dec) for n- and p-mode operation, respectively ($V_{PG} = \pm 4$ V, $V_{DS} = 2$ V). The symmetric properties of the devices can be attributed to the mid-gap pinning properties of the Al-Si junction. Furthermore, the independent control of injection barriers and channel conductivity effectively inhibits injection of the unwanted carrier type, resulting in extremely low off-currents ($<10^{-7}$ µA/µm) and a high on/off current ratio of $>5 \times 10^8$ for both operation modes. Furthermore, the high symmetry of the RFETs is maintained when switching to a single symmetric operation voltage level of ±2 V, ideal for their integration into logic circuits. The extraction of the transistor parameters showed a low device-to-device variability at the lab scale, which is also an important prerequisite for a larger scale circuit integration. Temperature-dependent measurements and the extraction of the activation energies for both operation modes are further conducted to provide more insights regarding the inherent transport mechanisms of the RFET. Measurements at elevated temperatures up to 400 K showed no significant degradation effects apart from an expected increase in off-state currents. The realization of MIGFET structures with two and three independent CGs has also been demonstrated, replacing two or three RFETs connected in series (with the same polarity), effectively reducing the transistor count and thus the critical path delays within a circuit.

To scale up the drive currents of the individual devices, a multi-wire RFET was fabricated consisting of a parallel array of ten Al-Si-Al heterostructures. Without extending the lateral dimensions of the devices, an increase in drive currents has also been achieved by integrating Ge-rich layers, in particular the vertical Si-$Si_{0.67}Ge_{0.33}$-Si heterostructure, into the nanosheet transistor channel. Importantly, the thermal oxidation of the Si capping layer allows to form a good quality SiO_2 gate oxide and prevents the formation of native Ge oxides, resulting in a reliable device operation with low hysteresis. Subsequently, the subthreshold characteristic of the devices was optimized by integrating HfO_2 into the

gate stack and thus effectively reducing the EOT. Despite the introduction of the Ge-rich layer, a fairly good on-state symmetry of the RFETs is retained, which can presumably be attributed to the formation of the Al-Si-$Si_{0.67}Ge_{0.33}$ multi-heterojunction, repositioning the Fermi-level pinning of Ge towards the middle of the band gap.

To put the results of the fabricated RFETs into perspective, a thorough comparison with various state-of-the-art RFETs from the literature is provided in Section 5.3.2. Throughout the literature, in particular the Al-Si-based RFETs achieved an outstanding on-state symmetry and on/off current ratios at even improved on-state currents. Remarkably, no strain engineering measures are required to achieve this symmetry. Furthermore, the RFETs with a Ge-rich transistor channel show an order of magnitude improvement in symmetry compared to the other Ge-channel devices based on Ge NWs or Ge nanosheets patterned from GeOI substrates.

Next, a short outlook regarding Ge layer integration is given. By facilitating a similar process scheme as for the $Si_{0.67}Ge_{0.33}$-based RFETs and refining the gate stack, the fabrication of RFETs with pure Ge layers embedded in a vertical Si-Ge-Si heterostructure and c-Al S/D contacts has recently been demonstrated by Fuchsberger et al. [LW9, LW3]. An on-state symmetry of $I^p_{on}/I^n_{on} = 1.96$ is achieved, which is remarkable for a Ge channel device, along with a distinct increase in current densities. The integration of Ge further allows to access an additional and stable NDR mode with gate-tunable peak currents [LW5, LW4]. The co-integration of these multi-mode devices in Si-based CMOS technology can enable the realization of circuits with enhanced performance and functionality, e.g., for multi-value logic [33, 103] or oscillators towards the THz range [105].

Additional performance enhancements of the devices are feasible by device scaling. Electrostatic gating can be improved by further scaling the EOT, in particular by using high-κ dielectrics and reducing the thickness of the SiO_2 interface layer. In addition, improved gating architecture, such as GAA, and a reduction of the transistor channel thickness are other effective measures to achieve enhanced device performance. Regarding the channel length scaling, Baldauf et al. [209] used TCAD simulations to estimate a stable device operation down to channel lengths $L_{ch} > 8\lambda$. Sessi et al. [72] recently even demonstrated the first fully integrated RFETS on a 22 nm FDSOI platform using a back-bias RFET architecture, thereby achieving Si channel lengths down to 20 nm.

Before the emerging RFET device concept can be transferred to industrial processing platforms, the devices need to be analyzed for reliability in realistic application scenarios. In this regard, Galderisi et al. [298] provided a first reliability analysis regarding bias temperature instabilities in three top-gated RFETs. However, further research is needed with a focus on deriving a complete degradation model including voltage, temperature, and area scaling.

Realization of adaptive complementary and combinational logic circuits

Based on the highly on-state symmetric Al-Si RFETs on the SOI platform, complementary and combinational logic circuits were realized by directly interconnecting multiple RFETs on chip. All demonstrated circuits were thereby analyzed by measuring both static output transfer characteristics as well as transient measurements and are capable of providing full-swing operation at single symmetrical supply rail voltages of $\pm 2\,\mathrm{V}$ on all device terminals. The complementary inverter based on two physically identical RFETs could be operated within a wide voltage range from $2.5\,\mathrm{V}$ to $1.2\,\mathrm{V}$, generally providing large and symmetric noise margins and a good suppression of the cross-current flow at the defined output states. With the runtime reconfigurable NAND/NOR gate based on three RFETs, resembling a minority gate, as well as the XOR/XNOR gate based on four RFETs (XOR3 gate), the reduction of the transistor count compared to conventional CMOS technology was successfully demonstrated experimentally. MAJ gate functionality has also been achieved by adapting the signal inputs of the XOR3 gate. By extracting 2D output color maps, the stability of the logic circuits against input voltage variations was analyzed, where overall sufficiently large operation windows were obtained, enabling a reliable full-swing operation. Combining the XOR3 and the MAJ gate, the realization of the first complementary 1-bit full adder circuit was obtained with a total of only eight physically identical RFETs. Conventional CMOS implementations, on the other hand, would require more than twice as many transistors. The operation frequency of the demonstrated circuits, however, is severely limited due to large parasitic capacitances resulting from the laboratory-based structure design with large planar contact pads on the SOI substrate. Through the use of advanced interconnect technology and additional scaling measures, simulations have shown that RFET-based circuits can operate at speeds in the GHz range and can even outperform their conventional CMOS counterparts due to the reduced number of transistors required [19, 79, 81].

Targeting large-scale integration of the devices, Al may not be ideal as an interconnect material due to problems with its gap-filling capabilities. In this regard, other metals with better gap-filling capabilities, such as Cu or W [299, 300], could be deposited on top of the (crystalline) Al contacts in the S/D region after Al-Si heterostructure formation. Therefore, additional diffusion barriers such as ALD-grown TiN or TaN should probably also be added to further stabilize the underlying Al layer [301].

Despite the expected benefits of large-scale integration of RFETs into logic-based circuits, this emerging device concept may not be powerful enough to fully replace conventional CMOS technology. However, it could very well be co-integrated into the CMOS platform to efficiently handle specific tasks that are otherwise resource intensive. As an alternative application to conventional computing, RFETs can enable emerging hardware security concepts to prevent theft of circuit design and functionality [23–25].

Non-volatile ferroelectric RFETs

Targeting adaptive logic-in-memory applications, the integration of a ferroelectric HZO layer into the SBFETs was investigated. The HZO film is deposited on an ultra-thin SiO_2 interface layer on the Si nanosheet channel to reduce charge trapping effects and enable low hysteresis transfer characteristics. In a first step, FeSBFETs with a global TG covering both the Al-Si junctions and the Si channel are analyzed. A stronger modulation of the I^p_{on}/I^n_{on} current ratio is observed, while the V_{th} shift is relatively small. This indicates that the HZO layer is mainly polarized near the Al-Si interface, which mainly modulates the carrier injection rather than the potential across the channel. When using the TG electrode to polarize the HZO and the BG to modulate the current flow, a change of the n-type current over three orders of magnitude between the two non-volatile polarization states was observed.

By adapting the transistor design, where the TG covers only the area around the Schottky junctions and serves as the PG, and the BG is used to modulate the current flow (CG), the first non-volatile RFETs implementing a ferroelectric gate stack (FeRFET) are demonstrated. So far, a comparable non-volatile operation mode switching was only demonstrated in 2D van der Waals heterostructure devices utilizing charge trapping layers [82]. In the demonstrated FeRFET, non-volatile switching between distinct n- and p-type operation modes is achieved by polarizing the HZO in the vicinity of the Schottky junctions using voltage pulses on the PG. This non-volatile polarity control can be, e.g., used to fabricate generic circuits in foundries and to program the proprietary circuit function or code by the customer. Furthermore, by varying the pulsing amplitude, multiple stable output states can be accessed due to a gradual switching of the HZO. Retention measurements were then carried out to demonstrate the stability of the polarization states over time. Especially when considering the p-type on-currents, the six analyzed states remain clearly distinguishable within the observation period of 6 h. However, more detailed analyses of the long-term stability of the stored states, also at elevated temperatures, as well as the cycling endurance, still need to be conducted.

Since the BG contact is used as CG to modulate the currents, rather high operating voltages of ± 20 V are required. To improve the electrostatic control, a CG electrode could be added between the two PGs, similar to the TTG RFET architecture. It is advantageous to deposit the CG after the crystallization of the HZO, as the HZO underneath then remains in a trivial dielectric phase, preserving the hysteresis-free current modulation.

The low on-state currents, as well as the on-state symmetry of the FeRFET, however, still need to be improved in order to meet the requirements for integration in logic circuits. The asymmetry can probably be attributed to the presence of a certain amount of negative charge, e.g., due to fixed oxide or interface states. However, the origin of this shifted device behavior with dominant p-type currents is not yet fully understood.

A viable approach to improve the ferroelectric switching can be the integration of a metal floating gate between the IL and the HZO in an MFMIS gate structure. This FG layer can enhance the electric field distribution during the polarization pulsing [132]. Furthermore, it can lower the influence of spatial variation of the HZO grains with different ferroelectric/dielectric phases, resulting in a more uniform channel conductivity and lowering device-to-device variability [238, 239]. Especially in FeSBFETs, this can help to polarize more ferroelectric grains across the semiconductor channel, resulting in a larger V_{th} shift for an increased MW.

In conclusion, the demonstrated FeFETs, especially the FeRFETs, have great potential for the realization of high-scale, CMOS-compatible logic-in-memory applications. In particular, the combination of adaptive RFETs with non-volatile, gradual switching capabilities could lead to novel concepts for highly adaptive artificial neural networks.

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Conference Contributions

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[LWC8] **L. Wind**, S. Preiß, D. Nazzari, J. Aberl, E. P. Navarrete, M. Brehm, L. Vogl, A. M. Minor, M. Sistani, and W. M. Weber, "Si/$Ge_{1-x}Sn_x$/Si Transistors with Highly Transparent Al Contacts," in *Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS)*, Athens, Greece, 5 2024.

[LWC9] A. Fuchsberger, **L. Wind**, D. Nazzari, J. Aberl, E. P. Navarrete, M. Brehm, L. Vogl, P. Schweizer, M. Sistani, and W. M. Weber, "Temperature-Dependent Electronic Transport in Reconfigurable Transistors based on Ge on SOI and Strained SOI Platforms," in *Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS)*, Athens, Greece, 5 2024.

[LWC10] D. Nazzari, **L. Wind**, D. Mayr, K. Kim, M. Sistani, A. Fuchsberger, R. Behrle, and W. M. Weber, "Ferroelectric-enhanced Schottky-Barrier FETs towards Logic-in-Memory applications," in *High-k Workshop*, Dresden, Germany, 5 2024.

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Curriculum Vitae

Personal Information

Name	Lukas Wind
Date of birth	06.06.1994
Address	Biedergasse 1/1A, 1190 Wien
E-Mail	lukas.wind@tuwien.ac.at
ResearchGate	www.researchgate.net/profile/Lukas-Wind
ORCID	https://orcid.org/0000-0002-1458-1358

Education

03/2021 - present	**PhD in Electrical Engineering** TU Wien - Institute of Solid State Electronics Thesis: *Si to SiGe Heterostructure Transistors for Reconfigurable Circuits and Functionality Enhancement via Ferroelectric Gating*
09/2018 - 02/2021	**Master Degree in Microelectronics and Photonic** TU Wien Thesis: *Wafer-scale Fabrication and Characterization of Monolithic Al-Ge Heterostructures*
09/2018 - 02/2019	**ERASMUS+ Semester - Photonics Master** Universitat Politécnica de Catalunya
09/2014 - 08/2018	**Bachelor Degree in Electrical Engineering and Information Technology** TU Wien Thesis: *Reconfigurable and Innovative Display - Infrared Data Channel and Image Computation*

Student Awards

2016, 2018	**TU Wien - Merit Scholarship**

Employment

03/2021 - present	**TU Wien - Institute of Solid State Electronics** University Assistant
04/2017 - 02/2021	**Elektrobit Austria GmbH** - Vienna, Austria Hardware Assembly, Testing and Repair