Master Thesis

Electrical characterization of p-GaN gate HEMTs: The role of intentional hole injection for dynamic $R_{DS,on}$ recovery

Master's degree programme

Technische Physik

submitted by

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Abstract

The Gallium Nitride (GaN) High Electron Mobility Transistor (HEMT) is a lateral device that leverages strong polarization effects in GaN and the bandgap difference of an AlGaN/GaN heterojunction to generate a Two-Dimensional Electron Gas (2DEG) with exceptionally high electron mobility. Due to their superior material properties and efficiency, these transistors are considered to be the next generation of semiconductor devices.

Since native GaN substrates are not available on an industrial scale and are prohibitively expensive, industry has turned to manufacturing GaN-based devices on silicon substrates, the material most of today's semiconductor devices are based on. This leads to orders of magnitude lower production costs, however results in side effects that have to be mitigated with a good understanding of the processes occurring in the device. A carbon-doped buffer is needed to insulate the electrically active device area from the conductive silicon substrate, while silicon nitride (SiN) based passivation protects the surface. Both of these locations provide electron trapping sites which are filled during stress conditions. These trapped electrons lead to transient drift effects, such as dynamic ON-resistance ($R_{\mathrm{DS,on}}$) and threshold voltage shift (ΔV_{TH}).

To better understand how active hole injection from a p-doped GaN region between the gate and the drain (p-drain) affects the recovery during and after hot-carrier stress, two Source-Measure-Unit (SMU) setups were investigated and compared. The effect of hole injection from the p-drain after hot-carrier stress was compared to hole injection from the p-GaN gate. This resulted in similar time constants, leading to the conclusion that fast lateral hole transport at the AlGaN back-barrier renders the lateral position of the hole injection site irrelevant within the measurement accuracy of the setup.

Another aspect that was investigated was active hole injection during hot-carrier stress. The Hybrid Drain-embedded Gate Injection Transistor (HD-GIT) is a commercially available device, that uses this effect passively to reduce stress related performance degradation. A clear reduction of the degradation was observed at a drain voltage of 150 V, which was correlated with the applied hole current. For higher stress voltages (>300 V), the initial degradation was found to be independent of the applied hole current.

In addition, the lateral hole transport properties of specially designed device structures were investigated at room temperature and at 150 °C. Four different epitaxy and process variations were available and tested using two different hole injection mechanisms. The hole diffusion constants of the carbon-doped buffer were calculated for hole injection from the p-GaN gate.

Zusammenfassung

Galliumnitrid (GaN) High Electron Mobility Transistoren (HEMT) sind laterale Bauelemente, die auf der hohen Elektronenmobilität eines zweidimensionalen Elektronengases (2DEG) basieren. Dieses 2DEG bildet sich an einem AlGaN/GaN-Heteroübergang aufgrund der Bandlückendifferenz sowie der starken spontanen und piezoelektrischen Polarisationseffekte in GaN. Aufgrund ihrer ausgezeichneten Materialeigenschaften und ihrer Effizienz werden diese Transistoren als die nächste Generation von Halbleiterbauteilen angesehen.

Da native GaN Wafer nicht in industriellem Maßstab zur Verfügung stehen und extrem teuer sind haben sich Hersteller dazu entschlossen Galliumnitrid-Transistoren auf Silizium Wafern zu fertigen. Das führt zu stark reduzierten Bauteilkosten, geht jedoch mit einigen Nachteilen einher. Diese Nachteile müssen durch ein gutes Verständnis interner Prozesse reduziert werden. Eine Kohlenstoff-dotierte Schicht ist notwendig um den elektrisch aktiven Bereich von dem leitfähigen Silizium Trägermaterial zu isolieren und eine Siliziumnitrid (SiN) Passivierung schützt die Oberfläche des Transistors. In beiden Bereichen sind Elektronenfallen, die während Stresszuständen befüllt werden können und in der Folge zu transienten Effekten führen, z.B. einem dynamischen ON-Widerstand ($R_{\mathrm{DS,on}}$) und einer Verschiebung der Schwellenspannung (ΔV_{TH}).

Um besser zu verstehen, wie sich aktive Lochinjektion von einer p-dotierten Region zwischen dem Gate und dem Drain (p-Drain) auf die Regeneration während und nach Hot-Carrier Stress auswirkt, wurden zwei Source-Measurement-Unit Setups untersucht und miteinander verglichen. Im Anschluss wurden die Auswirkungen von Lochinjektion vom p-Drain nach Hot-Carrier Stress mit den Auswirkungen von Lochinjektion vom p-dotierten Gate verglichen. Es wurde festgestellt, dass die laterale Position der Lochinjektion aufgrund der schnellen Lochausbreitung in der AlGaN back-barrier, innerhalb der Messgenauigkeit des Setups, keinen signifikaten Einfluss auf die Zeitkonstanten hat.

Der andere Aspekt, der untersucht wurde, ist die Auswirkung von aktiver Lochinjektion während dem Hot-Carrier Stress. Dieser Effekt wird bereits passiv beim Hybrid Drain-embedded Gate Injection Transistor (HD-GIT), einem am Markt erhältlichen Transistordesign, verwendet, um stressinduzierte Degradation zu verringern. Für kleine Drain Spannungen von 150 V wurde eine klare Reduzierung der Degradation festgestellt, abhängig vom injizierten Lochstrom. Für große Drain Spannungen (>300 V) war die Degradation des Transistors unabhängig vom injizierten Lochstrom.

Zusätzlich wurde die laterale Lochausbreitung in speziellen Teststrukturen bei Raumtemperatur und bei 150 °C untersucht. Hierfür standen vier verschiedene Epitaxie- und Prozessvarianten zur Verfügung, an denen zwei unterschiedliche Lochinjektionsmechanismen getestet wurden. Für die Lochinjektion vom p-dotierten Gate wurden die Diffusionskonstanten von Löchern in Kohlenstoff-dotiertem GaN bestimmt.

Contents

1 Introduction

Electric energy demand continuously increases, as more and more of the global community switches from using fossil fuels to electricity, to power transportation, heating and other needs. From the advent of the vacuum tube in the early 20th century, as one of the first active electrical component, to the invention of the silicon-based transistor, research was dedicated to improve overall efficiency and switching speed. However, after decades of intense research, the silicon-based power transistor approaches its theoretical limit, and new materials are necessary to make major advancements.

Over the recent years, wide bandgap semiconductors, like gallium nitride (GaN) and silicon carbide (SiC), have emerged as the main contenders to change the status quo, due to their superior material properties (Table 1.1) [1, 2].

Property	**Si**	**4H-SiC**	**GaN**
Bandgap (eV)	1.12	3.2	3.4
Critical field E_{cr} ($\frac{\mathrm{MV}}{\mathrm{cm}}$)	0.25	3	4
Dielectric constant ϵ	11.8	9.7	9.5
Saturation velocity v_{s} ($10^7 \frac{\mathrm{cm}}{\mathrm{s}}$)	1	2	3
Electron mobility μ ($\frac{\mathrm{cm}^2}{\mathrm{Vs}}$)	1350	800	1300 (2DEG)
Intrinsic carrier concentration n_{i} ($\frac{1}{\mathrm{cm}^3}$) at 300 K	10^{10}	10^{-7}	10^{-10}
Thermal conductivity ($\frac{\mathrm{W}}{\mathrm{cmK}}$)	1.5	4.9	1.3

Table 1.1: Overview of the material properties of silicon (Si), silicon carbide (SiC) and gallium nitride (GaN) [1].

These material properties are the key factors in determining power transistor performance. A wide bandgap and a high critical electric field enable high-voltage operation, while the saturation velocity and the electron mobility are important aspects in determining the possible switching frequency. In addition, a low intrinsic carrier concentration suppresses leakage currents, while a high thermal conductivity enables compact system designs and effective heat dissipation.

While SiC has a higher technological maturity and established markets in the high-voltage ($\geq$1200 V) segment, GaN, manufactured on silicon wafers, is catching up and mainly in use for high-frequency and medium-voltage ($\leq$700 V) applications [3].

The GaN-based High Electron Mobility Transistor (HEMT) is the device structure that has established itself as the alternative to the silicon-based Metal-Oxide Semiconductor Field Effect Transistor (MOSFET). It utilizes a AlGaN/GaN heterojunction to form a

Two-Dimensional Electron Gas (2DEG), where electrons exhibit a very high mobility. GaN-based devices however still suffer from dynamic performance degradation due to electron trapping within the structure, which has to be addressed by further research.

Figure 1.1 illustrates the theoretically achievable specific ON-resistance for a given breakdown voltage in silicon, silicon carbide, and gallium nitride, highlighting the efficiency gains enabled by gallium nitride advancements.

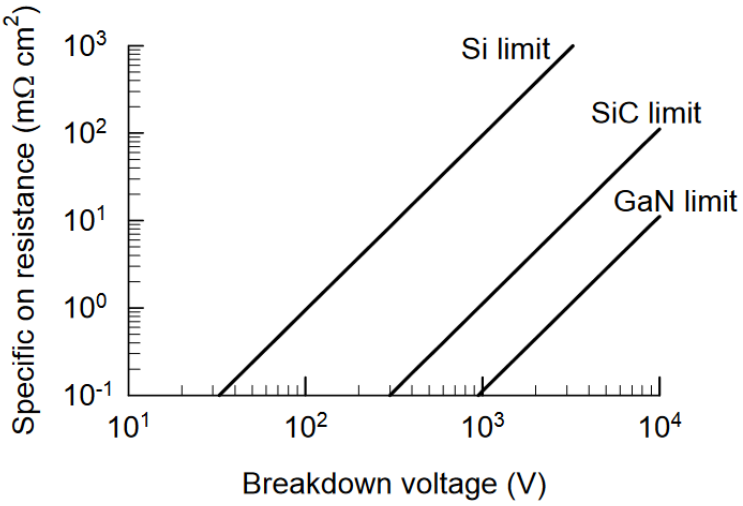

Figure 1.1: Specific ON-resistance over the breakdown voltage, highlighting the higher theoretical limit of GaN compared to Si and SiC. Figure from [4].

To further the understanding of device recovery from hot-carrier stress related performance degradation, active hole injection from a p-doped GaN region between the gate and the drain was studied. Hot-carrier stress is a term that refers to a state, where high voltages are applied to the drain of the transistor, while the channel is not completely pinched off. Another aspect that is addressed in this thesis are the lateral hole transport properties of the GaN-on-Si HEMT.

The body of this thesis is structured in five sections. In Section 2 the relevant properties of GaN, the HEMT and the charge trapping dynamics in GaN HEMTs will be discussed. Section 3 serves as an introduction to the measurement equipment and procedures, the device structures and the setups used to electrically characterize the devices. In Section 4 the results of the characterization will be presented and discussed, followed by a conclusion and an outlook for future investigations in Section 5.

2 Fundamentals on GaN-based devices

2.1 Crystal structure and properties of GaN

Group III-N semiconductors like GaN are formed by combining a group III metal, like aluminum (Al), gallium (Ga) or indium (In) with the group V element nitrogen (N). The resulting crystals have material characteristic highly advantageous for electronic applications. Key characteristics include high breakdown voltages, good thermal stability and a wide bandgap [5].

Under ambient pressures these III-N semiconductors crystallize in either the zinc-blende or wurtzite structure, while in high-pressure conditions crystallization in the rock-salt structure can occur [6, 7]. The wurtzite structure, illustrated in Figure 2.1, is the thermodynamically stable phase of AlN, GaN and InN. Additionally, the wurtzite configuration exhibits the highest potential for electrical applications due to its strong spontaneous and piezoelectric polarization effects, which are unique to this structure [6].

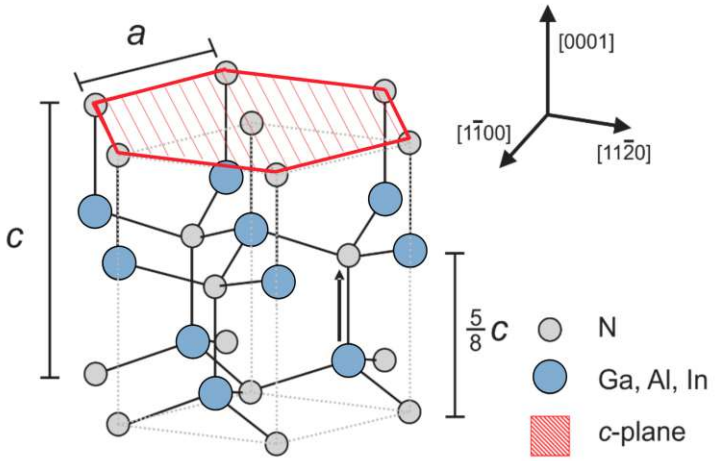

Figure 2.1: The wurtzite crystal structure of group III-N compounds, is formed by two interpenetrating hexagonally close packed lattices with a displacement of $\frac{5}{8}$c along the [0001] direction [8, 9], picture adapted from [10].

Wurtzite-type materials like AlN, InN and GaN consist of two hexagonally close-packed layers with an ABAB stacking pattern. The layers have a displacement of $\frac{5}{8}$c along the hexagonal axis, also referred to as the c-axis or the [0001] direction [8, 9]. The typical growth direction is also along this axis [6].

The primary lattice constants that define the hexagonal structure are the length of the sides of the hexagon, a, and the height along the hexagonal axis, c. Each nitrogen atom

is single-bonded to four equidistant group III atoms and vice versa in a tetrahedral configuration [5]. This atomic configuration contributes to the strong mechanical properties and the thermal stability of these materials.

III-N crystals can grow with either metal-face or nitrogen-face orientation. In metal-face orientation the metal atoms are in the top position of the {0001} bilayer, while in nitrogen-face orientation the nitrogen atoms are in the top position of the {0001} bilayer [11]. The specific crystal growth orientation depends on the growth technique and the used parameters. Metalorganic chemical vapor deposition (MOCVD) has been shown to primarily lead to metal-face growth, while other techniques like molecular beam epitaxy (MBE) lead primarily to nitrogen-face growth [12–14]. The orientation has a significant influence on the material properties and the device layout. Ga-face growth for example has been shown to result in a better surface quality [12]. For this reason research was mainly dedicated towards Ga-face GaN-based devices. However, recently the interest in manufacturing devices using N-face GaN has grown. [15]

The devices used for this thesis are manufactured using Ga-face GaN and all illustrations and explanations therefore refer to the this orientation.

The difference in electronegativity between nitrogen (3.04) and the group III elements (Al: 1.61, Ga: 1.81, In: 1.78) [16], combined with the lack of inversion symmetry in the wurtzite crystal structure leads to dipoles forming along the [0001] direction [17]. The summation of all these dipoles results in a strong spontaneous polarization in the material and positive and negative sheet charges at the nitrogen- and gallium-side of the crystal respectively, as shown in Figure 2.2.

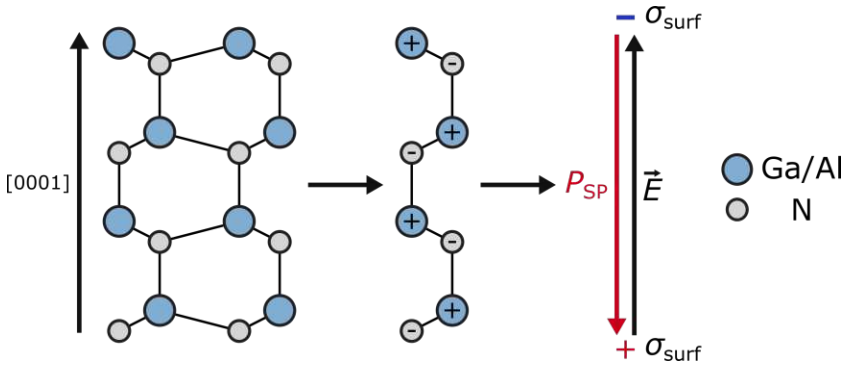

Figure 2.2: Due to the difference in electronegativity, dipoles form along the [0001] direction of the crystal, leading to a polarization pointing from the nitrogen to the nearest neighbor gallium atom in the c-direction. This results in a negative sheet charge at the gallium-side and a positive sheet charge at the nitrogen-side of the crystal. Picture adapted from [18].

In addition to the spontaneous polarization, a piezoelectric polarization occurs if the crystal is under mechanical stress. If the GaN crystal is under tensile stress, depicted in Figure 2.3, the piezoelectric polarization enhances the spontaneous polarization, while under compressive stress the piezoelectric polarization reduces the spontaneous polarization [19].

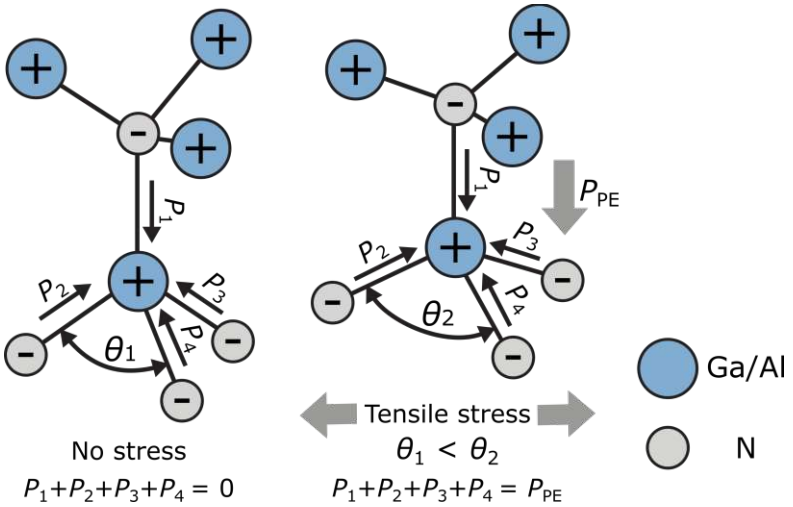

Figure 2.3: Illustration of the piezoelectric polarization due to tensile stress in the GaN crystal. Tensile stress leads to a polarization aligned with the spontaneous polarization. Picture adapted from [19]

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The total polarization $\vec{P}$ present in the GaN crystal is the vector sum of the spontaneous and the piezoelectric polarization.

$$\vec{P} = \vec{P_{\mathrm{sp}}} + \vec{P_{\mathrm{pe}}} \tag{2.1}$$

The electric field within the crystal, generated by the polarization, can be calculated using Equation 2.2, where ϵ_0 is the vacuum dielectric constant and ϵ_{r} the relative dielectric constant of the material.

$$\vec{E} = \frac{\vec{P}}{\epsilon_0 \epsilon_{\mathrm{r}}} \tag{2.2}$$

The built-in potential V_{bi} is then determined by

$$V_{\mathrm{bi}} = \vec{E} d \tag{2.3}$$

where d is the thickness of the crystal [20].

2.2 The High Electron Mobility Transistor (HEMT)

The most common type of GaN-based power electronics transistor is the High Electron Mobility Transistor (HEMT), illustrated in Figure 2.4. The substrate of choice to balance performance and profitability for this type of device is often Si (111), which is the substrate used for the devices in this thesis. Other substrates are available and their respective merits will be discussed in Section 2.4.

The first layer grown on the Si substrate is a transition layer. This is required to compensate for the relatively large mismatch of 17% between GaN and Si lattice constants and allow the growth of high quality, low defect density GaN layers. The transition layer, in combination with the carbon-doped GaN buffer epitaxially grown on top of the transition layer, isolates the electrically active region on top of the buffer from the conductive Si substrate. The GaN channel layer grown on top of the buffer, in combination with the AlGaN barrier, forms the heterostructure described in Section 2.3. A SiN-based passivation is deposited on the AlGaN barrier to protect the transistor from the environment and to passivate the surface.

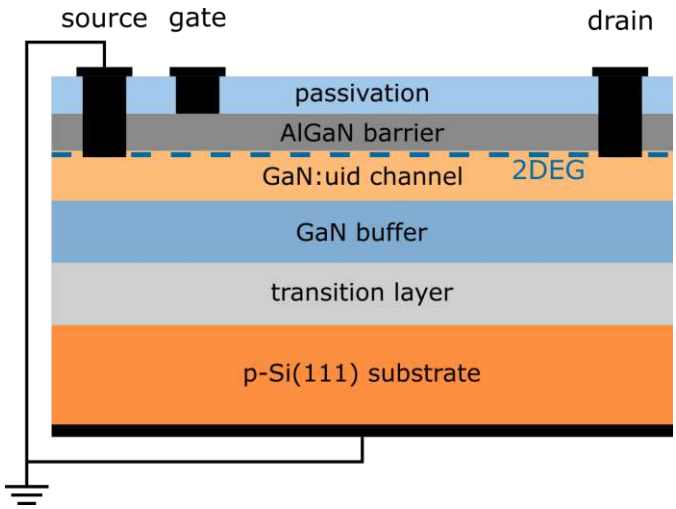


Figure 2.4: Schematic illustration of the High Electron Mobility Transistor (HEMT), the relative layer thicknesses are not to scale.

The source and drain contacts are connected via the two-dimensional electron gas (2DEG). Since the 2DEG is formed automatically upon the growth of the AlGaN barrier on the unintentionally doped GaN channel, a HEMT is, by definition, a normally-ON device. That means, that at 0 V applied to the gate, the transistor is in the ON-state, allowing current to flow between the source and drain. The application of negative voltages at the gate results in the depletion of the underlying 2DEG, thereby switching

the transistor to the OFF state.

In power electronics applications, however, a normally-OFF device behavior is strongly preferred due to safety considerations, lower driving power consumption and compatibility with existing driving circuits [21, 22]. A variety of techniques have been developed with the objective of achieving the desired characteristics. For example, fluorine implantation beneath the gate [23], a recess of the AlGaN barrier beneath the gate [24, 25] and the addition of a p-doped GaN layer beneath the gate [26, 27] have been employed to achieve normally-OFF characteristics. The combination of a normally-ON GaN HEMT with a normally-OFF Si-based transistor in a cascode configuration is also a viable method for achieving an overall normally-OFF characteristic while still capitalizing on the enhanced performance of GaN-based devices [28].

The most promising technique, and the technique on which the devices in this thesis are based, is the addition of a p-doped GaN layer beneath the gate. This device type is referred to as the Gate Injection Transistor (GIT), and will be described in detail in Section 2.6.1.

2.3 Formation of the 2DEG

The two-dimensional electron gas (2DEG) connects the source of the device to the drain, forming the channel of the device. This heterostructure forms the core building block of the HEMT and is realized by the pseudomorphic growth of a thin AlGaN barrier on top of the nominally undoped GaN layer deposited before.

The properties of III-N semiconductors, specifically the spontaneous and piezoelectric polarization, play a key role in this process. While the spontaneous polarization is present in both the AlGaN barrier and the GaN channel, the piezoelectric effect arises only in the AlGaN barrier, due to the strained crystal lattice resulting from the pseudomorphic growth.

The Al content in the barrier has a significant influence on the bandgap difference between the two materials [29], as well as the strength of the polarization effects [20]. Therefore the notation $Al_xGa_{1-x}N$ is used, where x represents the Al fraction of the material.

As discussed in Section 2.1 III-N semiconductors grow in either metal-face or nitrogen-face orientation. In metal-face orientation a negative sheet charge is present at the upper interface, while a negative sheet charge is present at the lower interface [20, 30]. This in turn results in an internal electric field (2.2), leading to slanted conduction (CB) and valence bands (VB) [31], as shown in Figure 2.5.

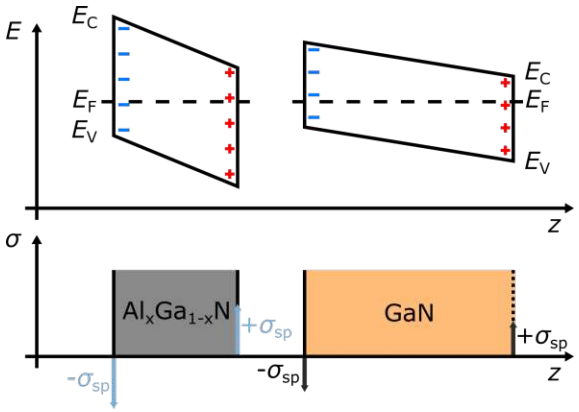


Figure 2.5: Schematic of free-standing undoped $Al_xGa_{1-x}N$ and GaN. The spontaneous polarization results in band bending of the CB and VB due to the built-in electric field.

The additional piezoelectric component, that arises when an $Al_xGa_{1-x}N$ barrier is pseudomorphically grown on the unintentionally doped GaN layer, results in an increase of the sheet charges at the $Al_xGa_{1-x}N$ surfaces. The positive sheet charge at the bottom of the $Al_xGa_{1-x}N$ layer compensates the negative sheet charge at the top of the GaN layer. This leads to a reversing of the electric field in GaN and results in a triangular potential well at the interface of the two materials, illustrated in Figure 2.6.

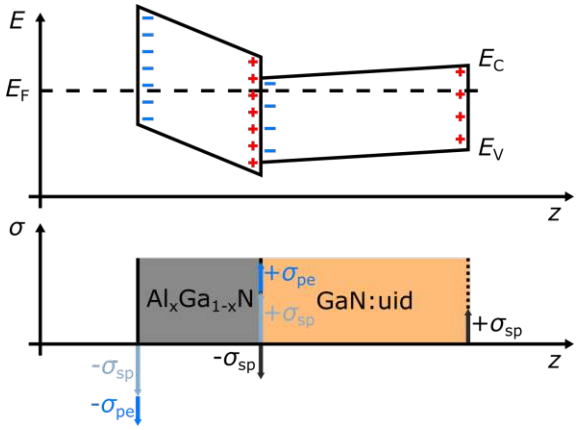


Figure 2.6: Pseudomorphic growth of the $Al_xGa_{1-x}N$ barrier on the GaN channel results in additional polarization in the barrier due to the piezoelectric effect. A triangular potential well is formed at the interface.

Free electrons will tend to accumulate at this minimum, in order to compensate the polarization induced sheet charge. This results in the formation of a 2DEG on the GaN side of the heterostructure, if the triangular quantum well drops below the Fermi level [20].

For this process to occur, a source of free electrons is required. These electron can not be thermally generated in the buffer, since it would leave positive space charges behind, resulting in a loss of electron confinement [32]. He et al. state, that the electrons for the 2DEG can not come from the $Al_xGa_{1-x}N$ barrier, because there are only few conductive electrons in undoped $Al_xGa_{1-x}N$ [31].

The accepted model therefore is, that the free electrons for the 2DEG are provided by donor-like surface states [32], illustrated in Figure 2.7. According to Smorchkova et al., the donor state energy level is located approx. 1.42 eV below the conduction band of the $Al_xGa_{1-x}N$ barrier [33]. This energy difference is denoted as E_D in the following equations. With increasing barrier thickness, the energy difference between the conduction band edge at the surface of the barrier and the Fermi level also increases. Once the surface states start to cross the Fermi level, the critical thickness (d_{CR}) of the $Al_xGa_{1-x}N$ barrier is reached and the 2DEG starts to form. The surface states get depleted and their electrons jump to the CB, where they migrate towards the potential well. The electrons form the 2DEG, while the positively charged surface states compensate the negative sheet charge at the top of the $Al_xGa_{1-x}N$ barrier, thereby reducing the internal electric field [31, 32]. An analogous process occurs with increasing the Al content in the barrier [17].

Neglecting the width of the Fermi distribution, Ibbetson et al. derive the following equation for the critical barrier thickness:

$$d_{CR} = \frac{\epsilon(E_D - \Delta E_C)}{q\sigma_{pz}} \tag{2.4}$$

where ϵ is the Al(GaN) relative dielectric constant, E_D is the energy level of the surface states with respect to the conduction band, ΔE_C is the $Al_xGa_{1-x}N$/GaN conduction band offset, q is the elementary charge and σ_{pz} ($= \sigma_{AlGaN} - \sigma_{GaN}$) is the net polarization induced sheet charge at the interface [32].

The 2DEG density n_s as a function of the barrier thickness can be calculated using the formula provided by He et al. [31]

$$n_s = \frac{\sigma_{AlGaN}}{q} - \frac{\epsilon}{q^2 d}(q\phi_b + E_g - \Delta E_C) \tag{2.5}$$

where σ_{AlGaN} is the polarization induced sheet charge of the barrier, d is the thickness of the barrier, ϕ_b is the surface barrier height and E_g is the Fermi level position with respect to the GaN conduction band edge at the $Al_xGa_{1-x}N$/GaN interface.

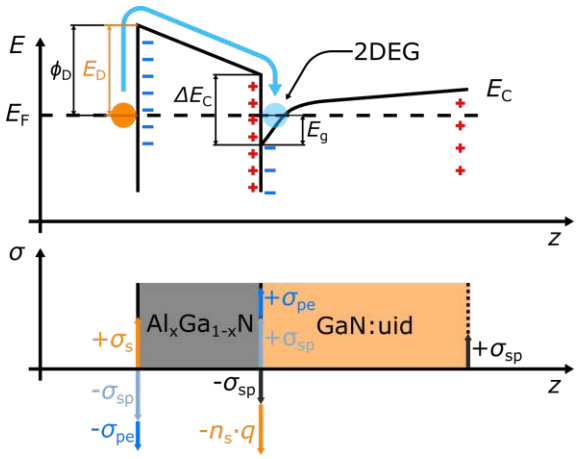


Figure 2.7: Surface donor states provide free electrons to the $Al_xGa_{1-x}N$/GaN interface, once the energy level of the surface state crosses the Fermi level. The free electrons migrate to the GaN side of the interface due to the built-in electric field and the conduction band offset, where they form the 2DEG.

For a more detailed derivation of the 2DEG density, the papers by Ibbetson et al. [32] and He et al. [31] are recommended.

Figure 2.8 shows the carrier concentration in the 2DEG, depending on thickness and the Al concentration in the $Al_xGa_{1-x}N$ barrier.

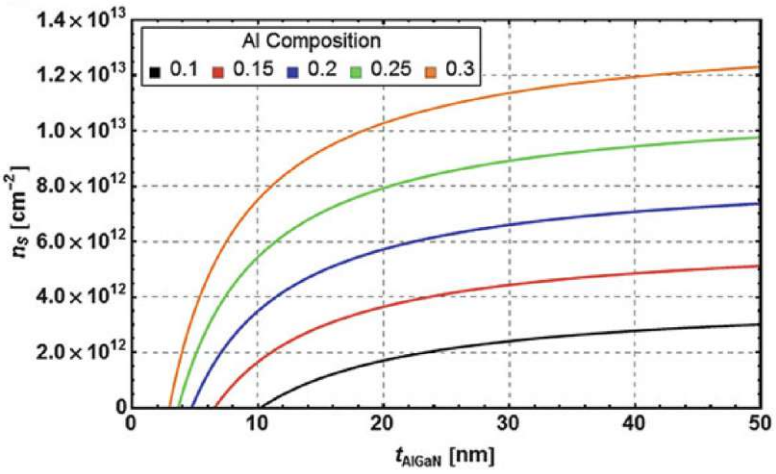


Figure 2.8: Carrier concentration at the $Al_xGa_{1-x}N$/GaN interface as a function of barrier thickness and aluminum content. Figure from [17].

2.4 GaN HEMT substrates

GaN-based devices can be manufactured on multiple different substrates, which include, but are not limited to:

- Gallium nitride (GaN)
- Silicon carbide (SiC)
- Sapphire (Al_2O_3)
- Silicon (Si)

Table 2.1 gives an overview of the most important properties of these substrates.

Property	**Sapphire**	**SiC**	**Si**	**GaN**
Lattice mismatch (%)	16	3.1	-17	0
Linear thermal expansion coefficient ($\times 10^{-6} K^{-1}$)	7.5	4.4	2.6	5.6
Thermal conductivity ($\frac{W}{cmK}$)	0.25	4.9	1.6	2.3
Cost	Cheap	Expensive	Cheap	Very expensive
Dislocation density of GaN films grown on substrate (optimized) ($\frac{1}{cm^2}$)	Low 10^8	Low 10^8	Low 10^8	$10^4 - 10^6$

Table 2.1: Properties of different substrates for GaN epitaxy [34].

Bulk GaN is the ideal substrate to manufacture GaN devices on, since it avoids complications due to lattice constant and thermal expansion coefficient mismatch. In addition, bulk GaN offers the possibility to produce vertical GaN devices, which enable higher breakdown voltages, increased power density and improved reliability [35]. The growth of large diameter bulk GaN crystals is still met with difficulties and current availability is limited to 4" diameter wafers, at very steep prices [5][36].

Research has therefore been dedicated to the fabrication of GaN-based devices on foreign substrates. Due to the relatively small lattice mismatch between SiC and GaN, as well as their comparable thermal expansion coefficients and the high thermal conductivity, SiC is a popular substrate for GaN HEMTs [5]. The high per area cost and the limitation to 6" wafers have restricted the spread of GaN-on-SiC devices to the most demanding high frequency and high power applications.

In contrast to bulk GaN and SiC substrates, sapphire is available in large diameters at relatively low cost. However, due to the low thermal conductivity of sapphire, GaN-

on-Sapphire devices are limited to applications in the low- to medium-power range and to optoelectronics.

Historically, the first devices based on GaN were developed with SiC or sapphire as substrate. Recent efforts however have been dedicated, in large part, to research on GaN devices grown on silicon [34], which is the substrate the devices used in this thesis are manufactured on.

GaN-on-Si

Si(111) is the substrate of choice for most GaN-based devices, due to its trigonal symmetry promoting the growth of GaN in the [0001] direction [37]. Crystal growth techniques like plasma-induced molecular beam epitaxy (PIMBE) and metalorganic chemical vapor deposition (MOCVD) are used to deposit high-quality GaN layers on Si substrates [38].

Due to its relative affordability, the availability of large diameter wafers and decades of intense research, silicon offers the best compromise for most applications. GaN-on-Si is compatible with the existing CMOS process and offers the possibility to combine silicon logic circuits with the power capabilities of GaN HEMTs [39, 40].

The challenges of growing GaN on Si are the relatively large mismatch of 17% between the lattice constants and the large mismatch between the thermal expansion coefficients of 54%. These mismatches lead to stress and can in turn lead to wafer bowing or cracking [41]. Various techniques have been developed to manage these stresses, and recent advancements have demonstrated the feasibility of manufacturing GaN-on-Si HEMTs on 300 mm wafers [42].

Growing GaN directly on silicon is further complicated by the tendency for island growth of GaN and an effect known as GaN melt-back etching, where the gallium from the MOCVD precursor alloys with the silicon substrate [38, 43]. To avoid these effects a AlN nucleation layer is deposited first, before the growth of GaN layers.

On top of the nucleation layer, a transition layer, also known as a stress relief layer, is grown to mitigate stress caused by lattice constant and thermal expansion coefficient mismatches and to reduce wafer bow. Four different techniques for the transition layer are illustrated in Figure 2.9. The first technique uses a graded $Al_xGa_{1-x}N$ transition layer, where the Al content is continuously reduced, while the second approach uses a AlN/GaN superlattice, where thin layers of AlN and GaN are alternatingly deposited. The third technique uses thicker AlN interlayers between GaN layers and the fourth method is to step-grade the Al content in the transition layer [34].

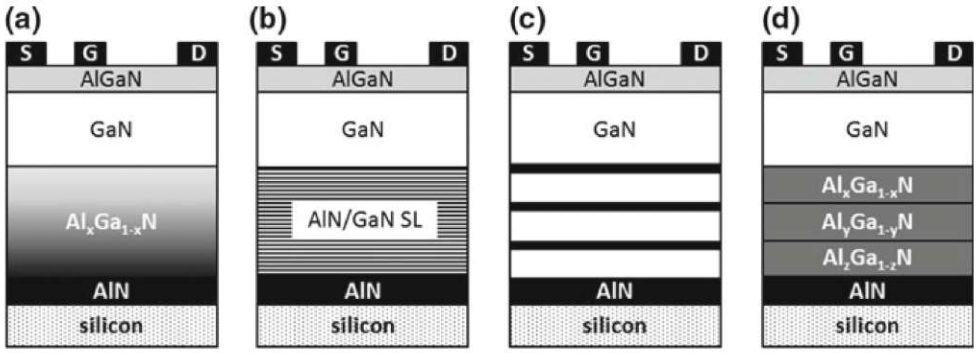


Figure 2.9: Schematic illustration of different approaches for the transition layer of GaN-on-Si HEMTs: (a) graded $Al_xGa_{1-x}N$, (b) AlN/GaN superlattice, (c) AlN interlayers, (d) step-graded $Al_xGa_{1-x}N$. Figure from [34].

The transition layer helps to manage the stress in the structure and significantly reduces the vertical threading dislocation density as can be seen in the Transmission Electron Microscope (TEM) - cross-section by Chiang et al. [44], displayed in Figure 2.10.

A GaN buffer is grown atop the transition layer. Due to background residual dopants, such as oxygen, silicon and carbon introduced during the growth process, the GaN buffer is unintentionally doped and exhibits n-type behavior. Oxygen and silicon act as a shallow donors and pin the Fermi level close to the conduction band edge of GaN, while carbon plays a more complex role and exhibits both advantageous and disadvantageous aspects [34].

Since the buffer has to insulate the electrically active region of the HEMT on top from the conductive silicon substrate, intentional doping with elements that produce deep-level donors and acceptors is required, resulting in a Fermi level pinned close to the center of the bandgap. The elements used to produce resistive buffers are iron and more commonly carbon. Experiments showed that higher vertical blocking voltages are achieved using carbon [34]. Carbon however also acts as a trapping location for electrons. This effect is discussed in more detail in Section 2.5.1. A highly resistive buffer, in concert with the transition layer, is an essential part of the HEMT and, together with the thickness of the buffer, defines the vertical breakdown voltage [34].

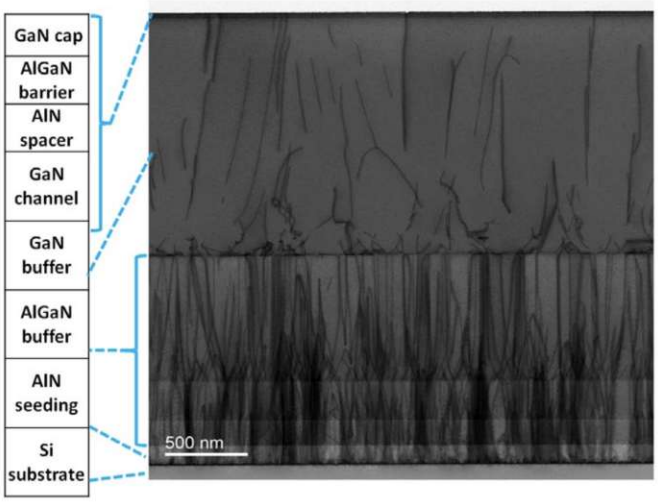


Figure 2.10: Cross-sectional transmission electron microscopic (TEM) image of a GaN-on-Si HEMT. The dislocations are visible as black lines and reduce with each subsequent layer. Image from [44].

2.5 Charge trapping dynamics in GaN HEMTs

In a pure GaN crystal in the wurtzite structure, the valence band (VB) and the conduction band (CB) are separated by a 3.4 eV bandgap with the Fermi level located in the middle [5]. However, defects and foreign element species in the crystal can lead to discrete energy levels within the bandgap. If these energy states, also known as traps, are located close to either the VB or the CB they are called shallow traps, while states deep within the bandgap are called deep-level traps. They can be further categorized into electron traps and hole traps.

As illustrated in Figure 2.11, electron traps are located in the upper half of the bandgap and therefore capture and emit mainly electrons to and from the CB, while hole traps are located in the lower half of the bandgap and primarily capture and emit holes from the VB.

The traps most commonly found in GaN-based HEMTs are:

- Point defects: due to intentional or unintentional doping, as well as crystal defects occurring during the growth process like interstitials, antisites and vacancies
- Threading dislocations: which result from distortions in the crystal lattice and can lead to increased vertical leakage [45]
- Interface traps: at the gate stack and at the AlGaN/passivation interface

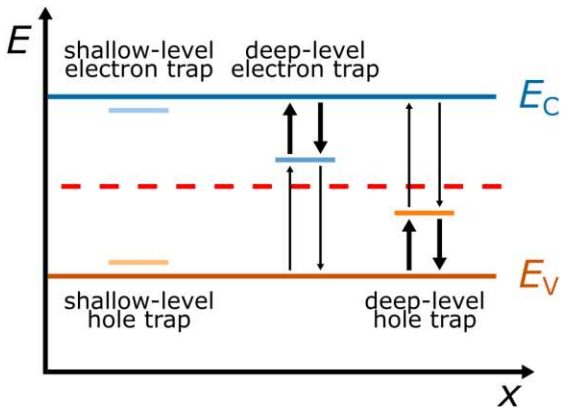


Figure 2.11: Schematic illustration of shallow-level donors with activation energies $< 0.1\,\mathrm{eV}$ to the left and deep-level donors and acceptors to the right. Image adapted from [46].

These trap states can be unintentional, like the unintentional doping from the Ga- and N-precursors and dislocations in the crystal lattice, or intentional like the doping of the buffer with carbon or the doping of the gate with magnesium. The intentional doping is used to pin the Fermi level closer to either the VB or the CB.

However, trapped charges in GaN-based HEMTs lead to a reduction of the 2DEG density and well known phenomena like current collapse, a reduction of the saturation current the device can carry, and dynamic $R_{\mathrm{DS,on}}$, an increase of the resistance in the linear operating regime of the transistor. Both effects are sides of the same coin and their influence on the device characteristics is depicted in Figure 2.12. A shift of the threshold voltage is also a common effect of trapped charges.

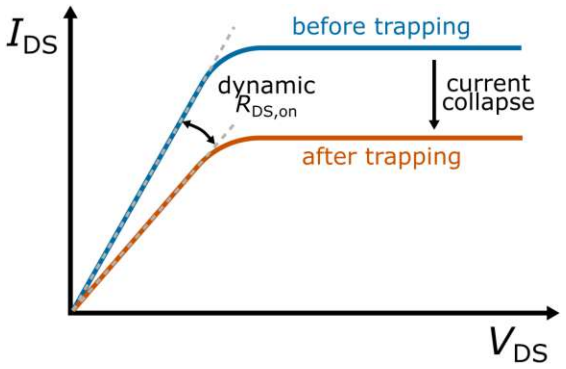


Figure 2.12: Schematic illustration of dynamic $R_{\mathrm{DS,on}}$ and current collapse, before and after charge trapping.

2.5.1 Buffer trapping

The deep-level traps due to carbon not only create a highly resistive buffer by pinning the Fermi level close to the center of the bandgap, they also provide energy states where electrons can trap during high stress conditions (for example OFF-state stress [47]). Trapped electrons in the buffer lead to a negatively charged buffer, which in turn leads to a reduction of the 2DEG density due to charge neutrality.

The primary trapping mechanism in the carbon-doped GaN buffer is considered to be due to hole emission, where electrons from the valence band gain sufficient energy to jump to the trap level [48].

2.5.2 Hot-carrier trapping

Hot-carrier trapping is an effect mainly observed during hard switching, e.g. switching from the OFF-state to the ON-state, while a high voltage is applied at the drain. It is also observed during DC semi-ON stress, which is stress condition where the gate voltage is close to the threshold voltage of the device, while high drain voltages are applied [49]. DC semi-ON stress is a condition usually not observed in real world applications, it is however a useful tool for device characterization. While the gate is in the semi-ON state, the 2DEG beneath the gate is not completely depleted, and the electrons are accelerated towards the drain by the high lateral E-field.

The large kinetic energies they acquire can lead to scattering and trapping in surface acceptor (SA) states at the AlGaN barrier/passivation interface [50, 51]. The susceptibility of the buffer to hot-carrier trapping depends on the distance of the carbon doped GaN region from the 2DEG [52].

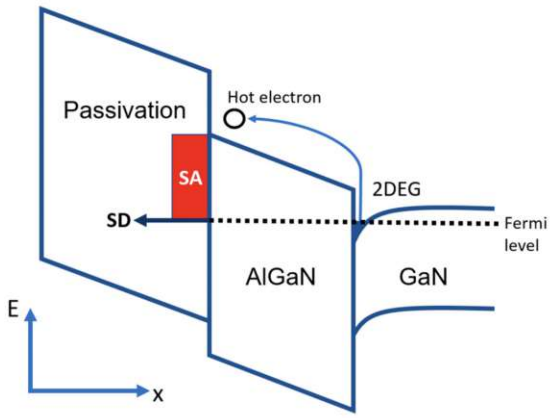


Figure 2.13: Schematic illustration of electron trapping in surface acceptor (SA) states during hard-switching events. Image from [49].

2.6 Advancements in HEMT Design

2.6.1 Gate Injection Transistor (GIT)

The Gate Injection Transistor is a device based on the HEMT operating principle that utilizes a p-doped GaN layer on top of the AlGaN barrier in the gate region. The addition of the p-doped GaN in the gate stack offers the possibility of manufacturing normally-OFF GaN HEMTs.

In 2000, Hu et al. described a novel approach to produce normally-OFF Heterojunction Field Effect Transistors (HFET) by depositing a Mg-doped p-GaN layer in the gate region [53]. Uemoto et al. developed this concept further to the so called Gate Injection Transistor (GIT), which uses a p-doped AlGaN layer to lift up the potential at the channel in the gate region and enable normally-OFF operation [26]. The latest approach for the GIT was developed by Okita et al. in 2016. It involves a complete removal of the AlGaN barrier in the gate region, followed by a regrowth of the AlGaN barrier and the p-doped GaN [54]. Using this approach, better threshold voltage reproducibility and an increased threshold voltage, without sacrificing the 2DEG density, is achieved [21].

Magnesium is typically used as dopant since it acts as acceptor when substituting for Ga, thereby producing p-type GaN [21]. As shown in Figure 2.14, an increased magnesium concentration in the p-GaN layer lifts the conduction band at the AlGaN/GaN heterojunction, thereby shifting the threshold voltage to positive values [55].

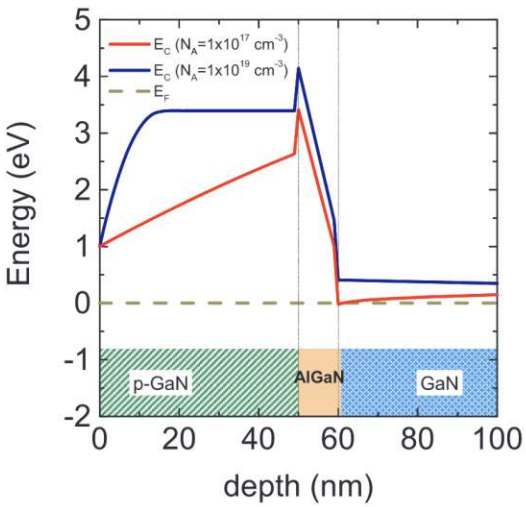


Figure 2.14: Simulated band diagrams for two different Mg-doping concentrations in the p-GaN layer. Figure from [55].

In addition to the magnesium concentration in the p-doped GaN, the barrier thickness as well as its aluminum content play an important role in determining the threshold voltage of the device. Figure 2.15 shows simulated conduction band diagrams for two different barrier thicknesses and two different Al concentrations. Taking both variables into account, a boundary between parameter pairs suitable for normally-OFF and normally-ON operation can be obtained.

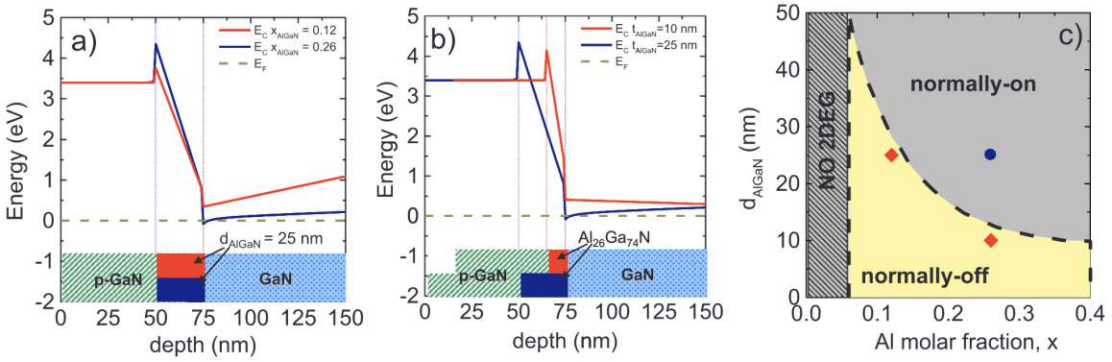
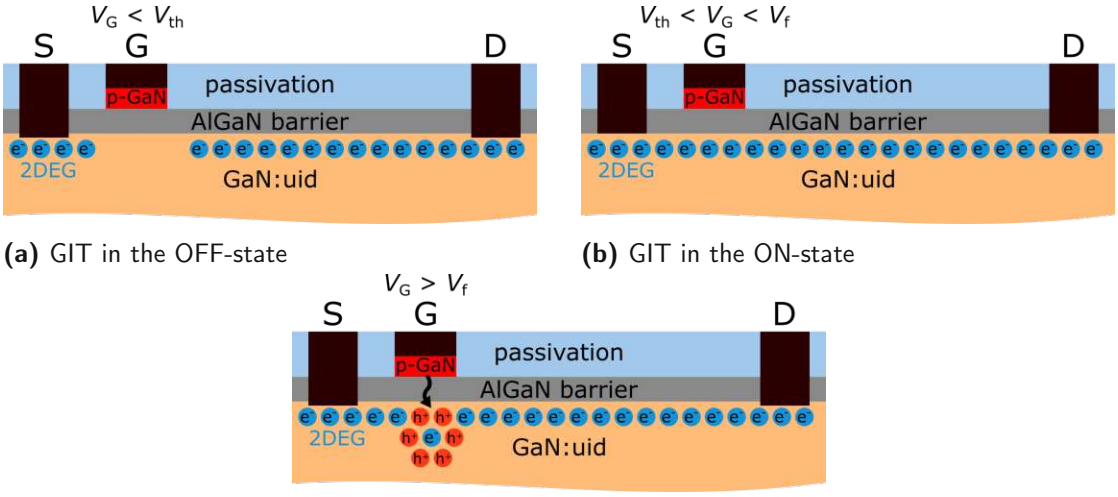


Figure 2.15: Simulated band diagrams for (a) the same AlGaN barrier thickness for two different Al molar fractions, (b) the same Al molar fraction for two different AlGaN barrier thicknesses, (c) a boundary for normally-ON and normally-OFF operation, depending on the Al molar fraction and the thickness of the barrier. Figure from [55].

The normally-ON Gate Injection Transistor has three different operating states, illustrated in Figure 2.16.

- $V_G < V_{th}$: When the voltage at the gate is smaller than the threshold voltage, the 2DEG beneath the gate is depleted and the transistor is in the OFF-state.
- $V_{th} < V_G < V_f$: When the voltage at the gate is larger than the threshold voltage of the device, but smaller than the forward built-in voltage of the gate PIN diode, the 2DEG beneath the gate is restored and current can flow from the source to the drain. The transistor is in the ON-state.
- $V_G > V_f$: For a gate voltage larger than the forward built-in voltage of the gate PIN diode, the transistor is in the ON-state and holes are injected from the p-GaN gate into the GaN buffer. This is the reason why the device is called a Gate Injection Transistor.

For the normally-OFF GIT, there are only two operating regimes, since $V_f < V_{th}$. Hole injection therefore always occurs in the ON-state.



(a) GIT in the OFF-state

(b) GIT in the ON-state

(c) GIT during hole injection

Figure 2.16: The gate injection transistor (a) in the OFF-state, (b) in the ON-state and (c) during hole injection. The state of the gate injection transistor is determined by the gate voltage (V_G) in relation to the threshold voltage (V_{th}) and the forward built-in voltage (V_f) of the gate diode.

The holes injected from the gate stack have to be compensated by an equal amount of electrons to fulfill the requirement of charge neutrality. While the holes stay in the vicinity of the gate due to their lower mobility, the electrons increase the 2DEG concentration and lead to an increase in the source-drain current. This effect is known as conductivity modulation.

Figure 2.17 shows the transfer characteristic of a normally-ON and normally-OFF GIT. The second increase of the drain current at approx. 1.3 V is clearly visible for the NON device and due to hole injection.

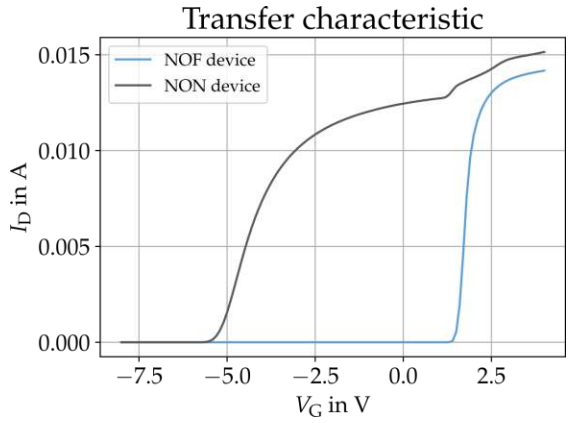


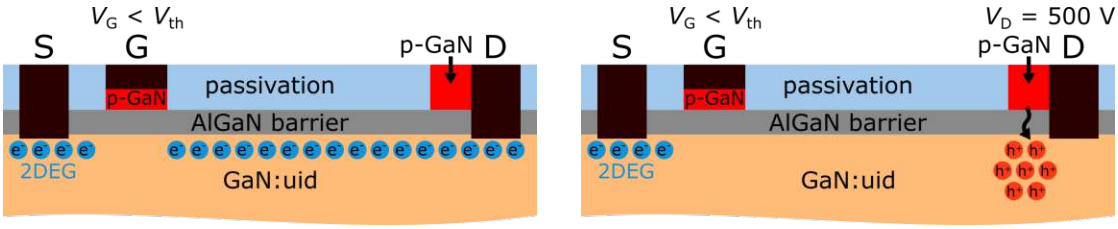
Figure 2.17: Transfer characteristic of a normally-ON (gray) and normally-OFF (blue) device.

2.6.2 Hybrid Drain-embedded – Gate Injection Transistor (HD–GIT)

The Hybrid Drain-embedded – Gate Injection Transistor (HD–GIT) is an extension of the GIT and especially suited to high-voltage operation. It features the p-doped GaN layer in the gate stack, like the GIT, but has an additional p-doped GaN region in ohmic contact with the drain, which is referred to as hybrid drain in the context of this thesis. While the AlGaN barrier beneath the gate is typically recessed to achieve the normally-OFF behavior, the barrier beneath the hybrid drain is not.

The device has the same three operating regimes as the GIT, with the influence of the hybrid drain becoming apparent while the transistor is under OFF- or semi-ON-state stress. During high-stress operation in the OFF- or semi-ON-state, the 2DEG in the gate-drain access region gets depleted. If the 2DEG is sufficiently depleted, an effective forward bias of the hybrid drain with respect to the 2DEG is realized, leading to hole injection from the hybrid drain [56]. This process is depicted in Figure 2.18

The injected holes compensate the negative charge accumulated during the stress condition, thereby suppressing the effects of current collapse and dynamic $R_{\mathrm{DS,on}}$. The measurements by Tanaka et al., shown in Figure 2.19, compare the ON-resistance of a GIT with the ON-resistance of a HD–GIT at various stress voltages, highlighting the advantages of the HD–GIT.



(a) HD–GIT in the OFF-state

(b) HD–GIT in the OFF-state during stress

Figure 2.18: The hybrid drain-embedded – gate injection transistor in the (a) OFF-state and in the (b) OFF-state under stress. The gate side operates analogous to the gate injection transistor. The additional p-GaN at the drain leads to hole injection during the off-state, if high voltage is applied at the drain.

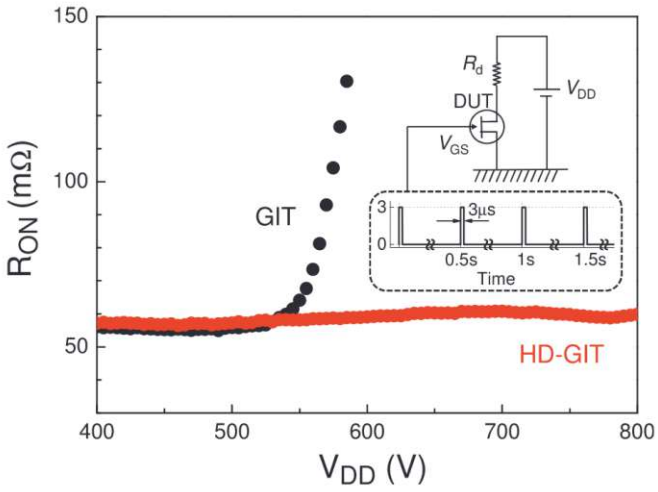


Figure 2.19: Dynamic $R_{\mathrm{DS,on}}$ after stress of a GIT (black) and a HD–GIT (red). The addition of the hybrid drain effectively mitigates the resistance increase for high stress voltages. Image from [56].

3 Experimental aspects

3.1 Measurement equipment

Table 3.1 provides a brief overview of the equipment used to conduct the measurements in this work.

Equipment	Model
Semi-automatic probestation	MPI TS3000HP
SourceMeter	Keithley 2636B
High-voltage SourceMeter	Keithley 2657A
Oscilloscope	Tektronix MSO44
Passive probe	Tektronix TPP1000
High voltage differential probe	Tektronix THDP0200

Table 3.1: Equipment used for the electrical characterization in this thesis.

Semi-automatic probestation

The semi-automatic probestation, termed *Semiprober*, is a MPI TS3000HP. It is a machine for semi-automatic, on-wafer device characterization and is capable of performing tests on wafers up to 300 mm in diameter, which are held in place by a vacuum. The machine is outfitted with a thermostatic chuck enabling measurements in the −60 °C to 210 °C range. To prevent condensation on the sample during measurements below the dew point, the test chamber is purged using compressed dry air.

Up to eight needles, mounted on manually adjustable manipulators, can be used to contact the device, while a digital microscope with adjustable magnification provides a top-down view of the structures. A user-generated wafer map enables automatic stepping between devices located on the wafer.

When used in combination with a Keithley 2657A SMU, up to 3 kV can be applied at the device, while an enclosure and an interlock system mitigate risks to the user.

Source-Measurement-Unit (SMU)

Source-Measurement-Units are electronic test equipment widely used in various fields ranging from semiconductor device testing and analysis to battery testing and simulation. At their core, SMUs are high-precision voltage or current sources, capable of measuring currents and voltages respectively with high accuracy.

They usually have a tight volumetric integration which allows for compact test setup design and their tight logical inter- and cross-device integration allows for accurate time synchronization and complex measurement procedures. These characteristics make SMUs

a staple in almost every lab working with electronic devices. The SMUs used in this work are the Keithley 2636B, capable of supplying up to 200 V, and the Keithley 2657A, capable of supplying up to 3 kV. Throughout this work, the Keithley 2636B is referred to as *standard SMU* or *low-voltage SMU*, while the Keithley 2657A is referred to as *high-voltage SMU*. The term *low-voltage* for the Keithley 2636B is technically inaccurate, since it typically applies to voltages below 40 V. However, it is used for clarity and ease of distinction between the two devices.

All SMUs are connected using a TSP-link, which enables time synchronization to within 500 ns.

Measurement software

An in-house developed measurement software, called *KAICAMS*, was used to perform the measurements.

KAICAMS is a graphical front-end, designed to enable researchers in the laboratory to easily define measurement sequences in Lua, a full-fledged and easy-to-learn scripting language. The software is programmed in LabVIEW and has a modular back-end to enable integration of new equipment and measurement procedures.

The primary commands used in this work are *base.livesweep*, which performs a voltage or current sweep on one SMU, while applying a constant bias on the other channels, and *base.stress*, which applies constant voltages or currents on all channels for the desired time interval.

3.2 Measurement techniques

Two measurement techniques were used to characterize the devices in this thesis.

Voltage Sweep

Voltage sweeps are essential in semiconductor device characterization, and used throughout this work. The basic principle is that a current or voltage is increased in steps while the resulting change in voltage or current is measured on the same or on a different channel.

The transfer characteristic is one of the most important properties of every semiconductor device and an example is shown in Figure 3.3a. In this measurement, the voltage is swept on the gate and the corresponding drain current is measured. After plotting the drain current over the gate voltage, the threshold voltage (V_{th}) of the device and the drain current at the respective gate voltages can be extracted.

Another important use case for voltage sweeps is to measure the diode characteristic of the gate, which is shown in Figure 3.3b. As before, the voltage applied to the gate is increased in steps, while the current flowing through the gate is measured. Plotting the gate current versus the voltage results in the diode characteristic, from which the built-in forward voltage V_{f} and the current at specific gate voltages can be extracted.

Measurement-Stress-Measurement Technique

The measurement-stress-measurement technique is used to assess the impact of electrical stress on the ON-resistance ($R_{\mathrm{DS,on}}$) and threshold voltage (V_{th}) of a transistor. The basic structure of the measurement sequence for the normally-ON HEMT used in the thesis is described in this section, while variations to this sequence are described separately in the specific sections. The technique consists of a reference phase, followed by a stress phase and finishes with a recovery phase.

In the reference phase, the initial $I_{\mathrm{D,on}}$, which is connected to $R_{\mathrm{DS,on}}$ via $V_{\mathrm{DS}}/I_{\mathrm{D}}$, of a fully recovered device is measured. For this phase, 0 V is applied at the gate, while a small voltage is applied at the drain. The current measured in this phase is used as a reference to calculate the degradation as a result of stress.

In the stress phase, the transistor is switched to the OFF- or semi-ON-state by applying the appropriate voltages at the gate. To place the transistor in the OFF-state, a gate voltage sufficiently below the threshold voltage is necessary, while setting a gate voltage similar to the threshold voltage places the transistor in the semi-ON-state. High drain voltages are then applied, which result in charge trapping in the GaN buffer if the transistor is in the OFF-state. If the transistor is in the semi-ON-state, charge trapping occurs in both the buffer and the passivation/AlGaN barrier interface [57]. To minimize self-heating effects of the device during semi-ON-state stress, $I_{\mathrm{D,str}}$ was limited to the 100 µA range in this work.

The influence of these trapped charges is assessed by measuring the drain current in the recovery phase, under the same conditions as in the reference phase.

Figure 3.1a shows a schematic illustration of these three phases, with the drain voltages indicated in orange, while the gate voltages are indicated in blue. Figure 3.1b shows the results using this technique. The dashed red line indicates the reference current measured in the reference phase, while the blue line shows the current measured in the recovery phase. The degradation D (in percent) is then calculated using Equation 3.1, where $I_{\mathrm{D,0}}$ is the first current reading in the recovery phase and $I_{\mathrm{D,ref}}$ is the current measured in the reference phase.

$$D = (1 - \frac{I_{\mathrm{D,0}}}{I_{\mathrm{D,ref}}}) \times 100 \tag{3.1}$$

Over time, the electrons de-trap either thermally, or via the injection of holes into the device. The time constant of this recovery can be extracted by plotting the drain current versus time. This can be accomplished by either fitting an appropriate exponential function, or, as a good approximation, finding the largest slope of the transient in a logarithmic plot.

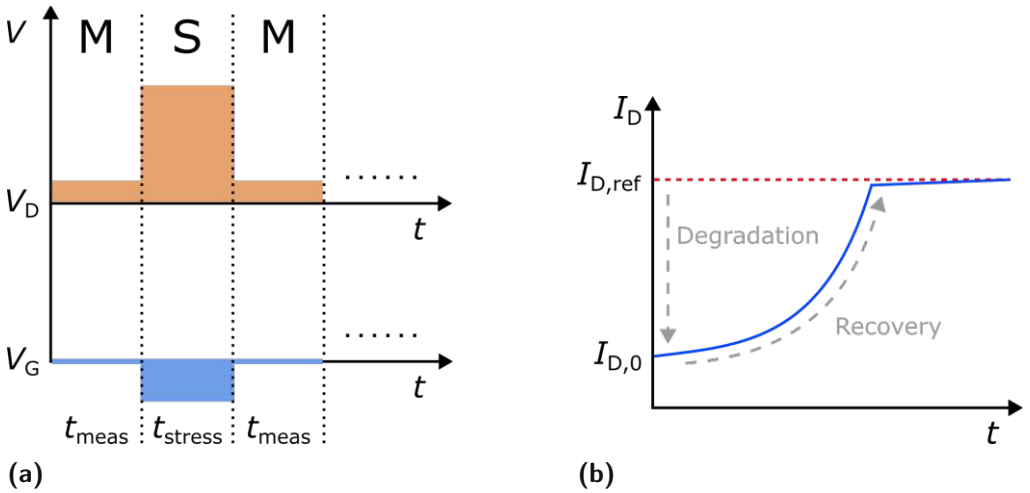


Figure 3.1: (a) Schematic illustration of the measurement-stress-measurement sequence and (b) a typical current transient as a result of this technique. The dashed red line shows the current measured in the reference phase $I_{\mathrm{D,ref}}$. The blue line shows the current after stress, measured in the recovery phase, with the first current reading $I_{\mathrm{D,0}}$.

3.3 Devices under test

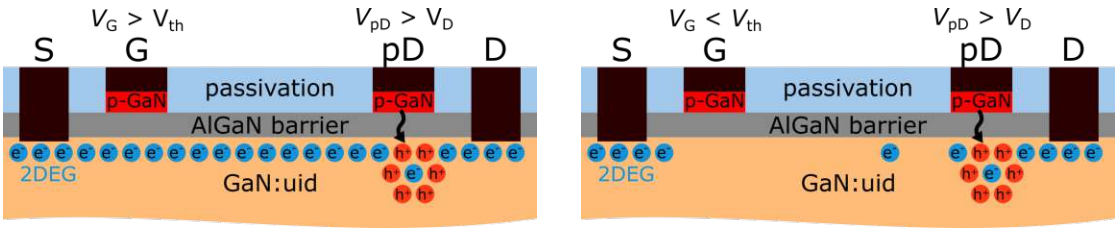
3.3.1 Separate p-drain – Gate Injection Transistor

The device used for Section 4.3 of this work is a normally-ON, separate p-Drain – Gate Injection Transistor, illustrated in Figure 3.2. It combines the p-doped GaN underneath the gate of the GIT, described in Section 2.6.1, with the p-doped GaN in the gate-drain access region, similar to the hybrid-drain described in Section 2.6.2.

The gate operates like a normally-ON gate in a GIT, while the p-doped GaN in the gate-drain access region is separated from the drain terminal and referred to as *p-drain*, compared to the hybrid drain which is in ohmic contact with the drain. Since the p-drain is separated from the drain, it can be addressed individually by an SMU, enabling active control of the hole current injected in the sep. p-drain-GIT. The amount of holes injected is determined by the forward bias of the p-drain with respect to the drain, denoted ΔV_{pD} in this thesis.

This configuration enables novel modes of operation, illustrated in Figure 3.2. Namely hole injection in the ON-state from a different site compared to the GIT and actively controlled hole injection in the OFF-state. Active hole injection in the sep. p-drain-GIT is possible while the 2DEG underneath the p-drain is not depleted and a forward bias of the p-drain with respect to the drain is applied. During high-stress conditions, the 2DEG underneath the p-drain gets depleted, therefore a forward bias at the p-drain is

not necessarily required for hole injection to occur. This mode of operation is analogous to the passive hole injection in a HD-GIT, which only occurs during high stress when the 2DEG underneath the hybrid-drain is depleted. With $\Delta V_{\mathrm{pD}} = 0\,\mathrm{V}$ the device essentially operates like a HD-GIT.



(a) sep. p-drain–GIT in the on-state

(b) sep. p-drain–GIT in the off-state during stress

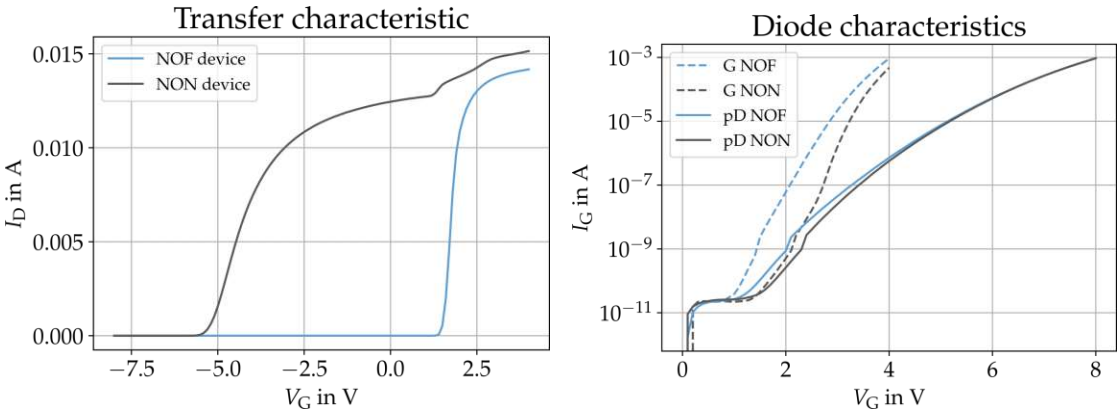
Figure 3.2: The separate p-drain–gate injection transistor in the (a) ON-state and in the (b) OFF-state. The gate side operates analogous to the GIT. Hole injection can also occur from the p-drain if $V_{\mathrm{pD}} > V_{\mathrm{D}}$, in either the ON-state or the OFF-state.

Figure 3.3 shows the transfer characteristic and the diode characteristics of both the normally-ON sep. p-drain-GIT, used for the measurements in this thesis, and the normally-OFF type. In Figure 3.3a, the gray line represents the transfer characteristic of the normally-ON transistor with a threshold voltage of $-5.3\,\mathrm{V}$. An additional increase in the drain current is observed at approx. $1.3\,\mathrm{V}$, which is the conductivity modulation aforementioned in Section 2.6.1. The blue line shows the transfer characteristic of the normally-OFF version of this device, with a threshold voltage of $1.5\,\mathrm{V}$. The normally-ON device type was used for the measurements in this thesis, since the transistor can be placed in the ON-state without hole injection from the gate.

Figure 3.3b shows the gate and the p-drain diode characteristics for both device configurations, with the normally-ON and the normally-OFF measurements again in gray and blue respectively. For all diode measurements, we observe a current below the resolution limit of the SMU, for forward biases below $0.9\,\mathrm{V}$. The current of the normally-OFF gate diode starts to increase above the resolution limit of the SMU for voltages larger than $0.9\,\mathrm{V}$, while the normally-ON gate diode shows currents above the resolution limit for voltages larger than $1.3\,\mathrm{V}$. A small discrepancy in the p-drain diode characteristic between the two variants is observed, attributed to device-to-device variation, as the processing of the p-drain diode is identical for the normally-OFF and normally-ON device.

At higher voltages the diode characteristics for the normally-OFF gate and the p-drain start to converge with their normally-ON counterpart.

There is a marked difference between the gate diode and the p-drain diode characteristic, due to different metals deposited above the p-GaN layer. At the same voltage level, a significantly higher hole current is observed for the gate compared to the p-drain diode.



(a) **(b)**

Figure 3.3: (a) Transfer characteristic of the sep. p-drain–GIT, normally-ON in gray ($V_{\text{th}} = -5.3\,\text{V}$) and normally-OFF in blue ($V_{\text{th}} = 1.5\,\text{V}$), (b) with their respective gate and p-drain diode characteristics.

3.3.2 Device with laterally spaced TLM structures

To investigate the lateral hole transport properties outside the active HEMT area, four different configurations of the device with laterally spaced TLM (Transfer Length Method) structures were available. A schematic of the general structure of these devices is shown in Figure 3.4.

It consists of a normally-ON HEMT in the center of the device, with four TLM structures located to both sides of the HEMT. The group of TLM structures to the left of the HEMT is omitted to streamline the schematic.

In essence, TLM structures are resistors, and their total resistance can be calculated using Equation 3.3. It consists of the contact resistance of the two pads in series with the resistance of the 2DEG. These TLM structures form an ohmic contact to the 2DEG and are usually used to determine the contact resistance of the device. In our case however, these resistors were used to measure the change in the TLM current (I_{TLM}), and therefore the change in 2DEG resistivity, due to holes diffusing under the structures.

$$R_{\text{tot}} = 2 \times R_{\text{contact}} + R_{\text{2DEG}} \tag{3.2}$$

$$I_{\text{TLM}} = \frac{V_{\text{TLM}}}{R_{\text{tot}}} \tag{3.3}$$

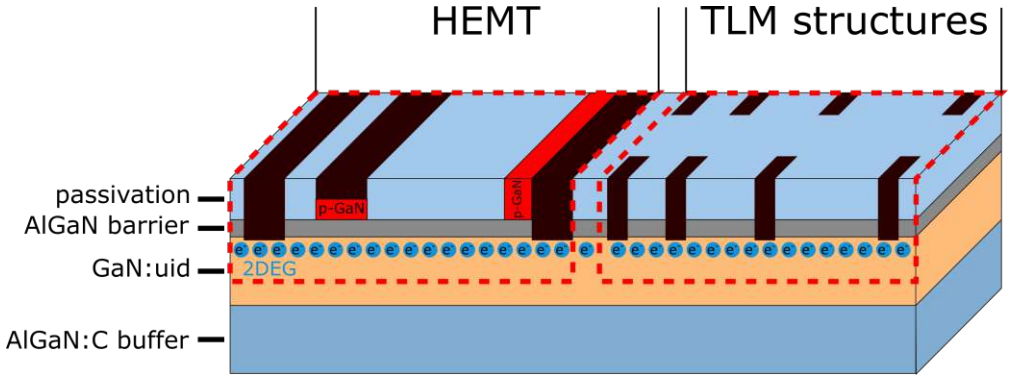


Figure 3.4: Device with laterally spaced TLM structures. The HEMT is drawn on the left, four laterally spaced TLM structures are drawn to the right of the HEMT. In the actual device, the HEMT is located at the center, while four TLM structures are located to each side.

Two different epitaxial stacks with two different methods for inhibiting the 2DEG between the HEMT and the TLM structures were available for a total of four different configurations. The difference in the stack is the inclusion of an AlGaN back-barrier between the GaN:uid and the AlGaN:C buffer layer, compared to the usual stack described in Section 2.2. The addition of the back-barrier provides a prime accumulation site for holes and is expected to increase hole mobility significantly, potentially leading to the formation of a 2D hole gas (2DHG), which is comparable to the 2DEG, but with positive charge. In Figure 3.5a the device is shown without the additional back-barrier, while in Figure 3.5b it is shown with the back-barrier.

The second difference is the method of 2DEG inhibition, which is necessary to prevent current flow between the HEMT and the TLM structures, thereby enabling high-voltage measurements. The first method involves the use of ion implantation to destroy the crystal structure, thereby preventing the formation of the 2DEG. The second method uses a partial barrier recess between the HEMT and the TLM structures, similar to the technique used to manufacture normally-OFF GaN HEMTs. Due to the reduced thickness of the AlGaN barrier, a stronger electric field within the barrier arises, which compensates a larger portion of the polarization charges and thereby reducing the 2DEG density [17].

During the measurements, we observed that the 2DEG was not completely suppressed by the partial barrier recess, which prevented high-voltage measurements. Measurements at low voltage, however, could still be conducted and provided valuable insights.

Figure 3.5a shows the device with ion implantation, where the 2DEG is fully destroyed, while Figure 3.5b shows the device with a partial barrier recess and a partially depleted 2DEG.

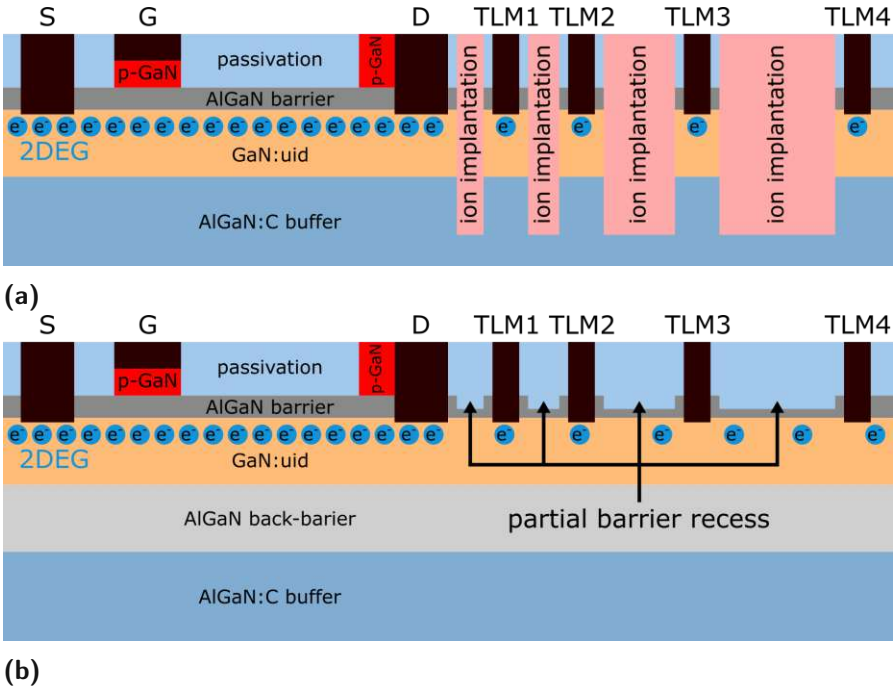


Figure 3.5: (a) The device without back-barrier and ion implantation between the HEMT and the TLM structures and (b) the device with back-barrier with a partial barrier recess between the HEMT and the TLM structures. The back-barrier is approximately as thick as the GaN:uid layer.

3.4 Measurement setups

Two different setup configurations were investigated for their relative strengths, weaknesses and their possible application for the measurements in this thesis.

3.4.1 Standard setup with floating p-drain SMU

The standard setup with a floating p-drain SMU consists of two Keithley 2636B, with two channels each. Figure 3.6 shows the wiring diagram of this setup.

SMU3 is directly connected to the gate of the HEMT, while SMU4 is connected to the source as well as the substrate. The most important aspect of this configuration however is the connection of the high from SMU1 not only to the drain of the HEMT, but also to the low of SMU2 which in turn is connected to the p-drain.

Since the p-drain SMU is floating on the high of the drain, voltage changes at the drain are automatically tracked by the p-drain if 0 V is applied. However, if hole injection into the HEMT using the p-drain is required, the voltage of the p-drain SMU can be increased and the resulting hole current can be directly inferred by consulting Figure 3.3b.

In this standard setup, ΔV_{pD}, the difference between V_{pD} and V_{D}, is directly controlled by one SMU.

The SMUs used in this configuration can supply up to 200 V, which is technically too small to observe hot carrier degradation at the surface. However, by changing the procedure, the effective V_{DS} can be increased to 380 V. This increase in the stress voltage is achieved by applying −190 V at the source and the substrate, effectively setting a new reference and increasing $V_{\mathrm{DS,eff}}$ to 380 V, with 10 V of margin in both directions. Another important aspect to consider is that Kirchhoff's Current Law (Equation 3.5) must be applied to determine the actual drain current, since both the p-drain current and the drain current are measured by the drain SMU.

$$I_{\mathrm{measured}} = I_{\mathrm{D}} + I_{\mathrm{pD}} \tag{3.4}$$

$$I_{\mathrm{D}} = I_{\mathrm{measured}} - I_{\mathrm{pD}} \tag{3.5}$$

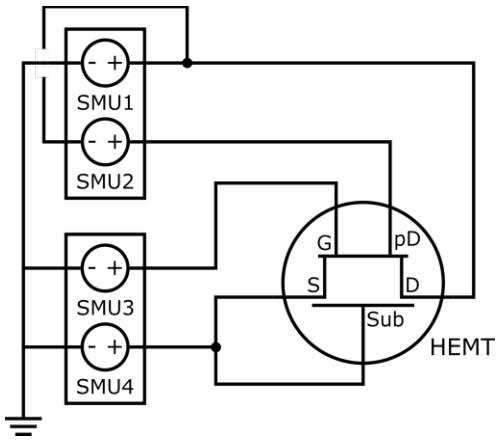


Figure 3.6: Schematic circuit diagram for the standard setup with floating p-drain SMU.

3.4.2 High-voltage setup with independently controlled p-drain SMU

The high-voltage setup consists of two Keithley 2657A high-voltage SMUs and one Keithley 2636B with two channels. All three devices work in concert with a Keithley 8020 protection unit, designed to protect the electronics of the Keithley 2636B from the high-voltage SMU. A LO connection box is connected to the protection unit and provides a common ground for both high-voltage SMUs and the low-voltage SMUs.

The wiring diagram of this setup is shown in Figure 3.7. To simplify the diagram, the protection unit is split in two parts, with an encircling dashed line to indicate that they are part of one device. In this configuration, the drain and the p-drain are each connected to one of the high-voltage SMUs, while the gate and the source/substrate are connected to the low-voltage SMUs. Using this setup, up to 3 kV can be applied during the stress phase.

As in the standard setup, the relevant voltage difference for hole injection is ΔV_{pD}, which in this case has to be calculated using Equation 3.6. Both V_{D} and V_{pD} are controlled independently and ΔV_{pD} is a result of the individual high-voltage SMU biases.

$$\Delta V_{\mathrm{pD}} = V_{\mathrm{pD}} - V_{\mathrm{D}} \tag{3.6}$$

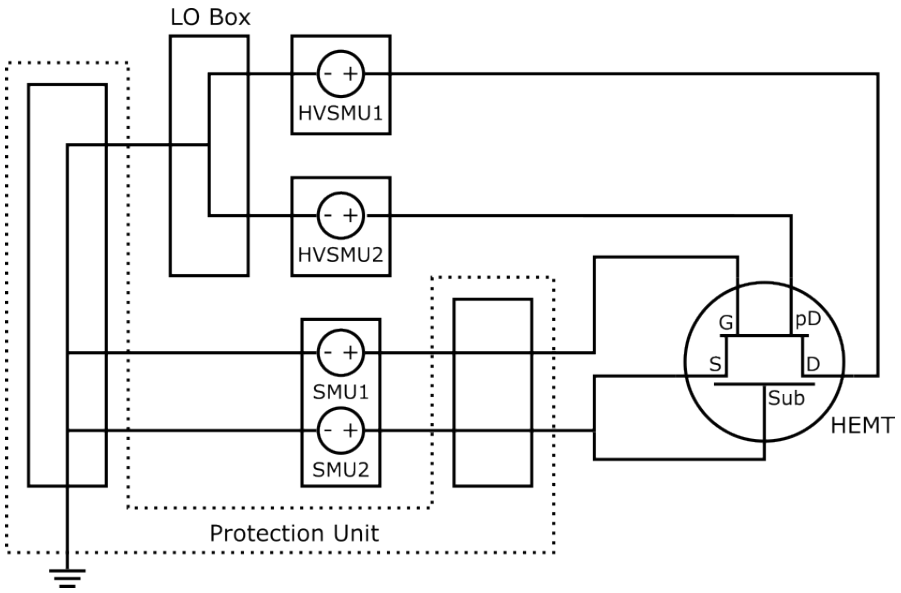


Figure 3.7: Schematic circuit diagram for the high-voltage setup with independently controlled p-drain SMU. To simplify the diagram, the protection unit is split in two parts, with an encircling dashed line.

4 Results and discussion

4.1 Voltage transitions for the different setup configurations

There are three important aspects which have to be considered for the voltage transitions between the different phases:

1. Soft-switching between the phases
2. Forward bias at the p-drain only during the intended phases
3. behavior of ΔV_{pD} during the transitions

Soft-switching is a term usually used in the context of alternating current and means, that the transistor is switched near the zero-crossing of the AC voltage. This switching mode is advantageous because it leads to improved lifetime and less stress on the device compared to hard-switching, where the transistor is switched while high voltages are applied to the drain. In our case, three phases, with static voltages in each phase, are used. Soft-switching here means, that the gate of the transistor is switched to the OFF-state or to semi-ON-state, before a high voltage is applied at the drain. This is accomplished using the *tholdbaseX* parameter of the *base.stress* command, where X is a placeholder for the channel the command applies to.

For the transition between the reference and the stress phase, *tholdbaseD* holds the reference phase voltage level of the drain for a specified time, while the other channels apply the stress phase voltage level immediately. The gate of the HEMT is therefore in the semi-ON-state before high voltages are applied. Conversely, for the transition from the stress phase to the recovery phase, *tholdbaseG* delays the switch from semi-ON-state to the ON-state, until the drain voltage is reduced to the recovery phase voltage of 0.5 V.

Concerning the second aspect, for the majority of the phases the correct forward bias can easily be guaranteed. During the switching between the phases, however, the timing parameters have to be set correctly to avoid unintentional hole injection, using the *thold* commands.

The third aspect is difficult to control and has to be studied carefully, especially in the high-voltage setup, since ΔV_{pD} is a function of V_{D} and V_{pD} which are controlled independently. This means that small differences in the SMU response times, due to impedances connected to the respective SMU channels, can lead to large effective biases at the p-drain.

The correct sequence for the switching between the phases is shown in Figure 4.1.

The blue line shows the gate, with the respective gate voltages annotated underneath the line, while the orange line shows the drain, with the respective drain voltages annotated above the line. The delays $t_{\mathrm{hold,D}}$ and $t_{\mathrm{hold,G}}$ are shown above the gate and drain voltages.

The dashed gray curve shows the intended intervals of forward bias, if hole injection is desired in the ON-state. The solid gray curve shows the interval when forward bias is intended during the stress phase.

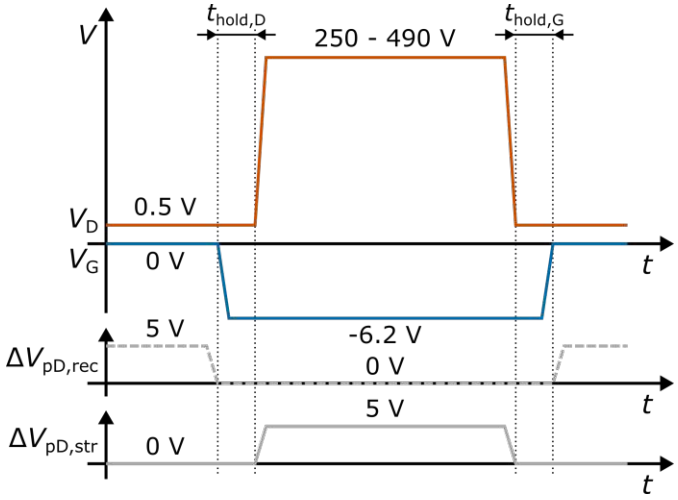


Figure 4.1: Timing for the drain and gate to ensure soft-switching between the phases at the top in orange (drain) and blue (gate). ΔV_{pD} if forward bias is desired in either the reference and recovery (dashed) or the stress (solid) phase below.

Since SMUs are non-ideal devices, with different characteristics, depending on small variations of their internal components as well as variance of the impedances of connected devices, the same command can lead to slightly different response characteristics in their output. This behavior is particularly important for the rise times of the drain and the p-drain bias since their difference, ΔV_{pD}, is what determines the amount of injected holes. Generally, if the exact same response cannot be guaranteed, it is preferable, that the drain voltage is higher than the p-drain voltage. This results in a reverse bias, where current flow is inhibited by the p-drain diode, therefore affecting the results not significantly.

Figure 4.2 shows, that the p-drain diode blocks current during reverse bias effectively up to at least $-60\,\mathrm{V}$. Conversely, even if small forward biases lead to a significant hole injection and would therefore affect the results.

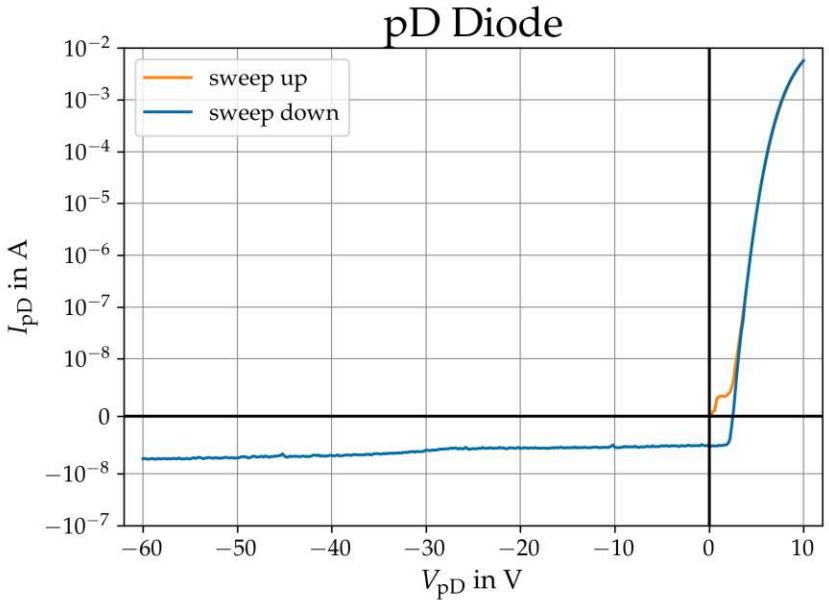


Figure 4.2: P-drain diode characteristics measured using a voltage sweep from $0\,\mathrm{V}$ to $10\,\mathrm{V}$ (sweep up) and then to $-60\,\mathrm{V}$ (sweep down), with the drain grounded. A 'sym-log' plot with linear interpolation near the zero-crossing is used. The negative current observed for small forward biases during the down sweep results from positive buffer charging during the up sweep.

4.1.1 P-drain forward bias during the stress phase

Figure 4.3 shows the transitions between the three phases, for the standard setup with the floating p-drain SMU. The transitions were measured using an oscilloscope and high-voltage differential probes connected to the probe needles. The is gate referenced to the source and the p-drain is referenced to the drain. Since the p-drain is referenced to the drain, the observed quantity is ΔV_{pD}.

Positive ΔV_{pD} means that hole injection (HI) occurs, while the current for negative voltages is blocked by the p-drain diode. To measure timing between the phases, $-6.2\,\mathrm{V}$ at the gate was defined as semi-ON-state and $5\,\mathrm{V}$ forward bias of the p-drain was desired during the stress phase.

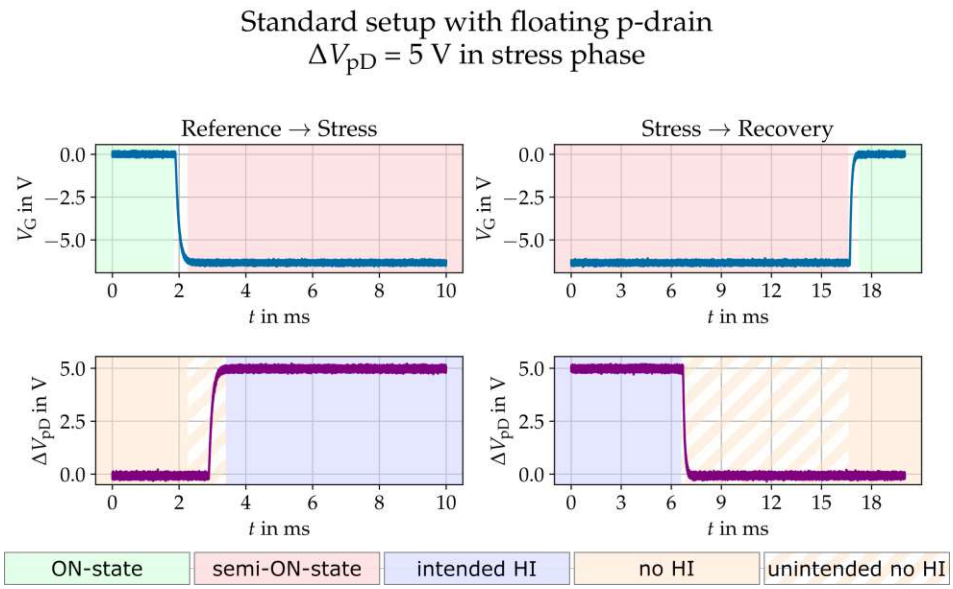
The transitions for the standard setup with a floating p-drain SMU and hole injection during the stress phase are displayed in Figure 4.3a. A sharp transition between $0\,\mathrm{V}$ and $-6.2\,\mathrm{V}$ for the gate, and between $0\,\mathrm{V}$ and $5\,\mathrm{V}$ for ΔV_{pD} is observed. The delay between the switching of the gate to the onset of hole injection is approx. $1\,\mathrm{ms}$ and the delay between the end of hole injection and the switching of the gate is approx. $10\,\mathrm{ms}$.

During these $10\,\mathrm{ms}$, the transistor is already undergoing a thermal recovery processes, which is not recorded. However, since the first datapoint of the recovery phase, obtained by the SMU measurement, is at approx. 80 ms, this does not affect the measurement data noticeably. The period of forward bias at the p-drain is contained entirely within the stress phase.

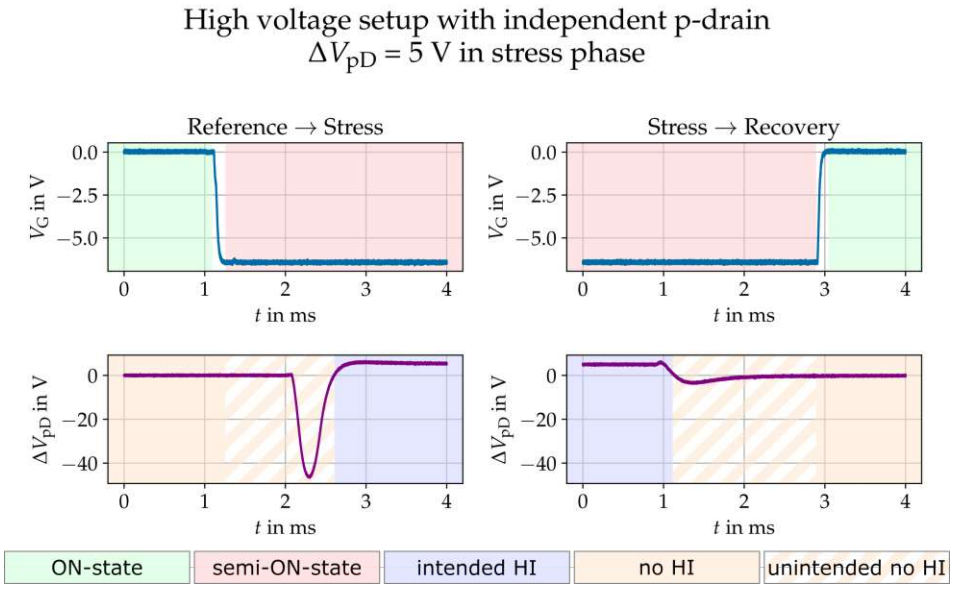
Figure 4.3b shows the transition for the gate and ΔV_{pD} using the high-voltage setup where the drain and the p-drain are controlled independently.

The behavior of the gate is similar to the standard setup, however, the transitions for ΔV_{pD}, especially during the transition from the reference to the stress phase, show a period of $1\,\mathrm{ms}$, where up to $-45\,\mathrm{V}$ of ΔV_{pD} is measured. For the transition from the stress to the recovery phase, a less pronounced reverse bias is observed.

This behavior is due to the previously mentioned small differences in the internal and external impedances of the SMUs and could not be mitigated. However, the measured voltage spikes are in reverse bias and a current flow is therefore blocked by the p-drain diode. The time between the switching of the gate to the onset of hole injection is approx. $1\,\mathrm{ms}$, while the delay between the end of hole injection and the switching of the gate is approximately $2\,\mathrm{ms}$. The period of hole injection from the p-drain is again contained entirely within the stress phase.



(a)



(b)

Figure 4.3: Transitions between measurement phases for the (a) standard setup with floating p-drain and the (b) high-voltage setup with independently controlled p-drain. Hole injection (HI) from p-drain only occurs during the periods, where the transistor is switched to the semi-ON-state. The voltage at the gate is displayed in blue, while ΔV_{pD} is displayed in gray.

4.1.2 P-drain forward bias during the reference and recovery phase

In these measurements hole injection is intended during the reference and recovery phase.

For the measurements of the standard setup with the floating p-drain SMU, displayed in Figure 4.4a, a sharp transitions of the gate voltage and ΔV_{pD} is observed. However, the forward bias of the p-drain continues 1 ms into the stress phase and starts 10 ms before the transistor is switched to the reference phase.

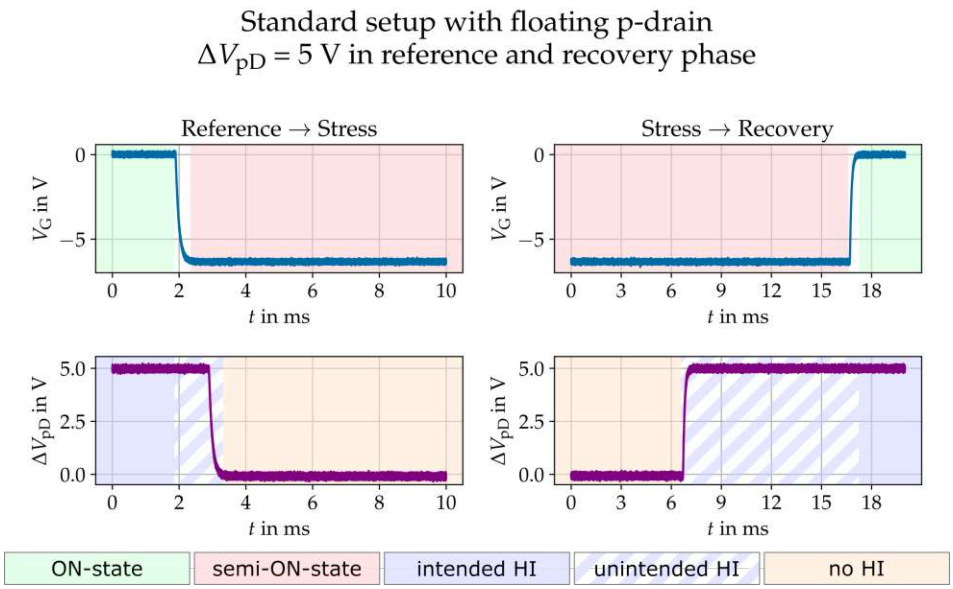
Comparing this behavior to the intended behavior described in Figure 4.1 we notice, that in total 11 ms of additional hole injection occurs during the stress phase. The forward bias at the p-drain of 5 V is already applied before the transistor is switched to the ON-state, however such small drain voltages are not considered to be hard switching.

Comparing the additional hole injection time at the end of the stress phase of 10 ms to the 80 ms delay before the first datapoint is recorded, we find that only the shortest time constants are affected. For time constants from the 1 s range onward, the influence is less than 1%, which is smaller than the reading error when extracting the time constants.

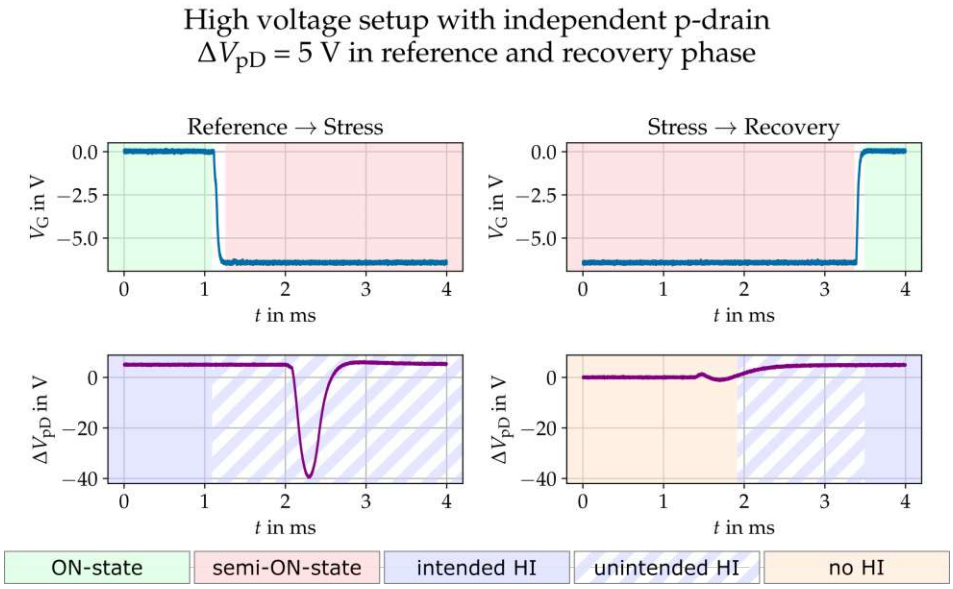
For the transitions using the high-voltage setup with the independently controlled p-drain, displayed in Figure 4.4b, we observe similarities to the standard setup. Hole injection continues into the stress phase and starts before the recovery phase.

During the transition from the reference to the stress phase a period of 1 ms of reverse bias of the pD diode is observed, followed by an exponential decay of the forward bias, which is expected to take less than 10 ms. Current during the period of reverse bias is again blocked by the p-drain diode.

For the transition from the stress to the recovery phase, only minor fluctuations of ΔV_{pD} are observed and the additional hole injection period during the stress phase lasts approximately 1.5 ms, which is significantly shorter than the delay of 80 ms before the first current reading.



(a)



(b)

Figure 4.4: Transitions between measurement phases for (a) the standard setup with floating p-drain and (b) the high-voltage setup with independently controlled p-drain. Hole injection (HI) from p-drain occurs during the reference and the recovery phase, with short periods of additional hole injection during the stress phase. The voltage at the gate is displayed in blue, while ΔV_{pD} is displayed in gray.

4.2 Evaluation of the different setup configurations

Table 4.1 gives an overview of the advantages and disadvantages of the two setups that were investigated.

The main benefits of using the standard setup with a floating p-drain SMU is the precise control of the value of ΔV_{pD}, since ΔV_{pD} is the difference between the p-drain and the drain, and this difference is controlled by one dedicated SMU. All forward biases used in subsequent measurements are below 10 V, which means that the 20 V range setting of the SMU that sets ΔV_{pD} can be used. With proper servicing the manufacturer guarantees an accuracy of 0.02% + 5 mV in this range. Another benefit is the precise transition between the different phases, where no overshoots of the desired voltages are observed.

The main drawback of the standard setup with the floating p-drain SMU is that the maximum stress voltage is limited to $V_{\mathrm{DS,max}} = 380\,\mathrm{V}$, which is insufficient for investigating surface degradation in 600 V class GaN HEMTs.

The high-voltage setup on the other hand can deliver stress voltages up to $V_{\mathrm{DS,max}} = 3\,\mathrm{kV}$. Since ΔV_{pD} in this case is not directly controlled, but a function of the voltages applied to the drain SMU and the p-drain SMU, it is more difficult to guarantee the effective bias at the p-drain, especially during transient periods of the measurement procedure.

490 V was chosen as $V_{\mathrm{DS,max}}$ to stay in the more accurate 500 V range of the high-voltage SMU with an error of 0.01% + 125 mV. The dependence ΔV_{pD} of rise and fall rates of both high-voltage SMUs led to the observed voltage spikes.

The behavior of ΔV_{pD} during the phases and during the transitions was investigated thoroughly, however due to the dependence of the SMU rise times on impedances, and the influence of the differential probes exert on the rise times, the exact behavior during the procedure can not be measured.

The results for hole injection during the reference and recovery phase and during the stress phase of the standard setup with the floating p-drain SMU were compared to the high-voltage setup with the independently controlled p-drain. At the measured stress biases of 250 V and 380 V the high-voltage setup produced the same results as the standard setup. This supported the conclusion, that high-voltage setup can be used for the subsequent measurements and for measurements beyond the capabilities of the standard setup.

Standard setup with floating p-drain
+ ΔV_{pD} directly controlled by one SMU + Smooth transition between phases
- V_{DS} limited to 400 V, 380 V V_{DS} can be used in practice, since some overhead is needed to switch the transistor to the OFF-state and to be able to forward bias the p-drain with respect to the drain
High-voltage setup with independently controlled p-drain
+ V_{DS} up to 3 kV
- ΔV_{pD} depends on the absolute values at the drain and p-drain contacts - Voltage spikes up to 45 V in reverse bias observed

Table 4.1: Comparison of standard setup and the high-voltage setup.

4.3 Hole injection dynamics from separate p-drain

In this section, the results from the investigation of the influence of hole injection from the separate p-drain during the recovery phase are presented. This gives insight into how hole injection from a different lateral position, compared to hole injection from the gate, influences the recovery process. Due to the electrons being accelerated from the source to the drain during semi-ON-state stress, higher trapped electron densities may arise closer to the drain side of the transistor. Hole injection directly at this site might therefore lead to faster recovery from the experienced degradation.

Another aspect that was investigated is hole injection during the stress phase. This is similar to the operation of an HD-GIT transistor, but with the important distinction, that the hole injection can be controlled actively, while hole injection from the hybrid drain of the HD-GIT is a passive process, which depends entirely on the applied stress voltage. It should be possible to mitigate degradation of the transistor during the stress phase by using the active hole injection, since the HD-GIT works in a similar way. However, the question is which hole current is necessary to mitigate buffer degradation and whether large enough hole currents can also mitigate surface degradation due to hot-carrier stress.

All measurements were performed at room temperature with semi-ON-state stress being applied during the stress phase, which in the context of this thesis is defined as a current of approx. 100 µA.

Three different stress voltages were considered. 250 V was chosen, because previous experiments [18] showed, that at this stress level surface degradation starts to occur. To achieve higher degradation during the stress phase, while still being able to perform comparisons between the two setup configurations, 380 V was chosen as the next stress level. Finally, measurements at 490 V were performed to remain within the more accurate

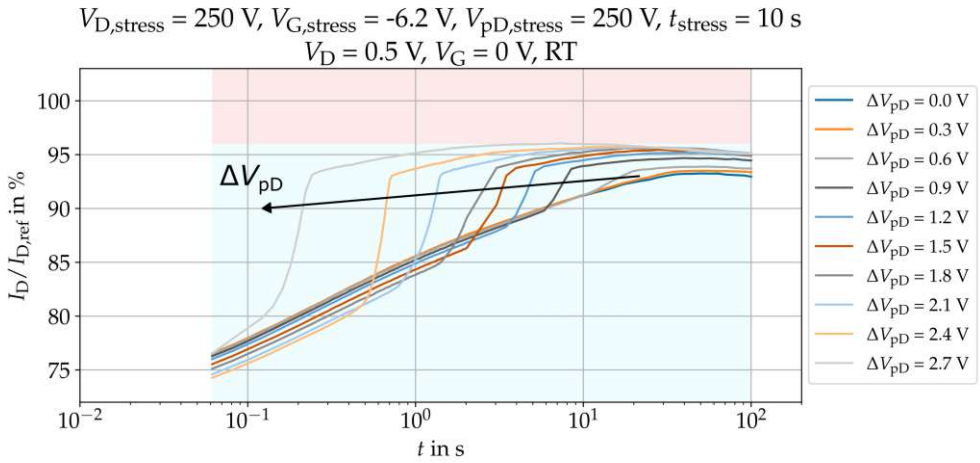
500 V range of the SMUs, while still approaching the limits of the 600 V class device used for the measurements.

4.3.1 Hole injection in recovery phase after semi-ON-state stress

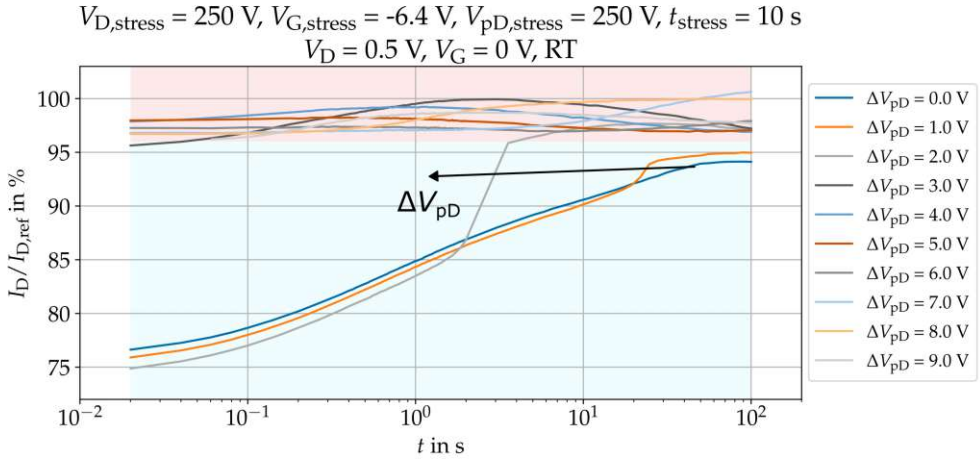
Measurements with 250 V applied to the drain

Figure 4.5a shows recovery by hole injection from the p-drain during the recovery phase. The forward biases used for these measurements range from 0 V, thermal recovery, to 2.7 V. Using forward biases in this range recover the transistor to 96% of the reference current within the observed timeframe of 100 s. The remaining 4% are deemed to be due to hot-carrier degradation of the surface. Acceleration of the time constants due to hole injection is noticeable from 0.6 V forward bias at the p-drain onwards. The time constants for buffer recovery range from 0.2 s at a forward bias of 2.7 V to 18 s at a forward bias of 0.6 V.

To be able to study the degradation of the surface, measurements using forward biases of up to 9 V were conducted and the results are displayed in Figure 4.5b. It is observed again that the device can be recovered up to approx. 96% of the reference current using smaller voltages, while using larger forward biases enables the recovery of the remaining 4%. The currents fluctuate in the 96% to 100% range, however, a clear trend toward shorter time constants can be observed as ΔV_{pD} increases from 7 V to 9 V.



(a) Recovery with forward biases up to $2.7\,\mathrm{V}$, in increments of $0.3\,\mathrm{V}$.



(b) Recovery with forward biases up to $9\,\mathrm{V}$, in increments of $1\,\mathrm{V}$. Surface recovery is observed using these higher forward biases.

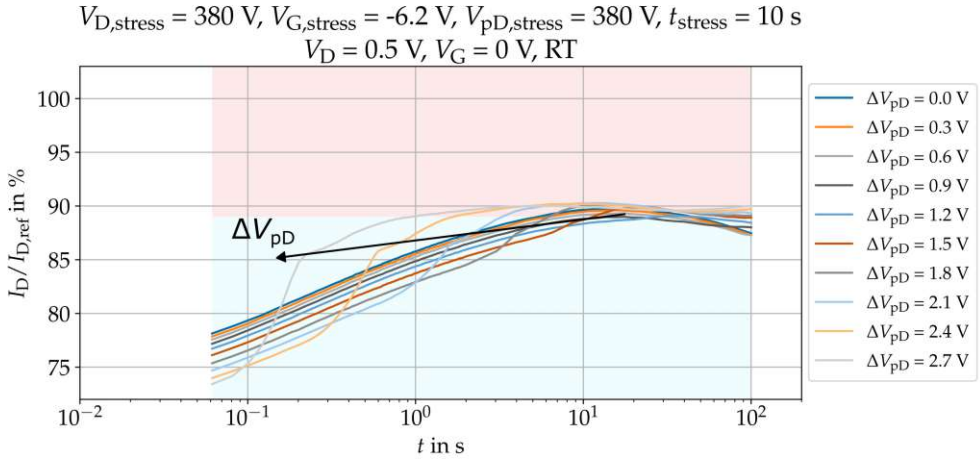
Figure 4.5: Recovery from the p-drain after $V_{\mathrm{DS,stress}} = 250\,\mathrm{V}$. (a) Low forward biases up to $2.7\,\mathrm{V}$ and (b) higher forward biases up to $9\,\mathrm{V}$.

Measurements with 380 V applied to the drain

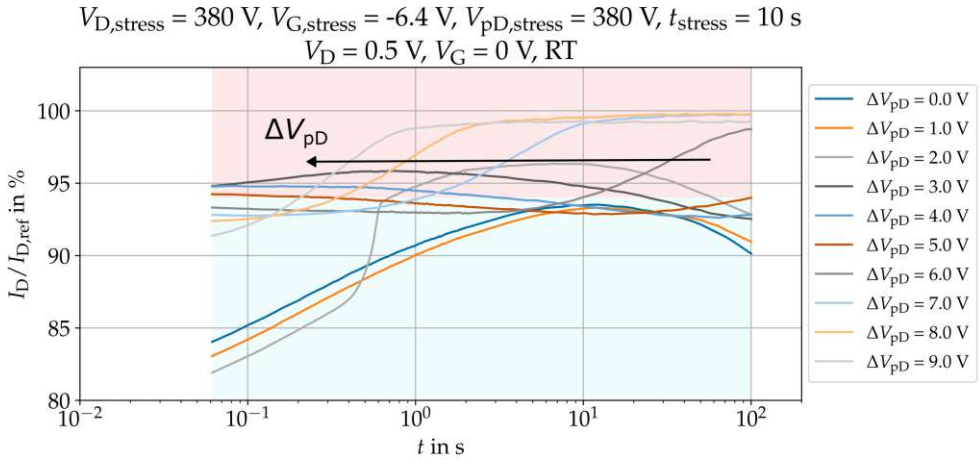
In Figure 4.6a an exponential increase of the recovery drain current is observed for ΔV_{pD} higher than 1.5 V, followed by a kink and a second increase. This is due to the fact, that GaN devices in general have a very high defect density. Therefore multiple trap states are addressed by the injected holes, which results in stretched exponential functions [58][59]. The initial current after stress is in the 73% to 78% range of the reference current and recovers to 89% within the observed timeframe. At a forward bias of 2.4 V and 2.7 V an increase at the end of the measurement period is observed and may indicate the beginning of surface recovery.

Concerning the measurements using higher forward biases, displayed in Figure 4.6b, we observe a smaller initial degradation and a lower surface degradation of 6%. Smaller forward biases start with an initial current of approximately 84% of the reference current, compared to the 73% to 78% observed in measurements with the standard setup. This might be due to device-to-device variation which could be traced back to the usage of small test structures in this thesis. Forward biases of 3 V and higher yield initial currents in the range of 91% to 95%, which indicates that the buffer is already recovered before the first data point is collected. From a forward bias of 5 V to 9 V we see a clear increase of the ON-state current due to the recovery of the surface at higher hole currents.

At 2 V in Figure 4.6b we observe a time constant of 600 ms, while comparable forward biases in Figure 4.6a lead to time constants of 4 s. This discrepancy is not observed for the other measurements, where 250 V and 490 V were applied at the drain during the stress phase and is therefore attributed to device-to-device variation. This aligns with the observation of lower surface degradation. Another explanation could be the small difference in the V_{G} used during the stress phase. However, this is deemed improbable since the same small difference in V_{G} did not affect the measurements with 250 V and 490 V.



(a) Recovery with forward biases up to $2.7\,\mathrm{V}$, in $0.3\,\mathrm{V}$ increments.



(b) Recovery with forward biases up to $9\,\mathrm{V}$, in $1\,\mathrm{V}$ increments.

Figure 4.6: Recovery from the p-drain after $V_{\mathrm{DS,stress}} = 380\,\mathrm{V}$. (a) Low forward biases up to $2.7\,\mathrm{V}$ and (b) higher forward biases up to $9\,\mathrm{V}$.

Measurements with 490 V applied to the drain

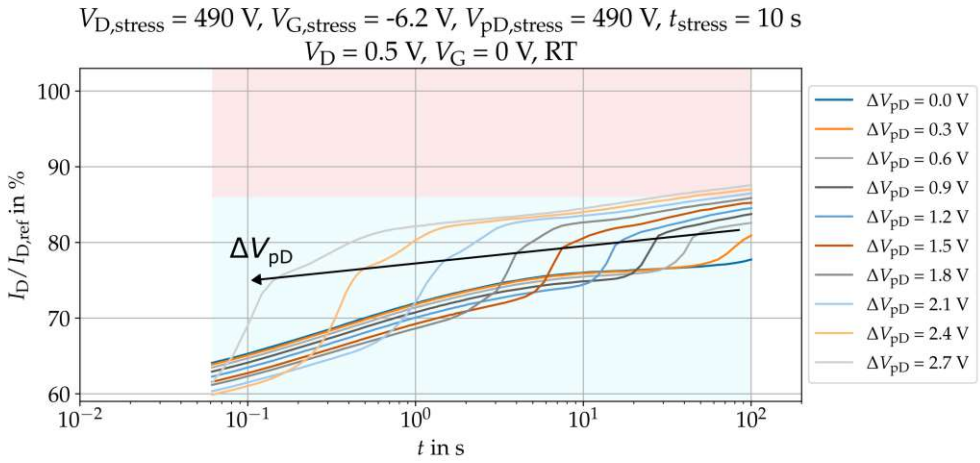
For the measurement with 490 V semi-ON-state stress and lower forward biases, displayed in Figure 4.7a, an initial degradation to between 60% and 65% of the reference current is observed. After buffer recovery 14% of surface degradation remain. A distinct exponential recovery is observed, again with a kink and a subsequent recovery, similar to the measurements conducted with 380 V applied at the drain.

As mentioned before, this is due to the high defect density in GaN devices, which have different de-trapping time constants and therefore result in deviations from the exponential curve, that would result from a single type of trap state. In contrast to the 250 V and 380 V measurements, no recovery peak with subsequent decline is observed for the 490 V measurements, and the device continues to improve after the initial recovery.

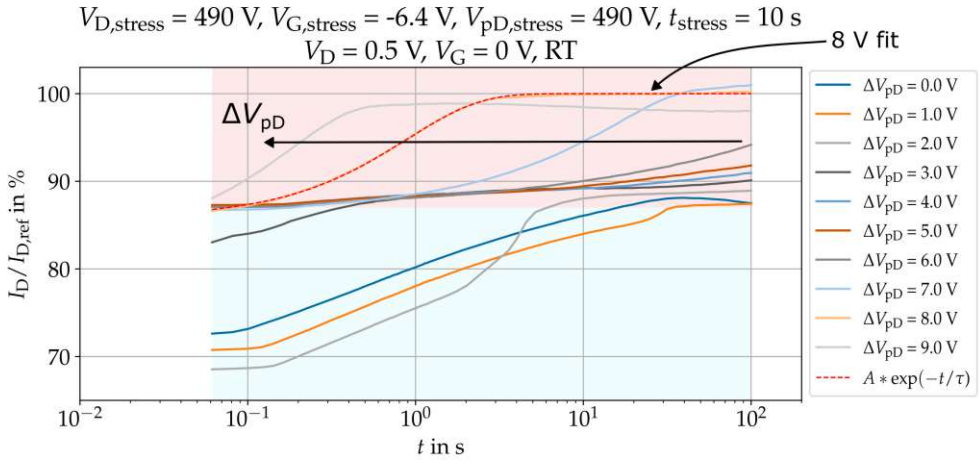
For the measurements with higher forward biases, displayed in Figure 4.7b, a surface degradation of 12% is observed. The time constant observed for the measurement with 2 V forward bias is in good agreement with comparable forward biases in Figure 4.7a. Measurements at smaller forward biases start out with an initial degradation of approximately 30%. At higher forward biases, the buffer degradation is recovered faster than can be observed with an SMU setup. Therefore these measurements start out with an initial degradation of 12% and only the recovery of the surface is recorded. A forward bias of 7 V is required to observe full surface recovery within the measurement timeframe.

The exponential function described in Equation 4.1 was fitted to the surface recovery at 8 V. $I_D(t)$ is the drain current at time t, $I_{D,0}$ is the drain current of a fully recovered device, A is the parameter that represents the initial degradation, and τ is the time constant of the recovery. The fitted function closely matches the data and resulted in an initial degradation A of 14.16% and a recovery time constant τ of 0.89 s.

$$I_D(t) = I_{D,0} \times (1 - Ae^{-t/\tau}) \tag{4.1}$$



(a) Recovery with forward biases up to $2.7\,\mathrm{V}$, in $0.3\,\mathrm{V}$ increments.



(b) Recovery with forward biases up to $9\,\mathrm{V}$, in $1\,\mathrm{V}$ increments.

Figure 4.7: Recovery from the p-drain after $V_{\mathrm{DS,stress}} = 490\,\mathrm{V}$. (a) Low forward biases up to $2.7\,\mathrm{V}$ and (b) higher forward biases up to $9\,\mathrm{V}$. An exponential function is fitted to the measurement with $8\,\mathrm{V}$ forward bias at the p-drain.

4.3.2 Time constants for hole injection during the recovery phase

Figure 4.8 presents the extracted time constants for hole injection during the recovery phase, as discussed in Section 4.3.1, plotted against the hole current from the separate p-drain diode. There are two ways of extracting these time constants. The first and most accurate method involves fitting a suitable test function (4.1) to the data.

The second method requires calculating the drain current at the time constant using Equation 4.3. The corresponding time is then determined by reading the time at this drain current from the graph, which gives the time constant.

$$I_{\mathrm{D}}(\tau) = I_{\mathrm{D},0} \times (1 - Ae^{-\tau/\tau}) \tag{4.2}$$

$$I_{\mathrm{D}}(\tau) = I_{\mathrm{D},0} \times (1 - A\frac{1}{e}) \tag{4.3}$$

The second method provides reliable results, since the slope is steep at these drain currents and small errors in determining the exact position result only in minor discrepancies to the fitting of an exponential function.

Two clusters of time constants are observed. The first cluster is shaded in blue and contains the time constants for the recovery of the buffer, while the second cluster contains the time constants for the recovery from surface degradation and is shaded in red. It is noted that the hole currents required for surface recovery are more than four orders of magnitude higher than those needed for buffer recovery.

A comparison with the results from Butej et al. [57], where the HEMT was recovered from the gate, shows very good agreement with the time constants gathered in this work. Due to the differing I-V characteristics of the gate and the p-drain diode, different forward biases are required to recover the device. However, since the recovery process is hole current driven, only the hole current corresponding to the respective forward biases is relevant. Since both results, recovery from the p-drain and recovery from the gate, are in agreement, it is concluded that the lateral position of the hole injection site has no significant influence on the recovery time constants. This behavior can be explained by the presence of an AlGaN back-barrier between the GaN channel and the carbon-doped buffer layer in the investigated test structures. The AlGaN back-barrier facilitates the fast lateral distribution of holes throughout the epitaxial stack. [60] As a result, the contribution of lateral hole movement to the observed time constants becomes negligible.

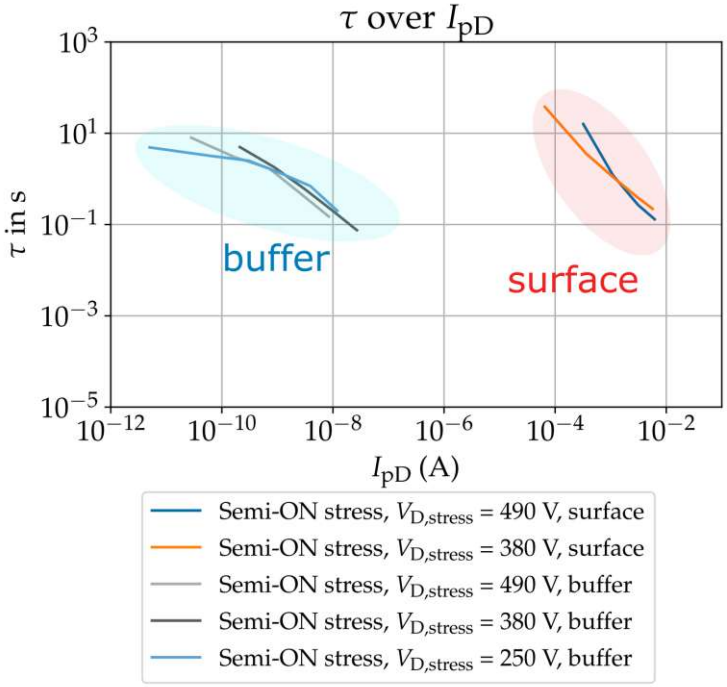


Figure 4.8: Time constants versus hole current from the separate p-drain diode. Time constants for the recovery of the buffer are highlighted by a blue ellipse, while time constants for surface recovery are highlighted by a red ellipse. The time constants are separated by more than four orders of magnitude.

4.3.3 Hole injection during semi-ON-state stress

The second type of measurements takes advantage of the possibility to actively control hole injection from the p-drain. To observe the influence of hole injection during the stress phase, a reference phase is used to measure the initial drain current of the transistor, followed by a stress phase in which the forward bias at the p-drain relative to the drain is varied between 0 V and 2.7 V. Afterwards, the HEMT is switched back to the ON-state where it recovers thermally. Degradation is determined by comparing the initial current reading in the recovery phase after stress to the current measured in the reference phase.

In addition to the previously used $V_{\mathrm{DS,stress}}$ values, measurements at 150 V at the drain during the stress phase were included, as this level is expected to result in the highest percentage of buffer degradation [47][61].

Figure 4.9 shows the degradation over the applied drain bias during stress, for the different p-drain forward biases applied during the stress phase, while Figure 4.10 shows the p-drain current during the stress phase for the different ΔV_{pD}. Previous measurements indicate that the forward biases used in these experiments are only sufficient to recover buffer degradation. Therefore the area below the highest ΔV_{pD} measurement is shaded in blue and considered to be buffer recovery, while the area above the 2.7 V measurement line represents surface degradation due to hot-carrier stress.

For 150 V, a low surface degradation of 5% is observed and the $I_{\mathrm{pD,stress}}$ readings correlate strongly with the applied forward bias at the p-drain, starting at 1.2 V, which is the built-in forward voltage V_{f} of the p-drain diode. At 250 V stress bias at the drain, two clusters of the degradation measurements are observed. Forward biases up to 2.1 V fall in the cluster with higher total degradation of 22% while higher forward biases lead to a degradation of 15% entirely due to surface degradation. This behavior is also reflected in the graph which shows $I_{\mathrm{pD,stress}}$ over the drain voltage. All forward biases up to 2.1 V result in a hole current of 2 µA, while higher forward biases result in lower hole currents. This observation is unexpected, as higher forward biases would typically result in a higher hole current. Additionally, the lower degradation observed at higher forward biases also implies increased hole currents during the stress phase. Various methods were employed to calculate the average hole current during the stress phase, but all consistently produced the same behavior. For the measurements with 380 V and 490 V at the drain, a degradation of 20% and 27% is observed, independent of the applied p-drain forward bias with respect to the drain.

It is hypothesized that the 2DEG underneath the p-drain is depleted at high drain voltages, leading to high effective forward bias at the p-drain, independent of the applied forward bias. This mode of operation resembles the behavior of the HD-GIT. The drain biases to the left of the black vertical line in Figure 4.9 do not lead to 2DEG depletion underneath the p-drain and active hole injection is possible, while the drain biases to the right of the black vertical line lead to 2DEG depletion and in turn to passive hole injection from the p-drain, independent of the applied forward bias.

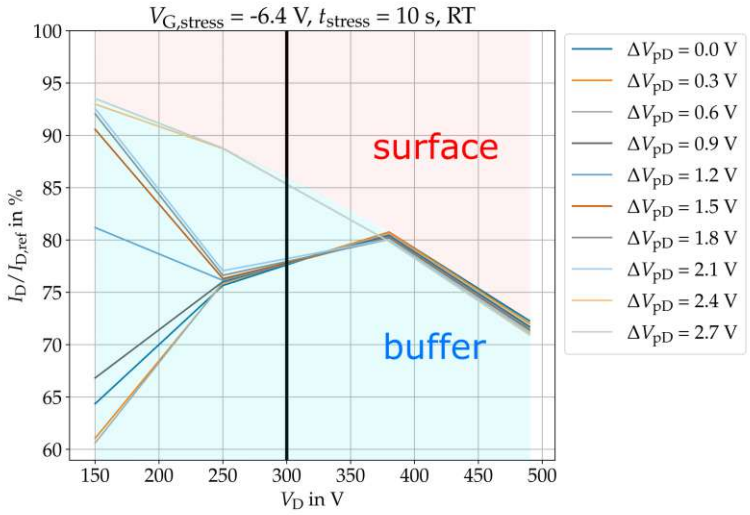


Figure 4.9: Initial degradation after hole injection during the stress phase. The area below the highest forward bias is considered buffer degradation, while the area above is considered surface degradation. The black vertical line at $300\,\mathrm{V}$ splits the graph into the area where active hole injection is possible (left) and where passive hole injection occurs (right).

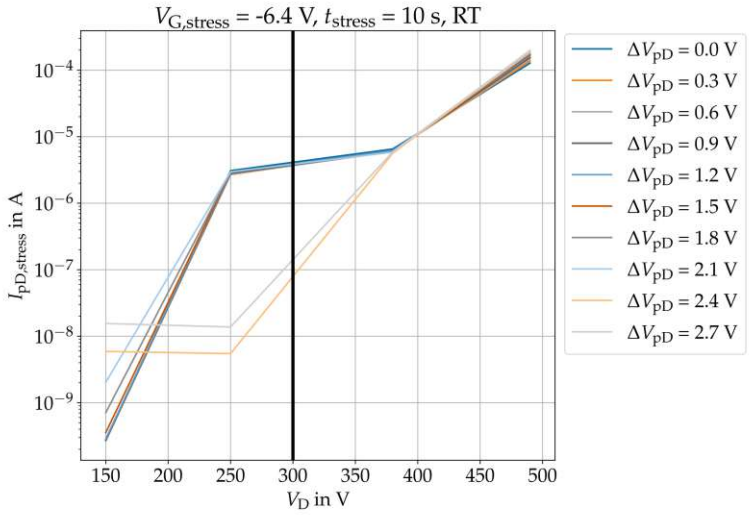


Figure 4.10: Hole current from the p-drain as a function of the applied drain bias during the stress phase for the respective p-drain forward biases.

Higher ΔV_{pD} values during the stress phase were also investigated to determine whether surface degradation could be mitigated, or if the higher forward bias could separate the degradation measurements at high drain voltages. However, device failure was observed under these conditions. This failure is believed to result from substantial hole injection from the p-drain while the HEMT is in the semi-ON-state stress, creating harsh operating conditions that do not occur in a regular transistor without external forward biasing of the p-drain.

4.4 Lateral hole transport in GaN HEMTs

While the effects of hole injection within the HEMT structure were investigated in the previous sections, the goal of this section is to investigate the transport of holes over a larger area, including the region outside of the electrically active area of the HEMT. To facilitate these measurements, the devices with laterally spaced TLM structures, described in Section 3.3.2, were used.

The formation of a 2DEG outside the HEMT region is inhibited either by ion implantation (Figure 3.5a) which disrupts the crystal structure at the AlGaN/GaN heterojunction or by a partial barrier recess (Figure 3.5b) which lifts the conduction band at the AlGaN/GaN interface.

The two different methods for hole injection were:

1. Hole injection from forward-biased p-GaN gate
2. Hole injection during OFF-state stress

All measurements were conducted on the normally-ON device type at room temperature and at 150 °C for a stress duration of 300 s. The current transients of the TLM structures adjacent to the HEMT were measured to examine the effect of hole injection outside the electrically active HEMT area.

4.4.1 Hole injection from forward-biased p-GaN gate

Hole injection from the forward-biased p-GaN gate, also referred to as *gate stress*, refers to a condition, where the transistor is in the ON-state and a large voltage, compared to the usual gate voltages, is applied to the gate. This high forward bias causes significant hole injection, and their diffusion throughout the structure is investigated. The sequence used to measure these effects consists of a reference and a stress phase with the following parameters.

1. Reference phase: $V_{\mathrm{G}} = 0\,\mathrm{V}$, $V_{\mathrm{D}} = 0.5\,\mathrm{V}$, $V_{\mathrm{TLM}} = 0.5\,\mathrm{V}$, $t = 5\,\mathrm{s}$
2. Stress phase: $V_{\mathrm{G}} = 5\,\mathrm{V}$, $V_{\mathrm{D}} = 0.5\,\mathrm{V}$, $V_{\mathrm{TLM}} = 0.5\,\mathrm{V}$, $t = 300\,\mathrm{s}$

Throughout the measurement procedure, the voltage at the source, substrate and one contact of the TLM structure was set to $V = 0\,\mathrm{V}$. The distances are measured from the drain-side edge of the gate to the drain-side edge of the respective TLM structures, located on the drain side of the HEMT.

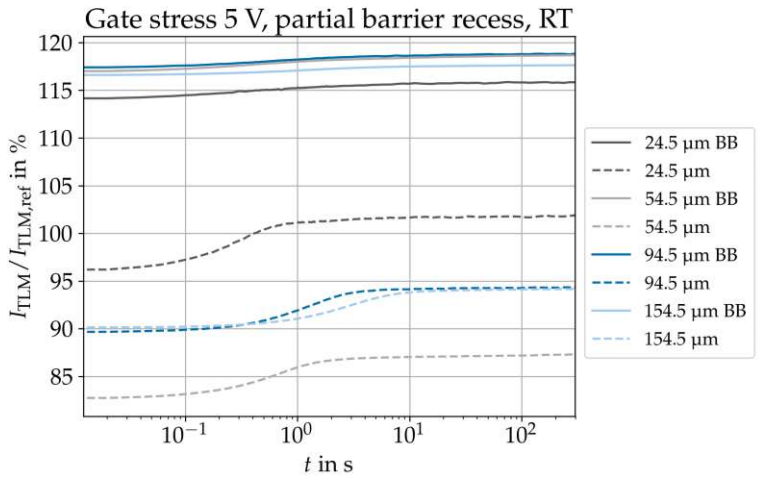
Device with 2DEG inhibition via partial barrier recess

Figure 4.11 shows the results of hole injection via the forward biased p-GaN gate, using the device with a partial barrier recess in the region between the HEMT and the TLM structures.

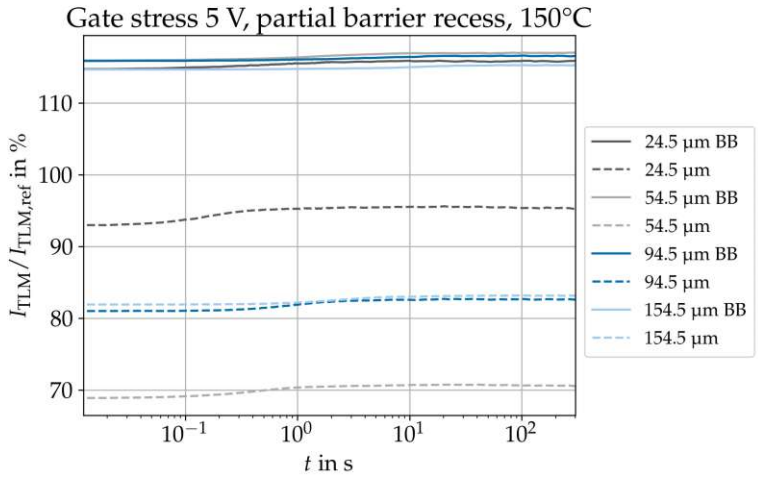
I-V characteristics showed that a small current flows between the HEMT and the TLM structures which confirmed the theory that the 2DEG is not completely eliminated by the partial barrier recess. This is due to the absence of a p-GaN cap layer, similar to the gate stack, over the partial barrier recess, which is required to raise the conduction band at the AlGaN/GaN interface above the Fermi level. Therefore, the channel below is not completely depleted and high voltage measurements are not possible. However, since only small voltages are applied to the transistor and TLM structure contacts, the gate stress measurements can still be conducted and general trends can be inferred.

A comparison of the measurements at room temperature with those at 150 °C reveals generally similar behavior, with the normalized TLM currents slightly reduced at 150 °C. A notable difference between the devices with and without a back-barrier is observed at both room temperature and 150 °C.

The TLM currents for the devices without back-barrier are reduced compared to the currents measured in the reference phase and have time constants in the 0.2 s to 3 s range. The TLM currents for the devices with back-barrier, on the other hand, show an immediate current increase of 14-17% compared to the reference current. The rapid nature of this increase exceeds the time resolution capability of a SMU setup and would necessitate the use of dedicated hardware for a closer investigation. A second, small increase, of the TLM currents is visible at approximately the same time constants as for the device without back-barrier. This suggests, that the immediate current increase is due to rapid hole transport at the GaN:uid/AlGaN back-barrier interface [60], while the second smaller increase of the current is due to the holes moving in the carbon-doped buffer.



(a)



(b)

Figure 4.11: Normalized TLM current for the HEMT with laterally spaced TLM structures during hole injection from the gate. In this device, the 2DEG in the region between the HEMT and the TLM structure is reduced by a partial barrier recess. The measurements were conducted at (a) room temperature and at (b) 150 °C.

Device with 2DEG inhibition via ion implantation

Figure 4.12 shows the measurements for the device, where the 2DEG between the HEMT and the TLM structures is eliminated by ion implantation. It is observed that shorter distances from the gate correlate with higher amplitudes of the current increase and with shorter time constants.

At room temperature, the differences between the devices with and without back-barrier are only marginal, with the inclusion of the back-barrier leading to slightly longer time constants and reducing the current increase amplitudes. At 150 °C, however, the difference between the different epitaxial stacks is more pronounced. While the device with back-barrier behaves similarly at both temperatures, the device without back-barrier shows significantly lower current increase amplitudes.

A comparison with the previous subchapter shows, that the fast lateral hole redistribution component at the GaN:uid/AlGaN back-barrier interface is absent. This suggests, that the ion implantation process reaches below the GaN:uid layer, disrupting the crystal lattice of the back-barrier and therefore inhibiting fast lateral hole transport.

Figure 4.13 shows the extracted time constants over the distance from the gate. To calculate the lateral hole diffusion constants, the Einstein-Smoluchowski equation (4.4) in one dimension was employed. The one-dimensional approximation is reasonable, because the gate width is larger than the distance from the gate to the TLM structures, and because the hole movement is confined to interfaces or single layers.

A linear equation was fitted to the data in a $\sqrt{\tau}$ versus distance plot. Subsequently, the hole diffusion constants for the different epitaxial stacks and temperatures were calculated based on the slope k, obtained from the linear fit, using Equation 4.7.

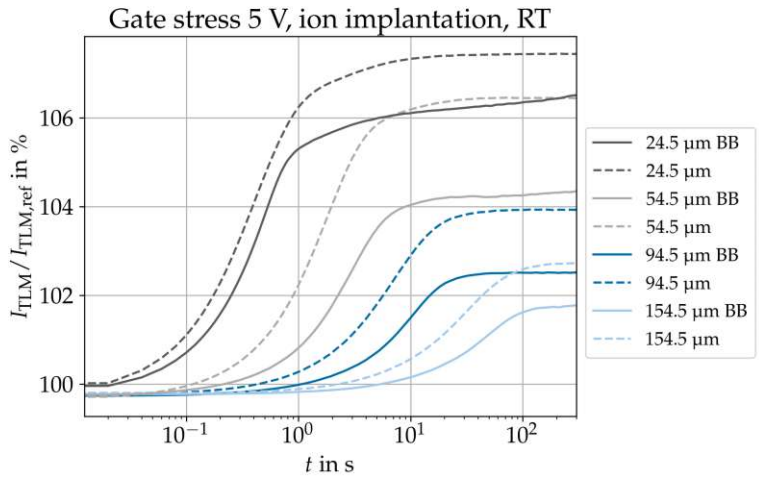
The slight decrease in hole mobility observed for the device with a back-barrier, compared to the devices without back-barrier, may be attributed to the increased distance between the gate and the carbon-doped buffer, where lateral hole transport occurs. The back-barrier approximately doubles the vertical distance the holes need to propagate before lateral transport in the GaN:C buffer outside the active device region can take place. Another possibility is that, within the HEMT area, holes first accumulate at the GaN:uid/AlGaN back-barrier interface before populating the carbon-doped buffer, where then lateral diffusion outside the active HEMT area occurs.

$$x^2 = 2D\tau \tag{4.4}$$

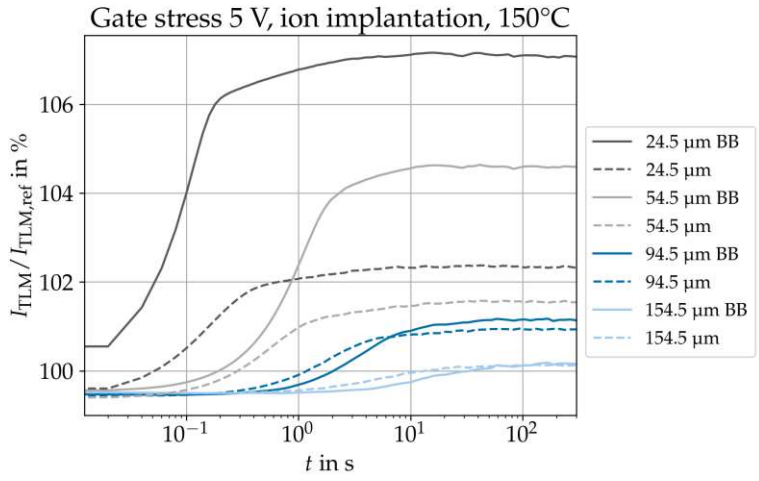
$$\sqrt{\tau} = kx \tag{4.5}$$

$$k = \frac{1}{\sqrt{2D}} \tag{4.6}$$

$$D = \frac{1}{2k^2} \tag{4.7}$$

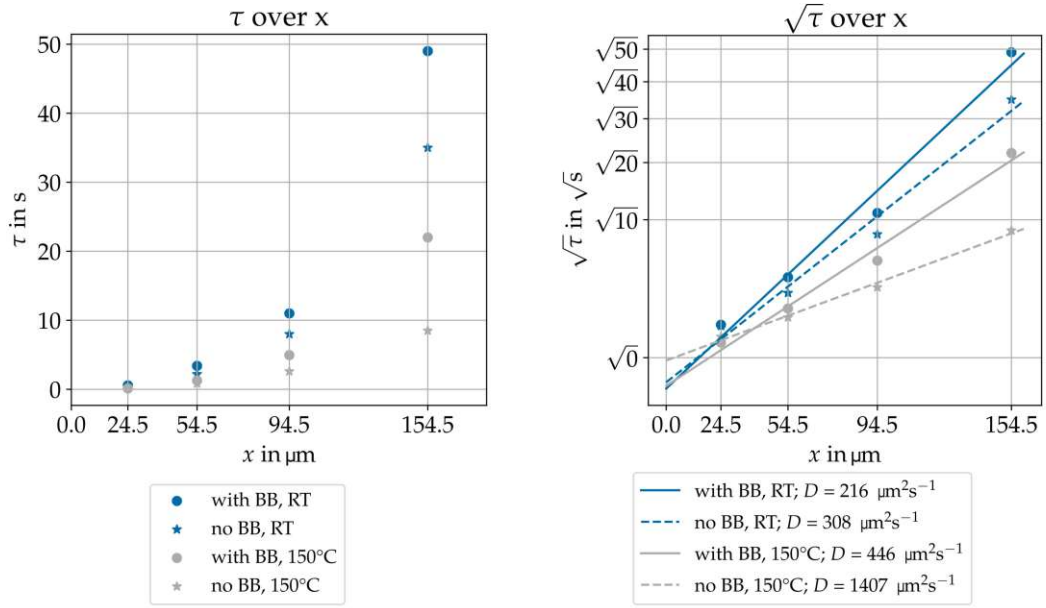


(a)



(b)

Figure 4.12: Normalized TLM current for the HEMT with laterally spaced TLM structures during hole injection from the gate. For this device, the crystal structure in the region between the HEMT and the TLM structure is destroyed by ion implantation. The measurements were conducted at (a) room temperature and at (b) $150\,^{\circ}\mathrm{C}$.



(a) Time constants over distance.

(b) Extraction of diffusion constants.

Figure 4.13: (a) Time constants over distance for the devices with ion implantation and (b) the square root of the time constants over the distance. A linear fit was used to calculate the diffusion constants from the slope of the fit using Equation 4.7.

4.4.2 Hole injection during OFF-state stress

Device with 2DEG inhibition via ion implantation

OFF-state stress measurements were conducted only on devices where the 2DEG between HEMT and TLM structures is destroyed via ion implantation. Since the 2DEG for devices with partial barrier recess is not completely eliminated, current flows between the drain and the TLM structures leading to the destruction of the device under high-stress conditions. The sequence used to measure these effects again consists of a reference and a stress phase with the following parameters.

1. Reference phase: $V_\mathrm{G} = 0\,\mathrm{V}$, $V_\mathrm{D} = 0.5\,\mathrm{V}$, $V_\mathrm{TLM} = 0.5\,\mathrm{V}$, $t = 5\,\mathrm{s}$
2. Stress phase: $V_\mathrm{G} = -8\,\mathrm{V}$, $V_\mathrm{D} = 600\,\mathrm{V}$, $V_\mathrm{TLM} = 0.5\,\mathrm{V}$, $t = 300\,\mathrm{s}$

For these measurements the two closest TLM structures on the drain and the source side of the HEMT were considered. Since the high stress during the stress phase leads to a majority of hole injection from the hybrid drain of the HEMT, distances to the TLM

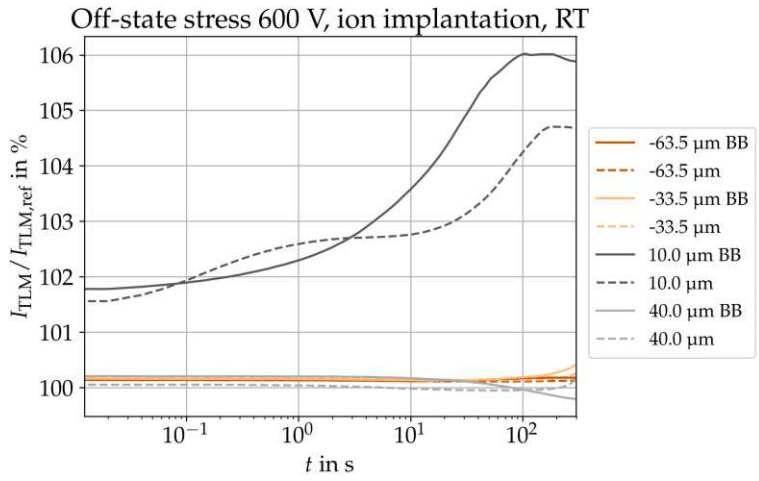
structures were measured from the centerline of the hybrid drain to the TLM structure edge, facing the hybrid-drain.

Figure 4.14a shows the results from the OFF-state stress measurements at room temperature. A significant capacitive coupling effect of 2% is observed for the closest structure at 10 µm. This effect arises from the high potential at the drain during stress conditions, which must drop to ground potential towards the substrate. As a result, the GaN buffer in the drain area exhibits a higher potential, influencing the band diagram underneath the TLM structure and consequently the 2DEG. For structures located further from the drain, this effect is negligible and does not appear in the data.

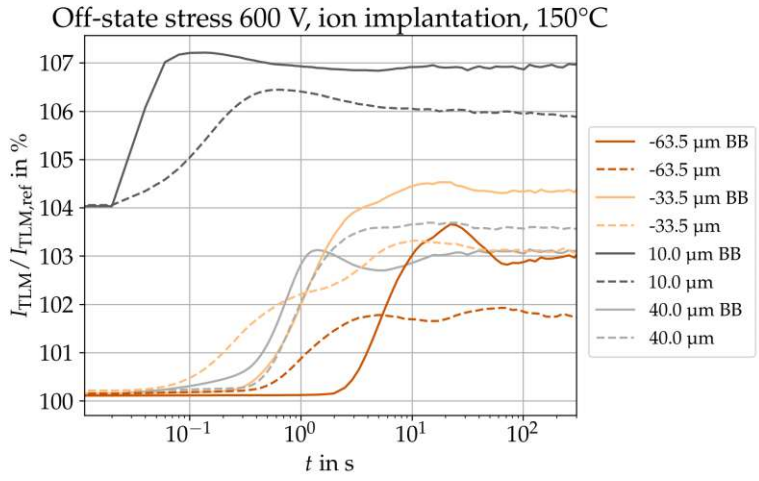
A significant current increase is observed only for the structure closest to the drain, with a time constant of approx. 40 s. The structures further away from the drain show a very stable current at 100% of the reference current for the first 50 s of the measurement with slight fluctuations afterwards.

For the measurements at 150 °C, presented in Figure 4.14b, a stronger capacitive coupling effect of 4% is observed at a distance of 10 µm from the drain. However, since higher temperatures are not expected to influence the strength of the capacitive coupling, this observation is attributed to the limited time resolution of the SMU setup combined with the faster time constants at elevated temperatures. This results in an apparent increase in the capacitive coupling effect. The actual capacitive coupling effect is still estimated to be 2%. The time constants for all distances are accelerated compared to room temperature. The structure 33.5 µm to the left of the drain and the structure 40 µm to the right of the drain have approximately the same time constant. Since the electric field extends in both directions from the drain, both structures are influenced equally due to their similar distances from the drain.

Comparing the measurements at room temperature with those at 150 °C, a significant acceleration of the time constants is observed. This shift to shorter time constants with increasing temperature is less pronounced in measurements from the previous subchapter involving hole injection from the forward-biased p-GaN gate.



(a)



(b)

Figure 4.14: Normalized TLM current for the HEMT with laterally spaced TLM structures during hole injection from hybrid-drain under OFF-state stress conditions. For this device, the crystal structure in the region between the HEMT and the TLM structure is destroyed by ion implantation. The measurements were conducted at (a) room temperature and at (b) $150\,^{\circ}\mathrm{C}$.

5 Conclusion and Outlook

Two different Source-Measurement-Unit setups were evaluated for their respective strengths and weaknesses, in investigating the effects of hole injection via a separated p-doped GaN region close to the drain contact, in specially designed test structures. The first setup utilized 200 V-class SMUs in a floating configuration, where the drain SMU serves as the reference for the p-drain SMU. This allows the p-drain SMU to operate within its smaller, more accurate voltage ranges, enabling exact control of the difference between the p-drain and the drain potential. To increase the effective stress voltages and therefore the percentage of surface degradation, the source and the substrate were biased to $-190\,\mathrm{V}$ to achieve effective stress voltages of up to 380 V. The second setup employed a mixture of 200 V- and 3 kV-class SMUs to enable stress measurements with up to 490 V applied to the drain.

Comparing both setups in their overlapping voltage range resulted in similar recovery profiles, leading to the conclusion that the high-voltage setup is better suited to study the effects of surface degradation on the 600 V-class devices.

An improvement to the overall measurement architecture could be the development of a setup using a high-side gate driver. This addition could provide more precise control of the forward bias at the p-drain and enable pulsed measurement techniques, thereby improving measurement accuracy and flexibility.

To investigate the effects of intentional hole injection in the gate-drain access region on surface degradation during and after the stress period, a measurement-stress-measurement technique was used.

Hole injection from the separate p-drain, after the stress period, leads to recovery time constants similar to the results previously published by Butej et al. [57], where recovery by hole injection from the p-GaN gate was studied. This observation leads to the conclusion that the lateral position of the hole injection site has no significant influence on the time constants of the surface recovery process, likely due to the presence of a back-barrier, which facilitates fast lateral hole distribution. Three possible continuations of this investigations could be:

- Measurements on the same device structure without a back-barrier, to compare the dependence of the recovery time constants on the lateral position, in devices with reduced hole mobility.
- Development of the high-side gate driver setup, to enable pulsed hole injection and varying stress sequences.
- Production of similar test structures with increased gate-drain distance (L_{GD}) to separate the time constants for hole injection from the gate and the p-drain. This would however lead to altered stress conditions.

To investigate the effects of active hole injection during the stress phase, similar to the HD-GIT, voltages ranging from 150 V to 490 V were applied during the stress phase. For lower stress voltages, a clear separation of the initial device degradation, depending on the forward bias of the p-drain, was observed. After high stress voltages on the other hand, the degradation of the device after the stress phase was independent of the p-drain forward bias during the stress phase. This was concluded to be a result of 2DEG depletion beneath the separated p-drain, which leads to a high effective forward bias and therefore a high hole current, independent of the nominal forward bias of the p-drain with respect to the drain. Higher nominal forward biases of the p-drain were also studied, which however lead to the destruction of the device.

For the last part, the lateral hole transport properties outside the active area of the HEMT were investigated. The hole injection occurred either from the gate, or from the hybrid drain during OFF-state stress conditions. To facilitate these measurements, four different device configurations were available, varying by their epitaxial stacks and the method of 2DEG inhibition between the HEMT and the TLM resistor structures. These measurements were conducted at room temperature and at 150 °C.

For hole injection from the gate, devices with ion implantation as the 2DEG inhibition method, showed only minor differences between the configuration with and without back-barrier. This is attributed to the fact, that the ion implantation reaches deep below the surface of the device, thereby not only inhibiting the formation of the 2DEG at the heterojunction, but also destroying the crystal structure of the GaN:uid/AlGaN back-barrier interface, where the fast lateral hole transport occurs. Measuring lateral hole transport properties, using the device were the 2DEG was inhibited by a partial barrier recess resulted in a marked difference, with the back-barrier leading to significantly faster hole transport. Increased temperatures lead to a shortening of the time constants, and therefore an increase in hole mobility across the board.

The OFF-state stress measurements were only conducted on the device with ion implantation as the 2DEG inhibition mechanism. The results at room temperature showed significantly longer time constants for hole injection from the hybrid drain compared to hole injection from the gate. In follow-up investigations, the OFF-state stress measurements could be expanded to the devices with 2DEG inhibition via a partial barrier recess by adding a p-GaN layer on top of the recess, similar to the gate stack, to completely eliminate the 2DEG in the region between the HEMT and the TLM structures. To study how device-to-device variation influences the lateral transport behavior, a dedicated setup with a purpose made probe card would enable more efficient measurements on a larger set of devices.

Overall, this thesis provides valuable insights into the effects of hole injection on the surface recovery behavior of GaN-based devices, with a particular focus on recovery

during and after after hot-carrier stress. Additionally it establishes a robust groundwork for studying lateral hole transport outside the active HEMT area, which future studies can build on to address open questions.

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I would also like to thank Prof. Wolfgang Werner for his support and supervision.

Last but not least, I would like to thank my family and friends for their support throughout my academic journey and life in general. I am very lucky to have you.

Statement on the use of Artificial Intelligence:
Artificial Intelligence (AI) tools such as ChatGPT and Deepl Write were used to polish the language and help with structuring. The content is original and all sources used are cited.

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