Diploma Thesis

Quenching circuit using HV transistors

submitted in satisfaction of the requirements for the degree of

Diplom-Ingenieur

of the TU Wien, Faculty of Electrical Engineering and Information Technology

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Diplomarbeit

Löschschaltung mit HV-Transistoren

ausgeführt zum Zwecke der Erlangung des akademischen Grades eines

Diplom-Ingenieurs

eingereicht an der Technischen Universität Wien, Fakultät für Elektrotechnik und Informationstechnik

im Rahmen des Masterstudiums

Schaltungstechnik

von

Sherwin Nasirifar, BSc

Matr.Nr.: 11712191

unter der Anleitung von

Univ.Prof. Mag.rer.nat. Dr.techn. **Horst Zimmermann**

Institute of Electrodynamics, Microwave and Circuit Engineering
Technische Universität Wien
Karlsplatz 13, 1040 Wien, Österreich

Wien, am January 2025

Abstract

This thesis presents the design and optimization of a quencher circuit for Single-Photon Avalanche Diodes (SPADs) fabricated in a 0.35-µm high-voltage CMOS process, aimed at improving the performance of SPAD-based photon detection systems. SPADs, known for their ability to detect single photons, are crucial in applications such as Time-of-Flight (ToF) sensors, quantum cryptography, and optical communication. A major challenge in SPAD operation is managing the avalanche process, which requires rapid quenching to prevent diode damage and ensure accurate photon detection. The proposed quenching circuit incorporates high-voltage transistors specifically chosen to optimize reset times and maximize photon detection efficiency. The design was fine-tuned to minimize afterpulsing and ensure stable operation across varying conditions. Pre-layout simulations in Cadence Virtuoso confirmed the circuit's ability to achieve precise timing optimization and voltage transitions, crucial for reliable photon detection. Post-layout simulations, accounting for parasitic effects, demonstrated robust performance despite process variations. The final design achieves improved response and passive quenching times, outperforming conventional circuits and similar works in reducing afterpulsing. This work significantly advances SPAD-based systems, enhancing photon detection efficiency and reliability for demanding optoelectronic applications.

Kurzfassung

Diese Arbeit präsentiert das Design und die Optimierung einer Quencherschaltung für Single-Photon Avalanche Dioden (SPADs), die in einem 0,35-µm Hochspannungs-CMOS-Prozess gefertigt wurden, mit dem Ziel, die Leistung von SPAD-basierten Photonendetektionssystemen zu verbessern. SPADs, die einzelne Photonen detektieren können, sind in Anwendungen wie Time-of-Flight (ToF)-Sensoren, Quantenkryptographie und optischer Kommunikation von entscheidender Bedeutung. Eine zentrale Herausforderung beim Betrieb von SPADs ist die Steuerung des Lawinenprozesses, der eine schnelle Quenchung erfordert, um Schäden an der Diode zu vermeiden und eine präzise Photonendetektion zu gewährleisten. Die vorgeschlagene Quencherschaltung verwendet speziell ausgewählte Hochspannungstransistoren, um die Rücksetzzeiten zu optimieren und die Detektionseffizienz zu maximieren. Das Design wurde gezielt angepasst, um Afterpulsing zu minimieren und eine stabile Funktion unter verschiedenen Betriebsbedingungen sicherzustellen. Pre-Layout-Simulationen in Cadence Virtuoso bestätigten die Fähigkeit der Schaltung, präzise Zeitoptimierung und Spannungsübergänge zu erreichen, die für eine zuverlässige Photonendetektion entscheidend sind. Post-Layout-Simulationen, die parasitäre Effekte berücksichtigen, zeigten eine robuste Leistung trotz Prozessvariationen. Das endgültige Design erreicht verbesserte Ansprech- und passive Quenchzeiten und übertrifft herkömmliche Schaltungen sowie ähnliche Arbeiten in der Reduzierung von Afterpulsing. Diese Arbeit leistet einen bedeutenden Beitrag zur Weiterentwicklung von SPAD-basierten Systemen, indem sie die Effizienz und Zuverlässigkeit der Photonendetektion für anspruchsvolle optoelektronische Anwendungen verbessert.

Acknowledgements

I would like to express my sincere gratitude to my supervisor, Univ.-Prof. Mag.rer.nat. Dr.techn. **Horst Zimmermann** , for his invaluable guidance and support throughout this thesis. His expertise and insightful feedback have been instrumental in shaping this work.

I am especially grateful to my co-supervisor, *Baset Mesgari*, whose unwavering support and dedication have been truly exceptional. He has always been available, offering guidance and assistance at every step, ensuring that I can navigate any challenges that arise. I would also like to sincerely thank *Christoph Ribisch*, who is dedicating his time to assist me, especially in the final stages of this project. His support during the ongoing measurement phase is invaluable, and I deeply appreciate his willingness to stand by my side as we complete this crucial part of the work.

I am profoundly thankful to my parents, whose unconditional love and support have been the foundation of my academic journey. Their belief in me has been my greatest motivation. Finally, I am truly grateful to my wife, *Leila*, who has been my pillar of strength. She does everything she can to support me, making countless sacrifices to ensure I can focus on my work. Her encouragement and unwavering belief in me mean more than words can express.

Contents

Acronyms

PET positron emission tomography. 6

PMTs Photomultiplier Tubes. 3, 7

PQC Passive Quenching Circuits. 10, 11, 13

QKD quantum key distribution. 6

SPAD Single-Photon Avalanche Diode. ix, 3–13, 15, 17–21, 23, 24, 26–28, 31, 33, 34, 36

TCSPC time-correlated single-photon counting. 4

ToF Time-of-flight. 2–4, 6

1 Introduction

1.1 Photodetectors

Photodetectors are crucial components in modern optoelectronic systems, converting light into electrical signals. They are widely used in various applications, including Time-of-flight (ToF) sensors, quantum cryptography, optical wireless communication, and medical diagnostic optical tomography [1,2]. These devices are essential for detecting weak optical signals, sometimes down to the single-photon level, which is a common requirement in these fields.

The working principle of most photodetectors involves the absorption of incident photons, which generates electron-hole pairs within a semiconductor material. These charge carriers are then separated by an electric field, resulting in a measurable current proportional to the intensity of the incoming light. Photodetectors come in various forms, each optimized for specific operational ranges, sensitivity levels, and response times, depending on the application.

Photodiodes are widely used due to their simplicity, fast response time, and ability to be integrated into various electronic systems. The choice of photodetector depends on the specific requirements of the application, such as sensitivity, response time, and wavelength range. Advances in photodetector technology continue to drive innovation in optoelectronics, enabling more precise and efficient light detection. There are several types of photodetectors, each with unique characteristics and advantages:

- **Photodiodes**: These are simple semiconductor devices that convert light into an electrical current in a linear fashion. They are widely used due to their reliability, low cost, and suitability for a range of light intensities. Photodiodes are found in applications like solar cells, optical receivers, and general-purpose light sensors.

- **Avalanche Photodiodes (APDs)**: APDs are similar to standard photodiodes but operate with a high reverse bias voltage, enabling internal gain through an avalanche multiplication process. This makes them more sensitive to low light levels compared to regular photodiodes. APDs are often used in applications where higher sensitivity is needed, such as in fiber-optic communication and low-light imaging.

- **Photomultiplier Tubes (PMTs)**: PMTs are highly sensitive vacuum tube devices that can detect extremely low levels of light by amplifying the signal through a series of dynodes. Despite their high sensitivity, PMTs are bulky, fragile, and require high voltage, which limits their use in portable and miniaturized systems.

- **Charge-Coupled Devices (CCDs) and Complementary Metal-Oxide-Semiconductor (CMOS) Sensors**: These imaging sensors are commonly used in cameras and scientific instruments. They are capable of capturing detailed images by converting light into electrical charge in a pixel array. CCDs are known for their high image quality, while CMOS sensors are favored for their lower power consumption and higher integration flexibility.

- **Single-Photon Avalanche Diode (SPAD)s**: SPADs are designed to detect single photons by operating in Geiger mode, where they are biased above their avalanche breakdown voltage. This makes them highly sensitive and able to detect extremely weak optical signals. SPADs are widely used in applications like light detection and ranging (LiDAR), ToF imaging, and quantum cryptography, where precise photon timing and high sensitivity are required. They are particularly valuable in systems where detecting individual photons is critical for performance.

As mentioned above, in many modern applications, the ability to detect light with high sensitivity and speed is crucial. Applications such as LiDAR, quantum communication, and biomedical imaging require not only the detection of low-light signals but also the precise timing of photon events. Therefore, photodetectors must exhibit several key characteristics, including:

- **High Sensitivity**: The ability to detect very weak light signals, sometimes down to single photons.

- **Fast Response Time**: Quick reaction to changes in light intensity, allowing accurate time resolution.

- **Low Noise**: Minimal unwanted signal or noise that could interfere with the accurate detection of photons.

- **Wide Dynamic Range**: Capability to accurately detect both very weak and very strong signals.

- **Integration Potential**: Compatibility with modern semiconductor processes (such as CMOS) for ease of integration into complex systems.

In systems requiring single-photon detection or extremely fast time resolution, more specialized devices, such as single-photon detectors, may be necessary. Single-photon detection, often required in time-correlated single-photon counting (TCSPC), quantum optics, and advanced LiDAR systems, represents a distinct area where cutting-edge photodetectors come into play.

In summary, photodetectors are indispensable in numerous technological fields, facilitating advancements in communication, security, and medical diagnostics. Their ongoing development promises to enhance the capabilities of systems that rely on accurate light detection.

1.2 Single-Photon Avalanche Diodes (SPADs)

Single-photon avalanche diodes (SPADs) have emerged as highly effective photodetectors in various optoelectronic applications due to their exceptional sensitivity and compatibility with CMOS technology. SPADs are capable of detecting single photons, making them ideal for applications requiring high sensitivity. including time-of-flight (ToF) measurements, quantum cryptography, fluorescence lifetime imaging microscopy (FLIM), and optical communication systems.

1.2.1 SPAD Operating Principle

The basic operating principle of SPADs can be understood by comparing them to conventional avalanche photodiodes (APDs), with a key distinction in their mode of operation. While APDs operate with a reverse bias slightly below the avalanche breakdown voltage to achieve signal amplification, SPADs are specifically designed to operate in "Geiger mode." In this mode, the reverse bias applied to the diode is set well above the breakdown voltage, typically on the order of several tens of volts beyond the threshold. When a photon is absorbed by the SPAD, it generates an electron-hole pair. This pair is then accelerated by the strong electric field present in the multiplication region of the diode. If the electron or hole gains sufficient energy, it can ionize other atoms, creating more electron-hole pairs in a process known as impact ionization. This chain reaction leads to a self-sustaining avalanche, resulting in a large current pulse that signifies the detection of a single photon. The current spike generated by the avalanche is much larger than the original signal, making it easily detectable by external electronics [3].

Unlike conventional photodiodes, SPADs do not produce a current proportional to the incident light intensity. Instead, they act as binary devices: when a photon is absorbed and triggers an avalanche, the SPAD outputs a standard pulse of current, representing the detection of one photon. No matter how many photons are absorbed within the same short time window, the SPAD will only produce one pulse and, indeed, sustain the avalanche current, representing the “on-state” as shown in figure 1.1. In the absence of a generated carrier, no current flows through the SPAD, indicating the “off-state.” If an ignition event occurs while the SPAD is biased above the breakdown voltage, the device quickly transitions from the off-state to the on-state. This makes SPADs ideal for single-photon detection and timing applications but limits their dynamic range in scenarios where photon flux is high [4].

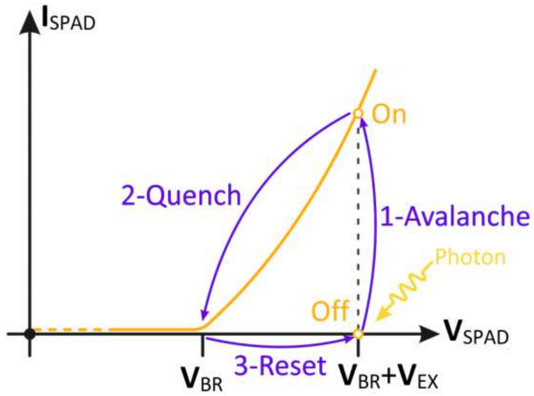


Figure 1.1: SPAD operation principle. [4]

1.2.2 SPAD Characteristics and Performance Metrics

The performance of SPADs is defined by a number of essential features that make them appropriate for single-photon detection in demanding applications. These include:

- **Photon Detection Efficiency (PDE)**: This refers to the probability that an incoming photon will be detected by the SPAD. PDE is dependent on several factors, including the wavelength of the incident light, the quantum efficiency of the SPAD's active region, and the over-bias voltage. Higher PDE is desirable in applications like quantum optics, where capturing as many photons as possible is essential.

- **Dark Count Rate (DCR)**: In the absence of light, SPADs can still produce spurious pulses due to thermally generated carriers within the depletion region, known as dark counts. The dark count rate is a measure of how often these noise pulses occur and is typically minimized through careful design and cooling. Low DCR is critical in low-light or photon-starved environments, such as astronomy or weak fluorescence imaging.

- **Timing Jitter**: This refers to the uncertainty in the time between when a photon is absorbed and when the corresponding avalanche is detected. Timing jitter is particularly important in applications like time-of-flight measurements, where precise time resolution is needed to measure distances or photon arrival times with high accuracy.

- **Dead Time**: After an avalanche is triggered and quenched, the SPAD requires a brief recovery period before it is ready to detect the next photon. This period, known as the *dead time*, is determined by the quenching and resetting circuit. Dead time limits the maximum photon detection rate of the SPAD, as it introduces a gap during which additional photons cannot be detected. Applications requiring high photon flux, such as LiDAR and fluorescence lifetime imaging, benefit from SPAD designs with minimized dead time. However, shorter dead times often come at the cost of increased afterpulsing, necessitating a balance between these parameters.

- **Afterpulsing Probability (APP)**: During the avalanche process, charge carriers can become trapped within defects in the multiplication zone. These trapped carriers may be released after the avalanche is quenched, leading to spurious pulses, commonly referred to as afterpulses. The likelihood of this phenomenon is quantified by the Afterpulsing Probability (APP), which is defined as the ratio of afterpulsing events to the total number of avalanches. A higher APP results in increased noise and reduced detection accuracy, particularly in time-sensitive applications. Managing APP is a significant challenge in SPAD design, often requiring advanced quenching techniques and optimized semiconductor fabrication processes to minimize carrier trapping and release.

1.2.3 Applications of SPADs

SPADs have found widespread use in several cutting-edge technologies:

- **Time-of-Flight (ToF) Systems**: In LiDAR and other ToF systems, SPADs are used to measure the time it takes for a photon to travel to a target and reflect back, allowing accurate 3D mapping and ranging in applications like autonomous vehicles, robotics, and augmented reality.

- **Quantum Cryptography**: In quantum key distribution (QKD) systems, SPADs detect individual photons used to transmit cryptographic keys securely. Their ability to accurately time and detect single photons makes them integral to ensuring secure communication channels.

- **Biomedical Imaging**: SPADs are employed in advanced imaging techniques like FLIM and positron emission tomography (PET), where precise photon detection enables high-resolution imaging of biological tissues.

1.3 Technology Requirements for SPAD

The successful implementation of a Single-Photon Avalanche Diode requires meeting several stringent technological and design conditions. These requirements ensure high sensitivity, low noise, reliable operation, and compatibility with modern electronic systems. The underlying technology must address challenges related to material quality, device structure, and fabrication processes to optimize SPAD performance.

1.3.1 Key Technological Requirements

To function effectively as a SPAD, the diode's p-n junction must meet several critical technological requirements. High material quality is essential to ensure a structure free from lattice imperfections, as defects can lead to premature breakdown or increased noise. The purity of the substrate material directly influences the dark count rate (DCR), with high-purity silicon being the most widely used due to its low thermal noise and excellent electronic properties. To prevent edge breakdown, where the electric field is concentrated at the junction edges, SPADs incorporate a guard ring that redistributes the electric field, ensuring uniform operation and improving reliability [5]. Another crucial factor is minimizing the afterpulsing probability (APP), a measure of the likelihood of spurious pulses caused by trapped carriers in the multiplication region being released after an avalanche [6]. This requires advanced semiconductor processing to reduce trapping sites and careful design of quenching circuits. Together, these technological considerations ensure that SPADs achieve high sensitivity, low noise, and reliable operation, making them suitable for demanding applications.

1.3.2 Evolution of SPAD Fabrication Technology

When SPAD technology was initially conceived, available fabrication techniques struggled to meet the stringent requirements for substrate quality and device design. Early SPADs suffered from high noise, limited reliability, and poor timing resolution due to the limitations of semiconductor fabrication processes.

In the 1980s, significant progress was achieved with the implementation of SPADs in planar-silicon technology. This development marked a turning point, as planar processes improved device uniformity, reduced noise, and facilitated large-scale production. Despite the widespread availability of CMOS processes during the 1980s, SPADs were not immediately implemented in CMOS technology due to the complexity of integrating SPAD structures with additional circuitry.

The first SPAD in CMOS technology was demonstrated in 2003, representing a major milestone in SPAD development. This advancement allowed for the integration of SPADs with on-chip quenching and signal-processing circuitry, reducing system complexity and cost. By the early 2000s, CMOS technology had enabled the fabrication of highly compact SPAD devices with impressive performance metrics:

- **High Timing Resolution**: The first CMOS SPAD, implemented in a high-voltage 0.8-μm CMOS technology, achieved a timing resolution of 50 ps, comparable to commercially available photomultiplier tubes (PMTs).

- **Array Compatibility**: The CMOS platform facilitated the development of SPAD arrays, paving the way for compact and cost-effective imaging systems. These arrays are particularly competitive with traditional Charge-coupled device (CCD) cameras in certain applications, offering advantages in speed, sensitivity, and integration.

Today, three main processes dominate SPAD fabrication, each optimized for different performance and application requirements:

1. **Standard CMOS Technology**

   The use of standard CMOS processes allows SPADs to be fabricated alongside complex quenching and readout circuits. This approach is widely favored for applications requiring compact and low-cost designs, such as time-of-flight sensors and consumer-grade LiDAR systems. However, standard CMOS SPADs may have limitations in terms of sensitivity and noise performance compared to specialized processes.

2. **Customized CMOS Processes**

   Customized CMOS processes introduce modifications to standard fabrication steps, such as tailored doping profiles and optimized isolation techniques, to improve SPAD performance. These processes strike a balance between cost-effectiveness and high-performance characteristics, making them suitable for professional-grade imaging and scientific applications.

3. **Specialized High-Voltage Technologies**

   High-voltage fabrication technologies are used to produce SPADs with enhanced sensitivity and timing resolution. These processes are ideal for applications demanding extreme precision, such as quantum optics, medical imaging, and advanced LiDAR systems.

1.3.3 Material Choices for SPADs

Although silicon remains the dominant material for SPAD fabrication due to its advanced technology and widespread availability, alternative materials are being explored for specialized applications. For instance:

- **InGaAs/InP SPADs** are used for near-infrared photon detection, extending the wavelength range beyond the capabilities of silicon SPADs. These devices are critical in applications like fiber-optic communication and long-range LiDAR systems.
- **GaAs and GaN SPADs** offer potential advantages in ultraviolet detection and high-speed applications, leveraging the unique properties of these wide-bandgap materials.

2 Quenching Circuits

One of the critical aspects of SPAD operation is managing the avalanche process once it has been initiated. A self-sustaining avalanche would persist indefinitely if left unchecked due to the nature of the avalanche mechanism in SPADs. It could damage the SPAD and prevent it from detecting subsequent photons. To remedy this, quenching circuits are required to stop the avalanche rapidly. The avalanche multiplication process is disrupted by lowering the bias voltage below the breakdown threshold, enabling the SPAD to revert to its starting condition(initial waiting condition) and become prepared to detect subsequent photons. This process is known as "quenching."

2.1 Structure

The design and implementation of quenching circuits directly impact the performance characteristics, such as timing precision, noise levels, and recovery speed. For instance, the system's maximum counting rate will be constrained by a slow quenching circuit (with a lengthy dead time). On the other side, selecting more costly technologies or creating solutions that take up more chip space to accomplish quick quenching and resetting times can be required. As a result, it's critical to create a quenching circuit that works best for the intended use.

Quenching circuits are classified into three main types: passive, active, and mixed. Each type exhibits unique advantages and limitations, making them suitable for specific applications. Their structures are designed to fulfill the critical task of terminating the avalanche current in photon detection systems while addressing different performance requirements. Passive quenching circuits rely on simple resistive components to naturally suppress the avalanche current, offering simplicity and reliability but often at the cost of slower recovery times. On the other hand, active quenching circuits use electronic components such as transistors and feedback loops to detect and halt the avalanche actively, enabling faster recovery and precise control but with added complexity and power consumption. Mixed quenching circuits combine elements of both passive and active designs, seeking a balance between efficiency, speed, and simplicity. These structural variations allow for tailored implementations that align with the specific demands of diverse photon detection applications.

The following sections explore these three types, providing insights into their operational principles, design considerations, and comparative effectiveness in photon detection systems, concentrating on how direct integration with the detector improves performance.

2.2 Passive Quenching Circuits

Passive Quenching Circuits (PQC) represents the simplest method to quench the avalanche current in a Single Photon Avalanche Diode (SPAD) by lowering its bias voltage below the breakdown voltage, effectively halting the multiplication process. These circuits employ a passive load, which can either be a high-value resistor or a MOSFET configured as an active load, to suppress the avalanche current. In resistor-based PQCs, the high-value quenching resistor is placed in series with either the SPAD's cathode or anode, as illustrated in Figures 2.4a and 2.4b. Alternatively, MOSFET-based PQCs utilize a MOSFET load tuned via a control voltage (VB1) to achieve a specific resistance range, with configurations connecting the MOSFET in series with either the cathode or anode, as shown in Figures 2.4c and 2.4d.

This simplicity makes PQCs an attractive choice for basic applications despite potential limitations in recovery speed and control precision compared to more complex quenching methods. In passive quenching circuits, the SPAD is initially biased to the desired voltage through a high-value quenching resistor during its waiting phase. When an avalanche is triggered, the avalanche current rises rapidly, reaching a peak value determined by the excess bias voltage divided by the SPAD's series resistance. This current discharges the SPAD's parasitic capacitance, causing the excess voltage to decay exponentially with a time constant defined by the circuit's resistance and capacitance:

$$\tau = R_q C_p \tag{2.1}$$

where R_q is the quenching resistance and C_p is the SPAD's parasitic capacitance. When an avalanche occurs, the excess voltage across the SPAD decays exponentially according to the relationship:

$$V(t) = V_{excess} e^{-t/\tau} \tag{2.2}$$

where V_{excess} represents the Initial excess bias voltage (bias voltage above the breakdown voltage) and $V(t)$ is the Voltage across the SPAD at time t. This decay behavior is governed by the time constant τ. A larger τ (resulting from a higher R_q or C_p) causes a slower voltage decay, while a smaller τ leads to faster decay. The time constant thus determines how quickly the excess bias voltage diminishes after an avalanche is triggered. A small time constant (low R_q or C_p) results in a rapid voltage decay. This quick reduction in the excess bias voltage below the breakdown voltage halts the avalanche multiplication process faster. Faster quenching minimizes the avalanche duration, reducing the risk of a self-sustaining avalanche caused by high current levels. However, a low R_q also leads to higher avalanche currents ($I_{avalanche} = V_{excess}/R_q$), which can damage the SPAD or increase noise. A key characteristic of passive quenching is that the SPAD's voltage does not drop below the

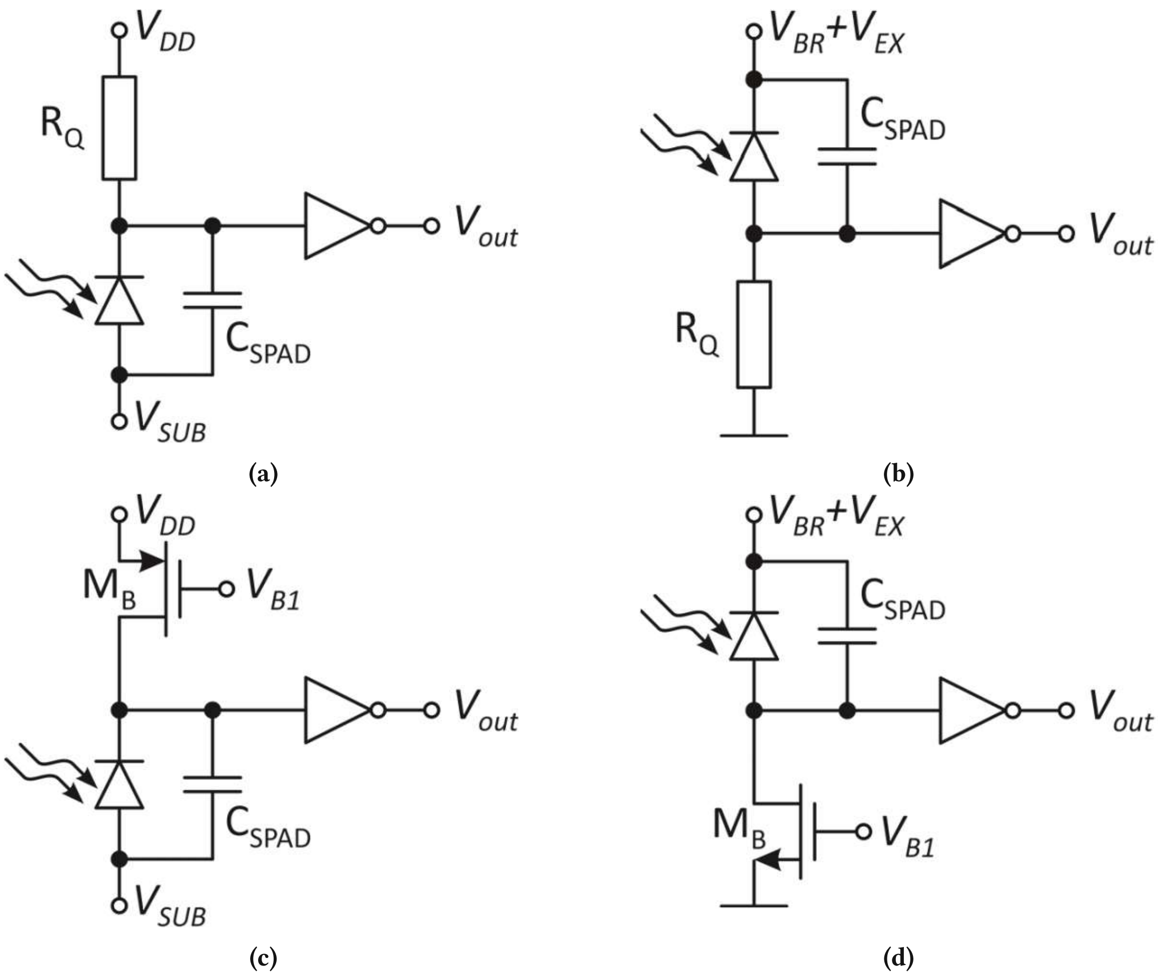


Figure 2.1: PQC: a) using quenching resistor at cathode's node, b) using quenching the resistor at the anode's node, c) using MOS-load at the cathode's node, d) using MOS-load at anode's node. [7]

breakdown voltage. As a result, the avalanche current may persist, potentially leading to a self-sustaining avalanche if the current is high enough to maintain the multiplication process. However, if the quenching resistor sufficiently limits the avalanche current, there is a high probability that all carriers will eventually leave the space charge region, allowing the avalanche to self-quench.

The operation of passive quenching circuits hinges on adequately selecting the quenching resistor. The resistor must have a sufficiently high value to limit the avalanche current and avoid self-sustaining avalanches to ensure effective quenching. At the same time, It should not be so high that it slows quenching excessively and hinders SPAD recovery. Indeed, the recovery time for subsequent photon detection events should be balanced. This design trade-off makes passive quenching circuits simple yet reliant on careful parameter optimization for reliable performance.

2.3 Active Quenching Circuits

Active quenching circuits represent a more sophisticated approach to managing avalanche currents in Single Photon Avalanche Diodes (SPADs). By incorporating fast electronic components capable of detecting the initiation of an avalanche, these circuits actively and precisely lower the bias voltage below the breakdown threshold, rapidly terminating the avalanche process. This proactive mechanism ensures faster recovery times compared to passive quenching and provides greater control over the quenching dynamics, reducing noise and enhancing performance. Active quenching circuits are indispensable in applications where high photon detection rates and precise timing are critical, such as LiDAR, quantum cryptography, and advanced imaging systems. This subsection explores active quenching circuits' operational principles, key design elements, and performance advantages.

In this type of quenching circuit, once the avalanche is detected, the control circuitry actively drives the bias voltage of the SPAD below the breakdown voltage. The avalanche current is sensed through a resistance path (resistor) and a comparator (COMP), while the quenching and resetting processes are typically achieved using high-speed electronic components such as transistors or switching circuits. The multiplication process is halted by lowering the bias voltage sharply and deliberately, preventing the avalanche from becoming self-sustaining. A pulse generator serves as the active circuitry in the simple design shown in Figure 2.2. Active quenching circuits (AQC) actively lowers the bias voltage of the SPAD below the breakdown voltage during quenching, in contrast to passive quenching circuits. This intentional decrease guarantees that the quenching procedure is not affected by statistical variations, leading to accurate and consistent performance. After the avalanche is quenched, the bias voltage is held below the breakdown threshold for a defined period, known as the hold-off time, to allow all residual charges to dissipate and prevent premature re-triggering.

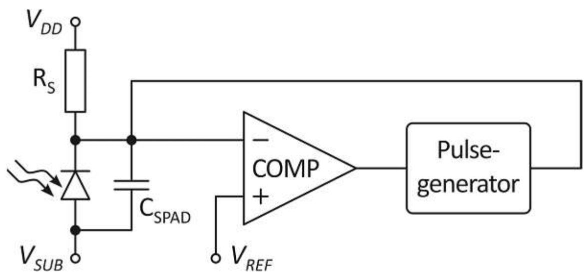


Figure 2.2: Simple schematic of an active quenching circuit. [7]

Following this hold-off time, the active circuit re-biases the SPAD to its original operating voltage. This reset process is carefully controlled to ensure the SPAD returns to its ready state as quickly as possible, minimizing downtime. The ability to dynamically control the bias voltage allows active quenching circuits to achieve much faster recovery times than passive methods, enabling high photon detection rates.

AQC has a quicker quenching transition than PQC, yet the quenching duration might not be much less. When the SPAD is linked to the AQC, the cathode voltage is displayed in Figure 2.3. An excessively extended quenching period will result in a large total avalanche charge, which in turn causes significant power dissipation and a high likelihood of after-pulsing because of trapped charges. Indeed one of the key aspects of the operation is the precise timing of quenching and resetting. The speed and accuracy of these operations depend on the quality of the sensing and control circuitry. Modern implementations use advanced signal processing and fast components to achieve nanosecond-level response times, making active quenching circuits highly suitable for applications requiring rapid and repetitive photon detection.

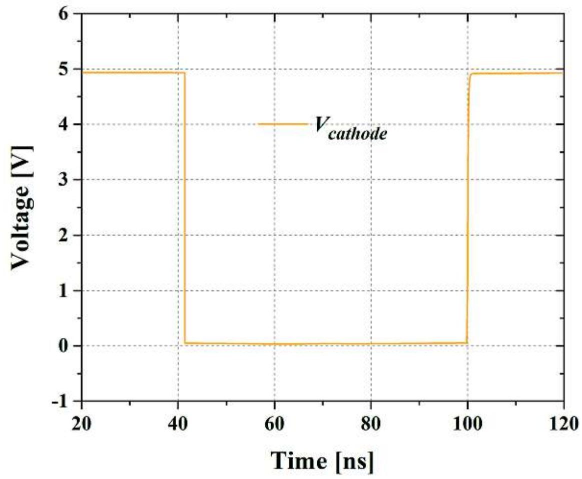


Figure 2.3: Ideal cathode voltage of the SPAD connected to the AQC. [7]

In summary, active quenching circuits operate by rapidly detecting avalanches, actively reducing the SPAD's bias voltage to stop the avalanche, and quickly resetting the SPAD to its operational state. This combination of fast detection, active intervention, and controlled resetting underpins the superior performance of active quenching circuits in demanding, time-critical applications.

2.4 Mixed Quenching Circuits

Mixed quenching circuits combine the simplicity of passive quenching with the precision and speed of active quenching, offering a balanced approach to managing avalanche currents in Single Photon Avalanche Diodes (SPADs). This hybrid technique leverages the initial current-limiting mechanism of passive quenching to moderate the avalanche current, followed by an active intervention to terminate the avalanche and reset the SPAD precisely. By integrating these two methods, mixed quenching circuits achieve a compromise between circuit complexity, quenching speed, and recovery efficiency. These circuits are particularly advantageous in applications that demand high photon detection rates but prioritize energy efficiency and robustness, such as biomedical imaging, optical communication, and scientific instrumentation. The following explores mixed quenching circuits' operational principles and advantages.

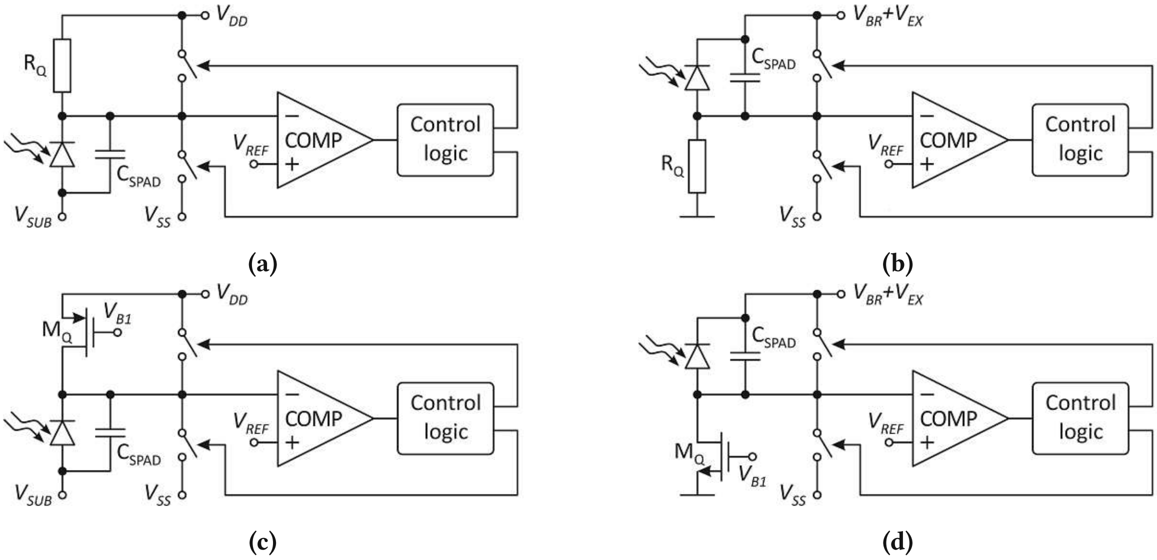


Figure 2.4: Mixed quenching circuits: a) using quenching resistor at cathode's node, b) using quenching resistor at anode's node, c) using MOS-load at cathode's node, d) using MOS-load at anode's node. [7]

In a mixed quenching circuit, the SPAD is connected to both a high-impedance load—either a high-value quenching resistor (R_Q) or a MOSFET configured as a load (M_Q)—and active quenching and reset circuitry. Figure 2.4 illustrates the basic schematics of mixed quenching circuits, showing configurations where the SPAD is paired with either the quenching resistor or the active MOSFET load. When an avalanche is triggered, the initial current flows through the quenching resistor (R_Q) or MOSFET load (M_Q), effectively limiting the avalanche current in a manner similar to Passive Quenching Circuits (PQCs). This initial passive quenching moderates the avalanche and ensures current limitation.

As the voltage drop across the SPAD reaches a predefined threshold, the active circuitry detects the avalanche event via a fast comparator. At this point, the active quenching process is initiated, taking over from the passive mechanism. The active circuitry then behaves as in an Active Quenching Circuit (AQC), driving the SPAD's bias voltage below the breakdown threshold to fully terminate the avalanche. Afterward, the circuit enforces a hold-off time to allow residual carriers to dissipate before actively restoring the SPAD's bias voltage to its operational level. This combination of passive and active mechanisms provides enhanced quenching efficiency and faster recovery times, making mixed quenching circuits a versatile solution for photon detection.

Integrating the quenching circuitry with the SPAD minimizes parasitic capacitance, resulting in more minor avalanche charges, faster reaction times, and shorter reset durations in mixed-mode quenching circuits. However, it is essential to consider the physical constraints of integration. The circuit's area requirements limit this approach to individual SPADs or small SPAD arrays, making it less suitable for large SPAD arrays. Compared to Passive Quenching Circuits (PQCs), mixed quenching circuits offer significant advantages, including faster reset times and a well-defined dead time, which align more closely with Active Quenching Circuits (AQCs). Notably, the total avalanche charge in Mixed Quenching Circuits (MQCs) is similar to that in PQCs when the active circuitry's slow reaction time allows passive quenching to dominate. Conversely, when the reaction time is sufficiently short, the active circuit limits the avalanche charge, reducing it below the levels typically observed in PQCs. This relationship between reaction time and total avalanche charge highlights the adaptability of MQCs and makes them a versatile solution for balancing speed, charge control, and integration efficiency.

As mentioned, quenching circuits are a fundamental component in the operation of Single Photon Avalanche Diodes (SPADs), playing a crucial role in reliably terminating avalanches and enabling efficient recovery for subsequent photon detection. The three primary types of quenching circuits—Passive Quenching Circuits (PQCs), Active Quenching Circuits (AQCs), and Mixed Quenching Circuits (MQCs)—each offer unique advantages suited to specific performance requirements and application needs. PQCs are characterized by their simplicity and reliability but are constrained by slower recovery times and less precise control. In contrast, AQCs deliver rapid response and precise quenching dynamics, making them ideal for time-sensitive applications, though their complexity can be a drawback. MQCs effectively combine the strengths of both approaches, offering a balance of speed, control, and simplicity, making them a versatile solution for diverse photon detection systems.

The next chapter will explore, according to the concepts discussed, the practical implementation of quenching circuits in 0.35-µM CMOS technology.

3 Circuit Design of Quencher for SPADs in 0.35-µm CMOS

Quenching circuits have seen significant advancements in recent years to enhance the performance of SPAD-based systems. As previously mentioned, the performance of SPAD optical sensors is directly influenced by the characteristics of their quenching circuits. For instance, a sluggish quenching circuit can degrade timing responsiveness or limit the maximum counting rate. Therefore, selecting and designing a quenching circuit that meets the specific requirements of the intended application is critical. This chapter addresses the necessity of high-voltage transistors, explores the limitations and opportunities of the 0.35-µm CMOS process technology, and provides a detailed analysis of the design and optimization of the proposed circuit. A fully controllable, fast-mixed quenching and active resetting circuit, fabricated in 0.35-µm high-voltage CMOS technology for integrated SPADs, is presented as an optimized version of the fully integrated optical sensor IC, as illustrated in Figure 3.1.

The proposed quenching circuit comprises several key blocks: a quenching/resetting switch, a sensing and current-cutting stage, a dead time control stage, voltage translators, and a quenching MOSFET disabling circuit. Built on a tunable-threshold inverter designed for 0.35-µm high-voltage CMOS technology, this fully integrated optical sensor IC incorporates a SPAD, a quenching/resetting circuit, and an innovative sensing stage. The circuit features an adjustable total dead time and a regulated excess bias voltage [8].

The quenching/resetting switch includes MOSFETs M_{Q1} and M_{Q2} for the quenching path and M_{R1} and M_{R2} for the resetting path. The sensing and current-cutting stages comprise MOSFETs M_1, M_3, M_4, M_{3R}, and M_{4R}, along with inverters I_1, I_3, I_4, and an operational amplifier. The dead time control stage comprises MOSFETs M_{S1}, M_6, and M_7, inverters I_5 and I_6, a Schmitt trigger (ST_1), a resistor RB_1, and a capacitor CT_1. Voltage translators and the quenching MOSFET disabling circuit include MOSFET M_{OFF}, inverters I_2, I_7, I_8, I_{11}, and I_{12}, resistors R_{S1} through R_{S4}, and capacitors C_{S1} and C_{S2}. Additionally, inverters I_9 and I_{10} shape the V_{reset} pulse, which controls the resetting MOSFET M_{R1}.

The operation of the circuit is categorized into three phases: the first phase, referred to as the sensing and current-cutting phase; the second phase, which is the quenching

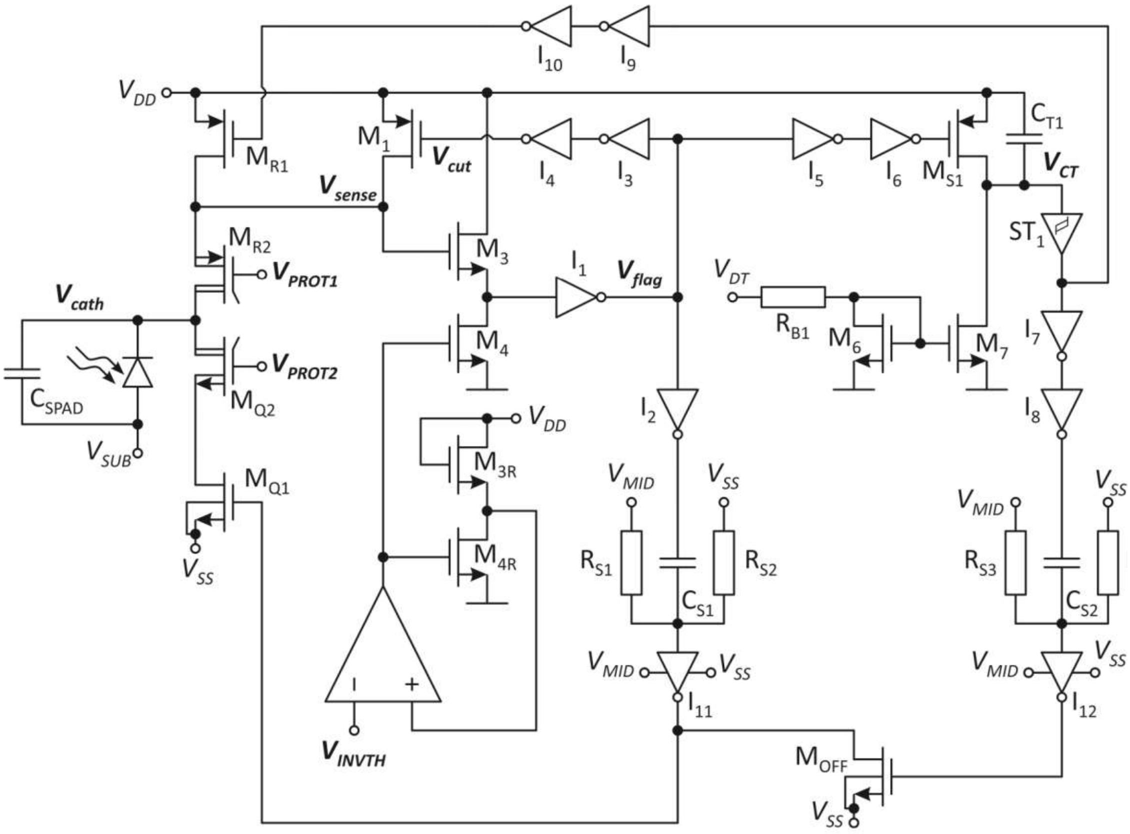


Figure 3.1: Ideal cathode voltage of the SPAD connected to the AQC. [8]

phase; and the third phase, known as the resetting phase. In the waiting mode, the SPAD cathode is maintained at a potential approximately equal to V_{DD} (+3.3 V). Simultaneously, the capacitor CT_1 in the dead-time control circuit is charged to V_{DD}. The control signals for the quencher when in its off-state, are defined as follows: V_{quench} = V_{off} = -16.7 V (logic low), and V_{reset} = 3.3 V (logic high).

An avalanche occurs when the SPAD absorbs a photon. During this event, the current flows through MOSFETs M_1 and M_{R2}. Furthermore, the SPAD's current causes a voltage drop at the V_{sense} node. Additionally, the source-follower circuit, composed of MOSFETs M_3 and M_4, buffers (or shifts) the V_{sense} voltage to the gate of inverter I_1. For a brief period, the quenching circuit operates as a passive quenching circuit until the shifted V_{sense} voltage exceeds the threshold level of inverter I_1. When the shifted V_{sense} voltage surpasses this threshold, the detecting MOSFET M_1 is switched off, and V_{flag} transitions from logic "0" to logic "1," generating the voltage V_{cut} = V_{DD}. With MOSFET M_1 turned off, no current path is established, preventing additional charges from flowing into the SPAD. The passive quenching time is defined as the interval between photon absorption and the disabling of MOSFET M_1, during which the SPAD's current is cut off. Once the SPAD's current is interrupted, the voltage V_{flag} is processed through a voltage translator circuit (R_{S1}, R_{S2}, C_{S1}, I_{11}), generating a V_{quench} voltage that controls the quenching MOSFET M_{Q1}. After the quenching delay, M_{Q1} turns on, initiating the active quenching phase and pulling the SPAD's cathode down to V_{SS}. The total excess bias is expressed as $V_{EX} = V_{DD} - V_{SS}$. Simultaneously, when V_{quench} is generated, MOSFET M_{S1} is turned off, and the voltage V_{CT} begins to decrease linearly. When V_{CT} drops below the threshold of the Schmitt trigger ST_1, its output transitions to logic "0". The signal V_{CT} is then buffered by inverters (I_7, I_8) and translated through another voltage translator circuit (R_{S3}, R_{S4}, C_{S2}, I_{12}), producing a V_{off} voltage that drives the disabling MOSFET M_{OFF}, pulling the gate of M_{Q1} down to V_{SS}. This action disables M_{Q1}, marking the end of the quenching phase. The duration of the quenching pulse determines the hold-off time T_{HOLD}, which is given by the equation

$$T_{HOLD} = (V_{THST} \times R_{B1} \times C_{T1})/(V_{DT} - V_{GS6}) \tag{3.1}$$

where V_{THST} is the threshold voltage of the Schmitt trigger ST_1.

The resetting MOSFET MR1 is driven by the resetting voltage Vreset, which is generated around the same time as the voltage V_{off}. When MOSFET M_{R1} is activated, the SPAD's cathode is restored to V_{DD} (+3.3 V). Once resetting is completed, the SPAD is rearmed and ready to detect a new photon.

As illustrated in Figure 3.1, this circuit incorporates two high-voltage transistors, M_{Q2} and M_{R2}, which could be critical components in designing these active quenching and resetting circuits for Single Photon Avalanche Diodes (SPADs). These transistors enable the circuits to handle the elevated voltages required for SPAD operation effectively. Since SPADs operate above their breakdown voltage, fast and reliable quenching mechanisms are essential for precise and efficient photon detection. High-voltage transistors provide the necessary voltage levels to achieve rapid quenching and resetting, thereby reducing afterpulsing effects and optimizing Photon Detection Probability (PDP). Moreover, they are adept at managing high photon count rates, allowing the circuits to perform efficiently at high speeds, as demonstrated across various CMOS technology implementations. By offering precise control over the quenching and resetting processes, these transistors enhance timing resolution and improve overall circuit performance, establishing themselves as indispensable components in SPAD-based photon detection systems. Further details about these transistors will be discussed in the following section.

3.1 High Voltage Transistors

High-voltage transistors are indispensable in the design of active quenching and resetting circuits for Single-Photon Avalanche Diodes (SPADs). Their ability to handle elevated voltages, facilitate rapid quenching, and support high-speed operation makes them an ideal choice for these applications. This section examines the role of high-voltage transistors in SPAD quencher circuits, emphasizing their critical contributions to achieving efficient photon detection and managing high count rates. By exploring their operational characteristics and performance benefits, we aim to establish a comprehensive understanding of their significance in SPAD-based systems.

N-channel double-diffused high-voltage transistors (NMOS), M_{Q2}, and their complementary PMOS counterparts, M_{R2}, were utilized in the design of the quencher circuit. These transistors were specifically chosen for their capability to manage the high voltages required for SPAD operation while ensuring efficient and reliable performance. The N-channel double-diffused high-voltage transistors and their PMOS counterparts play a crucial role in managing the elevated voltages and fast switching requirements of the quencher circuit. These transistors are specifically designed for high-voltage CMOS technologies, allowing them to operate reliably in environments with high electric fields. The double-diffused design of these transistors enhances their ability to withstand high voltages by optimizing the electric field distribution across the device. This is achieved through a carefully engineered doping profile, which reduces the risk of breakdown while maintaining high performance. The NMOS transistors, M_{Q2}, provide fast switching capabilities, essential for rapid quenching of the SPAD. Conversely, the PMOS transistors, M_{R2}, ensure efficient resetting of the SPAD by providing complementary functionality within the circuit. These high-voltage transistors are integral to achieving the precise control required in active quenching and resetting operations. Their robust design allows them to:

- Manage the high-bias voltages essential for the operation of Single Photon Avalanche Diodes (SPADs) without degradation.
- Facilitate rapid transitions to minimize afterpulsing and enhance photon detection probability (PDP).
- Ensure reliable operation under high-speed conditions, maintaining compatibility with the swift photon detection rates characteristic of SPAD systems.

A key advantage is the seamless integration of these transistors within conventional CMOS processes. This compatibility streamlines the fabrication of the quencher circuit, allowing for a compact and efficient design while ensuring performance consistency across various implementations. Advanced techniques, such as deep n-well isolation and specialized oxide growth, are employed to incorporate these transistors without compromising the density or scalability of the circuit. Some advantages of CMOS integration include:

- Compact Design: Combining high-voltage and low-voltage components on a single chip reduces overall footprint.
- Cost Efficiency: Leveraging established CMOS processes minimizes fabrication costs compared to custom high-voltage solutions.
- Process Compatibility: High-voltage CMOS technologies allow the integration of other critical components, such as signal processing and timing circuits, on the same substrate.

The double-diffused structure of high-voltage transistors is achieved through a tailored doping process that ensures a gradual electric field distribution across the device. For the NMOS transistors, the source and drain regions are heavily doped to minimize resistance, while the lightly doped drain (LDD) regions mitigate hot-carrier effects and improve reliability under high-voltage operation. Similarly, the PMOS transistors are engineered with complementary doping strategies to provide efficient switching and resetting functions. Their design not only ensures reliable operation under the stringent requirements of SPAD applications but also facilitates the scalability and efficiency needed for modern photon detection systems.

3.1.1 Performance Metrics in the Quencher Circuit

The performance of high-voltage transistors in the quencher circuit is critical for ensuring the efficiency and reliability of SPAD operation. These transistors are evaluated based on several key metrics, which collectively influence the overall performance of the photon detection system.

3.1.1.1 Switching Speed

Switching speed is one of the most critical metrics for high-voltage transistors in SPAD quencher circuits. It determines how quickly the transistors can transition between states, ensuring rapid quenching of the SPAD's avalanche current and resetting for subsequent photon detection [9].

- The rise and fall times of the transistors must be in the order of nanoseconds or faster. For example, in high-speed SPAD applications where the photon count rate exceeds 10^7 counts per second, the transistors must switch in under 100 ns. This allows the SPAD to operate efficiently at high count rates without missing photon events.
- A low gate capacitance is essential to achieve high-speed operation. The transistors in CMOS processes are optimized to minimize parasitic capacitance, which directly impacts the delay in switching.
- Faster switching speeds improve the SPAD's timing resolution, which is crucial in time-correlated photon counting applications like LiDAR and fluorescence lifetime imaging.

3.1.1.2 On-Resistance (R_{ON})

On-resistance (R_{ON}) refers to the resistance of the transistor in the ON state. This parameter has a direct impact on the power dissipation and efficiency of the quencher circuit [9].

- Minimizing Power Loss: Low R_{ON} in NMOS transistors reduces power loss during the quenching phase. For instance, if the quenching current (I_{Q}) is 10 mA and

$R_{ON} = 10\,\Omega$, the power dissipation is $P = I_Q^2 \cdot R_{ON} = 1\,\text{mW}$. Lower values of R_{ON} further reduce energy loss, enhancing circuit efficiency.

- High-Voltage Compatibility: Despite operating at elevated voltages, these transistors maintain a low R_{ON} through careful design of the channel length and doping profiles.

3.1.1.3 Breakdown Voltage (V_{BR})

The breakdown voltage defines the maximum voltage the transistor can sustain without undergoing permanent damage or degradation [10].

- High Bias Requirements of SPADs: SPADs typically operate at voltages exceeding their breakdown voltage by 5-10 V (over-biasing). For example, if the SPAD breakdown voltage is $25\,\text{V}$, the quenching circuit must reliably handle voltages up to $35\,\text{V}$.

- Ensuring Longevity: Transistors with higher V_{BR} ensure long-term reliability under continuous operation. This is achieved through optimized doping profiles and the inclusion of lightly doped drain (LDD) regions to reduce the peak electric field.

3.1.1.4 Thermal Performance

Thermal performance is crucial in high-speed SPAD applications, where the transistors experience continuous switching at high currents [11].

- Heat Dissipation: Efficient heat dissipation is essential to prevent thermal runaway. This is addressed through the use of materials and layouts that improve thermal conductivity. For instance, the substrate and metal layers are designed to spread heat effectively across the chip.

- Impact on Reliability: Poor thermal management can lead to a degradation in transistor performance, including an increase in R_{ON} and a reduction in V_{BR}. High-voltage transistors in SPAD quencher circuits are designed to operate within safe thermal limits, ensuring consistent performance.

The high-voltage transistors in SPAD quencher circuits must excel in switching speed, minimize on-resistance, reliably handle high breakdown voltages, and efficiently dissipate heat. Each metric contributes to the overall functionality, reliability, and efficiency of the system, ensuring it meets the stringent requirements of modern photon detection applications.

3.1.2 High-Voltage Transistors Used in the Design

As discussed in the previous section, selecting high-voltage transistors is critical in achieving optimal performance in SPAD quencher circuits. The high-voltage transistors, $ndhi$

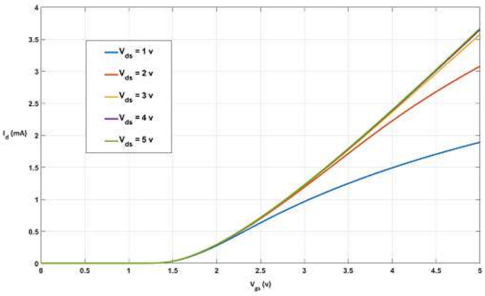
and $phvb$, were employed in the SPAD quencher circuit design [8] due to their proven high-voltage handling capabilities and seamless integration with CMOS technology. However, through the optimization process, it became clear that replacing these transistors with ndhf and phve could address certain performance limitations and significantly enhance the circuit's efficiency and reliability. The following provides a comparative analysis of the electrical characteristics of these transistors to explain the rationale for this substitution.

The $ndhi$, or N-channel Double-diffused High-Voltage Isolated transistor, is a specialized N-channel MOSFET designed for enhanced performance in high-voltage environments. Its double-diffusion technology ensures superior voltage tolerance, while isolation techniques mitigate latch-up and parasitic conduction, making it ideal for high-speed switching in power applications and active quenching circuits for SPADs. Complementing this is the $phvb$ transistor, or P-channel High Voltage Bulk transistor, a P-channel MOSFET optimized for high-voltage operation. The $phvb$ transistor is commonly employed for high-side switching, quenching circuits, and level shifters in high-voltage domains. It can handle voltages ranging from tens to hundreds of volts. These transistors provide the essential high-voltage handling and switching capabilities required for efficient SPAD quencher circuits.

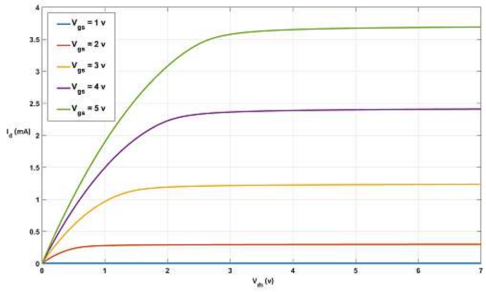
Figure 3.2 presents four diagrams that compare the electrical characteristics of the transistors under study. Subfigure 3.2a shows the I_d-V_{gs} curve for $ndhi$, while subfigure 3.2b illustrates its I_d-V_{ds} curve. Similarly, subfigures 3.2c and 3.2d depict the corresponding I_d-V_{gs} and I_d-V_{ds} curves for $ndhf$, respectively. These plots provide critical insights into the key performance parameters of each transistor type, enabling a comprehensive comparison.

The presented I_d-V_{gs} and I_d-V_{ds} curves reveal essential details about the electrical characteristics of the transistors used in the SPAD quencher circuit, with particular focus on parameters that govern performance and efficiency. One of the most critical parameters is the **threshold voltage** (V_{th}), which defines the minimum gate-to-source voltage required to turn the transistor on. A lower V_{th} enables faster switching and reduces the delay in the quenching and resetting processes, which is especially vital for maintaining high photon count rates in SPAD applications. In contrast, excessively low V_{th} may compromise noise immunity, requiring careful optimization to strike a balance between speed and stability.

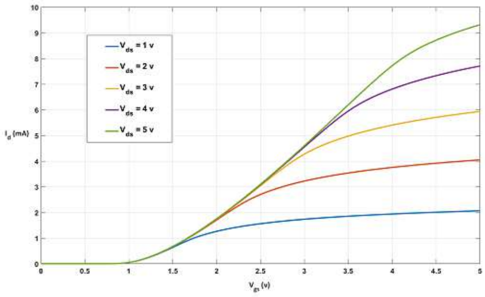
Another crucial factor is the **saturation current** ($I_{\text{D,sat}}$), representing the maximum drain current the transistor can achieve when operating in saturation mode. Higher $I_{\text{D,sat}}$ allows the transistor to handle larger current flows without significant performance degradation, making it suitable for high-speed, high-efficiency applications. Complementing this is the **on-resistance** (R_{ON}), a measure of resistance during conduction. Lower R_{ON} reduces power dissipation and heat generation, ensuring better energy efficiency and long-term reliability. This is particularly critical in SPAD circuits, where minimizing losses is essential for optimal thermal management. Finally, the **breakdown voltage** (V_{BR}) defines the maximum voltage the transistor can sustain without electrical breakdown. A high V_{BR} ensures the device operates reliably under elevated bias conditions, which is fundamental in SPAD systems that require consistent performance at high voltages. Together, these parameters highlight the intricate balance of electrical properties that determine the suitability of high-voltage transistors in quencher circuits, underscoring the importance of detailed performance



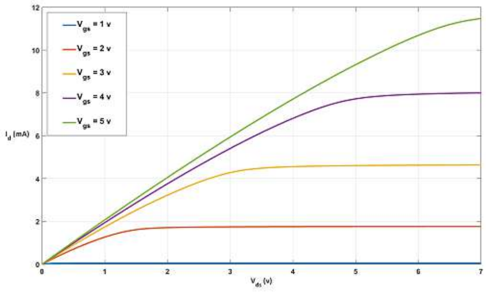
(a) I_d-V_{gs} $ndhi$



(b) I_d-V_{ds} $ndhi$



(c) I_d-V_{gs} $ndhf$



(d) I_d-V_{ds} $ndhf$

Figure 3.2: Characteristics of high voltage transistors

analysis during the design and optimization processes.

In the initial design of the SPAD quencher circuit, $ndhi$ and $phvb$ transistors were employed, offering reliable performance for high-voltage operation and the quenching/resetting processes. These transistors successfully met the basic requirements, ensuring the circuit functioned as intended. However, as the system's demands increased, certain limitations began to emerge. Specifically, the relatively higher threshold voltage and on-resistance of $ndhi$ and $phvb$ posed challenges to achieving optimal efficiency, particularly at high photon count rates. These constraints highlighted the need for an optimization process to enhance the circuit's overall performance.

Through the optimization process, the $ndhf$ transistor, or N-channel Double-diffused High-Voltage Fast transistor, which is a specialized N-channel MOSFET optimized for high-frequency or fast-switching operation, was identified as a superior alternative. Its high breakdown voltage and rapid response are ideal for timing-critical applications and signal amplification in high-voltage systems. Compared to $ndhi$, $ndhf$ exhibits a lower threshold voltage, enabling faster switching and reduced delay in quenching operations. At the same time, its higher saturation current enhances current-handling capabilities essential for high-speed SPAD systems. Complementing this, the PHVE transistor, or P-channel High Voltage Enhanced transistor, offers significant improvements over the $phvb$. With enhanced characteristics such as reduced on-resistance and improved switching efficiency, $phve$ minimizes power losses and boosts energy efficiency. These attributes improve circuit thermal performance by mitigating heat generation and allow $phve$ to handle higher power densities, making it suitable for power management and precision analog circuits.

The substitution of $ndhi$ and $phvb$ with $ndhf$ and $phve$ marked a pivotal improvement in the SPAD quencher circuit design. By leveraging the enhanced characteristics of $ndhf$ and $phve$, the circuit achieved faster switching speeds, better thermal management, and greater efficiency, even under the demanding conditions of high photon count rates. These advancements directly translated to improved overall system reliability and performance, highlighting the critical role of selecting appropriate high-voltage transistors for such applications.

This optimization process underscores the importance of tailoring transistor selection to meet the stringent requirements of SPAD-based systems. The transition from $ndhi$ and $phvb$ to $ndhf$ and $phve$ not only addressed specific limitations in the initial design but also demonstrated how strategic modifications can elevate the performance of high-voltage circuits. Such improvements are vital for maintaining the efficiency and accuracy demanded by modern photon detection technologies.

3.2 Process Technology

The semiconductor fabrication process employed in this thesis is the "XH035" from XFAB [12], a 0.35 µm high-voltage BiCMOS p-substrate process. This versatile process is tailored for standard cell, semi-custom, and full custom designs, primarily targeting industrial, automotive, and telecommunication applications.

The XH035 technology is based on a single poly triple metal 0.35 µm drawn gate length process, which supports both digital and analog functionalities. It features a variety of core and process modules, including low threshold voltage (low Vt) options, low leakage transistors, embedded non-volatile memory (NVM), and high-voltage (HV) transistors capable of handling operating voltages up to 100V. Additionally, it includes advanced features such as double poly and MIM capacitors, a high-resistance polysilicon layer, and options for a standard or thick fourth metal layer [13]. These components are critical for achieving precise analog performance, stable capacitance values, and compact circuit integration. The high-resistance polysilicon layer, in particular, facilitates the design of resistive components with minimal layout area and high linearity.

The process also provides MOS, bipolar, and Double diffusion metal oxide semiconductor (DMOS) transistors, making it highly flexible for a broad range of applications [14]. A particularly noteworthy feature of the XH035 process is its low-noise p-MOS and n-MOS transistors, which deliver a high signal-to-noise ratio, making them ideal for precision analog applications requiring minimal noise. Furthermore, the process includes 45V DMOS transistors with a 45% reduction in on-resistance, enabling significant chip area savings of up to 40% [14].

For the purposes of this thesis, which focuses on the design and implementation of SPADs, several process capabilities are critical. SPADs operate in Geiger mode, requiring a reverse bias voltage that exceeds the breakdown voltage, V_{break}, typically around -30V for devices in this process.The XH035's deep-nwell integration is indispensable for isolating sensitive SPAD devices from substrate noise and for enabling robust high-voltage operation. This feature is particularly crucial for SPAD implementations, where precise control of the avalanche region and electrical isolation from surrounding circuitry directly impact device performance.

3.2.1 0.35-µm HV-CMOS SPAD

As shown in Figure 3.3, a SPAD fabricated using a 0.35-µm high-voltage CMOS process employs an n+/p-well junction structure, which facilitates efficient avalanche multiplication while maintaining compatibility with standard CMOS fabrication processes. The deep p-well and deep n-well layers help define the avalanche region and provide isolation from the substrate, reducing noise and improving performance. The inclusion of these wells ensures that the high electric field necessary for avalanche breakdown is well-confined, leading to stable and reliable photon detection.

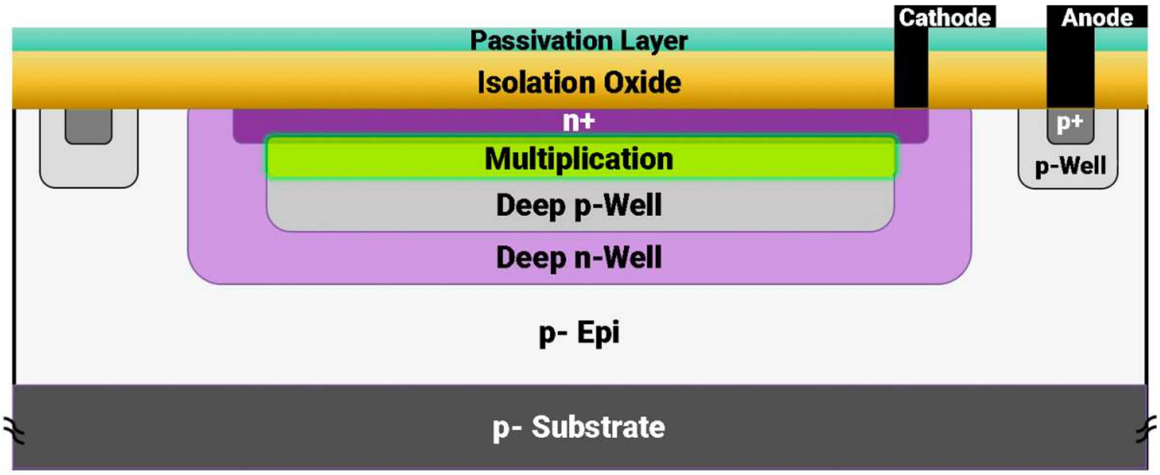


Figure 3.3: Cross section of the 0.35-µm HV-CMOS SPAD [15]

The photon detection process in SPADs begins when an incident photon is absorbed in the depletion region of the reverse-biased p-n junction, generating an electron-hole pair. Due to the high electric field in this region, the generated charge carriers (typically electrons in an n+/p-well SPAD) are rapidly accelerated, gaining sufficient energy to initiate impact ionization. This secondary ionization process produces additional electron-hole pairs, leading to a self-sustaining avalanche. This avalanche multiplication amplifies the initial signal to a detectable level, effectively converting a single-photon event into a measurable electrical pulse.

The XH035 high-voltage CMOS process provides a deep depletion region, which enhances the photon detection probability (PDP) and minimizes timing jitter by allowing for rapid avalanche buildup. However, a key challenge in CMOS-based SPADs is the absence of an anti-reflection coating, which can reduce quantum efficiency due to photon loss at the surface. To mitigate this, process optimizations such as junction engineering, optical stack tuning, and doping profile modifications are implemented to enhance PDP across a broad spectral range.

Additionally, the presence of shallow trench isolation (STI) and guard rings in the XH035 process helps suppress crosstalk and reduce the dark count rate (DCR). Crosstalk occurs when an avalanche in one SPAD unintentionally triggers a neighboring SPAD due to lateral charge diffusion. By integrating STI and optimized guard ring structures, electrical interference between adjacent pixels is minimized, leading to improved overall detection performance and reducing the probability of false detections.

Once the avalanche is triggered, the SPAD requires a quenching mechanism to stop the breakdown and reset the diode for the next detection event. This can be achieved using either passive quenching (with a simple resistor) or active quenching (using a MOSFET-based circuit). Active quenching provides faster recovery times and better control over avalanche behavior, which is particularly beneficial for applications requiring high photon count rates and low afterpulsing effects.

In the study [16], the performance of SPADs fabricated in a 0.35-μm high-voltage CMOS process was thoroughly analyzed. The study provides insights into photon detection efficiency, dark count rate, and timing resolution of these SPADs, demonstrating the advantages of using a high-voltage CMOS process for SPAD fabrication. The results indicate that careful process and layout optimizations, such as well-engineered doping profiles and optimized guard ring structures, can significantly enhance PDP while keeping DCR and afterpulsing effects at manageable levels.

By leveraging the benefits of a high-voltage CMOS platform, these SPADs achieve a balance between high sensitivity, low power consumption, and scalability, making them an ideal choice for advanced CMOS-based photonic and sensing systems. The integration of deep-well structures and STI isolation plays a crucial role in defining the avalanche region, reducing electrical crosstalk, and improving overall photon detection performance, as illustrated in Figure 3.3. These advancements highlight the potential of high-voltage CMOS SPADs in applications demanding precise single-photon detection, further emphasizing their role in next-generation imaging and sensing technologies.

The XH035 process not only enables the integration of high-voltage transistors and SPADs but also provides a versatile platform for advanced mixed-signal and optoelectronic applications. Its combination of high-voltage capability, optimized doping profiles, and well-engineered isolation structures ensures robust device performance across a wide range of applications. These attributes establish XH035 as a compelling choice for high-sensitivity detection circuits, including the SPAD-based designs explored in this thesis.

3.3 Circuit Design

Figure 3.4 shows a schematic of the proposed quenching circuit, centered around optimizing the performance of the SPAD by effectively managing the avalanche current and facilitating a rapid reset after photon detection. The chip designed in this thesis contains a fully integrated SPAD with circuitry for quenching and resetting it. As introduced at the beginning of this chapter, the quenching circuit comprises several key stages that work in tandem to ensure reliable operation and minimize dead time. These stages include the quenching/resetting switch, the sensing and current-cutting stage, the dead-time control stage, voltage translators, and a quenching MOSFET disabling circuit.

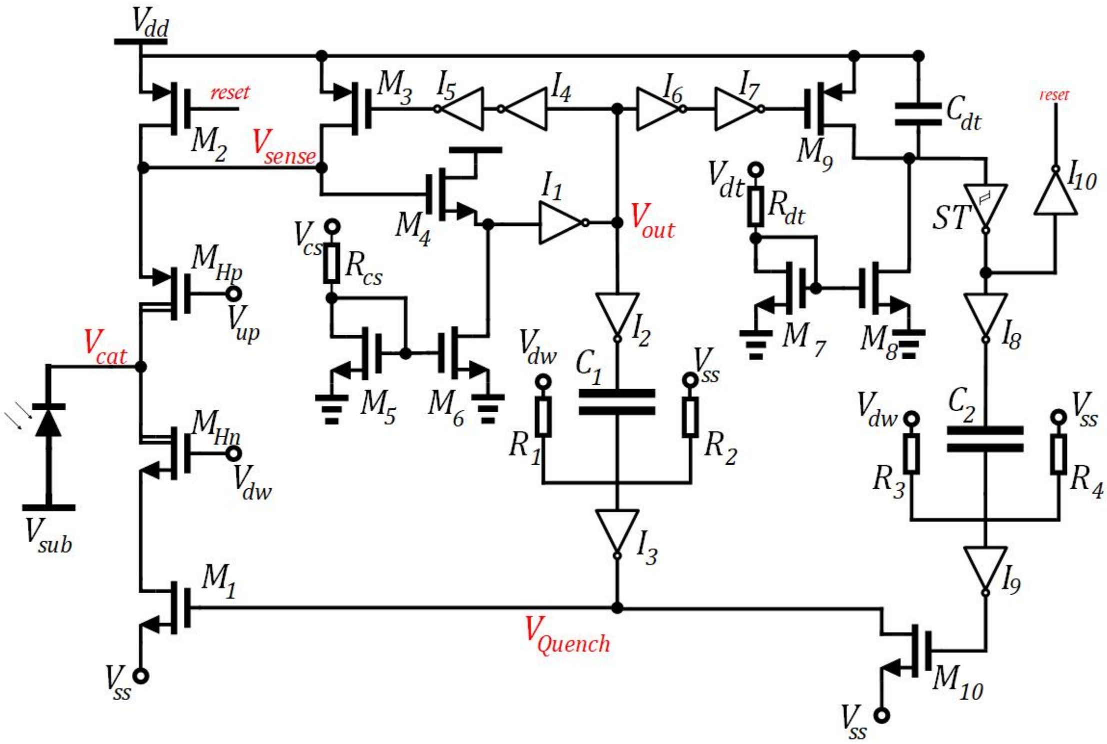


Figure 3.4: Schematic of proposed active quencher circuit

Each of these stages plays a critical role in controlling the SPAD's behavior during and after photon detection. In the following sections, the design considerations for each block will be discussed in detail, highlighting how each stage contributes to the overall performance of the SPAD, including aspects such as speed and power efficiency.

3.3.1 Overview of Design Philosophy

The design of the quenching circuit is driven by the need for fast and reliable quenching to ensure accurate single-photon detection. In the operation of a SPAD, the carrier flow must be quenched by reducing the voltage across the SPAD below its breakdown voltage. This decreases the electric field, effectively halting the impact ionization process and suppressing the avalanche current. To reset the SPAD for subsequent photon detection, the reverse bias voltage must be restored above the breakdown voltage. The interval between the avalanche trigger and the restoration of Geiger mode is defined as the dead time.

Minimizing dead time is essential for maximizing the detector's count rate; however, it introduces challenges related to afterpulsing. During the avalanche process, some carriers become trapped in the semiconductor's trapping centers and are randomly released later, potentially triggering a false photon detection known as the afterpulsing effect. The probability of afterpulsing is influenced by the density of trapping centers in the semiconductor and the total number of carriers generated during the avalanche.

To mitigate the afterpulsing probability (APP), the quenching circuit employs two complementary strategies. First, the active quenching mechanism increases the dead time, allowing more time for trapped carriers to recombine before the SPAD re-enters Geiger mode. However, longer dead times can reduce the maximum count rate of the detector, which introduces a design trade-off. Second, the circuit incorporates a fast quenching stage to limit the avalanche charge by quickly discharging the SPAD's capacitance. This approach effectively reduces the avalanche duration, thereby lowering the APP and minimizing the SPAD's self-heating effect and the emission of secondary photons.

Therefore, this quenching circuit's design philosophy is guided by the need to balance competing requirements: minimizing dead time for high-speed operation while reducing the APP to maintain detection accuracy. These objectives are achieved through precise voltage control, rapid quenching, and optimized dead-time management, ensuring compatibility with the SPAD's operating characteristics and the constraints of the XH035 process.

3.3.2 Block-by-Block Description

To ensure efficient and accurate operation of the SPAD, the proposed quenching circuit, figure 3.4 is divided into several functional blocks, each tailored to address specific operational requirements. Each block is designed to fulfill a unique role in the circuit's operation, from rapidly suppressing the avalanche current to managing precise timing and voltage transitions. Together, they form an integrated system that ensures high-speed operation while minimizing afterpulsing and self-heating effects.

The following sections describe each block, outlining its purpose, design considerations, and implementation within the XH035 process.

The **Quenching/Resetting Switch** is responsible for rapidly disconnecting the SPAD from the power supply upon detecting an avalanche event. This action suppresses the avalanche current, preventing potential damage to the SPAD and ensuring it is ready for subsequent detection. This block consists of MOSFETs M_1 and M_{Hn} for the quenching path and M_2 and M_{Hp} for the resetting path, Figure 3.5. The switch is implemented using high-voltage transistors that are capable of handling the voltage levels required by the XH035 process. The gate drive circuitry of these MOSFETs is carefully designed to minimize switching delays, ensuring the rapid suppression of avalanche current. By efficiently quenching the avalanche current, this block plays a pivotal role in reducing the afterpulsing probability (APP) and limiting the SPAD's self-heating effect, both of which are critical for maintaining the accuracy and reliability of the SPAD.

The **sensing** and **current-cutting stage** monitor the avalanche event and ensure precise timing for current suppression. As shown in Figure 3.6, it is composed of MOSFETs $M_3 - M_6$, resistor R_{cs}, and inverters I_1, I_4, and I_5. In this stage, M_6 and M_7 form a current

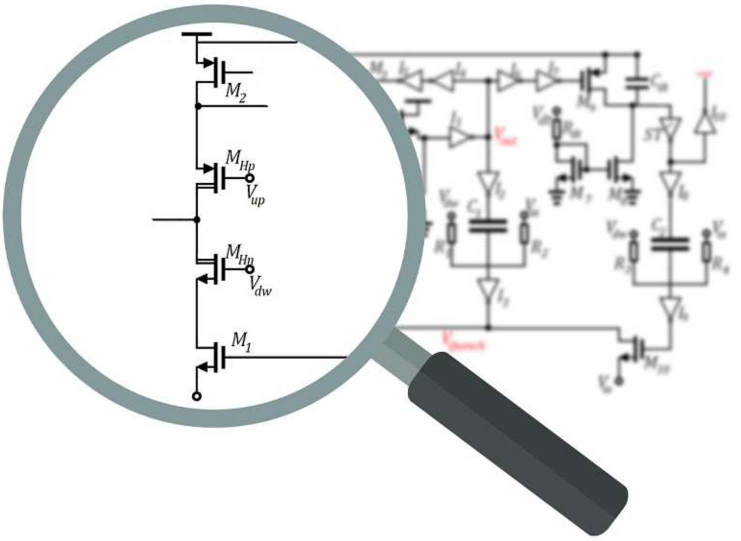


Figure 3.5: Quenching/Resetting Switch

mirror, with R_{cs} acting as the reference resistor to establish the mirrored current. The drain of M_7, which serves as the output of the current mirror, is connected to the source of M_4 and simultaneously to the input of inverter I_1. This connection maintains the input of the inverter at a specific voltage, ensuring stable operation of the sensing stage.

The design of this stage is critical for balancing sensitivity and noise suppression. The current mirror ensures accurate replication of the sensed current, while R_{cs} sets a precise reference for the mirrored current. The connection to inverter I_1 ensures that the voltage at its input remains well-defined, preventing transient noise from disrupting the sensing process. The inverter chain further amplifies the sensed signal and filters out high-frequency disturbances, enabling reliable current sensing and triggering of the quenching/resetting switch.

The **dead-time control stage** defines the interval between quenching and resetting, ensuring the SPAD remains inactive for a specified duration to minimize afterpulsing. This stage, Figure 3.7 comprises MOSFETs $M_7 - M_9$, resistor R_{dt}, capacitor C_{dt}, inverters I_6 and I_7, and a Schmitt trigger ST. In this stage, M_7 and M_8 form a current mirror, with R_{dt} acting as a variable resistor to control the mirrored current by adjusting the control voltage V_{dt}, they enable fine-tuning of the dead time. The capacitor C_{dt} works in tandem with the current mirror to determine the timing characteristics of the dead-time interval.

Voltage translators and **the quenching MOSFET disabling circuit** manage the voltage levels required for proper operation of the quenching and resetting paths. As shown in Figure 3.8, these blocks consist of MOSFET M_{10}, inverters I_2, I_3, I_8, and I_9, resistors $R_1 - R_4$, and capacitors $C_1 - C_2$.

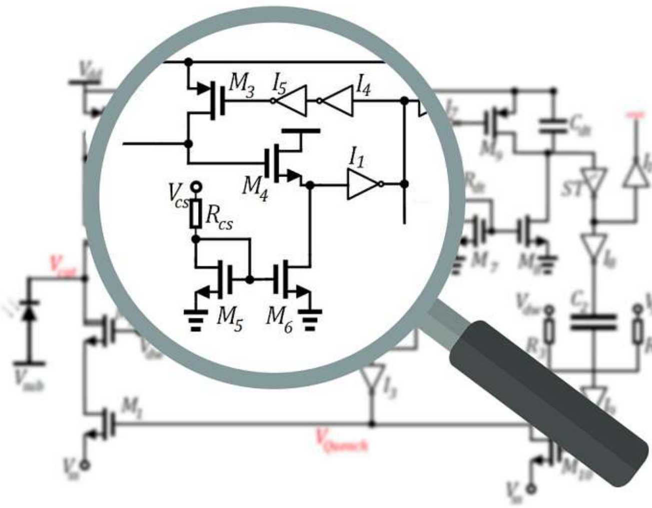


Figure 3.6: sensing & current-cutting stage

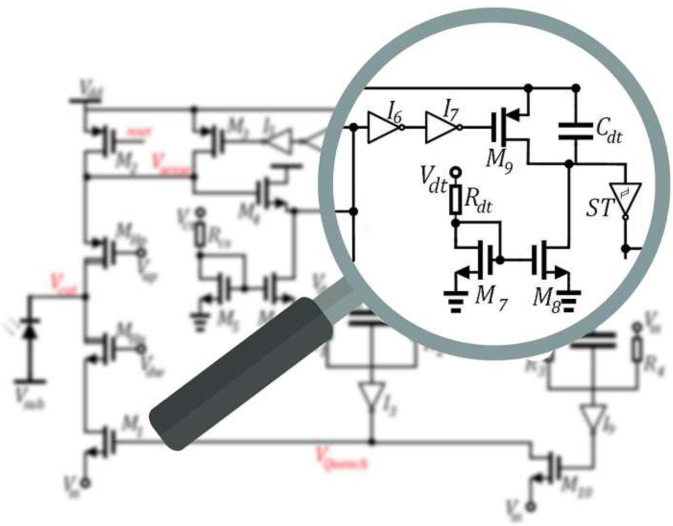


Figure 3.7: dead-time control stage

The primary function of the voltage translators is to align the control signals to the voltage levels needed by the high-voltage MOSFETs in the quenching/resetting switch.

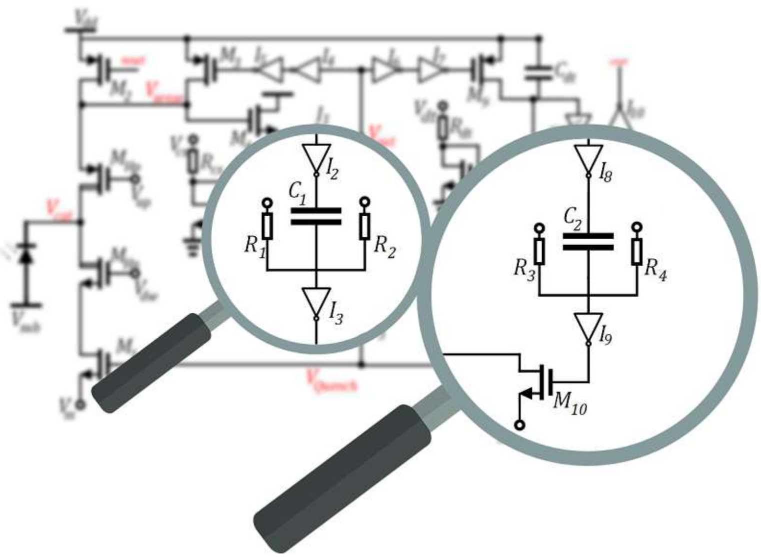


Figure 3.8: Voltage translators & the quenching MOSFET disabling circuit

The quenching MOSFET disabling circuit ensures that the quenching path remains inactive during the reset phase, preventing conflicts between the two operations. Additionally, inverter I_8 shapes the V_{reset} pulse, which drives the resetting MOSFET M_2, ensuring a sharp and well-defined reset signal.

Each block described above is designed to fulfill a specific role in the quenching circuit, from detecting avalanche events to managing dead time and voltage transitions. This modular approach to design ensures that each block can be optimized independently, contributing to the overall performance and reliability of the circuit.

Achieving a balance between detection rate and afterpulsing probability posed a significant design challenge. Reducing dead time to enhance detection rates necessitated precise control of the quenching/resetting mechanism to mitigate the risk of increased afterpulsing. The inclusion of adjustable components, such as R_{dt} and C_{dt} in the Dead-Time Control Stage, provided the necessary flexibility to fine-tune the circuit for optimal performance. This design approach underscores the critical importance of balancing competing requirements to meet the stringent demands of SPAD-based systems.

The design was validated through simulations to verify critical performance metrics, particularly timing. These simulations confirmed the accurate operation of the quenching circuit in maintaining proper timing intervals—a crucial factor in minimizing dead time and reducing the afterpulsing probability. These results demonstrate that the circuit effectively supports reliable single-photon detection, meeting the operational requirements of SPAD. While noise immunity and power efficiency could benefit from further evaluation, the initial timing results suggest a solid foundation for SPAD functionality. Future efforts may explore optimizing power consumption and conducting comprehensive noise analysis to potentially enhance the circuit's performance.

4 Simulation and Results

In this chapter, the performance of the proposed quenching circuit for SPADs is evaluated through a series of simulations conducted in Cadence Virtuoso, using a 0.35-µm BiCMOS process. The simulations are based on an existing SPAD design, with the load SPAD's capacitance varying between 100 fF and 200 fF for all cases. The primary goal is to assess the design's capability to meet the operational requirements of SPAD-based systems, with a particular focus on timing accuracy, dead time, and afterpulsing probability.

The simulations were performed under realistic operating conditions to ensure that the quenching circuit functions reliably within the parameters of the chosen process technology (XH035). Both individual block performance and the behavior of the entire circuit were analyzed to verify the design's robustness and identify potential areas for optimization. This chapter also includes a discussion of the results, highlighting any challenges encountered during the simulation process and the trade-offs involved in achieving the desired performance.

4.1 Timing Optimization and Stability Analysis

To evaluate the performance of the proposed quenching circuit, a series of simulations were conducted to analyze its controllability features. All simulations were based on the same SPAD model reported in [17], which has demonstrated high consistency with measured results. Additionally, the reliability of the design was investigated through Monte Carlo simulations. These evaluations provide critical insights into the robustness and efficiency of the redesigned circuit.

The performance of the quenching circuit is heavily influenced by precise timing characteristics, as these directly affect the SPAD system's operational accuracy and efficiency. Achieving optimal timing required a thorough exploration of various design parameters, with a particular focus on the quenching and reset phases of the circuit. These phases are essential for optimizing dead time, suppressing afterpulsing, and ensuring accurate photon detection. Iterative simulations and design adjustments were implemented to address these challenges, concentrating on modifications to the circuit topology.

A significant optimization strategy involved adjusting the W/L ratios of MOSFETs to fine-tune their switching behavior, ensuring acceptable speed, and balancing trade-offs between timing performance and power consumption. Additionally, the circuit topology underwent critical modifications, most notably replacing the operational amplifier (Op-Amp) used in [8] with a current mirror. This substitution aimed to simplify the design and improve efficiency while maintaining precise control of timing characteristics. Further adjustments included the addition or removal of NOT gates to optimize signal propagation and achieve the desired timing requirements without compromising circuit stability.

To validate the robustness of the proposed design under realistic conditions, simulations were conducted across a range of SPAD load capacitances, varying from 100 fF to 200 fF. These tests assessed the impact of load variations on key performance metrics, including quenching speed, dead time, and reset accuracy. The quenching speed of the circuit was influenced by the W/L ratios of the MOSFETs, particularly those driving the high-voltage transistors. In this design, the high-voltage transistors described in 3.1.2 were specifically selected to enhance speed while maintaining compatibility with the 0.35-µm process. By iteratively adjusting the W/L ratios, the switching behavior of these transistors was optimized to minimize quenching delay. Simulation results revealed an improvement in timing performance, with faster transitions achieved by selecting smaller channel lengths to increase switching speed. At the same time, the transistor widths were carefully balanced to minimize power dissipation and maintain efficiency.

The circuit's stability was also evaluated under varying environmental and operating conditions, such as supply voltage and temperature fluctuations, to ensure its reliability across diverse applications. The results demonstrated that the circuit consistently maintained robust performance under these conditions, highlighting the critical interplay between design parameters and timing performance.

By analyzing the outcomes of these iterative design efforts, valuable insights are offered into the strategies required to achieve high-performance, reliable quenching circuits for SPAD-based systems. As a critical evaluation point, the impact of specific design choices on circuit performance is assessed by examining the voltage at the SPAD cathode. Figure 4.1 presents the voltage response of the circuit to a few incident photons at an excess bias voltage of $V_{ex} = 24V$, providing a detailed view of the circuit's timing behavior and quenching dynamics.

As illustrated in Figure 4.2, the SPAD cathode voltage is initially held at 3.3 V by transistors M_3 and $M_{H}p$, ensuring that the device remains in its ready-to-detect state. Upon the detection of a photon, the avalanche breakdown is triggered, causing the cathode voltage to rapidly drop to V_{SS}. Consequently, the voltage across the SPAD's PN junction rises to the excess bias voltage $V_{ex} = 24V$, indicating that the quenching phase has been activated. During this period, the SPAD remains in a "dead" state, unable to detect additional photons until it is reset. To restore the SPAD to its initial active state, the circuit must drive the cathode voltage back to 3.3 V, allowing the device to resume photon detection. As described in the previous chapter, the dead time can be adjusted using V_{dt} and R_{dt}, the section of the circuit shown in Figure 3.7.

To further analyze the circuit's timing behavior, Figure 4.3 presents the waveform of the SPAD's cathode voltage V_{cat} for different maximum excess bias voltages V_{ex}. These

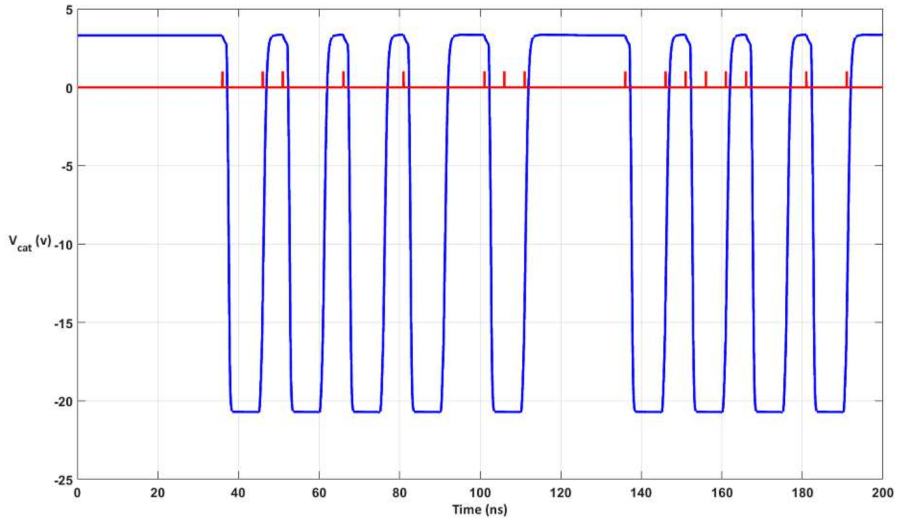


Figure 4.1: Voltage response of the SPAD cathode during photon detection

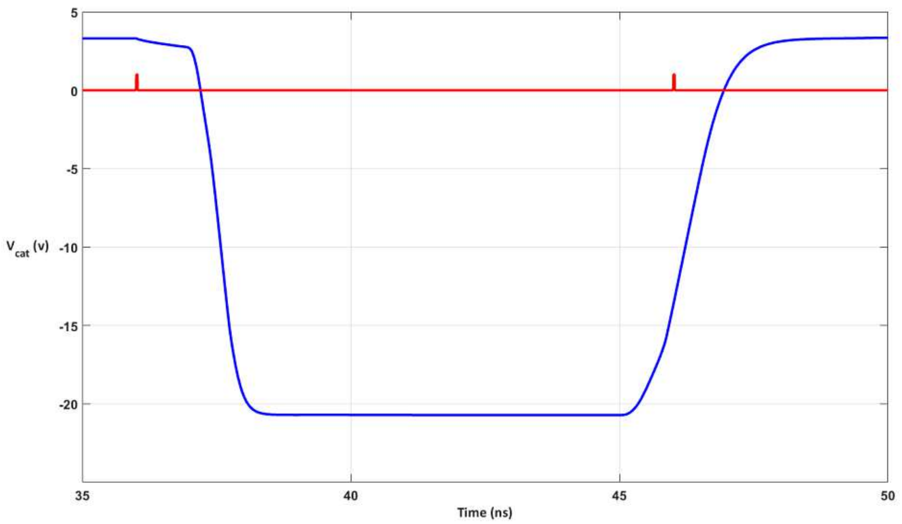


Figure 4.2: Waveform of SPAD's cathode for $V_{ex} = 24V$

waveforms demonstrate the excess bias voltage controllability feature of the proposed ultimate quenching circuit. The excess bias voltage V_{ex} can be varied from 8 V up to 24 V, allowing flexibility in optimizing SPAD performance. The maximum excess bias voltage can be adjusted by simultaneously varying the control voltages V_{ss} and V_{dw}, enabling precise tuning of the quenching dynamics.

The timing of critical circuit nodes is illustrated in Figure 4.4. As observed, the SPAD's current induces a voltage drop at the V_{sense} node Figure 4.4a, which subsequently causes

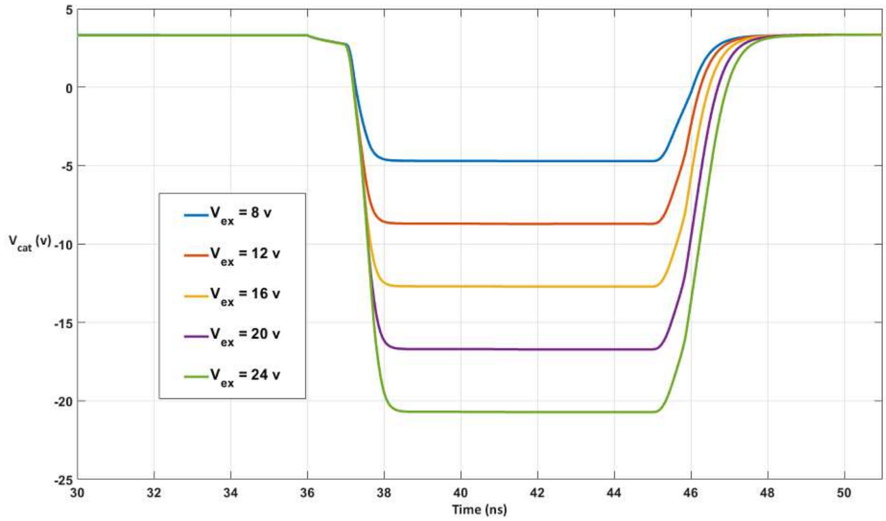


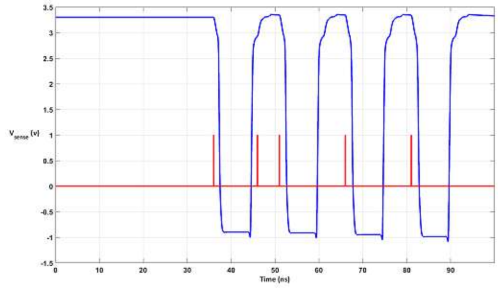
Figure 4.3: Waveform at SPAD's cathode for different excess bias voltages

V_{out}, Figure 4.4b, to transition from 0 to 1. Consequently, the gate voltage of M_3, V_g, rises to V_{dd}, leading to the deactivation of MOSFET M_3. Once the PMOS transistor M_3 is turned off, the current path is interrupted, effectively preventing further charge flow into the SPAD.

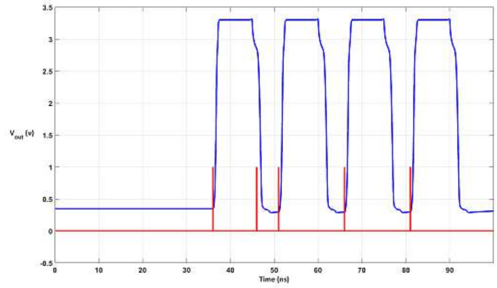
During this phase, passive quenching takes place, marking the interval between the absorption of a photon and the point at which MOSFET M_3 is turned off, thereby interrupting the SPAD's current flow. This quenching period is a critical aspect of the circuit's operation, as it directly influences the detector's ability to recover efficiently for subsequent photon detections. A well-controlled passive quenching duration helps suppress afterpulsing effects, which can introduce spurious detection events and compromise the accuracy of the SPAD system. By carefully optimizing this phase, the proposed quenching circuit achieves a balance between fast recovery and noise reduction, ensuring both high detection efficiency and improved reliability in photon-counting applications.

To suspend the SPAD's current, the voltage V_{out} is translated from the 0 V - 3.3 V domain to the domain defined by V_{dw} and V_{ss} using a voltage translator circuit. This circuit consists of R_1, R_2, C_1, and I_3, as illustrated in Figure 3.8. Within this translated voltage domain, the corresponding V_{quench} signal (Figure 4.4c) is generated to control the quenching MOSFET M_1. After a brief delay, M_1 switches on, initiating the active quenching phase, during which the SPAD's cathode voltage is rapidly pulled down to V_{ss}. This controlled discharge ensures a fast and efficient quenching mechanism, minimizing dead time and enabling the SPAD to quickly recover for subsequent photon detection events.

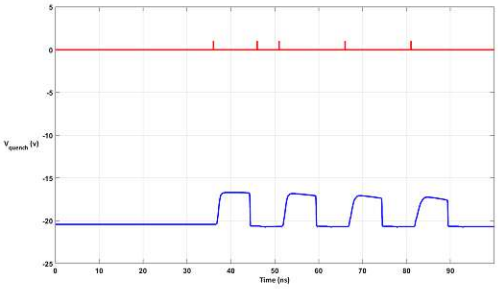
At the same time, when V_{quench} is generated, MOSFET M_9 is switched off, causing V_{ct} to decrease. Once V_{ct} falls below the threshold level of the Schmitt trigger, it outputs a logic "1". This output is changed to the "0" by inverter I_8 and translated from the 0 V / 3.3 V



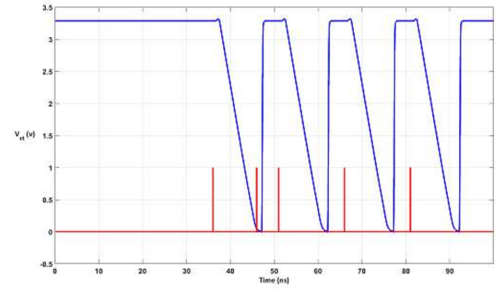
(a) V_{sense}



(b) V_{out}



(c) V_{quench}



(d) V_{ct}

Figure 4.4: The timing of critical circuit nodes

domain to the V_{dw} and V_{ss} domain through the voltage translator circuit comprising R_3, R_4, C_2, and I_9. As a result, the V_{off} signal is produced, which activates the disabling MOSFET M_{off}, pulling the gate of MOSFET M_1 to V_{SS}, thereby turning off M_1 and completing the quenching phase. The trend of V_{ct} voltage changes is shown in Figure 4.4d, where the behavior of the voltage throughout the entire process, from the initial decrease to the point where the quenching phase is terminated, is demonstrated.

During this period, when the voltage V_{off} is generated, the resetting voltage V_{reset} is also produced, activating the resetting MOSFET M_2. Once the PMOS M_2 turns on, the SPAD's cathode is restored to V_{dd} (3.3 V), completing the resetting phase. At the end of this phase, the SPAD is fully rearmed and ready to detect new photon events. Throughout the resetting phase, MOSFETs M_3 and M_1 remain in the off state, ensuring that the quenching mechanism does not interfere with the reset operation. As a result, even if a photon arrives during this interval, the quenching circuit does not respond, preventing any disruption to the reset process. This mechanism is crucial for maintaining the stability and reliability of the quenching circuit, ensuring consistent and predictable operation. By analyzing these waveforms, the timing characteristics of the reset operation can be further evaluated, providing insight into its efficiency and effectiveness.

As previously discussed, dead time is a critical parameter in SPAD-based systems, as it defines the minimum interval during which the detector remains inactive after detecting a photon event. This enforced inactivity prevents premature reactivation of the SPAD and mitigates afterpulsing, a phenomenon that can introduce false detections and degrade system performance. Consequently, the duration of dead time plays a crucial role in balancing the trade-off between detection rate and signal integrity. A shorter dead time increases the detection rate but heightens the risk of afterpulsing, whereas a longer dead time effectively suppresses afterpulsing at the expense of a reduced overall count rate.

In the proposed quenching circuit, figure 3.4, the Dead-Time Control Stage precisely regulates the dead time, ensuring an optimal delay before rearming the SPAD. As detailed in Chapter 3, the circuit section illustrated in Figure 3.7 serves as the primary component responsible for dead-time control. By adjusting the resistor R_{dt}, the duration of the dead time can be fine-tuned to achieve the desired balance between detection efficiency and noise suppression. Figure 4.5 illustrates the transient behavior of the cathode voltage for various dead-time settings, demonstrating the impact of R_{dt} on the overall system response.

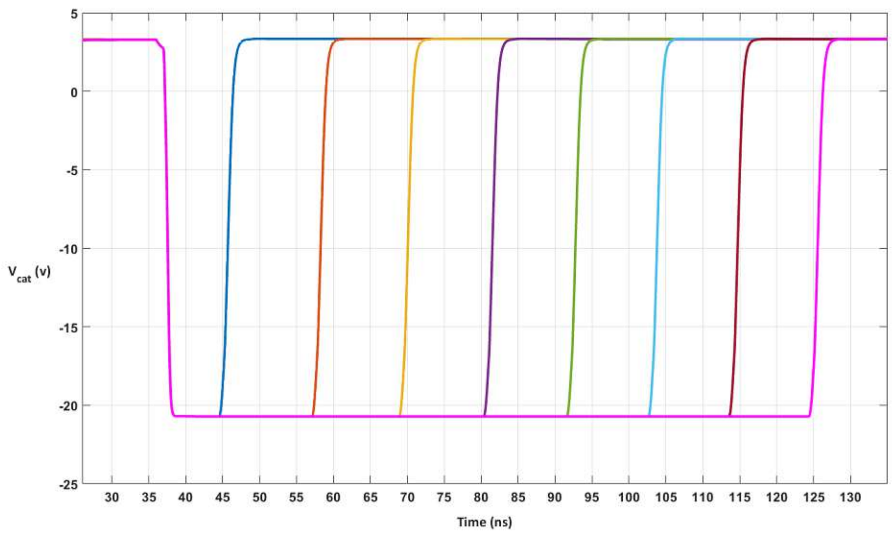


Figure 4.5: Cathode voltage transient for different dead-time settings with varying R_{dt}

The dead time in the proposed circuit is primarily governed by the controlled discharge of capacitor C_{dt} through resistor R_{dt}, forming a time constant $\tau = R_{dt}C_{dt}$. Additionally, the dead time can be adjusted by modifying the control voltage V_{dt}, which sets the current in the current mirror, thereby influencing the discharge rate of C_{dt}. The values of these components play a fundamental role in defining the overall duration of the dead time by determining the operating period of the Schmitt trigger and, consequently, the duration for which the SPAD remains inactive before the reset phase begins. Once this delay has elapsed, as described earlier, the reactivation of transistors M_{10} and M_2 restores the SPAD's cathode voltage, preparing it for subsequent photon detection. Figure 4.5 presents the simulated transient response of the cathode voltage for varying R_{dt} values, illustrating how modifications to both R_{dt} and V_{dt} influence system behavior and timing performance.

4.1.1 Monte Carlo Analysis

While the transient response of the SPAD's cathode voltage under nominal conditions provides valuable insight into the timing characteristics of the quenching and reset phases, real-world variations must also be considered. Process, voltage, and temperature (PVT) fluctuations inherently affect the behavior of semiconductor circuits, potentially introducing deviations in key performance parameters. These variations can influence the stability and consistency of the cathode voltage response, which, in turn, may impact the overall performance and reliability of the quenching circuit. Therefore, a comprehensive statistical evaluation is essential to ensure that the design remains robust under practical operating conditions.

To quantify the impact of fabrication-induced variations, a Monte Carlo analysis is conducted, capturing statistical fluctuations in the cathode voltage transient across multiple iterations. This simulation accounts for key process variations, including threshold voltage shifts, transistor mismatches, and other parametric deviations that affect circuit dynamics. By evaluating these variations, the analysis provides a deeper understanding of the circuit's sensitivity to manufacturing tolerances and its ability to maintain stable operation across different fabrication runs. The results indicated that the cathode voltage exhibits a consistent and predictable trend, demonstrating that the circuit remains resilient against process-induced perturbations.

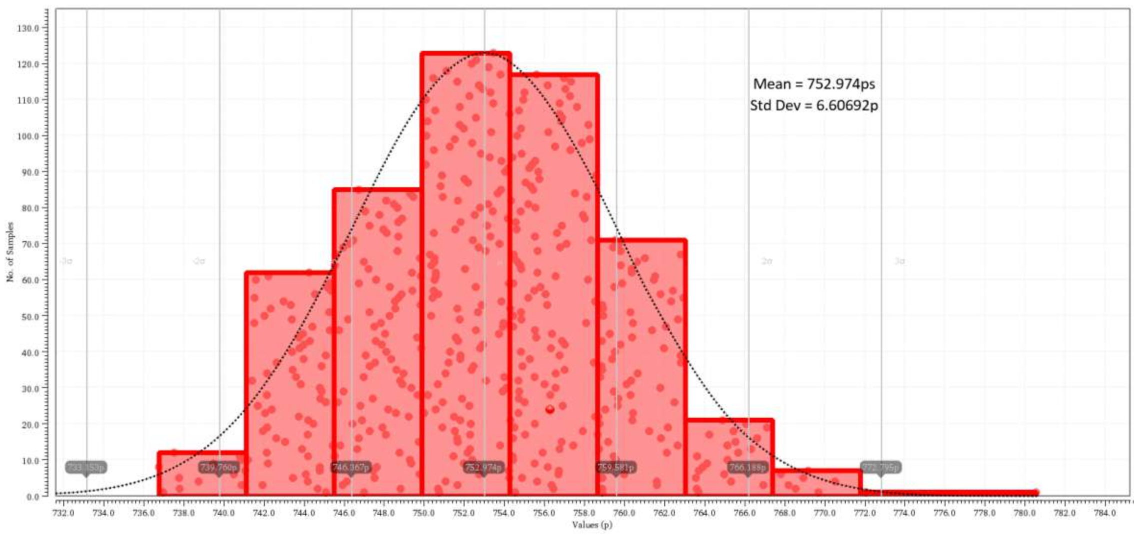


Figure 4.6: Monte Carlo simulation for falling time of the cathode voltage during the passive quenching phase

Figure 4.6 presents the Monte Carlo analysis of the falling time of the cathode voltage during the passive quenching phase, immediately preceding the onset of the quenching operation. The statistical distribution of the results highlights the range of voltage transitions observed under varying process conditions, offering insights into the design's reliability.

The findings confirm that despite inherent variations in semiconductor manufacturing, the proposed circuit maintains stable and repeatable performance. This robustness is critical in SPAD-based applications, where precise timing and reliable operation are paramount. To ensure a comprehensive evaluation, the Monte Carlo analysis was conducted over 500 iterations, accounting for both process variations and device mismatches.

The results further validate the robustness of the proposed quenching circuit, as the observed variations remain within an acceptable range, ensuring consistent operation across different fabrication runs. The statistical distribution of cathode voltage transitions demonstrates that the circuit effectively mitigates process-induced variations, reinforcing its suitability for practical SPAD implementations. Given the importance of maintaining predictable quenching behavior in photon detection systems, these findings confirm that the design is well-suited for applications requiring high reliability and performance stability.

4.2 Specification of Operating Conditions

The proper selection of operating conditions is critical for ensuring optimal circuit performance. This section defines the voltage ranges and conditions under which the quencher circuit functions reliably, emphasizing key parameters that influence its behavior.

The circuit operates with a primary supply voltage, denoted as V_{DD}, along with V_{SS}, V_{sub}, and a ground reference set to 0 V. The nominal value of V_{DD} is 3.3 V, while V_{SS} is adjustable within a specified range of -4.7 V to -20.7 V. Variations in these supply voltages influence timing characteristics and power consumption, which may impact quenching performance. Therefore, precise regulation of these voltages is crucial to ensure stable and reliable operation.

In addition, the substrate voltage V_{sub} plays a critical role in the circuit's functionality. Properly biasing V_{sub} helps reduce noise, improve signal integrity, and enhance the overall performance of the integrated circuit (IC), ensuring reliable operation under varying conditions. Moreover, in this circuit, V_{sub} is also used to bias the anode of the SPAD, providing the necessary conditions for Geiger-mode operation, where avalanche multiplication occurs. Consequently, maintaining an appropriate substrate voltage is essential not only for the correct functionality of the SPAD but also for ensuring the stability and efficiency of the quenching circuit.

Two key control voltages, V_{up} and V_{dw}, are applied to the gates of the high-voltage transistors M_Hp and M_Hn. These voltages determine the switching characteristics of the transistors and must be carefully selected to balance switching speed and reliability. As illustrated in Figure 3.4, V_{dw} also serves as the high-level voltage in the voltage translator circuit, which controls the quenching MOSFET. Therefore, V_{dw} must be precisely chosen to ensure that transistors M_1 and M_{10} switch on and off at the appropriate times, enabling proper quenching operation.

These control voltages must be carefully set to ensure that the quenching transistor activates as quickly as possible to suppress post-pulse effects while preventing unintended self-triggering. If improperly configured, the circuit may enter an unstable oscillatory state, continuously switching between quench and reset phases, thereby degrading performance. One of the key advantages of utilizing V_{up} and V_{dw} is the ability to fine-tune the circuit by adjusting these voltages as needed. This flexibility allows for optimization in response to input variations, ensuring consistently optimal performance.

The voltage V_{up} is set to $V_{DD} - 5$ V to ensure that the upper transistor operates within its optimal region, thereby preventing excessive leakage and minimizing transition delays. Similarly, V_{dw} is set to $V_{SS} + 4$ V to ensure proper turn-off characteristics and reduce the likelihood of unintended conduction states. However, as previously mentioned, these voltages can be adjusted under different operating conditions to fine-tune the circuit's performance and optimize its response.

Another critical voltage in the circuit is V_{dt}, which is applied to the current mirror to regulate the dead time during the quenching process. Proper selection of V_{dt} is essential to achieving an optimal balance between fast response times and circuit stability. A lower V_{dt} may introduce excessive delays, reducing the overall efficiency of the quenching mechanism, whereas a higher V_{dt} could result in insufficient dead time, potentially leading to premature re-triggering of the SPAD. The optimal value of V_{dt} is determined through empirical tuning to ensure a stable and reliable quenching response.

The drive voltage V_{cs} is a critical parameter applied to the second current mirror, as shown in Figure 3.6. It must be carefully adjusted to ensure that the drain of M_6 and the source of M_4, which are connected to the input of the inverter, remain as close as possible to the threshold voltage of I_1. This precise tuning is essential for achieving fast and reliable switching. If V_{cs} is set too low, the circuit may exhibit sluggish behavior, adversely affecting the quenching speed. Conversely, if V_{cs} is too high, it can lead to excessive leakage currents, reducing overall efficiency. Therefore, carefully calibrating V_{cs} is crucial to minimizing delays and ensuring optimal timing control within the quencher circuit.

It is important to reiterate that the simulations were conducted based on an existing SPAD design, with the load SPAD capacitance varying between 100 fF and 200 fF. This range accounts for process variations and different operating conditions, ensuring a realistic evaluation of circuit performance. Variations in load capacitance can impact the circuit's response time and influence quenching efficiency. Therefore, the selected capacitance values were chosen to ensure that the circuit maintains reliable operation across the expected variations in SPAD parameters.

By carefully defining these operating conditions, the quencher circuit is optimized to function reliably across various scenarios. Proper voltage selection ensures stable quenching performance, minimizes unwanted oscillations, and enhances the circuit's response time. These considerations are crucial in designing high-voltage SPAD quencher circuits, where precise control over switching behavior directly impacts detection efficiency and overall system reliability.

4.3 Layout

The layout of the quencher circuit for SPADs is crucial for ensuring its performance, stability, and overall functionality, especially within a high-voltage CMOS process. This section presents the layout process used to address process variations and enhance the reliability of the circuit. The design focuses on carefully placing and matching key components, such as high-voltage transistors, while also considering the arrangement of functional blocks to ensure efficient signal integrity. The layout was optimized to balance compactness with the necessary electrical performance, ensuring that all components of the quencher circuit are positioned to meet the required specifications.

This subsection provides a general overview of the layout, focusing on the final implementation of the quencher circuit rather than delving into the intricacies of specific layout techniques. Given the scope of this work, detailed discussions on layer configurations, advanced layout optimization, and process-specific considerations are not included. Instead, the primary emphasis is on presenting a clear representation of the circuit layout, including the placement of key components and the bonding pads. The figures included in this section serve to illustrate the final layout design, offering a comprehensive view of the circuit's physical realization and the resulting fabricated IC.

In the layout design of the presented quencher circuit, as shown in Figure 4.7, the components were placed as close together as possible to minimize metal lengths. This strategy helps reduce parasitic capacitance and inductance, thereby improving signal integrity and enabling faster signal propagation. Although the circuit's power consumption is relatively low, shorter interconnects further reduce power consumption, which is advantageous for low-power designs. Additionally, minimizing metal interconnect lengths helps mitigate electromigration concerns, enhancing the overall reliability of the integrated circuit. While the process technology supports the use of four metal layers, only three were employed in the layout to avoid unnecessary complexity and to minimize potential parasitic effects. Higher metal layers, while offering lower resistance, can introduce parasitic capacitance and inductance that must be carefully managed to maintain optimal circuit performance. The layout in Figure 4.7 shows the dimensions of the circuit, with a size of 150 µm by 180 µm.

In the final design, Metal 4 was used to connect the bonding pads to the relevant components within the circuit layout. Special attention was given to ensuring sufficient space for the SPAD diode, which was integrated as an internal chip. The placement of the bonding pads was carefully optimized to enable proper interfacing with external connections, ensuring the circuit's functionality once packaged. Figure 4.8 presents an overview of the pad placements, the output driver, the circuit components, and the integrated SPAD diode, highlighting the layout's configuration and how the external connections are organized for optimal performance.

Following the completion of the design and manufacturing process, the fabricated integrated circuit (IC) was received from the foundry. Figure 4.9 presents a microscope image of the final chip, illustrating the realized layout, including the bonding pads and key circuit components. The physical dimensions of the chip align with the design specifications, and

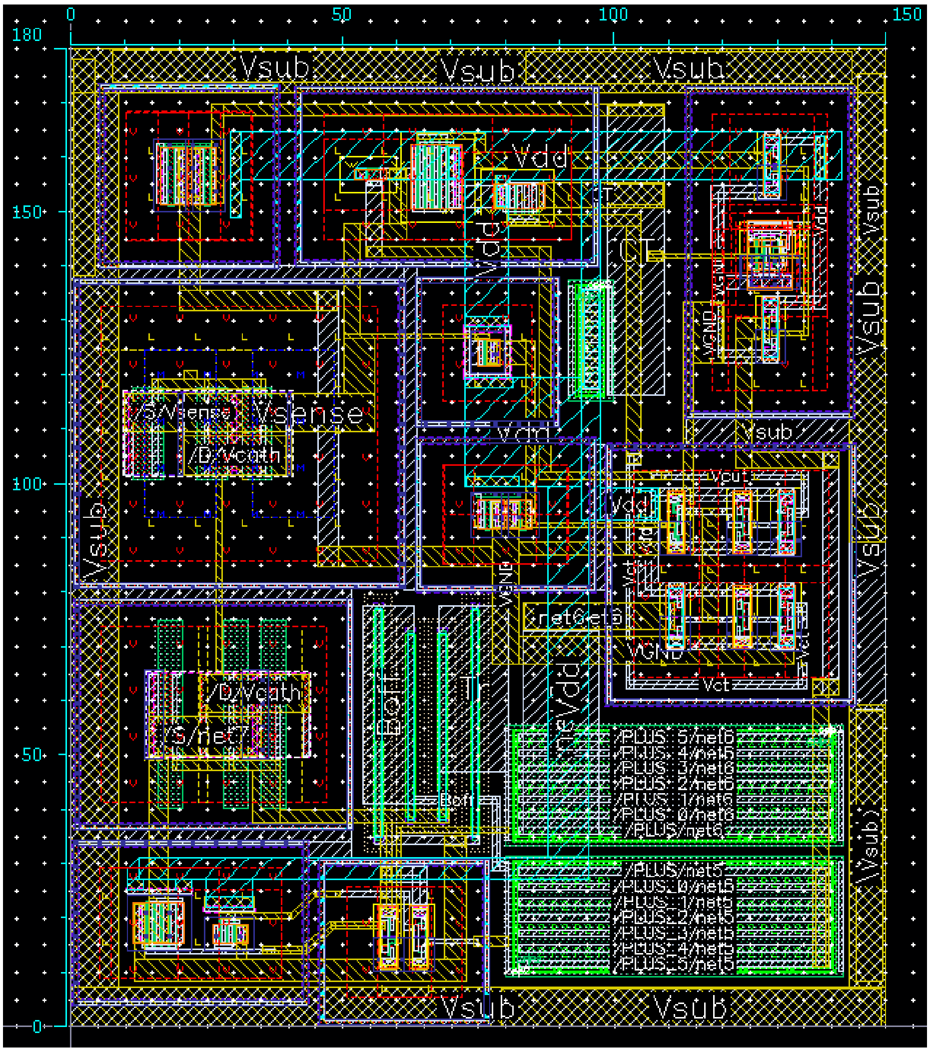


Figure 4.7: Layout of the circuit 3.4

initial visual inspection confirms the successful implementation of the layout. This image provides a clear representation of the fabricated IC, offering insight into the final structure and how the design translates into a manufactured device.

This section provided a high-level overview of the layout, focusing on the overall structure and key design considerations. To ensure the functionality and performance of the designed circuit, verification of the layout was conducted through post-layout simulations, which are discussed in detail in the subsequent sections.

4.4 Post-layout Simulation Results

Post-layout simulations are essential for validating the performance of the quencher circuit after the physical design process. While schematic-level simulations provide an idealized

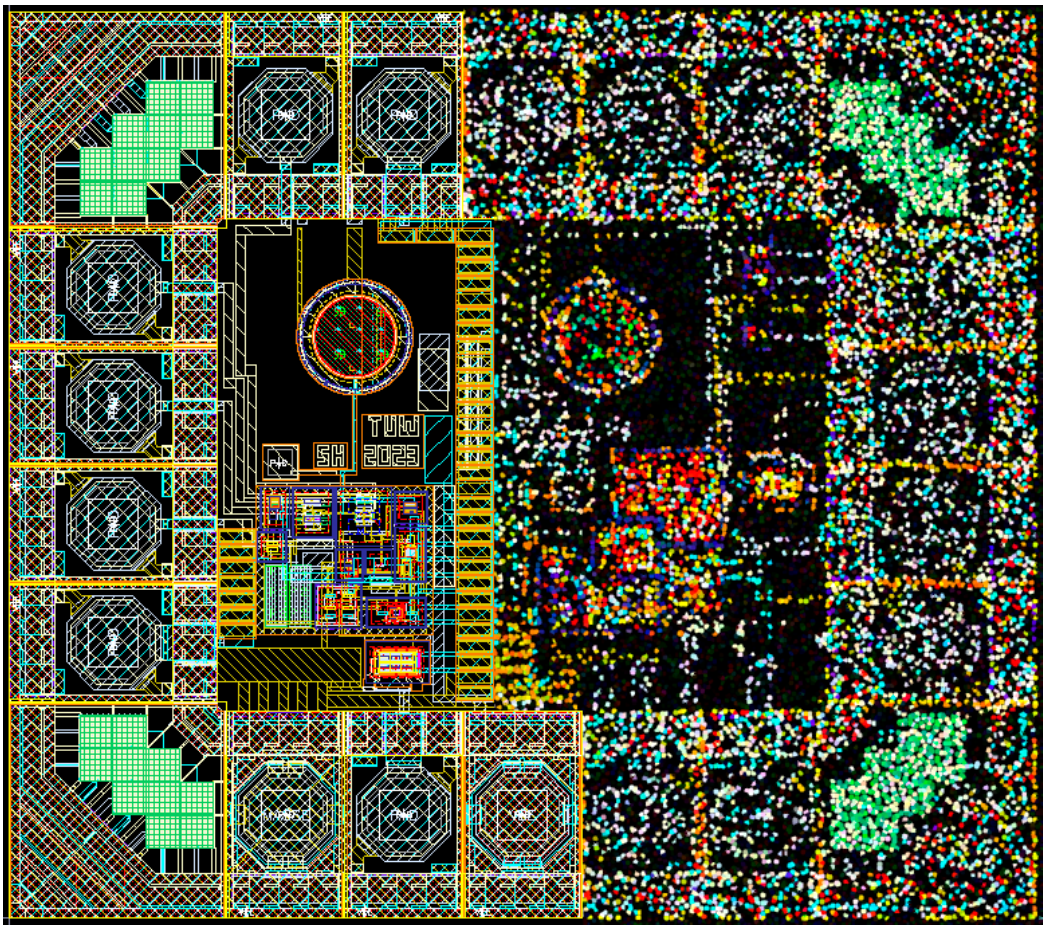


Figure 4.8: Layout of Chip

representation of circuit behavior, they do not account for the non-idealities introduced during layout. The physical implementation of the circuit introduces parasitic resistance, capacitance, and inductance due to metal interconnects, device placement, and routing constraints. These parasitic effects can lead to signal degradation, increased propagation delays, and potential mismatches between expected and actual circuit behavior. Without accounting for these effects, the designed circuit may not function as intended when fabricated. Therefore, post-layout simulations are performed to ensure that the circuit meets its intended performance specifications after layout-induced modifications.

This section focuses on analyzing the post-layout transient response of the quencher circuit and comparing it with the schematic-level results. Special attention is given to the impact of layout-induced parasitics on timing delays and voltage levels, particularly the voltage drop at the cathode of the SPAD during the quenching process. The findings provide insights into how the physical realization of the circuit influences its dynamic behavior and whether any deviations from the expected performance occur due to layout effects.

To evaluate the dynamic performance of the quencher circuit after layout implementation,

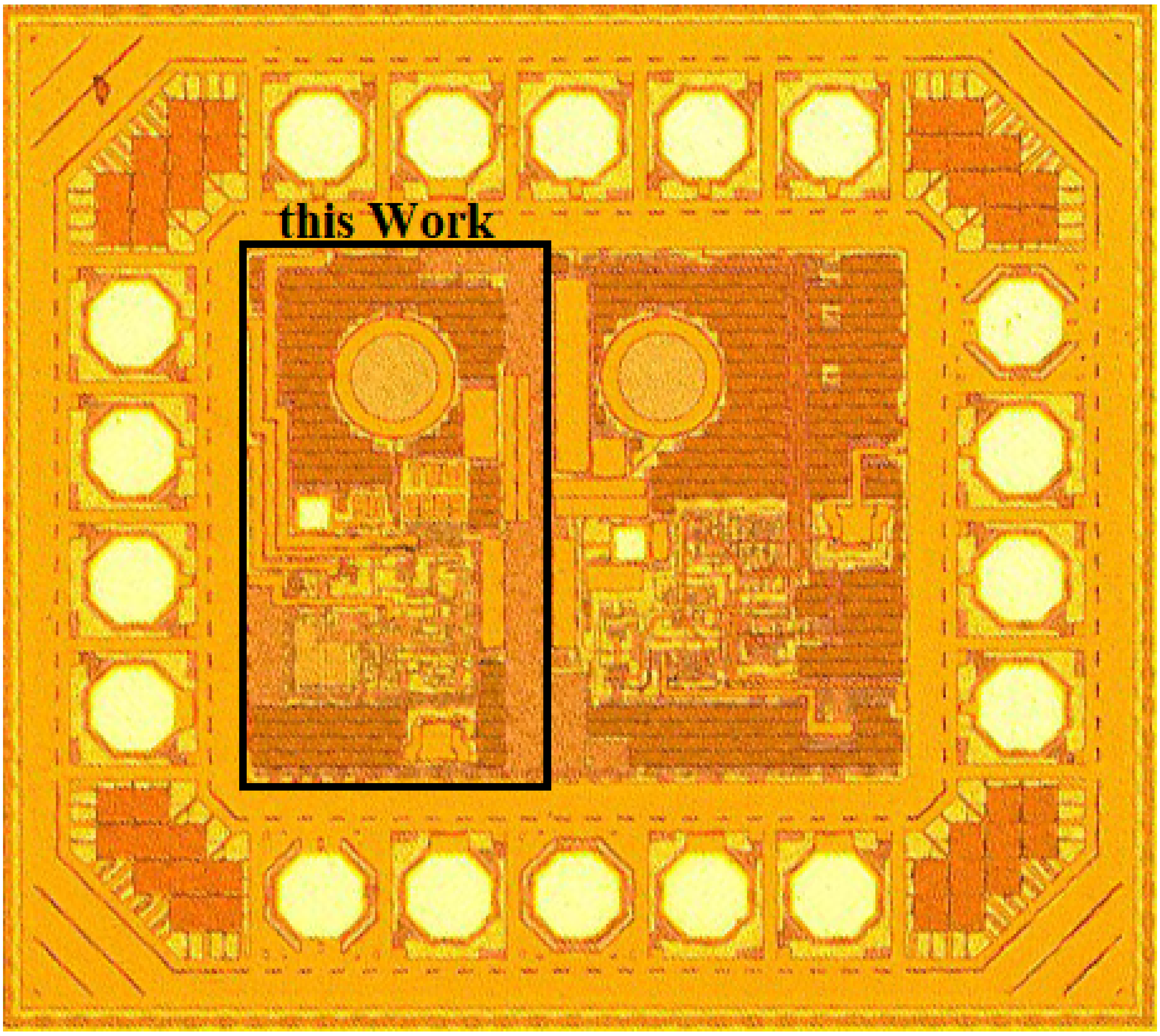


Figure 4.9: Chip

transient simulations were conducted and compared with schematic-level results. The primary objective was to assess whether the circuit maintained its expected response despite the introduction of layout-induced parasitics.

Figure 4.10 presents the transient response of the quencher circuit obtained from post-layout simulations. As observed, the circuit continues to function correctly, demonstrating the expected behavior during the quenching process. The cathode voltage of the SPAD exhibits a distinct transition through the passive and active quenching stages, similar to the schematic-level simulations. The response to an incident photon remains well-defined, ensuring that the circuit effectively quenches the avalanche event and restores the SPAD to its ready state.

While the overall transient response closely matches the schematic results, a minor increase in signal fall time was observed. This is attributed to the presence of parasitic resistance and capacitance introduced during layout, which slightly affects the switching

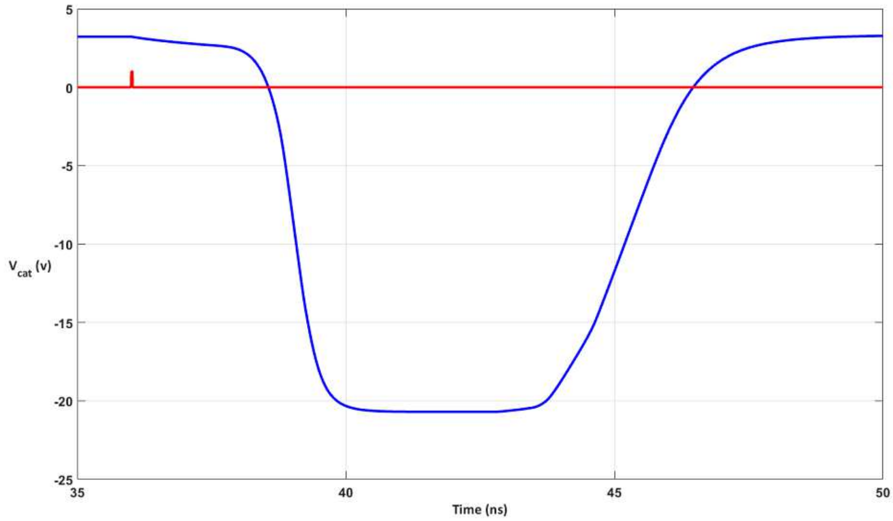


Figure 4.10: Cathode voltage transient in post-layout simulation

speed. However, the delay remains within acceptable limits, ensuring that the circuit meets its intended timing requirements.

The introduction of parasitic resistance and capacitance in the layout can influence the circuit's switching behavior by affecting signal propagation and timing. In particular, these parasitic elements can introduce small delays in the quenching process and slightly modify voltage levels at critical nodes. However, observed, the transition occurs as expected, confirming that the quenching mechanism remains effective even after layout implementation. The impact of parasitic effects on timing is imperceptible, and the voltage levels remain consistent with the schematic-level results. These findings indicate that the layout-induced variations do not significantly alter the fundamental operation of the circuit.

The post-layout simulations confirm that the circuit performs as intended, with any observed deviations well within acceptable design margins. These results validate the robustness of the quencher circuit against layout-induced parasitic effects, ensuring that the final fabricated implementation will function as expected.

5 Conclusion and Outlook

This work has successfully presented the design and analysis of a quencher circuit for Single-Photon Avalanche Diodes (SPADs) fabricated in a 0.35-µm high-voltage CMOS process. The proposed circuit was developed to efficiently quench the avalanche current while ensuring fast reset and stable operation. By thoroughly exploring the available technology options, carefully selecting high-voltage transistors, and optimizing key performance parameters, the quencher circuit demonstrates reliable functionality with significantly improved response times. The incorporation of high-voltage transistors enables the circuit to operate at elevated voltage levels, leading to enhanced Photon Detection Probability rates and overall improved efficiency.

Extensive simulations were conducted to validate the design, covering both schematic-level and post-layout analyses. Timing optimization techniques were applied to minimize delays and enhance overall circuit performance. Monte Carlo analysis confirmed the robustness of the design under process variations and mismatch, ensuring stable quenching and reset behavior across different operating conditions. Additionally, post-layout simulations accounted for parasitic effects, providing insights into real-world performance and verifying that the circuit meets the required specifications.

Compared to conventional quenching techniques, the proposed circuit offers significant advantages, including reduced passive quenching time, substantially lower power consumption, and improved timing stability. These improvements contribute to enhanced SPAD performance, making the design well-suited for applications requiring high-speed and low-noise photon detection.

It is important to note that the results presented for the designed receiver are based on post-layout simulations and have not yet been fully confirmed by measurements. To bridge this gap, we are currently conducting measurement tests to validate the circuit's performance under real-world conditions. With the help of several voltage sources, as shown in Figure 5.1, the conditions mentioned in the operating conditions specification section 4.2 are attempted to be met. The board will be placed in the relevant enclosure, and the results will be checked using a picoprobe and an oscilloscope. The next step involves analyzing the measured data and comparing it with simulation results to further refine the design and ensure its practical feasibility. The insights gained from these measurements will be crucial in confirming the accuracy of the simulated outcomes and identifying any potential improvements.

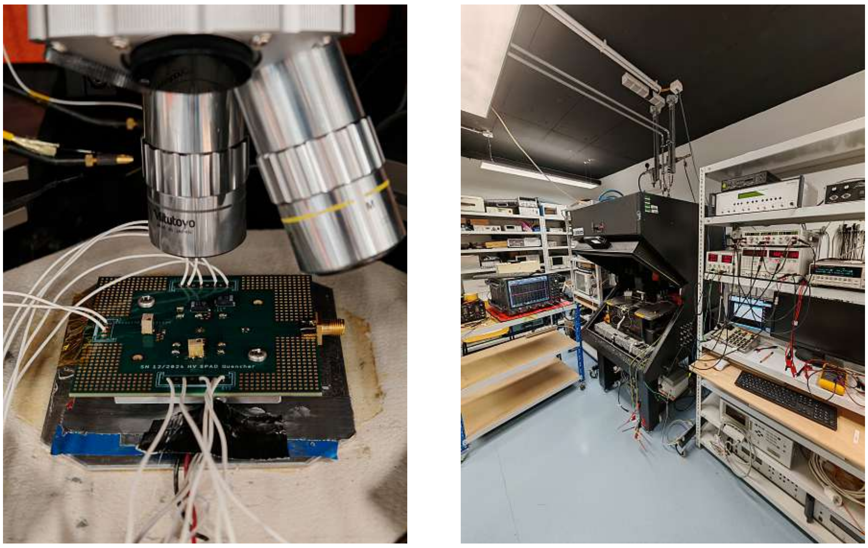


Figure 5.1: Overview of the experimental setup for measurement tests

The results achieved in this work provide a solid foundation for future advancements in SPAD-based systems and related circuit designs, paving the way for more efficient and reliable photon detection technologies.

While this work successfully presents a well-optimized quencher circuit for SPADs in a 0.35-µm high-voltage CMOS process, there are several avenues for future enhancements that could further improve its performance and expand its applicability.

The current design is based on the 0.35-µm high-voltage CMOS process, which is suitable for the specified requirements. However, exploring advanced process technologies such as 65-nm or 90-nm CMOS could provide opportunities to increase speed and improve scalability. These advanced nodes would also allow the integration of additional circuit features, such as on-chip voltage regulation, which could enhance overall system performance and stability.

Future work could focus on improving key performance metrics, such as quenching time and recovery time, through the refinement of circuit parameters and topologies. The integration of active quenching techniques could also be considered to improve timing stability. Additionally, optimizing the transistor sizing and layout for lower parasitic elements could lead to further improvements in the response time and noise reduction.

A natural extension of this work could involve integrating the quencher circuit with other crucial SPAD-related circuits, such as a photon counter or a timing discriminator, on the same chip. This would enable the development of a complete photon detection system in a single-chip solution, improving system efficiency and reducing the overall footprint. Additionally, integrating the quencher circuit with digital circuits for real-time signal processing could enable faster data acquisition and more advanced photon detection applications.

The proposed quencher circuit has significant potential for various applications, particularly in fields requiring high-speed and low-noise photon detection, such as in optical communication, quantum computing, and medical imaging technologies. Its ability to improve SPAD performance could contribute to the development of next-generation sensors used in LiDAR systems, fluorescence-based biosensors, and other time-of-flight measurement systems.

Furthermore, the insights gained from this research can serve as a foundation for future studies in the design and optimization of SPAD circuits, especially in the context of large-scale integration and system-level performance optimization. Future research could explore the use of emerging materials (such as graphene or III-V compounds) to further enhance the performance of SPAD-based systems.

Bibliography

[1] Bing Wang, Shipeng Zhong, Ping Xu, and Han Zhang. Recent development and advances in photodetectors based on two-dimensional topological insulators. *J. Mater. Chem. C*, 8:15526–15574, 2020. 2

[2] Tianjun Ma, Ning Xue, Abdul Muhammad, Gang Fang, Jinyao Yan, Rongkun Chen, Jianhai Sun, and Xuguang Sun. Recent progress in photodetectors: From materials to structures and applications. *Micromachines*, 15(10), 2024. 2

[3] Xuanyu Qian, Wei Jiang, Ahmed Elsharabasy, and M. Jamal Deen. Modeling for single-photon avalanche diodes: State-of-the-art and research challenges. *Sensors*, 23(7), 2023. 4

[4] Michael Hofbauer, Kerstin Schneider-Hornstein, and Horst Zimmermann. *Single-photon Detection for Data Communication and Quantum Systems*. 2053-2563. IOP Publishing, 2021. 5

[5] Aymeric Panglosse, Philippe Martin-Gonthier, Olivier Marcelot, Cédric Virmontois, Olivier Saint-Pé, and Pierre Magnan. Dark count rate modeling in single-photon avalanche diodes. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 67(5):1507–1515, 2020. 7

[6] Xudong Jiang, Mark A. Itzler, Rafael Ben-Michael, and Krystyna Slomkowski. Ingaasp–inp avalanche photodiodes for single photon detection. *IEEE Journal of Selected Topics in Quantum Electronics*, 13(4):895–905, 2007. 7

[7] Alija Dervić. *Circuits for Optical Receivers Near the Quantum Limit*. PhD thesis, Technische Universität Wien, 2021. 11, 12, 13, 14

[8] Alija Dervić, Saman Kohneh Poushi, and Horst Zimmermann. Fully-integrated spad active quenching/resetting circuit in high-voltage 0.35- m cmos for reaching pdp saturation at 650 nm. In *2021 24th International Symposium on Design and Diagnostics of Electronic Circuits Systems (DDECS)*, pages 1–5, 2021. 16, 17, 22, 34

[9] Giulia Acconcia, Ivan Rech, Angelo Gulinatti, and Massimo Ghioni. High-voltage integrated active quenching circuit for single photon count rate up to 80 mcounts/s. *Optics Express*, 24:17819, 07 2016. 20

[10] Z. Xiao, D. Pantic, and R. S. Popovic. A new single photon avalanche diode in cmos high-voltage technology. In *TRANSDUCERS 2007 - 2007 International Solid-State Sensors, Actuators and Microsystems Conference*, pages 1365–1368, 2007. 21

[11] Alija Dervić, Bernhard Steindl, Michael Hofbauer, and H. Zimmermann. High-voltage active quenching and resetting circuit for spads in 0.35 m cmos for raising the photon detection probability. *Optical Engineering*, 58:1, 04 2019. 21

[12] X-FAB. *X-FAB 0.35, 0.18, 0.13, 0.11m XMB10 MEMS Prototyping and Volume Production*. X-FAB, 2024. Available through EUROPRACTICE. 24

[13] X-FAB. X-fab europractice process portfolio 2022, 2022. 24

[14] X-FAB. X-fab process portfolio 2019, 2019. 24

[15] S. S. Kohneh Poushi, H. Mahmoudi, B. Steindl, M. Hofbauer, and Horst Zimmermann. Comprehensive modeling of photon detection probability in cmos-based spads. In *2020 IEEE SENSORS*, pages 1–4, 2020. 25

[16] S. S. Kohneh Poushi, H. Mahmoudi, M. Hofbauer, A. Dervic, and H. Zimmermann. Photodetection characterization of spads fabricated in 0.35µm pin photodiode and high voltage cmos technologies. In *2022 45th Jubilee International Convention on Information, Communication and Electronic Technology (MIPRO)*, pages 230–234, 2022. 26

[17] Bernhard Steindl, Michael Hofbauer, Kerstin Schneider-Hornstein, Paul Brandl, and Horst Zimmermann. Single-photon avalanche photodiode based fiber optic receiver for up to 200 mb/s. *IEEE Journal of Selected Topics in Quantum Electronics*, 24:1–8, 2018. 33

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