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RESEARCH ARTICLE

Low-Noise Modified-RGC Transimpedance Amplifier With Bandwidth Enhancement Using an Intrinsic Negative-RC Network

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ABSTRACT This paper presents a dual feedback transimpedance amplifier (TIA) with a modified regulated-cascode (RGC) topology that employs a negative resistance-capacitance (NRC) network to enhance both bandwidth and noise performance. By combining a negative resistance-capacitance network with transconductance boosting (g_m-boosting), the proposed topology provides greater flexibility in circuit design, improving the performance of the circuit, in relation to both input and output nodes, compared to conventional RGC topologies. This increased design flexibility enables optimal input impedance with lower power consumption, particularly in the presence of large photodiode (PD) capacitance, while avoiding output node headroom limitations. Additionally, the use of a negative capacitance at the output node allows for increment of the output resistance (gain) without concerns about headroom limitations or load capacitance constraints, resulting in a significant noise reduction and bandwidth enhancement. To demonstrate the effectiveness of the proposed circuit techniques, the TIA topology is fabricated in 0.35 μm CMOS technology. Measurement results show 69 dBΩ transimpedance gain, 1.7 GHz 3-dB bandwidth, and 6 pA/$\sqrt{\text{Hz}}$ input referred noise current spectral density. The circuit power consumption and area are 7.4 mW and of 0.01 mm^2, respectively.

INDEX TERMS Transimpedance amplifier (TIA), negative resistance-capacitance (NRC) network, photodiode (PD), modified dual-feedback regulated cascode (MDFRGC) topology, optical receiver.

I. INTRODUCTION

The demand for integrated circuit (IC) design in optical systems is driven by various applications such as high-speed data centers, visible light communication (VLC), wireless optics, sensors, as well as light detection and ranging (LiDAR). In order to meet these demands, expensive SiGe BiCMOS technologies are commonly used for high-speed applications due to their better frequency response and noise performance. Deep-submicron CMOS optoelectronic ICs are also of high interest for high-speed short-range applications. Additionally, long-channel CMOS technologies are considered good candidates for LiDAR and VLC systems [1], [2], [3], [4], [5], [6].

Generally, the design of high-speed and low-noise optical receivers in CMOS technology is challenging because of the low transconductance and large parasitic capacitance of CMOS transistors [5], [7]. In addition, the large diameter of plastic optical fibers or large transmission distances in VLC require the size of the photodiode (PD) to be inevitably large to increase the incident optical power. This leads to an increase in the parasitic capacitance at the input node of the receiver, degrading the bandwidth and noise performance. This input capacitance varies between tens of fFs and nF, depending on the application [7], [8], [9], [10], [11], [12]. Employing inductors can mitigate the effect of large parasitic capacitances to some extent, which suffer from increasing

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chip area. In such applications, power consumption and silicon area have become crucial factors in addition to speed and noise considerations. As a result, low-power inductorless optical receiver circuits in CMOS technology have been developed and presented [13], [14], [15]. Transimpedance amplifiers (TIAs) are the first block in the front end of optical receivers, influencing the performance of the receivers, particularly noise and bandwidth. They are specifically designed to isolate the effect of the input capacitance (C_{in}), which consists of the PD capacitance (C_{PD}) and other parasitic capacitances such as the input pad capacitance (C_{PAD}). This is achieved by reducing the input resistance (R_{in}) of the circuit. Reducing R_{in} enhances bandwidth and decreases input-referred noise, typically, at the expense of increased power consumption. Therefore, having more degrees of freedom to achieve a desired low value of R_{in} relaxes tradeoffs among the TIA circuit parameters. With this aim, various TIA topologies have been proposed [5], [7], [13], [16], [17], [18], [19], [20], [21], [22], [23], [24].

For example, in the CG circuit in Fig.1(a), R_{in} is related to the transconductance of the input transistor and the power consumption. However, Rin cannot be arbitrarily reduced because increasing the power consumption limits the voltage headroom at the output node and decreases the value of R_1, degrading the gain and noise performance. As a result, the dominant pole of this circuit usually occurs at the input node. The regulated-cascode (RGC) circuit shown in Fig.1(b) uses the transconductance-boosting (gm-boosting) technique to reduce R_{in} and isolate the effect of C_{in}. The reduction of R_{in} in the RGC circuit moves the input pole farther up compared with the CG circuit and the bandwidth is limited by the output node [18].

Various modified RGC (MRGC) topologies have been proposed to improve the performance of the original RGC structure. These structures introduce degrees of freedom for circuit design and improve the performance at the same power consumption compared to the CG configuration [16], [17], [21], [25].

In the dual-feedback RGC (DFRGC) topology shown in Fig.1(c), an additional feedback path, path C, has been employed. This path further reduces R_{in} and can isolate very large input capacitances. In addition, it decreases the output resistance and moves the output pole farther away from the origin, making it a good candidate for wideband applications. However, the gain is reduced in this topology due to the path C compared with the RGC structure [10], [11].

The super-gm-boosting topology of Fig.1(d) implements another method, by employing the feedback path C', to improve the performance compared to the DFRGC structure [7]. In this topology, C' is implemented by a two-stage common-source (CS) amplifier. Unlike DFRGC, the gain of this structure is not related to the value of R_1 and is determined by the transconductance of transistor M_t, i.e. by g_{mt}. By using a current bleeding technique through M_{cb}, the problem of gain reduction in this topology is solved to some extent and the noise performance is also improved compared to DFRGC. However, the current bleeding transistor, M_{cb}, increases the noise. In addition, the poles of the amplifier C' limit the TIA's bandwidth.

A modified dual-feedback RGC (MDFRGC) topology is proposed in this paper as shown in Fig.1(e). This topology further reduces R_{in}, both by g_m-boosting and by means of a negative term in the R_{in} expression, to save power consumption and provide more degrees of freedom in the design procedure. In this figure, the feedback path A1 is similar to the amplifier B in the RGC topology of Fig.1(b). The feedback path A2 introduces the terms X and Y as a function of the A2 gain in the R_{in} expression, as illustrated in Fig.1(e), and further reduces the input impedance to isolate the large C_{in}. The proposed topology offers greater design flexibility for achieving the desired input resistance with lower power consumption compared to conventional designs, while avoiding gain reduction, unlike the structure shown in Fig. 1(c).

In conventional structures, isolating the effect of C_{in} often leads to bandwidth constraints imposed by the output node. The proposed structure introduces a negative capacitor ($-C_{A2}$) at the output node to reduce the effect of the load capacitance (C_L) and increase the bandwidth, particularly in applications where C_L is large. This topology breaks the typical tradeoff among gain, input resistance, and headroom found in conventional structures. It allows for increasing R_1 (gain) without concerns about bandwidth degradation, ultimately improving the noise performance.

This paper is organized as follows. In section II, the analysis of the proposed TIA is explained to show the effectiveness of the proposed techniques. Section III provides measurement results of the implemented circuit followed by conclusions in section IV.

II. ANALYSIS OF THE PROPOSED CIRCUIT

A. INPUT IMPEDANCE

In optical communication systems, photodiodes with large photodetection areas improve the alignment of the fiber to the photodiode or enable larger transmission distances in VLC, leading to better system noise performance. However, they suffer from large parasitic capacitance, which limits the bandwidth. Additionally, the input resistance and wire bonding network affect the overall system performance. For current TIA structures, such as some shown in Fig. 1, with the simplified model illustrated in Fig. 2(a), equation (1) describes the relationship between the input current to the TIA and the output current from the photodiode [26]. The ideal value for this ratio is 1, meaning that all the photodiode current is transferred to the circuit across all frequencies.

$$\frac{i_{in}}{I_{PD}} = \frac{1 + R_{in}C_{in}s}{1 + R_{in}(C_{in} + C_{PD})s + L_B C_{PD}s^2 + L_B C_{PD}R_{in}C_{in}s^3} \quad (1)$$

According to (1), the TIA design is influenced by the bonding network. In monolithic structures, where the photodiode is integrated on-chip and the bonding wire inductance, L_B, is zero, the currents relationship is simplified as (2).

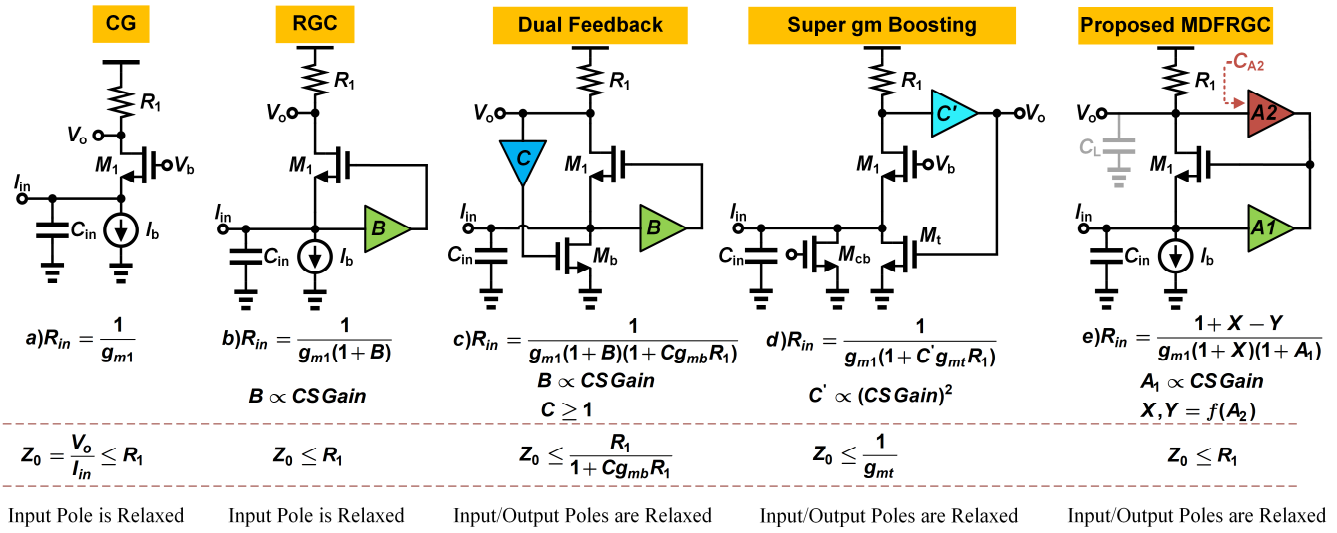

FIGURE 1. TIA topologies being employed to relax tradeoffs among the circuit parameters.

In this case, reducing R_{in} allows the current ratio to converge towards 1 over a broader frequency range, as depicted in Fig. 2(b).

$$\frac{i_{in}}{I_{PD}} = \frac{1+R_{in}C_{in}s}{1+R_{in}(C_{in}+C_{PD})s}$$
$$if: R_{in}=0 \rightarrow \frac{i_{in}}{I_{PD}}=1 \tag{2}$$

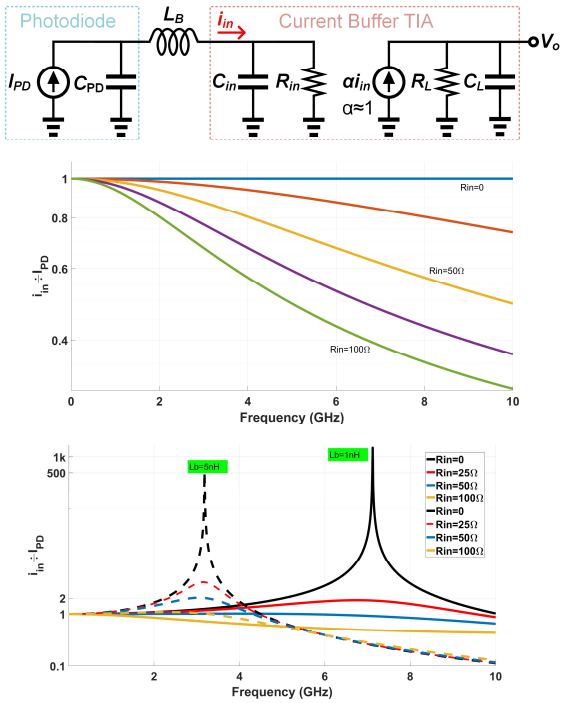

FIGURE 2. Simple PD and TIA connection model (top), I_{PD} and i_{in} currents transfer function for $L_b = 0$ (middle) and for L_b variations (bottom).

In case of $L_B \neq 0$, setting Rin = 0 in (1) leads to (3)

$$if: R_{in}=0 \rightarrow \frac{i_{in}}{I_{PD}}=\frac{1}{1+L_bC_{PD}s^2} \tag{3}$$

The values of L_B and C_{PD} should be small enough to ensure that the resonance in (3) occurs well beyond the system's operating 3-dB bandwidth. Fig. 2(c) illustrates the effect of different R_{in} values on the current transfer function in this case. The optimal R_{in} value for capturing most of the photodiode current is determined during the initial design phase [26]. Both of the aforementioned scenarios demonstrate that possessing design flexibility in the input impedance enables a TIA circuit to adjust effectively to diverse applications.

Both above scenarios show that having design flexibility in the input impedance allows a TIA circuit to adapt to various applications.

Fig. 3(a) shows the circuit schematic of the proposed topology. The amplifier A1 in Fig. 1(e) is implemented by a single-stage CS amplifier, and a CS amplifier with source degeneration implements A2. The capacitor C_3 is employed in the degeneration block to enhance the frequency response as described in the following paragraphs. Low-frequency gain and frequency response of A1 and A2 are given by

$$\begin{cases} A_1=\dfrac{-a_1}{1+\frac{s}{\omega'_{p1}}} \\ A_2=\dfrac{-a_2(1+\frac{s}{\omega'_{z1}})}{(1+\frac{s}{\omega'_{p1}})(1+\frac{s}{\omega'_{p2}})} \end{cases}, \begin{cases} a_1=g_{m2}R_2,\ a_2=\dfrac{g_{m3}R_2}{1+g_{m3}R_3} \\ \omega'_{p1}=\dfrac{1}{R_2C_2},\ \omega'_{p2}=\dfrac{1+g_{m3}R_3}{R_3C_3} \\ \omega'_{z1}=\dfrac{1}{R_3C_3} \end{cases} \tag{4}$$

Ignoring the effect of L_B and the parasitic capacitance C_2 in Fig. 3(a) and assuming that a large capacitance C_{in} =C_{PD}+C_{Pad} is present at the input node, the input impedance of the proposed structure can be written as

$$Z_{in}=\frac{1}{\alpha}\left\{\frac{1}{g_{m1}}-\beta\left(\frac{R_1C_L-R_3C_3}{1+sR_1C_L}+\frac{g_{m3}R_3C_3R_3}{1+g_{m3}R_3+sR_3C_3}\right)\right\}$$
$$Where: \begin{cases} \alpha=1+g_{m2}R_2 \\ \beta=\dfrac{g_{m3}R_2R_1}{R_1C_L(1+g_{m3}R_3)-R_3C_3} \end{cases} \tag{5}$$

The input impedance of (5) is modeled as illustrated in Fig. 3(b). In this model, R_b is the output resistance of the M_b current source and is assumed to have a large value.

The degrees of freedom, α, β, R_3, C_3, and g_{m3} in (5), enhance the TIA performance and relax circuit tradeoffs compared with the RGC, especially for large PD capacitors. For example, reducing R_{in}, improves the gain at low frequencies, Z_0. In most of the current buffer topologies like the proposed topology, Z_0 is simply related to R_{in} as follows

$$I_{in} = \frac{V_{in}}{R_b} + \frac{V_o}{R_1} \rightarrow Z_0 = \frac{V_o}{I_{in}} = R_1\left(1 - \frac{R_{in}}{R_b}\right) \tag{6}$$

According to (5), reducing R_{in} in the proposed topology without increasing the current of the input transistor M_1 relaxes the gain and output node headroom tradeoffs compared with other current buffer topologies. For example, in the CG circuit of Fig. 1(a), R_{in} can only be reduced by increasing the M_1 current. Because of headroom limitations, this current increment in the CG topology reduces R_1 and, hence, the gain.

B. FREQUENCY RESPONSE

Assuming that the small R_{in} isolates the effect of C_{in} in Fig. 2(a), the bandwidth of this circuit is limited by R_L and C_L at the output node. The transfer functions of the proposed topology and the RGC are derived in the Appendix. The RGC circuit exhibits a dominant real pole due to the output node and a pair of complex conjugate poles caused by the input node and the capacitance C_2, which is the parasitic capacitance at the output of the amplifier B in Fig. 1(b), as shown in Fig. 4(a). Therefore, in applications where C_L is large or a high gain is required, the 3-dB bandwidth of the RGC circuit decreases drastically according to (7) [17], [18], [27].

$$\omega_{3dB-RGC} = \frac{1}{R_1 C_L} \tag{7}$$

The pole-zero locations of the proposed topology are shown in Fig. 4(b) where there are one zero, two real poles, and one pair of complex conjugate poles. The location of the first zero, ω_{Z1}, and the first pole, ω_{P1}, is obtained according to (8) and (9), respectively.

$$\omega_{Z1} = \frac{1 + g_{m3}R_3}{R_3 C_3} \tag{8}$$

$$\omega_{P1} = \frac{1}{\frac{1}{\omega_{Z1}} + \underbrace{R_1 C_L - \frac{C_{in}}{1+a_1}\left(R_1 a_2 - \frac{1}{g_{m1}}\right)}_{\cong 0}} \tag{9}$$

According to (8), ω_{Z1} is related to M_3, R_3, and C_3 and introduces a degree of freedom for circuit design. These circuit parameters can be employed to place ω_{Z1} near ω_{P1}, as illustrated in Fig. 4(b), and cancel their effect on the amplifier bandwidth. In this case, the bandwidth of the proposed circuit is determined by P2 in Fig. 4(b) and can

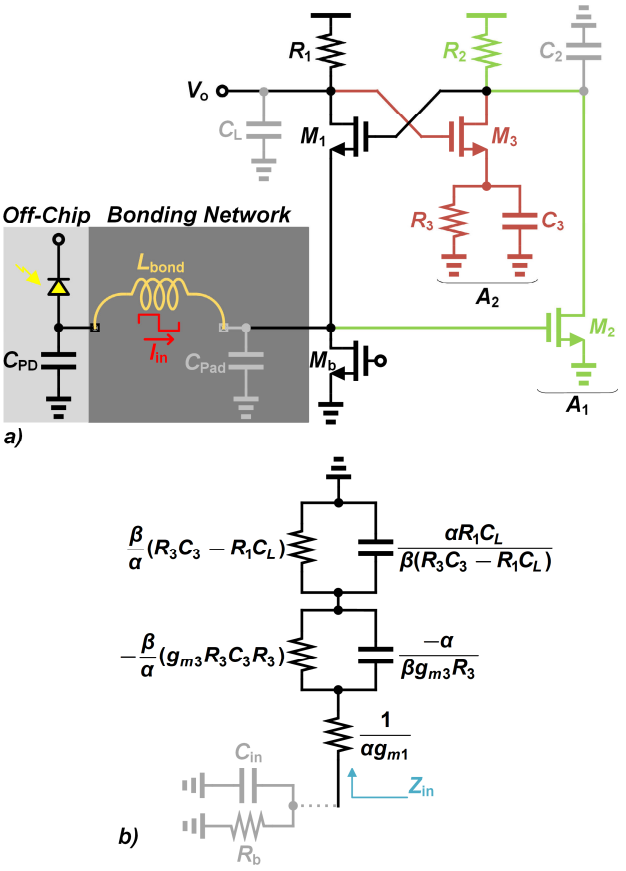

FIGURE 3. a) Circuit schematic of the proposed topology, b) model of the input impedance in the proposed topology.

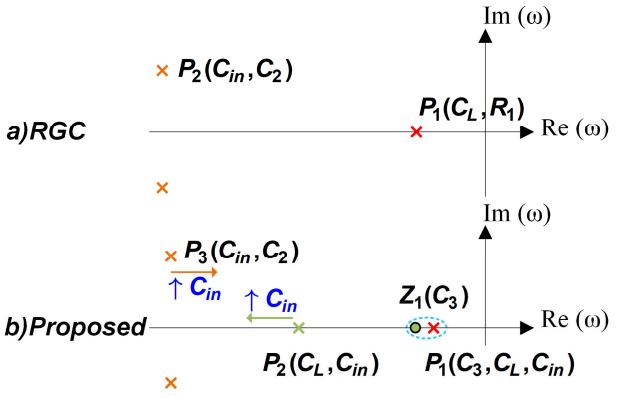

FIGURE 4. Pole-zero locations of (a) the RGC and (b) the proposed topology.

be expressed as

$$\omega_{P2} = \frac{1}{R_1 C_L - \frac{C_{in}}{1+a_1}\left(g_{m3}R_1R_2 - \frac{1}{g_{m1}}\right)} \tag{10}$$

Because of the negative term in the denominator of (10), the bandwidth of the proposed circuit is larger than the bandwidth of the RGC circuit in (7). In other words, the proposed

topology enhances the bandwidth regarding both the input and output nodes.

In order to further demonstrate the effectiveness of the proposed topology, the circuit's output admittance is expressed in equation (11), and its equivalent model is shown in Fig. 5(a),(b).

$$Y_{out}(s) \approx \frac{-a_2}{R_b\,(1+a_1)}\left\{1+s\,(1+g_{m3}R_3)\,R_bC_{in}-\frac{s\,(g_{m3}R_3R_bC_{in})}{1+s\frac{R_3C_3}{1+g_{m3}R_3}}\right\} \tag{11}$$

The model consists of a large negative resistance, which is related to the bias resistance R_b and can be ignored, in parallel with a negative capacitance, which is a function of C_{in}. It also includes a series combination of positive resistance and capacitance. The value of the positive resistance can be adjusted by C_3 so that the effect of positive capacitance is lowered, and the negative capacitance can reduce the effect of C_L, hence improving the bandwidth.

The simulation result of the output impedance behavior is shown in Fig. 5(c). The real part of the output impedance is negative and its imaginary part is positive, decreasing with increasing frequency. This behavior confirms that a negative capacitance is generated at the output, compatible with (11).

The effect of C_{in} and C_3 values on the output impedance is also examined as shown in Fig. 6. Fig. 6(a) depicts the output impedance magnitude, normalized to its low frequency value, for three different values of C_{in}. According to Fig. 5(b) and Fig. 6(a), increasing C_{in} increases the negative capacitance at the output node, deducts the C_L effects, and improves the bandwidth.

It is in contrast to conventional TIA topologies, in which, large values of C_{in} impose severe trade-offs among performance parameters. The bandwidth improvement of the proposed topology by increasing C_{in} occurs as long as the complex conjugate poles, P_3 in Fig. 4, are not dominant. Fig. 6(b) illustrates the output impedance for C_3 =0 and two other C_3 values. As shown in this figure, employing C_3 introduces the zero, ω_{Z1}, near the first pole, ω_{P1}, in the amplifier transfer function and enhances the bandwidth by increasing the positive resistance in the model of Fig. 5(b).

C. NOISE PERFORMANCE

The power spectral density of the input-referred current noise of the proposed circuit at low frequencies is given by

$$\overline{i_{n,in}^2} = \left[\frac{1}{R_b(1+g_{m2}R_2)}\right]^2\left\{\left(\frac{1}{g_{m1}}\right)^2\overline{I_{n,M1}^2}+(R_2)^2\,(\overline{I_{n,M2}^2}+\overline{I_{n,R2}^2})\right\} + \left[\frac{R_2}{R_b(1+g_{m2}R_2)(1+g_{m3}R_3)}\right]^2\left\{\overline{I_{n,M3}^2}+(g_{m3}R_3)^2\,\overline{I_{n,R3}^2}\right\} + \left(\frac{1+g_{m1}R_b(1+g_{m2}R_2)}{g_{m1}R_b(1+g_{m2}R_2)}\right)^2\overline{I_{n,R1}^2}+\overline{I_{n,Mb}^2} \cong \overline{I_{n,R1}^2}+\overline{I_{n,Mb}^2} = 4kT\left(\frac{1}{R_1}+\gamma g_{mb}\right) \tag{12}$$

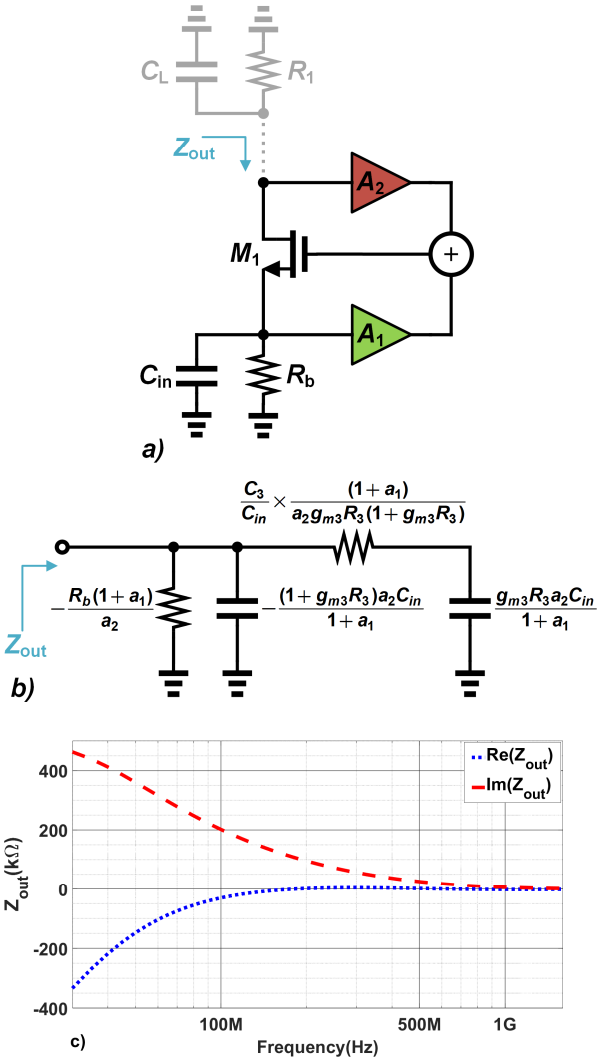

FIGURE 5. a), b) The equivalent model of the output impedance of the proposed topology, c) simulation results of the output impedance behavior.

Due to the relatively large value of R_b, the input-referred noise is mainly determined by the noise of the current source, M_b, and R_1. In contrast to the conventional RGC structure, various parameters could be set in the proposed topology to achieve the desired low input resistance, according to (5), and there is no need to increase the current of M_1 for this goal. Therefore, there are sufficient degrees of freedom to decrease the value of g_{mb} in (12). Additionally, the negative capacitance at the output node allows for an increase in R_1 without concern about the limitation of BW.

To validate (12), the noise contributions of all circuit components are depicted in Fig. 7(a). The figure demonstrates that the auxiliary path in Fig. 1(e), comprising M_3 and R_3,

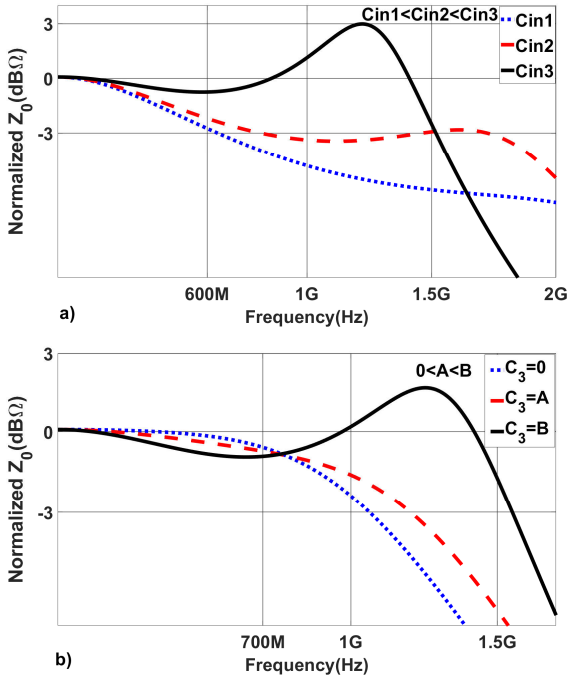

FIGURE 6. The effect of a) C_{in} and b) C_3 values on the output impedance.

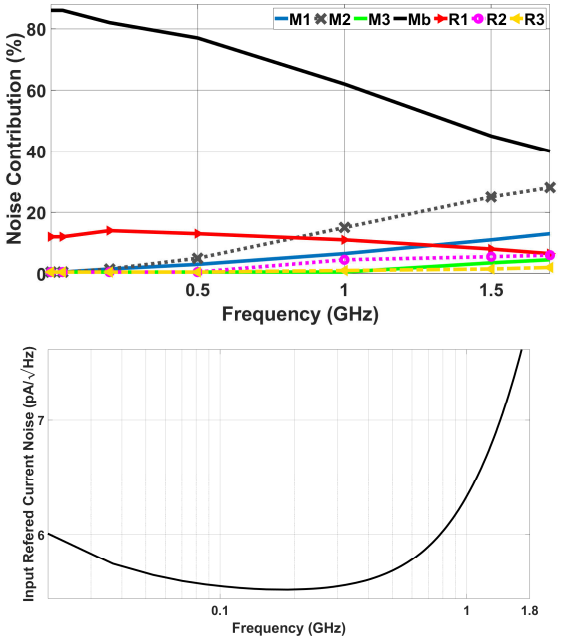

FIGURE 7. a) Noise contribution of circuit elements in the operating range(top), b) Input referred current noise(bottom).

does not significantly contribute to the overall noise, while introducing degrees of freedom to the design. Consequently, the noise level of the proposed circuit is significantly reduced compared with the conventional RGC. This feature makes the proposed topology a good candidate for broadband and low-noise applications.

Fig. 7(b) shows the total input referred noise of the proposed circuit in the frequency domain. The noise value initially decreases at low frequencies and starts to increase at high frequencies.

Fig. 8 shows the simulated eye diagrams of the proposed circuit. It shows the benefits of low-noise design in low-input current values and a linear behavior in high-input current values that suggests a robust and well-behaved structure. Transient noise, wire bond, and photodiode parasitic capacitance effects have been considered in the simulations in order to achieve as reliable results as possible.

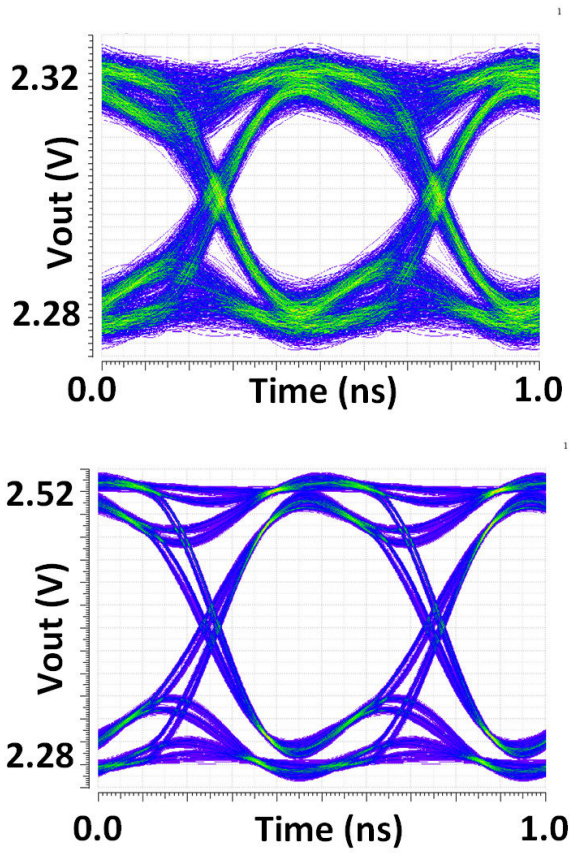

FIGURE 8. Simulated eye diagrams at the TIA output for DR = 2 Gbps and PRBS31 a) Iin = 11 μA (top), b) Iin = 70 μA (bottom).

III. EXPERIMENTAL RESULTS

The proposed TIA topology is implemented in four-metal 0.35 μm CMOS X-FAB technology using 3.3 V transistors with f_T = 20 GHz. The power consumption of the TIA is about 7.4 mW and the active area of the chip is about 0.01 mm^2. Fig. 9(a) shows the optical measurement setup. The Rohde & Schwarz ZNB8 Vector Network Analyzer (VNA) applies the modulated signal to a 1550 nm laser diode in this setup. The PC determines the attenuation level of the laser. The light beam is radiated to an InGaAs PIN PD through a single-mode fiber. The XYZ positioner is used to align the light on the PD. The PD connects the electrical

TABLE 1. Comparison of TIAs.

		BW (GHz)	Z_0 (dBΩ)	Noise (pA/√Hz)	Noise (μArms)	C_{in} (pF)	P_{dc} (mW)	Topology	Tech (nm)	FOM_1	FOM_2
THIS WORK		1.7	69	6	0.24	0.45	7.4	MDF-RGC	350	54	647
[18]	JSSC2004	0.86	58	6.3	N/A	1	85	RGC	600	1.3	8
		0.95	58	6.3	N/A	0.5	85	RGC	600	0.7	9
[28]	JSSC2004	0.67*	80	20.8**	0.54	1	27	RGC	250	11.9	248
[5]	ACCESS2024	1.8	60	9.2	0.39	0.45	2.2	LV CC-RGC	350	40	818
[30]	TVLSI2016	1	69	9.3	N/A	0.5	6	CC	180	25	470
[29]	JSSC2016	0.73	69	5**	0.135	0.7	9.9	SF	350	29	208
[8]	TCASI2013	1	78	7.2	0.28	1.8	12	SF	40	165	662
[31]	JSSC2023	0.94	85.2	8.8**	0.27	0.65	24.3	SF	180	52	704
[32]	TCASI2023	0.6	60	10.8**	0.266	5	31.5	SF	180	8.8	19
[33]	TVLSI2021	3	61	25.5**	1.4	0.2	N/A	SF	65	-	-
[34]	ELELETT2007	1	68	7.5	N/A	0.5	6.9	SF	350	24	364
[35]	SENSOR2021	2.6	59	16.8	N/A	N/A	40	CC	65	-	58
[36]	SENSOR2023	0.58	87	15.4	N/A	0.49	50.6	DF	180	8.2	256
[17]	TCASI2015	7	50	31.3	2.6	0.25	7.5	MRGC	130	2.4	295
[38]	TCASI2018	7	53	27	2.14	1	14.4	DF-RGC	130	8	217

*ON-CHIP INDUCTORS HAVE BEEN EMPLOYED.
** CALCULATED FROM THE REPORTED RMS NOISE AND BW USING (12).

signal to the chip through the bonding network. After being amplified by the proposed circuit, it finally reaches the VNA through an active picoprobe. In a similar setup, shown in Fig. 9(b), a bit pattern generator (BPG) applies the modulated signal to the laser, and finally, the signal is received by a Keysight MSOV204A signal analyzer (SA) to take the eye diagrams. Fig. 9(c) shows the close-up photomicrograph of the fabricated chip in 350 nm CMOS.

Fig. 10 shows the frequency response resulting from the optical measurement setup. The transimpedance gain of the circuit is about 69 dBΩ, and the 3-dB bandwidth is about 1.7 GHz for $C_{in} = 0.45$ pF.

Fig. 11 shows the output voltage histogram for dark conditions. The histogram's standard deviation is 690 μV_{rms} which includes the entire circuit's output noise and the SA's inherent noise. By excluding the inherent noise of the SA, which is 301 μV_{rms}, the input-referred noise current and its average spectral density ($I_{n,in,av}$) are obtained according to (13) and (14).

$$I_{n,in} \cong \frac{\sqrt{(V_{n,\text{total}})^2 - (V_{n,SA})^2}}{Z_{mid-band}} \cong \frac{\sqrt{(690)^2 - (301)^2}}{2512} = 0.247\ \mu A_{rms} \tag{13}$$

$$I_{n,in,av} \cong \frac{I_{n,in}}{\sqrt{Bandwidth}} = 6pA/\sqrt{Hz} \tag{14}$$

In (14), $I_{n,in,av}$ is calculated from the mid-band gain. If the low-frequency transimpedance gain of 69 dBΩ is employed in (13), $I_{n,in,av}$ decreases to 5.3 pA/√Hz.

Fig. 12 shows the measured eye diagrams of the TIA output at data rates (DR) of 2 Gbps and 3 Gbps, where buffer and optical measurement inherent losses are included.

Measurement results of the implemented topology are compared with shunt feedback (SF) TIAs and some current mode TIAs such as RGC, MRGC and cross-coupled (CC) in Table 1. Generally, the SF TIAs benefit from low noise performance. Current-mode TIAs are good candidates for isolating C_{in} effects at high frequencies, but they suffer from noise issues. Table 1 illustrates that the proposed topology, with the added degree of freedom in R_{in}, effectively isolates large C_{in} effects at high frequencies. Additionally, it demonstrates that the output negative capacitance allows for increasing the transimpedance gain, which results in noise reduction. The comparison of the proposed TIA with the original version of RGC in [18] and [28] confirms this result.

The low-noise SF structure in [29], which has also been implemented in the 0.35 μm CMOS X-FAB technology, is a suitable option for comparison. The proposed current-mode TIA has comparable noise performance with the low-noise SF in [29] while presenting twice the bandwidth. Also, the proposed structure demonstrates superior performance in terms of noise and bandwidth compared to the conventional SF in [34], under comparable conditions of power consumption, C_{PD}, gain, and technology.

In Table 1, two figures of merit (FOMs) are employed according to (15) and (16) to ensure a fair comparison [7], [8], [14]. In these expressions, Z_0 is the TIA gain, BW is the TIA bandwidth, C_{in} is the input parasitic capacitance, P_{DC} is the power consumption, and noise is the average input-referred current noise spectral density.

$$FOM_1 = \frac{Z_0(\Omega) \times BW(GHz) \times C_{in}(pF)}{Noise(pA/\sqrt{Hz}) \times P_{DC}(mW)} \tag{15}$$

$$FOM_2 = \frac{Z_0(\Omega) \times BW(GHz)}{P_{DC}(mW)} \tag{16}$$

As illustrated in Table 1, this work demonstrates superiority in terms of the FOMs when compared to most of the TIAs that have been reported. The table highlights the advantages

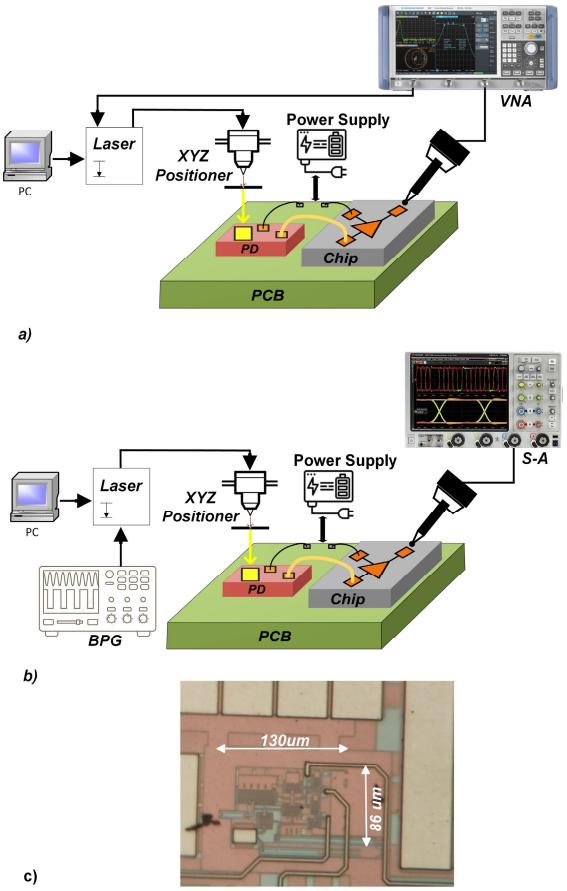

FIGURE 9. Measurement setup for a) frequency response, b) eye diagram, c) photomicrograph of fabricated chip.

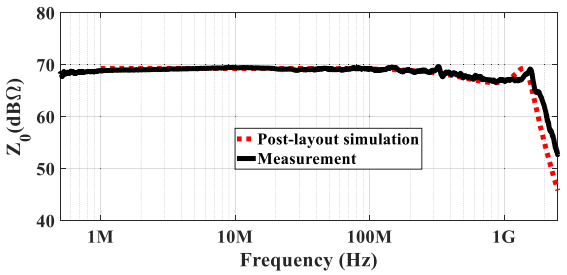

FIGURE 10. Frequency response and transimpedance gain of the proposed circuit with InGaAs PIN photodiode.

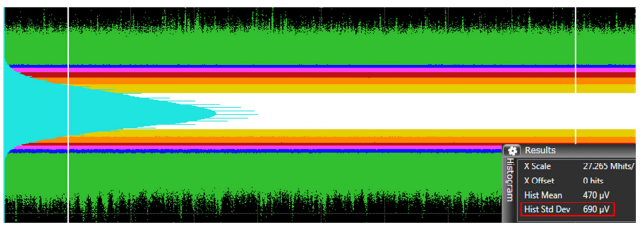

FIGURE 11. Output voltage histogram for dark conditions.

of the proposed circuit techniques in relaxing the tradeoffs in the design.

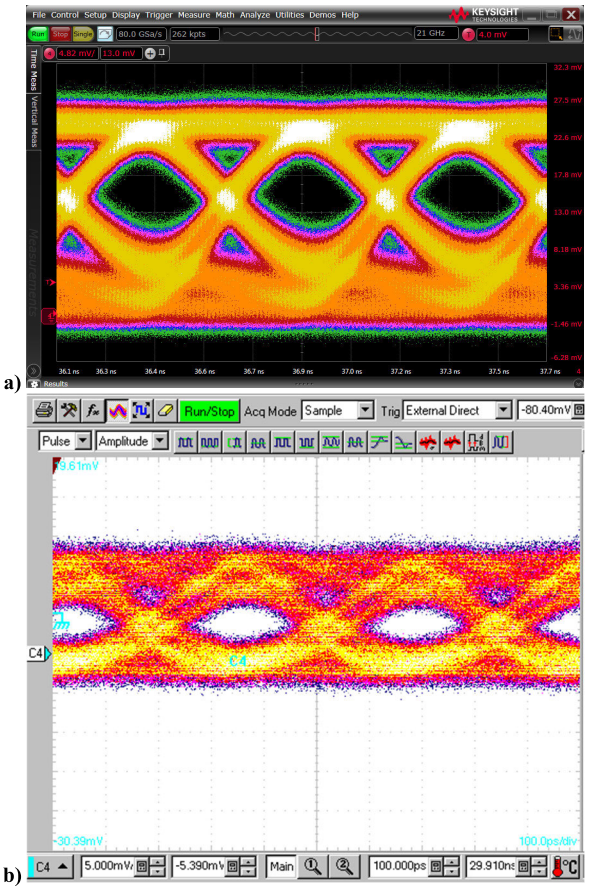

FIGURE 12. Measured eye diagrams at the TIA output for a) DR = 2 Gbps, I_{in} = 44 μA and PRBS31 (top), b) DR = 3 Gbps, I_{in} = 25 μA and PRBS7 (bottom).

IV. CONCLUSION

In this paper, an MDFRGC TIA topology has been presented to enhance the bandwidth regarding both the input and output nodes and improve the noise performance. This is achieved by the introduced NRC network, which reduces the input impedance and cancels the effect of the load capacitance simultaneously. The efficiency of the proposed TIA has been verified by analytical expressions and measurement results of the proposed TIA circuit, fabricated in 0.35 μm CMOS technology. Comparison of the results with other TIA topologies reported in the literature, regarding the defined FOMs, reveals that the proposed technique enhances the TIA performance in spite of employing a technology with a relatively low f_T and it can be used in TIAs implemented in more advanced technologies.

APPENDIX

The transfer function of the proposed circuit in Fig. 3 is expressed as in (17), shown at the top of the next page. The denominator of the transfer function is obtained as in (18), shown at the top of the next page, by substituting (4) into (17). Assuming that the poles are far from each other, the location of the dominant pole is obtained by dividing the first term

$$Z_{PRO}(s)=\frac{V_o(s)}{I_{in}(s)}=\frac{g_{m1}R_1(1+a_1+{}^{s}\!/_{\omega'_{p1}})(1+{}^{s}\!/_{\omega'_{p2}})}{(1+sR_1C_L)(1+{}^{s}\!/_{\omega'_{p2}})\left\{sC_{in}(1+{}^{s}\!/_{\omega'_{p1}})+g_{m1}(1+a_1+{}^{s}\!/_{\omega'_{p1}})\right\}-sC_{in}g_{m1}R_1a_2(1+{}^{s}\!/_{\omega'_{z1}})} \tag{17}$$

$$\begin{aligned}D(s)=&\,s^4\frac{R_1C_LC_{in}}{\omega'_{p1}\omega'_{p2}}+s^3\left\{(R_1C_L+\frac{1}{\omega'_{p2}})(\frac{C_{in}}{\omega'_{p1}})+(C_{in}+\frac{g_{m1}}{\omega'_{p1}})(\frac{R_1C_L}{\omega'_{p2}})\right\}\\&+s^2\left\{\frac{g_{m1}(1+a_1)R_1C_L}{\omega'_{p2}}+\frac{C_{in}}{\omega'_{p1}}+(R_1C_L+\frac{1}{\omega'_{p2}})(C_{in}+\frac{g_{m1}}{\omega'_{p1}})-\frac{g_{m1}a_2R_1C_{in}}{\omega'_{z1}}\right\}\\&+s\left\{\frac{g_{m1}(1+a_1)}{\omega'_{p2}}+g_{m1}(1+a_1)R_1C_L+C_{in}+\frac{g_{m1}}{\omega'_{p1}}-g_{m1}a_2R_1C_{in}\right\}+g_{m1}(1+a_1)\end{aligned} \tag{18}$$

$$\begin{aligned}D'(s)=&\,g_{m1}(1+a_1)+s\left\{g_{m1}(1+a_1)R_1C_L+C_{in}+\frac{g_{m1}}{\omega'_{p1}}-g_{m1}a_2R_1C_{in}(1+g_{m3}R_3)\right\}\\&+s^2\left\{\frac{C_{in}}{\omega'_{p1}}+R_1C_L(C_{in}+\frac{g_{m1}}{\omega'_{p1}})\right\}+s^3\frac{R_1C_LC_{in}}{\omega'_{p1}}\end{aligned} \tag{19}$$

$$Z_{RGC}(s)=\frac{g_{m1}R_1(1+a_1+{}^{s}\!/_{\omega'_{p1}})}{(1+sR_1C_L)\left\{g_{m1}(1+a_1)+s(C_{in}+{}^{g_{m1}}\!/_{\omega'_{p1}})+s^2{}^{C_{in}}\!/_{\omega'_{p1}}\right\}} \tag{20}$$

in (18) by the coefficient of the second term, resulting in (9). As the first zero, determined by C_3, could cancel the effect of the first pole of the circuit, C_3 can be considered like a short circuit at high frequencies. Therefore, by setting the C_3 value equal to zero in (18), we can rewrite the denominator polynomial as in (19), shown at the top of the page. Now, the second pole of the circuit, which determines the bandwidth, is approximately derived by dividing the first term in (19) by the coefficient of the second term, resulting in (10). The transfer function of the conventional RGC circuit is achieved as in (20), shown at the top of the page. with setting a_2 =0 in (17). According to (20), the zero is located at a frequency far from the origin and the dominant pole is real, associated with the output node, and expressed in (7).

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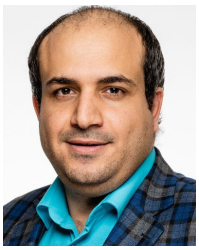

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