Diplomarbeit

Electrical Transport in Monolithic Al-Ge-Al Schottky Barrier Field-Effect Transistors

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Wien, 22. April 2025

Fabian Schwingshandl

Abstract

The increasing demand for microelectronic components has prompted the exploration of new device architectures, processing technologies, and material systems to replace traditional silicon (Si) based technology. Schottky barrier field-effect transistors (SB-FETs) represent one promising alternative, offering potential advantages in scaling and integration. Recent approaches to forming metal-semiconductor heterostructures through thermally induced exchange reactions have emerged as a particularly effective method for creating metal-semiconductor heterostructures with atomically sharp interfaces, opening new possibilities for improving device properties, including higher switching speeds and better power efficiency.
In recent years, germanium (Ge) has garnered significant attention due to its excellent processability, the availability of new passivation techniques, high charge carrier mobility, and strong quantum confinement effects compared to other group IV-based materials. The combination of Ge and aluminum (Al), along with their integration into Al-Ge-Al heterostructures, has facilitated the development of innovative field-effect transistor (FET) architectures.
In this thesis, nanosheet structures were fabricated using a top-down approach and a Germanium-on-insulator (GOI) substrate. The Al-Ge-Al heterostructures were finally established through a thermally induced metal-semiconductor solid-state exchange process, initiated by rapid thermal annealing (RTA). The precise placement and sizing of the nanosheets, along with the well-controlled diffusion process, enabled the creation of a large array of monolithic, single-crystalline Al-Ge-Al nanosheet heterostructures. This method accommodated various Ge segment lengths, including ultra-short segments, without the limitations typically imposed by conventional lithography.
The high-κ passivation of the sheet structure with alumina (Al_2O_3) and the vapor deposition of gold (Au) top gate structures enabled the integration of the heterostructures as channels in electrostatically gated SB-FETs. This setup facilitated a systematic investigation of charge carrier transport mechanisms across a range of Ge segment lengths from $50\,nm$ to $100\,\mu m$, at various temperatures.
The electrical characterization involved analyzing the transfer characteristics and conducting multi-variable bias spectroscopy. These techniques provided comprehensive insight into current modulation capabilities, revealing the effects of surface states and Fermi-level pinning. Furthermore, the analysis visualized the various dominant emission mechanisms at the Schottky barrier (SB), specifically thermionic emission (TE), thermionic-field emission (TFE), and field or tunnel emission (FE). This understanding enabled the determination of device resistivities and SB heights in both n-type and p-type transport regimes.
The low-temperature characterization enabled the exploration of cryogenic properties, considering the charge carrier freeze-out effect and the associated reduction in scattering. Due to the different device scalings, including ultra-short Ge segment lengths approaching the mean free path of electrons, short-channel effects were also examined. These effects include punch-through, drain-induced barrier lowering (DIBL), and ballistic transport.
The systematic evaluation of current transport mechanisms across different channel lengths and temperatures revealed key factors influencing device performance. These insights are essential for advancing the development of SB-FETs and exploring Ge as a fundamental material for emerging nanoelectronic and quantum devices.

Kurzfassung

Die steigenden Anforderungen an mikroelektronische Bauteile haben die Erforschung neuer Architekturen, Verarbeitungstechnologien und Materialsysteme zur Ablösung der traditionellen Silizium- (Si) basierten Technologie vorangetrieben. Schottky-Barrieren-Feldeffekttransistoren (SB-FETs) stellen dabei eine vielversprechende Alternative dar. Neue Ansätze zur Bildung von Metall-Halbleiter-Heterostrukturen durch thermisch induzierte Austauschreaktionen haben sich als besonders effektive Methode zur Erzeugung von Metall-Halbleiter-Heterostrukturen mit atomar scharfer Grenzflächen erwiesen.
In den letzten Jahren hat Germanium (Ge) aufgrund seiner hervorragenden Verarbeitbarkeit, der Verfügbarkeit neuer Passivierungstechniken, der hohen Ladungsträgermobilität und der starken „Quanten-Confinement-Effekte“ erhöhte Aufmerksamkeit erlangt. Diese Eigenschaften machen Ge für eine Vielzahl von Anwendungen, insbesondere in der Quantentechnologie, attraktiv. Die Kombination von Ge und Aluminium (Al) sowie ihre Integration in Al-Ge-Al-Heterostrukturen hat die Entwicklung innovativer Feldeffekttransistor- (FET) Architekturen ermöglicht.
In dieser Arbeit wurden Nanostreifen-Strukturen mittels Top-Down-Prozessierung unter Verwendung eines „Germanium-on-Insulator“ (GOI)-Substrates hergestellt. Die Bildung der Al-Ge-Al-Heterostrukturen wurde dabei durch einen thermisch induzierten Metall-Halbleiter-Austauschprozess hergestellt. Die präzise Platzierung und Dimensionierung der Nanostreifen sowie der gut kontrollierte Diffusionsprozess ermöglichten die Herstellung einer großen Anordnung monolithischer und einkristalliner Al-Ge-Al-Nanostreifen-Heterostrukturen. Diese Methode ermöglichte die Prozessierung verschiedener Ge-Segmentlängen, einschließlich ultrakurzer Segmente, ohne die üblichen Einschränkungen konventioneller Lithographieverfahren. Die high-κ-Passivierung der Schichtstruktur mit Aluminiumoxid (Al_2O_3) und die Gasphasenabscheidung von Gold (Au) für die Top-Gate-Strukturen ermöglichten die Integration der Heterostrukturen in SB-FETs. Diese Anordnung ermöglichte eine systematische Untersuchung der Ladungsträgertransportmechanismen über Ge-Segmentlängen von $50\,nm$ bis $100\,\mu m$ bei verschiedenen Temperaturen.
Die elektrische Charakterisierung umfasste Transferkennlinien und multi-Variable Bias-Spektroskopie. Diese Techniken lieferten umfassende Einblicke in die Strommodulationsfähigkeit und zeigten die Auswirkungen von Oberflächenzuständen und „Fermi-Level-Pinning“. Darüber hinaus visualisierte die Analyse die verschiedenen dominierenden Emissionsmechanismen an der Schottky-Barriere (SB), insbesondere thermionische Emission (TE), thermionische Feldemission (TFE) und Feldemission (FE). Dieses Verständnis ermöglichte die Bestimmung der Bauelement-Resistivitäten und SB-Höhen sowohl im n-Typ- als auch im p-Typ-Transportregime.
Die Tieftemperatur-Charakterisierung ermöglichte die Untersuchung kryogener Eigenschaften unter Berücksichtigung des Ladungsträger-Ausfriereffekts und der Reduktion der Streuung. Aufgrund der unterschiedlichen Bauelement-Skalierungen, einschließlich ultrakurzer Ge-Segmentlängen in der Größenordnung der mittleren freien Weglänge der Ladungsträger in Ge, wurden auch Kurzkanaleffekte untersucht. Diese Effekte umfassen den „Punch-Through“ die Drain-induzierte Potenzialabsenkung (DIBL) und ballistischen Transport.
Die systematische Auswertung der Stromtransportmechanismen bei verschiedenen Kanallängen und Temperaturen offenbarte die wesentlichen Einflussfaktoren auf das Bauelementverhalten. Diese Erkenntnisse sind essentiell für die Weiterentwicklung von SB-FETs und die Erforschung von Ge als grundlegendes Material für zukünftige nanoelektronische und Quantenbauelemente.

Acknowledgment

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Contents

Chapter 1

Introduction

The origins of modern semiconductor technology trace back to 1947 when the first point-contact transistor was discovered. [1, 2] This was followed by the invention of the first junction transistor in 1948 [2, 3], which revolutionized the semiconductor industry and led to the creation of the first integrated circuit (IC) in 1959. [4] Both of these milestones utilized Ge, highlighting this material's significance in the semiconductor technology development. Although Ge has several advantageous electrical properties compared to silicon (Si), the global availability and high-quality oxide of Si, silicon dioxide (SiO_2), have led to the replacement of Ge by Si, especially in the development of metal-oxide-semiconductor field-effect transistors (MOSFETs). In these devices, the semiconductor channel material is covered with a dielectric layer to electrically isolate the metal gate. [5, 6]

Over the past few decades, the evolving demands of new technologies, per Moore's Law [7], have constantly pushed transistor performance to its limits. This has resulted in the development of advanced processes that go beyond standard ICs, including high-performance, low-power, high-density, and cost-effective ultra-large-scale integrated (ULSI) circuits. These advancements are essential for meeting the needs of current emerging concepts such as 5G and 6G wireless communication, machine learning, and artificial intelligence (AI), among others. [8] So far, Si technology remains the leading approach in complementary metal-oxide-semiconductor (CMOS) fabrication processes, thanks to its well-controlled machinability. [9] However, as the transistor sizes continue to shrink, approaching gate lengths of $5\,nm$, parasitic effects such as leakage currents, degraded carrier mobility, and random dopant placement effects become increasingly problematic. These issues indicate that the physical limits of common scaling are being reached. [10, 11] Various new concepts have emerged to extend the life of CMOS and move beyond CMOS applications, including new materials and device architectures. [12, 13] One method that has been used for a long time to continue the enhancement of the performance of Si transistors is to increase carrier mobility by applying mechanical stress. [14, 15] With the discovery of high-κ dielectrics and improved passivation techniques for Ge, the potential for enhancing carrier mobility has increased, as Ge inherently possesses higher carrier mobility. [16] Another enhancement in device performance was realized with the implementation of silicon-on-insulator (SOI) substrates. [17] With the germanium-on-insulator (GOI) substrate already in use, these benefits can be applied to Ge as well. [18, 19]

Due to its unique properties, the benefits of Ge extend to various alternative applications. Notably, the highest mobilities for holes in Ge, the strong spin-orbit coupling [20], and the ability to support superconducting pairing correlations [21] play a significant role in quantum technologies. These quantum-confined holes are essential in advancing spin-based technologies, topological states, and gate-controlled superconducting qubits, commonly known as gatemons and transmons [22, 23], respectively. [24]
In recent years, the Si-Ge material system has garnered significant attention due to its ability to combine the chemical and physical properties of both Si and Ge. This combination opens up a wide range of potential applications, particularly in optoelectronics. One notable advantage is the lattice mismatch between the two materials, allowing strain to be applied to specific components. Furthermore, the Si-Ge system is fully compatible with low-cost CMOS fabrication. [25, 26]

As manufacturers moved towards sub-10-nanometer gate lengths, traditional methods for fabricating MOSFET devices, including polysilicon gates and doped source and drain contacts, have become exhausted. This has led to increased interest in using metal for gates, as well as for source and drain contacts. This shift completely removes the need to dope these contacts, resulting in a simpler fabrication process with enhanced scaling properties. [27, 28]
Additionally, introducing new device architectures has created opportunities and challenges in forming reliable, low-resistance contacts with semiconductor nanostructures. Traditional methods for interconnect formation, which involve top-down processes such as electron beam lithography, physical metal deposition, and lift-off techniques, often encounter problems related to impurities and interface states. These issues can degrade contact resistivity, impacting overall device performance. In the case of Si and Ge nanowires (NWs), one effective approach to overcome this challenge is the formation of intermetallic silicide [29–31] and germanide [32–35] contacts through phase transformation induced by thermal annealing. [32, 36] Metal-semiconductor contacts without intermetallic phases were successfully created in the Al-Si [37] and Al-Ge [36, 38–40] systems through a thermally induced exchange process for quasi 1D NWs and nanosheets. [38] The rapid thermal annealing (RTA) process allows for precise control over both the annealing temperature and duration, enabling careful management of the exchange process. This method allows the creation of ultra-short channel segments and quantum disks QDs with atomically sharp, single-crystalline metal-semiconductor interfaces. [36, 38–40]

As the lengths of semiconductor segments approach the mean free path of bulk charge carriers, the current transport transitions from a diffusive to a ballistic regime. [41] In the ballistic regime, charge carriers can travel through the segments without experiencing scattering. This type of transport is particularly achievable in Ge due to its large electron mean free path of $\approx 35\,nm$. [41] Further, the large exciton Bohr radius results in significant quantum confinement effects occurring at much larger structure sizes, even at room temperature, as demonstrated in Al-Ge-Al NW heterostructures. [41] Consequently, the speed of ultrashort Ge transistors is constrained by the current injection velocity at the source and drain contacts, rather than by the saturation velocity of the carrier mobility in the channel material. [41–43]

The Gunn, or transfer electron effect, also occurs in Ge under high electric fields. [44] This phenomenon allows an electron to be transferred from a conduction band valley with a low effective mass to a nearby valley with a higher effective mass. As a result, the current-voltage (I-V) characteristic exhibits negative differential resistance (NDR). This unique property enables the development of transferred electron devices (TEDs) based on Ge, as well as the creation of logic gate devices that are superior to conventional logic gates in terms of area, speed, and power consumption. [45–47]

This study examines the electrical characteristics of monolithic Al-Ge-Al nanosheet heterostructures, which have been created with different lengths of the Ge segment. The top-down fabrication process enables the well-defined arrangement of large arrays of nanoscaled device structures on a wafer-scale level. Using a GOI substrate, the vertical thickness of the channel structure is predetermined, facilitating the creation of precisely defined channel geometries. The process involves accurately manipulating the Ge layer through optical lithography and a dry etching technique. By combining these methods with the thermally induced formation of atomically sharp Al-Ge contacts, as well as simultaneous Al-Ge exchange, it is possible to create device structures with varying Ge segment lengths, including ultra-short segments. [48] Furthermore, the passivation of the Ge layer with Al_2O_3 using atomic layer deposition (ALD) enables the subsequent deposition of an electrically isolated top gate structure over the channel structure. This device can function as a top-gated MOSFET. More precisely, when Al and Ge are brought into contact, they create an electrical barrier known as the SB, which arises from their specific material properties. This formation is essential for the device to be classified as a SB-FET.
To investigate the current transport regimes across various temperatures, including cryogenic ones, standard FET characterization procedures are carried out. The current transport through a Schottky contact involves various transport mechanisms, which develop differently depending on the temperature. At room temperature, the primary mechanism for electrons is thermionic emission over the barrier. In contrast, as the temperature decreases, the current transport is increasingly dominated by direct tunneling through the barrier, also known as field emission. [49] Previous studies conducted at cryogenic temperatures below $10\,K$ have revealed additional transport phenomena such as Fano resonances [28, 50] and Coulomb blockade. [24, 51, 52] However, these effects are not investigated in this work.
The electrical device characterizations in this study are confined to a temperature range of $400\,K$ to $4.8\,K$, focusing on the fundamental current transport regimes in Al-Ge-Al heterostructures with varying lengths of the Ge segments. The organization of this thesis is structured as follows. Chapter 2 examines the theoretical concepts necessary to understand the processes involved in fabricating the Al-Ge-Al heterostructure, as well as the temperature-dependent electrical behavior of the materials. Chapter 3 outlines the individual steps taken in the fabrication of the Al-Ge-Al heterostructures, including a description of the measurement equipment and the data evaluation process. Chapter 4 highlights and discusses the results of the electrical characterizations and subsequent evaluations. Finally, Chapter 5 provides the conclusion of this work. The appendix contains additional evaluation results, graphs, and detailed process parameters.

Chapter 2

Theoretical Background

This chapter outlines the theoretical fundamentals necessary to understand the key physical characteristics essential for the realization of monolithic Al-Ge-Al heterostructures SB-FET and their electrical behavior across different temperature regimes.

The first part focuses on the materials involved, covering the basic properties of Al as the contacting material and Ge as the semiconducting channel material, and providing a brief overview of currently relevant passivation materials. The discussion also covers the Al-Ge material system, highlighting its properties that are crucial for creating void-free and atomically sharp Al-Ge junctions through a thermal annealing-induced material diffusion process. Additionally, it addresses the conditions required for the formation of the Schottky barrier and how different current transport mechanisms operate under an applied bias voltage. This discussion also considers how the barrier is influenced by material imperfections and low temperatures. Finally, the discussion includes the Al-Ge-Al heterostructure on the GOI comprising a SB-FET, considering the previously mentioned concepts, which encompass the impacts of oxide traps, short channels, and temperature.

2.1 Physical Material Properties

This section focuses on the essential physical properties of materials used in the fabrication of Al-Ge-Al SB-FETs. Special attention is placed on the thermal behavior of Al and Ge, emphasizing its pivotal role in this work. The basic properties of Al as the electrical contact material and Ge as the semiconductor channel material are examined. Additionally, the challenges associated with passivating Ge are addressed, along with the advantages and disadvantages of conventional high-κ dielectrics.

2.1.1 Aluminum

Al is a silvery-white metal, discovered in the 18$^{\text{th}}$ century. [53] The main isotope ^{27}Al is a stable element in group 13 and period 3 of the periodic table with an atomic weight of 26.98. [53] Its atomic number is 13 and the 13 electrons are distributed as [Ne] $3s^2$ and $3p^1$, resulting in 3 valence electrons. [53] Al crystallizes in a face-centered cubic (fcc) lattice with a lattice constant of $a = 404.96\,pm$ [54] and remains stable all the way up to its melting point. The atomic radius is $143\,pm$ and the unit cell includes a total of 4 atoms. [54]

Al is abundantly found in the earth's crust (8.1 %) and is extracted most commonly in the Bayer process from the bauxite ore and afterward produced in an electrolytic cell from molten Al_2O_3 using the Hall-Héroult process. [53] A commercial purity of 99.5 to 99.9% is reached through the electrolytic cell, whereby ultra-high purity of over 99.999 is achieved by „triple-layer refining electrolysis“. [53–55]

After steel, Al is the most widely used metallic material, due to its eminent properties and recyclability. Today, up to 30 % of the total Al production is fabricated from waste material, resulting in 95 % less energy consumption. Even in microelectronic scrap, it has been reported that Al is recovered up to 90 %, while still holding a purity of 85 %. [56, 57] Apart from this, Al is non-toxic, can easily be machined, and has strong corrosion resistance, attributed to the strong reactivity with oxygen to form a self-passivating oxide surface layer. [58] Furthermore, with a low density of $2.7\,g/cm^3$ [54], it is very lightweight while holding a tensile strength of 45 to 60 MPa. [54] The thermal conductivity of Al depends on the purity and has a relatively constant value of $\sim 2.37\,W/(cmK)$ down to $100\,K$, where it becomes strongly sensitive to the temperature. [54] As a result, the electrical resistivity also becomes strongly dependent on the purity and temperature below $100\,K$ where it rapidly falls from the room temperature value of $2.7\,\Omega m$. [53–55]

Al was the main material used for contacts and interconnects in microelectronics, meeting requirements such as low-resistive ohmic contacts to both p- and n-type Si, contact sintering, device packaging, and operating conditions. [59] However, as the feature size of the integrated circuits was shrinking over the course of time, the metal lines acquired thin-film properties rather than bulk metal properties, which directly resulted in electromigration problems due to the increased current density. [60] Inherent with the downsizing, a limiting factor to the switching frequency increase was the interconnect delay time resulting from the higher resistance of the conductor and higher capacity due to the reduced spacing between the interconnects. [61] In addition, the diffusion coefficient of Si in Al increases by an order of magnitude at 400 to 500 $^\circ C$ caused by grain-boundary diffusion. [62] This increase further enhances mass transport, which negatively impacts the material's properties. These changes are a result of structural transformations, phase transitions, and solid-state reactions. [58, 60]

2.1.2 Germanium

Ge is a very important, gray-white indirect semiconductor, discovered in the 19$^{\text{th}}$ century. [63] It can be found in group 14 of the periodic table with the atomic number 32, an atomic weight of 72.61 [53], and a density of 5.3234 g/cm^3 at 298 K. [53] It ocurrs naturally on the basis of five isotopes ^{70}Ge, ^{72}Ge, ^{73}Ge, ^{74}Ge, and ^{76}Ge. The electronic configuration is [Ar] $3d^{10}$ $4s^2$ $4p^2$, which indicates 4 valence electrons. [53, 64, 65]
Ge is estimated to be found at 6.7 ppm in the Earth's crust, and it is obtained from Ge containing minerals like argyrodite or germanite, but mainly gathered from zinc ores and coal. [53, 66] Ge is concentrated most commonly in a pyrometallurgical process as germanium monoxide (GeO) or germanium sulfide (GeS) fly ash. It is then heated in a smelter, whose fumes are chlorinated to obtain crude germanium chloride ($GeCl_4$). Ultra-pure $GeCl_4$ is prepared in a distillation process and afterward hydrolyzed to germanium dioxide (GeO_2). Finally, Ge for the semiconductor industry is provided via hydrogen reduction of GeO_2. Among various techniques, the Czochralski crystal pulling method is most widely used to grow dislocation-free Ge single crystals, using a zone-refined seed crystal with an impurity content of $\sim 10^{10}\, cm^{-3}$. [18]
Ge is used very widely, especially in fiber optics, where Ge from $GeCl_4$ acts as a dopant of SiO_2 to increase the refractive index and lower dispersion properties. Due to the transparency of Ge and GeO_2 to infrared light in the range of $\sim$ 1.8 to 18 μm [65], it is also used to build lenses and window panes for infrared detectors and thus, for instance, for surveillance, night vision, and satellite systems. [67] Because of its scarcity and its commercial importance, recycling of Ge plays a major role. It has been reported that 30 % of the annual Ge production contains recycled material, of which 60 % are obtained from optical devices. [67, 68]

As well as C or Si, Ge is characterized as a group IV element, whose crystal structure consists of two fcc lattices shifted to each other by 1/4 of the main diagonal length, forming a diamond structure. This covalent bond in tetrahedral configuration leads to a distance between adjacent atoms of $\sqrt{3}a/4$. The lattice parameter is given as $a = 565.79\, pm$ at 298.15 K [55] and slightly decreasing linearly with falling temperature. [55] As usual for the diamond structure, each atom resembles a tetrahedron with four surrounding atoms in the corners, resulting in a sp^3 hybrid electronic state. The electrons in the outer shell can be shared with the neighbors through low-energetic binding orbitals and higher energetic antibonding orbitals. The binding states make up the non-conducting valence band, while the conducting non-binding states form the conduction band, separated by the band gap. The band structure can be directly measured through, e.g., x-ray or ultraviolet photoemission spectroscopy (XPS/UPS). [69] The bandstructure of the Ge crystal at 0 K, calculated via quantum mechanical methods can be viewed in Fig. 2.1. [70]

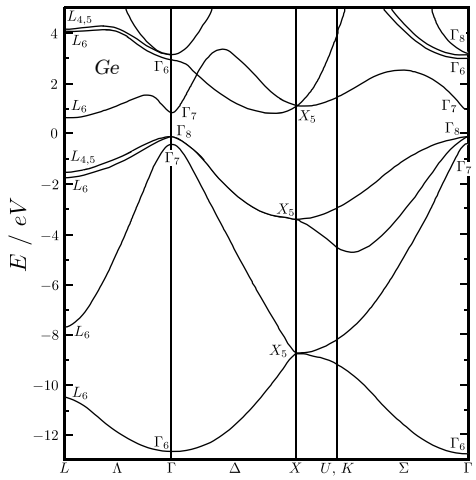

Figure 2.1: *Calculated band diagram of Ge at 0 K. From the point of view of the origin $\vec{k} = \vec{0}$ (Γ - position), the directions inside the Brillouin zone are given as $\Delta = [100]$ (Γ to X), $\Sigma = [110]$ (Γ to K) and $\Lambda = [111]$ (Γ to L). The points on the surface of the Brillouin zone are denoted as $\vec{k} = \langle 100 \rangle$ (L - position) and $\vec{k} = \langle 111 \rangle$ (X - position). The highest energy of the valence band can be found at position $\Gamma_8^v = 0\,eV$, and the lowest energy point of the conduction band is located at $L_6^c = 0.76\,eV$. The different positions of the valence band maximum and the conduction band minimum indicate an indirect semiconductor. The band gap energy can be obtained via $E_g = \Gamma_8^v - L_6^c = 0.76\,eV$, which corresponds to the value at 0 K. Image adapted from [69].*

The resulting curvature of the band structure exhibits small effective masses for electrons and holes, which gives rise to another major advantage of Ge over other semiconductors. The charge carrier mobility is connected to the effective mass via $\mu = q\tau_m/m^*$, with the mean scattering time τ_m. [71] This leads to large carrier mobilities of holes and electrons and a resulting high drift velocity of the charge carriers. This can be helpful to increase the switching frequency or reduce the power consumption of the device. In fact, Ge possesses the highest hole mobility of all semiconductors, which led to the first transistor being made of Ge in 1947. [16] A comparison of the carrier mobilities of electrons and holes of different semiconductor bulk materials can be seen in Fig. 2.2. [16]

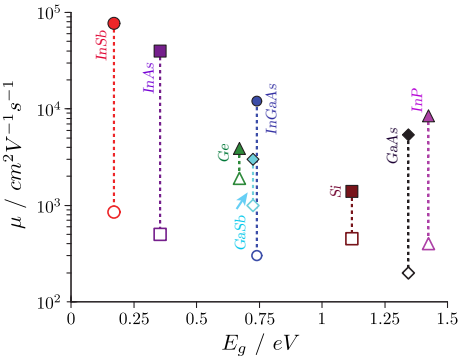

Figure 2.2: *Plot of bulk mobilities of relevant semiconductor materials as a function of the band gap energy. The filled symbols represent the electron mobilities, and the bare symbols indicate the hole mobilities. Ge has the overall highest mobility for holes. Ge, GaSb, and Si possess the smallest deviation between the mobility for electrons and the mobility for holes. In addition, their band gap size lies in the middle of the band gap range of the selected material range. Image taken from [16].*

According to Matthiessen's rule, the overall mobility depends on various scattering mechanisms like phonon scattering, ionized impurity scattering, Coulomb scattering, and surface roughness scattering, to name a few. The bulk mobilities show a strong carrier concentration and temperature dependence, where larger carrier concentrations lead to a lowering in mobility. Due to the carrier freeze-out at low temperatures, the ionized impurities become neutral, which entails an increase in mobility. The carrier mobilities in dependence on the temperature and impurity density can be seen in Fig. 2.3, where Fig. 2.3a corresponds to the mobility of electrons and Fig. 2.3b to the holes. [72]

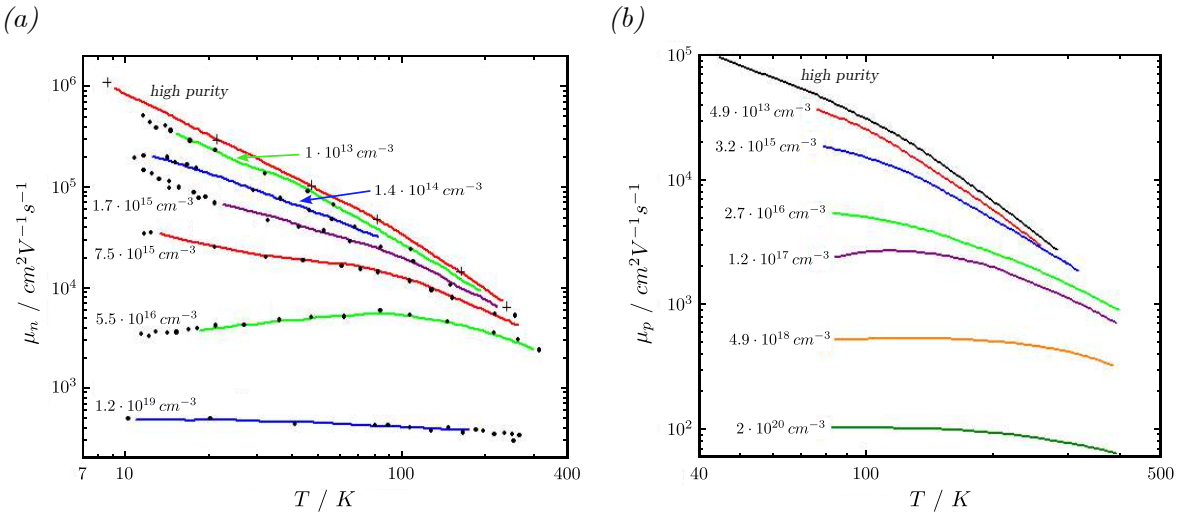

Figure 2.3: *Minority carrier mobility of electrons (a) and holes (b) as a function of temperature and doping concentration $N_A - N_D$. The mobilities of the high-purity Ge in subfigures (a) and (b) were measured using the time-of-flight technique. [73] The mobilities of the doped Ge were determined via the Hall effect. [74, 75] Image adapted from [76].*

2.1.3 Dielectrics

Ge as the base material for the transistor technology was soon after the discovery replaced by Si. It was in the mid-60s that the first MOSFET was built with the use of SiO_2 passivation. [16]

2.1.3.1 Native Germanium Oxide Passivation

In ambient air, Ge promptly forms a native oxide layer, which is unstable and decomposes into various Ge_xO_y suboxides. Some of them are furthermore hygroscopic, water-soluble, and have a high density of dangling bonds at the interface. [77] The resulting interface trap states, which cannot be hydrogen passivated via conventional forming gas anneal, as in the case of Si, significantly degrade the device characteristics. [16] Other attempts were made to grow a GeO_xN_y layer using thermal treatment with ammonia, while a sulfur layer was achieved through wet chemical treatment with ammonium sulfide ($(NH_4)_2$). [77] However, this required an additional high-κ material, due to the low relative permittivity of the nitride passivation layers. [77, 78] An alternative approach involved relocating the dielectric interface away from the surface of Ge and utilizing a Si/SiO_2 structure instead. This was accomplished by epitaxially growing a thin Si layer on top of the Ge. [16, 78]

Recently, a promising technique has emerged that uses the thermal oxidation of Ge, with carefully controlled process parameters. In contrast to Si, the thermal oxidation kinetics in Ge are completely different. The oxidation of Ge at the interface does not occur through a direct reaction with O_2. Instead, the oxidation process takes place via the unstable native germanium oxide layer (Ge_xO_y). In this process, one Ge atom reacts at the Ge_xO_y-Ge interface, resulting in the formation of GeO_2, GeO, and loosely bonded Ge atoms that diffuse through the oxide layer. As they diffuse, these Ge atoms continue to react with GeO_2, producing unstable and volatile GeO, which then desorbs at the surface of the oxide. [79, 80]
It has been shown that the interface state density D_{it} strongly depends on the surface bonding conditions such as growth temperature and O_2 pressure. [81] During the thermal oxidation process, four different oxidation states are confirmed. Namely, Ge^{1+}, Ge^{2+}, Ge^{3+} and Ge^{4+}, corresponding to the oxide species of Ge_2O, GeO, Ge_2O_3 and GeO_2, which appear with various spectral intensities depending on the oxidation temperature. [80, 82] To solely grow GeO_2, emission in Ge^{4+} state is necessary, whose peak intensity is at around 400°C. [81] To prevent the desorption of GeO and resultingly the increase of D_{it}, it is beneficial to grow the GeO_2 at $\sim 300\,°C$. This can be achieved through the use of ozone, which is more reactive than oxygen at lower temperatures. The interface state density can be further lowered by extending the thickness of the oxide layer. [83, 84] As the temperature decreases, the surface roughness tends to increase due to non-uniform oxide desorption. To achieve oxide growth with low surface roughness, longer annealing times are required, resulting in a thicker oxide layer, along with oxidation temperatures exceeding $450\,°C$ to ensure uniform oxide desorption. [80]

2.1.3.2 High-κ Dielectric Materials

Apart from the surface state density, the continuous downscaling of the device dimensions eventually led to unacceptably high gate leakage currents, due to increased tunneling. As a remedy, high-κ materials deposited by ALD, chemical vapor deposition (CVD), pulsed laser deposition (PLD), or sputter deposition were introduced. The large relative permittivity ε_r of high-κ material provides the possibility to increase the gate oxide thickness in order to decrease the gate leakage current while holding the same gate capacity. [42] The dielectric properties of the new material are usually concise by the equivalent oxide thickness $EOT = (\varepsilon_{r,SiO_2}/\varepsilon_{r,high-\kappa})\, t_{high-\kappa}$, which puts the relative permittivity and the thickness of the high-κ oxide in relation to SiO_2. [85]
High-κ materials are primarily utilized to create a thermally stable passivation layer with low defect density and to develop an oxide that enables scaling to very low EOT values. The resulting leakage current when scaling EOT for different high-κ materials can be found in Fig. 2.4b. With increasing ε_r, the band gap appears to become smaller, as depicted in Fig. 2.4a. This aligns with a common characteristic of high-κ materials. [85]
High values of ε_r alone are not sufficient. The oxide must also form a high barrier for electrons and for holes, to inhibit any leakage current. For Ge, this limits the selection to the thermally stable high-κ materials Al_2O_3, ZrO_2, HfO_2, Y_2O_3, and La_2O_3. Among other criteria, good interface quality in terms of roughness and low defect density is required. Trapped charges at the interface must be avoided because they alter the gate threshold voltage and reduce channel mobility by increasing scattering. Overall, the likelihood of oxide breakdown increases, leading to reduced device reliability. Commonly, Al_2O_3 is often used, especially because it remains amorphous and has a large atomic diffusion barrier. However, the resulting defect density is fairly high. [85]

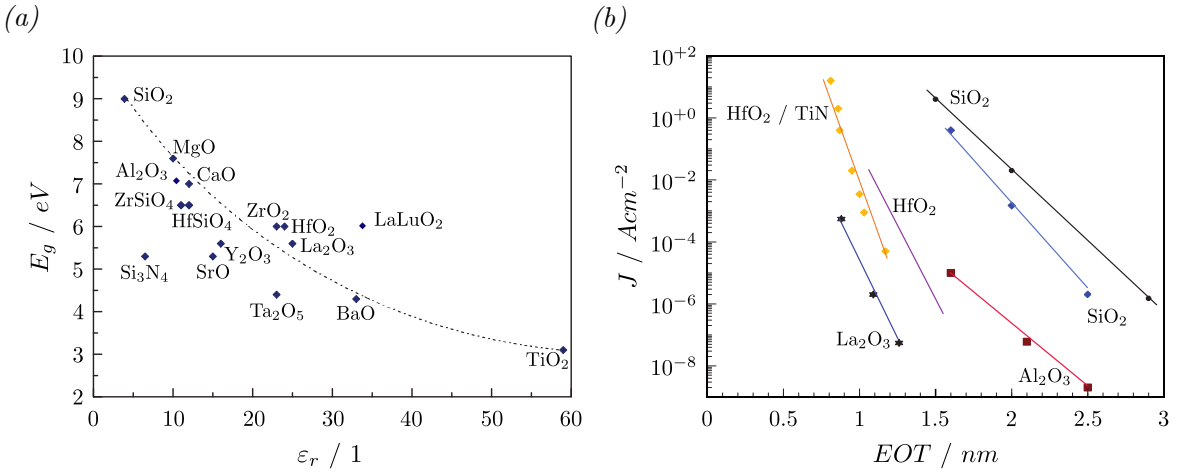

Figure 2.4: *Important dielectric properties of potentially interesting high-κ materials for the surface passivation of Ge. (a) depicts the band gap (E_g) versus the relative permittivity (ε_r) lineup of different high-κ materials. (b) indicates the measured leakage current density (J) at 1 V for various high-κ materials in dependence of the EOT. Image adapted from [85].*

One of the main challenges when depositing high-κ materials on Ge is ensuring adequate surface passivation to prevent the inclusion of Ge oxides at the high-κ dielectric/Ge interface. [86] Remedial measures include the introduction of an interfacial layer. [87] Rare earth oxides such as Y_2O_3, CeO_2, Sm_2O_3, and La_2O_3 have been proven to be successful, as they react with Ge to spontaneously form a catalytic and stable Ge oxide. [87, 88] In general, it has been demonstrated that the *EOT* could be significantly reduced by utilizing stacks of various high-κ materials. [42, 89, 90]

In conclusion, the interface trap density at the surface of Ge cannot be brought close to the level of the Si/SiO_2 interface, despite the best offers. The resulting scattering effects significantly diminish the intrinsically high mobility of Ge. The achievable mobility in n-doped MOSFETs is considerably lower than that of universal Si. [91] Alternative approaches, such as the quantum-well field-effect transistor, counteract mobility reduction by epitaxially growing Si on top of Ge. The lattice mismatch between Si and Ge induces biaxial strain, which in turn increases the mobility. [16, 85, 92]

2.2 Metal-Semiconductor Contact Formation

Recent advancements in the formation of metal-semiconductor junctions have opened an auspicious field of research. More precisely, the thermally assisted diffusion of metals into single-crystalline NWs has facilitated the creation of low-resistance metal-semiconductor contacts, previously a limiting factor. This paved the way for numerous new nanoelectronic devices that go beyond the spatial limitations of traditional lithography processes. [35, 36, 93] Initially, the thermal diffusion was examined using various metals such as Ni [29, 94, 95], Co [31], Pt [30], and Mn [96] in combination with Si NWs, in which silicide intermetallic compounds were created. The resulting atomically sharp interface between the Si and the formed silicide NW significantly reduced the contact resistance.
In the case of Ge, germanide formation can be achieved with Pt [34], Ni [94], Cu [32, 33], and Mn [97]. The germanides Mn_5Ge_3 and Ni_3Ge exhibit ferromagnetism, which could be useful for future spintronics applications. [35, 97, 98]
As previously mentioned, Ge has a high density of surface states, making it essential to develop a low-defect metal-germanium interface in order to mitigate the Fermi-level pinning effect. [35] The Al-Ge material system is particularly advantageous in this context because it does not form intermetallic phases, making it an ideal choice for this work. Furthermore, the superconducting properties of Al at low temperatures enhance its attractiveness, especially for applications in Josephson field-effect transistors (JoFETs) and superconducting quantum interference devices (SQUIDs). [24, 99] Therefore, the Al-Ge material system will be discussed in detail in the following sections.

2.2.1 Thermodynamic Properties of the Al-Ge Material System

The Al-Ge system forms a simple binary eutectic system consisting of three phases: the liquid, the fcc Al solid solution, and the diamond Ge solid solution, which can be viewed in the phase diagram shown in Fig. 2.5.

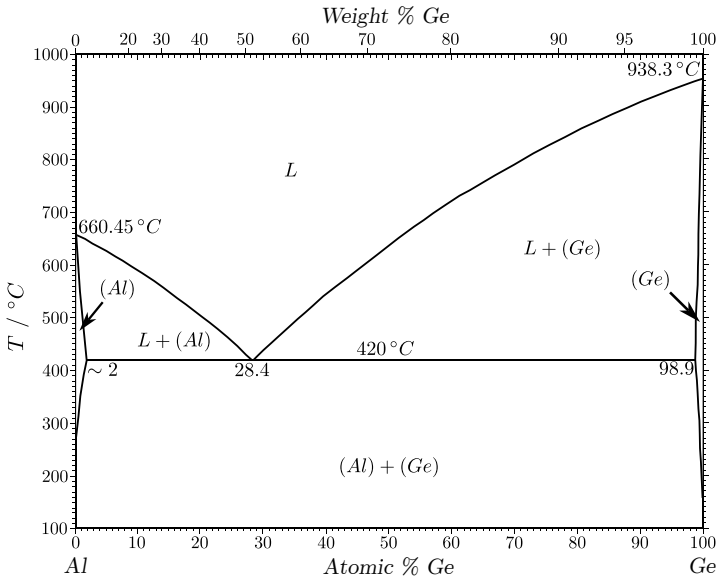

Figure 2.5: *Phase diagram of the eutectic Al-Ge system. The melting points are given as* 660 °*C for Al and* 938 °*C for Ge. The eutectic point is found at* 420 °*C and* 28.4 % (*at*) *Ge. The maximum solubility of Al in Ge is* 2 % (*at*) *and Ge in Al is* 1.1 % (*at*). *[36, 100] Image adapted from [101].*

2.2.2 Solid-State Diffusion Mechanism

The phase diagram shown in Fig. 2.5 illustrates the possibility of one material dissolving into the other. Below the eutectic temperature, Al and Ge atoms undergo mutual exchange through solid-state diffusion. To provide a comprehensive understanding, this discussion first explores the general diffusion mechanism before delving into the specific properties of the Al-Ge diffusion process.

In general, diffusion is the random movement of particles along a gradient of the chemical potential, known as Brownian motion. For diluted systems or ideal solid solutions, the gradient of the chemical potential is also proportional to the concentration gradient. During the processing of materials and the heat treatment of microstructures, diffusion processes are essential. Key examples of these processes include phase transformations, recrystallization, and thermal oxidation. In solids, such as semiconductors and metals, diffusion is governed by fundamental mechanisms, including direct site exchange, interstitial diffusion, interstitial-site exchange, and the lattice site vacancy mechanism. [102, 103]
The equations that govern diffusive transport are known as Fick's laws. In an isotropic medium, where the physical entities have no spatial dependence, Fick's first law is expressed as

$$\vec{J}_f = -D\vec{\nabla}C. \tag{2.1}$$

It describes the particle flux density $\vec{J}_f$ resulting from a concentration gradient $\vec{\nabla}C$. D represents diffusivity and serves as a proportionality factor. Since $\vec{J}_f$ is a conservation entity, an associated continuity equation can be written, resulting in Fick's second law.

$$\frac{\partial C}{\partial t} = \vec{\nabla} \cdot \left(D\vec{\nabla}C\right)$$

Considering the particles' Boltzmann distribution of energy, they stochastically follow a thermal movement. In crystalline solids, diffusion occurs as atomic hops between neighboring lattice sites. Since these jumps originate from thermal activation, their jump rates are determined by the Arrhenius law. It can be expressed for the diffusivity as follows:

$$D = D_0 \exp\left(-\frac{E_A}{k_B T}\right), \tag{2.2}$$

where D_0 is the frequency factor, E_A is the activation energy, k_B is the Boltzmann constant, and T is the absolute temperature. [102]
In a binary system, diffusion is driven by the internal chemical potential, leading to the interdiffusion of both species, denoted as the Kirkendall effect. [102] This leads to the creation of two separate diffusion fluxes $J_{f,A}$, J_B, each with material-dependent diffusion coefficients D_A, D_B, known as intrinsic diffusion coefficients. The non-vanishing difference between these two fluxes leads to a net flow of mass. The Kirkendall velocity can be defined using the intrinsic fluxes $J_{f,A}$ and J_B, as well as the partial molar volumes $\widetilde{V}_A$ and $\widetilde{V}_B$. It is given by the equation

$$v_K = \dot{x}_K = -\left(\widetilde{V}_A J_{f,A} + \widetilde{V}_B J_{f,B}\right),$$

which represents the velocity of the Kirkendall plane at the position x_K. From the ratio $dC_A/dC_B = -\left(\widetilde{V}_B/\widetilde{V}_A\right)$ follows Darken's first equation

$$v_K = \widetilde{V}_B \left(D_B - D_A\right) \nabla C_B, \tag{2.3}$$

where ∇C_B gives the concentration gradient at the Kirkendall plane. Darken's approach states that the interdiffusion flux at the Kirkendall plane can be formulated as the intrinsic diffusion flux of one of the components i plus (or minus) a term $v_K C_i$:

$$J_{f,i} = -D_i \frac{\partial C_i}{\partial x} \pm v_K C_i, \quad i = A, B. \tag{2.4}$$

Substituting Eq. 2.3 into Eq. 2.4 and comparing it with Eq. 2.1 yields the interdiffusion coefficient, known as Darken's second law.

$$\widetilde{D} = C_B \widetilde{V}_B D_A + C_A \widetilde{V}_A D_B \tag{2.5}$$

The intrinsic diffusivities can be determined using Darken's equations by measuring the interdiffusion coefficient and the Kirkendall velocity. Thus, the isothermal diffusion process in a binary system is fully described. [102]

2.2.2.1 Thermal Diffusion in the Al-Ge Material System

To analyze the diffusion processes in the Al-Ge system, parameters such as the activation energies and the frequency factors can be obtained from a reference table, listed in Table 2.1. The diffusion coefficient D is finally calculated via Eq. 2.2.

Table 2.1: *Activation energy E_A and frequency factor D_0 at the annealing temperature of $400\,°C$, used to calculate the diffusion coefficients D for interdiffusion and self-diffusion in the Al-Ge system. The values were taken from [104, 105].*

	Al in Al	Ge in Al	Al in Ge	Ge in Ge
E_A $[eV]$	1.28	1.26	3.45	3.14
D_0 $[cm^2/s]$	0.137	0.481	1000	44.5
D $[cm^2/s]$	$2.73 \cdot 10^{-11}$	$1.86 \cdot 10^{-10}$	$1.48 \cdot 10^{-23}$	$1.38 \cdot 10^{-22}$

The high diffusion coefficient of Ge in the Al solution, compared to the diffusion of Al in Ge, suggests effective out-diffusion of Ge across the Al-Ge interface and replacement of the Ge lattice sites. The empty spaces in the Al lattice are immediately reoccupied due to the fast self-diffusion of Al. The diffusion process progresses up to the solubility limit, which is 1.689 atomic % of Ge in Al at $400\,°C$. [106] Therefore, a sufficiently large Al reservoir must be provided to avoid the diffusion process coming to a halt. As previously mentioned in the materials section, Al has a trivalent electron configuration, while Ge has a tetravalent configuration. [53] This characteristic promotes the formation of intermetallic phases rather than stoichiometric compounds. However, the formation of these intermetallic phases can be minimized by conducting the process below the eutectic temperature of $420\,°C$. Under these conditions, less than 2 atomic % of Ge can be incorporated into Al, compared to less than 1.1 atomic % of Al that can be incorporated into Ge. [106]

Transmission electron microscopy (TEM) analyses in previous research have shown that the remaining Ge segment stays single crystalline and in the original crystal structure, without any Al contamination within the detection limit. [36, 38] Additionally, the intruded Al also maintains a single-crystalline structure, in the usual fcc arrangement. [40] However, the atomic planes of the Al and Ge layers seem to be rotated against each other due to strain minimization and lattice relaxation, contributing to accommodating the large lattice constant deviation of both materials. [38, 39]

A passivation layer of Al_2O_3 does not appear to degrade the annealing process, as no diffusion from the oxide into the Ge takes place due to the low diffusion coefficient. [36, 39, 40] The diffusion process in Al-Ge-Al nanosheet heterostructures is sketched in Fig. 2.6.

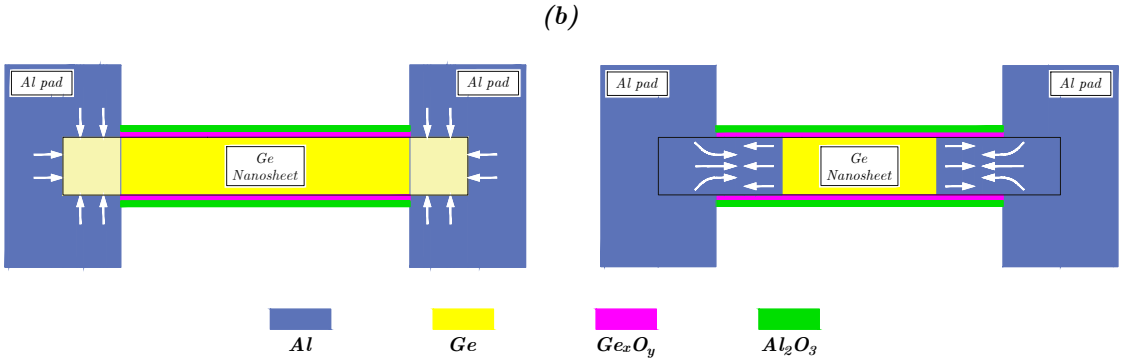

Figure 2.6: *The outlined illustration depicts the solid-state diffusion process in Al-Ge-Al nanosheet heterostructures. In subfigure (a), the initial state is shown, where Ge starts to diffuse into the Al pads. (b) illustrates the formation of two Kirkendall planes within the nanosheet, oriented perpendicular to the diffusion direction. As diffusion progresses, both atomically sharp Al-Ge interfaces gradually shift toward the center of the nanosheet.*
Image adapted from [48, 107].

Previous studies have shown that the surface diffusion of Ge to the metal reservoir depends on the crystallographic orientation and follows a proportionality to $\sqrt{t}$ while being inversely proportional to the square root of the structure's width, $1/\sqrt{W}$. [37, 40, 103]

2.3 The Schottky Contact

When a metal and a semiconductor are brought in contact from an electrical perspective, they form what is known as a Schottky contact. Ideally, this contact occurs on an atomic scale with no intermediate layer and interdiffusion between the materials. Additionally, the interface should be free of adsorbed impurities or surface charges. A potential energy barrier for charge carriers, known as the Schottky barrier, arises from the varying Fermi energy levels of the materials and can be illustrated using an energy band diagram. Fig. 2.7 shows schematically the general case of the formation of the Schottky barrier for the ideal contact of a metal with an intrinsic semiconductor. Both materials are characterized by their work functions ϕ_m and ϕ_s, with which the contact potential is defined via the vacuum energy level and the respective Fermi level of the material according to [108]:

$$q\phi_m = E_{vac} - E_{F,m}$$
$$q\phi_s = E_{vac} - E_{F,s}.$$

In semiconductors, the relationship between the vacuum energy level and the bottom of the conduction band is given by the equation $q\chi = E_{vac} - E_c$, where χ represents the electron affinity. [108] Consequently, the work function can be expressed as $q\phi_s = q\chi + E_c - E_{F,s}$. This relationship is a fundamental property of semiconductors.

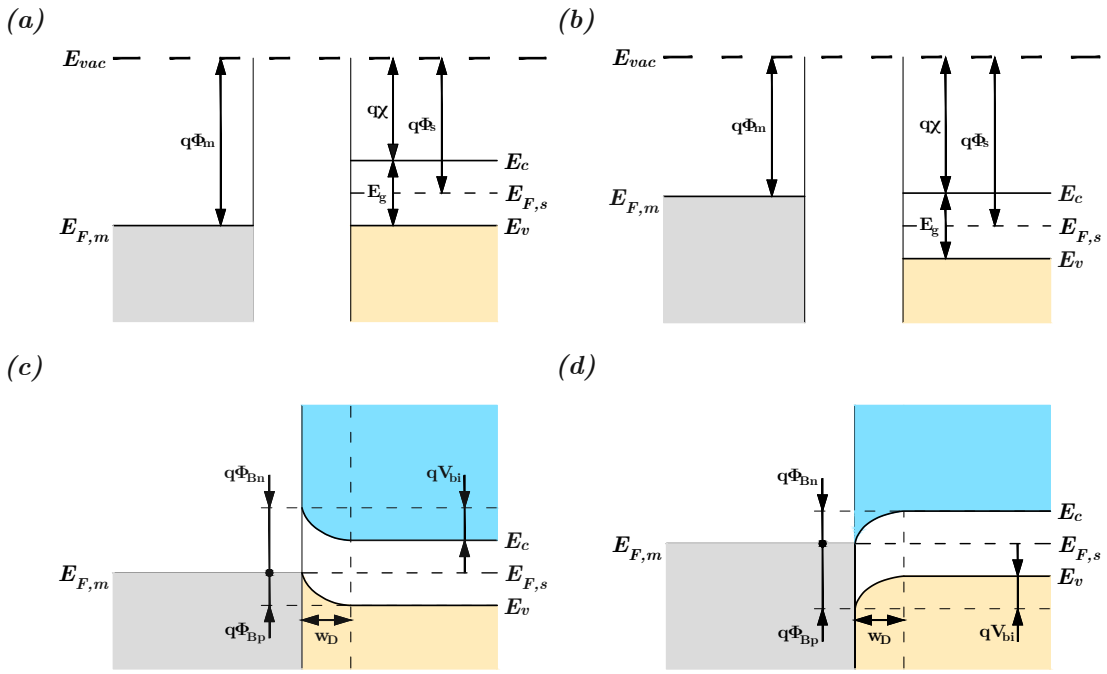

Figure 2.7: *Characterization of metals and intrinsic semiconductors in the energy band diagram. Subfigures (a) and (b) illustrate the materials characterized by their work function ϕ_m, ϕ_s, and electron affinity χ, with respect to the vacuum energy level E_{vac}. Subfigure (a) corresponds to the case $\phi_m > \phi_s$, and subfigure (b) represents the condition $\phi_m < \phi_s$. (c) and (d) demonstrate the resulting bending of the conduction and valence bands when the metal and semiconductor are brought into contact and establish thermal equilibrium.*

Since $E_{F,m} \neq E_{F,s}$, the materials are not in thermal equilibrium at the moment when brought in contact. As a consequence, charge carriers will move through the contact point, creating a depletion layer, which counteracts this diffusion process. Fig. 2.7a depicts the case of $\phi_m > \phi_s$, where electrons will flow from the semiconductor into the metal, and Fig. 2.7b describes

the case of $\phi_m < \phi_s$, where electrons move from the metal into the semiconductor. Thermal equilibrium $E_{F,m} = E_{F,s}$ between the materials is reached as soon as the gradient of their chemical potential is neutralized. The charge carrier transfer is stopped by the electrostatic force between the diffused electrons and the holes left behind. [108]
Even though the resulting depletion layer with thickness w_D appears charge-neutral, a built-in potential V_{bi} is now present. Consequently, this leads to a shift in the conduction and the valence band in the semiconductor. In Fig. 2.7c-d, the metal-semiconductor contact is depicted under thermal equilibrium with shifted bands and the marked built-in voltage, which can be addressed as

$$V_{bi} = \phi_m - \phi_s. \tag{2.6}$$

By applying an external voltage in the range of V_{bi} between the metal and semiconductor, the band bending can be flattened out. [109]
Assuming no electric field is present in the metal, the depletion region will expand only within the semiconductor. This is comparable to a one-sided abrupt p^+-n junction with the p^+ side being degenerated. Solving Poisson's equation using the abrupt depletion approximation provides the depletion width as follows:

$$w_D = \sqrt{\frac{2\varepsilon_0\varepsilon_s}{qN}\left(V_{bi} - V - \frac{k_B T}{q}\right)}. \tag{2.7}$$

Here, $\varepsilon_0\varepsilon_s$ is the permittivity of the semiconductor, V represents the externally applied voltage, and N corresponds to the density of dopants. [71]

In thermal equilibrium, the energy barrier for electrons is determined by the work function of the metal ϕ_m and the electron affinity of the semiconductor χ. For the energy barrier for holes, the band gap of the semiconductor E_g is also taken into account.

$$q\phi_{B,n} = q\left(\phi_m - \chi\right) \tag{2.8}$$
$$q\phi_{B,p} = E_g - q\left(\phi_m - \chi\right) \tag{2.9}$$

For Al, the work function is $\phi_m = 4.2\,eV$ [110], and the solid-state electron affinity of Ge is $\chi = 4.13\,eV$. [110] The band gap can be calculated for any temperature T using Varshni's formula [111]

$$E_g = E_{g,0} - \alpha_g \frac{T^2}{T + \beta_g}, \tag{2.10}$$

based on the band gap at $0\,K$ $E_{g,0}$. For Ge it is given as $E_{g,0} = 0.7412\,eV$, and the empirical constants are $\alpha_g = 4.561 \cdot 10^{-4}\,eV/K$ and $\beta_g = 210\,K$. [111]

By selecting specific materials and doping, the metal-semiconductor junction can result in a linear ohmic contact or rectifying Schottky contact, as can be seen in Fig. 2.8. In Fig. 2.8a, a Schottky contact formation with $\phi_m > \phi_s$ and n-doping can be seen. This configuration has a small potential barrier for electrons and a large barrier for holes. In Fig. 2.8b, holes are exposed to a lower barrier due to $\phi_m < \phi_s$ and p-doping. When an external voltage is applied in the forward direction, the majority carriers in the semiconductor in Fig. 2.8a are electrons, while the minority carriers are holes, leading to a reduction in the corresponding barrier. In contrast, in Fig. 2.8b, the situation is reversed. Consequently, current transport, in this case, is governed by majority carriers, unlike in a p-n junction, where it is driven by minority carriers. In Fig. 2.8c-d, an ohmic contact is formed due to the material properties:

for $\phi_m > \phi_s$ with p-doping, or $\phi_m < \phi_s$ with n-doping. Specifically, in Fig. 2.8c, the barrier vanishes for holes, whereas in Fig. 2.8d, it disappears for electrons. [109]

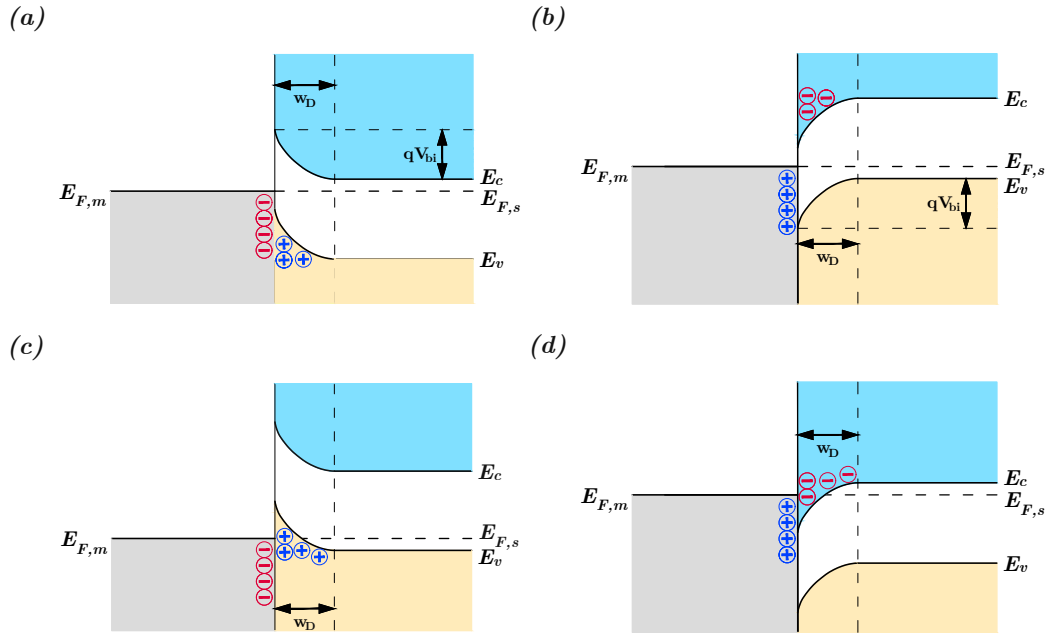

Figure 2.8: *The energy band structures of metal-semiconductor contacts in thermal equilibrium. Subfigure (a) illustrates the band structure of a metal in contact with an n-type semiconductor when $\phi_m > \phi_s$, resulting in a Schottky contact. Subfigure (b) depicts the band structure of metal with a p-type semiconductor when $\phi_m < \phi_s$, also resulting in a Schottky contact. Subfigure (c) shows the formation of an ohmic contact between a metal and an n-type semiconductor when $\phi_m > \phi_s$. Subfigure (d) presents the scenario of an ohmic contact formed between a metal and a p-type semiconductor when $\phi_m < \phi_s$. The symbols of charge carriers within the depletion width indicate the type of carriers present at thermal equilibrium. The width of the depletion layer within the metal is very narrow and, therefore, is not displayed here. Image adapted from [109].*

2.3.1 Electric Transport in Semiconductors

When impurity atoms are added to a semiconductor through processes such as implantation or solid-state diffusion, the material's conductivity changes. This relationship is expressed by the equation:

$$\sigma = q\left(\mu_n n + \mu_p p\right), \tag{2.11}$$

where n represents the electron concentration, and p denotes the hole concentration. A key advantage of semiconductors over metals is their tunable charge carrier concentrations, allowing direct control of n and p in Eq. 2.11 through doping.
Furthermore, when impurities become ionized and carriers are depleted, an electric field is generated, leading to the formation of a potential barrier within the semiconductor. This barrier gives rise to screening effects and Coulomb scattering. [13] In addition to intentionally introduced impurities, intrinsic material defects such as vacancies and self-interstitials are typically present and can act as unintentional dopants. Native point defects become particularly significant in diffusion processes, as they serve as carrier traps and contribute to device degradation. The impact of impurities on the electrical behavior of the metal-semiconductor junction is discussed in the following section. [71, 112]

2.3.1.1 Intrinsic Carrier Concentration and Fermi level

In solid materials, the energy distribution of electrons is described by the Fermi-Dirac statistics. The occupation of an electronic state at energy E by an electron in thermal equilibrium is given by the Fermi-Dirac distribution [113]:

$$f(E,T) = \frac{1}{1+\exp\left(\frac{E-E_F}{k_B T}\right)}, \tag{2.12}$$

where E_F is the Fermi level, which directly depends on the impurities. To find the electron concentration n in the conduction band and the hole concentration p in the valence band for the intrinsic case, the product of the density-of-states $N(E)$ and the occupation probability $f(E)$ needs to be integrated. The integration is carried out from the conduction band to infinity for electron concentration and from minus infinity to the valence band for hole concentration, as shown below [113]:

$$n = \int_{E_c}^{\infty} f(E,T)\, N(E)\, dE, \tag{2.13}$$

$$p = \int_{-\infty}^{E_v} [1 - f(E,T)]\, N(E)\, dE. \tag{2.14}$$

The majority of carriers are concentrated near the extrema of their respective energy bands. In the parabolic region of the $E\left(\vec{k}\right)$ relation, the effective mass remains constant. Thus, an approximate version of the density-of-states for an electron near the bottom of the conduction band and for a hole near the top of the valence band can be written according to [113]:

$$N(E) = \frac{1}{2\pi^2}\left(\frac{2m^*_{ds,e}}{\hbar^2}\right)^{\frac{3}{2}}\sqrt{E - E_c}, \tag{2.15}$$

$$N(E) = \frac{1}{2\pi^2}\left(\frac{2m^*_{ds,h}}{\hbar^2}\right)^{\frac{3}{2}}\sqrt{E_v - E}. \tag{2.16}$$

$m^*_{ds,e}$ represents the density-of-states effective mass for electrons, while $m^*_{ds,h}$ denotes the density-of-states effective mass for holes. The carrier concentrations are obtained by substituting Eqs. 2.12 and 2.15 into Eq. 2.13 and 2.14, then solving the integral for nondegenerate semiconductors:

$$n = N_c \exp\left(\frac{E_F - E_c}{k_B T}\right), \quad N_c = 2\left(\frac{m^*_{ds,e} k_B T}{2\pi\hbar^2}\right)^{\frac{3}{2}}, \tag{2.17}$$

$$p = N_v \exp\left(-\frac{E_v - E_F}{k_B T}\right), \quad N_v = 2\left(\frac{m^*_{ds,h} k_B T}{2\pi\hbar^2}\right)^{\frac{3}{2}}. \tag{2.18}$$

Here, N_c and N_v represent the effective density-of-states in the conduction band and the valence band, respectively. The Fermi level for the intrinsic case $n_i = n = p$ can be formulated from Eq. 2.17 and 2.18 as

$$E_{F,i} = \frac{E_c + E_v}{2} + \frac{k_B T}{2}\ln\left(\frac{N_v}{N_c}\right),$$

which lies close to band gap center $E_g/2$. The intrinsic carrier concentration can then be expressed as follows:

$$n_i = \sqrt{np} = \sqrt{N_c N_v}\exp\left(-\frac{E_g}{2k_B T}\right), \tag{2.19}$$

utilizing Eq. 2.17 and 2.18. [71, 113, 114]

2.3.1.2 Acceptor and Donor Impurities in Semiconductors

The presence of impurities in a semiconductor results in the creation of impurity energy levels within the energy gap. Donor impurities in Ge or Si are pentavalent atoms that provide an extra electron. When this excess electron occupies the impurity, it is considered neutrally charged. However, if the electron is not present, the impurity becomes positively charged and is considered ionized. In contrast, acceptor impurities in Ge and Si are trivalent atoms. These atoms tend to bind with an electron from the valence band, effectively creating a hole. An acceptor impurity is neutral when it is unoccupied, but it becomes negatively charged when it is bound to an electron. Impurities that create energy levels near the middle of the bandgap are considered deep levels, while those near the band edges are referred to as shallow impurities. Fig. 2.9 illustrates the measured ionization energies for different impurities in Ge at $300\,K$. It is common for single atoms to have multiple levels. For example, Au has both acceptor and donor levels. [71]

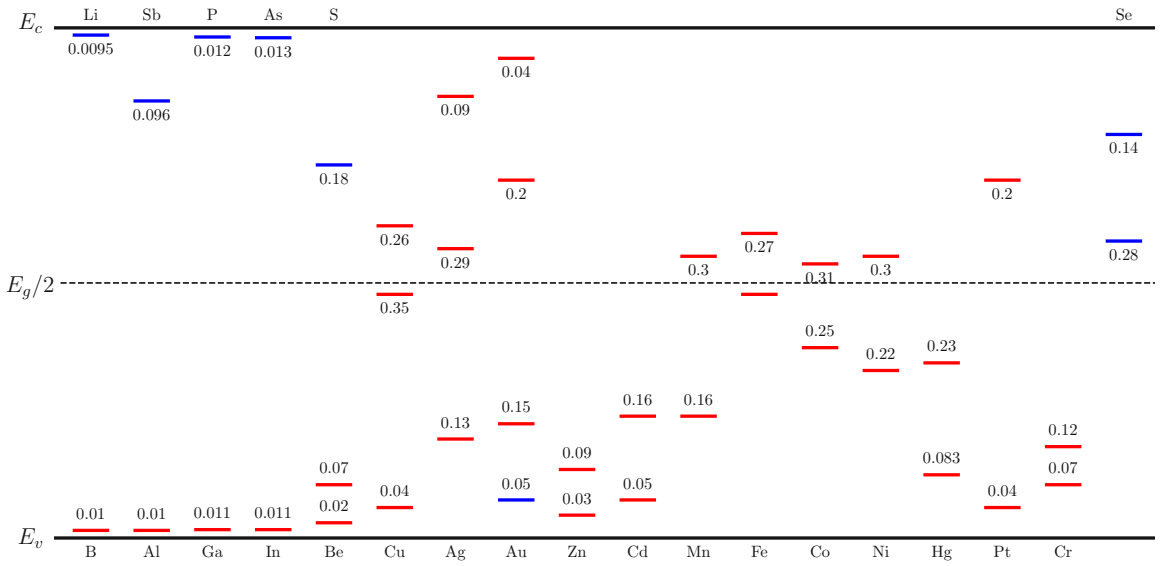

Figure 2.9: *Energy levels of various elemental impurities in Ge at $300\,K$, relative to the band edges. Levels located above the center of the energy gap are referenced to the bottom of the conduction band, while levels below the gap center are referenced to the top of the valence band. Impurities indicated in blue are classified as donor types, while those marked in red are classified as acceptor types. Al is a shallow acceptor-type impurity in Ge, with an ionization energy of approximately $10\,meV$ above the valence band edge. Image recreated from [115].*

In a state of complete ionization, all donor impurities release their excess electrons into the conduction band, while all acceptor impurities become filled with electrons from the valence band. The concentrations of ionized impurities depend on the impurity energy level itself and the lattice temperature. They can be calculated using the following formulas [116]:

$$N_D^+ = \frac{N_D}{1 + g_D \frac{n}{n_0}}, \quad n_0 = N_c \exp\left(\frac{E_c - E_D}{k_B T}\right), \tag{2.20}$$

$$N_A^- = \frac{N_A}{1 + g_A \frac{p}{p_0}}, \quad p_0 = N_v \exp\left(\frac{E_A - E_v}{k_B T}\right), \tag{2.21}$$

where $g_D = 2$ is the ground-state degeneracy of the donor impurity, as it accepts an electron with either spin. The ground-state degeneracy for acceptors, g_A in Ge, is equal to 4, as

acceptor impurities are double degenerate due to two degenerate valence bands at $\vec{k} = \vec{0}$, and they can also accept a hole of either spin. The charge neutrality condition requires that

$$n + N_A^- = p + N_D^+,$$

while the mass-action law $n_i^2 = pn$ still applies, accounting for degeneracy. Solving for the electron concentration yields the following equations [113]:

$$n = \frac{N_D^+ - N_A^-}{2} + \sqrt{\left(\frac{N_D^+ - N_A^-}{2}\right)^2 + n_i^2},$$
$$p = \frac{n_i^2}{n}.$$

For holes, the equations are:

$$p = \frac{N_A^- - N_D^+}{2} + \sqrt{\left(\frac{N_A^- - N_D^+}{2}\right)^2 + n_i^2},$$
$$n = \frac{n_i^2}{p}.$$

As the intrinsic carrier concentration is highly dependent on temperature, in regions unaffected by high temperatures, the charge neutrality condition can be approximated as follows [113]:

$$n = N_D^+ - N_A^- + p \approx N_D^+ - N_A^-, \quad N_D^+ - N_A^- \gg n_i \tag{2.22}$$
$$p = N_A^- - N_D^+ + n \approx N_A^- - N_D^+, \quad N_A^- - N_D^+ \gg n_i, \tag{2.23}$$

where for N_D^+ greater than N_A^- the material is n-type, and for N_A^- greater than N_D^+ the material is p-type. [113] If only a specific type of impurity is introduced into the semiconductor material, the approximation becomes:

$$n \approx N_D^+, \quad N_D^+ \gg n_i \tag{2.24}$$
$$p \approx N_A^-, \quad N_A^- \gg n_i. \tag{2.25}$$

This approximation allows for the calculation of E_F through substitution in Eq. 2.17 and 2.18 [116]:

$$n = N_c \exp\left(-\frac{E_c - E_F}{k_B T}\right) = \frac{N_D}{1 + g_D \frac{n}{N_c} \exp\left(-\frac{E_c - E_D}{k_B T}\right)}, \tag{2.26}$$
$$p = N_v \exp\left(-\frac{E_F - E_v}{k_B T}\right) = \frac{N_A}{1 + g_A \frac{p}{N_v} \exp\left(-\frac{E_A - E_v}{k_B T}\right)}. \tag{2.27}$$

Ultimately, solving for E_F results in the following expressions:

$$E_F = E_c + k_B T \ln\left(\frac{N_D}{N_c} \frac{1}{1 + g_D \frac{n}{n_c} \exp\left(-\frac{E_c - E_D}{k_B T}\right)}\right)$$
$$E_F = E_v - k_B T \ln\left(\frac{N_A}{N_v} \frac{1}{1 + g_A \frac{n}{n_v} \exp\left(-\frac{E_A - E_v}{k_B T}\right)}\right).$$

2.3.1.3 Carrier Concentration at Low Temperatures

At cryogenic temperatures, the intrinsic carrier concentration becomes negligible compared to the impurity concentration. Consequently, the approximations made in Eqs. 2.22-2.25 remain valid. At temperatures where the thermal energy is insufficient to ionize impurities from their respective energy levels, the carrier concentration decreases further exponentially, as predicted by Eqs. 2.20 and 2.21. Given the known impurity concentrations and ionization energies, the total carrier concentrations and the Fermi level can be determined using Eqs. 2.26 and 2.27. As the temperature decreases and the carrier freeze-out occurs, the Fermi level shifts closer to the ionization energy of the corresponding impurity. A graphical representation showing carrier concentration and Fermi level as a function of doping concentration and temperature for shallow impurities in Ge, based on the equations presented above, can be found in Fig. 2.10.

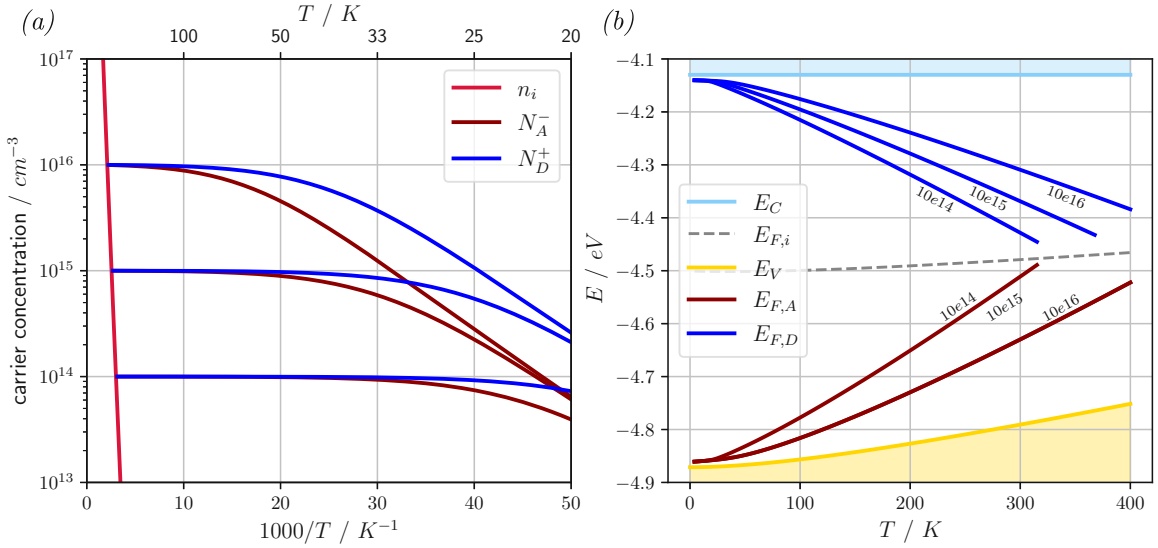

Figure 2.10: *A graphical representation of the calculated material parameters for Ge doped with shallow dopants at varying concentrations. The ionization energies are defined as* $E_A = E_v + 0.01\,eV$ *and* $E_D = E_c - 0.01\,eV$*. The representation also illustrates the behavior of these parameters as a function of temperature, including (a) an Arrhenius plot that displays both the intrinsic carrier concentration and the concentration of ionized impurities. For p-doping concentrations of* $N_A = 10^{14}\,cm^{-3}$*,* $N_A = 10^{15}\,cm^{-3}$*, and* $N_A = 10^{16}\,cm^{-3}$*, the values are indicated by red lines. In contrast, the ionized impurity concentrations for n-doping concentrations of* $N_D = 10^{14}\,cm^{-3}$*,* $N_D = 10^{15}\,cm^{-3}$*, and* $N_D = 10^{16}\,cm^{-3}$ *are represented by blue lines. (b) A band structure diagram illustrating the Fermi level of intrinsic Ge* $E_{F,i}$ *and the Fermi level affected by the presence of acceptor impurities* $(E_{F,A})$ *and donor impurities* $(E_{F,D})$*. All of these entities are plotted in relation to the vacuum energy level. Image based on [71].*

It is important to note that the results presented in Fig. 2.10 were derived by substituting the effective density-of-states expressions from Eqs. 2.17 and 2.18 with the following equations [76]:

$$N_c = 1.98e^{15} \cdot T^{3/2}\,cm^{-3},$$
$$N_v = 9.6e^{14} \cdot T^{3/2}\,cm^{-3}.$$

2.3.2 Interface States and Fermi Level Pinning at the Al-Ge Junction

Regarding symmetric devices, the Fermi level of the metal ideally aligns with the center of the band gap of the semiconductor, resulting in the same barrier height for electrons and holes. It would be reasonable to assume that the Fermi level alignment depends on the selected metal. However, due to surface imperfections on Ge and the consequently high density of interface traps, as discussed in Section 2.1.3, the Fermi level of the metal aligns electrostatically with the surface states when the metal and semiconductor surfaces are brought in contact. [117] This phenomenon causes the barrier height to become widely independent of the metal's work function.
The energy levels of surface states are typically located within the band gap and act as charge traps. The probability of these surface states being occupied can be described using the Fermi distribution. The trapping mechanism is similar to Shockley-Read-Hall recombination, but it occurs without recombining with carriers from the opposite band. Instead, the trapped charge carriers are eventually released back to their original state after some time. During this period, the trapped charges are not available for current transport, disrupting the equilibrium condition described in Eq. 2.19. [118]
To characterize the effect of these surface states, a neutral level ϕ_0 is introduced, as indicated in Fig. 2.11.

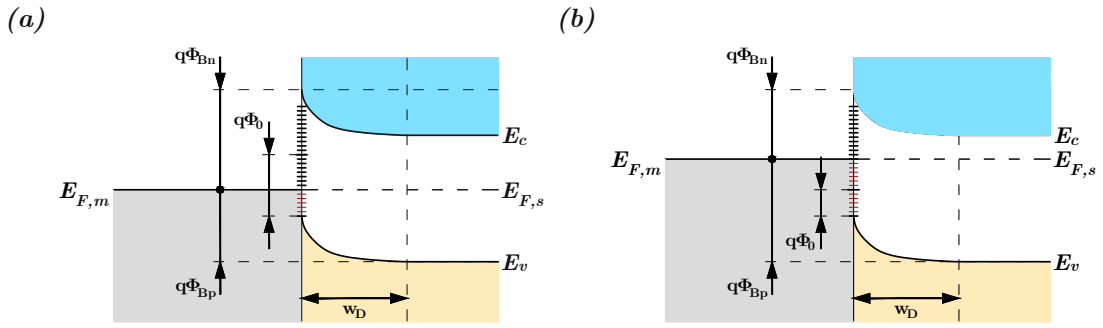

Figure 2.11: *Illustration of the surface states within the band gap at the Al-Ge interface. In subfigure (a), the charge neutrality level ϕ_0 is positioned above the common Fermi level E_F. As a result, the surface states between E_v and $E_{F,s}$ are occupied with electrons. These states act as hole traps, resulting in a total trap charge of 0. In subfigure (b), ϕ_0 is located below the common Fermi level E_F, which leads to all states between E_v and $E_{F,s}$ also being occupied with electrons. Consequently, the trap charge below ϕ_0 remains 0, while the net trap charge above ϕ_0 is negative. Image adapted from [71].*

ϕ_0 determines the Fermi level of the metal-semiconductor contact under thermal equilibrium to achieve a charge-neutral interface, and it is measured from the top of the valence band. The states above ϕ_0 are of acceptor type (electron traps): neutral when unoccupied and negatively charged when occupied, while the states below ϕ_0 are of donor type (hole traps): positively charged when unoccupied and neutral when occupied with electrons. [71] In the scenario illustrated in Fig. 2.11a, the energy level ϕ_0 is located above the Fermi level. Consequently, the energy states between the top of the valence band and the Fermi level are filled with electrons, while the higher surface states are left unoccupied. This results in a net positive charge across the interface states. On the other hand, when ϕ_0 is situated below the Fermi level, as shown in Fig. 2.11b, the surface states are filled with electrons up to the Fermi level. However, only the energy states between ϕ_0 and the Fermi level possess a net negative charge. The charge neutrality condition at the interface is given by the equation $Q_S + Q_D + Q_M = 0$. Here, Q_S represents the surface trap charge on the semiconductor side of the junction, Q_D

represents the charge of the depletion region inside the semiconductor, and Q_M represents the charge on the metal side of the junction. To compensate for the charge in the semiconductor, the metal side Q_M contains the same charge, but with a negative sign according to $Q_M = -(Q_S + Q_D)$. A charge increase in Q_S causes Q_D to decrease, leading to a reduction in the depletion width. Additionally, since band bending is proportional to the depletion width, it will also decrease, resulting in a lower effective barrier height. A decrease of the barrier height causes ϕ_0 to shift closer to E_F, resulting in the surface states acting like a negative feedback loop, with amplification directly proportional to D_{it}, meaning that the Fermi level is pinned by the surface states instead of the metal work function. [49, 71]
Under the influence of interface states, the initially proposed effective barrier heights for electron and hole injection in Eqs. 2.8 and 2.9 are modified as follows [71, 119]:

$$q\phi_{B,n} = qS\,(\phi_m - \chi) + (1 - S)\,(E_g - q\phi_0)\,,$$
$$q\phi_{B,p} = E_g - q\phi_{B,n}.$$

Here, S represents a sensitivity parameter that is determined metrologically and takes values between 0 and 1.

Multiple studies have measured the Fermi-level pinning in Ge in relation to different metals, reporting values that are consistently close to the valence band, indicating an intrinsically high barrier for electrons and a low barrier for holes. The observed values range from $80\,meV$ [120], $90\,meV$ [121], to $130\,meV$ [110] relative to the top of the valence band. Furthermore, interface trap densities in the range of $\sim 10^{13}$ have been reported. [110, 121] This ultimately results in stronger Fermi-level pinning in Ge compared to Si, as illustrated in Fig. 2.12 for various metals.

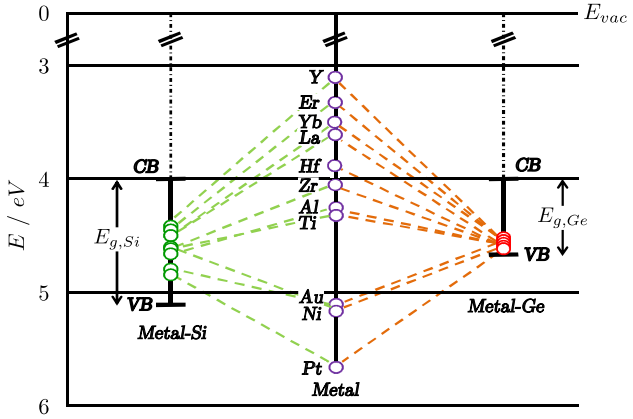

Figure 2.12: *Illustration of the Fermi-level pinning for Si and Ge. The work function of various metals is shown along with the band gap of Si and Ge, referenced to the vacuum energy level E_{vac}. The dashed lines indicate the pinning of the metal's Fermi level in Si and Ge, respectively, when they are brought into contact. As demonstrated, the red dashed lines representing the metal-Ge contact are all pinned close to the valence band (VB). Image adapted from [122, 123].*

Several different mechanisms have been identified that cause Fermi-level pinning. This includes intrinsic charge transfer due to the formation of metal-semiconductor contact, which is caused by metal-induced gap states (MIGS) and chemical metal-semiconductor bonds. Additionally, extrinsic effects are attributed to disorder-induced gap states, such as dangling bonds. Several studies have found that MIGS appear to be the primary cause of Fermi-level pinning. [39, 119, 120, 124]

The Fermi-level pinning effect does not seem to be reduced by contact formation through forming gas annealing. [125] However, Fermi-level de-pinning can be achieved by adding a thin oxide layer between the semiconductor channel and the metal, which may reduce the interface states as discussed in Section 2.1.3. [126, 127]

2.3.3 Charge Carrier Transport at Schottky Junctions

By applying a voltage across the junction, the metal-semiconductor contact is driven out of thermal equilibrium, resulting in the establishment of an electric current. The flow of electric current from the metal to the semiconductor across the Schottky barrier involves several charge carrier transport mechanisms, as shown in Fig. 2.13. These mechanisms include electron emission over the barrier, quantum mechanical tunneling of electrons through the barrier, recombination in the space charge region, diffusion of electrons in the depletion zone, electron injection in the neutral zone, hole injection from the metal, and hole diffusion into the semiconductor. However, the recombination processes account for only a small portion of the overall current transport and will not be discussed further. [49, 71]

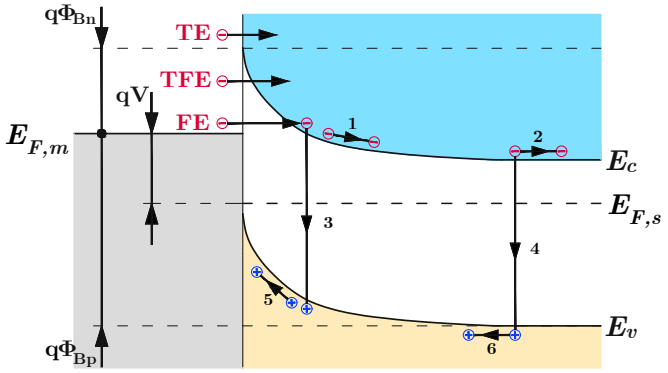

Figure 2.13: *Illustration of the basic transport mechanisms at the metal-semiconductor interface under reverse bias. These include thermionic emission (TE) of electrons over the barrier, thermionic field emission (TFE) and field emission (FE) through the barrier, diffusion of electrons in the space charge region (1), diffusion of electrons in the neutral region (2), recombination in the space charge region (3), recombination in the neutral region (4), diffusion of holes in the space charge region (5) and in the neutral region (6). Image adapted from [49, 128].*

The mechanism of charge carrier transport through the reverse-bias metal-semiconductor interface involves three main processes: thermionic emission (TE), thermionic field emission (TFE), and field emission (FE). As illustrated in Fig. 2.13, these processes are exemplarily applied to electrons. For Schottky junctions involving a p-type semiconductor, these mechanisms also pertain to holes.

Due to the thermal excitation of charge carriers, the primary current component at room temperature is over-the-barrier emission, which exhibits rectifying behavior. It implies that the effective barrier height ϕ_B is much larger than k_BT. The resulting resistance in this scenario is directly proportional to the electrons that reach enough energy to overcome the barrier. [28, 49, 71]

At low temperatures, current transport happens mainly via tunneling through the barrier. Thermal-assisted tunneling requires a higher thermal energy of the carriers than direct tunneling. However, this process occurs just below the top of the barrier, where the barrier width is smaller than that for direct tunneling. The increase in reverse bias voltage and the

corresponding band bending further reduces the barrier width, contributing to the overall tunnel current. [28, 49, 71]
Other processes that do not occur directly at the interface, such as recombination in the space charge region and recombination in the neutral region, generate a comparatively negligible current in relation to the previously mentioned processes. The recombination in the space charge region occurs through localized states, while recombination in the neutral region can happen, for example, when the Schottky barrier on an n-type material exceeds half the band gap. In this situation, the semiconductor adjacent to the metal has a high density of holes that can diffuse into the neutral region when a forward bias is applied. [28]

The most widely accepted model for current transport is the thermionic emission theory, which provides the current-voltage relation including both thermionic emission and tunneling as follows [129]:

$$J = J_0 \left[\exp\left(\frac{qV}{nk_BT}\right) - 1 \right] \tag{2.28}$$

where

$$J_0 = A^* T^2 \exp\left(-\frac{q\phi_{SBH,eff}}{nk_BT}\right). \tag{2.29}$$

In these equations, J_0 represents the reverse saturation current density, A^* is the Richardson constant, and $\phi_{SBH,eff}$ is the effective Schottky barrier height. The value of J_0 exhibits an exponential dependence on $\phi_{SBH,eff}$. [71] Since the Schottky barrier $\phi_B = \phi_{Bn}$ cannot be measured directly, the effective Schottky barrier height $\phi_{SBH,eff} = \phi_B - \Delta\phi_{bi}$ was introduced here. Generally, a Schottky barrier exists when $\phi_{SBH,eff} > k_BT$. Moreover, it also covers deviations from the ideal Schottky barrier, e.g., image-force lowering ($\Delta\phi_{bi}$). n represents the ideality factor. When the diffusion current is dominant, n equals 1. For higher doping, as the barrier width decreases or at lower temperatures, tunneling becomes more prominent, and n increases towards 2. [49, 71, 129]

2.4 Electrical Transport in Al-Ge-Al Heterostructures

To understand the electrical behavior of monolithic Al-Ge-Al heterostructures, it is useful to consider their fundamental structure. As illustrated in Fig. 2.14, this heterostructure can be viewed as two Schottky diodes connected in series, with the Ge channel serving as the intermediate region. When a voltage is applied, one of these Schottky diodes becomes forward-biased, while the other remains in the reverse direction. This configuration plays a crucial role in determining the transport characteristics of the device.

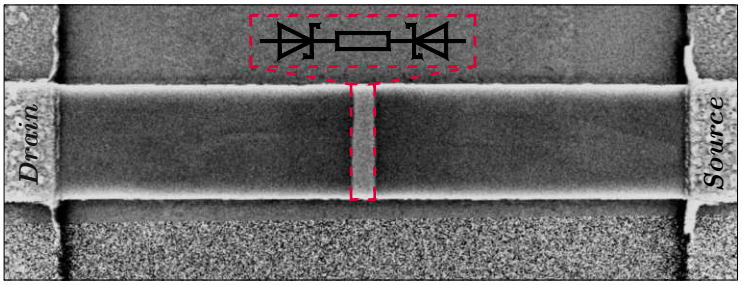

Figure 2.14: *SEM image of a monolithic Al-Ge-Al heterostructure showing the drain and source contacts, along with an inset of the equivalent circuit diagram that features the back-to-back Schottky diodes and the channel resistance. Image based on [128].*

Generally, due to imperfections in the metal-semiconductor formation, the resulting structure may be asymmetric, leading to different diode behaviors such as varying barrier heights. [130] Furthermore, the resistance R of the channel in the structure is now an additional factor limiting the current transport. For voltages higher than the barrier height and an ideality factor of the diodes close to 1, the current is driven by the series resistance R instead of the potential barriers. [131] This results in the channel resistance being the current limiting factor. The current-voltage relation in Eq. 2.28 is then modified for the current density through the structure as

$$J = J_0 \left[\exp\left(\frac{q\,(V - RAJ)}{n k_B T} \right) - 1 \right], \tag{2.30}$$

where A is the cross-section and R is the series resistance of the Ge segment. For high channel resistance and low barrier heights of the diodes, the resulting I-V characteristics exhibit ohmic contact behavior. [131] However, because the structure provided is asymmetric, the voltage drop across the individual components needs to be considered, rather than using a simple voltage-current relation as in Eq. 2.30. The voltage drop across a diode can be expressed as [131, 132]:

$$V = \frac{n k_B T}{q} \ln\left(\frac{J}{J_0} + 1 \right),$$

where J_0 represents the reverse saturation current density, and J represents the positive current density through the diode in forward direction. By incorporating the series resistance and considering the voltage drop sign convention, the total voltage drop across the structure can be written as [131, 132]:

$$V = V_{fd} + V_{rs} + RAJ = \frac{n_{fd} k_B T}{q} \ln\left(\frac{J}{J_{0,fd}} + 1 \right) - \frac{n_{rs} k_B T}{q} \ln\left(-\frac{J}{J_{0,rs}} + 1 \right) + RAJ. \tag{2.31}$$

Here, the indices „fd“and „rs“refer to the diode operating in the forward and reverse directions, respectively.

2.4.1 The Al-Ge-Al Schottky Barrier FET

The Al-Ge-Al Schottky barrier FET is a device that utilizes metal-semiconductor junctions to control charge transport in the Ge channel. Building on the previously discussed Al-Ge-Al heterostructure, an additional gating mechanism is introduced to modulate the band structure and carrier type. This is achieved by placing a gate electrode on top of an insulating passivation layer that covers both Schottky interfaces. Similar to metal-semiconductor contacts, the metal-oxide-semiconductor structure induces band bending, which influences charge carrier transport within the Ge channel. Due to the insulating nature of the interlayer, direct current transport to the gate is ideally suppressed, allowing the structure to function as a capacitor and enabling efficient electrostatic gating. Fig. 2.15 illustrates the band banding in the gated Al-Ge-Al system for positive, negative, and no bias applied to the gate. [71]

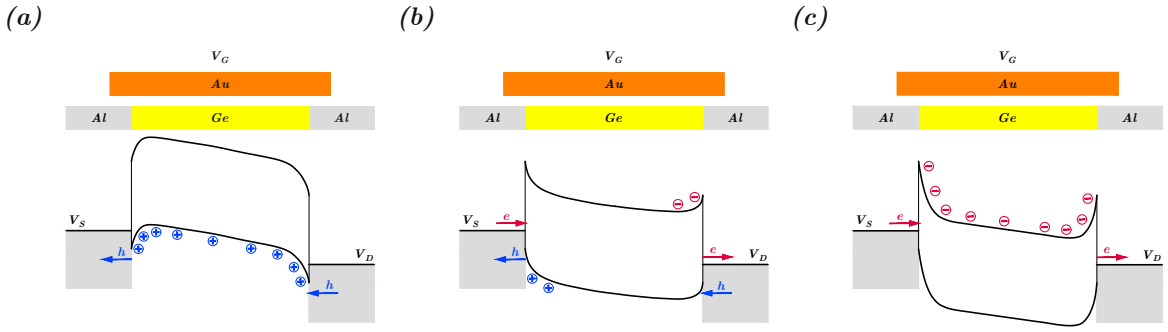

Figure 2.15: *The figure illustrates the band diagram of the Al-Ge-Al Schottky barrier FET, including a schematic representation of the Al-Ge-Al channel structure and the Au gate. In subfigure (a), a negative voltage is applied to the gate, resulting in a high barrier for electron injection and a reduced barrier for hole injection. Subfigure (b) shows the situation with no bias applied to the gate, which maintains a high barrier for both electrons and holes. Finally, subfigure (c) presents the case with a positive gate voltage, leading to a high barrier for holes and a lowered barrier for electrons. Image adapted from [45].*

When a negative voltage is applied to the gate, the bands are pulled upwards. This lowers the barrier for holes and thus increases the barrier for electrons (Fig. 2.15a). On the other hand, when a positive voltage is applied to the gate, the bands are pushed downwards. This effectively lowers the barrier for holes and increases the barrier for electrons (Fig. 2.15c). When no voltage is applied to the gate, a significant barrier for electrons and holes exists, effectively reducing the carriers available for current transport and resulting in the device being in the off-state. The control of the majority charge carrier type in the channel through the gate allows the transistor to operate in either n-mode or p-mode. By applying a bias voltage between the source and drain contacts, the entire band diagram is tilted. This enables electrons to move down the energy gradient along the conduction band edge, while holes are able to move upward against the gradient along the valence band edge. The current flow through the structure can thus be controlled via the gate and source-drain voltage. [13]

2.4.1.1 Oxide Trap Induced Band Bending

When analyzing the MOS structure, it's essential to consider not only the surface states of Ge but also the trapped charges inside the oxide layer situated between the Ge channel and the metal gate. Within this oxide layer, different types of charges can accumulate, including fixed oxide charges, mobile ionic charges, and charges trapped through various mechanisms.

The density of fixed oxide charges mainly relies on fabrication conditions, whereas mobile ionic charges can migrate through the oxide depending on the bias conditions. [71]
In considering the trapping mechanisms, a distinction must be made between the bulk states at the Ge surface and the oxide traps that are situated farther away from the Ge surface. The trapping mechanism of the bulk states operates similarly to what is described in Section 2.3.2. At the interface of Ge and its native oxide, all traps below the Fermi level are filled with electrons, causing the conduction and valence bands to bend upward near the surface, as shown in Fig. 2.16a. This bending leads to the accumulation of holes at the interface, directly resulting from the requirement to maintain charge neutrality. These charged traps behave like an effective negative gate, resulting in the p-type behavior of nominally intrinsic Ge. In contrast, oxide traps reside within the native oxide layer and can only be accessed via quantum mechanical tunneling, as illustrated in Fig. 2.16b. Traps situated directly at the interface have short lifetimes, typically in the μs range or less, and are therefore classified as „fast“ surface states. On the other hand, the lifetime of oxide traps can extend to several minutes, depending on their distance from the interface. Because of these long lifetimes, oxide traps are considered „slow“ traps. [118, 133–135]

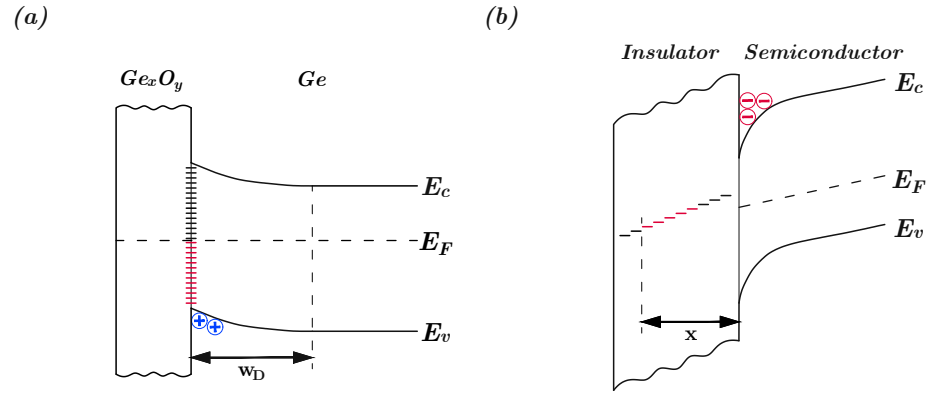

Figure 2.16: *Band diagram of an insulator-semiconductor system with trap levels. Subfigure (a) shows the surface states that develop due to the formation of native Ge_xO_y on the surface of Ge. The trap levels between the top of the valence band and the Fermi level are filled, resulting in an upward bending of the energy bands, which leads to the accumulation of holes and a p-type behavior of the Ge based device. Subfigure (b) demonstrates how the trap levels, positioned deep within the oxide, become filled when a voltage is applied to a MOS structure. The band bending allows carriers from the semiconductor to access these trap levels through quantum mechanical tunneling, extending up to the penetration depth x. Image adapted from [118, 136].*

The trapping of charge carriers in oxide states is initiated as soon as a voltage is applied to the gate. In a MOS structure, applying a positive gate voltage bends the conduction and valence bands further, leading to the occupation of additional surface states. Conversely, a negative gate voltage bends the bands in the opposite direction, depleting these previously filled surface states. At higher gate voltages, the increased tunneling probability allows charge carriers to access deeper oxide traps, which amplifies hysteresis in the transfer characteristics. Additionally, due to the kinetically limited trapping and de-trapping process, the associated lifetime constants exhibit a strong time dependence, increasing significantly as the temperature decreases. [118, 133, 135]
The quality of both the oxide layer and the Ge surface is strongly influenced by the fabrication process. As a result, optimizing the manufacturing process can effectively reduce trap density and improve device performance.

2.4.2 Ballistic Transport

Transistor downscaling has played a crucial role in enhancing power efficiency and switching speed. [11] As channel lengths decrease, short-channel effects become increasingly significant, fundamentally altering charge carrier transport mechanisms. One crucial transition occurs when devices approach the ballistic transport regime, where charge carriers traverse the channel with minimal scattering. [137]
In highly scaled devices, the source and drain depletion regions extend deeper into the channel. When the channel length is reduced to the point where these depletion regions interact, the charge carrier barrier lowers, leading to increased off-state leakage and altered current-voltage characteristics. [13, 28, 138] At extremely short channel lengths, where the device dimensions approach fundamental physical limits, scattering events become infrequent, and charge carriers can traverse the channel ballistically. In this regime, transport is primarily governed by injection at the source and drain rather than by scattering within the channel. [137]

The conductance G of a conductor is generally expressed as

$$G = \frac{\sigma A}{l}, \tag{2.32}$$

where A is the cross-sectional area, l is the length of the conductor and σ is the conductivity, which is a material-specific parameter. In semiconductors, conductivity is given by $\sigma = q\left(\mu_n n + \mu_p p\right)$, where the transport of current involves both electrons and holes (see Section 2.3.1). This equation highlights the direct relationship between conductivity and the mobilities of charge carriers. As discussed in Section 2.1.2, the mobilities of charge carriers are affected by several scattering mechanisms. When charge carriers collide, they transfer energy to the lattice, which causes heating and limits their velocity. As a result, conductance is significantly influenced by the density of charge carrier scatter centers and the temperature. [71]

The average distance between two collisions is referred to as the mean free path, denoted by l_{MFP}. As the length of the conductor approaches l_{MFP}, the mechanism of current transport undergoes a fundamental transition from diffusive to ballistic. In the ballistic regime, carriers do not experience scattering and are directly accelerated by the electric field. Their velocity increases over time according to $\propto qE_{field}t/m$, which can quickly exceed the saturation velocity within a short distance on the order of l_{MFP}. [71]
The mean free path can be expressed using the Fermi velocity v_F and the momentum relaxation time τ_m as follows [139]:

$$l_{MFD} = v_F \tau_m = \frac{\hbar}{m^*}\sqrt{2\pi n}\tau_m,$$

where m^* is the effective mass. This relationship demonstrates how the mean free path depends on both material properties (through m^*) and operating conditions (through carrier density n). The Fermi velocity is derived from electrons at energies close to the Fermi energy, which is influenced by the carrier density n. This, in turn, causes the mean free path to vary with temperature. l_{MFP} can range from just a few nanometers in group-IV semiconductors [140] to several microns in graphene. [141] For Ge, the mean free path is approximately $35\,nm$. [53, 140]

According to Eq. 2.32, conductance would theoretically increase towards infinity as the length of a conductor decreases. However, in the ballistic regime where the conductor length is much shorter than the mean free path ($l \ll l_{MFP}$), the conductance approaches a finite limiting value G_C. While ballistic conductors themselves are expected to have no resistance,

a measurable resistance G_C^{-1} still exists, originating from the interface between the ballistic conductor and the contacting materials. This interface resistance is therefore referred to as contact resistance. The origin of this contact resistance lies in the fundamental difference between current transport in macroscopic metallic contacts and ballistic conductors. While macroscopic metallic contacts support an infinite number of current-carrying sub-bands, ballistic conductors allow only a discrete number of sub-bands. This mismatch necessitates current redistribution at the interface, resulting in the contact resistance G_C^{-1}. [48, 107, 139]

Assuming reflectionless contacts, an electron in an unoccupied state with a group velocity $v_g = \hbar^{-1}(\partial E/\partial k)$, contributes to the microscopic current according to $I = q/t_t$, where $t_t = l/v$ is the transit time. The occupation of these states is described by the Fermi-Dirac probability function, leading to the following expression for the current [139]:

$$I = \frac{q}{l}\sum_{l,k}\frac{1}{\hbar}\frac{\partial E(k)}{\partial k}\left[f\left(E(k)-E_{F_L}\right)-f\left(E(k)-E_{F_R}\right)\right],$$

where E_{F_L} and E_{F_R} are the Fermi levels of the left and right contacts, respectively. This equation represents the sum of the microscopic currents from all contributing sub-bands $E(k)$. Taking into account a spin degeneracy factor of two and introducing the inverse of the one-dimensional spacing in k-space, this expression can be reformulated as:

$$I = \frac{q}{l}\frac{2l}{2\pi}\sum_{l}\int\frac{1}{\hbar}\frac{\partial E(k)}{\partial k}\left[f\left(E(k)-E_{F_L}\right)-f\left(E(k)-E_{F_R}\right)\right]dk,$$

$$I = \frac{2q}{h}\int\left[f\left(E(k)-E_{F_L}\right)-f\left(E(k)-E_{F_R}\right)\right]M(E)\,dE,$$

where $M(E)$ represents the number of conductive channels as a function of energy. For the case where M(E) remains constant over the energy range from E_{F_L} to E_{F_R}, we obtain:

$$I \approx \frac{2e^2}{h}\frac{E_{F_L}-E_{F_R}}{q}M,$$

where $(E_{F_L}-E_{F_R})/q$ represents the voltage between the contacting electrodes. Consequently, the contact resistance can be expressed as:

$$G_C^{-1} = \frac{h}{2q^2}\frac{1}{M}.$$

A particularly significant case occurs in a ballistic conductor with only one sub-band ($M = 1$), where the contact resistance takes on the universal value $G_C^{-1} = h/2q^2 = 12.9\,k\Omega$, known as the quantum resistance. [107, 139, 142]

2.4.2.1 Landauer Formula

The previous derivation assumed perfect transmission between contacts. However, in real devices, charge carriers traveling from one contact to another experience some degree of reflection. The Landauer formula provides a more complete description by incorporating the transmission coefficient T, which represents the probability of a carrier successfully reaching the opposite contact. This fundamental relationship between conductance and transmission is given by [137, 139, 143]:

$$G = \frac{2q^2}{h} \int T(E) M(E) \left[f\left(E(k) - E_{F_L}\right) - f\left(E(k) - E_{F_R}\right) \right] dE. \tag{2.33}$$

Notably, for channel lengths within the mean free path, this expression becomes independent of both device dimensions and material-dependent properties such as the effective mass.
At very low temperatures, the physics simplifies considerably as the Fermi functions approach step functions [144]:

$$f\left(E - E_{F_L}\right) - f\left(E - E_{F_R}\right) \approx \theta\left(E - E_{F_L}\right) - \theta\left(E - E_{F_R}\right),$$

where θ represents the Heaviside step function.
For small bias voltages, where $qV = E_{F_L} - E_{F_R} \approx 0$, this expression further reduces to [144]:

$$f\left(E - E_{F_L}\right) - f\left(E - E_{F_R}\right) \approx \delta\left(E - E_F\right), \tag{2.34}$$

where $\delta\left(E - E_F\right)$ indicates the resonant Fermi window. [28] Under these conditions, Landauer's formula simplifies to [139]:

$$G = \frac{2q^2}{h} M\left(E_F\right) T\left(E_F\right).$$

This result directly relates the conductance to the number of available channels and their transmission probability at the Fermi energy.

2.4.2.2 Quantum Ballistic Transport

While the previous sections described ballistic transport in general terms, quantum effects become particularly significant when the conductor's dimensions approach fundamental quantum mechanical length scales. Specifically, when the diameter of the conductor is reduced below the exciton Bohr radius a_B^*, the electronic structure experiences a significant transformation in that the continuous valence and conduction bands change into discrete, equally spaced sub-bands. a_B^*, a material and temperature-dependent parameter, defines the characteristic distance between an electron and a hole within an exciton. For Ge, this critical dimension is approximately $24.3\,nm$. [48, 107, 145]
When such a quantum-confined structure is integrated into a FET, the gate voltage provides direct control over the occupation of these discrete sub-bands. At very low temperatures, the quantum mechanical nature of transport becomes observable as the conductance varies in discrete steps of $2q^2/h$ when the gate voltage is adjusted. This quantization of conductance is most clearly visible at very low temperatures, as illustrated in Fig. 2.17.

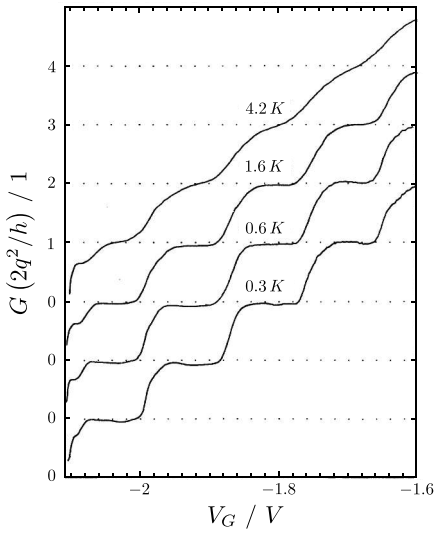

Figure 2.17: *Quantization of conductance at temperatures of* $0.3\,K$*,* $0.6\,K$*,* $1.3\,K$*, and* $4.2\,K$ *as a function of gate voltage in a* $GaAs/Al_{0.33}Ga_{0.67}As$ *heterojunction. Image taken from [146].*

The figure clearly demonstrates two key phenomena: first, as the gate voltage increases, more conductive channels become available, resulting in a stepwise increase in conductance. Second, increasing temperature progressively smears out these quantized steps due to thermal broadening, making the approximation in Eq. 2.33 using step functions increasingly invalid. [48, 107]
For quasi-one-dimensional structures exhibiting such quantization steps, the transmission coefficient in Eq. 2.33 can be determined experimentally, providing direct access to fundamental quantum transport parameters.

2.4.2.3 Tsu-Esaki Formula

While the Landauer formula describes ballistic transport through quantum channels, a complementary approach for coherent tunneling through barrier structures was developed by Tsu and Esaki in the context of resonant tunneling diodes. Their formulation describes the tunneling current density through the equation [147]:

$$J = \frac{4\pi qm}{h^3} \int N(E)\, T(E)\, dE. \tag{2.35}$$

Here, N(E) represents the supply function, which quantifies the availability of charge carriers for tunneling at a given energy level. Similar to the Landauer approach, this supply function is defined in terms of the Fermi functions of both contacts:

$$N(E) = f(E - E_{F_L}) - f(E - E_{F_R}), \tag{2.36}$$

which follows the same simplification rules discussed previously. With the supply function defined, the transmission coefficient remains the only parameter to be determined in Eq. 2.35. [147]
At temperatures above $0\,K$, the Fermi functions can no longer be approximated as simple step functions. Consequently, the integrals in both Eqs. 2.33 and 2.35 require explicit evaluation and cannot be solved analytically. One practical approach to this challenge is to reformulate these expressions in terms of Fermi integrals, which have known solutions for specific parameter ranges. [147, 148]

Chapter 3

Experimental Methods

This chapter presents a comprehensive specification for fabricating monolithic Al-Ge-Al SB-FETs and outlines the procedures for conducting electrical measurements. The first section details the fabrication of monolithic integrated Al-Ge-Al heterostructure devices with top gates, utilizing standard semiconductor manufacturing techniques. The second section focuses on the metrology techniques and routines used to characterize the electrical devices at cryogenic temperatures in this study.

The primal GOI wafer material used in this work is a $6\,inch$ wafer, which is diced into $12 \times 12\,mm^2$ pieces. Furtherly, $6 \times 6\,mm^2$ pieces were cleaved from this $12 \times 12\,mm^2$ die, specifying the overall size of the sample. The patterning of all structures was done using laser lithography. The Ge sheets were molded from the Ge device layer at the GOI wafer through dry etching. A passivation layer between the device channel and the top gate was introduced using ALD. Afterward, the Ge sheets were contacted at both ends with Al pads, which were deposited again using laser lithography for pattern transfer Al deposition, followed by a lift-off process. Additionally, an opening was created in the buried oxide layer through wet chemical etching to allow contact with the substrate from the top of the sample for back-gated operation. The Al-Ge contacts and the final length of the Ge segment were formed by conducting several sequences of RTA with pre-calculated annealing times. To enhance the durability of the drain-source pads during electrical characterizations, an additional layer of Ti/Au was sputtered on top of the Al pads. Finally, the top gates were deposited over the device channel bars using physical vapor deposition. The specific process parameters can be found in Appendix B.

The electrical characterization of the devices was performed using standard FET characterization techniques, which included measuring both the output characteristics (I-V) and the transfer characteristics. Measurements at room temperature and above were conducted in a vacuum-sealed needle probe station, allowing for the sequential characterization of various devices. For low-temperature characterizations, a flow-through cryostat using liquid helium (He) coolant was employed.

3.1 Fabrication of Device Structures on a GOI Substrate

The GOI wafer used for this application features a p-doped 500 μm thick Si handle wafer with a 0.15 μm buried oxide (BOX) layer. On top of the BOX, there is a 75 nm thick, monocrystalline Ge layer oriented along the ⟨100⟩ direction. To prevent oxidation of the Ge layer, the base GOI material is covered with a 58 nm thick protective SiO_2 capping layer. A sketchy illustration of the provided GOI wafer is shown in Fig. 3.1a, along with the layer arrangement depicted in Fig. 3.1b.

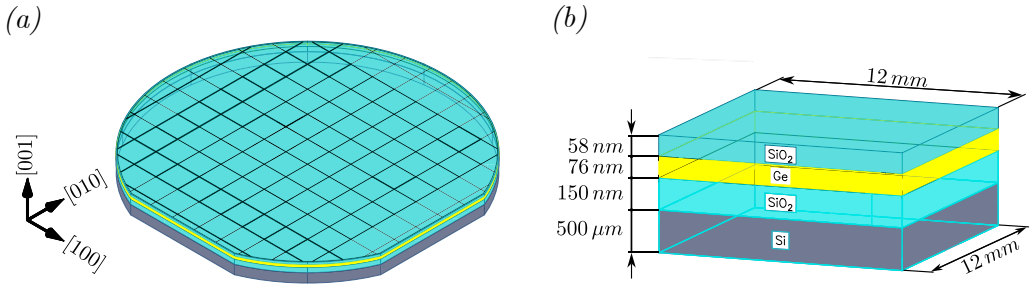

Figure 3.1: *Structural layout sketch of the GOI wafer. (a) A 150 mm GOI wafer featuring sawn-out $12 \times 12\,mm^2$ dies. (b) Dimensions of a $12 \times 12\,mm^2$ GOI substrate, which includes a monocrystalline Ge device layer oriented in the ⟨100⟩ direction, along with a BOX layer in between and a SiO_2 capping layer on top. Image adapted from [149].*

3.1.1 Device Layout and Dimensions

The sample layout was designed in Autodesk AutoCAD, allowing an optimized device placement with improved space utilization. Given the substrate size of $6 \times 6\,mm^2$, a structure placement window measuring $5.2 \times 5.2\,mm^2$ was established, leaving a fringe area of 0.4 mm thickness on each side. To avoid later positioning a device within the bulged area of the photoresist at the sample's edges, the final design of the Al-Ge-Al heterostructure was created within a window measuring $3.5 \times 5\,mm^2$, located between the markers. This design accommodates a total of 180 devices. A schematic representation of the device array is depicted in Fig. 3.2a. Figure 3.2b shows an enlarged view of device 11_03, identifiable by the gray marking in the top right corner, which was created during the Al sputter deposition process. The dimensions of the structures are indicated, including the expected final length of the germanium segment, denoted as l_{Ge}, and its width, labeled as w_{Ge}.

The basic structure comprises bone-like structures with a top gate architecture as shown in Fig. 3.2b. The width of the Ge sheet was set to 2 μm, establishing the smallest feature size on each device, which is well within the optical limit of the laser lithography system at approximately 600 nm. Different lengths of the Ge segments, denoted as l_{Ge}, were achieved by adjusting the distance between the Al pads while maintaining the same Al-Ge diffusion rate for all devices. This information can be referenced in Fig. 3.2b. To ensure there was enough space to place the top gate between the Al pads, the spacing between the Al pads was further increased. Ultimately, the distance between the two Al pads was set to $l_{Ge} + 10\,\mu m$. Due to the solubility issues discussed in Section 2.2.2, the minimum size of the Al pad must be at least 100 times the volume of Ge that needs to be thermally exchanged with the Al. This means that the area of the pad, where Ge is replaced by Al, must satisfy the condition $A_{pad} > 100 \times (2\,\mu m \times 10\,\mu m) = 2000\,\mu m^2$. This calculation assumes that the height of the Al pad is at least equal to the height of the Ge sheet.

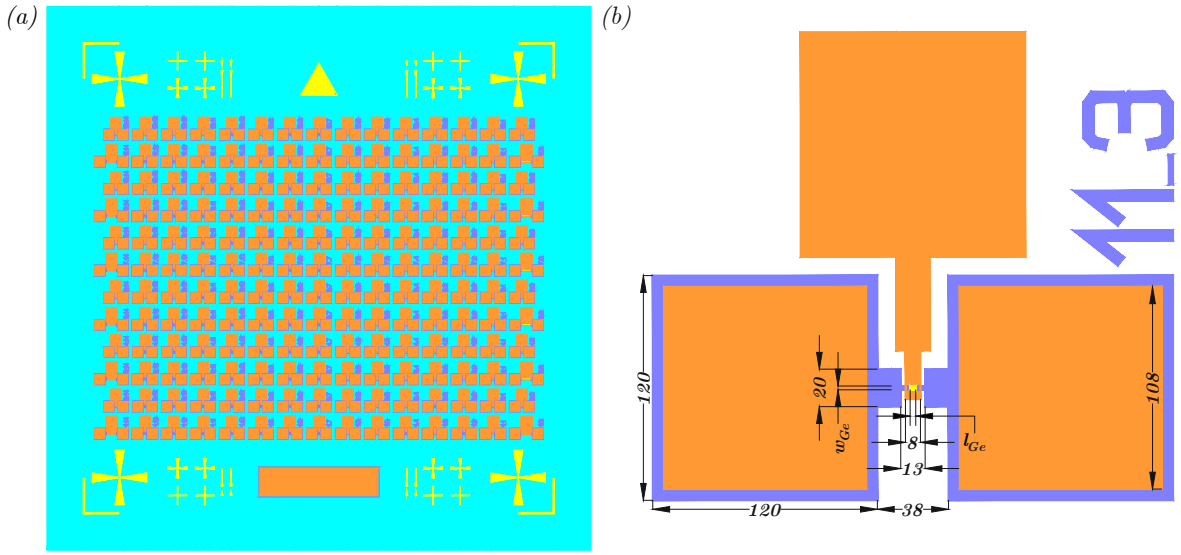

Figure 3.2: *Lithography mask layout of the Al-Ge-Al heterostructures with top-gates. Subfigure (a) illustrates the overall schematic of the device arrangement, including alignment markers at the edges. The areas are shaded according to the visible material layers from the top view. Subfigure (b) illustrates the design of device 11_03, which was structured during the Al sputter process. It details the dimensions of the structures, including the width w_{Ge} and the desired final Ge segment length, referred to as l_{Ge}.*

Additionally, another limitation on the minimum pad size arises from wire bonding, which becomes impractical for pad sizes smaller than $50 \times 50\,\mu m$. Taking all these factors into consideration, the final dimensions for the drain and source pads, as well as the top-gate pad, were set to $120 \times 120\,\mu m^2$. The total number of devices with variable Ge segment length l_{Ge} is provided below.

l_{Ge}	Count
$100\,\mu m$	12
$10\,\mu m$	12
$5\,\mu m$	12
$3\,\mu m$	12
$1\,\mu m$	12
$0.5\,\mu m$	12
$0.3\,\mu m$	12
$0.1\,\mu m$	48
$50\,nm$	42
$0\,\mu m$	6

After completing the design and placement of the structures, the layout was divided into five separate DXF files. These files can be converted for use with the lithography system software. Ultimately, the converted files will serve as lithography masks for the individual fabrication steps described in the following sections.

3.1.2 Formation of the Ge Nanosheets

Before processing the Ge device layer, the protective SiO_2 capping of the GOI wafer must be removed. This was accomplished via wet chemical etching with buffered hydrofluoric acid (BHF). Therefore, the sample was submerged in the solution for $80\,s$, assuming an etch rate of approximately $1\,nm/s$ (see Fig. 3.3a). The success of the etching process was confirmed through thickness measurements taken using ellipsometry. Fig. 3.3 schematically illustrates the preparation and process steps involved in the formation of Ge nanosheets from the Ge device layer of the GOI substrate.

To sputter the Ge sheets and alignment markers for the subsequent lithography steps, AZ 5214E photoresist was first spin-coated onto the sample at $6000\,rpm$ for $35\,s$ (see Fig. 3.3b). This was followed by a soft bake at $100\,°C$ for $60\,s$. Next, a positive lithography step was performed, exposing the areas between the Ge sheets with a dose of $140\,mJ/cm^2$ and no defocus (see Fig. 3.3c). The lithography process concluded with the development of the photoresist in AZ 726 MIF developer solution for $15\,s$ (see Fig. 3.3d).

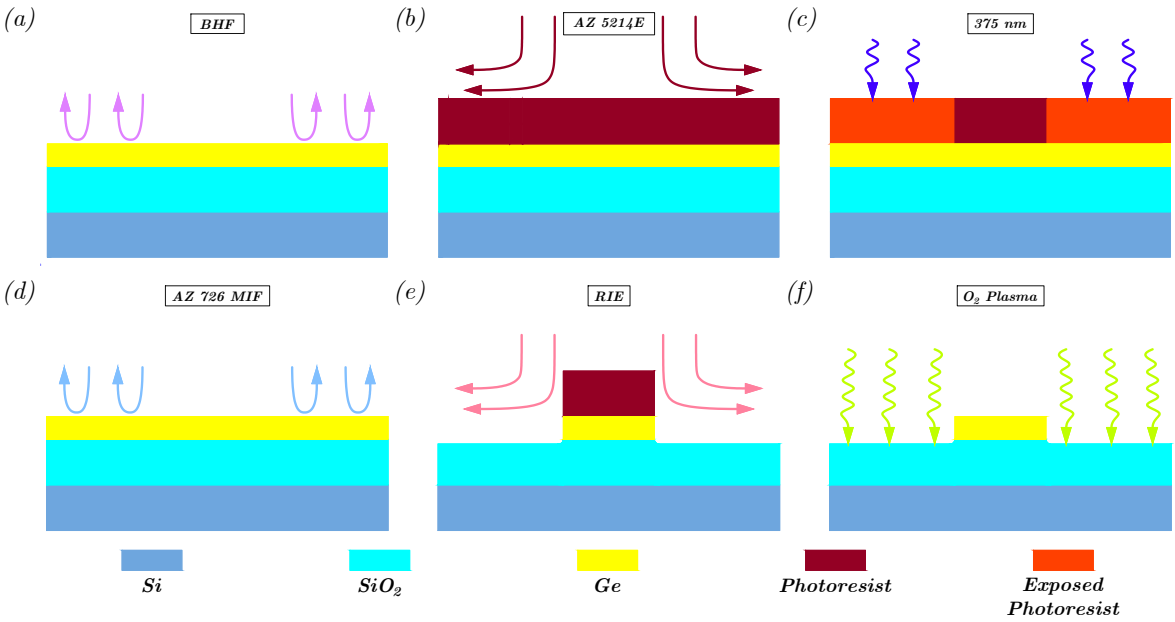

Figure 3.3: *Sketched illustration of the sample preparation including the formation of the Ge nanosheets through dry etching: (a) Wet chemical etching to remove the SiO_2 capping layer with BHF. (b) Spin-coating of AZ 5214E photoresist. (c) Positive lithography process for patterning of Ge sheets. (d) Development of the illuminated resist areas using AZ 726 MIF developer solution. (e) Reactive ion etching of the exposed Ge areas. (f) The elimination of organic residues through the process of O_2 plasma ashing. (g) Finished formation of the Ge sheets.*

The Ge sheets were ultimately created using reactive ion etching (RIE). To initiate a process that combines both physical and chemical etching reactions with high anisotropy and sharply defined profiles, a gas mixture of SF_6 ($50\,sccm$) and O_2 ($4\,sccm$) was introduced into the reactor chamber. [150] The SF_6-O_2 gas mixture reacts with the Ge surface, resulting in the formation of GeF_4, which is a volatile gas that escapes from the surface. At the same time, a GeO_xF_y passivation layer is created. This layer further reacts with fluorine, yielding additional GeF_4 and O_2 products, which are subsequently pumped away (see Fig. 3.3e). The anisotropy and etching rate are mainly influenced by the percentage of O_2 in the gas mixture, with a

lower percentage of O_2 necessary for achieving high anisotropy. [150, 151] For this process, the etching rate appeared to be approximately $2.5\,nm/s$. The etching rate for the underlying SiO_2 layer is significantly lower. The etching process was carried out for $70\,s$, ensuring there was no excessive over-etching.
After completing the process, the residual photoresist was removed using O_2 plasma ashing, followed by immersion in acetone and isopropanol (Fig. 3.3f). Finally, the Ge sheet structure remains, which later resembles the device's channel structure.

3.1.3 Passivation of the Ge Sheets

As discussed in detail in Section 2.1.3, Al_2O_3 was selected as the passivation for the Ge sheet and as the gate dielectric. The deposition of a thin film of Al_2O_3 was performed using ALD. By alternatingly flushing the reactor with H_2O and $Al_2(CH_3)_6$ for 120 cycles, a thickness of $12\,nm$ of Al_2O_3 was achieved. Due to the rapid oxidation of exposed Ge during transport to the ALD system, approximately $2,nm$ of native Ge_xO_y was unintentionally formed. As a result, the Al_2O_3 passivation was deposited over this native oxide. [152]

3.1.4 Ge Sheet Contacting

Electrical contacts were created on the Ge sheets by depositing Al pads at both ends of each sheet. This process involved a second lithography step, where the lithography mask was aligned according to the Ge alignment markers established previously (see Fig. 3.4a-c).

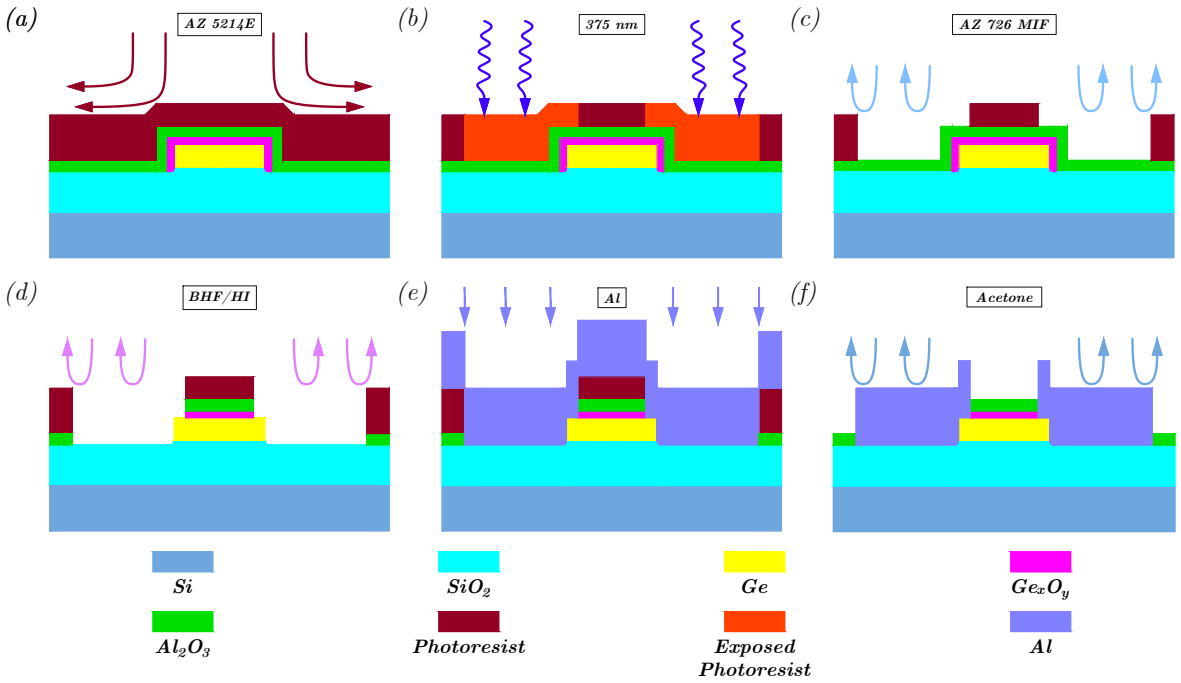

Figure 3.4: *Schematic sequence of the fabrication of the Al pads, to contact the Ge sheets: (a) Spin-coating of AZ 5214E photoresist. (b) Positive lithography process to form the openings for the deposition of Al. (c) Development of the illuminated resist areas. (d) Wet-chemical etching of the Al_2O_3 and native Ge_xO_y. (e) Al sputtering onto the sample. (f) Lift-off process in acetone to eliminate the photoresist and the excessive Al.*

The lithography mask used for sputter deposition of Al also served as an etching mask to remove Al_2O_3 and the native Ge_xO_y, thereby exposing both ends of the Ge sheet. Initially, the sample was immersed in BHF for 15 s to remove the Al_2O_3 layer. To eliminate the native Ge_xO_y and achieve a hydrogen-terminated Ge surface, the sample was then immersed in 14 % diluted hydroiodic acid (HI) for 5 s (see Fig. 3.4d). [153] To ensure physical contact between the Ge sheet and the Al pad, the regrowth of Ge_xO_y must be minimized. Therefore, the sample was quickly transferred into the load-lock of the sputter system.
Finally, a total of 125 nm of Al was deposited on the sample using RF sputtering (Fig. 3.4e). This process was concluded with a lift-off process, which removed the sacrificial Al layer (Fig. 3.4f).

3.1.5 Formation of Monolithic Al-Ge-Al Heterostructures

The Al-Ge-Al heterostructures with the desired Ge segment lengths (l_{Ge}), were finally created through a thermal diffusion process described in Section 2.2.2. The controlled diffusion process was initiated in a RTA oven, which features a quartz chamber that quickly heats up to 400 °C in approximately 12 s. The annealing process was conducted in forming gas atmosphere consisting of 90 % N_2 and 10 % H_2 to prevent oxidation. To improve control over the diffusion rates, the chamber was flushed with N_2 to rapidly cool the sample once the annealing time was completed. Fig. 3.5 illustrates the formation of the abrupt Al-Ge interface, facilitated by the deposited Al pads, while also showing the continuous shrinkage of the Ge segment due to the ongoing Al-Ge substitution process. [48]

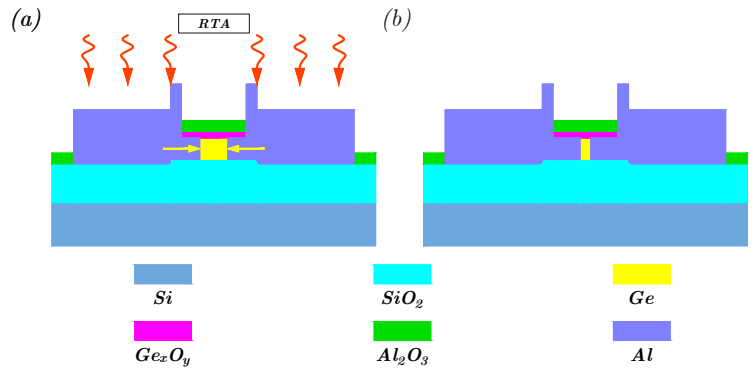

Figure 3.5: *The formation of abrupt Al-Ge Schottky junctions through RTA: (a) The thermal out-diffusion of Ge into Al reservoirs results in a continuous movement of the Al-Ge interface along the Ge channel. (b) Final Al-Ge-Al heterostructure characterized by abrupt Al-Ge junctions and a controlled length of the Ge segment.*

After each annealing cycle, the progress of the diffusion was observed using a scanning electron microscope (SEM). This monitoring allowed for the assessment of diffusion rates and the determination of the appropriate annealing time for the next step. This processing step was completed as soon as the desired number of devices reached the targeted length of the Ge segment.

3.1.6 BOX Opening for Back Gate Structure Formation

As stated at the beginning of this chapter, the substrate of the sample is composed of a doped Si handle wafer, which serves as a common back gate for all devices, with the buried SiO_2 as the gate dielectric. To enable contact with the back gate from the top side, a rectangular opening through the BOX layer was created. This required an additional lithography step to pattern the opening outside of the device array. The buried oxide layer was then dissolved by immersing the sample in BHF for 240 s.
The process of creating a metal contact within the back-gate opening is discussed in the following Section (see Section 3.1.7).

3.1.7 Contact Pad Reinforcement

The contacting pads often experience significant mechanical degradation when penetrated by probe needles or during wire bonding, primarily due to the relatively poor mechanical properties of Al. [154] To address this issue, reinforcement pads were added on top of the drain-source pads to enhance their durability after the annealing. The selected material for these reinforcement pads must possess superior mechanical properties compared to Al and be suitable for wire bonding. Since the back-gate opening required a metal contact that could be bonded, the deposition of this metal contact was done simultaneously with the deposition of the reinforcement pads. Additionally, it is important to ensure that the metal contact establishes an ohmic connection with the Si back-gate.

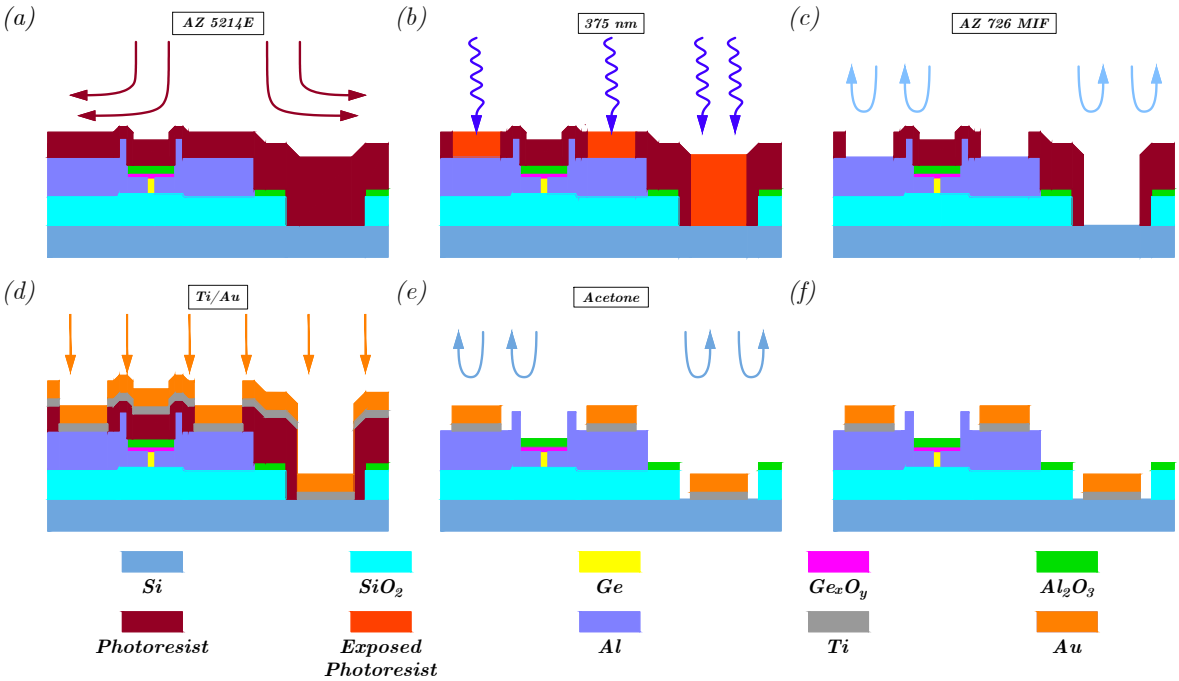

Figure 3.6: *Depiction of the processing steps for the deposition of the Ti-Au reinforcement pads: (a) Spin-coating of AZ 5214E photoresist, (b) positive lithography step, (c) development of the photoresist, (d) sputter deposition of* 10 *nm of Ti and* 180 *nm of Au, (e) removal of excess material and residual photoresist using the lift-off technique, (f) completion of the process.*

Considering all the requirements, a Ti-Au layer was sputtered onto the Al pads and into the back-gate opening. This process necessitated an additional lithography step (Fig. 3.6a-c). Initially, reverse sputtering was performed on the sample to eliminate any naturally formed Al oxides that could hinder the electrical contact between the Al pad and the Ti-Au layer. [155] This was followed by the deposition of a 10 nm Ti interlayer, which was intended to enhance adhesion between the Al pad and the subsequently sputtered 180 nm thick Au layer (see Fig. 3.6d). Finally, the process was completed by removing excess material through a lift-off technique (see Fig. 3.6e).

3.1.8 Au Top-Gates Deposition

Finally, the top gates were deposited onto the Al_2O_3 layer, covering the channel and both Al-Ge interfaces. To achieve this, an additional lithography process was performed (Fig. 3.7a-c). Due to the thinness of the 12 nm oxide layer, fabricating the top gates via sputter deposition posed a risk of damage from the high-energy particles ejected from the material target. To minimize leakage currents caused by impurities in the Al_2O_3 and ensure the integrity of the dielectric, the top gates were instead fabricated using physical vapor deposition. This process involved depositing 10 nm of Ti followed by 100 nm of Au through electron-beam evaporation (Fig. 3.7d).
The sample fabrication was completed with a final lift-off process (Fig. 3.7e). The drain, source, top gate, and back gate contacts of the device are labeled in subfigure Fig. 3.7f.

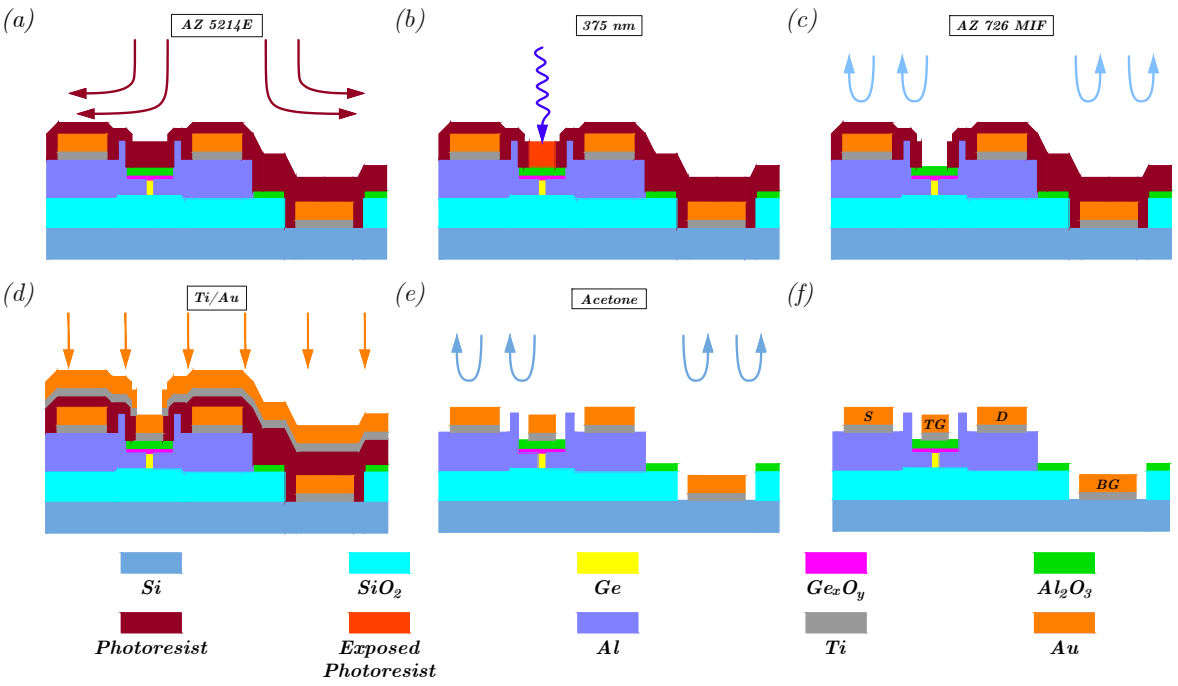

Figure 3.7: *Illustration of the top-gate deposition process: (a) Spin-coating of AZ 5214E photoresist, (b) positive lithography process, (c) developing of photoresist, (d) physical vapor deposition of 10 nm Ti and 100 nm Au via electron-beam evaporation, (e) removal of excess Ti and Au material through a lift-off process, (f) completion of the sample fabrication process. The device's electrical contacts are labeled as drain (D), source (S), top gate (TG), and back gate (BG).*

3.2 Electrical Characterization

The gated Al-Ge-Al heterostructures fabricated on top of GOI resemble SB-FETs, which are electrically characterized by measuring their transfer and output characteristics.
All measurements were performed using a Keysight B1500A semiconductor analyzer that has four source measurement units (SMU), three of which were utilized to contact the drain, source, and gate. Each SMU can be configured either as a voltage source or a current source, allowing for control over the specified voltage or current, respectively. In voltage source mode, the unit measures and records the current along with the actual output voltage. In current source mode, the unit measures and records the voltage along with the actual output current. A simplified circuit diagram of the SMU is shown in Fig. 3.8. Each SMU provides a voltage measurement resolution of up to $25\,\mu V$ and a current resolution of $1\,fA$. All measurements recorded in this work were conducted in voltage source mode while only recording the current. The current measurement range is organized in powers of ten. Lower currents require greater measurement precision, which leads to increased overall integration time. Additionally, the overall measurement time increases when multiple SMU units sequentially perform current measurements.
The measurement begins by adjusting the voltage to the starting level, followed by a hold time. After this period, a voltage sweep is performed by either increasing or decreasing the voltage to the next value, where it stays constant. Once the designated delay time has passed, the electrical current is sampled and averaged.

3.2.1 Measurement Equipment

The objectives of this work required measuring a temperature range from $4\,K$ to $400\,K$. Two different measurement setups and a semiconductor analyzer were used. Their properties and challenges are discussed below.

3.2.1.1 Semiconductor Analyzer and Needle Probe Station

In the first step, basic electrical characterizations were carried out in a Lakeshore needle probe station connected to the analyzer.

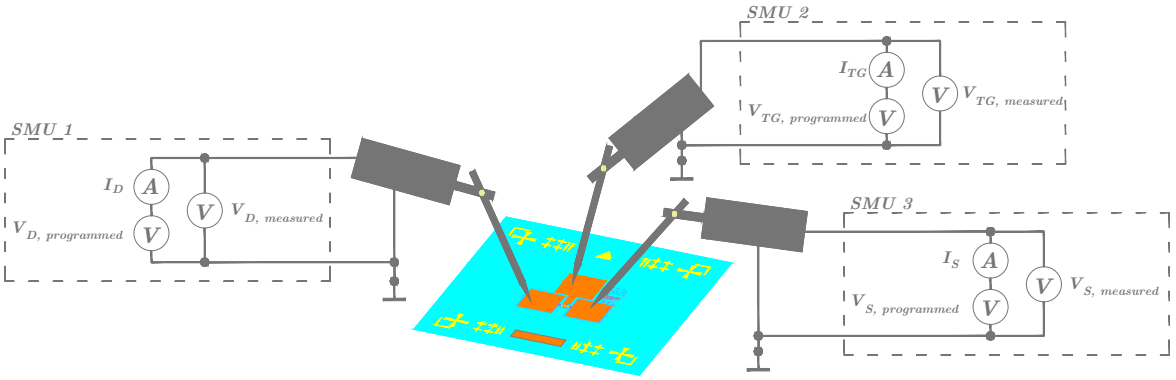

Figure 3.8: *Schematic representation of the connections for the drain, source, and gate, along with a basic circuit diagram of the SMUs. A Keysight B1500A semiconductor analyzer is used to carry out the electrical characterization with the help of three SMUs, which are connected via triaxial cables to the needle probes.*

This measuring system has four low-noise micromanipulators, each linked via a triaxial cable to a SMU of the analyzer. The sample is placed in a Lakeshore setup that can be evacuated

for measurements under vacuum conditions. Subsequently, the needles are positioned onto the contact pads of the devices using an optical microscope. Fig. 3.8 shows a schematic representation of the electrical connections for one device on the sample, utilizing needle probes that connect to a single SMU. Additionally, the measurement parameters, including voltage and current, are presented in a basic circuit diagram of the SMU.

3.2.1.2 Low-Temperature Measurement Setup

The cryogenic measurements were conducted in a separate flow-through cryostat that is approved for He use, allowing for cooling down to $4\,K$. Intermediate temperature levels were adjusted using a built-in heater, which is controlled by an external temperature controller. Fig. 3.9 illustrates the assembly of the flow-through cryostat.

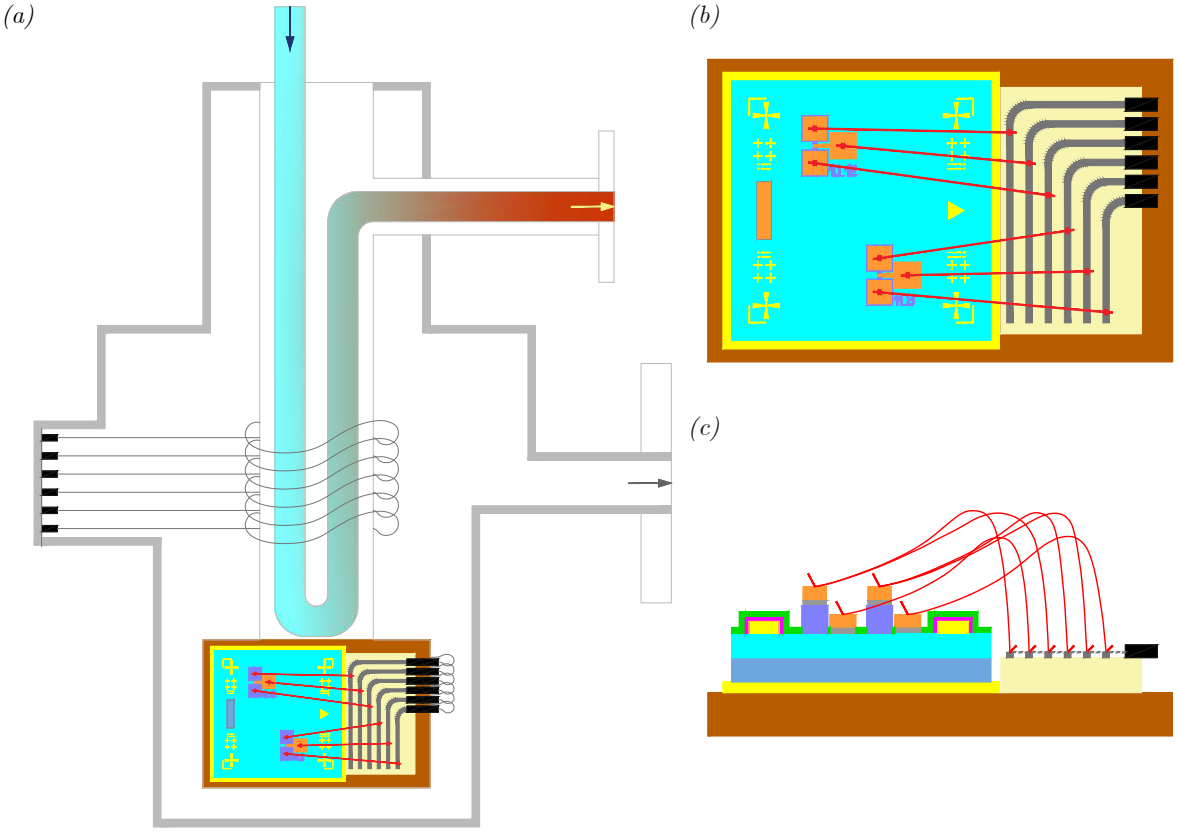

Figure 3.9: *Subfigure (a) illustrates the schematic structure of the flow-through cryostat, designed to achieve a cooldown to $4\,K$ using He coolant. The coolant is injected from the top, directly reaching the cryostat finger where the sample is mounted. Subfigure (b) shows the layout of the Cu plate with the PCB adhered on top. The sample is secured to the Cu plate using Kapton tape and silver paste, while the devices are connected to the PCB via bonding wires. Subfigure (c) presents a side view of the sample.*

The connection to the structures was established using cable connections, which required the devices to be wire bonded to a separate printed circuit board (PCB) mounted on the cryostat finger. Additionally, it is essential to ensure that there is no thermal isolation and no electrical contact between the substrate and the housing of the cryostat. To achieve this, a PCB with six parallel interconnects was attached to a copper (Cu) plate using adhesive silver paste. The sample was then attached to the Cu plate using Kapton tape and silver paste, which provided electrical isolation. The connection between the PCB interconnects and the outgoing cables

from the cryostat was established using socket and plug connectors. The cable terminals were soldered to the PCB interconnects, as shown in Fig. 3.9b. Afterwards, the Cu plate was secured to the cryostat finger using screw joints. The cryostat features six external plugs, allowing two devices to connect simultaneously. Additionally, the structures were linked via coaxial cables, which connected to triaxial cables that led to the SMUs of the analyzer.

3.2.2 Measurement of the Transfer Characteristics

The transfer characteristics were recorded by sweeping the top-gate voltage (V_{TG}) across a defined voltage range while monitoring the drain current I_D. Simultaneously, a constant drain-source bias voltage (V_{DS}) was applied to create a slight band bending.
The back gate was left floating throughout the measurements to minimize the impact of the drain/source pad-to-back-gate capacitance.
To prevent dielectric breakdown, the gate voltage was limited to $\pm 5\,V$, considering the gate oxide thickness. The drain-source voltage was equally distributed between source and drain contacts ($V_{DS} = V_D - V_S = V_{DS}/2 - (-V_{DS}/2)$) to maintain a low dielectric field across the gate oxide.

To assess the functionality of the devices, a transfer measurement was conducted by sweeping V_{TG} from $-5\,V$ to $+5\,V$ and back, with an applied bias of $V_{DS} = 10\,mV/100\,mV/1\,V$, depending on the length of the Ge channel. Capacitive charging currents were decayed by setting a hold time of $1\,s$, whereas the delay time was set to $0\,s$ to sweep at the maximum possible speed. To analyze the leakage current behavior, the drain current (I_D), source current (I_S) and top-gate current (I_G) were recorded. In the next step, six devices with a concise variety of l_{Ge} and the smallest possible hysteresis were selected for the cryogenic measurements.
All measurements were conducted in darkness to prevent photocurrent generation. Before each characterization procedure, the sample was heated on a hot plate at $125\,°C$ for 30 minutes to accelerate the de-trapping process and deplete occupied traps. The characterization sequence began with output characteristics measurements between $295\,K$ and $400\,K$ for activation energy evaluation, followed by cryogenic measurements.
To reduce the impact of surface traps on the transfer characteristics during low-temperature measurements, the measurement sweep was divided into two separate segments. [135] First, the positive gate voltage range from $0\,V$ to $+5\,V$ and vice versa was measured, followed by the negative gate voltage range from $0\,V$ to $-5\,V$ and vice versa. Both sweeps were conducted in $100\,mV$ voltage steps. Additionally, V_{DS} was adjusted to maintain a constant electric field strength of $0.2\,kV/cm$ in the Ge segment, therefore, V_{DS} was adapted for each device. The resulting drain-source voltages are listed in Table 3.1 below.

Table 3.1: *Determination of the bias voltages V_{DS} for a specified electric field strength $2 \cdot 10^2\,V/\mu m$.*

ID	l_{Ge}	V_{DS}
03_00	$102\,\mu m$	$2046.0\,mV$
05_13	$10\,\mu m$	$200.8\,mV$
11_03	$2\,\mu m$	$43.0\,mV$
11_08	$0.5\,\mu m$	$10.8\,mV$
10_12	$0.15\,\mu m$	$3.0\,mV$
08_03	$50\,nm$	$1.0\,mV$

As per [156] the electrical resistivity of 0.15 μm thick Al films exhibits a weak temperature dependence, decreasing from $8.0 \cdot 10^{-4}\,\Omega cm$ at 300 K to $5.5 \cdot 10^{-4}\,\Omega cm$ at 8 K. This implies that the same electric field is maintained in the Ge segment across the temperature range, without a significant voltage drop in the Al interconnects.

At lower temperatures, where significantly reduced currents were expected, only I_D was recorded to optimize measurement time.
Ultimately, the low-temperature measurements were conducted at the temperatures 4 K, 10 K, 50 K, 100 K, 200 K, and 295 K, starting from the lowest temperature. To prevent damage to the Al-Ge interface, the drain current was limited to 10 μA during all measurements.
For improved signal-to-noise ratio in the data presentation, a Savitzky-Golay smoothing filter was applied to I_D while preserving higher moments of the data.

3.2.3 Measurement of the Output Characteristics

To further investigate the conductivity of the Ge channel and the nonlinear behavior of the Schottky diodes, common I-V characteristics were measured. First, the temperature was lowered to 4 K to examine the I-V characteristics. Following this, the temperature was raised back to the same levels used in the previous measurement for a repeat assessment.

The output characteristics were measured by applying a constant V_{TG} and sweeping V_{DS} while recording I_D. A total of 11 I-V characteristics were recorded for gate voltages ranging from $+5\,V$ to $-5\,V$, in steps of 1 V. The bias voltage range was adjusted for each channel length to achieve a maximum current below 10 μA. The drain current was recorded while V_{DS} was swept over 101 discrete voltages within the selected range.

3.2.4 Determination of the Activation Energy for SB-FET's Charge Carrier Injection

The determination of the effective Schottky barrier through electrical voltage and current measurements is not directly feasible and, instead, must be evaluated using device modeling equations. For ordinary Schottky diodes, the effective Schottky barrier height, or, depending on the measuring method, even the Schottky barrier itself can be extracted using various methods presented in books, such as Sze [71], Rhoderick [49], and Schröder [72]. These methods include the current-voltage method (I-V), current-temperature (I-T) method, capacitance-voltage method (C-V), photoelectric measurement, and ballistic electron emission microscopy. It is evident that methods not involving current, such as photocurrent measurement, yield the most accurate results as they are not affected by interface trapping effects. [71, 72]
Nonetheless, the measurement methods used to determine the effective Schottky barrier height of a diode are not applicable to Al-Ge-Al heterostructures. This is because these structures consist of two back-to-back Schottky diodes, as discussed in Section 2.4. Additionally, since the measurements are limited to electrical current and voltage, it is not possible to determine the effective Schottky barrier height for either diode due to the inability to measure the voltage across them.
In this work, a combination of the I-V and I-T methods was employed to determine the activation energy ($E_{A,eff}$) necessary for injecting charge carriers. This approach is based on thermionic emission theory and is suitable for lightly doped semiconductors in metal-semiconductor-metal heterostructures, provided that the activation energies are greater than k_BT/q (approximately 25.42 meV at 295 K). This method can be interpreted as a rough estimation of the effective Schottky barrier height. [157]

Furthermore, the measurement of $E_{A,eff}$ takes into account contributions from both thermionic and field emission currents, and does not make any assumptions about the electrically active area. [158]

Eventually, to perform the procedure, I-V measurements were conducted in vacuum to gather information about the activation energy. To investigate the temperature dependence of the I-V characteristics, which is essential for presenting the data in the Richardson plot later, the temperature was gradually increased to $295\,K$, $325\,K$, $350\,K$, $375\,K$, $382.5\,K$, and $400\,K$.
In a manner similar to the I-V measurement procedure described in the previous section, the gate voltage was varied from $+5\,V$ to $-5\,V$ in steps of $1\,V$. At each fixed gate voltage, a bias voltage sweep was conducted, resulting in the recording of 11 I-V characteristics at 11 different gate voltages for each device.
Based on the preceding device functionality test and the recorded transfer characteristics, the device resistivity was calculated. This allowed the estimation of the maximum bias voltage, $V_{DS,max}$, for the I-V measurement. The goal was to obtain a specific maximum current value in the lower μA range during the V_{DS} sweep to effectively cover the linear and nonlinear I-V regime. Each device had its applied $V_{DS,max}$ set individually based on the parameter values displayed in Table 3.2.

Table 3.2: *Parameters for the measurement setup used to record the I-V characteristics of each device to obtain $E_{A,eff}$.*

l_{Ge}	$102\,\mu m$	$10\,\mu m$	$2\,\mu m$	$0.5\,\mu m$	$0.15\,\mu m$	$50\,nm$
$-V_{DS,max}$	$-1\,V$	$-600\,mV$	$-200\,mV$	$-200\,mV$	$-25\,mV$	$-1\,mV$
$+V_{DS,max}$	$+1\,V$	$+600\,mV$	$+200\,mV$	$+200\,mV$	$+25\,mV$	$+1\,mV$
ΔV_{DS}	$10\,mV$	$6\,mV$	$2\,mV$	$2\,mV$	$25\,\mu V$	$50\,\mu V$
n_{Steps}	200	200	200	200	200	40

3.2.4.1 Activation Energy as a Function of Gate and Bias Voltage

Fig. 3.10 illustrates exemplarily the evaluation process for determining the activation energy based on V_{TG} and V_{DS} for device 11_03 ($l_{Ge} = 2\,\mu m$). The I-V characteristics recorded at gate voltages ranging from $-5\,V$ to $+5\,V$ at $400\,K$ are shown in the semilogarithmic plot in Fig. 3.10a.

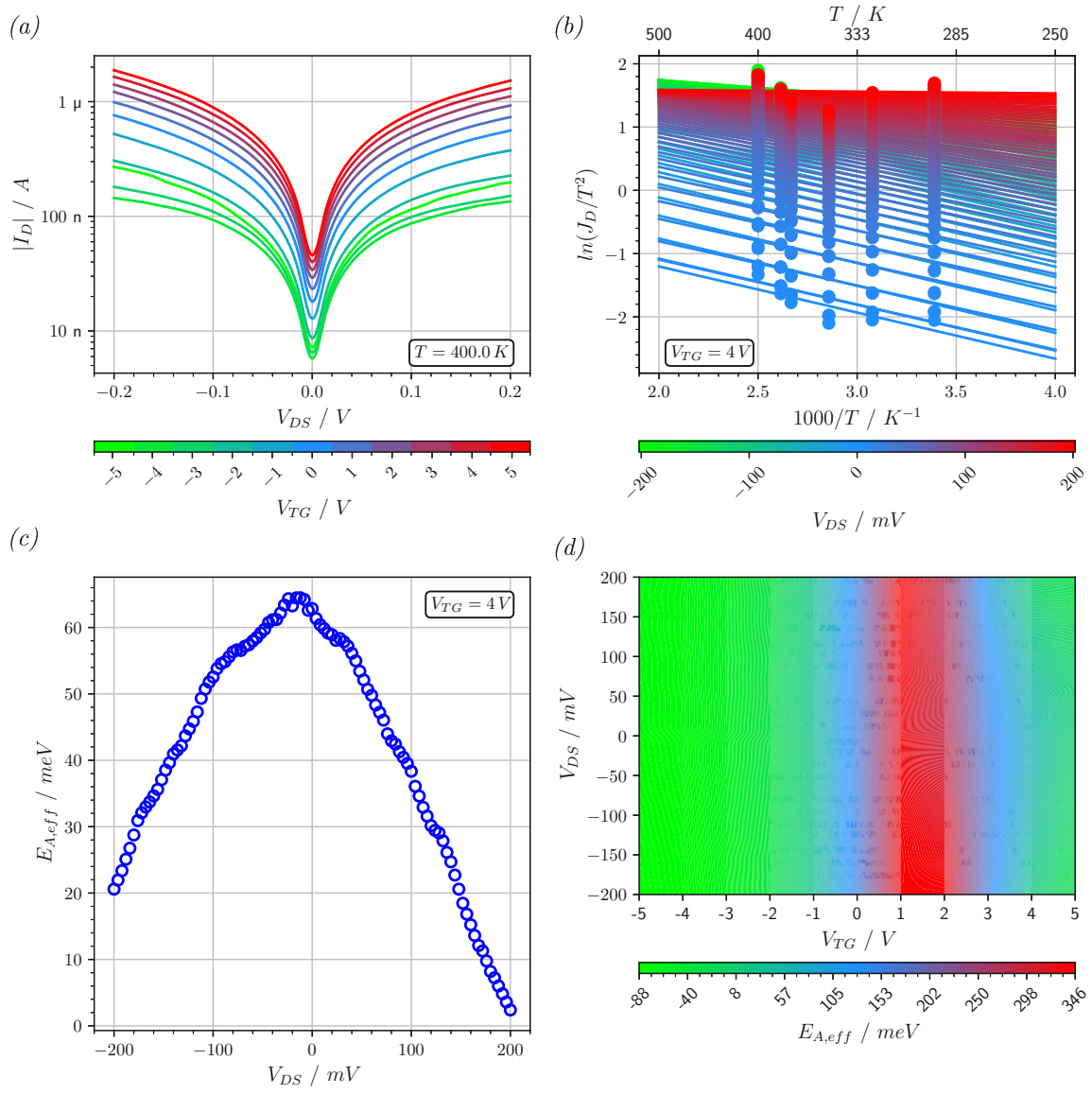

Figure 3.10: *Graphical representation of the evaluation procedure of the activation energy as a function of V_{DS} and V_{TG} using device 11_03 ($l_{Ge} = 2\,\mu m$) as an example. (a) depicts the $|I_D|$ versus V_{DS} characteristics with a logarithmic scaling on the y-axis at $T = 400\,K$ and V_{TG} ranging from $-5\,V$ to $+5\,V$. (b) corresponds to the Richardson plot at $V_{TG} = 4\,V$, with the points representing the data from (a) and taking the temperatures, as well as the cross-sectional area of the device, into account. The point values in (b) are then used to fit a straight line, with the slope corresponding to the activation energy, which is further plotted in (c) as $E_{A,eff}$ versus V_{DS} graph. Considering the other gate voltages, $E_{A,eff}$ as a function of V_{DS} and V_{TG} is obtained as a colormap in (d). Image based on [149].*

The I_D data were smoothed using a Savitzky-Golay filter before evaluation. Consequently, I_D at $V_{DS} = 0\,V$ seems unusually high.

The model used for the evaluation is based on Eq. 2.29, which is modified for the activation energy $E_{A,eff}$ as:

$$J_D\,(T) = A^* T^2 \exp\left(\frac{qV_{DS} - E_{A,eff}}{nk_B T}\right). \tag{3.1}$$

In order to display Eq. 3.1 linearly in the Richardson plot, it is rewritten as:

$$\ln\left(\frac{J_D}{T^2}\right) = \frac{qV_{DS} - E_{A,eff}}{k_B}\frac{1}{T} + \ln\left(A^*\right) = k\frac{1}{T} + \ln\left(A^*\right). \tag{3.2}$$

The ideality factor is assumed to be $n = 1$, as the individual contributions of thermionic and field emission cannot be determined. However, since the ideality factor depends on temperature, it is a rough estimate. The y-axis $\ln\left(J_D/T^2\right)$ is then plotted as function of $1000/T$. Here, the drain current density J_D is calculated by dividing the measured I_D points depicted in Fig. 3.10a by the cross-sectional area of the channel structure. Specifically, for device 11_03, the area is calculated as $A = 1.78\,\mu m \times 75\,nm$. The measurements may be performed within a restricted temperature range around room temperature to prevent carrier freeze-out effects and to ensure that $E_{A,eff}$ and A^* in Eq. 3.2 remain independent of temperature. [71, 72, 158] The resulting values are then entered into the $\ln\left(J_D/T^2\right)$ versus $1000/T$ Richardson plot. Since the I-V characteristic was measured with 200 V_{DS} measuring points, 200 points also appear for every temperature level and V_{TG} in the Richardson plot. The Richardson plot shown in Fig. 3.10b corresponds to the one at $V_{TG} = 4\,V$.
The results observed at various temperatures, illustrated in the Richardson plot, are fitted using a linear equation $y = kx + d$. Each step in the bias voltage corresponds to a separate straight line on the plot. The slope of each line is used to calculate the value of k in Eq. 3.2. The fitted straight lines can be found in Fig. 3.10b. A higher current flow in semiconductors is associated with increasing temperature, resulting in a negative slope representing the activation energy $E_{A,eff}$. [71]
The activation energy can be determined by interpreting the fitting parameter k according to

$$E_{A,eff} = qV_{DS} - k \cdot k_B \cdot 1000. \tag{3.3}$$

This calculated value of $E_{A,eff}$ can then be plotted against V_{DS} for a fixed gate voltage V_{TG}. An example of this is illustrated in Fig. 3.10c, where $V_{TG} = 4\,V$. The asymmetry of the device is clearly visible. For $V_{DS} = -200\,mV$, $E_{A,eff}$ is approximately $20\,meV$, while for $V_{DS} = +200\,mV$, $E_{A,eff}$ is approximately $2\,meV$.
In this simplified model, it is unhelpful to determine A^* by examining the fitting parameter d in the linear equation, as the intercept with the y-axis at $1000/T = 0$ is far from the measurement results. This makes this estimation very unreliable due to the fitting. Furthermore, it is not needed for the subsequent evaluation steps.
Ultimately, by recreating the plots in Fig. 3.10b-c for all other gate voltages, the activation energy can be displayed as a colormap $E_{A,eff} = E_{A,eff}\,(V_{DS}, V_{TG})$, which is depicted in Fig. 3.10d. This evaluation procedure covers both positive and negative bias voltage ranges, allowing for a direct comparison of the activation energy of both diodes in the heterostructures to be presented in a single graph. [158, 159] The asymmetry of the device is clearly visible in Fig. 3.10c. For $V_{DS} = -200\,mV$, $E_{A,eff}$ is approximately $20\,meV$, while for $V_{DS} = +200\,mV$, $E_{A,eff}$ is approximately $2\,meV$.

3.2.4.2 Activation Energy as a Function of Gate Voltage without Bias

When applying $V_{DS} = 0\,V$ to the device, the $E_{A,eff}\,(V_{DS}, V_{TG})$ plot does not yield reliable values. This is because the analyzer fails to measure any actual current. It only measures parasitic and capacitive charging currents or captures noise. These unwanted currents are included in the I-V measurement when sweeping across $V_{DS} = 0\,V$. Consequently, it was feasible to plot I_D logarithmically in Fig. 3.10a.
Applying a bias voltage changes the barrier due to effects such as image force lowering, which results from additional band bending. [160] Therefore, it is important to analyze how the activation energy depends solely on the gate voltage (with $V_{DS} = 0\,V$). To achieve this, the previously outlined procedure needs to be modified. The revised evaluation process is illustrated exemplarily in Fig. 3.11 for device 11_03 ($l_{Ge} = 2\,\mu m$).

Without a bias voltage, Eq. 3.3 becomes:

$$E_{A,eff} = -k \cdot k_B \cdot 1000.$$

However, since there is no current being measured at $V_{DS} = 0\,V$, the activation energy for this condition needs to be estimated. This is achieved by fitting a straight line of the form $y = kx + d$ using other values of $E_{A,eff}$ at $V_{DS} \neq 0\,V$. These values are derived from the $E_{A,eff}\,(V_{DS})$ graph presented in Fig. 3.11c, which was generated using the slope values from the Richardson plot shown in Fig. 3.11b for $V_{TG} = 4\,V$. In this linear equation, the fitting parameter d corresponds to the sought value $E_{A,eff}$ at $V_{DS} = 0\,V$.
The current-voltage relationship of the Al-Ge-Al heterostructures in Eq. 2.31 of Section 2.4 indicates a linear and non-linear voltage range. To accurately determine the activation energy while minimizing band bending effects, it is crucial to filter out the linear segment of $I_D\,(V_{DS})$. To do this, it is necessary to estimate a suitable range for the V_{DS} sweep based on the length l_{Ge} of the Ge segment. To clearly distinguish the linear and non-linear components of $I_D\,(V_{DS})$, the current-voltage relationship shown in Fig. 3.11a was plotted using a linear y-axis scale. By using an appropriate V_{DS} step size, one can differentiate between the linear and nonlinear portions. The straight-line fitting necessitated the consideration of higher bias voltages to obtain more accurate results. In Fig. 3.11c, the V_{DS} values ranged from $76\,mV$ to $200\,mV$. Additionally, the accuracy of the entire evaluation increases with each additional temperature level at which the I-V measurement is carried out.
This procedure can be performed on both diodes by conducting an I-V measurement with a bias voltage sweep from $-V_{DS,max}$ to $+V_{DS,max}$. However, the evaluation must be carried out separately for the intervals $V_{DS} \in [-V_{DS,max}, 0]$ and $V_{DS} \in [0, +V_{DS,max}]$. The evaluation process, as illustrated in Fig. 3.11, was conducted over the interval $[0, +V_{DS,max}]$ to comply with the polarization of the device during the subsequent measurements.
Eventually, by repeating the evaluation steps in Fig. 3.11b-c for each gate voltage, the activation energy $E_{A,eff}\,(V_{TG})$ at $V_{DS} = 0\,V$ was determined. The results are shown in Fig. 3.11d as data points, which were then connected with an interpolation line to show the evaluation result.

The evaluation process yields varying results for $E_{A,eff}$ depending on the direction of the V_{DS} sweep. This variation occurs because most of the applied V_{DS} drops across the reverse-biased Schottky diode, which predominantly affects the I-V characteristics and, consequently, the value of $E_{A,eff}$. This phenomenon has already been shown in Fig. 3.10, where the device's Schottky diodes have different barrier heights.

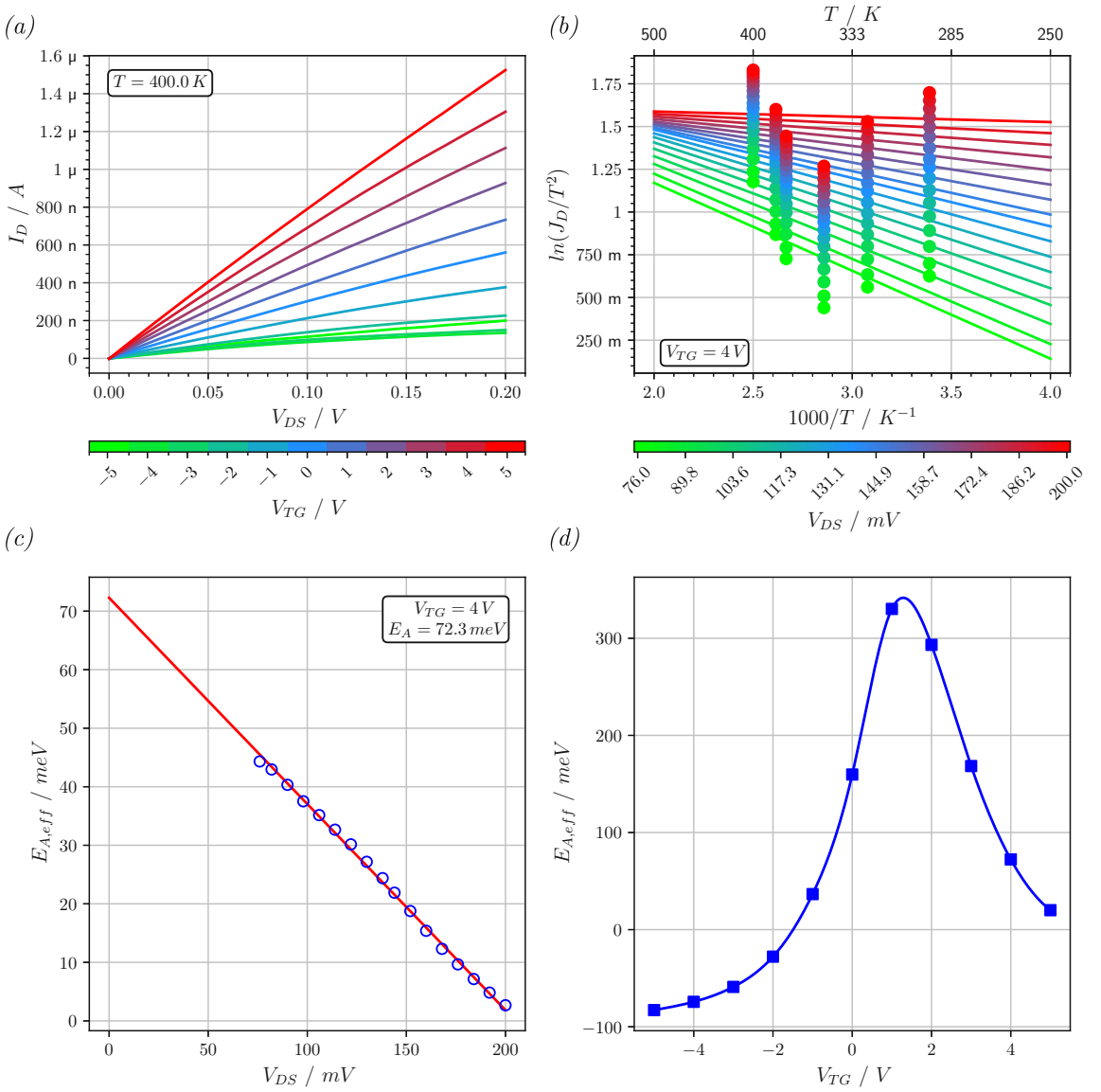

Figure 3.11: *Graphical representation of the evaluation procedure of the activation energy $E_{A,eff}$ as a function of the gate voltage V_{TG} for $V_{DS} = 0\,V$. The exemplary demonstration is for device 11_03 with $l_{Ge} = 2\,\mu m$. (a) depicts the recorded I-V characteristic at $T = 400\,K$ for the V_{DS} range of $0\,V$ to $200\,mV$. (b) corresponds to the Richardson plot at V_{TG} with the inserted data from I-V characteristics recorded at $295\,K$, $325\,K$, $350\,K$, $375\,K$, $382.5\,K$, and $400\,K$, in the V_{DS} range of $76\,mV$ to $200\,mV$. (c) shows the slope of the fitting lines (b) plotted over V_{DS} in the range from $76\,mV$ to $200\,mV$ and $V_{TG} = 4\,V$. The line in (c) estimates an activation energy at $V_{DS} = 0\,V$ as $E_{A,eff} = 72.3\,meV$ at the top gate voltage of $4\,V$. The plot in (d) shows the final $E_{A,eff}\,(V_{TG})$ at $V_{DS} = 0\,V$. Image based on [149].*

Chapter 4

Results and Discussion

This chapter analyzes the fabrication of the Al-Ge-Al heterostructure devices and discusses the evaluation results based on the data recorded as per the procedures outlined in the previous chapter. The results are derived from a dataset of six specific devices that were chosen to encompass a broad range of the Ge segment length, including ultra-short segment lengths.

The first part focuses on the fabrication process, particularly the thermally induced Al-Ge exchange process. The second part discusses the characterization of electrical devices at various temperatures, including cryogenic temperatures.

The electrical characterization process commenced with a detailed inspection of all devices. To achieve this, the transfer characteristics were recorded under ambient conditions. To determine the activation energy of the selected devices, data was gathered through I-V measurements conducted under vacuum conditions at various temperatures above room temperature.
Finally, the low-temperature device characterization involved measuring transfer and output characteristics. This was accomplished using a flow-through cryostat with He coolant, requiring the devices to be bonded to an external PCB.

4.1 Device Fabrication Process

As described in the previous section, in total 180 devices were manufactured on a $6 \times 6\,mm^2$ GOI substrate. Fabricating a large number of devices was necessary to increase the likelihood of obtaining a sample that includes a set of devices with adequately varying Ge segment lengths. A crucial intermediate step in the fabrication procedure was the thermally induced Al-Ge exchange process used to produce the monolithic Al-Ge-Al heterostructures. After completing the manufacturing process, it was found that one device was not properly annealed due to inadequate contact between the Al pad and the Ge sheet. Another device had a broken top gate, and further 10 devices did not have their interfaces entirely covered by the top gate. Additionally, five devices exhibited a gate leakage current exceeding $1\,pA$, whereas typical cases showed just a few tens of femtoamps. This issue was attributed to an insufficiently insulating gate oxide. In addition, thirteen Ge sheets were completely replaced with Al, with no remaining Ge. Eventually, 165 devices were tested as fully functional, of which six representative devices were selected for the comprehensive electrical characterizations. Thus, only their results are presented in the following.

4.1.1 Verification of the Al-Ge Exchange Process

Initially, the fabrication of atomically sharp junctions in the Al-Ge system was demonstrated with vapor-liquid-solid grown NWs. [36] However, Wind [38] proved the success of this procedure on structures of larger cross-sectional dimensions than NWs. The diffusion rates in the Al-Ge exchange process were significantly influenced by the geometry and varied among devices. This variation depended on the quality of the interface between the Ge sheet and the deposited Al pad, which was partially degraded by the native oxide growth during sample transfer after the wet-chemical etching to the sputter system chamber. [95] To achieve devices with extremely short Ge segment lengths, it was necessary to carry out multiple annealing cycles and afterward analyze the diffusion process using SEM. This allowed for the estimation of diffusion rates, with special attention to the devices with the shortest Ge segments.

Table 4.1: *Listing of the selected devices based on their identifiers (ID) for electrical characterization at cryogenic temperatures, including annealing times t_{RTA} and annealing temperature T_{RTA}. The length specifications comply with the Ge segment lengths l_{Ge}, which were determined using SEM after the corresponding annealing cycles. For unannealed devices ($t_{RTA} = 0\,s$), the Ge segment length equals the gap between the Al reservoirs. w_{Ge} represents the Ge sheet width.*

T_{RTA}	ID / t_{RTA}	03_00	05_13	11_03	11_08	10_12	08_03
–	$0\,s$	$109.4\,\mu m$	$19.42\,\mu m$	$12.52\,\mu m$	$9.76\,\mu m$	$9.68\,\mu m$	$9.62\,\mu m$
$400\,°C$	$3 \times 300\,s$	$103\,\mu m$	$10.27\,\mu m$	$2.4\,\mu m$	$0.75\,\mu m$	$0.37\,\mu m$	$0.3\,\mu m$
$400\,°C$	$1 \times 150\,s$						
$400\,°C$	$1 \times 200\,s$						
$400\,°C$	$1 \times 150\,s$						
$400\,°C$	$1 \times 50\,s$	–	–	–	–	$0.18\,\mu m$	$0.07\,\mu m$
$400\,°C$	$1 \times 90\,s$	$102\,\mu m$	$10\,\mu m$	$2\,\mu m$	$0.53\,\mu m$	$0.15\,\mu m$	$50\,nm$
w_{Ge}		$1.8\,\mu m$	$1.85\,\mu m$	$1.78\,\mu m$	$1.9\,\mu m$	$1.82\,\mu m$	$1.78\,\mu m$

Table 4.1 provides a list of the selected devices along with their identifiers (ID) on the sample. It includes the initial Ge segment length ($t_{RTA} = 0\,s$), which represents the distance between the sputtered Al contact pads. The sizes may vary slightly from those set in the lithography mask due to the limited resolution of the lithography system and measurement inaccuracies. Since the maximum allowed annealing duration for the RTA system is $300\,s$, it was initially operated three times consecutively for $300\,s$ each at a temperature of $400\,°C$. l_{Ge} remained within the resolvable size of the optical microscope, allowing for a brief verification of the diffusion progress during the first five annealing cycles. Following this, SEM was employed to verify l_{Ge}. In the subsequent annealing procedure, only the two devices with the shortest l_{Ge} were investigated to estimate the most critical diffusion rates. Fig. 4.1 shows the SEM images that were used to determine the value of l_{Ge}.

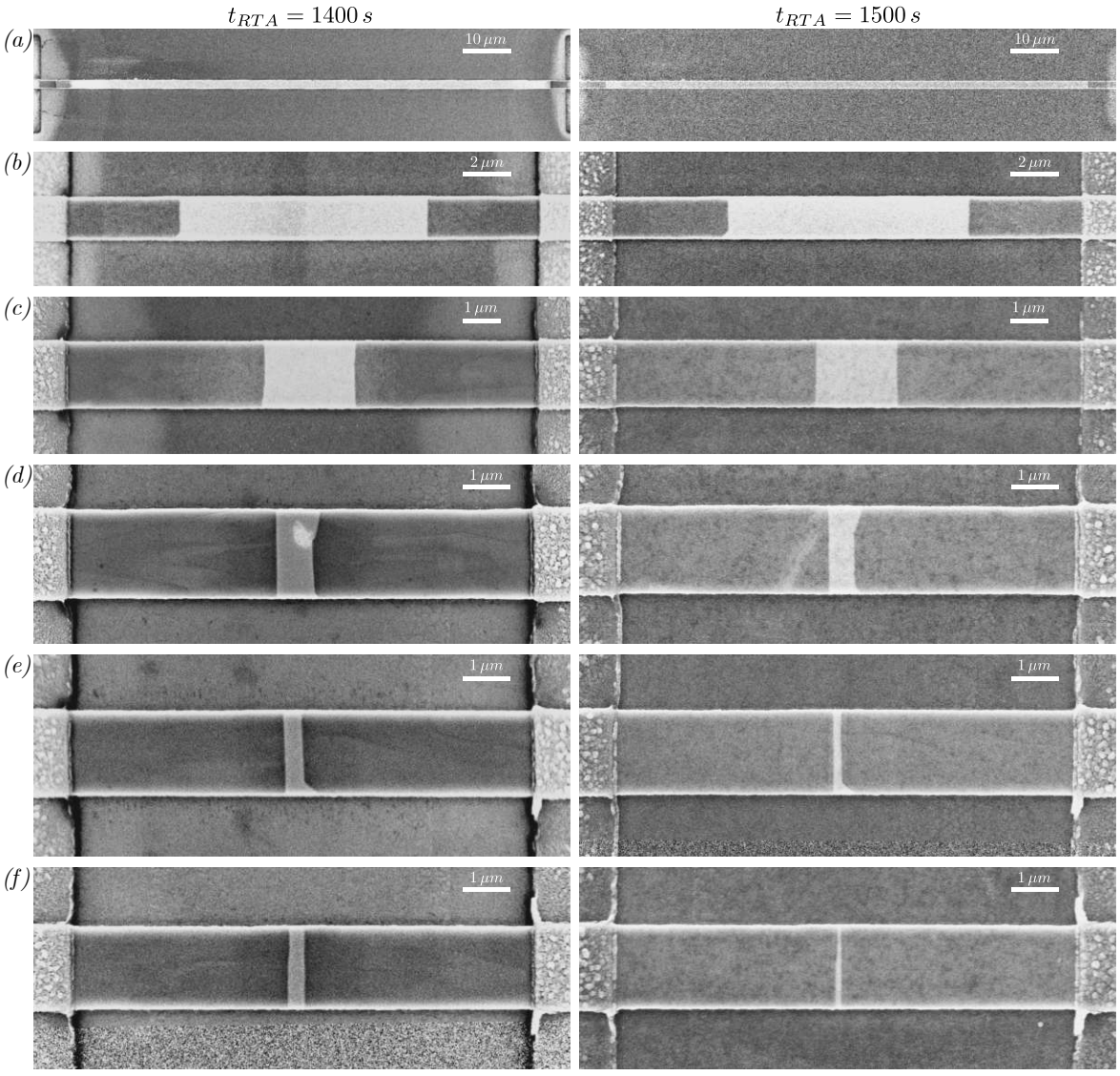

Figure 4.1: *SEM images of the Ge nanosheet after* $1400\,s$ *and* $1540\,s$ *of RTA. The devices are identified as (a) 03_00, (b) 05_13, (c) 11_03, (d) 11_08, (e) 10_12, and (f) 08_03. Their dimensions, such as the gap between the Al pads,* l_{Ge}*, and the width of the sheet structures, can be found in Table 4.1.*

The images in the first column were taken after the initial six annealing cycles, corresponding to a total annealing time of $t_{RTA} = 1400\,s$. The images in the second column were taken after the final annealing cycle, with a total annealing time of $t_{RTA} = 1540\,s$.

In the subfigures of Fig. 4.1, a bar-shaped structure representing the nanosheet channel of the device is clearly visible. The light gray stripe in the center of the structure appears, representing the remaining segment of monocrystalline Ge, which decreases in length with ongoing annealing duration. The dark gray surface on the left and right of the Ge segment corresponds to the Ge exchanged with Al. The Al contact surfaces at the left and right ends appear light gray with a rough surface. Due to a significant contrast difference between Al and Ge resulting from their different material responses to the electron beam, the two materials can be easily distinguished from each other. In Fig. 4.1b-e can be seen that some interfaces do not form a completely flat plane perpendicular to the diffusion direction. This is caused by diffusion inhomogeneities due to the large cross-section of the structures and was also reported by Wind [48] in his study on wafer-scale heterostructure formation. Additionally, in the first column of Fig. 4.1a-c, noticeable changes in brightness can be observed outside the device channel structure, particularly near the Al pads. This may indicate that the deposited Al_2O_3 has been affected by HF under-etching during the fabrication of the aluminum pads. As it was not possible to measure the local thickness of the insulation layer, the integrity of the dielectric layer could not be guaranteed. Therefore, another $\sim 12\,nm$ of Al_2O_3 were deposited, which eliminated the differences in contrast, as shown in the second column of Fig. 4.1.

4.1.1.1 Diffusion Rate Analysis

As previous studies [38, 40] have reported, the diffusion rates follow a nonlinear time dependence, proportional to the square root of time $\left(\sim \sqrt{t}\right)$. Consequently, it was necessary to recalculate the diffusion rates after just $50\,s$ of RTA to gain a clearer understanding of the ongoing diffusion process. To achieve the desired length of the Ge segment quickly, an extended overall annealing time of $1400\,s$ was employed. The subsequent annealing cycle was conducted using precisely calculated diffusion rates, although only the two critical devices were examined using SEM. Ultimately, a final annealing cycle with an annealing time of $90\,s$ was initiated to complete the fabrication process. Table 4.2 presents the diffusion rates derived from the Ge segment lengths obtained from SEM images. These values were calculated based on the difference in l_{Ge} observed after one annealing cycle.

Table 4.2: *Listing of selected devices based on their IDs for electrical characterization at cryogenic temperatures, including the annealing times t_{RTA} and the resulting Al-Ge diffusion rates. The l_{Ge} was determined at $t_{RTA} = 0\,s$ and $t_{RTA} = 1540\,s$ using SEM.*

ID / t_{RTA}	03_00	05_13	11_03	11_08	10_12	08_03
$1400\,s$	$4.57\,nm/s$	$6.54\,nm/s$	$7.23\,nm/s$	$6.44\,nm/s$	$6.65\,nm/s$	$6.66\,nm/s$
$140\,s$	$5.71\,nm/s$	$1.79\,nm/s$	$1.79\,nm/s$	$1.57\,nm/s$	$0.33\,nm/s$	$0.22\,nm/s$
$l_{Ge}\vert_{t_{RTA}=0\,s}$	$109.4\,\mu m$	$19.42\,\mu m$	$12.52\,\mu m$	$9.76\,\mu m$	$9.68\,\mu m$	$9.62\,\mu m$
$l_{Ge}\vert_{t_{RTA}=1540\,s}$	$102\,\mu m$	$10\,\mu m$	$2\,\mu m$	$0.5\,\mu m$	$0.15\,\mu m$	$50\,nm$

All devices were designed with the same cross-sectional area, so the diffusion rates were expected to be consistent across them. This was confirmed for devices 05_13, 11_08, 10_12, and 08_03 after an annealing time of $1400\,s$, where the diffusion rates were approximately $6.5\,nm/s$. After a further $140\,s$ of annealling, devices 05_13, 11_03, and 11_08 showed

comparable diffusion rates between $1.6\,nm/s$ and $1.8\,nm/s$. However, devices with shorter Ge segments (10_12 and 08_03) displayed signs of saturation, with significantly reduced diffusion rates of $0.33\,nm/s$ and $0.22\,nm/s$ respectively.
The main annealing phase ($1400\,s$) revealed diffusion rates varying from $4.57\,nm/s$ (device 03_00) to $7.23\,nm/s$ (device 11_03). During the final annealing step ($140\,s$), device 03_00 showed an unexpected increase to $5.71\,nm/s$, deviating from the theoretical $\sqrt{t}$ dependence. This anomaly might be attributed to measurement uncertainties in the SEM imaging of its relatively large structure.
Finally, the process of creating the Al-Ge-Al heterostructures was completed after obtaining a device with an ultra-short Ge segment measuring $50\,nm$, which was device 08_03. Lastly, the final SEM analysis of all devices revealed Ge segment lengths ranging from $50\,nm$ to $102\,\mu m$, and their SEM images are displayed in the second column of Fig. 4.1.

4.1.2 Al-Ge-Al SB-FETs with Top Gate Structures

After completing the formation of the Al-Ge-Al heterostructures with the desired lengths of the Ge segments, the device fabrication proceeded with the sputter deposition of Au reinforcement pads on top of the Al pads, followed by the vapor deposition of the Au top-gate structures. Fig. 4.2 presents an optical microscope image of the fully featured devices. Specifically, Fig. 4.2a displays a portion of the sample surface, featuring several top-gated Al-Ge-Al SB-FETs with varying channel lengths. Fig. 4.2b provides a close-up view of the channel section of a device.

(a) *(b)*

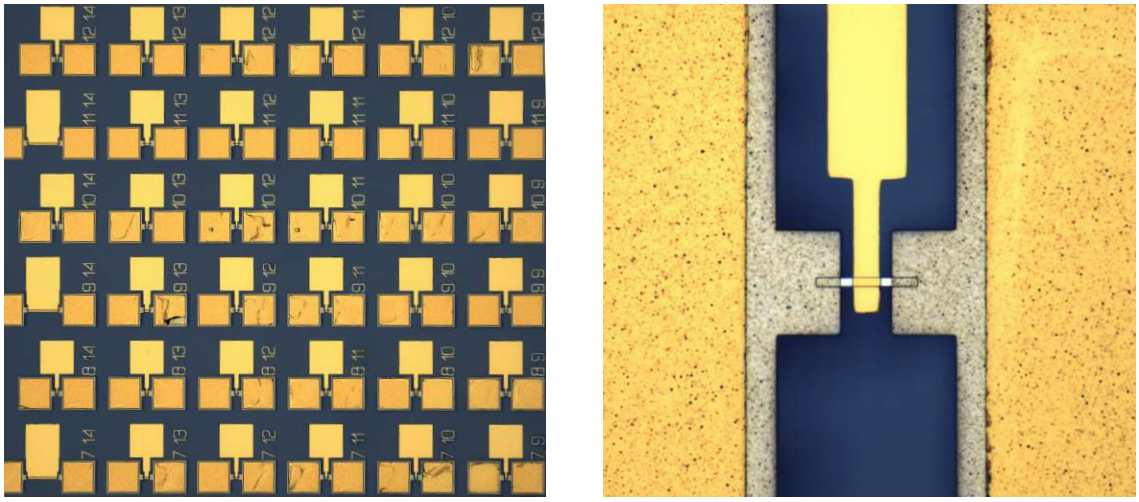

Figure 4.2: *Images of the finished sample obtained through optical microscopy. Image (a) displays a section of the sample surface, while (b) presents an enlarged view of a channel section within the device.*

4.2 Electrical Transport in Al-Ge-Al SB-FETs

This section presents a systematic investigation of the electrical transport properties in Al-Ge-Al SB-FETs, focusing on the relationship between device geometry, temperature, and charge carrier transport mechanisms. As detailed in Chapter 3.2, all measurements were conducted using device-specific parameters. The electrical characterization consisted of transfer and output measurements across various temperature ranges. For the transfer characteristics, bidirectional gate voltage sweeps were performed to investigate hysteresis effects. The temperature-dependent output characteristics were recorded at different gate voltages and are presented as logarithmic colormaps to visualize the dominant current transport regimes.
Output measurements above room temperature enabled the evaluation of the activation energy required for charge carrier injection. These results are presented as a function of gate voltage, both for zero bias and various drain-source voltages. The output characteristics measured at temperatures below room temperature allowed for the calculation of device resistivity, which was essential for modeling the device's I-V characteristics using the device equation.

4.2.1 Activation Energy for SB-FET's Charge Carrier Injection

To determine the activation energy needed to inject charge carriers into the device's channel, the output characteristics of the selected set of devices in Table 4.1 were recorded at temperatures of $295\,K$, $325\,K$, $350\,K$, $375\,K$, $382.5\,K$, and $400\,K$. This approach enabled the implementation of activation energy evaluation procedures, as outlined in Section 3.2.4.
For the analysis of the activation energy at $V_{DS} = 0\,V$, the evaluation was performed using the positive bias voltage regime. This choice was made to enable direct comparison with the transfer characteristics, which were consistently measured at fixed positive bias voltages.
A comprehensive comparison of the activation energies for all investigated devices, including both the complete gate-bias voltage dependence and the extrapolated zero-bias condition, is presented in Fig. A.1 found in Appendix A.

4.2.2 Temperature Dependent Transfer Characteristic Measurements

The modulation capability of the top-gated Al-Ge-Al SB-FETs was examined by sweeping the gate voltage while recording the channel current. The bias voltage V_{DS} was set dependent on the length of the Ge segment to maintain a constant electric field strength of $2 \cdot 10^2\, V/\mu m$ within the Ge segment.

4.2.2.1 Hysteresis Effects in the Transfer Characteristic

When a voltage is applied to the gate, an electric field forms within the oxide layer, attracting electric charges to the surface of the semiconductor. Due to the presence of interface traps at the Ge-Al_2O_3 interface, these traps become filled as a result of the electric field. Depending on the strength of the electric field, electric charges may tunnel further into the oxide, filling oxide states located deeper within the material. Oxide states typically exhibit long carrier lifetimes, greatly impacting the device's characteristics, see Section 2.4.1.1. [161]

When the measurement starts at $0\,V$, it is assumed that all the trap states in the Ge channel region have been depleted. As the gate voltage increases, these traps become filled with negative charges, creating an electric field. With a positive voltage applied to the gate, electrons compose the majority charge carriers. Consequently, the negatively charged traps effectively reduce the gate voltage. [135]
As the voltage is decreased and negative voltages are applied, the type of charge carriers transitions from electrons to holes. In this scenario, the previously filled negatively charged trap states enhance the hole-dominated current. Conversely, when the gate voltage is inverted, it initially depletes the traps. Subsequently, positive charges are attracted to the oxide layer, which fills these traps. Throughout the entire negative gate voltage range, holes remain the majority carriers. Consequently, the applied gate voltage reduces the modulation capability due to the accumulation of positively trapped charges at the Ge-Al_2O_3 interface. [135]

Due to the etching processes involved in the fabrication process, the increased surface roughness of the Ge sheets additionally contributes to the accumulation of surface states and the associated increase in hysteresis. Nevertheless, due to the low surface-to-volume ratio of the present structures, the impact of surface states is lower compared to NWs. [140, 162]

4.2.3 Temperature Dependent Output Characteristics

When examining electron current transport in SB-FETs, the contribution from thermionic emission increases as the bias voltage magnitude rises. Additionally, higher positive gate voltages shift the energy bands downward, enhancing the contributions from thermionic-field emission and field emission. These same considerations apply to hole transport processes, with the transport mechanisms operating under similar physical principles but at different voltage thresholds.
Due to Fermi level pinning close to the valence band, as discussed in Section 2.4.1.1, these devices exhibit inherent p-type behavior. Consequently, the Schottky barrier height for holes is significantly lower than for electrons. This asymmetry means that hole-dominated transport can be achieved with relatively modest negative gate voltages, while electron-dominated transport requires larger positive gate voltages to overcome the higher barrier.

4.2.3.1 Device Resistivity

It is possible to extract the device resistivity from the I-V curves when displayed individually for each gate voltage. For this purpose, the linear range of I_D is identified, which is located either in the positive or negative vicinity of $V_{DS} = 0\,V$, depending on which diode is limiting the current. The resistivity is expressed as $\rho_{Ge} = R_{Ge} \cdot A/l_{Ge}$, where R_{Ge} represents the series resistance of the channel. The value of R_{Ge} is determined as the inverse slope of the linear fit of I_D in the linear range of the I_D versus V_{DS} plot according to:

$$\rho_{Ge} = \left(\frac{\partial I_D}{\partial V_{DS}}\right)^{-1} \frac{A}{l_{Ge}}. \tag{4.1}$$

As the previously presented I-V characteristics were recorded for positive and negative bias voltages, two resistivity versus gate voltage and temperature graphs are obtained.

It's important to note that the resistance in Eq. 4.1 is determined as the gradient of I_D as a function of V_{DS}. This makes the results highly sensitive for measuring and evaluating faults. Additionally, determining the I-V characteristic requires long measurement times due to the often low currents observed, especially at low temperatures. The duration for which a specific voltage is applied to the gate during the I-V measurement affects the population of trap states, which significantly influences I_D and, in turn, the calculated resistivity.

4.2.3.2 Parameter Extraction using Thermionic Emission Device Modelling

In Section 2.4, Eq. 2.31 was introduced to model the current-voltage relationship based on thermionic emission theory. By utilizing the calculated device resistance, it is possible to adjust Equation 2.31 to better align with the measured I-V characteristics. This equation can be rewritten using the current I_D instead of the current density as follows:

$$V_{DS} = \frac{n_{fd} k_B T}{q} \ln\left(\frac{I_D}{I_{D0,fd}} + 1\right) - \frac{n_{rs} k_B T}{q} \ln\left(-\frac{I_D}{I_{D0,rs}} + 1\right) + R I_D. \tag{4.2}$$

The reverse saturation currents of the diode in the forward direction, denoted as $I_{D0,fd}$, and in the reverse direction, denoted as $I_{D0,rs}$, allow for the application of this equation to asymmetric devices. [131]
The ideality factors n_{fd} and n_{rs} for both the forward and reverse diodes will serve as fitting parameters to match the current-voltage relation in Eq. 4.2 with the measured current-voltage data. The ideality factor determines if the current emission at the Schottky interface is

primarily due to diffusion or tunneling, with tunneling current becoming more significant as the ideality factor increases. [49, 71, 129]

The following sections present a comprehensive analysis of four out of the six investigated devices. Their specific Ge segment lengths are $102\,\mu m$, $2\,\mu m$, $0.15\,\mu m$, and $50\,nm$. This selection spans from ultra-short channels ($l_{Ge} < 0.1\,\mu m$) to extended channel lengths ($l_{Ge} > 1\,\mu m$), enabling a thorough investigation of length-dependent transport mechanisms.
For each device, the analysis encompasses the activation energy for charge carrier injection, temperature-dependent transfer, output characteristics, device resistivity derived from output measurements, and subsequent modeling of the current-voltage characteristics. While all devices exhibit hysteresis effects in their transfer characteristics, the specific impact and extent of these effects are discussed individually.
Additional measurement results from devices with Ge segment lengths of $0.5\,\mu m$ and $10\,\mu m$ can be found in Appendix A.

4.2.4 SB-FET with a 100 μm long Ge Channel

This section examines device 03_00, which features the longest Ge segment analyzed with $l_{Ge} = 102\,\mu m$ and $w_{Ge} = 1.8\,\mu m$. This extended channel device serves as a baseline for understanding transistor behavior in a regime where the series resistance of the Ge segment dominates the transport characteristics.

Activation Energy

Fig. 4.3a shows the activation energy as a function of gate and bias voltage, represented as a color map. Given the substantial Ge segment length of $102\,\mu m$, the series resistance of the channel dominates over the Schottky barrier resistance. Therefore, the measured activation energies primarily reflect the channel properties rather than the Schottky barrier characteristics. The maximum value of the activation energy level $E_{A,eff}$ occurs at a gate voltage of approximately $0\,V$, indicating the intrinsic state where the device characteristics transition from p-type to n-type. [163]
When a negative gate voltage is applied, the energy bands are pulled upward, which lowers the barrier for holes. In contrast, applying a positive gate voltage pushes the bands downward, decreasing the barrier for electrons. Furthermore, blue shading indicates that holes compose the majority charge carriers, while red shading signifies that electrons compose the majority charge carriers.

As can be seen in Fig. 4.3a, activation energies between $-102\,meV$ and $292\,meV$ are found. The occurrence of negative barrier heights is generally associated with typical ohmic and quasi-ohmic contacts. [164] Since the Schottky barrier cannot be measured directly, determining the activation energy as a comparable parameter can yield negative values. The negative activation energy can be interpreted as a transparent barrier, and similar findings have been observed in other studies that utilized the same evaluation approach. [165, 166]
It can be observed, that under positive gate voltages and high bias voltage, $E_{A,eff}$ appears to decrease due to the enhanced field emission of electrons resulting from stronger band bending. In the negative range, a similar effect occurs with holes, although this appears to be less dependent on the bias voltage. A rough distinction between thermionic emission-dominated and field emission-dominated transport is illustrated by the dashed contour lines representing k_BT/q, which is $25.85\,meV$ at $300\,K$. [128] As described in Section 3.2.4, the resulting activation energy must be greater than k_BT/q for this evaluation process to yield reliable results.
The highest activation energy observed is approximately half the band gap of Ge ($\approx 0.66\,eV$). This suggests that the Fermi level of the metal is located near the mid-gap region of the semiconductor. However, an activation energy close to the band gap is expected due to the proven Fermi level pinning close to the valence band, as discussed in Section 2.3.2.

Fig. 4.3b displays the activation energy as a function of gate voltage at $V_{DS} = 0\,V$. This figure highlights the hole and electron transport regimes. The inset illustrates the band structure of a Schottky junction, depicting the transport of hole- and electron-dominated currents. Additionally, the transfer characteristic, represented by $|I_D\,(V_{TG})\,|$, at room temperature and a bias voltage of $1\,V$ is shown with a logarithmically scaled y-axis. These characteristics were recorded during a gate voltage sweep from $+5\,V$ to $-5\,V$, which aligns with the gate voltage sweep used to evaluate $E_{A,eff}$. This data illustrates the impact of activation energy on the current transport.

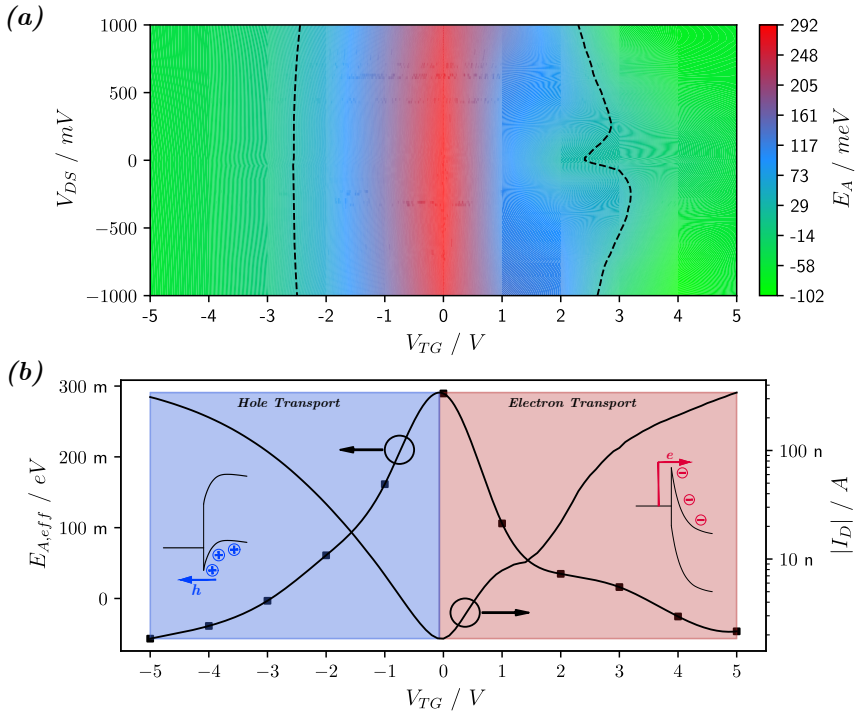

Figure 4.3: *Activation energy of device 03_00, with a Ge segment length of* $102\,\mu m$*. Subfigure (a) illustrates the activation energy as a function of* V_{TG} *and* V_{DS}*, represented in a colormap. The dashed contour lines represent the value of* k_BT/q *at* $300\,K$*, which is* $25.85\,meV$*. Subfigure (b) shows the activation energy evaluated for no bias voltage. Additionally, the transfer characteristic measured at room temperature with* $V_{DS} = 1\,V$*, obtained during the initial device testing, is included. The current is presented on a logarithmic scale. This transfer characteristic corresponds to the gate voltage sweep from* $+5\,V$ *to* $-5\,V$*. Image based on [167].*

Transfer Characteristics

The transfer characteristic of the device with a Ge segment length of $102\,\mu m$ is shown in Fig. 4.4. Fig. 4.4a presents the negative gate voltage regime, while Fig. 4.4b depicts the positive gate voltage regime. The current jumps in the courses of I_D at $4.8\,K$ and $50\,K$, observed at $\sim 200\,pA$ and $\sim 8\,nA$, were caused by the switching of the current measuring range. The sweeping direction is indicated by arrows, and the individual temperatures are represented by different colors.

When the gate voltage increases toward $+5\,V$, the energy bands bend downward. This leads to an increased emission of electrons and a higher energy barrier for holes, resulting in n-type characteristics. Vice versa, when a negative gate voltage is applied, the energy bands rise, increasing the barrier for electrons while lowering the barrier for holes. This results in p-type characteristics. The on-off ratios at various temperatures are listed in Table 4.3. The ratios in the hole-dominated and electron-dominated gate voltage ranges are displayed separately to allow for a clearer analysis of the distinct behaviors of hole current and electron current, respectively.

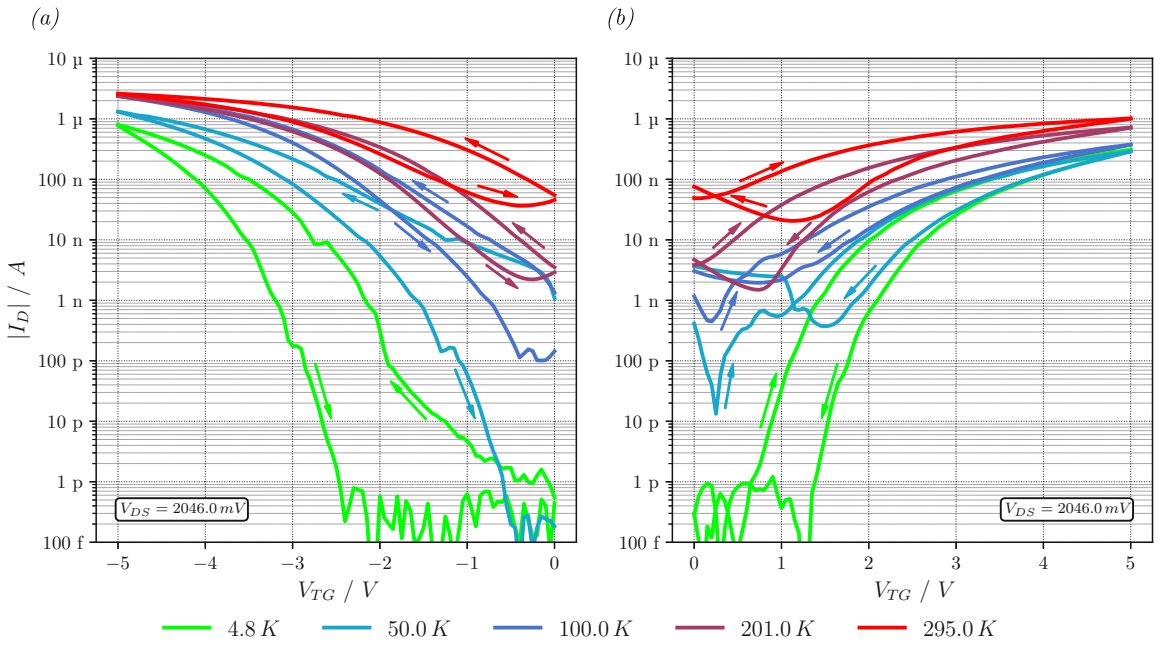

Figure 4.4: *The transfer characteristics of device 03_00 ($l_{Ge} = 102\,\mu m$) are presented as the absolute value of I_D in dependence of gate voltage and temperature. The temperature range spans from 295 K down to 4.8 K, and a bias voltage of 2046 mV applied. The sweeping direction is indicated by arrows, while individual temperatures are represented using different colors. Subfigure (a) illustrates the transfer characteristics in the negative gate voltage regime, while subfigure (b) presents the transfer characteristics in the positive gate voltage regime.*

Table 4.3: *Listing of the on-off ratios of device 03_00 ($l_{Ge} = 102\,\mu m$). The on-off ratios of I_D for the hole-dominated region ($V_{TG} < 0\,V$) as $I_{on,p}/I_{off}$ and for the electron-dominated region ($V_{TG} > 0\,V$) as $I_{on,n}/I_{off}$. I_{off} indicates the minimum current above the noise level achieved across the entire V_{TG} range.*

T	295 K	200 K	100 K	50 K	4.8 K
$\frac{I_{on,p}}{I_{off}}$	$1.3 \cdot 10^2$	$1.6 \cdot 10^3$	$2.4 \cdot 10^4$	$1.3 \cdot 10^7$	$8.0 \cdot 10^6$
$\frac{I_{on,n}}{I_{off}}$	$4.9 \cdot 10^1$	$4.8 \cdot 10^2$	$8.4 \cdot 10^2$	$2.9 \cdot 10^4$	$3.1 \cdot 10^6$

Considering the temperature behavior of the device, it is apparent that the current decreases as the temperature drops, following the typical temperature dependency of semiconductors. [71] As stated in Section 2.3.1.1, the charge carrier concentration in the conduction band diminishes with decreasing temperature, leading to a reduction of current through the channel of the device. However, the data shows that the current saturates for all temperatures at approximately $1\,\mu A$ to $6\,\mu A$ as the gate voltage approaches $-5\,V$, and at around $300\,nA$ to $1\,\mu A$ as the gate voltage approaches $+5\,V$. In this section, the activation energy is negative, which creates a transparent barrier and further reveals the channel resistance of the device. The Ge segment of this device is notably large, which means that its series resistance has a significant impact compared to the resistances of the Schottky diodes. At high gate voltages ($V_{TG} = \pm 5\,V$), the barriers are effectively lowered, and the temperature dependence primarily reflects the freeze-out of charge carriers in the semiconductor channel. In contrast, near $V_{TG} = 0\,V$, the temperature dependence is dominated by the Schottky barrier, resulting in on-off ratios that increase from one to two orders of magnitude at room temperature to

six orders of magnitude at $4.8\,K$. At these low temperatures and $V_{TG} = 0\,V$, transport is dominated by tunneling through the barrier, resulting in very low current levels.

Hysteresis Effects

Examining the transfer characteristic at $295\,K$ in Fig. 4.4b reveals clear hysteresis effects. When the measurement begins at $0\,V$, the initially depleted trap states in the metal-oxide-semiconductor region result in an immediate current increase. As the gate voltage rises, electrons gradually fill these trap states, effectively reducing the gate field and resulting in lower current during the reverse sweep from $+5\,V$ to $0\,V$.
During the subsequent sweep from $0\,V$ to $-5\,V$, the previously trapped negative charges enhance the hole-dominated current. When sweeping back from $-5\,V$ to $0\,V$, the repulsion of trapped electrons by the negative gate voltage leads to a significantly reduced current compared to the forward sweep.
This hysteresis behavior, which originates from charge trapping at the Ge-Al_2O_3 interface, persists throughout the entire temperature range.

Output Characteristics

The I-V characteristics were recorded during a bias voltage sweep from $-500\,mV$ to $+500\,mV$. The gate voltage was increased in $1\,V$ steps, ranging from $+5\,V$ to $-5\,V$, after each bias voltage sweep. In Fig. 4.5, the I-V characteristics are presented at temperatures of $295\,K$, $200\,K$, $100\,K$, $50\,K$, $10\,K$ and $4.7\,K$. The absolute value of I_D is displayed using a logarithmically scaled colormap.

The colormaps indicate that the area with the smallest current, from the perspective of the gate voltage, shifts from approximately $0\,V$ at room temperature to around $+3\,V$ at $4\,K$. Meanwhile, the electron-dominated current continues to increase from room temperature down to $100\,K$, after which it begins to decrease as the temperature drops further to $4.8\,K$. This behavior is evident in the linearly scaled I_D curves. The lowest recorded current occurs at $200\,K$. These observations, along with the extended measuring times, indicate that the oxide trap-filling state has a significant impact on the measurement results.

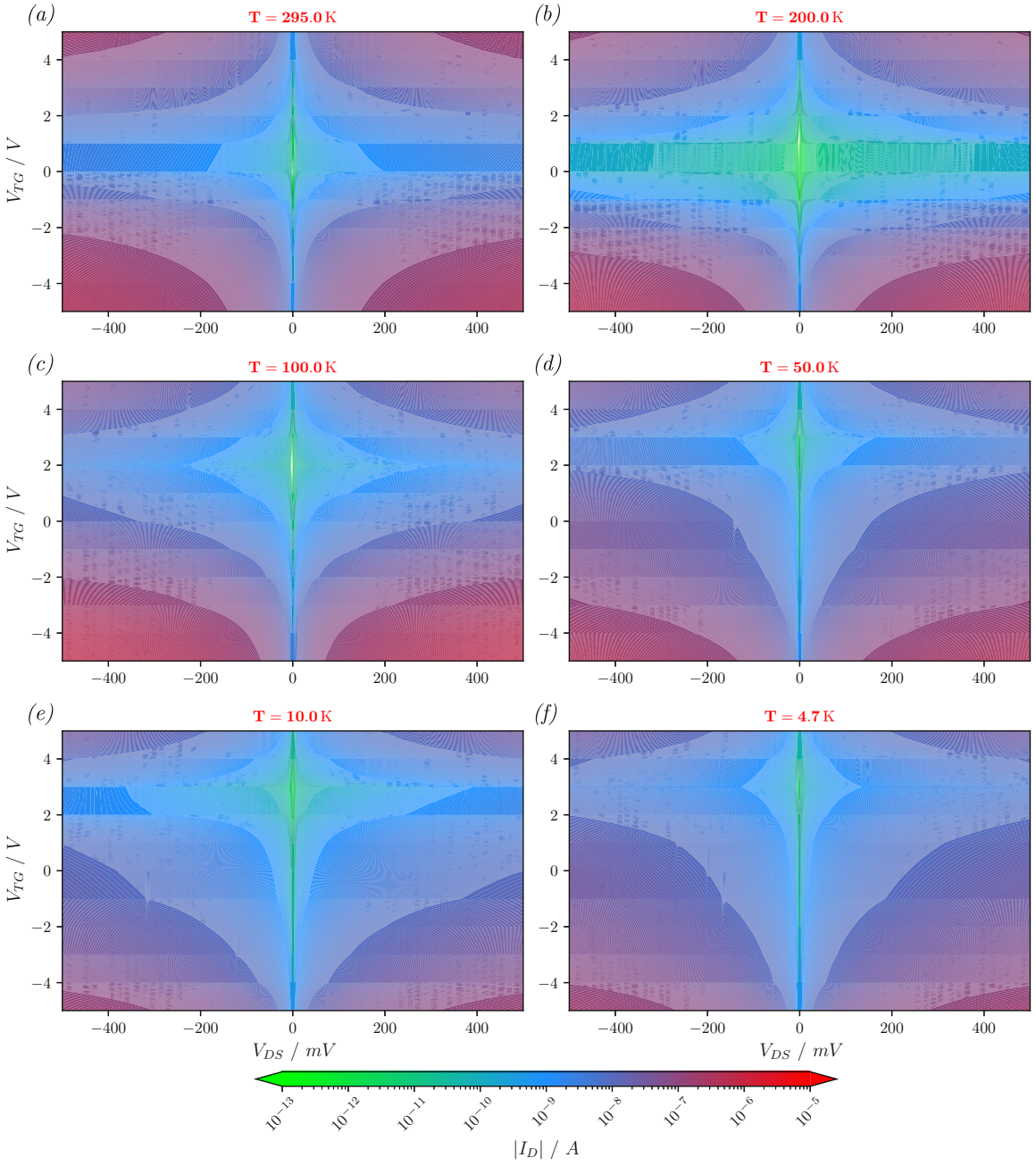

Figure 4.5: *The I-V characteristics of device 03_00 ($l_{Ge} = 102\,\mu m$) are presented as a function of temperature, bias, and top-gate voltage, shown as $|I_D\,(V_{DS}, V_{TG})\,|$ in a logarithmically scaled colormap. The temperature dependence can be understood by interpreting each subplot from top to bottom as corresponding to decreasing temperature.*

Device Resistivity

Fig. 4.6 presents the resistivity as a function of temperature and gate voltage for positive bias voltages. The resistivities measured from room temperature down to 4.8 K were obtained from the I-V characteristics depicted in Fig. 4.5. For temperatures between room temperature and 400 K, the resistivities were extracted from the I-V characteristics that were used to evaluate the activation energy.

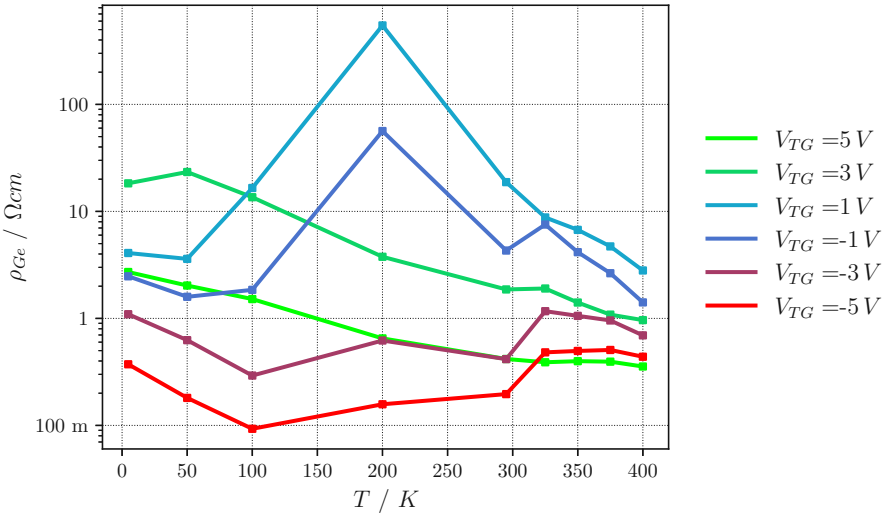

Figure 4.6: *Device resistivity of device 03_00 ($l_{Ge} = 102\,\mu m$) as a function of temperature and top-gate voltage calculated on the linear portion of the previously recorded I-V characteristics. The gate voltage ranges from $-5\,V$ to $+5\,V$, with a voltage spacing of $2\,V$, while the temperature varies from 4.8 K to 400 K. ρ_{Ge} is presented in a logarithmic format.*

Typically, a quasi-constant resistivity is observed for gate voltages ranging from $-3\,V$ to $-5\,V$. This stability is attributed to the quasi-ohmic barrier for holes, which remains nearly independent of temperature. A similar behavior is observed for positive gate voltages between $+3\,V$ and $+5\,V$, where only a slight increase in resistivity is noticeable as the temperature decreases.

Ideality Factor Extraction

Fig. 4.7 presents the I-V characteristics measured at various temperatures, compared with the calculated I-V characteristics (indicated by circles) according to Eq. 4.2.

The ideality factors used for fitting Eq. 4.2 are displayed individually for each bias voltage regime as inset, where n_{fd} represents the ideality factor of the diode in forward direction and n_{rs} corresponds to the diode in reverse direction. As discussed in Section 2.3.3, these factors provide insight into the dominant transport mechanisms at the Schottky interface. While the model achieves good agreement with the experimental data across the entire temperature range, even down to 4.8 K, the extracted ideality factors are notably high, particularly for the forward direction.

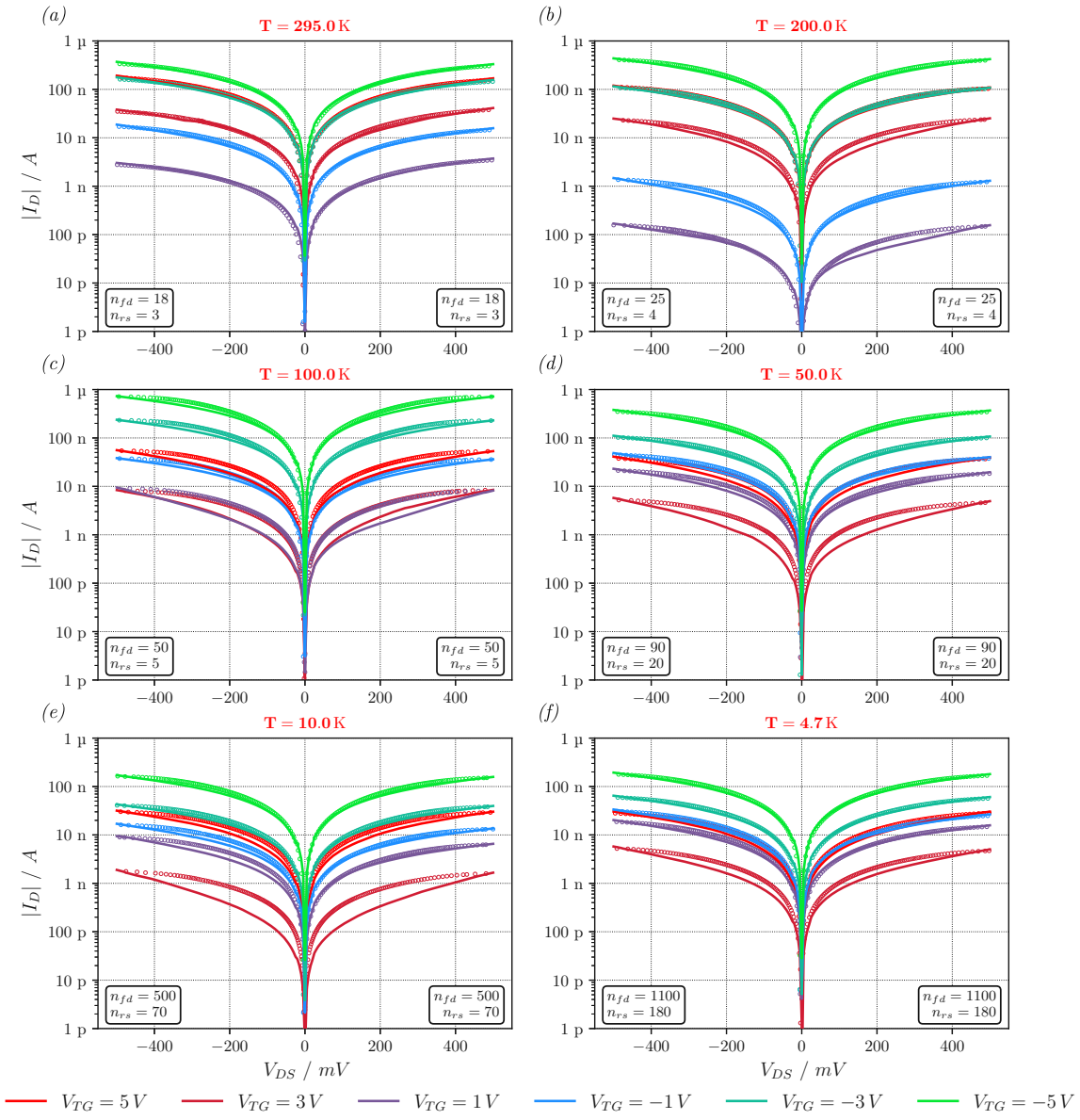

Figure 4.7: *Semilogarithmic plot of the I-V characteristics of device 03_00 ($l_{Ge} = 102\,\mu m$) at various temperatures. The circles indicate the I-V characteristics derived from the back-to-back Schottky diode device equation. Additionally, the fitting parameters related to the ideality factors are shown in the inset. Each subplot corresponds to a specific temperature at which the measurements were taken, ranging from 295 K down to 4.7 K. Image based on [132].*

At room temperature, where the most physically meaningful values are obtained, n_{rs} is approximately 3, which is reasonably close to the behavior of common devices, while n_{fd} reaches 18. These elevated values likely reflect both the limitations of the simplified back-to-back diode model and the complex nature of the actual transport mechanisms. [49, 71, 131] The values shown in the insets exhibit a further systematic increase at lower temperatures, which might be an indication of the known transition to tunneling-dominated transport where thermal excitation of carriers becomes negligible.

4.2.5 SB-FET with a 2 μm long Ge Channel

Device 11_03, with $l_{Ge} = 2\,\mu m$ and $w_{Ge} = 1.78\,\mu m$, represents an intermediate regime where both long-channel and short-channel effects may be observed. This section analyzes its electrical characteristics to identify the transition between transport regimes.

Activation Energy

Fig. 4.8 presents the results of evaluating the activation energy. Specifically, Fig. 4.8a shows the activation energy as a function of gate and bias voltage, displayed as a color map. Fig. 4.8b illustrates the activation energy assessed at $V_{DS} = 0\,V$, highlighting the p-type and n-type regimes. Additionally, the transfer characteristic at $295\,K$, biased with $100\,mV$ is included for reference.

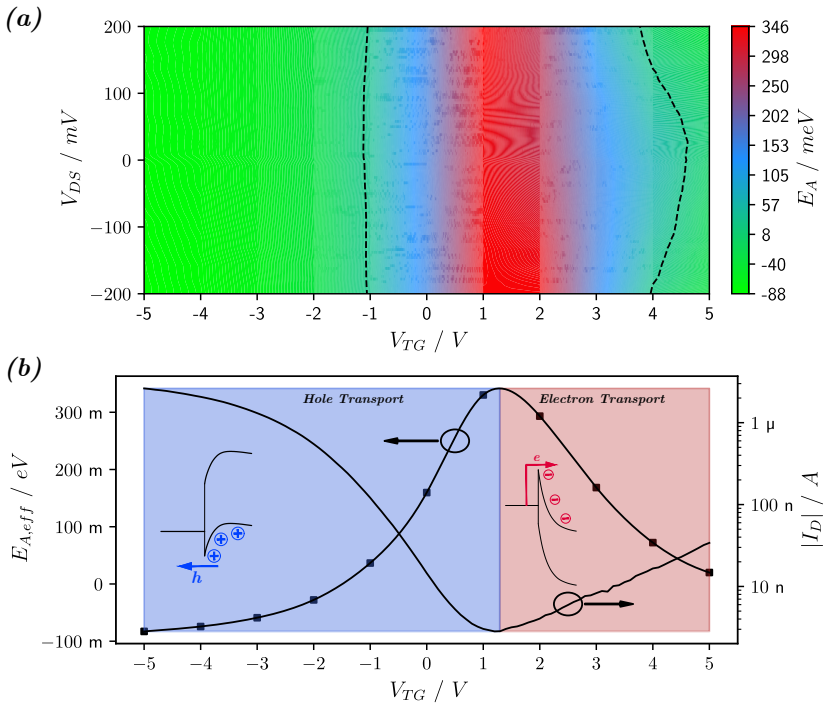

Figure 4.8: *Activation energy of device 11_03, with a Ge segment length of 2 µm. Subfigure (a) illustrates the activation energy as a function of V_{TG} and V_{DS}, represented in a colormap. The dashed contour lines represent the value of k_BT/q at 300 K, which is 25.85 meV. Subfigure (b) shows the activation energy evaluated for no bias voltage. Additionally, the transfer characteristic measured at room temperature with $V_{DS} = 100\,mV$, obtained during the initial device testing, is included. The current is presented on a logarithmic scale. This transfer characteristic corresponds to the gate voltage sweep from $+5\,V$ to $-5\,V$. Image based on [167].*

The activation energies shown in Fig. 4.8a range from $-88\,meV$ at a gate voltage of $-5\,V$ to $346\,meV$ at gate voltages between $1\,V$ and $2\,V$. In Fig. 4.8b, the evaluation conducted at zero bias voltage revealed a minimum activation energy of $81\,meV$ and a maximum of $339\,meV$. These values are consistent with those reported by Böckle [168] for back-gated SB-FETs fabricated on the same material system with comparable dimensions. Notably, the activation energy determined at the intrinsic point in this context is higher than that observed in the device with a Ge segment length of $102\,\mu m$ and has shifted slightly into the positive gate voltage region.

As the channel length decreases, the resistance of the Schottky contacts becomes more significant compared to the channel resistance. Due to the Fermi level pinning being close to the valence band, the barrier for holes is generally low, while the barrier for electrons is high. This effect is especially noticeable in the positive gate voltage region, where the intrinsic point signals a higher barrier for electron-dominated current transport and a lower barrier for hole-dominated current transport.

Transfer Characteristics

Fig. 4.9 shows the transfer characteristic as the absolute value of I_D in relation to V_{TG}. In Fig. 4.9a, the data corresponds to the negative gate voltage regime, while Fig. 4.9b illustrates the positive gate voltage regime. The sweeping direction is indicated by arrows, and different colors represent the individual temperatures.

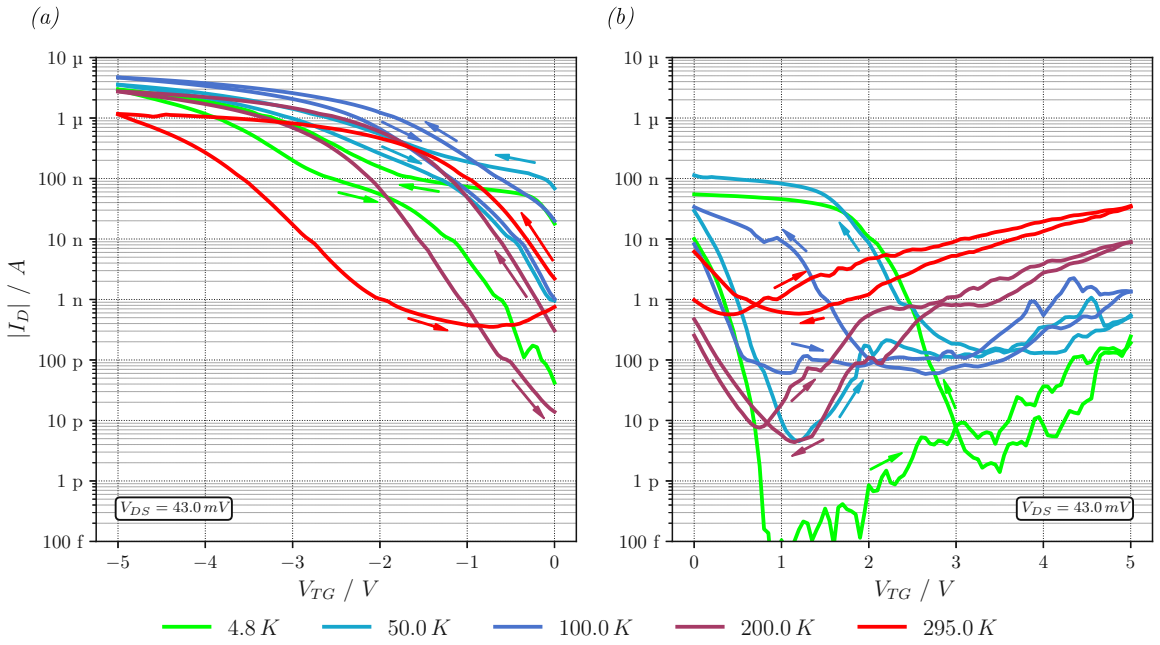

Figure 4.9: *The transfer characteristics of device 11_03 ($l_{Ge} = 2\,\mu m$), biased with $43\,mV$, are presented as a function of gate voltage and temperature. The sweeping direction is indicated by arrows, while individual temperatures are represented using different colors. The temperature range spans from $295\,K$ down to $4.8\,K$. Subfigure (a) illustrates the transfer characteristics in the negative gate voltage regime, while subfigure (b) presents the transfer characteristics in the positive gate voltage regime.*

When comparing the positive gate voltage regime of this device with that of the longest device shown in Fig. 4.4b, it becomes evident that the electron-dominated transport exhibits much stronger temperature dependence. This is noticeable as the current decreases from approximately $30\,nA$ at a gate voltage of $+5\,V$ at room temperature to around $200\,pA$ at $4.8\,K$, due to the activation energy required for electron injection. Additionally, a positive activation energy is noted in the positive gate voltage regime (see Fig. 4.8), indicating that the barrier for electrons persists. In contrast, the current at a gate voltage of $-5\,V$ appears to be nearly independent of temperature, due to a negative activation energy, as shown in Fig. 4.8. This effect significantly influences the on-off ratios shown in Table 4.4, where the on-off ratio is considerably larger in the p-type regime than in the n-type regime.

Table 4.4: *Listing of the on-off ratios of device 11_03 ($l_{Ge} = 2\,\mu m$). The on-off ratios of I_D for the hole-dominated region ($V_{TG} < 0\,V$) as $I_{on,p}/I_{off}$ and for the electron-dominated region ($V_{TG} > 0\,V$) as $I_{on,n}/I_{off}$. I_{off} indicates the minimum current above the noise level achieved across the entire V_{TG} range. For $I_{on,p}$, the value of I_D at $V_{TG} = -5\,V$ was used, while for $I_{on,n}$, the value of I_D at $V_{TG} = +5\,V$ was used.*

T	$295\,K$	$200\,K$	$100\,K$	$50\,K$	$4.8\,K$
$\frac{I_{on,p}}{I_{off}}$	$3.3 \cdot 10^3$	$6.3 \cdot 10^5$	$8.0 \cdot 10^4$	$7.9 \cdot 10^5$	$3.0 \cdot 10^7$
$\frac{I_{on,n}}{I_{off}}$	$6.2 \cdot 10^1$	$2.0 \cdot 10^3$	$2.3 \cdot 10^1$	$1.2 \cdot 10^2$	$1.9 \cdot 10^3$

Hysteresis Effects

In Fig. 4.9, it is evident that the transfer characteristics show a temperature dependence, which is not observed in the longest device. This is particularly noticeable as the hysteresis significantly increases when the temperature drops below $100\,K$. Although the electron-dominated current decreases in the positive gate voltage regime with falling temperatures, the hole-dominated current experiences a dramatic increase of five orders of magnitude when the gate voltage is swept from $+5\,V$ back to $0\,V$. This behavior is illustrated in the transfer characteristic depicted in Fig. 4.9b at $4.8\,K$.
Moreover, it is noticeable that the transition from n-type to p-type behavior occurs at $\sim 3.5\,V$, compared to around $1\,V$ at room temperature. This phenomenon may be due to the temperature dependence of carrier lifetime in traps. As the temperature decreases, the carrier lifetime increases significantly. [118] This also affects the negative gate voltage regime, as the hole-dominated current continues to be enhanced. Consequently, the hole-driven currents at negative gate voltages observed at low temperatures are slightly higher than those at room temperature.

Output Characteristics

The I-V characteristics shown in Fig. 4.10 were obtained by measuring the channel current over a bias voltage range of $-100\,mV$ to $+100\,mV$, while varying the gate voltage from $+5\,V$ to $-5\,V$ in $1\,V$ increments. These characteristics were recorded at temperatures of $295\,K$, $200\,K$, $100\,K$, $50\,K$, and $4.7\,K$.
In this device, hole-dominated current transport is more pronounced across the entire temperature range. It appears to increase as the temperature decreases from $295\,K$ to $100\,K$, after which it declines as the temperature continues to drop. In contrast, the electron-dominated current gradually decreases as the temperature lowers.
It can be observed that the area of the lowest shift changes from approximately $1\,V$ at room temperature to around $2\,V$ to $3\,V$.

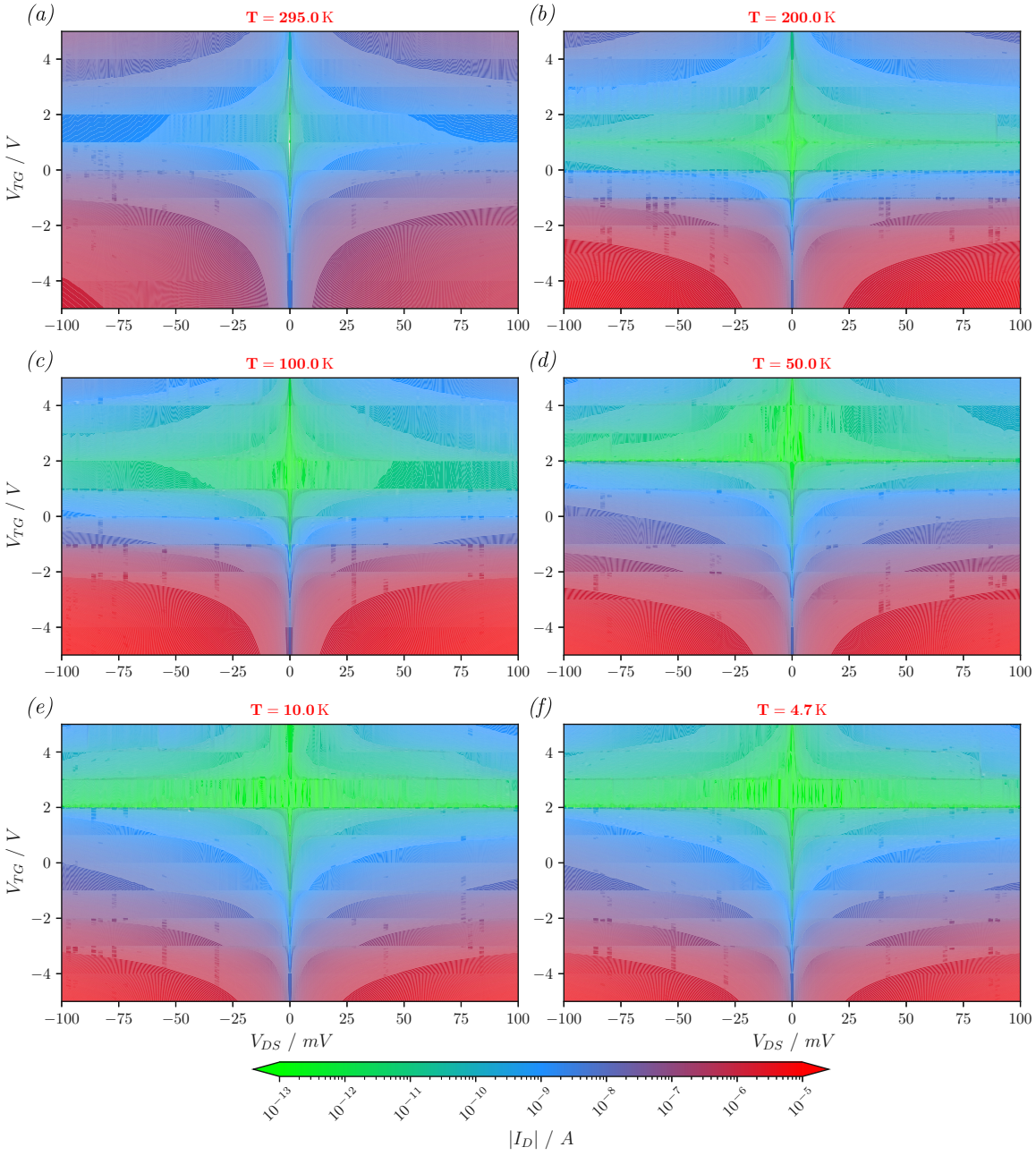

Figure 4.10: *The I-V characteristics of device 11_03 ($l_{Ge} = 2\,\mu m$) are presented as a function of temperature, bias, and top-gate voltage, shown as $|I_D\,(V_{DS}, V_{TG})\,|$ in a logarithmically scaled colormap. The temperature dependence can be understood by interpreting each subplot from top to bottom as corresponding to decreasing temperature. Image based on [128].*

Device Resistivity

The resistivity of the device with a channel length of $2\,\mu m$ is presented as a function of temperature and gate voltage in Fig. 4.11. This analysis spans a temperature range from $4.8\,K$ to $400\,K$, with the gate voltage varying between $-5\,V$ and $+5\,V$ in $2\,V$ increments. The resistivity values are plotted on a logarithmic scale on the y-axis.
The resistivity values between room temperature and $4.8\,K$ were derived from the I-V characteristics shown in Fig. 4.10. For temperatures ranging from room temperature to $400\,K$, the resistivities were calculated based on the I-V characteristics used to evaluate the activation energy.

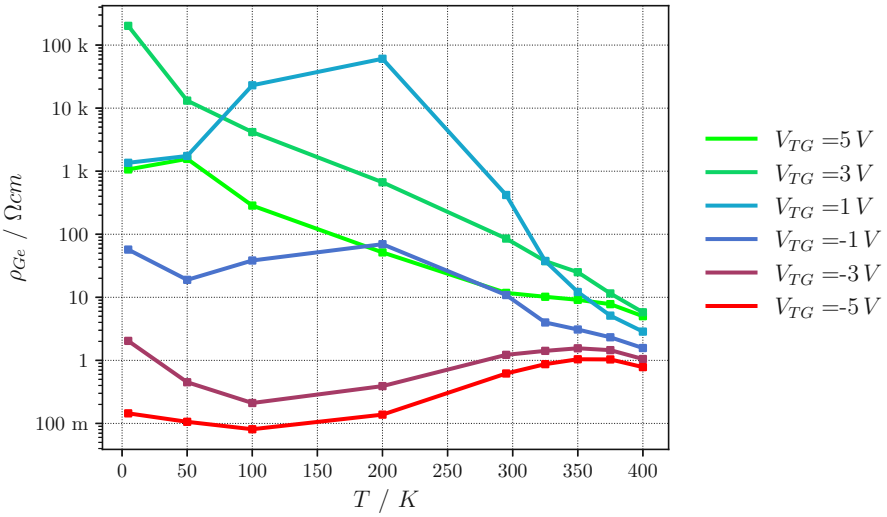

Figure 4.11: *Device resistivity of device 11_03 ($l_{Ge} = 2\,\mu m$) as a function of temperature and top-gate voltage calculated on the linear portion of the previously recorded I-V characteristics. The gate voltage ranges from $-5\,V$ to $+5\,V$, with a voltage spacing of $2\,V$, while the temperature varies from $4.8\,K$ to $400\,K$. ρ_{Ge} is presented in a logarithmic format.*

At $400\,K$, it is evident that resistivities increase as the temperature drops. Notably, for the electron-dominated current at higher positive gate voltages, there is a significant rise in resistivity, which extends the range of resistivity values compared to those measured at other gate voltages. In contrast, the resistivity for $V_{TG} = -5\,V$ shows a slight decrease as the temperature drops. This trend aligns with observations from the transfer characteristics, where a higher hole-dominated current was observed at lower temperatures.

Ideality Factor Extraction

Fig. 4.12 illustrates the I-V characteristics as a function of gate and bias voltage. The characteristics are represented by continuous lines that correspond to the first column of Fig. 4.10. In this presentation, the characteristics are shown as the absolute value of I_D, with the y-axis displayed on a logarithmic scale. The circles represent the I-V characteristics modeled according to Eq. 4.2. The temperature dependence can be observed by examining the individual subplots. The forward and reverse ideality factors used for fitting Eq. 4.2 are presented as insets in the individual subplots.

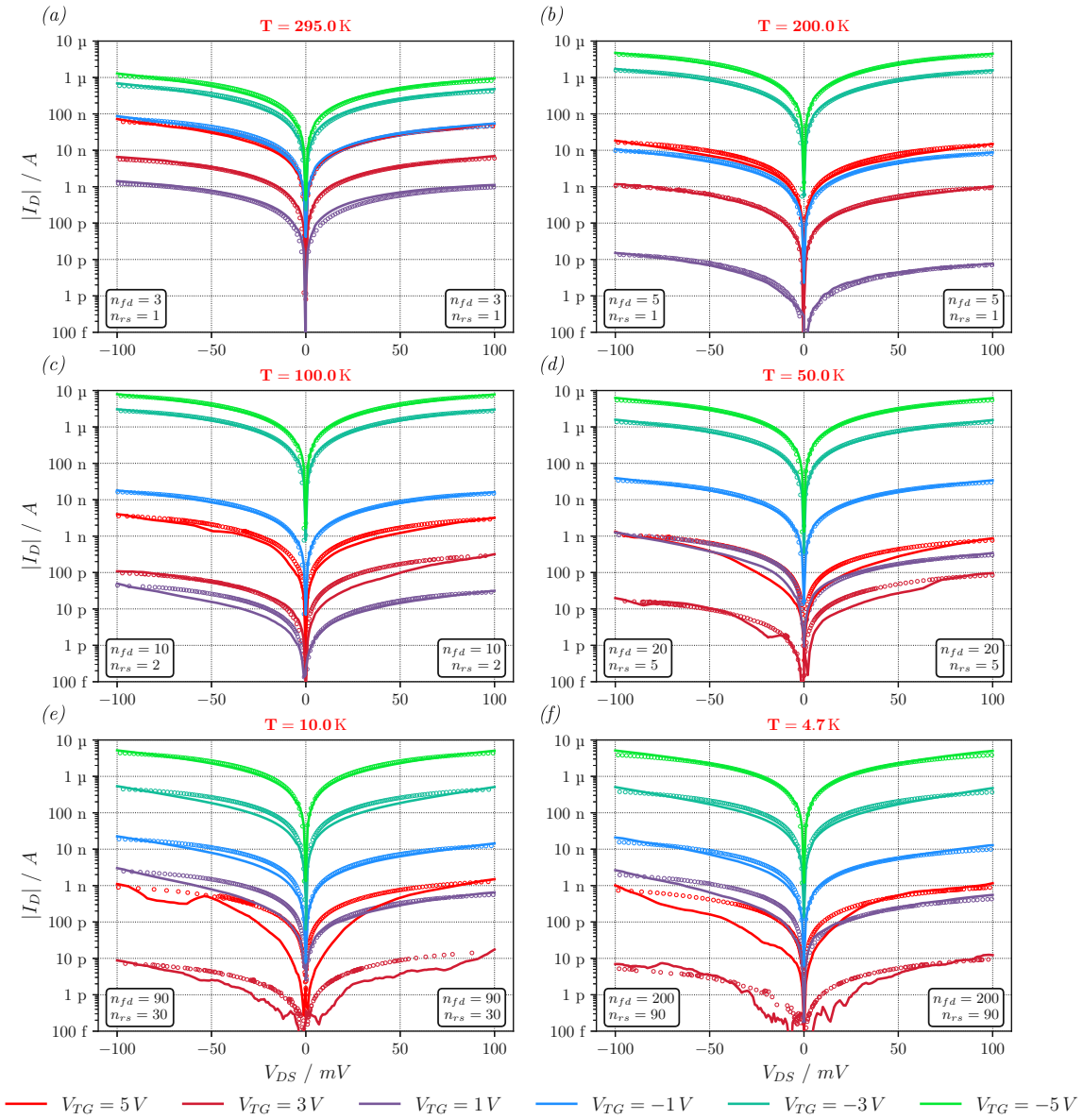

Figure 4.12: *Semilogarithmic plot of the I-V characteristics of device 11_03 ($l_{Ge} = 2\,\mu m$) at various temperatures. The circles indicate the I-V characteristics derived from the back-to-back Schottky diode device equation. Additionally, the fitting parameters related to the ideality factors are shown in the inset. Each subplot corresponds to a specific temperature at which the measurements were taken, ranging from 295 K down to 4.7 K. Image based on [132].*

Due to the larger on-off ratios observed in this device, the I-V characteristics encompass a wider range of currents. Despite the noisy I-V characteristics at very low currents, especially at high gate voltages and low temperatures (see Fig. 4.12e-f), the I-V characteristic fitting performed effectively. Notably, this device exhibits significantly lower ideality factors compared to the 102 μm device, with n_{rs} approaching the ideal value of 1 at room temperature and 200 K. This reduction in ideality factors might reflect the transition from channel-dominated to barrier-dominated transport as the Ge segment length decreases and the series resistance of the channel becomes less significant.

4.2.6 SB-FET with a 0.15 μm long Ge Channel

Device 10_12 features a Ge segment with $l_{Ge} = 0.15\,\mu m$ and $w_{Ge} = 1.82\,\mu m$, placing it well within the short-channel regime. The analysis focuses on the distinct transport phenomena that emerge at this scale, including space-charge-limited current transport.

Activation Energy

Fig. 4.13 shows the results of determining the activation energy for the device with a Ge segment length of $0.15\,\mu m$. In subfigure Fig. 4.13a, the activation energy is shown as a function of gate and bias voltage. Subfigure Fig. 4.13b, displays the activation energy evaluated at $V_{DS} = 0\,V$, emphasizing the p-type and n-type regimes. For reference, the transfer characteristic at $295\,K$, biased with $1\,mV$, is included. The current is shown as the absolute value $|I_D\,(V_{TG})\,|$ and is presented on a logarithmic scale.

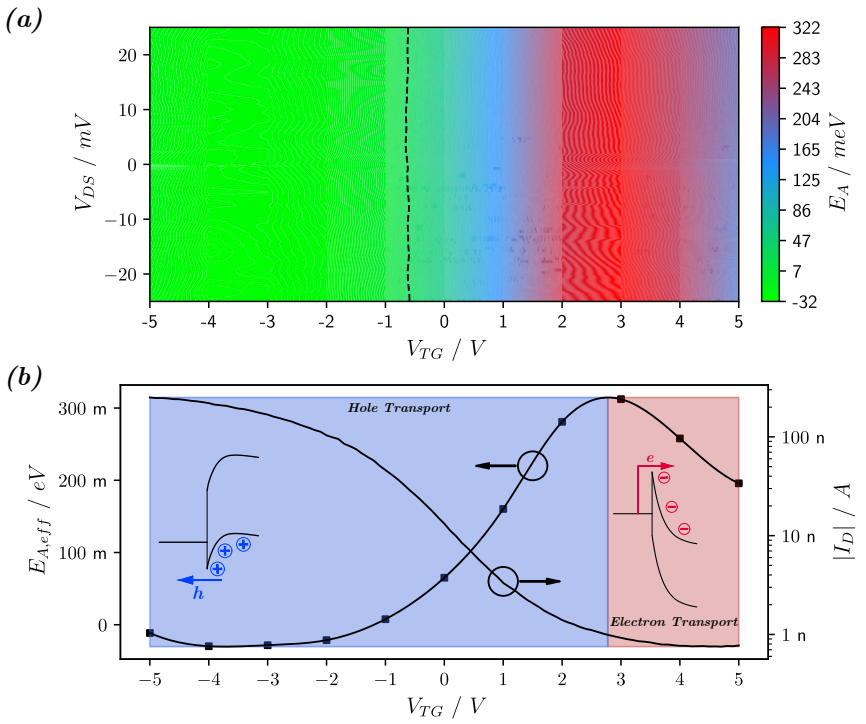

Figure 4.13: *Activation energy of device 10_12, with a Ge segment length of* $0.15\,\mu m$. *Subfigure (a) illustrates the activation energy as a function of* V_{TG} *and* V_{DS}, *represented in a colormap. The dashed contour lines represent the value of* k_BT/q *at* $300\,K$, *which is* $25.85\,meV$. *Subfigure (b) shows the activation energy evaluated for no bias voltage. Additionally, the transfer characteristic measured at room temperature with* $V_{DS} = 1\,mV$, *obtained during the initial device testing, is included. The current is presented on a logarithmic scale. This transfer characteristic corresponds to the gate voltage sweep from* $+5\,V$ *to* $-5\,V$. *Image based on [167].*

In Fig. 4.13a, an activation energy ranging from $-32\,meV$ at a gate voltage of $-5\,V$ to $322\,meV$ at a gate voltage of $\sim 3\,V$ is determined. In Fig. 4.13b, the evaluation conducted at zero bias voltage revealed a minimum activation energy of $-30\,meV$ and a maximum of $315\,meV$. The activation energy determined at the intrinsic point in this context is again lower than that observed in the device with a Ge segment length of $2\,\mu m$ and is further shifted into the positive gate voltage region.

The position of the maximum activation energy in the positive gate voltage region is consistent with the Fermi level pinning near the valence band, which naturally results in a low barrier for holes and a high barrier for electrons. While negative gate voltages can further reduce the already low hole barrier, the high electron barrier remains difficult to modulate effectively within the investigated gate voltage range. Only at gate voltages above $+3\,V$ does the electron barrier begin to decrease, highlighting the strong impact of Fermi-level pinning on the device's transport characteristics.

Transfer Characteristics

The temperature-dependent transfer characteristics for a $0.15\,\mu m$ Ge segmented device are presented in Fig. 4.14. In Fig. 4.14a, the negative gate voltage regime is displayed, while the positive gate voltage regime can be seen in Fig. 4.14b. Arrows indicate the sweeping direction, while different colors represent individual temperatures. Additionally, the inset band structures illustrate the band bending in dependence on the gate voltage.

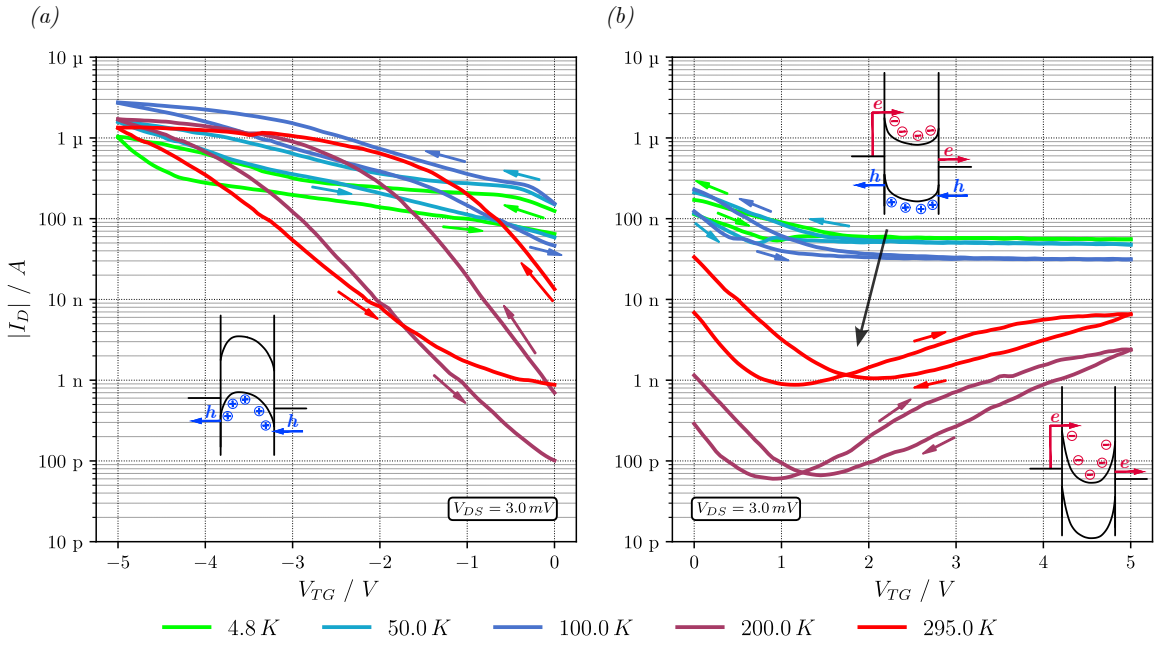

Figure 4.14: *Transfer characteristic of device 10_12 ($l_{Ge} = 0.15\,\mu m$) as a function of T, at the temperatures of 4.8 K, 50 K, 100 K, 200 K, and 295 K. Subplot (a) displays the negative top-gate voltage range, while subplot (b) presents the positive top-gate voltage range. The directions of the V_{TG} sweeps are indicated by arrows. The inset band structure in (a) shows a scenario where hole-dominated current transport is favored by band bending. In contrast, the inset band structure in the bottom right corner of (b) illustrates a situation where electron-dominated current transport is favored by band bending. Additionally, the inset band structure in (b) that includes both electron and hole current transport indicates the transition from hole-dominated to electron-dominated current transport.*

The on-off ratios for hole-dominated and electron-dominated currents, derived from Fig. 4.14, are presented in Table 4.5.

Table 4.5: *Listing of the on-off ratios of device 10_12 ($l_{Ge} = 0.15\,\mu m$). The on-off ratios of I_D for the hole-dominated region ($V_{TG} < 0\,V$) as $I_{on,p}/I_{off}$ and for the electron-dominated region ($V_{TG} > 0\,V$) as $I_{on,n}/I_{off}$. I_{off} indicates the minimum current above the noise level achieved across the entire V_{TG} range. For $I_{on,p}$, the value of I_D at $V_{TG} = -5\,V$ was used, while for $I_{on,n}$, the value of I_D at $V_{TG} = +5\,V$ was used.*

T	$295\,K$	$200\,K$	$100\,K$	$50\,K$	$4.8\,K$
$\frac{I_{on,p}}{I_{off}}$	$1.5 \cdot 10^3$	$2.8 \cdot 10^4$	$8.8 \cdot 10^1$	$3.3 \cdot 10^1$	$1.9 \cdot 10^1$
$\frac{I_{on,n}}{I_{off}}$	$7.4 \cdot 10^0$	$4.0 \cdot 10^1$	$1.0 \cdot 10^0$	$1.0 \cdot 10^0$	$1.0 \cdot 10^0$

In Fig. 4.14a, the saturation of current remains temperature-independent and is clearly observed around a gate voltage of $-5\,V$, as this device also exhibited a negative activation energy in the negative gate voltage region (see Fig. 4.13a). Specifically, this device saturates at approximately $1\,\mu A$ to $3\,\mu A$, which is consistent with the saturation levels observed in the longer devices previously discussed. Since the same electric field strength was applied to all devices, this resulted in a similar absolute value of I_D.
However, this device exhibits unusual behavior at temperatures below $200\,K$, as shown in Fig. 4.14b. Specifically, when the temperature decreases from $200\,K$ to $100\,K$, the current increases by at least two orders of magnitude. After this transition, the current appears to be widely independent of the gate voltage V_{TG}.
As the temperature drops, the carrier density decreases (see Eqs. 2.20 and 2.21), which reduces the scattering of charge carriers and enhances conductivity. Simultaneously, the depletion zones of both Schottky contacts expand according to Eq. 2.7, eventually leading to their overlap. This suggests that the punch-through effect, which results in a drain-source leakage current, may be occurring. This phenomenon will be discussed further below.

Hysteresis Effects

Compared to device 11_03, which has a Ge segment length of $2\,\mu m$, the impact of surface states is slightly reduced. However, as mentioned earlier, for temperatures below $200\,K$, the current cannot be modulated with gate voltages greater than approximately $1.5\,V$. Consequently, the current is not significantly affected by traps located between the Ge channel and the top gate electrode. Below around $1.5\,V$, a slight hysteresis and the ability to modulate current based on gate voltage can be observed. Nonetheless, the most significant hysteresis occurs at room temperature.

Output Characteristics

The I-V characteristics presented in Fig. 4.15 were obtained from a bias voltage sweep ranging from $-20\,mV$ to $+20\,mV$, while varying gate voltages between $+5\,V$ and $-5\,V$. The measurement results are displayed for temperatures of $295\,K$, $200\,K$, $100\,K$, $50\,K$ and $4.7\,K$. The increase in current due to the overlap of the depletion zones is visible in the colormaps at $200\,K$ (Fig. 4.15d) and $100\,K$ (Fig. 4.15f). For positive gate voltages, the current cannot be further modulated, which is evident as the contour lines become more linear on the y-axis.

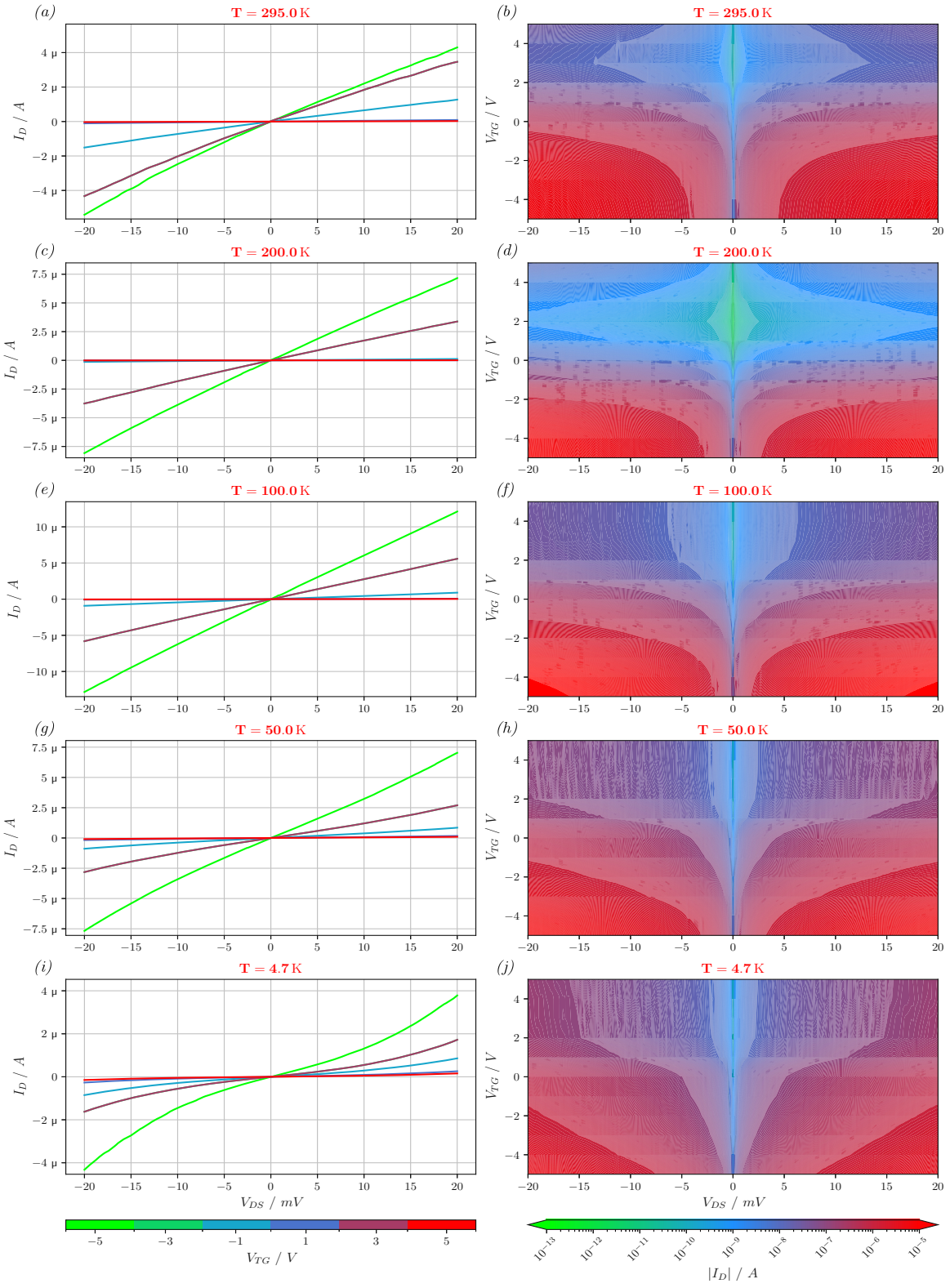

Figure 4.15: *The I-V characteristics of device 10_12 ($l_{Ge} = 0.15\,\mu m$) are shown as a function of temperature, bias, and top-gate voltage. In the first column, the I-V characteristic $I_D\,(V_{DS})$ is displayed with a linearly scaled y-axis, featuring separate lines for each gate voltage. A gate voltage spacing of $2\,V$ is utilized. The second column presents the I-V characteristics as $|I_D\,(V_{DS}, V_{TG})|$ in a logarithmically scaled colormap. The temperature dependence can be understood by interpreting each subplot from top to bottom as corresponding to decreasing temperature. Image based on [128].*

In general, strong non-linearities in the linearly scaled I-V characteristics were not observed. The apparent linear behavior may be due to the selected range of bias voltage. Furthermore, because the I_D axis is scaled linearly, only the I-V characteristics at high negative or positive gate voltages can be analyzed for linearity. However, at temperatures of $4.8\,K$ (see Fig. 4.15i) and $50\,K$ (see Fig. 4.15g), the I-V characteristics show non-linear behavior, where $I_D \sim V_{DS}^2$. This indicates the presence of a space-charge effect. [71, 107] This effect is also minimally observable at a Ge segment length of $l_{Ge} = 2\,\mu m$ at $50\,K$ (Fig. 4.10g) and $4.7\,K$ (Fig. 4.10i). Additionally, for device 11_08 ($l_{Ge} = 0.5\,\mu m$), the effect can be seen at $4.8\,K$ (Fig. A.4i).

Once a specific threshold bias voltage is reached, the carrier concentrations rapidly surpass the doping concentrations found in lightly doped semiconductors. Consequently, the space charge is determined by the injected carriers. This leads to an enhanced electric field strength, additionally increasing the current. When the drift component of the injected carriers is predominant within the mobility regime, the resulting current shows a quadratic dependence on the bias voltage. This type of current transport is known to operate in the space-charge-limited current regime. [71]
Sistani [107] has observed this phenomenon at room temperature in Al-Ge-Al NW heterostructures with comparable Ge segment lengths. The temperature-dependent occurrence of this effect seems to be linked to the freezing out of charge carriers, which in turn reduces the space charge density within the space charge region.

Device Resistivity

The resistivities for a device with a Ge segment length of $0.15\,\mu m$, as a function of temperature and gate voltage, are illustrated in Fig. 4.16. This analysis covers a temperature range from $4.8\,K$ to $400\,K$, with the gate voltage varying between $-5\,V$ and $+5\,V$ in $2\,V$ increments. A logarithmic scale is employed for the resistivity values.
The resistivity values for temperatures between room temperature and $4.8\,K$ were derived from the I-V characteristics depicted in Fig. 4.15. For temperatures ranging from room temperature to $400\,K$, the resistivities were calculated based on the I-V characteristics used to assess the activation energy.

The resistivity remains stable from $400\,K$ down to $4.7\,K$ when the currents are hole-dominated and the gate voltages are between $-3\,V$ and $-5\,V$. In contrast, for electron-dominated currents, the resistivity increases until the temperature reaches $200\,K$. Below this temperature, the resistivity for positive gate voltages significantly decreases due to the overlap of the depletion zones.

With the calculated resistivity, it is now possible to estimate the carrier concentration of the Ge segment. This analysis is performed at $V_{TG} = 0\,V$, neglecting the resistivity of the Al leads (following Eq. 4.1). The measurement results from Fig. 4.15a reveal that $\partial V_{DS}/\partial I_D = 4.628\,k\Omega$, the dimensions are $A = 75\,nm \times 1.82\,\mu m$, and $l_{Ge} = 0.15\,\mu m$. This leads to an resistivity of $\rho_{Ge} = 0.43\,\Omega cm$. Referring to the $\rho\,(N)$ diagram by Cuttris [169], the carrier concentration for p-doped Ge is found as $N_A \approx 10^{16}\,cm^{-3}$, which aligns closely with the wafer manufacturers' declarations of $N_A = 3 \cdot 10^{15}\,cm^{-3}$.

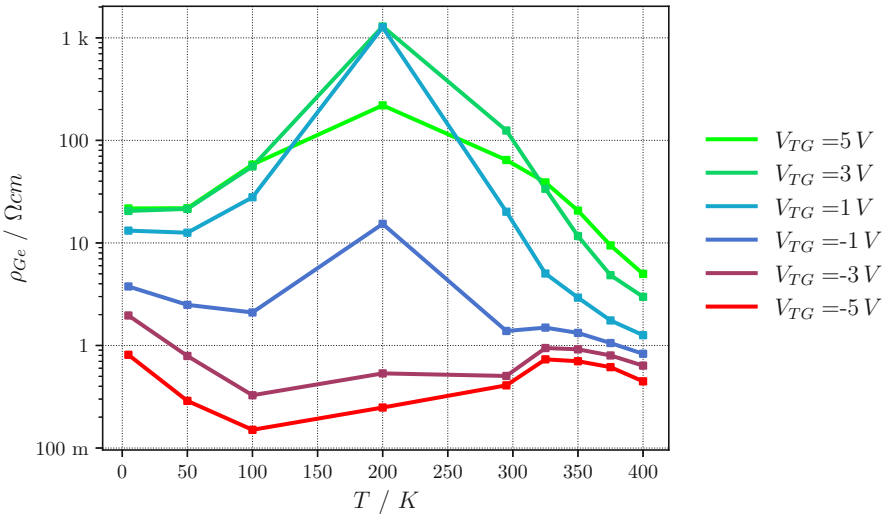

Figure 4.16: *Device resistivity of device 10_12 ($l_{Ge} = 0.15\,\mu m$) as a function of temperature and top-gate voltage calculated on the linear portion of the previously recorded I-V characteristics. The gate voltage ranges from $-5\,V$ to $+5\,V$, with a voltage spacing of $2\,V$, while the temperature varies from $4.8\,K$ to $400\,K$. ρ_{Ge} is presented in a logarithmic format.*

Ideality Factor Extraction

The I-V characteristics measured for device 10_12, which has a Ge segment length of $0.15\,\mu m$, are illustrated in Fig. 4.17. The characteristics are shown for gate voltages ranging from $-5\,V$ to $+5\,V$, with a spacing of $2\,V$ between each voltage. The temperature dependency can be observed in the individual subplots of Fig. 4.17, which cover temperatures from $295\,K$ down to $4\,K$. This figure also includes the derived bias voltage obtained by inserting the measured I_D data points into Eq. 4.2, along with the fitted ideality factors. To better display small values near the zero crossing of V_{DS}, the I_D values are presented as absolute values on a logarithmically scaled y-axis. The measured I-V characteristics are displayed as continuous lines, while the evaluated V_{DS} points are depicted as circles.
Continuing the trend observed with decreasing Ge segment length, this device exhibits even lower ideality factors at room temperature and $200\,K$, with sub-unity values for both forward and reverse directions ($n_{fd} = 1$, $n_{rs} = 0.1$ at $200\,K$). A notable transition occurs between $200\,K$ and $100\,K$, where the ideality factors show a marked increase ($n_{fd} = 3$, $n_{rs} = 0.06$ at $100, K$). This transition coincides with the onset of complete overlap between the source and drain depletion regions, signaling the emergence of short-channel effects. At even lower temperatures, the ideality factors continue to increase substantially, accompanied by an increase in conductivity, reflecting the transport characteristics in this short-channel regime.

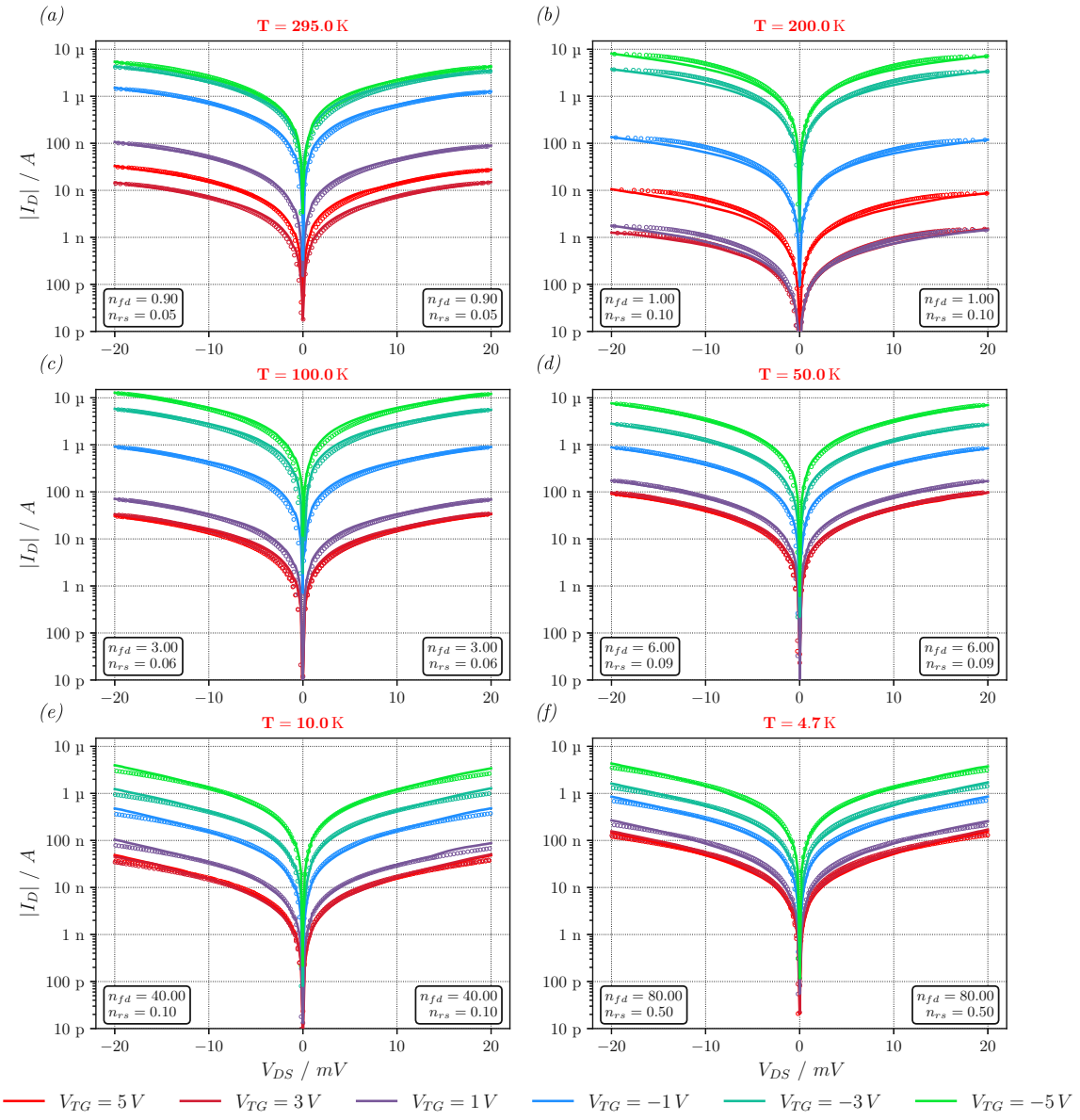

Figure 4.17: *Semilogarithmic plot of the I-V characteristics of device 10_12 ($l_{Ge} = 0.15\,\mu m$) at various temperatures. The continuous lines represent the measured behavior under applied top-gate voltages ranging from $-5\,V$ to $+5\,V$, with increments of $2\,V$. The circles indicate the I-V characteristics derived from the back-to-back Schottky diode device equation. Additionally, the fitting parameters related to the ideality factors are shown in the inset. Each subplot corresponds to a specific temperature at which the measurements were taken, ranging from $295\,K$ down to $4.7\,K$. Image based on [132].*

4.2.7 SB-FET with a 50 *nm* long Ge Channel

The ultra-short device 08_03, with $l_{Ge} = 50\,nm$ and $w_{Ge} = 1.78\,\mu m$, approaches the mean free path of electrons in Ge. This section examines its characteristics with particular attention to ballistic transport phenomena that become significant at this length scale. [107]

Activation Energy

The activation energy for a device with a Ge segment length of $50\,nm$ can be observed in Fig. 4.18. This activation energy, as a function of gate and bias voltage, is represented as a color map in subfigure a of Fig. 4.18, with the bias voltage varying from $-1\,mV$ to $+1\,mV$. Subfigure b of Fig. 4.18 displays the activation energy evaluated at $V_{DS} = 0\,V$, highlighting both the p-type and n-type regimes. Additionally, the transfer characteristic at $295\,K$, biased with $500\,\mu V$, is included. The current is shown as the absolute value $|I_D\,(V_{TG})\,|$ and is presented on a logarithmic scale.

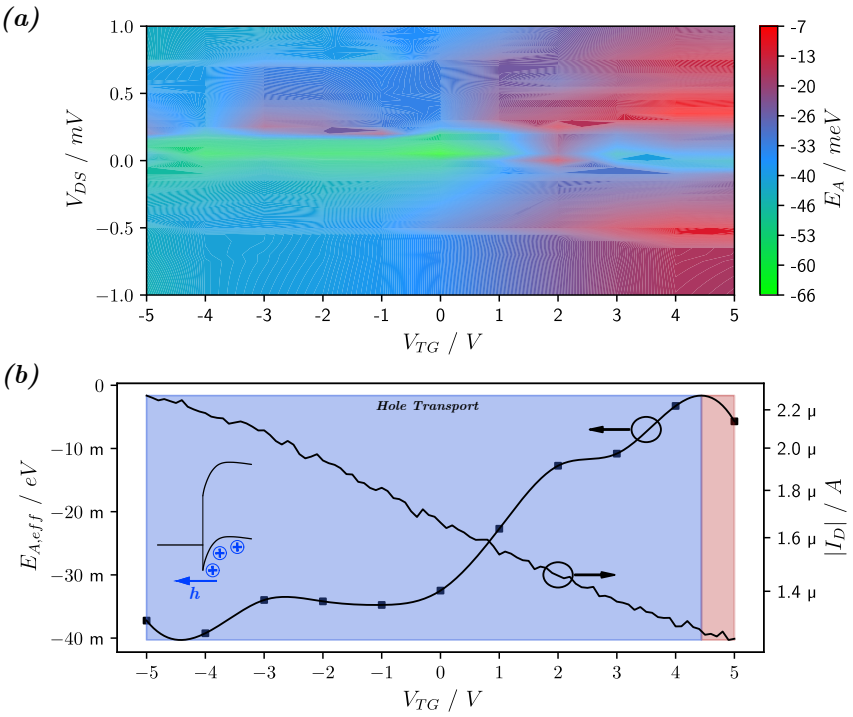

Figure 4.18: *Activation energy of device 08_03, with a Ge segment length of* $50\,nm$*. Subfigure (a) illustrates the activation energy as a function of* V_{TG} *and* V_{DS}*, represented in a colormap. The dashed contour lines represent the value of* k_BT/q *at* $300\,K$*, which is* $25.85\,meV$*. Subfigure (b) shows the activation energy evaluated for no bias voltage. Additionally, the transfer characteristic measured at room temperature with* $V_{DS} = 500\,\mu V$*, obtained during the initial device testing, is included. The current is presented on a logarithmic scale. This transfer characteristic corresponds to the gate voltage sweep from* $+5\,V$ *to* $-5\,V$*. Image based on [167].*

In Fig. 4.18, the activation energy shows minimal dependence on V_{TG} , ranging only from $-66\,meV$ to $-6.6\,meV$. Additionally, $E_{A,eff}$ appears to be largely independent of the bias voltage, as evidenced by the uniform coloring along the V_{DS} axis.
The consistently negative activation energies and the transfer characteristic shown in Fig. 4.18 indicate that the device operates with transparent barriers throughout the entire gate

voltage range. No distinct transition point between hole and electron-dominated transport is observed, suggesting that hole current dominates across all gate voltages with only minimal modulation capability.

Transfer Characteristics

The temperature-dependent transfer characteristics of the ultra-scaled device are shown in Fig. 4.19. Fig. 4.19a illustrates the characteristics of the negative gate voltage regime, while Fig. 4.19b shows the positive gate voltage regime. Arrows indicate the direction of the voltage sweep, and different colors correspond to individual temperatures. Additionally, the inset band structures demonstrate how band bending varies with gate voltage.

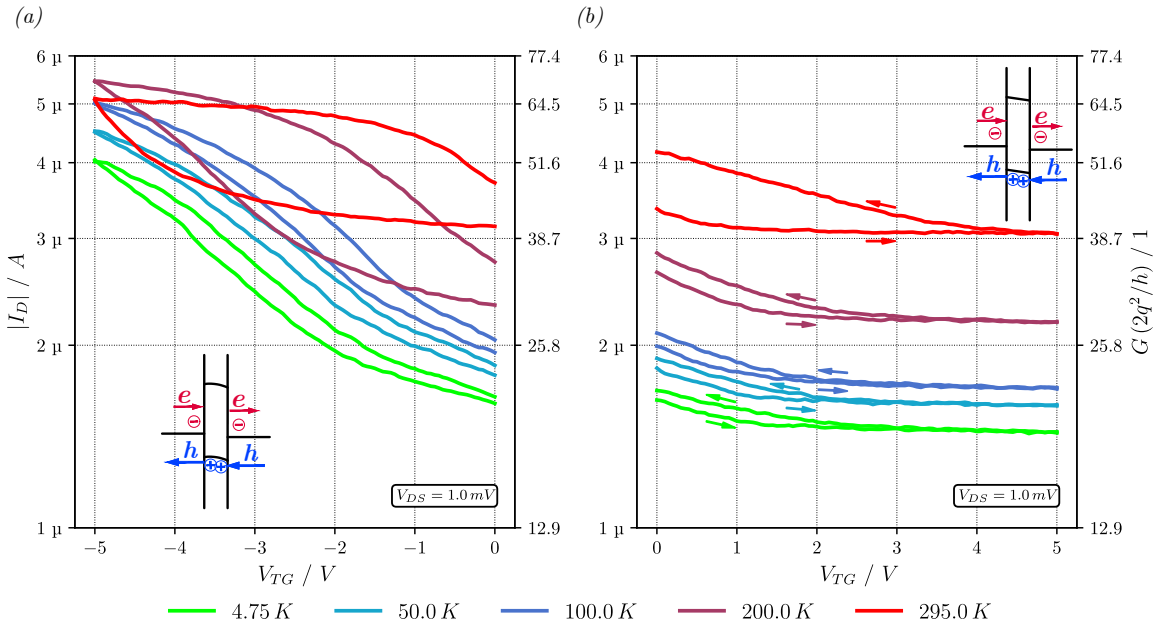

Figure 4.19: *Transfer characteristics of device 08_03 with Ge segment length of* 50 *nm, plotted as a function of temperature* T *and top-gate voltage* V_{TG}*, at the temperatures* 4.75 *K,* 50 *K,* 100 *K,* 200 *K, and* 295 *K. (a) represents the negative top-gate voltage regime and (b) the positive top-gate voltage regime. A logarithmic scale is used for* $|I_D|$ *on the left y-axis, as well as multiples of* $2q^2/h$ *for the right y-axis. Additionally, a schematic representation of the band structure is included as an inset. The inset band structure in the bottom left corner of subplot (a) illustrates a very small Ge segment, which allows for almost no upward band bending. In contrast, the inset band structure in subplot (b) displays completely flat bands, resulting in no downward bending. In both cases, only a hole-dominated current flow develops.*

Upon examining the scaling of the y-axis in Fig. 4.19, it appears that this device shows limited gate voltage response across the entire temperature range, with on-off ratios detailed in Table 4.6. The transfer characteristics indicate primarily hole-dominated transport, as the current decreases continuously in the positive gate voltage range while increasing for gate voltages below 4 *V* at room temperature. This dominance of hole current is consistent with the lower Schottky barrier for holes. The voltage at which current modulation becomes negligible shows temperature dependence, shifting from approximately 4 *V* at room temperature to 2 *V* at 4.8 *K*. The resulting on-off ratios in the p-type regime remain minimal, ranging from 1.67 at 295 *K* to 2.8 at 4.75 *K*, with the maximum ratio of 2.96 occurring at 100 *K*.

The ultra-short Ge segment length of $50\,nm$ results in complete overlap of the source and drain depletion regions throughout the channel. This full depletion zone coupling, evident in the negative activation energies observed across the entire gate voltage range (see Fig. 4.18), leads to flat bands even at room temperature, as illustrated in the insets of Fig. 4.19. While the channel length approaches the electron mean free path in Ge, suggesting potential ballistic transport for electrons, the observed current is primarily carried by holes due to their lower barrier height. Consequently, these devices cannot be turned off, explaining the minimal current modulation observed in the transfer characteristics. [28]

Table 4.6: *Listing of the on-off ratios of device 08_03 ($l_{Ge} = 50\,nm$). The on-off ratios of I_D for the hole-dominated region ($V_{TG} < 0\,V$) as $I_{on,p}/I_{off}$ and for the electron-dominated region ($V_{TG} > 0\,V$) as $I_{on,n}/I_{off}$. I_{off} indicates the minimum current above the noise level achieved across the entire V_{TG} range. For $I_{on,p}$, the value of I_D at $V_{TG} = -5\,V$ was used, while for $I_{on,n}$, the value of I_D at $V_{TG} = +5\,V$ was used.*

T	$295\,K$	$200\,K$	$100\,K$	$50\,K$	$4.8\,K$
$\frac{I_{on,p}}{I_{off}}$	1.7	2.5	3.0	2.8	2.8
$\frac{I_{on,n}}{I_{off}}$	1.0	1.0	1.0	1.0	1.0

Hysteresis Effects

In comparison to the previously presented device with a Ge segment of $0.15\,\mu m$, the current hysteresis decreases as the current becomes independent of the gate voltage in the positive gate voltage range, as shown in Fig. 4.19b. A small hysteresis is still observable in the hole-dominated current regime, with a trend of increasing hysteresis at higher temperatures.

Analysis of Ballistic Transport

As stated in Section 2.4.2, when the Ge segment length falls below the mean free path, ballistic transport takes place, where the conductivity of the Ge segment increases significantly as the charge carriers traverse the channel without scattering. In this regime, the conductivity is limited only by the contacts.

The segment of Ge measuring $50\,nm$ (device 08_03) is still above the mean free path. However, it warrants examination for ballistic transport phenomena.

The transfer characteristics displayed in Fig. 4.19 indicate almost no current modulation and negligible temperature dependence. The right y-axis in Fig. 4.19 is scaled in units of the quantum conductance $2q^2/h$, where each quantum corresponds to a single ballistic transport mode in the Ge segment. This scaling enables direct comparison between the measured conductance and quantum conductance, revealing the contribution of ballistic transport channels.

Fig. 4.20 presents the resistance as a function of the Ge segment length in a double logarithmic plot, based on the transfer characteristics of the measured devices at a gate voltage of $0\,V$ at room temperature. Most devices follow a clear trend, as indicated by the straight line fit, with the exception of the $2\,\mu m$ device, which shows unexpectedly higher resistance. The shortest device $(0.05, \mu m)$ exhibits a resistance significantly lower than the trend line, suggesting a transition towards ballistic transport behavior.

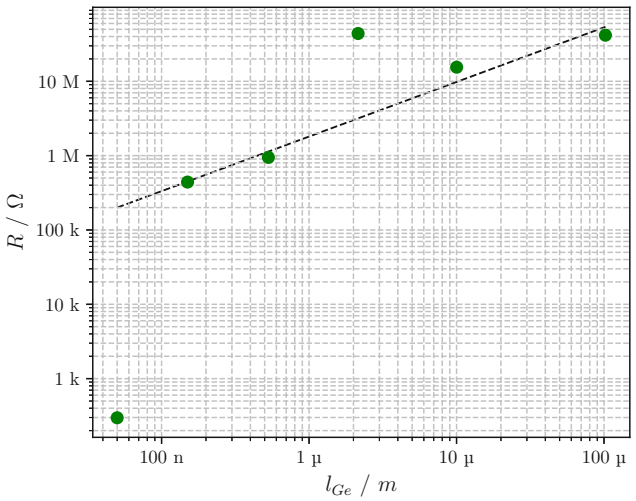

Figure 4.20: *The resistance is represented as a function of the length of the Ge segment, displayed in a double logarithmic format.*

Output Characteristics

To record the I-V characteristics of the shortest device, the bias voltage was varied from $-1\,mV$ to $+1\,mV$, while the gate voltage was adjusted between $+5\,V$ and $-5\,V$. The measurement results are presented for temperatures of $295\,K$, $200\,K$, $100\,K$, $50\,K$, and $4.7\,K$, with results at $10\,K$ excluded. The first column displays the I-V characteristics on a linear scale, with gate voltage increments of $2\,V$. The second column shows the absolute value of I_D using a logarithmically scaled colormap.
The device exhibits remarkably high current levels even at minimal bias voltages, as shown in Fig. 4.21. Currents exceeding $5\,\mu A$ are achieved with just $1\,mV$ bias, necessitating voltage limitation to prevent damage to the Al-Ge interfaces. A notable temperature-dependent behavior emerges below $200\,K$, visible in Fig. 4.21e-j as a broadening of the current flow with respect to gate voltage. This manifests as increasingly flatter I-V curves at higher gate voltages in the linear plots and as deformed contour lines in the colormap. Due to the analyzer's minimum step size of $25\,\mu V$, the limited resolution of 41 measurement points results in observable current discontinuities near $\pm 50\,\mu V$ bias voltage.
The device achieves high conductance values of $3.7\,mS$ at $4.7\,K$ and $5.17\,mS$ at $295\,K$, both measured at a gate voltage of $-5\,V$ (Fig. 4.21i and a, respectively). These values significantly exceed those of the $0.15\,\mu m$ device (10_12), which shows a maximum conductance of $0.23\,mS$ at $295\,K$ and $-5\,V$ gate voltage (Fig. 4.15a).
The device exhibits predominantly ohmic characteristics with a behavior pattern typically associated with drain-induced barrier lowering, where the bias voltage exerts stronger control over current modulation than the gate voltage. [28] This reduced gate control can be attributed to the ultra-short channel length, where the complete overlap of source and drain depletion regions effectively diminishes the gate's influence on the channel potential.

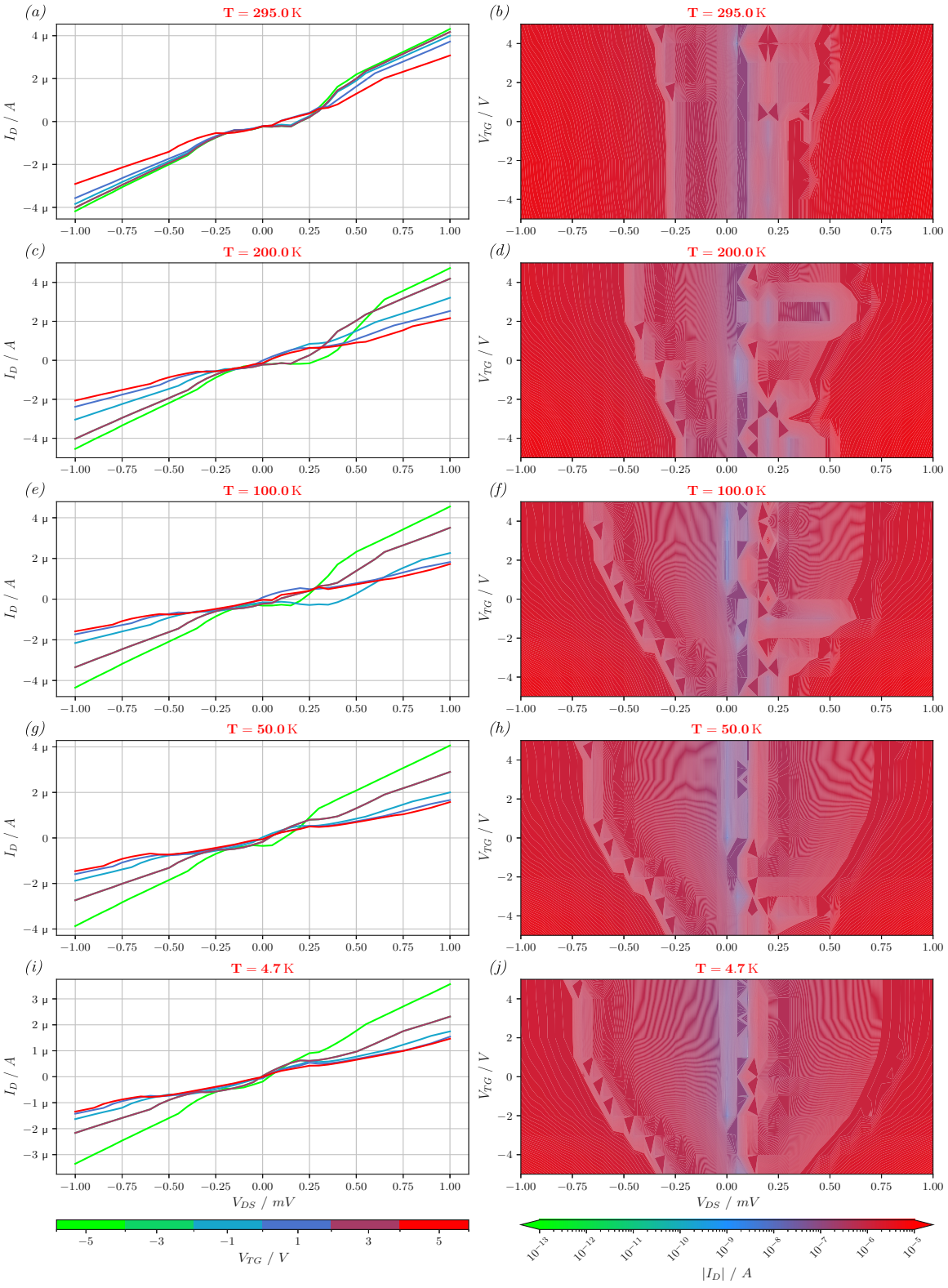

Figure 4.21: *The I-V characteristics of device 08_03 ($l_{Ge} = 50\,nm$) are shown as a function of temperature, bias, and top-gate voltage. In the first column, the I-V characteristic $I_D\,(V_{DS})$ is displayed with a linearly scaled y-axis, featuring separate lines for each gate voltage. A gate voltage spacing of $2\,V$ is utilized. The second column presents the I-V characteristics as $|I_D\,(V_{DS}, V_{TG})|$ in a logarithmically scaled colormap. The temperature dependence can be understood by interpreting each subplot from top to bottom as corresponding to decreasing temperature. Image based on [128].*

Device Resistivity

The resistivities obtained from the I-V characteristics, as a function of temperature and gate voltage, are illustrated in Fig. 4.22. This analysis covers a temperature range from $4.8\,K$ to $400\,K$, with the gate voltage varying from $-5\,V$ to $+5\,V$ in $2\,V$ increments.
Resistivity values for temperatures between room temperature and $4.8\,K$ were derived from the I-V characteristics depicted in Fig. 4.21. For temperatures ranging from room temperature to $400\,K$, the resistivities were calculated based on the I-V characteristics used to assess the activation energy.

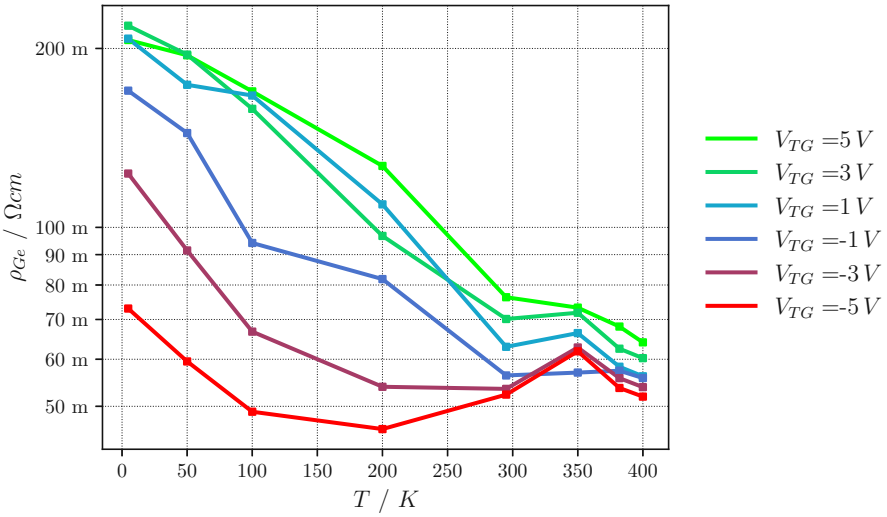

Figure 4.22: *Device resistivity of device 08_03 ($l_{Ge} = 50\,nm$) as a function of temperature and top-gate voltage calculated on the linear portion of the previously recorded I-V characteristics. The gate voltage ranges from $-5\,V$ to $+5\,V$, with a voltage spacing of $2\,V$, while the temperature varies from $4.8\,K$ to $400\,K$. ρ_{Ge} is presented in a logarithmic format.*

The resistivity shows minimal variation due to the weak dependence of the I-V characteristics on temperature and gate voltage. At a gate voltage of $+5\,V$, the resistivity increases with decreasing temperature from approximately $70\,m\Omega cm$ to about $200\,m\Omega cm$. Conversely, at a gate voltage of $-5\,V$, the resistivity remains around $70\,m\Omega cm$.

Ideality Factor Extraction

The semilogarithmic plot of the absolute value of I_D as a function of gate voltage and bias voltage is shown in Fig. 4.23. The characteristics are represented by continuous lines. A gate voltage spacing of $2\,V$ has been applied. The circles indicate the I-V characteristics modeled according to Eq. 4.2. The temperature dependence can be understood by viewing the individual subplots.

The device's ultra-short Ge segment length of $50\,nm$ leads to predominantly ballistic transport with ohmic-like characteristics, where the current shows minimal dependence on the gate voltage. This transport regime fundamentally differs from the assumptions underlying the back-to-back Schottky diode model described by Eq. 4.2, which is based on barrier-controlled transport mechanisms. Furthermore, the narrow range of applicable bias voltage combined with current fluctuations posed significant technical challenges for the fitting procedure, even with extensive data filtering.

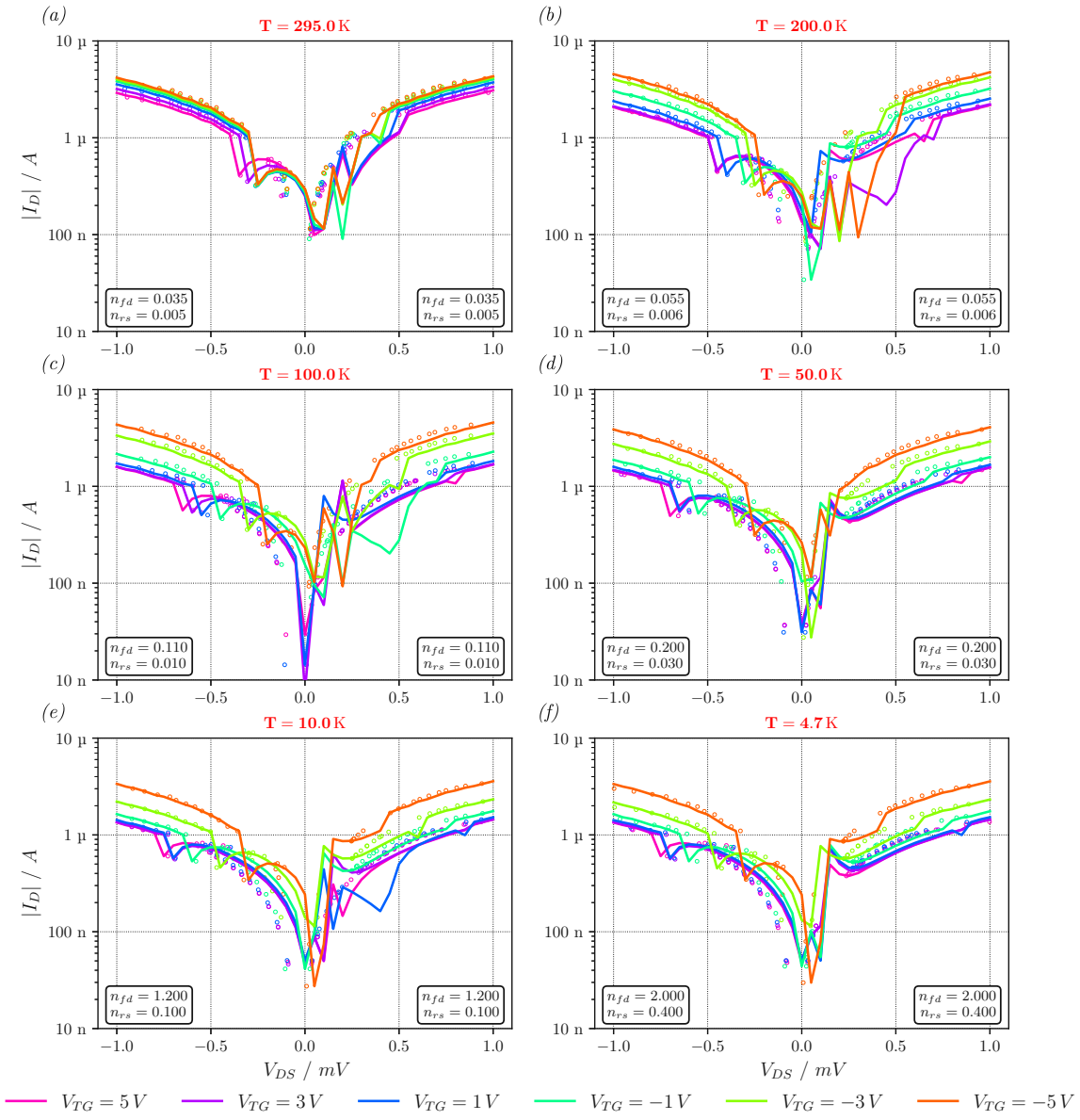

Figure 4.23: *Semilogarithmic plot of the I-V characteristics of device 08_03 ($l_{Ge} = 50\,nm$) at various temperatures. The continuous lines represent the measured behavior under applied top-gate voltages ranging from $-5\,V$ to $+5\,V$, with increments of $2\,V$. The circles indicate the I-V characteristics derived from the back-to-back Schottky diode device equation. Additionally, the fitting parameters related to the ideality factors are shown in the inset. Each subplot corresponds to a specific temperature at which the measurements were taken, ranging from $295\,K$ down to $4.7\,K$. Image based on [132].*

The attempted model fitting yields extremely low ideality factors ($n_{fd} = 0.035$ and $n_{rs} = 0.005$ at room temperature), as shown in the inset of Fig. 4.23. However, these values, while mathematically achieving a fit, lack physical significance in the context of Schottky barrier transport. The discrepancy between the model and the underlying physics suggests that transport in such ultra-scaled devices requires a different theoretical framework, one that properly accounts for ballistic transport phenomena.

Chapter 5

Conclusion

This work presents the electrical characterization of top-gated Al-Ge-Al SB-FETs with varying Ge channel lengths at different temperatures. The Ge channel structures were patterned in the Ge layer of a GOI substrate using laser lithography and RIE and were subsequently passivated with Al_2O_3. In the next step, drain and source contacts were created at each end of the Ge structure through Al sputter deposition. The close contact between Al pads and the Ge nanosheets facilitated the Al-Ge exchange process, resulting in atomically sharp transitions between the two materials. Moreover, using RTA to induce this exchange allowed for precise control over the length of the Ge segments. As a result, it became possible to create structures with widths of approximately $2\,\mu m$ and Ge segment lengths ranging from $100\,\mu m$ down to only $50\,nm$ - an achievement hardly possible with conventional optical lithography systems.
The passivation using Al_2O_3 enabled the electrically isolated deposition of Au top gates, allowing the devices to function as SB-FETs. Additionally, using a GOI substrate permitted the Si handle wafer to serve as a common back gate, which is isolated from the structures by the BOX.
The electrical characterization comprised comprehensive output and transfer characteristics measurements across a wide temperature range. Initial I-V characteristics were recorded from room temperature to $400\,K$ to determine the effective activation energy, followed by transfer characteristics measurements from $4.8\,K$ to room temperature. The analysis of devices with varying Ge segment lengths enabled the investigation of device resistance and current modulation capability as functions of segment length, temperature, and gate voltage. Bidirectional gate voltage sweeps during transfer characteristic measurements provided insight into the influence of surface and oxide traps on device performance. The transfer characteristics consistently revealed p-type behavior, attributed to the naturally high surface state density of Ge and the resulting strong Fermi level pinning near the valence band.
The measurement of the output characteristics at different gate voltages allowed for an exploration of the different transport regimes at the Schottky contact, enabling an approximate differentiation between TE, TFE, and FE. The colormap presentation comprehensively visualizes these transport regimes and their dependencies on temperature, gate voltage, and bias voltage. Additionally, displaying the data as current versus bias voltage with a linear current axis revealed the device's symmetry and transitions between linear and non-linear behaviors. Non-linear phenomena, such as space charge-limited current transport, were primarily observed at low temperatures.

Devices with longer Ge segments exhibited a strong dependence on temperature and gate voltage concerning their conductivity. This was particularly evident as conductivity significantly decreased at low temperatures due to charge carrier freeze-out, resulting in very high device resistances.
The extracted resistance values were incorporated into the back-to-back Schottky diode I-V model for asymmetric devices, which was then aligned with the measured I-V characteristics by adjusting the ideality factor. The ideality factor helped determine whether the current was mainly limited by the channel resistance or Schottky barriers.
Variations in the ideality factor of Schottky diodes were observed between forward and reverse directions, depending on the device's channel length and temperature. Notably, for a Ge segment length of $0.15\,\mu m$, low temperatures led to charge carrier freeze-out, causing a widening of both source and drain depletion zones that resulted in punch-through below approximately $200\,K$. This overlap caused an increase in current without any modulation capability for the electron-dominated current transport, and there was no influence from trapped charges. Additionally, the shortest device, which had a Ge segment length of only $50\,nm$, was examined separately for ballistic transport. The transfer characteristics of this device showed negligible dependence on both temperature and gate voltage.
The insights gained from electrical characterizations into the dominant current transport regimes, particularly their relationship with device dimensions and temperature, may aid in the development of future CMOS-compatible novel nanoelectronic, plasmonic, and optoelectronic devices. [170–172] Furthermore, the low-temperature characterization highlighted essential aspects for developing quantum computing systems, taking advantage of the strong spin-orbit coupling of Ge. [38] This includes superconducting quantum interference devices, oscillators, and amplifiers. [107, 173]

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List of Abbreviations

Symbol	Term
Al	Aluminum
AI	Artificial Intelligence
$Al_2(CH_3)_6$	Trimethylaluminium (TMA)
Al_2O_3	Alumina/Aluminium Oxide
ALD	Atomic Layer Deposition
Au	Gold
BHF	Buffered Hydrofluoric Acid
BOX	Buried Oxide
C	Carbon
CB	Conduction band
CMOS	Complementary Metal-Oxide-Semiconductor
CVD	Chemical Vapor Deposition
DHI	Dilluted Hydroiodic Acid
DI	Deionized Water
DIBL	Drain Induced Barrier Lowering
EDX	Energy-Dispersive X-ray Spectroscopy
FE	Field Emission
FET	Field-Effect Transistor
Ge	Germanium
Ge_2O_3	Germanium Sesquioxide
$GeCl_4$	Germanium Tetrachloride
GeF_4	Germanium Tetrafluoride
GeO	Germanium Monoxide
GeO_2	Germanium Dioxide
Ge_xO_y	Native Germanium Sub Oxides
GOI	Germanium-on-Insulator
H_2	Hydrogen
H_2O	Water
He	Helium
HF	Hydrofluoric Acid
HfO_2	Hafnium Dioxide
HI	Hydroiodic Acid
IC	Integrated Circuit
ICP	Inductively Coupled Plasma
ID	Identifier
JoFET	Josephson Field-Effect Transistors
MIGS	Metal-induced Gap States

MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
N_2	Nitrogen
NDR	Negative Differential Resistance
NH_4F	Ammonium Flouride
NW	Nanowire
O_2	Oxygen
PCB	Printed Circuit Board
PLD	Pulsed Laser Deposition
Pt	Platinum
QWFET	Quantum-Well Field-Effect Transistor
RF	Radio Frequency
RIE	Reactie Ion Etching
RTA	Rapid Thermal Annealing
Sb	Antimony
SB-FET	Schottky Barrier Field-Effect Transistor
SEM	Scanning Electron Microscope
SF_6	Sulfur Hexafluoride
Si	Silicon
SiO_2	Silica/Silicon Dioxide
SMU	Source Measurement Unit
Sn	Tin
SOI	Silicon-on-Insulator
SQUID	Superconducting Quantum Interference Device
TE	Thermionic Emission
TED	Transferred Electron Device
TEM	Transmission Electron Microscope
TFE	Thermionic Field Emission
Ti	Titan
UPS	Ultraviolet Photoelectron Spectroscopy
VB	Valence Band
ULSI	Ultra-Large-Scale Integrated Circuit
XPS	X-ray Photoelectron Spectroscopy

List of Symbols

Symbol	Term	Units
a	Lattice Constant	pm
A	Cross-Sectional Area	m^2
A^*	Richardson Constant	$Am^{-2}K^{-2}$
A_{pad}	Al Pad Area	m^2
C	Molar Concentration	m^{-3}
D	Diffusion Coefficient, Diffusivity	cm^2/s
$\tilde{D}$	Interdiffusion Coefficient	cm^2/s
D_0	Frequency Factor	cm^2/s
D_A, D_B	Intrinsic Diffusion Coefficients	cm^2/s
D_{it}	Interface State Density	$cm^{-2}V^{-1}$
E_A	Acceptor Impurity Ionization Energy, Activation Energy	eV
$E_{A,eff}$	Activation Energy for Charge Carrier Injection	eV
E_c	Energy of the Lower Boundary of the Conduction Band	eV
E_D	Donor Impurity Ionization Energy	eV
E_F	Fermi Level	eV
$E_{F,i}$	Intrinsic Fermi Level	eV
E_{field}	Electric Field Strength	V/cm
E_g	Band Gap Energy	eV
$E_{g,0}$	Band Gap Energy at 0K	eV
EOT	Equivalent Oxide Thickness	nm
E_v	Energy of the Higher Boundary of the Valence Band	eV
E_{vac}	Vacuum Energy Level	eV
f	Fermi-Dirac Probability Function	$-$
G	Conductance	S
G_C	Contact Conductance	S
g_A, g_D	Ground State Degeneracies	$-$
h	Planck Constant $\approx 6.62607 \cdot 10^{-34}\, Js$	Js
I_D	Drain-Source Current	A
I_G	Gate Current	A
I_{off}	Off Current	A
I_{on}	On Current	A
I_S	Source Current	A
J	Current Density	A/m^2
J_0	Reverse Saturation Current Density	A/m^2
J_f	Particle Flux Density	$m^{-2}s^{-1}$
$J_{f,A}$, $J_{f,B}$	Particle Flux Densities	$m^{-2}s^{-1}$
k	Wavenumber	rad/m
k_B	Boltzmann Constant $\approx 1.38065 \cdot 10^{-23}\, J/K$	J/K
k_F	Fermi Wave Number	rad/m
l	Conductor Length	m
l_D	Diffusion Length	m

l_{Ge}	Ge Segment Length	m
l_{MFP}	Scattering Mean Free Path	nm
M	Number of Ballistic Channels	–
m^*	Effective Mass	kg
$m^*_{ds,e}$, $m^*_{ds,h}$	Density-of-States Effective Masses	kg
n	Electron Concentration	cm^{-3}
n_i	Intrinsic Carrier Concentration	cm^{-3}
n	Ideality Factor	–
N	Impurity Concentration	cm^{-3}
N_A, N_D	Concentration of Impurities	cm^{-3}
N_A^-, N_D^+	Concentration of Ionized Impurities	cm^{-3}
$N(E)$	Density of States (3D)	$eV^{-1}m^{-3}$
N_c, N_v	Effective Densities of States Holes	cm^{-3}
p	Hole Concentration	cm^{-3}
q	Elementary Charge $\approx 1.60218 \cdot 10^{-19}\,C$	C
Q_D	Surface Charge of Depletion Region	C
Q_M	Surface Charge Metal	C
Q_S	Surface Charge Semiconductor	C
R	Channel Resistance	Ω
S	Sensitivity Parameter	–
T	Temperature, Transmission Coefficient	K, –
$t_{high-\kappa}$	Thickness of the high-κ Dielectric	nm
t_{RTA}	Annealing Time	s
t_t	Transit Time	s
v	Velocity	m/s
$\tilde{V}_A$, $\tilde{V}_B$	Partial Molar Volumes	m^3/mol
V_{bi}	Built-in Voltage	V
V_{DS}	Drain-Source Voltage	V
V_{GS}	Gate-Source Voltage	V
V_{TG}	Top-Gate Voltage	V
v_g	Group Velocity	m/s
w_D	Depletion Width	nm
w_{Ge}	Structure Width	μm
μ	Charge Carrier Mobility	$cm^2/(Vs)$
ε_0	Vacuum Permittivity $\approx 8.8542 \cdot 10^{-12}\,F/m$	F/m
ε_s	Relative Permittivity Semiconductor	–
$q\chi$	Electron Affinity	eV
$q\phi_0$	Charge Neutrality Level	eV
$q\phi_B$	Energy Barrier	eV
$q\phi_{B,n}$	Energy Barrier for Electrons	eV
$q\phi_{B,p}$	Energy Barrier for Holes	eV
$q\phi_m$	Metal Work Function	eV
$q\phi_s$	Semiconductor Work Function	eV
$q\phi_{SBH,eff}$	Effective Schottky Barrier Height	eV
ε_N	Sub-Band Cut-off Energies	eV
ε_r	Relative Permittivity	–
$\varepsilon_{r,high-\kappa}$	Relative Permittivity high-κ Dielectric	–
ε_{r,SiO_2}	Relative Permittivity SiO_2	–
ε_s	Relative Permittivity Semiconductor	–
λ	Wavelength	nm
ρ_{Ge}	Resistivity of the Ge segment	Ωcm
σ	Conductivity	S/cm
τ_m	Mean Scattering Time, Momentum Relaxation Time	s, s
θ	Heaviside Step Function	–

Appendix A

Additional Evaluation Graphs

The following content presents the measurement results for device 05_13, which has a Ge segment length of $10\,\mu m$, and device 11_08, with a Ge segment length of $0.5\,\mu m$. This includes both the transfer and output characteristics, as well as the evaluation of the effective activation energy.

Effective Activation Energy

Fig. A.1 presents the effective activation energy as a function of gate and bias voltage for all devices discussed in Section 4.2.
The color bar boundaries are defined by the highest and lowest values of effective activation energy across all devices. In Fig. A.1f, the device with the shortest Ge segment shows minimal variation in effective activation energy along the gate voltage axis, resulting in an almost uniform coloring.
The individual subplots reveal a length-dependent effective activation energy, with the intrinsic point shifting towards higher voltages as Ge segment lengths decrease.

Transfer Characteristics

Fig. A.2 presents the transfer characteristics of devices 05_13 and 11_08 at temperatures ranging from $295\,K$ to $4.7\,K$. For the $10\,\mu m$ device, the negative and positive gate voltage regimes are shown in subfigures (a) and (b), respectively. Similarly, for the $0.5\,\mu m$ device, the negative and positive gate voltage regimes are presented in subfigures (c) and (d).

Output Characteristics

Figs. A.3 and A.4 show the I-V characteristics at temperatures from $295\,K$ to $4.7\,K$ for the devices with $10\,\mu m$ and $0.5\,\mu m$ Ge segments, respectively. The absolute value of I_D is presented using logarithmically scaled colormaps.

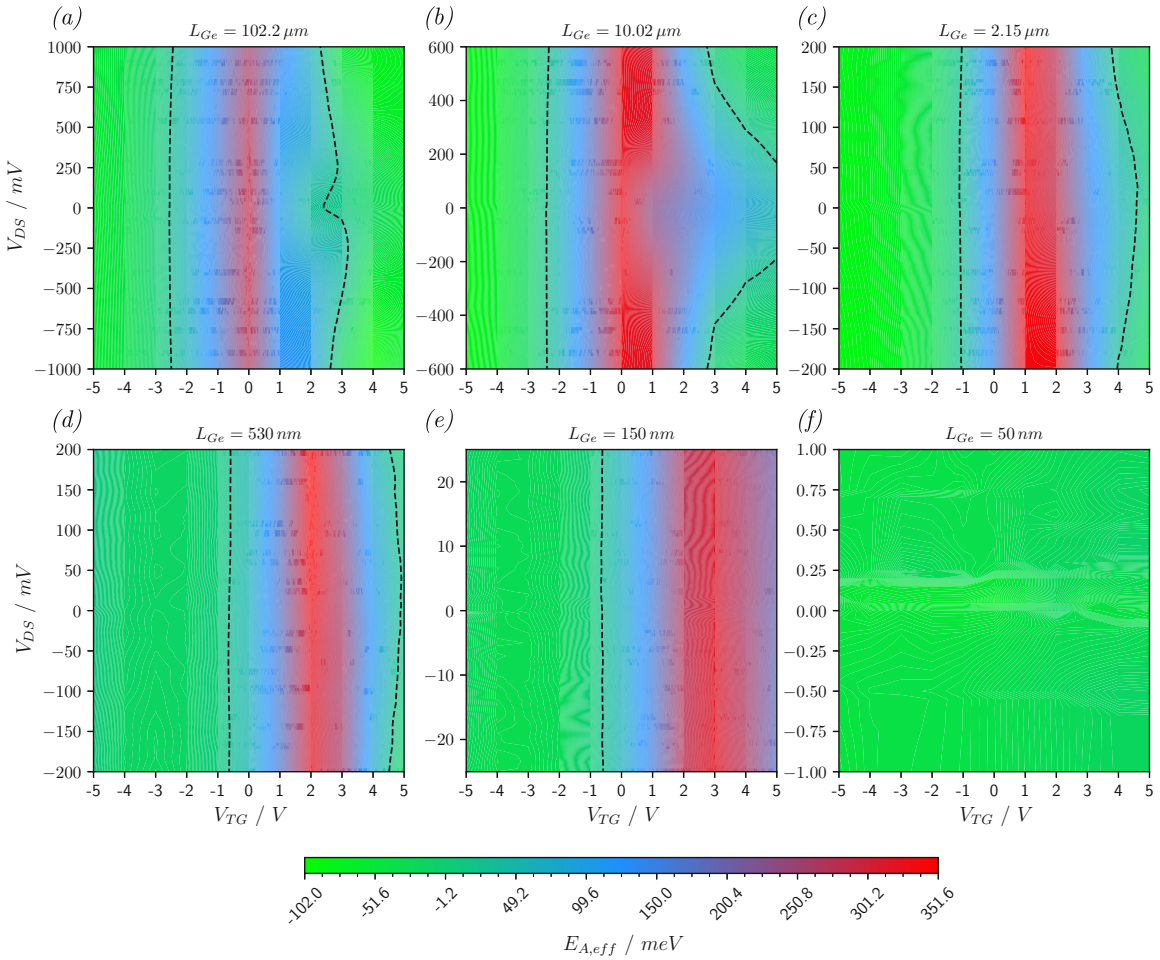

Figure A.1: *Effective activation energy as a function of the gate and bias voltage for devices with Ge segment lengths of* $102\,\mu m$ *(a),* $10\,\mu m$ *(b),* $2\,\mu m$ *(c),* $0.5\,\mu m$ *(d),* $0.15\,\mu m$ *(e), and* $50\,nm$ *(f). A dashed contour line indicates the value of* k_BT *at* $300\,K$*. Image based on [128].*

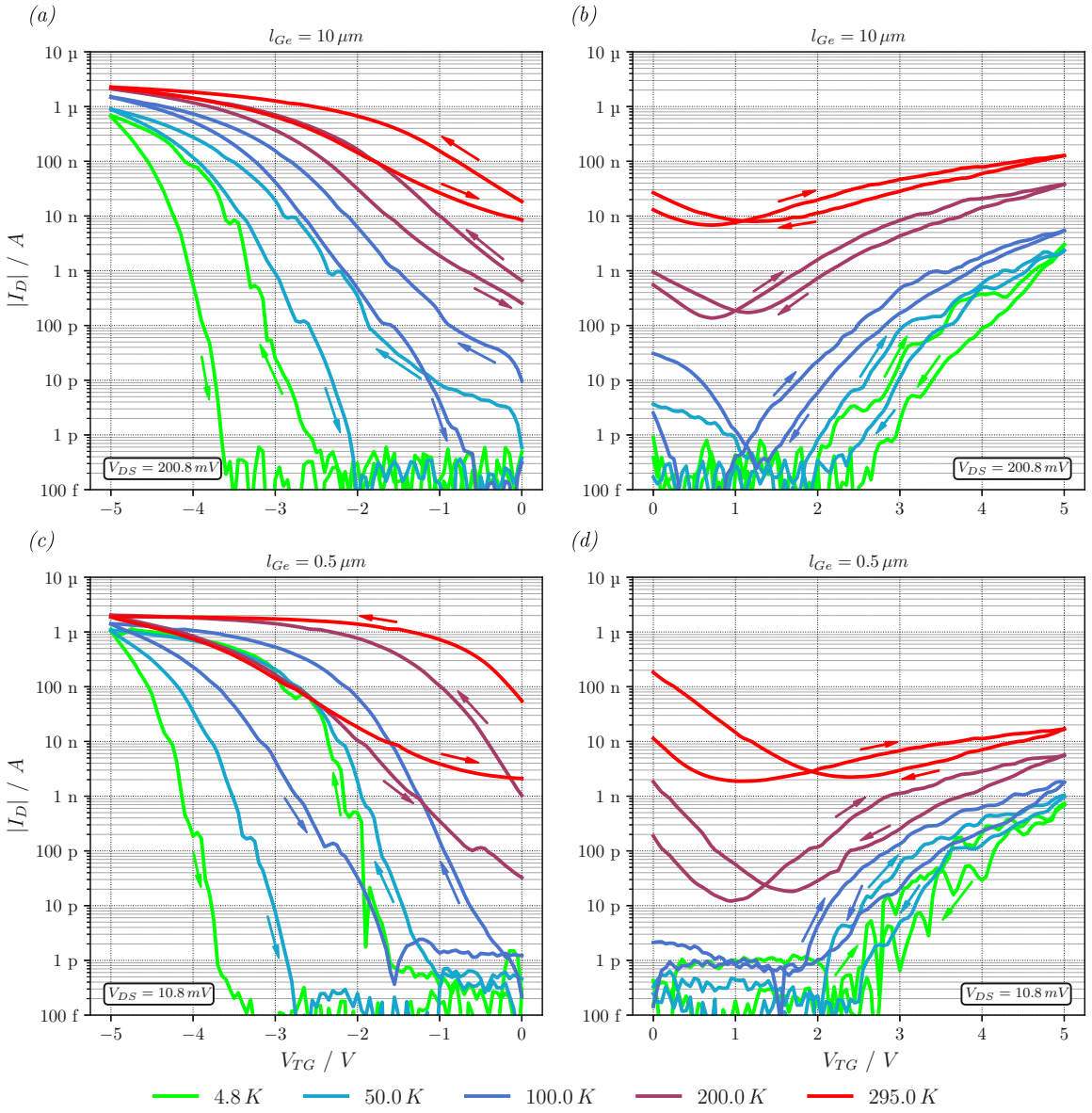

Figure A.2: *The transfer characteristics of two devices with varying Ge segment lengths, presented as the absolute values of I_D as a function of gate voltage and temperature. A logarithmic scale is used for I_D. The temperature range spans from 295 K down to 4.8 K. The direction of the voltage sweep is indicated by arrows, while different colors represent individual temperatures. Subfigure (a) shows the transfer characteristics of device 05_13 with a Ge segment length of 10 µm in the negative gate voltage regime, with a bias voltage of 200.8 mV. Subfigure (b) displays the transfer characteristics in the positive gate voltage regime for the same device. Subfigure (c) presents the transfer characteristics of device 11_08 with a Ge segment length of 0.5 µm in the negative gate voltage regime, with a bias voltage of 10.8 mV, while subfigure (d) illustrates the characteristics in the positive gate voltage regime for the 530 nm device.*

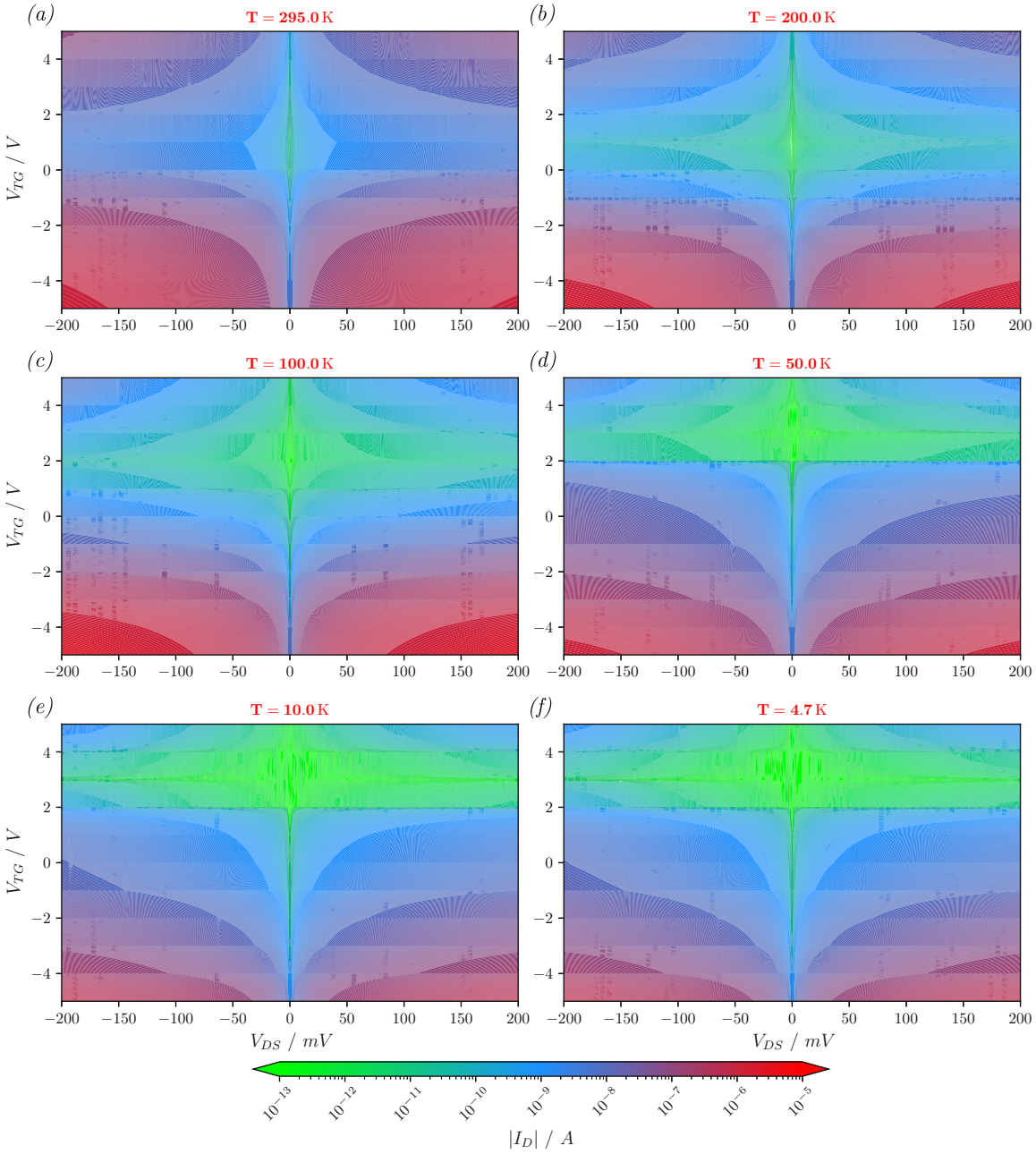

Figure A.3: *The I-V characteristics of device 05_13 ($l_{Ge} = 10\,\mu m$) are presented as a function of temperature, bias, and top-gate voltage, shown as $|I_D\,(V_{DS}, V_{TG})\,|$ in a logarithmically scaled colormap. The temperature dependence can be understood by interpreting each subplot from top to bottom as corresponding to decreasing temperature.*

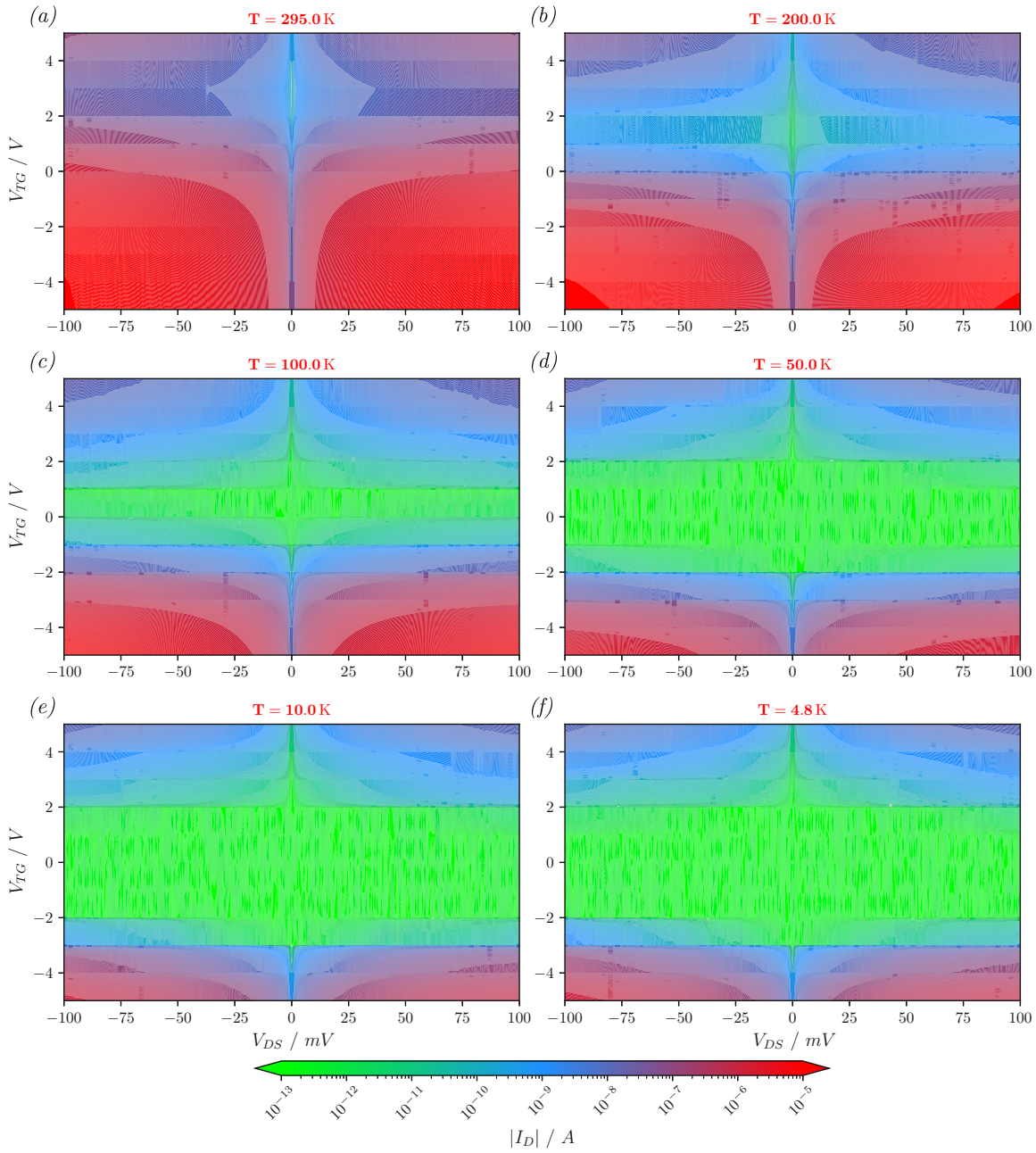

Figure A.4: *The I-V characteristics of device 11_08 ($l_{Ge} = 0.5\,\mu m$) are presented as a function of temperature, bias, and top-gate voltage, shown as $|I_D\,(V_{DS}, V_{TG})\,|$ in a logarithmically scaled colormap. The temperature dependence can be understood by interpreting each subplot from top to bottom as corresponding to decreasing temperature.*

Appendix B

Sample Processing Parameters

The devices were fabricated on a 6-inch GOI wafer with the following layer structure from top to bottom:

- A protective SiO_2 capping layer ($58 \pm 5\,nm$)
- A p-doped Ge layer oriented in the $\langle 100 \rangle$ direction ($76 \pm 5\,nm$), with a doping concentration of $3 \cdot 10^{15}\,cm^{-3}$
- A buried SiO_2 layer ($147 \pm 5\,nm$)
- A doped Si substrate ($500 \pm 5\,nm$)

The wafer was cleaved into pieces of $12\,mm \times 12\,mm$ for processing.

Substrate Preparation

(a) Wafer cleaving
  - Score blank wafer with diamond scriber
  - Cleave into $6\,mm \times 6\,mm$ pieces

(b) Surface cleaning
  - Clean surface alternately with acetone and isopropyl
  - Dry with N_2

(c) SiO_2 capping removal
  - Prepare BHF solution: HF (35 %) and NH_4F in 7 : 1 ratio
  - Etch in BHF for $80\,s$ (etch rate: $\sim 1\,nm/s$)
  - Rinse in DI for $10\,s$
  - Dry with N_2
  - Verify removal using ellipsometry

Formation of Ge Sheet Structures

(a) Photoresist coating
  - Spin coat AZ 5214E at $6000\,min^{-1}$ for $35\,s$ (ramp 1)
  - Softbake at $100\,°C$ for $60\,s$

(b) Positive laser lithography

- Expose using Heidelberg Instruments MLA 150 Advanced Maskless Aligner
- Parameters: 140 MJ/cm^2 power, 0 defoc

(c) Development

- Develop in AZ 726 MIF for 15-16 s
- Rinse twice in bubble rinse DI, 15 s each
- Dry with N_2

(d) RIE (Oxford Instruments PlasmaPro 100 Cobra)

- Clean chamber with O_2
- Precondition: cool with N_2 to 35 $°C$
- Load sample through load-lock
- Process parameters:
  - SF_6: 50 $sccm$
  - O_2: 4 $sccm$
  - ICP Power: 0 W
  - Forward Power: 15 W
  - Temperature: 35 $°C$
  - He backing: 10 $sccm$
- Etch for 70 s
- Unload sample
- Clean chamber with O_2 for 10 min

(e) Resist removal (PVA TePla Plasma Asher)

- Load sample
- Run plasma asher at 300 W for 3 min
- Strip resist in acetone at 50 $°C$ for 5 min
- Clean in isopropyl
- Dry with N_2

Passivation of Ge sheets

ALD of Al_2O_3 (Cambridge NanoTech Savannah 100)

- Heat reactor to 200 $°C$
- Vent reactor and load sample
- Pump down and set process parameters:
  - 120 cycles of H_2O and **TMA!**
  - Pulse length: 15 ms
  - Flow rate: 20 $sccm$
- Open **TMA!** precursor at 200 $°C$ and start process
- Close **TMA!** precursor after completion
- Vent reactor and remove sample

Formation of Al contact pads

(a) Photoresist coating

- Spin coat AZ 5214E at $6000\,min^{-1}$ for $35\,s$ (ramp 1)
- Softbake at $100\,°C$ for $60\,s$

(b) Positive laser lithography

- Expose pad openings using Heidelberg Instruments MLA 150
- Parameters: $140\,MJ/cm^2$ power, 0 defoc

(c) Development

- Develop in AZ 726 MIF for 16-17 s
- Rinse twice in bubble rinse DI, $15\,s$ each
- Dry with N_2

(d) Al_2O_3 removal at pad openings

- Etch in BHF for $15\,s$
- Rinse in DI for $10\,s$
- Rinse under water tap for $5\,s$
- Dry with N_2

(e) Native Ge_xO_y oxide removal

- Prepare DHI: HI (57 %) and DI in 1 : 3 ratio
- Etch in DHI for $5\,s$ (etch rate: $\sim 1\,nm/s$)
- Rinse twice in DI, $5\,s$ and $20\,s$
- Dry with N_2

(f) Al sputtering (Von Ardenne HF Sputter, rate: $20\,nm/min$ at $50\,W$)

- Load sample and pump down
- Set base pressure: $2 \cdot 10^{-6}\,mbar$
- Set working pressure: $3 \cdot 10^{-3}\,mbar$
- Clean sample: reverse sputter 3 layers at $100\,W$ RF for $60\,s$
- Clean Al target: $2 \times 60\,s$ at $100\,W$ RF
- Deposit $100\,nm$ Al: 5 layers at $50\,W$ RF for $60\,s$

(g) Lift-off

- Soak in acetone at $50\,°C$ for $30\,min$
- Rinse carefully with acetone using syringe
- Rinse in isopropyl
- Dry with N_2

Rapid Thermal Annealing

Process in UniTemp UTP 1100

- Place sample on carrier wafer in chamber
- Initial evacuation:
  - Pump down to $\sim 1\,mbar$ for $120\,s$
  - Flush with N_2 for $120\,s$
- Final evacuation:
  - Pump down to $\sim 1\,mbar$ for $120\,s$
  - Flush with forming gas (N_2/H_2 90 %/10 %) for $120\,s$
- Temperature ramp:
  - Heat to $300\,°C$ at $15\,°C/s$
  - Heat to $400\,°C$ at $50\,°C/s$ (prevent temperature overshoot)
- Hold at target temperature for specified duration
- Cool down:
  - Flush with N_2
  - Remove sample

Formation of Back-Gate Opening

(a) Photoresist coating

- Spin coat AZ 5214E at $6000\,min^{-1}$ for $35\,s$ (ramp 1)
- Softbake at $100\,°C$ for $60\,s$

(b) Positive laser lithography

- Expose back-gate opening using Heidelberg Instruments MLA 150
- Parameters: $140\,MJ/cm^2$ power, 0 defoc

(c) Development

- Develop in AZ 726 MIF for 16-17 s
- Rinse twice in bubble rinse DI, $15\,s$ each
- Dry with N_2

(d) Oxide removal (Al_2O_3 and SiO_2)

- Etch in BHF for $240\,s$
- Rinse in DI for $10\,s$
- Dry with N_2

Deposition of Ti/Au Reinforcement Pads

(a) Photoresist coating

- Spin coat AZ 5214E at 6000 min^{-1} for 35 s (ramp 1)
- Softbake at 100 °C for 60 s

(b) Positive laser lithography

- Expose pad openings using Heidelberg Instruments MLA 150
- Parameters: 140 MJ/cm^2 power, 0 defoc

(c) Development

- Develop in AZ 726 MIF for 16-17 s
- Rinse twice in bubble rinse DI, 15 s each
- Dry with N_2

(d) Native Al_xO_y oxide removal

- Etch in BHF for 4-5 s
- Rinse in DI for 10 s
- Dry with N_2

(e) Metal sputtering (Von Ardenne HF Sputter)

- Sputter rates:
  - Ti: 4.6 nm/min at 50 W
  - Au: 0.6 nm/s at 25 W
- Load sample and pump down
- Set base pressure: $2 \cdot 10^{-6}$ $mbar$
- Set working pressure: $3 \cdot 10^{-3}$ $mbar$
- Clean sample: reverse sputter 5 layers at 100 W RF for 60 s
- Clean Ti target: 2 layers at 100 W RF for 60 s
- Deposit Ti: 5 nm at 50 W RF for 60 s
- Deposit Au: 180 nm in 5 layers at 25 W RF for 60 s

(f) Lift-off

- Soak in acetone at 50 °C for 30 min
- Rinse carefully with acetone using syringe
- Rinse in isopropyl
- Dry with N_2

Deposition of Ti/Au Top-Gates

(a) Photoresist coating

- Spin coat AZ 5214E at 6000 min^{-1} for 35 s (ramp 1)
- Softbake at 100 $°C$ for 60 s

(b) Laser lithography

- Expose using Heidelberg Instruments MLA 150
- Parameters: 140 MJ/cm^2 power, 0 defoc

(c) Development

- Develop in AZ 726 MIF for 16-17 s
- Rinse twice in bubble rinse DI, 15 s each
- Dry with N_2

(d) Metal deposition (Plassys MEB 550 SL e-beam evaporator)

- Load sample through load lock
- Pump down to $3 \cdot 10^{-8}$ $mbar$
- Ti deposition:
  - Ramp up e-beam current to set emission rate
  - Deposit 10 nm at 0.05 nm/s
  - Ramp down current
- Au deposition:
  - Change crucible and ramp up current
  - Deposit 120 nm at 0.05-0.1 nm/s
  - Ramp down current and switch off e-beam
- Unload sample through load lock

(e) Lift-off

- Soak in acetone at 50 $°C$ for 30 min
- Rinse carefully with acetone using syringe
- Rinse in isopropyl
- Dry with N_2

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