Microelectronic Engineering 299 (2025) 112333

Contents lists available at ScienceDirect

Microelectronic Engineering

journal homepage: www.elsevier.com/locate/mee

Theoretical insights into the impact of border and interface traps on hysteresis in monolayer MoS_2 FETs

Rittik Ghosh *, Alexandros Provias, Alexander Karl, Christoph Wilhelmer, Theresia Knobloch, Mohammad Rasool Davoudi, Seyed Mehdi Sattari-Esfahlan, Dominic Waldhör, Tibor Grasser *

Institute for Microelectronics (TU Wien), Gusshausstrasse 27–29, 1040 Vienna, Austria

ARTICLE INFO

Keywords:
2D FET
Hysteresis
CMOS
Reliability
Physics-based models

ABSTRACT

Threshold voltage hysteresis (ΔV_h) in two-dimensional transistor transfer characteristics poses a bottleneck in achieving stable 2D CMOS integrated circuits. Hysteresis is primarily attributed to traps at the channel/oxide interface as well as in the oxide. In this study, we present a physics-based self-consistent modeling framework to investigate the impact of border and interface traps on ΔV_h and apply it to monolayer (1-L) MoS_2 field-effect transistors (FETs). The transient trapping and detrapping of charges during gate voltage sweeps across a wide range of frequencies and temperatures is analyzed using a two-state non-radiative multi-phonon (NMP) model. Our results reveal distinct dynamic responses for slow border and fast interface traps, with border traps exhibiting slower time constants due to larger relaxation energies and interface traps showing fast nuclear tunneling-dominated dynamics resulting from the smaller relaxation energies. These simulations highlights the critical role of the spatial and energetic distributions of the traps in determining ΔV_h, providing insights into the stability of 2D FETs and paving the way for improved device engineering.

1. Introduction

For the continuation of Moore's law into the sub-decananometer regime, the use of two-dimensional (2D) materials has been suggested [1–3]. Among them, two-dimensional molybdenum disulfide (2D MoS_2) is widely studied as a promising channel material for atomically scaled transistors [4,5]. In contrast to conventional silicon technology, monolayer (1-L) MoS_2 offers a sizeable mobility at atomic thinness, ideally a clean surface, as well as direct electronic band gap. This was first demonstrated by Radisavljevic et al. in 2011 by integrating a 1-L MoS_2 with a double gated FET architecture [6]. These devices exhibited ON-OFF current ratios of about 10^8 and a sub-threshold swing (SS) of 74 mV/dec.

While 2D FETs show promising electrical and mechanical properties, their stability and reliability has not yet met the rigorous standards set by silicon technologies [7]. Most importantly, due to material quality issues and unfavorable electronic band alignments, 2D FETs exhibit threshold voltage (V_{th}) drifts in the $I_D(V_G)$ transfer characteristics as a result of charge trapping from pre-existing oxide traps [8–10]. Such instabilities pose a challenge for achieving stable 2D complementary metal-oxide semiconductor (CMOS) technology. The resulting electrostatic degradation highlights the sub-par quality of current 2D channel/oxide interfaces and the significant trap density in gate insulators deposited on the 2D materials as a result of the weak out-of-plane van der Waals interactions [8]. It is well-known that one of the primary reasons for the observed threshold voltage hysteresis (ΔV_h) in the $I_D(V_G)$ up/down gate voltage sweep originates from charge carriers being trapped at localized trap states. However, ΔV_h is sensitive to the spatial and energetic position of these traps within the oxide. In this context, traps can be classified into slow border and fast interface traps. Oxide traps located within a few nanometers from the channel are referred to as border traps. Their energy levels, relaxation energy and spatial distribution results in broad time constant (τ) distributions. Particularly in amorphous insulators such as HfO_2 and Al_2O_3, these distributions can be exceptionally wide. On the other hand, traps in the channel have a narrow τ distribution due to the more crystalline environment. In addition, the time constants are typically much smaller since the charge carriers are in very close vicinty to the traps. Extensive studies on these border and interface traps were conducted by Fleetwood et al. on the conventional Si/SiO_2 system [11]. Similarly, a comprehensive physics-based framework is needed to understand the impact of border and interface traps on the stability of 2D channel/oxide

* Corresponding author.
E-mail addresses: ghosh@iue.tuwien.ac.at (R. Ghosh), grasser@iue.tuwien.ac.at (T. Grasser).

https://doi.org/10.1016/j.mee.2025.112333
Received 5 February 2025; Accepted 24 February 2025
Available online 8 March 2025

systems.

In our recent study [12], we have reported a physics-based modeling technique for border and interface traps and their impact on ΔV_h in 1-L MoS_2 FETs. Although the study used suitable trap relaxation energies (E_R) and trap level (E_t) for modeling the traps, an in-depth investigation of the factors affecting ΔV_h is required. In this study, we employ a self-consistent modeling approach using our 1-D TCAD simulator Comphy [13,14]. Slow border and fast interface traps are modeled using available trap parameters from literature [15,16]. We employ a two-state non-radiative multi-phonon (NMP) model in the simulation framework to describe transient trapping/detrapping of charges. We analyzed ΔV_h dynamics over a wide range of sweep frequencies ($1/t_{sweep}$) to develop a closer understanding of the intricate trapping/detrapping dynamics. While it is commonly suggested that interface traps are too fast for observable ΔV_h [17], our dynamic simulations show that degradation from some interface traps could be measured at lower temperatures.

2. Device under test and simulation framework

In this study, an example 1-L MoS_2 FET is analyzed within the simulation framework. The device schematic is illustrated in Fig. 1(a). The device architecture employs an atomically thin 1-L MoS_2 with an electronic band gap of 2.06 eV [18–20], deposited on 12 nm thick hafnium dioxide (HfO_2) along with a 4.3 nm thick HfO_2 layer on top of the 1-L MoS_2 acting as a top gate (TG) insulator. The work function (E_w) of the palladium TG is assumed to be 5.2 eV [21]. The device dimensions are identical with our previous work [12] with W= 1 μm and L= 5 μm. The electronic band gap of HfO_2 is 5.7 eV [22]. Furthermore, the electron affinity (χ_s) of 1-L MoS_2 and HfO_2 is set to 4.2 eV [23] and 2.7 eV [24] respectively. The carrier mobility is assumed to be 80 cm^2/Vs along with an electron mass (m_e^*) of 0.56 and a hole mass (m_h^*) of 0.55 [25]. The device $I_D(V_{TG})$ is evaluated with $V_{TG} \in [-1.5\ V, 2\ V]$ for increasing drain voltage $V_D \in [0.01\ V, 0.5\ V]$ in Fig. 1(b) and (c) at room temperature. In this 1D compact model, the $I_D(V_{TG})$ characteristics are obtained by using an analytic drift-diffusion based approach described in [26].

3. Physics based modeling

The time-dependent threshold voltage drift (ΔV_{th}) in the $I_D(V_{TG})$ is modeled using the NMP model. In our 1D model, the ΔV_{th} that results from the capture of a single electron is evaluated using the charge sheet approximation (CSA) that assumes a uniform distribution of the net oxide charge (Q_t) parallel to the channel/oxide interface at a distance (x_T):

$$\Delta V_{th}(t) = -Q_t\left(1-\frac{x_T}{t_{ox}}\right)\frac{t_{ox}}{\epsilon_0\epsilon_r WL} \tag{1}$$

Here, the net oxide charge (Q_t) is determined by the elementary charge multiplied by the trap occupation probability, t_{ox} represents the oxide thickness, ϵ_0 is the vacuum permittivity and ϵ_r is the relative permittivity of the oxide. The NMP model approximates the two different trap charge states as parabolic energy curves (PECs) shown in Fig. 2, where a trap is characterized by E_R, E_T, x_T and the PEC minima offset (ΔQ) [13,27,28]. In the classical limit, the charge transfer between the trap and the reservoir occurs by overcoming a thermal barrier (ϵ_{12}) given by the intersection points of the PECs. This thermal barrier is governed by the parameters introduced above. The charge transition rates (k_{12}) depend exponentially on the thermal barriers and are given by [13,14,28]:

$$k_{12} = n v_{th}\sigma\vartheta e^{-(\epsilon_{12}-E_F+E_{CB})/k_BT} \tag{2}$$

where n represents the channel electron density, v_{th} is the thermal velocity, σ denotes the capture cross section, E_F is the Fermi level in the channel, E_{CB} is the channel conduction band energy and ϑ is the Wentzel-Kramers–Brillouin (WKB) tunneling coefficient. It is important to note that the trap occupation probability is a function of k_{12} which then influences ΔV_{th}. To model the border traps in HfO_2, the previously extracted trap parameters E_T=1.9 eV above MoS_2 valence band maxima (VBM), E_R=1.2 eV and ΔQ= 3 amu$^{1/2}$Å were used [15,16,28] along with σ_{E_T} and σ_{E_R} of 0.1 eV and 0.3 respectively [29]. Typically, traps located within the first few nanometers of the oxide contribute to an observable ΔV_h. Fig. 2(a) shows the PECs of both states (1 and 2) with an

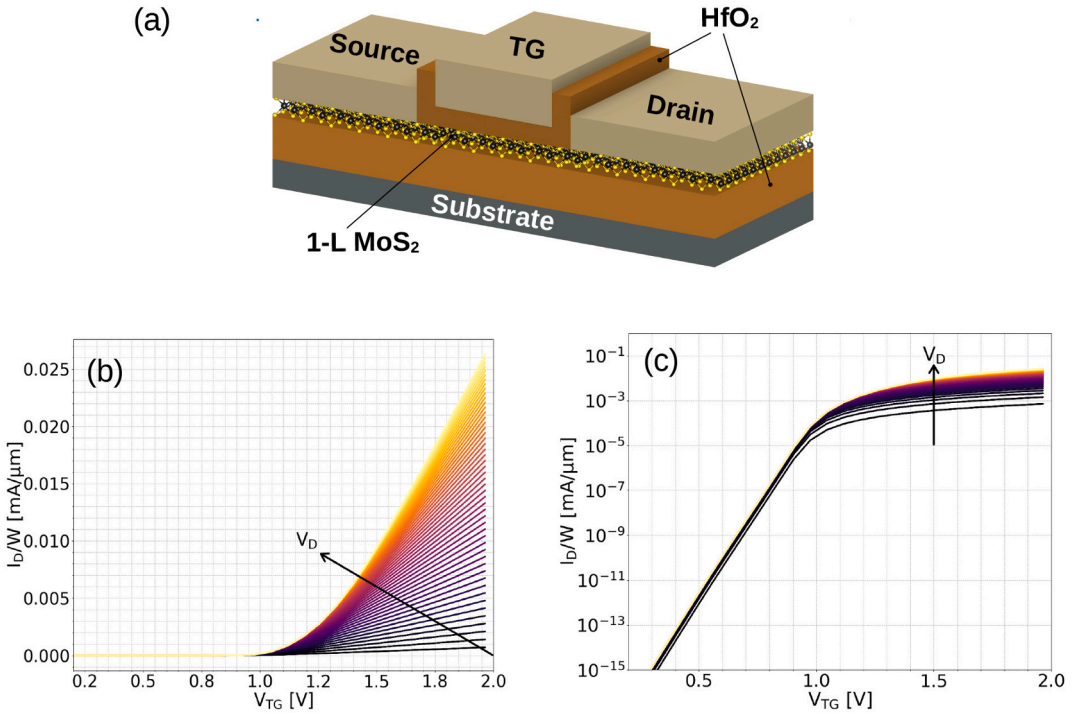

Fig. 1. (a) 3-D schematic of the 1-L MoS_2 FET. Simulated $I_D(V_{TG})$ characteristics for increasing drain voltages (V_D): (b) linear scale, (c) logarithmic scale.

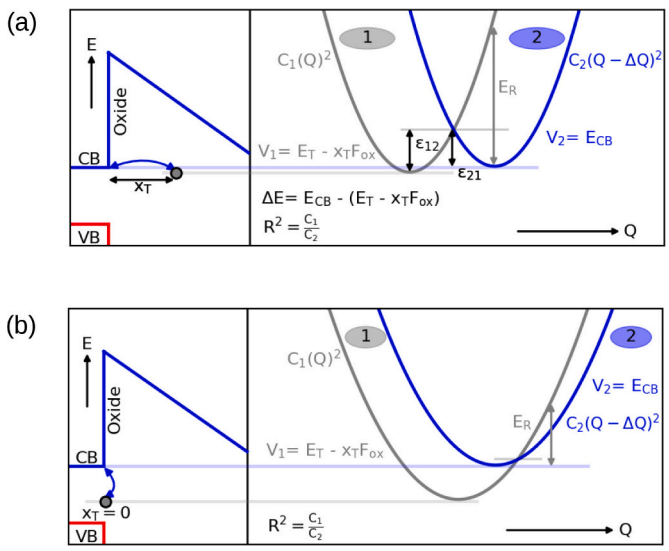

Fig. 2. Configuration coordinate diagram and the associated parameters (E_R, E_T, x_T, ΔQ) defining charge exchange within the harmonic approximation for (a) a border trap (b) an interface trap used in the NMP model. C_1, C_2 are the curvatures, R is the ratio of curvatures and ΔE is the energetic difference of the two PECs.

intersection between the two minima, indicating the strong electron-phonon coupling regime which is well described by Eq. (2). The comparatively large E_R of traps in the oxide together with the tunneling distance x_T leads to slower trap dynamics.

However, interface traps are right at the channel/oxide interface, meaning that x_T=0. In addition, since the channel is crystalline, E_R is small [30]. This typically results in weak electron-phonon coupling. To model interface traps, we use parameters typically for sulfur vacancies in MoS_2, E_T=1.5 eV above MoS_2 VBM and E_R=0.1 eV [12,30]. Compared to border traps, a much smaller value of σ_{E_T}, 0.05 eV is used. Hereby ΔQ is the crucial parameter as its value determines the nuclear tunneling probability which can (in many cases) be larger than the low probability to go over the thermally activated intersection point [13,28] as shown in Fig. 2 (b). Here, we use ΔQ= 1 amu$^{1/2}$Å [28,31]. In this regime, Eq. (2) cannot be used. Instead, full quantum mechanical (QM) charge transition rates $\left(k_{12}^{QM}\right)$ based on Fermi's golden rule have to be used [32]:

$$k_{12}^{QM}(T) = \frac{2\pi}{\hbar}|\theta_{12}|^2 \frac{1}{Z}\sum_{\alpha\beta}\left|\langle\eta_{1\alpha}|\eta_{2\beta}\rangle\right|^2 \delta(E_{1\alpha} - E_{2\beta})\, e^{-E_{1\alpha}/k_B T} \quad (3)$$

where θ_{12} represents the electronic matrix element, $E_{1\alpha}$ and $E_{2\beta}$ are the vibrational eigenenergies of each charge states. Here, the eigenenergy indices are denoted as α and β, $\eta_{1\alpha}$ and $\eta_{2\beta}$ are the vibrational wave functions and Z is the canonical partition function. The parameters used are consistent with the crystalline nature of the semiconductor (here 1-L MoS_2), which means that smaller E_R increases overlapping of the vibrational wave functions, allowing nuclear tunneling-mediated charge state transitions.

The impact of the gate bias on the trap occupation is shown in the energetic band diagrams in Fig. 3. Note that the border trap band is located within the MoS_2 electronic band gap. In Fig. 3(a), as V_{TG} becomes more positive, the border trap band bends downward, resulting in an increased number of trapping events within the oxide. On the contrary, since there is no spatial distribution of the interface traps as shown in Fig. 3(b), the trapping events are mostly independent of the oxide electric field (F_{ox}). A border trap density (N_{bt}) of 10^{19} cm^{-3} based on earlier studies [29] and an interface trap density (N_{it}) of 10^{12} cm^{-2} [25] is used in our simulations. The density of the occupied traps increases when the Fermi level (E_F) is swept across the band gap, shifting V_{th} during the corresponding up/down sweep. ΔV_h is extracted at $1/t_{Sweep}$= 10^3 Hz, shown in Fig. 4. Here, t_{Sweep} represents the sweep time for a complete up (V_{up}) and down sweep (V_{down}). To establish a consistent extraction method, a current criterion of 10^{-5}mA/μm is used. ΔV_h is extracted using this criterion by interpolating V_{up} and V_{down} near V_{th}. Fig. 4 (a) shows an observable $\Delta V_h \approx 18.6$ mV for the slow border traps while a significantly smaller $\Delta V_h \approx 0.01$ mV is obtained from the fast interface traps in Fig. 4 (b). The capture (τ_c) and emission (τ_e) time

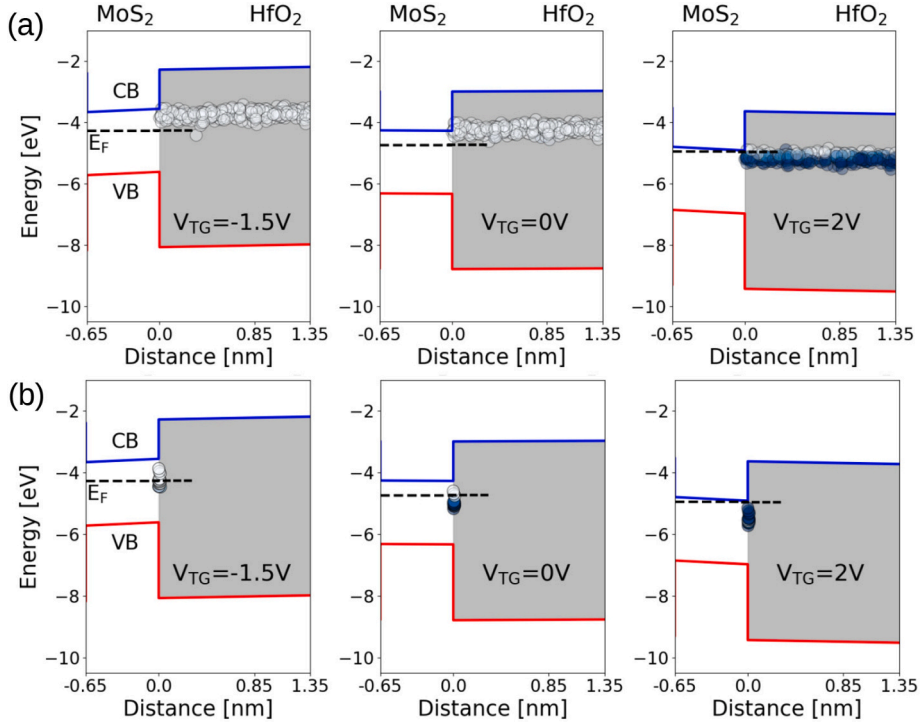

Fig. 3. Energy band diagram representing electron trapping in 1-L MoS_2/HfO_2 with suitable E_T for (a) border traps (b) interface traps.

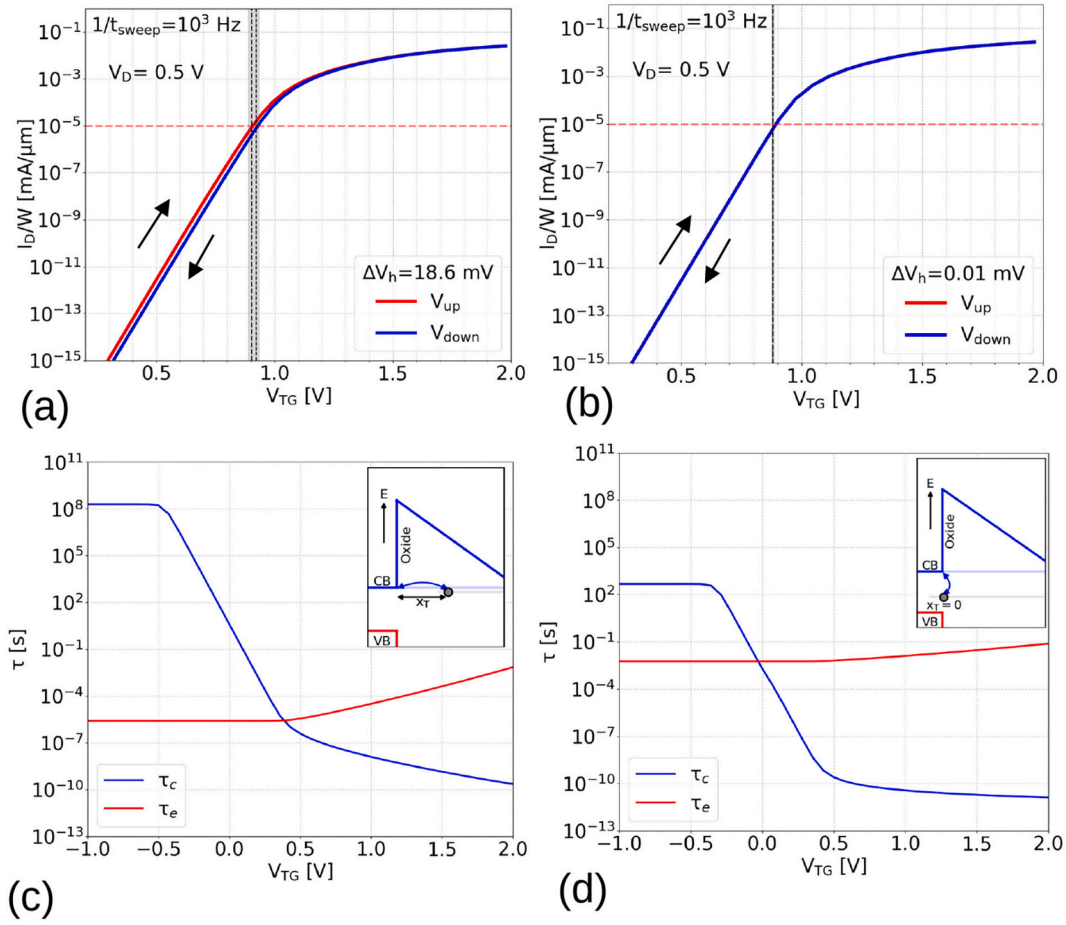

Fig. 4. ΔV_h extraction from the $I_D(V_{TG})$ profiles for (a) border traps and (b) interface traps. The capture and emission time constants for a single trap as a function of V_{TG} for (c) a selected border and (d) interface trap at room temperature.

constants as a function of V_{TG} are investigated for a selected border and interface trap in Fig. 4 (c) and (d), respectively. Traps can only actively contribute to ΔV_h if they can capture an electron during the up sweep but are too slow to emit it during the down sweep. In other words, this requires $\tau_c < \tau_e$ at the highest V_{TG} and $\tau_c > \tau_e$ at the lowest V_{TG} [25]. As discussed above, the slow border traps are associated with larger τ distributions which is consistent with Fig. 4 (c). Unlike slow border traps, fast interface traps can exchange carriers instantly with the semiconductor bands via nuclear tunneling, meaning that τ_e is independent of F_{ox} as shown in Fig. 4(d).

To study the complete ΔV_h dynamics, it has been suggested to consider a wide range of $1/t_{Sweep}$ [10,12,33,34]. In this work, we used $1/t_{Sweep} \in [10^{-6}\,\text{Hz}, 10^{9}\,\text{Hz}]$ for the theoretical analysis with an assumed measurement window of $1/t_{Sweep} \in [10^{-4}\,\text{Hz}, 10^{4}\,\text{Hz}]$ [10,33,34]. ΔV_h, when evaluated across a wide range of $1/t_{Sweep}$ values typically yields a bell-shaped curve. At slow $1/t_{Sweep}$, the traps remain close to their equilibrium state at every bias condition, which results in a small ΔV_h. A small ΔV_h is also observed at fast enough $1/t_{Sweep}$ since there is insufficient time for charge trapping/detrapping. Hence, ΔV_h at the peak $1/t_{Sweep}$ is the combination of suitably fast and slow sweeps. Fig. 5 (a)-(c) focuses on the dynamic response of ΔV_h as a function of $1/t_{Sweep}$ across different temperatures. Contrary to the slow border traps (blue line), the ΔV_h from fast interface traps (red line) lies mostly outside the measurement window for the studied temperatures. Notably, the validity of the NMP model at $1/t_{Sweep} > 1$ MHz remains uncertain due to factors such as the failure of the drift-diffusion model [35] and the frequency dependence of the permittivity [36]. Based on [37], the ΔV_h shift across $1/t_{Sweep}$ with temperature can be explained from the temperature

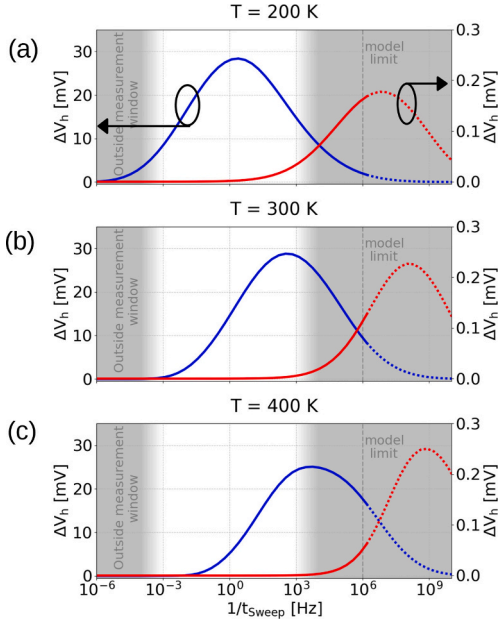

Fig. 5. Extracted ΔV_h vs. $1/t_{Sweep}$ for slower border (blue) and fast interface (red) traps at (a) 200 K (b) 300 K and (c) 400 K. Shaded regions show the $1/t_{Sweep}$ space outside the measurement window. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

dependence of the time constants. Therefore, an increase in the temperature reduces τ, making the traps faster thereby shifting ΔV_h towards faster $1/t_{Sweep}$. A key takeaway is that the Gaussian tail for the interface traps ΔV_h can shift inside the measurement window at lower temperatures, meaning that device degradation due to fast interface traps could be measurable at lower temperatures.

4. Conclusions

In this work, we have employed a physics-based self-consistent modeling framework to investigate the impact of border and interface traps on ΔV_h in 1-L MoS_2 FETs. Our simulations reveal that the spatial and energetic position critically influence their dynamic behavior. Border traps exhibit slower time constants due to large thermal barriers resulting from the large E_R, while the small E_R of interface traps results in the dominance of nuclear tunneling and shorter time constants. These findings provide a detailed understanding of the mechanisms governing ΔV_h, offering clarity on why border traps dominate within the typical measurement window, while interface traps can only contribute under specific conditions, such as lower temperatures or high sweep frequencies. Overall, the modeling approach presented lays the foundation for future studies exploring hysteresis phenomena in other 2D material systems or more complex device architectures.

Declaration of competing interest

The authors declare the following financial interests/personal relationships which may be considered as potential competing interests:

Rittik Ghosh reports financial support was provided by TU Wien University. If there are other authors, they declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgments

We acknowledge support by the Austrian Science Fund (FWF) through the doctoral college TU-DX [38] and the European Research Council (ERC) under Grant agreement no. 101055379 (F2GO).

Data availability

Data will be made available on request.

References

[1] Frank Schwierz, Jörg Pezoldt, Ralf Granzner, Two-dimensional materials and their prospects in transistor electronics, Nanoscale 7 (18) (2015) 8261–8283.
[2] Robert R. Schaller, Moore's law: past, present and future, IEEE Spectr. 34 (6) (1997) 52–59.
[3] Paolo Gargini, Francis Balestra, Yoshihiro Hayashi, Roadmapping of nanoelectronics for the new electronics industry, Appl. Sci. 12 (1) (2021) 308.
[4] Yu Yu Illarionov, et al., Process implications on the stability and reliability of 300 mm FAB MoS2 field-effect transistors, NPJ 2D Mater. Appl. 8 (1) (2024) 8.
[5] R. Bernard, et al., Electronic Transport in Bilayer MoS2 Encapsulated in HfO2, ACS Applied Materials & Interfaces, 2017.
[6] Branimir Radisavljevic, et al., Single-layer MoS2 transistors, Nat. Nanotechnol. 6 (3) (2011) 147–150.
[7] T. Knobloch, et al., Modeling the performance and reliability of two-dimensional semiconductor transistors, in: 2023 International Electron Devices Meeting (IEDM), IEEE, 2023, pp. 1–4.
[8] Luca Panarella, et al., Experimental-Modeling Framework for Identifying Defects Responsible for Reliability Issues in 2D FETs, ACS Applied Materials & Interfaces, 2024.
[9] Xiaolei Ma, et al., Defects induced charge trapping/detrapping and hysteresis phenomenon in MoS2 field-effect transistors: mechanism revealed by anharmonic Marcus charge transfer theory, ACS Appl. Mater. Interfaces 14 (1) (2021) 2185–2193.
[10] Yury Yu Illarionov, et al., The role of charge trapping in MoS2/SiO2 and MoS2/hBN field-effect transistors, in: 2D Materials 3.3, 2016, p. 035004.
[11] D.M. Fleetwood, et al., Effects of oxide traps, interface traps, and "border traps" on metal-oxide-semiconductor devices, J. Appl. Phys. 73 (10) (1993) 5058–5074.
[12] Rittik Ghosh, et al., Modeling the impact of interface and border traps on hysteresis in encapsulated monolayer MoS2 based double gated FETs, in: 2024 Austrochip Workshop on Microelectronics (Austrochip), IEEE, 2024, pp. 1–4.
[13] Dominic Waldhoer, et al., Comphy v3. 0—a compact-physics framework for modeling charge trapping related reliability phenomena in MOS devices, Microelectron. Reliab. 146 (2023) 115004.
[14] Gerhard Rzepa, et al., Comphy—a compact-physics framework for unified modeling of BTI, Microelectron. Reliab. 85 (2018) 49–65.
[15] Jack Strand, et al., Dielectric breakdown in HfO2 dielectrics: using multiscale modeling to identify the critical physical processes involved in oxide degradation, J. Appl. Phys. 131 (2022) 23.
[16] Eun Choi, Kee-Joo Chang, Charge-transition levels of oxygen vacancy as the origin of device instability in HfO2 gate stacks through quasiparticle energy calculations, Appl. Phys. Lett. 94 (2009) 12.
[17] Jae-Duk Lee, et al., Effects of interface trap generation and annihilation on the data retention characteristics of flash memory cells, IEEE Trans. Device Mater. Reliab. 4 (1) (2004) 110–117.
[18] Wenjun Hou, et al., First-principle insight into Ga-doped MoS2 for sensing SO2, SOF2 and SO2F2, Nanomaterials 11 (2) (2021) 314.
[19] Kristian Sommer Thygesen, Calculating excitons, plasmons, and quasiparticles in 2D materials and van der Waals heterostructures, 2D Mater. 4 (2) (2017) 022004.
[20] Filip A. Rasmussen, Kristian S. Thygesen, Computational 2D materials database: electronic structure of transition-metal dichalcogenides and oxides, J. Phys. Chem. C 119 (23) (2015) 13169–13183.
[21] Arpan De, et al., Investigation of MoS2 based dual gate MOSFET as a H2 sensor considering catalytic metal gate approach, in: 2022 IEEE VLSI Device Circuit and System (VLSI DCS), IEEE, 2022, pp. 5–8.
[22] Muhammad Usman, Christoph Henkel, Anders Hallén, HfO_2/Al_2O_3 bilayered high-k dielectric for passivation and gate insulator in 4H-SiC devices, ECS J. Solid State Sci. Technol. 2 (8) (2013) N3087.
[23] V.V. Afanas'ev, et al., Band alignment at interfaces of few-monolayer MoS_2 with SiO_2 and HfO2, Microelectron. Eng. 147 (2015) 294–297.
[24] Farah Hamid, et al., Reliability analysis of gate-all-around floating gate (GAA-FG) with variable oxide thickness for flash memory cell, in: 2020 4th IEEE Electron Devices Technology & Manufacturing Conference (EDTM), IEEE, 2020, pp. 1–4.
[25] Theresia Knobloch, et al., A physical model for the hysteresis in MoS2 transistors, IEEE J. Electr. Devices Soc. 6 (2018) 972–978.
[26] Enrique G. Marin, Samuel James Bader, Debdeep Jena, A new holistic model of 2-D semiconductor FETs, IEEE Trans. Electr. Dev. 65 (3) (2018) 1239–1245.
[27] Christoph Wilhelmer, et al., Over-and Undercoordinated atoms as a source of electron and hole traps in amorphous silicon nitride (a-Si3N4), Nanomaterials 13 (16) (2023) 2286.
[28] Tibor Grasser, Stochastic charge trapping in oxides: from random telegraph noise to bias temperature instabilities, Microelectron. Reliab. 52 (1) (2012) 39–70.
[29] Dieter Claes, Development of Reliable High-k Gate Dielectrics at Reduced Thermal Budget, for Integration on III-V Channels with Limited Thermal Stability and Sequential 3D Processing, 2022.
[30] Harikrishnan Ravichandran, et al., A stochastic encoder using point defects in two-dimensional materials, Nat. Commun. 15 (1) (2024) 1–11.
[31] Bernhard Ruch, et al., Applicability of Shockley–read–hall theory for interface states, IEEE Trans. Electr. Dev. 68 (4) (2021) 2092–2097.
[32] Jakob Michl, et al., Efficient modeling of charge trapping at cryogenic temperatures—Part I: theory, IEEE Trans. Electr. Dev. 68 (12) (2021) 6365–6371.
[33] A. Provias, et al., Reliability assessment of double-gated wafer-scale MoS_2 field effect transistors through hysteresis and Bias temperature instability analyses, in: 2023 International Electron Devices Meeting (IEDM), IEEE, 2023, pp. 1–4.
[34] Yury Yu Illarionov, et al., Improved hysteresis and reliability of MoS2 transistors with highquality CVD growth and Al_2O_3 encapsulation, IEEE Electron Device Lett. 38 (12) (2017) 1763–1766.
[35] Christoph Jungemann, et al., Failure of moments-based transport models in nanoscale devices near equilibrium, IEEE Trans. Electron Dev. 52 (11) (2005) 2404–2408.
[36] Kalim Deshmukh, et al., Dielectric spectroscopy, in: Spectroscopic Methods for Nanomaterials Characterization, Elsevier, 2017, pp. 237–299.
[37] Tibor Grasser, The capture/emission time map approach to the bias temperature instability, in: Bias Temperature Instability for Devices and Circuits, Springer, 2013, pp. 447–481.
[38] Austrian Science Fund (FWF), Research Radar - DOC 142, Accessed: 2024-12-11, 2024, https://doi.org/10.55776/DOC142.