

Reconfigurable Ge Transistors Enabling Adaptive Differential Amplifiers

Andreas Fuchsberger¹, Graduate Student Member, IEEE, Alexandra Dobler, Lukas Wind¹,
Andreas Kramer¹, Julian Kulenkampff¹, Maximilian Reuter¹, Daniele Nazzari¹,
Giulio Galderisi¹, Graduate Student Member, IEEE, Enrique Prado Navarrete¹,
Johannes Aberl¹, Moritz Brehm¹, Thomas Mikolajick¹, Fellow, IEEE,
Jens Trommer¹, Senior Member, IEEE, Klaus Hofmann¹, Senior Member, IEEE,
Masiar Sistani¹, and Walter M. Weber¹, Member, IEEE

Abstract—Exploiting the capabilities of multi-gated transistors is a promising strategy for adaptive and compensative analog circuits. Typically, reconfigurable transistors, which can be switched between n- and p-type operation at runtime, are used as universal transistors in fine grain programmable digital circuits. However, in the analog domain, by operating the transistors deliberately in intermediate states, they enable adjustments to application-specific requirements and allow for compensation of undesired deviations. Here, we propose a Ge-on-SOI transistor circuit primitive that enables an adaptable circuit design featuring n- and p-type common source (CS) and drain circuits, with electrostatically tuneable output-to-input ratio. Most notably, combined experimental and simulation studies promote verification and scalability assessment. Finally, the first experimental evidence of the electrostatic compensation of transistor/circuitpath-related device-to-device inequalities is shown in a differential amplifier featuring adaptable gain.

Index Terms—Adaptive circuits, electrostatic offset compensation, germanium, multi-gate transistors, reconfigurable transistors.

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Andreas Fuchsberger, Alexandra Dobler, Lukas Wind, Daniele Nazzari, Masiar Sistani, and Walter M. Weber are with the Institute of Solid State Electronics, Technische Universität Wien, 1040 Vienna, Austria (e-mail: masiar.sistani@tuwien.ac.at; walter.weber@tuwien.ac.at).

Andreas Kramer, Julian Kulenkampff, Maximilian Reuter, and Klaus Hofmann are with the Integrated Electronic Systems Laboratory, Technische Universität Darmstadt, 64289 Darmstadt, Germany.

Giulio Galderisi and Jens Trommer are with NaMLab gGmbH, 01187 Dresden, Germany.

Enrique Prado Navarrete, Johannes Aberl, and Moritz Brehm are with the Institute of Semiconductor and Solid State Physics, Johannes Kepler University Linz, 4040 Linz, Austria.

Thomas Mikolajick is with NaMLab gGmbH, 01187 Dresden, Germany, and also with the Chair of Nanoelectronics, Technische Universität Dresden, 01069 Dresden, Germany.

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I. INTRODUCTION

ADAPTABLE and thus application-specific implementations of systems and circuits enable energy and resource efficiency, as they can be tuned to best fit specific demands [1]. Therefore, facilitating the fundamental active primitives, the transistors, to become adjustable to required functionality holds the promise to realize efficient circuits, increasing the functional density in general [2], [3], [4], [5]. Moreover, this adaptability allows compensation of mismatching issues considering especially voltage and current variations and device-to-device inequalities due to e.g. fabrication variabilities [6], [7], [8]. The reconfigurable field-effect transistor (RFET) is such adaptive device that provides the possibility of toggling between n- and p-type operability during runtime [9], [10]. This selective configuration between one of the two states is particularly exploited in the digital domain in the form of logic circuits with fine-grain switchable logic [11], [12], [13], [14], [15] featuring, e.g., security primitives especially interesting for camouflaging applications in the field of hardware security [16], [17]. Recently, RFETs have been further functionally diversified by the implementation of a negative differential resistance (NDR) mode [18], [19], offering the possibility of realizing NDR-logic-based reconfigurable circuits [20]. Beyond that, analog blocks implementing frequency modulators have also been demonstrated providing a complete functional reconfiguration [21], [22], [23]. Additionally, in the analog domain, intermediate states can be used specifically to tune the properties of the corresponding RFETs according to the desired need to match individual devices in a circuit network, deliberately compensating for matching problems that become more important at scaled nodes. [24].

In this article, RFETs based on a Ge-on-SOI platform are proposed as fundamental circuit primitives for analog circuits. In this regard, common source (CS) and common drain (CD) circuits [25], [26], as well as basic differential amplifiers are implemented and investigated in terms of their potential control and adaptability. The symmetric n- and p-type characteristic of the applied Ge-on-SOI RFET [27] along with the bias-symmetric triple-gated arrangement [28], allows to realize adjustable n- and p-type CD and CS stages with the same circuit design providing a tuneable output-to-input

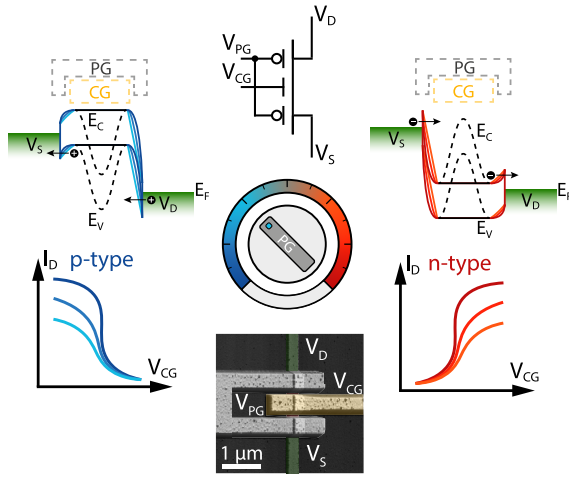


Fig. 1. Sketched principle of the electrostatically switchable n- and p-type operation of the proposed adaptive Ge-based SBFET using the PG functioning as a rotary switch. The respective equivalent circuit symbol and colored AFM image of the fabricated device are inserted.

ratio (gain). Connecting two stages leads consequently to a differential amplifier featuring enhanced functional density by allowing n- and p-type implementations with identical circuit designs with the possibility to control the individual transistor properties tailoring the amplification and compensating inequalities resulting potentially in undesired offset voltage or re-adaptions associated with operation regime shifts, so allowing electrostatic matching. The electrostatic controllability via additional electrodes, such as floating gates, provides a practical access point for various offset compensation strategies without the need for clocking or additional transistors [8], [29], [30], [31]. Moreover, the fabricated circuits and the experimental investigations are supported by simulations of a scaled 14 nm Ge nanowire RFET model [32], emphasizing the applicability of the proposed technology platform in the field of adaptive and compensative analog circuits.

II. EXPERIMENTAL RESULTS

A. Multi-Gate Ge Transistor Platform

The intended configurability of the Ge-on-SOI RFETs, is enabled by the electrostatic gating capabilities of the structure with gates directly above the metal-semiconductor junctions and in the middle of the channel. Circuits based on this basis element inherently possess the desired reconfigurability. Similar to a conventional MOSFET, the control gate (CG) in the middle of the channel controls the general charge carrier concentration and, consequently, the channel conduction. The polarity gates (PGs) directly atop both metal-semiconductor junctions are connected and consequently define the charge carrier type, so either electrons or holes pass the barrier. Additionally, the PG controls the injection capability, therefore tuning the electrical characteristic in terms of ON-state current and sub-threshold steepness, accordingly. This principle is illustrated in Fig. 1 including the circuit schematics of the RFET and an AFM-scan of the fabricated device, where the PG can be interpreted as a rotary switch determining the devices' behavior. Further, the presented band diagrams show schematically the

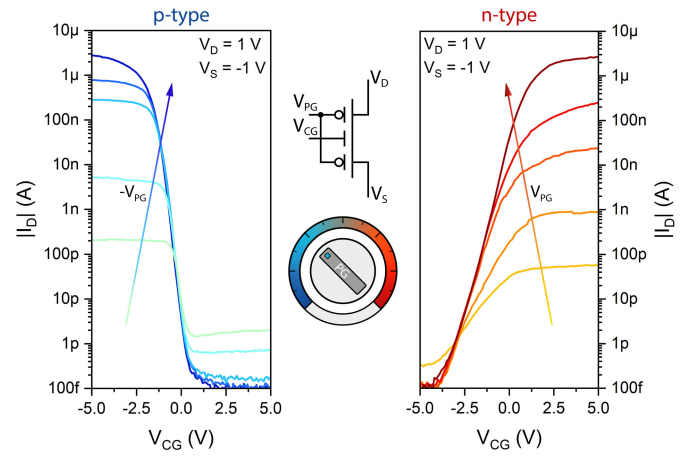


Fig. 2. Transfer characteristic of the n- and p-type operation modes of the proposed Ge RFET device for different V_{PG} .

related situation, where the effective tunnel barrier is thinned with higher absolute values of the applied PG voltage (either positive for electrons or negative for holes), while the CG voltage provides an additional barrier turning the channel on and off.

The used Ge-based RFETs provide symmetric ON-state regimes with a bias symmetric operability [27], allowing similar operation area for n- and p-type operation and dynamic adaption during run-time. Taking this bias symmetry, similar to standard CMOS transistors, where either positive (n-type) or negative (p-type) gate voltage in reference to the source potential must be applied, both operation types for the RFET can be implemented accordingly allowing the direct replacement of single transistors in conventional circuits. This is helpful in the circuit design domain as well-known designs can be adapted and diversified with the extended capabilities provided by RFETs. Therefore, the related transfer characteristic for the n-type (red) and p-type (blue) operation of the proposed Ge RFET is presented in Fig. 2, where the tuning of the transistor characteristic in dependency on the PG voltage is demonstrated.

B. Adaptive CS and Drain Circuits

As many complex integrated circuit designs are extensions or combined versions of basic building blocks, the focus is set on basic circuit primitives such as CS and CD amplifiers. PG taking the controllability of individual RFETs into account, circuit designs, consisting of two reconfigurable devices, not only comprising the ability to switch the functionality of the complete circuit, so enabling n- and p-type operation with the same design, but also tuning the characteristic output-to-input ratio for both n- and p-type operation, accordingly tailored to the application. Accordingly, Fig. 3(a) shows the n-type CS circuit, with the related circuit design as inset, where the upper RFET is used as an adjustable resistor by setting both the PG and CG voltage to a constant voltage level of 6 V. Considering the CG of the lower transistor (V_{CGL}) as input of the CS, the output-to-input ratio can be adapted by changing the V_{PGL} -voltage, i.e., from 3 to 6 V in 0.5 V steps.

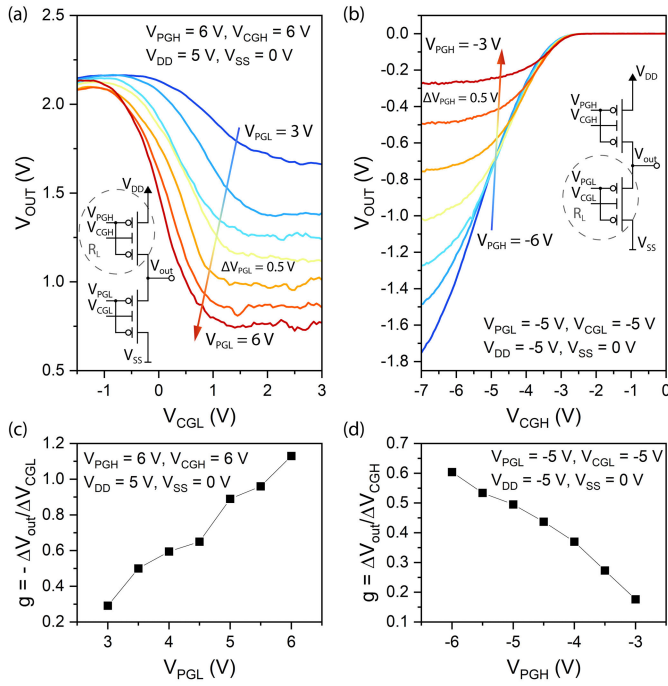


Fig. 3. (a) Transfer characteristic of the n-type CS circuit, where the upper RFET is used as resistor (inset). (b) Transfer characteristic of the p-type CD circuit, where the lower RFET is used as resistor (inset). (c) PG-related voltage-gain-controllability of the n-type CS circuit. (d) PG-related voltage-gain-controllability of the p-type CD circuit.

As evident, the associated maximum output-to-input ratio in dependency of the PGL-voltages, as presented in Fig. 3(c), increases with higher V_{PGL} starting from approx. 0.3 reaching gain values from approx. 1.2, indicating the need for sufficient high PGL-voltage for amplification as expected for the CS circuit, especially in the n-type regime. This increase in steepness is in line with the more efficient tunnel capability caused by the enhanced PG-related gating [27], as discussed before. Nonetheless, this degree of freedom can be used to tune the amplification in accordance with the application. This is particularly relevant considering a differential amplifier with non-matching transistors to compensate the offset voltage, as will be shown later.

To further exploit the concept of reconfigurability of the individual transistors and to investigate the potential of these RFET-based circuits, the p-type CD instead of the CS amplifier is presented in Fig. 3(b). Compared to the positive supply voltage V_{DD} of 5 V for the n-type CS circuit in Fig. 3(b), the bias direction is inversed by a V_{DD} of 5 V, while setting the transistors to p-type operation with a negative PG voltage. The proposed bias-symmetric Ge RFET architecture [27], which further provides symmetric n- and p-type operability, so similar operation regimes for holes and electrons, enables the use of the same circuit for CS and CD as well as for the n- and p-type configuration of those, as illustrated in the inset. Accordingly, to implement a p-type CD circuit, the lower, R_L -marked, RFET must be considered as an adjustable resistor by setting the related PG- and CG-voltages to 5 V. In the upper transistor, CG functions as input, whereas the PG introduces an additional degree of freedom by allowing the adaption of the output-to-input ratio. As evident, the more negative the PGH

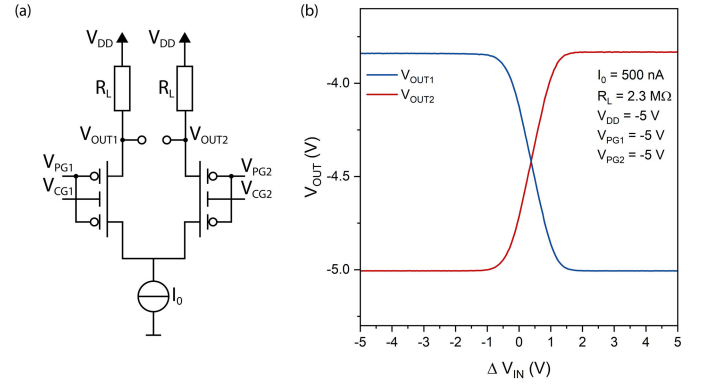


Fig. 4. (a) Proposed adaptive and compensative differential amplifier circuit consisting of two Ge-on-SOI RFETs. (b) Related transfer characteristic of the p-type differential amplifier. ($\Delta V_{IN} = V_{CG1} - V_{CG2}$).

value is, the steeper the slope in the active region of the CD, while the threshold voltage remains constant. The related peak output-to-input ratios reach from approx. 0.2 at 3 V up to about 0.6 at 6 V of V_{PGH} . To obtain a ratio closer to 1 as expected for the CD circuit, it is necessary to lower the PGH voltage further, meaning increasing the absolute values, consequently resulting in a more distinct p-type operation. This electrostatic adaptability is not only very useful in adjusting circuit parameters to specific requirements, but it also opens the door to compensate for mismatching issues and inequalities dynamically during runtime.

C. Offset Compensated Differential Amplifier

One prominent candidate for electrostatic offset compensation is the basic differential amplifier, which consists, in general, of two CS circuits. As presented in Fig. 4(a), the proposed adaptable differential amplifier is implemented with two Ge-on-SOI RFETs and external resistors of 2.3 M Ω . Considering the bias-symmetry of the transistors and the ability of the RFETs allowing electron and hole operation, the same circuit design can be used for n- and p-type differential amplifiers. Accordingly, Fig. 4(b) shows the experimental investigation of the p-type implementation, where the bias direction is inversed with a supply voltage V_{DD} of 5 V and an I_0 of 500 nA. As evident, the p-type differential amplifier in that configuration has a working point of about 4.4 V, which is in good agreement with the chosen device parameters and, however, an undesired offset of approx. 0.3-0.4 V which can be attributed to inequalities of the transistors and the external resistors.

In this regard, the potential of the adaptability of the RFETs is shown precisely in this case, as a perfect matching of the two circuit branches is not necessary at all, due to the ability of dynamic compensation. The PG voltage can be understood as an adjustable control switch, as already shown in Fig. 1, by tuning the electrical properties of the respective transistors so that the offset voltage is eliminated. To theoretically analyze the effect of PG voltage difference, the same circuit was first simulated using a scaled Ge RFET Verilog-A model. The model was designed to yield a maximum output current of 1400 $\mu\text{A}/\mu\text{m}$ at a nominal voltage of 0.8 V at

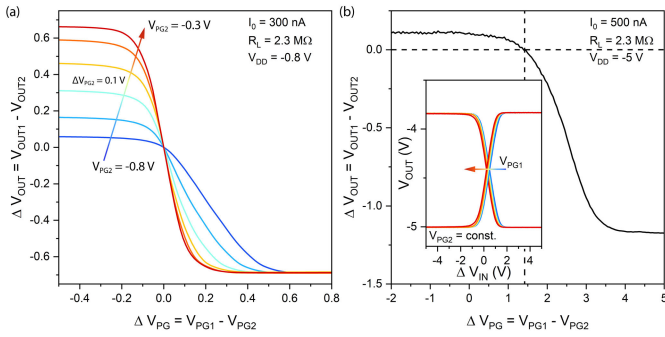


Fig. 5. (a) Simulated output voltage of the proposed differential amplifier concerning PG-related offset adjustment. (b) Electrostatic compensation of the offset by changing the PG voltage difference. The inset of (b) offset correction of varying PG1 at a constant PG2 voltage level.

all terminals [32]. Results are shown in Fig. 5(a), predicting a strong dependency of the output offset on V_{PG} . For the circuit simulation, the PG of the left (PG1) of two identical RFETs was swept from 0.5 to 0.8 V while the PG of the other RFET (PG2) was stepped from 0.8 to 0.3 V with a stepsize of 100 mV. Meanwhile, the CGs of both devices are held at a constant voltage of 0.8 V. The absolute output offset voltage increases with the difference between both PGs, showing the possible tuneability of the resulting offset voltage. As expected for identical devices, at an input voltage difference of 0 V the output also exhibits an offset of 0 V. While in this simulation identical devices are influenced to create an offset, which is in general undesired, the principle of adjusting the individual transistor characteristics electrostatically can be inversely used to compensate the offset caused by production variabilities in volume manufactured devices, such as line-edge-roughness (LER) or work-function-fluctuations [24], [33]. Accordingly, considering the fabricated differential amplifier, see Fig. 4(b), the experimentally determined compensation performance is given in Fig. 5(b), where the corresponding output voltage delta (ΔV_{OUT}) is plotted over the difference between the PG voltages (ΔV_{PG}) of the individual RFETs, revealing a needed delta of approx. 1.4 V to compensate the offset voltage. The inset of Fig. 5(b) shows one possible approach how to compensate the offset practically, by keeping V_{PG2} constant at 5 V and reducing the absolute value of V_{PG1} , so making the transistor less conductive resulting in a lower offset point for this configuration. Importantly, the PG voltages must remain within a certain operating range to ensure operability of the circuit in general, as already discussed above. Furthermore, the found offset-compensation value is only valid for one specific circuit configuration, in terms of applied voltages and used elements, and needs to be adjusted for every change. However, as RFETs feature run-time reconfigurability, the proposed circuit inherently provides this property by the extent of introducing further complexity, such as control circuits. Additionally, note that it is not absolutely necessary to keep one PG potential constant. With the chosen design both PG voltages could be simultaneously be changed to enable an offset compensation. Moreover, the external resistor can also be realized as an adjustable resistor, similar as already shown for the single CS/CD stages in Fig. 3, which would introduce

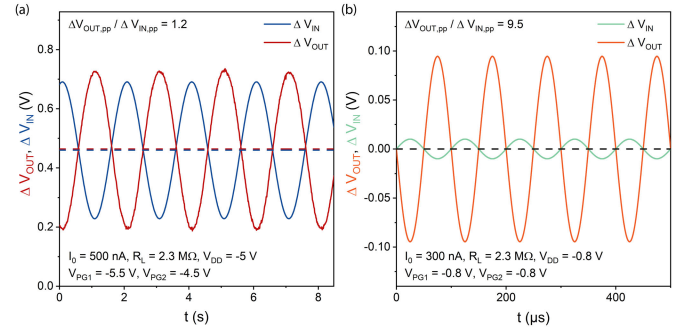


Fig. 6. (a) Experimentally determined transient behavior of the proposed differential amplifier in p-type operation. (b) Simulated transient investigations using the scaled Ge RFET model.

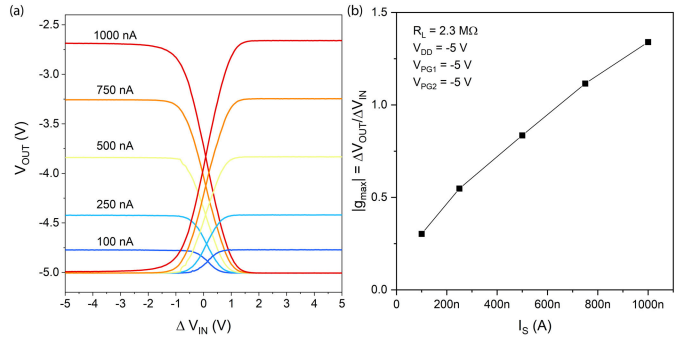


Fig. 7. (a) Voltage transfer characteristic of the p-type differential amplifier for different supply current values I_0 . (b) Related gain values for different I_0 .

an additional degree of freedom allowing the tuning of the individual paths, accordingly, and consequently supporting the compensative and adaptive ability of the proposed circuit design by the extend of increased complexity.

The principle of adapting the offset voltage can be used not only for compensative purposes of the differential amplifiers' offset, but also to set the differential output voltage, ΔV_{OUT} , to a specific dc output level. Accordingly, Fig. 6(a) shows the transient investigation of the experimentally characterized differential amplifier set to p-type operation, with a supply voltage V_{DD} of 5 V, an I_0 of 500 nA, and external resistors of 2.3 MΩ. Importantly, the difference of the PG voltages of -1.5 V introduces an increase of the offset voltage resulting in an output dc level similar to the dc level of the input signal of approx. 0.46 V, while having an absolute value of amplification of 1.2. The possibility to adjust the normally undesired offset voltage features an additional degree of freedom, which can also offer some advantages utilizing signal adjusting circuits, i.e., as an intermediate stage for subsequent optimized stages. Moreover, emphasizing the potential of the proposed transistor technology, the transient investigations are also performed with the scaled Ge RFET simulation model, with a supply voltage V_{DD} of 0.8 V, an I_0 of 500 nA, and external resistors of 2.3 MΩ, revealing a potential frequency range above 10 kHz, while providing an amplification up to 9.5 and the possible adaptability and compensation of the offset voltage. In addition to scaling, there are also other strategies specifically designed to enhance amplification such as more complex input stages or adapting general parameters like supply voltage and current.

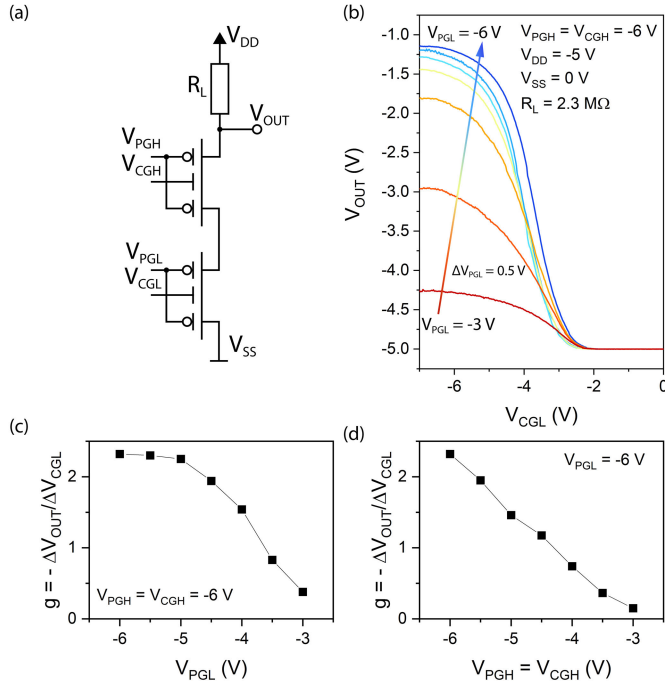


Fig. 8. (a) Schematics of the implemented cascode circuit. (b) Transfer characteristic of the p-type cascode circuit for different V_{PGL} -values. (c) V_{PGL} -related gain-controllability with constant V_{PGH} and V_{CGH} and (d) $V_{PGH} = V_{CGH}$ -related gain-controllability for a constant V_{PGL} of the p-type cascode circuit.

To further underline the stability of the proposed differential amplifier as well as to enhance the output-to-input ratio, different supply current values (I_0) are investigated. As evident, in Fig. 7(a), for increasing I_0 -values the operation regimes are unaffected, while the absolute values of the working point decrease and the slopes of the active region get steeper resulting in higher output-to-input ratios. Fig. 7(b) shows exactly this increase from approx. 0.3 at 100 nA to approx. 1.4 at 1000 nA for 5 V at PGs and as the supply voltage. Importantly, within this supply current operation regime, the ability to electrostatically adjust the offset point, ideally compensating it, is still applicable but with adapted PG voltage differences, as discussed before. The inherent configurability of the RFETs makes it possible to not only tune the amplification and optimize dynamically the circuit but also to adapt to “outer,” occasionally undesirable, changes such as current or voltage variations within larger circuitry, allowing to retain specific requirements. For instance, with an unstable current supply, to keep a desired constant amplification, the PG voltages can be either increased or decreased, accordingly, resulting in a change in conductivity of the transistors and, consequently, in the general amplification. However, to achieve a stable and constant working point, the resistors need also to be designed to be adjustable, similar to the one shown for the CS/CD circuits (Fig. 3).

D. Gain Enhancement by Cascode Circuits

In terms of improving the output-to-input ratio, an additional potential approach is the improvement of the input stage,

as the CS circuit can be exemplarily replaced by a cascode circuit or more advanced stages. Emphasizing the abilities of the configurable circuits, Fig. 8 shows the investigation of the p-type cascode circuit, as it can be used to increase the amplification. Fig. 8(a) gives the experimentally investigated cascode circuit, where the adaptable CS/CD implementation is extended with an additional external resistor, comprising half of the differential amplifier with a basic cascoded input stage. Importantly, similar to before, the proposed circuit can be configured for n- and p-type operation with altered bias direction and operation modes for the individual transistors. Accordingly, Fig. 8(b) exhibits the captured output voltages V_{OUT} over V_{CGL} , considering the lower RFET, consequently CGL, as input and the upper RFET as adjustable transistor configured with 6 V at V_{CGH} and V_{PGH} . The load resistor R_L is 2.3 M Ω and the supply voltage V_{DD} is 5 V for that specific measurement. To examine the influence of the gating capabilities, the PG of the input transistors is changed from -3 to 6 V in 0.5 V-steps resulting in the expected change in steepness while retaining stable operation regimes underlying the potential of tuning the output-to-input ratio. The determined maximum values of the slope for this configuration over various PGL-values are depicted in Fig. 8(c), reaching gain values above 2.3. The improved steepness can be explained by the enhanced tunnel probability, as already shown before for the CS/CD-circuit (Fig. 3). Moreover, the implementation of the upper transistor as adjustable one introduces another degree of freedom to control the output-to-input ratio, as presented in Fig. 8(d), where V_{PGL} is set to -6 V, while changing CGH and PGH of the upper RFET, accordingly, providing an almost linear control knob of the gain within the specific operation regime.

III. CONCLUSION

In conclusion, applying the concept of reconfigurability, inherently featured by the proposed multi-gate device architecture, we have, for the first time, experimentally demonstrated adaptable analog circuits utilizing RFETs. The electrostatic controllability of the proposed Ge-based transistors allows the dynamic adaption of circuit parameters, such as the output-to-input ratio, to required specifications during run-time, which can be distinctively used to compensate undesired mismatches caused occasionally due to voltage- or current-variations, especially within larger circuits and systems, or transistor/circuit-path inequalities due to fabrication variations. Additionally, this control feature enables also to tailor the circuit to application-specific needs by using the available degree of freedom, i.e., in changing the gain with the related gating, accordingly, potentially resulting in an altered operation regime, which can also be re-adapted in order to meet the requirements like offset compensation. Not only the circuit parameters but also the complete functionality of the circuit can be adapted by switching the RFET operability, allowing the implementation of CD and CS circuits for n- and p-type operation with the same circuit design, permitting the adjustment and compensation of non-ideal characteristics.

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