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Temperature-dependent electronic transport in reconfigurable transistors based on Ge on SOI and strained SOI platforms☆

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ABSTRACT

Integrating Ge onto SOI should enhance the drive currents and switching speeds of transistors. However, Ge on insulator platforms have fallen short of providing these benefits and are additionally facing processing issues and high fabrication costs. To cope with these issues, we use an ultra-low-temperature molecular-beam epitaxy growth of Ge layers on SOI and strained SOI substrates, as device prototyping platforms. Thereof, we obtain symmetric IV-on-states in Ge based reconfigurable transistors, enabling to investigate the temperature-dependent gating capabilities and identify the dominant transport mechanisms. In this respect, to give a comprehensive picture of the influence of different parameters on transport mechanisms, temperature-dependent gate- and bias-dependent current–voltage data was evaluated constructing 2-D colormap representations.

1. Introduction

Reconfigurable field-effect transistors (RFETs), with their ability of dynamic run-time switching of both n- and p-type operation in a single device, are interesting candidates to implement multi-function logic cells, like switchable NAND/NOR gates [1,2]. These devices employ two independent gate electrodes to steer charge polarity and source-drain conductance. The integration of Ge on SOI platforms introduces potential benefits such as higher on-state currents and consequently faster switching speeds due to lower effective masses and higher carrier concentrations enhancing the performance of transistors [3,4]. However, unstable Ge-oxides along with high fabrication costs of Ge on insulator (GeOI) wafers [5] and reliable contact formation [6] are problematic and obstruct so far the use of Ge platforms. In this work, we propose two Ge-advanced (001)-surface oriented SOI platforms, one with highly compressive and bidirectionally-strained Ge grown on a conventional SOI substrate (GeSOI) and the other with Ge layers grown on a strained-SOI (GesSOI) exhibiting a more relaxed strain level. Both are covered by a 3 nm thin Si capping layer. These platforms bypass the mentioned issues by encapsulating Ge with Si and SiO_2 and using Al as source/drain contacts constituting an Al-Si-Ge multi-heterojunction [7]. Gating spectroscopies, allow the examination and interpretation of charge carrier transport in a more comprehensive and resilient fashion compared to a single operation point analysis [8]. Importantly, such temperature-dependent gating control maps have already provided the basis for setting up table based compact models [3,9].

2. Results and discussion

The triple-gated RFET, as used for the platform comparison, is presented in the false-color AFM image in Fig. 1**a**. Polarity gates (PG) are placed atop the metal–semiconductor junctions to control the tunneling barrier shape and transmissibility and define consequently the charge carrier type. The control gate (CG) in the middle of the channel introduces a further barrier for controlling the transistor's source-drain conductivity. The two Ge platforms are presented schematically as stacks in Fig. 1b with dimensions provided. The differences between GeSOI and GesSOI is the Ge layer thickness and the related strain

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introduction from the underlying Si or s-Si layer. The Ge including the Si buffer layer is grown via ultra-low temperature molecular-beam epitaxy [10] upon conventional SOI or s-SOI wafers, illustrated in green colors in Fig. 1b. The use of s-SOI substrates enables to grow thicker pseudomorphic Ge layers for the same growing conditions, because the layers exhibit a more relaxed level or strain [11,12]. Out of the proposed Ge-advanced SOI stacks, the nanosheet mesa-structures were patterned in top-down methodology, with subsequent lithography, etching, Si-cap oxidation and ZrO_2 encapsulation by atomic layer deposition steps [7], eventually comprising the material systems depicted in Fig. 1b. Nanoscaled mono-crystaline Al Schottky barrier (SB) contacts were fabricated via a thermally activated solid-state exchange reaction previously described in Ref. [13]. Compared to our prior art with Ge nanowires and GeOI devices, we observe an enhanced thermal stability of the junctions towards Al as well as higher stability in the IV characteristics, as assumed to be attributed to lower value of interface- and border-trap densities at the semiconductor/insulator interface [7]. The gating was performed by Ti/Au atop the SiO_2/ZrO_2 stack, where the pinning is set with 10 nm of Ti, while Au was used as a bonding contact.

To allow the electrostatic mode-switching, as illustrated by band diagrams in Fig. 2, the PG controls the injection capabilities allowing either electrons (positive voltages) or holes (negative voltages) passing the SBs. Additionally, comparable to an accumulation mode MOSFET, the CG controls the charge carrier concentration in the channel, consequently introducing a further barrier by applying a positive or negative voltage depending on the charge carrier type. The corresponding on- and off-states are labelled with roman numerals to make the identification of associated regimes in the following figures clearer.

Considering the band diagrams, transfer characteristics for a swept CG voltage and a constant PG voltage, either 5 V for n- or -5 V for p-type operation, are depicted in Fig. 3**a** for both transistor platforms. The GesSOI exhibits a more 0 V-symmetric behaviour with narrower threshold voltages (V_{th}), steeper sub-threshold slopes (STHS), as well as higher drive currents for both p- and n-types, compared to GeSOI. These features are also evident in the statistical evaluation provided in Fig. 3b. The off-state currents for both platforms is in the 100 fA-region and even below, especially for GesSOI, which is given by the resolution limit of the measurement setup. This fact leads to an impressive on-to-off-state ratio for both Ge SBFETs types of approx. 1×10^7 to 1×10^8. Differences between platforms are likely due to the different Ge thickness as well as different in-plane strains due to the use of unstrained or tensile-strained Si templates. The gate leakage current remains insignificant under the resolution limit for both RFETs, as also evident in grey in Fig. 3a.

To provide a more general picture and emphasize the stability of those transistor platforms, the switching capabilities were investigated. Thereto, Both CG and PG voltages were swept accordingly from -5 V to 5 V, while keeping the source-drain bias voltage constant at 2 V. The

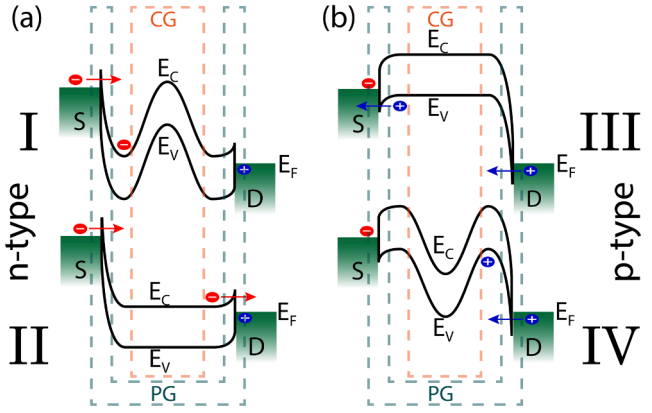

Fig. 2. Band diagram of the n-type (a) and p-type (b) operation.

captured drain-current data is presented in colored maps, allowing estimations of on- and off-state regions as well as current variations caused by unstable voltage gating, which can occur in electronic systems. As shown, in Fig. 4 for both transistor platforms, there are distinct on-state regions, indicated with *II* and *III* and outlined with a dashed line as guide to the eye, and off-state areas, indicated with *I* and *IV*. Indeed, the results confirm that the GesSOI (Fig. 4b) has wider and more symmetric on-state regimes over a large range of gate operation voltages compared to the GeSOI RFET (Fig. 4a).

Linearizing the captured drain current for each temperature, from RT up to 400 K in 25 K-steps for the GeSOI and 50 K-steps for the GesSOI platform, at each CG/PG-related operation point in the gating capability maps, Fig. 5 shows the determined slope, i.e. the drain-current gradient over temperature ($dI_D[V_{CG}|V_{PG}]/dT$). As evident in this representation, the on-state temperature dependency of regions *II*, *III* can be assessed. Both platforms exhibit for p-type (region *III*) operation a negative gradient for a sufficiently high PG voltage applied, which is an indication of a transparent contact [13]. This is consistent with a smaller SB height for holes vs. electrons leading to the high $I_{on,p}/I_{on,n}$ ratio. Interestingly, this negative slope area for GeSOI is preceded for smaller $|V_{PG}|$ by a region with a positive gradient indicating a barrier dominated transport. A distinct constant V_{CG} boundary line is observed between these two regions. Apparently, the PG can tune the barrier for hole injection to be so thin so that tunneling dominates. For the n- type on-state region (*II*), the barrier is slightly higher so that this high transparency region cannot be entered within the operation region. However for GesSOI (Fig. 5b) negative gradients in both regions *II*, *III* imply high contact transparency for both electrons and holes. Interestingly, there is a V_{CG} dependent transition in GesSOI for the gradient change of sign. (Fig. 5b).We speculate that these differences arise from the distinct band edge offsets and effective masses as tuned by biaxial strain, nevertheless

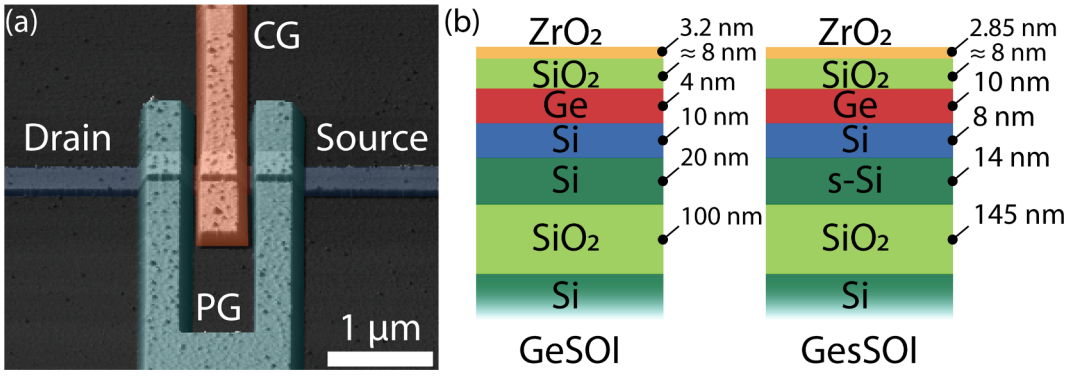

Fig. 1. (a) False-color AFM image of a triple-gated RFET. (b) GeSOI and GesSOI stacks with individual layer thicknesses. The MBE-grown layers are colored blue (Si) and red (Ge). (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

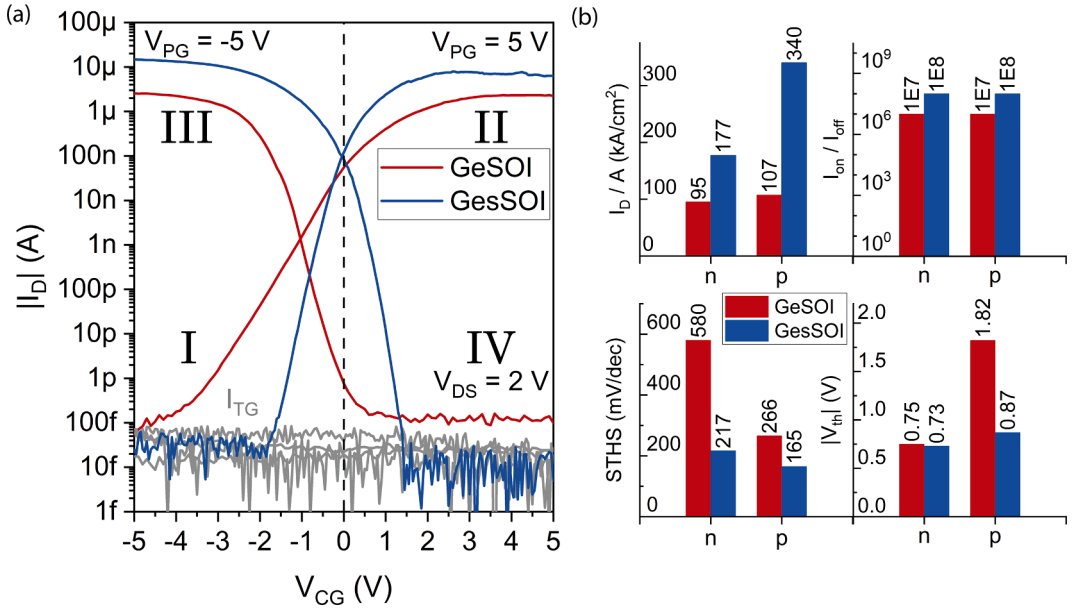

Fig. 3. (a) Transfer characteristic of both operation modes of the used Ge platforms. (b) Statistics of relevant parameter of the presented device platforms.

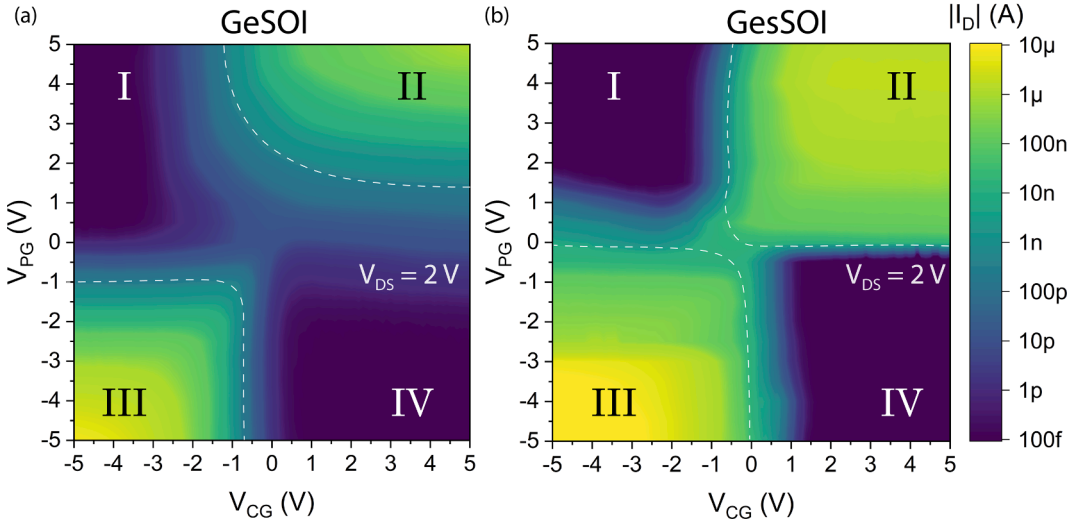

Fig. 4. Gating capability maps of the GeSOI (a) and GesSOI (b) platform.

further verification with theory is required e.g. with device TCAD simulations.

To determine the relative temperature gradient and make assumptions about the dominant underlying transport mechanism [4,14], the extracted change of each CG/PG-related operation point is normalized to the corresponding RT drain current $(1/I_D[V_{CG}|V_{PG}](RT)\cdot dI_D[V_{CG}|V_{PG}]/dT)$, see Fig. 6. For both plat-forms the relative change of the off-state region for electrons and holes (*I*, *IV*) is substantially more pronounced than the on-state regions (*II*, *III*). This can be explained by considering thermionic contributions as being the major part of the off-state current, whereas tunneling, which is less temperature-dependent, becomes more dominant in the on-state, which is characteristic for SBFETs [14]. In particular, the normalized temperature gradient reveals the intermediate region where tunneling- and thermionic emission-related currents are respectively dominating, see area *II* in Fig. 6a. This is in line with the idea that, for n-type operation for the GeSOI (Fig. 6a), bands are not bent sufficiently strong by gating to make the heterotructure transparent.

Apart from determining the temperature gradient, by applying the simplistic thermionic emission theory[15], the activation energy, as an abstraction over two metal–semiconductor junctions with various gating potentials, supports the identification of the on- and off-state regions and the dominant transport mechanisms. Accordingly, the gating capability measurements, see Fig. 4, are captured for different temperatures from RT up to 400 K.

Using the following equation $J_{TE}(T)=A^*T^2\exp(-E_a/k_BT)$, with J_{TE} the measured current normalized over the cross-sectional area and A^* the effective Richardson constant, the related activation energy E_a can be determined by linearizing the Arrhenius plots according to $\ln|J_{TE}/T^2| = \ln|A^*| - E_a/k_BT$, where the natural logarithm was applied. The corresponding activation energy is extracted by $E_a = -k\cdot k_B$, with k being the slope of the linearization [16]. Note, for the use of the thermionic emission theory it is necessary to make assumptions and limitations of applicability [15,16]. However, in accordance with the temperature gradient investigations, such activation energy maps obtain carefully interpretations of transport mechanisms regimes. Additionally, different models and theories can be applied to accomplish the picture of the gating-related charge carrier transport [17]. The extracted

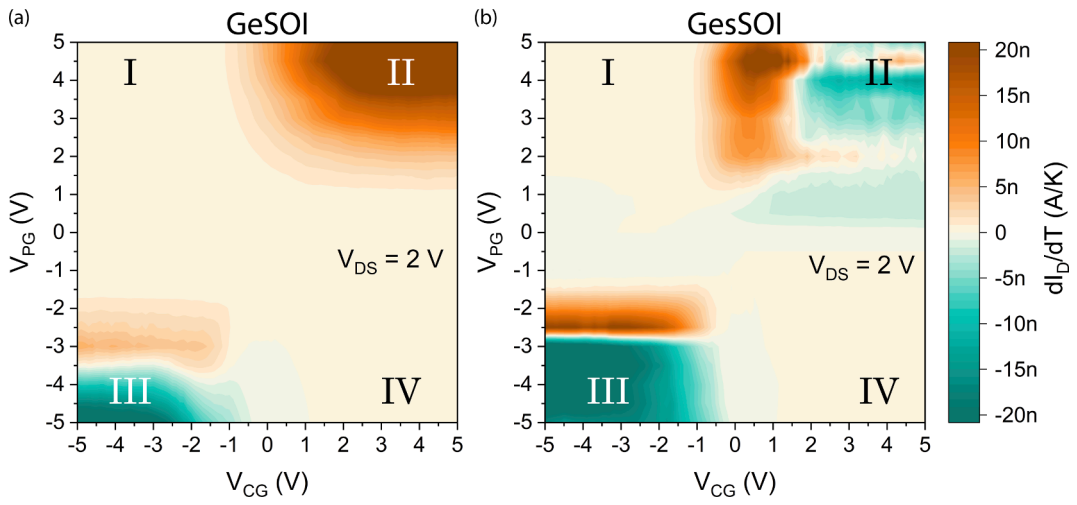

Fig. 5. Temperature dependency of the gating capability maps of both transistor platforms, GeSOI (a) and GesSOI (b), considering temperatures from RT up to 400 K.

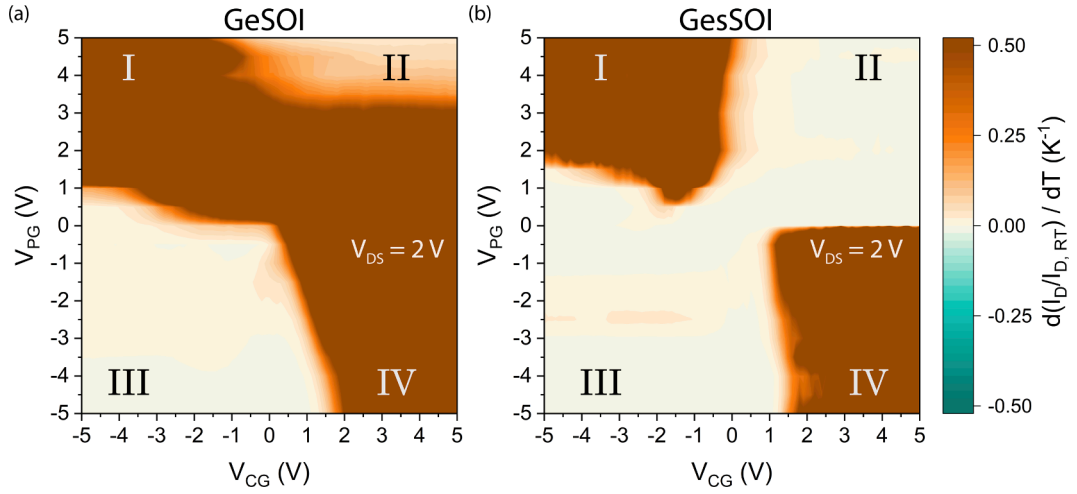

Fig. 6. Room-temperature normalized temperature dependency of the gating capability maps of both transistor platforms, GeSOI (a) and GesSOI (b), considering temperatures from RT up to 400 K.

activation energy maps of both Ge platforms are presented in Fig. 7. Comparing both material platforms, the already identified on- and off-state areas are also visible. Especially, a transparent heterojunction, as indicated with a low to negative activation energy, is clearly obtained for the GesSOI (Fig. 7b) for n- and p-type on-state operation (*II*, *III*) and for the GeSOI (Fig. 7a) for the p-type on-state (*III*), whereas the n-type

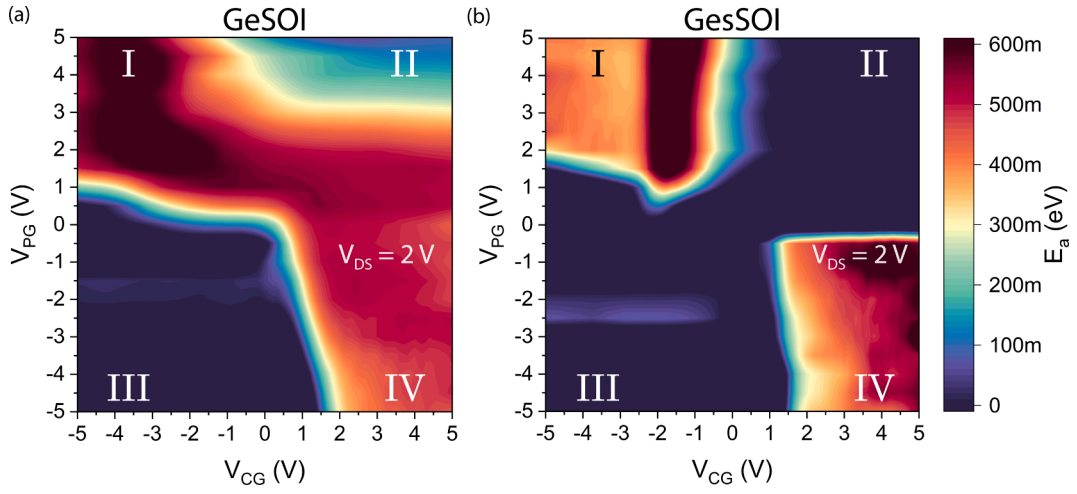

Fig. 7. Related activation energy of the gating capability maps of both transistor platforms, GeSOI (a) and GesSOI (b).

on-state (*II*) exhibits only a lowered barrier.

Comparing all color map representations (Figs. 4–7), a very consistent impression is obtained, as for the GesSOI platform very center-symmetric on- and off-state areas related to the gating is evident, with a negative temperature dependency and a low or even negative activation energy for the on-state regions (*II*, *III*) indicating a transparent heterojunction [13]. Contrary, the GeSOI exhibits transparency only for p-type operation (*III*). For n-type operation (*II*) the related bands are not bent sufficiently to enable high tunnelling transmissibility thus resulting in a positive temperature gradient and consequently only a lowered activation energy, indicating the presence of an intermediate region between tunneling and thermionic-dominated regions. However, by increasing the gating voltages, it is possible to force also the GeSOI RFETs into transparency for n-type operation. This negative activation energy is in strong contrast to SBFET devices with common metal-germanide-Ge junctions, which are not obtaining transparency limiting consequently on-state conduction [18]. The off-state regions (*I*, *IV*) for both platforms are thermionic dominated, as determined via the normalized temperature gradient and can be assessed with the relatively higher activation energy in that areas. Interestingly, the GeSOI platform exhibits a continuous off-state area especially for low gating voltages, different to the GesSOI. This property can also be estimated by considering the crossing-point at higher currents for both operation types in transfer characteristics (Fig. 3a). We attribute this to Ge layer thickness and strain differences in the different systems. Nonetheless, this does not mean that the transistor cannot be turned off, only that sufficient gating voltage must be applied to achieve off-states.

3. Conclusion

We investigated two different advanced Ge- on SOI transistor platforms in terms of temperature-dependent gating capabilities. Key for this investigation is the stable operability of the devices, which is related to the encapsulation of the Ge channel within Si/s-Si underneath and in between the Al-Si-Ge multi-heterojunction as well as the SiO_2 layer atop the Ge channel. While the characteristic transistor metrics, except for on-state symmetry, were improved using the GesSOI platform, this wafer stack is more complex to fabricate. Importantly, for both platforms, the temperature gradient in combination with the activation energy of the gating capability maps allowed to determine the regions of tunneling-dominated on-states and thermionic emission-dominated off-states as well as intermediate regions where no mechanism is dominant.

CRediT authorship contribution statement

Andreas Fuchsberger: Writing – original draft, Visualization, Methodology, Investigation, Formal analysis, Data curation. **Lukas Wind:** Methodology, Investigation. **Daniele Nazzari:** Methodology. **Johannes Aberl:** Methodology. **Enrique Prado Navarrete:** Methodology. **Moritz Brehm:** Methodology. **Jean-Michel Hartmann:** Methodology. **Frank Fournel:** Methodology. **Lilian Vogl:** Investigation. **Peter Schweizer:** Investigation. **Andrew M. Minor:** Investigation. **Masiar Sistani:** Writing – review & editing, Project administration, Methodology, Investigation, Funding acquisition, Conceptualization. **Walter M. Weber:** Writing – review & editing, Validation, Supervision, Methodology, Funding acquisition, Conceptualization.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Data availability

Data will be made available on request.

References

[1] Wind L, Maierhofer M, Fuchsberger A, Sistani M, Weber WM. Realization of a complementary full adder based on reconfigurable transistors. IEEE EDL 2024;45(4):724–7.
[2] Galderisi G, Mikolajick T, Trommer J. The rgate: An 8-in-1 polymorphic logic gate built from reconfigurable field effect transistors. IEEE EDL 2024;45(3):496–9.
[3] Baldauf T, Heinzig A, Mikolajick T, Weber WM. Scaling aspects of nanowire Schottky junction based reconfigurable field effect transistors. EUROSOI-ULIS 2019:1–4.
[4] Weber W, Mikolajick T. Silicon and germanium nanowire electronics: Physics of conventional and unconventional transistors. Rep Prog Phys 2017;80(6):066502.
[5] Choudhary S, Schwarz D, Funk HS, Weißhaupt D, Khosla R, Sharma SK, et al. A steep slope mbe-grown thin p-ge channel fets on bulk ge-on-si using hzo internal voltage amplification. IEEE TED 2022;69(5):2725–31.
[6] Nishimura T. Understanding and controlling band alignment at the metal/germanium interface for future electric devices. Electronics 2022;11(15):2419.
[7] Fuchsberger A, Wind L, Nazzari D, Kühberger L, Popp D, Aberl J, et al. A runtime reconfigurable ge field-effect transistor with symmetric on-states. IEEE JEDS 2024;12:83–7.
[8] Jeon D-Y, Zhang J, Trommer J, Park SJ, Gaillardon P-E, De Micheli G, et al. Operation regimes and electrical transport of steep slope Schottky Si-FinFETs. JAP 2017;121(6):064504.
[9] Quijada JN, Baldauf T, Rai S, Heinzig A, Kumar A, Weber WM, et al. A germanium nanowire reconfigurable transistor model for predictive technology evaluation. IEEE Trans Nanotech 2022:1–8.
[10] Aberl J, Brehm M, Fromherz T, Schuster J, Frigerio J, Rauter P. SiGe quantum well infrared photodetectors on strained-silicon-on-insulator. Opt Express 2019;27(22):32009.
[11] Salomon A, Aberl J, Vukušić L, Hauser M, Fromherz T, Brehm M. Relaxation delay of Ge-rich Epitaxial SiGe films on Si(001). Phys Stats Sol (A) Appl MaterSci 2022;219(17):2200154.
[12] J. M. Hartmann, A. Abbadie, S. Favier, Critical thickness for plastic relaxation of SiGe on SI(001) revisited, J Appl Phys 110 (8).
[13] Wind L, Sistani M, Böckle R, Smoliner J, Vukušić L, Aberl J, et al. Composition dependent electrical transport in $Si_{1-x}Ge_x$ nanosheets with monolithic single-elementary Al contacts. Small 2022;18(44):2204178.
[14] Schwarz M, Vethaak T, Derycke V, Francheteau A, Iniguez B, Kataria S, et al. Calvet, The Schottky barrier transistor in emerging electronic devices. Nanotechnology 2023;34(35):352002.
[15] Rhoderick E, Williams R. Metal-Semiconductor Contacts. Oxford: Oxford University Press; 1988.
[16] Fuchsberger A, Wind L, Sistani M, Behrle R, Nazzari D, Aberl J, et al. Reconfigurable field-effect transistor technology via heterogeneous integration of SiGe with crystalline al contacts. Adv Electr Mat 2023;9(6):2201259.
[17] Pacheco-Sanchez A, Claus M. Device design-enabled Schottky barrier height extraction for nanoFETs based on the 1D Landauer-Büttiker equation. APL 2017;111(16):163108.
[18] Marshall E, Wu C, Pai C, Scott D, Lau S. Metal-germanium contacts and germanide formation. MRS Proc 1985;47:161.