DISSERTATION

Integrated Circuits for Photonic Quantum Simulators

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Curiosity is the key to problem solving

Galileo Galilei (1564 – 1642)

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I. Kurzfassung

Quantensimulatoren sind essenzielle Werkzeuge, die versprechen die Geheimnisse der Quantenmechanik zu lösen und verschiedene Bereiche zu revolutionieren, welche für klassische Computer oft unüberwindbare Herausforderungen darstellen. Ein photonischer Quantensimulator verwendet Photonen als Qubits, welche die grundlegende Einheit der Quanteninformation darstellt. Diese sind vergleichbar mit klassischen Bits, Qubits können sich jedoch in einer Superposition zweier Zustände befinden [1].

Diese Dissertation beschreibt die Entwicklung von (opto)elektronisch integrierten Schaltkreisen für einen integrierten photonischen Quantensimulator, der im Rahmen eines EU-Projektes entwickelt wurde. Eine Photonisch Integrierte Schaltung (engl. photonic integrated circuit, PIC) ermöglicht gatterbasierte Quantensimulationen mit Pfadkodierung, die Implementierung von Quantengattern mit Interferometern und die Auswertung der Ergebnisse mit Einzelphotonen-Lawinenfotodioden (engl. single photon avalanche diode, SPAD). Dabei müssen die elektronischen Schaltkreise dreidimensional (3D) mit der PIC integriert werden, wobei die Verlustleistung gering sein muss, um die PIC so wenig wie möglich zu beeinflussen.

In der vorliegenden Arbeit wird die Entwicklung und Charakterisierung der anwendungsspezifischen integrierten Schaltungen (engl. application-specific integrated circuit, ASIC), welche in der 0,18 µm Hochspannungs-CMOS-Technologie von X-FAB entworfen und in zwei Produktionsläufen hergestellt wurden, beschrieben. Die Mixed-Signal-Schaltungen verteilen sich auf vier Heizungssteuerchips (PWM-ASICs) und einen Gater-ASIC für die Kontrolle der SPADs. Im Forschungsprojekt wurden zwei Versionen des Gater-ASIC entworfen, ein Gater-ASIC mit monolithisch integrierten SPADs und ein Gater für externe SPADs, die mittels Drahtbond-Technik mit dem ASIC verbunden sind.

Die Gater-ASICs verwenden eine hohe Überspannung (engl. excess bias voltage) von bis zu 9,9 V und sind vollständig mit dem Takt des Quantensimulators synchronisiert. Jeder ASIC verfügt über neun unabhängige Kanäle, welche detektieren können, ob zumindest ein Photon innerhalb eines einstellbaren Zeitfensters eintrifft. Das kürzest mögliche Zeitfenster ist knapp unter 1 ns lang. Der Gater mit externen SPADs weist dank des sehr kurzen Zeitfensters eine

äußerst niedrige Dunkelzählrate von etwa 10 bis 100 Dunkelzählungen pro Sekunde sowie eine hohe Photon-Detektions-Wahrscheinlichkeit (engl. photon detection probability, PDP) von ungefähr 70 % auf (635 nm; 9,9 V Überspannung). Ein Kanal erreichte sogar eine noch höhere PDP von beinahe 80 %. Der Gater mit integrierten Silizium-SPADs erzielt eine PDP von etwa 50 % bei einer Wellenlänge von 635 nm und einer Überspannung von 9,9 V. Beide Gater-ASICs haben eine Gesamtleistungsaufnahme von weniger als 250 mW und eine sehr schnelle Anstiegsgeschwindigkeit von über 20 GV/s an der Kathode.

Der PWM-ASIC verwendet ein pulsdauermoduliertes (eng. Pulse-width modulation, PWM) Spannungssignal, um die Temperatur der Interferometer zu steuern und gleichzeitig die Verluste innerhalb der PWM-ASIC und damit den Gesamtstromverbrauch des Quantensimulators drastisch zu reduzieren. Die variable Pulsdauer des PWM-Signals bestimmt direkt die durchschnittliche Heizleistung an den Heizwiderständen. Die PWM-Erzeugung basiert auf einem Verzögerungsleitungsansatz (engl. delay-line approach) und liefert einen Spannungshub von 9,9 V, welcher mit dem Takt des Quantensimulators synchronisiert und auf eine Basisfrequenz von bis zu 100 MHz ausgelegt ist. Der Chip verfügt über 40 PWM-Kanäle, von denen jeder bis zu 130 mW Heizleistung an die 750 Ω Widerstände liefern kann. Acht zusätzliche Transimpedanzverstärker-Kanäle (eng. Transimpedance amplifier, TIA) stehen zur Verfügung, die eine Echtzeitüberwachung der optischen Leistung innerhalb der PIC zur Charakterisierung ermöglichen. Die Heizleistung jedes Kanals lässt sich individuell über eine SPI-Schnittstelle einstellen.

Alle (opto)elektronisch integrierten Schaltkreise sind monolithisch in den ASICs integriert, wodurch zusammen mit der PIC ein dreidimensional integrierter Quantensimulator möglich wird. Die entwickelten Topologien legen den Grundstein für einen kostengünstigen integrierten Quantensimulator mit einer großen Anzahl von Quantengattern und Detektoren, welcher bei Raumtemperatur betrieben werden kann. Die neuartigen Ansätze aller ASICs sind vollständig skalierbar und können leicht auf eine größere Anzahl von Qubits erweitert werden. Ein Quantensimulator mit einer großen Anzahl an Qubits bietet der Menschheit erhebliche Potenziale, indem er hilft, komplexe quantenmechanische Probleme zu verstehen und Lösungen für Herausforderungen zu finden, die bisher nicht simuliert oder experimentell überprüft werden konnten.

II. Abstract

Quantum simulators are crucial tools that promise to solve the mysteries of quantum mechanics and revolutionise various fields that are often prohibitively difficult for classical computers. A photonic quantum simulator uses photons as qubits, which are basic quantum information, analogous to classical bits but capable of being in a superposition of two states [1]. In this thesis, the (opto)electronic integrated circuits of an integrated photonic quantum simulator were developed within the framework of an EU project. A photonic integrated circuit (PIC) enables gate-based quantum simulations with path encoding, implementation of quantum logic gates with interferometers, and evaluation of the results with single-photon avalanche diodes (SPADs). The electronic circuits must be 3D integrated to the PIC, and the power dissipations need to be low to keep the PIC as cool as possible.

In this thesis, full custom application-specific integrated circuits (ASICs) were designed and produced in two wafer production runs using 0.18 µm high-voltage CMOS technology from X-FAB. The necessary mixed-signal circuits are split into four heater control chips (PWM ASICs) and a Gater ASIC for the SPADs. Two versions of the Gater ASIC were investigated, a Gater ASIC with monolithically integrated SPAD and a Gater for external SPADs wire-bonded to the ASIC.

The Gater ASICs employ a high excess bias voltage of up to 9.9 V and are fully synchronised to the clock of the quantum simulator. Nine individual channels are monolithically realised within every ASIC and each channel can determine if a single photon arrives during the adjustable gating time window, which can be slightly shorter than 1 ns. The Gater with external SPADs on the PIC outputs an extremely low dark count rate in the range of 10 to 100 counts per second, thanks to the short gating windows, and reaches a high photo detection probability PDP of approximately 70 % (635 nm; 9.9 V excess bias). The best channel reaches a PDP of nearly 80 % with the 9.9 V excess bias. The Gater with integrated silicon SPADs achieving a PDP of around 50 % at a wavelength of 635 nm with 9.9 V excess bias. Both Gater ASICs have a total power consumption of less than 250 mW and a cathode slew rate well above 20 GV/s.

The PWM ASIC uses a pulse-width modulation (PWM) signal to control the temperature of the interferometers to drastically reduce the losses within the

chips and therefore the overall power consumption of the quantum simulator. The variable duration of the pulse directly determines the average heating power delivered to the resistors. The PWM-ASIC uses a delay-line approach to generate the PWM signal and outputs a voltage swing of 9.9 V. The PWM Signal is synchronised to the clock of the quantum simulator and supports a base clock of up to 100 MHz. The chip incorporates 40 PWM channels, each capable of delivering up to 130 mW to 750 Ω heating resistors. Eight additional transimpedance amplifier (TIA) channels are available, enabling real-time monitoring of optical power levels within the PIC for characterisation. The heating power of each channel can be set individually via an SPI interface.

All (opto)electronic circuits are monolithically integrated within the ASICs which enable with the PIC a 3D integrated quantum simulator.

The developed topologies lay the foundation for a cost-effective integrated quantum simulator with a huge number of quantum gates and detectors that can be operated at room temperature. The novel approaches of all ASICs are fully scalable and can be easily extended to a larger number of qubits. A quantum simulator with a large number of qubits offers significant potential to humanity by helping to understand complex quantum mechanical problems and to find solutions to challenges that could not be simulated or experimentally tested so far.

III. Acknowledgement

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VI. List of Abbreviations

APP	After-pulsing probability
AQC	Active quenching circuit
ASIC	Application-specific integrated circuit
ASIC	Application specific integrated circuit
CMOS	Complementary metal-oxide semiconductor
DCR	Dark count rate
DMIM	Double metal-insulator-metal
epi	Epitaxial
ESD	Electrostatic discharge
FPGA	Field-programmable gate array
HQC	Hybrid quenching circuit
InGaAs	Indium gallium arsenide
MEMS	Microelectromechanical systems
MIM	Metal-insulator-metal
MLM	Multi-layer-mask
MOSCAP	Metal oxide semiconductor capacitor
MOSFET	Metal–oxide semiconductor field-effect transistor
PCB	Printed circuit board
PDM	Pulse-density modulation
PDP	Photon detection probability
PIC	Photonic integrated circuit
PQC	Passive quenching circuit
PVT variations	Process, voltage, and temperature variations
PWM	Pulse width modulation
SiN	Silicon nitride
SPAD	Single-photon avalanche diode
SPAD	Single-photon avalanche diode
SPI	Serial peripheral interface
STI	Shallow trench isolation

TEC	Thermoelectric cooler
TIA	Transimpedance amplifier

1. Introduction

1.1 Motivation and Introduction

Quantum simulators are controllable quantum systems that can be used to mimic and investigate other quantum systems [2]. In many research fields, such as quantum physics, quantum simulators have become an extremely versatile and powerful tool. Quantum simulators are crucial tools that promise to solve the mysteries of quantum mechanics and revolutionise various fields that are often prohibitively difficult for classical computers. By enabling the controlled emulation of complex quantum phenomena, these simulators offer insights into fundamental physics, accelerate the discovery of novel materials, optimise quantum technologies, and address societal challenges. With their potential to advance scientific understanding and drive technological innovation, quantum simulators represent a fundamental step towards unleashing the power of quantum mechanics for the benefit of humankind. Compared to quantum computers, which are universal systems, quantum simulators are especially designed to investigate a limited set of quantum systems or one specific quantum system. These custom systems are often less error-prone and are easier to realise in practice. Although photons are challenging to employ in universal quantum computing due to their bosonic nature and lack of mutual interaction, they are promising candidates as quantum objects for quantum simulators. Individual photons that function as fundamental carriers of quantum information are used in photonic quantum simulators. They are manipulated through a variety of optical elements such as beam splitters, phase shifters, and integrated waveguides to enable precise control over their quantum state. Photonic quantum simulators have undergone strong development in recent years and are able to solve real problems like optimisation problems. Quantum advantage was reached with a Gaussian boson sampling quantum simulator published in 2020 [3]. Although in 2021 further progress in complexity and scaling was shown in [4], it also indicates a problem with further scaling of these systems. Integrated silicon photonics seems, especially because of its small size, to be very promising for significant further

scaling. A big advantage of integrated optoelectronics is that control and redout circuits can theoretically be directly integrated onto the same chip. Although current quantum simulators still work with very few photons, integration promises to greatly increase this number in future years. [5]

Photonic quantum simulators often use three main stages, the preparation, the manipulation (quantum interference circuit), and the detection stage, as shown in Figure 1. Using a static structure of photonic components in the manipulation stage does not offer the possibility of making changes or adjustments to the function. To keep the simulator flexible and cope with process and temperature variations at the same time, programmable components are necessary. One method to get this flexibility is the usage of configurable phase shifters in the arms of integrated interferometers, which are built from integrated waveguides [6]. To control the phase shifters, different physical effects, such as the thermo-optic effect, can be used to change the reflective index [7]. When the temperature of the material changes, the reflective index changes, and therefore the phase shift. Heating resistors can be used to individually control the temperature in each arm of the phase shifter. To regulate the temperature of a large number of integrated phase shifters, an energy efficient way to control the power of the heating resistors is necessary. [5]

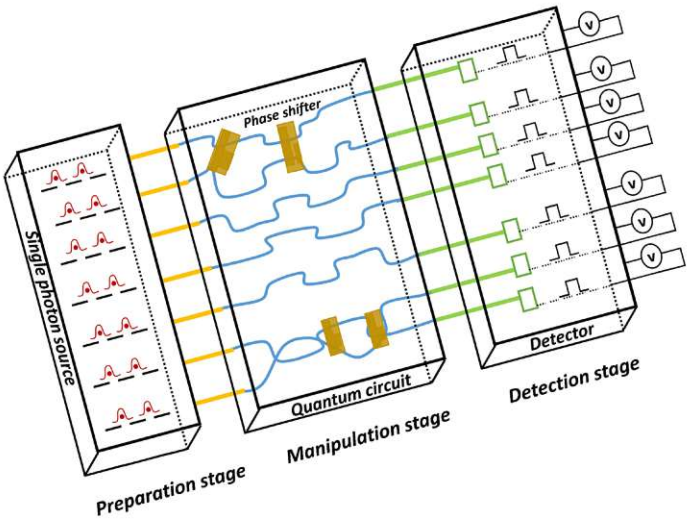


Figure 1 - Basic architecture of a photonic quantum simulator. Adapted from [8]

Using a simple constant (in time) current or voltage approach generates, depending on the output power, a huge amount of loss in the regulator, and therefore, unwanted heat, which might influence the individual phase shift itself as well as the necessary cooling of the complete chip. Switching the resistors fully

on for only a specific time could ideally eliminate the losses in the controller, because either the current or the voltage across the control circuit is zero. In a real switch, this would not be the case, but it can significantly reduce losses compared to the constant voltage or current approach. This so-called pulse width modulation (PWM) synchronised to the photon source is used to control the heaters in this work. [5]

The photons coming from the manipulation stage need to be detected and the results processed. The input of the detection stage are single photons on different paths. Therefore, multiple photon detection which can also detect single photons is required. To integrate the detectors directly into the CMOS chip single-photon avalanche diode (SPADs) with electronic circuits are investigated in this work. Unlike other photodiodes they can operate in the Geiger mode, where they can detect single photons with a high photon detection probability.

The usage of PWM heating control and integrated photon detection enables high efficiency, lower power consumption and photon losses. It enables the construction of quantum simulators that are fully integrated and function at room temperature. This is necessary for the photonic quantum simulator developed in the EU Horizon project EPIQUS. The project is set to develop an affordable, user-friendly, and high-performance quantum simulator by fully integrating silicon nitride photonics with ASICs (silicon electronics) investigated in this work which are responsible for the control and read out of the integrated photonics chip (photonic integrated circuit, PIC). The primary goal of this project is to establish a foundational technology by delivering the first breakthrough device that can simulate quantum mechanical problems within a compact unit operating at room temperature. [9], [10]

In this work, all electronic application-specific integrated circuits are designed for the EPIQUS photonic quantum simulator. The designed ASICs control the photonic components and detect the results (single photons) of the quantum simulator. Two full MLM production runs are done for this work. The ASICs from the first run were designed for wire bonding, while those from the second run are intended to be flip-chip (3D integration) mounted. The mixed-signal circuits are split into four heater control chips (PWM ASICs) and to the gating circuits for the single-photon avalanche diodes (SPADs). All ASICs are synchronised to the laser pulses. To be active only when photons are expected, the active gating window needs to be very

short, ideally shorter than 1 ns. Within this thesis a Gater ASIC with external SPADs (wire bonded to the PIC) and a Gater ASIC with integrated SPADs are investigated. Two production runs are conducted with different sized integrated SPADs.

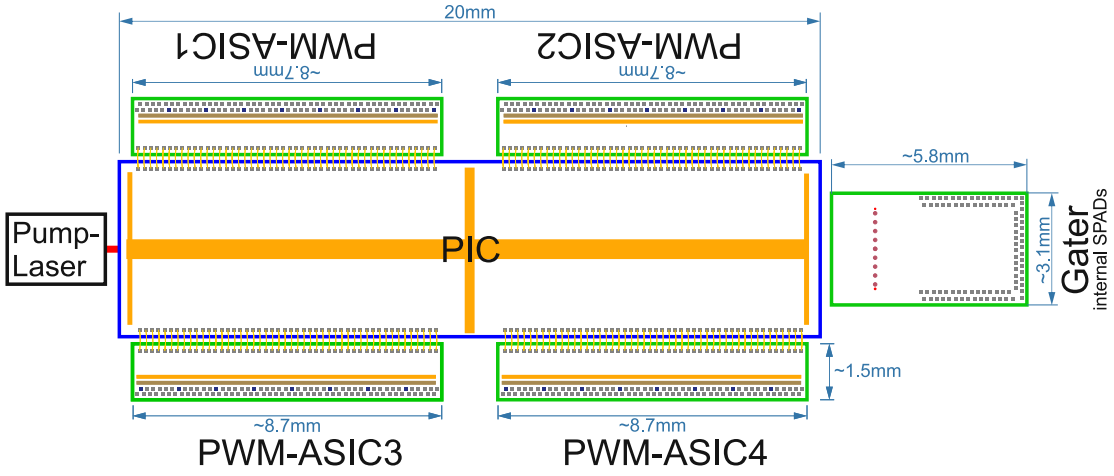


Figure 2: Overview of components of the quantum simulator with the Gater with integrated SPADs.

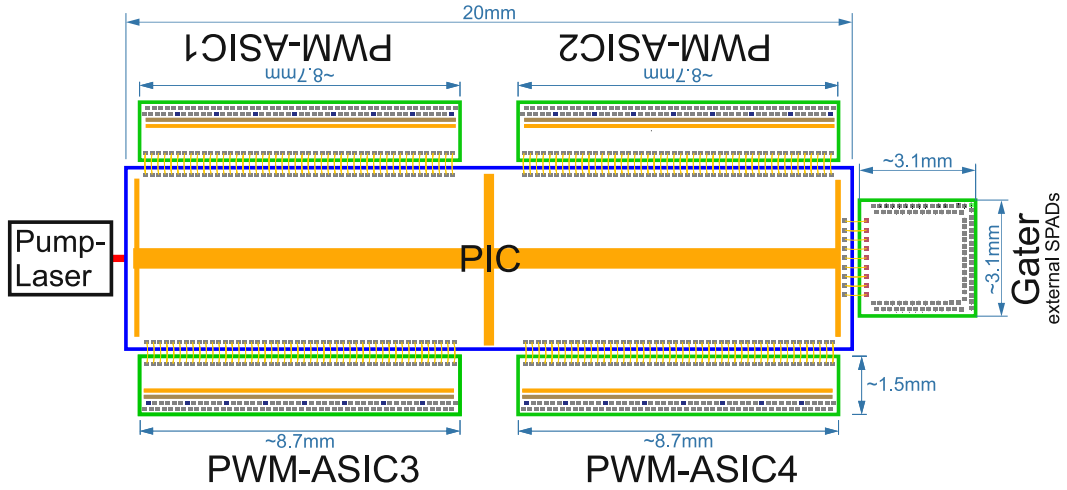


Figure 3: Overview of components of the quantum simulator with the Gater for external SPADs on the PIC (wire bonded).

The Gater with integrated SPADs, called internal Gater, is connected via fibres to the PIC. A schematic overview of this configuration is shown in Figure 2. Due to the fact that the laser and the internal Gater is only connected via fibres, they could be placed a bit further away from the PIC. The Gater for external SPADs, called external Gater, controls SPADs integrated into the PIC. This configuration is pictured in Figure 3. The PIC has an area of 20 x 5 mm^2. One single big ASIC would be possible but would lead to too long metal traces and very high production costs.

In the second production run all chips are redesigned and only the Gater for external SPADs (integrated into the PIC) is used. All chips are designed for 3D integration. The mixed-signal circuits are again split into five ASICs, because the needed size of the chip would exceed the budget of the project. The enlarged PIC area of 10 x 20 mm hosts all the five ASICs in a similar locataion as in the wire bonding variants. A schematic overview of the flip-chip configuration is shown in Figure 4.

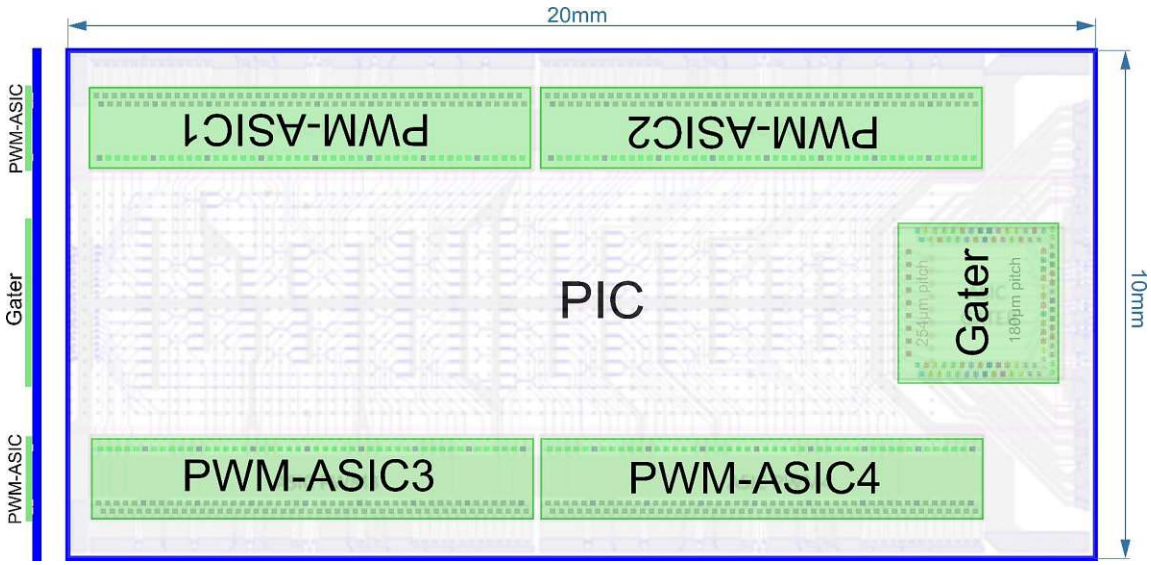


Figure 4: Overview of the quantum simulator with the PIC and five ASICs (left: side view; right: top view).

1.2 ASIC Technology and Design Tools

In this work, all application-specific integrated circuits (ASICs) are designed, laid out, and simulated with Cadance Virtuoso Studio. Cadence Virtuoso is a widespread design environment for custom analog, mixed signal, and photonics development. It is an integrated suite of tools for schematic, layout design, and different simulators, enabling to model and optimise circuit behaviour. All pre- and post-layout simulations used to verify and design the chips in this work are performed with the high-performance simulators “APS” and “Spectre X” in the ADE Assembler. As compute platform Red Hat Enterprise Linux on a x86_64 based 96 core server with 3 TB RAM was used. The design workflow used for the analog parts of the mixed signal design is shown in Figure 5 and derived from the analog IC design flow presented in [11] and [12].

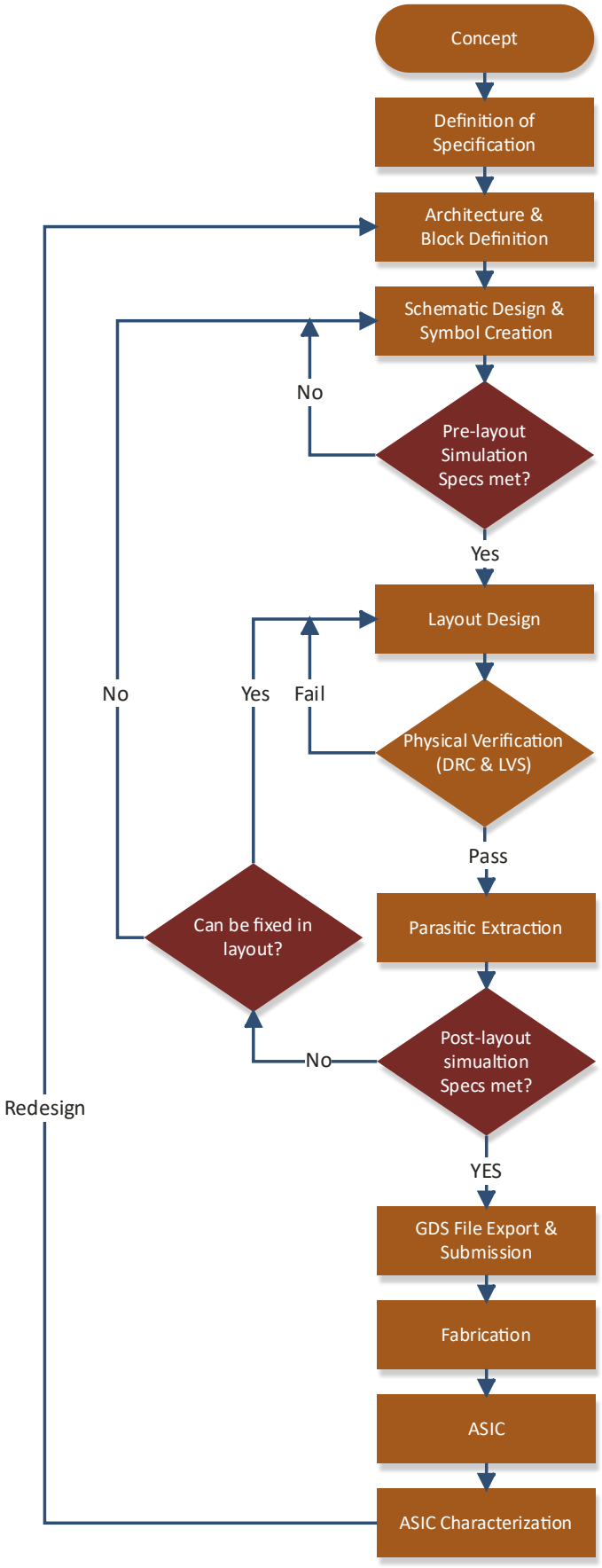


Figure 5: Analog chip design flow.

It is an iterative process; starting with the concept in mind, the specifications are defined, and the architecture and blocks are identified. The blocks represent, for example, function units like an output driver or a shift register. In the next step, a loop with schematic designs and pre-layout simulations is performed, until the requirements are met. After this step, the layout is designed and verified. Verification includes layout versus schematic check (LVS) and design rule check (DRC).

In the LVS the extracted netlist from the layout is compared to the source schematic netlist to determine if they match. The DRC ensures that the physical layout adheres to a set of rules from the foundry. If there is a mismatch in the LVS or a rule violation a redesign of the layout, in some cases also of the schematic, is necessary. The result of the post-layout simulation determines if changes to the schematic are necessary, and a new iteration starts. After all requirements are met a layout of all chips for the tape-out is combined to a layout of the full 11 x 9 mm^2 reticle.

The process used is the XH018 process from X-FAB. It is a 0.18 µm high-voltage CMOS technology that is engineered for robust analog and mixed-signal integrated circuit designs. It enables the integration of high-voltage, optical, analog and digital parts. [13] A simplified cross-section of important layers of the process is shown in Figure 6.

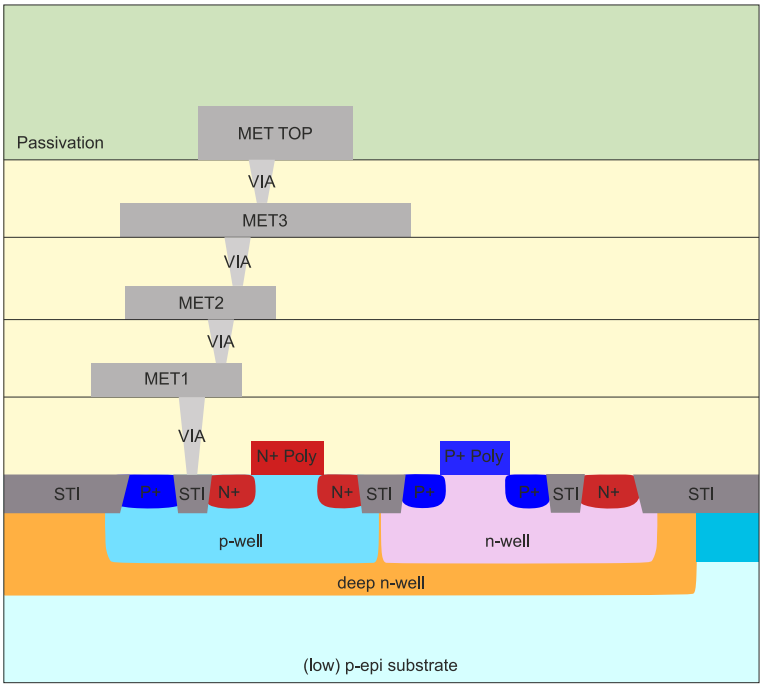


Figure 6: Wafer cross-section. Source: [14]

The process includes 1.8 V and 3.3 V MOSFETs, a UV window, isolating deep n-wells and double metal-insulator-metal (MIM) capacitors. A deep n-well is a heavily doped, deep n-type semiconductor region that sits beneath the normal n-well and p-well region. It isolates the devices from the substrate by creating a reverse-biased junction with the substrate, which reduces noise coupling through the substrate and allows different voltage domains. To keep all PN junctions at a PMOS reverse biased, the deep n-wells must be at least equal to or higher than the highest PMOS source, drain, and substrate voltage. The bulk of the PMOS and the corresponding deep n-well have the same bias voltage because both are n-type regions, and no PN junction is formed. To keep all PN junctions reverse biased at a NMOS, the deep n-wells must be at least equal to or higher than the bulk (p-well) and substrate voltage. The bulk of an NMOS (p-well) and the corresponding deep n-well can therefore have different voltage levels.

Three standard metal layers (MET1, MET2, MET3) and a thicker top metal layer (METMID) were selected. Two full production runs with multiple wafers were conducted. In the second run, the LVT module was additionally added to get MOSFETs with a lower threshold voltage. The HVMOS module, which adds high voltage transistors and was only used for alignment necessary for the process modifications in the first run, was removed in the second run to reduce production costs. The HVMOS transistors were too slow for the designs and were not used. In the first run 31 and in the second run 30 mask layers were necessary. The modules and further details of the two production runs are listed in Table 1.

Table 1: ASIC production run details.

Production run	Mask type	Mask layers	Produced wafers	Modules
Run 1	MLM 4	31	3 x standard 3 x low-epi	LPMOS, MET3, METMID, ISOMOS, ISOMOS2, HVMOS, DMIM, CATDOP, UVWINDOW, AVLA
Run 2	MLM 4	30	1 x standard 2 x low-epi	LPMOS, MET3, METMID, ISOMOS, ISOMOS2, LVT, DMIM, CATDOP, UVWINDOW, AVLA

For each of the runs, a multi-layer mask set (MLM) was used to cut costs. The used MLM 4 combines four different mask layers on one physical mask plate (reticle,

photomask), which is the maximum possible number of layers per reticle supported by the process. The higher the MLM number, the more layers are shared per reticle, leading to reduce mask costs but increases the production cost per wafer caused by a more complexity. For the research project done in this thesis, the cost per wafer does not really matter because only 6 in the first und and 3 wafers in the second run are produced. Some small process modifications were made. A wafer split with low-epitaxial substrate wafers was introduced to allow a ticker active region and, therefore, better integrated photodiodes and integrated PIN photodiode. In these devices, the intrinsic (i) region, which is responsible for absorbing photons and generating electron-hole pairs, is formed from a lightly doped (or nearly intrinsic) epitaxial layer. This low doping is critical for creating a wide depletion region to improve quantum efficiency and minimise capacitance, thus improving and reducing noise. [15] All chips that require integrated photodiodes are picked from a low-epi wafer. The PWM ASICs are picket from standard wafer because the required larger isolation spacings would increase the chip area if the same low-doped epitaxial layer was present in the PWM ASIs. The solution to this issue is a wafer split with low-epi wafers for the Gater ASIC with integrated SPADs and standard wafers for the other ASICs. To keep the ASIC costs low, the process steps and the masks are identical for both wafer types. In fact, the Gater ASIC without integrated SPADs (external Gater) uses the low-doped epi wafers as well, although with an optimised design (with respect to a smaller chip area) the standard wafers could have been used. Due to a lack of time, this optimised design was not carried out.

1.3 Single-Photon Avalanche Diodes

Single-photon avalanche diode (SPADs) are highly sensitive photodetectors that can operate in the Geiger mode, where they can detect single photons with high temporal precision. Unlike other photodiodes, which rely on the linear response of a current proportional to the incident light intensity, SPADs utilise avalanche multiplication to amplify the signal generated by the absorption of a single photon. This process involves a reverse bias voltage that is higher than the diode breakdown voltage, resulting in a self-sustaining avalanche current after a photon

is detected. [16], [17] The direct photocurrent of a single photon would be too low to be detected by connected electronics.

The key advantage of SPADs lies in their extraordinary sensitivity and temporal resolution, which make them indispensable in applications requiring the detection of extremely low light levels and precise timing. These applications range from quantum cryptography and fluorescence lifetime imaging to LIDAR systems and optical communication. The ability of SPADs to detect single photons makes them crucial for advancements in fields such as quantum computing and biological imaging, where traditional photodetectors fall short. Overall, SPADs represent a significant technological advancement in photodetection, offering high performance in terms of sensitivity and can be integrated into photonic integrated circuits. SPADs are therefore highly suitable as detectors in integrated quantum simulators.

To operate the SPAD in the Geiger mode and to detect single photons, the SPAD must be biased with a reverse voltage.

$$v_{SPAD} = v_{BD} + v_{exess} \quad (1)$$

above its breakdown voltage v_{BD}. The difference between the breakdown voltage and the bias voltage on the SPAD is called excess bias voltage v_{exess}. This results in a high electric field across the PN junction. Figure 7 shows the basic operating principle in Geiger mode. In the first step, the SPAD is charged to $v_{BD} + v_{exess}$ as shown. The SPAD cathode is then connected to the rest of the circuit through a high-impedance connection. If a photon hits the detector, it can generate an electron-hole pair. These carriers are then accelerated by the electric field applied across the junction, gaining enough energy to overcome the energy gap of the material. This process, known as impact ionisation, can generate additional electron-hole pairs. Accelerated carriers may trigger further ionisations, leading to a cascading effect known as self-sustaining avalanche or carrier multiplication. The current rises and the resulting voltage drop from discharging can be detected and counted as a photon hit. The current flows until the voltage across the SPAD drops below the breakdown Voltage v_{BD}. This voltage reduction can be done passively with a quenching resistor or with an active quenching circuit. The SPAD is then in the off state and cannot detect a photon. To be again sensitive to photons the SPAD is again biased to $v_{BD} + v_{exess}$ and the process starts again. [18]

It should be mentioned that not all photons hitting the SPAD cause a self-sustaining avalanche and therefore cannot be detected. The photon can be reflected on the detectors surface, absorbed outside the detector, or transmitted through the martial (depending on the wavelength) and therefore no electron-hole pair is generated. If the photon is absorbed outside the depletion region (space charge region), it is possible that the generated electron-hole pair recombines on the surface before reaching the depletion zone. Even if a photon generates an electron-hole pair in the active region, the carriers must gain enough energy from the electric field to initiate an avalanche. Carriers may lose energy through scattering before reaching the threshold for impact ionisation, or material defects can trap carriers. This leads to a photon detection probability (PDP) lower than 100 %. [19], [20] This key parameter is discussed in Chapter 1.3.1. In contrast to this, it is also possible that an avalanche is triggered without the presence of light. This is described in Chapter 1.3.2.

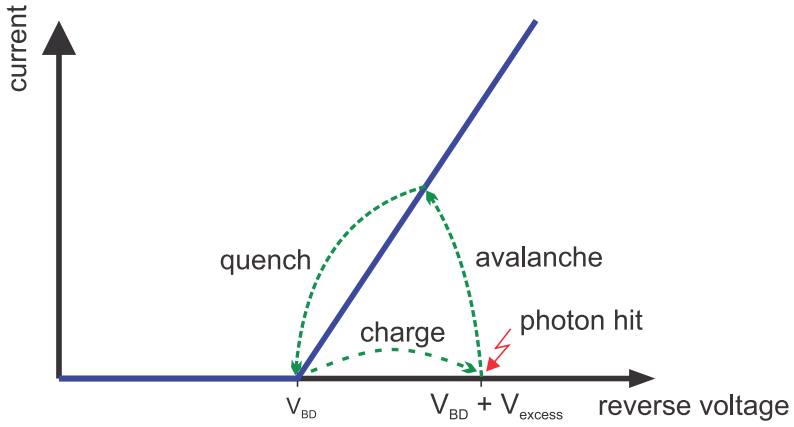


Figure 7: Geiger mode operation of a SPAD. [18]

1.3.1 Photon Detection Probability and Photon Detection Efficiency

One of the most important parameters of an SPAD is the photon detection probability (PDP) and the photon detection efficiency. These two parameters are very similar and are not always clearly defined and distinguished depending on the literature. Often the photon detection efficiency includes not only the probability of the SPAD to detect a photon, but also additional factors which are system dependent. Both parameters state the probability that an incoming photon is detected. The photon detection probability

$$PDP(\lambda) = \int_0^{\infty} P_{ab}(\lambda, x) * P_{av}(x)\, dx \qquad 2$$

can be calculated from the absorption probability $P_{ab}(\lambda,x)$ and the total avalanche-triggering probability $P_{av}(x)$. [18], [21] For measurement it is defined by the ratio of detected N_d photons to incoming photons $N_p(\lambda)$.

$$PDP(\lambda) = \frac{N_d}{N_p(\lambda)} \qquad 3$$

The PDP is always < 1 and depends on the wavelength of the incoming light. [18], [22] To increase the PDP reflections can be reduced by using an antireflection coating, increasing the excess bias, or matching the active area to the penetration depth of the photons.

1.3.2 Dark Count Rate and Afterpulsing Probability

If an avalanche discharge is triggered and detected even though no photon has hit the detector, it is called a dark count. This phenomenon can be caused by either thermally generated electrons or holes or by charge carriers that tunnel through potential barriers (band-to-band tunnelling and trap-assist tunnelling). Dark counts can also be caused by afterpulsing from trapped charges. The SPAD can therefore trigger a false photon count in the dark with no photons present. [18] The counts N_{dark_counts} divided by the measurement time $T_{measurement}$ when no photons are present, results in the dark count rate

$$DCR = \frac{N_{dark\_counts}}{T_{measurment}} \qquad 4$$

The DCR is another important parameter of an SPAD and should be as low as possible. Higher reverse current (from defects, impurities, high temperatures, higher bias voltage, or larger active area) increases the likelihood of thermal carriers initiating avalanches. The dark count rate is approximately proportional to the reverse current (leakage current). [23] Therefore, the DCR vary significantly with temperature, bias voltage, structure, and defects (traps). A higher temperature increases the dark counts because of a higher thermal energy, which raises the likelihood of thermal events (electrons or holes generation). A higher bias voltage resulting in a higher electric field within the SPAD can induce direct (band-to-band) or indirect (trap-assisted) tunnelling of charge carriers across the energy bandgap, contributing to additional dark counts. Larger active areas collect

more thermal and tunnelling carriers, increasing the DCR. More defects and impurities, from manufacturing, radiation, or ageing also increase thermal generation and the trap-assisted tunnelling. A material with a narrower bandgap (like InGaAs) has a higher band-to-band tunnelling, which results in a higher leakage current and consequently an increased DCR.

During an avalanche, the PN junction becomes flooded with charges. Defects (traps) in the semiconductor might store some of these charges, which are released after some time and can cause another avalanche event. [24], [25] This phenomenon is called afterpulsing as mentioned above. The afterpulsing probability (APP) is another important parameter of a SPAD and should also be as low as possible. Although afterpulses are not technically equivalent to dark counts, defects that extend carrier capture times can indirectly increase the measured DCR.

Although some factors that increase DCR can be controlled externally (e.g., temperature), others (e.g., material defects) require optimisation during manufacturing of different materials. Reducing the reverse bias voltage (lower excess voltage) decreases the DCR but also generally decreases the photon detection probability. One common method to reduce DCR is cooling the SPAD to reducing thermal generation, which is a trade-off because with the APP. In contrast to the DCR, the APP increases at lower temperatures as the traps typically have a longer lifetime at lower temperatures. [26], [27], [28] Depending on the type of quenching circuit, the deadtime can be artificially increased to reduce the APP and the DCR, because of the shorter active time window. The deadtime is the period followed immediately after an avalanche was trigger until a new photon can be theoretically detected. Therefore, longer deadtimes decrease the afterpulsing portability of a SPAD, but it also reduces the detection rate. [29].

The capacitance of an SPAD is also an important key figure, especially for gating circuits. To achieve fast voltage rise and fall times at the cathode and, therefore, short gating windows, the capacitance of the SPAD should be as low as possible. The total capacitance at the input node, including the parasitic capacitance from pads, metal lines, and transistors, determines primarily the rise and fall time of the output node of the circuit, because the input impedance of a real circuit (‘switch’) is not zero. In addition, a high capacitance leads to more reverse current (charges through the depletion region) in the case of an avalanche and increases

the afterpulsing probability by filling and then releasing traps. According to [30] the afterpulsing probability is directly proportional to the capacitance of the SPAD until trap saturation occurs. For a reverse-biased photodiode, the capacitance is predominantly determined by the depletion capacitance of the PN junction. Within the depletion region, the minority carrier density is very low and a strong electric field is present because of the charges from ionised impurity atoms. In contrast, the electric field outside the depletion region can be neglected. If a reverse bias voltage is applied, the electric field across the junction increases and pushes charge carriers away from the junction; the depletion region expands, and the capacitance decreases. This behaviour can be compared to that of a parallel plate capacitor. [15] The depletion region continues to expand with increasing reverse bias. This further reduces the capacitance as the effective 'distance' between the capacitive 'plates' (edges of the depletion region) increases until the intrinsic (i) region is fully depleted, and the depletion region cannot expand anymore. [31]

2. Photon Detection

The basic unit of quantum information is the qubit, analogous to a classical bit but capable of being in a superposition of two states [1]. As described in Chapter 1.1 qubits are in photonic quantum systems represented by photons where the state can be encoded by various physical photon properties. Each encoding scheme has unique challenges and advantages, depending on the application. Possible options are polarization, path, frequency-bin or time-bin encoding. [32], [33], [34], [35], [36] In the investigated quantum simulator, the qubits are path encoded, because it is robust against decoherence in short-distance setups and easy to integrate in a photonic chip. For example, if a photon takes path A, it represents $|0\rangle$, and if it takes path B, it represents $|1\rangle$. After the simulation process (where the photons are manipulated using beam splitters, phase shifters, and other optical components), the photons exit the manipulation stage through different paths. Single-photon detectors in the detection stage are necessary to detect which path each photon takes. The quantum simulator is clocked, and every cycle a photon or no photon is expected at each output. Since quantum systems are probabilistic, the simulator needs to run many cycles to build up statistics. By collecting photon counts from detectors over many trials, the probability distribution of the output states is estimated. This distribution represents the result of the simulation. There are various methods available for detecting individual photons. For a fully integrated quantum simulator hardware, also fully integrated detectors, like superconducting nanowire single-photon detectors (SNSPD or SSPD) or single-photon avalanche diodes (SPAD) are necessary. As the name suggests, SNSPDs must be superconductive and therefore require cryogenic cooling to operate. SPADs can be operated at room temperature and monolithically integrated in CMOS ASICs. For this reason, SPADs are used in this project, which are either integrated directly in the CMOS ASICs or in the PIC.

2.1 Types of Quenching Circuits

When an SPAD enters an avalanche breakdown state, caused by a dark count or a photon, a self-sustaining avalanche of charge carriers is triggered. This state

prevents the SPAD from detecting another photon because there is already an avalanche. To restore the SPAD to its ready state and prepare it for subsequent photon detection, a quenching circuit is required to stop the avalanche. The circuit lowers the voltage across the SPAD v_{SPAD} below its breakdown voltage v_{BD} to stop the avalanche ($v_{exess} \leq 0$). Quenching circuits play an important role in the operation of SPADs by stopping the avalanche and resetting the device, preventing damage to the SPAD, and reducing the afterpulsing. The selection of the quenching circuit affects the SPAD performance, including its timing resolution, deadtime, power consumption, and photon detection probability. There are several types of quenching circuits, each with its own advantages and disadvantages. The circuits can be roughly classified as active, passive, gated, or hybrid circuits. [16], [37]

2.1.1 Passive Quenching Circuit

Passive quenching circuits are an easy way to quench an avalanche. A resistor in series with the SPAD is the simplest form of a passive quenching circuit, shown in Figure 8 on the left side. The circuit model of the SPAD, shown in Figure 7 on the right side, is simplified and describes the basic behaviour of the SPAD. In reality, the internal avalanche resistance R_s and the SPAD capacitance C_s are not constant over bias voltages. Therefore, a piecewise linear resistor and capacitor can be used get to a much better model. [38], [39]

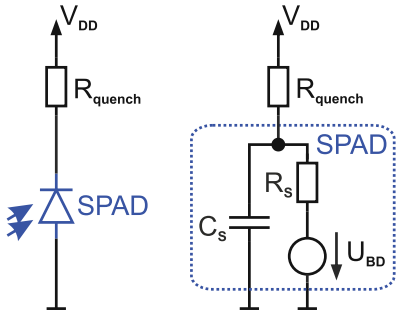


Figure 8: Simple passive quenching circuit (left) simplified circuit model of the behaviour during avalanche (right).

When an avalanche occurs, the current flowing through the resistor causes a voltage drop, which gradually reduces the bias voltage of the SPAD below its breakdown voltage, thus quenching the avalanche. The external resistor is typical in the range of 10 k to 2.5 MΩ. [40] The advantage, that the circuit is very simple

comes of the cost that the deatimes are relatively long and the whole current through the SPAD also increase the afterpulsing probability.

2.1.2 Active Quenching Circuit

Another way to quench SPADs is to use a dedicated circuitry which actively monitors the voltage across the SPAD and, therefore, can detect and quench an avalanche. The first active quenching circuit was reported in [41]. The principal function of an active quenching circuit (AQC) is shown in Figure 9. Upon detection, the circuit actively reduces the voltage below the SPAD breakdown threshold v_{BD}, rapidly stopping the avalanche. The detection (sensing) and the following automatic quenching require a closed-loop circuit, which adds some delay. The duration of quenching T_{quench}

$$T_{quench} = T_{loop} + T_{ft\_quench} \quad (5)$$

results from the addition of this loop delay T_{loop} and the fall time of the SPAD node T_{ft_quench} and is constant for a fixed excess bias. [16] The required time to detect and quench an avalanche significantly determines the current through the SPAD and affects the afterpulsing probability. A fast closed loop and short fall time is crucial to reduce the afterpulsing probability. [42] After a controlled time, which distinguishes the deadtime, the circuit restores the voltage above the breakdown voltage, recharging the SPAD for the next photon detection.

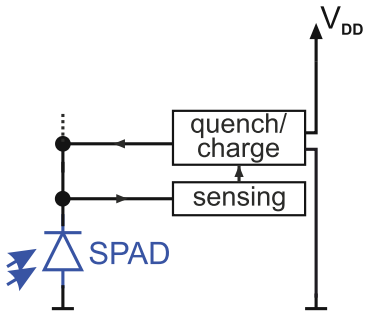


Figure 9: Principal concept of an active quenching circuit.

The shortest possible deadtime is therefore limited to the rise and fall times, the loop delay, and an intentional delay. The active reset is normally much faster compared to passive circuits with a quenching resistor, and the deadtime is also adjustable, constant, and well-known. On the downside, the design complexity, the power consumption, and the required chip area is increased.

2.1.3 Hybrid Quenching Circuit

Hybrid quenching circuits offer a further alternative by combing the benefits of passive and active quenching techniques to utilise the advantages of both approaches. The resulting circuits have mixed passive and active features to use the best combination for the specific applications. The transition to quenching and resetting (charging) does not necessarily have to be both passive and both active, and also a single transition can be partly passive or partly active. [16]

Figure 10 shows a basic concept that illustrates a possible configuration. In this type of quenching circuit, the SPAD is connected to both a high-impedance resistor to supply and an active quench and reset circuit. Hybrid quenching circuits can, in contrast to active quenching circuits, reduce the maximum avalanche charge if the avalanche current and the quenching time are relatively the same.

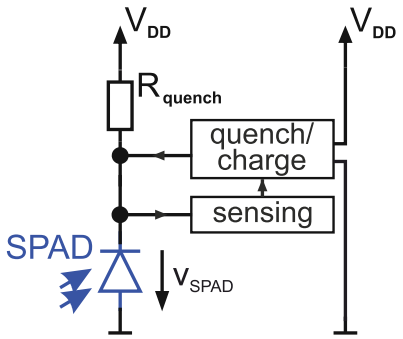


Figure 10: Principal concept of a simple hybrid quenching circuit.

2.1.4 Gated Quenching Circuit

Gated quenching circuits (Gater) enables the SPAD to detect photons only in a predetermined time window. Gated quenching circuits achieve this by shifting the reverse voltage at the SPAD v_{SPAD} between a level below the breakdown voltage v_{BD} and a level above. The gating frequency defines the repetition rate of the gating window. The principal function of a gated quenching circuit is shown in Figure 11.

This gating allows the SPAD to be ready for photon detection only during the specified time windows. When a SPAD is gated, it is active within defined, typically periodic time slots during which it is activated and ready for photon detection until either a photon is detected or the active period ends. Compared to active quenching methods, this minimises the occurrence of dark counts and reduces

the likelihood of an afterpulse, a phenomenon typically triggered by prior photon absorptions or residual dark counts. [43], [44]

The main difference from an active quenching circuit is the absence of an active sensing circuit or other feedback to quench the SPAD. An active quenching feature could be added to reduce the current through the SPAD in the case of an avalanche. In addition to the advantage that a detection is only possible if desired, a Gater can also achieve very short gating windows and quench faster than an AQC, if the windows are very short. Depending on the technology, it takes a relatively long time to detect the voltage drop and quench the SPAD. Gaters are ideal for quantum simulator because the arrival time of possible expected photons is well known, and the gating windows need to be very short. [45], [46], [47] Therefore, a gated quenching circuit is used in this work.

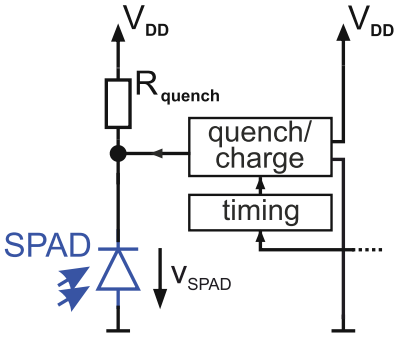


Figure 11: Principal concept of a simple gated quenching circuit.

Table 2 gives a rudimentary comparison of some properties of passive, active, gated, and hybrid quenching circuits.

Table 2: Comparison of Quenching Circuits

Quenching circuit	Deadtime	Complexity	Power consumption	Chip area
Passive	High	Low	Low	Low
Active	Low	High	Moderate to High	High
Gated	Adjustable	High	Moderate	High
Hybrid	Moderate	Moderate to High	Moderate	High

2.2 Multi-channel Gating ASIC wit Integrated SPADs

This Section is partly based on my work published in the peer reviewed paper [5] as well as (confidential) reports and internal documentations within the EPIQUS project that I have independently authored.

The detection stage described in Chapter 1 and shown in Figure 1 is realised as a dedicated ASIC with monolithically integrated SPADs (internal Gater), as shown in the configuration shown in Figure 3. Light from the waveguides on the PIC will be coupled via a fibre ribbon containing lensed fibres (127 µm pitch) into the integrated SPADs on the Gater ASIC. The end of the fibre ribbon is mounted close to the surface of the ASIC to couple almost all of the light from the fibre cores into the SPADs. Two PIN photodiodes are also integrated to facilitate the adjustment of the fibre ribbon. In a second version of the quantum simulator system, the detection stage is split into the SPADs on the photonic integrated chip and a gating ASIC with the electronic integrated circuit, which is described in Chapter 2.3. The COMOS process XH018 from X-FAB is used as described in Chapter 1.2.

As previously mentioned in Chapter 2.1.4 a gated quenching circuit is best for quantum simulations because of the known arrival time, the reduced dark count, and afterpulsing rate. Therefore, the SPAD is operated in gated mode by the CMOS circuitry in a way that it is only photosensitive during the gating window (t_{on}). During the rest of time, it absorbs photons, but no avalanche is triggered (T_{off}). This is achieved by operating the SPAD slightly below the breakdown voltage during T_{off}. The electrical field in the SPAD is in that operation condition not strong enough to allow a self-sustaining avalanche. During the gating window (T_{on}), the voltage is increased by the excess bias voltage over the breakdown voltage. In this phase, the SPAD is sensitive to photons. The topology of the quantum simulator required very short gating windows in the range of $T_{on} \approx 1$ ns and below. The loop delay (including level shifting) to detect and quench an avalanche is in the used XH018 CMOS process in the range of 0.5 ns, which would be too long to achieve active time windows shorter than the required 1 ns with an AQC.

A high photon detection probability is also crucial in quantum simulators because the rate of valid calculations scales exponentially with the number of qubits (photons), effectively the rate depends on the PDP to the power of the number of qubits (supplementary information in [48]). The photon detection probability is

known to increase as the excess bias voltage is increased. [49], [50] Consequently, the quantum simulator requires a high excess bias voltage. A low APP is also crucial for quantum simulators. The APP is directly proportional to the capacitance of the SPAD; in fact, it scales with the total capacitance at the output node of the Gater, including the intrinsic capacitance of the SPAD. Integrating the SPADs directly on the gating ASIC significantly reduces the node capacitance because bond pads and metals traces are eliminated. Also, the inductance resulting from the bond wire and the much longer metal tracks is drastically reduced.

To achieve short gating windows, fast switching transistors are needed, which support a small structure size technology. Meeting the requirement of a high excess bias and fast switching calls for an advanced circuit topology, such as cascoding. [51] The cascoding concept used for the switch is derived from the previous designed circuit presented in [52] in a 0.35 µm process in my institute. In this thesis, I designed and characterised a nine-channel gating chip with integrated SPADs. The design leverages the very fast 1.8 V MOSFETS in the 0.18 µm CMOS process to achieve fast rise and fall times with a double cascoding architecture. To the best of my knowledge, this represents the first implementation of a double cascoded configuration in an SPAD gating circuit, delivering a maximum excess bias voltage v_{exess} of 9.9 V. To simplify matters, the multi-channel gating ASIC with integrated SPADs is called internal Gater. In contrast, the ASIC presented in Chapter 2.3 with external SPADs is called external Gater.

2.2.1 Integrated SPADs

The SPAD used to integrate into the Gater ASIC was designed by a colleague at my institute. Figure 12 presents the cross-sectional view of the integrated SPAD using the 0.18 µm X-FAB process. The tick low-doped epitaxial layer enables a high quantum efficiency for red and near-infrared light. With a wavelength of about 850 nm the quantum simulator in the EPIQUS project operates in the near-infrared wavelength. The device features a thin n^+ region and a customised p-well avalanche region (AVA), both on a p-type doped epitaxial layer with a thickness of approximately 24 µm and a doping concentration near 1.3×10^{13} cm^{-3}. This thick epitaxial layer should help to achieve low capacitance (i.e., reducing APP) and a high photon detection probability (PDP) for red and near-infrared light. [5]

The specialised avalanche layer (AVA) was developed in collaboration with X-FAB. Simulations showed the ideal p-well doping profile for the avalanche region, and X-FAB subsequently simulated several process refinements to achieve the desired profile. The standard XH018 avalanche layer does not meet the requirements. The diameter of the p-well is 50 µm, which is intentionally smaller than the 55 µm diameter of the n^+ cathode to prevent early edge breakdown. An STI with a width of 10.1 µm separates the n+ cathode and the p+ anode ring. A UV window is incorporated to reduce optical interference from the isolation and passivation stack. This design incorporates a thick absorption region. When the SPAD is reverse biased beyond its breakdown voltage, a strong electric field forms at the n^+–p-well junction, establishing an avalanche multiplication region. Concurrently, a comparatively lower electric field extends from beneath the PN junction through the p-well and the epitaxial (p-type) layer, reaching the substrate, which serves as the photon absorption region. Electrons photogenerated within this thick absorption layer drift toward the multiplication region, where they experience impact ionisation. This process significantly enhances carrier multiplication, resulting in a high PDP. [5]

The SPADs integrated into this ASIC do not incorporate an antireflection coating, resulting in interference effects within the oxide layers. Consequently, these interference phenomena induce a wavelength dependence in the PDP, as discussed in [53]. The simulations predict a PDP of ~69% at 840 nm and ~72 % at 635 nm. It should be noted that the thickness of the UV window is not tightly controlled, leading to variations in the positions of the PDP maxima and minima due to thickness tolerances between individual chips and across different wafers.

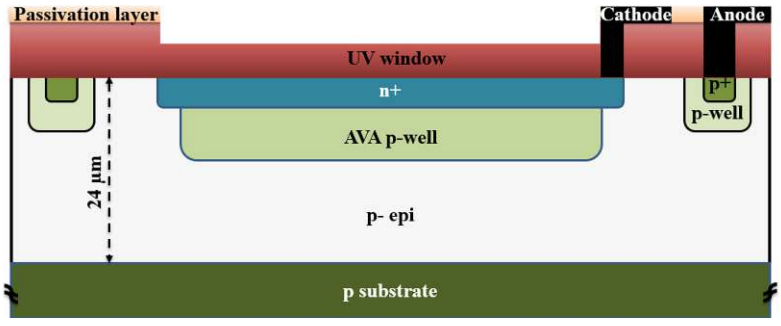


Figure 12: Schematic cross-sectional view of the CMOS SPAD structure, illustrating the n $^+$-avalanche-p-well junction regions (not to scale). Source: [5]

Silvaco Atlas simulations (further information [54]) predict a breakdown voltage of 34.4 V and a SPAD capacitance of 20 fF. The electric field along a vertical cut line

in the centre of the SPAD with the desired 10 V excess bias is pictured in Figure 13. The data are obtained from Geiger mode device simulations using Atlas. [5] The multiplication region is clearly visible at the n+/AVA p-well junction. The figure indicates that the 24 µm tick absorption zone is fully depleted. The large electric field strength between 3 µm and 19 µm (thick absorption zone/epitaxial layer) of more than 5 x 10^3 V/cm ensures a high drift velocity in the thick absorption zone. The resulting electron drift velocity of more than 4 x 10^6 leads to a collection of the charge carrier within 0.5 ns. This fact makes the control with gating windows in the range of 1 ns feasible, as the device is fast enough. [5] In the first production run, also an Gater with integrated SPADs with a diameter of 20 µm (AVA p-well) was produced as a backup but was not characterised.

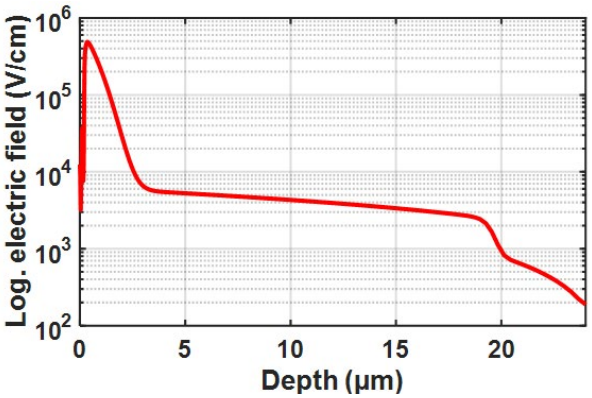


Figure 13: A vertical cross-sectional profile of the electric field through the centre of the SPAD at an excess bias voltage of 10 V. source: [5]

2.2.2 Circuit and Chip Design

Chip overview

Figure 14 presents a simplified block diagram with integrated SPADs. The proposed system comprises a timing section (shown in violet) and nine individual channels (shown in orange). Each channel incorporates a double cascoded Gater switch (yellow), a sample-and-hold stage (red), a sensitive comparator (green), and multiple digital output drivers in series (blue). The circuit is implemented in the described high-voltage 0.18 µm CMOS technology using both 1.8 V and 3.3 V MOSFETs. The 3.3 V transistors enable a 9.9 V voltage swing at the SPAD cathodes, whereas the faster 1.8 V transistors are employed to optimise timing performance and minimise power consumption. Additionally, the driver Section in each channel is subdivided into multiple smaller drivers to distribute the signal across the chip via metal tracks totalling approximately 5 mm in length per

channel. An output driver is placed directly adjacent to each corresponding digital output pad. [5]

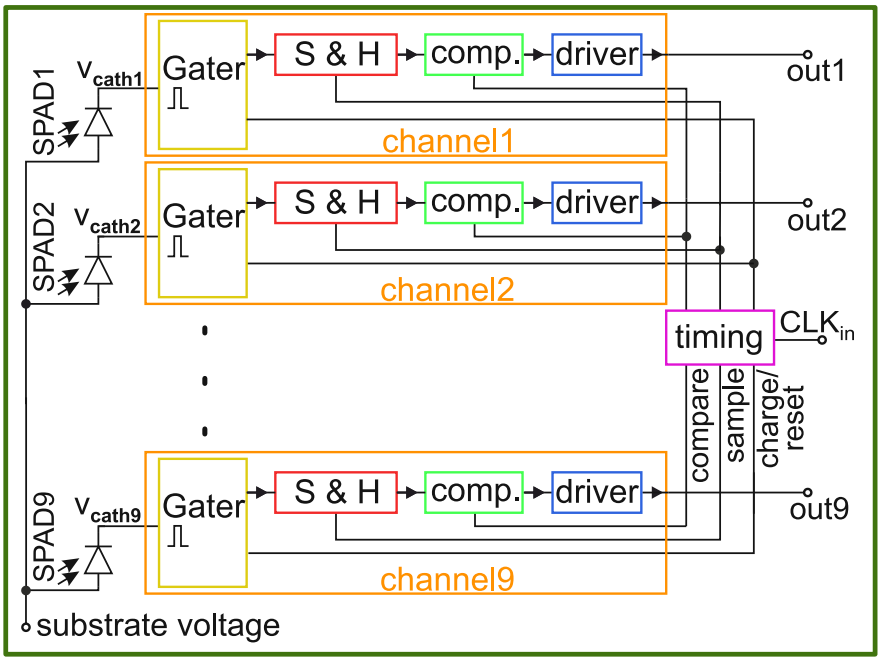


Figure 14: Block diagram of the Gater ASIC with integrated SPADs. Source: [5] modified

The timing signals for all channels are generated within a centralised timing module (shown in violet) and propagated to individual channels through matched delay lines, ensuring synchronisation across distances of up to 1 mm. Each channel incorporates a dedicated bias voltage input for the comparator reference voltage, enabling compensation for process-induced mismatches and temperature-dependent variations. To optimise performance of the sample-and-hold stages, an external adjustable bias voltage is used, which is shared across all channels, minimising the required number of bond wires in the system architecture. The charging duration of the SPADs and of the gating window are independently tuneable via two global bias voltages. Variable delay elements within the timing module are regulated by these voltages, allowing simultaneous adjustment across all channels. By reducing the excess bias voltage (v_{exess} < 9.9 V), the gating window can be shortened, offering the possibility of gating windows shorter than with full swing. This dual bias configuration ensures global control over timing parameters while maintaining channel-specific compensation for local variations. [5] The loop delay of the technology is too large, to employ an automatic adaptive charging control and reach the desired short gating windows.

High-voltage cascode switch

To drive the SPAD in the Geiger it must be biased with a reverse voltage v_{SPAD} alternating between slightly below the breakdown voltage v_{BD} and the breakdown voltage increased by the excess bias voltage $v_{BD} + v_{exess}$. The desired excess bias is required to be v_{BD} = 9.9 V to obtain a high PDP. While a high excess bias benefits SPAD operation, it also increases the dark count rate and afterpulsing probability. To mitigate these parasitic effects, the SPADs must be active only for a very short time. Given that the quantum simulator laser pulse rate is approximately 80 MHz the clock period is about 12.5 ns. As a consequence, the gating window was required to be in the range of 1 ns and shorter. This requirement poses a significant challenge for the gating circuit, which must achieve a slew rate well above 1 GV/s for a voltage swing of approximately 9.9 V. Extensive circuit simulations have demonstrated that the high-voltage MOSFETs and DMOS transistors available in the XH018 technology are not suitable for this task. These transistors could directly withstand 9.9 V, but the slew rate is much too slow, furthermore they need a relatively high Gate voltage (e.g. 6.6 V), which requires a similarly complicated circuit as if the 9.9V were switched directly. Instead, the optimal solution to achieve a voltage swing near 10 V is to employ the standard 3.3 V I/O transistors in a double cascoded topology. Six MOSFETs are stacked to get a push/pull configuration and enable very high slew rates. The developed gating switch including an adaptive biasing circuit, designed for a maximum swing of 9.9 V, is illustrated in Figure 15. [5]

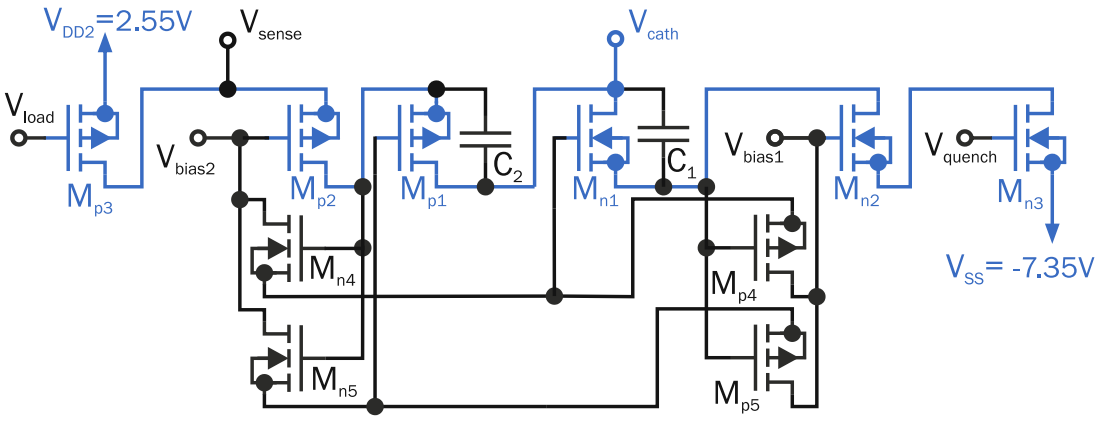


Figure 15: High-voltage double cascoded switch with dual adaptive bias shift. Source: [5]

This circuit consists of a high voltage double cascoded switch with a dual adaptive bias circuit. The design modifies the active quencher architecture implemented in

a 0.35 µm CMOS process reported in [52]. It was necessary to extend the single adaptive gate biasing scheme implemented in [52] to two separate adaptive bias circuits with M_{n4} and M_{p4} for M_{n1} as well as M_{n5} and M_{p5} for M_{p1} to keep the voltages also during the transition phases in their specified voltage limits. With a single adaptive bias circuit, the MOSFETs voltage limits cannot be kept for some operation phases. The SPAD's cathode is connected to V_{cath}. V_{DD2} is 2.55 V and V_{SS} is -7.35 V, resulting in a voltage swing of 9.9 V, which is the maximum possible excess bias voltage v_{exess}. The blue transistors in Figure 15 represent the primary switching path. The SPAD anode is connected to the ASIC substrate, which is a very negative voltage

$$v_{anode} = -(v_{BD} + 7.35V) \quad (6)$$

if the full access voltage should be obtained. The bulks of the transistors M_{n1} – M_{n2} and M_{p1} – M_{p3} are connected to their corresponding sources. Either the three NMOS transistors M_{n1} – M_{n3} are on (then V_{cath} is at V_{SS} and the SPAD is off) or the three PMOS transistors are on (then V_{cath} is at V_{DD2} and the SPAD is active; the gate window is on). Consequently, either the three stacked PMOS transistors (M_{p1} – M_{p3}) must withstand 9.9 V during quenching, while the three stacked NMOS transistors (M_{n1} – M_{n3}) are required to withstand 9.9 V when the SPAD is charged and awaiting photon arrival. Three transistors per side are necessary because each individual transistor is rated for a nominal voltage of 3.3 V and an absolute maximum voltage of 3.6 V. Reserve to the absolute maximum voltage is necessary during the shifts in the transition process and can only be applied for very short time slots. The SPAD cathode, connected to V_{cath}, can be switched between –7.35 V and 2.55 V. All transistors are isolated from the substrate using deep n-wells. To conserve space, the NMOS transistors M_{n1} – M_{n3}, as well as M_{n4} - M_{n5}, share the same deep n-well. Due to the high voltage differential between the isolating deep n-wells and the substrate, the corners of the deep n-wells are rounded, which is described in the layout section of this chapter. Similarly, the corners of the p-wells for transistors M_{n1}, M_{n2}, M_{n3}, M_{n4}, and M_{n5} are also rounded to reliably handle voltages exceeding the maximal allowed 8 V between the p-wells and the deep n-wells.

When quenching is initiated ($V_{quench} \approx V_{bias1}$) and charging is turned off ($V_{charge} \approx V_{DD2}$), the NMOS M_{n3} turns on while the PMOS M_{p3} turns off. Consequently, the drain of M_{n3} discharges to –7.35 V, and the drain of M_{p3} drops

to V_{bias2} + V_{th} (threshold voltage). Additionally, transistor M_{n2} switches on and M_{p2} is turned off due to their fixed gate bias voltages (M_{p2} at V_{bias2} = –0.75 V and M_{n2} at –4.05 V). This discharges the drain of M_{n2} to V_{ss} = –7.35 V. As a result, M_{p4} and M_{p5} are switched on and the gate voltage of M_{n1} is shifted to V_{bias1} = -4.05 V. The following shift at the gate of M_{n1} causes the transistor to turn on and discharges its drain as well as V_{cath} to V_{ss} (–7.35 V). M_{p1} is switched off due to of the downshift at its gate, caused by M_{n5} and M_{p5}. [5]

The adaptive bias circuitry, comprising M_{n4}, M_{n5}, M_{p4}, and M_{p5}, is critical to maintaining the voltages at M_{n1} and M_{p1} within the process limits. To ensure that the potential difference across M_{p1} and M_{n1} remains within the absolute maximum ratings during rapid switching, two distinct adaptive bias voltages are employed, with slightly different temporal behaviours. This behaviour is achieved by using different sized transistors for the individual paths. One bias circuit consists of M_{p5} and Mn5 and the other of M_{p4} and M_{n4}. The use of the dual adaptive bias circuit is not sufficient to fully comply with voltage limits under all operating conditions. Metal trace and Via resistance with DMIM capacitors C_1 and C_2 act as a snubber [55] and supress static and peak voltage violations, even during very short gating windows (< 1 ns). Without this snubber networks voltage peaks exceeding 5 V depending on the operating conditions would occur on different single transistors in the switching path (blue), which would destroy the transistors after some time. [5]

Sample & hold and comparator

To detect a voltage drop at the cathode and, therefore, an avalanche, a sensitive comparator is necessary. Due to the possible short windows, a direct connected comparator is not suitable because the voltage would be applied too briefly to make a sensible decision. A transmission gate is used to sample and store the voltage to make a sensitive decision with the comparator afterwords. Figure 16 shows this high-speed comparator with the sample & hold stage with V_{DD} at 1.8 V and V_{DD2} at 2.5 V. [5]

The voltage at V_{cath} is indirectly sensed at the end of the gating window at the source of M_{p2} at the switch, with the source follower M_{n1} and the transmission gate (M_{p1} and M_{n3}). The voltage is stored at the capacitance C_1, consisting of a dedicated dual metal-oxide-metal capacitor, the parasitic capacitance of the corresponding MOSFETS, and metal tracs. The input of the comparator is the gate

of M_{n4}. The voltage V_{sense} is in the range of V_{bias1} (-0.75 V) and V_{DD2} (2.55 V), which is a 3.3 V swing. The source follower with a current source load (M_{n1}, M_{n2}) shifts the signal into the 0 V - 1.8 V supply range of the transmission gate and the comparator. This downshift is necessary to use the 1.8 V XH018 standard transistors in all the following stages. Only MOSFET M_{n1} in Figure 16 is a 3.3 V transistor; the transistors in the following stages are 1.8 V MOSFETs to obtain the best possible timing performance and save energy. The "sample and hold ref." bias regulates the current through the source follower and externally adjusts the voltage to compensate for process, voltage, and temperature (PVT) variations. A single reference voltage is applied to all nine channels to minimise the required number of bonding pads. Additionally, the resistor R_5 and capacitor C_2 function as a low-pass filter, attenuating noise and distortion arising from long metal interconnects, which can reach lengths of up to 7 mm. When the window is open and the transmission gate conducts, the capacitance C_1 is charged to approximately V_{sense}. The transmission gate, composed of M_{n3} and M_{p1}, serves to isolate C_1 just before the SPAD is quenched, thereby storing the voltage V_{sense}. The stored voltage V_{samp} indicated if an avalanche was triggered, as it indicates whether V_{sense} and consequently V_{cath} were discharged due to an avalanche event. The timing signals "sample" and "sample inv." are centrally generated for all channels within the timing section to ensure simultaneous switching (see Figure 14). Due to the short time between sampling and quenching (< 100 ps range), the timing signals must be very accurate for all channels even over PVT variations. Post-layout corner simulations are used to ensure that the quenching is initiated after sampling. These signals are cross-coupled to ensure a synchronised transition of both transistors of the transmission gate, optimising switching behaviour. [5]

The stored voltage is applied to the NMOS M_{n4}, which is the input transistor of the clocked comparator. It is a modified version of the comparator in 65 nm CMOs presented in [56]. The circuit comprises a latch formed by transistors M_{p3}, M_{n9}, M_{p4}, and M_{n10}, complemented by two reset MOSFETs (M_{p2} and M_{p5}). The comparator has two input transistors M_{n4} and M_{n5}, a pair of cross-coupled MOSFETs (M_{n6} and M_{n7}), two tail transistors (M_{n8} and M_{n11}), and two output CMOS inverters, each including an ohmic feedback resistor (inverter one: M_{p6} and M_{n12}; inverter two: M_{p7} and Mn_{13}). Only the output from the second inverter (M_{p7}, M_{n13})

is used, while the first inverter (M_{p6}, M_{n12}) serves to maintain symmetrical loading at the latch output nodes (L_{out1}, L_{out2}). The resistive feedback incorporated into the CMOS inverters mitigates the slope of the transfer characteristic, thereby reducing the likelihood of multiple switching events in subsequent logic stages throughout the decision phase. During reset (compare = 0 V), the tail transistors M_{n8} and M_{n11} are turned off, and the transistors M_{p2} and M_{p5} reset the latch output nodes to V_{DD}. Subsequently, in the compare phase (compare = V_{DD} = 1.8 V), the reset transistors M_{p2} and M_{p5} are in the off state, while M_{n8} and M_{n11} are in the on state. This enables the input transistors to pull the following latch into the correct decision state. Additionally, transistors M_{n6} and M_{n7} remain activated from the reset phase, as their gates are biased at V_{DD}. These two transistors are used to significantly reduce energy consumption by preventing static current flow. The input transistors M_{n4} and M_{n5} discharge the latch nodes L_{out1} and L_{out2}. The gate voltages of M_{n4} and M_{n5} define the relative discharge rates of L_{out1} and L_{out2}, thereby indicating whether the reference voltage (compare ref.) or the sampled voltage (V_{samp}) is lower. Every channel has a sperate comparison reference voltage, which sets a specific threshold voltage for detection voltage drops from a potential avalanche and can therefore compensate for PVT variations. When the reference voltage exceeds the sampled voltage V_{samp}, which means that an avalanche occurred, node L_{out2} discharges more rapidly through M_{n10} and M_{n5}. Once L_{out2} reaches the voltage level of $V_{DD} - V_{th}$ (threshold voltage of M_{p3} and M_{p4}), the transistor M_{p3} activates, triggering a complete latch transition due to positive feedback, switching the output to L_{out1}. [5]

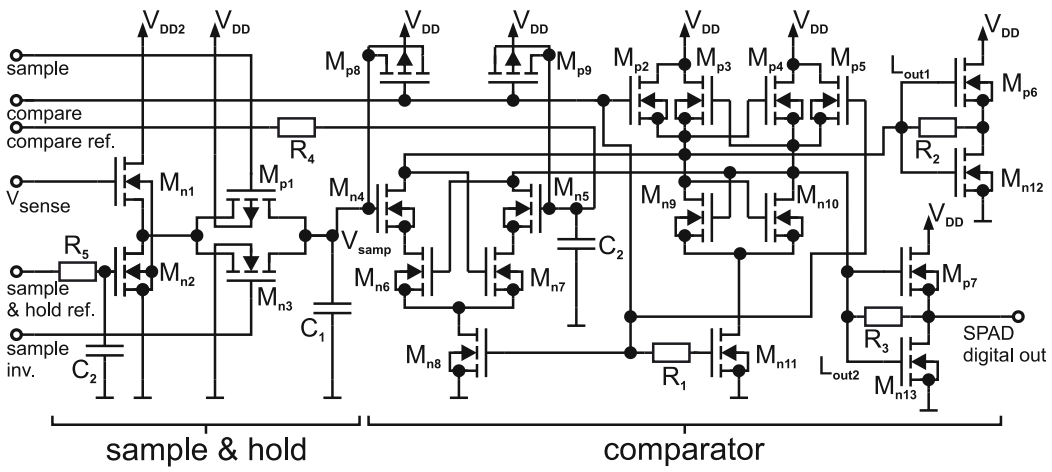


Figure 16: Sample & hold and Comparator stage including level shifting (M_{n1} is a 3.3V transistor; all other transistors are 1.8V transistors). Source: [5]

To enhance the sensitivity of the comparator, charges, caused by the transition from the rest to the comparison phase, are compensated with charge injections with M_{p8} and M_{p9}, which act as MOSCAPs. The reference voltage (compare ref.) is filtered and stabilised through resistor R_4 and capacitor C_2, which form a low-pass filter. This arrangement mitigates noise and distortion introduced by lengthy metal interconnections. The comparator clock (compare) is again centrally generated within the timing section for all channels, as illustrated in Figure 16. To enhance sensitivity by minimising distortions originating from quenching, the compare phase initiates approximately 1 ns after closure of the transmission gate. The negative edge of the clock input triggers the reset phase. This time gap between the rest and the new charging phase helps to keep interferences from switching off the digital output drivers away from the charging phase of the SPADs. Therefore, the duty cycle of the chip clock must be carefully chosen. Depending on how long the gating window is, a 50 % duty cycle of the clock is not feasible because the digital output pulse would be very short or not present at all. A duty cycle of, e.g. 85 % is reasonable to cover also longer windows. For the assumed gating period of 12.5 ns this would result in a 10.625 ns high (1.8 V) and 1.875 ns low (0 V) state of the input clock. It should be mentioned again that the duty cycle of the clock does not determine the duration of the gating window. The resistor R_1 introduces a very short delay between the gate activation of transistors M_{n11} and M_{n8} and the reset transistors M_{p2} and M_{p5}. This intentional delay arises from the interaction between resistor R_1 and the gate capacitance of M_{n11}, slightly postponing the discharge of nodes L_{out2} and L_{out1}. Consequently, this delay increases the initial voltage difference ΔU_0 at the latch nodes L_{out2} and L_{out1}, which causes the latch to regenerate. A larger ΔU_0 enhances the robustness of the latch against noise and device mismatches [56]. [5]

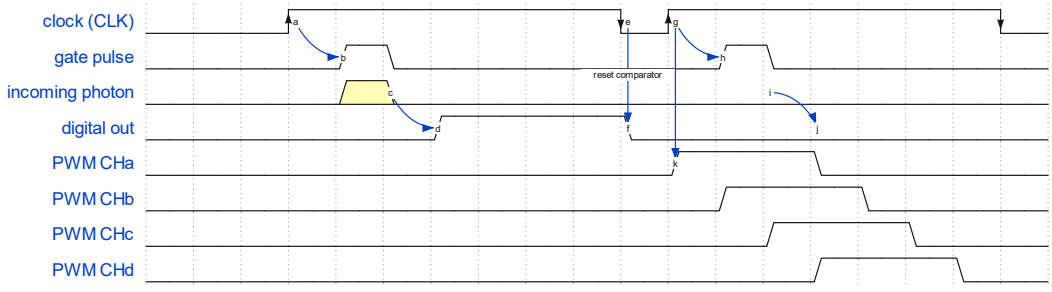


Figure 17: Schematic representation of the chronological sequence of the Gater ASIC and four PWM channels.

A schematic representation of the chronological sequence of the Gater is shown in Figure 17. The start of the gating window is triggered by the positive edge of the input clock of the chip. The delay between the positive edge of the input clock and the start of the gating window can be roughly estimated with 1.0 to 1.8 ns (process corners from 20 °C to 80 °C) and depends on PVT variation and does not include the rise/charge time. The calculated delay is according to post-layout simulations at the typical mean corner with 20 °C about 1.32 ns. The clock input must be shifted externally so that the gating window matches the laser pulse. If an avalanche is detected, the digital output driver switches on (marked 'd' in Figure 17) or stays low (marked 'j'). After powering on and all supply voltages are stable, it can take up to 20 ns until the first gating pulse is outputted. Therefore, the first photons can get loss after power up. Figure 17 also pictures the timing of four channels of the heater control chips (PWM ASIC) to show how they are linked. All ASICs for the quantum simulator are synced via a global clock from the PCB and get the same clock signal. Individual ASICs can independently get the clock with different delays to reduce peak loads on the supplies. The correct phase is only important for the Gater ASIC. The clock must be externally adjusted so that the gating window is then placed correctly with respect to the laser pulse. The charging time of the SPADs need to be set and adjusted via the charge bias voltage input. Depending on the actual capacitance of the SPAD node (determined by process variation), the needed charge time varies a bit. It should be long enough for the SPAD to be fully charged, so the voltage at the SPAD cathode is about 2.55 V, but at the same time as short as possible. During the charging time, detection of photons is not possible; therefore, the charging time should not be longer than necessary to fully charge the SPADs. To obtain gating windows shorter than 1 ns, the SPAD can also not be fully charged. The bias voltage "S&H" and the reference voltage of the comparators must be adjusted. To work, the achieved charge voltage may only be changed in the range of about 2.25 to 2.55 V. The duration of the gating window is set via the window bias voltage. [5]

Layout

To integrate the SPAD directly into the Gater ASICs silicon wafers with a low-epitaxial substrate was selected. A low-epi wafer has a relatively thin epitaxial (epi) layer grown on top of a heavily doped substrate. Integrating the SPADs into the CMOS chip requires that the negative anode of the SPAD be connected directly to

the ASIC substrate. This configuration necessitates robust isolation of the transistors and other structures from the substrate. In the initial design phase of the SPAD, there was the possibility that the SPAD could have a breakdown voltage of up to 60 V. The necessitated isolation including the 10 V excess bias required an isolation of 70 V, which is nearly double the maximum voltage rating of the process specification (deep n-well to substrate).

The increase in maximum isolating voltage is realised by a different wafer substrate (low-epi), rounded corners, and increased spacings. The usage of a low-epi substrate layer, which is lightly doped, typically increases the breakdown voltage of the isolation n-well to the substrate junction. This is because the lower doping level expands the depletion region, allowing the junction to sustain a higher reverse bias before reaching breakdown. [57] To retain the advantage of a higher breakdown voltage using the low-epi substrate, the spacing between deep n-wells must be increased. With a lower doping concentration, the depletion regions extend further laterally under reverse bias conditions. This increased lateral extension can lead to higher electrical field overlap between neighbouring wells, potentially causing premature breakdown or leakage. Therefore, additional spacing between deep n-wells is needed to maintain isolation and ensure reliable operation. To further increase the breakdown voltage of the deep n-wells, the corners are rounded. Breakdown typically initiates at the edges or corners of the deep n-well. These areas tend to exhibit higher concentrations of the electric field due to field crowding, which makes them the most vulnerable points for the onset of avalanche breakdown between the deep n-well and the substrate [58]. Therefore, all corners are rounded. Another possibility to obtaining a higher breakdown voltage is to increase the lateral distance between the deep n-well and the substrate guard ring. This reduces the electric field crowding at the junction edges, thereby increasing the breakdown voltage. Implementing this design modifications made some design rule violations of the process necessary, such as the spacing between isolating deep n-wells and the spacing between substrate guard ring (high voltage p-well) and deep n-well. The changes were approved by the foundry for fabrication. [5]

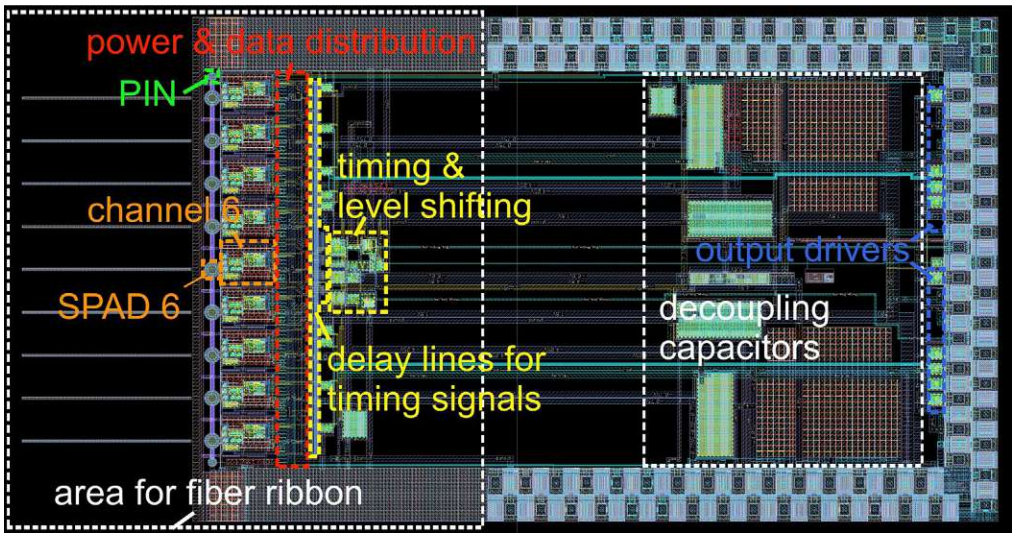


Figure 18: Layout of the Gater ASIC with 9 integrated 50 µm SPADs. Source: [5]

AS described in 1.2 the layout of the Gater ASIC was designed in Cadence Virtuoso Layout GXL. The layout of the Gater with integrated SPADs is shown in Figure 18 and has a size of approximately 3 x 5.8 mm². The dimensions and placement of the pads are shown in Figure 19. The SPADs are arranged at a pitch of 254 µm to precisely align with the intended fibre ribbon [59], causing the ASIC dimensions to exceed what would otherwise be possible with the circuitry alone. The end of the fibre ribbon must be mounted as close as possible to the surface of the Gater ASIC to couple almost all of the light from the fibres into the SPADs, thereby restricting the location of the bond wires and pads from occupying this area. The dimensions of the fibre ribbon measure 10.0 mm × 4.25 mm. The area needed to place the fibre ribbon is marked in white in Figure 18. This is the reason why the Gater for external SPAD presented in the following Chapter 2.3 only requires a fraction of the area.

Two integrated PIN photodiodes, positioned with a spacing of 127 µm on each side of the SPAD array, should also help to place and glue the fibre ribbon to the ASIC. To use them, the fibre ribbon has two additional optical fibres on each side where a constant light intensity is coupled in. By moving the fibre ribbon and monitoring the PIN photodiodes, the perfect position can be located. The fibres in the ribbon have a spacing of 127 µm with only every second fibre being used to couple the light into the SPAD. [5]

Due to fast and simultaneous switching across all channels, significant current peaks emerge. Consequently, large arrays of DMIM and MOS capacitors, shown on the right side of Figure 18, stabilise the various supply voltages. The MOS

capacitors have higher area capacitance but are only available with a maximum voltage rating of 3.3 V. The layout of the DMIM capacitors was challenging due to the complex antenna design rules from X-Fab. Missing design rules in the design rule file used for the design rule check in 'Assura' make a reading of the thousands of capacitors necessary, which took nearly a hole person month. [5]

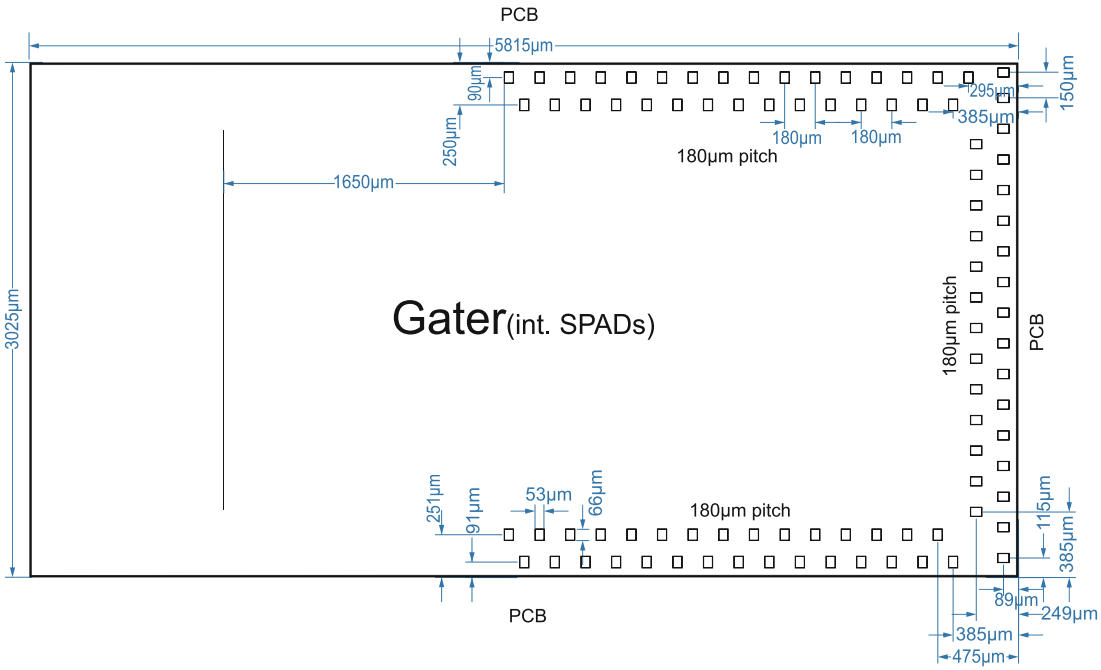


Figure 19: Dimensions of the Gater chip with external SPADs, outer dimensions without saw trench (values rounded to µm).

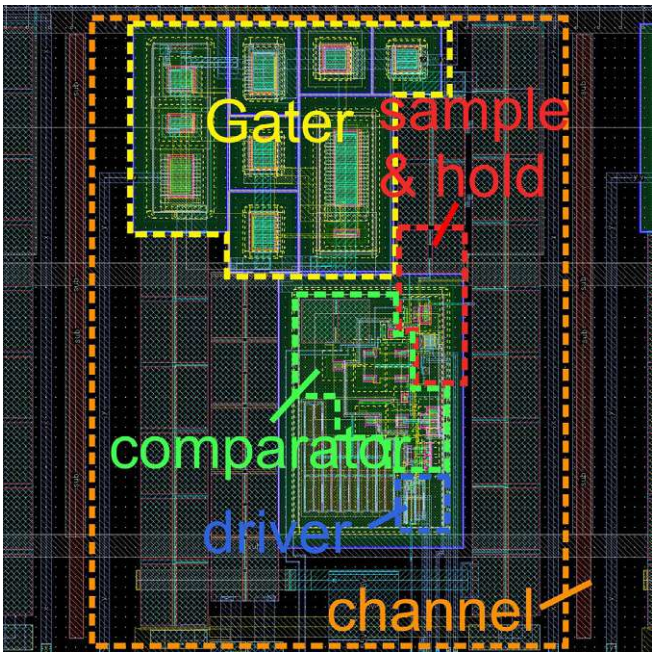


Figure 20: Layout of one Gater channel including power, data and timing connections. Source: [5] (modified)

A detailed view of a single gating channel (compare Figure 14), which occupies an area of 380 × 640 µm² in Figure 20. The yellow marked 'Gater' includes the high-voltage cascode switch with the dual adaptive bias circuit. The 10 MOSFETs are placed in 8 deep n-wells with different bias voltages to keep their voltage ratings within the 9.9 V configuration and isolate them from the very negative substrate. To save space, the NMOS transistors M_{n1} – M_{n3}, as well as M_{n4} - M_{n5} in Figure 15, share the same deep n-well. Due to the high voltage differential between the isolating deep n-wells and the substrate, the corners of the deep n-wells are rounded. Similarly, the corners of the p-wells for transistors M_{n1}, M_{n2}, M_{n3}, M_{n4} and M_{n5} within the high-voltage switch are also rounded to reliably handle voltages exceeding the nominal 8 V between the p-wells and the deep n-wells. [5]

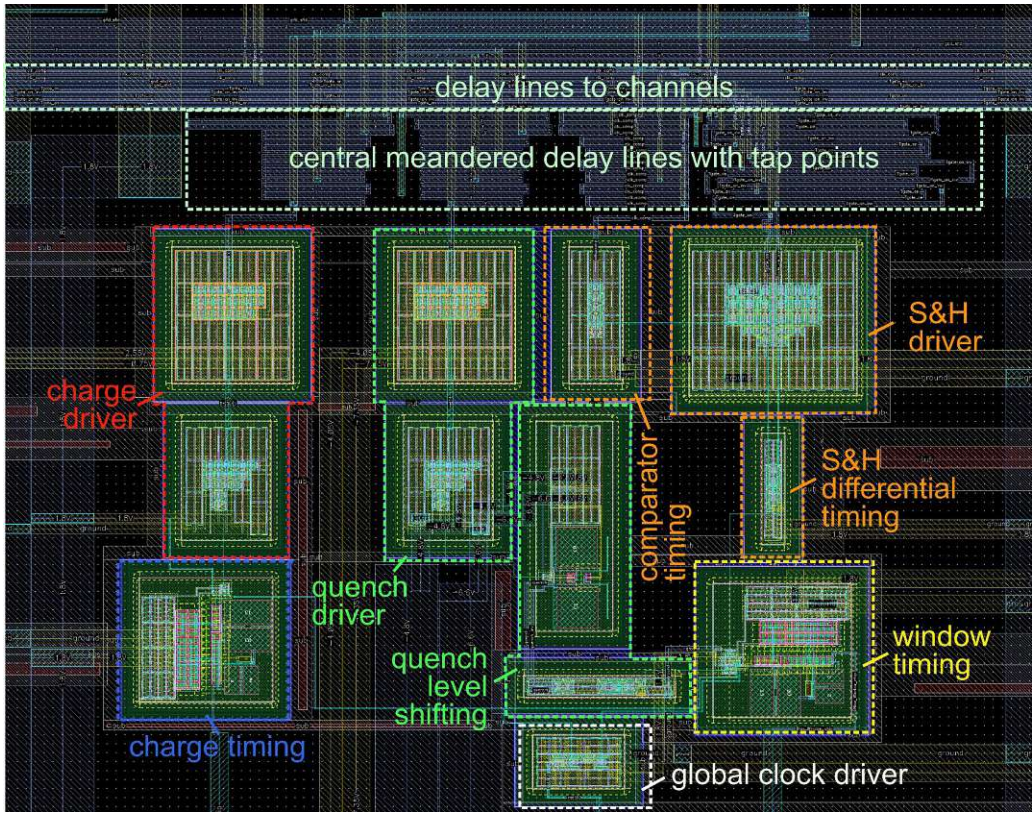


Figure 21: Layout of timing generation, level shifting circuits and delay lines.

The PMOS transistors M_{p1} – M_{P5} from the circuit shown in Figure 15 needs to be in separate deep n-wells, because each one requires a separate body connection (bulk) which is connected to their corresponding drain contacts and shift therefore during the switching process individually. An array of MOS capacitors is placed directly next to the comparator to prevent wrong decisions caused by distortions. The blue-marked driver is only the first small driver followed by a powerful driver outside the channel, which drives the tract to the digital output driver next to the

corresponding digital output pad on the other side of the ASIC. Each driver includes a MOS capacitor bank and a defined metal resistance to reduce feedback to the global 1.8 V supply lines. The digital output driver located directly next to the pads has separate 1.8 V supply pads to further mitigate the effects of switching operations on the analog circuits. [5]

The central timing generation and level shifting circuits for all channels are shown in Figure 21 occupies an area of about 420 × 320 µm². The large distances between the individual channels and the extreme demands on simultaneity were a major challenge. A delay line architecture was proposed. Post-layout simulations with corner analysis were performed for a large variety of variants to create the best possible matching between the channels. In the upper part of Figure 21 the delay lines for the timing signals are visible. They ensure that the propagation delay is the same for all channels. After the driver, the traces are meandered to create tap points with different delays which are then connected to the horizontal distribution traces to the channels. The meandering interconnect structure reduces the capacitive load on central drivers, thereby minimising associated power dissipation. The correct distribution of the timing signals was one of the biggest challenges of the layout.

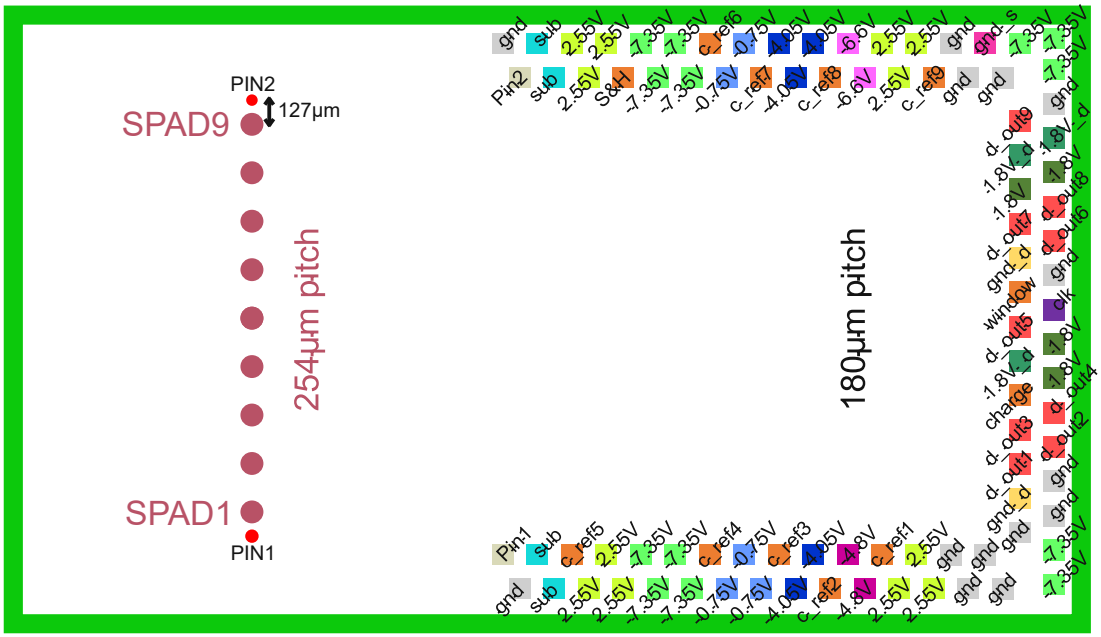


Figure 22: Pad layout of the Gater with integrated SPADs (internal Gater).

The pad layout for the internal Gater is shown in Figure 22. The padring, the outermost structure that surrounds the chip, consists of a ring of I/O pads, power pads, and ground pads. The pads in the padring are surrounded by metals that

form a ring around the chip and distribute the 2.55 V supply, the -7.35 V supply, and the substrate voltage. 2.55 V is connected to the top metal layer, -7.35 V to the metal 3 layer, and the substrate voltage to metal 1. This configuration adds decoupling capacitance between the supplies on metal 3 and metal top. The metal 2 layer is used as a guarding layer with a separate ground pad to shield substrate from -2.55V in the padring. The pitch of the pads to the PCB is 180 µm, only one pad at the corner has a pitch of 150 µm (red marked in drawings). All pads have a size of 53 µm x 66 µm. Toward the PCB the ASIC has 12 bias pads, 46 supply voltage pads with 7 different voltages, 16 ground pads (separated in ground groups), 9 digital output pads, 4 substrate voltage pads, two PIN photodiode pads, and one clock pad. In Table 3 all different pad types are listed with a short description and further voltage and current information.

Table 3: Description of the pads of the Gater with integrated SAPDs, including estimated voltage and current range.

connected to	pad name	description	type	voltage (range)
PCB	gnd_d	ground for digital output drivers	ground	0 V
PCB	gnd	ground for analog control circuits	ground	0 V
PCB	gnd_sh	shield ground connected to layer which shields substrate from -2.55V in padring	ground	0 V
PCB	1V8	1.8V for digital and analog control circuits	voltage supply	1.8 V
PCB	1.8V_d	1.8V for digital output drivers	voltage supply	1.8 V
PCB	2.55V	2.55V for the Gater switch	voltage supply	2.55 V
PCB	-0.75V	-0.75V for the Gater switch	voltage supply	-0.75 V
PCB	-4.05V	-4.05V for the Gater switch	voltage supply	-4.05 V
PCB	-7.35V	-7.35V for the Gater switch	voltage supply	-7.35 V
PCB	-4.8V	-4.8V for a control circuit	voltage supply	-4.8 V
PCB	-6.6V	-6.6V for a control circuit	voltage supply	-6.6 V

PCB	CLK	clock input which triggers with a delay the gating window and resets the comparator/digital output (80MHz)	clock	digital 0 V / 1.8 V
PCB	d_out1 ... d_out9	separate digital output from comparators of every channel	digital output	digital 0 V / 1.8 V
PCB	sub	substrate voltage of the Gater chip; same voltage as of the backside of the ASIC	voltage supply	-30 V – -60 V
PCB	Pin1	integrated pin-photodiode for positioning the fibre array: Pad - Cathode | PIN1 | Anode - Substrate	PIN photodiode	
PCB	Pin2	integrated pin-photodiode for positioning the fibre array: Pad - Cathode | PIN2 | Anode - Substrate	PIN photodiode	
PCB	charge	determines the SPADs charging time; voltage which is applied at the pad generates a corresponding dc current out of the Pad	Bias	0 – 1 V (-1 – 0 mA)
PCB	window	determines the gating window duration; voltage which is applied at the pad generates a corresponding dc current out of the Pad	Bias	0 – 1 V (-1 – 0 mA)
PCB	S&H	bias voltage for sample and hold stages for all channels; determines indirect also the comparator threshold because it level shifts the comparator input voltage	Bias	0 – 1.8 V (no dc)

Figure 23 shows a stitched microscopic image of the ASIC mounted on a printed circuit board (PCB), displaying attached gold bond wires but without the fibre ribbon. A ball bonder was used to obtain the best bonding result. The SPADs shown in the chip layout in Figure 18 have a diameter of 50 µm.

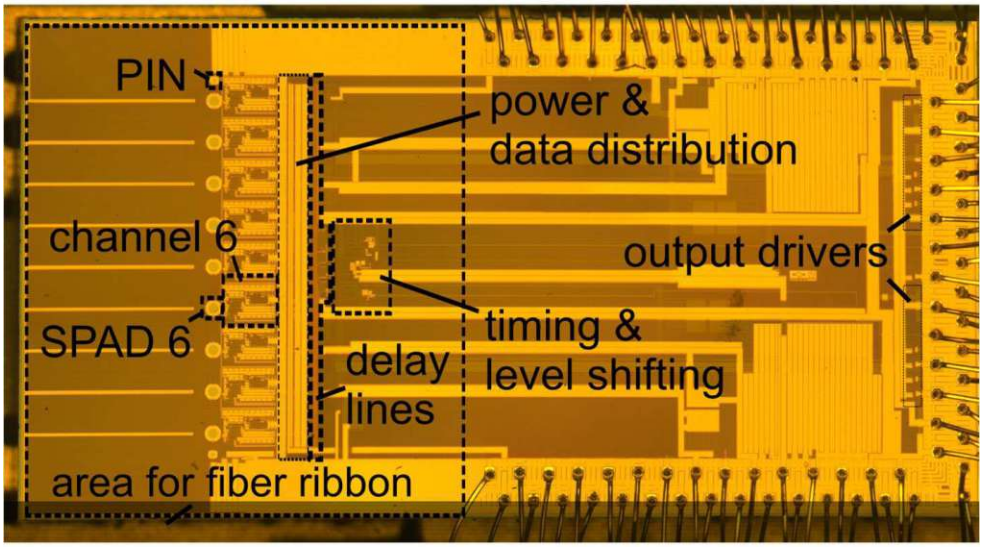


Figure 23: Microscopic image of the complete multi-channel gating ASIC with integrated 50 µm SPADs glued on a PCB with bonding wires. Source: [5]

The layout of the complete MLM from the first production run, where the ASICs and the PIC are connected via wire-bonds and test structure, is shown in Figure 25. The total usable are of the MLM reticle (photomask) module is 9 × 11 mm². The final wafer and therefore the ASICs are sanded to a thickness of 300 µm. The diameter of the wafers produced is approximately 200 mm. As described in Chapter 2.2.1 the Gater ASIC with integrated 20 µm SPADs was also designed and produced in the first production run. The versions with the 20 µm and the 50 µm SPADs are shown in the MLM layout.

Three dicing plans for the first production run, shown in Figure 24, were necessary to avoid a picking step and to get all chips, including test structures. Although this procedure results in many chips being destroyed by the cutting process, enough remain available for characterisation and integration into the quantum simulator.

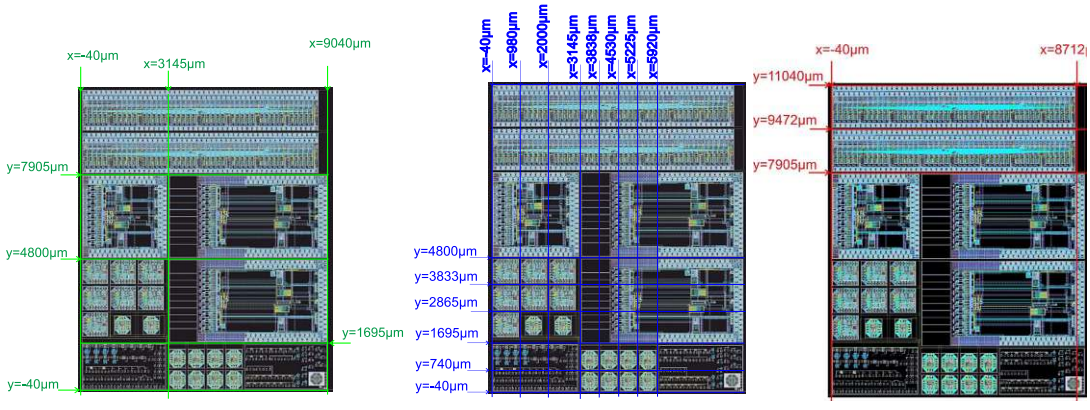


Figure 24: Dicing plan for the wafers from the first XH018 run (left and middle on low-epi substrate wafer; right on stand substrate wafer).

Figure 25: Complete layout of the MLM for the first production run.

2.2.3 Simulation and Measurement

As described in Section 1.2, the analog design flow was employed for the development of the Gater ASIC. Within the virtual testbench environment of Cadence, the chip was connected to the bond wire models and appropriate load conditions on the digital outputs. A design loop was carried out that included pre- and post-layout simulations, including DC, AC, and transient analyses, to ensure that all performance specifications were met and to optimise the physical layout. Estimations from the post-layout simulations indicate possible values for the bias voltages can be found in the appendix in Table 7. Furthermore, parameter sweeps and corner analyses (temperature, process) were conducted to evaluate the design's robustness under variations and to verify compliance with all defined

requirements.

To test the Gater ASIC, a test-PCB is necessary. One test-PCB which can host either the intern Gater or the external Gater with an external SPAD array is used to reduce costs. For designing the PCB especially, the supply and bias currents of different inputs were post-layout simulated. As expected, the currents of the external Gater are higher and therefore are used for designing the PCB. (Simulated supply and bias current curves at the pads of the external Gater can be found in the appendix Figure 100 - Figure 109.) Despite the large decoupling on the ASIC, it turned out that the required variations in supply current to meet the specifications are very high. Therefore, HF capacitors with the lowest possible ESR were placed near the bond pad on the PCB. The simulation results show that all bond wires should have the lowest possible inductance, ideally less than 1 nH, which corresponds approximately to a wire length of 1 mm. This requirement is particularly critical for power supplies and ground connections, which are very sensitive to parasitic inductance. In the second pad row, slightly longer bonding wires can be tolerated. For the bias pads an inductance up to 5 nH is permissible. The bond wires to the digital output pads may also be up to 5 mm long; however, this length affects the slew rate of the digital output signals. The bond wires connected to the PIN photodiode pads are used solely for the alignment of the fibre ribbon during setup and are not critical for dynamic operation; therefore, only their DC performance is relevant and significantly longer bond wires are tolerable.

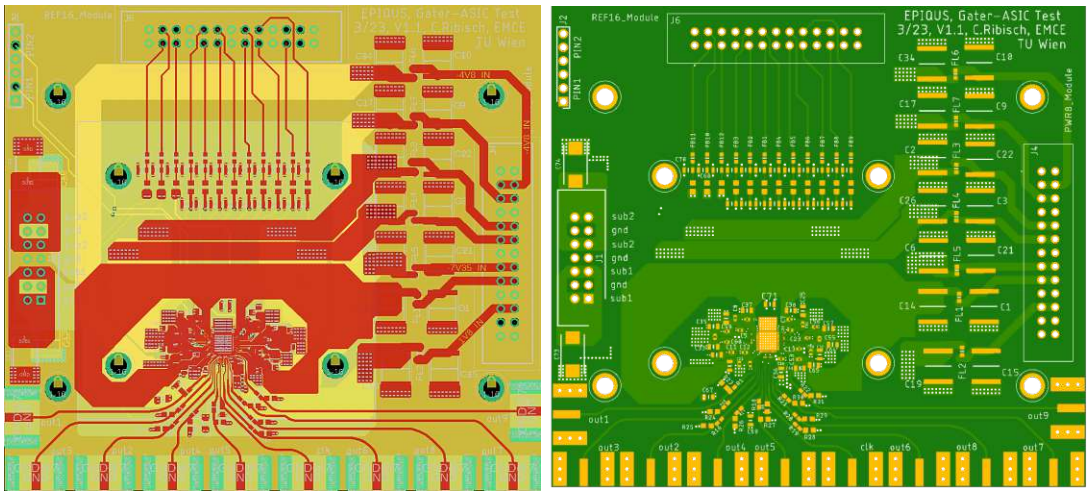


Figure 26: Test-PCB for either the internal or external Gater from the first run (left: layout; right: rendering).

A test-PCB with 6 layers and FR4 substrate was designed and produced by “Multi Leiterplatten GmbH”. The layout of the test-PCB shown on the left in Figure 26. It

is designed to host either an internal or external Gater with a dedicated SPAD chip. This was realised with a gap in the substrate pad, which makes a substrate split for the external SPAD chip possible. The split in the substrate pad is also visible in the rendering of the test-PCB on the right in Figure 26. The smallest PCB pads for wire bonding have a spacing of 100 mµ, which is the minimum possible distance of the PCB manufacturer.

The chip temperature is actively regulated at 25 °C using a thermoelectric cooler on the back of the PCB. The pad on which the chip is glued has 84 vias (0.2 mm hole) to conduct heat to a large metal area on the bottom layer. Stabilisation of the Temperature is essential for accurate characterisation of SPADs, as key parameters such as breakdown voltage and dark count rate exhibit a strong temperature dependence [60]. A fully assembled test-PCB with a glued Gater ASIC with integrated SPADs and soldered parts ready for characterisation is shown in Figure 27.

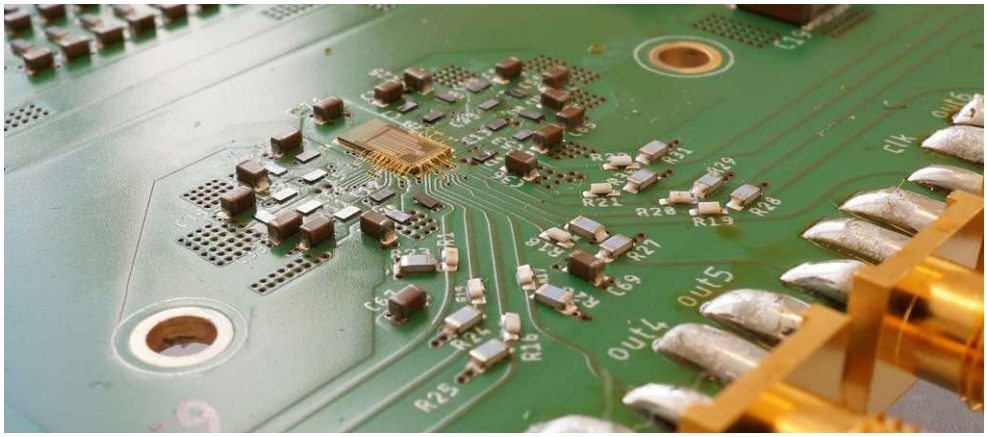


Figure 27: Glued internal Gater on the assembled test-PCB.

The measurement setup is based on the configuration described in [61] and is controlled by a PXI system from National Instruments (NI), consisting of an NI-PXIe-1082 chassis and an NI-PXIe-8840 controller, as illustrated in Figure 28. The system is equipped with a FlexRIO FPGA module (NI-PXIe-7972R), which facilitates real-time streaming of sampled data from a high-speed digitiser (NI-PXIe-5162) that operates at 625 MS/s. The FPGA (field programmable gate array) is utilised to extract output pulses from the Gater ASIC and to compute pulse statistics used in evaluating the dark count rate (DCR) and afterpulsing probability (APP). The APP is determined by analysing interarrival time histograms obtained during dark condition measurements [60]. [5]

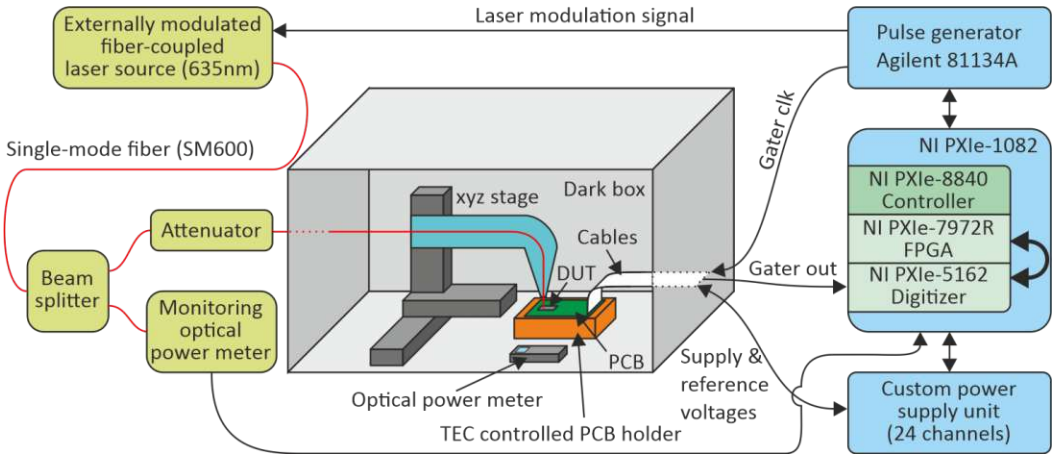


Figure 28: Experimental setup employed for the characterisation of Gater with integrated SPADs. Source: [5]

The PCB containing the Gater ASIC is placed inside a light-tight enclosure (dark box), shown in Figure 29, to eliminate background illumination during measurements. Light is coupled into the Gater's SPADs through a single-mode fibre (SM600, Thorlabs), which has a mode field diameter of approximately 5 µm, which is significantly smaller than the SPAD's active area, ensuring efficient coupling of nearly all incident photons into the active region. The precise alignment of the fibre output on the SPAD is achieved using a motorised XYZ positioning stage (MTS50, Thorlabs). The Optical power delivered to the SPAD is monitored using an optical power metre (PM100USB with a S150C sensor, Thorlabs) positioned outside the dark box. The fibre output is split using a fibre optic splitter, where one arm is connected to the power metre and the other to the SPAD. To prevent SPAD saturation while maintaining sufficient signal for accurate monitoring, an optical attenuator is placed in the SPAD arm to achieve a calibrated splitting ratio of 1125:1. Prior to measurement, this ratio was calibrated using a second optical power metre inside the dark box. The fibre output is aligned with the sensor head using the XYZ stage to ensure accurate power readings at the SPAD input. [5]

Only the Gater ASIC with 50 µm SPAD was characterised, because even this version does not show a clear intensity plateau by scanning the SPAD with the fibre. With an even smaller SPAD size, fewer of the generated electron-hole pairs would lead to a sufficiently large and self-sustaining charge carrier avalanche due to the field distribution. The 20 µm SPAD would be too small and the corresponding Gater ASIC was not characterised.

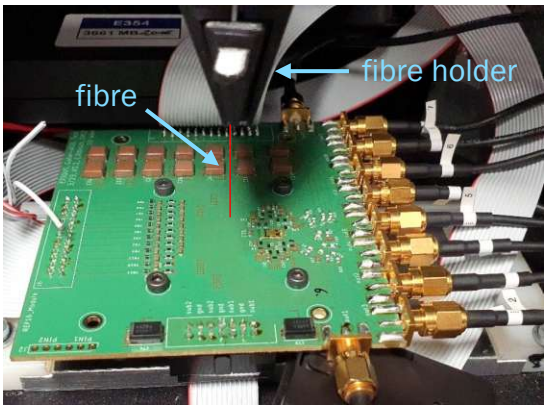


Figure 29: Internal Gater bonded to test-PCB with fibre on XYZ stage in dark box.

A custom-built, fibre-coupled laser source emitting light with a wavelength of 635 nm was employed for optical characterisation. This laser is externally modulated using an electro-optic modulator (AM635, Jenoptik). Due to the availability of this high-speed light source with a high extinction ratio, SPAD characterisation was conducted exclusively at this wavelength. The measured extinction ratio within the experiments was approximately 100. The laser was modulated with 2 ns optical pulses repeating at 15 MHz, which determines the gating frequency. It is important to note that, due to the finite extinction ratio, the measured optical power includes contributions from both the pulse and the interpulse interval. As a result, the instantaneous optical power during the pulse is overestimated, leading to an underestimation of the photon detection probability. Therefore, the real PDP of the ASIC will be slightly higher than calculated. For PDP characterisation, the mean photon arrival rate was set to 255,000 photons/s. A relatively low gating frequency of 15 MHz was deliberately selected to suppress the afterpulsing probability. The modulation signal for the laser, along with the gating signal for the Gater ASIC, was generated using a precision pulse generator (Agilent 81134A), which enabled fine control of the temporal delay between the gating window and the photon arrival window. This allowed an accurate alignment of the gating window with the arrival of optical pulses at the SPADs. [5]

During the measurements, the gating window was set to approximately 4.5 ns. The reference voltage was individually optimised for each SPAD channel, while a sweep of the substrate voltage V_{sub} from −32 to −43 V was done to evaluate performance across biasing conditions. The dark count rate (DCR) and the afterpulsing probability were measured under dark conditions with the laser

source deactivated. The reference voltage (V_{ref} = compare ref.) for each channel was individually tuned to ensure optimal performance. [5]

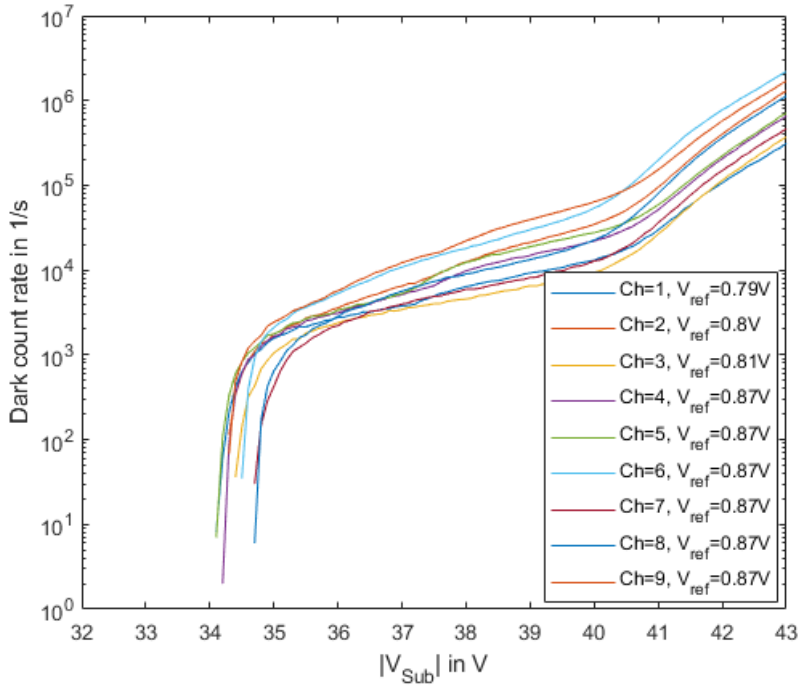


Figure 30: Extracted Dark count rate (DCR) of the internal Gater depending on the substrate voltage for all nine channels at room temperature (25 °C). Source: [5]

Figure 30 presents the extracted dark count rate (DCR) for all nine gating channels. Within the typical operating range, the DCR values range from several thousand to several tens of thousands of counts per second. It is important to note that these measurements were performed at room temperature (25 °C). As demonstrated in [60], device cooling can significantly reduce the DCR, making thermal management a key factor for further optimisation. The breakdown voltage across the channels shows a variation of less than 1 V, indicating good process uniformity. To optimise performance, particularly in terms of PDP and DCR, an individually reference voltage is assigned to each channel. Increasing the reference voltage effectively lowers the comparator detection threshold, thus enhancing PDP by enabling the detection of smaller avalanche pulses. However, a too low detection threshold increases the sensitivity to noise, particularly thermal noise and mainly power supply noise, resulting in an increased false positive detection, which increases DCR and APP. Hence, the reference voltage for each channel is carefully tuned to maximise PDP while keeping noise induced triggering at an acceptable level. This is done by incrementally increasing the

reference voltage (i.e. reducing the detection threshold) until the comparator begins to exhibit a significant response to noise. Notably, the first three channels in Figure 30 require slightly lower reference voltages, which may be attributed to systematic variations such as unequal on-chip supply line resistance. However, since the reference voltage can be independently adjusted per channel, these variations do not compromise overall device performance. [5]

The afterpulsing probability (APP) was determined by analysing the distribution of interarrival times between consecutive detection events, using the methodology described in [60]. The results are shown in Figure 31. Within the useful operating range, the extracted APP remains relatively low, indicating favourable performance under standard conditions. Afterpulsing is known to be strongly influenced by the deadtime of the device. Consequently, a further reduction in the gating frequency of gating pulses could lead to a decrease in APP, as it allows more time for trapped carriers to recombine or dissipate. On the contrary, increasing the gating frequency shortens the effective recovery time, thus worsening the afterpulsing. [5]

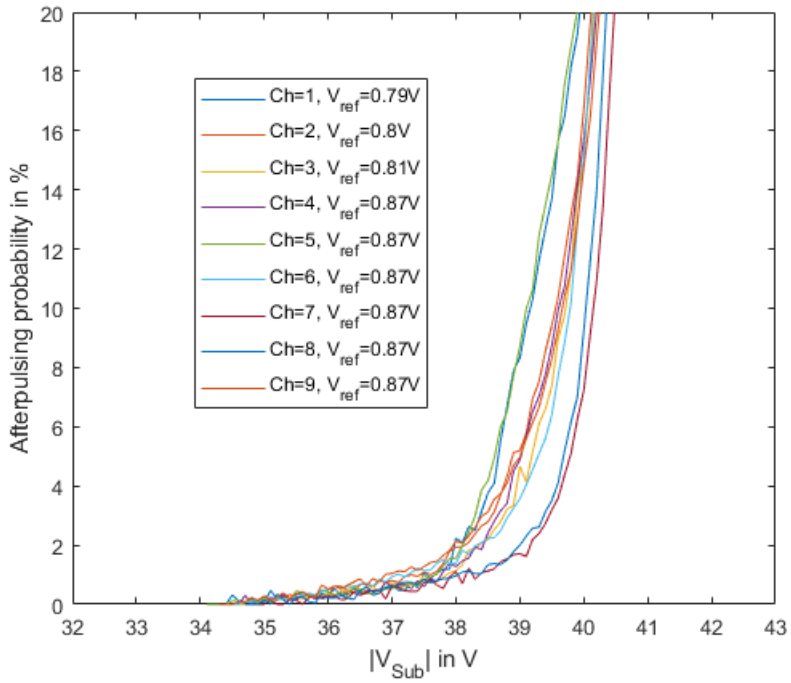


Figure 31: Extracted afterpulsing probability (APP) depending on the substrate voltage for all nine channels of the internal Gater at room temperature (25 °C). source: [5]

Figure 32 illustrates the extracted photon detection probability (PDP), measured at a photon rate of approximately 255,000 photons per second. The data have

been corrected for saturation effects of the Gater ASIC, as well as for contributions from afterpulsing and dark count events. However, the limited extinction ratio of the laser source was not compensated for, as photons incoming between two gating windows may still contribute to the count rate. This occurs if these photogenerated carriers diffuse into the absorption region when the gating window is active again. As a result, the reported PDP values represent a slight underestimation of the actual performance. Differences in PDP, caused by optical transmission through the oxide stack, can cause variations between channels. The SPADs implemented in this ASIC lack an antireflection coating, which introduces interference effects within the oxide layers. These interference effects result in a strongly wavelength-dependent PDP, as discussed in [53]. Variations in the thicknesses of the oxide layers, either across one chip or between wafers, cause significant differences in optical transmission. These variations can shift the positions of constructive and destructive interference, leading to measurable and wavelength-dependent differences in transmission between channels. These factors lead to a different wavelength-dependent PDP for every SPAD. [5]

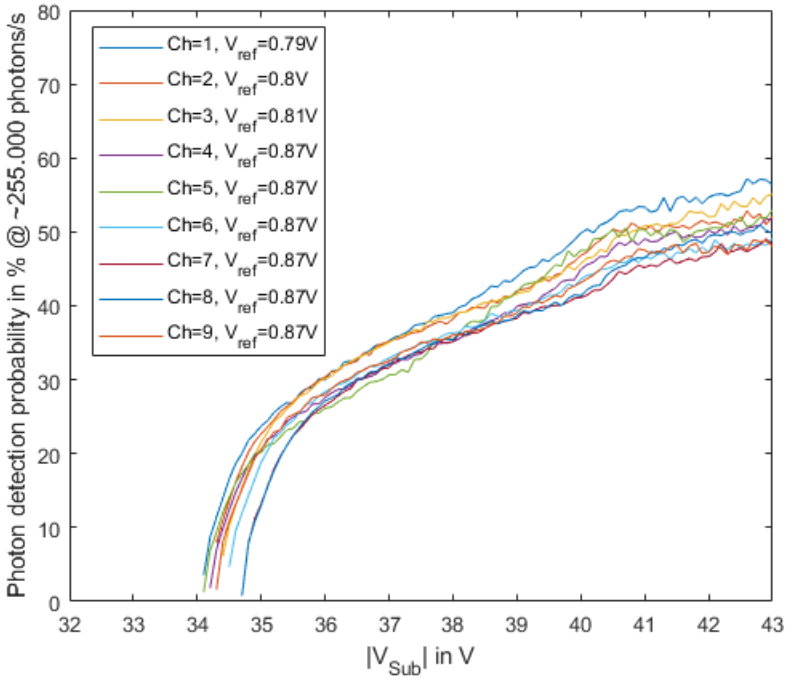


Figure 32: Extracted photon detection probability (PDP) depending on the substrate voltage for all nine channels of the internal Gater chip at room temperature (25 °C) and at a photon rate of ~255.000 photons/s with 635 nm laser source. source: [5]

Measurements of dark count rate (DCR) and afterpulsing probability (APP) show consistent behaviour across channels, suggesting comparable defect densities

within the SPAD structures. The observed differences in PDP may indicate variations in the dose or profile of ion implantation within the avalanche region, which can influence the carrier multiplication efficiency. The PDP achieved is significantly higher than the ~35 % reported at 635 nm in [62], where SPADs were implemented in a 0.35 µm CMOS technology with a maximum excess bias voltage limited to 6.6 V. The SPAD implemented in 0.35 µm CMOS in [52] achieves with an excess bias voltage of 9.9 V a much higher PDP (67.8 %, 642 nm) than the investigated SPADs in 0.18 µm CMOS. However, in principle, the results highlight the advantage of operating a SPAD at higher excess bias voltages, which enables increased avalanche triggering probability and thus improved PDP. [5]

The measurement showed that the internal Gater has a mean power dissipation of less than 250 mW. The thermoelectric cooler on the backside of the PCB could easily cool the chip to stable 25 °C. The 55 x 55 mm surface area of the connected cooling block appears to be more than sufficient.

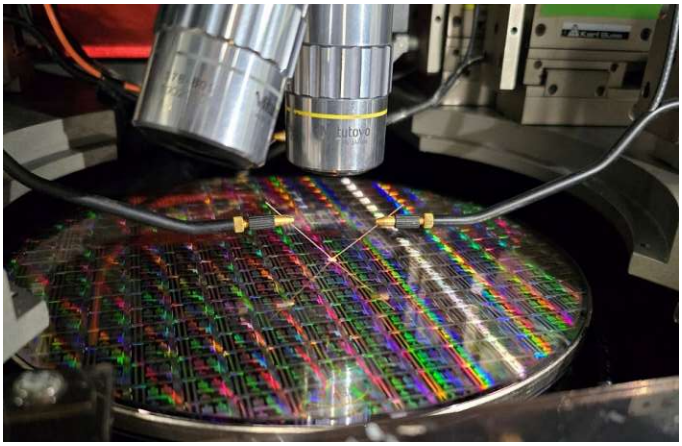


Figure 33: Deep n-well breakdown measurements with needles directly on a wafer on the wafer prober.

To prove whether the modification to the isolation really increased the breakdown voltage of the deep n-well, measurements were performed with test structures from the production runs. A full wafer (low-epi substrate) was placed on the wafer prober, and needles were placed to contact a deep n-well and substrate, as shown in Figure 33. The regular corners show a breakdown at about 55 V, while the rounded corners show a breakdown at 75 V. The standard edge corners with the standard (design rules) spacing between a deep n-well and substrate guard ring (p-well) reduces the breakdown voltage to about 53 V. This leads to the conclusion that the breakdown is probably caused mainly by the deep n-well corners and happens close to the bulk surface.

Comparison and conclusion

Compared to the gating circuit implemented in 0.35 µm CMOS technology employing single cascoded structures and supported a maximum excess bias voltage of 6.6 V, resulting in a photon detection probability (PDP) of approximately 35 % (635 nm) [62], the present design achieves a PDP of around 50 % (635 nm) with an increased excess bias voltage of 9.9 V. However, the result is significantly lower than expected from device simulations (~72 % at 635 nm, 9.9 V excess bias) and lower than the 67.8 % PDP in 0.35 µm CMOS (642 nm, 9.9 V excess bias) reported in [52]. Therefore, the development of a custom SPAD in XH018 (see Chapter 2.2.1) was not successful. Further examination and simulations by the colleague who designed the SPAD indicated that the fact that the PDP of this SPAD is very sensitive to process variations might be the reason for the worse results.

The total power consumption of the gating switch, comparator, and output driver in [63] was approximately 60 mW at 100 MHz. The CMOS gating circuit presented in this thesis exhibits a significantly lower power consumption of 27.8 mW per channel. The proposed circuit also demonstrates superior dynamic performance. The simulated quenching 90%-to-10% fall time is 0.28 ns, corresponding to a quenching slew rate of 28.3 V/ns, an exceptionally high value. This result outperforms that of the 0.35 µm SiGe BiCMOS-based gating circuit reported in [64], where the comparator alone has a power consumption of 30 mW and needs a switching time of 250 ps at a 1 MHz count rate, and the excess bias voltage was limited to 5 V. The PDP achieved with the integrated SPADs significantly exceeds the approximately 25 % PDP of the InGaAs SPADs at 1.55 µm wavelength, which are commonly used in quantum simulation experiments (supplementary information: [65]). As such, the Gater ASIC with integrated SPADs offers a promising platform for improved quantum simulators. [5]

The combination of fast switching times and short full width at half maximum (FWHM) of the gating pulses enables the use of high repetition rate laser pulses, making the system well suited for the quantum simulator. Furthermore, the modular architecture of the Gater ASIC allows for straightforward scaling to a higher number of channels, thereby enabling simulations with a greater number of qubits. [5]

To further enhance performance, several design optimisations are suggested. Reducing the mismatch in the SPAD breakdown voltages would improve uniformity across channels. The availability of an antireflection coating would mitigate interference effects within the oxide stack, thereby reducing process-dependent variations in PDP. Additionally, minimising the dark count rate and afterpulsing probability, particularly at excess bias voltages above 6 V, and increasing the PDP remains a key objective. Finally, to simplify system integration, future designs should eliminate the need for per-channel reference voltage adjustments by enabling the use of a single shared bond pad. [5]

2.2.4 Second Run and Outlook

To enable flip-chipping for the desired 3D integration of all chips, a second X-FAB XH018 production run was necessary. An improved version of the integrated SPADs based on the XH018 X-FAB process was developed to reduce dark counts and afterpulsing. This enhancement was achieved by modifying the n+ region and removing the STI that contacted it. Three slightly different versions (two of them redesigned) of the integrated SPADs were created and integrated into the nine-channel Gater design.

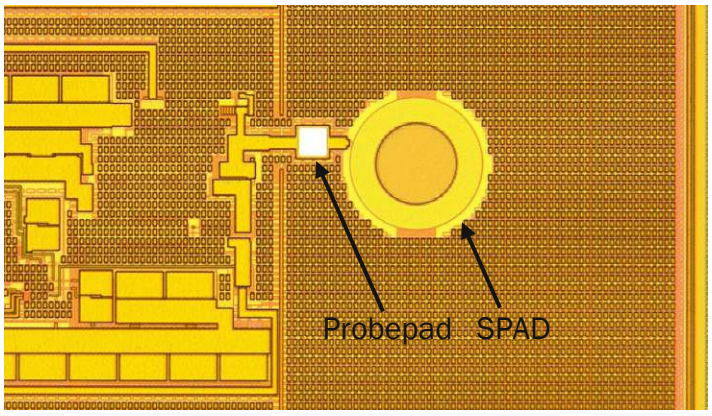


Figure 34: Microscopic image of a SPAD and a Probepad of internal Gater from run 2.

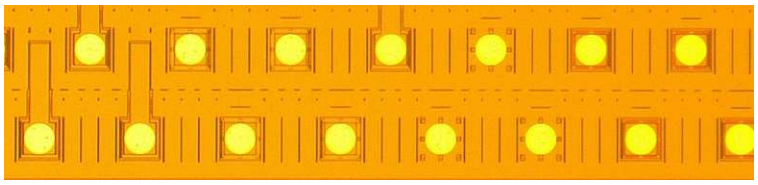


Figure 35: Microscopic image of the padring, with circular shaped pads, of the internal Gater from run 2.

Additionally, to capture the transient behaviour at the cathode, small probe pads (18 × 18 µm) were placed directly into the metal line between the Gater output driver and the SPAD cathode, adding only about 2 fF of capacitance from the cathode node to the substrate. The low increase in capacitance is possible because only the top metal without a via stack was used, with the downside that it is relatively fragile. While 15 × 15 µm pads were technically feasible, slightly larger pads were chosen to facilitate the placement of probe needles (e.g.: Picoprobe) easier. A close-up image of the SPAD and Probepad is shown in Figure 34.

The chip has been significantly reduced in size, as a fibre optic ribbon is no longer required above the SPADs. Therefore, also the two PIN photodiodes for placing the ribbon and the corresponding pads were reassigned to power supplies and ground inputs. The layout is shown on the left side in Figure 36. As required for the flip-chipping process, the passivation opening of all pads was changed to a circular shape with a diameter of 53 µm, as shown in Figure 35. This violates another design rule of the XH018 process, but it worked well. In addition, small improvements have been introduced, such as slightly longer active windows. A stitched microscopic image is pictured on the right side of Figure 36. The ASICs from the second production run have already arrived and are pending to be characterised at the time of writing this dissertation.

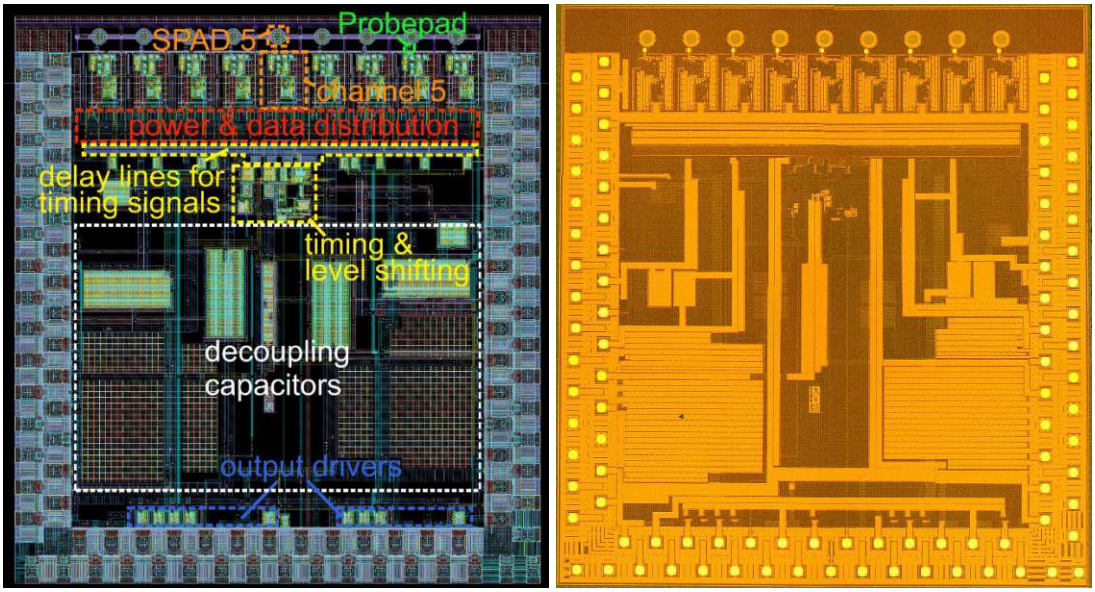


Figure 36: Layout (left) and a stitched microscopic image (right) of the Gater with 9 integrated SPADs.

The complete MLM layout for connecting PIC and electronic control circuits, including all ASICs for the quantum simulator and the test structure, is shown in Figure 37. The total usable are of the MLM reticle (photomask) is again $9 \times 11\text{mm}^2$. Three dicing plans, shown in Figure 38, were necessary to avoid a pick-up process. Although this procedure results in many chips being destroyed by the cutting process, a sufficient number remain available for characterisation and integration into the quantum simulator. Dicing Plan C is identical to Plan B and, therefore, is not shown in Figure 38 (the chips were sent directly to a project partner).

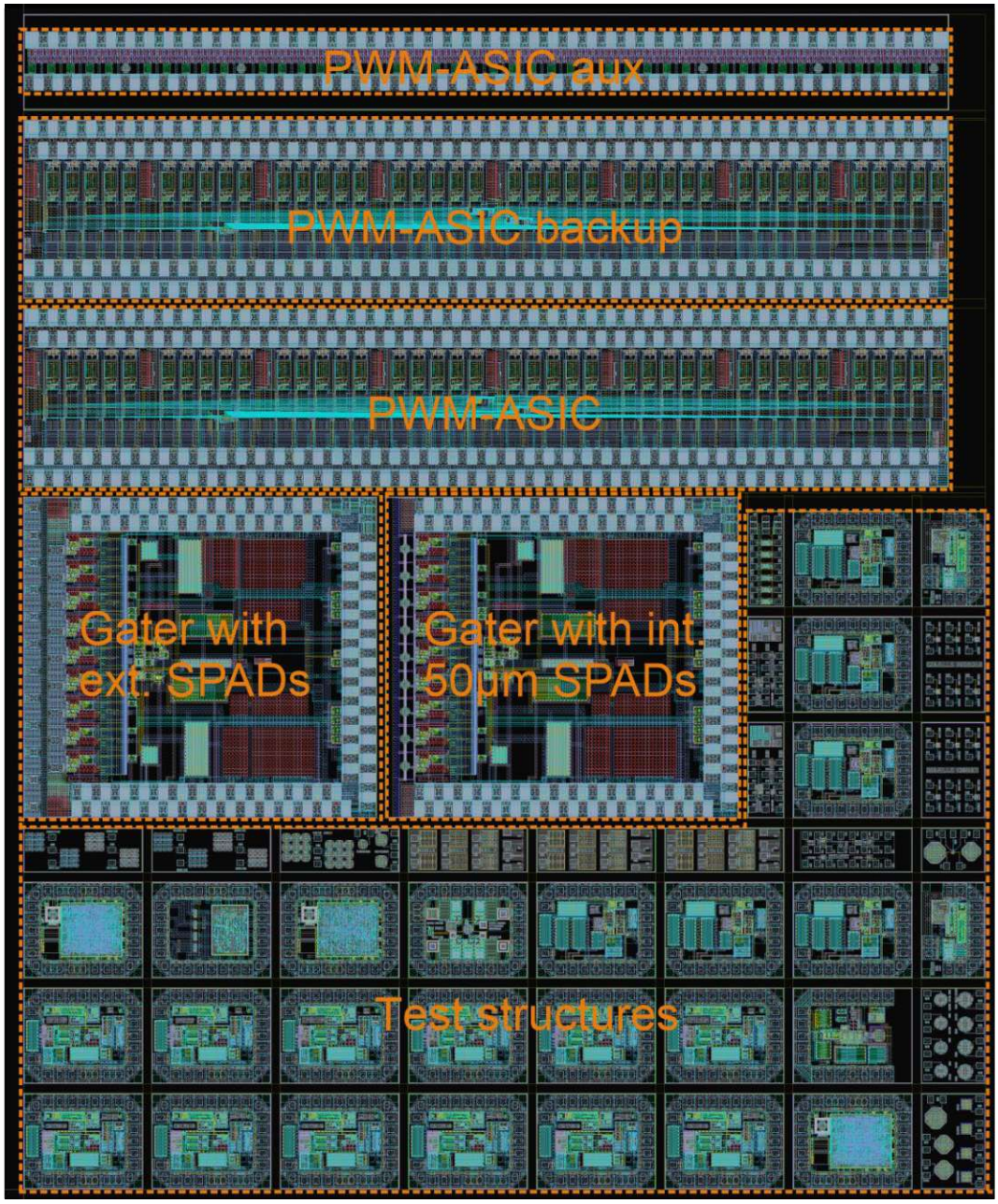


Figure 37: Complete layout of MLM ASIC run 2.

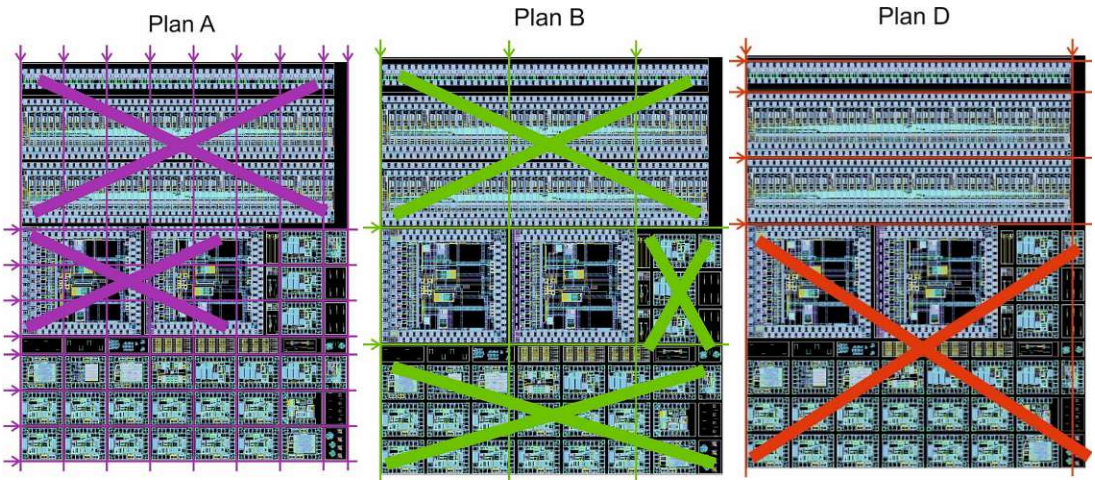


Figure 38: Dicing plan for the wafers from the second XH018 run (Plan A and Plan B on low-epi substrate wafer; PLAN D on stand substrate wafer).

To test the new chips, the test-PCB was also adapted and some improvements were made. Like the test-PCB for the Gaters from the first run, the test-PCB shown in Figure 39 was again designed to host either an internal Gater or an external Gater with a dedicated SPAD chip.

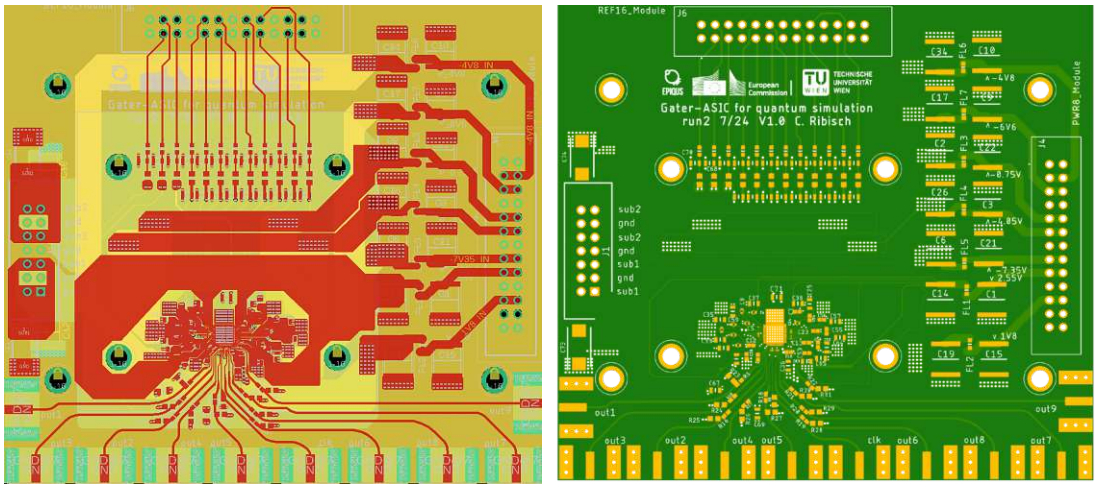


Figure 39: Test-PCB for either the internal or external Gater from run 2.

To further improve the ASIC in another production run, longer gating windows in the range of serval 10 ns could be implemented to make ASIC and SPAD characterisation more flexible and easier. Another improvement would be an additional active quenching circuit that quenches the SPAD if an avalanche is triggered. Due to the loop delay, the quenching time is slower than it is with very short gating windows, which was originally set to be in the range of 1 ns. By introducing longer active windows, an additional active quenching would be beneficial to reduce afterpulsing and prevent the SPAD from damage.

2.3 Multi-channel Gating ASIC with External SPADs

This chapter deals with the Gater ASIC which is designed to operate with external SPADs in contrast to the integrated version described in the previous Section 2.2 and is partly based on (confidential) reports and internal documentation within the EPIQUS project that I have independently authored. In this version of the quantum simulator system the detection stage is split into the SPADs on the PIC and a gating ASIC with the electronic integrated circuit, shown in the quantum simulator configuration in Figure 3. The SPADs are integrated into the PIC and their cathodes are wire bonded to the outputs of the external Gater ASIC. This combination represents the detection stage of the quantum simulator described in Chapter 1 and shown in Figure 1. The circuits are designed in the XH018 process from X-FAB as described in Chapter 1.2.

The ASIC is implemented as a gated quenching circuit, which is particularly advantageous for quantum simulations due to the precise knowledge of photon arrival times, as well as its capability to significantly reduce dark counts and afterpulsing. The SPAD is therefore operated in gated mode, which means that it is only photosensitive during the gating window (T_{on}). During the rest of time, it absorbs photons, but no avalanche is triggered (T_{off}). The gating widows need to be in the range of 1 ns and below. The output swing at the output pads and therefore the excess bias v_{exess} is 9.9 V. The main difference from the internal Gater is the much larger capacitive load and the inductance to the SPAD cathode. Bonding pads, metal tracs on the PIC and much wider metal traces on the ASIC are needed which add significant capacitive load to the Gater output node compared to the version with integrated SPAD. This additional capacitance increases the APP, because the APP is proportional to the total capacitance at the output node of the Gater. The bond wires also add some resistance and inductance into the connection between the switch and the SPADs. The fundamental functions and circuits are identical to those of the internal Gater described in Chapter 2.2.

2.3.1 Circuit and Chip Design

Figure 40 shows a simplified block diagram of the Gater for external SPADs. Each channel incorporates a double cascoded Gater switch (yellow), a sample-and-hold

stage (red), a sensitive comparator (green), and a series of digital output drivers (blue). Each output (for example 'SPAD1') features a dedicated bond pad, enabling direct wire bonding to the cathode of a SPAD. In the context of the quantum simulator, this refers specifically to the SPAD array integrated within the PIC. The circuit and function description of the High-voltage cascode switch, Sample & hold, comparator, and timing behaviour is identical to the internal Gater and described in Section 2.2.2. A microscopic picture of the integrated SPAD in the PIC is shown in Figure 41. Parasite capacitance, from the metal track and the PIC pad, and the SPAD intrinsic capacitance are estimated to be 450 fF. Therefore, the Gater switch must be able to drive such a load.

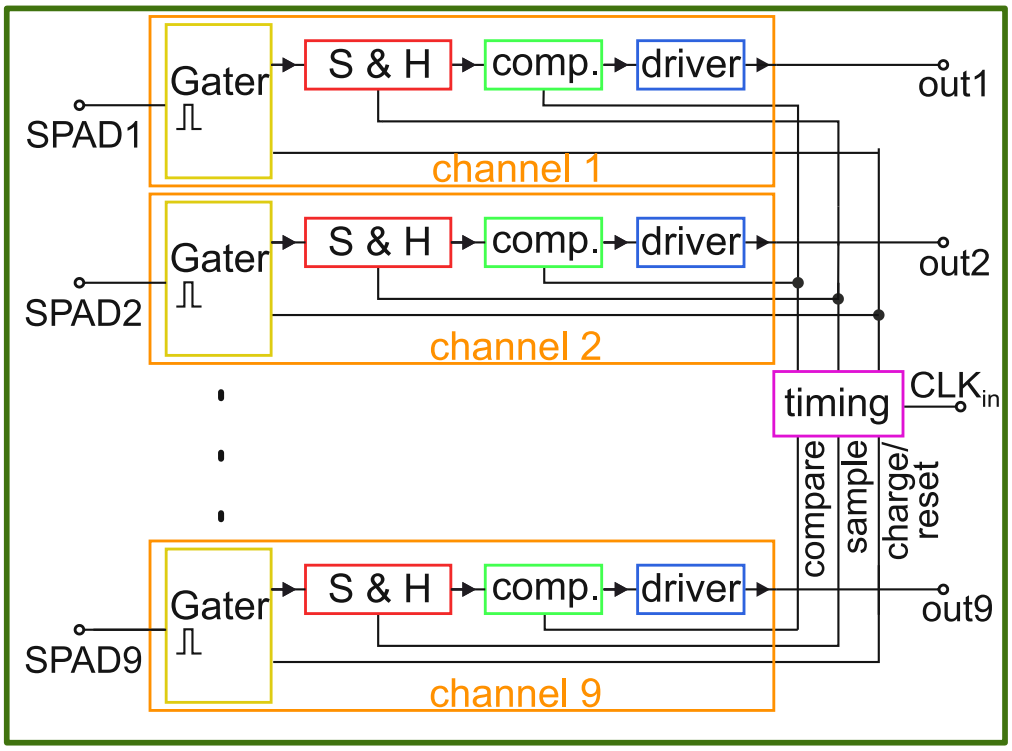


Figure 40: Block diagram of the Gater ASIC with external SPADs.

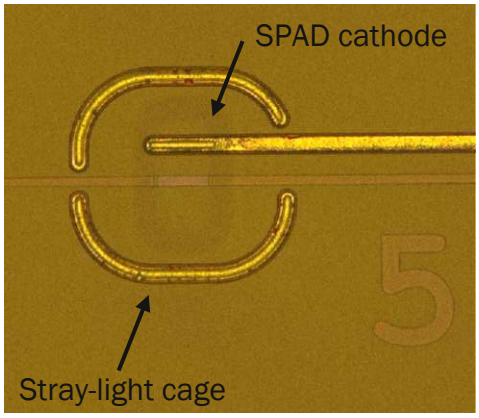


Figure 41: Microscopic image of an integrated SPAD in the PIC.

Layout

The layout of the ASIC for gating external SPADs is specifically designed to wire bond nine external SPADs to the output pads. The layout blocks, which are described in 2.2.2, are mainly identical to the internal Gater blocks.

Due to the absence of integrated photodiodes, a strongly negative substrate bias voltage and a low epi substrate are not required. The substrate bias needs to be at V_{ss},(-7.35 V) the lowest voltage on the chip. Therefore, strong isolation with rounded deep n-wells and higher distances between deep n-wells is not necessary. To have the possibility to use the same substrate pad for the external SPADs and the eternal Gater, the ASIC is nevertheless designed to withstand a very negative substrate voltage if produced on a low-epi wafer. Consequently, the Gater ASIC for external SPADs works on both types of wafers (standard and low-epi). This makes the dicing of the wafers easier, because the height matches the internal Gater dimensions and only one dicing step is necessary, as shown in the left dicing plan shown in Figure 24 (green). In this work only external Gater ASICs from low-epi wafers are used.

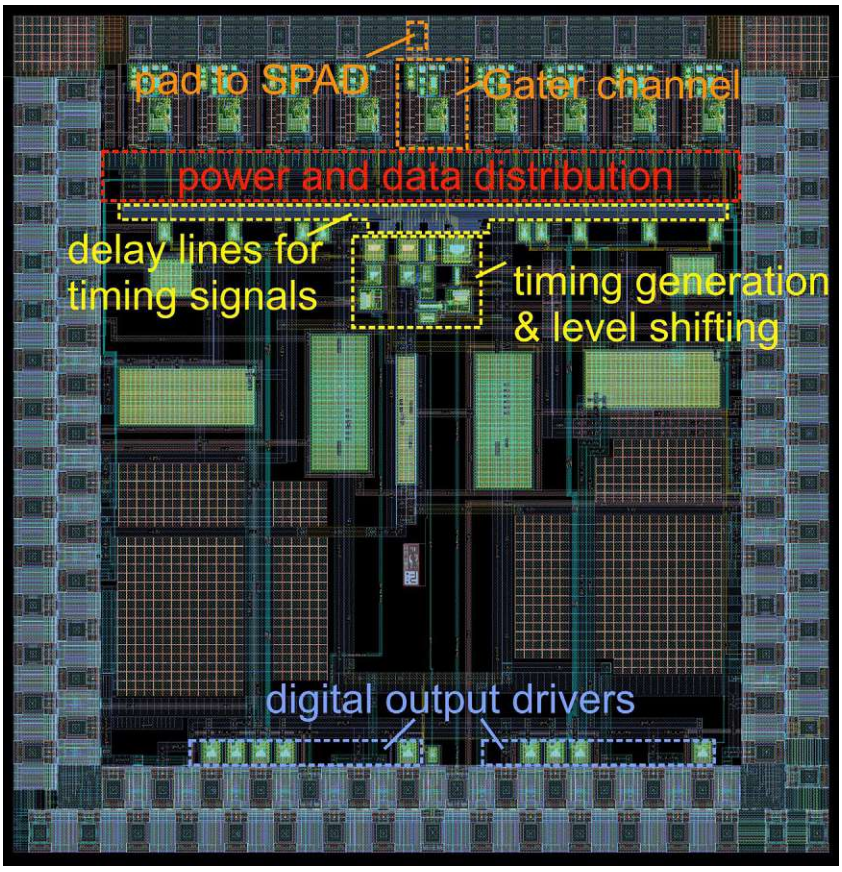


Figure 42: Layout of the Gater chip containing 9 synchronous channels for wire-bonding to 9 SPADs on the PIC (external Gater).

The layout of the complete MLM including the external Gater ASIC is shown in Figure 25. The external Gater ASIC has an area of about 3.1 mm × 3 mm and is shown in Figure 42. Although the general building blocks are the same, the external Gater is much smaller and has a different arrangement of the circuits. Theoretically the ASIC could be even smaller, by reducing the decoupling area. However, this would worsen the performance of the chip and violate the requirement of the bond pad pitch of the project partners (180 µm). An illustration of the chip dimensions is shown in Figure 43. The values are the exact decimal values of the layout design and do not include a remaining saw trench. The height after back-grinding of all ASICs is about 300 µm.

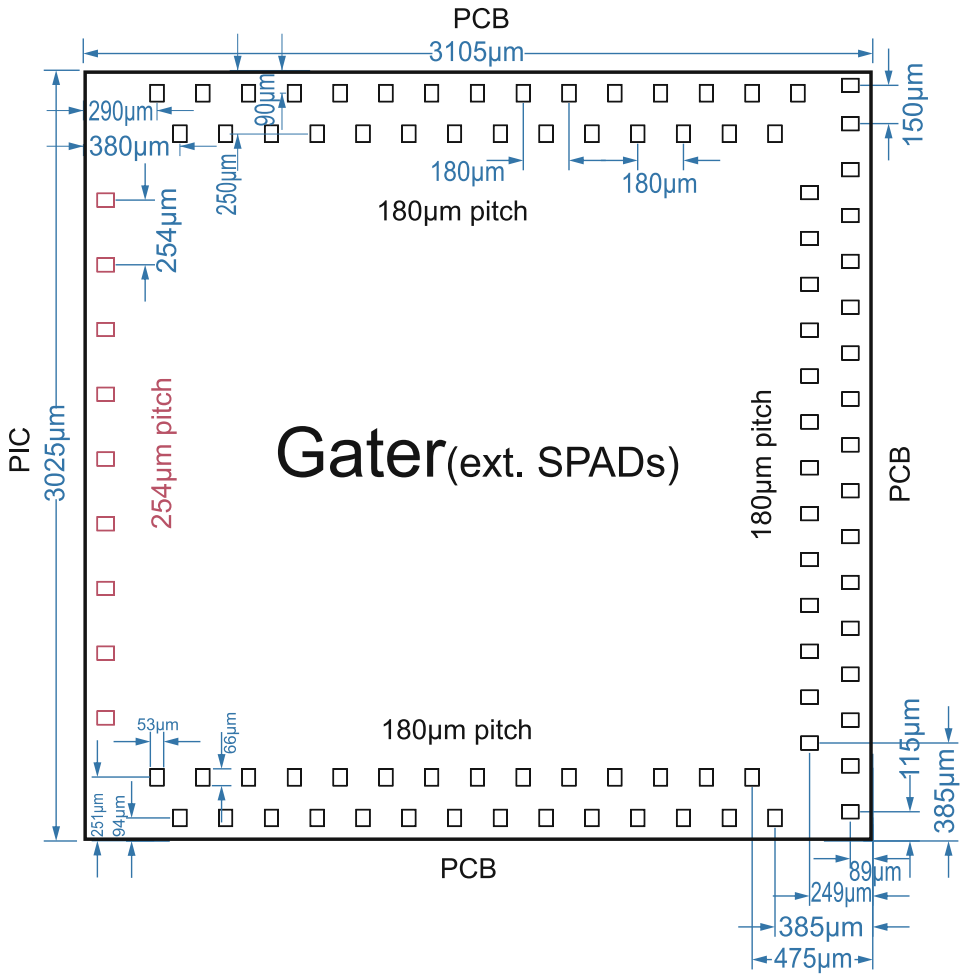


Figure 43: Dimensions of the Gater chip with external SPADs, outer dimensions whiteout saw trench (values rounded to µm).

The high capacitive load on the Gater output node causes high currents for charging and discharging the node every 12.5 ns (photon injection period of the quantum simulator). This requires much thicker metal tracks to the supply pads, the decoupling sections, and to the output pads. The connection to the output pad

is routed with a wide metal top track (METTP), which is thicker than the other metals and ensures the lowest possible parasitic capacitance, as well as the lowest serial inductive and resistive load.

Caused by fast and simultaneous switching across all channels, significant current peaks emerge. Consequently, large arrays of DMIM and MOS capacitors stabilise the various supply voltages. The MOS capacitors have higher area capacitance but are only available with a maximum voltage rating of 3.3V. More than 50 % of the chip area is used for decoupling. In comparison to the Gater with integrated SPADs, decoupling is much more important for the external Gater ASIC.

The pad layout is nearly identical to the one from the internal Gater, with four missing pads in the main padring and nine added pads for the SPADs. The two pads for the PIN photodiodes and the two ground pads are missing. The pitch of the pads to the PCB is 180 µm, only one pad at the corner has a pitch of 150 µm (red marked in drawings). All pads have a size of 53 µm x 66 µm. The pad layout is shown in Figure 44. In Figure 3 all different pads are listed with a short description.

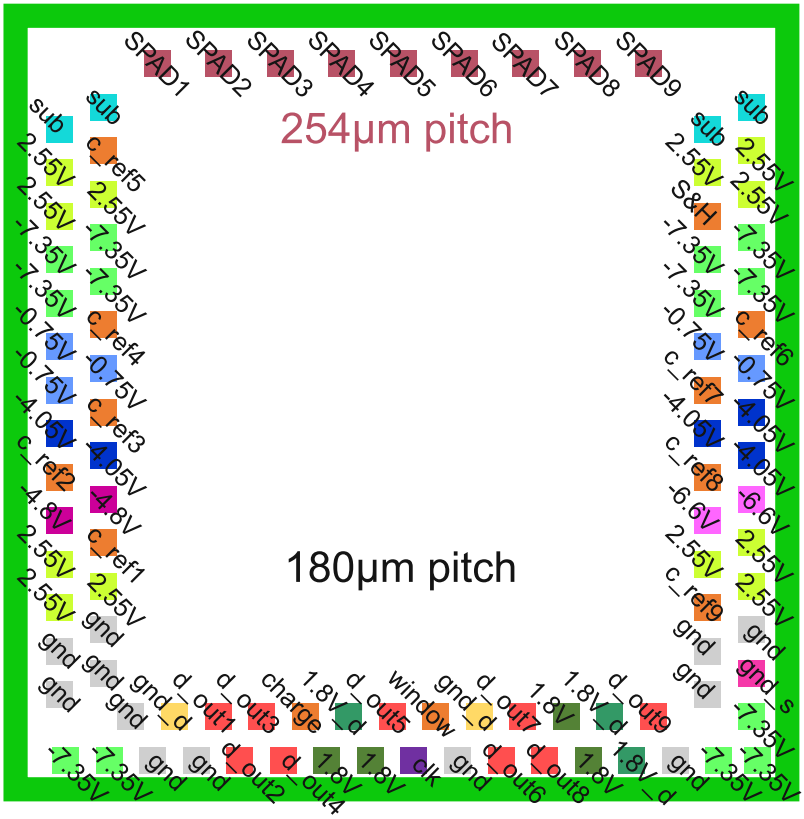


Figure 44: Pad layout of the Gater with wire bonded SPADs (external Gater).

Table 4: Description of the pads of the Gater for external SAPDs, including estimated voltage and current range.

connected to	pad name	description	type	voltage (range)
PCB	gnd_d	ground for digital output drivers	ground	0 V
PCB	gnd	ground for analog control circuits	ground	0 V
PCB	gnd_sh	shield ground connected to layer which shields substrate from -2.55V in padring	ground	0 V
PCB	1V8	1.8V for digital and analog control circuits	voltage supply	1.8 V
PCB	1.8V_d	1.8V for digital output drivers	voltage supply	1.8 V
PCB	2.55V	2.55V for the Gater switch	voltage supply	2.55 V
PCB	-0.75V	-0.75V for the Gater switch	voltage supply	-0.75 V
PCB	-4.05V	-4.05V for the Gater switch	voltage supply	-4.05 V
PCB	-7.35V	-7.35V for the Gater switch	voltage supply	-7.35 V
PCB	-4.8V	-4.8V for a control circuit	voltage supply	-4.8 V
PCB	-6.6V	-6.6V for a control circuit	voltage supply	-6.6 V
PCB	CLK	clock input which triggers with a delay the gating window and resets the comparator/digital output (80MHz)	clock	digital 0 V / 1.8 V
PCB	d_out1 ... d_out9	separate digital output from comparators of every channel	digital output	digital 0 V / 1.8 V
PCB	sub	substrate voltage of the Gater chip; same voltage as of the backside of the ASIC	voltage supply	≤ -7.35 V
PIC	SPAD1 ... SPAD9	Gater output; wire bond to cathode of external SPAD	SPAD connection	-7.35 V – 2.55 V
PCB	charge	determines the SPADs charging time; voltage which is applied at the pad generates a corresponding dc current out of the Pad	Bias	0 – 1 V (-1 – 0 mA)

PCB	window	determines the gating window duration; voltage which is applied at the pad generates a corresponding dc current out of the Pad	Bias	0 – 1 V (-1 – 0 mA)
PCB	S&H	bias voltage for sample and hold stages for all channels; determines indirect also the comparator threshold because it level shifts the comparator input voltage	Bias	0 – 1.8 V (no dc)

Figure 45 shows a microscopic image of the ASIC mounted on a printed circuit board (PCB). The U-shaped pad ring padas are wire bonded to the PCB and the Gater outputs are directly wire bonded to the cathode pads of the SAPAD array. A ball bonder was used to get the best bonding result.

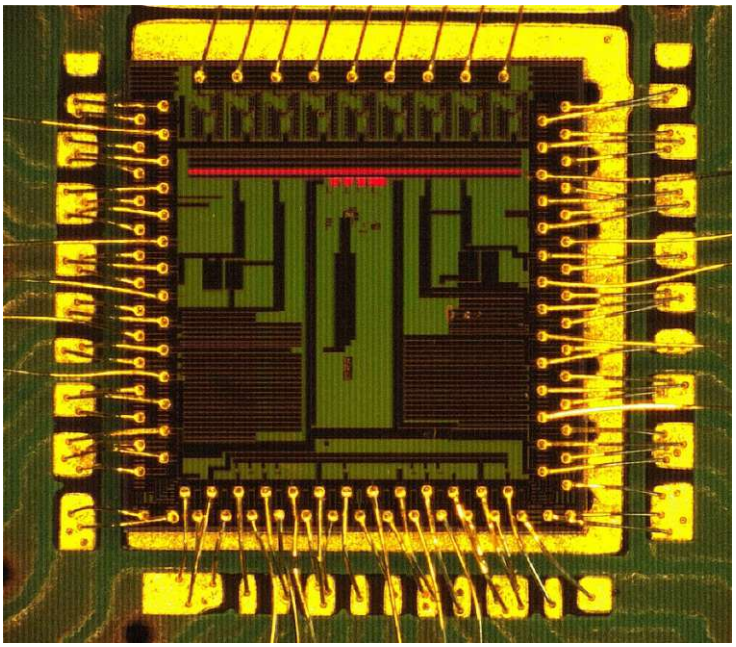


Figure 45: External Gater from ASIC run 1 glued and bonded to test-PCB.

2.3.2 Simulation and Measurement

As described in Section 1.2, the analog design flow was employed for the development of the Gater ASIC. Within the Cadence virtual testbench environment, the chip was connected with bond wire models and appropriate load conditions at the digital outputs. A design loop incorporating pre- and post-layout simulations was carried out, including DC, AC, and transient analyses, to ensure that all performance specifications were met and to optimise the physical layout. Furthermore, parameter sweeps and corner analyses (temperature, process) were

conducted to evaluate the design robustness under variations and to verify compliance with all defined requirements. To obtain external SPAD for testing, the PIC was sub-diced into a smaller chip containing only the SPADs, shown in Figure 46. The wide T-shaped metal tracks is power supply of the heaters used for the control of the phase shifter (see Chapter 3).

To test the Gater ASIC, a test-PCB was necessary. The same test-PCB design used for the internal Gater, described in Section 2.2.3, was used. The PCB and parts are already designed for the higher currents from the external Gater. The layout of the test-PCB with 6 layers and FR4 substrate is shown in Figure 26. This was realised with a gap in the substrate pad, which makes a substrate split for the external SPADs possible.

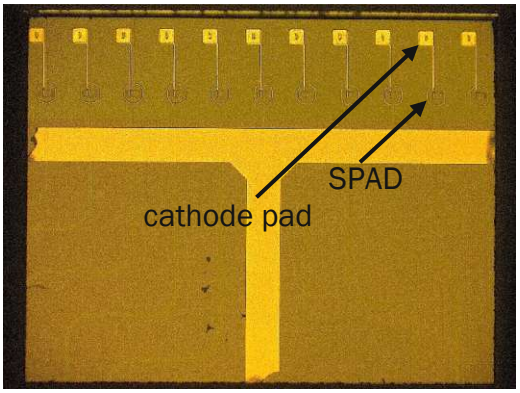


Figure 46: Sub-diced PIC with 11 integrated SPADs.

One critical parameter is the actual capacitance of the SPAD cathode note on the PIC. The capacitance of the external SPAD for different reverse voltages was measured to ensure that it behaves like it was simulated and can therefore be driven with the external gating ASIC. As mentioned before, the Gater was designed to drive an SPAD with a total node capacitance lower than 450 fF. The SPAD array, which was cut from the PIC, was glued to a gold pad of the test-PCB. The electrically conductive glue enables connecting the anodes of the SPADs, which are only connected to the backside contact of the chip. Two needs were placed, one on the gold pad where the array was glued and the other on the corresponding cathode pad. The chip temperature was actively regulated to 25 °C. The LCR meter Agilent 4284A was used to determine the parallel capacitance (R_p-C_p mode). A reverse bias voltage sweep was performed with amplitude of 1 V at 1 MHz, which is the maximum measurement frequency of the LCR metre. Prior to measurement, the cathode needle is lifted to calibrate the device with an open structure. This

workflow was chosen because no open or short structure was available. Figure 47 presents the measured capacitance of two external SPADs for different reverse voltages. The two SAPDs behave very similar, like all other SPADs on the array. Considering that the breakdown voltage is approximately -34 V and the applied reverse voltage is therefore consistently at or below 34 V, the effective capacitance can be assumed to be less than 300 fF. This value matches with design expectations and falls within the target range for which the ASIC was developed.

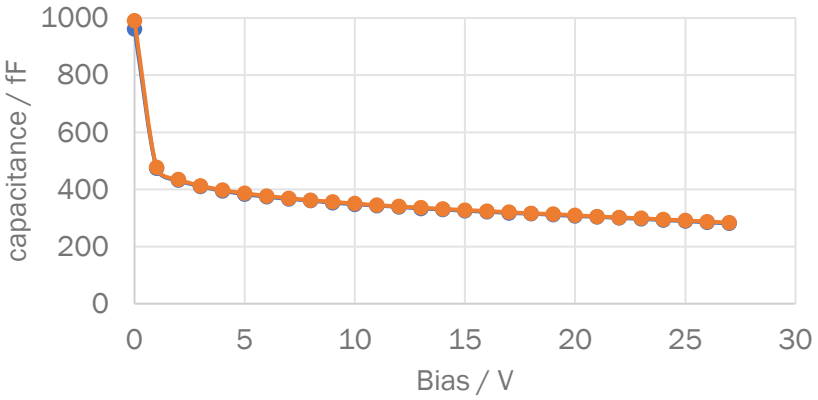


Figure 47: Measured capacitance of the external SPAD for different reverse voltages.

A fully assembled test-PCB with a glued Gater ASIC and a glued sub-diced PIC to the conductive gold pads, as well as soldered parts ready for characterisation, is shown in Figure 48. It is clearly visible that the PIC is much higher than the thinned Gater ASIC. The advantage of the thinned Gater is that the supply bond wires are shorter and therefore the parasitic inductance is smaller.

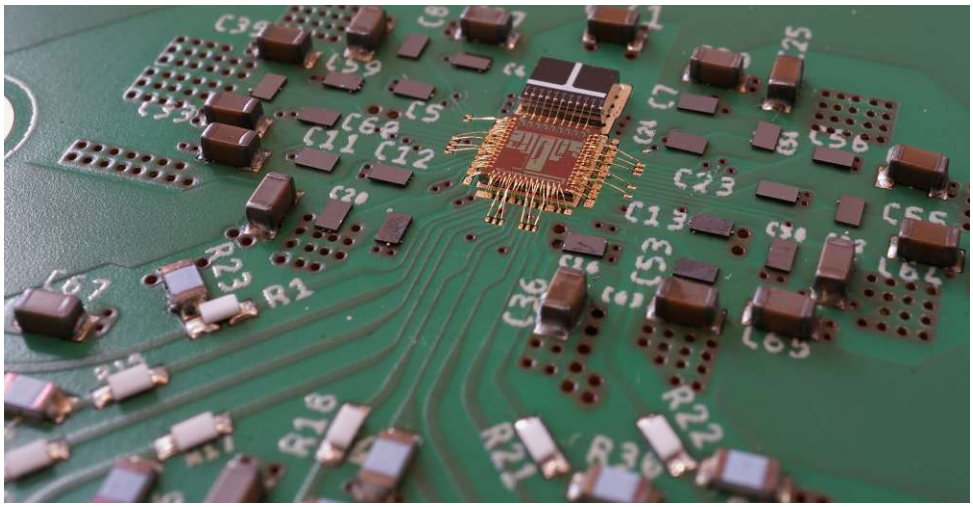


Figure 48: Glued external Gater and sub-diced PIC on the assembled test-PCB

Measurements

For measuring the dark count rate (DCR), afterpulsing probability (APP), and photon detection probability (PDP), the same measurement setup used to characterise the internal Gater is utilised. The measurement setup is based on the configuration described in [61] and is illustrated in Figure 28. The PCB with the Gater ASIC, placed inside the dark box, is shown in Figure 49. The optical power metre is shown on the left side of the picture. A camera on the right side helps to place the fibre in the approximate position before the XYZ stage moves the fibre, and the LabVIEW software can find the optimum positioning. To ensure that all PN junctions of the deep n-wells are reverse biased, the Gater ASIC substrate is set to – 10 V and the substrate of the SPAD is independently swept.

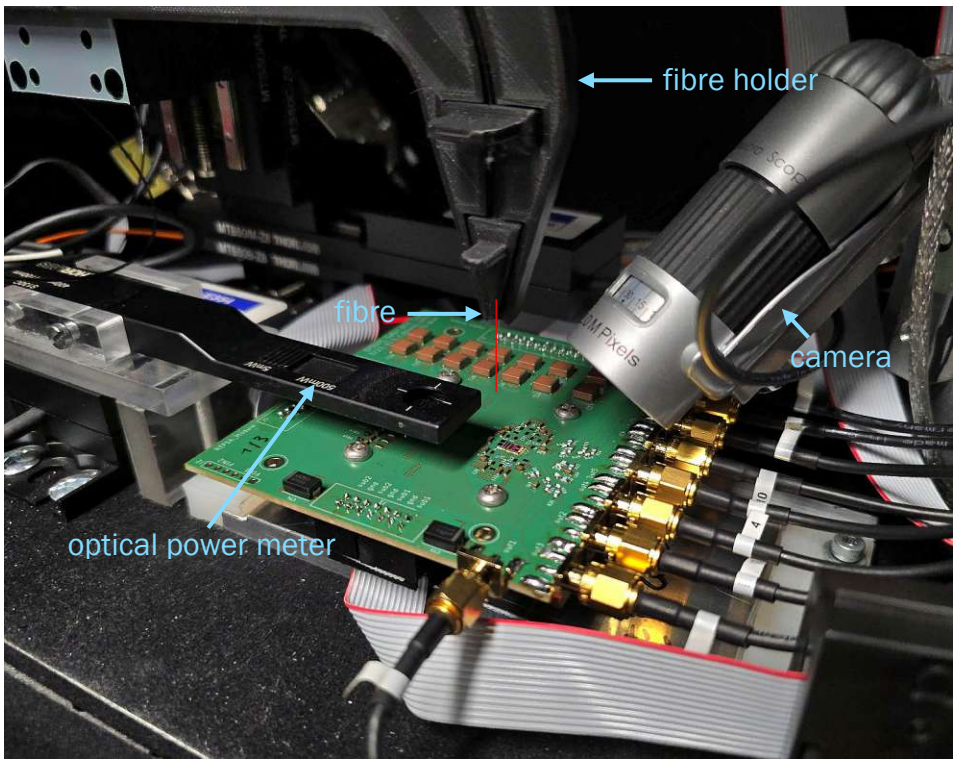


Figure 49: External Gater with PIC SPADs bonded to a test-PCB with fibre on XYZ stage in a dark box.

The ASIC and the sub-diced PIC are regulated to room temperature (22 °C). During the measurements, the gating window was set to approximately 7.5 ns. The reference voltage was individually optimised for each SPAD channel, while the substrate voltage V_{sub} was swept from –26 V to –34 V to evaluate performance across biasing conditions. The dark count rate (DCR) and afterpulsing probability (APP) were measured under dark conditions with the laser source deactivated. The reference voltage (V_{ref} = compare ref.) of each channel was tuned to ensure

optimal performance. The dark count rate is shown in Figure 50 for all nine channels depending on the substrate voltage of the SPAD chip (anode). Channel 9 seems to be a screamer with a significantly higher DCR compared to the other channels. The dark count rate in the range 10 to 100 counts per second is extremely low.

Different gating frequencies (repetition rate of the gating window) are measured to test the impact of a longer death time. Figure 52 and Figure 53 show the DCR and APP, respectively, at different gating frequencies depending on the substrate voltage for channel 1 at room temperature (22 °C). It shows that the APP is 0.24 % at 20 MHz clock and 8.5 V excess bias voltage. However, at 40 and 80 MHz the APP increases to 10.74 and 84.25 %, respectively. Cooling the device could reduce the DCR significantly [60]. The breakdown voltage across the channels, excluding channel 8, shows a variation of less than 1 V, indicating good process uniformity.

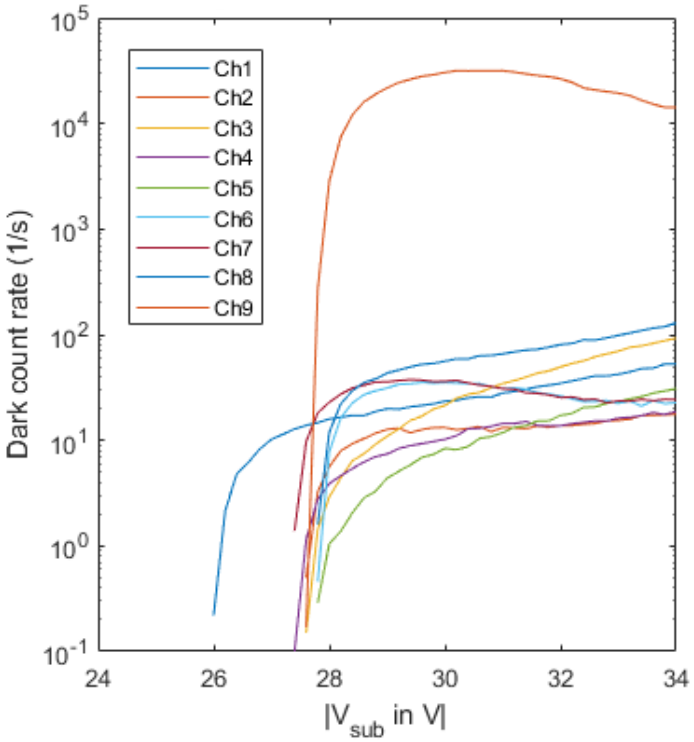


Figure 50: Extracted dark count rate (DCR) and afterpulsing probability (APP) at 40 MHz depending on the substrate voltage for all nine channels of the external Gater at room temperature (22 °C).

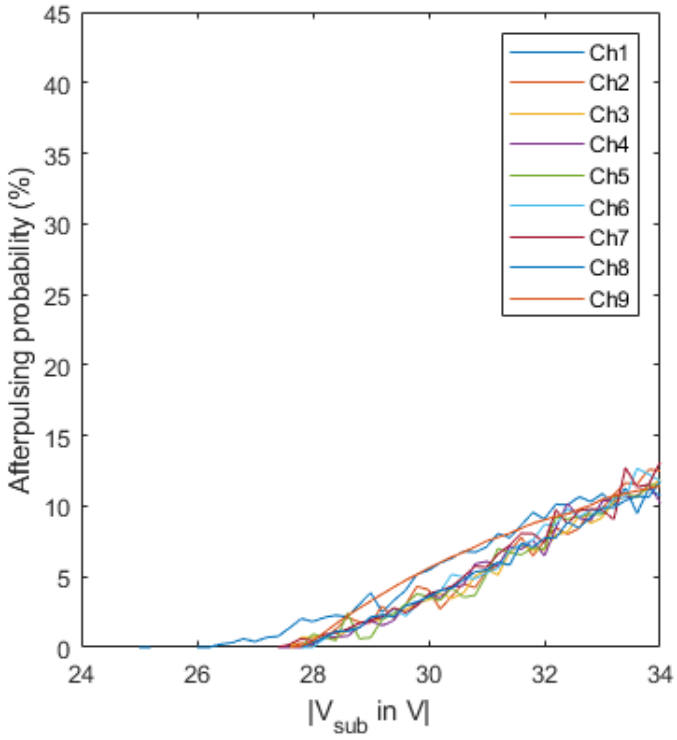


Figure 51: Extracted afterpulsing probability (APP) at 40 MHz depending on the substrate voltage for all nine channels of the external Gater at room temperature (22 °C).

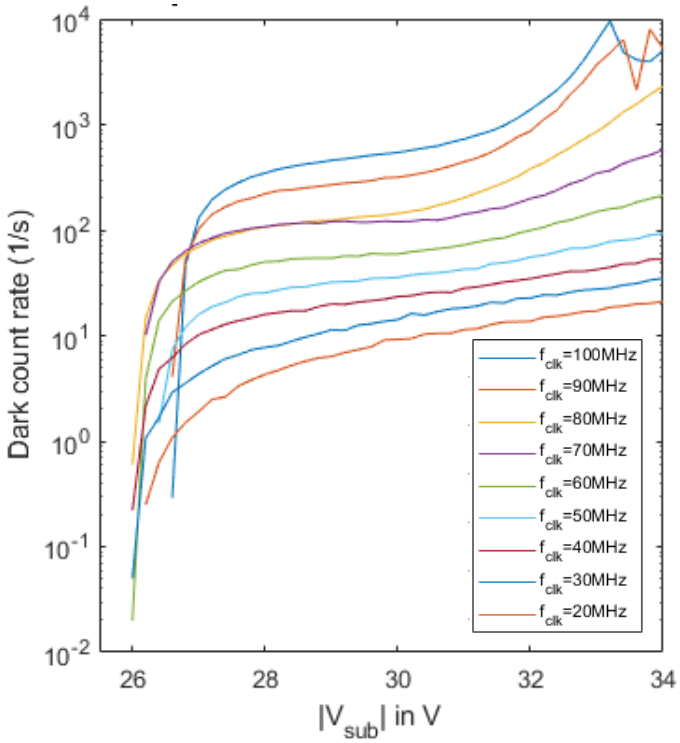


Figure 52: Extracted Dark count rate (DCR) at different gating frequencies depending on the substrate voltage for channel 1 of the external Gater at room temperature (22 °C)

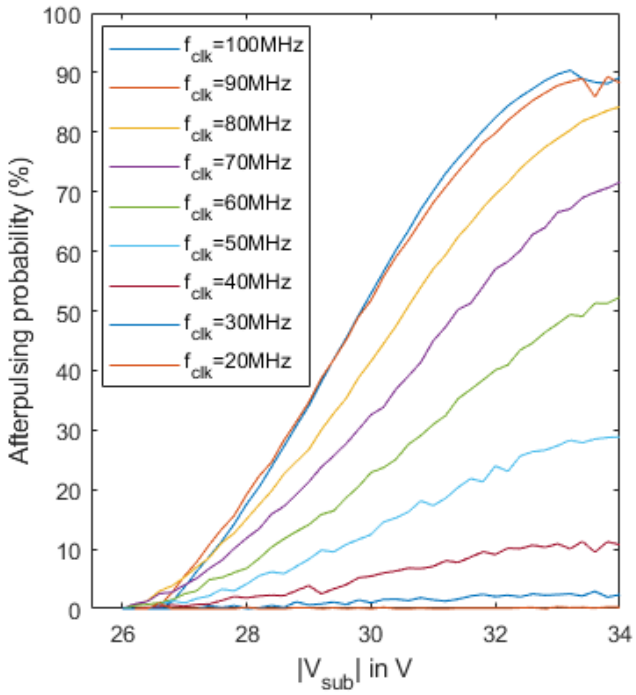


Figure 53: Extracted afterpulsing probability (APP) at different gating frequencies depending on the substrate voltage for channel 1 of the external Gater at room temperature (22 °C)

The photon detection probability (PDP) for a gating frequency of 20 MHz is shown in Figure 54. A custom-built, fibre-coupled laser source on a XYZ stage emitting light with a wavelength of 635 nm was used for optical characterisation. The laser is externally modulated using an electro-optic modulator (AM635, Jenoptik). Because of the availability of a high-speed light source with a high extinction ratio, the PDP was only measured at this wavelength. The measured extinction ratio during the experiments was approximately 100. The laser was modulated with 3 ns optical pulses at a repetition rate of 20 MHz, which is identical to the gating frequency. The gating window was in the range of 7 ns and shifted with the clock input to algin with the arrival of the optical pulses at the SPADs. Due to the limited extinction ratio, the measured optical power comprises contributions from both the pulse and inter-pulse intervals. Consequently, the instantaneous optical power during the pulse is overestimated, resulting in an underestimation of the photon detection probability (PDP). Therefore, the actual PDP of the SPADs is slightly higher than the calculated value. For PDP characterisation, the average photon arrival rate was set at 405,000 photons per second. The PDP is really high with 65 to 75 % for the highest excess bias. Internal power measurement with the

custom voltage supply showed that the external Gater has a mean power dissipation of less than 250 mW as expected.

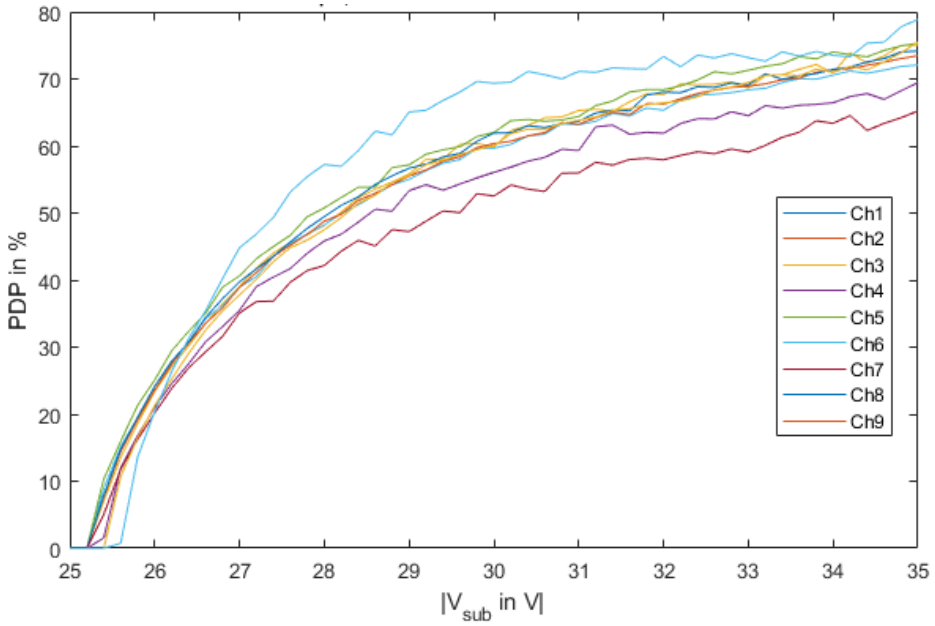


Figure 54: Photon detection probability (PDP) depending on the substrate voltage for all nine channels of the external Gater at room temperature (22 °C) and at a photon rate of ~405,000 photons/s with 635 nm laser source.

In contrast to the Gater with integrated SPADs, the bonding pads enable transient measurement of the cathode voltage. A second measurement setup, shown in Figure 55 was used to capture the voltage. The setup is controlled by a PXI-based system from National Instruments (NI), which includes the NI PXIe-1062Q chassis and the embedded controller NI PXIe-8133. It includes a pulse generator (Agilent 81134A) and two programmable power supply units.

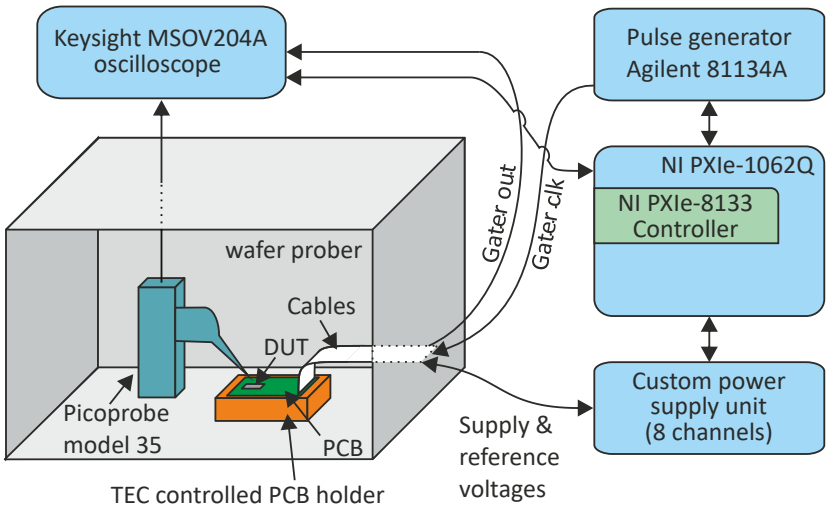


Figure 55: Experimental setup employed for transient characterisation of Gater for external SPADs.

The transient voltage at the cathode was measured with the Picoprobe model 35 and a 20 GHz oscilloscope (Keysight MSOV204A) in a wafer prober (Karl Suss PA 200), as shown in Figure 56. The Picoprobe is a microwave probe specifically designed for on-wafer testing with an input frequency range of up to 26 GHz. Only about 0.05 pF capacitance is added to the tested pad and has a high input resistance of 1.25 MΩ [66].

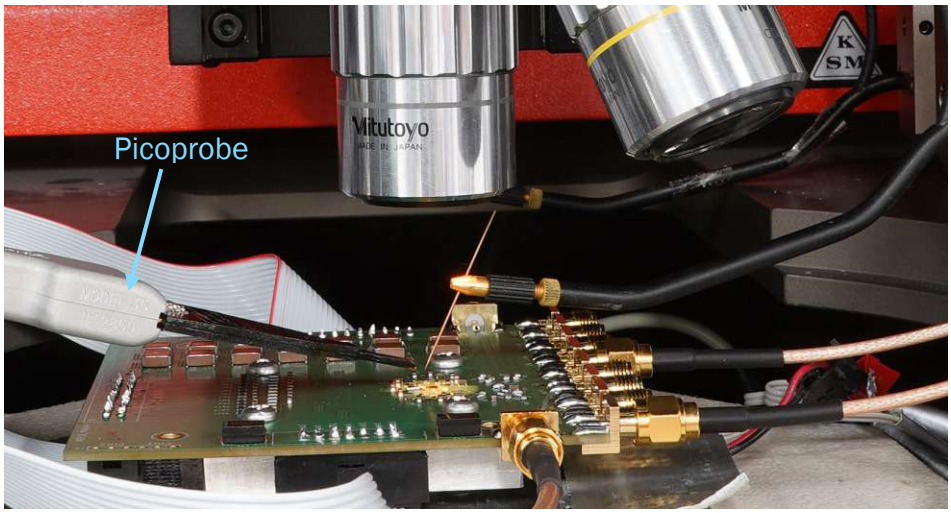


Figure 56: Transient measurements with the Picoprob on the wafer prober.

This approach ensures that the measured transient voltage is as unaffected by external loads as possible. The point radius of the Picoprobe tip is smaller than 2 µm, which makes the placement on the already bonded pad possible, shown in the microscopic image in Figure 57. A different sample (Gater and SPAD) was used because the measurements needed to be performed in parallel to speed up the measurements.

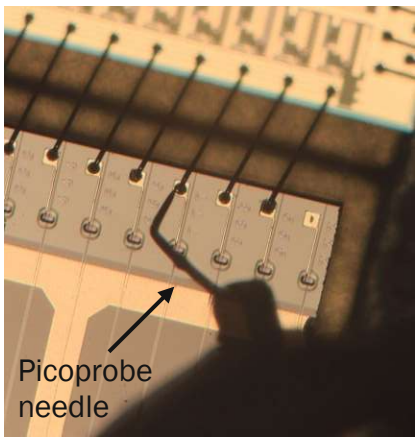


Figure 57: Placed Picoprobe tip on the cathode pad of the PIC SPAD.

The discharge caused by an avalanche (in that case a dark count in the first gating window) and the charge (reset) from the Gater are shown in Figure 58. To capture

this rare event, the oscilloscope triggers the digital output of the Gater, which indicates an avalanche event at the SPAD. In some cases, there is also a discharge in the second gate window, which can be caused by another dark count or afterpulsing. With increasing substrate voltage and, thus, higher excess bias, the discharge through an avalanche happens faster and faster. The SPAD discharges itself at an excess bias of about 9.5 V within 1 ns by about 3 V

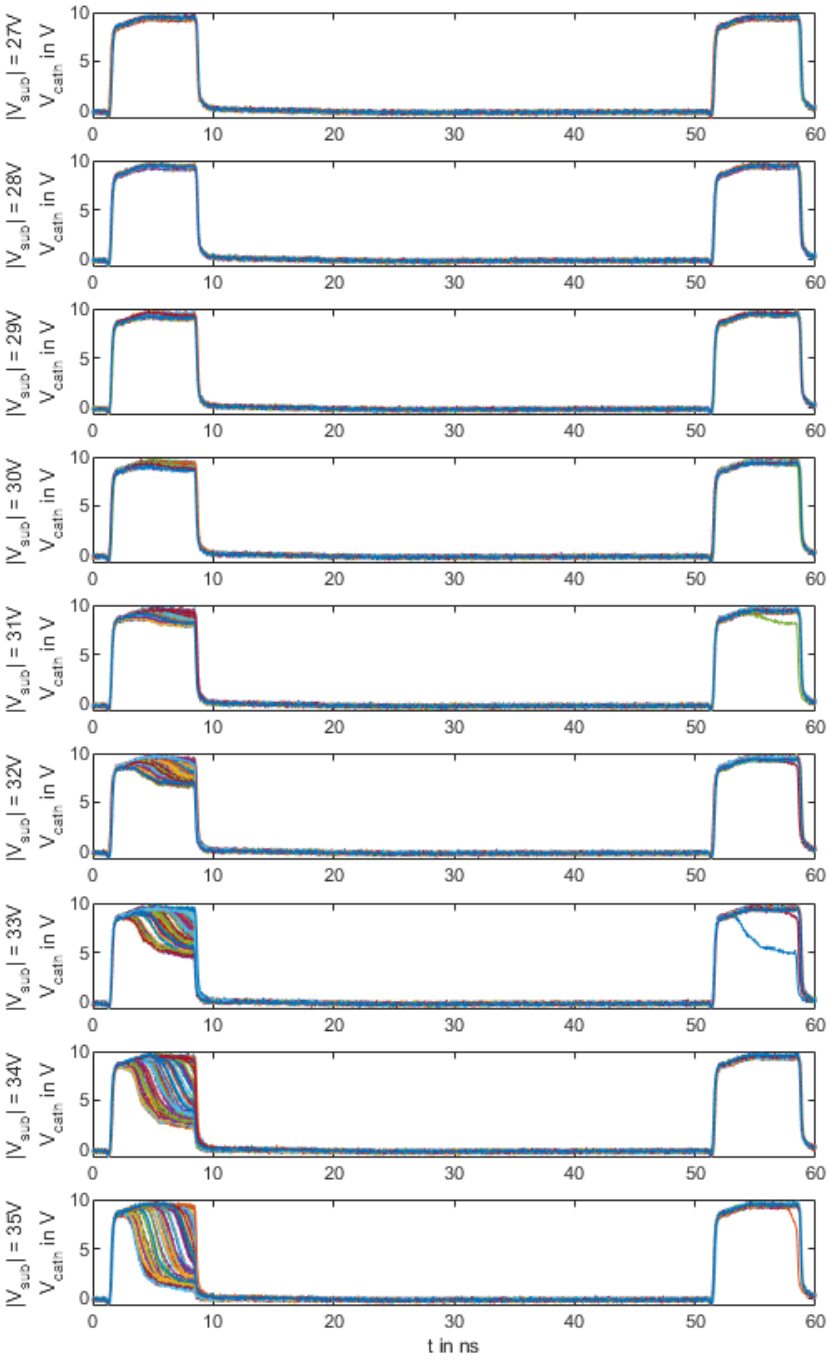


Figure 58: Measured transient voltage on one PIC SPAD connected to the external Gater depending on the substrate voltage (excess bias from about 1.5 V to 9.5 V) for 100 dark counts.

Comparison and conclusion:

The results of the SPAD integrated into the PIC with the external Gater ASIC are promising for the complete quantum simulator. The dark count rate in the range of 10 to 100 counts per second is extremely low, and the PDP in the range of 70 % is very high. Parameters are significantly better compared to the SPAD in 0.18µm X-FAB CMOS. Nevertheless, the results showed that the APP is too high for gating frequencies above 40 MHz to be used for the quantum simulator. Consequently, the photon rate of the quantum simulator needs to be reduced or the SPADs of the PIC need a redesign to improve this behaviour. At the moment, a new PIC with improved SPADs, which should reduce the APP, is produced but is not characterised. Cooling the chip to lower temperatures would help to reach a even lower DCR but would further increase the APP.

2.3.3 Second Run and Outlook

For flip chipping (3D integration) the external Gater onto the PIC, the layout was modified for the second production run, described in Section 2.2.4. The layout of the entire reticle for the second run, including the Gater for external SPADs, is shown in Figure 37. The external Gater height matches the internal Gater height to make dicing easier, as shown in dicing plan B in Figure 38.

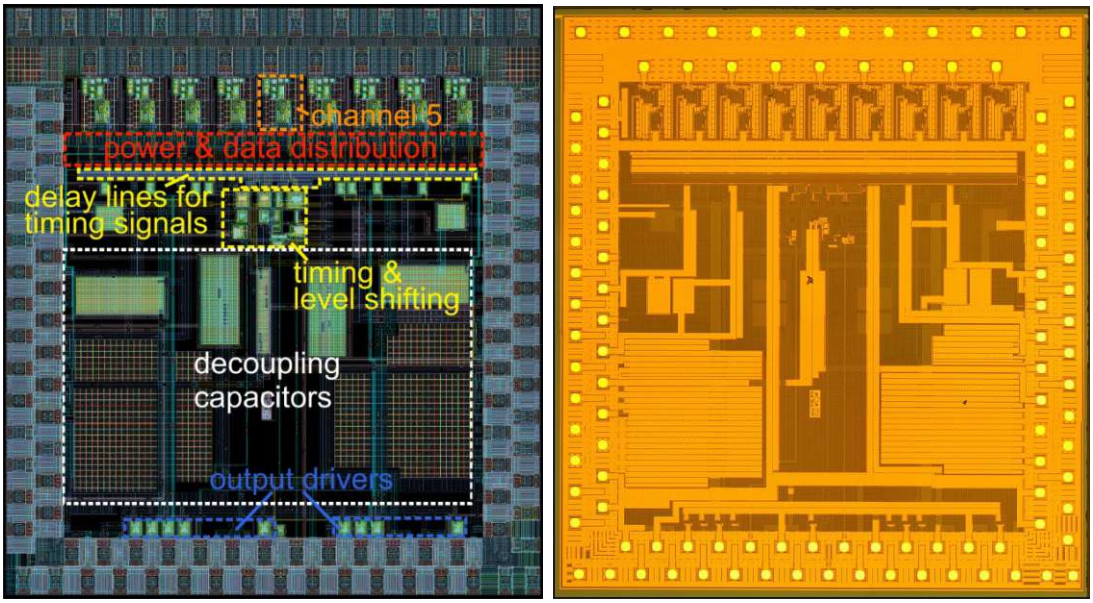


Figure 59: Layout (left) and a stitched microscopic image (right) of the Gater chip containing 9 synchronous channels for flip chip bonding to 9 SPADs on the PIC.

The layout of the external Gater ASIC for flip-chipping to the PIC is shown on the left side in Figure 59. The ASIC got a second bond pad row on all sides, to match the flip-chip process requirement of an equal pad density on all sides. The dual row pad layout around the ASIC is more uniform than the pad layout of the internal Gater, which has no pads on one side. Therefore, the 3D integration of the external Gater with the PIC will have a higher success rate. For flip-chipping, the passivation opening of the pads is circular shaped. A Gater channel with dual pad layout is shown in Figure 60.

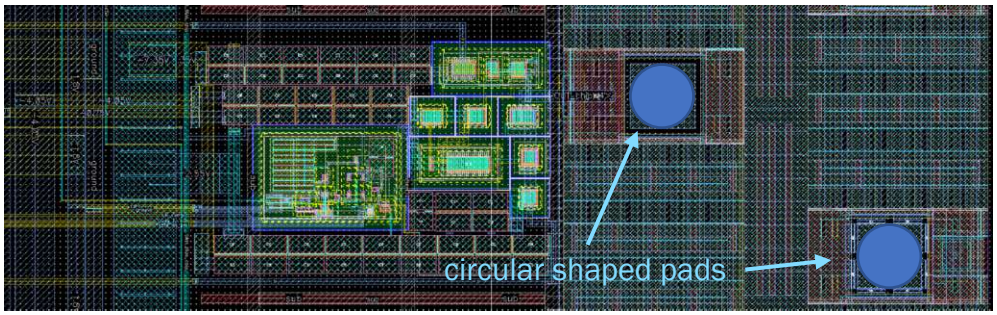


Figure 60: Layout of a Gater channel with circular shaped pads.

A microscopic image of the diced external Gater from run 2 is sown on the right side in Figure 59. To test the ASIC, the test-PCB, described in 2.2.4 and shown in Figure 39, is used. It can host an internal Gater or an external Gater with a dedicated SPAD chip. This was again achieved with a gap in the substrate pad to split the substrate for the external SPAD chip. The diced ASICs from the second production run have already arrived and are pending to be characterised at the moment of writing this dissertation.

Longer gating windows in the range of serval 10 ns would help to characterise externals SPADs mor easily and could be an improvement for a possible next run. Therefore, an additional active quenching would also be desirable, as described in Section 2.2.4.

3. Temperature Control of Phase Shifters

This Section is based on my work published in the peer reviewed paper [67] as well as (confidential) reports and internal documentation within the EPIQUS project.

As described in chapter 1 and shown in Figure 1 the quantum simulator needs programmable phase shifters in the manipulation stage. Thay are used in the arms of interferometres built from integrated waveguides [6]. This enables the routing of single photons (qubits) along distinct optical paths, thereby forming sequences of quantum logic gates that function analogously to transistors in electronic integrated circuit circuits [10].

The phase shift in an optical waveguide can be adjusted using several methods, typically involving changes in the effective refractive index. Also, changes in waveguide dimensions (width, thickness, bending radius) influence the mode propagation constants, altering the phase shift. These geometrical changes to alter the phase shift could be programmable via MEMS-based waveguide geometry tuning [68], but are complex and cannot be integrated into the available PIC platform. Altering the reflective index by material-based changes (doping, compositional engineering) is, of course, possible, but not programmable. Physical effects, like the thermo-optic effect, the electro-optic (Pockels) effect and dependence on the density of free carriers (Carrier Injection/Depletion) can be used to dynamically controlled the reflective index [7], [69], [70].

The thermo-optic effect refers to the dependence of a material's refractive index on temperature. Integrated heaters, composed of resistive elements, are employed to precisely control the waveguide temperature. To induce localised changes in the refractive index, electrical power is applied to these resistive heaters positioned near the targeted waveguide regions. This technique is used in the quantum simulator. Small heaters, made of titanium nitride (TiN) above silicon oxynitride (SiON) waveguides are used to heat the waveguide underneath it, shown in Figure 61. These tiny micro heater units allow one to reconfigure the manipulation stage of the quantum simulator [10].

Despite the disadvantages that the thermo-optic effect is slow and has higher power consumption, it is commonly used in integrated photonics because it can

be efficiently integrated and has low optical losses. The relatively slow response time, due to thermal time constants (microseconds to milliseconds), is insignificant for the quantum simulator, because the phase shift must be changed only for different configurations and to compensate process fluctuations, where the reaction time is sufficient. Thermal crosstalk and self-heating of the complete system can also be a problem. Therefore, an external temperature regulation is needed and the crosstalk between the heaters needs to be reduced. Deep trenches were investigated to thermally isolate the integrated heating resistor and its associated phase shifter (as illustrated in Figure 61) from the rest of the chip. The trenches reduce the necessary local temperature at the resistors required to achieve a given temperature at the waveguides underneath, leading to lower temperature of the TiN heaters and a more linear resistance over heating power. This approach effectively reduces the necessary heating power for each waveguide arm and, therefore, minimises overall heat dissipation. Consequently, it significantly enhances device performance by decreasing the cooling demands and minimising thermal crosstalk between close phase shifters. About 70 mW of heating power is required to obtain a phase shift of π with trenches compared to 105 mW without. Consequently, the ASIC controlling the heaters must have the power to drive at least 70 mW per channel. The ASIC is designed to deliver a minimum of 105 mW of power due to the absence of tranches in the initial design iterations.

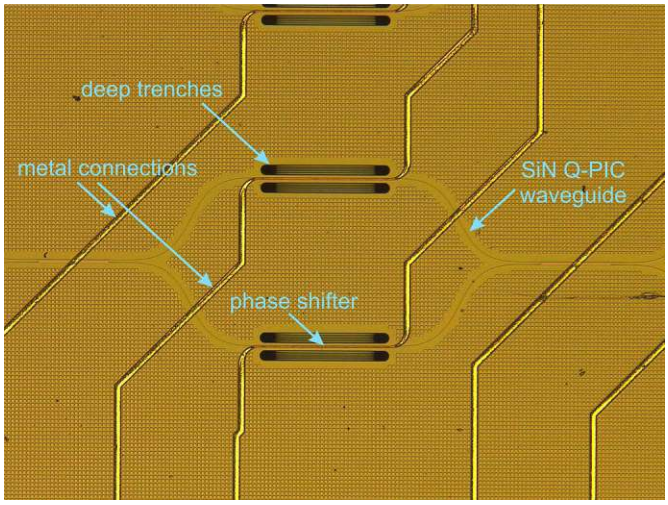


Figure 61: Microscopic image of phase shifters with heating resistors and SiN Q-PIC waveguides.

Measurements showed that the resistance of TiN heaters changes over temperature from 703 Ω (0 W) to 832 Ω (117.8 mW). The heater reaches the

maximum heating power consumption of 117,8 mW if 9.9 V are constantly applied.

Scaling the photonic quantum simulator to accommodate a higher photon count inherently leads to an increased number of programmable phase shifters, thereby necessitating control circuitry that is both efficient and scalable. The easiest way to regulate the power of a resistor is to apply a constant (in time) current or voltage. Depending on the amount of power, this results in significant power dissipation within the control ASIC, producing unwanted heat that can adversely affect both the intended phase shift and overall chip cooling requirements. The power dissipation in a linear regulator is highly dependent on the heating power required by the resistor [71]. Especially for the second run, where 3D integration (flip-chipping) should be employed, this approach would not be suitable. A pulsed operation, where the voltage is switched on only for a defined interval, ideally reduces these regulator losses to zero, as either current or voltage across the control circuit is momentarily absent. Although practical implementations cannot completely eliminate losses, this approach significantly reduces power dissipation compared to continuous voltage or current methods. In practical implementations involving MOSFETs, the on-resistance results in a small voltage across the transistor during the conductive state. Additionally, the unavoidable charging and discharging of the parasitic capacitances of the metal traces and resistors introduce further power dissipation. Nevertheless, theoretical analyses and complete circuit simulations showed that, despite these non-idealities, a PWM-based control significantly reduces power dissipation in comparison to linear regulator approaches (depending on the load capacitance). [7] demonstrated that employing PWM techniques for heater resistors can substantially decrease controller power losses.

It is important to keep the parasitic capacitive load of the pads and the tracs as low as possible. The charging/discharging losses every PWM cycle

$$E_{charge\_cycle} = \frac{1}{2} * C_{load} * U^2 \qquad 7$$

increase linearly proportional to the capacitance and quadratically proportional to the voltage. Accordingly, it is advisable to maintain the voltage at the lowest practical level with respect to parasitic capacitance and ohmic losses. Increasing the PWM frequency increases the losses. Figure 62 shows a theoretical

comparison of charging/discharging losses with a PWM approach assuming the expected maximum capacitive load of 0.75 pF and of the losses of a constant (in time) voltage/current regulator. The theoretical power saving of a PWM compared to a constant current/voltage regulator is up to a factor of 11. With a higher capacitance, the losses for the PWM regulator would shift horizontally to higher values. [67]

The capacitance to a stable net (e.g. ground) on the power supply side of the resistor needs to be as high as possible to enable a stable voltage and therefore power of the resistor despite the pulsed PWM current. Another important parameter is the series inductance of the hole loop from the power supply (or capacitors) to the resistor, from the resistor to the ASIC and from the ASIC back to the supply (or capacitors).

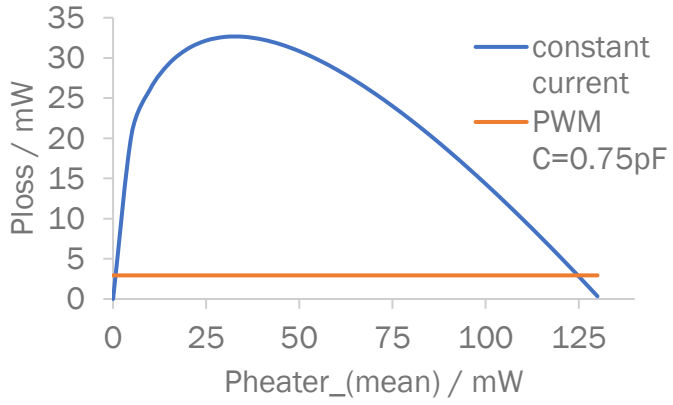


Figure 62: Theoretical power losses in the driver for constant voltage/current heating and pulse-width modulation (PWM) heating, assuming a 750 Ω heating resistor. The comparison excludes the effects of control circuitry, level shifters and neglects the on-resistance of the PWM switching element. Source: [67]

3.1 Multi-channel PWM ASIC

In this work, pulse width modulation (PWM), synchronised to the photon source, is utilised to efficiently control the temperature. The duration of the constant voltage pulses applied to the resistor is directly proportional to the heating power. By adjusting the on-time of the voltage within each period, the average power delivered to the heater can be precisely controlled. This ratio of on-time to the total period is referred to as the duty cycle, expressed as a percentage. Lower duty cycles correspond to lower heating powers.

To ensure stable thermal behaviour, the PWM period must be significantly shorter than the thermal time constant of the system, thereby limiting temperature fluctuations caused by switching. Furthermore, the PWM signal is synchronised to the laser source of the quantum simulator. This synchronisation provides a distinct advantage over previously reported free-running PWM approaches [7]. The synchronisation ensures that even a small temperature ripple does not affect the phase shift because the temperature is always at the same level when a photon is present. To reduce and spread supply voltage spikes caused by bond wires and other parasitic inductances, the individual PWM channels on each ASIC are delayed across the PWM period. Despite this delay, each channel has a constant phase relationship to the laser clock. The circuits are optimised for a PWM period of approximately 12.5 ns (80 MHz), matching the specified laser clock frequency of the quantum simulator. A PWM clock of up to 300 MHz would be feasible with slight adoption in the bias distribution.

Due to requirements, the width of the metal traces on the PIC was limited. Since electrical power is the product of current and voltage, maximising the voltage allows the current to be minimised for a given power level, thereby reducing ohmic losses in the metal interconnects. These metal lines must remain narrow to limit parasitic capacitance and support high-frequency switching. Achieving rapid voltage transitions is essential to minimise power dissipation during switching. This requires high-speed MOSFETs that have a limited voltage swing in the CMOS process. The proposed circuit architecture achieves a 9.9 V voltage swing, significantly lowering the current and associated resistive losses in the metal tracks to the heating resistors. The circuits are designed in the X-FAB XH018 presented in Chapter 1.2 and employ double cascoding using 3.3 V transistors. This design enables the realisation of a 40 channel PWM driver capable of operating at 80 MHz. The available high voltage MOSFETs in the process are too slow and need a large gate voltage, which mitigates their advantage of having a single MOSFET instead of three 3.3 V cascoded MOSFETs at the output. To my knowledge, this is the first PWM chip that utilises double cascoding while delivering a 9.9 V output at such a high switching frequency.

The circuit is split into four identical PWM ASICs as shown in the configuration in Figure 2 and Figure 3 to reduce the length of the metal track and reduce costs. A single ASIC would exceed the production costs available in this project.

3.1.1 Circuit and Chip Design

Figure 63 presents a simplified block diagram of the PWM ASIC. The architecture comprises an address decoder and 40 independent PWM channels (orange). Each channel incorporates a shift register stage SR (green), a data processing unit (blue), a PWM generation and adjustment unit (red), a double cascoded driver stage (yellow), and a delay block. Additionally, the chip integrates eight transimpedance amplifier (TIA) channels for real-time monitoring of optical power levels in waveguides on the photonic integrated circuit (PIC), supporting closed-loop control and diagnostics.

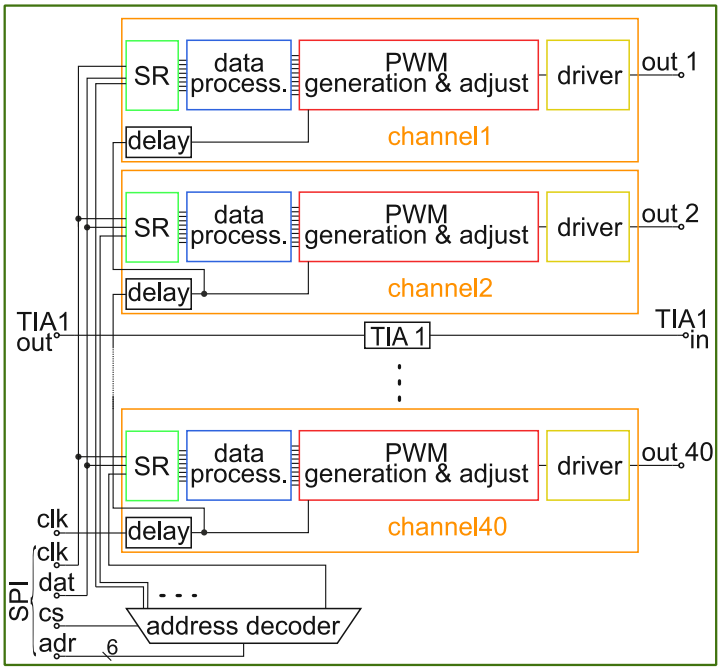


Figure 63: Simplified block diagram of the PWM ASIC. Source: [67]

The circuit is implemented using 1.8 V and 3.3 V MOSFETs. High-voltage 3.3 V transistors are used within the driver stages to achieve a voltage swing of 9.9 V at the heating resistors, effectively reducing current and associated line losses. In contrast, the remaining logic and control blocks utilise 1.8 V transistors to optimise switching speed and minimise overall power consumption. To minimise simultaneous switching events and thereby reduce supply noise, the PWM clock signal is intentionally delayed incrementally across the channels. These short delays help to distribute switching activity uniformly throughout the PWM period. The fixed internal delays are optimised to a PWM base block of 12.5 ns.

The circuit also incorporates two externally supplied bias voltages to tune the PWM signal generation, allowing for compensation of process and temperature variations and enabling adaptation to different base frequencies. The charge bias voltage (V_{charge}) controls the rate at which the average heating power increases with rising digital input values. The shift bias voltage (V_{shift}) provides a global offset, shifting the mean heating power level downward or upward for all digital input values.

The address decoder integrated into the SPI interface has six address bits to pick one of the 40 available PWM channels. The SPI interface itself consists of a serial data (dat), a clock (clk), and a chip select (cs) input. Each channel can be individually configured via the SPI by transmitting a 9-bit digital value, corresponding to a heating power, ranging from 0 to 511 (000000000 to 111111111) through the serial data input.

PWM generating and adjusting circuit

Each of the 40 PWM channels has a separate PWM generation unit based on a delay line architecture [72], [73], [74]. Figure 65 illustrates the adaptation of this principle for application within the quantum simulator. In this design, the duration of the voltage pulse and consequently the average heating power is determined by a capacitor bank that contains switchable, binary weighted capacitors (C_1–C_8). These capacitors are charged by a constant current source where the combined capacitance defines the charging duration. Each capacitor is controlled through a MOSFET switch (M_{p2}–M_{p9}), which are driven by configuration values stored in registers programmed through the SPI interface. To enhance linearity and improve matching, both capacitors and their corresponding switches are implemented as arrays of smaller unit elements and are spatially distributed. For example, the largest capacitor consists of 128 small unit capacitors and 128 MOSFET switches, and the smallest capacitor consists of 1 unit capacitor and 1 MOSFET switch. This splitting enlarges the needed chip area and metal trac length, which increases the parasitic capacitance if all capacitors or off. Resulting in a minimum charging time even if all capacitors are switched off and reduce the tuning range of the PWM generator but significantly improves the matching and linearity.

Switching on more capacitors increases the charging time, thus extending the PWM pulse and increasing the heating power. The charge bias regulates the charging current. Increasing the voltage V_{charge} leads to faster charging of the

capacitor banks, which shortens both the minimum and maximum achievable pulse widths. Figure 64 shows a schematic representation of the principal effect of the bias settings on the average heating power of a channel over the decimal value (SPI). The red curves show how the heating power curve changes with different charging bias voltages. The red curve (1) represents the highest bias and the curve (4) the lowest bias voltage in this figure. The shift bias is for all red curves the same. This is only a theoretical representation of the principle of bias settings. In reality, the power is not perfectly linear over the decimal values (SPI). In the range of very small and large powers, the linear curve becomes more like a quadratic curve. As an example, the post-layout simulated power curve with perfect bias voltages is shown in Figure 67.

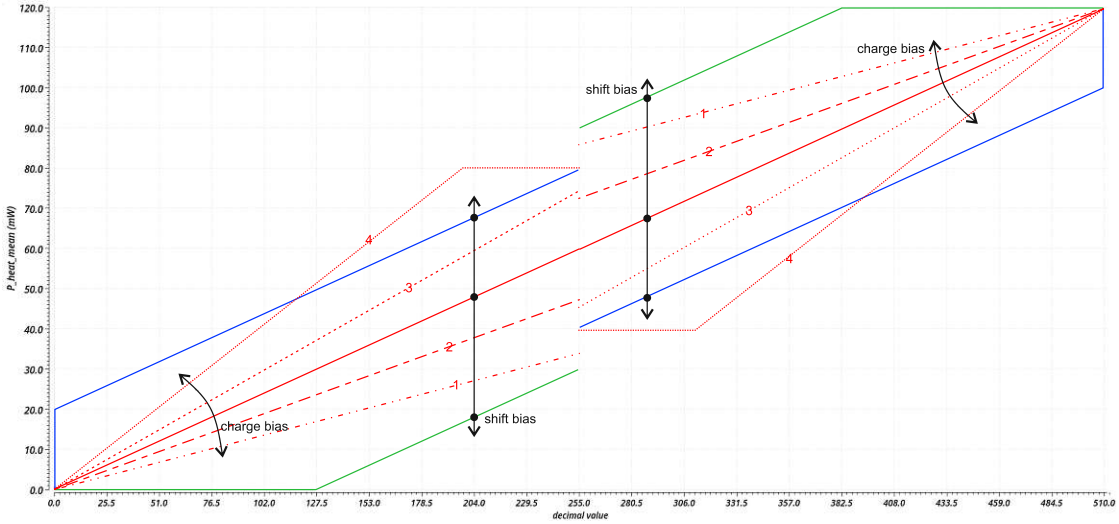


Figure 64: Mean heating power of a channel depending on the bias voltages (theoretical representation of the principal effect of the bias settings).

Figure 65 shows a previous investigated version of the PWM generator and the PWM adjustment stage. It incorporates MOS capacitors (MOSCAPs) as switchable unit capacitors. This previously tested MOSCAPs exhibit a much higher area capacitance compared to other integrated capacitors but also adds a higher parasitic capacitance to the substrate. After the first post-layout simulations they were replaced with double metal-insulator-metal (DMIM) capacitors The smaller parasitic capacitance of the DMIM capacitors reduce the minimum effective capacitance. Additionally, the p-wells beneath the DMIMs are removed to further decrease substrate coupling. This shortens the minimum possible charging duration and expands the tuning range. Residual parasitic capacitance remains on the delay line despite all capacitors being switched off, preventing the pulse

width from reaching zero. This parasitic capacitance always induces a charging time greater that zero, and therefore a minimum pulse duration resulting in a minimum heating power. To reduce the effective minimum heating power, the pulse width of PWM can be shortened. The heating powers are shifted down, and the lowest possible heating power is reduced. This is shown in Figure 64 for three different fictitious shift bias voltages (green, red, blue). The shift is achieved by a constant current from M_{p20} charging the capacitor C_1 and the AND_2 logic gate. The shift functionality is externally adjustable via the shift bias input (V_{shift}), which regulates the drain-source current through the M_{p20} transistor. Depending on PVT variations, the achievable duty cycle range with the 8-bit capacitor tuning (fist 8 bits of the SPI) is restricted to approximately 0 to 70 % tuning range. As a result of this limited tuning range, the 8-bit version (Figure 65) was not produced.

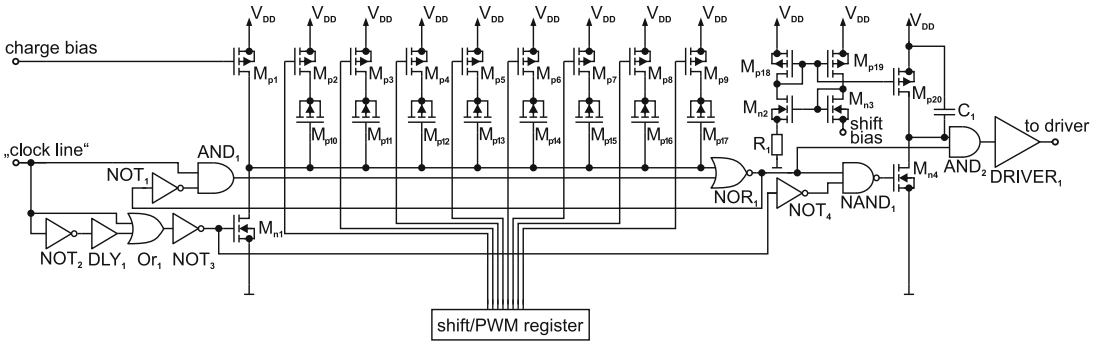


Figure 65: Circuit diagram of the previous version PWM generator, incorporating MOSCAP arrays and are controlled via a 9 bit SPI interface. Source: [67]

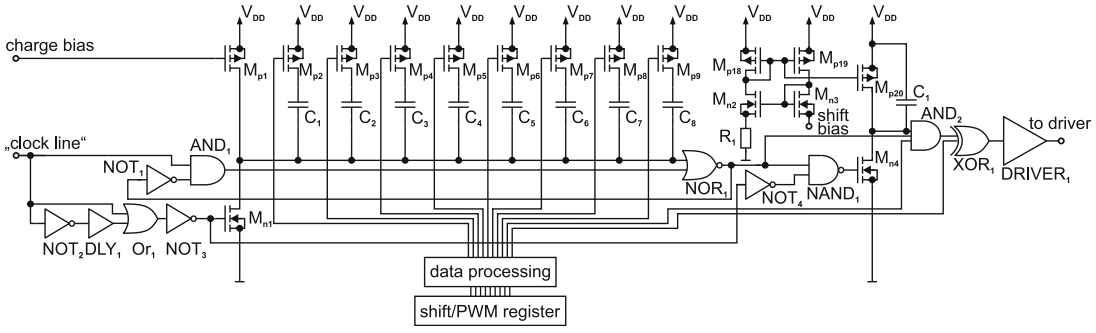


Figure 66: Circuit diagram of the enhanced PWM generator, incorporating DMIM capacitors and are controlled via a 9 bit SPI interface. Source:[67]

To further increase the tuning range to 100 % a data processing block and an XOR gate were added before the output driver. The final circuit diagram is shown in Figure 66. The SPI input was extended to nine bits. Based on the state of the ninth bit, the data processing unit automatically inverts all bits of the digital control word, as well as the corresponding PWM output. This bit extends the digital range

from 256 to 511 and enables the use of the remaining duty cycles. When the ninth bit is activated, the start and end triggers of the PWM pulse are exchanged, allowing for the generation of complementary duty cycles without requiring user intervention during value specification in the range of 256 to 511. Inverting the output introduces a phase jump relative to the input clock at the transition between 255 and 256; however, the phase remains stable within each subrange (0–255 and 256–511) and is always stable during a specified digital value. If the bias voltages are not adjusted, digital values in the range of 256–511 (ninth bit active) correspond to duty cycles of approximately 30 to 100 %, based on the conditions described above. Consequently, at the transition from 255 to 256, the duty cycle abruptly drops from 70 to 30 %. By adjusting the bias voltages, the pulse width can be shifted such that digital values from 0 to 255 correspond to duty cycles ranging from 0 to 50 %, while values from 256 to 511 correspond to 50 to 100 %. In addition, the data processing unit ensures defined boundary conditions. The PWM output continuously stays off for the digital value 0 and continuously on for the value 511. The post-layout simulated power curve with perfect bias voltages is shown in Figure 67

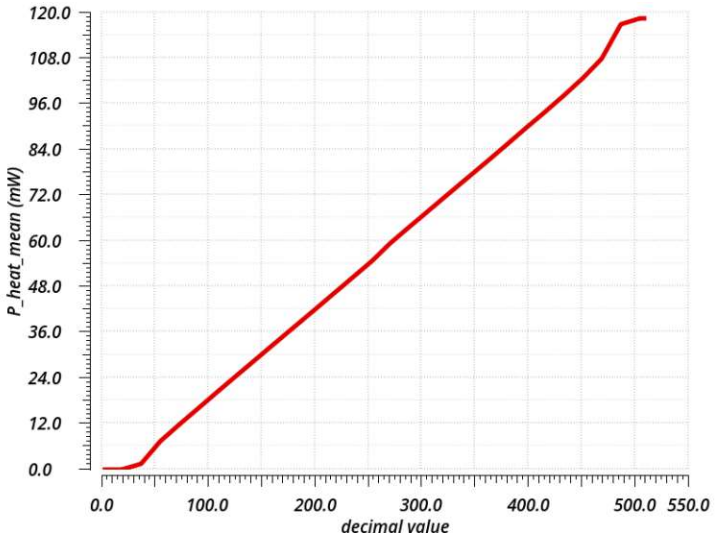


Figure 67: Simulated mean heating power in a 750 Ω heater resistor for 9-bit.

Shift Register and Data Processing

To enable individual storage and configuration of the duty cycle and thus the average heating power of each channel, every PWM channel is equipped with its own dedicated 9 bit shift register. These registers are configured through a custom Serial Peripheral Interface (SPI), which uses 11 input pads, including a dedicated reset input. A central address decoder with 6 bits is investigated to select one of

the 40 PWM channels. All PWM ASICs of the quantum simulator get the same SPI signal; the chip select (cs) input determines which chip reacts to the commands. Once a channel is addressed, its corresponding shift register accepts 9 data bits transmitted serially through the data input line (dat). Each bit is latched on the rising edge of the SPI clock, which supports operation at frequencies up to 200 MHz. To simultaneously disable all channels and reset their outputs to zero (000000000), a dedicated reset input is implemented. Digital control logic, including the SPI interface and address decoding, was designed using a digital VHDL workflow and integrated into the overall mixed signal layout. The timing diagram in Figure 68 shows the start up with a reset at the beginning and two channels (adress1, adress2), which are set.

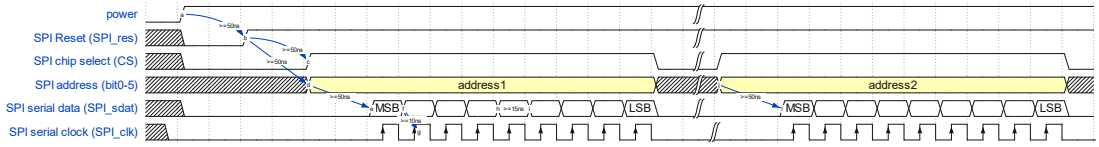


Figure 68: Timing diagram of the serial peripheral interface (SPI).

Bias Distribution

To minimise the required number of bond pads, a common charge and shift bias is employed across all 40 channels, necessitating distribution over the approximately 8.6 mm width of the chip. [75], [76] and my own simulations indicate that distributing current rather than voltage over extended distances achieves a better matching. In the proposed design, the current distribution is reached through multiple locally matched current mirrors, as depicted in Figure 69. Matched MOSFETs are grouped and highlighted with the same colour in Figure 69. Transistors marked in blue and grey are centrally placed on the chip and matched, while those marked in orange are positioned within each of the 40 channels.

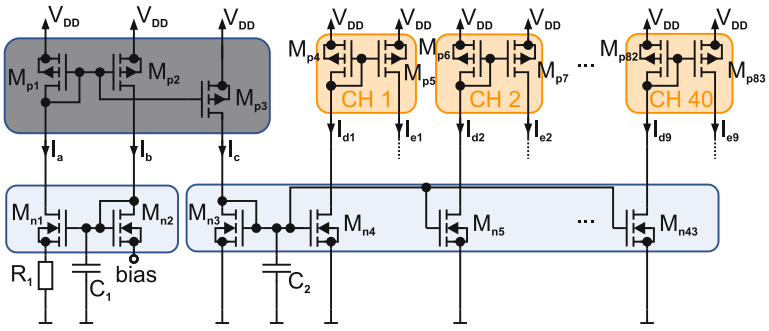


Figure 69: Principal circuit diagram of the bias current distribution for all 40 PWM channels. Source: [67]

The bias voltage and an internal resistor R_1 define the currents I_a and I_b. These currents are mirrored through transistor M_{p3} at a 1:1 ratio, generating a current I_C. The generated current I_C is mirrored again through 40 transistors (M_{n4}–M_{n43}) to the individual current mirrors within each channel. The metal interconnections leading to each channel (I_{d1}, I_{d2}, etc.) extend up to 4.5 mm. Provided that all transistors operate in the saturation region, variations in resistance, and consequently voltage drops, along these long metal tracks introduce a negligible influence on the mirrored currents within the channels. [67]

High-Voltage Cascode Switch (Driver)

The substantial reduction of power losses within the driver is the main benefit of employing pulse width modulation. Theoretically, with ideal instantaneous switching, no voltage drop occurs across the driver's output transistors when switched on and no current flows when switched off, resulting in no power loss since power equals voltage multiplied by current. In practice, however, power losses are present and are significantly influenced by switching losses during transition phases and the voltage drop due to the MOSFETs' ON resistance in the active state. Switching losses are predominantly determined by transition times, which are strongly affected by capacitive load. The switch is designed to drive a total node capacitance lower than 550 fF.

To achieve minimal transition durations for a 9.9 V voltage swing in the XH018 technology, a high-voltage double cascoded switch utilizing adaptive bias voltages has been implemented, similar to the switch used for the Gater ASICs (see Chapter 2.2 and 2.3) and is a modified version of the switch presented 0.35 µm CMOS technology in [52]. Figure 70 illustrates the proposed driver switch designed for a maximum voltage swing of 9.9 V (transistors M_{p5} – M_{p7} and M_{n7} – M_{n9}). The output node (V_{heat_res}) connects to one side of a resistor and the other resistor terminal is connected to V_{DD} at 9.9 V.

Although theoretically, transistors M_{n7}–M_{n9} alone are sufficient to toggle the heating resistors on and off, as the output node would automatically recharge to 9.9 V when the transistors switch off, additional MOSFETs (M_{p5} – M_{p7}) are included to reach a fast transition to 9.9 V. This increases switching performance and reduces losses. Furthermore, the adaptive bias structure relies on the PMOS transistors M_{p5} – M_{p7} to shift the bias voltages of the NMOS transistors M_{n7}–M_{n9}. [67]

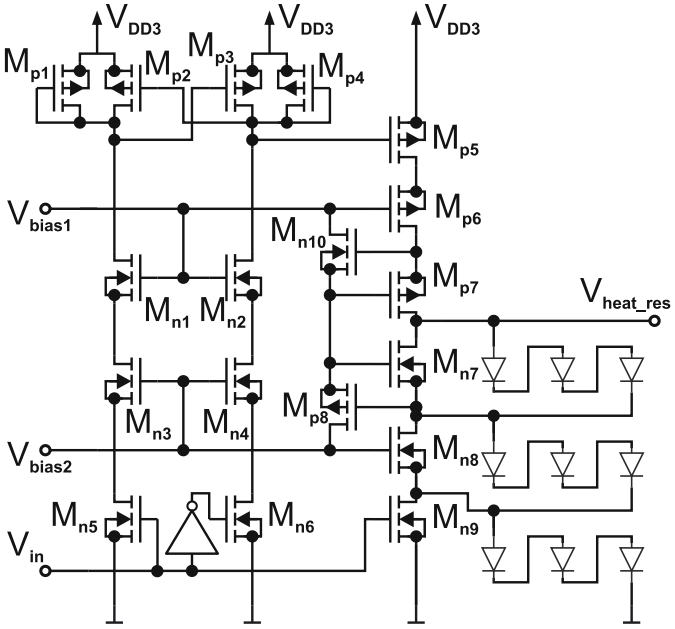


Figure 70: High-voltage double cascoded switch with level shifter and protective diodes. Source: [67]

The maximum heating power (on state) is reached when the output is at 0 V, while an output of 9.9 V resalts in zero heating power (off state). Stacked 3.3 V MOSFETs are used to implement the circuit which can switch between 0 V (ground) and 9.9 V (V_{DD3}). To withstand the full output voltage range, three stacked NMOS transistors (M_{n7}–M_{n9}) and three stacked PMOS transistors (M_{p5} – M_{p7}) are employed. When the driver output is in the off state (9.9 V), M_{n7} – M_{n9} must sustain the full 9.9 V across their combined drain-source terminals because the transistors M_{p5} – M_{p7} pull the output to V_{DD3} (9.9 V). On the contrary, during the on state (0 V), the PMOS stack (M_{p5} – M_{p7}) must withstand the 9.9 V difference as the NMOS stack pulls the output to 0 V (ground). Given that the nominal maximum voltage of a single transistor is 3.3 V, a minimum of three devices in series are required on both the pull-up and pull-down paths to safely tolerate the voltage. The bulk terminals of transistors M_{n7}–M_{n9} and M_{p5}–M_{p7} are connected to their related source terminals. Medium deep n-wells, which withstand nominal 10 V to the substrate, are used to isolate the transistors. Given that the substrate potential is tied to ground, the isolation provided is sufficient. For transistors M_{n7} and M_{n8}, the corners of the p-wells are rounded to mitigate the risk of breakdown due to the higher voltages than the maximum 8 V between the p-well and the deep n-well. To reduce the layout area, M_{n7} and M_{n8} are integrated within a shared medium deep n-well. The

driver operates in the on or off state, necessitating complementary control of the upper (M_{p5} – M_{p7}) and lower (M_{n7}–M_{n9}) transistor stacks. Since M_{p5} and M_{n9} operate in different voltage domains, a level shifter is required to appropriately bias the gates. This is achieved with the transistors M_{n1}–M_{n6} and M_{p1}–M_{p4}, based on the architecture described in [77]. The level shifter ensures that the gate voltage of M_{p5} is maintained within the range of V_{DD3} (9.9 V) to V_{bias1} (6.6 V).

When the input control voltage V_{in} = 1.8 V (on state), the transistor M_{n9} turns on while M_{p5} is turned off due to the level shifter applying V_{DD3} to its gate. This results in the drains of M_{n9} and M_{p5} being pulled to 0 V and $V_{bias1} + V_{th}$, respectively. MOSFET M_{n8} turns on and M_{p6} turns off, because the gate of M_{p6} is fixed at V_{bias1} = 6.6 V, while M_{n8}'s gate is biased at V_{bias2} = 3.3 V. The drain of M_{n8} is discharged to approximately 0 V.

Consequently, M_{p8} is activated, which biases the M_{n7} and M_{p7} gates to V_{bias2} = 3.3 V. This shift turns M_{n7} on, pulling its drain, and therefore the output to approximately 0 V, while simultaneously turning M_{p7} in the off state. The adaptive bias circuit, consisting of M_{n10} and M_{p8}, is used to ensure that the gate voltages of M_{n7} and M_{p7} remain within permissible process voltage limits. With a fixed voltage, the maximum voltages would exceed the limits.

The total voltage across M_{n7} – M_{n9} can be unevenly distributed between the MOSFETs for some output pulse durations. To address such conditions in which the drain-source voltage on the individual transistor would exceed its absolute maximum voltage rating (3.6 V), protection diodes are incorporated, as illustrated in Figure 70. These diodes distribute the voltage across the NMOS stack. Polysilicon diodes, selected for their higher forward voltage compared to those of crystalline silicon diodes, are used for this purpose. Circuit simulations showed that the resulting current at an evenly distributed 1.1 V per device (over 9.9 V total) is nominally 1.93 µA and therefore is not significant for power consumption and losses. [67]

Transimpedance amplifier

The chip also implements eight monitoring amplifiers to monitor light powers in the integrated waveguides on the PIC. The amplifiers are implemented as transimpedance amplifiers (TIAs), which convert the input current from the monitoring photodiodes into a proportional output voltage. The photodiodes are directly integrated into the PIC above the waveguides to monitor the intensity. As

an example, a microscopic image of a photodiode above a waveguide on the PIC is shown in Figure 71. The amplifiers were realised with CMOS inverters and directly output the analog signal. The feedback resistor was chosen at 100 kΩ, which results in a photocurrent of 0.5 µA to an output voltage of 50 mV. The output voltage range of the TIAs is in the range of 0 V to 1.8 V and is relatively linear up to a current of 7 µA, which corresponds to an output voltage of about 1.6 V (high impedance termination).

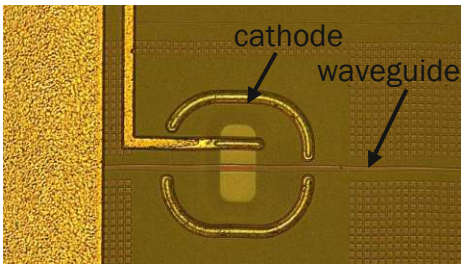


Figure 71: Monitoring photodiode integrated into the PIC.

Layout

The PWM ASIC, comprising 40 pulse width modulation (PWM) channels and eight monitoring channels, occupies a die area of approximately 1.5 × 8.7 mm². The complete chip layout is illustrated in Figure 72. The device features a double row of pads that includes connections for data, clock, bias, and multiple power supply voltages. The pads in the single row are dedicated to the outputs of the 40 heater channels and the current input pads of the eight transimpedance amplifiers, indicated in blue, which will be direct wire bonded to the PIC. The rounded dimensions and placement of the pads are shown in Figure 73.

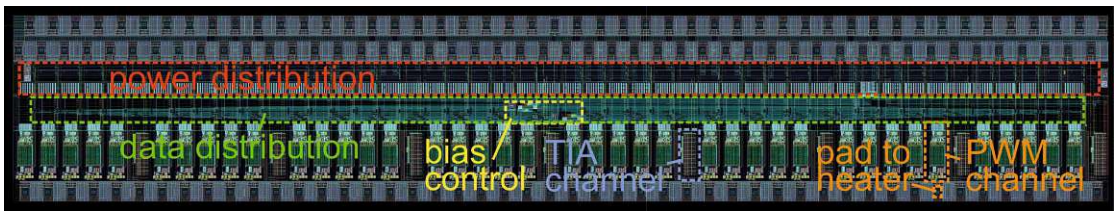


Figure 72: Layout of the 1.5 × 8.7 mm² PWM ASIC. Source: [67]

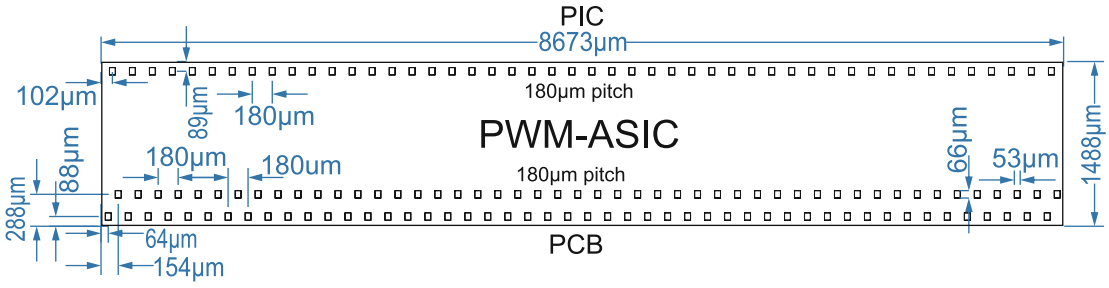


Figure 73: Dimensions of the PWM ASIC, outer dimensions whiteout saw trench.

A significant portion of the chip area is allocated to power and data distribution networks, primarily due to high current requirements and the large number of signal lines. The layout of a single PWM channel is shown in Figure 75, with each channel occupying an area of 170 × 440 µm². The channel layout is designed at a pitch of 180 µm to align with the integration constraints of the corresponding PIC. Although it is feasible to reduce the pitch of the channel to approximately 100 µm, the primary limitation arises from the size of the bond pads. Reducing the pitch would not affect static power consumption and would result in only a marginal increase in dynamic power consumption, because of the longer metal interconnects. As the overall area of each PWM channel would remain almost constant, reducing the pitch would necessitate a corresponding increase in width, leading to longer metal routing paths. [67]

To improve linearity and improve component matching, both the capacitors and their associated switching elements are implemented as arrays of smaller unit elements that are spatially distributed across the layout, with the PWM generator shown in Figure 75. Capacitors are arranged within a grid-based common-centroid scheme shown in Figure 76. The capacitors are connected in parallel and charged and discharged in every PWM cycle. All units of the same colour in Figure 76 (e.g. C8) for a capacitor bank which are only all switched on or off. The number of unit capacitors doubles from one capacitor bank to the next larger one to obtain a binary weighted set of capacitance values.

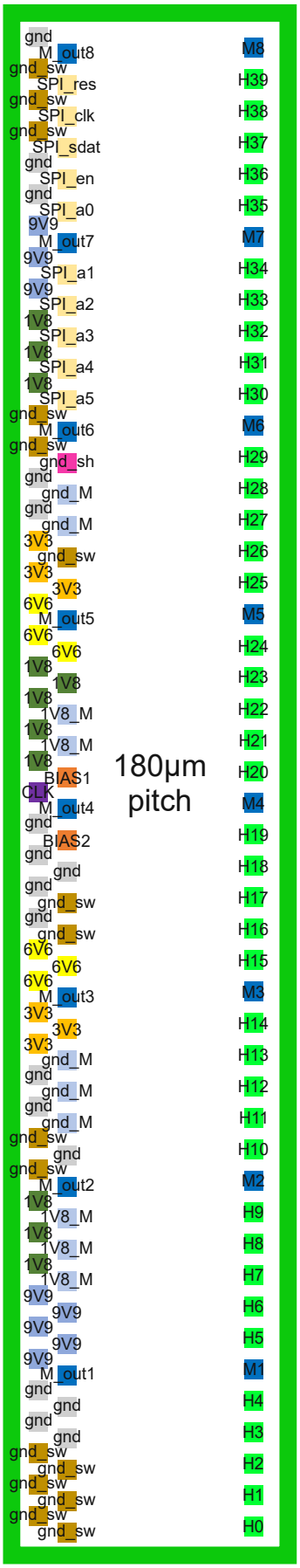


Figure 74: Pad-layout of the PWM ASIC.

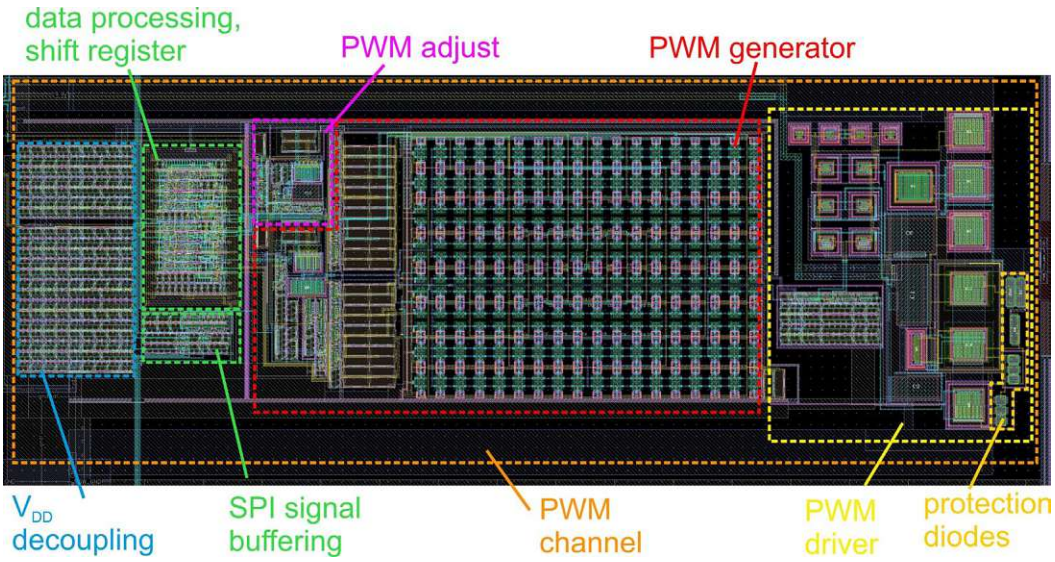


Figure 75: Layout of one PWM channel. Source: [67]

This segmentation facilitates better matching, but increases the overall chip area and the length of the interconnecting metal traces. Dummy capacitors (Cx), with a switch and small capacitor, are placed on the edges and in the middle of the layout to achieve an even better match for their surrounding capacitors. These dummy capacitors are permanently switched on and connected to the 1.8 V supply to stabilise the supply. The layout of the capacitor array is shown in Figure 77. The MOSCAPs on the left side of Figure 77 are used to stabilise the control signal for the individual control voltage of each capacitor bank. Metal interconnections use a sophisticated design to reduce the parasitic capacitance between the control lines and the delay line connecting the capacitors.

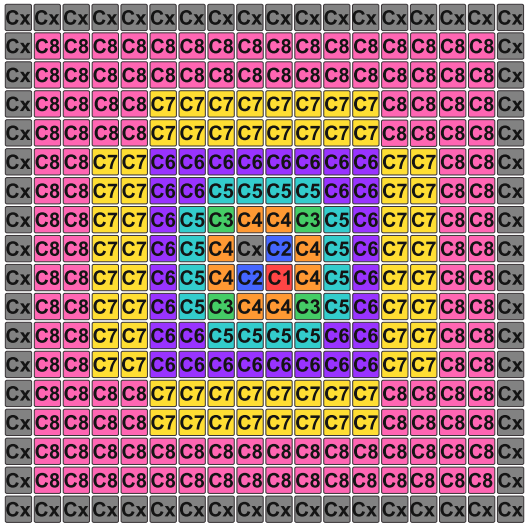


Figure 76: Used common-centroid capacitor layout scheme.

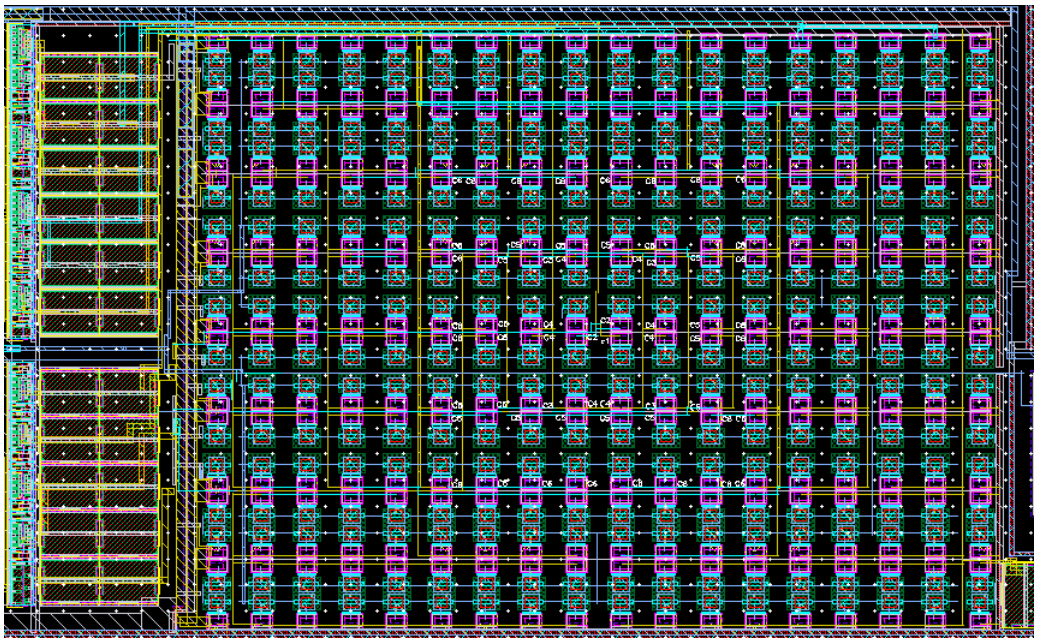


Figure 77: Layout of the capacitor banks.

The pitch of the pads to the PCB is 180 µm. The pads in the second row are shifted by 90 µm. All pads have a size of 53 µm x 66 µm. The layout of the pads is shown in Figure 74. Towards the PCB, each PWM ASIC has 2 bias pads, 37 supply voltage pads with 4 different voltages, 38 ground pads (separated in ground groups), 10 SPI pads, 8 monitoring output pads and one clock pad. In Table 5 all different pad types are listed with a short description and information about voltages.

Table 5: Description of the input and output pads of the PWM ASIC; including estimated voltage and current range.

connected to	pad name	description	type	voltage/current range
PCB	gnd_sw	ground associated 9.9V, 6.6V and 3.3V	ground	0 V
PCB	gnd	ground for analog control circuits	ground	0 V
PCB	gnd_M	0V ground for the monitoring TIAs	ground	0 V
PCB	gnd_sh	shield ground connected to layer which shields gnd from 9.9V in padring	ground	0 V
PCB	1V8	1.8V for digital and analog control circuits	voltage supply	1.8 V
PCB	1V8_M	1.8V for monitoring TIAs	voltage supply	1.8 V
PCB	9V9	9.9V for the heater switch	voltage supply	9.9 V
PCB	6V6	6.6V for the heater switch	voltage supply	6.6 V
PCB	3V3	3.3V for the heater switch	voltage supply	3.3 V
PIC	H	outputs to the heaters on the PIC (Channel 0 to 39)		0 V / 9.9 V

PCB	CLK	clock input to synchronize PWM to laser clock (80MHz)	clock	digital 0 V / 1.8 V
PCB	M_out	analog voltage TIA output operating point: 0.9 V (Channel 1 to 8)	analog voltage output	0 V – 1.8 V
PIC	M	to monitoring photodiodes operating point: 0.9 V (Channel 1 to 8)	analog current input	0 – 9 µA
PCB	SPI_res	SPI Reset	SPI	digital 0 V / 1.8 V
PCB	SPI_clk	SPI serial clock	SPI	digital 0 V / 1.8 V
PCB	SPI_sdat	SPI serial data in	SPI	digital 0 V / 1.8 V
PCB	SPI_en	SPI chip enable/select	SPI	digital 0 V / 1.8 V
PCB	SPI_a0	SPI address in 0	SPI	digital 0 V / 1.8 V
PCB	SPI_a1	SPI address in 1	SPI	digital 0 V / 1.8 V
PCB	SPI_a2	SPI address in 2	SPI	digital 0 V / 1.8 V
PCB	SPI_a3	SPI address in 3	SPI	digital 0 V / 1.8 V
PCB	SPI_a4	SPI address in 4	SPI	digital 0 V / 1.8 V
PCB	SPI_a5	SPI address in 5	SPI	digital 0 V / 1.8 V
PCB	PWM Bias 1 (charging)	determines the charging current of the switchable capacitor bank in the delay line and therefore the pulse duration voltage which is applied at the pad generates a corresponding dc current out of the Pad	Bias	0 – 1 V (-1.6 – 0 mA)
PCB	PWM Bias 2 (shift)	determines the charging current of the switchable capacitor bank in the delay line and therefore the pulse duration voltage which is applied at the pad generates a corresponding dc current out of the Pad	bias	0 – 1 V (-0.5 – 0 mA)

The source of bias generation (M_{n1}–M_{n2} and M_{p1}–M_{n3} in Figure 69) and the bias current mirror which generates the currents for the individual channel (M_{n3}–M_{n43} in Figure 69) are centrally placed. The layout of a bias generation source is shown in Figure 79 and the layout of a bias current mirror is shown in Figure 78. The individual transistors are split into many smaller transistors which are common-centroid placed to get a better matching of the individual currents. On all four

sides, dummy transistors are used to achieve an even better match of the edge transistors. In both layouts capacitors on each side are used to stabilise the gate voltages. The metal traces to the channels have a different width to obtain more uniform resistance (shown in Figure 79). In principle, the Bias 1 and Bias 2 distributions share the same layout.

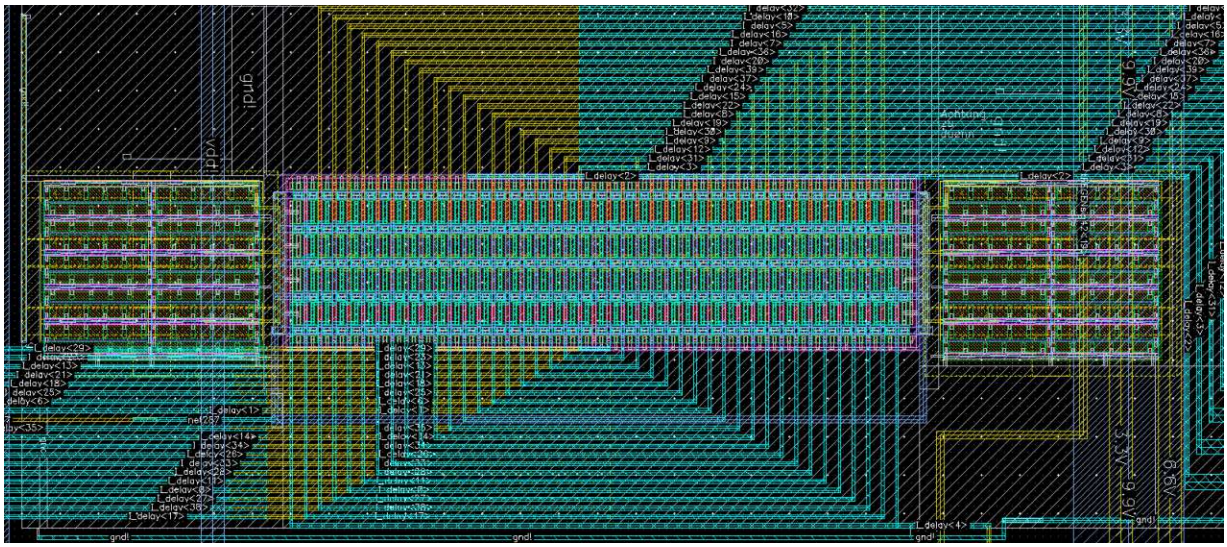


Figure 78: Layout of a central bias distribution mirror (M_{n3}–M_{n43} in Figure 69).

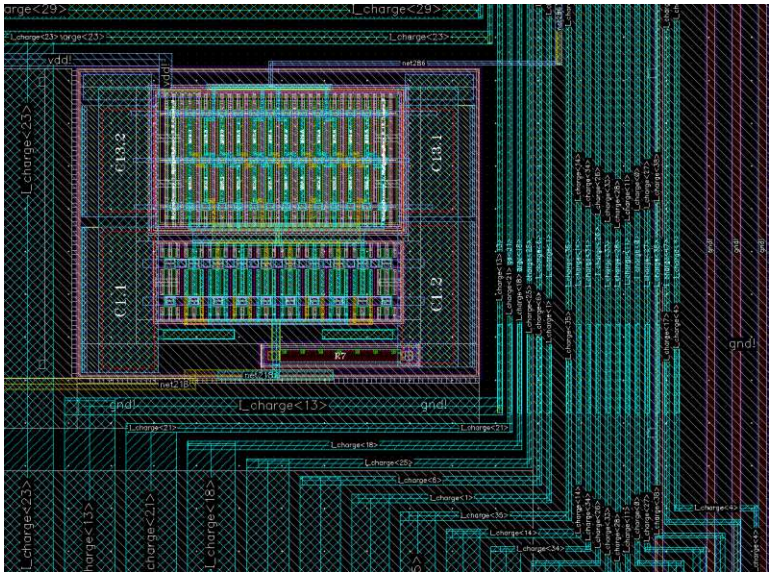


Figure 79: Layout of one central bias generation source (M_{n1}–M_{n2} and M_{p1}–M_{n3} in Figure 69).

3.1.2 Simulation and Measurement

The measurement setup includes a pulse generator (Agilent 81134A), two oscilloscopes (Keysight MSOV204A and Tektronix TDS6124C), two programmable power supply units and a Picoprobe Model 35. These components are controlled

by a PXI-based system from National Instruments (NI), which includes the NI PXIe-1062Q chassis and the embedded controller NI PXIe-8133, as illustrated in Figure 80. Digital signals for SPI programming are generated using the NI PXI-6552 digital I/O module. [67]

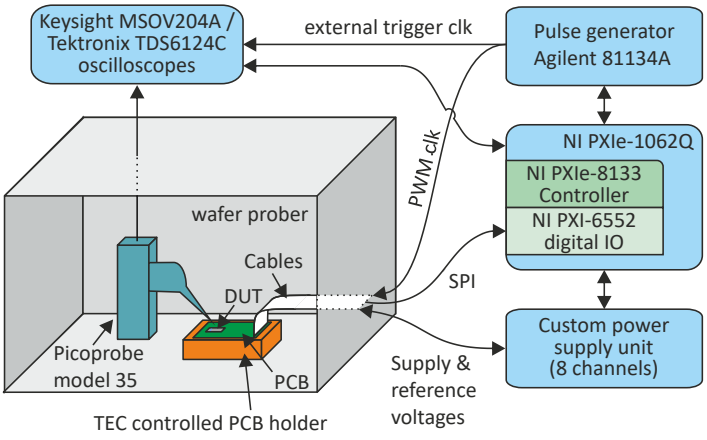


Figure 80: Measurement setup for characterising the PWM ASIC. Source: [67]

To test the PWM ASIC, a test-PCB is necessary. The circuit board size is 65 x 100 mm and consists of 6 layers to accommodate the various signals and power supplies. The layout of the test-PCB is shown in Figure 81 on the left side and a rendering is shown on the right side. The PCB has a defined layer structure which ensures that the clock and digital signals can be routed with traces with 50 Ohm characteristic impedance. This minimises signal losses and reflections, resulting in efficient signal transmission. For designing the PCB especially, the supply and bias currents of different inputs were post-layout simulated (simulated currents at the pads can be found in the Appendix in Figure 110 to Figure 114). Despite large decoupling capacitors on the chip, simulations showed that HF capacitors with the lowest possible ESR were necessary. Therefore, the PCB incorporates multiple decoupling capacitors positioned in close proximity to the chip pads to ensure stable operation. The simulation results show that all power and ground bond wires should have the lowest possible inductance, ideally less than 1 nH, which corresponds approximately to a wire length of 1 mm. For this reason, the bod pads on the PCB are placed near to the chip edges and are shorter than 1 mm. The PWM ASIC is glued to a test-PCB by conductive adhesive and are wire bonded, as illustrated in Figure 82. In this setup, heating resistors with a resistance of 750 Ω are not wire-bonded to a photonic integrated circuit (PIC) but are instead placed directly on the PCB. [67]

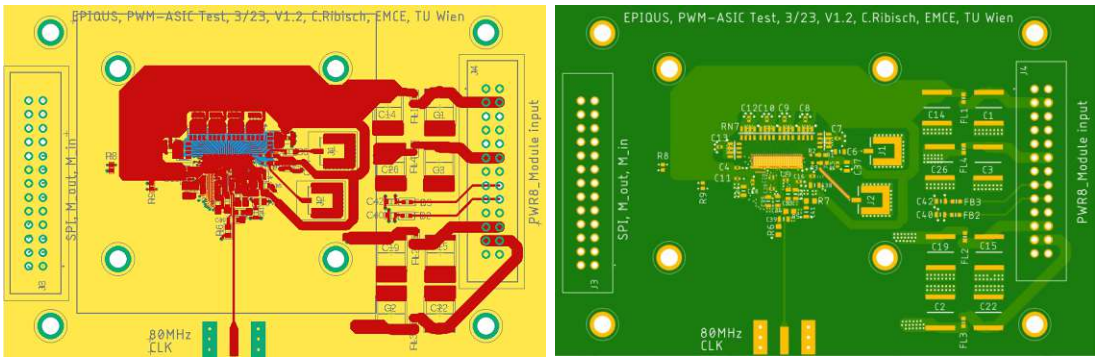


Figure 81: Test-PCB for the PWM ASIC from Run 1 (left: layout; right: rendering).

The entire assembly is mounted on a thermoelectric cooler (TEC), maintained at a temperature of 25 °C, to account for the required thermal management due to the cumulative heating effect of multiple phase shifters within the PIC. The PCB, the TEC, and the Picoprobe are housed within a Karl Suss PA 200 wafer prober. The Picoprobe needle is placed on the appropriate bond pad of the PCB and its output is connected to the oscilloscope for signal acquisition. The pulse generator provides an 80 MHz base clock signal, which is simultaneously applied to the clock input of the PWM ASIC and to the external trigger input of the oscilloscope. [67]

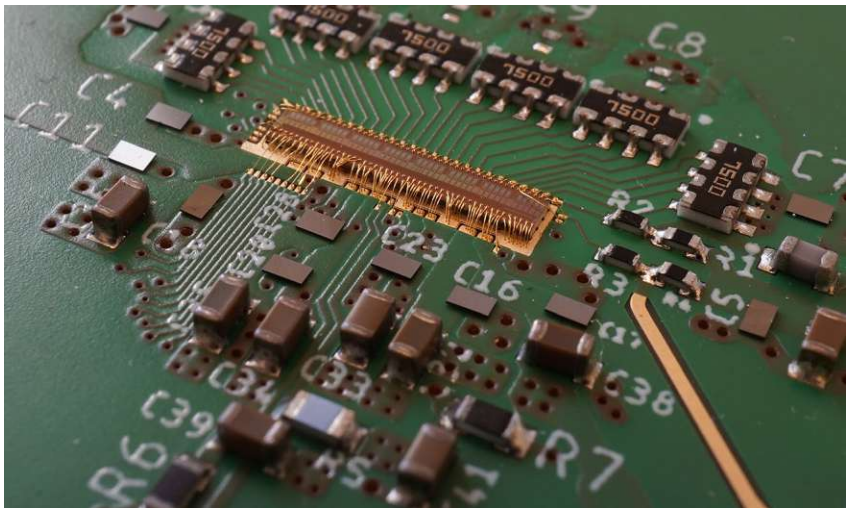


Figure 82: Glued and wire-bonded PWM ASIC on the assembled test-PCB. Source: [67]

A Keysight MSOV204A oscilloscope with a 20 GHz bandwidth is used to measure voltage transients, enabling the calculation of signal rise and fall times. For all remaining measurements, a Tektronix TDS6124C oscilloscope is used due to equipment availability. The SPI interface, including the channel-specific shift registers, is controlled via the digital I/O card of the PXI system. All SPI signals from

the PXI are externally terminated with 50 Ohm on a separate PCB which is directly connected to the SPI connector on the test-PCB. [67]

For the first measurements, only the first 8 bits of the serial control are utilised. This approach enables a smooth variation of the power dissipated in the heating resistors without a possible abrupt transition in the heating power and phase. On the downside, it restricts the maximum achievable tuning range and, consequently, the maximum heating power. Relative to the theoretical maximum heating power, defined by applying a constant voltage of 9.9 V across the heating resistor, approximately 70 % of this maximum power is achieved. To accommodate this, charge and shift biases are adjusted to reduce the charging speed, thereby enabling longer pulse durations at lower digital input values. The shift bias V_{shift} is set to 0.25 V and the charge bias V_{charge} to 0.15 V, optimising the system to achieve the maximum available tuning range (≈ 70 %) with only 8 bits of resolution. [67]

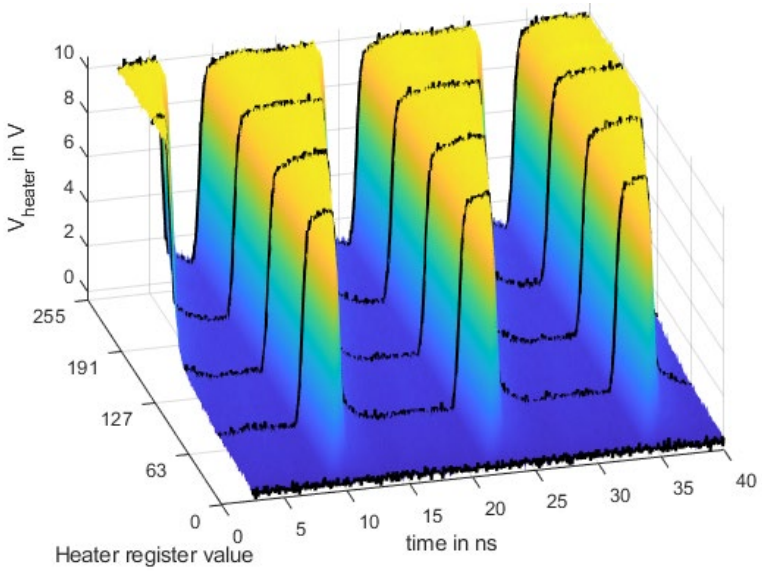


Figure 83: Transient voltage measured at heating resistor 24 on the test-PCB at different specified digital values using 8 bits (V_{shift} = 0.25 V, V_{charge} = 0.15 V). Source: [67]

Figure 83 illustrates the transient voltage on the heating resistor 24 over time and digital input values. The voltage level in the Figure is colour-coded. It clearly shows an increase in the pulse width with increasing digital values. The measured 20%-to-80% output rise time is 0.46 ns, and the 80%-to-20% fall time is 0.44 ns. Figure 84 presents the calculated average heating power (normalised as a percentage of the maximum) for a subset of randomly selected heaters 14, 15, and 24 with only 8 bits. A duty cycle of roughly 70 % is reached, corresponding to a heating

power of approximately 90 mW for the used 750 Ω resistor, at the maximum digital value (255) is reached. The mean heating power

$$P_{heater} = \frac{1}{R * T} * \int_0^{\infty} (u_{heater}(t))^2 \, dt \qquad 8$$

is calculated for every digital input value from the transient voltage $u_{heater}(t)$ shown in Figure 83. [67]

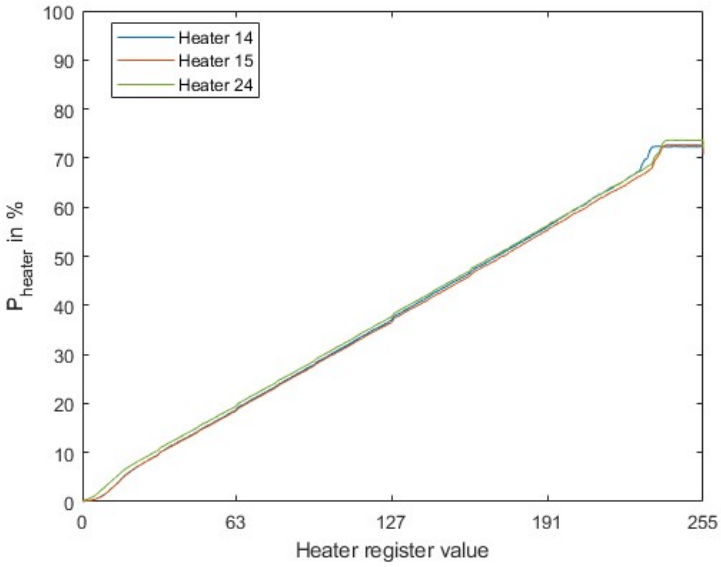


Figure 84: Mean heating power of heaters 14, 15, and 24 at the different specified digital values using 9 bits (V_{shift} = 0.25 V, V_{charge} = 0.15 V). Source: [67]

Figure 85 illustrates the transient voltage across a heating resistor as a function of time and digital input value, using a 9 bit control scheme. A tuning range from 0 to 100 % is achieved by using 9 bits. Charge and shift biases are carefully adjusted to ensure a smooth and continuous transition between digital values 255 and 256, where the ninth bit switches from 0 to 1. A phase jump is observed at this transition point; however, the phase remains stable for all subsequent higher digital input values. Figure 86 presents the average heating power using 9 bits, expressed as a percentage of the maximum heating power for heaters 14, 15, and 24. The mean power is derived from the transient voltage waveforms using the same methodology described in Equation 8. [67]

The entire chip has a static average power consumption of approximately 460 mW, corresponding to about 11.5 mW per channel, with the majority of the consumption attributed to the level shifter circuitry in the cascoded switch. Each channel consumes up to 15 mW dynamic power when it is active. [67]

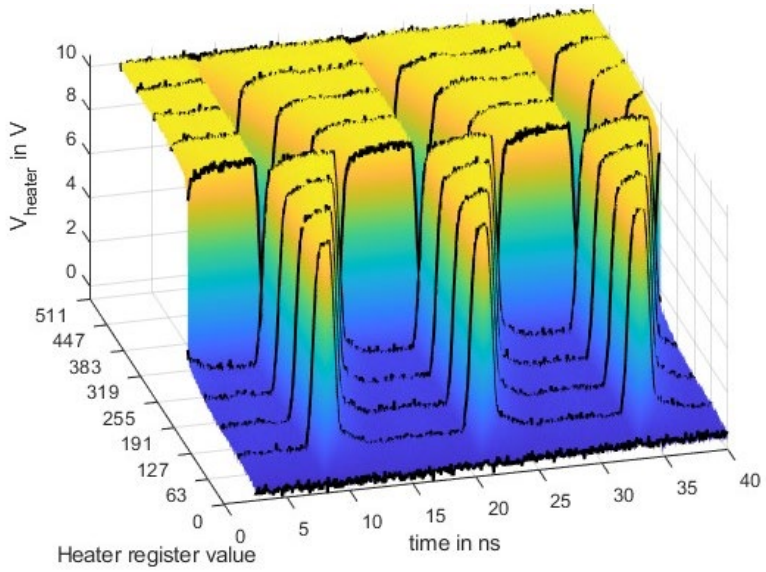


Figure 85: Transient voltage measured at heating resistor 24 on the test-PCB at different specified digital values using 9 bits (V_{shift} = 0.38 V, V_{charge} = 0.25 V). Source: [67]

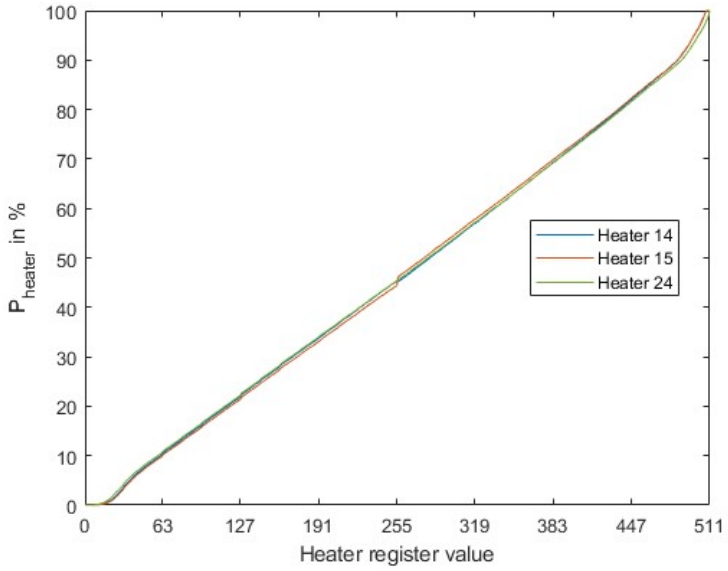


Figure 86: Mean heating power of heaters 14, 15, and 24 at the different specified digital values using 9 bits (V_{shift} = 0.38 V, V_{charge} = 0.25 V). Source: [67]

Comparison and conclusion

In the scope of this doctoral thesis, a PWM heater control ASIC in XH018 (0.18 µm CMOS) was developed for a quantum simulator. To ensure constant temperature of the phase shifters and consequently a stable optical phase of the photons for each laser pulse, the PWM signal is synchronised with the laser pulses. Each ASIC comprises 40 independent PWM channels, each capable of delivering a 9.9 V pulse with a maximum heating power of up to 130 mW at a 750 Ω load resistor. The architecture presented is entirely scalable and can be extended to a higher

number of channels with a minor modification. Compared to the implementation reported in [78] based on a 160 nm BCD8sP technology, which achieves a maximum output power of 14 mW, the present design delivers approximately nine times higher heating power per channel. The measured rise and fall times of the PWM output (20%-to-80% and 80%-to-20%) are 0.46 and 0.44 ns, respectively. The static mean power consumption of the entire chip is approximately 460 mW when operated with an 80 MHz PWM base clock, but could be increased to up 300 MHz with small adoptions in the bias distribution. For a single active channel, the maximum additional dynamic power dissipation is approximately 15 mW, which is significantly lower than the maximum heating power of 130 mW. [67]

In the context of 3D integration of the PIC with the ASICs, the use of a PWM approach significantly reduces the heat dissipation from the control electronics into the PIC. This thermal efficiency is essential for enabling the control of a larger number of phase shifters within the quantum simulator under a fixed thermal budget, making PWM a key enabler for the scalability of more complex quantum photonic systems. Moreover, the reduced power dissipation minimises temperature drifts within the simulator, thereby enhancing thermal stability. This facilitates the use of smaller thermoelectric coolers to maintain the global temperature of the photonic chip, contributing to overall system compactness and energy efficiency. [67]

In addition, the high frequency of the PWM signal, combined with accurate synchronisation with the laser pulses for the PIC, leads to a substantial suppression of effective thermal ripple, maintaining thermal fluctuations well below the critical thresholds required for high precision quantum operations. [67]

Table 6 provides an overview of selected literature references in which integrated resistors are controlled to set a temperature. In references [79], [80], [81], [82], the heating power is regulated by externally applied constant voltage or constant current (DC) signals. According to the information available in these publications, none of these DC-based solutions implement an on-chip control, which may be attributed to the high-power losses in the controller circuitry, as discussed in the Introduction. In contrast, references [78], [83], [84], [85] describe fully integrated heater control circuits, featuring output voltage swings from 1.8 V to 5 V and operating frequencies ranging from 583.5 kHz to 50 MHz, with implementations in 65 nm CMOS technology and driver designs targeting up to 400 MHz. In

addition, references [86] and [87] employ externally generated pulse width modulation (PWM) signals to control the heating power. [67]

Table 6: State of the art comparison of references with integrated heaters. Source: [67]

Ref.	Type	Sync	Int.	PWM frequency (MHz)	Voltage (V)	Max. heater power (mW)
[79]	DC	-	N	-	< 2.1	104
[80]	DC	-	N	-	< 11	18
[81]	DC	-	N	-	n. r.	21
[82]	DC	-	N	-	n. r.	2.5
[83]	PWM	N	Y	< 78*	1.8	14
[84]	PDM	Y	Y	50 (400)	3.3	40
[85]	PWM	Y	Y	0.584	5	n. r.
[78]	PWM	Y	Y	9.4	1.8	14
[86]	PWM	n. r.	N	2	5	5
[87]	PWM	n. r.	N	4	2	25
This work	PWM	Y	Y	80	9.9	130

Y: yes; N: no; *: peak at 50 % duty cycle; PDM: pulse density modulation, n. r.: not reported

3.1.3 Second Run and Outlook

To enable flip-chipping and a fully 3D-mounted version, a second production run was necessary. Some circuits were also redesigned and improved, and a new pad ring design was introduced. In the second ASIC run, small ESD protection diodes at the digital inputs are investigated to reduce the sensitivity to electrostatic discharge (ESD). To keep the chip size small, no standard ESD diodes could be integrated. Another improvement is the implemented pull-up or pull-down resistors depending on the input type. The inputs are equipped with 36 kΩ resistors to be able to utilise as many channels as possible in the event of faulty SPI bond connections. For example, an SPI address line without a bond connection is pulled down, providing a known safe state for debugging and guaranteeing the usage of more channels compared to a false “high” state at this address line.

The bias current for charging the capacitors and the bias current that determines the PWM signal is distributed with multiple current mirrors, shown in Figure 87. Except in the last mirrors, which are integrated into the channels (orange), 1.8 V transistors with lower threshold voltages (using the XH018 LVT process module) are used in the second run to achieve a wider operating range. The generated current in dependence on the input bias voltage is shown in Figure 88. The wider linear region due to the LVT transistors (yellow curve) is clearly recognisable. The LVT process module, which made this MOSFET types possible is added in the second ASIC production run. The power supply voltage of this PWM circuitry and of the bias distribution is again 1.8 V (V_{DD}).

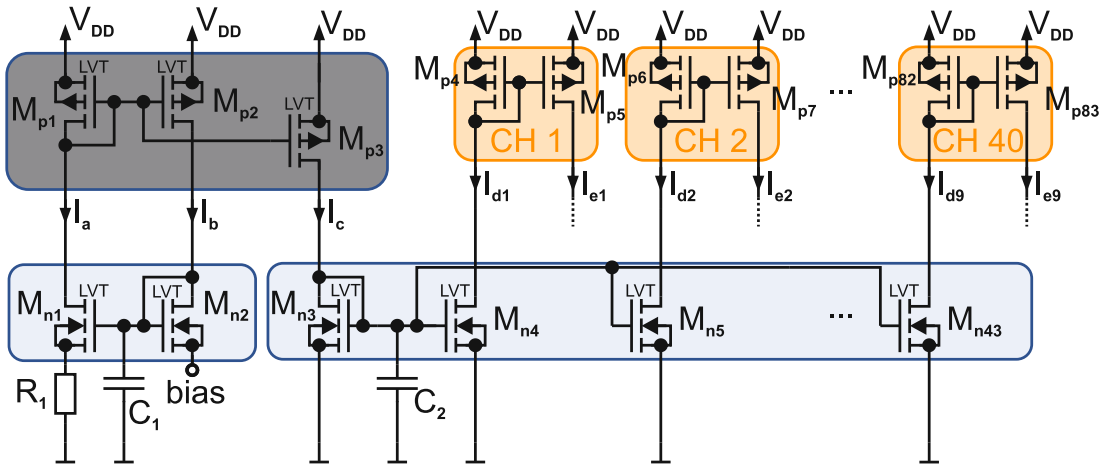


Figure 87: Simplified Circuit diagram of a bias current distribution with LVT MOSFETS.

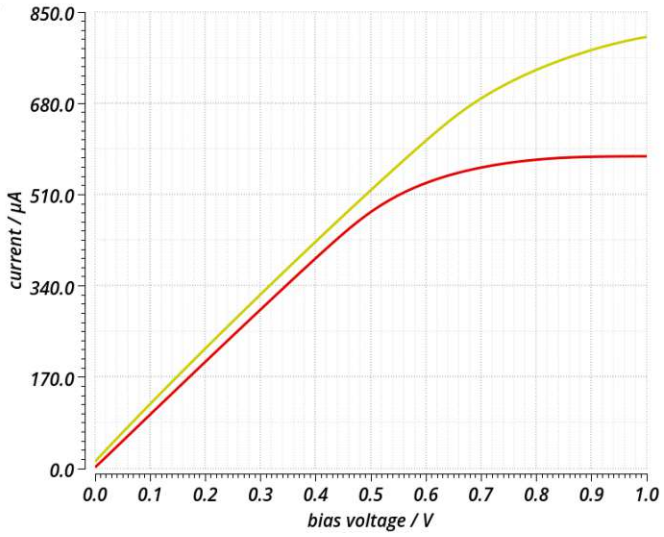


Figure 88: Simulated generated bias current versus input bias voltage (red: normal MOSFETs, yellow: LVT MOSFETs).

In addition, a new version of the double cascoded switch (driver) was investigated and optimised by circuit simulation to achieve minimum rise/fall times at a voltage swing of 9.9 V to reduce dynamic power consumption. A simplified version of the improved PWM driver and level shifter is shown in Figure 89. It again uses double cascoding of 3.3 V transistors to obtain the voltage blocking capability for the 9.9 V used to drive the heating resistors on the PIC. Due to double cascoding, adaptive gate biasing had to be implemented for M_{n7} and M_{p7}. Two bias voltages (V_{bias1} = 3.3 V, V_{bias2} = 6.6 V) are necessary for the gates of the cascode transistors to keep the drain-source voltages in the allowed range. Transient simulations showed that the maximum drain-source voltages of the transistors in the output path can be exceeded during switching, even with the protection diodes used in the first run. Therefore, protection diodes and a snubber (R_1 and C_3) were investigated, which reduce these peak voltages. To drastically reduce the static power consumption of the level shifter used in the first run, a completely new capacitive level shifter design was investigated to control the gate of M_{p5}.

The capacitive level shifter uses the capacitors C_1 and C_2 to couple fast signal edges (transitions) from the lower voltage domain V_{in} (0 V to 3.3 V) to the higher voltage domain (6.6 V to 9.9 V) at the gate of M_{p5}. The capacitors do not pass the full DC signal but instead transmit changes (edges) in voltage, which are then interpreted at the higher voltage domain. When the input changes from low to high (or high to low), the capacitors cause brief voltage spikes on the receiving sides and cause the cross-coupled inverter latch (INV_4 and INV_5) to eventually toggle and store the logic level until the next transition occurs. A series of inverters (DRV_4) is used to drive the gate of M_{p5}. The first CMOS inverter within the driver circuit (DRV2) is designed with a shifted switching threshold to minimise the pulse width distortion resulting from the transition in the supply voltage from 0 – 1.8 V to 0 – 3.3 V. The new principle increased the switching speed and significantly reduced static power consumption. A disadvantage is that the level shifter only detects transitions (edges) of the input signal, since the capacitor only transmits transient voltage changes (edges). If the input pulse is very short, one of the edges (either rising or falling) could be missed or inadequately captured, potentially causing incorrect logic levels at the output. In the worst-case scenario, quenching and charging could be activated at the same time, causing a short circuit.

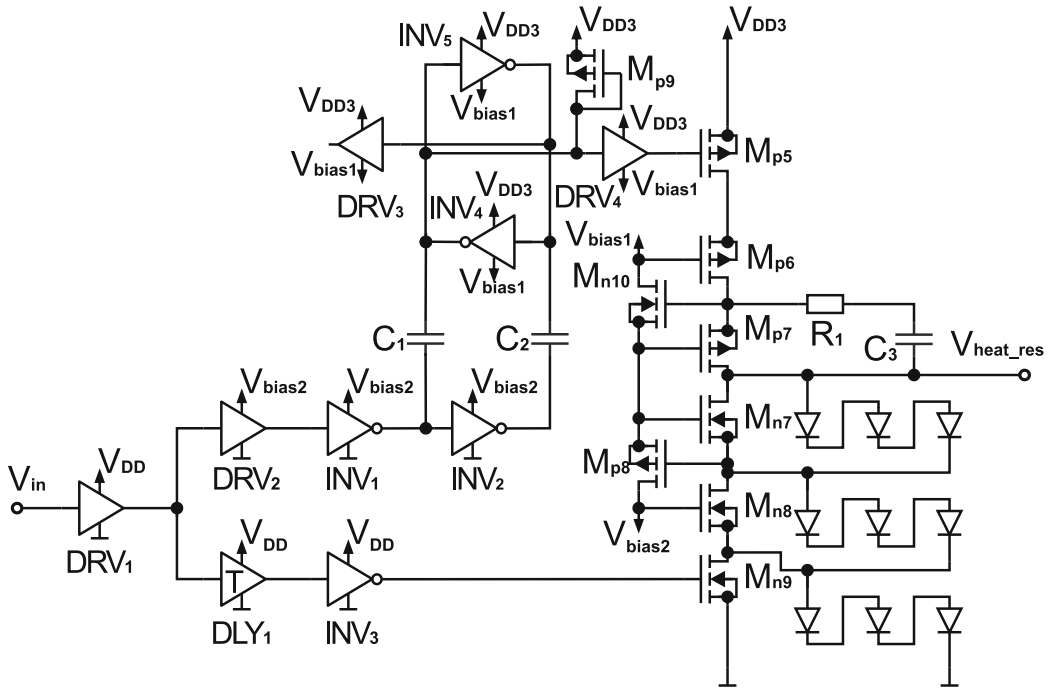


Figure 89: Simplified circuit diagram of the PWM driver in run 2.

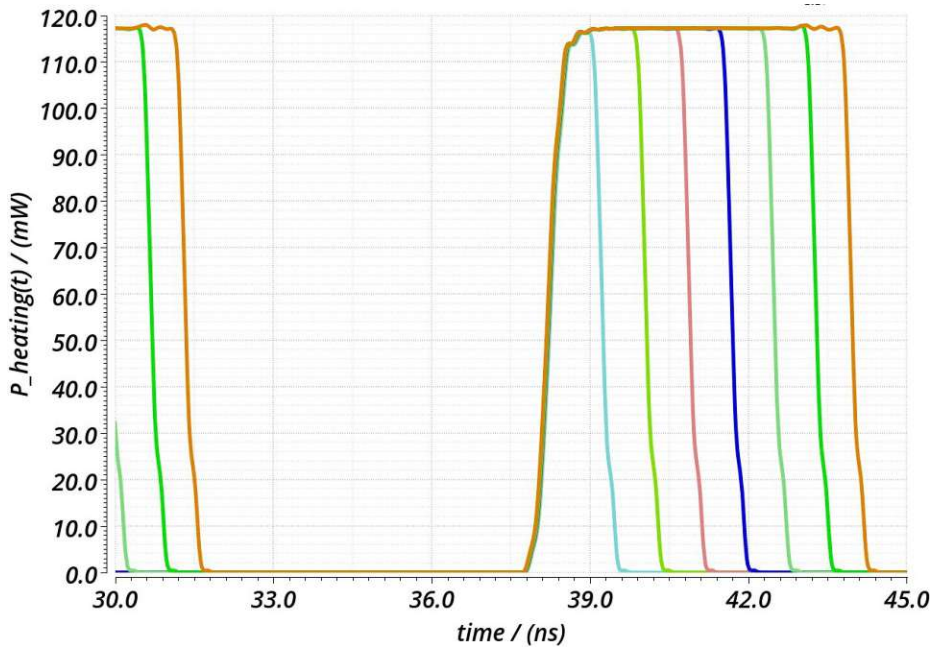


Figure 90: Transient heating power at a 750 Ω heating resistor for decimal values from 1 to 255 obtained by post-layout circuit simulation (run 2).

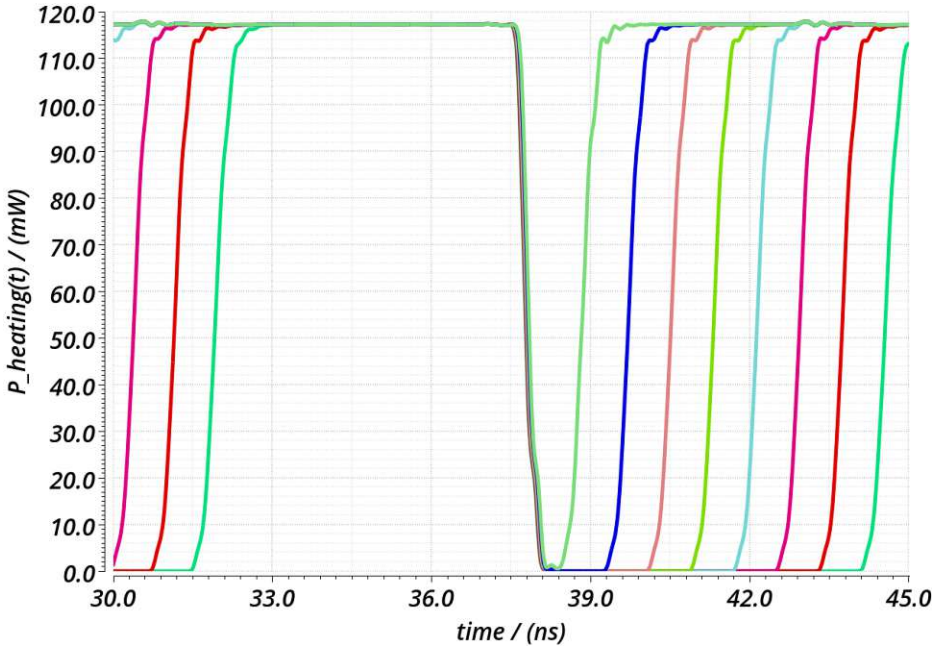


Figure 91: Transient heating power at a 750Ω heating resistor for decimal values from 256 to 511 obtained by post-layout circuit simulation (run 2).

Figure 90 shows the heater power with a duty cycle from 0 to 50 % and Figure 91 shows the heating power with a duty cycle from 50 to 100 % obtained from post-layout circuit simulations. Heater powers from 0 to 117 mW are obtained for a 750 Ohm resistor according to Figure 92. According to Figure 90, the 80%-to-20% fall time of the heater current is 0.21 ns and the 20%-to-80% rise time is 0.33 ns and, which is faster compared to the post-layout simulation results in the first ASIC run (rise time 0.35 ns and fall time 0.36 ns). The switching speed includes the capacitive load of two bond pads, as well as the capacitance and inductance of 3 mm long metal lines on the PIC. These switching speeds are excellent for a 9.9 V swing considering the load. The static power consumption reduces from approximately 460 mW (corresponding to 11.5 mW per channel) in the first ASIC run to approximately 104 mW (corresponding to 2.6 mW per channel), which is a significant reduction of approximately 77 %. This will considerably reduce the heating of the photonic IC by the 3D-mounted PWM ASICs.

The PWM ASIC was designed for fabrication on standard wafers in the XH018 CMOS technology. There are two versions of the PWM ASIC with differences, especially in the switch (driver) and the bias distribution. The second version is produced to have a backup version, which includes more parts of the PWM ASIC produced in the first run and is proven to work. The PWM drivers and the bias current distribution are identical to the circuitry used in the first ASIC run in this

version for risk reduction. For 3D integration both versions got a second bond pad row on all sides and a circular shaped passivation opening at the pads, to match the flip-chip process requirement of an equal pad density on all sides. For flip-chipping,

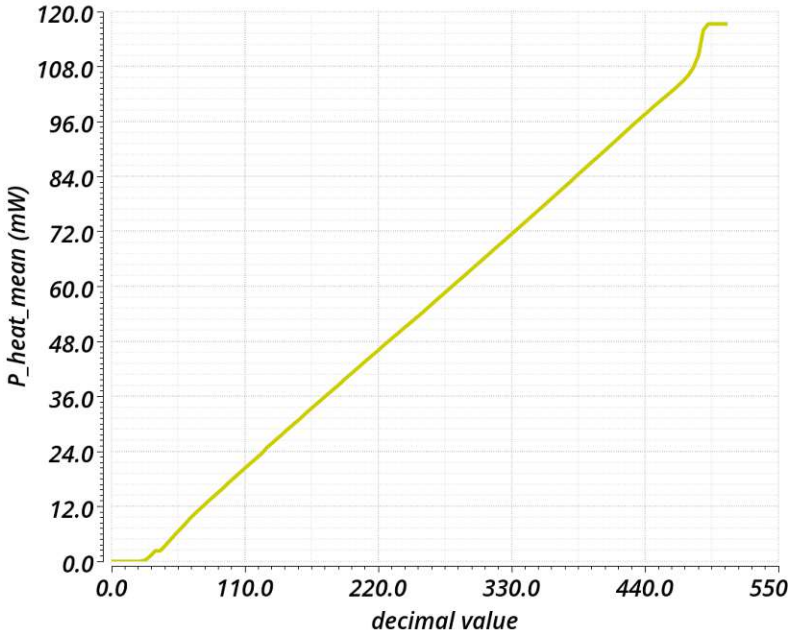


Figure 92: Heater power in a 750Ω heater resistor for 9-bit values from 1 to 511 obtained by post-layout circuit simulation (run 2).

A new PWM ASIC aux chip was designed for easier testing of the PWM ASICs, which can be directly bonded to a PWM ASIC outputs. The chip includes 40 heating resistors (750 Ω) and eight integrated photodiodes to characterise the PWM and monitor channels of the PWM ASICs. The pads are designed in a way that it can be directly glued next to a PWM ASIC and wire-bonded from chip pad to chip pads. It enables a fast characterisation of all channels because the previously used discrete resistor arrays do not provide enough channel to test all PWM channels without new bonding.

The layout of the improved PWM ASIC and a zoomed part is shown in Figure 93. The dimensions of the PWM ASIC are about 1.5 × 8.7 mm^2. The chip area of one channel is approximately 170 ×440 μm^2 and is presented in Figure 94 (a). A channel from the 'PWM ASIC backup' chip is sown in Figure 94 (b). The main difference between these two channel versions is the level shifter, the snubber, and the protection diodes in the PWM driver (marked yellow).

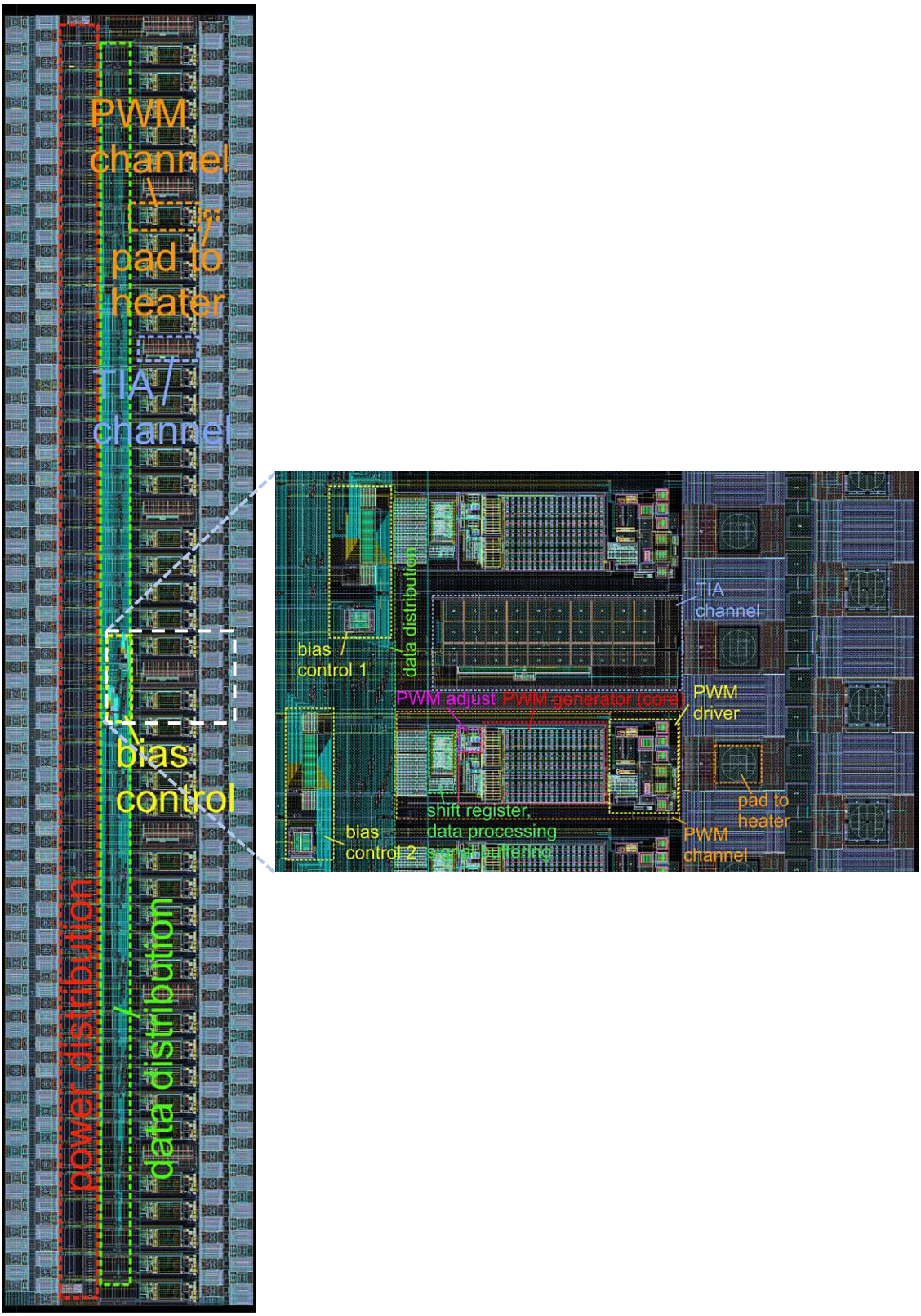
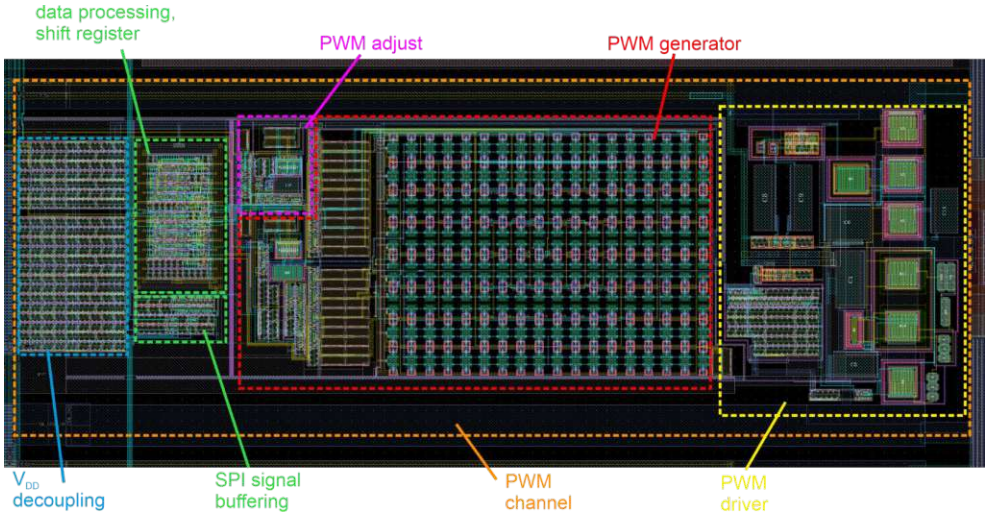
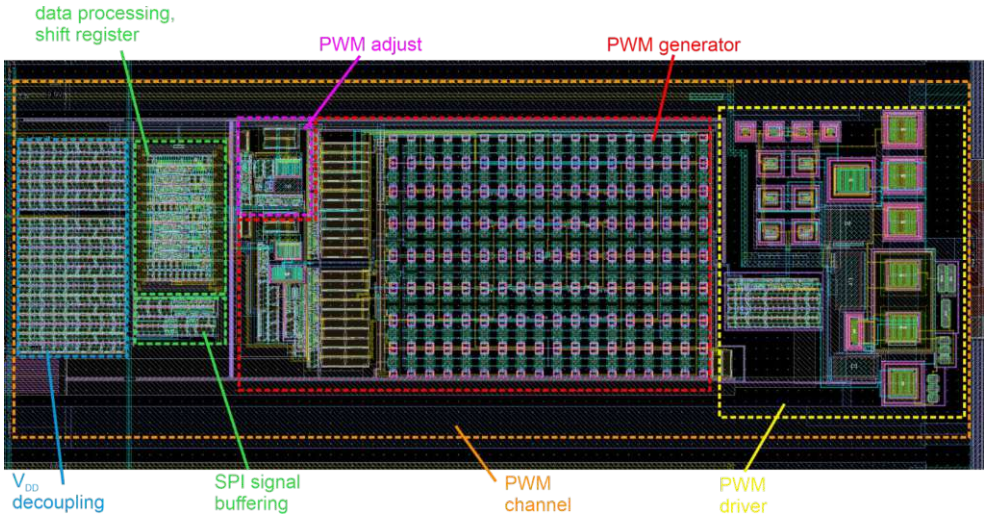


Figure 93: Layout of the PWM ASIC run2 for 3D-integration.



(a)



(b)

Figure 94: Layout of a PWM channel run 2. (a) normal version. (b) backup version.

In order to test the new chips, the test-PCB was also adapted and some improvements were made. As the size of the chips has changed in the second run, mainly due to a second bond row for flip-chip bonding, the PCB is also adapted to the new ASICs. Some components were changed due to the availability of parts or to improve performance. In particular, ESD-sensitive capacitors with a breakdown voltage of 11 V are mainly replaced by versions with a breakdown voltage of 16 V. These capacitors have a slightly higher series resistance and are therefore less able to stabilise very fast voltage drops, but this change should significantly improve the robustness of the PCB during soldering and bonding. In the first version, some capacitors were shorted after soldering or bonding and had to be detected with a thermal image and replaced. The new PWM ASIC aux chip can be

glued directly next to the PWM ASIC on the PCB. This should make it possible to characterise all channels of a PWM chip and reduce the inductance between the outputs and the heaters, making the test setup more comparable to the final quantum simulator configuration. Figure 95 shows the layout on the left and a rendering of the test-PCB on the right. The PCB has a size of 65 x 100 mm and consists of 6 layers to route the various signals and supplies. The PCB has a defined layer buildup, which ensures that the clock and digital output signals can be routed with traces with 50 Ohm characteristic impedance. This minimises signal loss and reflections, resulting in efficient signal transmission. The test-PCB and the diced ASICs from the second production run already arrived and are pending for characterisation at the moment of writing this dissertation.

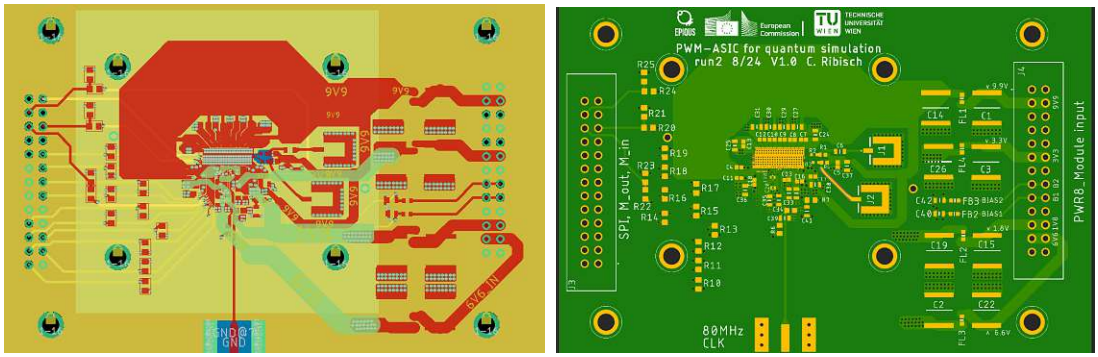


Figure 95: Test-PCB for the PWM ASIC with PWM ASIC aux-chip test-PCB (left: layout; right: rendering).

4. Quantum Simulator System

The complete quantum simulator system including the ASICs designed in this dissertation and the PIC designed by project partners was assembled in the configuration shown in Figure 3. The system PCB was designed by project partners. Figure 96 shows the first system integration with four PWM ASICs, one external Gater, and the PIC in the middle glued on the Hostboard PCB. The complete PCB set-up with power supplies on the mainboards and a FPG board on the backside is shown in Figure 97. The FPG is used to process the data coming from the Gater, communicate with the PWM-ACIS, synchronises all chips, and control the power supplies.

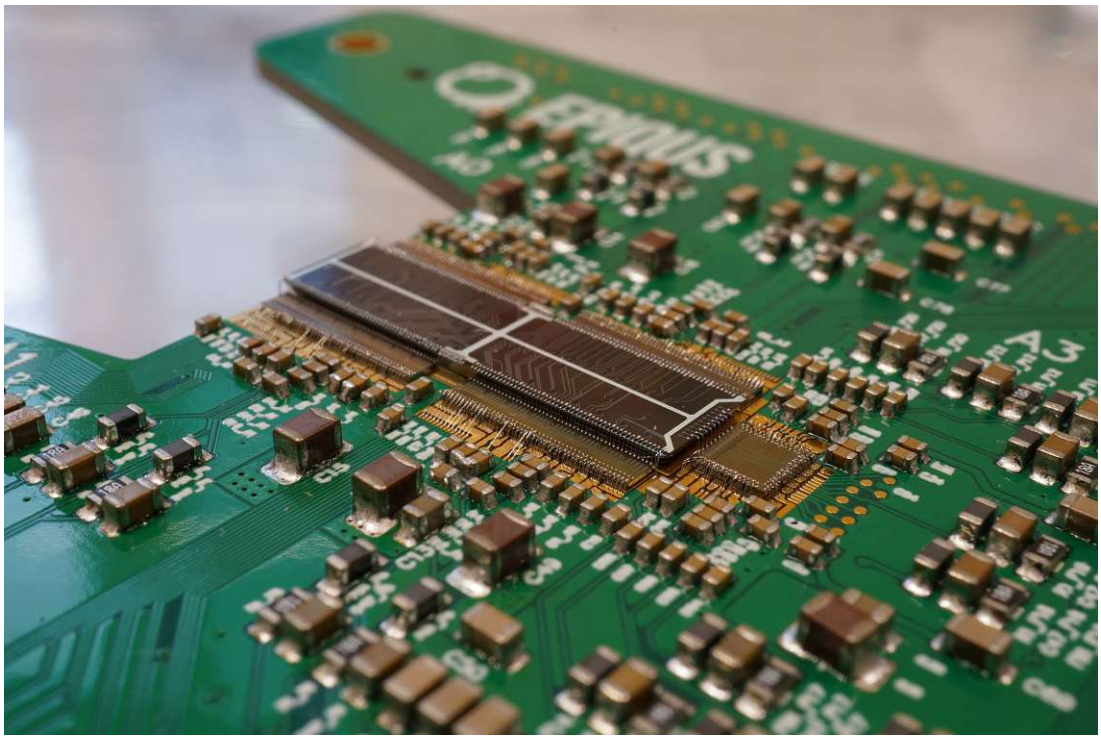


Figure 96: Quantum simulator Hostboard PCB with ASICs and PIC.

The whole system was successfully powered up and the principal function of the chips were tested. The Gater ASIC generated digital output pulses as expected. The digital output pulse duration behaved for different clock cycles as expected, and the count rate increases with more injected light. The PWM ASICs were tested with different combinations and the temperatures were monitored with a thermal camera. For example, Figure 98 shows the configuration when every channel is

powered on. The not calibrated camera shows temperatures peaks of 84.1 °C in the centre of the heaters. The ASIC stays relatively cool compared to the PIC.

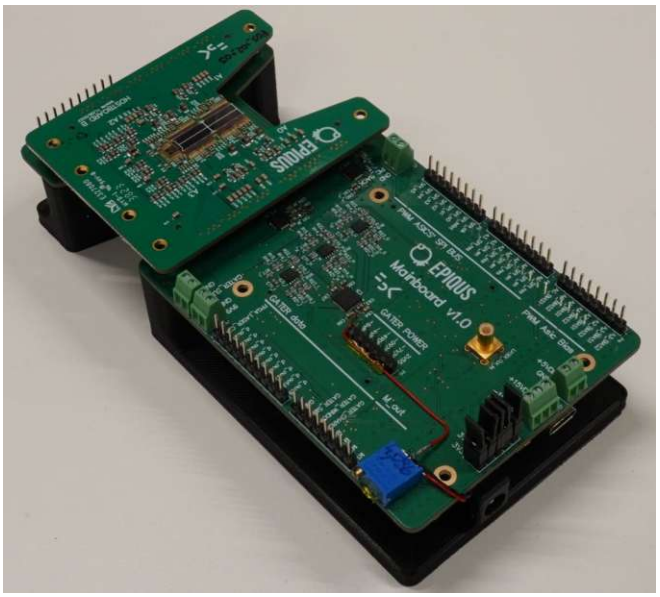


Figure 97: Quantum simulator PCB setup including FPGA for data processing on the backside.

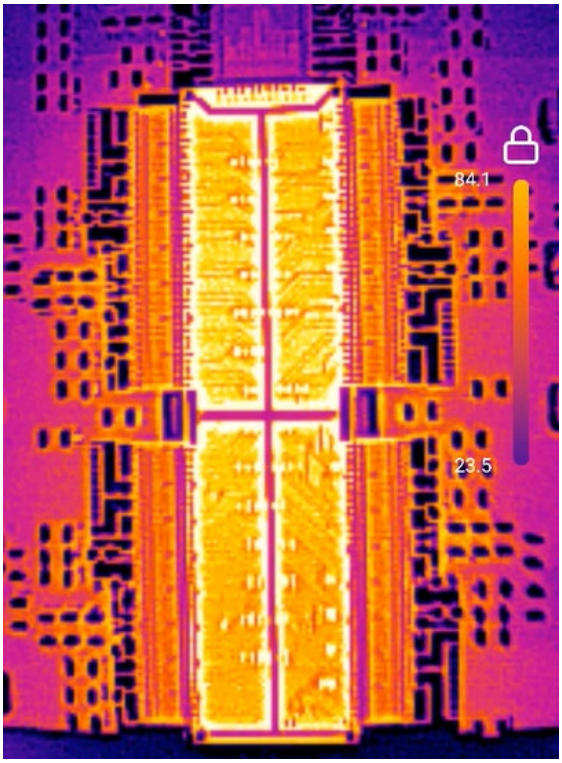


Figure 98: Thermal image of the quantum simulator hostboard with all channels fully on.

Figure 99 shows on the left a configuration where all heaters connected to ASIC 3 are active. Individual heaters are clearly visible in this picture. On the right picture of Figure 99 one single heater, connected to a channel of ASIC 4, is active. The

pictures clearly show a thermal crosstalk if many heaters are active. The heating of larger parts of the PIC might also be a problem of the thermoelectric cooler.

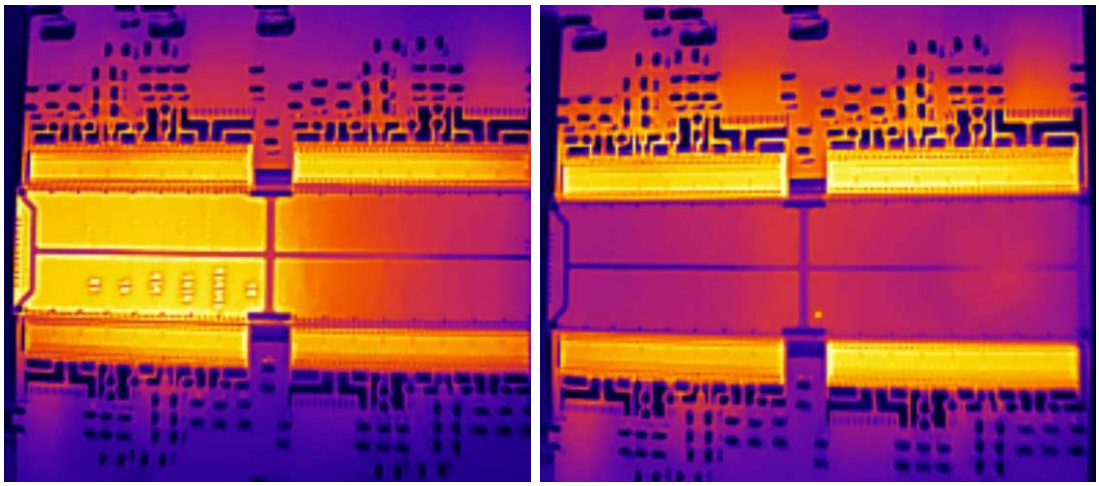


Figure 99: Thermal image of the quantum simulator hostboard with all heaters active on ASIC 3 (left) and one heater active on ASIC 4 (right).

This first commissioning was a full success, but further measurements and experiments need to be conducted. At the moment of writing this dissertation, further characterisations are ongoing. All chips for the second system integration with 3D integration (flip-chip) are diced and are ready to be flip-chip mounted. At the moment of writing this dissertation, the flip-chip quantum simulator system was not assembled yet.

4.1 Conclusion

The proposed Gater ASIC with integrated SPADs in 0.18 µm CMOS advances over prior designs by increasing the excess bias voltage from 6.6 V to 9.9 V, thus improving the photon detection probability (PDP) from ~35 % to ~50 % (635 nm). [62] However, the measured PDP is significantly lower than the estimated PDP from device simulations (~72 %) and the 67.8% PDP reported in [52] in 0.35 µm CMOS process at 642 nm with an excess bias of 9.9 V. Therefore, the SPAD developed by a colleague did not meet expectations and needs further improvements. Further analysis suggests that the reduced performance may be attributed to a high sensitivity of the developed SPAD's PDP to process variations. The circuit itself demonstrates enhanced dynamic performance, including a quenching time of 0.28 ns and a high slew rate of 28.3 GV/s. The integrated SPADs exhibit superior PDP relative to standard InGaAs SPADs (~25% at 1.55 µm).

The Gater ASIC with external SPADs in the PIC yields highly favourable results for quantum simulation, with a remarkably low dark count rate (10 – 100 counts/s) and a high photon detection probability (~70%), surpassing performance observed in 0.18 µm X-FAB CMOS SPADs. The results are much better than the 67.8 % PDP and the 63.000 dark counts/s with an excess bias voltage of 9.9 V (642 nm) in 0.35 µm CMOS reported in [52]. With the external SPADs, the proposed gating circuits can show its strengths. The extremely short gating windows are instrumental in achieving the observed low dark count rate. However, at gating frequencies above 40 MHz, the afterpulsing probability (APP) becomes excessive, limiting suitability for high-rate quantum simulation. Addressing this requires either reducing the photon rate or redesigning the SPADs to suppress the APP. A new PIC with optimised SPADs aimed at reducing APP is under fabrication but has not yet been characterised.

Both Gater ASICs support adjustable, synchronised and very short gating windows, which can be approximately 1 ns short and support a high repletion rate above 80 MHz. The designs are fully modular, enabling scalability to larger qubit systems.

The PWM ASIC presents a very efficient way to control the temperature of phase shifters on the PIC. Compared to a constant voltage or current regulator, the PWM approach offers theoretically power savings of more than 90 %. The designed ASIC implements 40 independent channels delivering up to 130 mW per channel with 9.9 V pulses and also integrates monitoring TIAs to overserve the light intensity on the PIC. The architecture outperforms prior designs in power output and scalability while maintaining low dynamic power consumption. The PWM approach significantly reduces the thermal load on the PIC, enabling compact, energy-efficient integration, and stable operation under a fixed thermal budget. Compared to constant current/voltage solutions, the integrated PWM approach offers superior efficiency and scalability for complex quantum photonic systems.

The results showed that the investigated electronic circuits, monolithically integrated within ASICs, in combination with a PIC, enable a fully integrated quantum simulator. The novel approaches implemented in these ASICs are inherently scalable, facilitating straightforward extension to accommodate an increased number of qubits in future quantum simulators. This developed methodology establishes the foundation for integrated photonic quantum simulators that feature large arrays of quantum gates and detectors.

5. References

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6. Appendix

6.1 Gating ASIC with Integrated and External SPADs

Table 7: Suggested initial values for adjusting the input bias voltages, simulated values at typical mean corner with 20 °C and a load capacitance of 410 fF on the Gater output (may vary greatly over PVT and actual capacitance)

pad	description	input voltage range	resolution	possible current	initial start value ext. Gater	initial start value int. Gater
charge	determines the SPADs charging time voltage which is applied at the pad generates a corresponding dc current out of the Pad	0 V – 1 V	< 1 mV	0 - < 1mA (“dc”´)	0.36 V	0.38 V
window	determines the gating window duration voltage which is applied at the pad generates a corresponding dc current out of the Pad	0 V – 1 V	< 1 mV	0 - < 1mA (“dc”´)	0.4 V	0.4 V
S&H	bias voltage for sample and hold stages for all channels determines indirect also the comparator threshold because it level shifts the input voltage of the comparator	0 V – 1.8 V	< 1 mV	< ±1 mA peaks	1.3 V	1.3 V

c_ref1 ... c_ref9	separate reference voltage for every comparator to determine the threshold to detect an avalanche	0 V – 1.6 V	< 1 mV	< ±1 mA peaks	0.90 V	0.90 V

Figure 100 to Figure 109 show the post-layout simulation result of the supply currents of the external Gater ASIC from the first run used to design the test-PCB. It should be considered that the current curves at the supply pads depend on different parameters (selected settings, line loop inductance, chip temperature, etc.). The simulations include bond wires, but no parasitics on the PCB. All power supply inputs need fast but also large capacitors placed as close to the pads as possible. The line loop should also have a very low inductance because of the fast current peaks needed for operation.

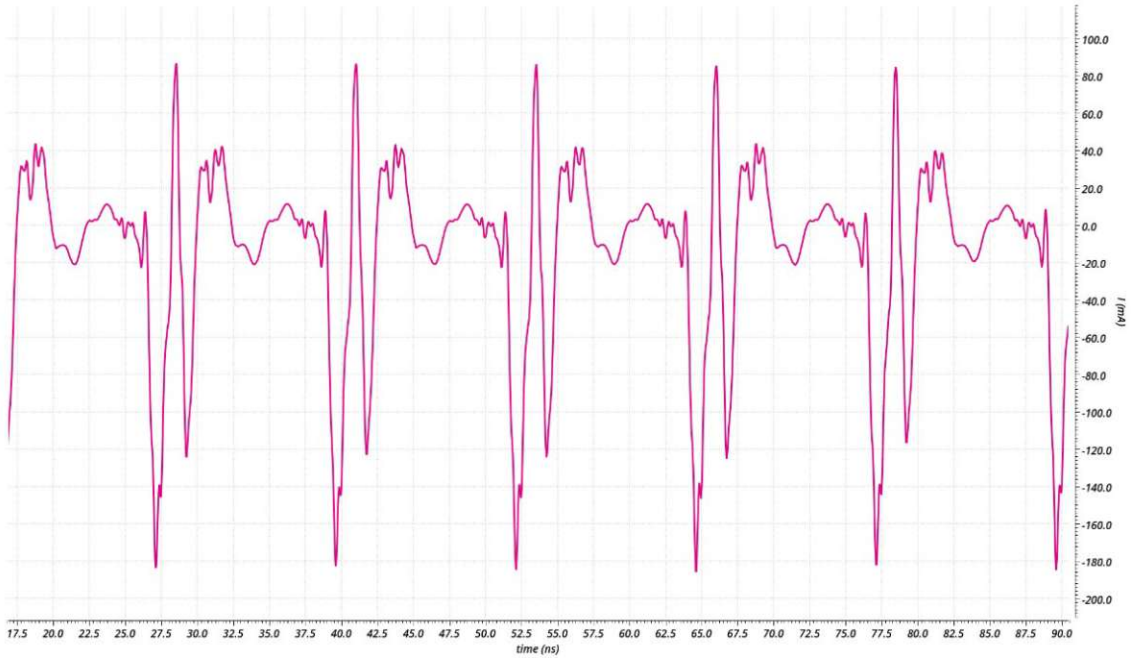

Figure 100: Post-layout simulation of 2.55V supply current (external Gater).

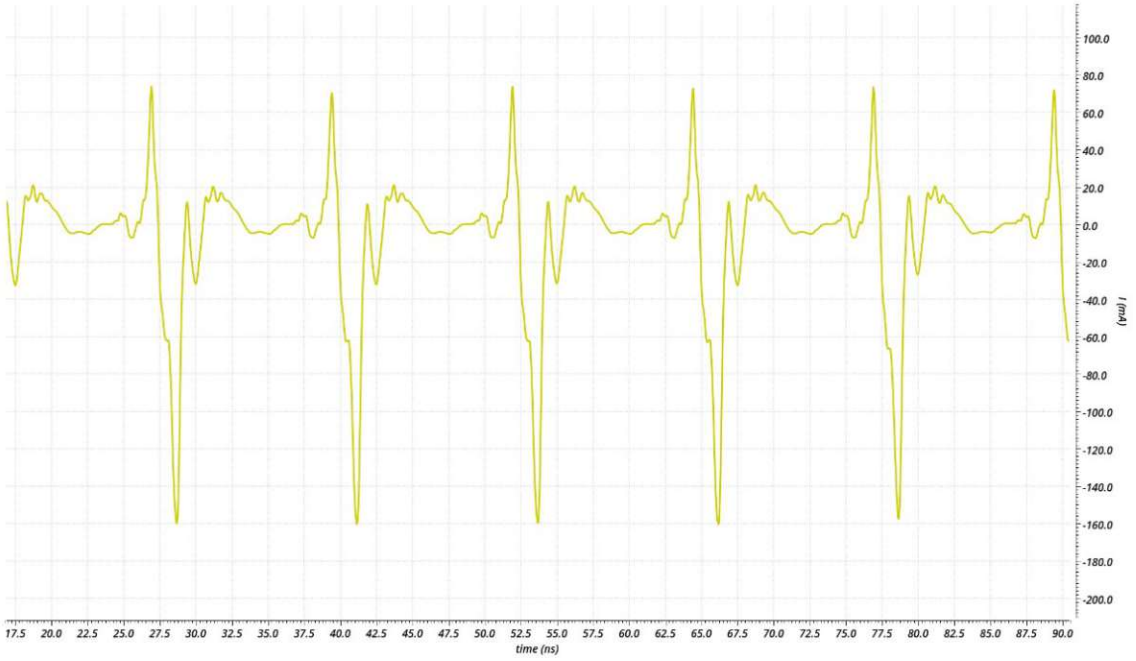

Figure 101: Post-layout simulation of -0.75V supply current (external Gater).

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Figure 102: Post-layout simulation of 4.05V supply current (external Gater).

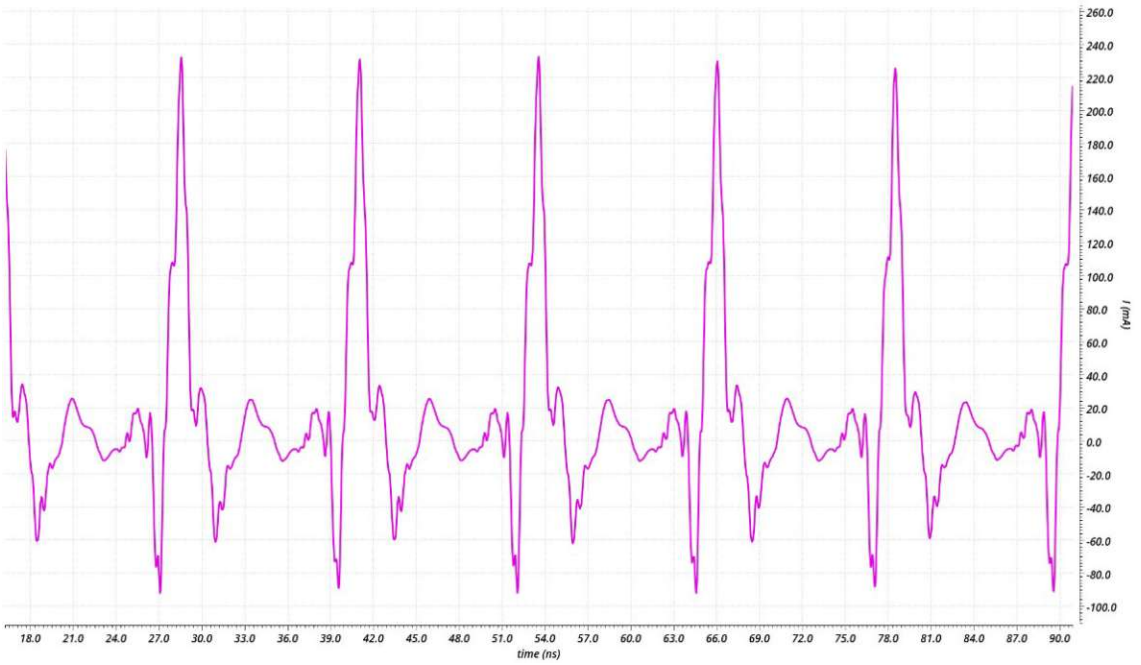

Figure 103: Post-layout simulation of -7.35V supply current (external Gater).

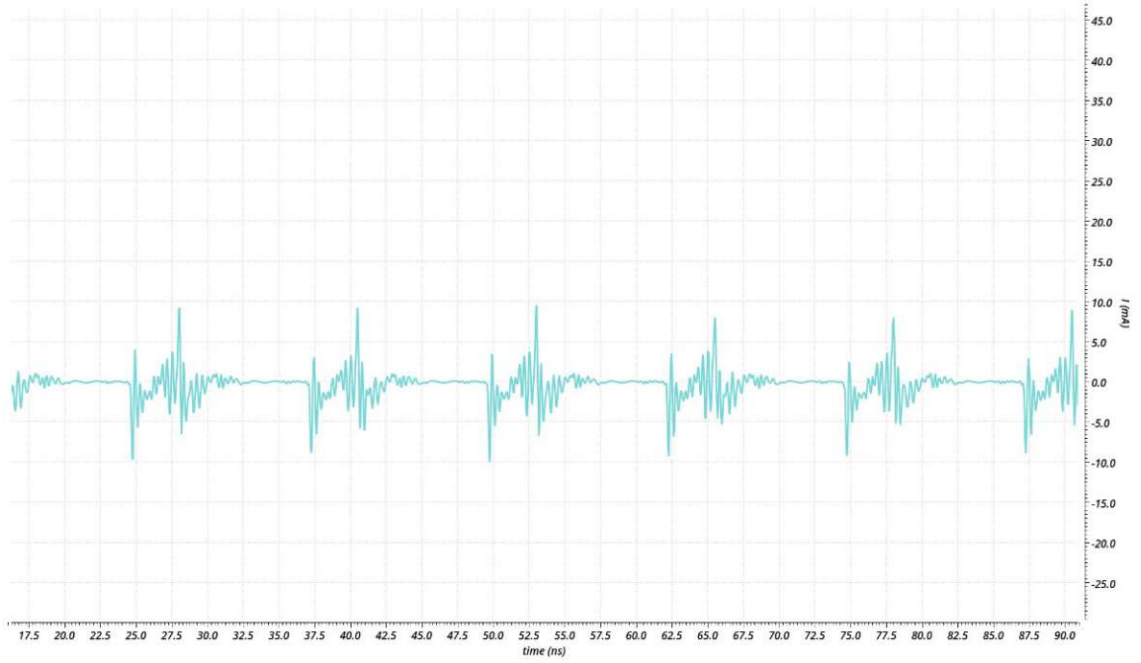

Figure 104: Post-layout simulation of -4.8V supply current (external Gate).

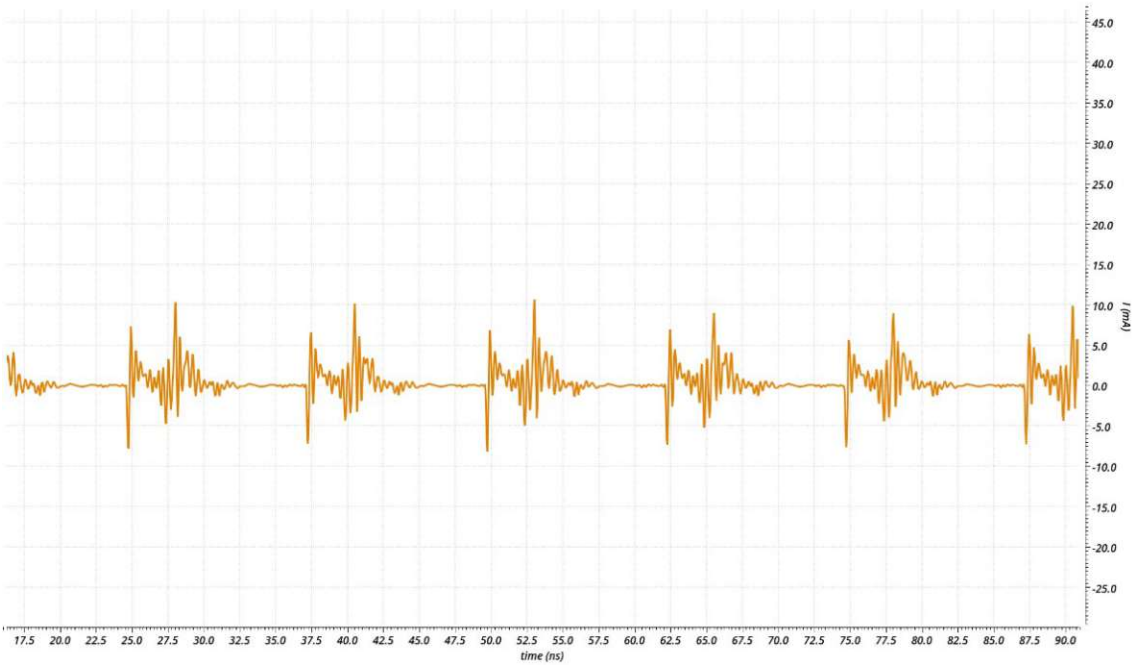

Figure 105: Post-layout simulation of -6.6V supply current (external Gater).

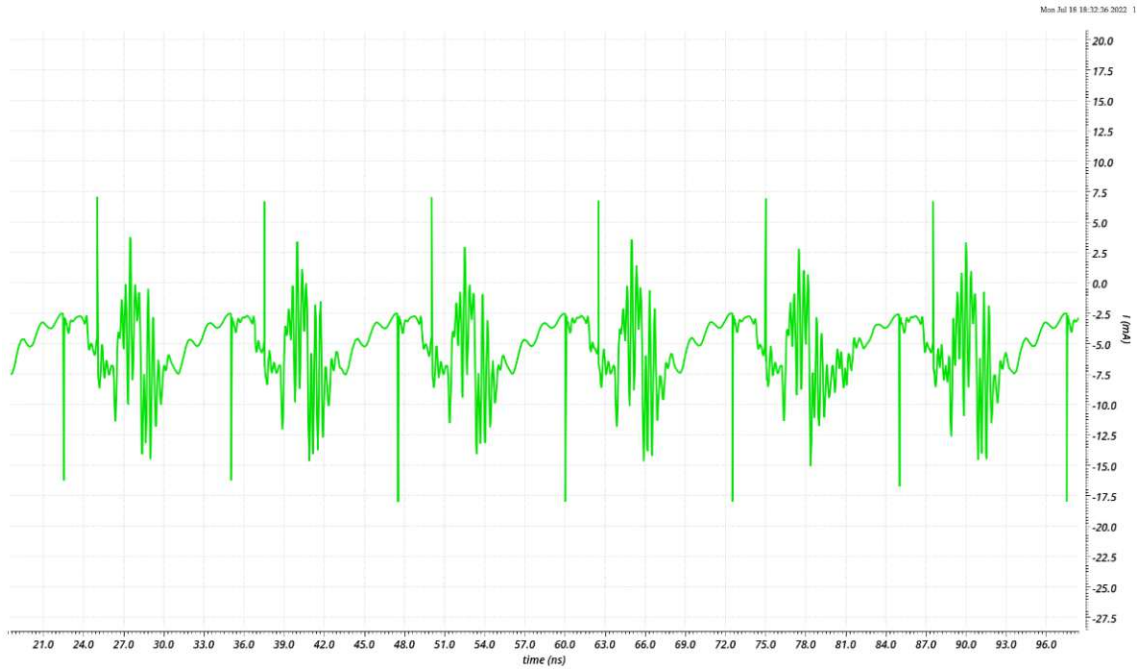

Figure 106: Post-layout simulation of 1.8V (without 1.8V_d) supply current (external Gater).

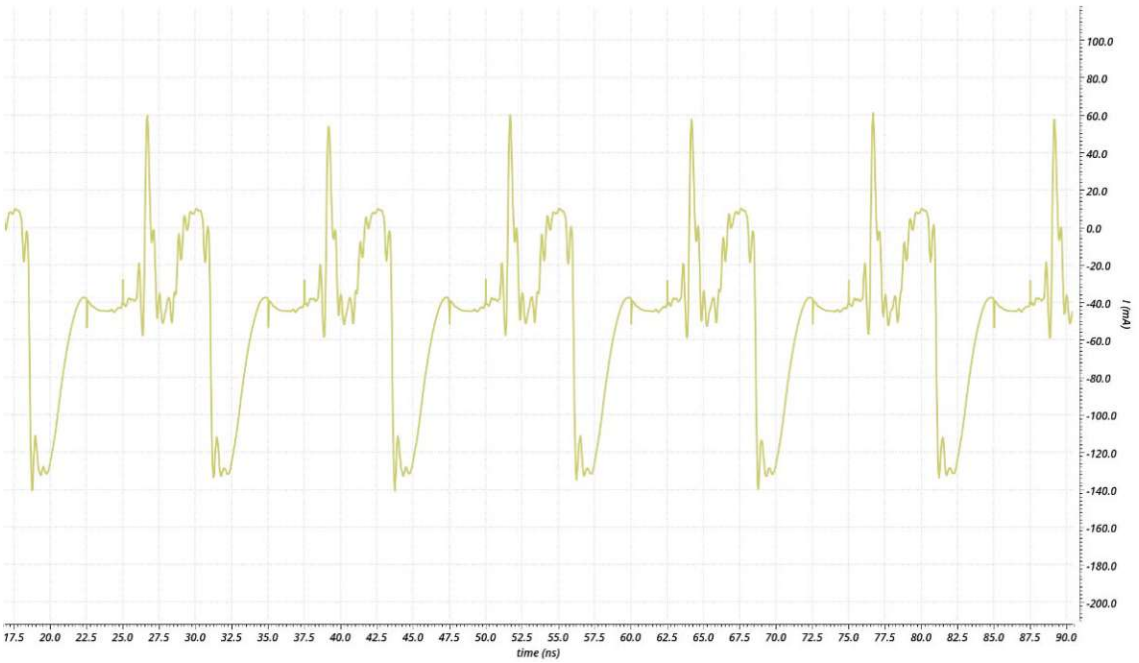

Figure 107: Post-layout simulation of 1.8V including 1.8V_d supply current (external Gater).

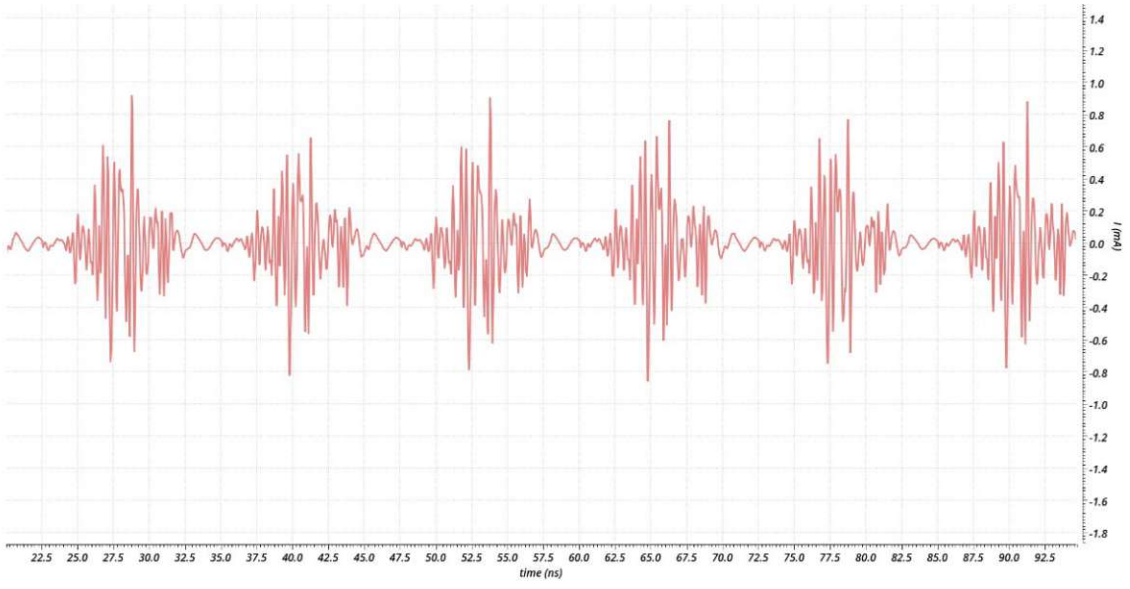

Figure 108: Post-layout simulation of C_ref1 pad current (external Gater).

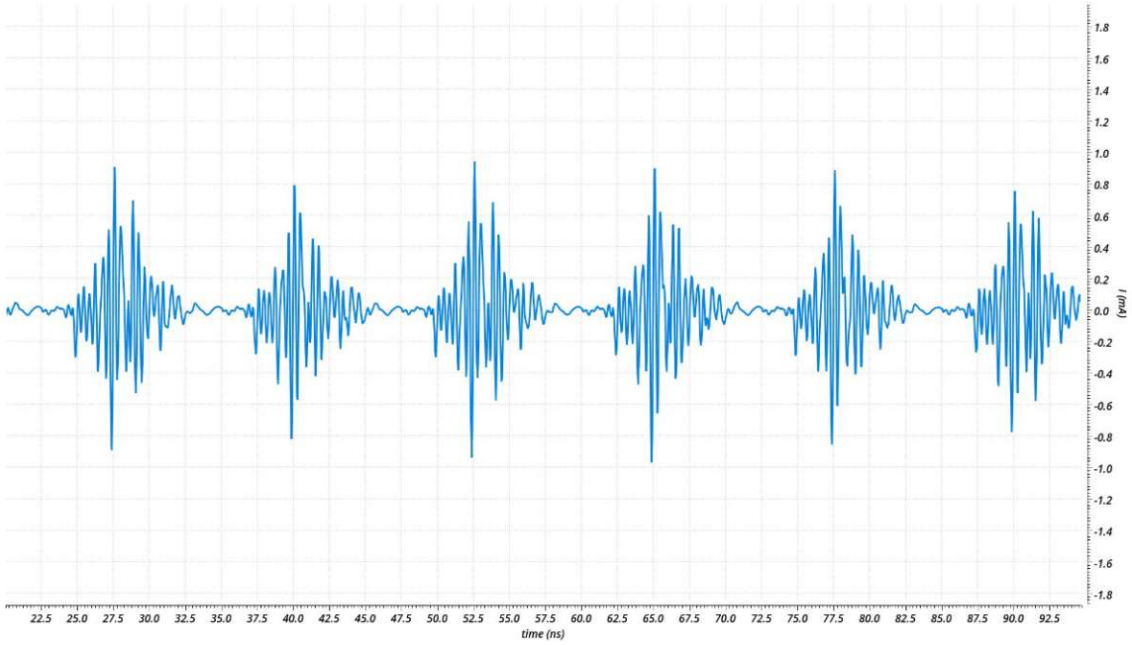

Figure 109: Post-layout simulation of S&H Bias pad supply current (external Gater).

6.2 PWM-ASIC

Figure 110 to Figure 114 show the post-layout simulation result of the supply currents of the PWM-ASIC from the first run used to design the test-PCB. It should be considered that the current curves at the supply pads depend on different parameters (selected settings, line loop inductance, chip temperature, etc.). The simulations include bond wires, but no parasitics on the PCB. All power supply inputs need fast but also large capacitors placed as close to the pads as possible. The line loop should also have a very low inductance due to the fast current peaks needed for operation.

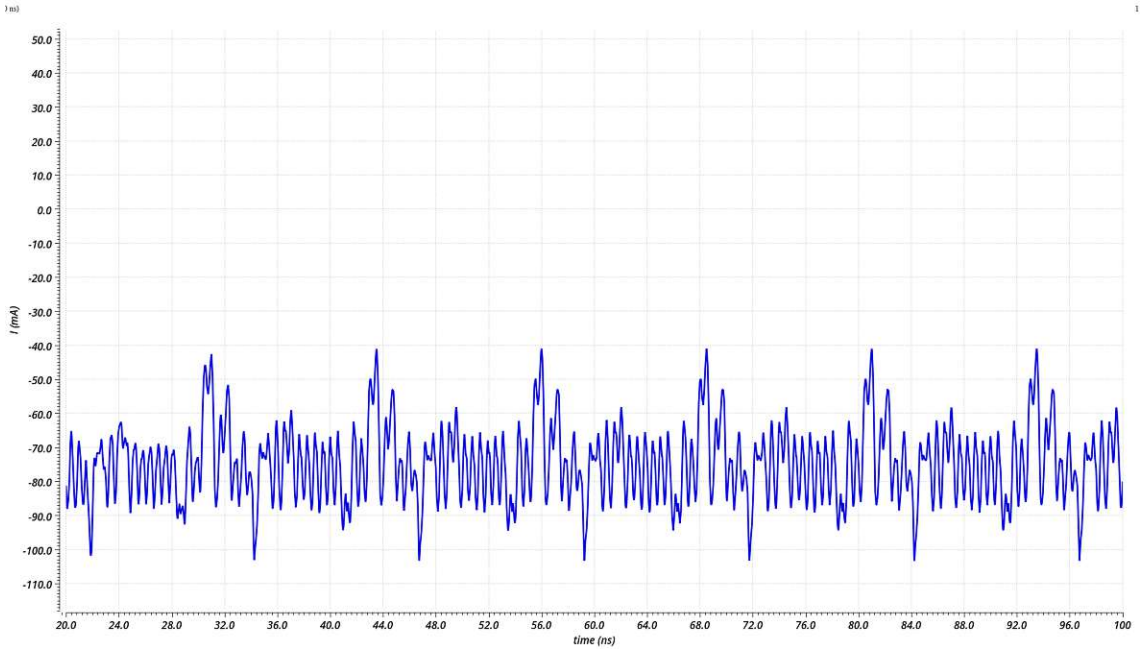

Figure 110: Post-layout simulation of 2.55V supply current (PWM ASIC without PIC).

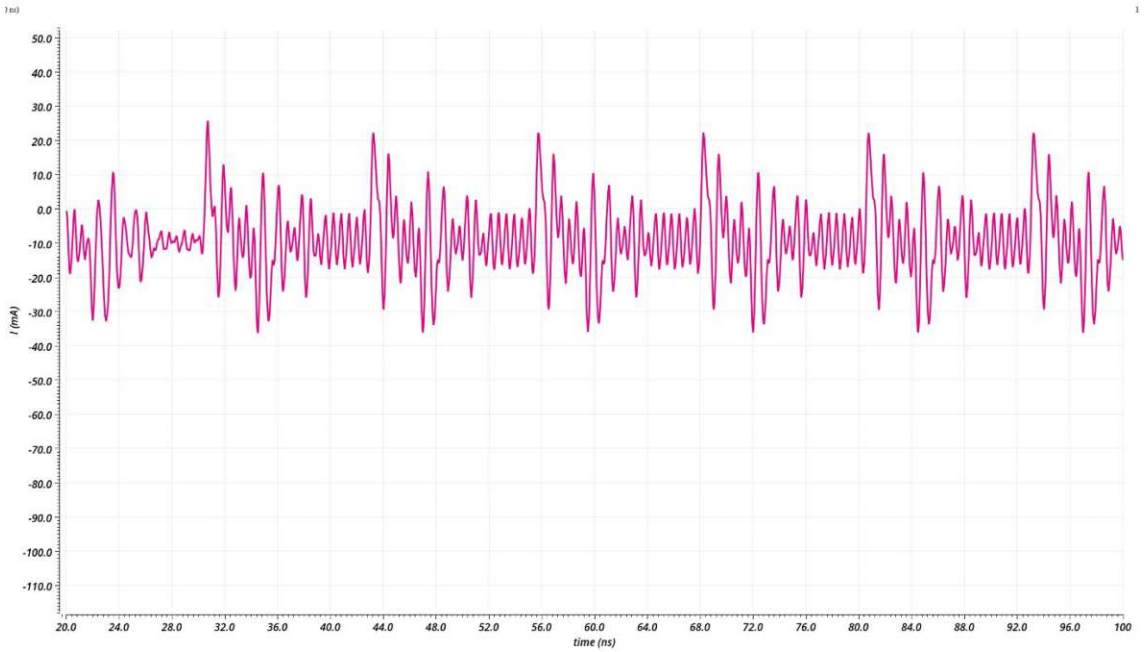

Figure 111: Post-layout simulation of 6.6V supply current (PWM ASIC)

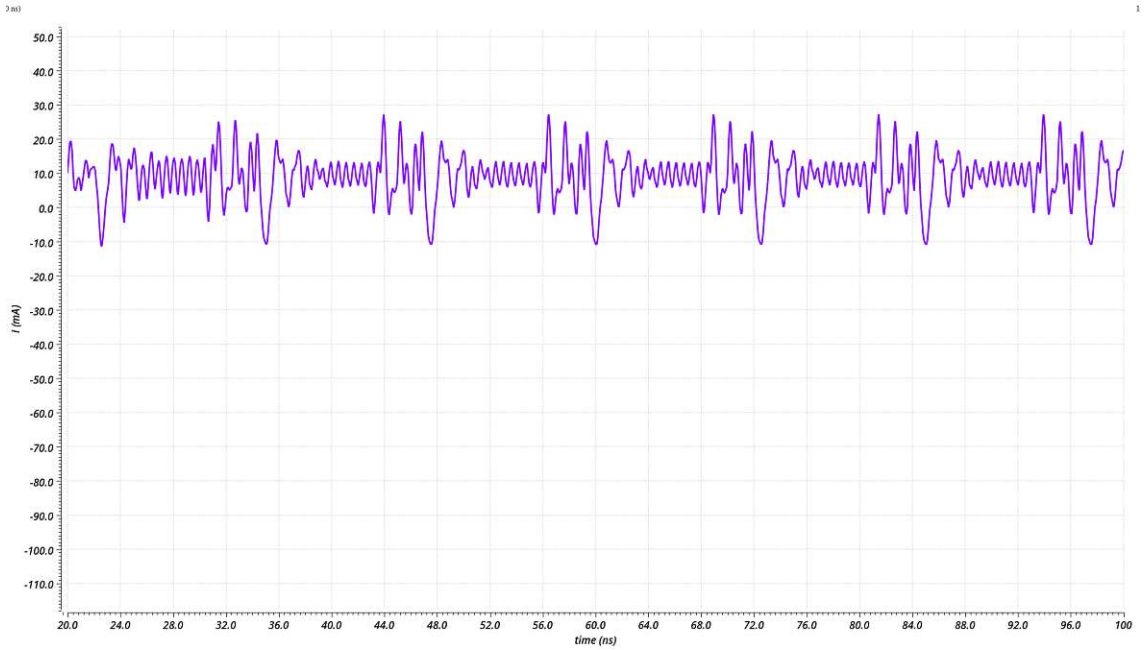

Figure 112: Post-layout simulation of 3.3V supply current (PWM ASIC).

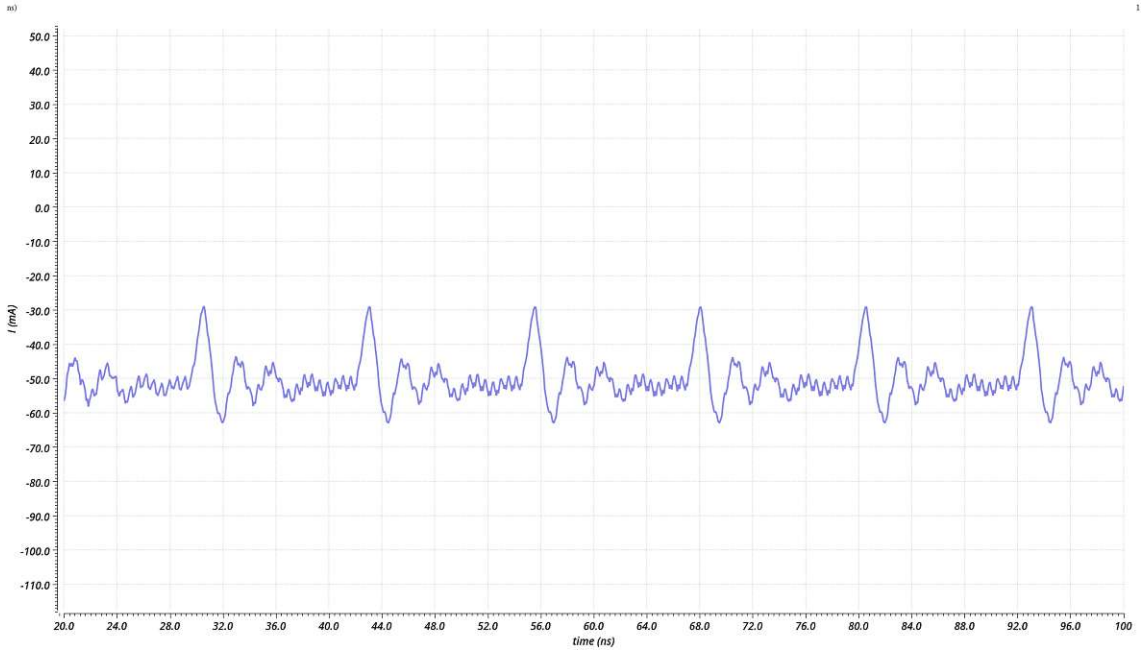

Figure 113: Post-layout simulation of 1.8V supply current without monitoring TIAs (PWM ASIC).

Figure 114: Post-layout simulation of 1.8V supply current for monitoring TIAs (PWM ASIC).

Overview of Generative AI Tools Used

Tool	usage
DeepL Translator	Used to translate text from German to English.
DeepL Write	Used to refine the writing, make spelling corrections and give suggestions for a better spelling.
Writefull	Used for proofreading and clarifying statements and make them more precise and clearer.
ChatGPT	Used to refine the writing, make spelling corrections, improve the writing of full sentences (rewrite(scientific)) and give suggestions for a better spelling.
DeepSeek	Used to make spelling corrections, improve the wording of whole sentences. (rewrite(scientific)) and give suggestions for a better spelling.

7. List of Own Publications

- C. Ribisch, M. Hofbauer, S. S. Kohneh Poushi, A. Zimmer, K. Schneider-Hornstein, B. Goll, H. Zimmermann, 'Multi-channel gating chip in 0.18 µm high-voltage CMOS for quanstum applications', MDPI Sensors, 2023, 23, 9644. doi: 10.3390/s23249644.
- C. Ribisch, M. Hofbauer, K. Schneider-Hornstein, A. Kuttner, M. Jungwirth, H. Zimmermann, 'Multi-channel PWM heater control chip in 0.18µm high-voltage CMOS for a quantum simulator', IEEE Photonics Journal, Vol. 16, No. 3, pp. 1-8, 7500208 (2024), doi: 10.1109/JPHOT.2024.3396213.
- C. Gasser, C. Ribisch, S. M. Laube, K. Schneider-Hornstein, and H. Zimmermann, "Ultra-Sensitive Reset-Less Integrator-Based PIN-Diode Receiver with Input Current Control," IEEE Solid State Circuits Lett, 2024, doi: 10.1109/LSSC.2024.3520338.

STATUTORY DECLARATION

I hereby declare that I have prepared this thesis in accordance with the Code of Conduct - Rules for Safeguarding Good Scientific Practice, in particular without unauthorised assistance from third parties and without the use of aids other than those specified. Data and concepts taken directly or indirectly from other sources are labelled with the source. The thesis has not been presented in the same or a similar form in other examination procedures in Austria or abroad.

I further declare that I have used generative AI tools only as an aid and that my own intellectual and creative efforts predominate in this work. In the Appendix, 'Overview of Generative AI Tools Used' I have listed all generative AI tools that were used in the creation of this work.

Vienna, Mai 2025

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Christoph Ribisch