Hardware Model Checking Competition 2025

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***Abstract*—The Hardware Model Checking Competition 2025 (HWMCC'25) was the 13th competitive event for hardware model checkers. Affiliated to the 25th conference on Formal Methods in Computer-Aided Design 2025 (FMCAD'25) it took place in Menlo Park, California, USA, from Oct. 6 to 10, 2025.**

***Index Terms*—Automated Reasoning, Model Checking, Hardware Verification, Word-level Reasoning, Bit-Vectors, Certificates**

The *Hardware Model Checking Competition* in its 2025 edition (HWMCC'25) is the 13th incarnation in this series of competitive events to evaluate hardware model checking. Since it started in 2007 it was repeated annually with few exceptions. After the competition in 2020 the organizers took a break to resume the competition in 2024. The competition in 2025 was affiliated, as most of the time, with the conference on *Formal Methods in Computer-Aided Design* (FMCAD), which is considered the primary venue for formal hardware verification. In 2007, 2008, 2010 and 2014 it was affiliated with the conference of *Computer-Aided Verification* (CAV).

Since 2019, HWMCC features two *word-level* tracks, which focus on bit-vector models, one track *with arrays* and one *without arrays*, both in the BTOR2 format [1]. Prior to 2019, all competition tracks used *bit-level* models in the AIGER format [2], which were split into *safety*, *multi-property*, *liveness* and *deep* tracks. In 2024, participating model checkers submitted to the bit-level safety track were required to produce model-checking *certificates* [3]. These certificates are AIGER circuits that should have an inductive property and need to simulate the original circuit as formalized in [4], [5], [6]. The tool CERTIFAIGER was used to check both requirements using SAT solvers. The goal of the certified track is to increase trust in verification results produced by model checkers, following the success story of proof producing SAT solvers in both academia and industry, e.g., producing proofs became mandatory in the main track of the SAT competition in 2016 [7].

The introduction of certificates for the bit-level safety track of HWMCC'24 was a big success, with eight competing model checkers producing certificates. The model checkers were able to produce compact and correct certificates that were verified with minimal overhead. In HWMCC'24 the certifying winner of the bit-level safety track rIC3 [8] was even able to outperform the previous non-certifying state-of-the-art model checker ABC [9]. The results of mandatory certificates in HWMCC'24 demonstrated that certification can be adopted without compromising model checking efficiency [3]. The HWMCC'24 case-study [3] became a distinguished paper.

In 2025, the competition (HWMCC'25) continued with the word-level and bit-level tracks, but reintroduced the bit-level liveness track. In this track, participating model checkers were required to produce certificates for satisfiable liveness properties. Certificates for unsatisfiable liveness properties were optional, but may be required in future editions of HWMCC.

More details on the competition, including provided tools, submission procedure and deadlines, results and their presentation are available at https://hwmcc.github.io/2025.

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