Electrostatic Gating in Ge-Based Reconfigurable Field-Effect Transistors

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***Abstract*— Nanoscale Ge has been identified as a promising channel material to enable a reduction of power consumption and an enhancement of the switching speed of reconfigurable field-effect transistors (RFETs). Such multigate transistors allow the run-time switching between n- and p-type operation in a single device. In this work, the specific characteristics and benefits of dual- and triple-independent-gate Ge-based RFETs are discussed by a systematic temperature-dependent investigation of the electrical-gating-related charge carrier transport. While the dual-gate configuration features both a unipolar and ambipolar operation mode, the triple-gate configuration offers bias-independent unipolarity with a symmetric behavior regarding its gating capabilities and ON-state currents with an enhanced ON-to-OFF-state ratio by one order of magnitude.**

***Index Terms*— Electronic transport, germanium, multigate devices, reconfigurable field-effect transistor (RFET).**

I. Introduction

RECONFIGURABLE field-effect transistors (RFETs) [1] represent a promising novel device and circuit co-design methodology to progress beyond the More-Moore scaling paradigm that is limited in terms of functionality by the static and doping-defined character of the conventional CMOS technology. Distinctly, RFETs target application-adaptable alteration of the transistor's operation mode dynamically during run-time offering interesting applications for adaptive circuits [2], neuromorphic computing [3], and hardware security [4]. In general, to establish the ability of reconfiguration, there are various potential gate arrangements, such as back-gated (BG), dual top-gated (DTG), and triple top-gated (TTG) architectures [1]. To provide reconfigurability, it is necessary to have at least two independent gate electrodes. While the DTG arrangement is less demanding with respect to fabrication, the geometrical symmetry of the TTG configuration is an advantage in designing adaptive reconfigurable circuits, i.e., in logical circuits such as XNOR/XOR- and AND/NOR-switching logic cells [5], [6]. Ge, compared with Si as channel material, offers the possibility to increase the switching speed, thus reducing the dynamic power consumption while increasing the ON-state current due to its smaller band gap and effective charge carriers' masses and the resulting enhanced tunneling probabilities [7], [8]. Nevertheless, experimental implementations of Ge RFETs based on synthesized nanowires [7], [9] and Ge on insulator have fallen short in exhibiting the promised performance and power-efficiency enhancement predicted by theory. Encouraging results have been shown recently by the epitaxial integration of Ge on top of unstrained silicon-on-insulator (SOI) substrates [8]. Nevertheless, the Ge used in that work is strongly biaxially and compressively strained on (100) Si as its grown lattice matched, altering the band structure and thus the effective masses, band gap, and barrier heights compared with relaxed Ge. Moreover, the Ge layer thickness is limited to a few nanometers restricting the geometric design space of the devices. In this work, we focus on RFETs built from a thin pseudomorphically strained Ge layer grown on strained SOI substrates with the aim to obtain a Ge lattice more similar to bulk Ge and thereby approaching the inherent Ge properties. Furthermore, the electrical gating capabilities of RFET architectures and their abilities regarding symmetric unipolar operability are explored. Therefore, a temperature-dependent bias and gate voltage spectroscopy is conducted to identify the occurring charge carrier transport regimes and dominant current contributions.

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II. Device Fabrication

The starting point for the fabrication of the DTG and TTG RFETs, as presented in Fig. 1(a), respectively, was a 10-nm-thin pseudomorphically strained Ge layer on a 14-nm-thick strained Si (s-Si) layer on top of a buried oxide. Si buffers and Ge layers were grown via ultralow-temperature molecular-beam epitaxy (ULT-MBE) [10]. ULT-MBE is necessary to obtain a sufficiently thick Ge layer thickness supersaturation [11] that is practicable for realistic device applications. The s-Si-on-insulator (s-SOI) layer exhibits the

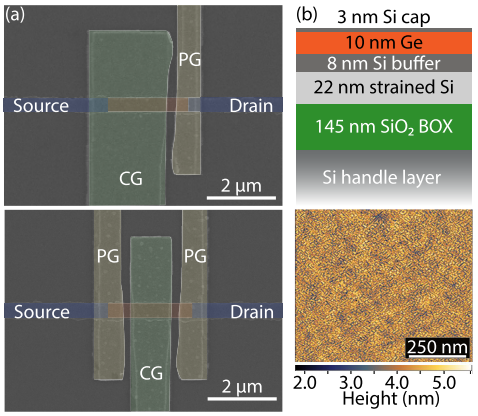

Fig. 1. (a) False-colored SEM image of a DTG with a channel length of 1.9 μm and a TTG RFET with a channel length of 1.7 μm. (b) Stack of the Ge on strained-SOI nanosheet structure and AFM scan of the top surface.

same in-plane lattice constant as a relaxed $Si_{83}Ge_{17}$ alloy but without the need of incorporating Ge, with the benefit that the Ge channel integrated on top can be electrically isolated more effectively from the buffer below. The corresponding wafer stack is depicted in Fig. 1(b) with the respective atomic force microscopy (AFM) image of the layer surface. The root-mean-square (rms) surface roughness is less than 0.5 nm confirming stable layer growth. The presence of the s-SOI layer reduces the lattice mismatch between Ge and Si, thus allowing for the growth of Ge layers as thick as more than 10 nm versus what could be obtained on relaxed Si [8]. The nanosheets with an average width of 450 nm were patterned via laser lithography and $SF_6 + O_2$ reactive ion etching (RIE). The used gate dielectric consists of a thermally grown SiO_2 (~8 nm) for interface stability and an ALD-grown high-k, ZrO_2 (2.85 nm). Detailed high-resolution transmission electron microscope images of the fabricated devices are shown in [12], showing an intact Ge layer after thermal oxidation of the Si capping layer. The Al source/drain (S/D) contacts were formed by a thermally induced exchange reaction [13] at T of 573 K, forming ultimately an Al/ultrathin-Si/Ge multiheterojunction [8]. Accordingly, DTG and TTG gate structures were fabricated by electron-beam lithography consisting of 10 nm Ti, defining the work function, and a 100-nm Au layer as bonding pads.

III. RFET Characteristics

To begin the discussion, Fig. 2 shows the transfer characteristics for DTG and TTG RFETs with the respective schematic band diagrams. The DTG arrangement, controlled by two gates, tunes only one injection barrier separately (PG), while the channel is gated together with the second barrier (CG). Instead, the TTG device decouples the charge carrier injection from the charge carrier modulation by the central CG using two connected PGs at the junctions. The corresponding transfer characteristics of various top-gated arrangements are presented in Fig. 2, revealing a comparison of general parameters as ON-state current ratio between n- and p-program and OFF-state current as well as threshold voltage shift of the devices. For both the TTG (black line in Fig. 2) and DTG (red line) configurations, the mode is set with the PG voltage of either 5 V for n-type or −5 V for p-type operation, while

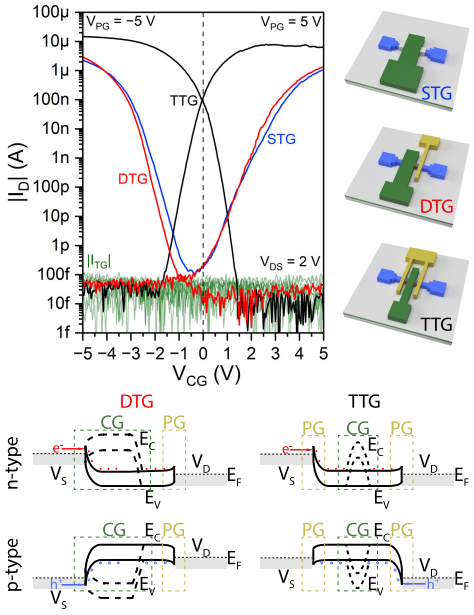

Fig. 2. (a) Comparison of STG, DTG, and TTG transfer characteristics operated with identical top-gate and bias voltages of $V_{DS} = 2$ V, applied either 2 V symmetrically, so that $V_D = -V_S$, or, in case of the DTG, asymmetrically, so that $V_D = \pm 2$ V and $V_S = 0$ V. The insignificantly low top-gate leakage currents I_{TG} are presented for all three devices (green curves). The lower panel shows the schematic band diagrams of the DTG and TTG RFET architectures.

sweeping the CG from 5 V to −5 V or vice versa. The bias voltage is applied symmetrically, meaning $V_D = -V_S$, for the TTG arrangement, whereas applied asymmetrically, so V_D is 2 V or −2 V for n-mode or p-mode, while keeping V_S to 0 V, for the DTG configuration. This is necessary to operate the RFET device in the unipolar regime, thus guaranteeing polarity setting and charge carrier filtering capabilities [14]. Importantly, the TTG structure allows the decoupling of the control of the tunneling barriers from the channel control. To set the reconfigurable structures in comparison to a Schottky barrier (SB) FET, the transfer characteristic of a single top-gated (STG) device is also given (blue line). Contrary to the RFET structures, the STG arrangement exhibits only one gate which covers both metal–semiconductor transitions and the channel region, resulting in an ambipolar behavior. Comparing the transfer curves of the individual structures, the TTG configuration provides the highest ON-state currents with an ON-state reached relatively lower CG voltages, approximately one order of magnitude higher than for the DTG and STG arrangements, by retaining an OFF-state current below 100 fA, resulting in an enhanced ON-to-OFF-state ratio for both the operation modes and an ON-to-ON-state ratio of approximately 2. In addition, the leakage current (green curve in Fig. 2) of all the configurations remains below the noise floor of the system.

IV. Gate and Temperature-Dependent Measurements of Dual- and Triple-Gated RFETs

With respect to its gating capabilities, also in dependency of the related applied bias voltage, Fig. 3 shows the PG-dependent transfer characteristic of a DTG configuration

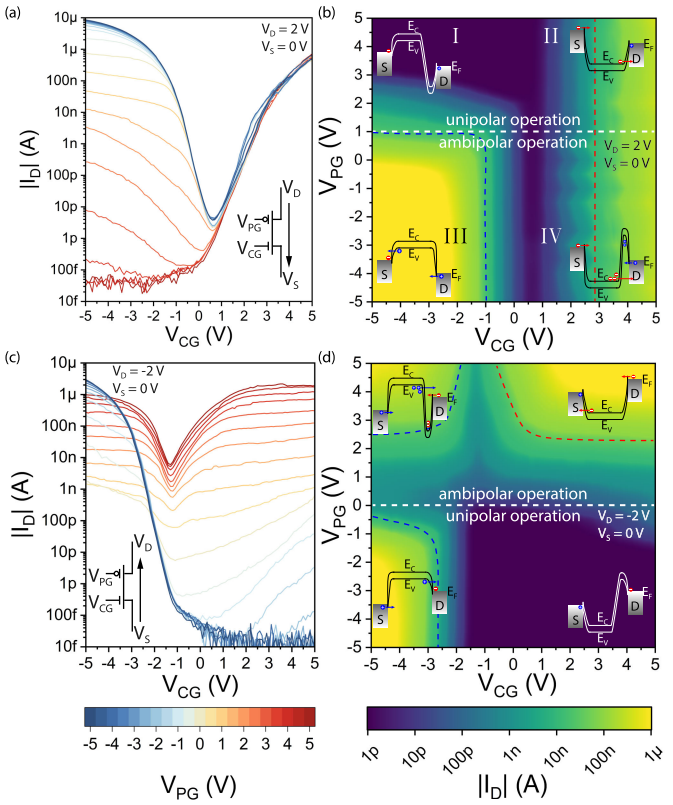

Fig. 3. Transfer characteristics of a DTG RFET with V_{PG} as parameter. (a) and (c) Conventional I–V curves and (b) and (d) corresponding transport map. (a) and (b) obtaining the switching situation with a positive bias voltage V_D of 2 V and V_S of 0 V, contrary to (c) and (d) with a negative bias voltage V_D of −2 V and V_S of 0 V. The insets show the circuit symbols, the associated bias directions, and the related band diagrams in accordance with the applied voltages.

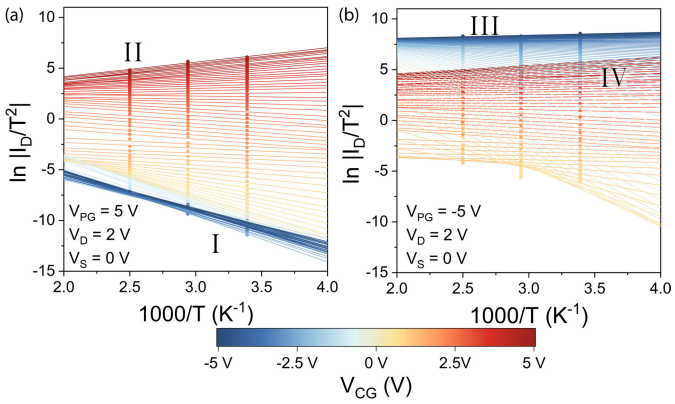

Fig. 4. Richardson plots for applying $V_D = 2$ V in the DTG configuration. (a) N-type operation ($V_{PG} = 5$ V) and (b) p-type operation ($V_{PG} = -5$ V). The roman letters indicate the corresponding regions in Fig. 3(b).

with a positive V_{DS} of 2 V, (a) and (b), as well as a negative V_{DS} of −2 V, (c) and (d), while retaining V_S at 0 V. The applied top-gate voltages are in the range between 5 V and −5 V, respectively. The left side of Fig. 3 provides the conventional I–V transfer curves for various PG voltages, whereas the right side presents the corresponding spectroscopy map, which makes estimations of voltage variations and their influence on the operability visible, considering, i.e., electronic circuits, and the distinction between occurring transport regimes easier. As mentioned before, V_{DS} bias direction is important to define the desired unipolar conduction type together with V_{PG}, so that distinct ON-state and OFF-state regions are established.

To shed light on the transport regimes, maps are recorded, highlighting the dependence of I_D on a broad range of V_{PG} and V_{CG} values for both positive and negative V_{DS} biases. The associated schematic band diagrams are located in each corner of the map, with the PG voltage applied above the drain junction and the CG voltage applied over the channel and the source junction. In this regard, the positive bias voltage situation in Fig. 3(a) and (b) exhibits this unipolar n-type behavior for a PG voltage greater than approximately 1 V. For applying negative CG voltages (upward band bending, state labeled I) in the unipolar n-type regime, an efficient blocking of both the charge carrier types is evident. Contrary to that, positive CG voltages (downward band bending, state labeled II) allow electrons to pass through the multiheterojunction, while holes are still rejected at the drain-side barrier. Furthermore, considering negative PG voltages (lower than −1 V), charge carriers interestingly flow for both the polarities of V_{PG} consequently leading to ambipolar operability. Accordingly, for a negative V_{CG}, the associated bands are shifted up (state III), allowing holes to tunnel through the barriers more efficiently into the valence band, while still blocking electron injection. For positive CG voltages (state IV), I_D rises again. The obtained ambipolar behavior has been identified as an interesting characteristic for analog circuits. This behavior is distinctly different to the behavior of dual-gated RFETs published so far [7]. We speculated that a band-to-band tunneling window opens up at the region between both the gates. Thereto, both the electrons injected at the source, as well as holes injected at the drain, can tunnel, leading to the increase in I_D. This assumption is supported by the resulting lower current compared with the occurring currents for "thinner" barriers. Further band-bending due to charge carrier accumulation, as indicated in the respective insets, and the corresponding changing energy landscape affects the resulting charge carrier transport in transient operation. This possibly leads to a displacement, i.e., reduction of barrier height as the charge carriers accumulate in the respective potential wells. Yet another possibility is the accumulation of charge carriers in the potential pits that transiently charge up these regions. Thus, the source-sided electron pit gets lifted, and the drain-sided hole pit gets lowered, leading to an overspilling of charge carriers into the buffer Si region under the Ge layer. This hypothesis is supported by the degradation of the subthreshold slope in Region IV compared with Region II. To further clarify the underlying transport properties, temperature-activated I/V characteristics were taken and evaluated in Arrhenius plots; see Fig. 4. Comparing different temperature dependencies of the current, indications for tunneling as the dominant transport contribution were found by comparing the slopes for the different voltage situations for positive bias voltage, as indicated with Roman letters in Figs. 3(b) and 4.

A similar but complementary situation for Fig. 3(a) and (b) arises with negative bias voltages applied, as presented

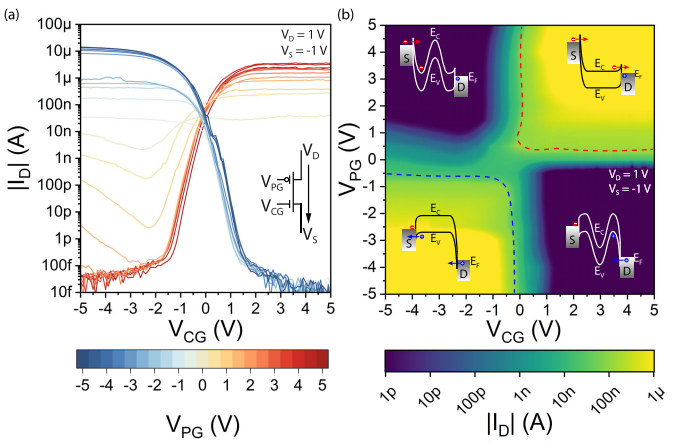

Fig. 5. PG-dependent transfer characteristic of a TTG RFET. (a) Conventional *I*–*V* characteristic and (b) corresponding color map for a symmetrically applied bias voltage V_D of 1 V and V_S of −1 V. The insets show the circuit symbol, the associated bias direction, and the related band diagrams in accordance with the applied voltages.

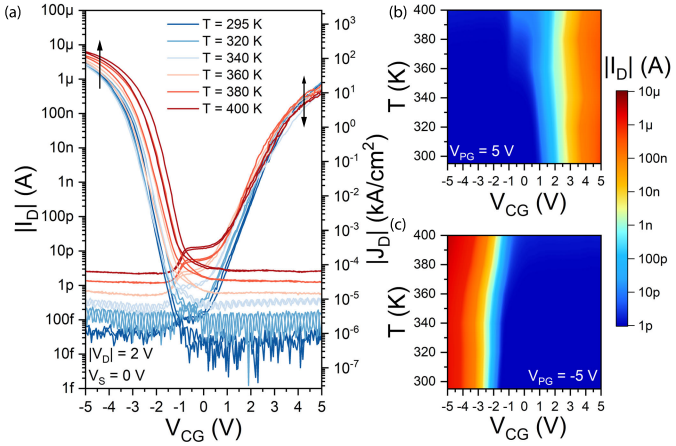

Fig. 6. Temperature-dependent transfer characteristic for a DTG RFET from RT up to 400 K. The bias is set with the drain level of 2 V for n-type operation (V_{PG} = 5 V) and −2 V for p-type operation (V_{PG} = −5 V), respectively. The temperature-dependent *I*–*V* curves for both the modes are presented in (a), whereas the temperature maps obtaining the individual modes are shown in (b) n-type and (c) p-type.

in Fig. 3(c) and (d). Accordingly, for negative PG voltages, the unipolar regime is established, while positive PG voltages lead to an ambipolar behavior, as indicated by a white dashed line and the related band diagrams. Note that the PG remains above the drain junction, so the resulting characteristic depends on the bias direction only. The differences between PG voltages of the operation regime border can be attributed to slightly different barrier heights for holes and electrons resulting from Fermi-level pinning of Al in the Si interlayer [15]. This also explains the slightly higher currents for hole-dominated charger carrier transfer. Summing up, the bias applied at the DTG configuration is decisive for the operability of the devices, which makes it necessary to not just apply the related PG voltage but also the correct bias direction when unipolar configuration is necessary. Nevertheless, this further degree of freedom by operating the DTG configuration in either the unipolar or ambipolar mode can also be interpreted as an additional lever to adapt functionality of the same device, ultimately enabling an additional mode for enhanced reconfigurable circuit design.

Similar to the DTG gating investigation, Fig. 5(a) provides the conventional *I*–*V* curves of the symmetrically (i.e., $V_D = -V_S$) and positively biased TTG structure ($V_{DS} = 2$ V), with the top-gate voltages varied between 5 V and −5 V, respectively. Fig. 5(b) presents the corresponding bias color map, where the occurring ON-state and OFF-state regions can be assessed. In addition, band diagrams of the related voltage-dependent band bending situation are inserted, in each corner of the four quadrants of the color map, indicating the assumed dominant charge carrier transport. At positive PG and CG voltages, both the PG-related barriers and the CG-related channel potential are lowered, consequently allowing electrons to tunnel through the barriers more efficiently and pass the channel, while, at the same time, holes are rejected, resulting in an n-type-dominated current across the heterostructure. Changing the CG voltage to negative values, i.e., lifting the CG-related channel band, ends in blocking the electrons and thus reaching the OFF-state region of the n-type dominated regime. A similar but complementary situation is obtained for negative PG voltages and for holes instead of electrons while maintaining the equal bias condition, finally resulting in four different gating areas. As can be seen, the borders of these four distinct regions, so the ON-state/OFF-state region and n-/p-type region, are very aligned to 0 V for each individual top-gate. Moreover, contrary to the DTG, there is no bias-dependent ambipolarity. In this respect, the applied symmetric bias voltages reduce measurement-induced source- and drain-induced level shifts and help assess better the inherent degree of I/V-symmetry in the devices, although potentials may be applied differently in a circuit.

Temperature-dependent investigations of the DTG configuration, as given in Fig. 6, reveal a stable unipolar operability up to 400 K for both the operation modes with respect to the correctly applied bias direction, i.e., $V_D = 2$ V, $V_S = 0$ V for n-type $V_D = -2$ V, and $V_S = 0$ V for p-type operation. As evident in Fig. 6(a), for p-type operation, both the ON-state currents increase with temperature, and the threshold voltages are reduced as expected by the strong bandgap narrowing dependence with temperature exhibited by Ge [16]. However, in the n-type regime, the ON-state varies slightly with a trend toward decreasing currents. The OFF-state current increases for both the operation types, which is in agreement with the dominant thermionic-emission (TE)-based current [16], [17]. Interestingly, the temperature-dependent investigations of the p-type mode do not show such a plateau in its transfer characteristic even up to 400 K. The captured temperature-dependent transfer characteristics can be plotted into a colored 2-D map, Fig. 6(b) for n-type and Fig. 6(c) for p-type operation, to identify regions of stable operation from RT up to 400 K. The n-type operation reveals a very stable ON-state and OFF-state region, with the mentioned plateau at elevated temperatures, while the p-type operation exhibits a slight shift of the ON-state region to lower CG voltages at increased temperatures.

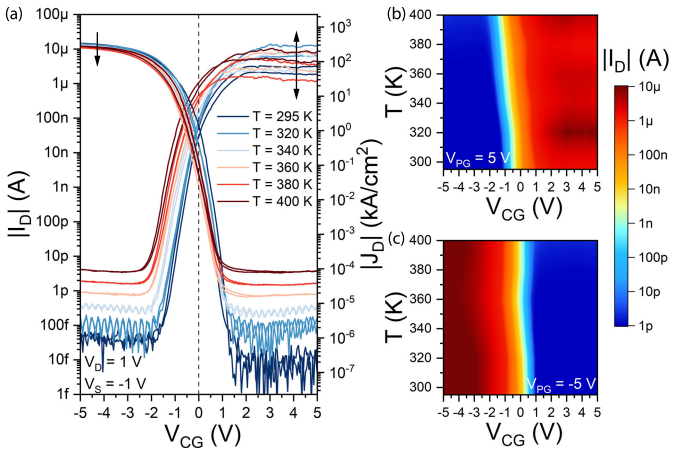

Fig. 7. Temperature-dependent transfer characteristic for a TTG RFET from RT up to 400 K. The bias is applied symmetrically with V_D of 1 V and V_S of −1 V for both n-type (V_{PG} = 5 V) and p-type operation (V_{PG} = −5 V), respectively. The temperature-dependent *I*–*V* curves for both the modes are presented in (a), whereas the temperature maps obtaining the individual modes are shown in (b) n-type and (c) p-type.

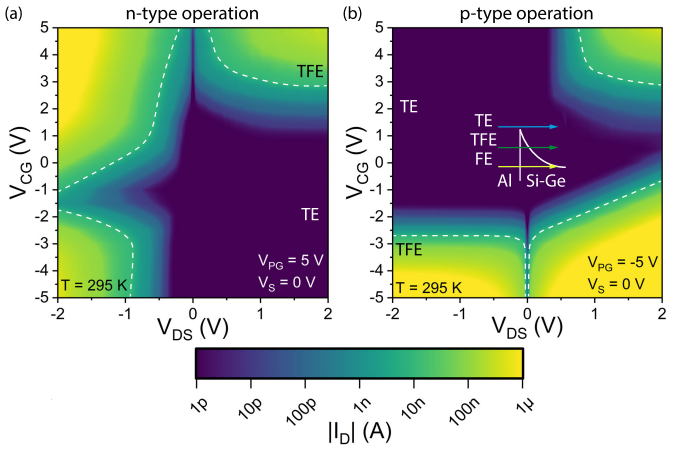

Fig. 8. Output characteristics of DTG RFET presenting (a) n-type operation and (b) p-type operation at a constant polarity-gate voltage of either 5 or −5 V, respectively. The source voltage level V_S is set to 0 V, while V_D is swept respectively. The ON-state regions, as well as the TE and the TFE, are indicated with dashed lines.

The temperature-dependent transfer characteristics of the TTG configuration are presented in Fig. 7. The bias is applied symmetrically, so that V_D is 1 V and V_S is −1 V, while the temperature is increased from RT up to 400 K. Contrary to the DTG, the mode is only set with the PG voltage, either 5 V for n-type or −5 V for p-type operation, while keeping the equal positive bias voltage applied. The CG is swept from the ON-state to the OFF-state and reversed for each operation type, allowing the estimate of the hysteresis also in dependency on the temperature. As evident, the unipolar behavior is present even up to 400 K, with an increased OFF-state current and a slightly decreasing p-type ON-state current. This indicates that at elevated temperatures, the influence of charge carrier scattering is becoming the main contributor to the resistance, which is the signature of a transparent (quasi-ohmic) contact [8], [13], [16]. However, the ON-state of the n-type mode is widened for higher temperatures with two explicit outliers at 320 K and 380 K. The general trend of the n-type ON-state current is toward increased currents at elevated temperatures. Moreover, regarding the temperature-dependent variation in the ON-state current of each mode, it appears that the TE contribution is higher for n-type than for p-type operation, considering different temperature dependencies [16], [17], resulting in a wider ON-state current range, which can also be attributed to slightly unequal barriers for electrons and holes [15]. Nevertheless, there are stable operation regions, as visible in Fig. 7(b) (n-mode) and (c) (p-mode), up to 400 K, with a remarkable symmetric behavior regarding V_{CG} = 0 V. In general, comparing the ON-states of the various modes of different architectures, it is evident that only the p-type of the TTG configuration can be tuned to reach a transparent contact, as identified according to the decreasing ON-state currents over temperature. On one side, this can be attributed to the fixed tunneling barrier levels via the PG, contrary to the DTG, on the other side, also to the generally higher barriers for electrons due to slight differences in Fermi-level pinning [15]. Finally, as the bias is decisive for proper operation, especially for DTG, the bias-dependent gating capabilities of the configurations are investigated. With respect to that, the output characteristics for various CG voltages between 5 and −5 V for both the operation modes are captured and presented as colored output maps.

In Fig. 8, the output spectroscopy of the related DTG arrangement is presented for n-type Fig. (a) and p-type Fig. (b) operations, where the mode is set with a PG voltage of 5 V or −5 V, respectively. The bias voltage is applied via V_D, swept from 2 V to −2 V, while keeping V_S to 0 V. In addition, the conventional I/V representation of the output characteristic for the DTG arrangement is presented in the Supporting Information; see Fig. S1. As evident for n-type operation, a positive bias results in unipolar behavior, whereas a negative bias leads to an ambipolar behavior. Moreover, considering bias symmetry, which means equal ON-state (and OFF-state) regions for bias voltages of equal values but different signs, the DTG structure does not fulfill this property. Ideally, the output characteristic exhibits an ON-state quadrant region that is as square as possible and mirrored with respect to the V_{DS}-zero axis. In addition, temperature-dependent investigations of the output characteristics reveal that the OFF-state region is dominated by TE caused current, while the major part of the ON-state current is attributed to tunneling, as indicated in the maps. The determination bases on different temperature dependencies of field-emission (FE) and TE [16], [17]. However, it should be noted that it is difficult to fully distinguish between the individual occurring transport mechanisms, and therefore, it is assumed to be a mixture with a dominant contribution of the identified emission [18].

Similar to DTG structure investigations, Fig. 9 shows the output bias spectroscopy of the related TTG arrangement, but with a symmetrically applied bias ($V_D = -V_S$). The mode is set with a PG voltage of 5 V for n-type and −5 V for p-type operation. Moreover, the conventional I/V representation of the output characteristic for the TTG structure is presented in the Supporting Information; see Fig. S2. For this configuration, a unipolar behavior is evident independently of

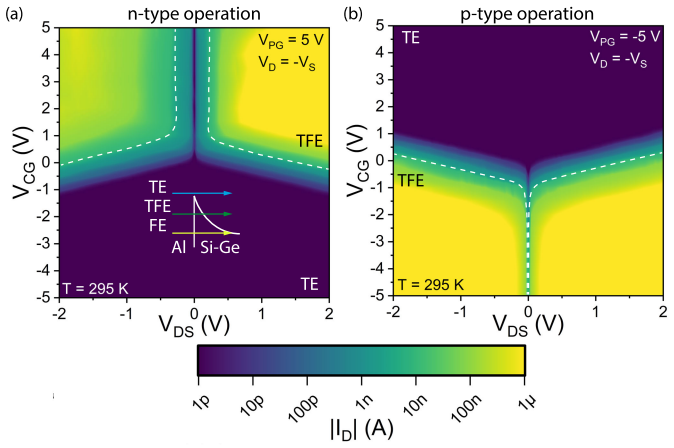

Fig. 9. Output characteristics of TTG RFET presenting (a) n-type operation and (b) p-type operation at a constant polarity-gate voltage of either 5 or −5 V, respectively. The bias voltage is applied symmetrically, with $V_D = -V_S$. The ON-state regions, as well as the TE and the TFE, are indicated with dashed lines.

the bias applied. Furthermore, in contrast to the DTG device, the bias symmetry with respect to the bias direction is given. In addition, the general shape of the ON-state operation region is broader and more square-shaped compared to DTG devices. The overall symmetry can be attributed to the architectural design, which exhibits a geometrical symmetry with respect to the top-gates contrary to the DTG structure. This attribute provides advantages regarding circuit design, especially in adaptive applications, due to the ability to alter the bias direction without losing functionality, enabling a further degree of freedom. Moreover, the dominant transport mechanisms, determined by temperature-dependent investigations of the output characteristics, are indicated in the maps, where TE is dominant in the OFF-state region, while tunneling is the dominant mechanism in the ON-state.

V. Conclusion

In conclusion, we have investigated the influence of charge carrier injection and modulation by electrostatic gating considering different gate configurations. The DTG architecture, with its bias-dependent polarity, in addition to the unipolar n- and p-type operation, offers access to the ambipolar operation mode, which is especially interesting for analog signal modulation applications. The TTG arrangement provides higher ON-state currents and, consequently, an enhanced ON-state-to-OFF-state ratio. Furthermore, due to its geometrical symmetry, the TTG architecture offers bias-independent operability and centered ON-state to OFF-state symmetry, enabling a further degree of freedom for the design of reconfigurable circuits.

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References

[1] W. M. Weber, A. Heinzig, J. Trommer, D. Martin, M. Grube, and T. Mikolajick, "Reconfigurable nanowire electronics—A review," *Solid-State Electron.*, vol. 102, pp. 12–24, Dec. 2014.

[2] K. Jabeur, I. O'Connor, and S. Le Beux, "Ambipolar independent double gate FET (Am-IDGFET) for the design of compact logic structures," *IEEE Trans. Nanotechnol.*, vol. 13, no. 6, pp. 1063–1073, Nov. 2014.

[3] F. Xi et al., "Artificial synapses based on ferroelectric Schottky barrier field-effect transistors for neuromorphic applications," *ACS Appl. Mater. Interfaces*, vol. 13, no. 27, pp. 32005–32012, Jul. 2021.

[4] P. Wu, D. Reis, X. S. Hu, and J. Appenzeller, "Two-dimensional transistors with reconfigurable polarities for secure circuits," *Nature Electron.*, vol. 4, no. 1, pp. 45–53, Dec. 2020.

[5] M. De Marchi et al., "Polarity control in double-gate, gate-all-around vertically stacked silicon nanowire FETs," in *IEDM Tech. Dig.*, Dec. 2012, pp. 8.4.1–8.4.4.

[6] L. Wind et al., "Reconfigurable Si field-effect transistors with symmetric on-states enabling adaptive complementary and combinational logic," *IEEE Trans. Electron Devices*, vol. 71, no. 2, pp. 1302–1307, Feb. 2024.

[7] J. Trommer et al., "Enabling energy efficiency and polarity control in germanium nanowire transistors by individually gated nanojunctions," *ACS Nano*, vol. 11, no. 2, pp. 1704–1711, Feb. 2017.

[8] A. Fuchsberger et al., "A run-time reconfigurable Ge field-effect transistor with symmetric on-states," *IEEE J. Electron Devices Soc.*, vol. 12, pp. 83–87, 2024.

[9] R. Böckle et al., "A top-down platform enabling Ge based reconfigurable transistors," *Adv. Mater. Technol.*, vol. 7, no. 1, Jan. 2022, Art. no. 2100647.

[10] J. Aberl, M. Brehm, T. Fromherz, J. Schuster, J. Frigerio, and P. Rauter, "SiGe quantum well infrared photodetectors on strained-silicon-on-insulator," *Opt. Exp.*, vol. 27, no. 22, p. 32009, 2019.

[11] M. Brehm et al., "Key role of the wetting layer in revealing the hidden path of Ge/Si(001) Stranski–Krastanow growth onset," *Phys. Rev. B, Condens. Matter*, vol. 80, no. 20, Nov. 2009, Art. no. 205321.

[12] A. Fuchsberger et al., "A reconfigurable Ge transistor functionally diversified by negative differential resistance," *IEEE J. Electron Devices Soc.*, vol. 12, pp. 541–547, 2024.

[13] L. Wind et al., "Composition dependent electrical transport in $Si_{1-x}Ge_x$ nanosheets with monolithic single-elementary Al contacts," *Small*, vol. 18, no. 44, Nov. 2022, Art. no. 2204178.

[14] B. Sun et al., "On the operation modes of dual-gate reconfigurable nanowire transistors," *IEEE Trans. Electron Devices*, vol. 68, no. 7, pp. 3684–3689, Jul. 2021.

[15] T. Nishimura, K. Kita, and A. Toriumi, "Evidence for strong Fermi-level pinning due to metal-induced gap states at metal/germanium interface," *Appl. Phys. Lett.*, vol. 91, no. 12, Sep. 2007, Art. no. 123123.

[16] A. Fuchsberger et al., "Reconfigurable field-effect transistor technology via heterogeneous integration of SiGe with crystalline Al contacts," *Adv. Electron. Mater.*, vol. 9, no. 6, Apr. 2023, Art. no. 2201259.

[17] S. J. Park et al., "Channel length-dependent operation of ambipolar Schottky-barrier transistors on a single Si nanowire," *ACS Appl. Mater. Interfaces*, vol. 12, no. 39, pp. 43927–43932, Sep. 2020.

[18] M. Schwarz et al., "The Schottky barrier transistor in emerging electronic devices," *Nanotechnology*, vol. 34, no. 35, Aug. 2023, Art. no. 352002.