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A Schottky barrier field-effect transistor platform with variable Ge content on SOI☆

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ABSTRACT

Advancing SOI-based transistors with Ge-rich layers aims to increase device performance in terms of on-state operation and switching speed. Here, we investigate multi-heterojunction SiGe-based Schottky barrier FETs with Ge concentrations up to 75% by means of temperature- dependent electrical characterizations to identify the transport regimes and the effective barrier heights with a thermionic-emission-based model. Importantly, incorporating 33% Ge gives the best compromise for n- and p-type on-state symmetry. As the Ge concentration increases, the p-type on-state current becomes dominant, which is interesting for low-power p-type transistors.

1. Introduction

Schottky barrier field-effect transistors (SBFETs) are promising candidates for emerging devices such as cryo-CMOS qubit readout circuits, Josephson FETs for quantum computation, [1,2] and run-time adaptive reconfigurable transistors (RFETs) used for analog [3,4] and digital circuits [5–7]. Importantly, Ge and SiGe are predicted to enhance the on-state behavior compared to pure Si, due to their lower effective masses and consequently higher tunneling probabilities, resulting in faster switching speeds and enhanced transistor performance [8,9]. Nonetheless, considering Schottky contact formation as well as the oxide formation due to the presence of Ge, the integration of SiGe is still challenging, and hence limiting the application of actual SiGe devices. In this work, we propose SiGe SBFET platforms with variable Ge-content based on conventional Si on insulator (SOI), which allows abrupt and oxide-free contacts by the formation of an Al-Si-SiGe multi-heterojunction [10]. Therefore, ultra-thin $Si_{67}Ge_{33}$, $Si_{50}Ge_{50}$ and $Si_{25}Ge_{75}$ layers on SOI were taken into account. To further investigate the platforms' reproducibility and electrical stability, temperature-dependent transport investigations and consequently the determination of the related activation energy and flat-band voltage in dependence on the Ge-content were performed. Especially, to underline the on-state enhancement, a comparison to a reference SOI sample is provided, emphasizing the potential of the SiGe platforms towards their applicability in a large field of emerging devices.

2. Results and discussion

For the investigation of variable Ge content within the proposed SBFET platform, a conventional SOI is extended by SiGe layers with different Ge content via ultra-low temperature molecular beam epitaxy (ULT-MBE) [11]. The device integration, starting from the SiGe on SOI (SGOI) samples as depicted in Fig. 1b, undergoes various fabrication steps. Similar for all individual samples, the mesa structure is defined via laser lithography and SF_6-O_2 reactive ion etching, resulting in nanosheets with approx. 500 nm width. To provide a gate interface with high structural and electrical quality, the SiGe layer is capped with an additional ULT-MBE-grown Si layer. This protection layer is then dry oxidized, resulting in an oxide thickness of approx. 5 nm. A very critical aspect of SBFETs is the contact properties. The proposed SBFETs are

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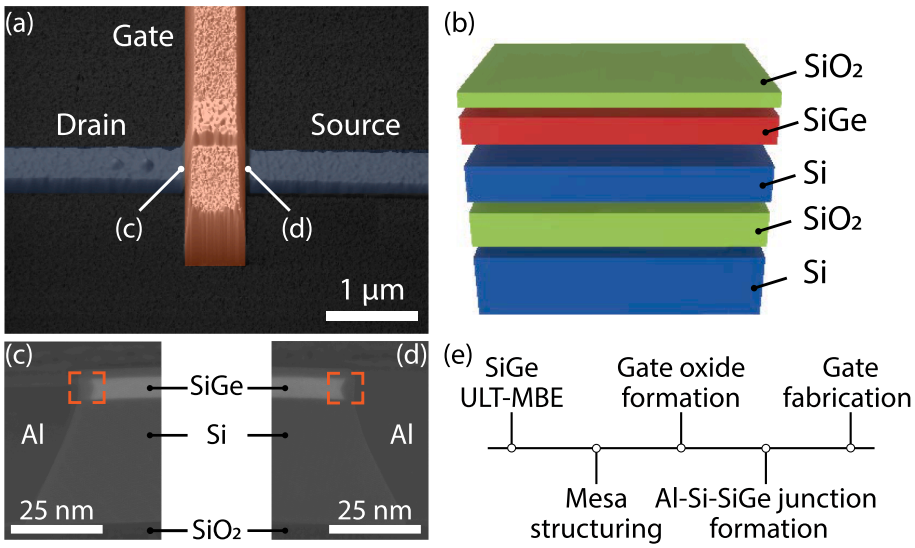

Fig. 1. (a) Colored AFM-image of a SBFET device. (b) Channel stack with the SiGe layers atop a conventional SOI. (c) and (d) show TEM images of the source/drain contacts of the SBFET with highlighted Al-Si-SiGe multiheterojunction (orange squares). (e) Generalized fabrication process. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

Table 1
Dimensions in terms of channel length (L), width (W) and device layer (DL) thickness of the used devices for each SiGe platform.

Platform	L (µm)	W (nm)	DL (nm)
$Si_{67}Ge_{33}$	1.44	400	8
$Si_{50}Ge_{50}$	1.46	840	8
$Si_{75}Ge_{33}$	1.82	356	5

contacted with Al as metal, as it provides a Fermi-level pinning in the middle of the Si band-gap [12], which enables equal barriers for holes and electrons and consequently symmetric on-state operation for n- and p-type operation. Further, the nanoscale crystalline Al contacts establish structurally high-quality junctions, allowing stable and reproducible electrical characteristics [10]. Ge, however, causes a Fermi-pinning close to the valence band [12] and consequently a p-type preferred characteristic. Importantly, with the proposed thermally-induced solid-state exchange reaction of Al and Si/SiGe and the asymmetry in the diffusion coefficients, a Si interlayer between the Al and the related SiGe is formed, which can be seen in the TEM scan in Fig. 1c and Fig. 1d. This Si interlayer causes a re-pinning of the Al and therefore symmetric n- and p-type operation as well as the encapsulation and thus protection of the Ge-rich layers [10,13]. Finally, a gate consisting of 10 nm Ti, responsible for the gate pinning, and 100 nm Au, as bonding metal, is fabricated. The fabricated structure is presented as AFM scan in Fig. 1a.

The dimensions of the used devices for each SiGe platform are summarized in Table 1. Note, that the maximum reachable thickness of the device layer (DL) strongly depends on the introduced strain of the different Ge concentration considering defect-free and flat MBE-layers. Obviously, the higher the Ge content of the SiGe, the thinner layers are obtained under equal growing conditions [14].

With a gate atop both metal–semiconductor junctions and the

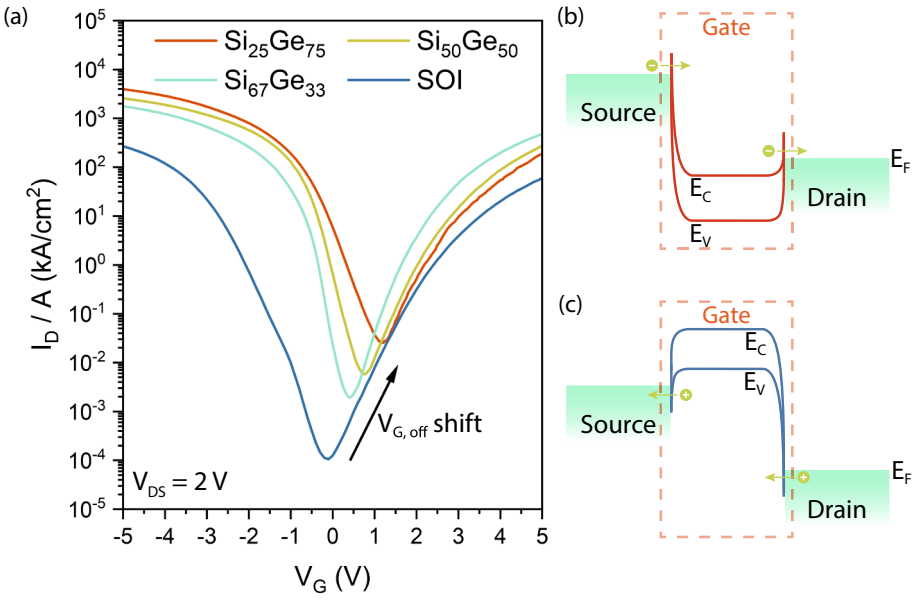

Fig. 2. (a) Transfer characteristic normalized over the cross-section for each SiGe-configuration with the respective off-state shift indicated. On-state band diagram of the SBFETs for n-type (b) and p-type (c) operation.

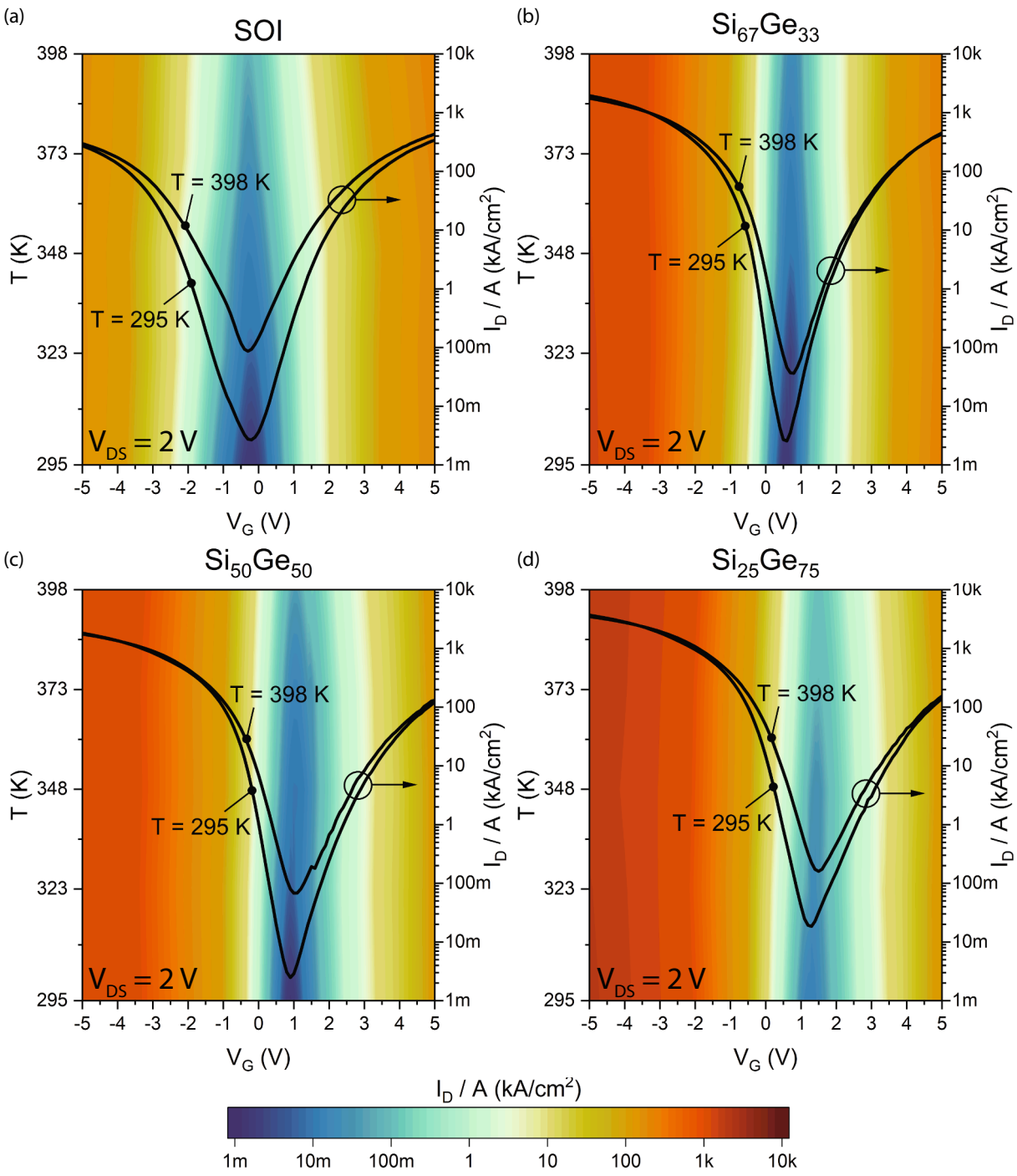

Fig. 3. Temperature-dependent investigations of the transfer characteristics from RT up to 398 K for each SiGe-configuration, starting from the reference SOI sample (a), $Si_{67}Ge_{33}$ (b), $Si_{50}Ge_{50}$ (c) to $Si_{25}Ge_{75}$ (d).

semiconductor channel, the related band diagrams of the proposed SBFET can be lifted by applying a negative voltage or lowered by applying a negative voltage, as depicted in Fig. 2. Respectively, the decreased bands (Fig. 2b) allow electrons passing the metal–semiconductor barrier as well as the channel, so the complete source-drain-path, while holes remain rejected.

Similarly, the lifted bands (Fig. 2c) provide hole transfer and electron rejection, resulting in an ambipolar transfer characteristic, with two on-states (n- and p-type) and one distinct off-state (intrinsic) gate voltage point. Considering the presented transfer characteristic for various SiGe-configurations in Fig. 2a, the reference SOI structure exhibits a $V_{TG} = 0$ V- and n- and p-type symmetric on-states with the proposed operation regime of V_{DS} of 2 V and the gate voltage V_G between −5 V and 5 V. Increasing the Ge content to 33 %, as evident, the on-states normalized over the respective cross-section area are enhanced, while retaining the on-state symmetry. The off-state point ($V_{G,\,off}$) is slightly increased and shifted to positive voltages. This can be attributed to the introduced band-offset within the Al-Si-SiGe multi-heterojunction, contrary to the Al-Si junction of the reference sample. Following this trend, with higher Ge-concentrations, the off-state increases and is shifted to positive gate voltages, causing an enhanced p-type and reduced n-type on-state within the proposed operation regime.

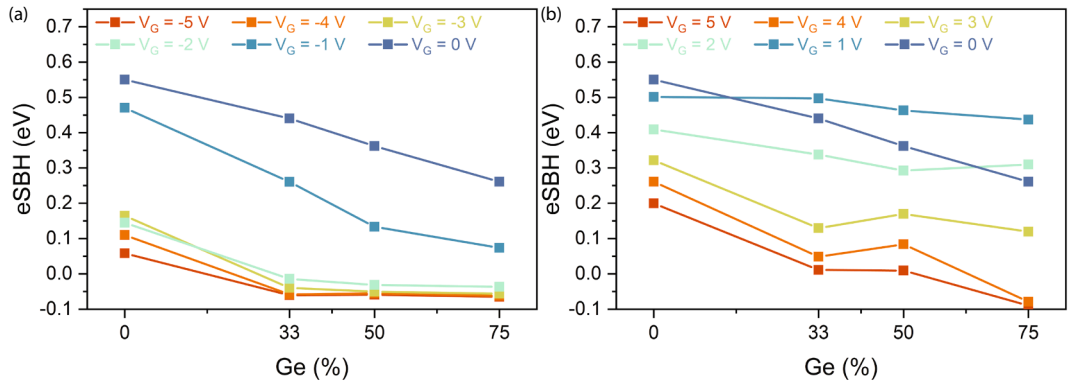

Fig. 4. Activation energy, extracted based on the thermionic-emission theory, in dependency of the applied gate voltage over the Ge-content.

As stated above, the protection of the SiGe layers by Si and at the multi-heterojunction as well as SiO_2 atop the channel, provides reproducible and stable electrical operation, allowing for temperature-dependent investigations. Fig. 3 depicts the temperature-related transfer characteristics for all SiGe-configurations including the reference SOI sample for a bias voltage V_{DS} of 2 V and a gate voltage V_G between −5 V and 5 V from room temperature (RT) up to 398 K in 25 K-steps. Comparing the individual investigations, the off-state is increasing with elevated temperatures, which is an indication of a thermionic-emission (TE) dominated transport, typically for the off-state of an SBFET [9,15]. Moreover, the on-states, especially for the SiGe-configurations, remain almost unaffected or even decrease with higher temperatures, which indicates a quasi-ohmic, transparent contact and a tunnelling-dominated charge carrier transport [9,16]. Nonetheless, for all investigated SBFET platforms, it is evident that the on-state as well as the off-state regions are very confined over temperature within similar operation areas. This is especially important regarding device applications within circuits and larger systems, as temperature variations can cause undesired characteristics. Further, this electrical stability and reproducibility allows investigations to be conducted, such as the determination of the activation energy based on the TE theory [17] as an abstraction of the metal-semiconductor-metal heterojunc- tion system, which can be interpreted as an effective barrier height for charge carriers. Linearizing the equation $J_{TE}(T) = A^*T^2 \exp(-eSBH/k_BT)$, which sets the captured current flow in dependency of the temperature in relation to the activationenergy (eSBH), by constructing the Arrhenius

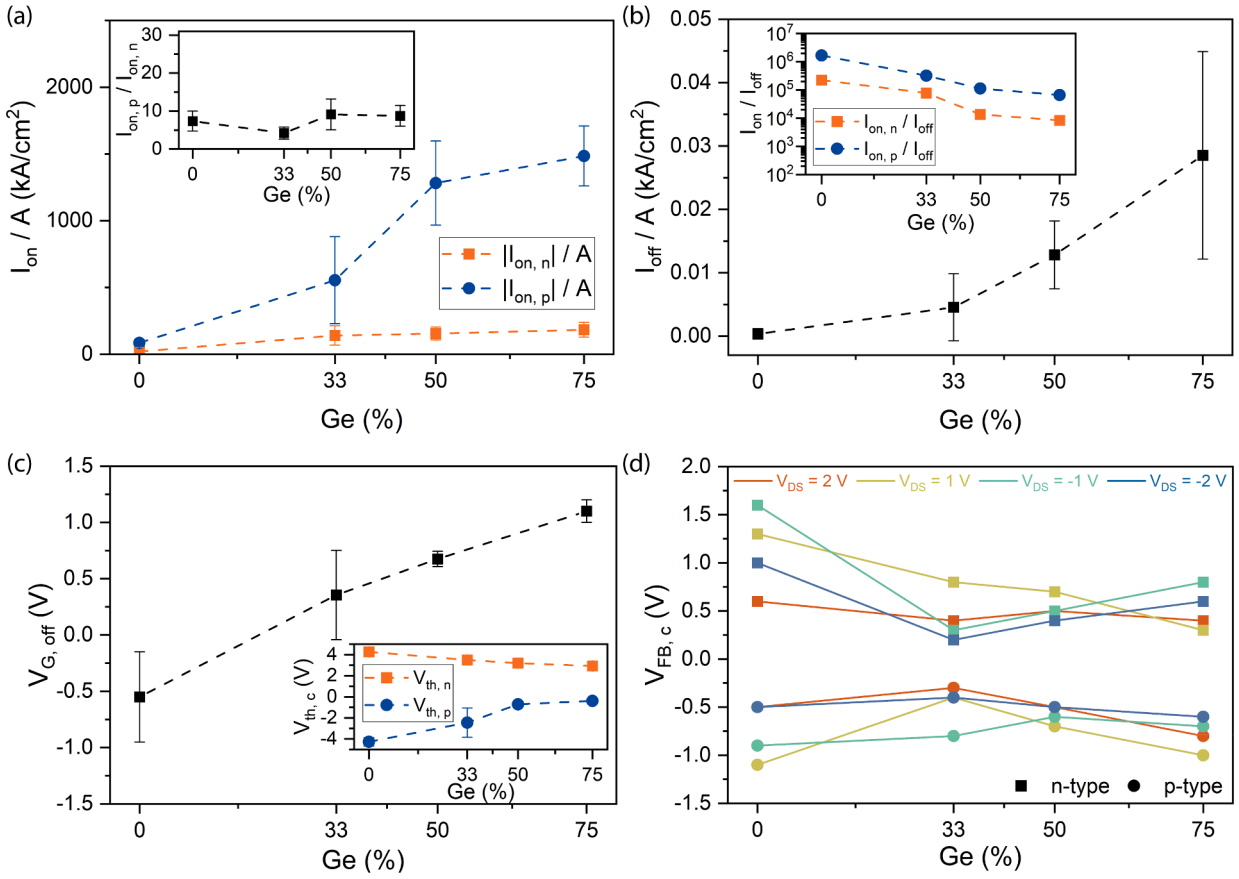

Fig. 5. Statistics based on 10 devices for each SiGe-composition. (a) On-state current over Ge-content, with the respective on-state symmetry in the in-set. (b) Off-state current over Ge-content, with the respective on-state to off-state ratio in the inset. (c) Off-state point shift over Ge-content, with the determined threshold voltage values corrected with that off-state shift in the inset. (d) Flat-band voltages over Ge-content corrected by the off-state voltage point for various bias voltages.

plots according to $\ln|J_{TE}/T^2| = \ln|A^*| - eSBH/k_BT$, with a constant effective Richardson constant A^*, the determined slope k of this $1/T$-plot gives the related eSBH value: $eSBH = -k \cdot k_B$ [13,17].

Taking now gate-dependent I/V characteristics over temper-ature into consideration and applying the presented formalism gives the possibility to extract the gate-dependent activation energy for all different Ge concentrations, as presented in Fig. 4. As evident, for gate voltages from 0 V to −5 V (Fig. 4a), towards p-type operation, the effective barrier height decreases, independent of the Ge content, the more negative the gate voltage gets reaching consequently even negative values, which is an indication of the already mentioned transparent contact and the tunneling dominated transport. Comparing the individual concentrations, the higher the Ge-content, the less voltage has to be applied to the gate to achieve this state. This is also in line with the determined off-state shift, see Fig. 2. For gate voltages from 0 V to 5 V (Fig. 4b), so towards n-type operation, it is also evident, that the Ge-containing samples reach this state of low to negative activation energy values within the chosen operation window. Interestingly, also the off-state shift can be extracted as the *eSBH*-value increases for a gate voltage of 1 V compared to the reference SOI sample. The presented formalism, however, considers a general 3-D TE-dominated charge carrier transport, taking the 2-D nature of the channels into account, which allows for further parameters such as the flatband voltage V_{FB}. The proposed TE-based equation alters to the following [18–20]:

$$I_D = AA^*_{2D}T^{2/3}\exp[-eSBH/k_BT + \gamma(V_{GS} - V_{FB})/k_BT] \quad (1)$$

where A is the cross-section, A^*_{2D} the 2-D Richardson constant, $\gamma = (1 + C_{it}/C_{ox})^{-1}$, with the interface capacitance C_{it} and the oxide capacitance C_{ox}, V_{GS}, the related gate-source voltage and V_{FB}, the flat-band voltage. Following the similar linearization method by setting up Arrhenius plots and extracting the linearized slope $k = -eSBH/k_B + \gamma(V_{GS} - V_{FB})/k_B$, additionally, the flat-band voltage V_{FB} can be determined for a specific bias voltage [18], as it will be discussed in Fig. 5.

Setting typical transistor parameters into perspective, the mean value of 10 representative devices of each SBFET platform is presented in Fig. 5. However, due to the occurring off-state point shift, the on-state currents for various Ge-concentrations normalized over the cross-section area (Fig. 5a) considers the current value shifted by ± 3.75 V from the intrinsic point. The delta voltage window from the intrinsic point was chosen to remain within the selected operation window of ± 5 V of gate voltage for all samples. This enables, to some extent, a direct comparison of the on-state as the complete device characteristic can be shifted, for instance, by using the back gate, so correcting the inherent influence of the material-related shift. As evident, the p-type on-state (blue) as well as the n-type on-state (orange) increase with higher Ge-content, whereas the n- and p-type on-state symmetry remains very comparable, as visible in the inset, with $Si_{67}Ge_{33}$ providing the best n- and p- current on-current symmetry. This increase can be attributed to the higher Ge-content within the multi-heterojunction and consequently the changed band-offset due to the altered band-configuration. Comparing the off-state current normalized over the cross-section (Fig. 5b), with higher Ge-concentrations the off-state increases, resulting in a worse on-state-to-off-state ratio, as depicted in the inset for both operation types. Fig. 5c gives the mean value of the off-state point-shift, which tends towards more positive gate voltages. The inset of Fig. 5c shows the related threshold-voltage values corrected by the inherent off-state point shift. The corrected threshold voltages $V_{th,\,c}$ get smaller with increased Ge-content, as it is also forecasted for Ge-rich SBFETs [8,21]. Coming back to the extracted bias voltage-dependent flat-band voltages for various Ge-concentrations again corrected by off-state point shift, as presented in Fig. 5d, it is evident, that especially for the 2 V and −2 V bias situation the corrected $V_{FB,\,c}$ is in the range of 0.5 V for n-type and −0.5 V for p-type operation. In general, considering the evaluated statistic of the different transistor platforms, depending on the specific application, the $Si_{67}Ge_{33}$ sample provides a compromise between enhanced on-state and competitive low off-state currents compared to pure Si-based SBFETs, while keeping the on-state symmetry, which is desirable, i.e., for reconfigurable transistors and circuits [13].

3. Conclusion

In conclusion, we have experimentally investigated SBFET platforms with SiGe layers of variable Ge content towards their temperature-dependent electrical characteristics. Evaluating ten representative devices of each SiGe composition and setting the integrated SiGe-samples into perspective, the revealed on-state enhancement as well as the transparent, quasi-ohmic con-tact properties make those devices an interesting candidate for beyond-CMOS applications. Identifying the n- and p-type on-state symmetry as a crucial parameter for adaptive electronics, the $Si_{67}Ge_{33}$ sample gives higher on-state currents with similar n- and p-type on-state symmetry compared to the reference SOI sample. In contrast, the Ge-rich SiGe layers might be promising for enhanced PMOS devices with high on-currents and low threshold voltages, which are especially interesting for cryoCMOS devices and quantum computation.

CRediT authorship contribution statement

Andreas Fuchsberger: Writing – original draft, Visualization, Methodology, Investigation, Formal analysis. **Lukas Wind:** Methodology, Investigation. **Aníbal Pacheco-Sanchez:** Methodology, Investigation, Funding acquisition. **Johannes Aberl:** Investigation. **Moritz Brehm:** Investigation, Funding acquisition. **Lilian Vogl:** Investigation. **Peter Schweizer:** Investigation. **Masiar Sistani:** Writing – review & editing, Validation, Supervision, Project administration, Investigation, Funding acquisition, Formal analysis, Conceptualization. **Walter M. Weber:** Writing – review & editing, Validation, Supervision, Project administration, Funding acquisition, Conceptualization.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Data availability

Data will be made available on request.

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