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ABSTRACT

Germanium (Ge) is recognized as a highly promising substrate for a broad spectrum of electronic, optical, and quantum applications, owing to its exceptional properties, including high charge carrier mobility, strong spin-orbit coupling, and its behavior as a quasi-direct semiconductor. However, the electron transfer effect in Ge, similar to the Gunn effect in GaAs, which induces negative differential resistance, has received relatively little attention thus far. This is likely due to the requirement for a well-defined material system and device architecture for its realization and usually at low temperatures.

This study presents a wafer-scale fabrication approach and characterization of monolithic Al–Ge–Al heterostructures integrated into Schottky barrier field-effect transistor (SBFET) architectures, demonstrating negative differential resistance (NDR) even at room temperature. Utilizing Ge nanosheets, NDR is achieved through electron transfer from L- to lower mobility Δ-valleys under high electric fields with pronounced peak-to-valley ratio (PVR). First-principles and Boltzmann transport simulations confirm these findings. The PVR was found to be highly sensitive to the gate voltage and channel thickness, but largely unaffected by the length and width of the SBFET channel, highlighting its scalability and reproducibility across different device geometries. These findings position Ge-based NDR devices as a CMOS-compatible platform for multi-valued logic, reconfigurable electronics, static memory cells, and high-frequency oscillators, promising substantial advancements in speed, power efficiency, and scalability of integration.

The continuous advancement in nanofabrication as well as electronic device architectures and design enabled emerging distributed computing paradigms indispensable in the information and communication technology of everyday life. Although conventional silicon metal-oxide-semiconductor FETs (MOSFETs) are still the primary choice of nanoelectronics, the search for novel electronic devices with an alternative conduction mechanism and superior performance is continuously ongoing. Consequently, a shift of research efforts toward the integration of new materials and the exploration of tailored device and circuit architectures beyond the capabilities of conventional MOSFETs with over barrier conduction mechanism is obligatory.[1–3] In this respect, an interesting transport mechanism observed in certain materials with specific conduction band requirements is the transferred electron effect. Based on the Ridley–Watkins–Hilsum theory,[4,5] this transport mechanism is triggered by the application of high electric fields forcing a scattering of electrons from an energetically favorable conduction band valley, characterized by a low effective mass, to a heavy mass valley nearby. Such electron transfer, in GaAs better known as the Gunn effect, ultimately results in NDR with potential applications such as fast-switching multi-valued logic devices, static memory cells, or high-frequency oscillators.[6] Paving the way for practical applications of NDR beyond expensive and rather large-scale GaAs[5] and GaN[7] based devices, we have recently exploited NDR in bottom-up grown Ge nanowire devices.[8] However, for practical

applications, an approach based on CMOS-compatible, wafer-scale substrates is highly desirable. Ge-on-Si heteroepitaxy,[9] in particular, offers a more cost-effective integration solution compared to III-V-on-Si. Ge-based NDR devices offer further the advantage of higher carrier mobility compared to GaAs or GaN, enabling faster switching speeds and improved performance in high-speed and low-power applications. However, a significant drawback is the presence of surface and interface traps at the Ge/dielectric interface. These traps can lead to increased leakage currents, hysteresis effects, and degraded threshold voltage stability, ultimately reducing the overall reliability and performance of the devices. Accessible at room temperature,[8,10] the unique NDR characteristic bears enormous potential for the design of Ge-based multi-valued logic,[11,12] reconfigurable logic gates,[13] and static memory cells[6] with significantly improved performance metrics, but effective passivation and interface engineering are crucial to fully leverage its benefits.

As previously noted, field-induced electron transfer leading to NDR requires in general materials with a particular, i.e., multi-valley, energetic landscape with different effective masses that are not too far apart in terms of energy. However, this also opens up the possibility of influencing the electron transfer effect by modifying the band structure somewhat through, e.g., alloying or nanostructuring.

In this Letter, we investigate electrical transport in monolithic Al–Ge–Al heterostructures with abrupt interfaces fabricated via a thermally induced Al–Ge exchange reaction.[14] As the starting substrate, we used a germanium on insulator (GeOI) wafer, fabricated via Smart Cut™ technology, featuring a 58 nm oxide capping layer, a 76 nm undoped (100)-oriented Ge device layer with 0.2% in-plane tensile strain, a 147 nm buried oxide layer, and a Si handle wafer. Figure 1(a) schematically shows a fully featured Al–Ge–Al heterostructure device with the Ge sheet integrated in a back-gated SBFET device architecture. Therefore, using electron beam lithography and reactive ion etching, the 85 nm thick device layer of a ⟨100⟩ oriented GeOI wafer was patterned to nanosheets with structural widths between W = 100 nm and 3 μm. Next, Al contact pads were fabricated by optical lithography, native oxide removal, sputter deposition of an about 125 nm thick Al layer, and liftoff techniques (see the supplementary material). Finally, a well-controlled rapid thermal annealing at T = 624 K in a forming gas atmosphere induces the actual heterostructure formation.[14,15] In order to reduce the thickness of the Ge layer and thus ultimately the channel thickness of the Al–Ge–Al SBFET, the Ge device layer can be wet-chemically etched before device processing. A detailed process description and structural characterization including further HRTEM, energy dispersive x-ray spectroscopy, and electron backscatter diffraction investigations can be found in the work of Wind *et al.*[16] The lower panel in Fig. 1(a) shows exemplarily a cross-sectional scanning transmission electron microscopy (STEM) image of an ultra-scaled Ge nanosheet with a thickness T of only 10 nm (see the supplementary material for details). Making use of the highly p-doped Si handle wafer as a global back-gate, the Al–Ge–Al device can be operated as an accumulation SBFET.[16] Figure 1(b) shows the respective transfer characteristics for SBFETs with three different Ge channel thicknesses (T). All reveal a distinct p-type behavior, which is commonly observed for Ge nanostructures due to the surface doping effect.[17] Thereby, acceptor-like traps result in a shift of the energy band structure throughout the Ge channel.[18,19] Furthermore, based on the Arrhenius plot of temperature-dependent I/V measurements, it was observed that the effective Schottky barrier height of the Al–Ge junction exhibits a strong asymmetry between the barriers for electrons and holes, resulting from Fermi level pinning near the valence band.[20–22] However, for the devices with thinner channels the enhanced gating capability results in a significantly improved I_{ON}/I_{OFF} ratio with even more pronounced p-type behavior. Thus, as shown in the respective schematic band diagram in the inset of Fig. 1(b), high

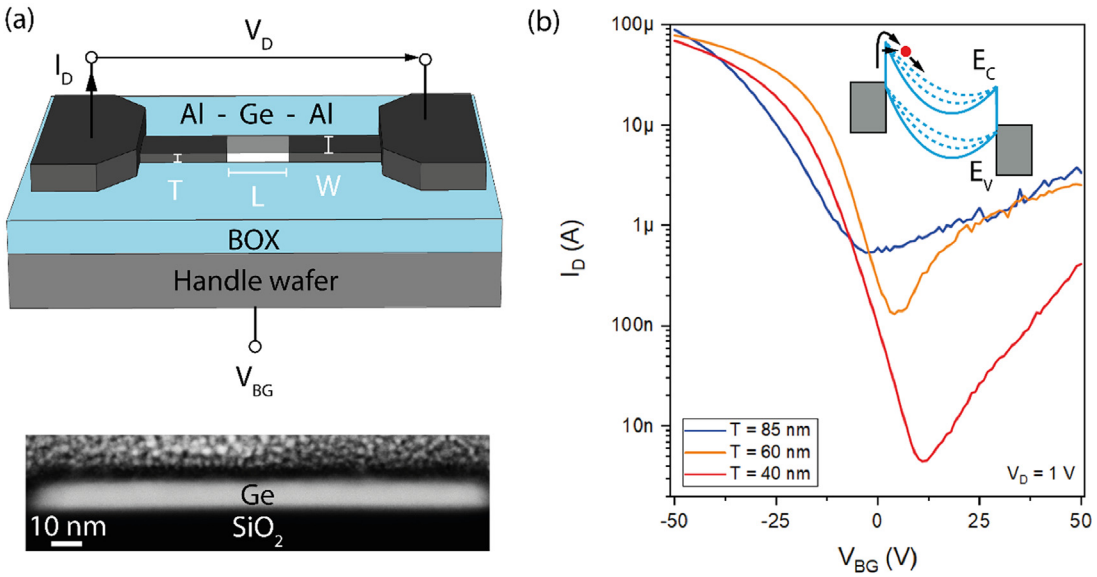

FIG. 1. (a) Schematic and STEM image of an Al–Ge–Al nanosheet device on a GeOI substrate. (b) Transfer characteristics at $V_D = 1$ V of Al–Ge–Al SBFET devices with different Ge channel thicknesses T but the same length and width of L = 3 μm and W = 100 nm, respectively. The schematic band diagram in the inset shows the electron injection at the Al–Ge interface at high positive gate and drain voltages.

positive gate and drain voltages are required to lower the effective barrier height for electron injection by Fowler–Nordheim tunneling and thermionic emission.

Figure 2(a) shows the respective I/V characteristics for the same devices at the maximum back-gate voltage of $V_{BG} = 50$ V. Even higher back-gate voltages would lead to irreversible damage to the gate oxide and ultimately to the breakdown and destruction of the devices. However, an increase in the drain voltage initially leads to a strong rise of the current, but then to a flattening or, for the devices with thinner Ge channels, even to a decrease in the current before it rises again. Thus, within a specific regime, an increase in the voltage across the device's terminals leads to a decrease in the output current, which characterizes the NDR effect. Thereby, the peak-to-valley ratio (PVR), which is defined by $PVR = I(V_{Peak})/I(V_{Valley})$ increases for the devices with the thinner Ge channel.

Figure 2(b) shows exemplarily the influence of the gate voltage on NDR behavior for the device with a Ge channel thickness of only 40 nm. Since NDR relies on the transfer of electrons into conduction bands with higher effective mass, it can only be observed at positive gate voltages, where current transport occurs through the electrons accumulated in the Ge channel. As the gate voltage increases, the overall current rises, and the NDR effect becomes more pronounced, leading to a higher PVR.

To demonstrate the generality and reproducibility, Fig. S1 compares 10 devices with various channel widths for each Ge layer thickness of T = 85, 60, and 40 nm, respectively. For those devices with Ge thicknesses of T = 60 or 40 nm, where NDR was clearly observed, the current at the peak maximum increases with the width of the devices, but the PVR remains largely unchanged. As we determined an average PVR of 1.25 ± 0.53 for the device with a Ge channel thickness of T = 60 nm and 2.5 ± 0.75 for a thickness of T = 40 nm, each based on measurements from 10 devices, a clear influence of channel thickness on the PVR values is evident.

At low temperatures and high electric fields, a negative differential mobility has been reported in Ge in the past and was attributed either to the presence of band nonparabolicity[23] or to an electron transfer mechanism[24] as for compound semiconductors. The particular NDR effect in Ge presented here, notably observed at room temperature, can be explained by a momentum space transfer of electrons between the L- and Δ-valley.[5] Figure 2(c) shows a sketch of the conduction band of Ge and the red arrow illustrates the proposed electron transfer path. Although the minimum of the conduction band of Ge lies at an L-point, sufficiently large electric fields initiate a momentum space transfer primarily to the Δ-valley of the conduction band, related to the high coupling efficiency between these two minima.[25,26] As the simulations carried out using first-principles and the Boltzmann transport equation, including the effects of intra- and inter-valley electron-phonon scattering, in Fig. 3(a) clearly show, the repopulation of electrons in the Δ-valleys increases rapidly with V_{DS} (see the supplementary material for details). In the simulations, we consider both ideal and Schottky contacts, meaning the entire voltage drop occurs across the Ge channel, or partially in the contacts. In the actual device, the voltage distribution is influenced by the component geometry and, most importantly, the gate voltage, which determines the effective barrier height and, consequently, the injection of charge carriers. As a result, a significant portion of the applied drain voltage also drops across the reverse-biased Schottky diode, leading to a lower voltage drop at the Ge segment than assumed in the simulations for ideal contacts. Regardless of the voltage range, a redistribution of electrons from the L-valley to the Δ- or Γ-valley is consistently observed across the entire simulated range as the drain voltage increases. Notably, even though the L- and Γ-minima are energetically closer in energy [see Fig. 2(c)], the electrons are more likely scattered to the Δ-minima rather than the Γ-minima due to the much larger density of states of the 6 Δ-valleys.[27] Figure 3(b) shows the corresponding simulated values of electron mobilities in the respective valleys as a function of drain voltage. The previously mentioned considerations regarding the comparability of the applied drain voltages in the simulations for Ohmic contacts and the actual experiment also apply here. Nevertheless, across the entire simulated voltage range, the Δ- and Γ-valleys, which become increasingly populated with rising drain voltage, exhibit lower mobilities. Overall, the scattering of electrons from the energetically favorable low effective mass L-valley to a heavy mass Δ-valley nearby, plus an increase in inter-valley electron-phonon

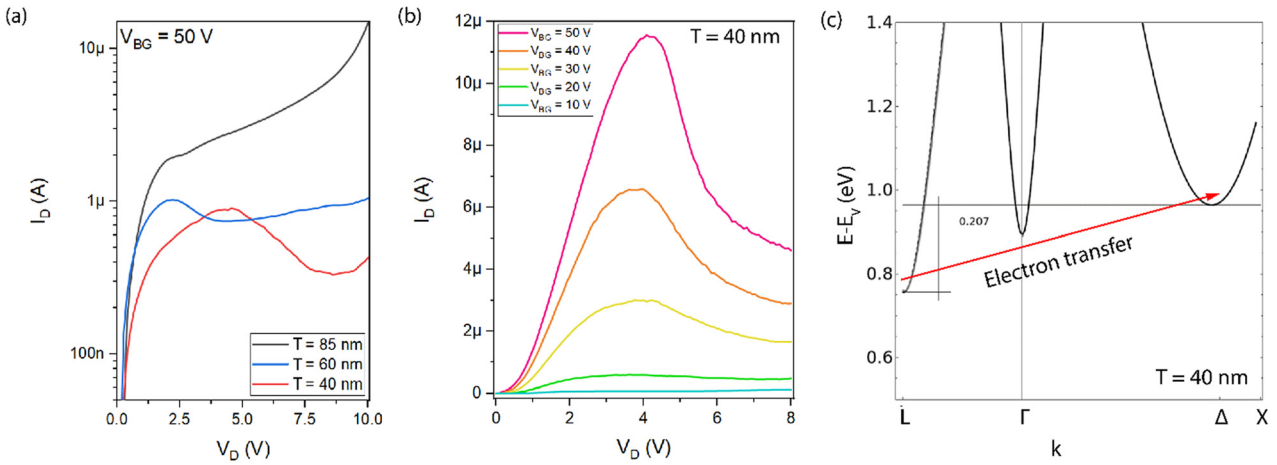

FIG. 2. (a) Semi-logarithmic I/V characteristics of Al–Ge–Al heterostructure devices with Ge channel thicknesses of T = 85, 60, and 40 nm. (b) Gate-tunability of the NDR in an Al–Ge–Al heterostructure device with a Ge channel thickness of T = 40 nm. (c) Electronic band structure of Ge vs crystal momentum.

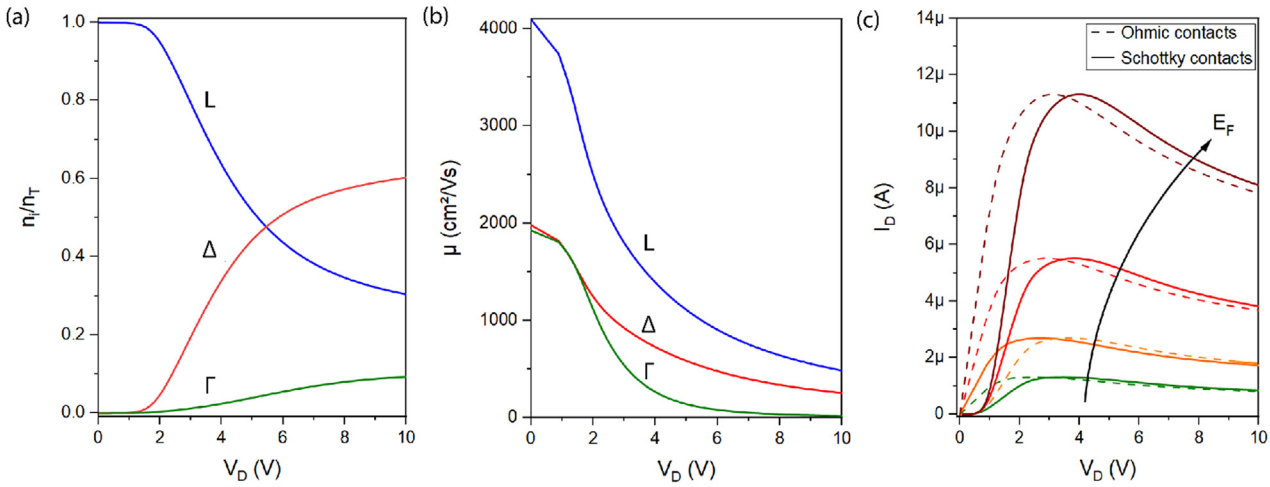

FIG. 3. (a) Relative occupation of the L-, Δ-, and Γ-valleys as a function of drain voltage V_D at a Fermi energy of $E_F = 0.56$ eV. (b) Mobility of electrons in L-, Δ-, and Γ- valleys as a function of drain voltage V_D at a chemical potential of $E_F = 0.56$ eV. (c) Calculated drain current I_D vs V_D at different E_F, mimicking the applied gate voltage. The E_Fs have been chosen such that they produce similar I_Ds as the measurement for the dimensions of T = 40 nm, W = 100 nm, and L = 3 μm. Solid lines: calculation including voltage drop due to Schottky contacts (barrier height 0.2 eV). Thin-dashed lines: calculation considering ideal Ohmic contacts.

scattering induces therefore NDR in the same way as the Gunn effect in GaAs.

Based on the simulated redistribution and mobility changes of electrons with increasing drain voltage, Fig. 3(c) presents a calculation of I/V characteristics for different Fermi energies. Increasing Fermi energies correspond to increasing gate voltages and the highest value, $E_F = 0.56$ eV, lies close to the conduction band for a bandgap of $Eg = 0.66$ eV,[28] indicating electron-dominated charge transport. As with the drain voltage, a direct transfer of the gate voltage from the experiment to the exact position of the Fermi energy in the simulation is hardly possible. The applied gate voltage modulates both the charge carrier density in the device channel (Ge) and the injection barrier at the Al–Ge interface. While both effects significantly influence the current flow, only the modulation of the charge carrier density is considered in the simulation. The effect of the additional Schottky barrier is also clearly visible (solid vs dashed lines) as an exponential increase in the current and a shift of the NDR peak to higher drain voltages. The NDR effect is well reproduced in the simulations, where we notice that the only effect of the Schottky barrier is the suppressed current at low voltages, resulting in a shift of the NDR peak to slightly higher voltages. The height of the peak is not affected by the contact barriers. Once the injection barrier is considered, the observed NDR effect is quantitatively well reproduced through the field-induced momentum space transfer of electrons and the associated change in their mobility.

The exploration of NDR in CMOS integrable Al–Ge–Al SBFET devices highlights the transformative potential of Ge-based nanoelectronics for advanced computing applications. Our experimental and simulation results confirm that the integration of tailored Ge nanosheets enables a highly tunable NDR effect accessible at room temperature, driven by electron transfer between conduction band valleys. This mechanism offers a promising alternative to conventional MOSFET architectures, with potential applications in multi-valued logic devices, static memory cells, and high-frequency oscillators. The distinct PVR observed across varying Ge layer thicknesses underlines the influence of effective electrostatic control on transport properties. These findings pave the way for further material and device engineering to optimize Ge-based systems for energy-efficient, high-performance computing. While the long-term behavior of the devices remains to be thoroughly investigated, initial results are promising. Even without specific optimization of the passivation to reduce the influence of interface traps, no significant degradation was observed after 50 switching cycles or continuous operation for 5 h at the maximum operating voltage of 8 V and a gate voltage of 40 V (see the supplementary material). By refining fabrication techniques and harnessing the unique properties of the materials involved, the integration of NDR in scalable nanosheet architectures emerges as a highly promising path for advancing nanoelectronics beyond the limitations of conventional silicon technologies.

See the supplementary material for details related to device fabrication, TEM investigations, electrical measurements and theoretical calculations, comparison of NDR measurements of various Al–Ge–Al nanosheet devices of different widths, and initial investigations into the long-term stability of the devices.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Masiar Sistani: Data curation (equal); Investigation (equal); Methodology (equal); Writing – original draft (equal). **Ezgi Tatli:** Investigation (equal). **Lukas Wind:** Investigation (equal). **Raphael Behrle:** Investigation (equal). **François Lefloch:** Resources (equal); Writing – review & editing (equal). **Sebastian Lellig:** Investigation (equal); Writing – review & editing (equal). **Xavier Maeder:** Resources (equal); Writing – review & editing (equal). **Walter M. Weber:** Resources (equal); Writing – review & editing (equal). **F. Murphy-Armando:** Investigation (equal); Methodology (equal); Software (equal); Writing – original draft (equal); Writing – review & editing (equal). **Alois Lugstein:** Conceptualization (lead); Funding acquisition (lead); Methodology (lead); Project administration (lead); Supervision (equal); Validation (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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