

Received 15 September 2025, accepted 29 September 2025,
date of publication 3 October 2025, date of current version 10 October 2025.

Digital Object Identifier 10.1109/ACCESS.2025.3617104

RESEARCH ARTICLE

Low Junction Capacitance PIN and Avalanche Photodiodes in 180 nm CMOS

CHRISTOPH GASSER¹, SEYED SAMAN KOHNEH POUSHI¹, (Member, IEEE),
SIMON MICHAEL LAUBE¹, KERSTIN SCHNEIDER-HORNSTEIN¹,
AND HORST ZIMMERMANN¹

Faculty of Electrical Engineering and Information Technology, Institute of Electrodynamics, Microwave and Circuit Engineering-E354, TU Wien, 1040 Vienna, Austria

Corresponding author: Christoph Gasser (christoph.e354.gasser@tuwien.ac.at)

This work was supported by Austrian Science Fund (FWF) through the Project USPAR under Grant 10.55776/P34649.

ABSTRACT This paper presents a comprehensive study of low-capacitance PIN photodiodes and avalanche photodiodes (APDs) implemented in 180 nm CMOS. The approach utilizes the dot-shaped cathode design to achieve hemispherical space-charge regions, effectively decoupling the photosensitive area from the junction capacitance and thus optimizing device performance for optical communication applications. Key device parameters—capacitance, bandwidth, light-sensitive area, and excess noise—are characterized and compared. All devices were fabricated on the same wafer for direct performance comparison. The presented dot-cathode photodiodes achieve significantly reduced total and normalized (per area) capacitance without compromising bandwidth compared to planar APDs. Among them, electric field line crowding (EFLC) based APDs demonstrate superior performance with the highest responsivity (0.4 A W^{-1} @ 642 nm), lowest capacitance per area ($1.58 \text{ aF } \mu\text{m}^{-2}$), and low excess noise ($F = 1.8$ @ $M = 10$) with a bandwidth of 1.6 GHz. In contrast, the presented n+/p-well (NPPW) based APDs exhibit high excess noise making them unsuitable for data receiver applications. Notably, the only PIN device presented, uniquely operates in *PIN mode* with maximum bandwidth, while all other devices show reduced bandwidth unless they are operated in *APD mode*.

INDEX TERMS PIN photodiode, p-i-n Diode, avalanche photodiode, APD, CMOS, low capacitance, red enhanced.

I. INTRODUCTION

The photodiode (PD) is crucial for optical communication receiver performance, with capacitance, bandwidth, responsivity, and light-sensitive area being key parameters. Image sensor PDs feature low capacitance as intended; however, they generally have a very small active area and limited bandwidth [1], [2], [3], [4], [5], [6]. PDs for optical communication need a high bandwidth and large active area but come with comparably high junction capacitance [7], [8].

The capacitance of p/n-junctions increases proportional to the PD area and inversely proportional to the width of the space-charge region [9]. The vertical depletion width can be significantly extended by embedding the PD into a thick and

low doped epitaxial layer, having a decreasing effect on the junction capacitance [10]. Further reduction can be obtained by reducing the p/n-junction area, which at first hand, will also decrease the light-sensitive area. However, by shrinking the cathode to a dot, a hemispherical space-charge region can be established, which leads to vertical and lateral depletion area and decouples the light-sensitive area from the p/n-junction area [9], [10], [11], [12].

This method has been applied to obtain enhanced silicon-photomultipliers (SiPMs) [10], single-photon avalanche diodes (SPADs) [11] and recently CMOS-compatible ultra-low-capacitance PIN-diodes [12], [13] and avalanche photodiodes (APDs) [14], [15]. The so-called dot-PIN diodes have already successfully been applied in ultra-sensitive optical receivers for data rates between 50 Mbps and 250 Mbps [16], [17], [18], [19], [20] enabling optical sensitivities of

The associate editor coordinating the review of this manuscript and approving it for publication was Sukhdev Roy.

down to 17.2 dB (at 100 Mbps, [20]) distance to the quantum limit.

This work provides an overview of research on dot photodiodes implemented in 180 nm CMOS and focuses on PIN-diodes and APDs. Some of the presented devices have already been published with somewhat different radii; however, previously unpublished measurement data for additional parameters are reported here for the first time. In addition, devices that were previously realized in a larger process node (350 nm) have been adapted for 180 nm CMOS and characterized, enabling a direct performance comparison within a uniform technology framework. Migrating to a smaller technology node size is motivated by the reduced parasitic capacitances in the receiver frontend. Especially scaling of the gate-drain overlap capacitance C_{gd} of the input transistor significantly improves the receiver sensitivity [16], [17], [18], [19], [20].

The following list provides a detailed description of each presented device, highlighting the contributions presented in this work. For devices that have been previously reported, the emphasis is placed on newly acquired measurement data that extend the characterization. For devices newly implemented in 180 nm CMOS, the focus is on design adaptations, implementation details, and their corresponding measurement results:

- **PIN-SD:** A single-dot (SD)-PIN diode, first published in [12], and already successfully applied in ultra sensitive integrator-based optical receivers running at a data rate of 50 Mbps [16] up to 250 Mbps [20]. This work adds capacitance and spectral responsivity measurements to the previous publication.
- **EFLC-SD:** A SD-APD based on the electric field line crowding (EFLC) effect, already published in [14]. This work reports the first implementation with an opto-window, extends the characterization by capacitance and spectral responsivity measurements, and the excess-noise factor measurements for higher gain by using an improved transimpedance amplifier.
- **NPPW-SD:** A SD-APD with a hemispherical n+/p-well multiplication region. The geometry was first realized in 350 nm CMOS with a grown epitaxial layer thickness of 15 μm [15]. The present work demonstrates the first 180 nm CMOS implementation, with some adaptations (different radii and thicker epitaxial layer) to the device geometry. Excess noise is reported for the first time.
- **EFLC-MD:** A multi-dot (MD)-APD based on the EFLC-SD cathode design, comprising four dots to increase the photosensitive area. This is the first reported implementation of this device topology.
- **NPPW-MD:** A MD-APD based on the NPPW-SD cathode design, also consisting of four dots. A 5×5 version of this topology was previously realized in 350 nm CMOS with a grown epitaxial layer thickness of 15 μm [15]; the present work reports its first implementation in 180 nm CMOS. In addition, the thickness of the low-doped epitaxial layer was

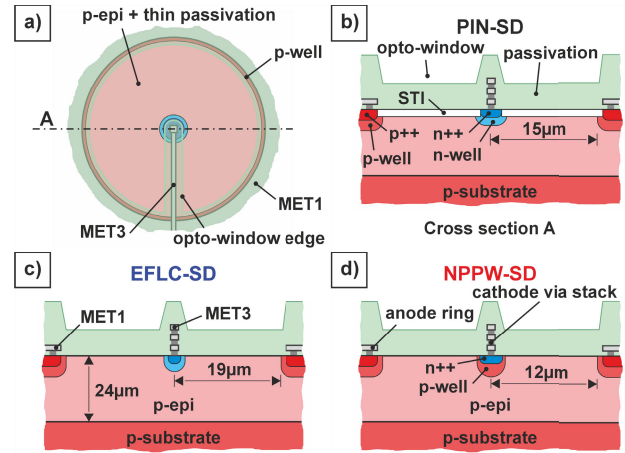


FIGURE 1. Schematic illustration of the single-dot (SD) PDs. a) top view of PIN-SD. The other devices look similar with different cathode dots and radii, b) cross section of PIN-SD, c) cross section of EFLC-SD and d) cross section of NPPW-SD.

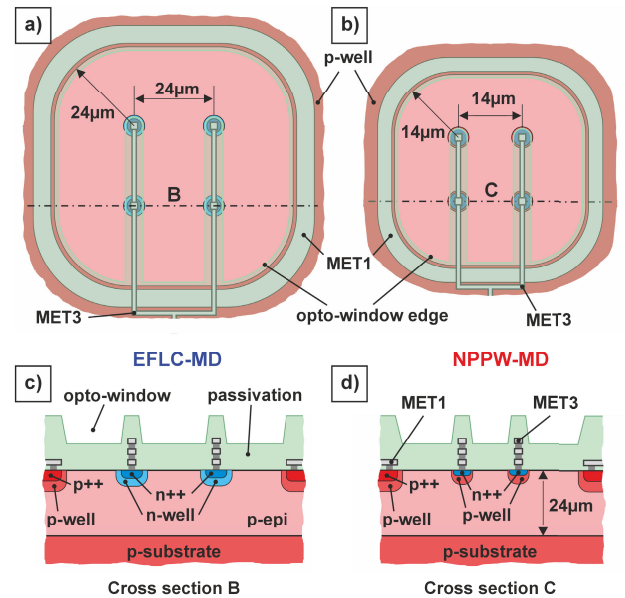


FIGURE 2. Schematic illustration of the multi-dot (MD) PDs, a) top view of EFLC-MD, b) top view of NPPW-MD, c) cross section of EFLC-MD and d) cross section of NPPW-MD.

increased to 24 μm . Excess noise is reported for the first time.

II. PHOTODIODES

A. PROCESS AND PD GEOMETRY

The presented PDs are fabricated in the same fabrication run in a 180 nm CMOS technology. The process features a p-doped epitaxial layer with a thickness of 24 μm and doping concentration close to $1.5 \cdot 10^{13} \text{cm}^{-3}$. The PDs are directly embedded in the p-epi layer, co-integrated circuits can be isolated in deep n-wells. The highly doped p-type bulk acts as a backside anode.

TABLE 1. Summary of PD geometry, units in μm .

	Type	Radius [†]	Pitch [‡]	Cathode radii [†]		
				n++	n-well	p-well
PIN-SD	PIN	15	-	0.71	1	-
EFLC-SD	APD	19	-	0.37	0.6	-
NPPW-SD	APD	12	-	0.85	-	0.85
EFLC-MD	APD	-	24	0.37	0.6	-
NPPW-MD	APD	-	14	0.85	-	0.85

[†] Drawn surface radius, the actual radius will be larger due to dopant diffusion.

[‡] Width of the device is three times the pitch.

The presented SD devices are circular (Fig. 1a), differing in drawn radius r and cathode dot constitution. The anode is formed by a p-well ring, contacted by metal layer 1 (MET1). The choice of metal layer for the cathode connection involves a trade-off between parasitic capacitance and light-shadowing. Parasitic capacitance is determined by the height above the substrate surface and the minimum width of the metal layer. The light-shadowing area refers to the portion of the PD covered by the cathode metal, which also increases with metal layer width. In the selected process, metal layer 3 (MET3) emerges as the optimal choice for the cathode dot connection, because it is the topmost thin metal layer. The MD devices are implemented in a 2×2 configuration, see Figs. 2a and b; the cathode dots are also connected via MET3. All presented devices contain an opto-window, which is exempted above the cathode metal connection, see Figs. 1 and 2. Passivation consists of a silicon-oxide/silicon-nitride stack (bottom to top); the opto-window is formed by etching the silicon nitride. Silicide is blocked above the light-sensitive area. The geometry parameters are listed in Table 1. Some of the presented PDs contain minor changes compared to the originally published devices. The electric-field distributions of the PIN-SD were published in [12], those of the EFLC APD in [14], and those of the NPPW APD in 350 nm CMOS in [15]. Since the radius and the epi-layer thickness are much larger than the n++ and p-well radius in both, 350 nm and 180 nm CMOS, their field distribution is qualitatively similar.

B. PIN-SD

The PIN-SD (Figs. 1a and 1b) has a radius of $15 \mu\text{m}$ (active area of $707 \mu\text{m}^2$) and an n++/n-well cathode dot with drawn¹ surface radii of $0.71 \mu\text{m}/1 \mu\text{m}$ (instead of $2 \mu\text{m}$ n-well radius in [12]). The distribution of the electric field for semi-spherical cathodes was derived in [9]. As the radial distance from the center increases, the electric field decays with $1/r^2$ [9], [13]. The space-charge region is hemispherical and reaches far into the p-epi layer.

In contrast to all other presented devices, the PIN-SD has additional shallow trench isolation (STI) oxide between cathode (n++) and anode (p++). The STI oxide has two effects that were reported in [12]: (i) it reduces the

effective pn-junction area, which slightly lowers the junction capacitance and (ii) it marginally reduces the responsivity. The PIN-SD was optimized for minimum capacitance, therefore it was implemented with STI. For all following APDs, however, we anticipated that the STI would introduce a higher surface trap density at the pn-junction, which could deteriorate the excess-noise performance. Therefore, the APD structures were realized without STI, accepting a slightly higher capacitance in exchange for likely improved noise characteristics.

C. EFLC-SD

The small size of the n++/n-well cathode causes the electric field lines to crowd near the cathode (EFLC-effect). For small enough radii, the electric field exceeds the breakdown limit for silicon ($\approx 2 \cdot 10^5 \text{ V/cm}$) close to the pn-junction, forming a multiplication zone to trigger avalanche events through impact ionization [11], [14]. Since more electric potential is used to create the multiplication zone, if the cathode dot radius is reduced, the depleted region shrinks, which results in a bandwidth reduction for constant surface anode radius [10]. This can be counteracted by decreasing the device radius.

The EFLC-SD (Fig. 1c) has a total radius of $19 \mu\text{m}$ (active area of $1134 \mu\text{m}^2$), approximately equivalent to the vertical thickness of the p-epi layer,² leading to a good approximation of a hemispherical space-charge region. It has a n++/n-well cathode dot with radii of $0.37 \mu\text{m}/0.6 \mu\text{m}$. The geometry is similar to [14] but the presented device is implemented with an opto-window.

D. NPPW-SD

In contrast to the previous two devices, the NPPW-SD has an n++/p-well cathode dot ($0.85 \mu\text{m} / 0.85 \mu\text{m}$), and the total radius is $12 \mu\text{m}$ (active area of $452 \mu\text{m}^2$). For this type of diode, avalanche breakdown is achieved as a result of the relatively high doping concentration of the p-well compared to that of the p-epi layer. It results in a peak electric field ($\approx 5 \cdot 10^5 \text{ V/cm}$) at the cathode/p-well junction.

Compared to the device from [15] (in 350 nm CMOS) with a drawn epi-layer thickness of $15 \mu\text{m}$, the p-epi layer is $24 \mu\text{m}$ thick in the 180 nm CMOS process used (to enhance the near-infrared responsivity), resulting in the backside anode having a weaker effect on the field distribution. Therefore, for the presented device, the radius of the central p-well was reduced by $0.05 \mu\text{m}$ and the total radius by $2 \mu\text{m}$ in order to counteract the expected drop in bandwidth.

E. EFLC-MD AND NPPW-MD

Both APD cathode designs were also realized in multi-dot (MD) configurations, enabling large-area photodetectors while maintaining low capacitance per unit area. Each MD device incorporates four cathode dots, as shown in the top views of Fig. 2a and b, with corresponding cross sections in

¹ Dopant diffusion causes the actual radius to exceed the drawn dimensions especially in the cases of the wells.

² During epitaxy, dopants of the p-substrate are expected to diffuse several micrometers into the p-epi layer.

Fig. 2c and d. As discussed in [15], the active area of MD devices can be scaled by increasing the number of dots, while keeping the pitch.

A key design parameter for MD arrays is the pitch. If it is too large, the electric field strength in the inter-dot regions decreases, which leads to higher carrier transit time and a reduced bandwidth. The maximum lateral drift distance occurs at $\text{pitch}/\sqrt{2}$ between four adjacent dots, where the electric field is weakest [15]. In other words, excessive pitch creates slow-response regions at the center of each group of four dots. For the EFLC-MD, a pitch of $24\text{ }\mu\text{m}$ results in an active area of $4690\text{ }\mu\text{m}^2$, whereas the NPPW-MD uses a $14\text{ }\mu\text{m}$ pitch, yielding $1596\text{ }\mu\text{m}^2$.

III. MEASUREMENT RESULTS

A. CAPACITANCE

The capacitance of the SD PDs was measured using test structures comprising 16 devices connected in parallel, with the results subsequently normalized to a single device. This parallel configuration was employed to improve measurement accuracy, as the capacitance of a single SD PD approaches the resolution limit of the measurement equipment.³ Due to area constraints, the test structures for the MD PDs consisted of individual devices only. Nevertheless, this does not compromise accuracy, since the expected capacitance of the MD PDs is substantially higher than that of the SD devices. The test structures each consisted of the device under test (DUT) and a calibration structure (see Fig. 3), in which the cathode connection is interrupted by a small gap located at a distance from the PD center equal to the device radius.

The measured capacitance comprises both the junction capacitance and parasitic contributions from the via stack and a short MET3 segment. For the SDs, this segment length corresponds to the PD radius (see Fig. 1a). In the case of the MDs, the parasitic contribution arises from the MET3 routing network, illustrated in Fig. 2a and b.

Up to a bias voltage of 7 V, both, PIN-SD and EFLC-SD show comparable widths of the depletion region (see Fig. 4). This similarity is caused by akin cathode dots, the slightly smaller one of EFLC-SD results in a lower minimum capacitance of 1.8 fF compared to 1.9 fF for PIN-SD. In contrast, the NPPW-SD achieves its minimum capacitance of 1.6 fF at a lower bias voltage of 2.5 V. Considering the capacitance per area, the EFLC-SD ($1.59\text{ aF}/\mu\text{m}^2$) performs best, followed by PIN-SD ($2.69\text{ aF}/\mu\text{m}^2$) and NPPW-SD ($3.54\text{ aF}/\mu\text{m}^2$).

The MD devices exhibit somewhat larger absolute capacitances, with the final value (8.1 fF) for the EFLC-MD being reached at 16 V, whereas the NPPW-MD attains its final value (7.6 fF) already at 4 V. The similarity of the final values suggests that a significant portion of the capacitance originates from parasitic contributions associated with the cathode routing network.

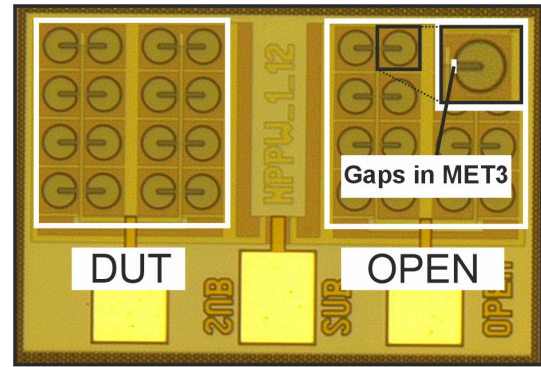


FIGURE 3. DUT (left) and open-calibration structure (right) for NPPW-SD capacitance measurement test structure. It contains 16 NPPW-SDs in parallel.

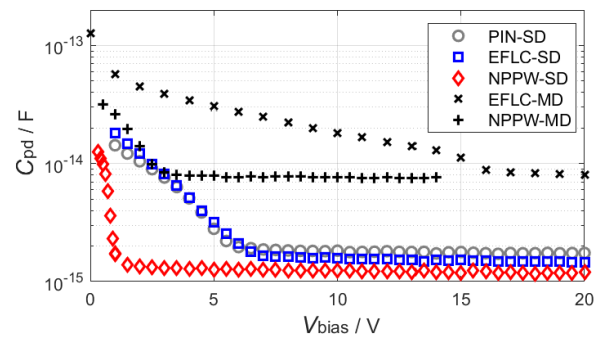


FIGURE 4. Capacitance results, the reported values include, in addition to the junction capacitance, a parasitic contribution from the cathode MET3 contacts. For the SDs the length corresponds to the PD radius (see Fig. 1a). For the MDs, the contribution corresponds to the MET3 routing network shown in Fig. 2a and b.

Both MD devices show less capacitance-per-area efficiency compared to the SD versions. The capacitance per area for the EFLC-MD device is $1.72\text{ aF}/\mu\text{m}^2$ and the NPPW-MD device has $4.76\text{ aF}/\mu\text{m}^2$. The scaling of the MD-area depends on the difference between MD-pitch and SD-radius. For example the NPPW-SD device has an area of $452\text{ }\mu\text{m}^2$ and the NPPW-MD device has only $1596\text{ }\mu\text{m}^2$. For 4 dots, the area is a factor of 3.53 higher, which leads to an increased capacitance density. Another factor is the metal routing network. The MD-pitch is larger than the SD-radius and the MDs have an additional metal segment connecting the two cathode branches. This results in more metal area per dot. Both phenomena reduce the area efficiency especially for low dot counts. For very large multi-dot diodes, the capacitance density improves due to a better scaling ratio and a more even share of the additional metal capacitance. This trend has been confirmed by capacitance measurements of 7-dot, 9-dot and 36-dot PIN PDs in [19].

B. RESPONSIVITY

The spectral responsivity was determined by illuminating the biased PDs with monochromatic light at various wavelengths. For each wavelength, the corresponding photocurrent⁴ and

³Agilent 4284A, $f = 1\text{ MHz}$, $V_{pp} = 250\text{ mV}$.

⁴Keithley 2612.

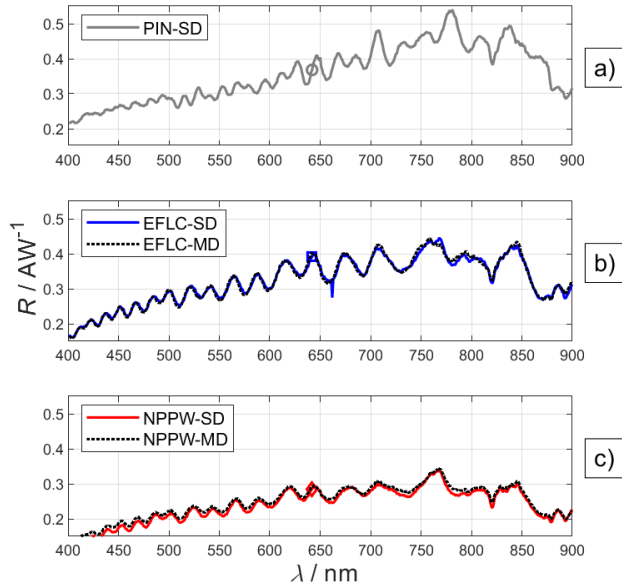


FIGURE 5. Spectral responsivity at $V_{\text{bias}} = 10\text{V}$ ($M = 1$).

incident optical power⁵ were measured, and the responsivity was calculated as their ratio. To account for variations in transmission through the single-mode fibers, a calibration step was performed prior to the measurements.

Despite having an opto-window, a ripple remains visible in the responsivity spectrum (see Fig. 5). This is likely caused by the fact that the opto-window extends only down to the MET2 layer, allowing refractive index-related Bragg reflections to occur in the layers beneath. At a wavelength of 642 nm, all devices based on the n++/n-well cathode exhibit, as expected, comparable responsivity. The PIN-SD achieves 0.37 A W^{-1} (Fig. 5a), the EFLC-SD 0.39 A W^{-1} , and the EFLC-MD 0.40 A W^{-1} (both Fig. 5b). In contrast, the NPPW-SD and NPPW-MD exhibit significantly lower responsivity, with both devices reaching 0.29 A W^{-1} at the same wavelength (both Fig. 5c). We attribute this to a smaller depleted volume compared to the PIN-SD and the EFLC devices. Consequently, a higher share of carriers are generated in diffusion regions and recombine before collection. All devices were biased at 10 V, which corresponds to a gain of $M = 1$.

C. GAIN

The gain of the PDs was determined by measuring their IV-characteristic⁵ under irradiation of a 642 nm laser⁶ (single-mode fiber) with an average optical power of $1\text{ }\mu\text{W}$. The gain was referred to the reverse current value at 1 V, and the dark current characteristic was subtracted for the calculation.

The EFLC-SD exhibits a relatively high breakdown voltage, resulting in $M = 100$ at 64 V (see Fig. 6). For $M < 20$, the gain slope increases gradually, enabling precise control of the multiplication factor. In contrast, the

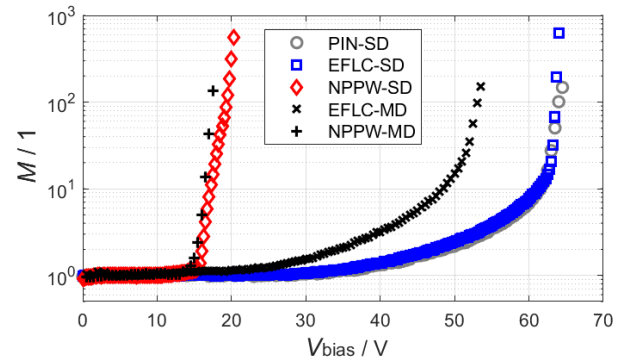


FIGURE 6. PD gain over bias voltage, dark current is considered.

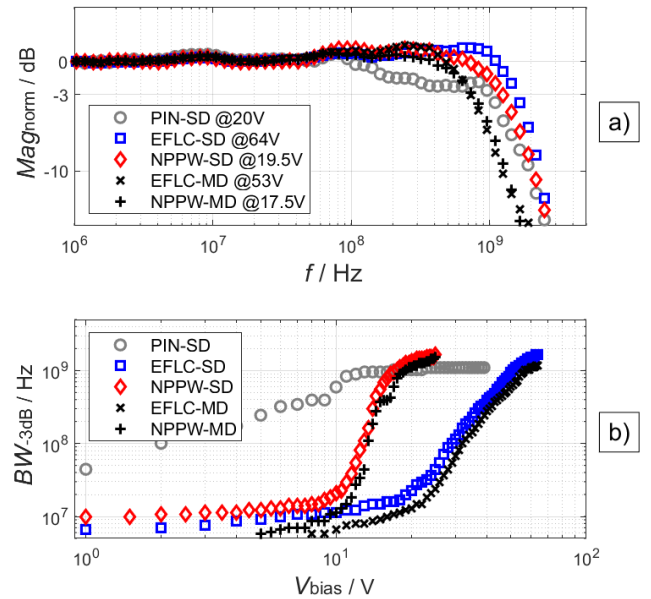


FIGURE 7. a) Normalized frequency response of proposed PDs (EFLC-SD, NPPW-SD, EFLC-MD, NPPW-MD) were biased for $M = 100$). b) Bandwidth over bias voltage.

NPPW-SD shows a significantly lower breakdown voltage and $M = 100$ is already achieved at 19.5 V, allowing operation at substantially lower bias voltages. Both MD PDs exhibit earlier breakdown than their SD counterparts, namely 53 V for the EFLC-MD and 17.5 V for the NPPW-MD.

Although designed as a PIN-diode, the PIN-SD exhibits a breakdown characteristic similar to that of the EFLC-SD, despite its larger n-well diameter. This similarity may result from the STI layer reducing the effective cathode n-well radius, making the geometry more similar to the EFLC-SD.

D. AC-RESPONSE

The frequency response was measured with a vector network analyzer.⁷ The cathode of the test structures was bonded to a $50\text{ }\Omega$ -transmission line (microstrip) that was connected to a bias-tee.⁸ The DC-bias voltage was applied between

⁵Thorlabs PM100USB-S150C.

⁶Thorlabs CLD1010LP & Thorlabs LP642-SF20, Bias current 60 mA.

⁷Rohde&Schwarz ZNB8.

⁸Picosecond 5530B.

TABLE 2. Summary of measurement results and comparison to other APDs.

	Junction	$A / \mu\text{m}^2$	C_{PD} / fF	$C_{PD}'' / \text{aF}\mu\text{m}^{-2}$	R / AW^{-1}	$V_{BD}^\dagger / \text{V}$	$BW_{\text{max}} / \text{GHz}$	$F_{10} / 1$	$F_{100} / 1$
[8]	planar, n++/pw/dnw	23200	125	5.38	0.41 *	66	0.85	-	10
[7]	planar, n++/pw	10000	150	15	0.35 *	30	1.15	-	7.9 - 11 [‡]
[28]	GaAsSb/AlGaAsSb ^x	31415	2500 ^o	79.6	0.503 ^x	49 ^o	-	1.52	-
[29]	InGaAs/AlAsSb ⁺	38012	-	-	0.92 ⁺	85 ^o	10 [#]	2.5	-
PIN-SD	dot, n++/nw	707	1.9	2.7	0.37	64.5	1	-	-
EFLC-SD	dot, n++/nw	1134	1.8	1.58	0.39	64	1.6 [†]	1.8	11
NPPW-SD	dot, n++/pw	452	1.6	3.54	0.29	19.5	1.25 [†]	600	200
EFLC-MD	dot, n++/nw	4690	8.1	1.72	0.40	53	0.72 [†]	1.8	11
NPPW-MD	dot, n++/pw	1596	7.6	4.76	0.29	17.5	0.73 [†]	600	200

* Wavelength 670 nm.

^x Values for APD_{125nm}-device, Wavelength 1550 nm.⁺ Values for P1-device, Wavelength 633 nm.[#] For $M = 10$.^o Determined from plotted data.[†] For $M = 100$.[‡] Values depend on opt. input power, 7.9 for 1 μW and 11 for 0.2 μW .

bias-tee and PD-anode using a source meter⁵. Since the bandwidth of the 642 nm laser source was not sufficient, we used a fast 675 nm multi-mode laser for the ac-response characterization. The potentially different responsivity at 675 nm does not affect the result, since we are interested in the normalized response. The bandwidth result is conservative, as PDs become slower with increasing wavelength.

Fig. 7a shows the frequency response of the presented PDs. The APDs were biased at $M = 100$, the PIN-SD was biased at $M = 1$. The maximum bandwidth is 1.0 GHz for the PIN-SD, 1.25 GHz for the NPPW-SD and 1.6 GHz for the EFLC-SD. Both MD devices have slightly lower bandwidth at $M = 100$, with 0.72 GHz for the EFLC-MD and 0.73 GHz for the NPPW-MD. Plotting the bandwidth as a function of bias voltage (Fig. 7b) reveals that the PIN-SD is the only device that can be operated at a low bias voltage (*gain* ≈ 1 : *PIN mode*), while reaching its maximum bandwidth. All other devices must be operated at a bias voltage where they already have gain (*APD mode*) to approach their maximum bandwidth.

E. NOISE

The excess noise factor (F) was determined from the power spectral density (PSD)⁹ of the APD photocurrent in the range of 100 MHz to 200 MHz under illumination at 642 nm⁷. Various avalanche gains (M) were obtained by adjusting the reverse bias voltage while monitoring the photocurrent⁵ ($M = 1$ reference taken at $V_{\text{bias}} = 10 \text{ V}$). The DUT cathodes were directly wire-bonded to the input of a custom-designed low-noise TIA with $R_T = 45.5 \text{ k}\Omega$ and $\text{BW} = 250 \text{ MHz}$.

For each bias point, the PSD was acquired with and without optical illumination, and the difference taken as the calibrated photocurrent PSD. The usable photocurrent range (0.2 μA to 2 μA) was defined by the TIA's input noise (lower bound) and its dynamic range (upper bound). Different optical input powers were applied to cover a broad range of gains while keeping the multiplied photocurrent within this range. Fiber alignment was verified at the start and end of

each measurement run. The excess noise factor F was then calculated for each bias point according to [21] (or [14]).

For the EFLC-SD, the excess noise factor was previously measured with the same method (but a commercial TIA with smaller measurement range) and published in [14]. The experimental results presented here (Fig. 8) extend the EFLC-SD characterization to $M = 100$ and include, for the first time, measurements of the NPPW-SD as well as of both MD versions. The EFLC-based devices exhibit $F = 1.8$ at $M = 10$ and $F = 11$ at $M = 100$, values comparable to those reported for planar Si APDs [7], [8]. Published results in [14] showed $F = 1.5$ at $M = 10$ for the same device.

In contrast, the NPPW-based devices show a steep increase in F even at low gain, reaching $F \approx 600$ at $M = 10$. Although F decreases thereafter, it remains at a high level with $F \approx 200$ at $M = 100$. This noise performance is significantly inferior to that of the EFLC-based devices and substantially worse than values reported for planar APD designs.

We hypothesize that the high excess-noise factor observed in the NPPW devices may be linked to the width of the multiplication region (region with $E > 2 \times 10^5 \text{ V/cm}$). In thick, approximately uniform-field multiplication regions, F follows McIntyre's theory, increasing with M and with the ionization-coefficient ratio [22]. When the multiplication layer is thinned to near the carrier dead-space length, dead-space effects suppress ionization, usually yielding F below the McIntyre prediction [23], [24], [25], [26]. However, ultrathin (or equivalently highly-localized field) non-uniform multiplication regions may increase the excess-noise factor, due to a softened ionization path-length distribution [27]. Moreover, an interaction with Si/SiO₂ interface states is likely, as the excess-noise factor F decreases with increasing optical power (i.e., with larger signal).

Electric-field distributions for the presented devices, published in [14] and [15], show profiles along a diagonal from the device center at the surface into the p-epi layer. Along this direction, the NPPW devices exhibit a narrow field peak of approximately 0.5 μm within the avalanche p-well, followed by a certain decay in field strength, particularly pronounced directly beneath the cathode dot. This highly

⁹Rohde&Schwarz FSP.

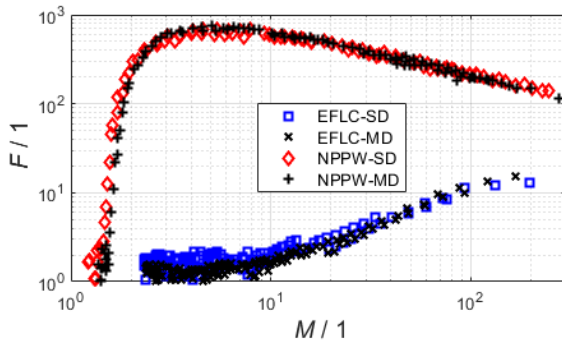


FIGURE 8. Excess noise factor of the presented APDs, determined at a wavelength of 642 nm.

localized peak may contribute to the observed high excess-noise factor. Since the NPPW-based devices in 350 nm [15] share a qualitatively similar field distribution, they likely also have a very high excess noise factor. In contrast to the NPPW devices, the multiplication region of the EFLC devices extends over a larger volume (approximately $1 \mu\text{m}$ along the plotted direction), and the electric field strength decreases more gradually with distance from the cathode.

IV. COMPARISON AND CONCLUSION

Tab. 2 summarizes the measurement results and compares them to two planar Si-APDs [7], [8] and two low-noise heterostructure APDs [28], [29]. The dot-cathode topologies achieve a substantial reduction in total capacitance and capacitance per area. The presented devices also show no bandwidth penalty relative to the Si-APDs. A key advantage of the CMOS platform, compared to heterostructure technologies, is the possibility of monolithic co-integration with electronic circuits, which makes it attractive for compact industry solutions. Mature CMOS processes have lower production cost and less process complexity but are usually outperformed by heterostructure-based technologies in the field of photodiodes. Nevertheless, when comparing the excess noise factors F at $M = 10$, our EFLC-based CMOS APDs achieve $F = 1.8$ at $\lambda = 642 \text{ nm}$. This performance lies between the two low-noise heterostructure APDs: [28] reports $F = 1.52$ at $\lambda = 1550 \text{ nm}$ in an AlGaAsSb heterostructure process, while [29] reports $F = 2.5$ at $\lambda = 633 \text{ nm}$ in an AlAsSb heterostructure process. This demonstrates that our EFLC-based APDs match the excess noise performance of advanced heterostructure technologies, while retaining the cost and integration benefits of the CMOS platform.

Comparing the presented dot-PDs, we have to conclude that the NPPW-based APDs are unsuitable for data receiver applications due to their high excess noise factor. Despite having the lowest responsivity, they might still offer a small-size, low capacitance and low breakdown voltage option for DC-sensing applications. In most other regards the EFLC-based APDs are superior. They show the highest responsivity, lowest capacitance per area and lowest excess noise. The PIN-SD, however, is the only device among those presented that can be operated in *PIN mode* while exhibiting

maximum bandwidth. All other devices show significantly less bandwidth in *PIN mode* compared to *APD mode*.

Ultimately, the EFLC-based APDs show great promise for enhancing the performance of ultra-sensitive PIN-diode receivers [16], [17], [18], [19], [20] by providing additional internal gain, which improves sensitivity without requiring complex changes in circuit design. Future work will focus on integrating EFLC-APDs into receiver architectures to exploit their gain benefits in data communication systems.

ACKNOWLEDGMENT

This research was funded in whole or in part by the Austrian Science Fund (FWF) [10.55776/P34649]. For open access purposes, the author has applied a CC BY public copyright license to any author accepted manuscript version arising from this submission. The authors would like to thank the TU-Wien Library for covering the open access fee.

REFERENCES

- [1] A. E. Gamal and H. Eltoukhy, "CMOS image sensors," *IEEE Circuits Devices Mag.*, vol. 21, no. 3, pp. 6–20, May 2005, doi: 10.1109/MCD.2005.1438751.
- [2] A. Theuwissen, "CMOS image sensors: State-of-the-art and future perspectives," in *Proc. 37th Eur. Solid State Device Res. Conf. (ESSDERC)*, Sep. 2007, pp. 21–27, doi: 10.1109/essderc.2007.4430875.
- [3] R. Xu, B. Liu, and J. Yuan, "A 1500 fps highly sensitive 256×256 CMOS imaging sensor with in-pixel calibration," *IEEE J. Solid-State Circuits*, vol. 47, no. 6, pp. 1408–1418, Jun. 2012, doi: 10.1109/JSSC.2012.2192662.
- [4] D. Wei and E. R. Fossum, "Towards a high-speed photon-counting CMOS quanta image sensor (QIS)," in *Proc. Int. Image Sensor Workshop*, Jun. 2021, doi: 10.60928/nqn6-1wq7. [Online]. Available: <https://imagesensors.org/papers/10.60928/nqn6-1wq7/>
- [5] J. Ma, S. Masoodian, D. A. Starkey, and E. R. Fossum, "Photon-number-resolving megapixel image sensor at room temperature without avalanche gain," *Optica*, vol. 4, no. 12, p. 1474, Nov. 2017, doi: 10.1364/optica.4.001474.
- [6] J. Ma, D. Zhang, O. A. Elgendy, and S. Masoodian, "A 0.19e[−] rms read noise 16.7 Mpixel stacked quanta image sensor with 1.1 μm -pitch backside illuminated pixels," *IEEE Electron Device Lett.*, vol. 42, no. 6, pp. 891–894, Jun. 2021, doi: 10.1109/LED.2021.3072842.
- [7] W. Gaberl, B. Steindl, K. Schneider-Hornstein, R. Enne, and H. Zimmermann, "035 μm CMOS avalanche photodiode with high responsivity and responsivity-bandwidth product," *Opt. Lett.*, vol. 39, no. 3, pp. 586–589, Feb. 2014, doi: 10.1364/ol.39.000586.
- [8] B. Steindl, R. Enne, S. Schidl, and H. Zimmermann, "Linear mode avalanche photodiode with high responsivity integrated in high-voltage CMOS," *IEEE Electron Device Lett.*, vol. 35, no. 9, pp. 897–899, Sep. 2014, doi: 10.1109/LED.2014.2336678.
- [9] B. J. Baliga and S. K. Ghandhi, "Analytical solutions for the breakdown voltage of abrupt cylindrical and spherical junctions," *Solid-State Electron.*, vol. 19, no. 9, pp. 739–744, Sep. 1976, doi: 10.1016/0038-1101(76)90152-0.
- [10] E. Engelmann, W. Schmailzl, P. Iskra, F. Wiest, E. Popova, and S. Vinogradov, "Tip avalanche photodiode—A new generation silicon photomultiplier based on non-planar technology," *IEEE Sensors J.*, vol. 21, no. 5, pp. 6024–6034, Mar. 2021, doi: 10.1109/JSEN.2020.3041556.
- [11] E. Van Slegheem, A. Suss, P. Boulenc, J. Lee, G. Karve, K. De Munck, C. Cavaco, and C. Van Hoof, "A near-infrared enhanced silicon single-photon avalanche diode with a spherically uniform electric field peak," *IEEE Electron Device Lett.*, vol. 42, no. 6, pp. 879–882, Jun. 2021, doi: 10.1109/LED.2021.3070691.
- [12] B. Goll, K. Schneider-Hornstein, and H. Zimmermann, "Dot PIN photodiodes with a capacitance down to 1.14 aF/ μm^2 ," *IEEE Photon. Technol. Lett.*, vol. 35, no. 6, pp. 301–304, Mar. 2023, doi: 10.1109/LPT.2023.3242047.
- [13] B. Goll, K. Schneider-Hornstein, and H. Zimmermann, "Ultra-low capacitance spot PIN photodiodes," *IEEE Photon. J.*, vol. 15, no. 2, pp. 1–6, Apr. 2023, doi: 10.1109/JPHOT.2023.3251893.

- [14] S. S. K. Poushi, C. Gasser, B. Goll, M. Hofbauer, K. Schneider-Hornstein, and H. Zimmermann, "A near-infrared enhanced field-line crowding based CMOS-integrated avalanche photodiode," *IEEE Photon. J.*, vol. 15, no. 3, pp. 1–9, Jun. 2023, doi: [10.1109/JPHOT.2023.3280251](https://doi.org/10.1109/JPHOT.2023.3280251).
- [15] S. S. K. Poushi, B. Goll, K. Schneider-Hornstein, M. Hofbauer, and H. Zimmermann, "Area and bandwidth enhancement of an n⁺/p-well dot avalanche photodiode in 0.35 μ m CMOS technology," *Sensors*, vol. 23, no. 7, p. 3403, Mar. 2023, doi: [10.3390/s23073403](https://doi.org/10.3390/s23073403).
- [16] K. Schneider-Hornstein, B. Goll, and H. Zimmermann, "Ultra-sensitive PIN-photodiode receiver," *IEEE Photon. J.*, vol. 15, no. 3, pp. 1–9, Jun. 2023, doi: [10.1109/JPHOT.2023.3279935](https://doi.org/10.1109/JPHOT.2023.3279935).
- [17] C. Gasser, S. M. Laube, K. Schneider-Hornstein, and H. Zimmermann, "Ultra sensitive PIN-diode receiver utilizing photocurrent integration on a parasitic capacitance," *IEEE Access*, vol. 12, pp. 118371–118376, 2024, doi: [10.1109/ACCESS.2024.3447731](https://doi.org/10.1109/ACCESS.2024.3447731).
- [18] C. Gasser, C. Ribisch, S. M. Laube, K. Schneider-Hornstein, and H. Zimmermann, "Ultrasensitive reset-less integrator-based PIN-diode receiver with input current control," *IEEE Solid-State Circuits Lett.*, vol. 8, pp. 17–20, 2025, doi: [10.1109/LSSC.2024.3520338](https://doi.org/10.1109/LSSC.2024.3520338).
- [19] S. M. Laube, C. Gasser, K. Schneider-Hornstein, and H. Zimmermann, "Highly-sensitive integrating optical receiver with large PIN photodiode," *IEEE Photon. J.*, vol. 16, no. 6, pp. 1–9, Dec. 2024, doi: [10.1109/JPHOT.2024.3487302](https://doi.org/10.1109/JPHOT.2024.3487302).
- [20] S. M. Laube, C. Gasser, K. Schneider-Hornstein, and H. Zimmermann, "Slow-slope reset scheme for highly-sensitive CMOS integrate-and-dump receiver OEIC," *IEEE Access*, vol. 13, pp. 154599–154609, 2025, doi: [10.1109/ACCESS.2025.3602093](https://doi.org/10.1109/ACCESS.2025.3602093).
- [21] T. Jukić, P. Brandl, and H. Zimmermann, "Determination of the excess noise of avalanche photodiodes integrated in 0.35- μ m CMOS technologies," *Opt. Eng.*, vol. 57, no. 4, p. 1, Apr. 2018.
- [22] R. J. McIntyre, "Multiplication noise in uniform avalanche diodes," *IEEE Trans. Electron Devices*, vols. ED-13, no. 1, pp. 164–168, Jan. 1966, doi: [10.1109/T-ED.1966.15651](https://doi.org/10.1109/T-ED.1966.15651).
- [23] B. E. A. Saleh, M. M. Hayat, and M. C. Teich, "Effect of dead space on the excess noise factor and time response of avalanche photodiodes," *IEEE Trans. Electron Devices*, vol. 37, no. 9, pp. 1976–1984, Sep. 1990, doi: [10.1109/16.57159](https://doi.org/10.1109/16.57159).
- [24] A. R. Pauchard, P.-A. Besse, and R. S. Popovic, "Dead space effect on the wavelength dependence of gain and noise in avalanche photodiodes," *IEEE Trans. Electron Devices*, vol. 47, no. 9, pp. 1685–1693, Sep. 2000, doi: [10.1109/16.861578](https://doi.org/10.1109/16.861578).
- [25] J. David and G. Rees, "Low noise avalanche photodiodes," in *Proc. 14th Annu. Meeting IEEE Lasers Electro-Opt. Soc. (LEOS)*, vol. 2, Nov. 2001, pp. 693–694, doi: [10.1109/LEOS.2001.969003](https://doi.org/10.1109/LEOS.2001.969003).
- [26] S. A. Plimmer, C. H. Tan, J. P. R. David, R. Grey, K. F. Li, and G. J. Rees, "The effect of an electric-field gradient on avalanche noise," *Appl. Phys. Lett.*, vol. 75, no. 19, pp. 2963–2965, Nov. 1999, doi: [10.1063/1.125202](https://doi.org/10.1063/1.125202).
- [27] O.-H. Kwon, M. M. Hayat, J. C. Campbell, B. E. A. Saleh, and M. C. Teich, "Effect of stochastic dead space on noise in avalanche photodiodes," *IEEE Trans. Electron Devices*, vol. 51, no. 5, pp. 693–700, May 2004, doi: [10.1109/TED.2004.825798](https://doi.org/10.1109/TED.2004.825798).
- [28] Y. Cao, T. Blain, J. D. Taylor-Mew, L. Li, J. S. Ng, and C. H. Tan, "Extremely low excess noise avalanche photodiode with GaAsSb absorption region and AlGaAsSb avalanche region," *Appl. Phys. Lett.*, vol. 122, no. 5, Jan. 2023, Art. no. 051103, doi: [10.1063/5.0139495](https://doi.org/10.1063/5.0139495).
- [29] X. Yi, S. Xie, B. Liang, L. W. Lim, J. S. Cheong, M. C. Debnath, D. L. Huffaker, C. H. Tan, and J. P. R. David, "Extremely low excess noise and high sensitivity AlAs_{0.56}Sb_{0.44} avalanche photodiodes," *Nature Photon.*, vol. 13, no. 10, pp. 683–686, Oct. 2019, doi: [10.1038/s41566-019-0477-4](https://doi.org/10.1038/s41566-019-0477-4).



CHRISTOPH GASSER received the B.Sc. degree in electrical engineering and information technology and the Dipl.-Ing. degree in embedded systems from TU Wien, Vienna, Austria, in 2018 and 2020, respectively, where he is currently pursuing the Dr. Techn. degree with the Institute of Electrodynamics, Microwave, and Circuit Engineering. His research focuses on highly sensitive optical receivers and analog integrated circuits.



SEYED SAMAN KOHNEH POUSHI (Member, IEEE) received the M.Sc. degree in electrical engineering from Tarbiat Modares University, in 2013, and the Ph.D. degree in CMOS integrated optical sensors from TU Wien, in March 2024. In 2019, he joined the Integrated Circuit Group with TU Wien as a Project Assistant. Since February 2024, he has been a Scientist in electronic sensors with Silicon Austria Laboratories. His research focuses on CMOS-based photodiodes and ASIC readout circuits.



SIMON MICHAEL LAUBE received the B.Sc. degree in electrical engineering and information technology and the Dipl.-Ing. degree in embedded systems from TU Wien, Vienna, Austria, in 2020 and 2021, respectively, where he is currently pursuing the Dr. Techn. degree in ultra-sensitive optical receivers.



KERSTIN SCHNEIDER-HORNSTEIN received the Dipl.-Ing. and Dr. Techn. degrees from Vienna University of Technology, Austria, in 2000 and 2004, respectively. Since 2001, she has been with the Institute of Electrodynamics, Microwave and Circuit Engineering, Vienna University of Technology. She is the author of the Springer book 'Highly Sensitive Optical Receivers', the co-author of the IOP Book "Single-Photon Detection for Data Communication and Quantum Systems", and the author and co-author of more than 65 journal and conference papers. Her major fields of interest are optoelectronics, photonic-electronic integration, and integrated circuit design.



HORST ZIMMERMANN received the Dr.-Ing., in 1991. He was an Alexander-von-Humboldt Research Fellow with Duke University, Durham, N.C., working on diffusion in Si, GaAs, and InP. In 1993, he joined Kiel University working on optoelectronic integration. Since 2000, he has been a Full Professor of circuit engineering with TU Wien, working on (Bi)CMOS analog and optoelectronic full-custom integrated circuits. He is the author of two Springer books, the co-author of five more Springer books, the author of an IOP book, the co-author of another IOP book, and the co-author of more than 600 publications on integrated PDs and integrated circuits.

...