



# APD direct detection receiver OEIC operating 14.1 dB above the shot noise quantum limit

SIMON MICHAEL LAUBE,<sup>\*</sup>  CHRISTOPH GASSER, KERSTIN SCHNEIDER-HORNSTEIN,  AND HORST ZIMMERMANN

*Institute of Electrodynamics, Microwave and Circuit Engineering, Technische Universität Wien, 1040 Vienna, Austria*

*\*simon.laube@tuwien.ac.at*

**Abstract:** This paper presents a highly-sensitive direct detection receiver optoelectronic integrated circuit (OEIC) with a dot-cathode avalanche photodiode (APD) in 180 nm high-voltage CMOS. Experimental sensitivity results of the APD receiver are compared to a reference PIN photodiode receiver. Both photodiodes are integrated on the same wafer, with identical integrate-and-dump source-follower front-end. At a wavelength of 642 nm, bit rate of 100 Mb/s with 80 % return-to-zero (RZ) on-off keying (OOK) modulation, and reference BER = 0.002, the APD receiver achieves a sensitivity of  $-56.6$  dBm. The sensitivity equals a gap of 14.1 dB to the shot noise quantum limit, that is an average of 71 photons per bit. The minimum normalized sensitivity ( $\eta\bar{P}$ ) improvement over the PIN receiver is 4 dB.

Published by Optica Publishing Group under the terms of the [Creative Commons Attribution 4.0 License](https://creativecommons.org/licenses/by/4.0/). Further distribution of this work must maintain attribution to the author(s) and the published article's title, journal citation, and DOI.

## 1. Introduction

APDs improve the sensitivity of optical direct detection (DD) receivers. Noise of the front-end circuit limits PIN photodiode (PD) receivers, but APDs overcome this limit with intrinsic current gain. Around 10 dB sensitivity advantage over PIN PDs can be expected [1].

In general, the shot noise quantum limit (QL) restricts the sensitivity of DD receivers [2]. Since the QL accounts for wavelength, bit rate, and bit error probability (BER), the gap between receiver sensitivity and the QL is an independent metric for receiver comparison. A discrete silicon-APD receiver [3] achieved a sensitivity that is 20.2 dB above the QL at a bit rate of 1.25 Gb/s. Highly-sensitive monolithic (Bi)CMOS receivers with planar APDs operated 22.5 dB above the QL at 500 Mb/s [4], and 19.8 dB above the QL at 1 Gb/s [5]. More recently, high-speed CMOS APD DD receivers demonstrated a sensitivity gap of 26.2 dB at 10 Gb/s [6] and 23.9 dB at 25 Gb/s [7]. The latter sensitivity was calculated from the optical modulation amplitude (OMA) sensitivity  $P_{\text{OMA}}$  [7] via  $\bar{P} = P_{\text{OMA}}/2$  [8].

The advent of CMOS single-photon avalanche diode (SPAD) receivers [9–16] improved DD sensitivity beyond previous APD and PIN receivers. The best SPAD receivers reduced the sensitivity gap to the QL to below 12 dB [13–16], at bit rates from 1 Mb/s [16] up to 400 Mb/s [13,15]. Most receivers employ large SPAD arrays [9,13–16] to compensate the limited bit rate or sensitivity of single SPADs [12]. SPAD limitations are caused by its dark count rate (DCR), after-pulsing probability (APP), dead time between detections, and low photon detection probability (PDP).

In an effort to catch up on SPAD receivers, recent research by our group focussed on highly-sensitive PIN PD DD receivers [17–21]. Their integrating front-ends accumulate photocharges only on the parasitic capacitances of the PD, transistors and metal tracks. Low-capacitance dot-cathode PIN PDs [22,23] are a major design element that promotes high sensitivity. Our best PIN receivers achieved a sensitivity gap of 17.3 dB to the QL at 50 Mb/s [17] and 100 Mb/s [21].

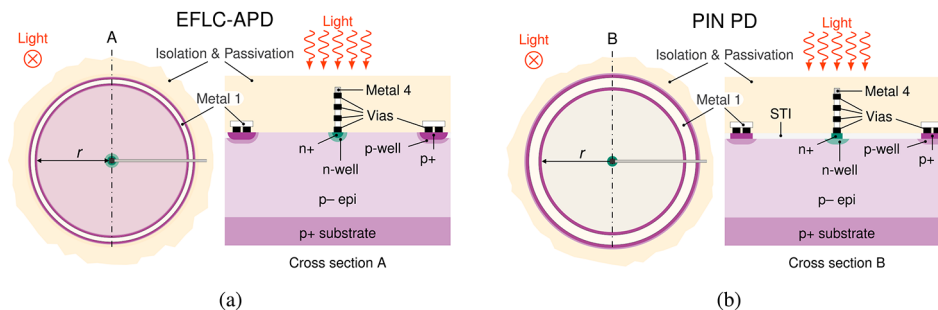
Although these PIN receivers reduce complexity by employing only a single PD, they have not yet matched SPAD sensitivity.

Considering the PIN receiver results, an APD DD receiver based on the same circuit principles seems promising. Until recently, however, no appropriate low-capacitance CMOS APD existed. Thanks to the introduction of the electric field-line crowding avalanche photodiode (EFLC-APD) [24,25], the requirements for a low-capacitance integrating APD DD receiver are now met.

In this paper we investigate the sensitivity improvement of an integrate-and-dump front-end with APD over PIN PD. We report the first monolithic receiver OEIC utilizing the EFLC-APD. Both, the EFLC-APD and a PIN PD of the same size (Section 2), are fabricated with a proven source follower (SF) front-end (Section 3). The main contribution is an experimental comparison of both receivers (Section 4), demonstrating the outstanding sensitivity of the APD receiver.

## 2. Photodiodes

For direct experimental comparison, the receiver is realized with an APD and a PIN PD on the same wafer in 180 nm high-voltage CMOS. The wafer is comprised of a p+ substrate with 24  $\mu\text{m}$  thick p- epitaxial layer that has a low doping concentration of around  $1.5 \times 10^{13} \text{ cm}^{-3}$ , see Fig. 1. Within the PDs, the p- layer acts as a thick absorption zone, that improves quantum efficiency for higher wavelengths. Both PDs make use of a hemispherical n+/n-well cathode. The standard n-well is contacted by the n+ region made from an NMOS transistor source/drain implant.



**Fig. 1.** Top view and cross section of single dot-cathode APD and PIN PD (not to scale). (a) Electric field-line crowding APD [24,25]. (b) PIN photodiode [23].

The APD is a single dot-cathode APD [24,25] with 0.6  $\mu\text{m}$  drawn radius of the n-well dot and 0.37  $\mu\text{m}$  drawn radius of the n+ contact, see Fig. 1(a). Due to this small cathode radius, the electric field is peaking near the cathode, resulting in avalanche gain. Because of these dense (crowded) electric field-lines at the cathode, we refer to the device as “EFLC-APD”. The circular p+/p-well surface anode has a radius of  $r = 15 \mu\text{m}$  (active area  $707 \mu\text{m}^2$ ). At a gain of  $M = 80$  and  $\lambda = 675 \text{ nm}$ , the EFLC-APD achieves a bandwidth of over 1 GHz [25]. The simulated capacitance of the EFLC-APD is 0.6 fF (not including cathode metal tracks). Electric field plots and detailed measurement data of the EFLC-APD are provided in [25].

The PIN PD is a single dot-cathode PD, device 2 from [23], with the same anode radius ( $r = 15 \mu\text{m}$ ) as the EFLC-APD, but different dot geometry, see Fig. 1(b). An n-well dot with a drawn radius of 1  $\mu\text{m}$  forms the cathode. At the surface, the active area is covered by shallow trench isolation (STI), except for the n+ contact of the cathode dot and the p+ contact of the surface anode. Based on simulation [23], the PD capacitance without metal tracks is 0.8 fF at  $-30 \text{ V}$ . The measured bandwidth at  $-30 \text{ V}$  and wavelength 675 nm is 300 MHz [23]. Electric field plots and further measurements are given in [23].

### 3. Receiver circuit

The front-end circuit of the DD receiver is essential for sensitivity. Front-end noise dominates the PIN receiver sensitivity and the worst case APD receiver sensitivity. In general, noise optimization is concerned with the reduction of PD capacitance and input node capacitance [26]. We employ an integrate-and-dump transimpedance amplifier (TIA) based on a SF stage. The circuit is identical to the reference PIN PD receiver in [21], that is also the reference receiver in this work. Monolithic integration of the TIA circuit with the EFLC-APD is presented for the first time in this work.

Figure 2 shows the full receiver architecture. Starting at the PD, the photocurrent exits the cathode and charges the input node capacitance  $C_T$ .  $C_T$  includes the gate-drain capacitance of  $M_0$  and  $M_1$ , the total gate capacitance of  $M_2$ , parasitic capacitances of metal tracks to neighbouring nodes, and the PD capacitance  $C_{PD}$ . Without the PD, the post-layout extracted input node capacitance (including Miller effect) is  $C_T - C_{PD} = 1.5$  fF. The input voltage  $v_{in}$  is buffered by the SF composed of  $M_2$  and  $M_3$ .  $M_2$  is capacitance-matched to  $C_{PD}$  and parasitic metal capacitance, to minimize its noise contribution [26]. The length  $L$  and width  $W$  of  $M_2$  are chosen to achieve both, capacitance match and large  $W/L$  to increase transconductance (bandwidth).  $M_3$  is designed to provide near-unity voltage gain (0.97 post-layout) of  $M_2$ . Therefore,  $L$  of  $M_3$  must be large, whereas its  $W$  is scaled accordingly to set the DC operating point. The NMOS capacitor  $C = 2$  pF eliminates the noise contribution of the bias transistor  $M_4$ . The SF front-end has a bandwidth of 135 MHz and thus defines the overall receiver frequency response. Post-layout simulation showed a total input-referred root mean square (RMS) noise current of 0.52 nA.

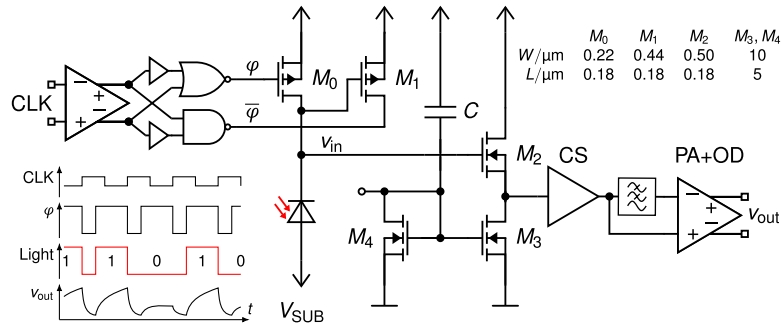


Fig. 2. Receiver circuit, transistor dimensions, and waveforms.

Transistor  $M_0$  implements the reset switch, whereas  $M_1$  is a dummy switch for the compensation of charge-injection [27–30]. Both,  $M_0$  and  $M_1$ , should have minimal size for low parasitic capacitance, but charge-injection compensation requires a larger size of  $M_1$ . The reset pulses  $\varphi$  and  $\bar{\varphi}$  are derived from an off-chip 100 MHz square wave clock (CLK). CLK amplitude and offset conform to the low-voltage differential signaling (LVDS) standard. An NMOS differential amplifier with resistive load amplifies the CLK to full-swing 1.8 V digital levels on-chip. The on-chip clock is delayed and combined with itself to obtain complementary rectangular pulses  $\varphi/\bar{\varphi}$  with a pulse-width of 2 ns. The 2 ns reset pulse-width is necessary to fully reset the input node after each bit, including a design margin to account for process variations of  $M_0$ . To avoid a power penalty, the optical signal is RZ OOK modulated.

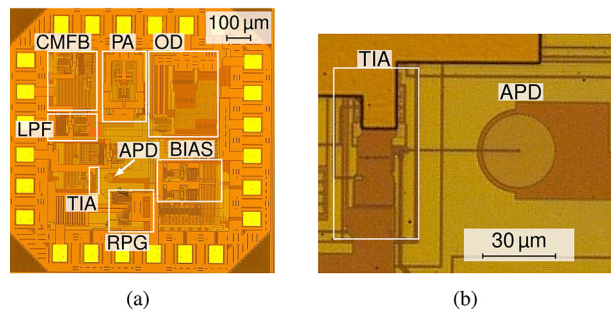
The receiver chip provides an analog output voltage  $v_{out}$ . Post-amplification of the SF output is required to drive the signal into an off-chip 100  $\Omega$  differential load. The first post-amplifier is an NMOS common-source (CS) stage with a voltage gain of 5 and a bandwidth of 400 MHz. A 2.5 kHz second-order Sallen-Key Butterworth lowpass transforms the single-ended CS output signal into a pseudo-differential signal. The following post amplifier (PA) is a fast differential

amplifier with resistive load and SF output buffer. Its post-layout voltage gain and bandwidth are set to 2.9 and 519 MHz, respectively, via resistive feedback. The output driver (OD) is a pair of PMOS SFs that achieve a bandwidth of 392 MHz into a  $100\ \Omega$  differential load.

Correlated double sampling (CDS) equalization [31] is applied to the analog output voltage  $v_{\text{out}}$  to recover the digital signal. In our prototype receiver, CDS is implemented off-chip as a post-processing software (see Section 4.1).

#### 4. Experimental results

The  $1.02\ \text{mm} \times 1.02\ \text{mm}$  receivers were fabricated in 180 nm high-voltage 5M1P CMOS without opto-window. A deep n-well isolates all circuits from the negatively biased substrate (PD anode). The PIN PD receiver substrate is biased at  $-30\ \text{V}$ . The APD receiver substrate bias is approximately  $-70\ \text{V}$ , but depends on the optimal gain setting. The TIA, PA, and OD supply voltage is  $2\ \text{V}$ ; the CLK and reset pulse circuit supply voltage is  $1.8\ \text{V}$ . Figure 3 shows a micrograph of the full APD chip and front-end with APD. Two samples were measured for the APD and PIN PD, respectively.



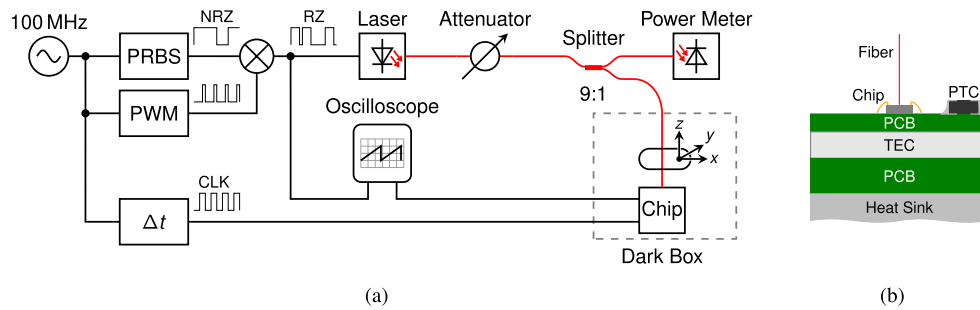
**Fig. 3.** APD chip micrograph with circuit blocks annotated. (a) Full chip. (b) Front-end section.

##### 4.1. Methods

The experimental setup is shown in Fig. 4(a). Each chip is mounted and wire-bonded to a PCB assembly. A metal dark box encloses the PCB assembly to block ambient light. To avoid temperature shift of the breakdown voltage, the temperature of the APD receivers is controlled to  $25\ ^\circ\text{C}$  on the PCB by a thermoelectric cooler (TEC), see Fig. 4(b). A positive temperature coefficient (PTC) thermistor senses the temperature on the PCB. The temperature of the PIN receivers is not controlled (ambient  $20\ ^\circ\text{C}$ ), because they were mounted on a different PCB assembly. Moreover, temperature dependence is negligible for the PIN PD, because it is biased below breakdown.

Chip clock generation and pseudorandom bit sequence (PRBS) modulation are based on a sinusoidal 100 MHz signal from a function generator (Agilent 81150A). A commercial PRBS generator (Sympuls BMG2500) produces the non-return-to-zero (NRZ) OOK PRBS15 test pattern. We use a custom-built emitter-coupled logic (ECL) pulse-width modulation (PWM) circuit (Analog Devices MAX40026 & Microchip SY89295U) that outputs periodic 2 ns pulses. The pulses gate (onsemi MC100LVEP05) the NRZ PRBS signal to yield the RZ OOK modulated PRBS signal. An amplifier (Analog Devices ADL5569) boosts the RZ signal to 1.35 V peak-to-peak voltage, which directly modulates a 642 nm laser (Thorlabs CLD1010LP & Thorlabs LP642-SF20, bias current 55 mA).

Single-mode fibers (Thorlabs SM600, mode field diameter  $3.6\ \mu\text{m}$  to  $5.3\ \mu\text{m}$ ) guide the light through an electronic attenuator (Thorlabs V600F) and a 9:1 splitter (Thorlabs TW630R2F2).



**Fig. 4.** Experimental setup for BER measurement. (a) Block diagram. (b) Cross section of the APD chip PCB assembly (not to scale).

The reference branch (90 %) of the splitter is connected to a power meter (Thorlabs PM100USB & Thorlabs S150C; calibration factor 0.1014) to measure the optical power. The actual power ratio between the two branches is calibrated once before chip measurements. A motorized  $xyz$ -stage (Thorlabs MTS50/M-Z8) is used for fiber alignment.

The chip clock (CLK) is delayed (Microchip SY89295U) to compensate the static delay of all cables and optical fibers. Since the delay line is digital, it simultaneously delays and converts the sinusoidal reference into a square wave CLK.

An oscilloscope (Keysight MSOV204A) samples the analog chip output voltage and the RZ PRBS for BER analysis. Its sample rate is 20 GS/s and the analog bandwidth was set to 1 GHz to record all significant harmonics of the 100 Mb/s analog voltage. A continuous stream of more than  $10^6$  data bits is recorded for each optical power setting. CDS [31] and BER computation are implemented in a Python script that processes the stored waveforms. Any static delay between PRBS and chip output is synchronized via correlation. Sample instants and bit decision threshold are optimized for each waveform (i.e. optical power) to obtain the minimal BER. Due to the limited record length of 1 Mb, only BERs above  $10^{-6}$  can be resolved.

The substrate bias is provided by an electrometer (Keysight B2987A). In addition, the electrometer allows substrate current measurements.

#### 4.2. Sensitivity

Because the PDs are covered by the full isolation/passivation stack (no opto-window, cf. Figure 1), process variations of the responsivity  $\mathcal{R}$  and quantum efficiency  $\eta$  occur.  $\mathcal{R}$  and  $\eta$  of each sample are calculated from the measured chip substrate current at different optical powers, see Table 1. For this measurement we set the APD substrate bias to  $-40$  V, to avoid avalanche gain. The APD and PIN PD show similar  $\mathcal{R}$  and  $\eta$ , with anticipated process variations.

**Table 1. Measured responsivity, quantum efficiency, and sensitivity at BER = 0.002 and  $\lambda = 642$  nm**

	$\mathcal{R}/(\text{A/W})$	$\eta$	$V_{\text{SUB}}/\text{V}$	$\bar{P}/\text{dBm}$	$\Delta P/\text{dB}$
PIN(1)	0.240	0.464	-30.00	-49.41	21.27
PIN(2)	0.362	0.700	-30.00	-52.06	18.62
APD(1)	0.303	0.586	-71.25	-56.56	14.13
APD(2)	0.298	0.576	-67.50	-55.16	15.53

$\mathcal{R}, \eta$  of APDs measured at  $V_{\text{SUB}} = -40$  V

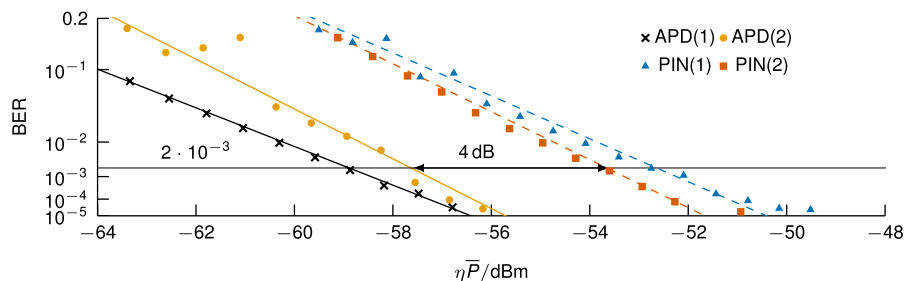
To find the optimum APD gain  $M$ ,  $V_{\text{SUB}}$  was varied in increments of 250 mV near the breakdown voltage ( $\approx 70$  V). As shown in Table 1, the two APD samples have different optical

bias points. Note that we cannot determine the value of  $M$  from the substrate current at the sensitivity, because the weak photocurrent is indistinguishable from other substrate currents, such as deep n-well leakage. Due to the nonlinearity of avalanche breakdown, APD gain increases exponentially with reverse bias voltage. Therefore, deviations from the optimal APD reverse bias are critical, if they increase  $M$  and thus excess noise. Starting at the optimum bias, we found that a 250 mV increase towards higher  $M$  increased the BER by a factor of 7.8. In contrast, a bias decrease by 2 V towards lower  $M$  only increased the BER by a factor of 4.1. At the optimum bias, the balance between APD gain, APD excess noise, and front-end noise results in the highest sensitivity.

The measured substrate dark current of both samples is below  $0.1 \mu\text{A}$  at  $V_{\text{SUB}} = -70 \text{ V}$ . Note, however, that the large-area deep n-wells, that isolate the circuits from the substrate, may contribute the major part of this current.

Absolute receiver sensitivity  $\bar{P}$  and the distance to the QL  $\Delta P$  are shown in Table 1. The best APD receiver achieved a sensitivity of  $2.21 \text{ nW}$  ( $-56.56 \text{ dBm}$ ) at  $100 \text{ Mb/s}$  and at the reference  $\text{BER} = 2 \cdot 10^{-3}$ . This equals a distance of  $14.13 \text{ dB}$  to the QL, corresponding to an average of 71 photons per bit. The APD(1) sample improves the sensitivity by  $4.5 \text{ dB}$  compared to the PIN(2) result. Overall, the absolute APD advantage is between  $3.1 \text{ dB}$  and  $7.1 \text{ dB}$ .

To separate the influence of the isolation/passivation stack from the intrinsic sensitivity, CDS BER is plotted against the detected power  $\eta\bar{P}$  in Fig. 5. This normalized setting facilitates a less biased comparison between APD and PIN results. The normalized APD advantage ranges from  $4.0 \text{ dB}$  to  $6.1 \text{ dB}$ , where APD(1) is  $5.3 \text{ dB}$  more sensitive than the better PIN(2) sample. Compared to the absolute sensitivity advantage (Table 1), it is evident that the isolation/passivation stack adds around  $1 \text{ dB}$  of variation at either end of the range. The remaining variation between APD(1) and APD(2) in Fig. 5 is due to the process variation of the SF front-end and EFLC-APD. Since the sensitivity difference of around  $1 \text{ dB}$  between the APD samples is strictly less than the APD sensitivity advantage, we infer that process variations are insignificant to the overall result.



**Fig. 5.** Measured BER versus detected power at  $100 \text{ Mb/s}$ ,  $80\%$  RZ modulation. The lines are least squares fitted to the measured data.

Although our experimental data show a distinct improvement over the PIN receiver, the typical  $10 \text{ dB}$  value [1,4] has not been achieved. APD excess noise [32] could limit sensitivity at high gain  $M$ . The measured excess noise factor  $F$  of the EFLC-APD [25] does not suggest such a limit for  $M < 60$ , but our EFLC-APD receiver may operate at higher gain. As mentioned above, we cannot measure  $M$  with our experimental setup. According to theory, the relation between  $M$  and  $F$  dictates the optimal  $M$ . At very low optical power  $M$  should be large, which may cause high excess noise. To retain the necessary signal-to-noise ratio of the APD receiver in this case,  $M$  must be reduced to lower  $F$ .

### 4.3. Comparison

Table 2 relates the sensitivity of our EFLC-APD to state-of-the-art DD receivers. Our EFLC-APD receiver bridges the gap between our highly-sensitive PIN receivers [17,18,21] and SPAD receivers [12–15]. Both, the PIN and SPAD receivers operate at similar bit rates between 20 Mb/s and 400 Mb/s. The best PIN receivers [17,21] are 3 dB less sensitive than our EFLC-APD receiver. This result is in line with the PIN vs. APD comparison presented in this work, see Section 4.2. Although we cannot match the sensitivity of the SPAD array receivers [13–15], our EFLC-APD receiver requires only a single APD. Compared to the single-SPAD receiver [12], the EFLC-APD receiver is both faster and equally sensitive. The main disadvantage of the EFLC-APD receiver is its high APD bias voltage, compared to PIN PDs and SPADs that require below 32 V.

**Table 2. Comparison to state-of-the-art**

Ref.	Process	Power cons. $P_S$ /mW	PD Type (Reverse Bias)	Bit Rate 1/Mb/s)	BER	Wavel. $\lambda$ /nm	Sensitivity $\bar{P}$ /dBm	Dist. to QL $\Delta P$ /dB	Photons $\bar{n}_{ph}^d$
[4] <sup>a</sup>	350 nm <sup>b</sup>	251	APD (18.3 V)	500	$10^{-9}$	675	-35.8	22.5	491
[3]	Discrete	—	APD (—)	1250	$10^{-9}$	820	-35	20.2	290
[5] <sup>a</sup>	350 nm	182	APD (73.7 V)	1000	$10^{-9}$	675	-35.5	19.8	264
[18] <sup>a</sup>	350 nm	3.9 <sup>c</sup>	PIN (20 V)	100	$2 \cdot 10^{-3}$	642	-52.3	18.4	191
[17] <sup>a</sup>	180 nm	24	PIN (20 V)	50	$2 \cdot 10^{-3}$	635	-56.4	17.3	149
[21] <sup>a</sup>	180 nm	164	PIN (32 V)	100	$2 \cdot 10^{-3}$	642	-53.5	17.2	145
[12] <sup>a</sup>	350 nm	281	SPAD (32 V)	50	$2 \cdot 10^{-3}$	635	-57.0	16.6	127
This work	180 nm	164	APD (73.25 V)	100	$2 \cdot 10^{-3}$	642	-56.6	14.1	71
[12] <sup>a</sup>	350 nm	119	SPAD (32 V)	20	$2 \cdot 10^{-3}$	635	-64.0	13.6	64
[13]	130 nm	115	64×64 SPAD (15.2 V)	400	$2 \cdot 10^{-3}$	450	-49.9	13.2	58
[13,14]	130 nm	115	64×64 SPAD (15.2 V)	50	$2 \cdot 10^{-3}$	450	-60.5	11.7	41
[15]	Discrete	—	SiPM, 5676 SPADs (28 V)	400	$10^{-3}$	405	-50.8	11.3	38

<sup>a</sup>Work by our research group.

<sup>b</sup>BiCMOS

<sup>c</sup>Without output driver.

<sup>d</sup>Average per bit. All results converted to BER = 0.002, assuming constant  $\Delta P$ :  $\bar{n}_{ph} = -1/2 \cdot \ln(2 \cdot 0.002) \cdot 10^{\Delta P/10}$

Although previous APD receivers [3–5] achieved distinctly higher bit rates than the EFLC-APD receiver, they are at least 5.7 dB less sensitive. The most sensitive APD receiver [5], however, requires an equally high APD bias voltage than our EFLC-APD receiver.

In terms of power consumption, the EFLC-APD receiver is comparable to previous APD receivers [4,5] and SPAD receivers [12–14]. The majority of highly-sensitive PIN receivers [17,18] consumes less power than the EFLC-APD receiver. Note, however, that most of the EFLC-APD receiver power consumption is due to the wideband PA and OD design (cf. Section 3). These stages may be optimized, and will not be required if a fully digital output is realized.

All APD [3–5] and SPAD [12–15] receivers, including this work, require temperature control to stabilize their breakdown voltage. This is a disadvantage of the EFLC-APD receiver compared to the PIN receivers [17,18,21].

## 5. Challenges

Monolithic integration of the EFLC-APD presents some challenges. First, the high substrate bias of around -70 V requires more stringent circuit isolation, compared to the lower -30 V of the PIN PD. The (surface) geometry of the deep n-well has to be carefully designed. Rounded deep n-well corners increase protection against deep n-well to substrate breakdown [33,34]. Additionally,

sufficient lateral distance between APD and front-end circuit (deep n-well) is necessary to avoid photocurrent losses [34]. The device simulation in [34] recommends a minimum distance of 10  $\mu\text{m}$  between the deep n-well and the surface anode of the PIN PD. For monolithic integration of the EFLC-APD in this work, we doubled the distance to 20  $\mu\text{m}$  because of the high substrate bias. The additional distance, however, increases the parasitic capacitance of the metal tracks by approximately 150 aF, i.e. around 6 % of the total input node capacitance. Because front-end noise increases with capacitance [26], longer distance also deteriorates sensitivity.

The highest sensitivity occurs at the specific APD gain that optimizes the trade-off between APD excess noise and front-end circuit noise [1,8]. McIntyre's APD noise theory [32] leads to well-known formulas for the optimal gain [1,8]. As discussed in [25], however, the McIntyre theory cannot be applied to the EFLC-APD due to its inhomogeneous electric field. Moreover, monolithic integration inhibits measurement of the APD gain characteristic. Therefore, we determined the optimal bias (gain) experimentally, as described in Section 4.2.

Another difficulty is input overload current. Simultaneous application of high avalanche gain and high optical power (above 1  $\mu\text{W}$ ) can destroy the EFLC-APD. Two reasons seem plausible: Firstly, the high current density at the small cathode dot may destroy the dot or its contact. Secondly, because of the ultra-low input capacitance, high input current may quickly charge the input node to a voltage beyond the limits of the input transistors. Unfortunately, we cannot verify our assumptions via measurements, because the cathode node is inaccessible in the monolithic OEIC. On the contrary, sufficiently low APD gain does not destroy the chip, even at 10  $\mu\text{W}$  optical power.

## 6. Conclusion

A monolithic EFLC-APD receiver OEIC in 180 nm high-voltage CMOS was presented. The sensitivity of the APD receiver approached the SPAD range. At 100 Mb/s, the APD receiver achieved a best-case sensitivity of  $-56.56$  dBm, that is a gap of 14.1 dB to the shot noise QL. Compared to the reference PIN receiver with the same integrate-and-dump TIA, the EFLC-APD improved the (normalized) sensitivity by 4 dB. On the downside, the high bias voltage of the EFLC-APD complicates monolithic integration.

**Funding.** Austrian Science Fund (P34649).

**Acknowledgment.** This research was funded in whole or in part by the Austrian Science Fund (FWF) grant DOI: 10.55776/P34649. The authors acknowledge TU Wien Bibliothek for financial support through its Open Access Funding Programme. The authors would like to thank A. Zimmer from X-FAB, Erfurt, Germany for chip fabrication and technical support.

**Disclosures.** The authors declare no conflicts of interest.

**Data availability.** Data underlying the results presented in this paper are not publicly available at this time but may be obtained from the authors upon reasonable request.

## References

1. T. V. Muoi, "Receiver design for high-speed optical-fiber systems," *J. Lightwave Technol.* **2**(3), 243–267 (1984).
2. J. R. Barry and E. A. Lee, "Performance of coherent optical receivers," *Proc. IEEE* **78**(8), 1369–1394 (1990).
3. H. Le Minh, D. O'Brien, G. Faulkner, *et al.*, "A 1.25-Gb/s Indoor Cellular Optical Wireless Communications Demonstrator," *IEEE Photonics Technol. Lett.* **22**(21), 1598–1600 (2010).
4. T. Jukic, B. Steindl, R. Enne, *et al.*, "200  $\mu\text{m}$  APD OEIC in 0.35  $\mu\text{m}$  BiCMOS," *Electron. Lett.* **52**, 128–130 (2016).
5. D. Milovančev, P. Brandl, T. Jukić, *et al.*, "Optical wireless APD receivers in 0.35  $\mu\text{m}$  HV CMOS technology with large detection area," *Opt. Express* **27**(9), 11930–11945 (2019).
6. S. Nayak, A. H. Ahmed, A. Sharkia, *et al.*, "A 10-Gb/s  $-18.8$  dBm Sensitivity 5.7 mW Fully-Integrated Optoelectronic Receiver With Avalanche Photodetector in 0.13- $\mu\text{m}$  CMOS," *IEEE Trans. Circuits Syst. I* **66**(8), 3162–3173 (2019).
7. K. C. Chen and A. Emami, "A 25-Gb/s Avalanche Photodetector-Based Burst-Mode Optical Receiver With 2.24-ns Reconfiguration Time in 28-nm CMOS," *IEEE J. Solid-State Circuits* **54**(6), 1682–1693 (2019).
8. E. Säckinger, *Analysis and Design of Transimpedance Amplifiers for Optical Receivers* (Wiley, 2018).
9. E. Fisher, I. Underwood, and R. Henderson, "A Reconfigurable Single-Photon-Counting Integrating Receiver for Optical Communications," *IEEE J. Solid-State Circuits* **48**(7), 1638–1650 (2013).

10. D. Chitnis and S. Collins, "A SPAD-Based Photon Detecting System for Optical Communications," *J. Lightwave Technol.* **32**(10), 2028–2034 (2014).
11. H. Zimmermann, B. Steindl, M. Hofbauer, *et al.*, "Integrated fiber optical receiver reducing the gap to the quantum limit," *Sci. Rep.* **7**(1), 2652 (2017).
12. B. Goll, M. Hofbauer, B. Steindl, *et al.*, "A Fully Integrated SPAD-Based CMOS Data-Receiver With a Sensitivity of  $-64$  dBm at 20 Mb/s," *IEEE Solid-State Circuits Lett.* **1**(1), 2–5 (2018).
13. J. Kosman, O. Almer, T. A. Abbas, *et al.*, "A 500Mb/s  $-46.1$  dBm CMOS SPAD Receiver for Laser Diode Visible-Light Communications," in *International Solid-State Circuits Conference (IEEE, 2019)*, pp. 468–470.
14. A. D. Griffiths, J. Herrnsdorf, O. Almer, *et al.*, "High-sensitivity free space optical communications using low size, weight and power hardware," *arXiv* (2019).
15. Z. Ahmed, R. Singh, W. Ali, *et al.*, "A SiPM-Based VLC Receiver for Gigabit Communication Using OOK Modulation," *IEEE Photonics Technol. Lett.* **32**(6), 317–320 (2020).
16. F. Liu, J. Farmer, A. Schreier, *et al.*, "Ultra-sensitive UV solar-blind optical wireless communications with an SiPM," *Opt. Lett.* **48**(20), 5387–5390 (2023).
17. K. Schneider-Hornstein, B. Goll, and H. Zimmermann, "Ultra-Sensitive PIN-Photodiode Receiver," *IEEE Photonics J.* **15**(3), 1–9 (2023).
18. C. Gasser, S. M. Laube, K. Schneider-Hornstein, *et al.*, "Ultra Sensitive PIN-Diode Receiver Utilizing Photocurrent Integration on a Parasitic Capacitance," *IEEE Access* **12**, 118371–118376 (2024).
19. C. Gasser, C. Ribisch, S. M. Laube, *et al.*, "Ultrasensitive Reset-Less Integrator-Based PIN-Diode Receiver With Input Current Control," *IEEE Solid-State Circuits Lett.* **8**, 17–20 (2025).
20. S. M. Laube, C. Gasser, K. Schneider-Hornstein, *et al.*, "Highly-Sensitive Integrating Optical Receiver With Large PIN Photodiode," *IEEE Photonics J.* **16**(6), 1–9 (2024).
21. S. M. Laube, C. Gasser, K. Schneider-Hornstein, *et al.*, "Slow-Slope Reset Scheme for Highly-Sensitive CMOS Integrate-and-Dump Receiver OEIC," *IEEE Access* **13**, 154599–154609 (2025).
22. B. Goll, K. Schneider-Hornstein, and H. Zimmermann, "Ultra-low capacitance spot PIN photodiodes," *IEEE Photonics J.* **15**(2), 1–6 (2023).
23. B. Goll, K. Schneider-Hornstein, and H. Zimmermann, "Dot PIN Photodiodes With a Capacitance Down to  $1.14$  aF/ $\mu\text{m}^2$ ," *IEEE Photonics Technol. Lett.* **35**(6), 301–304 (2023).
24. S. S. Kohnh Poushi, B. Goll, K. Schneider-Hornstein, *et al.*, "CMOS Integrated 32 A/W and 1.6 GHz Avalanche Photodiode Based on Electric Field-Line Crowding," *IEEE Photonics Technol. Lett.* **34**(18), 945–948 (2022).
25. S. S. Kohnh Poushi, C. Gasser, B. Goll, *et al.*, "A Near-Infrared Enhanced Field-Line Crowding Based CMOS-Integrated Avalanche Photodiode," *IEEE Photonics J.* **15**(3), 1–9 (2023).
26. E. Säckinger, "On the Noise Optimum of FET Broadband Transimpedance Amplifiers," *IEEE Trans. Circuits Syst. I* **59**(12), 2881–2889 (2012).
27. K. Stafford, R. Blanchard, and P. Gray, "A completely monolithic sample/hold amplifier using compatible bipolar and silicon-gate FET devices," in *International Solid-State Circuits Conference*, vol. XVII (IEEE, 1974), pp. 190–191.
28. R. E. Suárez, P. R. Gray, and D. A. Hodges, "All-MOS charge-redistribution analog-to-digital conversion techniques. II," *IEEE J. Solid-State Circuits* **10**(6), 379–385 (1975).
29. P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design* (Oxford University Press, 2012), 3rd ed.
30. C. Eichenberger and W. Guggenbühl, "Dummy transistor compensation of analog MOS switches," *IEEE J. Solid-State Circuits* **24**(4), 1143–1146 (1989).
31. M. H. White, D. R. Lampe, F. C. Blaha, *et al.*, "Characterization of surface channel CCD image arrays at low light levels," *IEEE J. Solid-State Circuits* **9**(1), 1–12 (1974).
32. R. J. McIntyre, "Multiplication noise in uniform avalanche diodes," *IEEE Trans. Electron Devices* **ED-13**(1), 164–168 (1966).
33. S. M. Sze, Y. Li, and K. K. Ng, *Physics of Semiconductor Devices* (John Wiley & Sons, Inc., 2021), 4th ed.
34. H. Zimmermann, *Ultra-Sensitive PIN and Avalanche Photodiode Receivers* (IOP Publishing, 2023).