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Cryogenic Si and SiGeSn Schottky-Barrier Field-Effect Transistors

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Abstract

Cryogenic electronics is gaining increasing relevance for applications such as readout and control circuits for quantum qubits and low-temperature data processing, where conventional doped CMOS technologies suffer from fundamental limitations. In particular, dopant freeze-out, band-tail effects and an unfavourable threshold-voltage increase significantly degrade the device performance at cryogenic temperatures. In this thesis, Schottky-barrier field-effect transistors (SBFET) are experimentally investigated with a particular focus on their behaviour at cryogenic temperatures. The primary focus lies on Si-based reconfigurable field-effect transistors (RFETs), which enable both n-type and p-type operation by an electrostatic control of metal-semiconductor junctions. Their electrical characteristics are analyzed between the room temperature and 4.5 K with respect to subthreshold swing, threshold voltage, transconductance and on- and off-state currents. In addition, a similar SiGeSn-based p-SBFET with a channel composition of 33% silicon, 66% germanium, and 0.5% tin and Al_2O_3 as the gate dielectric is being investigated to evaluate the influence of an advanced channel material and gate stack structure on the behavior of cryogenic devices. For the Si RFETs, stable operation is demonstrated for both n-mode and p-mode over the entire investigated temperature range. Upon cooling, a pronounced improvement of the subthreshold swing is observed for both operation modes, reaching values of 24 mV/dec for n-type and 27 mV/dec for p-type operation at 4.5 K. An analysis of the current-dependent subthreshold behaviour reveals distinct transport regimes, with thermionic emission dominating the subthreshold region and tunneling processes becoming increasingly relevant in the on-state at cryogenic temperatures. Despite the favourable subthreshold swing, the threshold voltage of the Si RFETs shifts undesirable with decreasing temperature, moving the on-state away from the desired operating point. The SiGeSn SBFET exhibits a similar improvement of the subthreshold characteristics at cryogenic temperatures, including a strong suppression of the off-state current and steep subthreshold swings of approximately 23 mV/dec at 5 K. In contrast to the Si RFETs, the threshold voltage of the SiGeSn device improves upon cooling, with reductions of up to 25% and 50% depending on the applied drain bias. These results indicate that the cryogenic threshold-voltage is strongly influenced by the channel material system and the gate-stack structure rather than being a property of Schottky-barrier devices. Overall, this thesis demonstrates that Schottky-barrier based transistors provide robust cryogenic operation with strongly improved subthreshold behaviour. At the same time, the results highlight that achieving favourable subthreshold behaviour remains a key challenge for Si-based RFETs, motivating the future work on electrostatic optimization and alternative channel materials for low-power cryogenic electronic systems.

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Kurzfassung

Die Kryoelektronik gewinnt zunehmend an Bedeutung für Anwendungen wie Ausleseschaltungen in der Quanteninformatik sowie für die Datenverarbeitung bei tiefen Temperaturen, bei denen konventionelle dotierte CMOS-Technologien grundlegenden Einschränkungen unterliegen. Insbesondere Dotierstoff-Freeze-out, Bandflankenverbreiterung sowie ein ungünstiges Schwellenspannungsverhalten führen bei kryogenen Temperaturen zu einer deutlichen Verschlechterung der Bauelementeigenschaften. In dieser Arbeit werden Schottky-Barrieren-Feldeffekttransistoren (SBFETs) experimentell untersucht, wobei der Schwerpunkt auf ihrem Verhalten bei kryogenen Temperaturen liegt. Der Hauptfokus liegt auf siliziumbasierten rekonfigurierbaren Feldeffekttransistoren (RFETs), die durch eine elektrostatische Kontrolle der Metall-Halbleiter-Übergänge sowohl einen n- als auch einen p-Betrieb ermöglichen. Deren elektrische Eigenschaften werden im Temperaturbereich zwischen Raumtemperatur und 4.5 K hinsichtlich des Subthreshold-Swings, der Schwellenspannung, der Transkonduktanz sowie der Ein- und Ausschaltströme analysiert. Ergänzend dazu wird ein vergleichbarer SiGeSn-basierter p-SBFET mit einer Kanalzusammensetzung von 33% Silizium, 66% Germanium und 0.5% Zinn sowie Al_2O_3 als Gate-Dielektrikum untersucht, um den Einfluss eines alternativen Kanalmaterials und der Gate-Stack-Struktur auf das kryogene Bauelementverhalten zu bewerten. Für die Si-RFETs wird ein stabiler Betrieb sowohl im n- als auch im p-Modus über den gesamten untersuchten Temperaturbereich nachgewiesen. Beim Abkühlen zeigt sich für beide Betriebsarten eine deutliche Verbesserung des Subthreshold-Swings, wobei bei 4.5 K Werte von 24 mV/dec für den n-Betrieb und 27 mV/dec für den p-Betrieb extrahiert wurden. Die Analyse des stromabhängigen Subthreshold-Verhaltens offenbart unterschiedliche Transportregime, bei denen die thermionische Emission den Subthreshold-Bereich dominiert, während Tunnelprozesse im Einschaltzustand bei kryogenen Temperaturen mehr an Bedeutung gewinnen. Trotz des günstigen Subthreshold-Verhaltens verschiebt sich die Schwellenspannung der Si-RFETs mit abnehmender Temperatur in eine ungünstige Richtung, wodurch sich der Einschaltpunkt vom gewünschten Arbeitspunkt entfernt. Der SiGeSn-basierte SBFET zeigt bei kryogenen Temperaturen eine vergleichbare Verbesserung der Subthreshold-Eigenschaften, einschließlich einer starken Unterdrückung des Ausschaltstroms sowie eines steilen Subthreshold-Swings von etwa 23 mV/dec bei 5 K. Im Gegensatz zu den Si-RFETs verbessert sich die Schwellenspannung des SiGeSn-Bauelements beim Abkühlen, wobei, abhängig von der angelegten Drain-Source-Spannung, Reduktionen von bis zu 25% bzw. 50% beobachtet wurden. Diese Ergebnisse verdeutlichen, dass das kryogene Schwellenspannungsverhalten maßgeblich durch das verwendete Kanalmaterial und die Gate-Stack-Struktur beeinflusst wird und keine Eigenschaft von Schottky-Barrieren-Bauelementen darstellt. Zusammenfassend zeigt diese Arbeit, dass Schottky-Barrieren-basierte Transistoren ein robustes Betriebsverhalten bei kryogenen Temperaturen mit deutlich verbesserten Subthreshold-Eigenschaften aufweisen. Gleichzeitig wird deutlich, dass ein günstiges Schwellenspannungsverhalten weiterhin eine zentrale Herausforderung für Sibasierte RFETs darstellt, was zukünftige Arbeiten zur gezielten elektrostatischen Optimierung sowie zur Untersuchung alternativer Kanalmaterialien für energieeffiziente kryogene Elektronik motiviert.

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Chapter 1

Introduction

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Conventional complementary metal-oxide-semiconductor (CMOS) technology forms the backbone of modern analog and digital electronics at room temperature [1]. However, an increasing number of emerging applications require reliable and energy-efficient circuit operation at cryogenic temperatures. Prominent examples include the control and readout electronics for quantum compuSng systems, cryogenic sensor interfaces and low-temperature data processing platforms. Under such operaSng conditions, classical CMOS devices face fundamental limitations that significantly degrade their performance. At cryogenic temperatures, effects such as dopant freeze-out, band tailing, and a temperature-induced shift of the threshold voltage (V_{th}) strongly impact the electrical behaviour of MOSFETs [2]. Furthermore, the subthreshold swing (STHS) is fundamentally limited by thermal charge carrier dynamics, while the V_{th} typically increases at lower temperatures. These effects result in higher operaSng voltages, reduced drain currents, and overall higher power consumption, which is highly undesirable for cryogenic systems. To address these challenges, cryogenic CMOS (cCMOS) has emerged as a promising approach for low-temperature and beyond-CMOS compuSng [3]. Cooling CMOS devices can, in principle, improve subthreshold behaviour and enable lower supply voltages without losing speed. However, achieving reliable and scalable cryogenic operation with conventional doped MOSFET architectures remains a challenge due to the intrinsic limitations imposed by the dopant-based carrier injection.

In this context, Schottky-barrier field effect transistors (SBFETs) represent an attractive alternative device concept. Unlike conventional MOSFETs, SBFETs are based on charge carrier injection via metal-semiconductor junctions instead of doped source and drain regions. This makes them inherently less sensitive to the dopant freeze-out and allows them to maintain their conductivity even at cryogenic temperatures [4, 5]. Charge transport in SBFETs is controlled by the thermionic emission and tunneling across Schottky-barriers, which fundamentally differs from the behavior of classical MOSFETs, especially in the sub-

threshold region. Building on this concept, reconfigurable field-effect transistors (RFETs) offer additional functionality by enabling both n-type and p-type operation in a single device and enable compact circuit designs which expand functional density and reduce power consumption [6–8]. This is achieved by a electrostatic control of the Schottky-barriers, allowing the dominant charge carrier type to be selected dynamically. RFETs therefore offer an attractive platform for adaptive electronics and enable compact logic circuits with a reduced number of transistors as well as analog circuits with dynamically adjustable properties [9–11]. While SBFETs have already been investigated for cryogenic operation in both n-type and p-type implementations [12–19], experimental investigations of RFETs at cryogenic temperatures are still rare and largely limited to operation at liquid nitrogen temperature (77.5 K) [20].

In addition to the device architecture, the choice of channel material plays a crucial role for the performance of transistors, especially at low temperatures. Among Group IV semiconductors, GeSn and SiGeSn alloys have attracted considerable interest due to their tunable band structure and compatibility with established Si technology. The integration of Sn has been shown to improve key performance indicators such as transconductance and operaSng frequency compared to conventional Ge-based devices [21–23]. Importantly, SiGeSn offers greater flexibility in bandgap design, improved thermal stability, and lower the defect density compared to GeSn, making it particularly attractive for monolithic integration on Si-on-insulator platforms [24, 25]. The contacts for these devices are particularly important for cryogenic applications, as the doped semiconductor contacts for MOSFETs suffer from carrier freeze-out and an exponential increase in resistivity at low temperatures [26], while metallic source and drain contacts can exhibit reduced resistivity upon cooling. Various metal-based contacts for GeSn and SiGeSn devices have been investigated, including metal compounds and silicides [27–29]. However, due to the complex phase formation and stoichiometry control, it remains difficult to achieve reproducible and reliable contacts at the nanoscale. Recent studies have shown that Al-based Schottky contacts can offer a high transparency and stable operation at cryogenic temperatures [30, 31].

The aim of this thesis is to experimentally investigate reconfigurable Schottky-barrier field-effect-transistors under cryogenic operaSng conditions. The focus is on a systematic analysis of the temperature-dependent behavior of Si-based RFETs, with particular attention paid to important device parameters such as threshold voltage, subthreshold swing, on- and off-state currents, the symmetry between n-type and p-type operation and the transconductance. These properties are investigated over a wide temperature range from room temperature (295 K) down to 4.5 K in order to capture the fundamental changes in the behavior of the devices at cryogenic temperatures. In addition to Si-based RFETs, SiGeSn-based SBFETs are being investigated to evaluate the influence of advanced channel materials on the transistor performance. The composition for the alloy is 33% Si, 66% Ge, and 0.5% Sn. The analysis covers operations at room temperature and at cryogenic temperatures, which enables a direct comparison of temperature-related effects in the different material systems. Overall, this thesis seeks to contribute to a deeper understanding

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of the operation of cryogenic RFETs by combining systematic experimental investigation with a detailed discussion of the transistors key parameters. In this way, the presented results serve to assess the potential of Schottky-barrier-based devices as promising building blocks in the future for low-power and energy-efficient cryogenic electronic like quantum compuSng systems.

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Chapter 2

Theory

This chapter provides the theoretical foundations and physical principles relevant to the work presented in this thesis. Since the fabricated devices are evaluated in the context of state-of-the-art cryogenic electronics, the chapter begins with a concise review of the ideal operation of metal-oxide-semiconductor field-effect transistors (MOSFETs) and discusses how their characteristics fundamentally change at cryogenic temperatures. Subsequently, the device concepts employed in this thesis, Schottky-barrier field-effect transistors (SBFETs) and reconfigurable field-effect transistors (RFETs), are introduced, with emphasis on their operation principles and their advantages for low-temperature applications. Finally, the Si-Ge-tin (SiGeSn) material system, which is used for some fabricated devices, is briefly discussed with respect to its electronic properties and its relevance at cryogenic temperatures.

2.1 Cryo-CMOS

2.1.1 Ideal MOSFET

A MOSFET controls the current between source and drain by electrostatically modulating the channel potential barrier through the gate dielectric [32, 33]. A classical planar MOSFET is shown in figure 2.1.(a). To overcome this barrier a certain voltage has to be applied on the gate electrode, the so-called threshold voltage. In the subthreshold regime, the drain current increases exponentially with the height of the channel barrier, leading to the characteristic subthreshold swing (SS or STHS). For an ideal MOSFET, STHS is determined solely by the thermal distribution of carriers and is given by

$$STHS_{ideal} = \frac{k_B T}{q} ln(10) \tag{2.1}$$

and should be as low as possible for switching fast between off- and on-state (at room temperature approximately 60 mV/decade) [18][34]. This relation implies that lowering the temperature should continuously reduce STHS and therefore improve switching steepness, while the suppression of phonon scattering should enhance carrier mobility and increase the on-state current.

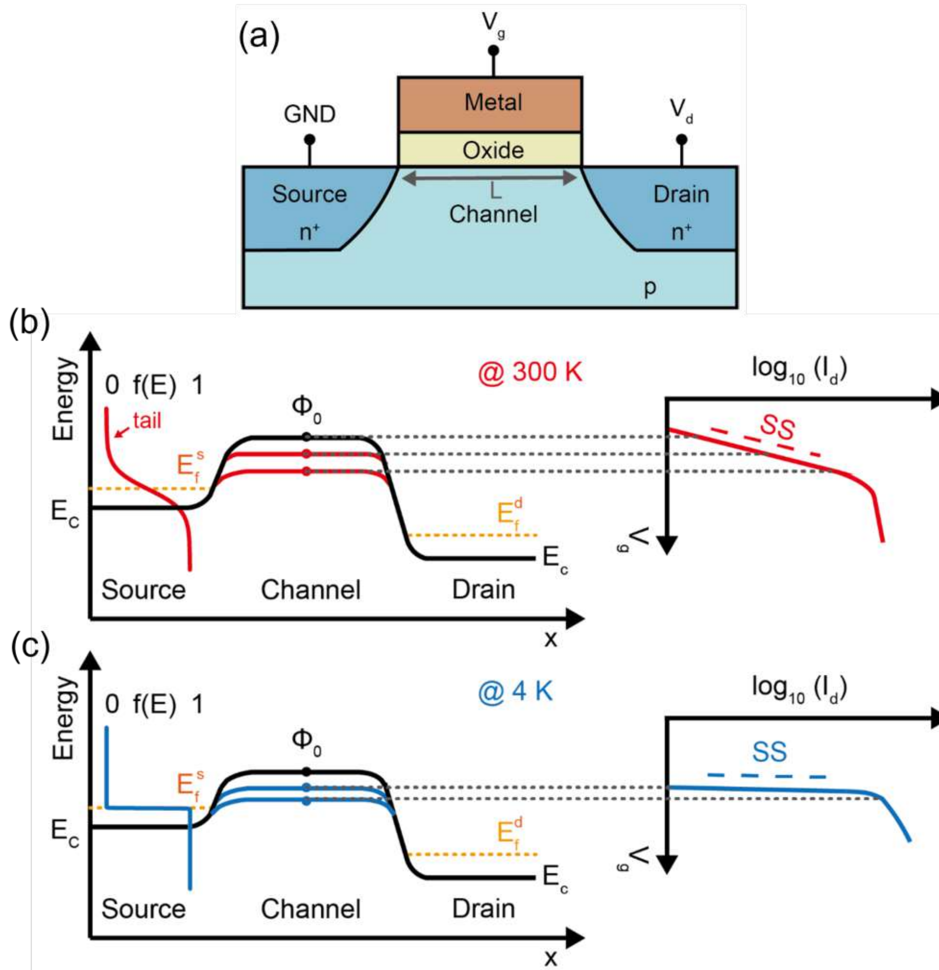

Figure 2.1: *(a) Schematic of a planar MOSFET. Energy band diagram, corresponding subthreshold behavior and related transfer characteristics of an ideal MOSFET at (b) 300 K and at (c) 4 K. At room temperature, the broadened Fermi–Dirac distribution allows carriers above the barrier to contribute to the current, while the sharp distribution at cryogenic temperatures ideally results in a steeper subthreshold swing [35].*

Figure 2.1.(b) and (c) illustrate the ideal behavior at room and cryogenic temperatures. At 300 K (b), thermionic emission over the barrier dominates transport, whereas at 4 K (c), the sharply defined Fermi-Dirac distribution suppresses thermal carriers and lowers the channel barrier, ideally leading to a much steeper STHS, while a positive gate voltage is applied [35]. In addition, the increase in mobility and the resulting increase in on-current should result in reduced leakage (at 4 K STHS_{ideal} is approximately 0.84 mV/decade)

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and thus a lower off-current [36]. This would also mean that a higher on/off ratio of the currents could be expected. In practice, however, real devices increasingly diverge from this ideal behavior as temperatures approach the cryogenic regime.

2.1.2 Operation at cryogenic temperatures

At cryogenic temperatures, operation introduces several phenomena that alter the physical mechanisms of the transistor. This change in behavior includes limitations of the STHS, threshold-voltage shift, interface and band-tail effects, dopant freeze-out, and changes in carrier mobility, which will be discussed in the following. [35].

2.1.2.1 Threshold voltage shift

One of the key deviations from the ideal MOSFET behavior at cryogenic temperatures is the shift in threshold-voltage V_{th}. Fundamental semiconductor parameters change significantly when temperatures drop [37]. In a long-channel MOSFET under equilibrium conditions and neglecting mobile carriers relative to the depletion charge, the threshold voltage can be written as

$$V_{th} = 2\varphi_B + \varphi_{ms} - \frac{Q_{depl}}{C_{ox}} - \frac{Q_{it}}{C_{ox}} \tag{2.2}$$

,

where φ_B is the bulk potential, φ_{ms} the metal-semiconductor work-function difference, Q_{depl} the depletion charge, Q_{it} the interface-trap charge, and C_{ox} the geometrical oxide capacitance [35]. At low temperatures the bulk potential increases and therefore a higher gate voltage is required to reach inversion. The dominant contribution to this threshold-voltage shift is the widening of the semiconductor bandgap and the corresponding exponential reduction in intrinsic carrier concentration. As a result, the Si bandgap increases from 1.12 eV at 300 K to approximately 1.17 eV at 4 K. Also the Fermi-level of the energy (E_F) is shifting due to lowering the thermal excitation [32, 33]. This means that at low temperatures, electrons and holes are hardly thermally excited at all, so the energy distribution of the charge carriers is greatly narrowed. This shifts the Fermi level in n-doped Si closer to the donor level and approaches it in the middle between the conduction band edge and the donor energy. Due to this shift, a stronger band bending is required to satisfy the inversion condition. As a result, the threshold voltage increases significantly at cryogenic temperatures [3]. The temperature dependency of the threshold voltage for NMOS devices is also clearly visible in Figure 2.2, where the extracted V_{th} rises steadily towards cryogenic temperatures due to the growing bulk potential and the widening of the Si bandgap.

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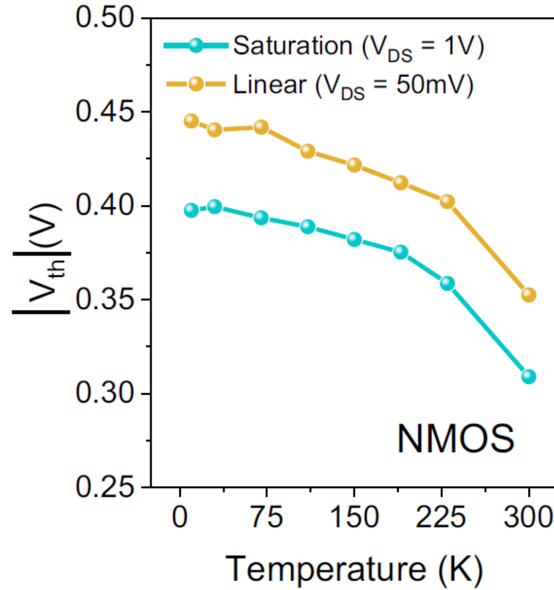

Figure 2.2: *Temperature dependence of the threshold voltage extracted from NMOS transfer characteristics. As temperature decreases, the threshold-voltage increases due to the rise of the bulk potential and the widening of the Si bandgap, both of which require a higher gate voltage to reach inversion [3].*

2.1.2.2 Subthreshold swing

Ideally, STHS decreases with temperature and should approach very small values. Experimental data shows that MOSFETs no longer follow the linear STHS $\propto T$ dependency once a characteristic temperature T^* is reached [18]. Increasing dominance of non-thermal mechanisms such as electron-electron interactions, electron-phonon interactions and especially band-tail states, causes this deviation. At sufficiently low temperatures, STHS saturates at a value significantly higher than the theoretical limit. Band tailings can therefore be understood as the formation of localized electronic states near the conduction or valence band edge, which arise from structural disorder or imperfections in the semiconductor lattice [26]. These states create an exponential tail of state density that extends into the band gap, allowing charge carriers to tunnel into the channel even when the thermal energy is too low to overcome the barrier [33, 38]. Consequently, band-tailing states fundamentally limit the minimum achievable STHS at cryogenic temperatures, as the turn-off current is dominated by tunneling through these localized states rather than by thermionic emission [39]. Figure 2.3 shows how band-tail states dominate the subthreshold region at cryogenic temperatures. At room temperature, thermal broadening blurs out the influence of these localized states, but at 4 K, the Fermi distribution narrows to an almost ideal step function [18, 37]. As a result, thermally excited electrons contribute hardly at all to the off-current. Instead, the off-current is now dominantly determined by the band tail.

In addition to STHS saturation, many cryogenic MOSFETs exhibit inflection phenomena or curvature in the transfer characteristic around the threshold region [35]. This effect orig-

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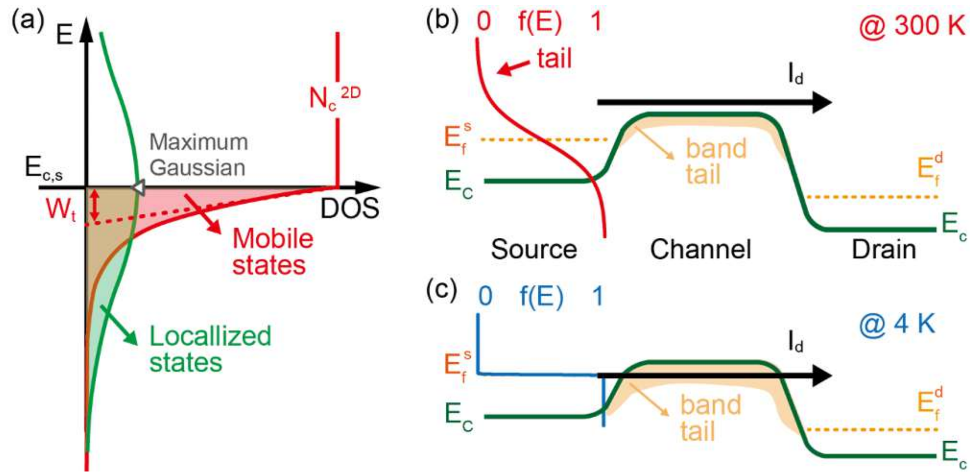

Figure 2.3: *(a) Localized and mobile states contributing to the conduction-band tail. (b) At 300 K the broad Fermi distribution masks band-tail effects. (c) At 4 K, the sharp Fermi distribution enhances the influence of band-tail states, limiting the achievable SS [35].*

inates from localized trap states that introduce an additional interface-trap capacitance, reducing the electrostatic gate control. As a result, the transition from subthreshold to strong inversion becomes less ideal. A more realistic expression for STHS is provided by

$$STHS_{real} = \frac{k_B T}{q} ln(10)(1 + \frac{C_{it}}{Cox} + \frac{C_{depl}}{Cox})[1 + \alpha ln(1 + exp(\frac{T - T^*}{\alpha T^*}))] \tag{2.3}$$

with C_{it} being the capacitance related to interface traps, C_{ox} the geometrical oxide capacitance, C_{depl} for the capacitance for the depletion and α a smoothing parameter. The saturation of the subthreshold swing at low temperatures is illustrated in figure 2.4, where both linear and saturation operation modes deviate from the ideal thermal limit and exhibit a pronounced STHS saturation in NMOS devices.

2.1.2.3 Dopant freeze-out and mobility behavior at low temperatures

Below roughly 50-70 K, dopants are no longer fully ionized, so that the proportion of effective acceptors or donors decreases significantly [18]. This reduces the channel, which requires greater band bending and results in a higher threshold voltage. In nanoscale MOSFETs, quantum confinement increases the needed dopant ionization energy and amplifies this effect. At the same time, freeze-out in the source/drain regions leads to significantly increased series resistances, and the extended space charge zone causes an increase in Drain-Induced Barrier Lowering (DIBL), which should reduce the threshold voltage. Although high doping levels can suppress freeze-out, they reduce mobility due to increased Coulomb and defect scattering, while phonon scattering is strongly suppressed at cryogenic temperatures [3]. Therefore, real MOSFETs at 4 K show only a 10 to 25% improvement in forward currents, rather than the large increases predicted by phonon-limited mobility models.

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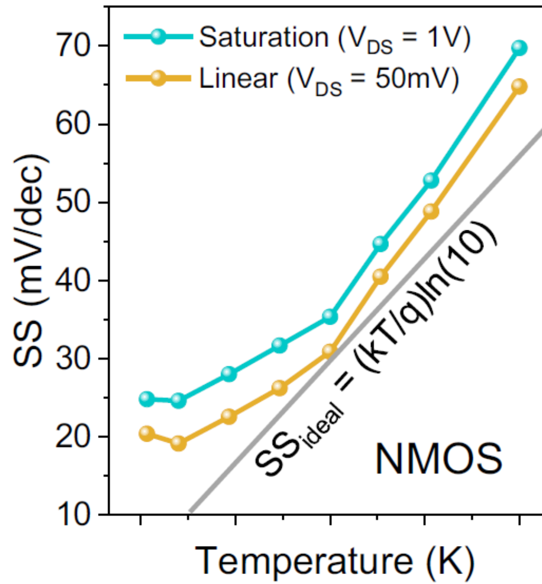

Figure 2.4: *Measured SS of an NMOS transistor in linear and saturation operation regimes as a function of temperature compared to the ideal SS. [3].*

2.2 Reconfigurable field-effect transistors (RFETs)

Reconfigurable field-effect transistors (RFETs) extend the concept of Schottky-barrier FETs by enabling a dynamic selection of the charge-carrier type during operation. Their functionality relies on metal-semiconductor-metal (MSM) heterostructures in which the source and drain contacts form Schottky-barriers to an undoped semiconductor channel. Through the gate voltage, these barriers can be selectively modulated such that either electrons or holes are the dominating carriers for the current. This tunability introduces an additional degree of freedom compared to conventional MOSFETs and satisfies a key element of the "More-than-Moore" design section [40–42]. The following subsections summarize the device principle, charge-carrier injection mechanisms and functional flexibility of RFETs.

2.2.1 Schottky-barrier fundamentals

When a metal is brought into contact with a semiconductor, their Fermi levels align and a potential on this metal-semiconductor interface is formed. This leads to a characteristic band bending inside the semiconductor and creates an energy barrier, which carriers must overcome or tunnel through. The theoretical height of this Schottky-barrier is mainly determined by the metal work function ϕ_m and the electron affinity of the semiconductor ϕ_s, while the interface states and the effects of the image-force can further modify the effective barrier height. This is why often the effective Schottky-barrier height or activation energy is considered for actual devices [33, 43, 44]. For a semiconductor where his Fermi-level E_F is nearer to the conduction band E_C (n-type), this band bends upward

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at the interface, forming a barrier for electrons, like in figure 2.5(a), means ϕ_m is higher than ϕ_s . Otherwise for a p-type semiconductor, an analogous barrier forms in the valence band E_V, which is shown in figure 2.5(b). Such material-systems are also called as pinned, as their Fermi-level is not adjustable with dopants. Particularly for this work, this pinning of the Fermi level is almost in the middle of the band gap, but slightly shifted toward the valence band, for Al-Si interfaces [33]. Carrier transport across such a junction occurs via thermionic emission, thermionic-field emission, or direct tunneling, depending on temperature, barrier shape and the applied bias [45, 46]. In nanoscale devices, the tunneling component becomes increasingly relevant due to the reduced depletion width at the interface. These principles form the physics of Schottky-barrier FETs, where current injection is not controlled by dopant-induced junctions but by electrostatic modulation of the barrier profile.

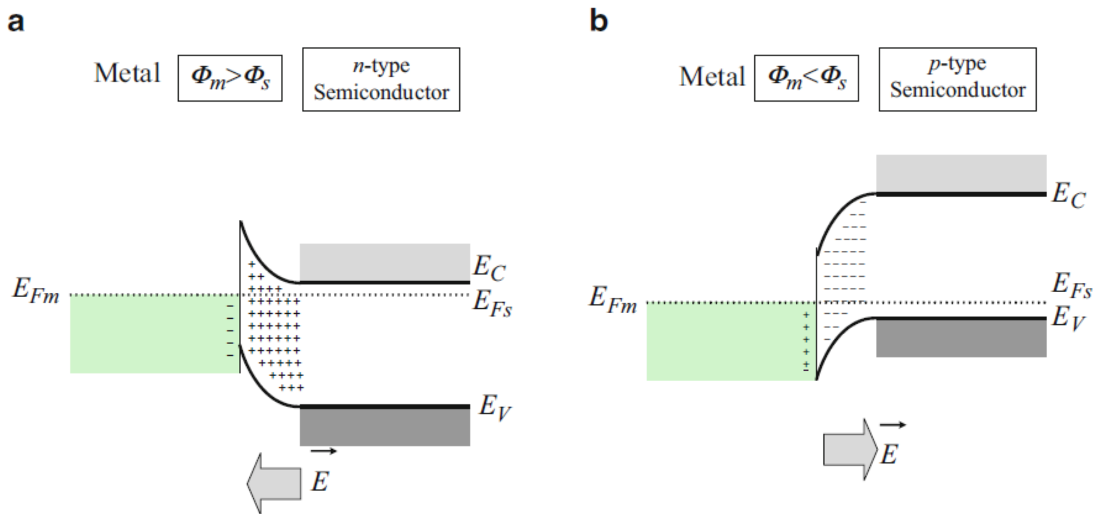

Figure 2.5: *Schottky-barrier at a metal-semiconductor interface for (a) n-type semiconductor and (b) p-type semiconductor [44]*

2.2.2 Device concept

Reconfigurable field-effect transistors are based on a symmetric metal-semiconductor-metal (MSM) structure in which the channel remains intrinsically undoped, and the device polarity is defined purely electrostatically by the applied gate potentials [41]. It should be noted that related concepts using doped device architectures have also been reported, where electrostatic polarity control is combined with conventional doping to improve access resistance and drive current [6, 47], which are not considered in this thesis. In contrast to conventional MOSFETs, where n- and p-type operation is fixed through source/drain doping, RFETs use metallic top gates, so-called program or polarity gates (PG). These are placed above the contact regions of the MSM-structure to modulate the Schottky barriers and thereby select whether electrons or holes are injected into the channel. A separate control gate (CG) located above the channel center then regulates the barrier height along

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the transport path and thus determines the on- and off-state of the device. Between the gate electrodes and the nanostructure lies a oxide or more generally a dielectric similar to a MOSFET.

Depending on the number and arrangement of these gates, several RFET architectures can be realized. Figure 2.6 illustrates the most common top-gate configurations: (a) a single-top-gate (STG) device, (b) a dual-top-gate (DTG) version with one program and one control gate, (c) the widely used triple-top-gate (TTG) structure containing two program gates and one control gate. (d) shows a multi-gate extensions that allow advanced potential shaping and optimization of electrostatic control. All these layouts share the same functional principle: The PGs select the dominant carrier type by locally adjusting the contact barriers, while the CG tunes the channel barrier to control the device state [40]. In this work, only STGs and TTGs are fabricated, measured and their behavior discussed.

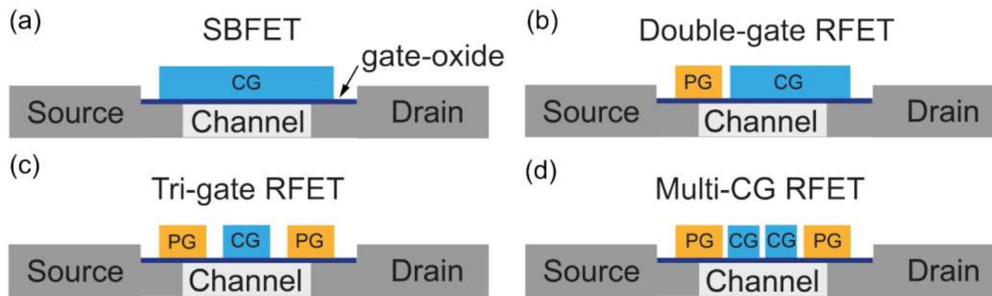

Figure 2.6: *Common top-gate configurations of MSM-based RFETs: (a) a single-top-gate (STG) Schottky-barrier transistor, (b) a dual-top-gate (DTG) structure enabling polarity control at both contacts, (c) a triple-top-gate (TTG) architecture with two polarity gates and one control gate, and (d) generalizations with multiple control gates. The additional gates independently control carrier polarity and channel conductance [48]*

2.2.3 Electrostatic barrier modulation and carrier injection

The operation of RFETs is governed by the electrostatic modulation of the Schottky barriers at the metal-semiconductor interfaces, which determines whether electrons or holes experience the lower injection barrier and therefore defines the transport mode [40]. A negative PG voltage level shifts the local bands upward and reduces the barrier width for holes, leading to p-type operation. Analogous, a positive PG voltage lowers the conduction-band barrier, enabling electron injection and establishing n-type operation. Because the MSM structure is symmetric, the choice of carrier type is fully controlled by the gate potentials rather than by the bias-voltages of source and drain. Once the carrier type is selected, the CG modulates the central channel barrier and thereby controls the current flow. By reducing the barrier height or width, the CG enables the on-state, while increasing the barrier suppresses current to the off-state. The resulting band configurations for p-type and n-type operation are shown in figure 2.7, using a TTG structure, the most important concept for this thesis. For n-type operation, shown on the left-hand side in 2.7(a) and (c), a positive voltage is applied to the PG, which bends the energy barriers towards lower

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energies and facilitates electron transport across the heterostructure. In (a), the CG is biased negatively, leading to the formation of a barrier for electrons and thus representing the off-state. In contrast, for n-type conduction (c), the conduction-band profile forms a continuous transport path with positive CG voltage, allowing electrons to move from source to drain and corresponding to the on-state [40, 42, 49]. For p-type operation 2.7(b), the on-state is shown, where the valence-band profile is raised at the contacts and a negative CG voltage does not introduce an additional barrier for holes, defining a continuous path for the holes. Subfigure (d) represents the off-state, where a positive CG voltage creates a potential barrier within the semiconducting segment, effectively blocking hole transport through the channel. The band-diagram for a STG looks similar, as PGs and CG are connected. Here, the voltage on the gate modulates Schottky-barriers and that in the channel at the same time, which describes ambipolar device behavior.

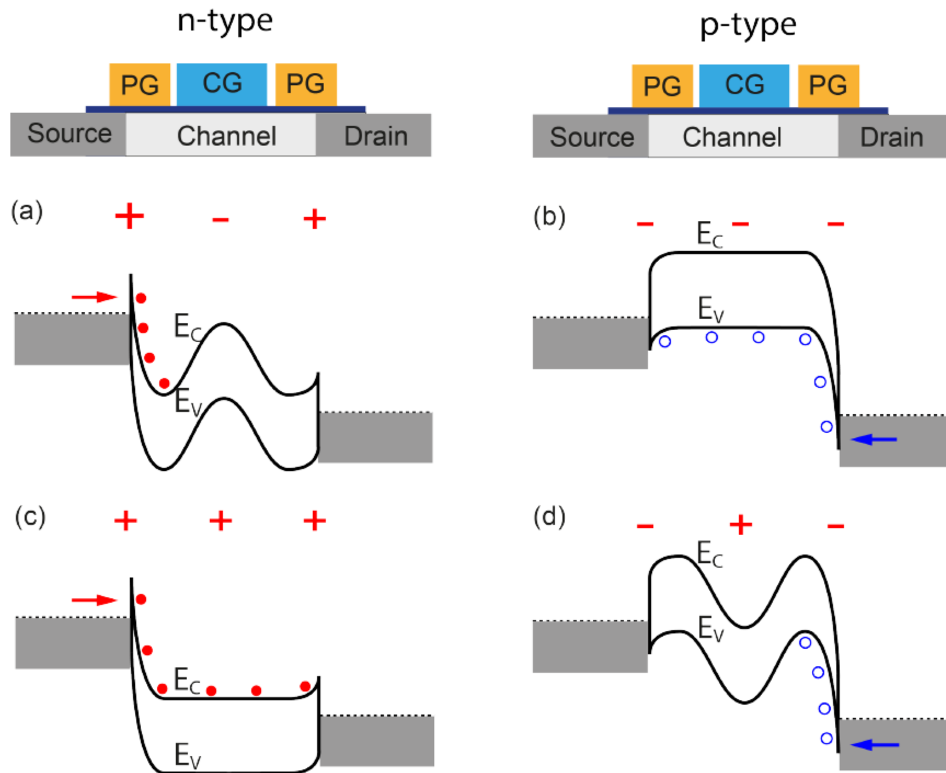

Figure 2.7: *Qualitative band diagrams for the TTG RFET in n-type (a,c) and p-type (b,d) operation. The program gates (PG) define whether the conduction-band or valence-band barrier is lowered at the contacts, while the control gate (CG) modulates the central barrier to establish the on- and off-state. Negative PG voltages enable hole injection (p-type), whereas positive PG voltages promote electron injection (n-type) [48].*

The carrier transport in RFETs depends strongly on the effective Schottky-barrier shape at the metal-semiconductor regions and the electrostatic potential along the channel. There are different transport regimes, which may dominate the device behavior, depending on the applied gate voltages and the barrier width [45]. At large barrier heights, thermionic

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emission (TE) is the primary contribution. For intermediate barrier widths, thermionic-field emission (TFE) becomes relevant, while in nanoscale devices with sharply modulated barriers, direct tunneling (field emission, FE) dominates the on-state current. The off-state current is typically governed by thermionic emission, whereas the on-state is dominated by tunneling in modern RFET geometries [46].

2.2.4 Advantages for cryogenic and doping-free technologies

RFETs offer several advantages compared to conventional MOSFETs, especially in nanoscale and cryogenic operation. First, due to their MSM structure, RFETs do not require source or drain doping. Since dopant activation and freeze-out represent major limitations for cryogenic MOSFET operation, the doping-free architecture eliminates these issues entirely [40]. The electrostatic control of the Schottky barriers replaces the role of dopants, enabling stable carrier injection even at deep-cryogenic temperatures. Second, RFETs reduce circuit complexity thanks to their dual-mode functionality, allowing lower device counts in digital logic, potentially reduced static power consumption, and compact implementations of polymorphic or adaptive circuits [40]. These features make RFETs promising candidates for future cryogenic electronic systems and beyond-CMOS computing architectures.

2.3 SiGeSn as transistor channel material

SiGeSn is a ternary group-IV alloy that enables continuous band-structure engineering by adjusting the relative Si, Ge, and Sn content. The hyperdoping with Sn introduces a strong bandgap bowing, which results in a substantial reduction of the energy gap and a observed downward shift of the Γ-valley relative to the indirect minimum [24, 50]. This behaviour allows SiGeSn compositions to transition from an indirect toward a quasi-direct or direct bandgap, depending on the Sn concentration. The associated lowering of the effective mass of the electrons enhances carrier transport, which is advantageous for both transistor operation and optoelectronic applications. High-quality SiGeSn layers can be grown using chemical vapour deposition (CVD), enabling controlled Sn integration beyond the solid-solubility limit of Si and Ge. Experimental studies demonstrate that such layers exhibit low effective masses, high carrier mobilities and reduced thermal conductivity. This properties makes the material attractive for electronic, photonic and thermoelectric devices [51, 52]. The reduced bandgap also lowers the required threshold voltage for carrier injection, which is beneficial for cryogenic device concepts where limited carrier ionisation, explained in 2.1.2.3 typically restricts the performance of devices with Si or SiGe channels. Strain plays an important role in determining the resulting band structure. Due to the lattice mismatch between the constituent elements, tensile strain can further reduce the bandgap and stabilise the Γ-valley. These alloy disorder effects and Sn-induced potential fluctuations generate band-tail states near the band edges [52]. Such band-tail states strongly affect the subthreshold behaviour and become particularly relevant for cryogenic MOSFETs, where weak-inversion transport dominates [32, 37].

Overall, SiGeSn offers a highly flexible group-IV material platform with a tunable bandgap,

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reduced effective mass, and excellent compatibility with CMOS processing. In addition, the incorporation of Sn leads to enhanced charge-carrier mobilities and increased carrier concentrations compared to Si and Ge, enabling higher drive currents at reduced bias voltages [21, 22]. These properties are particularly advantageous for low-power and cryogenic electronic devices, where efficient current injection and operation at low supply voltages are essential [30]. Consequently, SiGeSn represents an attractive material system for cryogenic electronics, tunnel transistors, and optoelectronic integration.

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Chapter 3

Experimental Techniques

As this thesis focuses on the electrical characterization of Si based RFETs and SiGeSn SBFETs at room temperature and cryogenic temperatures, this chapter discusses the electrical setups and measurement routines. However, first, there is a brief description of how these two different devices were obtained, although their process flow is very similar.

3.1 Device Fabrication

3.1.1 Si-based RFET

The starting point of the fabrication of Si based RFETs used in this work is a SOI wafer. It consists of a 100 nm buried oxide (BOX) made of SiO_2 on a undoped Si bulk substrate and a instrinsic 20 nm Si device layer (DL) on top of it, shown in figure 3.1(a).

3.1.1.1 Si nanosheets structuring

The upper epitaxial Si layer is now obtained into an RFET structure using a top-down process flow, including lithography, etching and sputtering. First, this layer forms a native SiO_2, which is not wanted for further processing. To remove this oxide, a standard surface cleaning process and a buffered hydrofluidic acid (BHF) dip is used. Then an laser-lithography process step is used to pattern nanosheets from this layer, with a resolution of nearly 100 nm [53]. For that, the sample is spin-coated with a photosensitive resist via a spinner followed by a bake-out on a heat plate, to reach homogenous thickness. After the resist has been developed and the exposed areas have been removed with a solvent, the Si DL is etched using SF_6/O_2-based reactive-ion-etching (RIE). In reactive ion etching, a plasma is generated in a vacuum by two electrodes which accelerates ions onto the sample, causing anisotropic physical etching but also uses the reactive ions and neutral radicals present in the plasma for chemical removal [53]. As can be seen in the figure 3.1(b), the

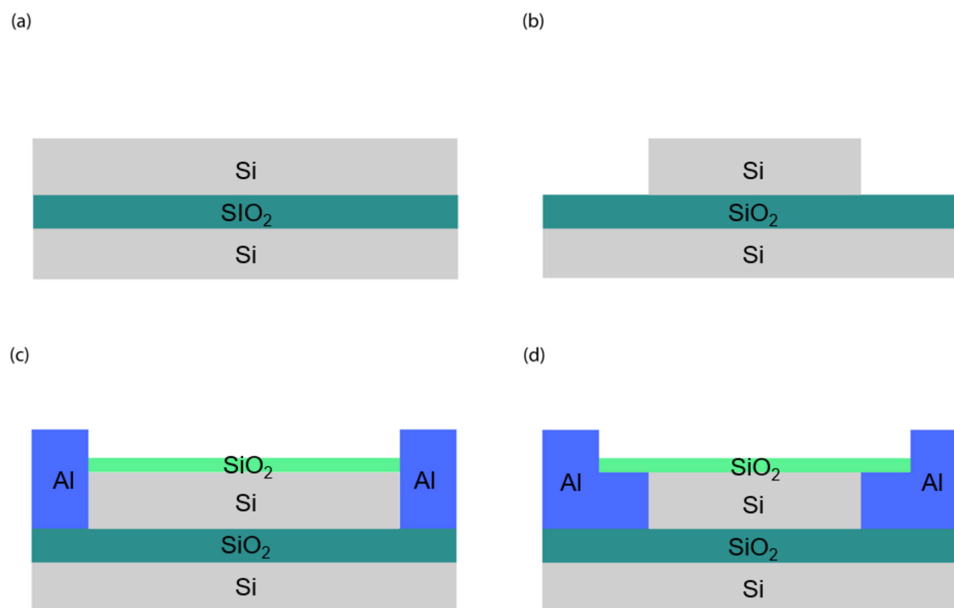

Figure 3.1: *Cross-sectional schematic of the initial fabrication steps for the RFET nanosheet structures. (a) Starting SOI wafer stack with a thin Si layer on top of the buried oxide (BOX). (b) Definition of the Si nanosheet by lithography and anisotropic etching. (c) Opening of the source/drain contact regions and deposition of Al to form the metal contacts. (d) Finalized Al-Si interface after annealing, forming the basis of the MSM heterostructure before top-gate processing*

nanosheets are now formed on the oxide with nominal sheet lengths of 10 μm and widths in the sub-μm range.

As a short note, newer samples were structured with electron-beam lithography (EBL), which has better resolution in the nanometer range. This process takes place in a vacuum chamber and it is important to ensure that the chip is electrically connected to the substrate holder to prevent electrostatic charging. Also a negative photo-resist is used, means the exposed areas remain after developing and rinsing.

3.1.1.2 Oxidation and source/drain structuring

After structuring the Si nanosheets, the next process step is the gate-dielectric formation. The gate-dielectric consists of a native oxide and is formed by dry thermal oxidation of the Si surface at a temperature of 1174 K in order to form a thermal 6 nm SiO_2, indicated in figure 3.1(c) as light green. For this process, first oxygen and later nitrogen were supplied for 3 minutes each. Further, Si oxide can subsequently be combined with high-k dielectrics, like HfO_2 or Al_2O_3. This additional oxide can be grown via atomic-layer-depostion (ALD). For this process TEMAHf and H2O are used as precursor gases, besides N2 as carrier gas at a reactor temperature of 524K.

Next, the source and drain contacts were defined in a further laser-lithography step like for

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the nanosheets. As the preferred structure is a MSM-stack, the oxide has to be removed on both ends of the nanosheet before the Al-depostion. Here, wet chemical etching via a BHF dip is a popular method because only the oxide is etched and not the Si, in contrast to physical etching, where everything is etched equally. However, the etching rate for HfO_2 with BHF is too slow, meanings physical etching is needed for this high-k material. This process is performed with argon-based reverse sputtering. Now the deposition of a 125 nm high Al layer was accomplished via sputtering for the source/drain pads. Sputtering is a process in which ions are fired at a target material in a vacuum. This impact causes individual atoms to detach from the material and fly through the vacuum to the substrate, where they ultimately form a layer. The ions are generated by a plasma, and a magnetron is often placed behind the target to increase the number of noble gas ions and thus also the sputtering rate [54, 55]. Using a lift-off process, which dissolves the resist under the deposited metal, the not desirable material can be removed. The result for this step is also shown in figure 3.1(c) as the blue colour indicates the Al pads.

3.1.1.3 Metal-semiconductor-metal heterostructure formation

This section describes what is probably the most critical and important step in the fabrication of cryogenic RFETs in order to form a reproducible and reliable abrupt metal-semiconductor-metal junction. Through a thermally induced metal-semiconductor exchange process, the Si/Ge/Sn diffuses into the Al source/drain pads, causing the metal to migrate into the nanostructure in a monolithic crystalline phase [56]. This annealing process is performed at 774 K in a N_2-H_2 atmosphere rapid thermal annealing (RTA) [57]. Additionally, several annealing steps are processed with various duration to reach a sufficient small semiconducting channel segment, as preferred lengths are between 500 nm and 3 μm. A sharp abrupt transition is formed between the Si and the Al without any intermetallic compounds to ensure low contact resistance and a little or ideally no interface traps, indicated in figure 3.1(d) [56]. Through an optical microscope, the achieved semiconductor lengths can be observed and captured. Important to mention is that the Al does not diffuse into the gate-dielectric.

3.1.1.4 Structuring of the top-gates

The next step in the fabrication specifies the functionality of the devices, as the number of top gates implements this behavior. As already mentioned, the devices in this thesis are either single-top-gate or triple-top-gate, with two PGs and one CG. As described in section 2.2.3, the role of the gates is to control the Schottky-barriers and that of the channel, to determine the carrier-injection mode and the current strength through the heterostructure. The PGs must therefore lie precisely above the metal-semiconductor interfaces in order to modulate the Schottky barriers, which is why the Al-Si-Al heterostructure is geometrically measured using optical microscopes. For STG devices, the top gate was defined in a further step using laser lithography, and the desired material combination (Ti-Al, Ti-Au) for the electrode was deposited using sputtering or vapor deposition, as used for the source/drain-pads. Laser lithography is no longer sufficient for the top gates of TTG devices, as the

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gaps between the individual gates are only 375 nm. To achieve these dimensions, top gates are obtained using EBL and sputtered like STGs. The gate material combination is in total 10 nm of titanium and either 177 nm of Au or 105 nm of Al. The Ti determines the associated work function, whereby the Au/Al prevent it from oxidation. Similar to the source/drain-pads structuring, the last process step for the top gates is a lift-off, which dissolves the resist under the deposited metal, the not desirable material can be removed. A final TTG-RFET-structure is shown in figure 3.2 as cross-section in (a) and in (b) as top view, where the PGs are connected together to one pad. This structure makes it easy to use, as only one electrical signal needs to be applied for the two PGs, shown later in figure 3.4.

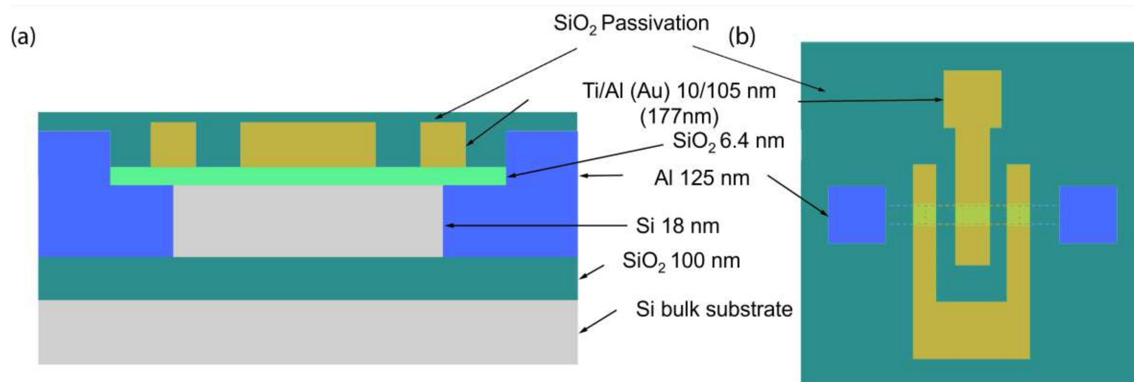

Figure 3.2: *(a) Cross-sectional view of the TTG-RFET, highlighting the individual layers along with the top gates. (b) The top view of the corresponding RFET structure, note that the gates are covered by the passivation layer, but for illustration purposes this is not shown here (based on [58]).*

3.1.1.5 Passivation layer

The RFET is already fully applicable for measurements at room temperature and without a vacuum, which is necessary during cooling to protect the measurement environment from freezing. The next and final step in the fabrication will be implemented because the devices, especially the p-mode, have problems at cryogenic temperatures and under vacuum, illustrated at section 4.1.3.1 in the results chapter. Under these conditions, ungated regions of the device are particularly sensitive to surface-related effects. Surface charge traps, fixed oxide charges, and interfacial states can lead to a gradual depletion of the semiconductor surface, resulting in additional electrostatic barriers and undesirable threshold voltage shifts [59, 60]. The deposition of a passivation layer is therefore essential to stabilize the electrostatic environment of the ungated areas, as suitable passivation materials can suppress surface charge fluctuations and reduce charge trapping, resulting in improved threshold voltage stability and more reproducible device behavior under these conditions [59, 61]. To counteract these effects in the present devices, a SiO_2 passivation layer is deposited by plasma-enhanced chemical vapor deposition (PECVD) at 573 K. After that, another laser lithography step is required for the source/drain contact pads and the gates, as these are freed from the overlying SiO_2 via RIE. This passivation or capping layer has a thickness of 200 nm and is also indicated in figure 3.2, although it

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should be noted that the gates in top view (b) are also covered by this layer, but for illustrative purposes this is not shown here. The temperature of the PECVD process can cause metals and semiconductors to diffuse again, which is a problem and is described in more detail in section 4.1.3.1 in the results chapter and illustrated with measurements.

3.1.2 SiGeSn-transistor fabrication

The fabrication of the SiGeSn p-channel transistor with multi-gate architecture is very similar to the already described for Si-based RFET, which is why the following description is short and highlights the key differences. The starting point here is an SOI wafer with a 20 nm Si DL and a thin, nominally intrinsic $Si_{0.33}Ge_{0.665}Sn_{0.005}$ layer grown via ultra-low temperature molecular beam epitaxy (MBE) [62]. In addition, an 8 nm thick Si buffer layer is grown by MBE to ensure a suitable interface to the metal prior to the SiGeSn growth. After that, a 3 nm thick Si passivation layer is applied, which also serves as the interface layer for the gate dielectric. As described in section 3.1.1.1, the nanosheets are produced using laser lithography and RIE and have a width of approximately 180 nm and a length of 10 μm. A 11.8 nm thick layer of Al_2O_3 is used as the dielectric in these devices and is deposited by ALD. It is important to note that this can slightly oxidize the Si capping layer, creating an interface of SiO_2/Al_2O_3, which can influence the results as a voltage shift due to negative fixed oxide traps [61], more on this in chapter 4. A picture by a transmission electron microscope (TEM) of the gate-stack is shown in figure 3.3(b). Furthermore, the source/drain pads are made of Al as in section 3.1.1.2, and the annealing steps via RTA from section 3.1.1.3 are applied at a temperature of 773 K to create monolithic and single-crystalline Al contacts by diffusion. Something interesting also happens during this thermally-induced solid-state exchange reaction, as a Si interlayer forms between Al and SiGeSn. This thin layer affects the band diagram and the interfaces and originates from the different diffusion speeds of Si and Ge [63]. Now a so-called multi-heterojuntion is formed with a structure of Al-Si-SiGeSn, indicated in figure 3.3(a). The channel lengths produced in this way are in the range of approximately 2 μm. As a final step, the top gates are now fabricated again using EBL, sputtering, and lift-off as described in section 3.1.1.4. Here, the structure of the top gates is the same as in a TTG, but it cannot be referred to as an RFET, as n-mode is only possible to a limited extent with this material system. Therefore, in all of the following, we will refer to the gates of the device via CG, as with RFETs, and to a junction gate (JG). Both consist of 10 nm Ti as pinning metal and 100 nm Au as oxidation protection and bonding material. Figure 3.3(c) illustrates the process flow.

3.2 Electrical characterisation

3.2.1 Lakeshore PS-100

The electrical characterisation was done by a two-part measurement setup, the cryogenic needle probe station Lakeshore PS-100 and the connected a Keithley B1500A analyzer. This probing station has 5 needles, 4 so-called source-measure-units (SMU) and one for

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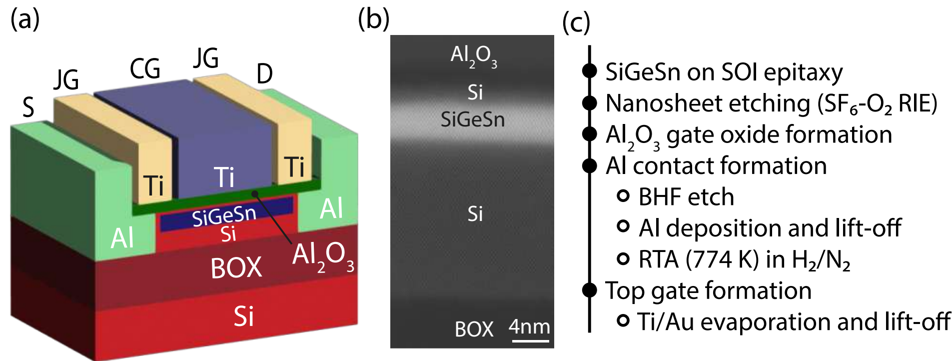

Figure 3.3: *(a) Cross-section of the SiGeSn-transistor device. (b) TEM-picture of the channel-oxide stack. (c) Short overview of the device fabrication [64].*

ground signal, which are needed to measure the devices for this thesis. These SMUs are used to apply certain voltages and also measure the resulting currents. The resolution limit of this setup is at 40 fA. As already mentioned, the transistors in this thesis are STGs and TTGs where 3 and 4 SMUs are needed. The following figure 3.4 demonstrates the electrical connections for these two structures. The choice of applying drain and source is arbitrary due to symmetry of the devices. The voltage on this two pads can be set independent from each other and results in the so called bias-voltage V_{DS}. This voltage drop along the nanosheet has a standarized direction, as the name says, from drain to source. Moreover, as the difference between drain current I_D and source current I_S is negligible (but shows other sign), the current I_{DS} through the channel will be referred as I_D. Gate currents I_{TG}, I_{PG} and I_{CG} are designated as leakage currents and are ideally zero or negligible small depending on the dielectric used. If this is not the case, the leakage current is a sign for a damaged device or a poorly set up of the measurement. It is similar to a normal MOSFET where the leakage current results in the difference between I_D and I_S or the current measured by the related SMU, which is driving the corresponding gate. The range of these reach from fA up to nA, which already represents a large risk to destroy the nano-structure and depends on the current strength through the channel. In most cases destruction happens in the gate dielectric or between S/D-pads and the gates. For limiting not wanted influences like charging effects, the whole sample is placed on a copper plate with silver paint and connected to the ground of the analyzer via the ground needle. The Lakeshore has a built-in heating chuck and a corresponding temperature controller for temperature depending measurements. For cryogenic operations a certain cooling is required and so these measurements were performed in a continuous flow of liquid nitrogen (down to 77.5 K) or liquid helium (down to 4.2 K). To prevent damaging the devices and the whole setup by freezing, the measurement chamber of the Lakeshore was evacuated at a pressure of approximately $2.5 \cdot 10^{-5}$ mbar at room temperature. To monitor the temperature of the radiation shield, the lid of the vacuum chamber, and the sample the temperature controller was used. To ensure correct measurement, the sample, needles and chamber must be at the same temperature level. As the needles do not have a thermal sensor, they were placed on a substrate for approximately 30 minutes. This

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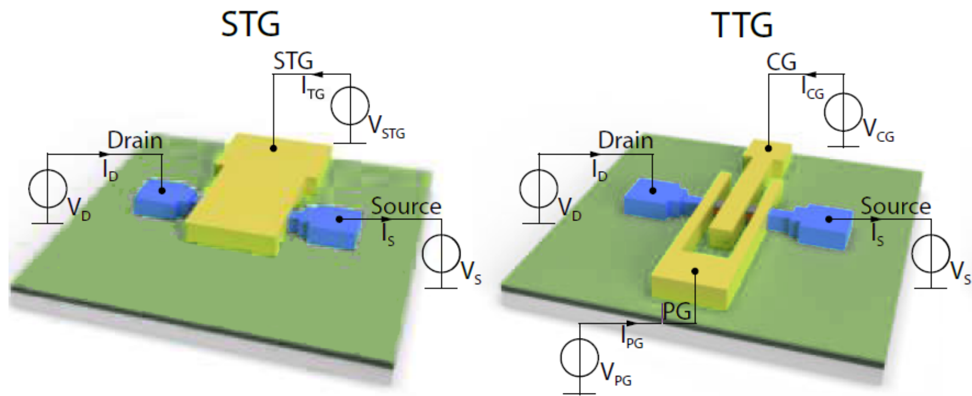

Figure 3.4: *Electrical measurement setup for STG- and TTG- devices and the corresponding designations (based on [58].*

is an important step cause thermal energy caused by temperature differences can falsify results or even damage the device. That means that cooling down needles on the S/D- or gate-pads is harmful for the nanostructure. In addition, the temperature of the sample must be constant before the needles are applied, as variations can cause mechanical stress that can damage the needles and the sample.

3.2.2 Transfer characteristic

The transfer characteristic describes the device response for a certain fixed bias-voltage V_{DS} while sweeping the voltage level at the gate. It represents the resulting drain current I_D, typically its absolute value, as function of the gate voltage. From these curves, key parameters such as the on-state current I_{on} and off-state current I_{off}, the threshold voltage V_{th}, and the subthreshold swing $STHS$ can be extracted for both p-type and n-type operation. For the STG configuration shown in the left of figure 3.4, the drain and source voltages are kept constant while the STG voltage is swept. Due to the Schottky-barrier FET nature of the device, as discussed in Section 2.2.3, an ambipolar characteristic is expected, means current flows through the nanostructure for both positive and negative STG voltages. Consequently the gate electrode modulates both Schottky-barriers of the metal-semiconductor interfaces on drain and source side. For a TTG device (right-side of 3.4) the constant voltage level on the two PGs above the metal-semiconductor interfaces are suppressing the intrinsic ambipolar behavior, while the CG is swept. The charge carrier injection depends on the electrostatically modulation through the PGs, as we get n-mode for positive and p-mode for negative voltage, like in figure 2.7. As we have two modes, two separated transfer curves are obtained to observe the device behavior.

In most measurements drain is biased at +0.5 V and the source at -0.5V, resulting in a drain-source voltage V_{DS} of 1 V. Since the same electrical voltage, in absolute terms, is applied to both S/D pads, this setup is referred to as symmetrical bias in the following. To investigate potential asymmetries in the nanostructure, non-symmetric drain and source

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voltages can also be applied; however, this is not done in this thesis. It is also advisable to reduce the V_{DS} in order to observe transfer characteristics at different bias voltages, while higher values can damage the device. The gate-voltage range is chosen such that reliable switching behavior is achieved without harming the device. For p-type operation, the PG is set to its maximum negative voltage, and the CG (or STG) is swept from this negative limit to the maximum positive value; for n-type operation, the procedure is mirrored. A single sweep corresponds to a transition from on-state to off-state (or vice versa). A double sweep consists of two consecutive single sweeps: first on to off, then immediately off to on, enabling the assessment of hysteresis. The corresponding transfer characteristics in this thesis are presented 4.

3.2.3 Output characteristic

The output characteristic describes the behavior of the device when the drain-source voltage V_{DS} is swept while the resulting drain current I_D is recorded for a fixed top-gate voltage. For this current curve, the voltage on the CG or STG acts as an input parameter, while the resulting current response as a function V_{DS} and represents the output behavior of the device [33]. For practical reasons, the current response for multiple gate-voltages is measured one after another resulting in a so-called output-array. Usually, defined steps like 0.5 V from the minimum to the maximum gate-voltages are used, while the drain-source bias is swept between a range-minimum and maximum, similar to the V_{DS} of the transfer characteristic. This curves together represents the output characteristic of the device and provides insight into the saturation behavior, output resistance, and current-driving capability.

In STG devices, the relevant gate voltage is given by V_{STG}, while for TTG structures the control-gate voltage V_{CG} defines the output conditions. Since TTG devices allow electronic switching between p-type and n-type operation via the program gates (PGs), two distinct output characteristics are needed (one for each operation). Consequently, TTG RFETs exhibit two output-arrays, in contrast to STG SBFETs, which show only a single output family. The resulting output characteristics for the fabricated devices are presented in 4.

3.2.4 PG sweep characteristic

In addition to the transfer and output characteristics, which represent standard measurement procedures for field-effect transistors, the PG sweep characteristic highlights a unique aspect of RFETs. As they have the ability to switch dynamically between electron and hole conduction, this feature requires dedicated analysis about the mechanisms, which is not present in conventional transistors. This sweep is interesting, as the resulting information provides insight about this dynamically switching behavior, or in other words, at which program-gate voltage V_{PG} a n-type or p-type operation dominates the current. While for this measurement one or more PGs are needed, this is obviously not applicable for STG devices.

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The PG sweep characteristic is obtained by measuring a sequence of transfer curves, while the voltage level at PG is various. Similar to the transfer characteristic, this voltage is kept constant while the one for the control gate is swept across its full range. With predefined steps for the PG, like for the CG in the output measurements, a whole set of curves are the result. Consequently, as a TTG device can switch between n-mode and p-mode, two measurement runs are needed to observe the behavior of the device, cause of the direction from off to on state. As before, the drain-source bias V_{DS} is applied symmetrically such that $V_D = -V_S$. The captured sweeps for TTGs fabricated for this thesis are shown in chapter 4.

3.2.5 Evaluation of important parameters

As already discussed, several characteristic parameters of the devices can be obtained from the measured curves, particularly from the transfer characteristics. This subsection introduces the set of parameters derived from these transfer curves, which will later be presented and discussed for the fabricated samples. Furthermore, the analysis focuses exclusively on TTG structures, as they provide all necessary data for determining the targeted characteristics. Parameters like the on/on ratio of the two on-currents for RFETs displays the symmetry between the two carrier operation modes, while the ratio between on-state and off-state current directly influences the static power consumption. The key parameters for this thesis are the threshold voltage V_{th} and the subthreshold swing STHS, which will be addressed in the following subsections. They are also relevant when evaluating the performance of the device, as they give information about the switching speed and the electrical voltage that a device needs to switch [42, 65].To evaluate all these parameters, a Python script is used.

3.2.5.1 Threshold voltage evaluation

The threshold voltage V_{th} is not defined by a single universal method, and several extraction techniques exist in the literature [59]. In this thesis, a combined approach based on the linear-extrapolation method and the transconductance method is applied, illustrated in figure 3.5(a). First, the transconductance is obtained by $g_m = dI_D/dV_{CG}$. Then a vertical line is drawn from the maximum of g_m to the corresponding point on the transfer curve. At this intersection, a linear tangent is fitted to the curve, and V_{th} is defined as the point where this tangent crosses the x-axis (V_{CG}-axis). As shown in the subfigure, both the transfer curve and the transconductance, which is slightly smoothed to easier find the maximum, are plotted linearly. Since manual extraction is inherently subjective and not always reproducible, the automated python routine is preferred, as it provides identical evaluation conditions at higher resolution. The resulting values in this work are presented and discussed in chapter 4.

3.2.5.2 Subthreshold swing evaluation

The STHS for both p-type and n-type operation is obtained from the corresponding transfer characteristics. Similar to the threshold-voltage extraction, the logarithmic transfer

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curve with respect to the applied V_{CG} is differentiated, and the maximum value of this derivative within the transition region between the on- and off-state is taken as the STHS. Figure 3.5(b) illustrates the extraction procedure. As shown there, the slope of the absolute drain current is plotted on a logarithmic scale between the on- and off-state corresponds to the reciprocal of the STHS. To capture the steepest part of the transfer curve accurately, the automated python routine is used instead of relying on manual, graph-based evaluation. The results for the devices fabricated and observed in this thesis are presented and discussed in chapter 4.

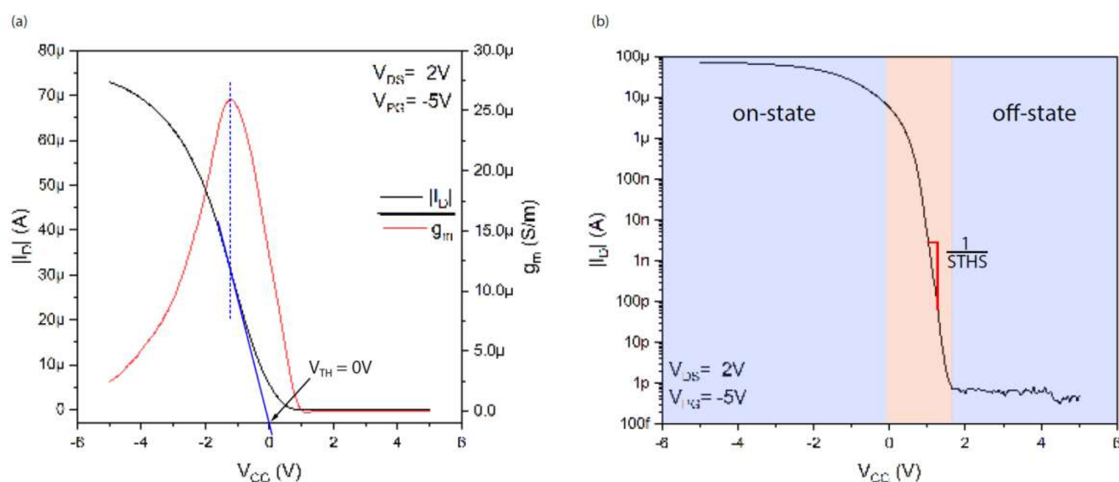

Figure 3.5: *Determination of the corresponding (a) threshold voltage V_{th} with the described transconductance method, and (b) the sub-threshold swing STHS [58].*

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Chapter 4

Results and Discussion

In this chapter, the behavior of the fabricated devices are observed in accordance to the already described theoretically aspects chapter 2 and the experimental methods in chapter 3. First, Si-based STGs are measured and discussed for a certain sample at roomtemperature. Later, Si-based RFET TTG-structures are measured and their difficulties and behavior in cryogenic environments are recorded. Finally, a SiGeSn p-channel transistor is presented, their properties analyzed, and compared with the results obtained previously.

4.1 Si based devices

This section describes and discusses two different samples, both of which, as already mentioned in chapter 3, are based on a SOI wafer. Table 4.1 shows the final gate stack for both samples.

layer	**SOI29**	**SOI41**
gate material	Ti 10.9 nm + Al 105 nm (or Au 177 nm)	10 nm + Au 130 nm
dielectric	SiO_2 6.4 nm	SiO_2 2.8 nm + HfO_2 5.3 nm (EOT = 3.8 nm)
semiconductor	Si 18 nm	Si 20 nm
BOX (SiO_2)	100 nm	100 nm
substrate	Si	Si

Table 4.1: *Gate stacks for the observed samples SOI29 and SOI41*

The titanium is used as the work function material and is covered with Al/Au as an oxidation protective and bonding pad. The material for source/drain pads is for both samples Al and formed to monolithic single-crystalline Al-Si heterostructures by annealing [57].

4.1.1 Si-based single top-gates at room temperature

The nanosheets of sample SOI41 are fabricated using EBL, and its mask has different sizes for the width of the channels in order to observe their influence on the behavior of the devices. Some pictures for these geomertrical differences are shown in figure 4.1 captured by scanning electron microscope. Here some varying in the fabrication is observed as the designated geometrical widths in the mask are (a) 250 μm, (b) 175 μm, (c) 150 μm and (d) 125 μm. A picture for a Au top-gate STG device is captured by optical microscope

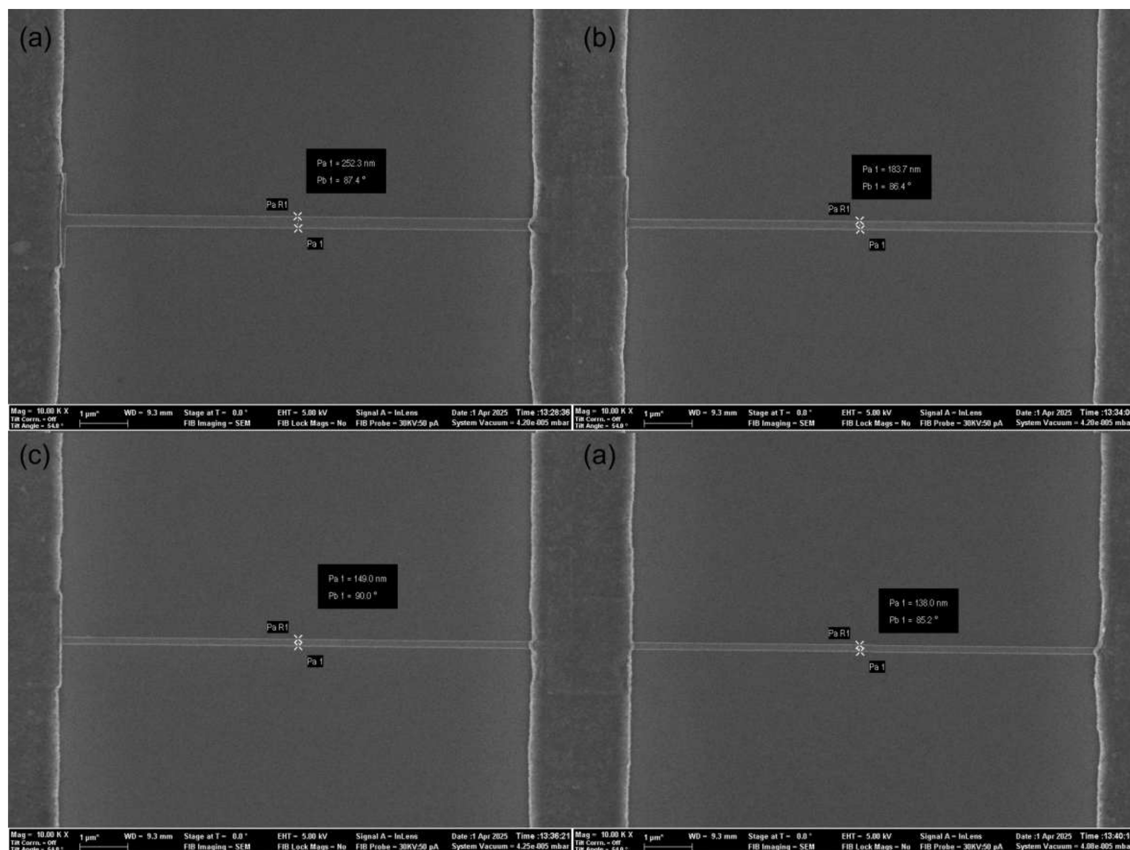

Figure 4.1: *Geometrical measurements for nanosheet widths for different mask properties by SEM.*

and shown in figure 4.2.

4.1.1.1 Transfer characteristics - STG

The transfer curves for these STG devices of sample SOI41 are discussed and illustrated in the following. The measurement environment and the characteristics themselves have already been introduced in the experimental chapter, in section 3.2.2. An ambipolar curve is to be expected with these structures, as the Schottky-barriers and the channel barrier are modulated in the same way by a single gate and the electrical voltage applied there. Or in other words, no specific charge carrier type, holes and electrons, is surppressed. The measurements illustrated in the figure 4.3 were taken in a vacuum and show precisely this

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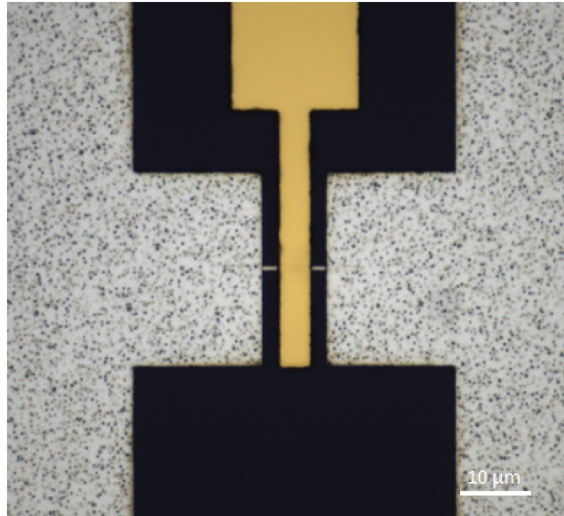

Figure 4.2: *STG device with Au top-gate captured by optical microscope.*

behavior. It should be noted that the length of this device is approximately 0.186 μm and the width is 0.123 μm, which is very small. In (a), the measurement is performed from V_{TG} = -3V to 3V, and in (b) from -4V to 4V, as a double sweep. V_{DS} is applied symmetrically, meaning V_D = - V_S, in both cases, and two different values, namely 1V and 2V, are used. Here, a large difference and a dependence of the drain-current I_D on both voltages can already be seen. It seems that in subfigure (a) the p-current for the higher bias voltage corresponds to an increase of about 3 times, from 2.107 μA to 6.395 μA , as well in (b) from 6.862 μA to 16.83 μA. The n-mode is about one order smaller, which is to be expected due to the material system with regard to Fermi-level pinning. The electron current in (a) rise from 0.804 μA to 1.612 μA and in (b) from 1.627 μA to 2.335 μA. Here, the dependency on the voltage is lower, also the curves have a more pronounced hysteresis, which can be explained by slow surface traps causing a built-in voltage. Furthermore, a voltage shift to the right can be seen in both plots for the threshold V_{th}, with the higher V_{DS}. The same measurements are performed for another device with length and respectively width of 1.003 μm and 0.193 μm, shown in figure 4.4. The biggest difference is that the symmetry of the p and n currents is better, with the p-mode exhibiting comparable saturation. Furthermore, it is noticeable that hysteresis practically disappears, which is a desirable characteristic, but the threshold voltage shift is similar. For further measurements of these STGs, wider structures with different lengths are used.

4.1.1.2 Output characteristics - STG

As described in the experimental chapter, in section 3.2.3, the output characteristics of STG are obtained. Since the geometrically larger device D12 performed better in the previous section and this characteristic is only a minor and relatively unimportant aspect of this work, it will only be discussed for this device. As shown earlier, it has ambipo-

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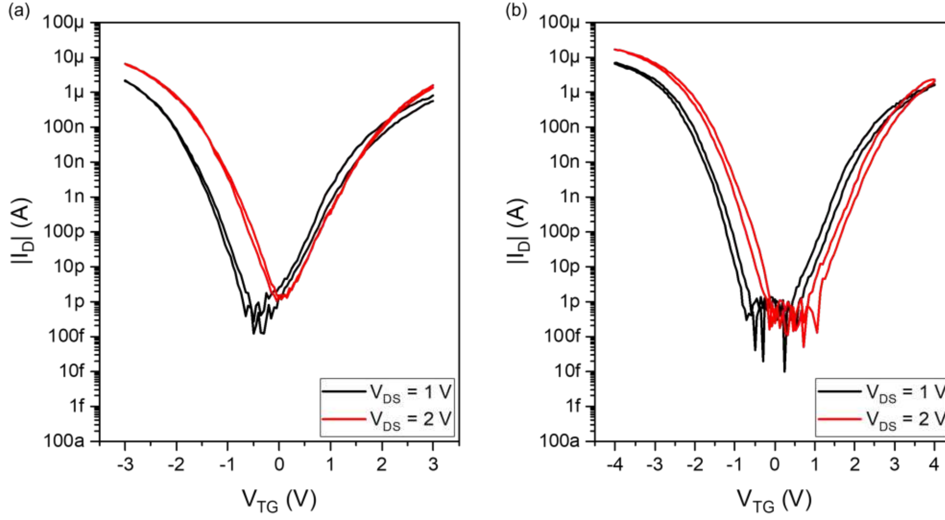

Figure 4.3: *Double sweep transfer characteristics of sample SOI41 device D91 (length = 0.186 µm , width = 0.123 µm): (a) V_{TG} = -3 V .. 3V, (b) V_{TG} = -4 V .. 4V; Bias-voltage V_{DS} is applied symmetrically and is 1/2 V for the black/red curves*

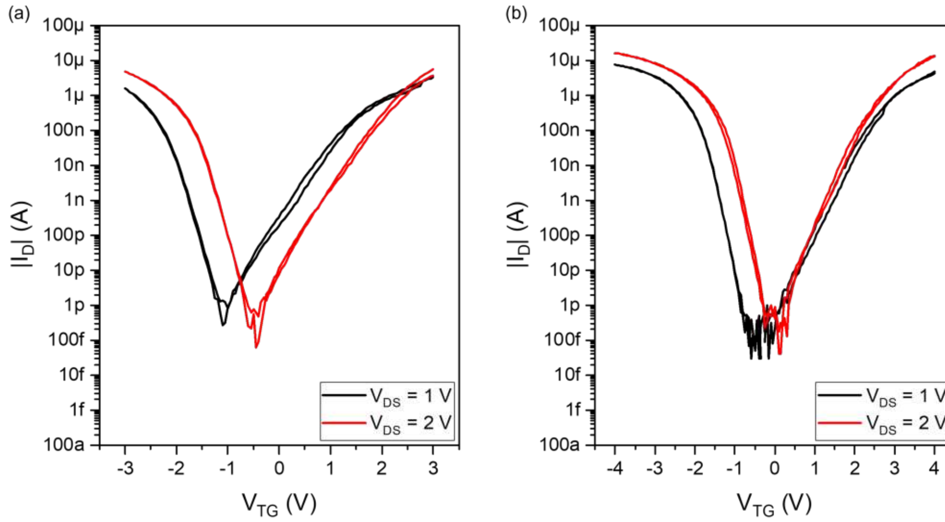

Figure 4.4: *Double sweep transfer characteristics of sample SOI41 device D12 (length = 1.003 µm , width = 0.193 µm): (a) V_{TG} = -3 V .. 3V, (b) V_{TG} = -4 V .. 4V; Bias-voltage V_{DS} is applied symmetrically and is 1/2 V for the black/red curves*

lar behavior, which allows it to be switched with positive and negative voltage at the gate. In principle, the measurements are performed with a symmetric bias-voltage V_{DS} ranging from -1V to 1V, meaning that V_D is swept from 0.5 V to -0.5 V while maintaining V_D = -V_S. The different voltage levels at V_{TG} are varied between -3 V and 3 V in steps of 0.5 V, yielding a total of 13 individual curves. Because the STG operates ambipolarly, neither type of charge carrier is suppressed, which means both conduction modes appear, although with different on-current. Furthermore, a sufficiently large top-

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gate voltage must be applied to shift the barriers thickness and thereby enable higher currents, consistent with observations from the transfer measurements. For this purpose, the areas for n- and p-operation are divided in the figure 4.5 at V_{TG} = -0.5 V. Subfigure (a) shows the n-mode, and it can be seen that it is difficult to divide whether an electron or hole current is observed with regard to lower V_{TG}. The actual off-state, where one of the two charge-carrier types is likely to become dominant, should be between curves V_{TG} -0.5 V and -1 V, which is also indicated in the voltage shift in figure 4.4 from the zero point. However, the hole current reaches the desired saturation range more quickly, which means that less source-drain bias V_{DS} is required. This can be explained with the asymmetric Schottky-barrier for the charge-carrier types. The non-linear increase of the V_{STG}-dependent current, which is visible in the logarithmic representation, shows a typical characteristic of a SBFET, attributed to the bias dependent change of barrier thickness and related tunneling transmissibility [45, 66].

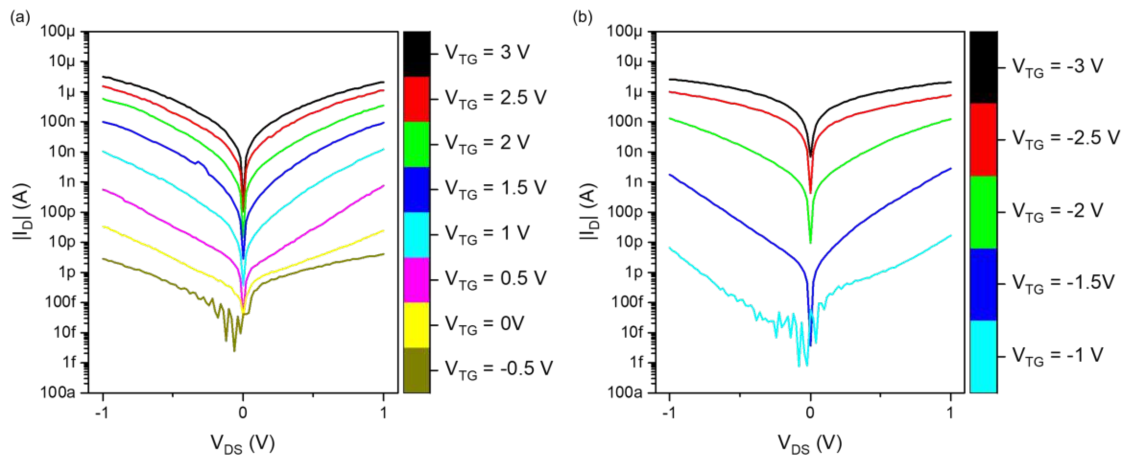

Figure 4.5: *Output characteristics of sample SOI41 device D12 (length = 1.003 µm , width = 0.193 µm): (a) electron dominant current, (b) hole dominant current; Bias-voltage V_{DS} is applied symmetrically and is swept from -1 V to 1 V*

4.1.2 Si-based single top-gates at cryogenic temperatures

After the devices of sample SOI 41 have delivered a solid impression at room temperature, the next step is to cool them down and observe their behavior. The sample is first cooled down to approximately 5 K and then gradually brought back to room temperature (295 K). As described in section 3.2.1, this is done using helium and nitrogen and three devices of different lengths are selected for this purpose. Their geometrical properties are given in 4.2. The transfer characteristic is particularly interesting here, as it can be used to determine temperature-related changes in the subthreshold swing STHS, threshold voltage V_{th} and conductance g_m. The evaluation of these parameters are investigated in section 4.1.4 for TTGs, as the measurements on STGs are just meaningful for starting this work.
Figures 4.6 and 4.7 show the three devices with two different symmetrical bias voltages V_{DS}, 1 V and 0.25 V, in the subfigures. V_{TG} is swept from -3 to 3 V respectively from

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device	**length**	**width**
D05	0.218 μm	0.190 μm
D10	0.65 μm	0.226 μm
D12	1.003 μm	0.193 μm

Table 4.2: *Geometric dimensions of the semiconductor channels of the measured STGs*

-4 to 4 V, and the curves are represented for three different temperatures by the colors red (room temperature), orange (medium temperature) and blue (cryogenic). Looking at the measurements, you can see that they behave similarly for all three temperatures. The curves become considerably steeper at lower temperatures, resulting in lower STHS, which was to be expected, as discussed in the theory section for CMOS 2.1. The current I_D reaches the resolution limit (noise) of the measuring environment much faster and rises to the desired level for the p-mode, but needs more than 3V at V_{TG}. In contrast to 295 K, the curves for cryogenic measurements show a distinct off-state and not just a minima. The electron current decreases at lower temperatures, which is interesting because, as described in section 2.1.2.3, it should actually increase or remain the same. It could be that the Schottky barrier becomes higher or wider for the electrons due to surface states. The fact that there is a large shift for V_{th} is also confirmed here and can be explained by the widening of the band gap of Si. However, when comparing the curves, the largest device D12 in (e) and (f) exhibits the best symmetry and a marginal small hysteresis, confirming the argument in section 4.1.1.1. Also, the shift in V_{th} seems to be more consistent, meaning that at a certain temperature, the change of the shift for cryogenic operation is approximately the same. Although the p-mode appears relatively similar for all three devices in terms of the shape and strength of the current curve, the n-modes are very different. With smaller structures, especially with smaller source-drain voltages, more charging effects seem to occur, which can be observed by the peaks on the right side. Note that it can be quite challenging to maintain the same temperature for a long period of time, as the measurement system is not automated and the pressure and flow of the coolant must be adjusted manually. In a further note, no curve close to 5K is shown for D05, as the problem with the cooling of the needles, described in section 3.2.1, was discovered during the evaluation. Nevertheless, the 25 K measurement is a good indication of the cryogenic behavior of this device and would only change marginally at lower temperatures. Further evaluations are made for TTG structures, as they are more important, because of their ability to suppress one carrier-type and the STG devices are meant as a starting point for this thesis.

4.1.3 Si-based triple top-gates at room temperature

After the discussion of the behavior of STG devices for transfer and output characteristics, the next aspect to show are the corresponding curves for TTG devices. The band bending resulting from the applied TG voltages is illustrated and discussed in figure 2.7 of section 2.2.3. Consequently, in the following, the structures of samples SOI29 and SOI41 are measured as illustrated in figure 3.4. These fabricationd samples contain structures with

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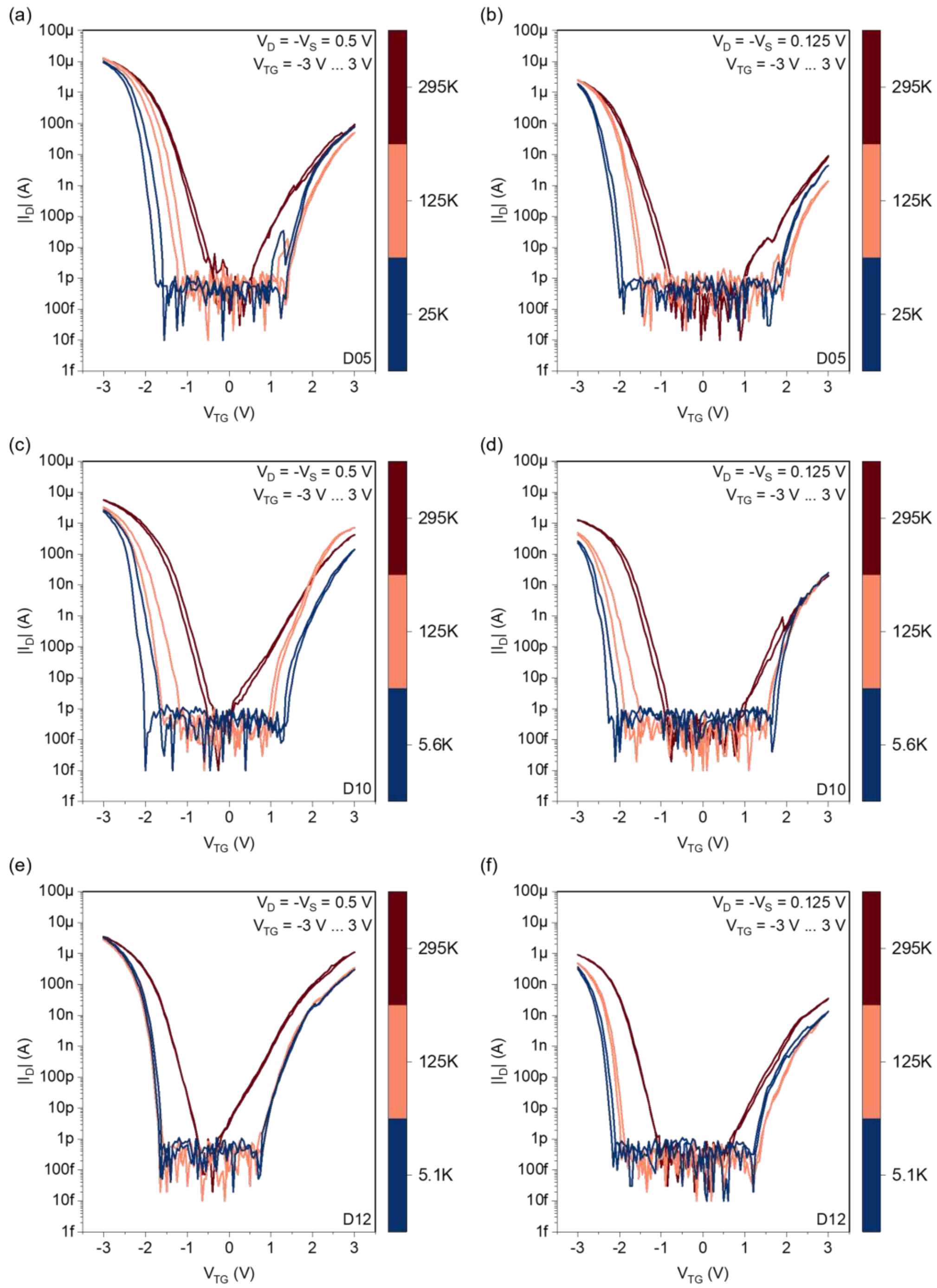

Figure 4.6: *Double sweep transfer characteristics of STG devices from sample SOI 41 for different temperatures and bias voltages V_{DS}: (a), (c) and (e) for V_{DS} = 1 V; (b), (d) and (f) for V_{DS} = 0.25 V; Gate-voltage V_{TG} is swept from -3 V to 3 V*

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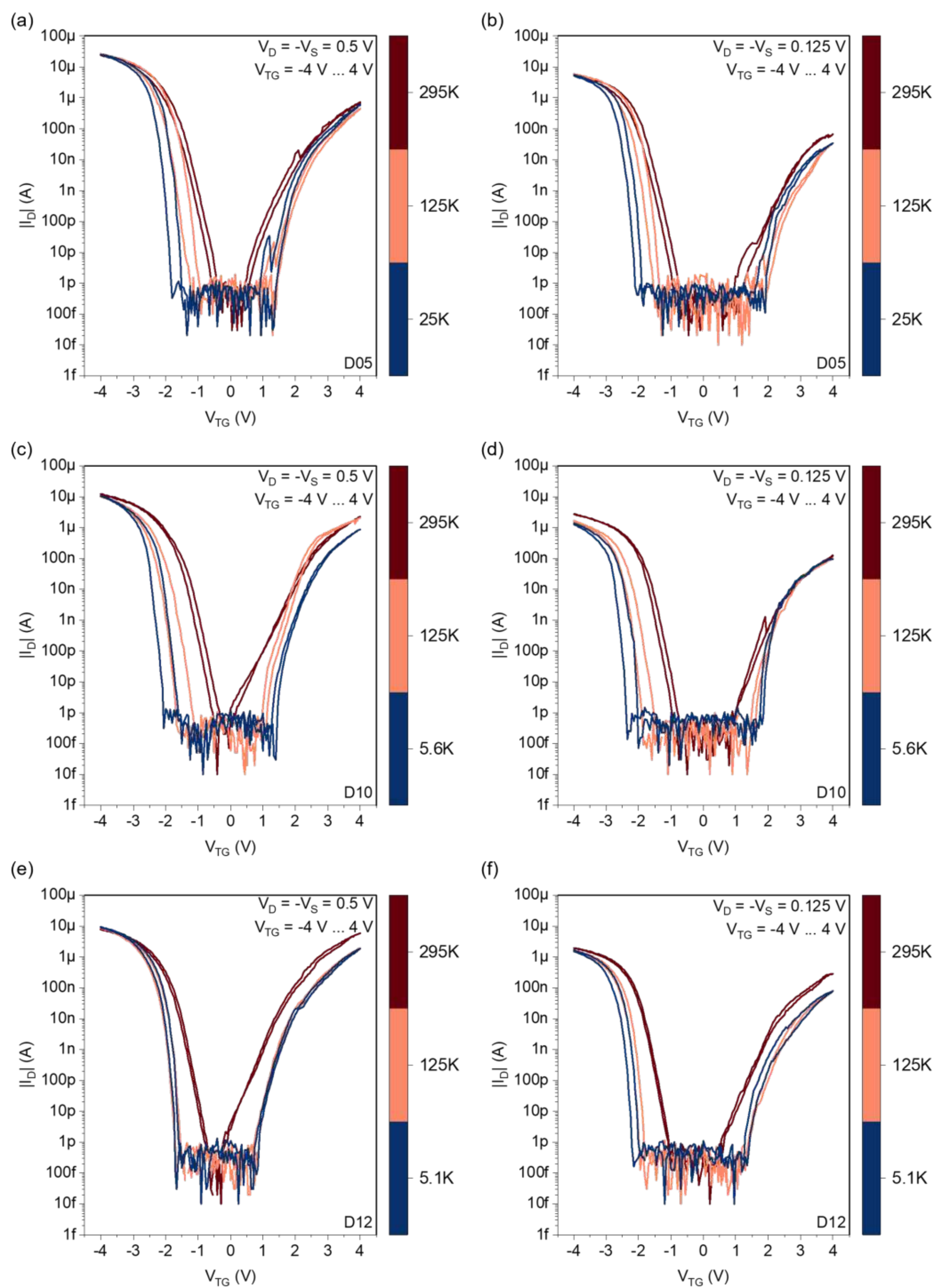

Figure 4.7: *Double sweep transfer characteristics of STG devices from sample SOI 41 for different temperatures and bias voltages V_{DS}: (a), (c) and (e) for V_{DS} = 1 V; (b), (d) and (f) for V_{DS} = 0.25 V; Gate-voltage V_{TG} is swept from -4 V to 4 V*

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Au and Al top gates, as already indicated in table 4.1. In figure 4.8, one device of SOI29 with a Al top gate is captured by (a) an optical microscope and (b) by a SEM.

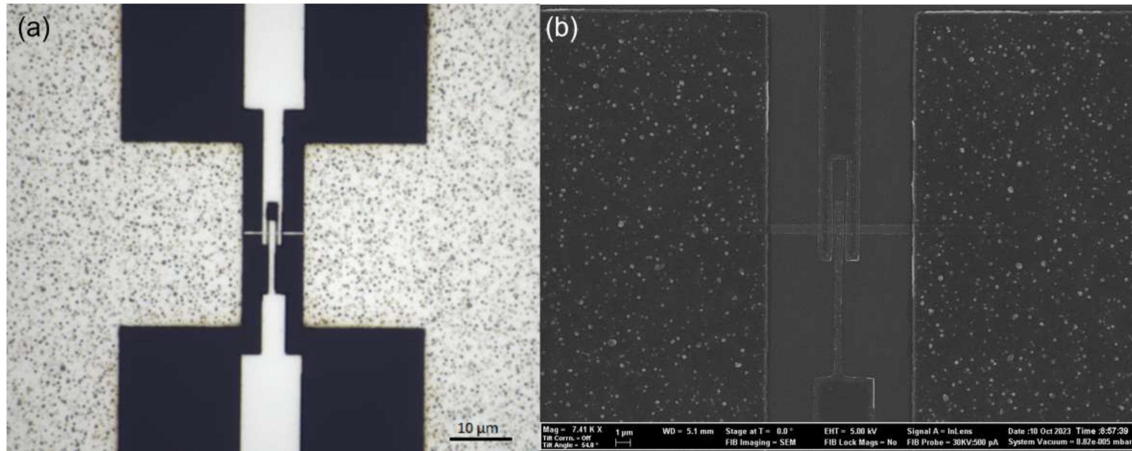

Figure 4.8: *TTG device with Al top-gate captured by (a) optical microscope and (b) SEM.*

4.1.3.1 Evolution of the project

Unlike the STG devices, where the off-state current appears as a single minimum point or, depending on hysteresis effects, as multiple minima, the TTG structures show clearly separated off-states. This distinction arises from the additional control provided by the CG, which enables the suppression of unwanted carrier conduction and allows for defined n-type and p-type operation modes. As already discussed in section 3.2.2, there is one transfer curve for each operating mode, which is selected via the applied voltage level at the PG. Figure 4.9(a) shows one transfer characteristic of a device from sample SOI41 for both modes in atmospheric ambient. The currents of the on-states are lower than expected here, at 1.824 μA for the p-mode and 273.4 nA for the n-mode, whereas the off-state is solid. If now the same structure is measured in a vacuum, as in subfigure (b), the behavior changes significantly and one cannot speak of a functioning device under these conditions. The p-mode on-currents drop dramatically and no longer exhibits actual characteristics of a transistor, while the n currents decrease by about half.
Since only the environment has changed between these two measurements, it is obvious that this makes a difference. Comparisons between the STG, which worked in a vacuum, and the TTG structures are made, so the cause can be suspected. In STG, there is a large gate covering the entire channel and the dielectric, which protects it from external influences and provides certain surface states at this interlayer. Looking at the TTG, there are gaps (ungated regions) between the gates where the oxide comes into contact with the vacuum. It is assumed that surface traps on the dielectric limit the performance of this structure [60]. The thought of solving this was to deposit a passivation or capping layer over the sample to fill these open trenches between the gates. The first attempts are made with PECVD-grown Si nitride, but turned out that this layer is not well suited for temperature cycling in vacuum. These films exhibit significant intrinsic stress and strong

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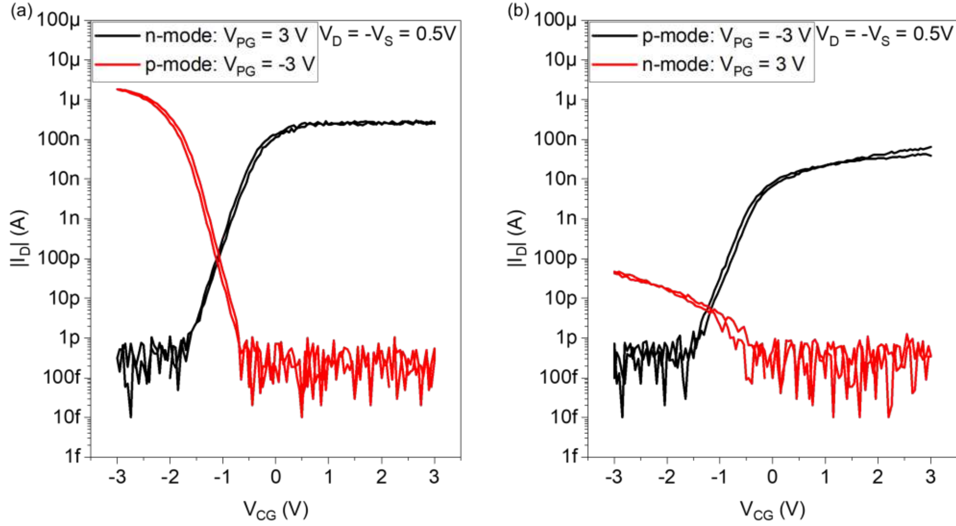

Figure 4.9: *Double sweep transfer characteristics of sample SOI41 device D06 (a) in atmospheric ambient and (b) in vacuum for V_{CG} = -3 V .. 3V; Bias-voltage V_{DS} = 1V (V_D = - V_S).*

thermal stress responses due to differences in thermal expansion and hydrogen incorporation during deposition[67]. This can lead to cracking, delamination, and mechanical instability under thermal cycling and vacuum conditions. Unfortunately, this meant that sample SOI41 is rendered unusable for further research for this thesis. Another experiment with SiO_2 oxide deposited using PECVD proved successful. The deposition process has already been described in section 3.1.1.5 and is carried out for sample SOI29. However, there are two types of TTGs on this sample: one with Au and one with Al top gates. Figure 4.10 shows a transfer characteristic before, during, and after vacuum for p-mode and n-mode for devices with (a) Au and (b) Al gates. The curves in (a) show clear differences for the respective conditions. While a relatively expected curve can be observed before the vacuum, the off-state increases during it and remains permanent. The on-state respectively the slope reminds of the inflection phenomena for CMOS described in section 2.1.2.2. The transfers in subfigure (b) look solid for all three circumstances and only a small permanent shift in the threshold voltage is noticeable, which in this case even occurs in the desired direction. To get to the bottom of the problems with Au top gates, figure 4.11 shows the gate currents for both devices. In subfigure (a), these are increased for the range of V_{CG} between -3 V and approximately -0.5 V, suggesting a conductive path in the oxides. One explanation for this would be that Au diffuses into the SiO_2 capping layer and the dielectric, creating a tunneling current between CG, PG and the semiconductor channel. Since PECVD passivation takes place at a temperature of 573 K, such diffusion is very likely to occur, as Au is known to diffuse easily into amorphous SiO_2 at temperatures even below 600 K [68, 69]. In contrast, Al shows negligible diffusion into SiO_2 under comparable process conditions, which explains why the gate currents in subfigure (b) exhibit no increased plateaus [33]. All in all, no devices with Au are used in the following work, since passivation with SiO_2 is a fundamental building block for TTG structures in relation to cryogenic measurements that must be performed in a vacuum.

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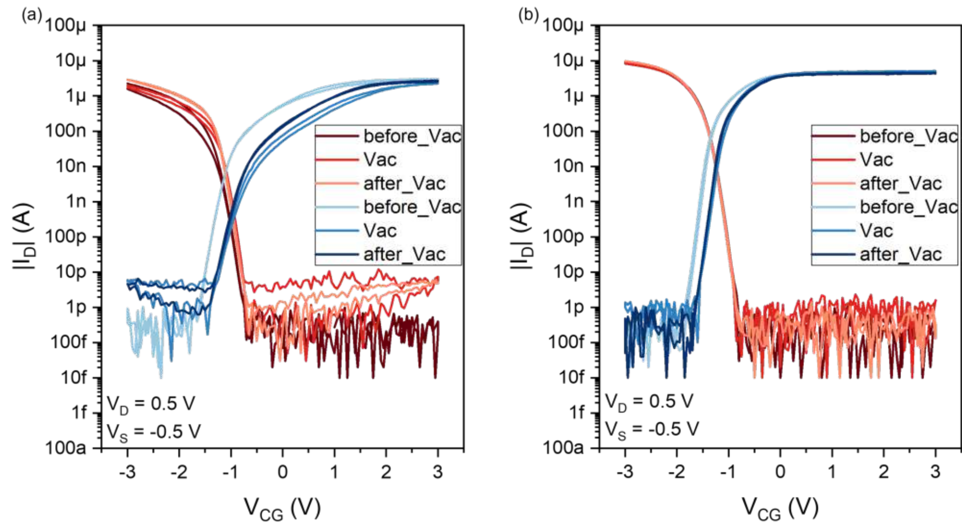

Figure 4.10: *Double sweep transfer characteristics performed before, during and after vacuum with (a) Au and (b) Al gates.* V_{CG} *= -3 V .. 3V; Bias-voltage* V_{DS} *= 1V (*V_D *= -* V_S*).*

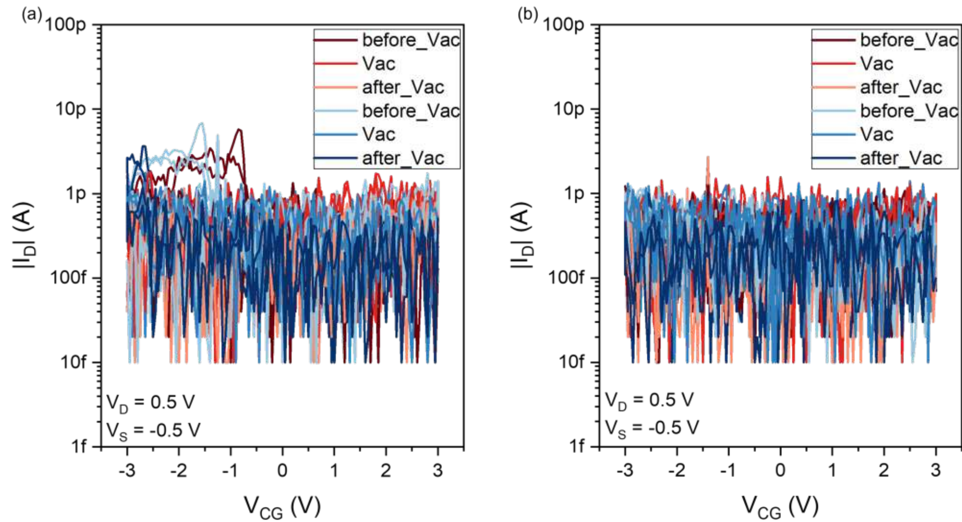

Figure 4.11: *Relating gate currents for transfer characteristics in figure 4.10 for (a) Au and (b) Al gates.* V_{CG} *= -3 V .. 3V; Bias-voltage* V_{DS} *= 1V (*V_D *= -* V_S*).*

4.1.3.2 Transfer characteristics - TTG

Having now functioning devices, their behavior in a vacuum is examined more closely. To this end, a transfer characteristic is again recorded for various electrical measurement setups, as was already done for STGs. As described in section 4.1.3.1, a certain voltage on the program gate V_{PG} enables the suppression of unwanted carrier conduction to get two off-states. Figure 4.12 provides curves for (a) the p-mode (V_{PG} = -3 V) and (b) the n-mode (V_{PG} = 3 V) with different source-drain voltages V_{DS} of 0.2 V and 1 V in a vacuum at room temperature. For p-type operation the control gate voltage V_{CG} is

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swept from 3 V to -3 V, whereas for n-type operation it is swept from -3 V to 3 V, as double characteristics. The associated semiconductor channel width and length of the selected TTG are 0.417 μm and 2.96 μm. The curves are shifted slightly to the left of zero, indicating a negative threshold voltage. Such shifts are a characteristic of the SiO_2 dielectric used, as different oxides and high-k materials can alter the threshold voltage through their intrinsic charge and band alignment properties, allowing either positive or negative V_{th} tuning depending on the oxide choice [70]. Furthermore, threshold voltage can be influenced by an additional back-gate bias applied to the substrate to re-center the curves, by modulating the body potential [71]. In this work the substrate is grounded with the analyzer via the copper plate and the effect of other signals is not considered in the analysis. The shift is also bias voltage dependent, which is discussed in more detail in section 4.1.4.1. However, as with the STG in section 4.1.1.1, a clear dependence of the current on the source-drain voltage can also be seen. For p-mode, the current increases from 1.638 μA to 8.665 μA, whereas for n-mode, from 489.6 nA to 8.370 μA. The on-states are very symmetrical for the curves with 1 V bias, there is no hysteresis and therefore no trap effects can be detected. Both off-states are at the desired value, the noise level of the measuring system. Additionally, it should be noted that a direct comparison between STG and TTG devices is not straightforward, since their structural designs differ and the STG devices typically feature shorter channel lengths. Therefore, any comparison between the two device types must be interpreted with appropriate caution. In addition, it must be said that the on-current for the p-mode is not yet fully saturated here, which can be achieved with a higher V_{CG}. For safety reasons, in order not to destroy the devices, this is not used.

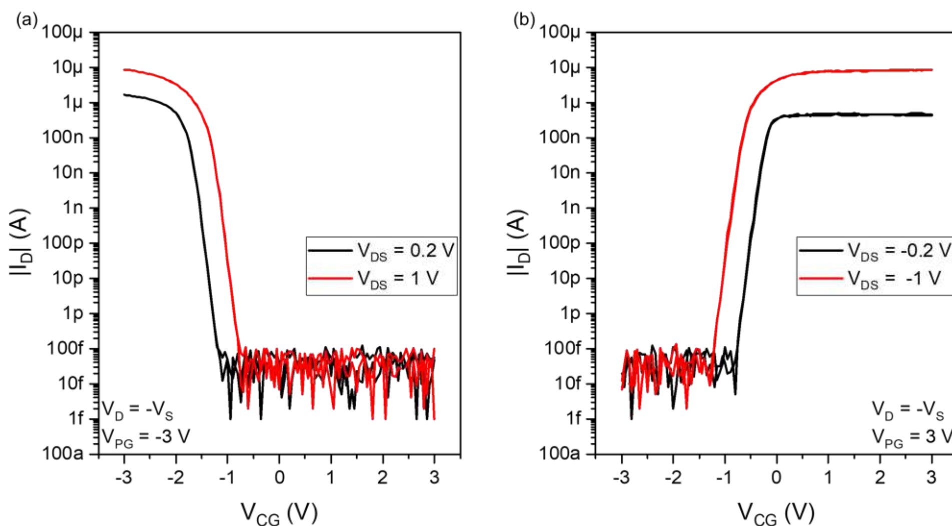

Figure 4.12: *Double sweep transfer characteristics of sample SOI29 device D32 (length = 2.96 µm, width = 0.417 µm): (a) p-mode: V_{PG} = -3 V, (b) n-mode: V_{PG} = 3 V; Bias-voltage V_{DS} is applied symmetrically and is 0.2/1 V for the black/red curves*

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4.1.3.3 Output characteristics - TTG

In a similar way to the STG output characterization, the measurement procedure for the TTG output characteristics is explained in section 3.2.3. Unlike the ambipolar STG devices, the TTG structures use an additional program gate (PG) to suppress undesired charge-carrier transport, enabling distinct p-type and n-type operation modes. Consequently, the output characteristics include separate output curves for both carrier types. Figure 4.13 is logarithmic representation of the output curves for (a) p-mode and (b) n-mode. Note, that this is the same TTG structure as for the transfer characteristic in section 4.1.3.2 and all data is captured in vacuum at room temperature. The bias voltage V_{DS} is applied symmetrical and swept from -1 V to 1 V for different voltages on CG, changed from -3 V to 3 V in 0.5 V steps. The operation modes are set with the PG voltage V_{PG} of -3 V for p-type and 3 V for n-type. It is apparent, that also the TTG device shows non-linear increase of the current with respect on V_{CG} for both modes, visible in the subfigures. This a conventional characteristic of Schottky-barrier FETs [45, 66]. In general, it can be observed that the curves exhibit a certain symmetry with respect to the different bias voltages. The difference between the on-states of the two modes can be explained by Fermi-level pinning and the resulting different Schottky-barriers. That there are more curves with higher currents for the n-operation is related to the threshold voltage shift. Furthermore, it should be noted that the barriers created by the applied V_{PG} suppress unwanted charge carriers, so that certain ranges of V_{CG} generate only very low currents, indicating that the RFET is in the off state. This behavior is in contrast to the observed ambipolar characteristics of the STG structures.

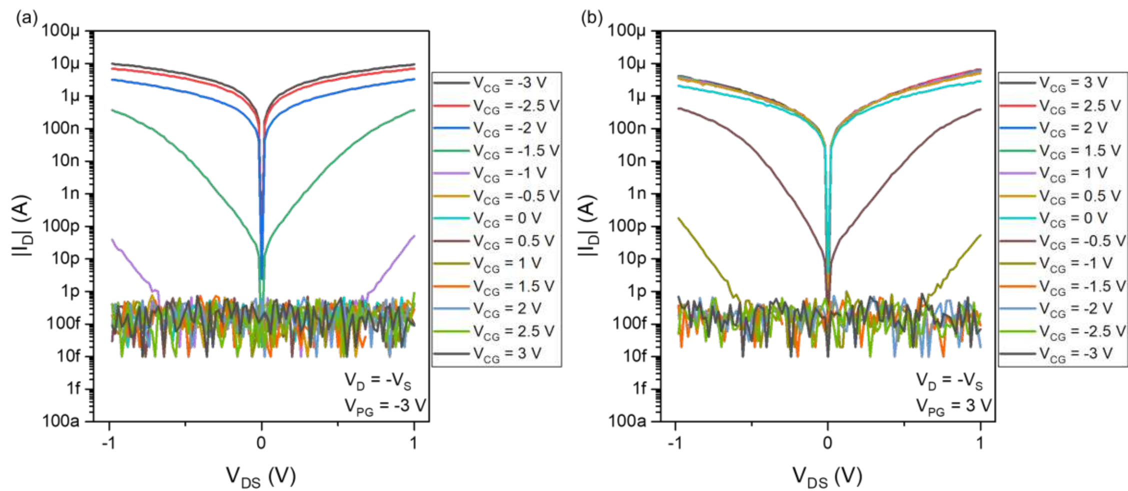

Figure 4.13: *Output characteristics of sample SOI29 device D32 (length = 2.96 μm, width = 0.417 μm): (a) p-mode, (b) n-mode; Bias-voltage V_{DS} is applied symmetrically and is swept from -1 V to 1 V*

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4.1.3.4 PG sweep

As already described in section 3.2.4, RFETs have another important characteristic to investigate due to their ability to suppress charge carriers. This PG sweep provides information about the voltage V_{PG} at which one mode or the other becomes dominant, means at what point the current between holes and electrons switches through the electrostatic control of the barriers. The same device as for transfer and output characteristic is examined for this purpose in figure 4.14. V_{PG} changes from -3 V to 0 V in (a) and in (b) from 3 V to 0 V in 0.5 V steps. The source-drain voltage V_{DS} is applied symmetrically with 1 V and the voltage on control gate V_{CG} is swept from -3 V to 3 V and back, again in vacuum at room temperature. In other words, transfer characteristics are measured with different voltage level on the metal-semiconductor interfaces. It is apparent, that also this characteristic shows non-linear increase of the current with respect on V_{PG} for both modes. Taking a look at subfigure (a), it can be said that the hole dominant current again has fewer curves for this measurement setup and the measurements for V_{PG} of -0.5 V and 0 V already represent a low electron current. This behavior may again be related to the threshold voltage and the used dielectric and could be improved by using other materials. Interestingly, the 0 V curve in subfigure (b) delivers a higher current, which could be related to the different sweep directions for V_{PG} and V_{CG} in the two measurements.

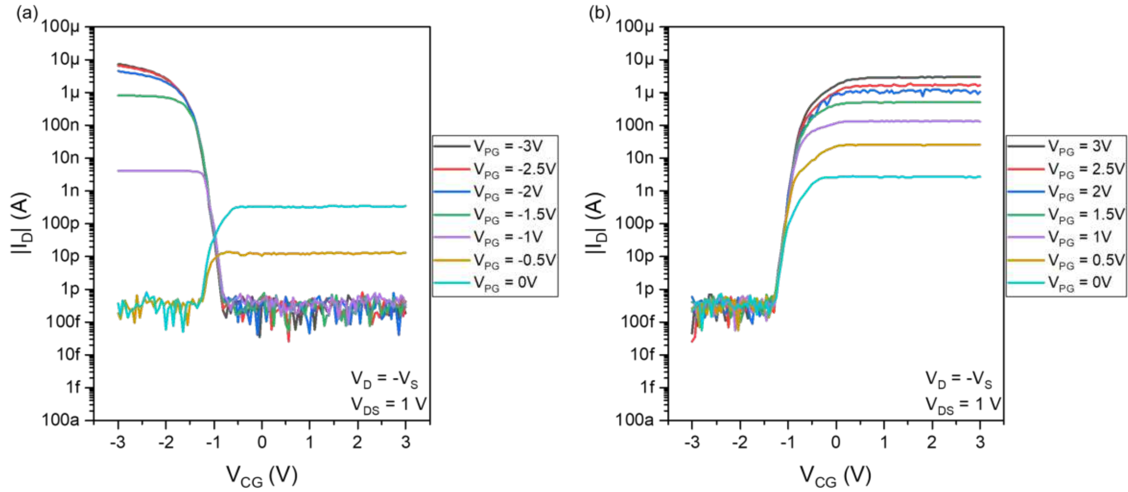

Figure 4.14: *PG sweep of sample SOI29 device D32 (length = 2.96 µm, width = 0.417 µm): (a) V_{PG} from -3 V to 0 V, (b) V_{PG} from 3 V to 0 V; Bias-voltage V_{DS} is applied symmetrically and equals 1 V; V_{CG} is swept from -3 V to 3 V*

4.1.4 Si-based triple top-gates at cryogenic temperatures

Having established that the TTG structures exhibit desirable behavior in a vacuum at room temperature, they are now being investigated at lower temperatures. The sample is first cooled down to approximately 4.5 K and then gradually brought back to room temperature (295 K). As described in section 3.2.1, this is done using helium and nitrogen. For this purpose, as with the STGs, two devices from sample SOI29 with different-sized

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semiconductor channels are investigated to demonstrate reproducibility, which are listed in Table 4.3. The widths of the devices are relatively similar, but there are greater differences in length. The transfer characteristic is particularly interesting here, as it can be used to determine temperature-related changes in the subthreshold swing STHS, threshold voltage V_{th} and transconductance g_m.

device	**length**	**width**
D12	2.554 μm	0.429 μm
D38	2.122 μm	0.445 μm

Table 4.3: *Geometric dimensions of the semiconductor channels of the measured TTGs*

The transfer curves of both modes for the respective devices are shown in figures 4.15 and 4.16 for symmetrical source-drain voltages V_{DS} of 1 V, 0.5 V and 0.2 V, respectively. The voltage at the control gate V_{CG} is swept from 3 V to -3 V for the p-mode and from -3 V to 3 V for the n-mode as a double characteristic. The respective modes are set by applying the voltage to the program gate V_{PG} and is 3 V for n-mode on the right and -3 V for p-mode on the left. Overall, measurements are taken at 7 different temperatures, but to make the differences easier to see, only 4 are shown in the transfer curves. A look at the figures shows that both devices exhibit similar behavior and that the curves become steeper at lower temperatures, which means subthreshold swing STHS is decreasing. Furthermore, the threshold voltage V_{th} is shifted to the left for p-operation and to the right for n-operation. These properties of the structures have already been observed in STGs, and the reasoning behind this behavior is the same. Detailed analysis for these parameters will be done in the following sections. The currents of the respective on-states decrease for both types as the temperature drops, while the off-state remains the same desired value of the noise level of the measuring system, except for the 295 K curves of D38. The devices have an I_{on}/I_{off} ratio for $V_{DS} = 1V$ between 10^8 and 10^9 for all temperatures and both modes. The on-state currents of the two devices are plotted against temperature in Figures 4.17 and 4.18, with subfigure (a) showing the values for the p-mode and (b) for the n-mode. The left axis shows the absolute values of the current, and the right axis has them normalized over the width W of the structure. Here, the exponential decline for lower temperatures is clearly visible for all three measurement setups. Attached to the figures are tables with the values at 295 K and 4.5 K for both modes and all bias voltages, so that the drop can also be read in numbers. In order to make a quantitative statement, the drop in current from 295 K to 4.5 K is given below as a percentage. For device D12, the on-currents I_{on} at 4.5 K for V_{DS} 1 V, 0.5 V, and 0.2 V in p-mode are 46.8%, 19.1%, and 6.8% of the current at 295 K, for n-mode 51.6%, 40.1%, and 31.5%. Analogously, the values for device D38 are 58.9%, 46.3%, and 12.8% for p-mode and 61.3%, 38.1%, and 24.1% for n-mode. These increasing differences can also be seen very clearly in the transfer curves, meaning that the hole current loses considerably more strength at cryogenic temperatures than the electron current.

Note that the current for the p-mode for D12 is smaller than the n-mode, which should not be the case due to the mechanism involving Fermi level pinning to the valence band

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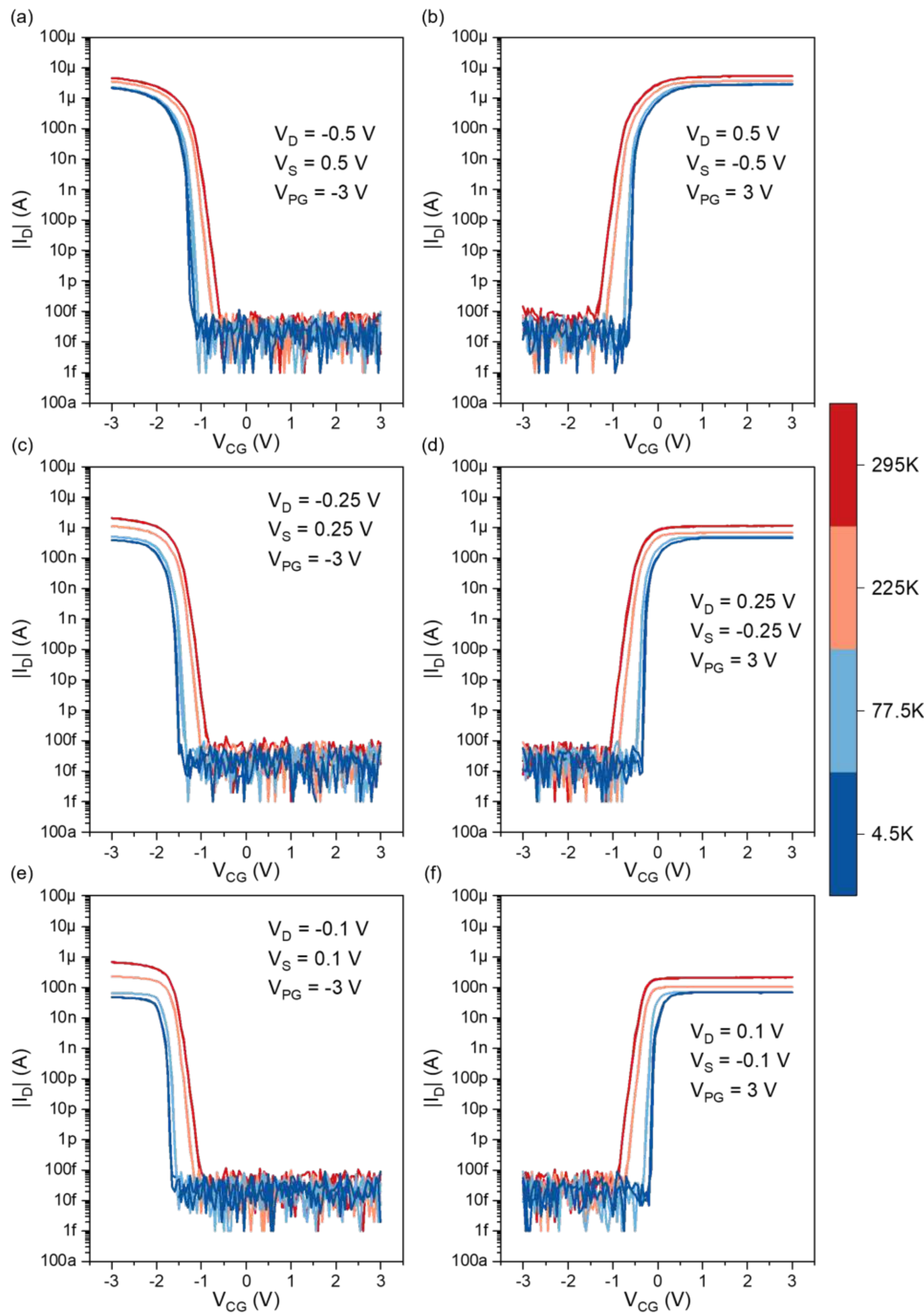

Figure 4.15: *Double sweep transfer characteristics of TTG device D12 from sample SOI29 for different temperatures and different symmetrical source-drain voltages V_{DS}: subfigures on the left illustrate the p-mode means V_{PG} = -3 V with V_{DS} (a) = 1 V, (c) = 0.5 V, (e) = 0.2 V, while subfigures on the right shows the n-mode means V_{PG} = 3 V with V_{DS} (b) = 1 V, (d) = 0.5 V, (f) = 0.2 V; Gate-voltage V_{CG} is swept from -3 V to 3 V for the p mode and for the n-mode from -3 V to 3 V*

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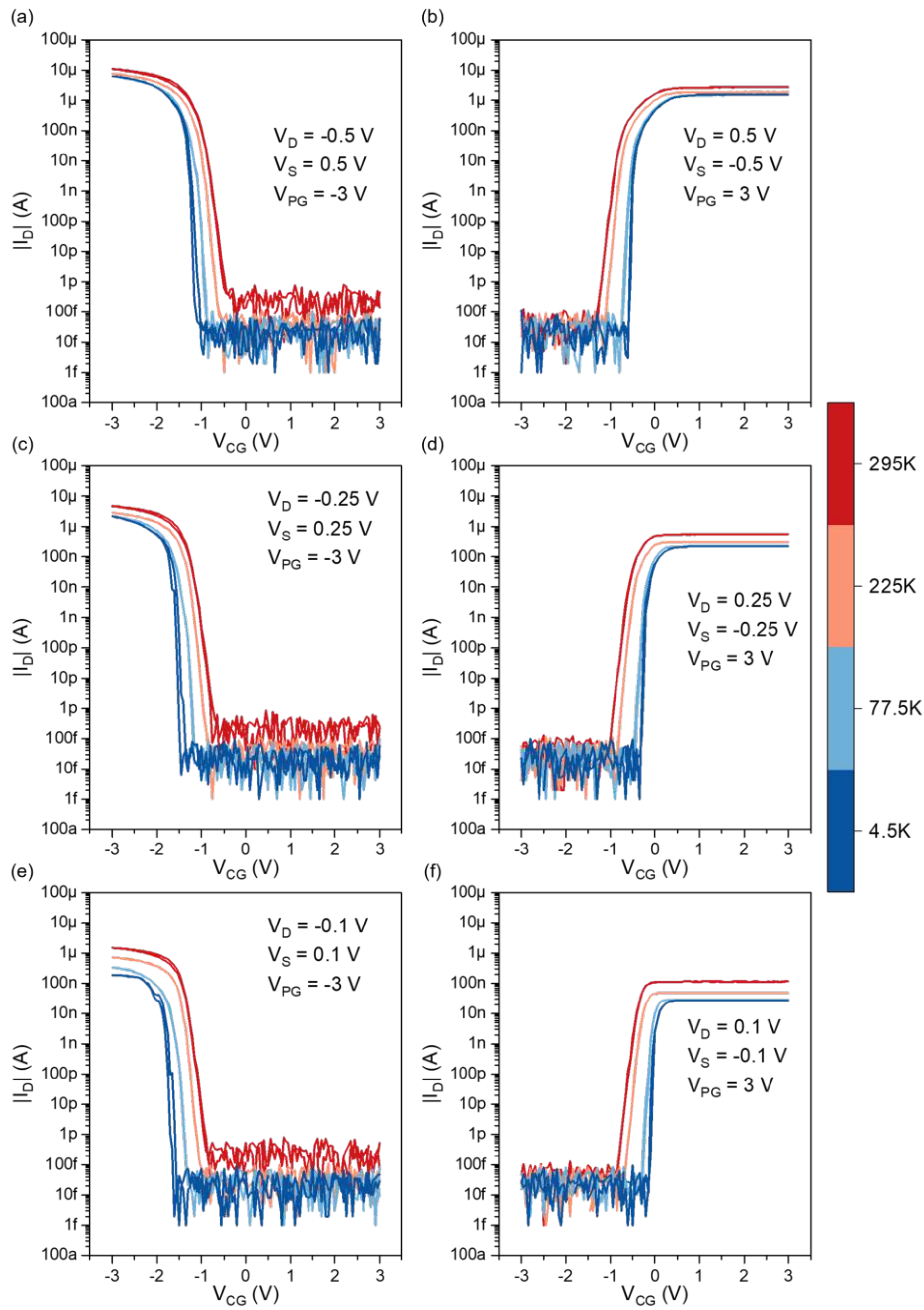

Figure 4.16: *Double sweep transfer characteristics of TTG device D38 from sample SOI29 for different temperatures and different symmetrical source-drain voltages V_{DS}: subfigures on the left illustrate the p-mode means V_{PG} = -3 V with V_{DS} (a) = 1 V, (c) = 0.5 V, (e) = 0.2 V, while subfigures on the right shows the n-mode means V_{PG} = 3 V with V_{DS} (b) = 1 V, (d) = 0.5 V, (f) = 0.2 V; Gate-voltage V_{CG} is swept from -3 V to 3 V for the p mode and for the n-mode from -3 V to 3 V*

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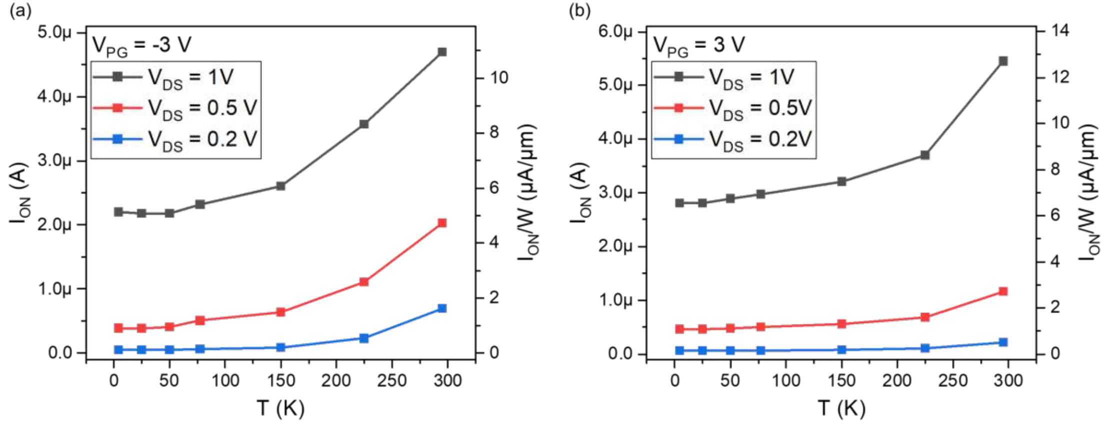

V_{DS} = 1 V

T (K)	$I_{ON,p}$ (μA)	$I_{ON,p}/W$ $(\mu A/\mu m)$	$I_{ON,n}$ (μA)	$I_{ON,p}/W$ $(\mu A/\mu m)$
295K	4.7	10.955	5.453	12.711
4.5K	2.198	5.124	2.813	6.557

V_{DS} = 0.5 V

T (K)	$I_{ON,p}$ (μA)	$I_{ON,p}/W$ $(\mu A/\mu m)$	$I_{ON,n}$ (μA)	$I_{ON,p}/W$ $(\mu A/\mu m)$
295K	2.03	4.732	1.159	2.703
4.5K	0.388	0.904	0.465	1.085

V_{DS} = 0.2 V

T (K)	$I_{ON,p}$ (μA)	$I_{ON,p}/W$ $(\mu A/\mu m)$	$I_{ON,n}$ (μA)	$I_{ON,p}/W$ $(\mu A/\mu m)$
295K	0.695	1.619	0.216	0.504
4.5K	0.047	0.111	0.068	0.158

Figure 4.17: *On-state currents of the transfer curves from figure 4.15 of TTG device D12 from sample SOI29 plotted against temperature for different symmetrical source-drain voltages V_{DS}: (a) for the p-mode and (b) for the n-mode. In addition, the current values and the currents normalized over the width, 0.429 µm ,of the structure are given in tables for temperatures of 295K and 4.5K.*

[33]. This leads to the assumption that the p-mode could be not yet fully saturated in this device at this operating window, but could be also the devices behavior. Furthermore, the current intensity of the two structures normalized to the width can be compared, but this will only be done for the surely saturated n-mode in the following. Here, structure D12 has approximately twice the current of D38 for all source-drain voltages at temperatures of 295K and 4.5K, which is interesting because it has a longer channel. In SBFETs the drain current is primarily limited by the Schottky- barriers rather than by the channel

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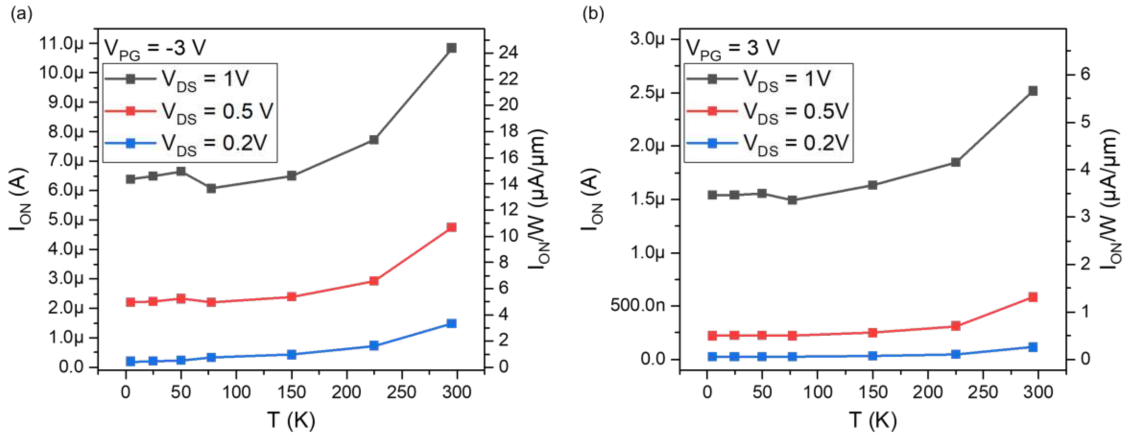

V_{DS} = 1 V

T (K)	$\mathbf{I}_{ON,p}$ (μA)	$\mathbf{I}_{ON,p}/W$ $(\mu A/\mu m)$	$\mathbf{I}_{ON,n}$ (μA)	$\mathbf{I}_{ON,p}/W$ $(\mu A/\mu m)$
295K	10.846	24.372	2.518	5.658
4.5K	6.386	14.351	1.544	3.469

V_{DS} = 0.5 V

T (K)	$\mathbf{I}_{ON,p}$ (μA)	$\mathbf{I}_{ON,p}/W$ $(\mu A/\mu m)$	$\mathbf{I}_{ON,n}$ (μA)	$\mathbf{I}_{ON,p}/W$ $(\mu A/\mu m)$
295K	4.761	10.698	0.582	1.31
4.5K	2.202	4.95	0.222	0.499

V_{DS} = 0.2 V

T (K)	$\mathbf{I}_{ON,p}$ (μA)	$\mathbf{I}_{ON,p}/W$ $(\mu A/\mu m)$	$\mathbf{I}_{ON,n}$ (μA)	$\mathbf{I}_{ON,p}/W$ $(\mu A/\mu m)$
295K	1.491	3.351	0.116	0.26
4.5K	0.191	0.429	0.028	0.062

Figure 4.18: *On-state currents of the transfer curves from figure 4.16 of TTG device D12 from sample SOI29 plotted against temperature for different symmetrical source-drain voltages V_{DS}: (a) for the p-mode and (b) for the n-mode. In addition, the current values and the currents normalized over the width, 0.445 µm ,of the structure are given in tables for temperatures of 295K and 4.5K*

length. Small variations in the effective barrier height or width due to gate coupling can lead to large, exponential changes in the injection current, which explains why device D12 has higher currents despite its longer channel [33, 45, 72]. Furthermore, the drain current in such structures is mainly determined by the effective Schottky-barrier height at the metal-semiconductor interfaces. Variations in this barrier height therefore dominate the observed device-to-device current differences, whereas channel length and carrier mobility play only a minor role in silicon-based SBFETs [33, 41, 45].

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4.1.4.1 Threshold voltage at cryogenic temperatures

Now that we have discussed the transfer characteristics and current values of the devices, the following sections will focus on the other important parameters for transistors measured at cryogenic temperatures. This section discusses and evaluates the threshold voltage V_{th} described in 3.2.5.1. The three measurement setups from 4.1.4 are considered in relation to the source-drain voltage, whereby only one device, namely D38, is considered, as they behave similarly with regard to this parameter. Figure 4.19(a) shows the temperature-dependent change in V_{th} relative to the value at room temperature (295K) (a) for the p-mode and (b) for the n-mode. The values for V_{th} at room temperature referred to are approximately -1.15 V, -1.33 V, and -1.36 V for p-mode, and -0.53 V, -0.46 V, and -0.42 V for n-mode for the respective voltages V_{DS} 1 V, 0.5 V, and 0.2 V. It is clear to see how strongly V_{th} increases in the respective directions as the temperature decreases, and that these shifts become even greater at lower V_{DS}. This dependency on V_{DS} is now shown in figure 4.20. It should be noted that V_{DS} has a different sign here. In conventional MOSFETs, the increase in power consumption at cryogenic temperatures is often linked to a rise in V_{th}, which results from a temperature-dependent shift of the Fermi-level between the dopant energy level and the band edge [2]. For the Si-RFET studied in this thesis, the observed increase in V_{th} can be caused by the reduced number of thermally activated charge carriers available at low temperatures. As the Fermi–Dirac distribution becomes significantly sharper at the metal-semiconductor interface, the onset of conduction shifts to higher gate voltages, which leads to an undesired rise in V_{th} when cooling the device down. For the investigated RFET, threshold-voltage shifts of about 0.25 V in n-mode and -0.35 V in p-mode is extracted between room temperature and 4.5 K at V_{DS} of 1 V. It can also be highlighted that in n-mode figure 4.19(b), all three curves behave like an exponential, which is not really observable for p-mode.

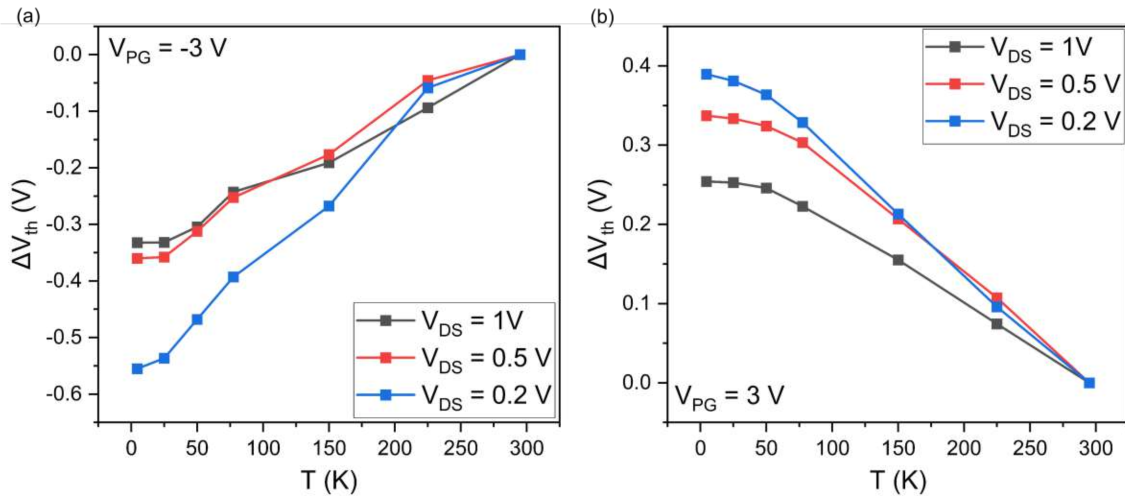

Figure 4.19: *Temperature-dependent change in V_{th} relative to the value at room temperature (295K) against the temperature: (a) p-mode with V_{PG} = -3 V and (b) n-mode with V_{PG} = 3 V ; Evaluation is based on transfer curves with V_{DS} = 1 V, 0.5 V, and 0.2 V and V_{CG} ranges from -3 V to 3 V as a double sweep*

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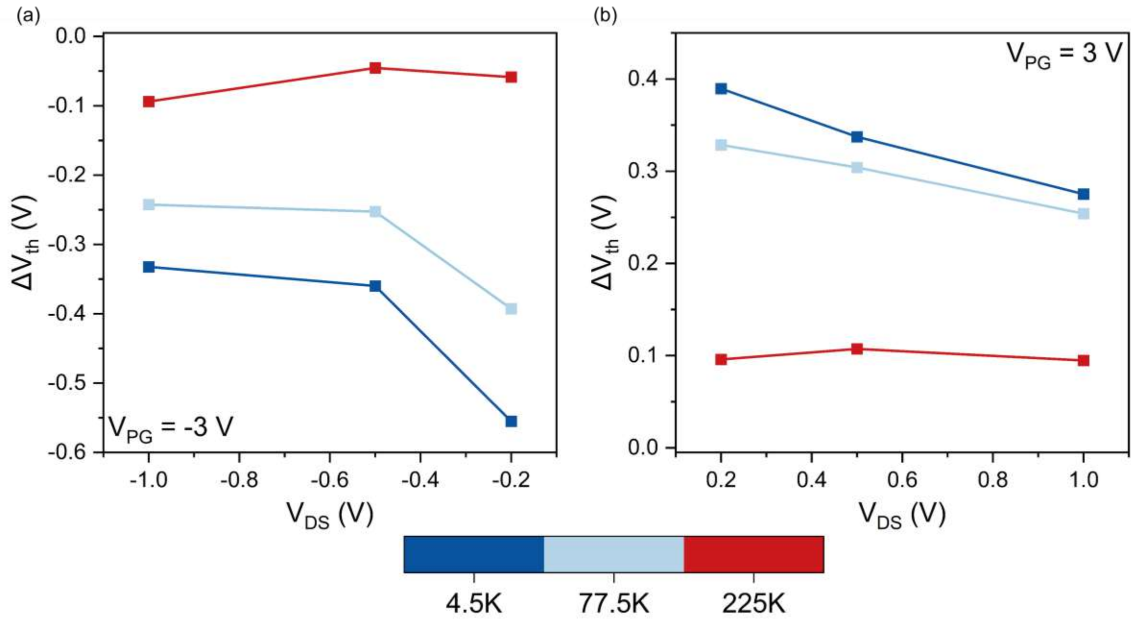

Figure 4.20: *Temperature-dependent change in V_{th} relative to the value at room temperature (295K) against the source-drain voltage V_{DS} = 1 V, 0.5 V, and 0.2 V: (a) p-mode with V_{PG} = -3 V and (b) n-mode with V_{PG} = 3 V; Evaluation is based on transfer curves with V_{CG} ranges from -3 V to 3 V as a double sweep*

4.1.4.2 Subthreshold swing at cryogenic temperatures

The next parameter to be examined for the transfer characteristics is the subthreshold swing STHS, which describes how fast the device switches between the off state and the on state. The evaluation is already described in section 3.2.5.2 and is used to find the steepest slope for the transfer curves in section 4.1.4 for the respective temperatures. As in section 2.1.2.2, there is a thermal limit, $STHS_{ideal} = \frac{k_B T}{q} ln(10)$, which cannot be physically undercut [18]. In MOSFETs, the STHS exhibits a linear dependence on temperature which originates from the electrostatic control of carrier injection from the Boltzmann tail of the Fermi-Dirac distribution. In contrast, SBFETs feature a pronounced barrier in the off-state and are therefore much more sensitive to cryogenic temperatures, since thermionic emission across the Schottky-barrier governs the onset of conduction. The unit of this key property is mV/dec, meaning how much voltage of V_{CG} per current decade is required. For this purpose, the lowest value is determined by the evaluation described above, means at the steepest point of the transfer curve. In order to maintain the scientific aspect, only device D38 is considered here, which was also analyzed for threshold voltage. In figure 4.21, the STHS is plotted against temperature for the respective source-drain voltages V_{DS} of 1 V, 0.5 V, and 0.2 V for (a) the p-mode and (b) the n-mode. In addition, the thermal limit $STHS_{ideal}$ is displayed to provide a reference point. Although SBFETs generally show an off-state that is strongly affected by cryogenic temperatures, as thermionic emission over the Schottky-barrier determines the onset of conduction, the

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extracted STHS displays an almost linear behaviour. It is particularly noteworthy that the device exhibits a fairly symmetric subthreshold slope in both operation modes. The STHS values for room temperature 295 K and 1 V V_{DS} are approximately 80 mV/dec for p-type and 72 mV/dec for n-type. At 4.5 K, STHS values of 24 mV/dec for n-type operation and 27 mV/dec for p-type operation are obtained, indicating that both branches respond similarly under cryogenic conditions. These values highlight that, despite the temperature-sensitive nature of the off-state in SBFETs, the overall subthreshold behaviour remains well structured and comparable between the two charge-carrier injection types. Note that for the n-mode a saturation for low temperatures can be observed.

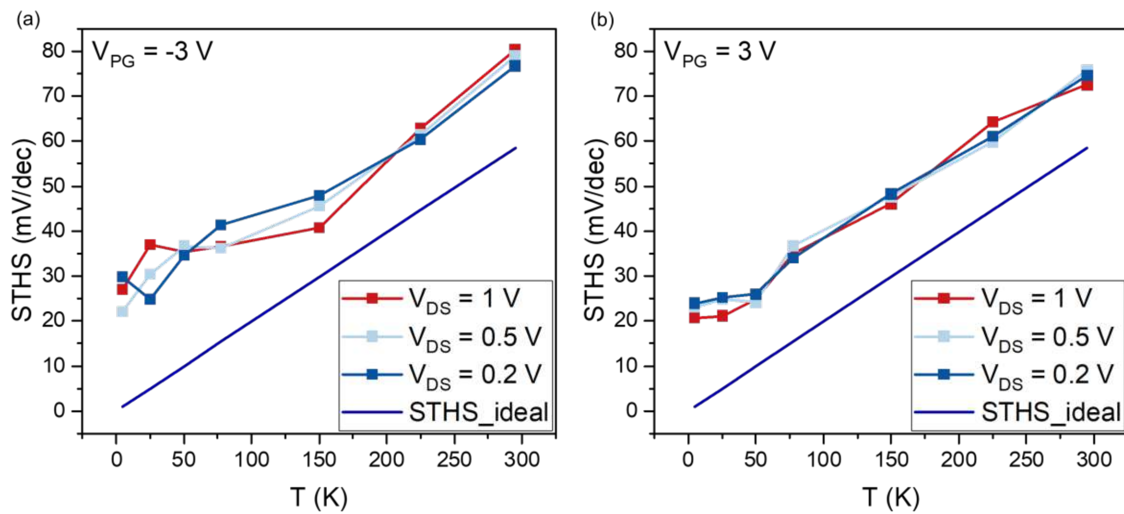

Figure 4.21: *Temperature-dependent change in STHS against the temperature for V_{DS} = 1 V, 0.5 V, and 0.2 V: (a) p-mode with V_{PG} = -3 V and (b) n-mode with V_{PG} = 3 V; Evaluation is based on transfer curves with V_{CG} ranges from -3 V to 3 V as a double sweep*

In addition, figure 4.22 illustrates the temperature-dependent STHS extracted for (a) the p-mode and (b) the n-mode as a function of I_D/W over the full temperature range from 4.5 K to 295 K. From these characteristics, three distinct regimes can be identified that reflect how the behaviour of subthreshold swing evolves with the current level. First, at low current densities up to approximately 0.01 $\mu A/\mu m$, where STHS has its smallest values, marking the region in which the transfer characteristic exhibits its steepest slope. Second, as the current increases into the range between 0.01 $\mu A/\mu m$ and 1 $\mu A/\mu m$, STHS begins to rise steadily. Both of these regimes show a pronounced dependence on temperature, indicating that thermionic emission remains the dominant conduction mechanism in this part of the characteristic. Consistently, STHS decreases as the temperature is lowering, in line with the expected sharpening of the thermally driven carrier distribution. As third regime, currents are exceeding roughly 1 $\mu A/\mu m$, where STHS reaches comparatively high values and exhibits only a weak dependence on temperature. Here the on-state is observed and is consistent with direct tunneling becoming the prevailing conduction mechanism. Here the influence of temperature is significantly reduced. Most notably, both operation modes of the presented Si-RFET show a very similar temperature dependence

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with respect to V_{DS} and STHS. This parallel behaviour indicates that the underlying transport mechanisms respond comparably in the n-type and p-type branches when the device is cooled down, and that both modes are influenced in a consistent manner by variations in source-drain bias and temperature.

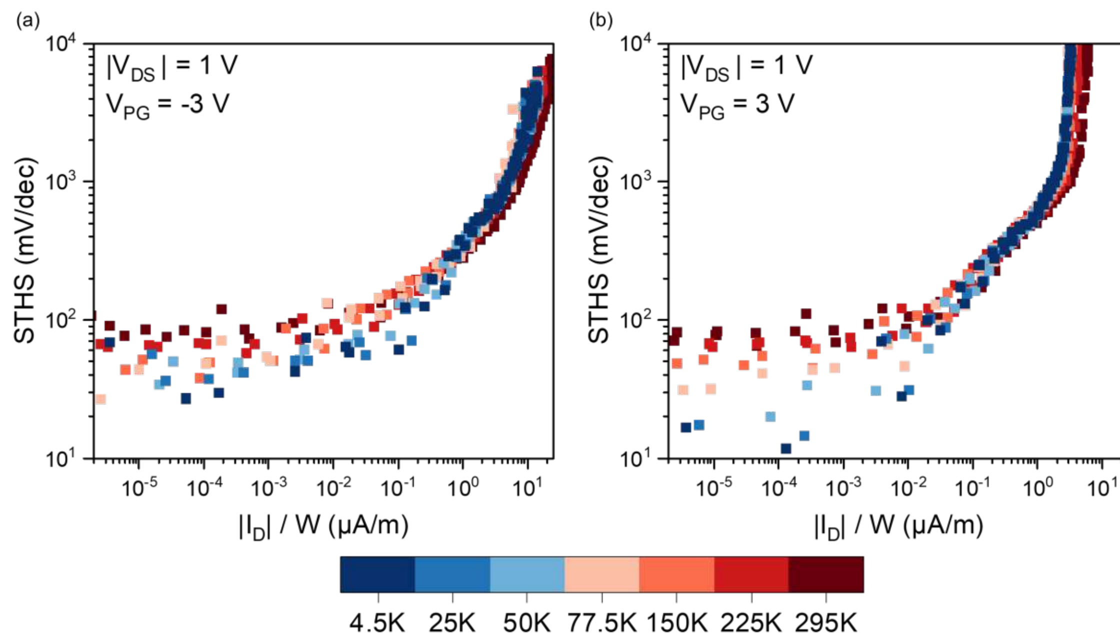

Figure 4.22: *Temperature-dependent change in STHS against the over the width normalised drain current I_D/W for V_{DS} = 1 V: (a) p-mode with V_{PG} = -3 V and (b) n-mode with V_{PG} = 3 V; Evaluation is based on transfer curves with V_{CG} ranges from -3 V to 3 V as a double sweep*

4.1.4.3 Transconductance at cryogenic temperatures

Another important parameter of the devices is the transconductance g_m normalized over the width W of the device, which plays an important role in the evaluation of the threshold voltage, as described in section 3.2.5.1. It describes how effectively a change in gate voltage modulates the drain current and is therefore an important indicator of how strongly the channel responds to the electrostatic control of the top gates. Higher g_m means more efficient charge-carrier injection and a steeper transition in the transfer characteristic, making it an important value for evaluating device performance [59]. This is derived from the first derivative of the absolute drain current I_D of the transfer curves and smoothed using Savitzky-Golay. This smoothing reduces the peak values of the curves slightly, but improves the visibility of the plots. The resulting curves are shown in figure 4.23 for (a) p-mode and (b) n-mode. The highest curve is at room temperature, which is not surprising, since the on-currents are strongest at this temperature. The values for lower temperatures are smaller and their peaks are shifted to the right for p-mode and to the -left for n-mode. This is also not surprising, since the threshold voltage V_{th} changes in exactly these directions, as described in section 4.1.4.1. The somewhat noisy drops in the curves represent the onstates of the transfer characteristics, whereas the very smooth

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rises show the switching of the device. This phenomenon is a strong indication that these Al-Si heterostructures are highly transparent (quasi-ohmic) [73]. Furthermore, figure 4.24 shows the dependence of the peaks for g_m on the source-drain voltage for (a) p-type and (b) n-type. In this plot, the values are not smoothed and are therefore displayed accurately. This dependency is clearly visible for all three temperatures, and the values decrease significantly. For a bias voltage V_{DS} of 1 V, g_m decreases for the p-mode from 18.2 $\mu S/\mu m$ at 295 K to 11.5 $\mu S/\mu m$ at 4.5 K, or from 3.8 $\mu S/\mu m$ to 0.81 $\mu S/\mu m$ at a voltage of 0.2 V. Furthermore, for n-mode, g_m changes from 6.9 $\mu S/\mu m$ at 295 K to 4.1 $\mu S/\mu m$ at 4.5 K for a voltage of 1 V, and from 0.85 $\mu S/\mu m$ to 0.19 $\mu S/\mu m$ for voltages of 0.2 V. The fact that the values for n-mode are lower than for p-mode can again be explained by the lower on-state currents.

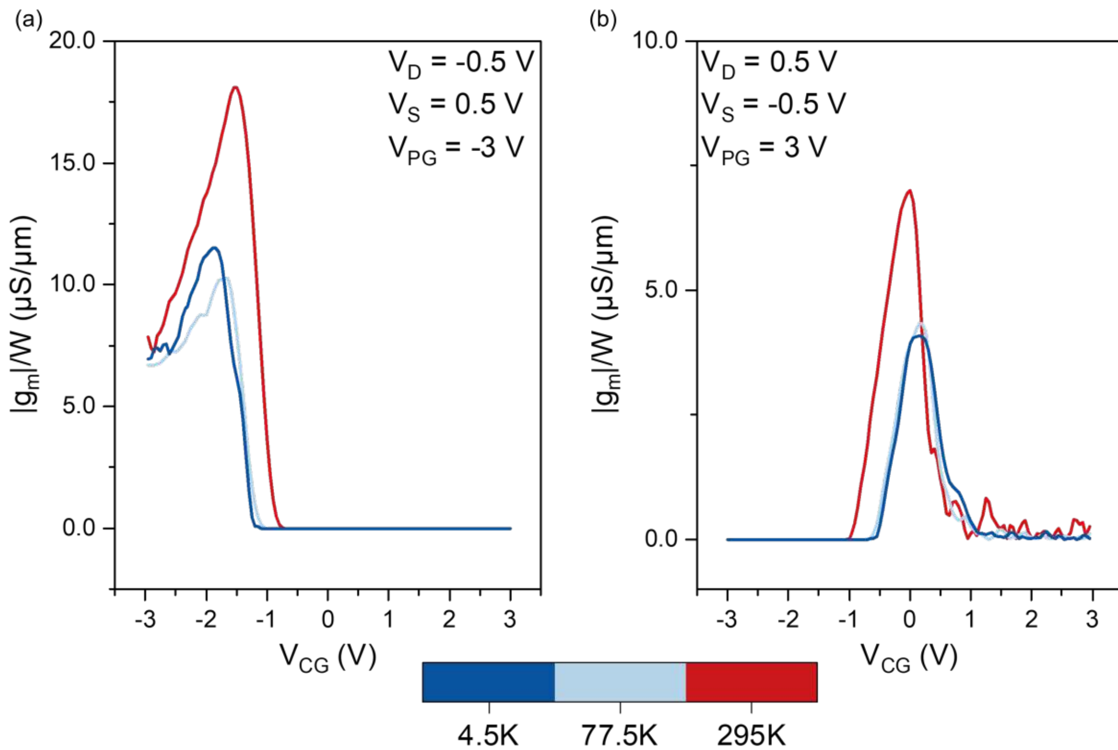

Figure 4.23: *Temperature-dependent change in transconductance g_m against control gate voltage V_{CG} with V_{DS} = 1 V, 0.5 V, and 0.2 V: (a) p-mode with V_{PG} = -3 V and (b) n-mode with V_{PG} = 3 V; Evaluation is based on transfer curves with V_{CG} ranges from -3 V to 3 V*

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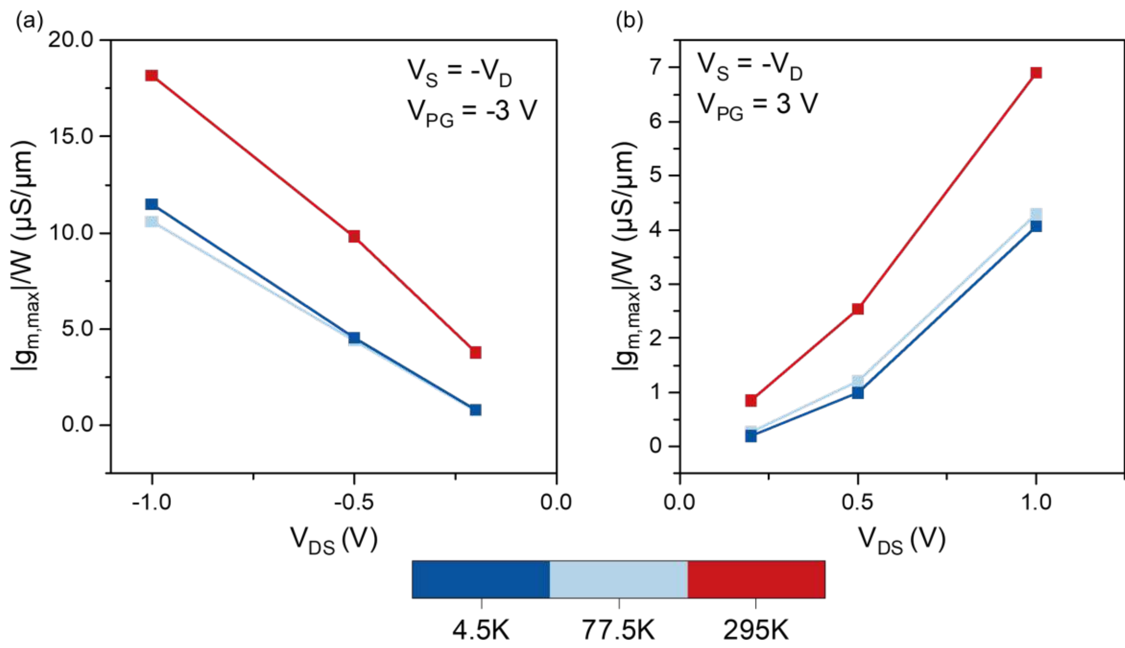

Figure 4.24: *Temperature-dependent change in transconductance g_m against source-drain bias voltage V_{DS} = 1 V, 0.5 V, and 0.2 V: (a) p-mode with V_{PG} = -3 V and (b) n-mode with V_{PG} = 3 V; Evaluation is based on transfer curves with V_{CG} ranges from -3 V to 3 V*

4.2 SiGeSn SBFET

Now that Si-based devices have been discussed in detail, the second part of this chapter is dedicated to SiGeSn transistors. The unique property of changing the band gap with the composition of these alloys has already been described in section 2.3, while the structure and fabrication have already been covered in section 3.1.2. The following section examine a transistor with a composition of 33% Si, 66% Ge, and 0.5% Sn, i.e., $Si_{0.33}Ge_{0.66}Sn_{0.005}$. Unlike Si-based devices, this material system is expected to exhibit a improvement in threshold voltage during cooling. Figure 4.25 shows the structure of this device as (a) a coloured scanning electron microscopy (SEM) image of the fabricated SiGeSn SBFET, while a schematic cross-section in (b) of the channel-oxide stack to provide a clearer view of the layer arrangement. Subfigure (c) displays an energy-dispersive X-ray spectroscopy (EDX) map of the left source-channel interface to verify the material composition in the source and drain regions. The EDX analysis confirms that the vertical Si-SiGeSn-Si heterostructure remains intact throughout the exchange process, with no visible mixing of the epitaxial layers, moreover the monolithic Al contacts appear crystalline[63]. The semiconductor channel has a length of 1.8 μm and is 180 nm wide. It should be noted that this device, despite of having multiple gate electrodes, is not an RFET and therefore does not have the ability to provide two proper modes for charge carrier injection. Here, the hole current is dominant, making it a P-SBFET, as the material system blocks electrons through increased barriers. This behaviour can be attributed to the pronounced Fermi-level pinning near the valence band, together with the vertical Si-SiGeSn-Si heterostructure, which very likely leads to the formation of a hole gas due to the abrupt band discontinuities at the interfaces [30]. Even though the structure of the top gates is similar to the TTGs of Si-based RFETs, in these transistors, the program gate is instead a junction gate (JG), as it only effectively lowers the Schottky barriers for the holes and blocks charge-carrier injection for electrons.

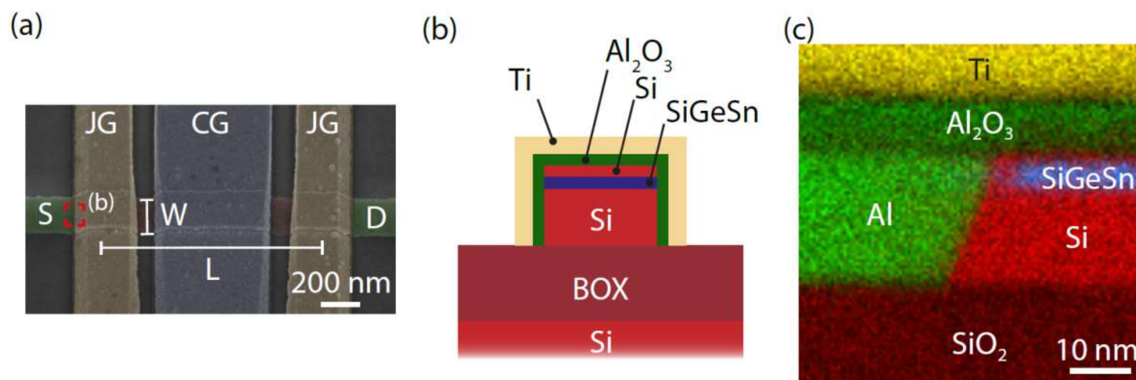

Figure 4.25: *(a) Coloured SEM image of the SiGeSn SBFET with a channel length of L = 1.8 µm and a channel width of W = 180 nm. (b) Schematic cross-section of the device illustrating the channel-oxide stack. (c) TEM cross-section with EDX elemental mapping of the metal-semiconductor interface, showing the Al-Si-SiGeSn multi-heterojunction [64].*

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4.2.1 Transfer characteristics - SiGeSn SBFET

As with Si-based devices, the performance of the SiGeSn SBFET is first examined at room temperature in vacuum. For this purpose, as shown in Figure 4.26(a), the transfer characteristics of the device are measured for different source-drain voltages V_{DS} of 2 V, 1.5 V, 1 V, and 0.5 V. The voltage at the junction gate V_{JG} is -3 V, and that of the control gate V_{CG} is swept between -3 and 3 V as a double sweep. It is immediately apparent that this structure behaves completely differently from those already discussed, as a curve requires the entire range of V_{CG} to switch from off- to on-state. Furthermore, a dependence on V_{DS} for the current strength of the on- and off-currents can be seen, which is illustrated in subfigures (b) and (c). As bias voltages decrease, I_{on} and I_{off} decrease, with the off-state much more sharply, thus improving the I_{on} /I_{off} ratio at lower bias voltages. The exact values for this development are given in table 4.4, whereby it is noticeable that the values correspond very well with the respective V_{DS}. The large on-state currents are most likely enabled by the high contact transparency of the proposed Al-Si-SiGeSn source/drain-channel junctions for hole injection, combined with the previously discussed hole gas formation induced by the vertical Si-SiGeSn-Si heterostructure. The current for the on-state has increased almost linearly at 2 V to about four times the value of 0.5 V and a linear fit is shown in subsection (b). For the off-state, an exponential increase from 0.5 V to 2 V V_{DS} can be seen, which can be very well demonstrated with the fit in subfigure (c). It should also be noted that the threshold voltage V_{th} sees a positive shift for lower bias voltages, and the curves become somewhat steeper, meaning that STHS decreases. Additionally, a hysteresis can be observed in the measured characteristics, which becomes more pronounced for decreasing V_{DS}. One possible reason is that at lower V_{DS} the lateral electric field is weaker, so charge trapping and detrapping at oxide/interface states become slower, which can make the forward and reverse sweeps differ more strongly [33, 59]. Such behaviour is consistent with reports on Schottky-barrier nanowire FETs, where charge trapping at oxide-semiconductor interface states leads to a bias-dependent hysteresis in both sweeps [41]. It should be noted that these transistors do not require a passivation or capping layer for these measurements, which might be related to the SiGeSn layer being capped by Si and the respective hole gas at the Si-SiGeSn interface.

V_{DS} (V)	I_{on} (μA)	I_{off}(pA)	I_{on}/I_{off}
2 V	17.48	979.05	$1.785{\cdot}10^4$
1.5 V	13.58	301.33	$4.507{\cdot}10^4$
1 V	9.424	94.81	$9.94{\cdot}10^4$
0.5 V	4.763	25.11	$1.897{\cdot}10^5$

Table 4.4: *On- and off-state currents I_{on} and I_{off} values for curves in figure 4.26*

4.2.2 Output characteristics - SiGeSn SBFET

For the sake of completeness, this section shows the output characteristic of the SiGeSn SBFET, as has already been done for Si-based devices. The principle of section 3.2.3 is applied again for this purpose, and figure 4.27 shows precisely this characteristic curve all

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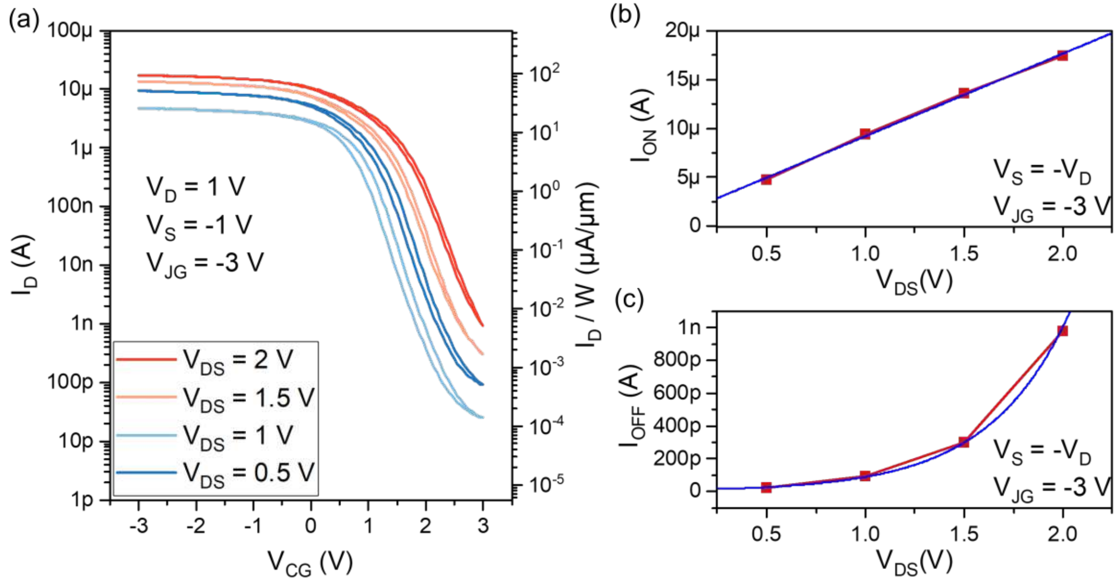

Figure 4.26: *(a) Double sweep transfer characteristics SiGeSn SB-FET for different source-drain voltages at 295K in vacuum: V_{JG} = -3 V, V_{CG} ranges from -3 V to 3 V, V_{DS} = 2 V, 1.5 V, 1 V, and 0.5 V (b) relating on-state currents I_{on} with a linear fit and (c) relating off-state currents I_{off} with a exponential fit*

in vacuum at room temperature. The bias voltage V_{DS} is applied symmetrical and swept from -2 V to 2 V for different voltages on CG, changed from -3 V to 3 V in 0.5 V steps. As mentioned above, this device only has one p-mode, so only one output is recorded, and the voltage at the junction gate V_{JG} is -3 V. It is easy to see that the currents quickly become the on-state currents in the transfer curves of section 4.2.1 as the V_{CG} increases. This increase is non-linear, as has already been observed for Si-based devices. At a voltage V_{CG} of -0.5 V or higher, the on-states are already at the desired level for the bias voltage of 2 V.

4.2.3 SiGeSn SBFET at cryogenic temperatures

Since the room temperature measurements of the SiGeSn SBFET appear promising, the following discussion focuses on their behavior at cryogenic temperatures. For this purpose, the sample is first cooled down to approximately 4.5 K and then gradually brought back to room temperature (295 K). As described in section 3.2.1, this is done using liquid helium and nitrogen. In order to analyze the most important parameters of the device again, transfer characteristics for the respective temperatures are recorded, which can be seen in figure 4.28. Curves are shown for the four source-drain voltages V_{DS} of (a) 2 V, (b) 1.5 V, (c) 1 V, and (d) 0.5 V for different temperatures. When the device is cooled from room temperature down to approximately 5 K, the transfer characteristics become noticeably steeper and the threshold voltage shifts to the left. While the on-currents remain essentially unchanged, the the off-currents decrease progressively and reach the noise level of the measurement system at 150 K. This behaviour can be explained by the temperature-

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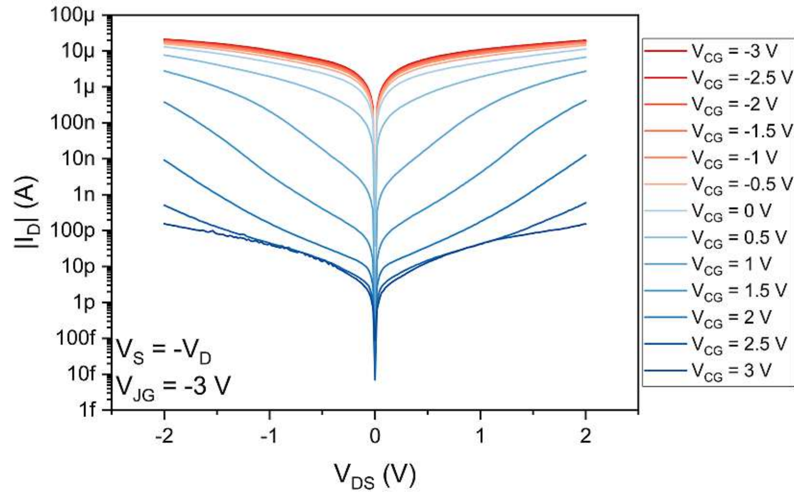

Figure 4.27: *Output characteristics of SiGeSn SBFET in vacuum at roomtemperature for contol-gate voltage range V_{CG} of -3 V to 3 V in 0.5 V steps: Bias-voltage V_{DS} is applied symmetrically and is swept from -1 V to 1 V ; Junction-gate voltage V_{JG} = -3 V*

dependent sharpening of the Fermi-Dirac distribution, which affects the carrier injection at the metal-semiconductor junction and leads to the observed improvements for the STHS. In subfigures (e) and (f), the corresponding I_{on} and I_{off} of the curves are plotted over the source-drain voltage V_{DS}. Importantly, as already discussed, the off-current falls below the resolution limit of the measurement setup (40 fA) for temperatures of 150 K, making it no longer detectable in this regime. Whereas, it becomes clear that for temperatures above 150 K, the off-current increases with higher V_{DS}. This behaviour is mainly attributed to the enhanced generation of thermally activated carriers, together with additional barrier thinning at the metal-semiconductor junctions under increased drain bias. In the on-state, their consistency is evident at all temperatures. The on-state current at 5 K for V_{DS} = 2 V is 16.19 μA, which results in an I_{on}/I_{off} ratio of approximately $1.6{\cdot}10^{-9}$, which is an improvement of nearly 5 orders of magnitude.

4.2.3.1 Threshold voltage at cryogenic temperatures

Now that we have discussed the transfer characteristics and current values of the SiGeSn SBFET, the following sections will focus on the other key parameters for transistors measured at cryogenic temperatures, like for the Si-TTGs. This section analyzes and evaluates the threshold voltage V_{th} described in 3.2.5.1. For this purpose, the values determined for V_{th} of the curves from 4.2.3 are plotted in figure 4.29(a) against temperature and in (b) against the source-drain voltage. In both plots, V_{th} gradually improves as the temperature is reduced. For V_{DS} = 2V a drop from 1.325 V at 295K to 1.034 V is achieved, which is roughly a improvement of 25%. The dependency on the applied drain bias is shown when investigating the values with V_{DS} = 0.5 V, where the improvement is from 0.929 V to 0.461 V, means about 50%. As can be seen in both plots, the values from 75K onwards do not differ greatly for lower temperatures for the respective bias and saturate at a certain

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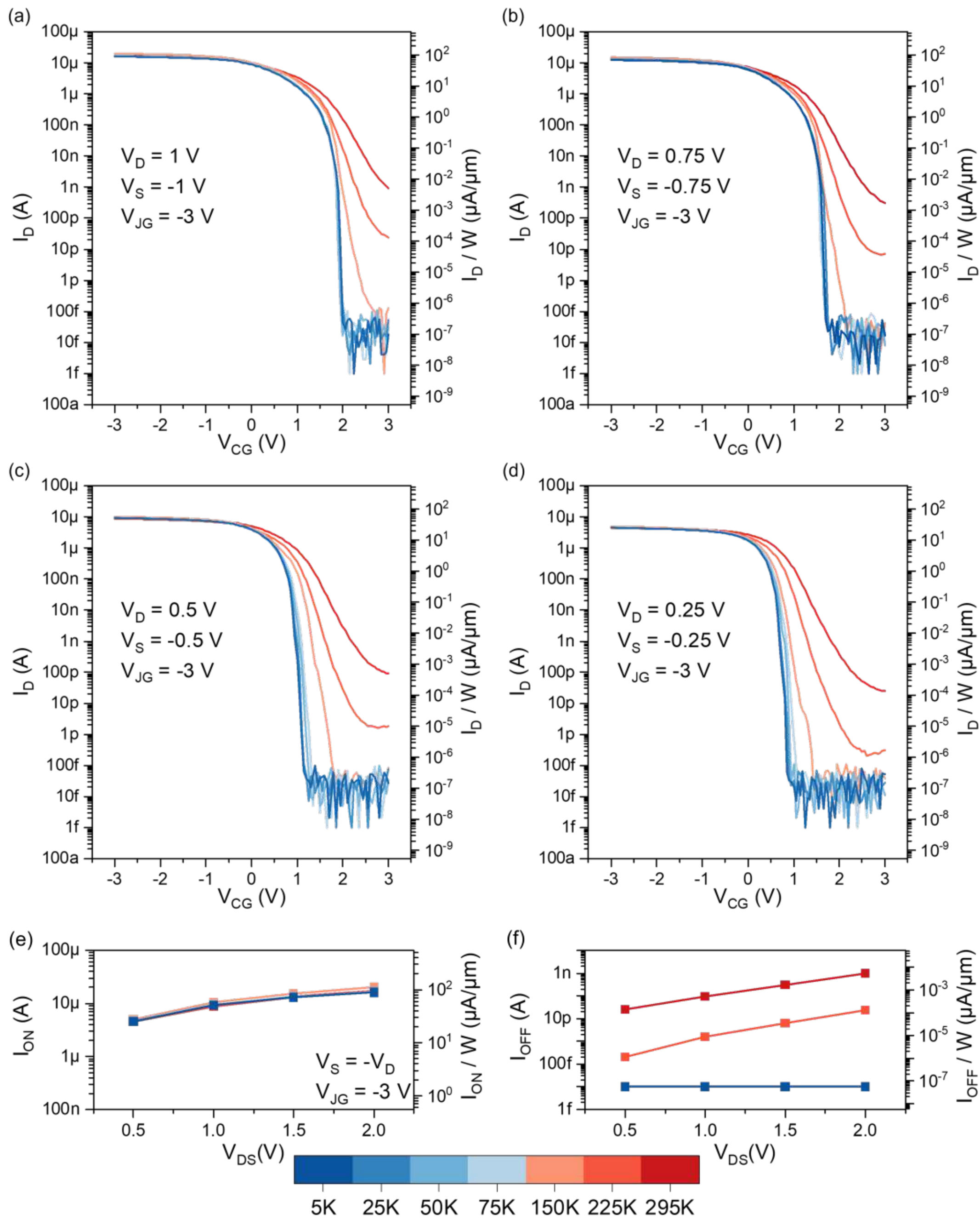

Figure 4.28: *Transfer characteristics of SiGeSn SBFET for different temperatures and different symmetrical source-drain voltages: (a) V_{DS} = 2 V, (b) V_{DS} = 1.5 V,(c) V_{DS} = 1 V and (d) V_{DS} = 0.5 V; Gate-voltage V_{CG} is swept from -3 V to 3 V and junction-gate voltage is held constant at -3 V. In additon (e) shows the relating on-state currents I_{on} and (f) the relating off-state currents I_{off}.*

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value. A reason for the improvement lies in the fabricating process, as the Al_2O_3 layer partially oxidises the underlying Si surface. It creates a SiO_2/Al_2O_3 interface that introduces negative fixed oxide charges and lead to a positive shift [61]. These negative fixed oxide charges could also be a reason why no passivation layer is required for these transistors. Another possible explanation for the improvement of V_{th} is the temperature-induced band gap widening of the semiconductor materials, as discussed in section 2.1.2.1. Please note that improvement here refers to a shift toward zero, as less voltage is required at the control gate to reach the on state. If, as with Si-based devices for p-mode, the voltage shifts more toward negative, this is a worsening, even though V_{th} changes in the same direction.

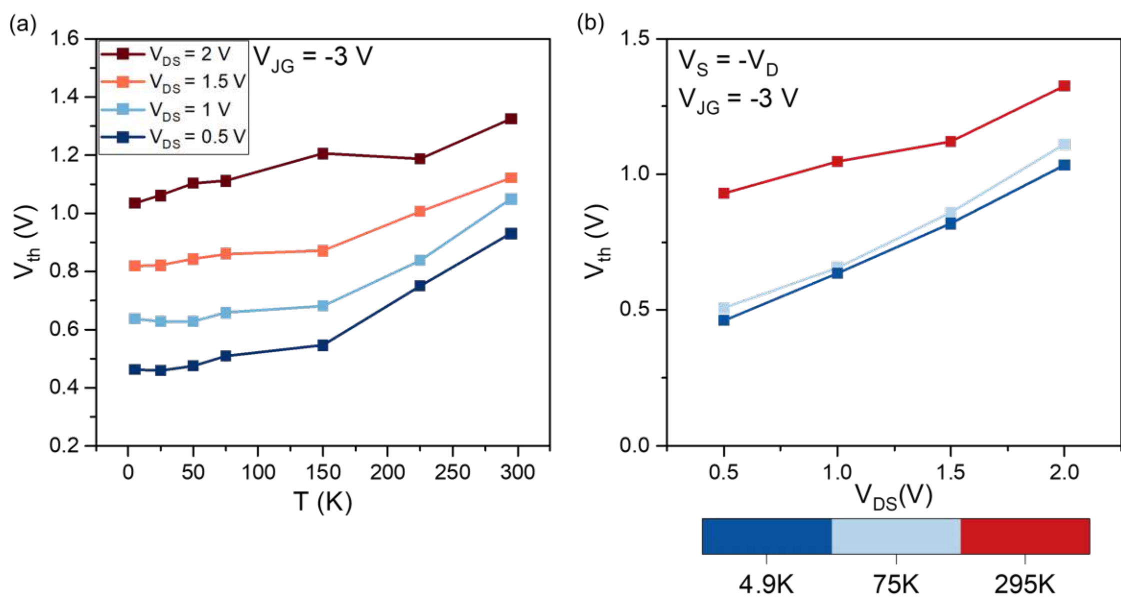

Figure 4.29: *Temperature-dependent change in V_{th} in (a) against the temperature and in (b) against the source-drain voltage with V_{JG} = -3 V. Evaluation is based on transfer curves of 4.28 with V_{DS} = 2 V, 1.5 V, 1 V and 0.5 V. V_{CG} ranges from -3 V to 3 V.*

4.2.3.2 Subthreshold swing at cryogenic temperatures

The next key parameter for the SiGeSn SBFET is the subthreshold swing STHS, which describes how fast the transistor switches from the off state to the on state. The evaluation is already described in sections 3.2.5.2 and 4.1.4.3. The STHS is plotted against the temperature for the respective source-drain voltages V_{DS} of 2 V, 1.5 V, 1 V and 0.5 V in figure 4.30(a), where again the thermal limit $STHS_{ideal}$ is displayed to provide a reference point. In contrast to Si-RFETs, which had almost a linear behavior, a exponential improvement is achieved. For V_{DS} = 2 V, the STHS value is 352.6 mV/dec for 295 K and 23.3 mV/dec for 5 K, whereas for V_{DS} = 0.5 V, the values determined are 310.8 mV/dec and 34.2 mV/dec. This is interesting because, apparently, the curve with the higher bias becomes steeper than the one with the lower bias at a certain point in contrast to the curves at 295 K. Precisely because of this phenomenon, figure 4.30(b) shows this

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dependency, means STHS is plotted against the source-drain voltage. It is evident that there is a turning point at the measurement for the 150 K temperature. The reason why the curves become steeper is the same as for Si-RFETs, with pronounced barriers in the off state, making the device much more sensitive to cryogenic temperatures, since thermionic emission across the Schottky-barrier determines the onset of conduction. The values for 5 K are comparable for both devices, but the SiGeSn SBFET requires twice the source-drain voltage. The value for 1 V V_{DS} is 32.3 mV/dec, which is slightly higher than the 24 mV/dec achieved for n-type operation and 27 mV/dec for p-type operation of the Si-TTG. In the range from 5 K to 50 K for figure 4.30(a) , saturation can be observed in the values, which remain relatively constant above 20 mV/dec. This behaviour may be attributed to band-tail effects, which can arise from two distinct contributions [2]. First, Gaussian-distributed localized states, which introduce an inflection and thereby degrade the STHS, as observed around 150 K. Second, an exponentially decreasing density of mobile states, which ultimately leads to the saturation of STHS at lower temperatures. Figure 4.31 illustrates the extracted temperature-dependent STHS as a function of I_D/W

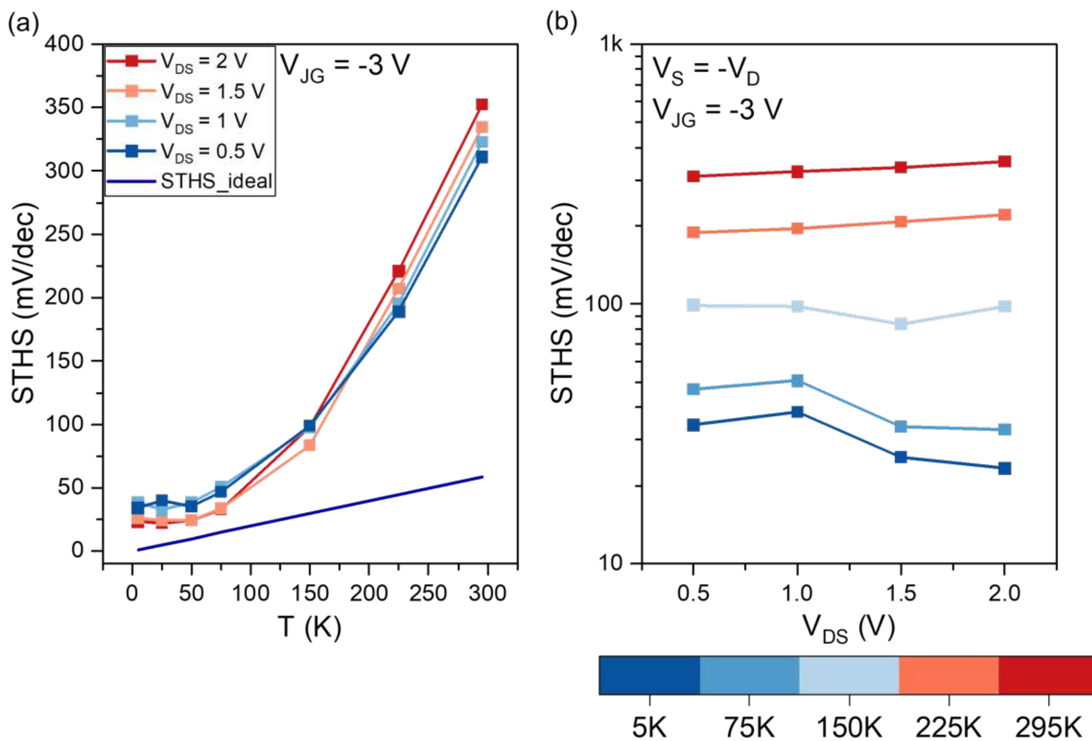

Figure 4.30: *Temperature-dependent change in STHS (a) against the temperature and (b) against the source-drain voltages with V_{JG} = -3 V. Evaluation is based on transfer curves of 4.28 with V_{DS} = 2 V, 1.5 V, 1 V and 0.5 V. V_{CG} ranges from -3 V to 3 V.*

for all temperatures and a V_{DS} of 1 V. From these characteristics, several regimes can be distinguished. In the TE-dominated regime at currents approxiamtely 0.5 $\mu A/\mu m$, the STHS remains nearly constant at its minimum value for temperatures below 150 K,

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corresponding to the steepest part of the transfer curve. For temperatures above 150 K, the STHS increases, which can be attributed to the flattening of the transfer characteristic in the off-state. At higher currents, the STHS rises again strongly, indicating that direct tunneling becomes the dominant transport mechanism in the on-state of the device.

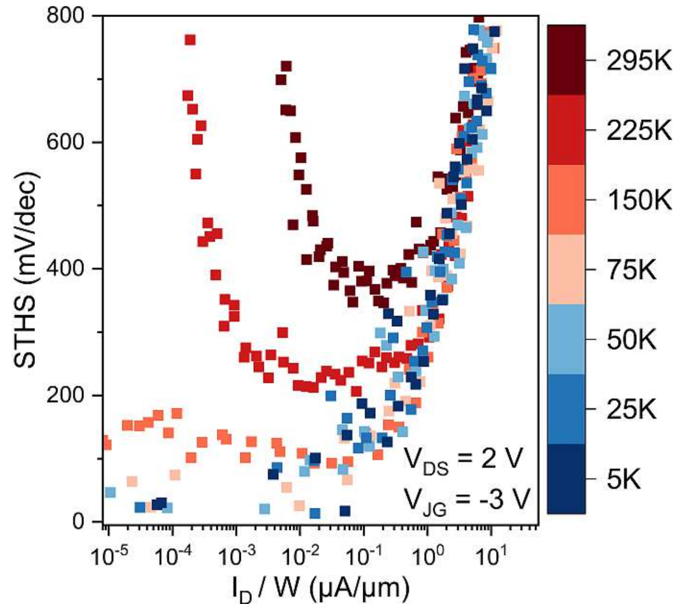

Figure 4.31: *Temperature-dependent change in STHS against the over the width normalised drain current I_D/W for V_{DS} = 2 V, 1.5 V, 1 V and 0.5 V: (a) p-mode with V_{PG} = -3 V and (b) n-mode with V_{PG} = 3 V; Evaluation is based on transfer curves with V_{CG} ranges from -3 V to 3 V.*

4.2.3.3 Transconductance at cryogenic temperatures

The last parameter for SiGeSn SBFETs to be analyzed is the transconductance gm normalized over the width W of the device. Like for the Si-RFETs, it is derived from the first derivative of the absolute drain current I_D of the transfer curves and smoothed using Savitzky-Golay, which reduces the peak values of the curves slightly. The resulting curves for temperatures of 295 K, 75 K and 5 K are shown in figure 4.32(a). The noisy drops in the curves represent the onstates of the transfer, whereas the very smooth rises show the switching of the device. At room temperature, a peak of approximately 40.8 $\mu S/\mu m$ is found, which is more than double that of the p-mode for Si-RFET. But here, the device behaves quite differently, as g_m increases with decreasing temperature. In figure 4.32(b), g_m/W is plotted against the source-drain voltage and has nearly a linear behavior. The transconductance yields a peak value of approximately 46 $\mu S/\mu m$ at 5 K, which is about four times that of the Si-RFET, but with doubled drain bias. For V_{DS} of 1 V, 32.3 $\mu S/\mu m$ are achieved, which is less than three times. Figure 4.33 shows the curves for 295 K for all drain biases, which have interestingly all the same decrease after the peaks. This behaviour is rather unusual, as such a degradation is typically observed only in SBFETs that exhibit well-defined barriers under specific bias conditions [73]. The fact

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that this effect appears consistently across all measured conditions strongly suggests that the Al-Si-SiGeSn multi-heterojunctions behave like pure Al-Ge junctions [74] and have a high transparency. It can be regarded as quasi-ohmic contacts, no like the Si-RFETs from the previous chapter that have higher extent of thermionic emission contributing to their transport.

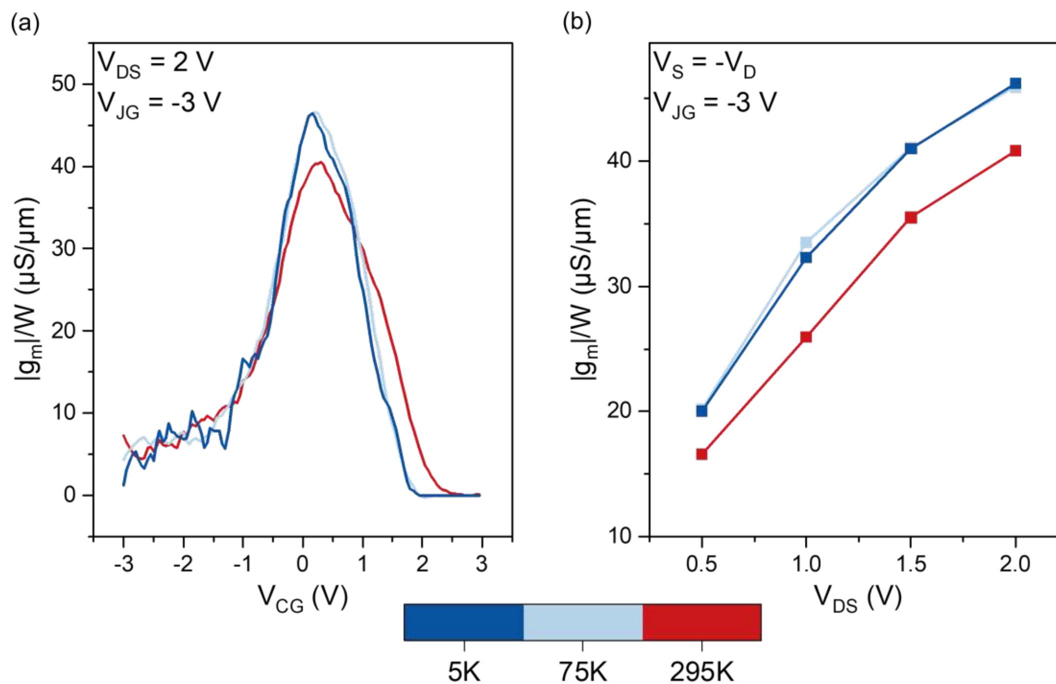

Figure 4.32: *Temperature-dependent change in transconductance g_m (a) against control-gate voltage V_{CG} and source-drain voltage V_{DS} = 2 V, (b) against V_{DS} with curves for 2 V, 1.5 V, 1 V and 0.5: V_JG = -3 V; Evaluation based on transfer curves with V_{CG} ranges from -3 V to 3 V*

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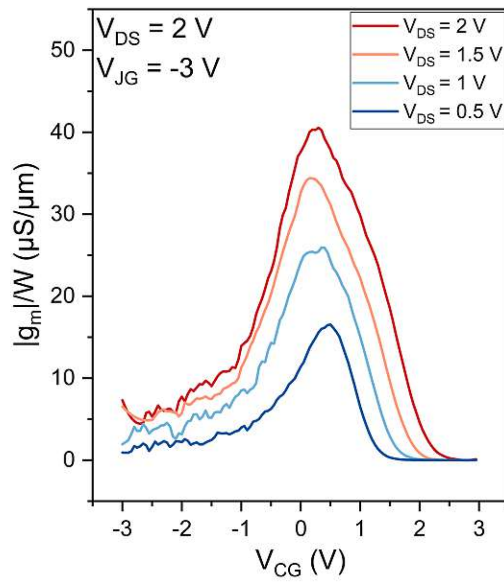

Figure 4.33: *Temperature-dependent change in transconductance g_m against control-gate voltage V_{CG} for source-drain voltage V_{DS} = 2 V, 1.5 V, 1 V and 0.5: V_JG = -3 V; Evaluation based on transfer curves with V_{CG} ranges from -3 V to 3 V*

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Chapter 5

Conclusion

In this thesis, Schottky-barrier based transistor concepts were experimentally investigated with a particular focus on their behaviour at cryogenic temperatures. The work addressed key limitations of conventional doped CMOS technologies at low temperatures by analysing alternative device architectures that rely on metal-semiconductor junctions for carrier injection. Silicon-based reconfigurable field-effect transistors (RFETs) and a complementary SiGeSn-based Schottky-barrier transistor, composition of 33% silicon, 66% germanium, and 0.5% tin, were investigated between room temperature and cryogenic temperatures, down to 4.5 K.

For the Si RFETs, stable operation was demonstrated for both n-mode and p-mode over the entire investigated temperature range. Upon cooling, a strong improvement of the subthreshold swing was observed for both operation modes. At 4.5 K, STHS values of 24 mV/dec for n-type and 27 mV/dec for p-type operation were extracted, indicating steep and a largely symmetrical switching behaviour. An analysis of the current-dependent STHS reveals distinct transport regimes, where thermionic emission dominates the subthreshold region at small values for STHS and tunneling processes increasingly govern the on-state at cryogenic temperatures. Despite the favourable subthreshold behaviour, the temperature dependence of the threshold voltage represents a central challenge for the investigated Si RFETs. With decreasing temperature, the threshold voltage shifts in the undesirable directions for both operation modes. This results in moving the onset of conduction away from the desired operating point. For a drain bias of $V_{DS} = 1$ V, shifts of approximately 0.25 V in n-mode and -0.35 V in p-mode were extracted between 295 K and 4.5 K. While a back-gate bias could be used to partially compensate for these shifts and centre the operating window, this approach is considered more of a workaround than a fundamental solution, as it does not eliminate the underlying temperature sensitivity of the threshold voltage.

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Furthermore, a SiGeSn-based Schottky-barrier transistor was investigated using the same architecture for the gates, but this device only operates in p-mode. Similar to the silicon devices, the SiGeSn SBFET exhibits a pronounced improvement of the subthreshold characteristics at cryogenic temperatures, including a strong suppression of the off-state current and the steep subthreshold swing. Here a STHS of approximately 23 mV/dec was extracted for $V_{DS} = 2$ V, while increasing for smaller source-drain voltages. Importantly, in contrast to the Si RFETs, the threshold voltage of the SiGeSn device improves upon cooling. Depending on the applied drain bias, threshold-voltage reductions of approximately 25% and 50% were extracted when comparing room temperature to 5 K. This behaviour indicates that the cryogenic threshold-voltage behavior is strongly influenced by the channel material system and the gate-stack structure, rather than being an inherent property of Schottky-barrier devices alone.

Overall, the results demonstrate that SBFETs and RFETs offer clear advantages for cryogenic electronics, particularly with respect to robust low-temperature operation and strongly improved subthreshold behaviour. At the same time, the findings highlight that achieving favourable threshold-voltage behaviour at cryogenic temperatures remains a key challenge for Si RFETs. Consequently, future work should focus on targeted electrostatic optimization, for example through the use of high-k gate dielectrics and improved oxide interfaces. In addition, exploring alternative channel materials beyond pure silicon, such as the SiGeSn or other related group-IV alloys, appears to be a promising path toward reducing the temperature sensitivity of the threshold voltage while maintaining the steep switching characteristics. In summary, this thesis provides a comprehensive experimental assessment of cryogenic Schottky-barrier transistors and identifies their potential and limitations. The combination of reconfigurable device concepts with advanced material systems emerges as a great approach for future low-power cryogenic electronic circuits, provided that threshold-voltage behavior is further improved.

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