TECHNISCHE
UNIVERSITÄT
WIEN

Master's Thesis

Adaptive Analog and Digital Circuits based on Reconfigurable Germanium Transistors

submitted in partial fulfillment
of the requirements of the degree of
Master of Science

at Technische Universität Wien
Institute of Solid State Electronics

under supervision of
Univ.Prof. Dipl.Ing. Univ. Dr.-Ing. Walter Michael Weber
and
Privatdoz. Dipl.-Ing. Dr.techn. Masiar Sistani, BSc

by
Daniel Popp, BSc
Student ID 11802457

Vienna, January 2026

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU WIEN Bibliothek Your knowledge hub

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.

Statutory Declaration

I declare, that I have authored the present work independently according to the code of conduct, that I have not used other than the declared sources and that I have explicitly marked all material quoted either literally or by content from the used sources. This work was not yet submitted to any examination procedure neither in Austria, nor in any other country.

Erklärung zur Verfassung der Arbeit

Hiermit erkläre ich, dass die vorliegende Arbeit gemäß dem Code of Conduct – Regeln zur Sicherung guter wissenschaftlicher Praxis – ohne unzulässige Hilfe Dritter und ohne Benutzung anderer als der angegebenen Hilfsmittel, angefertigt wurde. Die aus anderen Quellen direkt oder indirekt übernommenen Daten und Konzepte sind unter Angabe der Quelle gekennzeichnet. Die Arbeit wurde bisher weder im In- noch im Ausland in gleicher oder in ähnlicher Form in anderen Prüfungsverfahren vorgelegt.

Vienna, January 2026

....

Daniel Popp, BSc

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU WIEN Bibliothek Your knowledge hub

Abstract

Reconfigurable field effect transistors (RFETs) based on Schottky contacts offer polarity control enabling runtime NMOS/PMOS switching without channel doping and therefore represent a promising device concept for compact, adaptive, and energy efficient electronic systems. Germanium on silicon on insulator (GeSOI) provides improved carrier injection but requires optimized contact engineering to achieve symmetric electron and hole injection. This work investigates the technological evolution, electrical behavior, and circuit functionality of the second and third generation of Al-Si-Ge multi-heterojunction RFETs based on the GeSOI platform.

The study combines fabrication improvements with an extended characterization methodology. Solid-state exchange based Al-Si-Ge multi-heterojunction contacts and a SiO_2/ZrO_2 gate stack were implemented to improve symmetry and electrostatic control. Automated DC and transient measurements, including multidimensional large parameter sweeps, were performed to evaluate transfer characteristics, on-to-off ratios, temperature stability, and circuit performance. Several circuit configurations were realized, including complementary inverters, common source and common drain amplifiers, and a reconfigurable transmission gate.

The results show a clear progression from the first generation devices toward symmetric and high performance RFET circuits. The third generation achieves nearly balanced conduction in both, the NMOS and PMOS mode, with I_{on}^{p}/I_{on}^{n} improving from 4.1 in the first generation to ≈ 0.88 and on-to-off ratios of approximately six decades. Common source amplifier gains increased from near unity in early devices to values around 10 in the third generation, while common drain gains reached up to 0.75 with stable operating points. The transmission gate demonstrates correct bidirectional switching, tunable attenuation, and reproducible transient behavior, with an effective resistance adjustable from the $G\Omega$ to the 100 $k\Omega$ range.

These findings establish the third generation GeSOI RFET as a robust platform for reconfigurable analog and mixed signal circuits. The demonstrated gain tunability, symmetric operation, and bidirectional transmission capability highlight the versatility of RFET based architectures. Remaining challenges include charge trapping effects and limited dynamic performance, which may be addressed through improved passivation, optimized dielectrics, and enhanced measurement integration. The results provide a foundation for the development of more complex reconfigurable circuits and adaptive electronic systems based on RFET technology.

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU WIEN Bibliothek Your knowledge hub

Kurzfassung

Rekonfigurierbare Feldeffekttransistoren (RFETs) auf Basis von Schottky-Kontakten bieten eine Polaritätssteuerung ohne Kanaldotierung, die ein NMOS/PMOS-Umschalten während der Laufzeit ermöglicht, und stellen daher ein vielversprechendes Bauelementkonzept für kompakte, adaptive und energieeffiziente elektronische Systeme dar. Germanium auf Silizium auf Isolator (GeSOI) bietet eine verbesserte Ladungsträgerinjektion, erfordert jedoch eine optimierte Kontakttechnik, um eine symmetrische Elek- tronen- und Lochinjektion zu erreichen. Diese Arbeit untersucht die technologische Entwicklung, das elektrische Verhalten und die Schaltungsfunktionalität der zweiten und dritten Generation von Al-Si-Ge Multi-Heterojunction-RFETs auf Basis der GeSOI-Plattform.

Die Arbeit kombiniert Verbesserungen auf Fertigungsebene mit einer erweiterten Charakterisierungsmethodik. Um die Symmetrie und die elektrostatische Steuerung zu verbessern, wurden auf Festkörperaustausch basierende Al-Si-Ge Multi-Heterojunction und ein SiO_2/ ZrO_2 Gate-Stack implementiert. Zur Bewertung der Übertragungseigenschaften, der On-Off-Verhältnisse, der Temperaturstabilität und des Schaltverhaltens wurden automatisierte Gleichstrom- und Transientenmessungen durchgeführt, darunter mehrdimensionale große Parametersweeps. Es wurden mehrere Schaltungskonfigurationen realisiert, darunter komplementäre Inverter, Common-Source- und Common-Drain-Verstärker sowie ein rekonfigurierbares Transmission Gate.

Die Ergebnisse zeigen eine deutliche Weiterentwicklung von den Geräten der ersten Generation hin zu symmetrischen und leistungsstarken RFET-Schaltungen. Die dritte Generation erreicht eine nahezu ausgeglichene Leitung in NMOS und PMOS Modus, wobei sich I_{on}^{p}/I_{on}^{n} von 4.1 in der ersten Generation auf ≈ 0.88 verbessert und das On-to-Off-Verhältnis etwa sechs Dekaden beträgt. Die Verstärkung von Common-Source-Verstärkern stieg von nahezu Eins bei frühen Geräten auf Werte um 10 in der dritten Generation, während die Verstärkung von Common-Drain-Verstärkern bis zu 0,75 mit stabilen Arbeitspunkten erreichte. Das Transmission Gate zeigt korrektes bidirektionales Schalten, abstimmbare Dämpfung und reproduzierbares Übergangsverhalten mit einem effektiven Widerstand, der im Bereich von GΩ bis 100 kΩ einstellbar ist.

Diese Ergebnisse etablieren die dritte Generation von GeSOI-RFETs als robuste Plattform für rekonfigurierbare analoge und gemischte Signalschaltungen. Die nachgewiesene Verstärkungsabstimmbarkeit, der symmetrische Betrieb und die bidirektionale Übertragungsfähigkeit unterstreichen die Vielseitigkeit von RFET-basierten Architekturen. Zu den verbleibenden Herausforderungen zählen Ladungseffekte und eine begrenzte dynamische Leistung, die durch eine verbesserte Passivierung, optimierte Dielektrika und eine verbesserte Messintegration gelöst werden können. Die Ergebnisse bilden die Grundlage für die Entwicklung komplexerer rekonfigurierbarer Schaltungen und adaptiver elektronischer Systeme auf Basis der RFET-Technologie.

TU WIEN Bibliothek Your knowledge hub
Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.

Acknowledgement

I would like to express my gratitude to the following persons and institutions for their contributions to the successful completion of this thesis.

Andreas Fuchsberger
for providing essential technical assistance, for supporting the implementation and optimization of the measurement setups, and for his continuous support in supervising the experimental work in this thesis.

Masiar Sistani
for his direct supervision and for providing scientific guidance that shaped the conceptual and methodological framework of this thesis.

Walter M. Weber
for his supervision at the professorial level and for contributing constructive remarks and strategic guidance through his external perspective on the project.

Kilian Eysin
for fabricating the circuit samples used throughout this work.

Sherif Soliman
for implementing the python-based measurement framework.

Institute of Solid State Electronics
for providing access to office, cleanroom, and laboratory infrastructure, as well as for the scientific exchange with institute staff.

Felix Wagner
for providing encouragement during the preparation of this thesis and for undertaking the proofreading of the manuscript.

EU Sensoteric Project
for providing financial support through a research scholarship within the project and for the scientific contributions from the associated collaboration partners.

I acknowledge the use of ChatGPT for translations, proofreading, and summarization.

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU WIEN Bibliothek Your knowledge hub

Contents

1 Introduction **1**

2 Theory **5**
2.1 Materials 5
2.1.1 Silicon 5
2.1.2 Germanium 6
2.1.3 Aluminium 7
2.2 Metal-Semiconductor Heterostructures 8
2.3 Schottky Barrier Field-Effect Transistor 12
2.4 Reconfigurable Field-Effect Transistor 13
2.5 Fundamental Transistor Circuits 15
2.5.1 Common Source Amplifier 16
2.5.2 Common Drain Amplifier 18
2.5.3 Complementary Inverter 20
2.5.4 Transmission Gate 21

3 Experimental Techniques **23**
3.1 Fabrication of RFET Devices 23
3.2 Measurement setups 26
3.2.1 Karl Suss Needle Prober 28
3.2.1.1 HP 4156B Precision Semiconductor Parameter Analyzer . . 29
3.2.2 Cascade Summit Probe Station 30
3.2.2.1 Keithley 4200A-SCS Parameter Analyzer 32
3.2.3 Semi-Automatic Needle Prober 32
3.2.3.1 Keithley 4200A-SCS Parameter Analyzer - remote controlled 34
3.2.3.2 Python-based Control Framework 34
3.2.4 Transient Measurement 36
3.2.4.1 Keithley 4200A-SCS Parameter Analyzer - pulsed operation 37
3.2.4.2 Zurich Instruments MFLI 37

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU Wien Bibliothek Your knowledge hub

3.3 Electrical Characterization . . . 38
3.3.1 Transfer Characteristic . . . 38
3.3.2 Output Characteristic . . . 39
3.3.3 PG Sweep . . . 40
3.3.4 VD Sweep . . . 40
3.3.5 Large Parameter Sweep . . . 40
3.3.6 Transient Measurement . . . 41

4 Results and Discussion 43
4.1 Project Evolution . . . 43
4.2 GeSOI 20 Basic Characterization . . . 45
4.3 GeSOI 20 Complementary Inverter . . . 47
4.4 GeSOI 20 Common Source Amplifier . . . 49
4.5 GeSOI 20 Common Drain Amplifier . . . 52
4.6 GeSOI 21 Basic Characterization . . . 55
4.7 GeSOI 21 Common Source Amplifier . . . 57
4.8 GeSOI 21 Common Drain Amplifier . . . 60
4.9 GeSOI 21 Transmission Gate . . . 62
4.9.1 Control Gate Dependent Transfer Behavior . . . 62
4.9.2 Input Voltage Dependent Switching . . . 62
4.9.3 Program Gate Influence . . . 64
4.9.4 Transient Characteristics . . . 66

5 Summary and Outlook 69

List of Figures 73

Bibliography 75

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU WIEN Bibliothek Your knowledge hub

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU WIEN Bibliothek Your knowledge hub

Chapter 1

Introduction

The invention of the first semiconductor transistor in 1947 by Bardeen and Brattain initiated the development of modern microelectronics [1]. Since that time, continuous refinement of device architectures and fabrication technologies has enabled exponential growth in integration density and computational capability. Moore formulated this trend in 1965 with the prediction that the number of transistors on an integrated circuit would double within approximately eighteen months [2]. Over several decades, this development was primarily driven by geometric downscaling of silicon-based metal-oxide-semiconductor field-effect transistors, supported by the availability of high quality SiO_2 and the well-controlled fabrication of complementary CMOS circuits [3, 4].

As device dimensions approach few-nanometer length scales, several physical limitations restrict further downscaling. Thinner gate dielectrics induce substantial gate leakage through direct tunneling [3], while the electrostatic integrity of the channel degrades because of pronounced short-channel effects. Doping profiles cannot be scaled arbitrarily, which results in increased variability of threshold voltage and reduced drive current [5]. The mismatch in carrier mobility between electrons and holes requires geometric adjustments in complementary logic, which increases device area and impacts performance [6]. Furthermore, as highlighted by the International Roadmap for Devices and Systems, future systems are expected to require enhanced functionality, adaptivity, and energy efficiency beyond what conventional CMOS scaling can provide [7].

To address these challenges, alternative transistor concepts that extend or complement CMOS have been investigated. One promising direction is the use of Schottky-barrier field-effect transistors. In these devices, metal-semiconductor junctions replace the doped source and drain regions, which avoids the difficulties associated with nanoscale doping and allows the modulation of the carrier injection barrier by gate biases [3]. Reconfigurable field-effect transistors represent an extension of this principle in which the polarity of the device can be

selected during operation by adjusting the potential of additional program gate electrodes [8, 9]. This enables a single device to emulate either n-type or p-type behavior, which reduces the required number of transistors in complementary logic blocks and allows novel circuit architectures that exploit dynamic reconfigurability. Such capabilities are of interest for low power mixed-signal interfaces, polymorphic logic, hardware security primitives, and neuromorphic computing concepts in which the behavior of the circuit changes in response to external conditions.

Germanium is an attractive semiconductor for reconfigurable devices due to its high hole and electron mobilities and its compatibility with silicon processing [4]. However, a key challenge for germanium-based Schottky devices is the strong Fermi-level pinning close to the valence band, which leads to asymmetric barrier heights for electrons and holes [3]. Symmetric injection requires suppressing this pinning and establishing well-controlled metal-semiconductor interfaces. Solid-state exchange reactions between aluminum and silicon-germanium alloys have been shown to form abrupt Al-Si-Ge multi-heterojunctions with a thin silicon interlayer that reduces near valence band pinning and stabilizes the barrier configuration [8]. These developments provide a pathway toward symmetric, reproducible, and thermally stable reconfigurable devices.

Building on this foundation, the present thesis investigates the technological improvement, electrical behavior, and circuit-level functionality of second and third generation Al-Si-Ge multi-heterojunction RFETs fabricated on GeSOI substrates. The fabrication process employs a top-down nanosheet approach combined with rapid thermal annealing to induce solid-state exchange and form monocrystalline Al-Si-Ge structures. The SiO_2/ZrO_2 gate stack is selected for its combination of high interface quality and strong electrostatic coupling. Different top-gate configurations are implemented to allow either conventional Schottky-barrier operation or fully reconfigurable operation with program and control gates.

A comprehensive measurement framework was developed to evaluate the devices across a wide range of bias conditions and temperatures. Automated routines enable two-dimensional and multi-dimensional parameter sweeps, allowing the simultaneous variation of drain-source voltage, control gate voltage, program gate voltage, and device temperature. These measurements provide detailed insight into on-state currents, off-state leakage, symmetry properties, and the influence of temperature on barrier modulation. In addition, a transient measurement setup was implemented to study dynamic behavior under pulsed excitation.

The central objective of this work is to evaluate whether the introduced fabrication improvements lead to the targeted increase in polarity symmetry, on-to-off ratio, and analog performance. The study compares the early first-generation devices reported by Dobler [10] with the GeSOI 20 and GeSOI 21 platforms. The analysis investigates how the Al-Si-Ge contact formation, gate dielectric configuration, and geometric refinements translate

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU WIEN Bibliothek Your knowledge hub

into electrical improvements. Furthermore, the work explores how these device characteristics influence circuit behavior and identifies circuit topologies that can benefit from the reconfigurability of the RFET.

To demonstrate the applicability of the fabricated devices, several circuits are realized and characterized. These include complementary inverters, common-source and common-drain amplifiers with tunable gain, and a reconfigurable transmission gate that provides bidirectional switching and continuous resistance control. These circuits illustrate how reconfigurability can be used to adjust gain, shift operating points, and influence signal transmission characteristics without modifying the device geometry. The experimental results show that the GeSOI 21 generation exhibits improved symmetry, higher gain, and more stable operating points compared to previous generations.

In summary, this thesis provides an analysis of the technological, electrical, and circuit-level characteristics of Al-Si-Ge multi-heterojunction RFETs on GeSOI. The work demonstrates that with proper interface engineering and dielectric optimization, reconfigurable transistors can achieve symmetric conduction and high analog performance. Based on these results, Al-Si-Ge multi-heterojunction RFETs represent a promising platform for future adaptive and reconfigurable electronic systems.

This thesis is organized into five chapters. Chapter 2 introduces the theoretical background relevant to this work. It summarizes the material properties of Si, Ge, and Al, discusses metal-semiconductor heterostructures and Schottky-barrier transport, and outlines the operating principles of Schottky-barrier transistors and reconfigurable field-effect transistors. In addition, the fundamental transistor circuits used throughout this thesis are reviewed to establish the connection between device behavior and circuit functionality.

Chapter 3 describes the fabrication of the investigated Al-Si-Ge multi-heterojunction RFETs and SBFETs using a top-down nanosheet process on GeSOI substrates. The chapter also presents the measurement setups used to characterize the devices and ciruits.

Chapter 4 presents the experimental results. First, the evolution from first-generation devices reported in earlier work toward the GeSOI 20 and GeSOI 21 platforms is discussed. The electrical characteristics of both generations are analyzed, including transfer behavior, symmetry, temperature dependence, and on-to-off ratios. Based on these device insights, several circuits are demonstrated, including complementary inverters, common-source and common-drain amplifiers with tunable gain, and a reconfigurable transmission gate.

Chapter 5 summarizes the main findings of this work, evaluates their implications for reconfigurable device and circuit design, and discusses the limitations of the presented technology. The chapter concludes with an outlook on potential future research directions, including improved passivation, enhanced measurement integration, and the development of advanced RFET-based analog and mixed-signal circuits.

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU WIEN Bibliothek Your knowledge hub

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU Bibliothek Your knowledge hub WIEN

Chapter 2

Theory

This chapter develops the physical basis for the devices studied in this work and establishes the notation used throughout. First, the essential material properties of silicon, germanium, and aluminum are summarized (2.1). On this basis, the formation and electrostatics of metal-semiconductor heterostructures are discussed, including band alignment, barrier modulation, and dominant transport mechanisms (2.2). The device concepts then build up from these interfaces: the Schottky barrier field-effect transistor, where current is controlled by gate-induced modulation of contact barriers (2.3), and the reconfigurable field-effect transistor, which extends this principle to enable polarity control within the channel (2.4). Finally, fundamental transistor circuits used later in this thesis are reviewed to link device behavior to circuit-level functionality (2.5). The chapter provides the framework needed to interpret the experimental results presented in Chapter 4.

2.1 Materials

This section summarizes the essential properties of the materials used in this work: silicon (Si), germanium (Ge), and aluminum (Al). Si and Ge serve as semiconductors, together with Al they form the metal-semiconductor junctions of the investigated transistor devices.

2.1.1 Silicon

Silicon is a group-IV semiconductor with four valence electrons (atomic number 14, relative atomic mass 28.08 [11–13]). It crystallizes in the diamond lattice, as shown in Fig. 2.1(a), which can be described as two interpenetrating face-centered cubic lattices offset by one quarter of the body diagonal. Each atom forms four tetrahedral bonds of length $\sqrt{3}a/4$. The unit cell contains four tetrahedra, corresponding to a packing density of approximately 34% [3, 14, 15]. The room-temperature lattice constant is $a_{\text{Si}} = 0.5431\ nm$ [11, 15]. Although Si constitutes 25.7 % of the earth's crust, it occurs in oxides and silicates rather

than in elemental form and therefore requires purification, typically by vacuum float-zone processing [12]. Melting and boiling points are 1687 K and 3538 K, respectively [12]. Si is an indirect semiconductor with a conduction-band minimum at the Δ valley (15 % from X along $\langle 100 \rangle$) and a band gap of $E_G = 1.1\ eV$ at 300 K [3, 14, 16, 17], see Fig. 2.1(d). Typical room-temperature mobilities are $\mu_n \approx 1900\ cm^2/Vs$ and $\mu_p \approx 500\ cm^2/Vs$ [3, 12, 17].

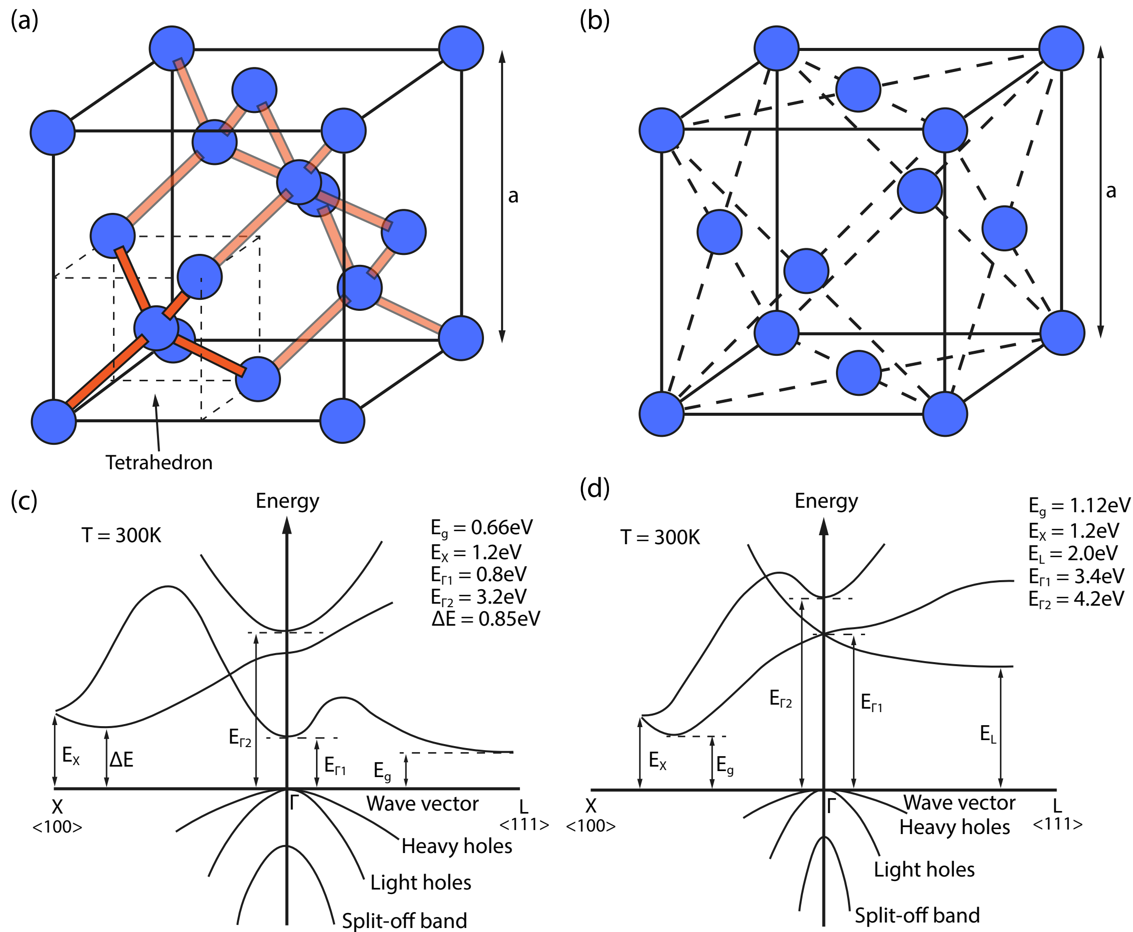


Figure 2.1: *Lattice structures of the materials used and the band diagrams of Si and Ge. (a) Diamond lattice, (b) Face-centered cubic (fcc), (c) Band diagram of Ge and (d) band diagram of Si. Lattice structures adapted from [3], band diagrams adapted from [3, 16, 17], graphics appended from [18].*

2.1.2 Germanium

Germanium, discovered by C. A. Winkler in 1886 in argyrodite (Ag_8GeS_6) [19], is likewise a group-IV semiconductor with properties similar to Si [4, 12, 20]. It has atomic number 32 and a relative atomic mass of 72.63 [11–13]. Ge crystallizes in the diamond lattice with $a_{\mathrm{Ge}} = 0.5658\ nm$ at room temperature [11, 15] and, like Si, requires high-purity refining for device applications [12]. The melting and boiling points are 1211 K and 3103 K [12, 21]. Ge exhibits an indirect band gap of $E_G = 0.66\ eV$ at the L point and a direct

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU WIEN Bibliothek Your knowledge hub

gap of $E_G = 0.8\ eV$ at Γ at 300 K, depicted in Fig. 2.1(c) [11, 16, 17]. Room-temperature mobilities are $\mu_n \approx 3800\ cm^2/Vs$ and $\mu_p \approx 1820\ cm^2/Vs$ [11, 12, 17].

Silicon dominates contemporary microelectronics due to its larger band gap (higher allowable operating temperatures), the availability of a high-quality native oxide (SiO_2) that provides device passivation, and the low interface-state density at the Si/SiO_2 interface enabling very high integration density [4].

A quantitative comparison of the bulk carrier mobilities of the discussed materials and selected III-V semiconductors is summarized in Table 2.1. The values demonstrate the superior carrier transport in Ge and III-V materials compared to Si, which explains their relevance for high-performance device concepts.

	Si	Ge	GaAs	GaN	GaP	InAs	AlAs
Lattice structure	D	D	Z	W	Z	Z	Z
Electron mobility $\mu_n\ (cm^2/Vs)$	1900	3800	9000	400	300	33000	1200
Hole mobility $\mu_p\ (cm^2/Vs)$	500	1820	500	0.27	150	460	420

Table 2.1: *Comparison of room-temperature bulk electron and hole mobilities for common semiconductor materials. Values from [3, 12, 17]. With D descirbing the diamond lattice, Z the zincblende lattice and W the wurtzite lattice.*

2.1.3 Aluminium

Aluminum (Al) is a group-III metal (atomic number 13, relative atomic mass 26.98 [12, 22]) that crystallizes in the face-centered cubic lattice with $a_{\mathrm{Al}} = 0.405\ nm$ at 298 K [22], see Fig. 2.1(b). Elemental Al is abundant but chemically reactive and is therefore obtained from bauxite via Bayer and Hall-Heroult processes. The production is energy-intensive, which motivates large-scale recycling [11, 12]. Al is lightweight, non-toxic, and exhibits high thermal and electrical conductivity [12]. The melting and boiling points are 933 K and 2792 K [12]. At room temperature the electrical conductivity is $\sigma_{\mathrm{Al}} \approx 37.7\ MS/m$, about 60 % of copper [12], with a strong temperature dependence. In advanced interconnects Cu and Cu/low-k stacks have largely replaced Al due to higher conductivity and improved electromigration robustness [23, 24].

For device fabrication, Al is also relevant beyond metallurgy. Compounds with group-V elements form III-V semiconductors with diverse properties (e.g., piezoelectric AlN with a direct band gap, indirect wide-gap AlP) [11, 25]. High-purity Al (>99.99 wt%) becomes superconducting below $T_C \approx 1.2\ K$ [11]. A practically important feature is the formation of a thin, compact native oxide (Al_2O_3) upon air exposure, which passivates the surface and protects the underlying metal. Alumina can also be deposited intentionally, e.g., by atomic layer deposition, to serve as a dielectric in electronic devices [11, 26, 27].

TU Bibliothek Your knowledge hub
Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.

2.2 Metal-Semiconductor Heterostructures

Following the introduction of the constituent materials, the next step toward functional devices is the formation of reliable metal-semiconductor heterostructures, which define carrier injection and control the electronic behavior of the devices. This section outlines the interplay between the metal (Al) and the semiconductor (Ge) and discusses the resulting junction characteristics, before addressing the junction model.

The contact material must enable abrupt, well-defined transitions with low barriers in the on-state, large barriers in the off-state and minimal interface trap density. In addition, the chosen material pair should avoid intermetallic phase formation to ensure process control, reproducibility, and stable junction stoichiometry [28, 29]. A viable route is thermally induced diffusion of the metal into the semiconductor. Numerous material systems have been explored, forming silicides or germanides (e.g., Ni-Si [30], Ni-Ge [31], Co-Ge [32]). For the present Al-Ge system, experiments demonstrate abrupt, reproducible metal-semiconductor transitions without intermetallic phases, which reduces device variability [28, 29, 33].

Diffusion denotes the stochastic motion of particles that equalizes concentration gradients. The rates range from mm/s to cm/s in fluids but are typically on the order of nm/s in solids and strongly temperature dependent. In crystalline solids, diffusion proceeds via point defects. Two principal mechanisms are relevant: (i) interstitial diffusion, where small atoms migrate between interstitial sites and (ii) vacancy diffusion, where atoms hop into thermally generated vacant lattice sites, prevalent near the melting point [34, 35]. For the Al-Ge system, both cross- and self-diffusion must be considered. Using rapid thermal annealing at 774 K, [28] extracted diffusion coefficients for Ge and Si in Al, Al self-diffusion, and self-diffusion in the semiconductors. The values are summarized in Table 2.2.

Al in Al	Al in Si	Al in Ge	Si in Al	Si in Si	Ge in Al	Ge in Ge
(cm^2/s) at 774 K						
$6.3 \cdot 10^{-10}$	$2.0 \cdot 10^{-22}$	$3.3 \cdot 10^{-20}$	$4.4 \cdot 10^{-8}$	$6.5 \cdot 10^{-19}$	$3.1 \cdot 10^{-9}$	$8.4 \cdot 10^{-20}$

Table 2.2: *Diffusion coefficients for the Al-Si and Al-Ge systems at 774 K. Data from [28].*

The data indicate significantly higher diffusion of Si and Ge in Al (and Al self-diffusion) compared to self-diffusion in Si or Ge or to Al diffusion into Si/Ge. This asymmetry promotes Al supply via Al self-diffusion while Si/Ge atoms out-diffuse, resulting in a sharp interface. Residual diffusion within Si or Ge depends on temperature and time but is negligible for the anneals used in this work, yielding abrupt transitions [28].

The Schottky barrier height (SBH) of the metal-semiconductor transition, which strongly affects the band structure and hence the device behavior, is governed by the metal and interface properties. As shown in Fig. 2.2, for Si, many metals pin close to midgap, whereas for Ge pinning is near the valence band [28, 36, 38]. To understand the electrical characteristics of these heterostructures, the fundamental band alignment and charge transport at the metal-semiconductor interface are discussed in the following.

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU WIEN Bibliothek Your knowledge hub

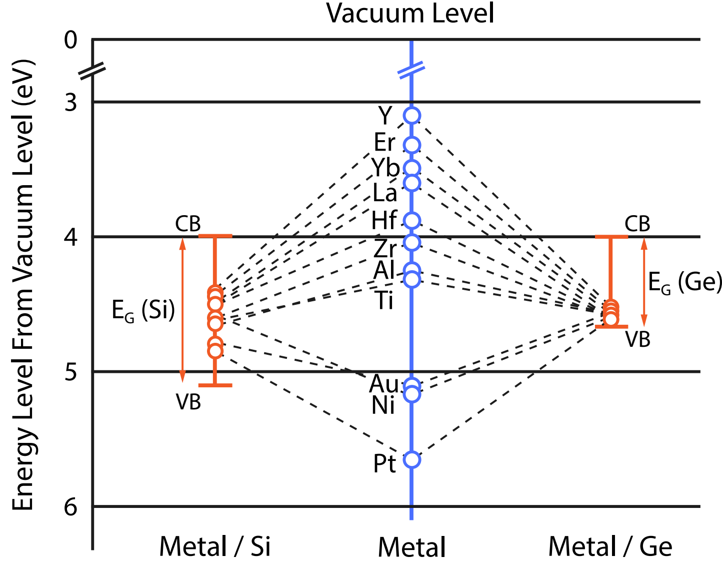


Figure 2.2: *Schottky barrier heights for various metal contacts. Showing the fermi level pinning of the metal to the semiconductor. With metal-silicon junctions on the left and metal-germanium junctions on the right. Adapted from [36, 37], graphics appended from [18].*

When a metal and a semiconductor are brought into direct contact, as in the Al/Ge system investigated in this work, thermal equilibrium requires a common Fermi level. The alignment of the Fermi energies causes band bending to compensate for the initial potential difference, achieved through charge transfer until charge neutrality is established [3, 39].

The characteristics of the metal-semiconductor transition are mainly determined by the work functions of the materials involved. Their difference defines a potential barrier, also referred to as the contact potential. The relevant quantities are the metal work function $q\phi_M$, the semiconductor work function $q\phi_S$, and the semiconductor electron affinity $q\chi$, which is the energy difference between the vacuum level and the conduction-band edge E_C. The semiconductor work function can be expressed as $q\phi_S = q(\chi + \phi_n)$, where $q\phi_n = E_C - E_F$ denotes the distance between the conduction band and the Fermi level. The barrier height ϕ_B depends on the semiconductor type and follows

$$q\phi_{B,n} = q(\phi_M - \chi), \tag{2.1}$$

$$q\phi_{B,p} = q\phi_S - q(\phi_M - \chi). \tag{2.2}$$

Fig. 2.3 illustrates the energy band structures of n-type and p-type semiconductors before and after contact formation. Subfigures (a) and (c) show the isolated semiconductor with the relevant parameters defined above for n-type and p-type material, respectively. When the metal and the semiconductor are brought into contact, charge transfer occurs until equilibrium is reached, resulting in band bending and the formation of a contact potential,

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU WIEN Bibliothek Your knowledge hub

as shown in subfigures (b) and (d) for n-type and p-type cases, respectively. The width of the resulting depletion region is indicated by W.

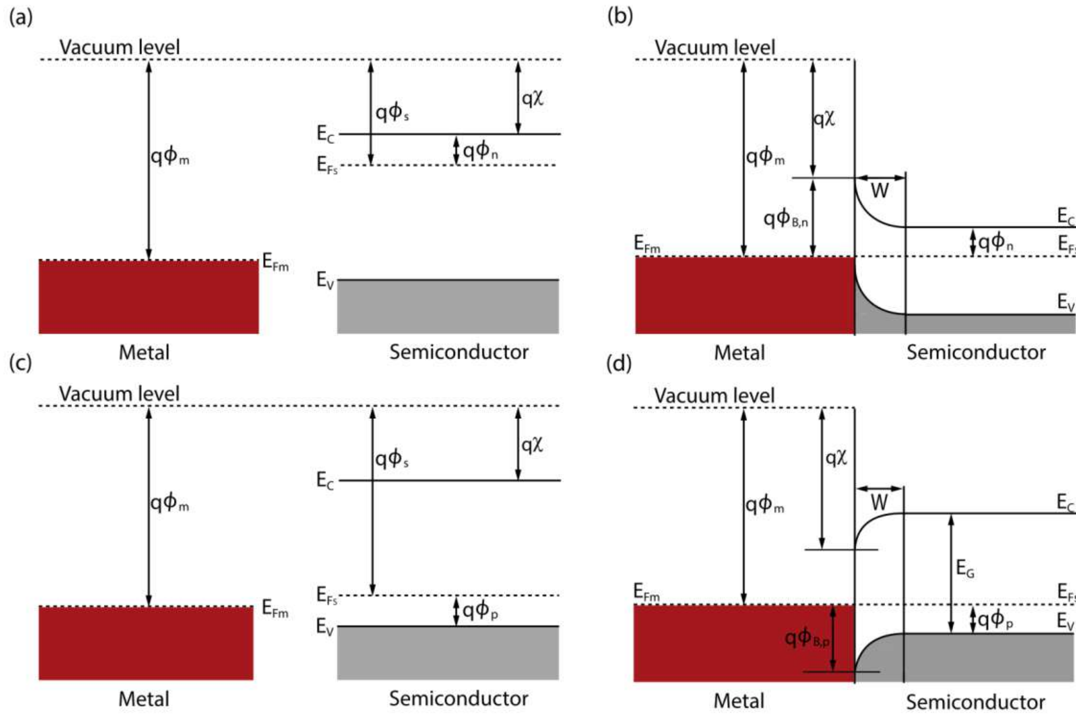


Figure 2.3: *Parameters and band diagrams for metal-semiconductor junctions. (a,c) Isolated n-type and p-type semiconductors; (b,d) corresponding junctions with band bending and depletion width W. Adapted from [3, 39], graphics appended from [18].*

The direction of band bending depends on the individual work functions $q\phi_S$ and $q\phi_M$. Four limiting cases exist, producing either rectifying or ohmic contacts. For an n-type semiconductor with $q\phi_M > q\phi_S$, electrons are depleted near the interface, resulting in a rectifying (Schottky) contact which limits current flow in one direction. Conversely, a p-type semiconductor with $q\phi_M > q\phi_S$ exhibits hole accumulation and thus ohmic behavior allowing bidirectional current flow. The complementary cases follow in an analogous manner [3, 14, 39].

Applying a bias voltage across the metal-semiconductor junction modifies the band bending and the effective barrier height for the charge carriers. Depending on the applied potential, the band alignment can shift toward higher or lower energies, which results in an increased or decreased carrier flow along the heterostructure. The applied voltage bias primarily affects the semiconductor side of the junction, where the band bending and the corresponding potential barrier for charge carriers are modified. On the metal side, the potential remains essentially unchanged due to the much higher carrier concentration. The situation for an applied forward voltage bias V is illustrated in Fig. 2.4 [3, 14].

TU WIEN Bibliothek Your knowledge hub
Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.

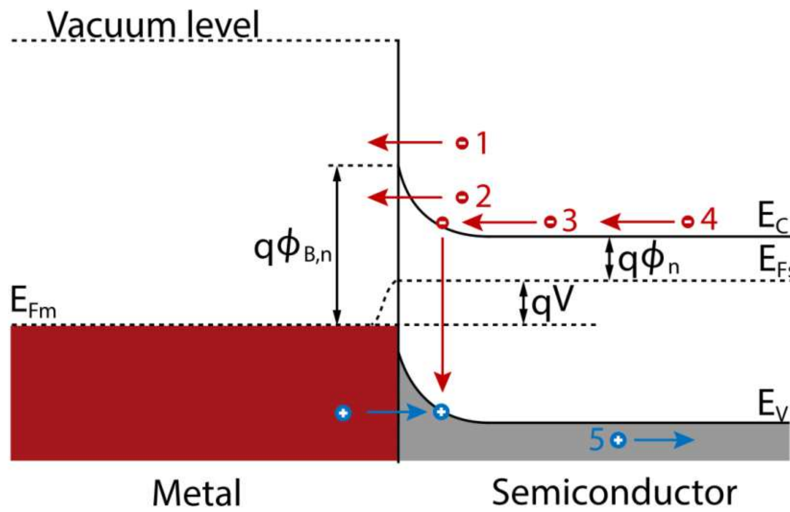


Figure 2.4: *Charge transport processes at a Schottky barrier: (1) thermionic emission, (2) tunneling, (3) recombination, (4) diffusion, and (5) injection of holes from the metal into the semiconductor. Adapted from [3], graphics appended from [18].*

The current through a metal-semiconductor junction is mainly governed by majority carriers. Under forward bias, five fundamental transport mechanisms contribute: (1) thermionic emission over the Schottky barrier, (2) quantum-mechanical tunneling through the barrier, which is dominant in highly doped semiconductors, (3) recombination in the depletion region, (4) diffusion of charge carriers into the depletion zone, and (5) hole injection from the metal into the semiconductor. Additional leakage currents may arise from interface traps. At moderate doping and room temperature, thermionic emission typically dominates, while tunneling can increase the current beyond the ideal exponential dependence. In practice, all contributions coexist, and the separation of individual mechanisms is often difficult. The processes shown in Fig 2.4 for electrons apply analogously to holes [3, 14, 40].

These mechanisms are often grouped into three categories: thermionic emission (TE), field emission (FE), and thermionic-field emission (TFE). Field emission describes tunneling near the Fermi level, whereas thermionic-field emission represents intermediate transport, where charge carriers possess insufficient energy to surmount the barrier but tunnel through a reduced potential width at elevated energies [3, 8].

For the Al/Ge system considered here, aluminum exhibits a work function of approximately 4.2 eV depending on surface orientation [12, 37], while germanium has a band gap of 0.66 eV [3] and an electron affinity χ_{Ge} of 4.0 eV [37]. As shown in Fig. 2.2, the Fermi level in Ge tends to pin near the valence band, resulting in a lower Schottky barrier compared to Si, where pinning occurs close to midgap. The deviation from the ideal Schottky-Mott prediction arises from interface states that modify the effective barrier

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU Bibliothek Your knowledge hub WIEN

height [3, 36, 39].

Metal-semiconductor heterostructures enable fast rectifying diodes [3]. Contacting both ends of a semiconductor channel with Schottky junctions yields a Schottky barrier field-effect transistor (SBFET) [8]. Adding a top metal gate separated by an insulator forms a Schottky barrier metal-insulator field-effect transistor (SB-MISFET), analogous to a MOSFET. Such devices offer simplified fabrication, reduced leakage, and suppression of parasitic bipolar effects compared to conventional FETs [41]. In the following, the operating principle of the SBFET is outlined, providing the foundation for the reconfigurable field-effect transistor (RFET) architecture investigated in this work.

2.3 Schottky Barrier Field-Effect Transistor

Based on the previously described heterostructures, transistors can be realized in which charge transport is governed by Schottky barriers rather than by doped source and drain regions. These devices, referred to as SBFET, employ metal-semiconductor contacts that form potential barriers for electrons and holes. The device current is controlled by gate-induced modulation of these Schottky barriers [3, 8, 41].

In conventional MOSFETs, the drain current is primarily determined by the formation of an inversion channel and is therefore strongly linked to the channel mobility, the gate-oxide capacitance, and the device geometry. In contrast, the current in SBFETs is fundamentally governed by carrier injection across the metal-semiconductor contacts. As a result, the drain current depends not only on transport through the semiconductor channel but also on the effective height and width of the Schottky barriers at the source and drain interfaces. Consequently, SBFETs can operate in a contact-limited regime, where Fermi-level pinning, barrier modulation, and gate control of the junction regions dominate the current characteristics[3, 41].

A schematic structure and the corresponding band diagrams of an SBFET are shown in Fig. 2.5. The transistor consists of a semiconducting channel contacted by two metallic electrodes forming Schottky barriers at the source and drain interfaces. A gate electrode, separated from the channel by a dielectric, controls the carrier injection by modulating the band profile and thus the effective barrier height at the junctions beneath the gate. In the off-state, both Schottky barriers are wide and high, effectively suppressing carrier injection from source and drain. A positive gate bias [Fig. 2.5(b)] lowers the barrier for electron injection into the conduction band, while a negative gate bias [Fig. 2.5(c)] reduces the valence-band barrier and promotes hole injection. The total current is thus controlled electrostatically by the gate-induced modulation of the carrier injection through the Schottky barriers. This operating principle allows ambipolar current flow using undoped channels while maintaining full gate controllability [3, 8, 14].

The SBFET offers several advantages compared to conventional MOSFETs. The absence

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU WIEN Bibliothek Your knowledge hub

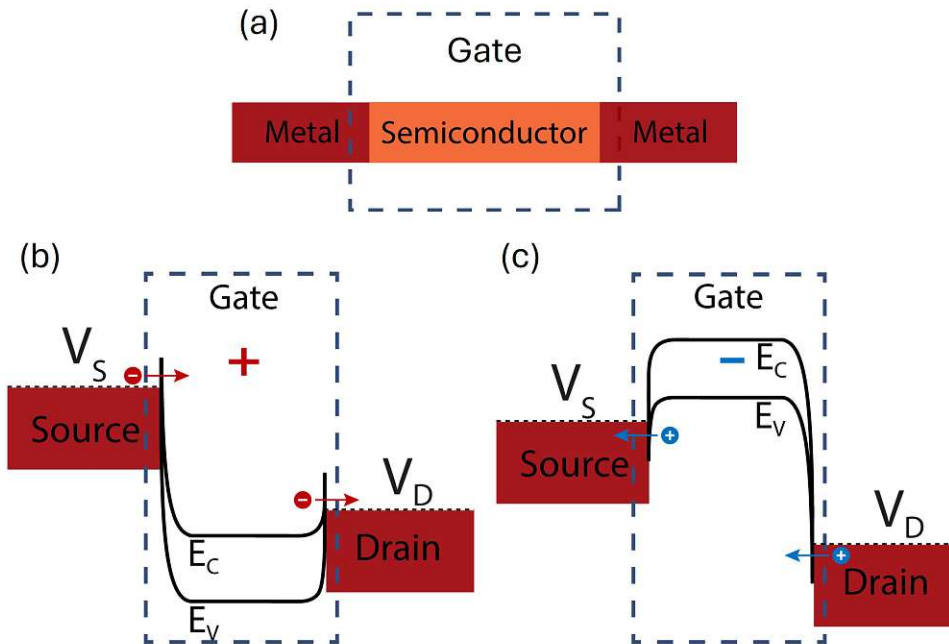


Figure 2.5: *Schottky barrier field-effect transistor: (a) schematic structure, (b) band diagram for positive gate bias and (c) band diagram for negative gate bias. The conduction and valence bands are modulated by the applied gate voltages and the source/drain potentials. Band diagrams adapted from [42].*

of heavily doped source and drain junctions simplifies fabrication and reduces the required thermal budget. The symmetric device design allows operation with either electron or hole conduction, resulting in ambipolar transfer characteristics when using an undoped channel [8, 41]. Furthermore, the absence of junction capacitances minimizes parasitic delay and enables high-frequency operation [3, 14].

However, Fermi-level pinning restricts the tunability of the Schottky barrier, leading to potentially asymmetric current characteristics for electrons and holes. These limitations motivate the development of advanced device concepts that allow independent and dynamic control of both Schottky barriers, forming the foundation of the reconfigurable field-effect transistor discussed in the following section [8, 28].

2.4 Reconfigurable Field-Effect Transistor

The reconfigurable field-effect transistor is an extension of the SBFET and enables dynamic control over the dominant charge carrier type within a single device. Although RFET can be doped, all devices discussed in this work are undoped metal-semiconductor-metal multi-heterostructures. In contrast to conventional CMOS technology, where the conduction type is fixed by doping, the RFET uses electrostatic gating to select between electron and hole transport through the channel. The underlying heterostructure consists of two

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU WIEN Bibliothek Your knowledge hub

individual Schottky barriers formed at the metal-semiconductor interfaces [7, 8].

Several RFET architectures exist, differing mainly in the number and configuration of the gate electrodes. The triple top-gate arrangement used in this work includes two program gates (PGs), also referred to as polarity gates, above the metal-semiconductor junctions and one control gate (CG) in the center of the semiconductor. Typically, both PGs are biased identically to shift both barriers symmetrically, although individual control is possible for more flexible operation [8, 43, 44].

The electrical transport in RFETs is determined by the electrostatic modulation of the Schottky barriers and the channel. Depending on the program gate potentials, two distinct conduction modes are obtained: p-type and n-type operation. The respective band alignments are shown in Fig. 2.6. For p-type operation, illustrated in Fig. 2.6(a) and (c), a negative program-gate voltage raises the energy bands, allowing hole transport across the heterostructure. When the control gate is also biased negatively, the device is in the on-state (a), whereas a positive control-gate voltage bends the bands downward, introducing an additional barrier within the channel and leading to the off-state (c). Conversely, for n-type operation, depicted in Fig. 2.6(b) and (d), a positive polarity-gate voltage lowers the energy bands, enabling electron transport. A negative control-gate voltage produces an additional potential barrier and suppresses current (b), while a positive control-gate voltage removes this barrier, resulting in the on-state (d). The ability to switch between these two operating modes purely by external bias enables dynamic reconfiguration of the transistor polarity without physical or structural modification [8, 43–45].

The RFET architecture offers several advantages compared to conventional transistor concepts. The use of undoped semiconductor channels avoids the complexity and variability associated with nanoscale doping [8]. The reconfigurable polarity during operation allows complementary logic functionality within a single transistor, reducing device count and circuit area [44, 46]. Moreover, the inherent reconfigurability provides opportunities for hardware security applications, such as physically unclonable functions and resistance against side-channel attacks [47, 48]. Due to its adaptability, the RFET also shows potential for neuromorphic and artificial intelligence hardware implementations [49].

Despite its advantages, the RFET performance is limited by the properties of the metal-semiconductor interfaces. Fermi-level pinning and barrier inhomogeneities can lead to asymmetric transport characteristics between electron and hole operation. Furthermore, parasitic coupling between polarity and control gates may reduce the effective reconfigurability. The optimization of contact materials, interface quality, and gate alignment is therefore essential for achieving symmetric and efficient device behavior. In this work, Al-Ge-based RFETs fabricated via a top-down process are investigated to evaluate their transport symmetry and switching capability. The experimental results presented in Chapter 4 demonstrate the functionality and potential of Al-Ge RFETs in reconfigurable circuits.

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU WIEN Bibliothek Your knowledge hub

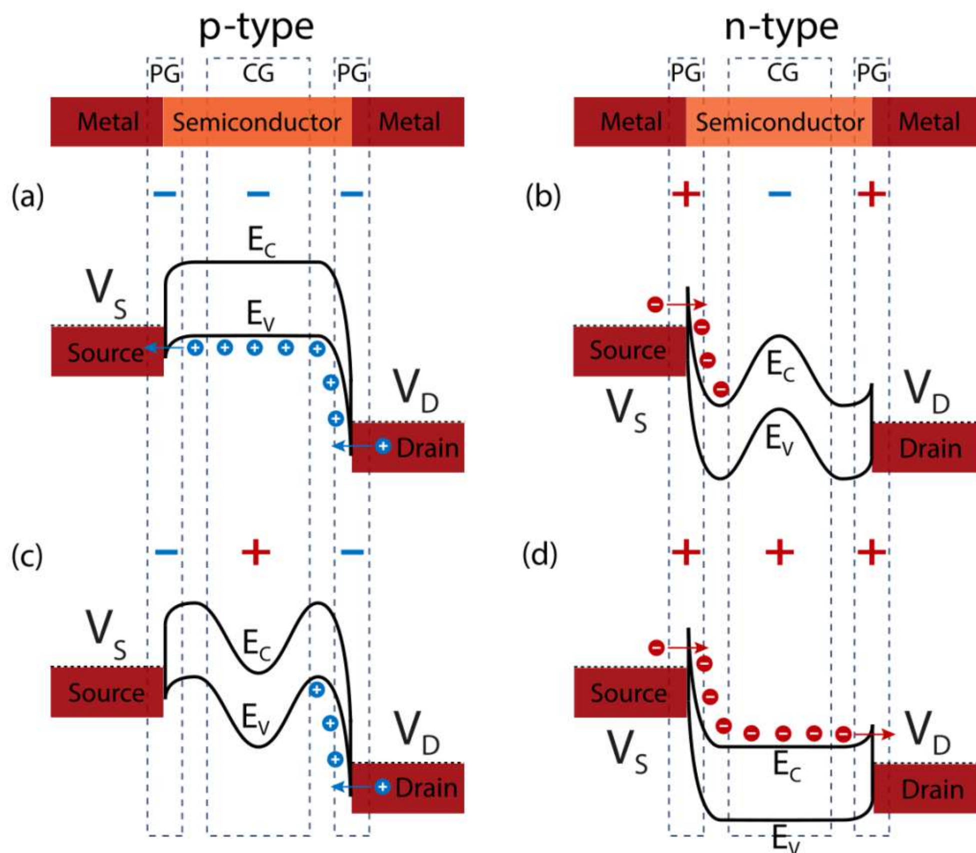


Figure 2.6: *Structure and operation principle of the RFET for different bias conditions. (a) p-type on-state, (b) n-type off-state, (c) p-type off-state, and (d) n-type on-state. The conduction and valence bands are modulated by the applied gate voltages and the source/drain potentials. Band diagrams adapted from [18].*

2.5 Fundamental Transistor Circuits

In this section, the fundamental transistor circuit configurations are introduced, which serve as the basis for both analog and digital circuit implementations. These basic circuits illustrate the characteristic voltage and current relationships of field-effect transistors and provide the foundation for understanding amplification and switching behavior in subsequent applications.

Three fundamental configurations are distinguished according to the terminal that is kept at a constant potential: the common source, the common drain, and the common gate circuit. The designation refers to the terminal that is not part of the signal path between input and output. In the context of this work, only the common source and common drain configurations are considered, as they are of primary importance for signal amplification and for the realization of complementary logic circuits.

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU Bibliothek WIEN Your knowledge hub

In all configurations, n-channel transistors are preferred over p-channel devices, as they exhibit a higher charge carrier mobility and therefore a larger transconductance for identical channel geometry. This results in higher current drive capability and improved gain performance compared to their p-channel counterparts.

The analysis of these configurations can be derived from the transistor transfer characteristics and small-signal models. In the following, the discussion is limited to qualitative aspects that are relevant for understanding the voltage transfer behavior and the influence of the bias potentials on the operating point. The common source and common drain circuits form the basic amplifier stages, whereas the complementary inverter represents the fundamental logic element in digital circuit design. Finally, the transmission gate is introduced as a bidirectional switch combining complementary transistors to achieve symmetric signal transmission [50, 51].

2.5.1 Common Source Amplifier

The common source amplifier is one of the fundamental voltage amplifier stages. In an n-MOS configuration, the source terminal is connected to a constant potential, typically V_{SS}, while the input signal is applied to the gate and the output is taken from the drain terminal. The drain is connected to the supply voltage V_{DD} through a resistive load R_L. The circuit schematic is shown in Fig. 2.7(a). Small variations in the gate-to-source voltage V_{GS} modulate the channel conductivity, resulting in corresponding changes of the drain current I_D. These current variations cause voltage changes at the drain node, which represent the output signal of the amplifier.

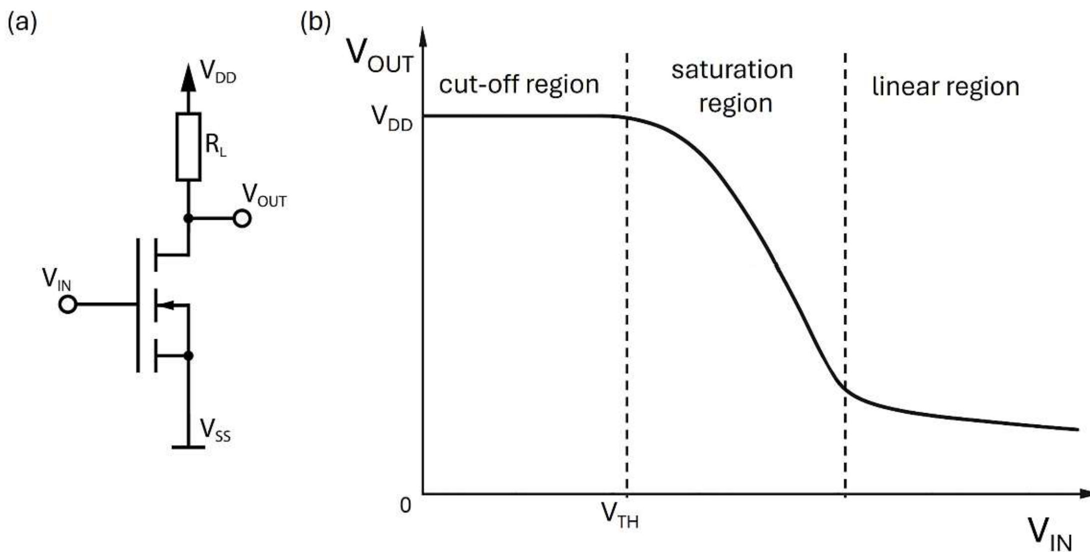


Figure 2.7: *Common source amplifier: (a) circuit schematic with resistive load and (b) corresponding transfer characteristic adapted from [50].*

The transfer characteristic of the common source amplifier as seen in Fig. 2.7(b) describes

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU WIEN Bibliothek Your knowledge hub

the relation between the input voltage $V_{IN} = V_{GS}$ and the corresponding output voltage $V_{OUT} = V_{DS}$. For input voltages below the threshold voltage V_{TH}, the device operates in the cut-off region and no drain current flows. Consequently, the output voltage equals the supply voltage V_{DD}.

As V_{GS} exceeds V_{TH}, the transistor enters the saturation region (with $V_{DS} \geq V_{GS} - V_{TH}$). In this regime, the drain current increases quadratically with the gate-to-source voltage. The increasing drain current causes a corresponding voltage drop across the load resistor R_L, resulting in a decreasing output voltage. The resulting voltage transfer curve therefore exhibits an inverted, non-linear characteristic with a steep slope in the central region. The slope of this section determines the voltage gain derived later in this section.

For further increasing V_{GS}, the transistor leaves the saturation region and enters the linear region (with $V_{DS} < V_{GS} - V_{TH}$), where the drain current rises only weakly with V_{GS}. In this regime, the output voltage approaches a minimum value determined by the voltage drop across R_L and the on-state resistance of the channel.

The usable operating range for analog amplification is located within the saturation region, where the transfer characteristic shows an approximately linear relationship between V_{GS} and V_{OUT}. The bias point, further referred to as A, is typically chosen in the middle of this region to allow for symmetrical signal swing around the operating point and maximum dynamic range.

For the small-signal analysis, the input variable is the gate-to-source voltage $V_{IN} = V_{GS}$. Around the bias point in the saturation region, the drain current follows

$$I_D = \frac{K}{2}(V_{GS} - V_{TH})^2, \tag{2.3}$$

where K denotes the device constant, neglecting parasitic like short channel modulation or the Early effect, from which the transconductance at the bias point results as

$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_A = K(V_{GS,A} - V_{TH}). \tag{2.4}$$

The output voltage obeys the relation

$$V_{OUT} = V_{DD} - I_D R_L, \tag{2.5}$$

considering small variations around A (denoted by Δ), differentiation of (2.5) yields

$$\Delta V_{OUT} = -\Delta I_D R_L. \tag{2.6}$$

Using (2.4) to relate current to voltage at the input gives

$$\Delta I_D = g_m \Delta V_{GS} = g_m \Delta V_{IN}. \tag{2.7}$$

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU WIEN Bibliothek Your knowledge hub

Combining (2.6) and (2.7) leads to the small-signal voltage gain

$$A_V = \frac{\Delta V_{OUT}}{\Delta V_{IN}} = -g_m R_L, \tag{2.8}$$

with the negative sign indicating the phase inversion between input and output [50, 51].

In integrated circuit implementations, the resistive load of the common source amplifier is frequently replaced by an active load to achieve higher voltage gain and improved area efficiency. The active load is typically realized using a MOS transistor connected as a current source or a diode-connected device. In this configuration, the load transistor operates in the saturation region, providing a large small-signal output resistance that significantly increases the overall gain of the amplifier. Furthermore, the use of an active load allows precise biasing through current mirrors and facilitates compact differential amplifier stages in analog CMOS design [51–53].

2.5.2 Common Drain Amplifier

The common drain amplifier, also referred to as a source follower, is another fundamental amplifier configuration of the field-effect transistor. In an n-MOS implementation, the drain terminal is connected to a constant potential, typically V_{DD}, while the input signal V_{IN} is applied to the gate and the output voltage V_{OUT} is taken from the source terminal. The source is connected to the reference potential V_{SS} through a resistive load R_L. The circuit schematic is shown in Fig. 2.8(a). In this configuration, the output voltage follows the input voltage with a small offset of approximately the threshold voltage V_{TH}. The circuit therefore acts as a voltage buffer providing high input and low output impedance.

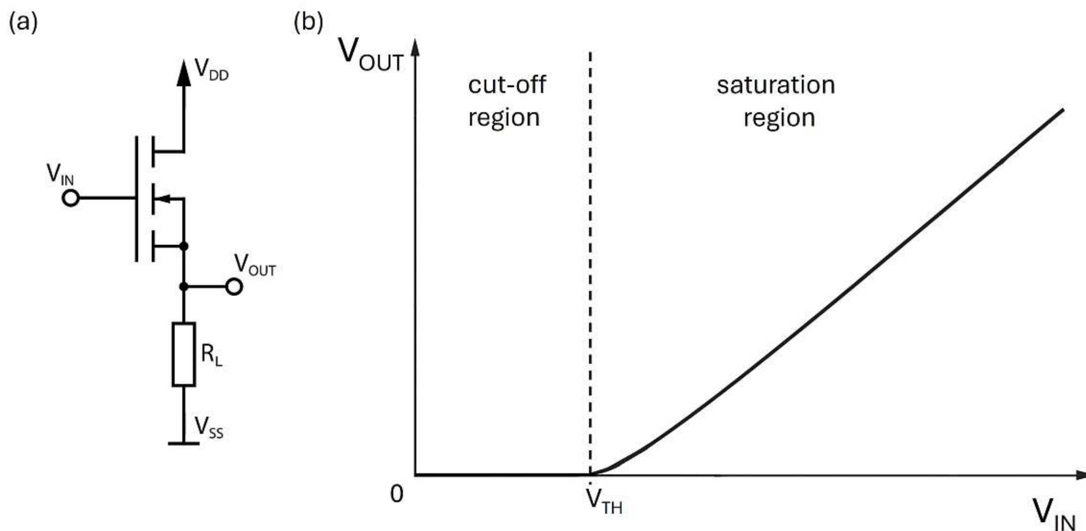


Figure 2.8: *Common drain amplifier: (a) circuit schematic with resistive load and (b) corresponding transfer characteristic adapted from [50].*

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU Bibliothek Your knowledge hub WIEN

The transfer characteristic of the common drain amplifier as seen in Fig. 2.8(b) describes the relation between the input voltage V_{IN} and the output voltage $V_{OUT} = V_S$. For input voltages below the threshold voltage V_{TH}, the transistor operates in the cut-off region and no current flows through R_L, resulting in an output voltage equal to V_{SS}.

When V_{IN} increases such that $V_{GS} = V_{IN} - V_{OUT}$ exceeds V_{TH}, the device enters the saturation region (with $V_{DS} \geq V_{GS} - V_{TH}$). The drain current is described by the square-law relation as given in (2.3) under the assumption of negligible Early effect. The corresponding voltage drop across R_L increases with I_D, which raises V_{OUT}. Hence, the output voltage follows the input voltage with a slope smaller than unity as derived later. Throughout normal operation, the transistor remains in the saturation region as long as the input signal stays below the supply voltage or exceeds it by no more than the threshold voltage V_{TH}.

The bias point, further referred to as A, is chosen in the middle of the saturation region to allow for maximum symmetrical signal swing. Around this point, small-signal variations of the input voltage produce proportional variations of the output voltage.

For the small-signal analysis, the drain potential is assumed constant and the transistor is represented by its transconductance g_m as introduced in (2.4). The small-signal relations follow from the linearized, incremental form of the transistor equations around the bias point

$$\Delta I_D = g_m \Delta V_{GS} = g_m(\Delta V_{IN} - \Delta V_{OUT}), \tag{2.9}$$

$$\Delta V_{OUT} = \Delta V_S = \Delta I_D R_L. \tag{2.10}$$

Combining (2.9) and (2.10) yields

$$\Delta V_{OUT} = g_m R_L(\Delta V_{IN} - \Delta V_{OUT}), \tag{2.11}$$

from which the small-signal voltage gain follows as

$$A_V = \frac{\Delta V_{OUT}}{\Delta V_{IN}} = \frac{g_m R_L}{1 + g_m R_L}. \tag{2.12}$$

The gain is below unity, indicating that the common drain amplifier does not provide voltage amplification but functions as a voltage follower. Its main advantage lies in the high input and low output impedance, making it suitable as a buffer stage in analog circuits [50, 51].

As in the common source configuration, the resistive load of the common drain amplifier can be replaced by an active load to improve integration density and bias control. The active load is typically implemented as a MOS transistor operating in the saturation region, acting as a constant current source for the source follower [51–53].

TU Bibliothek Your knowledge hub WIEN
Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.

2.5.3 Complementary Inverter

The complementary inverter represents the fundamental logic element in digital circuit design and serves as the basic building block for more complex CMOS logic gates. It performs a logical inversion between input and output signals and can be realized using complementary n-channel and p-channel transistors. As shown in the circuit schematic in Fig. 2.9(a), the gates of both transistors are connected together and form the common input terminal. The drains of the n-MOS and p-MOS are tied to a common node, which constitutes the output terminal. The source of the p-MOS and n-MOS are connected to the positive supply V_{DD} or the reference potential V_{SS}, respectively. Depending on the input voltage, either the pull-up path through the p-MOS or the pull-down path via the n-MOS conducts, establishing a low-impedance connection of the output node to one of the supply rails.

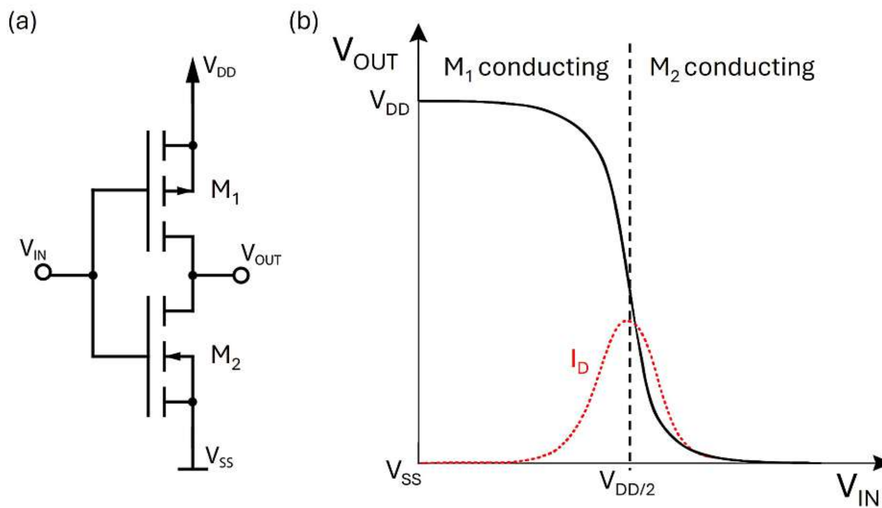


Figure 2.9: *Complementary CMOS inverter: (a) circuit schematic and (b) corresponding voltage transfer characteristic (black) and drain current (red), adapted from [54].*

As seen in Fig. 2.9(b), when the input voltage V_{IN} is low, the n-MOS is in the cut-off region and the p-MOS conducts, providing a low-impedance connection between the output node and the supply voltage V_{DD}. As a result, the output voltage equals V_{DD}, representing a logical high level. Conversely, when V_{IN} is high, the n-MOS conducts and connects the output node to the reference potential V_{SS}, while the p-MOS is cut off. The output voltage is therefore pulled to V_{SS}, corresponding to a logical low level. The circuit thus provides an inverted output relative to the input voltage, with the output switching sharply between the two supply rails depending on the input logic state.

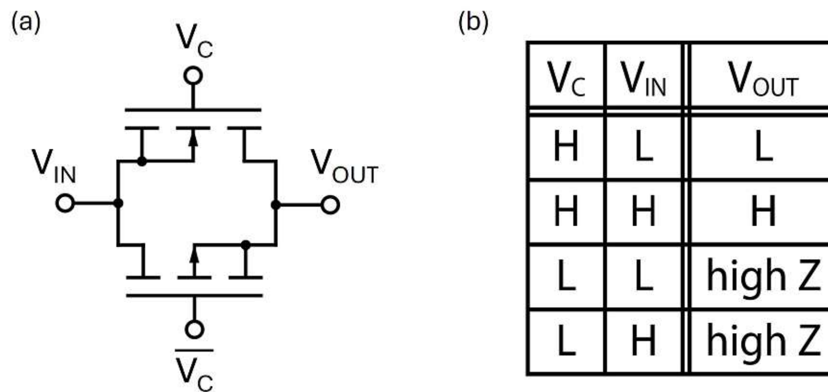
Around the switching point, where the input voltage V_{IN} is approximately half of the supply voltage V_{DD}, both transistors are nominally turned off. However, due to the finite subthreshold conduction of both channels, a small current still flows through the inverter. The total resistance between V_{DD} and V_{SS} is minimal at this point, resulting in a distinct

TU WIEN Bibliothek Your knowledge hub
Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.

current peak during the switching transition. This current does not occur because both transistors are fully conducting, but rather because their channel resistances overlap in the subthreshold region. As shown with the dashed red line in Fig. 2.9(b), this effect manifests as a short current spike in the transition region, which is responsible for the dynamic power dissipation of the complementary CMOS inverter. In the steady-state one transistor is completely turned off. As a result, there is no direct current path between the supply rails V_{DD} and V_{SS}, and ideally no static power is dissipated. In practice, small leakage mechanisms such as subthreshold conduction, gate tunneling, and junction leakage cause a residual static current through the inverter [54].

2.5.4 Transmission Gate

The transmission gate represents a bidirectional switch implemented with complementary field-effect transistors. It consists of an n-MOS and a p-MOS device connected in parallel, as shown in Fig. 2.10(a). The gate terminals are driven by complementary control signals V_C and $\overline{V_C}$. The sources and drains of both transistors are tied together, forming two symmetric signal terminals that allow bidirectional current flow. This configuration combines the low on-resistance of the n-MOS for high input voltages and of the p-MOS for low input voltages, thereby ensuring a low impedance path over the full voltage range.



V_C	V_{IN}	V_{OUT}
H	L	L
H	H	H
L	L	high Z
L	H	high Z

Figure 2.10: *Transmission gate: (a) circuit schematic with complementary control signals V_C and $\overline{V_C}$ and (b) corresponding truth table illustrating the relation between input V_{IN}, control signal V_C, and output V_{OUT}.*

As illustrated in Fig. 2.10(b), when the control signal V_C is high, the n-MOS is turned on and the p-MOS is activated by the low level of $\overline{V_C}$. Both transistors conduct simultaneously, establishing a low-impedance connection between the input V_{IN} and the output V_{OUT}. In this state, the transmission gate behaves as a closed switch and transfers the input signal without significant voltage drop across the channel.

When the control signal V_C is low, both transistors are turned off. The transmission gate is then in its high-impedance state, and the connection between input and output is effectively open. In this condition, V_{OUT} is electrically isolated from V_{IN}, and only small

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU WIEN Bibliothek Your knowledge hub

leakage currents caused by subthreshold conduction and junction leakage remain.

The complementary configuration of the transmission gate allows signal conduction over the entire voltage range between V_{SS} and V_{DD}, avoiding the threshold voltage degradation of single-transistor pass gates. This bidirectional switching capability enables its use as an analog switch, logic multiplexer, or sampling element in both digital and mixed-signal circuits. Due to its low distortion, low charge injection, and symmetrical structure, the transmission gate is widely employed in multiplexers, bus switches, and sample-and-hold circuits in modern CMOS systems [51, 55].

The circuits presented in this section are the fundamental configurations used throughout this work. Building on the RFET introduced in Section 2.4, their functionality can be extended by device-level electrostatic polarity control, enabling tunable amplification, inversion, and bidirectional switching within compact topologies. The practical implications of this tunability are demonstrated in Chapter 4. This chapter has established the physical and conceptual basis for the devices and circuits investigated in this work. The material properties of Si, Ge, and Al, together with the formation and transport mechanisms of metal-semiconductor heterostructures, provide the framework for understanding Schottky-barrier based devices. Building on this, the operating principles of SBFETs and RFETs were introduced, highlighting how electrostatic control of Schottky barriers enables ambipolar transport and dynamic polarity reconfiguration. Finally, the fundamental transistor circuits relevant to this thesis were reviewed to link device-level behavior to circuit-level functionality. In the next chapter, these concepts are translated into concrete experimental implementations: the fabrication flow of Al-Si-Ge multi-heterojunction RFETs on GeSOI and the development of the DC and transient measurement setups are described in detail.

TU WIEN Bibliothek Your knowledge hub
Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.

Chapter 3

Experimental Techniques

This chapter introduces the experimental methods, fabrication technologies, and measurement techniques used in this work to investigate the reconfigurable field-effect transistor concept and its circuit implementations. The objective is to describe the physical realization of the devices, the measurement environments employed for their electrical characterization, and the data acquisition procedures that form the basis for the subsequent analysis presented in Chapter 4.

The chapter is divided into three main sections. Section 3.1 provides an overview of the fabrication process of the GeSOI based RFETs and SBFETs used throughout this work, focusing on the material stack, contact formation, and gate architecture. Section 3.2 describes the different measurement setups employed for the electrical characterization, ranging from manual to fully automated probe stations, and outlines their respective capabilities in terms of bias control, temperature regulation, and measurement automation. Section 3.3 summarizes the electrical measurement routines, including static and dynamic characterization techniques, which were developed and implemented within the automated framework.

Together, these sections establish the experimental foundation for evaluating the functionality, reconfigurability, and performance of the fabricated RFET devices and their circuit-level applications.

3.1 Fabrication of RFET Devices

This section summarizes the fabrication flow of the devices investigated in this work. Wafer fabrication was performed at the cleanroom facilities of the Institute for Semiconductor and Solid-State Physics, Johannes Kepler University Linz, while device and circuit integration were carried out at the Institute of Solid State Electronics, TU Wien. Emphasis

TU Bibliothek Your knowledge hub WIEN
Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.

is placed on the GeSOI wafer platform, the top-down nanosheet definition, the dielectric stack formation, and the solid-state exchange based Al-Si-Ge multi-heterojunction contact technology.

All devices are realized on a GeSOI platform. The wafer stack consists of a Si substrate with a 100 nm buried oxide (BOX) of SiO_2, followed by an unstrained SOI layer of 20 nm. On top, a 10 nm Si buffer layer and a 4 nm Ge layer are grown by molecular beam epitaxy (MBE) on [100]-oriented SOI. A final 3 nm Si capping layer protects the Ge surface from oxidation and provides an interface for the subsequent dielectric formation. Fig. 3.1(a) illustrates the resulting GeSOI wafer structure.

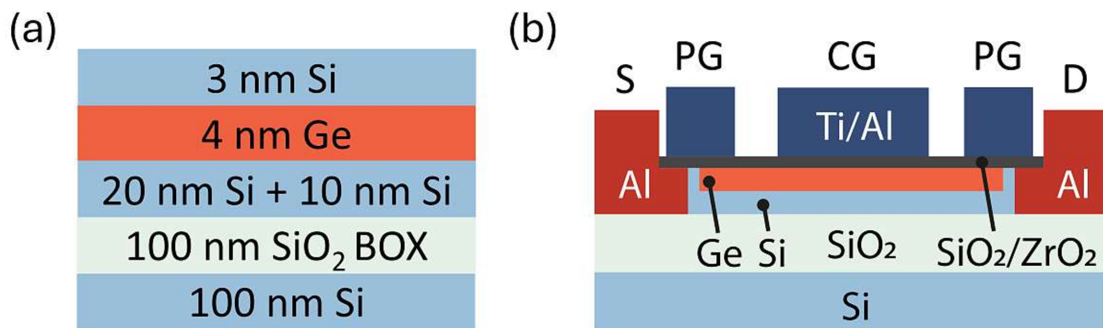


Figure 3.1: *Schematic of the GeSOI wafer stack and structured RFET. (a) Stack consisting of Si substrate / 100 nm BOX / 20 nm Si device layer, 10 nm MBE Si buffer layer, 4 nm Ge and 3 nm Si capping layer. Layer thicknesses not to scale. (b) RFET structure with Al source and drain Pads, SiO_2/ZrO_2 Gate Oxide and Ti/Al Gates.*

The devices are fabricated in a top-down approach, where the active nanosheets are structured out of the GeSOI stack. Laser lithography (Laser writer of the type HIMT MLA150) is used with AZ5214 image reversal resist to define nanosheet mesas of approximately 10μm length and 700 nm nominal width. After post bake at 100 $°C$ for 60 s, the structures are exposed and developed (AZ726 MIF), leaving the desired nanosheet regions protected by resist. Reactive-ion etching (RIE) in an SF_6/O_2 plasma is then used to transfer the pattern into the Ge/Si layers, exposing the BOX underneath. The residual resist is removed by plasma cleaning and acetone. The resulting Ge nanosheets serve as the active channels for both SBFET and RFET structures.

Following nanosheet definition, the surface is passivated and the gate dielectric stack is formed. The intentionally implemented Si cap on top of the Ge channel is first oxidized by dry thermal oxidation at approximately 900 $°C$ for 2.5 min in O_2, followed by an N_2 anneal of the same duration. This forms an interfacial SiO_2 layer of approximately 6.4 nm. Subsequently, a 2.5 nm ZrO_2 layer is deposited by atomic layer deposition. The combination of a high quality SiO_2 interface and a high-k ZrO_2 dielectric ensures low interface state density and sufficient gate coupling.

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU Bibliothek, Your knowledge hub, WIEN

Source and drain pads are structured using a second laser lithography step with AZ5214. After defining the contact regions, the dielectric stack is opened to expose the Ge channel. The ZrO_2 layer is removed by RIE using Ar/SF_6 plasma (forward power 50 W, 20 $°C$, 44 s), while the underlying SiO_2 is etched by a short HF dip of 18 s in buffered HF (7:1). Subsequently, 125 nm Al is sputtered onto the sample, and lift-off is performed to define the Al source and drain pads. These Al regions later serve as diffusion sources for the self aligned metal semiconductor contacts.

The crucial step in achieving reconfigurable device behavior is the formation of abrupt and symmetric metal semiconductor junctions. This is realized by a thermally induced solid-state exchange reaction between Al and the underlying Ge/Si layers. The process is carried out in a forming gas (N_2/H_2) atmosphere using flash rapid thermal annealing (RTA). Typically, four short pulses at approximately 500 $°C$ ($T_A = 773\ K$) and a cumulative duration of 315 s are applied. During this exchange, Si and Ge diffuses laterally into Al while Al atoms counter diffuse to fill up the empty space, resulting in a monocrystalline Al-Si-Ge heterostructure. The Si interlayer, inherently formed due to the different diffusion coefficients of Si and Ge, encapsulates the Ge core and acts as a Fermi level re pinning layer. This configuration ensures reproducible, symmetric barrier heights for both carrier polarities and thus enables the symmetric operation of the RFET. The resulting structure is an Al-Si-Ge-Si-Al heterostructure with two abrupt Schottky junctions defining the transistor channel. After the exchange process, the remaining semiconductor segment length (1 μm - 3.5 μm) is determined by optical microscopy to define the subsequent top gate alignment.

In addition to the lateral device geometry, the GeSOI stack determines the vertical charge carrier distribution in the channel. Together with Global TCAD Solutions (GTS), the electron and hole concentration profiles in the vertical Si-Ge channel were evaluated using a self-consistent 1-D Schrödinger-Poisson approach. The simulations indicate that, in the on-state, both carrier types are predominantly confined within the 4nm Ge layer close to the gate oxide interface. Due to the large valence band offset between Ge and Si, holes remain strongly localized in Ge over the full bias range, whereas electrons can partially extend into the underlying Si layer at lower positive gate voltages because of the small conduction band offset. Overall, carrier transport is governed mainly by the Ge layer for the relevant operating conditions [56].

In the final process step, Ti/Al top gates are defined above the nanosheet to modulate the Schottky barriers and channel potential. Depending on the structure type, either laser lithography - for the single-gated SBFET - or electron beam lithography (EBL) - for the triple-gated RFET - is employed. For EBL, PMMA resist is used. After development, 10 nm Ti and 100 nm Al are deposited by sputtering, followed by lift-off in acetone with ultrasonic agitation. Ti defines the effective gate work function, whereas Al provides stable probe pads and prevents oxidation of Ti.

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU Bibliothek WIEN Your knowledge hub

Two gate layouts are implemented: the SBFET, consisting of a single top gate overlapping both Al-Si-Ge junctions, and the RFET with three gates in total. Two Program Gates located directly above the junctions (electrically tied in this work) and one Control Gate above the Ge segment. Accurate PG alignment with the junction positions is essential for proper operation. Mask spacing is derived from post anneal optical measurements.

The structured device is schematically shown in Fig. 3.1(b), the final GeSOI sample, including all fabricated structures, is illustrated in Fig. 3.2(a). All of the measurements on circuits in this work were performed on the inverter structure as shown in the lower left quarter of the sample. Additionally, a close up scanning electron microscope capture of a single device is presented in Fig. 3.2(b).

3.2 Measurement setups

The experimental workflow of this thesis is structured to establish a direct link between device fabrication, electrical characterization, and data-driven modeling. The objective is to investigate the static and dynamic behavior of reconfigurable field-effect transistors (RFETs) and their integration into basic circuit configurations. The individual measurement setups introduced in the following sections each serve a specific role within this workflow and differ primarily in automation level, temperature control, and temporal resolution.

The core of the characterization process consists of direct-current and transient measurements of single RFET devices and small circuits. From these measurements, key parameters such as the threshold voltage, transconductance, and on/off current ratio are derived, as well as transient switching properties for pulsed operation. Each experiment type targets a particular aspect of the device physics: transfer and output characteristics describe the steady-state transport behavior, program gate and drain sweeps enable bias-dependent analysis of reconfigurability, and transient measurements provide time-resolved information on switching dynamics.

Three complementary setups were used to cover the full range of required measurements. The *Karl Suss Needle Prober* enables flexible multi-terminal probing and was primarily used for circuit-level tests. The *Cascade* setup provides precise wafer-level measurements with controlled temperature and defined light conditions. The most advanced configuration, the *PA300* semi-automatic prober, integrates fully automated device navigation and data acquisition through the Python-based control framework developed in this work. This framework allows extended temperature-dependent and multi-parameter sweeps to be carried out autonomously. For time-resolved measurements, the *Transient Measurement* setup combines the biasing capability of the Keithley 4200A-SCS system with high-speed data acquisition using a Zurich Instruments MFLI Lock-In Amplifier.

Together, these setups establish a consistent measurement chain that connects material

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU WIEN Bibliothek Your knowledge hub

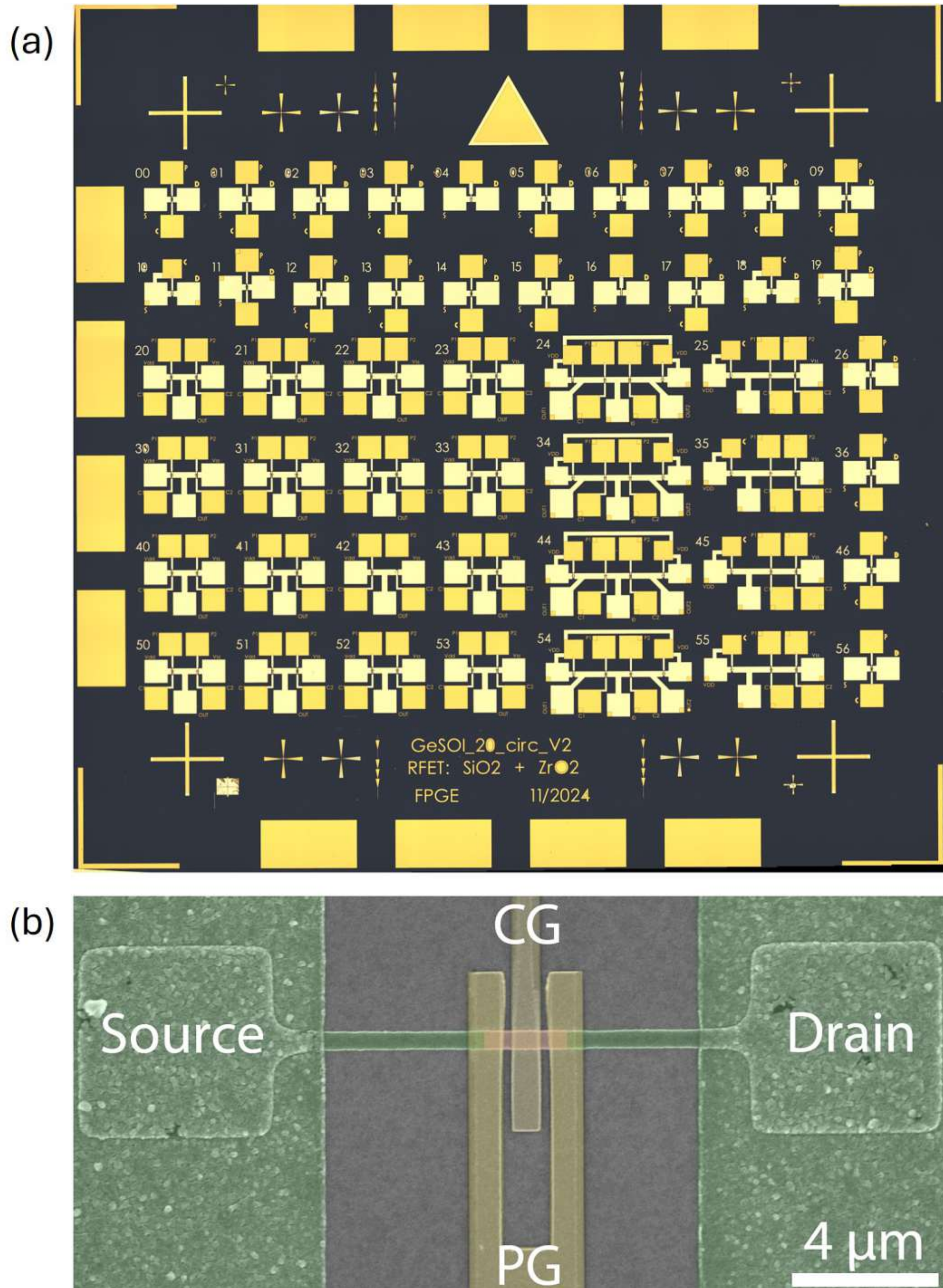


Figure 3.2: *Structures on the GeSOI 20 circuit sample. (a) final sample with the first and second row, as well as last column: RFET, SBFET and MOS diode reference structures. 4x4 structures on the bottom left: complementary inverter circuits. Column from 24 to 54: current mirror circuits. Column 25 to 55: cascode circuit. (b) False-color SEM image of the structured GeSOI RFET adapted from [57]. Aluminium source and drain pads in green, Aluminium-Titanium Control and Program Gate Electrodes yellow and the germanium channel in orange.*

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU Bibliothek, Your knowledge hub, WIEN

properties and device fabrication with electrical performance. The following sections describe the individual systems in more detail and explain how their specific capabilities were utilized within this workflow.

Each measurement setup consists of two essential components: a mechanical probing system for the electrical contact to the device under test (DUT) and an electrical characterization unit for the generation and acquisition of voltage and current signals. The mechanical part provides precise positioning of the probe needles on the contact pads, stable sample fixation, and, if required, temperature control of the sample environment. The electrical part performs biasing, signal sourcing, and measurement routines with high accuracy and repeatability.

3.2.1 Karl Suss Needle Prober

This setup was primarily used for the characterization of circuits with a large number of contact pads. The investigated devices required up to seven electrical terminals to be contacted simultaneously, which exceeded the capabilities of most probe systems present in the institute facility. The Karl Suss Needle Prober setup therefore combines a highly flexible manual probe station with a versatile semiconductor parameter analyzer, allowing comprehensive DC characterization of multi-terminal reconfigurable devices. An overview of the setup is shown in Fig. 3.3.

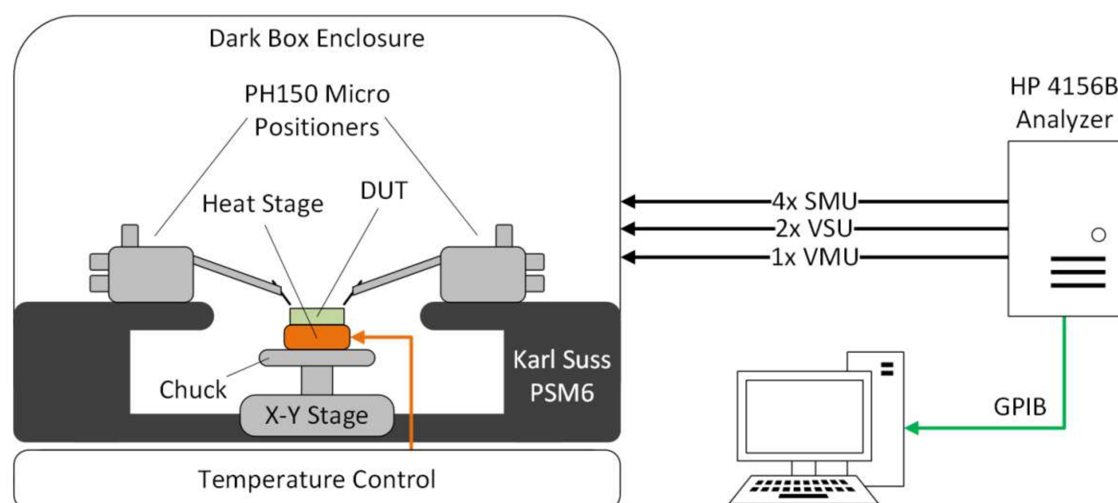


Figure 3.3: *Layout of the Karl Suss Needle Prober setup consisting of the probe station, connected to the parameter analyzer via triaxial cables for each measurement channel, and the GPIB connection to the workstation for measurement data export.*

The electrical characterization was performed using a Karl Suss PSM6 manual probe station enclosed in a Karl Suss Dark Box to minimize ambient light and electrical interference. The system is designed for wafers and substrates up to 150 mm in diameter and provides a highly stable mechanical platform through its massive cast frame and granite base that supports the air-bearing X-Y stage. The stage is positioned manually without

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU Bibliothek WIEN Your knowledge hub

calibrated precision but allows smooth, vibration-free motion and can be fixed in place by vacuum once aligned. The Z-axis coarse adjustment is realized through a leadscrew and a pneumatic lift mechanism with a travel of 10 mm, enabling reproducible contact and separation of the probe needles while maintaining safe mechanical clearance to the sample. The mechanical design provides excellent rigidity and submicron stability for low-current electrical measurements [58].

Up to seven PH150 Micro Positioners equipped with probe needles were mounted on the platen to access all electrical terminals of the investigated devices. Each PH150 unit provides independent linear motion in all three spatial directions with a travel range of 10 mm in X and Y and 8 mm in Z direction. The positioners use precision cross-roller bearings and backlash-free high-resolution screws with 250 or 500 μm per revolution, depending on the axis, and a corresponding motion resolution down to approximately 0.5 μm. Each axis is mechanically decoupled, allowing independent movement without mechanical cross-talk. The vacuum base system ensures strong and stable adhesion to the platen without deviation during activation or release [59].

Temperature-dependent measurements were enabled by an externally attached custom-built heat station. The system consists of a resistive heat pad placed on the chuck and a thermocouple sensor positioned near the DUT. The controller manually regulates the pad's supply voltage according to the thermocouple feedback until the desired temperature is reached. This configuration allows adjustment from room temperature up to approximately 150 $°C$ and provides sufficient thermal stability for measurements, even though the regulation is not automated.

This setup provided the basis for electrical characterization performed with the HP 4156B analyzer described in the following section.

3.2.1.1 HP 4156B Precision Semiconductor Parameter Analyzer

Electrical measurements were performed using a Hewlett Packard HP 4156B Precision Semiconductor Parameter Analyzer [60]. The instrument provides four High-Resolution Source Measure Units (SMU), each capable of sourcing and measuring voltages up to ± 100 V and currents from 10 fA to 100 mA with a minimum resolution of 1 fA and 2 μV. Additionally, two Voltage Source Units (VSU) with ± 20 V output range and one Voltage Measurement Unit (VMU) with ± 20 V input range and 2 μV resolution are available. The analyzer features Kelvin triaxial connections, ensuring remote sensing and minimal influence of cable resistances.

The instrument supports both voltage and current compliance limits for device protection, and internal auto-calibration ensures long-term measurement stability. The input impedance in high-resistance measurement modes exceeds 10^{15} Ω, enabling accurate detection of leakage and sub-threshold currents. Measurement accuracy is specified to better than 0.02 % of the measured value plus a range-dependent offset.

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU WIEN Bibliothek Your knowledge hub

All measurement routines were programmed directly on the analyzer using its control interface. The HP 4156B provides built-in functionality for voltage or current sweeps (linear or logarithmic) with up to 1001 steps, as well as pulsing with one SMU and a maximum frequency of 200 Hz. These routines are stored on the analyzer's floppy disk and can be loaded and executed autonomously without external control software. The workstation connected via GPIB serves exclusively for data read-out, archiving, and analysis using a LabVIEW-based interface.

Within the HP 4156B measurement framework, the sweep control is implemented by the internal VAR functions. The primary sweep variable, VAR1, defines the main staircase or pulsed voltage or current sweep that is applied to a selected SMU channel. The subordinate sweep variable, VAR2, can be used to perform two-dimensional sweeps by incrementing its value after each complete VAR1 cycle, enabling nested parameter variations such as gate and drain voltage combinations. In addition, the coupled sweep variable VAR1′ allows the generation of a synchronized sweep signal that is mathematically related to VAR1 through a user-defined linear relationship of the form VAR1′ = a × VAR1 + b, where a and b are programmable constants. This functionality enables correlated voltage sweeps with adjustable scaling and offset, which are particularly useful for biasing symmetric or complementary terminals. These built-in sweep definitions were used as the basis for all DC measurement routines developed in this work but exhibit limitations that motivated the development of the remote controlled setup described in Subsection 3.2.3.

The HP 4156B supports time-domain sampling with linear or logarithmic scaling, covering sampling intervals between 60 μs and 65 s with down to 20 μs resolution, corresponding to a maximum sampling rate of approximately 16.7 kHz. While suitable for slow transient or quasi-stationary analyses, faster switching dynamics cannot be resolved with this setup. This limitation motivated the development of the dedicated transient measurement system described in Subsection 3.2.4.

3.2.2 Cascade Summit Probe Station

The Cascade setup was primarily employed for fast and flexible wafer-level characterization. In contrast to the Karl Suss Needle Prober, this system provides precision X-Y-θ chuck control, allowing rapid switching between adjacent devices on the same sample without the need for manual needle reconfiguration. The combination of a mechanically stable probe station with integrated dark enclosure and a modern semiconductor parameter analyzer enables efficient measurements under controlled environmental conditions. However, the system is limited to five available needles and four measurement channels, which constrains its use to circuits with a smaller number of electrical terminals. An overview of the Cascade setup is shown in Fig. 3.4.

Measurements were conducted using a Cascade Summit 11000B-AP manual probe station, operated within the integrated MicroChamber to suppress light and electromagnetic interference. The system supports wafers up to 200 mm in diameter and features Cascade

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU WIEN Bibliothek Your knowledge hub

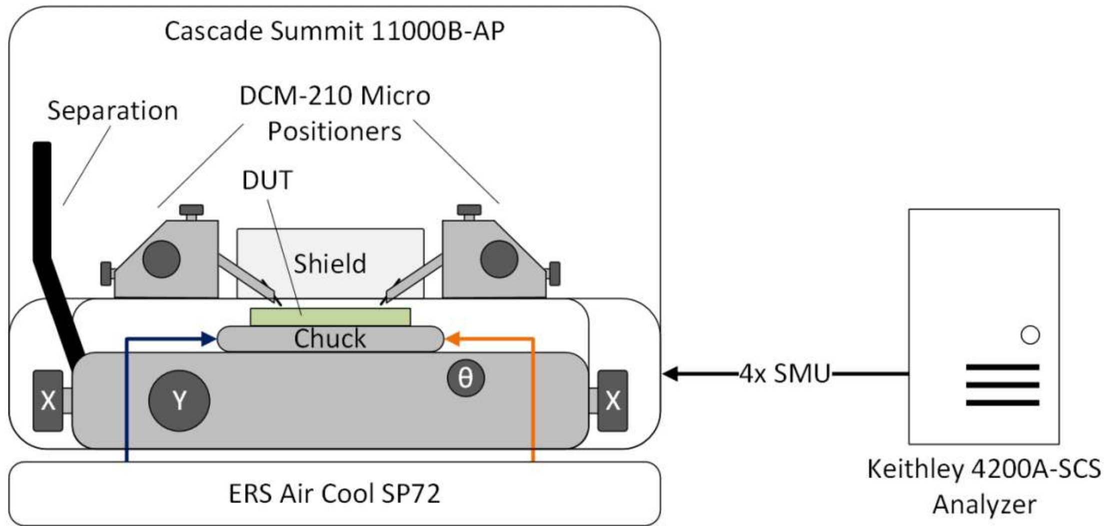


Figure 3.4: *Layout of the Cascade setup consisting of the probe station, connected to the parameter analyzer via triaxial cables for each measurement channel.*

PureLine and AttoGuard technologies for minimized AC and spectral noise. The manual X-Y-θ stage provides a travel range of 203 $mm \times 203$ mm with rotary controls of 5 mm per turn and a mechanical θ-rotation range of ± 5.7 ° at 0.8 °/turn resolution. The platen is mounted on a precision four-point lift system with 5 mm vertical range and repeatability below 3 μm, allowing reliable contact and separation during probing operations. The MicroChamber enclosure achieves light attenuation greater than 120 dB and EMI shielding above 20 dB for frequencies up to 20 GHz, providing a stable electrical environment [61].

Five DCM-210 precision micro positioners were mounted on the magnetic platen to contact the device terminals. Each unit offers 12.7 mm travel range in X, Y, and Z directions with screw resolutions of 250 μm per revolution and fine control resolution of approximately 2 μm. The positioners employ cross-roller bearings for backlash-free motion and can be operated with either vacuum or magnetic bases for strong adhesion to the platen surface [62]. Cascade 154-001 probe needles were used to establish electrical contact with the DUT [63].

Temperature-dependent measurements were carried out using an ERS Air Cool SP72 thermal controller connected to the integrated thermal chuck. The system provides active temperature regulation from -55 °C to 200 °C with a typical accuracy of ± 0.08 °C around the manually set temperature and thermal repeatability of ± 0.2 °C. The air-cooled design allows fast transitions between temperature setpoints while maintaining low vibration and acoustic noise levels [64].

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU Bibliothek Your knowledge hub WIEN

3.2.2.1 Keithley 4200A-SCS Parameter Analyzer

The electrical characterization was performed using a Keithley 4200A-SCS Parameter Analyzer [65]. The instrument integrates four Source Measure Units (SMU), each capable of sourcing and measuring voltages up to $\pm 210\ V$ and currents from $100\ fA$ to $1\ A$, providing sub-femtoampere resolution and high-accuracy I-V characterization. In addition, the system supports CV measurements via the equipped CVU modules, however these were not used in this work. All instrument control and data acquisition are executed through the Clarius software environment, which offers a graphical interface for defining test projects, configuring instrument channels, and performing automated sweeps or multi-step measurement sequences. Data can be analyzed directly within Clarius or exported for further post-processing.

The 4200A-SCS enables fully synchronized sweeps across multiple SMUs, including nested voltage sweeps comparable to the VAR1/VAR2 framework of the HP 4156B, but with significantly higher timing precision and modern software automation. The system's compact configuration and software-based project handling substantially increased throughput for wafer-level characterization compared to the legacy setup described in Subection 3.2.1. However, the available degrees of freedom are still limited by the underlying VAR1/VAR2 sweep structure, which constrains the simultaneous variation of multiple bias parameters. In addition, temperature control requires manual adjustment of the thermal setpoint. These limitations are addressed in the semi-automatic prober system described in Subsection 3.2.3, which enables a nearly fully automated characterization process with an extended number of configurable parameters and measurement degrees of freedom.

3.2.3 Semi-Automatic Needle Prober

The semi-automatic needle prober setup represents the most advanced measurement environment developed as part of this work. It combines a PA300 semi-automatic probe station, an external temperature controller, and a Keithley 4200A-SCS parameter analyzer. All components are centrally controlled from a workstation via Ethernet using a custom Python-based control framework that enables fully automated multi-parameter device characterization across a wide range of temperatures and bias conditions. The Python-based framework was developed during a Bachelor's thesis by S. Soliman under supervision of the author, following the conceptual design and measurement requirements defined in this work. The layout of the setup is shown in Fig. 3.5.

The automated measurements were performed using a PA300 probe station [66], a high-precision semi-automatic wafer prober designed for wafer diameters up to $300\ mm$. The system combines motorized X-Y-θ chuck movement with submicron resolution and an automated Z-axis lift mechanism for reproducible contact and separation sequences. The X-Y stage provides a total travel range of $300\ mm \times 300\ mm$ with an incremental resolution of $0.5\ \mu m$ and a repeatability of $\pm 1\ \mu m$ over the full range. The Z-axis lift has a travel range of $10\ mm$ with a resolution of $0.25\ \mu m$. The rotational θ-axis allows a mechanical

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU WIEN Bibliothek Your knowledge hub

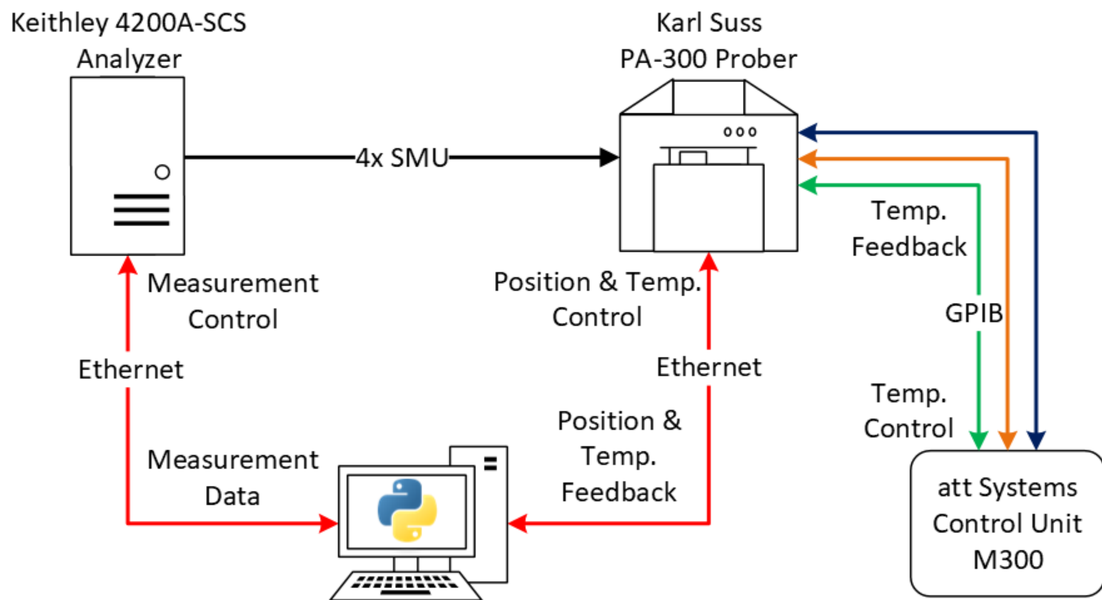


Figure 3.5: *Layout of the Semi-Automatic Needle Prober setup. The workstation controls the 4200A-SCS Analyzer and PA300 Prober via Python over an Ethernet connection. Temperature commands are forwarded to the M300 Temperature Controller via GPIB.*

travel of ±5 ° with a minimum step size of 0.0001 °, enabling precise alignment of the wafer to the probe coordinate system. All stage movements are controlled through closed-loop servomotors with encoder feedback, ensuring high positioning accuracy and long-term stability during extended automated measurement campaigns.

The chuck is vacuum based, providing reliable wafer fixation throughout thermal stress cycles. It incorporates a multi-zone heating system connected to an external temperature controller that enables active wafer heating and cooling over a nominal temperature range from $-60\ °C$ to $300\ °C$. The temperature stability is specified to be within $\pm 0.1\ °C$, and the uniformity across the chuck surface better than $\pm 0.5\ °C$. Temperature feedback is provided by integrated sensors located close to the wafer surface, ensuring accurate control of the sample temperature during characterization. The chuck and probe area are fully enclosed in a shielded housing that suppresses both ambient light and electromagnetic interference, providing a low-noise measurement environment crucial for sub-picoampere current measurement.

The probe station is further equipped with an integrated optical microscope and camera assembly that allows precise visual inspection of the contact points and needle positions. The PA300 supports full external control through the NI-VISA framework, providing access to stage positioning and temperature parameters. This interface enables seamless integration into the Python-based measurement framework described in Subsection 3.2.3.2, which performs automated probe navigation, device contact, and temperature control.

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU WIEN Bibliothek Your knowledge hub

3.2.3.1 Keithley 4200A-SCS Parameter Analyzer - remote controlled

The electrical characterization was again performed using a Keithley 4200A-SCS Parameter Analyzer, identical in base configuration to the Cascade setup but extended by additional hardware and a fully remote-control interface [65]. The system integrates four SMUs for standard DC measurements, one 4225-PMU module for fast pulsed and transient characterization, paired with two 4225-RPM units for automatic switching between DC and pulsed operation, which were installed but not utilized in this setup [67].

While the hardware platform remains the same, the operational mode differs fundamentally. Instead of being controlled through the Clarius graphical user interface, the 4200A-SCS in this setup operates entirely via remote communication using the KXCI interface [68]. All measurement commands, parameter definitions, and sequencing are transmitted from the workstation through a TCP/IP connection, allowing the instrument to execute predefined routines autonomously. This remote control mode provides direct access to the underlying hardware functions of the analyzer and eliminates the need for user interaction during measurement runs.

Compared to the Cascade setup, this configuration removes the limitations imposed by the VAR1/VAR2 sweep structure, allowing multiple independent bias parameters to be externally controlled. In addition, all measurement data are transferred directly to the workstation and stored in a unified format for subsequent analysis. The resulting setup combines the precision of the Keithley measurement hardware with the flexibility of a fully programmable control environment, enabling continuous, unsupervised device characterization over extended time scales. The integration of the analyzer into the automated control framework is realized through a custom Python framework described in detail in the following subsection.

3.2.3.2 Python-based Control Framework

The automation and synchronization of all instruments in the semi-automatic measurement setup were implemented using a custom Python-based control framework developed under the supervision of the author. The software coordinates the communication between the PA300 probe station and the external temperature controller, and the Keithley 4200A-SCS parameter analyzer, providing a unified interface for fully automated device characterization. The prober and analyzer communicate with the workstation via Ethernet and are controlled using the NI-VISA framework for standardized instrument communication. The temperature commands and feedback are forwarded from the prober to the temperature controller via GPIB. This design allows direct hardware access through TCP/IP commands without relying on proprietary user interfaces.

The program is structured into two principal components: the measurement module, which defines the measurement routines and manages the communication with the analyzer, and the main script, which orchestrates the complete measurement flow, including wafer

TU WIEN Bibliothek Your knowledge hub
Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.

navigation and temperature control. This modular separation provides a clear hierarchy between low-level instrument commands and high-level process automation.

The measurement module implements a library of predefined characterization routines that can be executed independently as part of a larger measurement campaign. Predefined routines include transfer and output characteristics, program gate and drain sweeps, and multi-dimensional large-parameter sweeps. Each routine defines the required bias configuration for the analyzer, including which SMUs are used, the sweep type (voltage or current), the step count, and compliance limits. Communication with the 4200A-SCS is handled through its KXCI command interface, which accepts SCPI-like instructions via TCP/IP sockets. The module compiles the appropriate command sequences, transmits them to the analyzer, and retrieves the resulting measurement data. All measurement data are stored in a structured directory hierarchy organized by device identifier, measurement type, and temperature. Each dataset includes the complete raw data, the configuration parameters, and an automatically generated plot for visual inspection. This ensures reproducibility and traceability of every individual measurement.

In contrast to the VAR1/VAR2 sweep logic of the internal Keithley firmware, the Python implementation allows flexible nesting of multiple sweep parameters. This enables complex multi-dimensional measurements in which several voltages or currents are varied hierarchically within a single automated run. For example, in a Large Parameter Sweep (Subsection 3.3.5), the inner loop may vary the control gate voltage V_{CG}, followed by the program gate voltage V_{PG}, the drain-source voltage V_{DS}, and finally the device index and temperature. This structure effectively replaces the limited two-dimensional sweep capability of the instrument with an arbitrarily scalable software-driven loop hierarchy, providing full freedom over the experimental parameter space.

The main control script defines the experimental configuration and executes the measurement sequences across multiple devices and temperatures. It contains the global parameters such as measurement compliance, voltage and current limits, device spacing, device matrices, and the list of measurement routines to be executed. The program begins by initializing communication with the instruments and calibrating the wafer coordinate system. Once reference points are set, all device positions are calculated automatically. The PA300 probe station is then instructed to move to the first device coordinates, and the analyzer executes the selected measurement routines. After all devices at a given temperature are completed, the system adjusts the chuck temperature to the next setpoint and repeats the full sequence.

The system operates autonomously once sample alignment and prober coordinate calibration are completed and the measurement parameters, device matrix, and temperature sequence are defined. A single automated characterization cycle can last up to 24 hours per device and several days for complete wafer maps without requiring human supervision. The integration of the analyzer, prober, and temperature controller into a single

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU WIEN Bibliothek Your knowledge hub

programmable control environment therefore represents a major advancement over the previous setups, enabling continuous, unsupervised, and highly reproducible electrical characterization across multiple devices and temperatures.

3.2.4 Transient Measurement

The transient measurement setup represents a further development of the automated measurement environment established in this work. It extends the Python-based control framework introduced for the Semi-Automatic Needle Prober setup by integrating pulse generation and transient data acquisition. This configuration combines the precise bias and pulsing capabilities of the Keithley 4200A-SCS system with the high temporal resolution of a Zurich Instruments MFLI Lock-In Amplifier operated in scope mode. The setup was developed entirely in the course of this work and enables transient characterization of reconfigurable transistor circuits with significantly higher time resolution compared to the measurements previously performed with the Karl Suss Needle Prober setup. The layout of the setup is illustrated in Fig. 3.6.

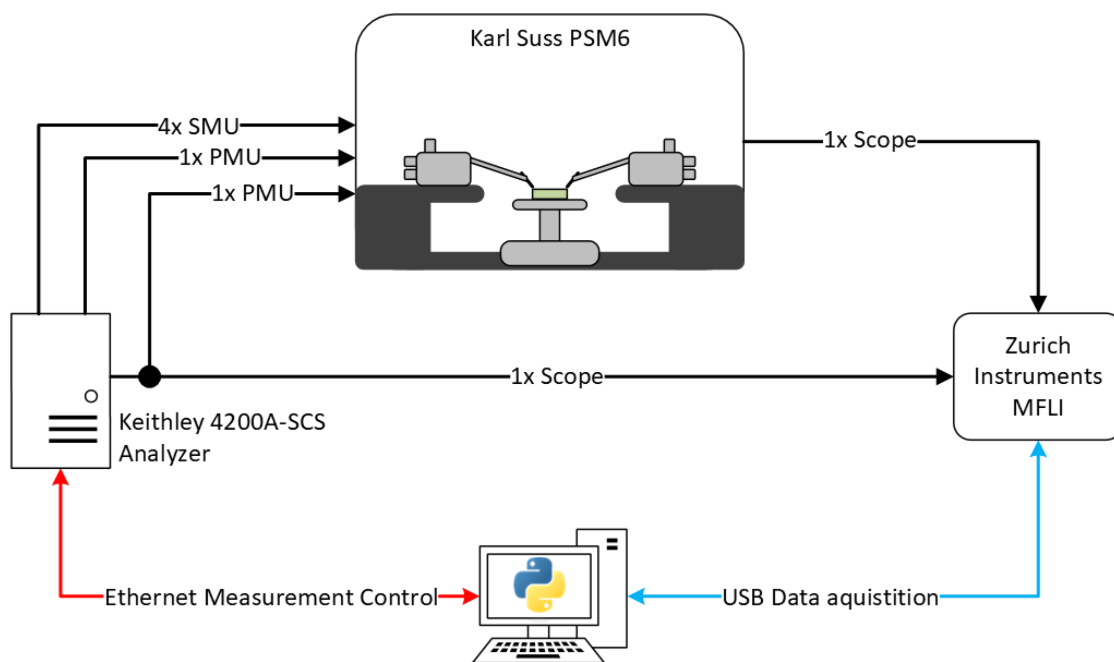


Figure 3.6: *Layout of the Transient Measurement setup. The Workstation controls the 4200A-SCS Analyzer via Python over an Ethernet connection. Data acquisition is performed via a USB connection to the MFLI.*

The transient measurements were carried out using the Karl Suss PSM6 manual probe station as described in Sec.3.2.1. Nevertheless, the transient measurement equipment is fully modular and portable and can be used with any probe station providing a sufficient number of micro positioners.

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU Bibliothek Your knowledge hub WIEN

3.2.4.1 Keithley 4200A-SCS Parameter Analyzer - pulsed operation

The bias voltages required for transient characterization were generated using the Keithley 4200A-SCS Parameter Analyzer equipped with four SMUs, one 4225-PMU, and two 4225-RPM units. The analyzer was controlled via the same Python-based framework employed in the PA300 setup through the KXCI remote interface. The SMUs provided stable DC bias conditions for the devices under test, while the PMU channels were used to generate input pulses with programmable amplitude, duration, and repetition rate. The RPM units allowed use of both PMU channels. This configuration provided synchronized pulse generation and bias control within a single automated measurement environment.

The 4225-PMU module supports pulse amplitudes up to $\pm 40\ V$ and current range up to $\pm 800\ mA$, with programmable pulse widths ranging from 20 ns to 1 s. The output waveform is digitized at up to 200 MSa/s with 16-bit vertical resolution and a typical timing jitter below 2 ns [69]. Each channel can either source voltage and measure current or source current and measure voltage. Consequently, it is not possible to generate an input pulse with one channel and record the corresponding voltage response on the other. Furthermore, circuits such as transmission gates require complementary pulsing of both input terminals, which occupies both PMU channels and leaves no channel available for time-domain signal detection. These hardware constraints motivated the integration of an external transient acquisition system based on the Zurich Instruments MFLI Lock-In Amplifier.

3.2.4.2 Zurich Instruments MFLI

To record the transient output signals, a Zurich Instruments MFLI Lock-In Amplifier equipped with the MF-DIG upgrade was employed. While the instrument is primarily designed for phase-sensitive detection, it also provides a high-performance scope mode that enables direct time-domain signal acquisition. The MFLI was connected to the workstation via USB and controlled using the Zurich Instruments LabOne API. During measurements, the input pulse waveform was recorded via the Aux In 1 channel, while the circuit output was connected to the high-impedance Voltage In input.

The Voltage In input stage provides an input impedance of 10 $M\Omega \parallel < 1\ pF$ and a maximum input range of $\pm 3\ V$, minimizing loading of the measured circuit. The analog-to-digital converter operates with 16-bit vertical resolution and supports sampling rates up to 60 MSa/s in scope mode, corresponding to a temporal resolution of approximately 17 ns [70]. The MF-DIG option extends the instrument's functionality with a second digitizer channel, enabling differential or dual-point time-domain measurements with sampling synchrony better than 1 ns.

In contrast to a conventional oscilloscope, the MFLI combines high sampling rates with high input impedance, making it particularly suitable for transient measurements on high-impedance semiconductor devices where a standard 1 $M\Omega$ oscilloscope input would signif-

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU Bibliothek Your knowledge hub WIEN

icantly distort the measured signal. The 16-bit ADC and the low-noise analog front end ensure a typical input noise density below 5 $nV/\sqrt{Hz}$ at 100 kHz, providing excellent signal fidelity even for low-amplitude transients.

Triggering and synchronization were handled internally by the MFLI, which served as the master timing and acquisition unit. The Python control program coordinated the bias and pulse generation sequence via the Keithley analyzer, while the MFLI operated as an independent data acquisition device. The recorded waveforms were saved directly on the workstation connected to the MFLI.

A future extension of the framework could include a complete integration of the MFLI via its Ethernet interface into the Python control layer, allowing synchronized control and data acquisition within a single program environment. Even in its current configuration, the system represents a significant advancement over earlier configurations. The combination of the Keithley 4200A-SCS and the Zurich Instruments MFLI provides both precise biasing and high temporal resolution, enabling transient characterization with sub-microsecond accuracy that was not achievable with any of the earlier measurement configurations used prior to this work.

3.3 Electrical Characterization

The electrical characterization provides a comprehensive understanding of the static and dynamic behavior of the fabricated RFET devices. It forms the experimental foundation for evaluating device performance, verifying the reconfigurability concept, and supplying data for compact modeling.

The characterization comprises several types of measurements that target different aspects of device behavior. The transfer characteristic represents the fundamental dependence of the output on the input parameter. The output, PG sweep, and V_D sweep measurements were implemented to extend the framework toward a complete set of bias-dependent characterization routines, even though their results are not presented in this work. Beyond these static measurements, the large parameter sweep and transient measurement provide multidimensional and time-resolved insights into the RFET behavior.

3.3.1 Transfer Characteristic

The transfer characteristic provides the fundamental description of the device behavior under variation of the gate potential. In this measurement, the drain current I_D is recorded as a function of the applied gate voltage, while the remaining terminal voltages are kept constant. The transfer characteristic reflects the gate control over the channel and allows the extraction of key parameters such as the threshold voltage V_{TH}, the transconductance g_m, and the subthreshold slope.

For the SBFET configuration, the measurement is performed by sweeping the gate voltage

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU WIEN Bibliothek Your knowledge hub

V_G while keeping the drain and source terminals at fixed bias levels, typically $V_D = +1\ V$ and $V_S = -1\ V$, resulting in a drain-source bias $V_{DS} = 2\ V$. The resulting I_D-V_G curve exhibits ambipolar behavior with current flow for both positive and negative gate voltages, as expected for Schottky barrier FETs. The current is typically evaluated and plotted as its absolute value.

In contrast, the RFET employs two independently biased gates. The PG defines the device operation mode by setting the dominant charge carrier type, while the CG modulates the channel conductance. During the transfer measurement, V_{PG} is fixed to either a positive value for n-type or a negative value for p-type operation, and V_{CG} is swept across the defined voltage range. Consequently, two transfer curves are obtained, representing the complementary conduction modes of the device.

Measurements are conducted either in a single sweep or as a dual sweep, where the voltage is ramped forward and backward to reveal hysteresis effects. The sweep direction, from on-state to off-state or vice versa, can be selected depending on the measurement objective. The resulting curves provide insight into threshold control and hysteresis effects caused by interface states.

When considering complete circuit configurations rather than single devices, the concept of the transfer characteristic can be extended accordingly. In such cases, the circuit exhibits a defined input and output quantity, for example an input voltage V_{IN} and an output voltage V_{OUT}. The corresponding transfer characteristic $V_{OUT}(V_{IN})$ describes how the circuit converts or amplifies the input signal and thus provides information about the overall functionality and signal behavior of the system. This approach allows the evaluation of circuit-level performance parameters such as gain, transfer symmetry, and switching behavior.

3.3.2 Output Characteristic

The output characteristic describes the drain current I_D as a function of the applied drain-source voltage V_{DS} for various gate voltage levels. It provides insight into current saturation, channel resistance, and the transition between linear and saturation regions.

For the SBFET, the output measurement is implemented by sweeping V_{DS} between its minimum and maximum values while stepping the gate voltage V_G. The gate voltage defines the channel state for each drain sweep, resulting in a family of output curves $I_D(V_{DS})$ for discrete V_G levels. The source is typically grounded (asymmetric measurement) or biased symmetrically with respect to the drain ($V_D = -V_S$). The complete data set is often visualized as a color map, where V_{DS} and V_G define the two axes and I_D is represented by color intensity.

For the RFET, the corresponding measurement uses the control gate voltage V_{CG} instead of V_G and includes a constant program gate bias V_{PG} to fix the operation mode. Two

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU WIEN Bibliothek Your knowledge hub

complete output characteristics are acquired, one for the p-type and one for the n-type mode, yielding complementary color maps.

3.3.3 PG Sweep

The PG sweep measurement is specific to the RFET and demonstrates its reconfigurability. In this two-dimensional sweep, the program gate voltage V_{PG} and the control gate voltage V_{CG} are both varied systematically to map the transition between p-type and n-type conduction. During the measurement, the drain and source terminals are biased at fixed symmetric levels, and the drain current I_D is recorded for each pair of gate voltages.

In practical implementation, V_{PG} is stepped over the defined polarity range, while for each PG level, V_{CG} is swept across its complete range. The resulting data are represented as two-dimensional color maps with V_{CG} on one axis and V_{PG} on the other, and the magnitude of I_D encoded by color. These PG sweep maps reveal the voltages at which the device transitions between p-type and n-type operation, providing direct evidence of its reconfigurable operation.

3.3.4 VD Sweep

The VD sweep characteristic represents a measurement configuration analogous to the output characteristic but with interchanged sweep sequence. Instead of sweeping V_{DS} for fixed gate steps, the gate voltage is swept completely at each discrete V_{DS} bias level. This approach yields equivalent information about the current modulation and channel transport while also serving as a reproducibility and consistency check for the obtained output data.

For the SBFET, the drain-source bias V_{DS} is set stepwise within the desired range, and for each step the gate voltage V_G is swept. The routine can be performed using symmetric ($V_D = -V_S$) or asymmetric bias configurations. For the RFET, the control gate voltage V_{CG} is swept, while the program gate voltage V_{PG} remains constant at the value defining the desired conduction mode. Hence, two VD sweep data sets are recorded per device, one for each operation type. The resulting I_D-V_{CG} curves complement the output data and are evaluated in the same way.

3.3.5 Large Parameter Sweep

The Large Parameter Sweep measurement was carried out to obtain a comprehensive multidimensional data set that enables the physical analysis and modeling of the RFET operation. The motivation for this measurement originates from the EU project Sensoteric, within which this thesis was conducted. As part of the project, the TU Darmstadt performs numerical RFET simulations based on a Verilog-A table model. Such a model describes the device behavior not analytically but by interpolating experimental data tables. To build this model in a physically consistent and numerically stable way, large data sets covering multiple bias dimensions are required. The Large Parameter Sweep performed

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU Bibliothek Your knowledge hub WIEN

in this work provides this data basis, linking experimental device characterization with compact modeling and circuit simulation.

In this measurement, the drain-source bias V_{DS}, the program gate voltage V_{PG}, and the control gate voltage V_{CG} were varied systematically at different temperature levels. The corresponding drain current I_D was recorded for each parameter combination.

The measurement sequence was carried out for four temperature points, 25 $°C$, 50 $°C$, 75 $°C$ and 100 $°C$. At each temperature, the prober set the sample contact and maintained thermal stability before the bias sweep started. The drain-source voltage V_{DS} was varied by setting $V_D = -V_S$, sweeping V_D from $+1$ V to -1 V in steps of 0.1 V. For each V_{DS} point, a series of PG Sweep measurements, as described in Subsection 3.3.3, was performed, each capturing a two-dimensional $I_D(V_{PG}, V_{CG})$ data set.

To maintain high resolution while respecting the internal memory limitations of the Keithley 4200A, the complete V_{PG} range from -5 V to $+5$ V was divided into four subranges: -5 V to -2.5 V, -2.5 V to 0 V, 0 V to 2.5 V, and 2.5 V to 5 V, all with a step size of 0.1 V. Each subrange was measured as an individual routine, with short pauses between runs to allow for electrical and thermal stabilization. In the postprocessing step, the four partial sweeps were combined to reconstruct the full high-resolution data matrix across the entire V_{PG}-V_{CG} range. This segmentation prevents the instrument memory from overflowing while preserving the fine granularity of the sweep.

During each measurement, the source and drain voltages were kept constant at the selected V_{DS} value, while the control gate voltage V_{CG} was continuously swept over the entire voltage range from -5 V to $+5$ V. The sweep direction of V_{CG} changed between successive subranges to capture both p-type and n-type transfer characteristics from on-state to off-state.

The resulting data set forms a multidimensional parameter space described by

$$I_D = f(T, V_{DS}, V_{PG}, V_{CG}),$$

which enables the analysis of reconfigurability, operational symmetry and temperature dependence. Furthermore, it provides a comprehensive experimental foundation for the Verilog-A modeling of the RFET performed by the TU Darmstadt.

3.3.6 Transient Measurement

The transient measurement investigates the dynamic switching behavior of the RFET-based transmission gate under time-varying control gate signals. In contrast to the quasi-static measurements discussed in the previous sections, which evaluate steady-state current-voltage characteristics, this measurement focuses on the temporal response of the output voltage V_{OUT} to pulsed gate stimuli. It provides information about the switching

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU WIEN Bibliothek Your knowledge hub

speed and transient behavior of the device during the transition between the conducting and non-conducting states.

The measurement was carried out using the setup described in Subsection 3.2.4. Two PMU channels applied synchronized but phase-inverted 5 V pulses to the two control gates V_{CG1} and V_{CG2} of the transmission-gate configuration. During the measurement, the program gates V_{PG} were kept at constant bias levels of $-5\ V$ and $+5\ V$, defining the device configuration, while the input voltage V_{IN} was set to a constant value of 1 V. The output voltage V_{OUT} was recorded using a Zurich Instruments MFLI Lock-In amplifier.

The output terminal of the transmission gate is connected to a load resistor R_L of 100 $M\Omega$ referenced to ground. The measured output voltage V_{OUT} therefore follows the dynamic response of the channel resistance R_{CH} relative to the load, described by

$$V_{OUT} = V_{IN} \frac{R_L}{R_L + R_{CH}}.$$

In the on-state ($R_{CH} \ll R_L$), V_{OUT} approaches V_{IN}, whereas in the off-state ($R_{CH} \gg R_L$), V_{OUT} tends toward zero. The transient evolution of $V_{OUT}(t)$ thus directly reflects the switching dynamics of the transmission gate.

In the standard configuration, the control gate voltages are pulsed between $-5\ V$ and $+5\ V$ in a complementary manner, that is $V_{CG2} = -V_{CG1}$. The pulse period T_P is typically 0.1 s, with a pulse width of approximately 50 ms and rise and fall times of 100 ns. The number of cycles is defined by the pulse count parameter, usually set to 10. The MFLI records the output voltage $V_{OUT}(t)$ synchronously with the gate pulse train, providing a time-resolved view of the transmission and blocking phases of the device.

The transient measurement is not limited to rectangular gate pulses as described above. Instead, it allows the generation and execution of arbitrary waveform sequences with freely defined amplitude, timing, and phase relations within the limits described in Subsection 3.2.4. This flexibility enables the investigation of complex transient phenomena and signal responses beyond conventional two-level switching. For instance, it has been successfully applied to the study of multi-value logic inverters, where the control gates are driven by non-binary voltage waveforms to emulate multi-level logic operation. Although such experiments are not part of this thesis, they demonstrate the versatility and scalability of the implemented framework for future studies of dynamic and reconfigurable logic circuits.

The experimental techniques presented in this chapter establish the complete methodological framework used throughout this thesis. The fabrication overview provides the physical basis of the GeSOI RFET platform, while the different measurement setups enable reliable and reproducible electrical characterization for extracting relevant device and circuit parameters. Together, these methods lay the foundation for the analysis and interpretation of the experimental results discussed in Chapter 4.

TU Bibliothek WIEN Your knowledge hub
Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU WIEN Bibliothek Your knowledge hub

Chapter 4

Results and Discussion

This chapter presents the experimental results obtained in the course of this work and discusses their implications for reconfigurable device and circuit design. It begins with a summary of the technological and methodological evolution (4.1) that forms the basis for the subsequent measurements, highlighting the progression from the first to the third generation of GeSOI reconfigurable field effect transistors.

The following sections provide a detailed characterization of the GeSOI 20 (4.2) and GeSOI 21 (4.6) platforms, including their transfer behavior, symmetry, temperature dependence, and achievable on-to-off ratios.

Based on these device level insights, the circuit capabilities of both generations are investigated, covering complementary logic (4.3), common source (4.4, 4.7) and common drain amplifier (4.5, 4.8) configurations and finally the reconfigurable transmission gate (4.9).

Together, the presented results demonstrate the advances in device fabrication, measurement methodology, and circuit functionality, and establish the third generation as the most robust and highest performing platform developed in this work.

4.1 Project Evolution

The work presented in this thesis builds on the foundation established in [10]. In this initial study, fundamental analog circuits were realized using the first generation GeSOI RFET.

To interpret the measured improvements across the three device generations, it is important to clarify the technological origin of the samples. All three generations were realized on chips originating from the same GeSOI wafer material provided by JKU Linz. The

transition from the first generation GeSOI 14 devices to the second generation GeSOI 20 devices was accompanied by a change in the top gate metallization from TiAu to TiAl, which affects the gate stack and can influence electrostatics, interface quality, and bias stress behavior. Between the second generation GeSOI 20 and the third generation GeSOI 21, the fabrication flow remained unchanged. Therefore, the observed differences between GeSOI 20 and GeSOI 21 are attributed primarily to sample to sample variability within the GeSOI wafer. In particular, the processed chip may originate from different wafer locations, such as the center and the edge region, which can lead to variations in film thickness, defect density, or strain conditions and thereby modify the balance between electron and hole injection as well as trap related effects.

The first part of the present work focused on the development of new measurement setups and a significantly expanded characterization methodology. The introduction of the large parameter sweep, as described in Subsec. 3.3.5, enabled the extraction of complete device characteristics across all combinations of Temperature, V_{PG}, V_{CG}, and V_{DS}. These data sets were used to create table based device models and to support device simulation for subsequent fabrication or circuit implementation. In parallel, a transient measurement setup (Subsec.3.3.6) capable of generating and measuring pulses up to 100 MHz while providing state-of-the-art DC semiconductor biasing was implemented. This provided access to the dynamic behavior of the reconfigurable devices and the circuits derived from them.

The second generation GeSOI 20 devices demonstrated substantial improvements in circuit level performance compared to the first generation. A symmetric complementary inverter centered around was realized, showing equal switching behavior for both polarities. In addition, the use of an active load instead of an external resistor enabled compact and fully integrated common drain and common source amplifier configurations. The common drain amplifier exhibited gain levels comparable to the first generation but now without external components, while the common source amplifier exceeded unity gain for the first time with values above 1. These results confirmed the benefits of improved device symmetry and the advantages of active load operation in the reconfigurable architecture.

The third generation GeSOI 21 devices continued this development and achieved further improvements in gain, symmetry, and dynamic performance. The common drain amplifier reached gain values up to 0.75, while the common source amplifier achieved maximum gains close to 11, representing an order of magnitude improvement over the previous generation. Furthermore, the enhanced symmetry and reduced trap influence enabled the realization of a new bidirectional transmission gate circuit. This circuit was demonstrated both in direct current measurements and in transient operation at 10 Hz, showing stable switching and adjustable transmission behavior. These results highlight the progress from early proof of concept implementations toward fully functional and reconfigurable analog circuit elements based on germanium on insulator RFET technology.

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU WIEN Bibliothek Your knowledge hub

4.2 GeSOI 20 Basic Characterization

The electrical characterization of the second generation GeSOI 20 devices was carried out to evaluate their reconfigurable operation and temperature dependent behavior. To investigate the electrostatic control and carrier injection properties, a comprehensive large parameter sweep as described in Subsec. 3.3.5 was conducted on the reference structures. During the measurements, the drain and source terminals were biased symmetrically at $V_D = -V_S$, from $V_{DS} = 2\ V$ to $-2\ V$, while the drain current $|I_D|$ was recorded as a function of the control gate voltage V_{CG} for various program gate voltages V_{PG}. The program gate voltage was stepped from $-5\ V$ to $5\ V$ in equidistant steps and the procedure was repeated for multiple temperatures to assess the thermal dependence. Representative subsets of the measurement data are shown in Fig. 4.1(a)-(c) for $T = 323\ K$, $T = 348\ K$, and $T = 373\ K$.

The transfer characteristics exhibit the ambipolar behavior typical of reconfigurable field effect transistors. The polarity of the device can be continuously adjusted by V_{PG}, resulting in a smooth transition between p-type conduction for negative V_{PG} and n-type conduction for positive V_{PG}. For $V_{PG} \leq 0\ V$, a pronounced p-type operation is observed with an on region for $V_{CG} < 0\ V$ and an off state above $V_{CG} > 2\ V$. Within this range, the on current I_{on}^p decreases slightly with increasing V_{PG}, whereas the off current I_{off}^p remains nearly constant. For $V_{PG} \geq 2.5\ V$, the transistor switches to n-type operation. In this regime, the on current I_{on}^n increases with V_{PG}, accompanied by a moderate rise in off current I_{off}^n. Between these regions, a transition zone occurs where neither conductiontype dominates. Around $V_{PG} \approx 1.5\ V$, the current at strongly negative and strongly positive V_{CG} is lower than at $V_{CG} = 0\ V$, representing the ambipolar minimum where both injection barriers are balanced.

A quantitative comparison of the extracted current levels is summarized in Tab. 4.1. At all investigated temperatures, the GeSOI 20 devices exhibit the characteristic increase of both on and off currents with temperature. The rise in current magnitude can be attributed to thermionic emission and thermionic field emission. With increasing temperature, charge carriers gain higher potential energy, which reduces the effective barrier height for thermionic emission and enhances the tunneling probability through the Schottky barriers for thermionic field emission.

Table 4.1: *Extracted current levels for the GeSOI 20 RFET at different temperatures.*

	$T = 323\ K$	$T = 348\ K$	$T = 373\ K$
I_{on}^p	1.8 μA	2.4 μA	6 μA
I_{on}^n	800 nA	1 μA	3.5 μA
I_{off}^p	8 pA	30 pA	60 pA
I_{off}^n	60-170 pA	350-500 pA	1-3 nA

For the p-type operation, the on current I_{on}^p increases from 1.8 μA at $T = 323\ K$ to 6 μA at $T = 373\ K$, while the off current I_{off}^p rises from 8 pA to 60 pA. The n-type operation

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU WIEN Bibliothek Your knowledge hub

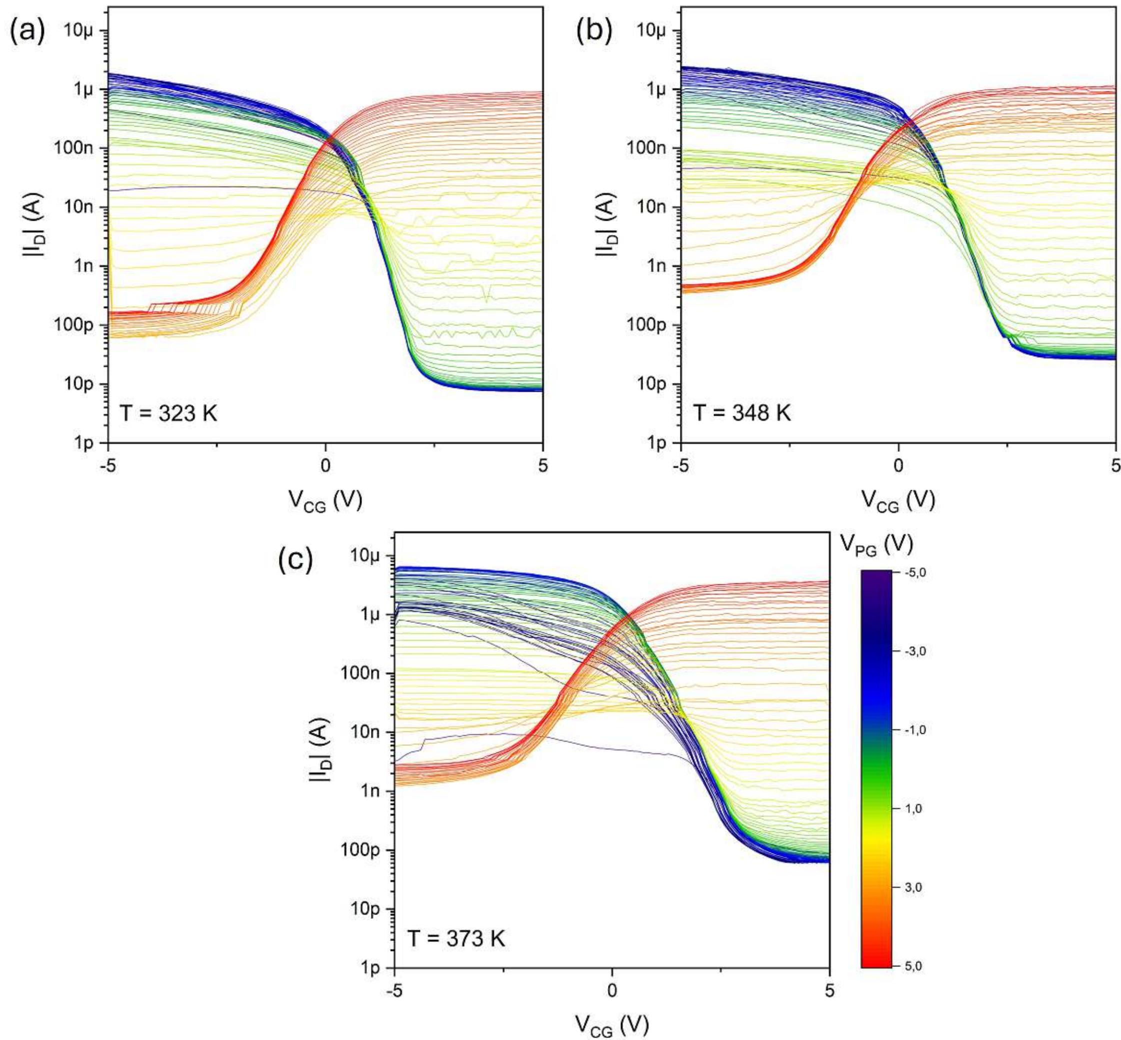


Figure 4.1: *Subset of Large Parameter Sweep of the second generation GeSOI 20 RFET for different program gate voltages V_{PG} at three temperatures. The drain current $|I_D|$ is plotted as a function of the control gate voltage V_{CG} for (a) $T = 323\ K$, (b) $T = 348\ K$, and (c) $T = 373\ K$. The color scale indicates the program gate voltage V_{PG} from $-5\ V$ (blue) to $5\ V$ (red). All measurements were performed with symmetric biasing of drain and source at $V_D = -V_S = 0.9\ V$.*

follows the same trend with I_{on}^n increasing from 800 nA to 3.5 μA and I_{off}^n rising from approximately 100 pA to about 2 nA. This proportional increase across both polarities confirms the symmetric influence of temperature on the injection barriers for electrons and holes. The results demonstrate that the GeSOI 20 devices maintain their reconfigurable functionality across the entire temperature range without degradation of the ambipolar transition.

Minor irregularities are visible in the experimental data but are attributed to the measurement setup rather than the device. In the n-type regime at $T = 323\ K$, discrete

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU Bibliothek Your knowledge hub WIEN

current steps between approximately 230 pA and 170 pA occur due to automatic current range switching of the analyzer. This artifact can be avoided by using longer integration times and was eliminated in subsequent measurements. Additionally, the transfer curves for $V_{PG} = -5\ V$ lie slightly below those for higher V_{PG} values, which results from charge trapping and accumulation effects during the sequential acquisition of the large parameter sweep. These effects intensify for higher temperatures, corresponding to later stages of the measurement sequence.

Despite these measurement related deviations, the overall behavior of the GeSOI 20 devices is highly symmetric with respect to the control gate voltage even though germanium typically favors p-type conduction due to Fermi level pinning near the valence band. The observed balance between both conduction-types arises from the thin silicon interlayer introduced during fabrication, as discussed in Sec. 3.1. This interlayer shifts the effective Fermi level toward the midgap, resulting in comparable Schottky barrier heights for electron and hole injection. This observation is remarkable for a germanium channel since previous Ge on SOI RFETs as presented by Fuchsberger et al. [57] show on-current ratios I_{on}^{p}/I_{on}^{n} of 1.96 ± 1.78, while first generation devices from Dobler [10] show a ratio of 4.1. The presented GeSOI 20 device exhibits a ratio of 1.43 at 373 K. The obtained symmetry confirms the effectiveness of the Al-Si-Ge multi-heterojunction contact technology and validates the GeSOI 20 platform as a stable and reconfigurable transistor generation.

4.3 GeSOI 20 Complementary Inverter

To verify the complementary functionality and demonstrate the circuit capability of the GeSOI 20 platform, an inverter structure was realized. by connecting two RFETs in series. The upper transistor operates in p-type mode with $V_{PGH} = -5\ V$, while the lower transistor is configured in n-type mode with $V_{PGL} = 5\ V$. The control gates are connected together and driven by a common input voltage $V_{CGH} = V_{CGL} = V_{IN}$. The output node is located at the connection point the two transistors and the supply terminals are biased at $V_{DD} = -1\ V$ and $V_{SS} = 1\ V$, resulting in $V_{DS} = 2\ V$. The resulting transfer characteristic is shown in Fig. 4.2.

The transfer characteristic shows the expected complementary switching behavior. For negative input voltages, the p-type transistor in the upper branch conducts, resulting in an output voltage close to the positive supply V_{SS}. As the input voltage increases, the p-type device gradually turns off, while the n-type device becomes conductive. The output voltage therefore transitions sharply from V_{SS} to V_{DD}, corresponding to a logical inversion of the input signal. The inverter exhibits a symmetric voltage transfer curve with a switching point close to $V_{IN} = 0\ V$, confirming the balanced characteristics of the two transistors. Although a hysteresis of approximately 1 V is visible, it does not affect the functionality of the inverter, as it is centered around $V_{IN} = 0\ V$ and far from the discrete switching levels of $V_{CGH} = \pm 5\ V$.

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU Bibliothek WIEN Your knowledge hub

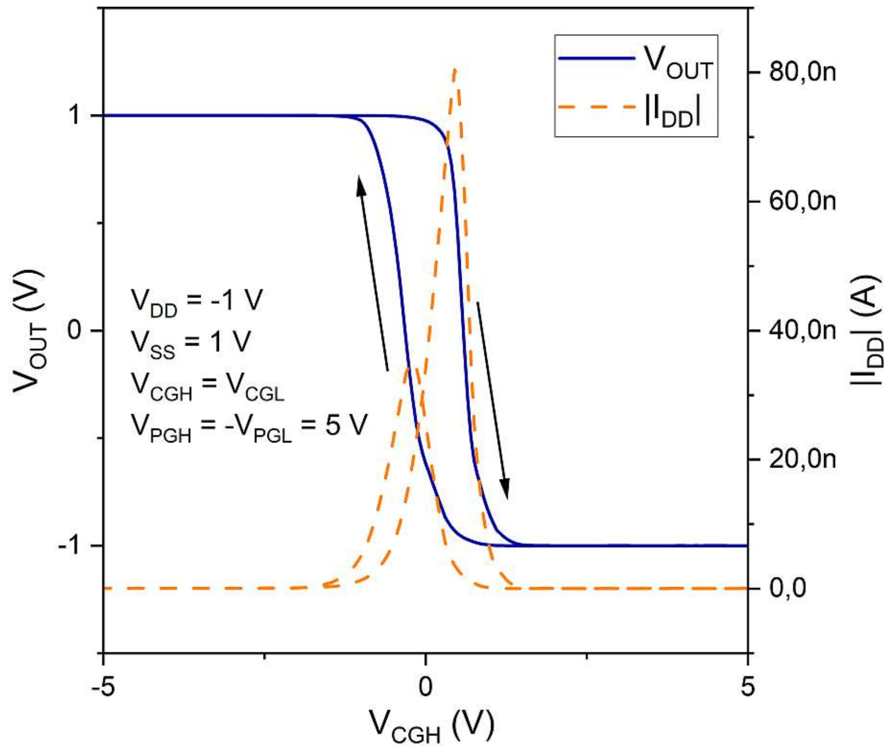


Figure 4.2: *Complementary Inverter transfer characteristic of the GeSOI 20 sample. The output voltage V_{OUT} (blue) and the absolute supply current $|I_{DD}|$ (orange) are plotted as a function of the common control gate voltage $V_{CGH} = V_{CGL}$. The circuit had a symmetric source and drain bias of $V_{SS} = -V_{DD} = 1\ V$ with complementary program gate voltages of $V_{PGH} = -5\ V$ and $V_{PGL} = 5\ V$.*

The corresponding supply current $|I_{DD}|$ exhibits a narrow peak around the transition voltage, which corresponds to the short interval during which both transistors are partially conductive. An interesting observation is the difference in the current peak magnitude between the first and second switching events, showing approximately 35 nA for the first transition and 80 nA for the second. This behavior can be attributed to charge trapping effects within the gate stack and the Al-Si-Ge multi-heterojunction junction regions. During the first switching cycle, the traps are largely unoccupied and therefore do not influence the potential distribution within the channel region. After the initial transition, a fraction of these traps becomes charged, modifying the local electrostatics and delaying the subsequent detrapping process during the return sweep. This dynamic trap charging results in a higher overlap of the conductive states of the p-type and n-type devices, leading to the increased peak current observed during the second switching event. Outside the transition region, the supply current remains low, confirming proper complementary behavior and minimal leakage in both logic states. The extracted static power consumption is below the nanowatt range for all input voltages, demonstrating the suitability of

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU WIEN Bibliothek Your knowledge hub

the GeSOI 20 technology for low power operation.

The measured symmetry and sharp switching characteristics indicate that the fabrication and contact scheme of the GeSOI 20 generation yield closely matched n-type and p-type devices. The balanced Fermi level alignment achieved by the silicon interlayer ensures nearly equal Schottky barrier heights for both carrier polarities. As a result, the inverter exhibits a well centered switching voltage and equal output swing for positive and negative supply rails. These results confirm that the GeSOI 20 platform enables the realization of complementary logic circuits based entirely on reconfigurable transistors.

Since the inverter configuration can be regarded as a common source amplifiers with active loads, operating in n-type mode for positive input voltages and in p-type mode for negative input voltages, it was a logical next step to investigate these amplifier configurations individually. For this purpose, the control gate potentials of both transistors were separated, allowing independent operation of each device. The corresponding measurements and analysis are presented in the following section.

4.4 GeSOI 20 Common Source Amplifier

To verify the hypothesis of an amplifier with an active load, two complementary sets of measurements were carried out. In the first experiment, transfer characteristics were recorded while varying the program gate voltage of the input transistor. In the second experiment, the program gate voltage of the active load transistor was varied instead. In both cases, a change in amplification was expected due to the dependence of the transconductance on the program gate voltage. A higher V_{PG} applied to the input transistor increases g_m and, according to Eq. 2.8, also increases the voltage gain A_V. The opposite behavior is expected for the active load transistor, where the control gate and program gate were connected to the same electrical potential. Increasing V_{PG} in this configuration raises the transconductance of the load device, but since this is accompanied by a reduction in channel resistance, the overall voltage gain of the amplifier decreases.

This controllability of the voltage gain was investigated as a function of temperature using the setup described in Subsec. 3.2.1. Transfer characteristics were measured for different program gate voltages and temperatures ranging from $T = 295\ K$ to $T = 398\ K$.

The first analysis focused on the dependence on the input, or control, transistor. Fig. 4.3 shows in (a) the measured transfer characteristics for program gate voltages from $V_{PGH} = -2.5\ V$ (red) to $V_{PGH} = -5\ V$ (blue) at $T = 373\ K$. The circuit schematic is shown as an inset, where the control transistor is highlighted. Subfigure (b) presents the calculated voltage gain $|A_V|$ of the amplifier as a function of the program gate voltage over the measured temperature range.

In the transfer characteristics, the voltage swing increases with the magnitude of the

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU WIEN Bibliothek Your knowledge hub

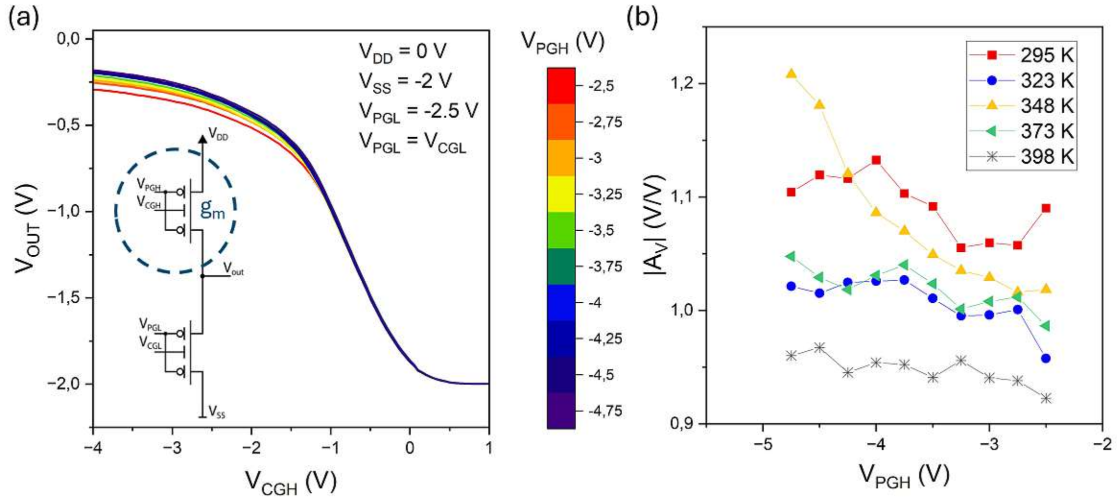


Figure 4.3: *Transfer characteristic of the GeSOI 20 p-mode common source amplifier showing the g_m variation. The output voltage V_{OUT} is plotted as a function of the control gate voltage V_{CGH} for various program gate voltages V_{PGH} from $-4.75\ V$ (blue) to $-2.5\ V$ (red). The circuit was biased at $V_{DD} = 0\ V$ and $V_{SS} = -2\ V$, with the load transistor fixed at $V_{PGL} = -2.5\ V$. (a) Measured transfer characteristic at $T = 373\ K$ and (b) extracted voltage gain $|A_V|$ as a function of V_{PGH} for different temperatures.*

program gate voltage. At low $|V_{PGH}|$ values, the on-resistance of the transistor is higher, causing stronger loading of the voltage divider even when the device is fully turned on. With increasing $|V_{PGH}|$, this loading effect decreases, leading to an enhanced voltage swing. Consequently, the slope of the transfer characteristic around the operating point, selected at approximately $V_{CGH} = -1\ V$, increases. As a result, the amplification rises with increasing $|V_{PGH}|$. This trend is also evident in Fig. 4.3(b), where the corresponding amplification values are shown as green triangles.

The investigated temperature dependence, on the other hand, does not reveal a consistent trend. All amplification curves exhibit a positive correlation between gain and the magnitude of the program gate voltage, but no systematic relationship between the individual temperatures. This observation can be attributed to charge trapping effects that occurred during the heating process and between measurement cycles. The common source g_m dependence was measured first at each temperature, which makes the data more susceptible to changes in ambient and surface charge conditions during the experimental sequence.

In a second measurement, the influence of the active load transistor on the overall amplifier behavior was examined. For this purpose, the control and program gate of the load transistor were connected to the same electrical potential, while the program gate voltage V_{PGL} was varied. The program gate voltage of the control transistor was kept constant at $V_{PGH} = -5\ V$. This configuration allows the load resistance R_L to be tuned electrostatically, directly influencing the voltage gain of the amplifier.

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU Wien Bibliothek Your knowledge hub

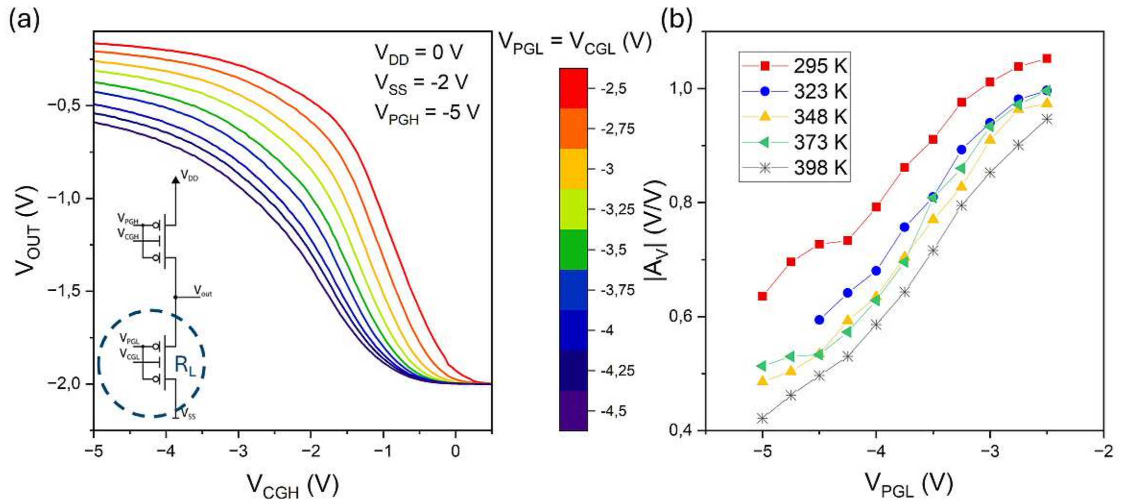


Figure 4.4: *Transfer characteristic of the GeSOI 20 p-mode common source amplifier showing the R_L variation. The output voltage V_{OUT} is plotted as a function of the control gate voltage V_{CGH} for various program gate voltages V_{PGL} from $-4.5\ V$ (blue) to $-2.5\ V$ (red). The circuit was biased at $V_{DD} = 0\ V$ and $V_{SS} = -2\ V$, with the control transistor fixed at $V_{PGH} = -5\ V$. (a) Measured transfer characteristic at $T = 323\ K$ and (b) extracted voltage gain $|A_V|$ as a function of V_{PGL} for different temperatures.*

The measured transfer characteristics for different V_{PGL} values at $T = 323\ K$ are shown in Fig. 4.4(a). As expected, the slope of the curves and the voltage swing depend strongly on the applied V_{PGL}. At lower $|V_{PGL}|$, the load device exhibits higher resistance, resulting in a larger voltage swing and steeper slope. Increasing $|V_{PGL}|$ lowers the effective resistance of the load transistor, which reduces the output voltage swing and consequently the amplification. The extracted absolute gain values for different V_{PGL} and temperatures are summarized in Fig. 4.4(b).

The data show that the amplifier gain decreases systematically with increasing temperature for all measured V_{PGL} values. This behavior can be attributed to thermally enhanced thermionic emission and thermionic field emission, which lead to an effective reduction in the output resistance of the load transistor. At higher temperatures, the increased carrier energy and enhanced barrier tunneling reduce the voltage swing and thereby the achievable voltage gain. The maximum gain of approximately $|A_V| = 1.1$ was obtained at $T = 295\ K$ and $V_{PGL} = -2.5\ V$, confirming the expected correlation between the load resistance and the voltage amplification.

It should be noted that, in contrast to the control transistor, the load transistor does not maintain a fixed operating point. In an actual circuit implementation, the program gate signal of the load device would therefore need to be coupled to the control transistor input in order to dynamically adjust the operating point. This coupling would ensure that the bias conditions of both transistors remain aligned and that the amplifier operates within

TU Bibliothek, WIEN Your knowledge hub
Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.

its intended linear region.

Overall, the measurements of the p-mode common source amplifier demonstrate that both the control transistor and the active load transistor have a significant influence on the overall amplification. The program gate voltage provides effective control of the transconductance of the amplifying device and the resistance of the load, allowing fine control of the gain and the operating point. The results confirm that the voltage gain increases with the magnitude of the program gate voltage applied to the control transistor and decreases with increasing $|V_{PGL}|$ at the load transistor. By exploiting these effects, adjustable amplifiers can be realized that enable temperature compensation through their inherent reconfigurability.

4.5 GeSOI 20 Common Drain Amplifier

After analyzing the common source amplifier, the corresponding common drain amplifier was investigated. The circuit configuration remained identical to the previous setup, with all connections and bias potentials at the source and drain kept constant. Only the roles of the control and load transistors were interchanged. The operating point was determined experimentally and measurements were carried out for temperatures from $T = 295\ K$ to $T = 398\ K$ in 25 K steps. As before, the control transistor was characterized first, followed by the investigation of the load transistor.

For the g_m variation, the load transistor was biased at a constant $V_{PGH} = V_{CGH} = -2.5\ V$ to ensure strong suppression, while the control transistor was swept at its control gate from $V_{CGL} = -5\ V$ to $5\ V$. At the same time, the program gate voltage of the control transistor V_{PGL} was varied from $-2.5\ V$ to $-5\ V$ in steps of $0.25\ V$. Fig. 4.5(a) shows the measured transfer characteristic at $T = 295\ K$, with the circuit schematic and the highlighted control transistor shown in the inset.

It can be observed that higher V_{PGL} values lead to a steeper transfer characteristic and thus a higher voltage gain compared to lower V_{PGL} values. The explanation follows the same reasoning as for the common source configuration: an increased program gate voltage enhances the transconductance, resulting in a higher gain as described by Eq. 2.12. The extracted gain values as a function of the program gate voltage and for different temperatures are shown in Fig. 4.5(b). A clear trend can be observed, indicating that the voltage gain increases with temperature. Furthermore, the positive correlation between gain and the magnitude of the program gate voltage is consistently observed across all temperatures.

The maximum measured voltage gain of approximately $|A_V| = 0.5$ remains below the theoretical unity limit. This deviation is attributed to the behavior of the active load transistor, which does not act as an ideal resistive element. Consequently, the simplified gain expression in Eq. 2.12 no longer captures the full small-signal behavior. Additional

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU WIEN Bibliothek Your knowledge hub

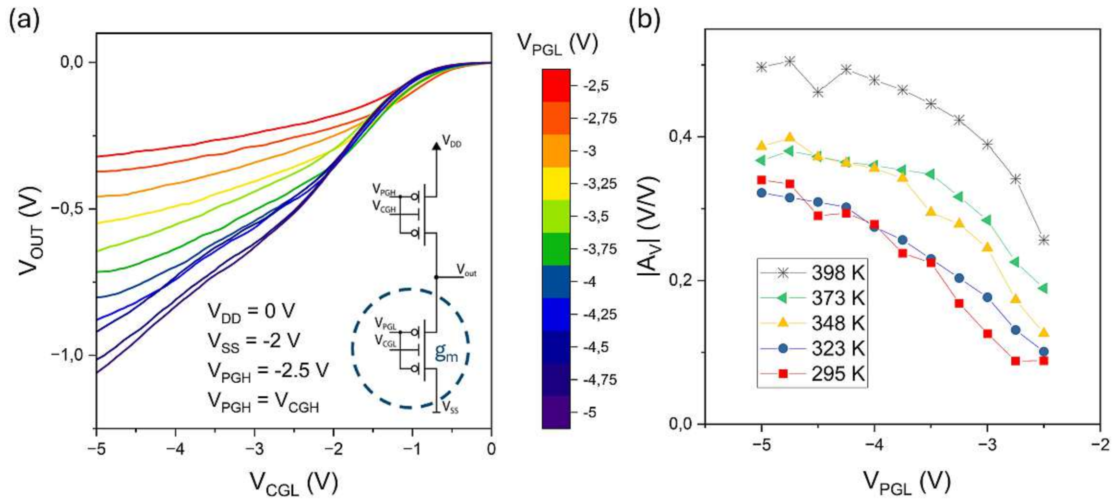


Figure 4.5: *Transfer characteristic of the GeSOI 20 p-mode common drain amplifier showing the g_m variation. The output voltage V_{OUT} is plotted as a function of the control gate voltage V_{CGL} for various program gate voltages V_{PGL} from -5 V (blue) to -2.5 V (red). The circuit was biased at $V_{DD} = 0\ V$ and $V_{SS} = -2\ V$, with the load transistor fixed at $V_{PGH} = -2.5\ V$. (a) Measured transfer characteristic at $T = 295\ K$ and (b) extracted voltage gain $|A_V|$ as a function of V_{PGL} for different temperatures.*

parameters such as the output conductance of the control transistor and the corresponding finite r_0 caused by the Early effect, contribute to the overall gain and effectively limit the attainable amplification.

It can also be seen that an operating point around $V_{CGL} = -1.5\ V$, which was used to calculate the voltage gains, is valid for all applied program gate voltages. This demonstrates that the circuit can be temperature compensated entirely through electrostatic control by adjusting the program gate voltage of the control transistor, without requiring any additional circuit complexity.

Furthermore, the transfer characteristic does not exhibit a continuously rising follower behavior as described in Sec. 2.5.2. Instead, the transfer characteristic gradually flattens toward the supply voltage. This behavior is also linked to the non-ideal nature of the active load transistor. Because the load does not behave as a purely resistive element, the control transistor is driven into the ohmic operating region, which causes the observed reduction in slope toward the supply voltage.

The same analysis was carried out for the load transistor. In this case, the program gate voltage of the control transistor V_{PGL} was fixed at $-5\ V$, while the program gate voltage of the load transistor $V_{PGH} = V_{CGH}$ was varied from $-2.5\ V$ to $5\ V$. For each value of V_{PGH}, transfer characteristics were recorded by sweeping the control gate voltage V_{CGL}. The resulting transfer curve at $T = 295\ K$ is shown in Fig. 4.6(a), where the load

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU WIEN Bibliothek Your knowledge hub

transistor is highlighted in the circuit inset. It is evident that lower magnitudes of the load program gate voltage lead to steeper transfer curves, whereas higher magnitudes result in a reduced slope. This trend is consistent with the observations made for the common source amplifier and demonstrates that the effective load resistance, and therefore the gain, can be adjusted through the program gate voltage of the load transistor. As in the previous measurement, a stable operating point around $V_{CGL} = -1.5\ V$ is maintained for all applied program gate voltages.

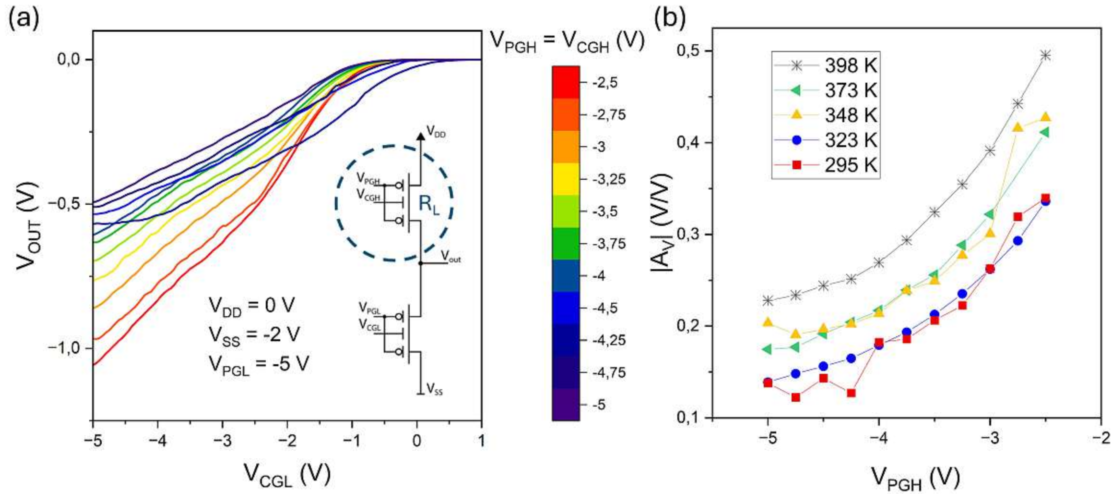


Figure 4.6: *Transfer characteristic of the GeSOI 20 p-mode common drain amplifier showing the R_L variation. The output voltage V_{OUT} is plotted as a function of the control gate voltage V_{CGL} for various program gate voltages V_{PGH} from $-5\ V$ (blue) to $-2.5\ V$ (red). The circuit was biased at $V_{DD} = 0\ V$ and $V_{SS} = -2\ V$, with the control transistor fixed at $V_{PGL} = -5\ V$. (a) Measured transfer characteristic at $T = 295\ K$ and (b) extracted voltage gain $|A_V|$ as a function of V_{PGH} for different temperatures.*

Fig. 4.6(b) presents the extracted voltage gain for different temperatures and different values of V_{PGH}. Again, the gain increases as the magnitude of the program gate voltage decreases, and this trend is consistent across all temperatures. It is also clearly visible that the gain generally increases with temperature. A plausible explanation is that the effective resistance of the load transistor decreases with increasing temperature, while the transconductance of the control transistor increases even more strongly. As a result, the ratio of transconductance to load resistance improves, leading to higher gain at elevated temperatures.

An interesting observation is the grouping of the gain curves. The data for $T = 295\ K$ and $T = 323\ K$ lie close together, as do the curves for $T = 348\ K$ and $T = 373\ K$. Distinct steps appear only between these pairs and the highest temperature of $T = 398\ K$. This suggests that there may be specific temperature ranges in which additional thermally activated processes significantly influence the balance between transconductance and load resistance, thereby affecting the overall gain.

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU Bibliothek WIEN Your knowledge hub

In this case as well, it becomes evident that a voltage controlled adjustment of the gain can compensate for temperature induced variations. A gain in the range of approximately 0.24 to 0.32 can be achieved at all measured temperatures solely by adjusting the program gate voltage V_{PGH}. Although the gain remains well below the ideal target value of unity, these measurements confirm that the circuit fundamentally exhibits the intended functionality of a voltage controllable amplifier.

In summary, the measurements of the GeSOI 20 common source and common drain amplifiers demonstrate that reconfigurable transistors enable full electrostatic control of both the transconductance and the load resistance, allowing the gain of the circuits to be adjusted through the program gate voltages of the individual devices. Both amplifier configurations exhibit stable and reproducible operation across a wide temperature range, and a consistent bias point can be maintained for different program gate settings, which illustrates the feasibility of voltage controlled and temperature compensable analog circuits based on reconfigurable device technology. At the same time, the results also reveal the current limitations of the GeSOI 20 platform. The achievable gain remains well below the theoretical ideal values due to the non ideal behavior of the load transistor, finite output conductance, and the influence of device asymmetries. Furthermore, the active load does not yet provide a perfectly resistive characteristic, leading to a gradual transition into the ohmic region and a reduced voltage swing near the supply rails. These effects highlight the need for improved device symmetry, reduced parasitic conductances, and enhanced gate control.

These findings form an important basis for the following investigation of the third generation GeSOI 21 platform. With optimized fabrication, improved electrostatic design, and reduced variability, the GeSOI 21 devices address several of the limitations identified in the GeSOI 20 amplifiers and enable more robust and higher performance reconfigurable circuits. The next section therefore focuses on the basic characterization of the GeSOI 21 technology and its impact on analog and mixed signal circuit functionalities.

4.6 GeSOI 21 Basic Characterization

The basic electrical characterization of the third generation GeSOI 21 devices was carried out to evaluate the improvements in device symmetry, temperature stability, and reconfigurable operation achieved with the updated fabrication flow. In contrast to the second generation measurements, the experiments were not performed on the PA300 prober but on the Cascade system, as described in Subsec. 3.2.2, using the implemented python framework. Besides the different measurement platform, the characterization methodology itself was refined. Before each measurement cycle, a full transfer sweep was recorded to remove residual charge from previous biasing conditions, ensuring stable device operation and significantly reducing hysteretic or history dependent effects.

As a result, the obtained data shown in Fig. 4.7 exhibit clean and continuous evolution of

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU WIEN Bibliothek Your knowledge hub

the transfer characteristics for all program gate voltages and temperatures. In contrast to the large parameter sweep of the GeSOI 20 generation, the curves show smooth transitions between the measurement ranges of the analyzer without visible steps or discontinuities. For all values of the program gate voltage, the saturated current lies between the neighboring program gate settings, and no outliers or unexpected deviations are observed.

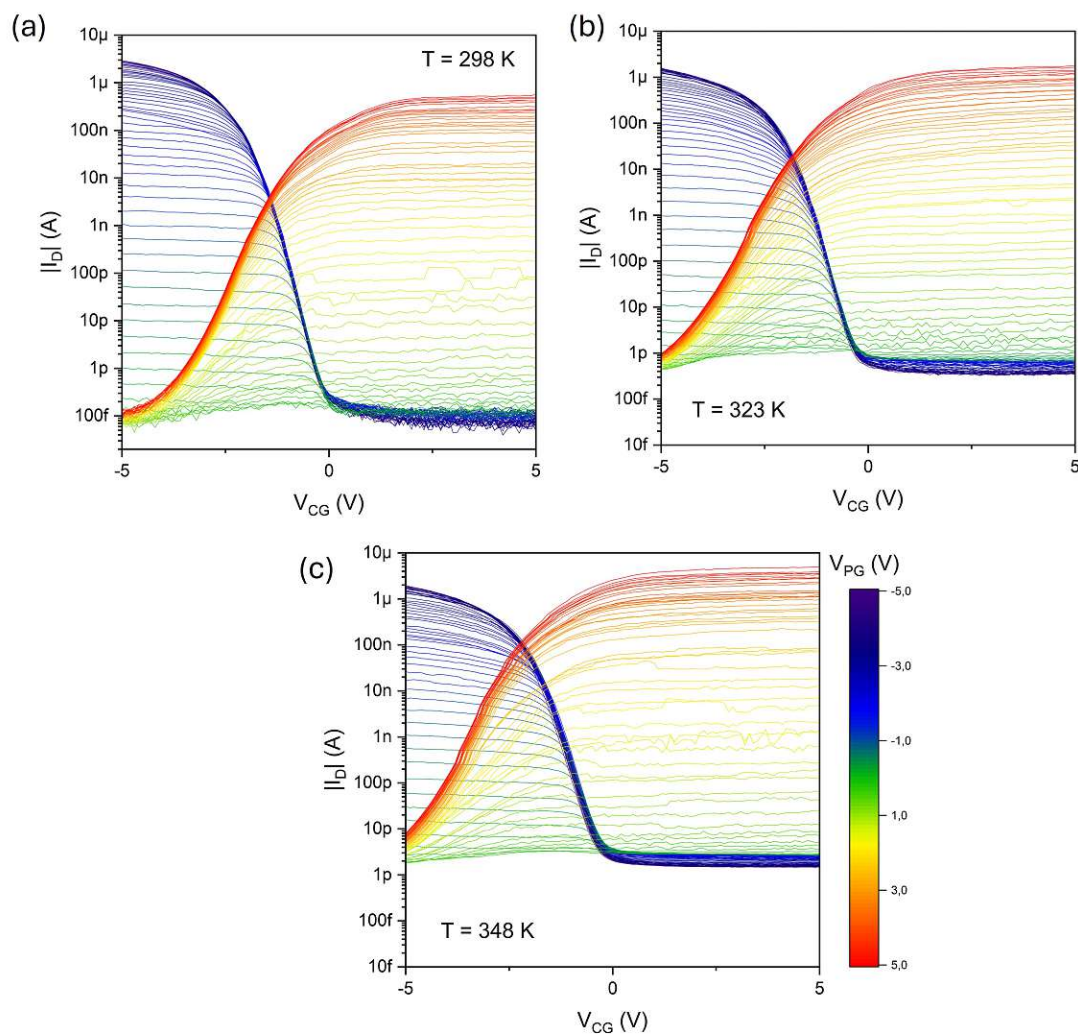


Figure 4.7: *Subset of the large parameter sweep of the third generation GeSOI 21 RFET for different program gate voltages V_{PG} at three temperatures. The drain current $|I_D|$ is plotted as a function of the control gate voltage V_{CG} for (a) $T = 298\ K$, (b) $T = 323\ K$, and (c) $T = 348\ K$. The program gate voltage V_{PG} was varied from $-5\ V$ (blue) to $5\ V$ (red), and all measurements were performed with symmetric biasing at $V_D = -V_S = 0.9\ V$.*

The transfer characteristics of the GeSOI 21 devices show a pronounced improvement in symmetry compared to the previous generation. For p-type operation, the on current I_{on}^p decreases slightly with increasing temperature, while for n-type operation, the on current

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU WIEN Bibliothek Your knowledge hub

I_{on}^n increases with temperature. The off currents I_{off}^p and I_{off}^n rise with temperature for both polarities, as expected from thermionic emission and thermionic field emission. Across the full temperature range, an on-to-off ratio of approximately six orders of magnitude is achieved for both conduction types at $T = 323\ K$, which represents a substantial improvement over the GeSOI 20 generation, where the p-type and n-type on-to-off ratios amounted to five and four orders of magnitude, respectively.

A quantitative comparison of the extracted current levels is provided in Tab. 4.2. At $T = 323\ K$, the p-type on current decreases from 2.9 μA at $T = 298\ K$ to 1.5 μA and increases again slightly at $T = 348\ K$. In contrast, the n-type on current increases continuously from 560 nA to 5 μA over the same temperature range. The off currents rise from values on the order of the 100 fA measurement resolution of the Cascade system to the low picoampere regime at $T = 348\ K$, while remaining symmetric for both polarities. Notably, the lowest currents occur at n-type off-operation, which moves out of the measured range at higher temperatures due to the temperature induced left shift of the transfer characteristic.

Table 4.2: *Extracted current levels for the GeSOI 21 RFET at different temperatures.*

	$T = 298\ K$	$T = 323\ K$	$T = 348\ K$
I_{on}^p	2.9 μA	1.5 μA	1.96 μA
I_{on}^n	560 nA	1.8 μA	5 μA
I_{off}^p	75 fA	347 fA	1.56 pA
I_{off}^n	75 fA	468 fA	1.87 pA

A direct comparison between the GeSOI 20 and GeSOI 21 devices at $T = 323\ K$ highlights the improvements achieved with the third generation. The p-type to n-type on current ratio I_{on}^p/I_{on}^n decreases from 2.25 in GeSOI 20 to 0.88 in GeSOI 21, indicating significantly improved symmetry. Likewise, the off current ratio I_{off}^p/I_{off}^n increases from approximately 0.07 to 0.74, showing a much better balance of leakage behavior. The p-type on-to-off ratio increases from 10^5 to 10^6, and the n-type on-to-off ratio increases from 10^4 to 10^6. These results demonstrate that the third generation GeSOI RFET exhibits a substantially more symmetric and thermally stable behavior than its predecessor.

Overall, the GeSOI 21 characterization confirms that the improvements in material stack, contact engineering, and device geometry result in a more balanced and more predictable reconfigurable operation. The enhanced symmetry, the extended on-to-off ratios, and the reduced trap influence establish GeSOI 21 as the most stable and best performing reconfigurable device generation presented in this work.

4.7 GeSOI 21 Common Source Amplifier

The common source amplifier of the third generation GeSOI 21 device was characterized to assess the impact of the improved device symmetry and contact engineering on the analog performance. As in the previous generation, the bias point of the amplifier was

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU WIEN Bibliothek Your knowledge hub

determined experimentally. All measurements were carried out at room temperature The amplifier was biased at $V_{DD} = 0\ V$ and $V_{SS} = -3\ V$.

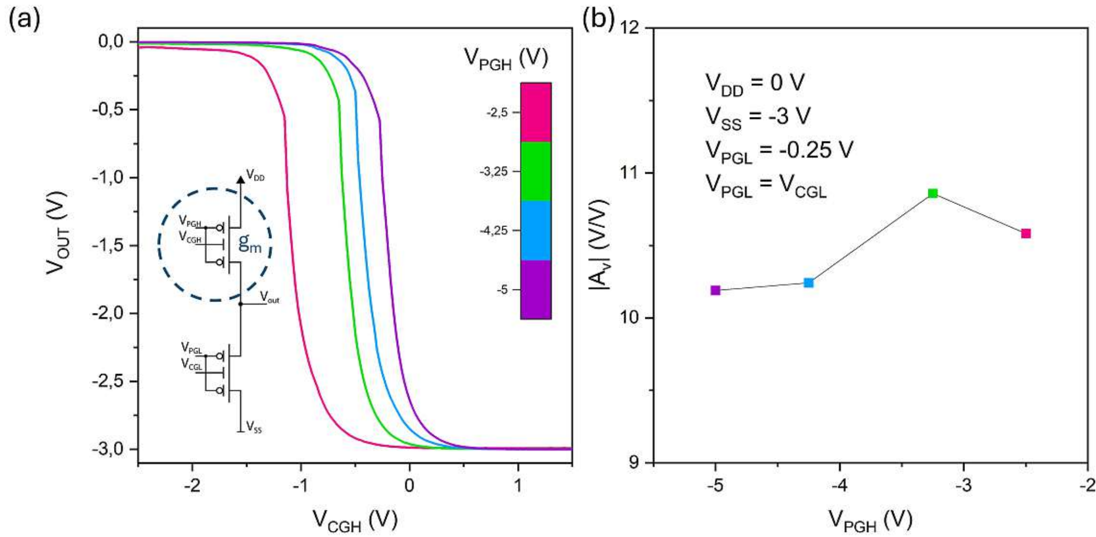


Figure 4.8: *Transfer characteristic of the GeSOI 21 p-mode common source amplifier showing the g_m variation. The output voltage V_{OUT} is plotted as a function of the control gate voltage V_{CGH} for various program gate voltages V_{PGH} from $-5\ V$ (purple) to $-2.5\ V$ (pink). The circuit was biased at $V_{DD} = 0\ V$ and $V_{SS} = -3\ V$, with the load transistor fixed at $V_{PGL} = -0.25\ V$. (a) Measured transfer characteristic at room temperature and (b) extracted voltage gain $|A_V|$ as a function of V_{PGH}.*

Fig. 4.8(a) shows the corresponding transfer characteristics for different values of V_{PGH}. In contrast to the GeSOI 20 devices, where the slopes differed visibly between the program gate biases, the GeSOI 21 characteristics are extremely steep and nearly parallel. As a result, the influence of the program gate voltage on the steepness of the curve cannot be seen directly from the transfer characteristic. Instead, the curves appear as horizontal shifts of one another, with the transition moving toward more positive values of V_{CGH} as the magnitude of V_{PGH} is increased. This behavior prevents the definition of a common operating point for all program gate voltages, since the operating point of one curve would lie close to either V_{SS} or V_{DD} for another curve.

As indicated by nearly identical slopes in the transfer characteristic, the extracted gains shown in Fig. 4.8(b) reveal no significant dependence on the program gate voltage. Apart from a indicated positive trend through the outlier at $V_{PGH} = -3.25\ V$, resulting from the small dataset of 4 points, no trend can be observed. The achievable gains of the GeSOI 21 common source amplifier lie between approximately 10.2 and 10.8. This represents a substantial improvement over the GeSOI 20 generation, where the gains ranged only from 1 to 1.13. The significantly higher gain is attributed to the improved symmetry, higher transconductance, and reduced parasitic effects of the third generation device.

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU Bibliothek WIEN Your knowledge hub

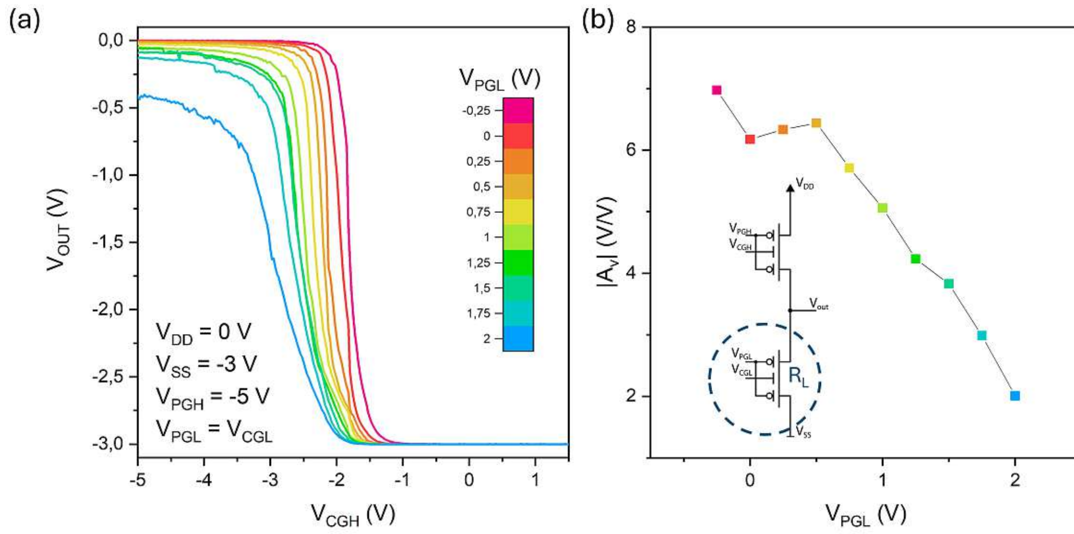


Figure 4.9: *Transfer characteristic of the GeSOI 21 p-mode common source amplifier showing the R_L variation. The output voltage V_{OUT} is plotted as a function of the control gate voltage V_{CGH} for various program gate voltages V_{PGL} from $-0.25\ V$ (pink) to $2\ V$ (blue). The circuit was biased at $V_{DD} = 0\ V$ and $V_{SS} = -3\ V$, with the control transistor fixed at $V_{PGH} = -5\ V$. (a) Measured transfer characteristic at room temperature and (b) extracted voltage gain $|A_V|$ as a function of V_{PGL}.*

The influence of the load transistor on the amplifier behavior is shown in Fig. 4.9. In analogy to the GeSOI 20 devices, lower magnitudes of V_{PGL} result in higher effective load resistance and therefore higher voltage swing, while higher magnitudes of V_{PGL} reduce the load resistance and decrease the swing. The transfer characteristics again shift horizontally with increasing V_{PGL}, and the transition occurs at progressively more negative values of V_{CGH}. Despite the steep characteristics, a consistent dependence of the extracted gains on the program gate voltage is observed, as shown in Fig. 4.9(b). Higher magnitudes of V_{PGL} lead to lower gains, and the total gain range extends from approximately 2 to 6.7, which again significantly exceeds the performance of the GeSOI 20 devices, where the gain ranged only from 0.63 to 1.

Overall, the common source amplifier characterization demonstrates that the GeSOI 21 devices provide a substantial improvement in gain, symmetry, and electrostatic control compared to the second generation. The extremely steep transfer characteristics and the large achievable gain highlight the suitability of the GeSOI 21 platform for analog signal processing, while the observed horizontal shifts of the curves indicate that fine tuning of the operating point is required for circuit integration. Nevertheless, the results clearly show that the GeSOI 21 generation offers the most robust and highest performance common source amplifier operation among the devices investigated in this work.

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU WIEN Bibliothek Your knowledge hub

4.8 GeSOI 21 Common Drain Amplifier

The common drain amplifier of the third generation GeSOI 21 devices was characterized using a bias configuration with $V_{DD} = -2\ V$ and $V_{SS} = 1\ V$. In contrast to the common source configuration of GeSOI 21, a fixed operating point could be defined for all investigated program gate voltages.

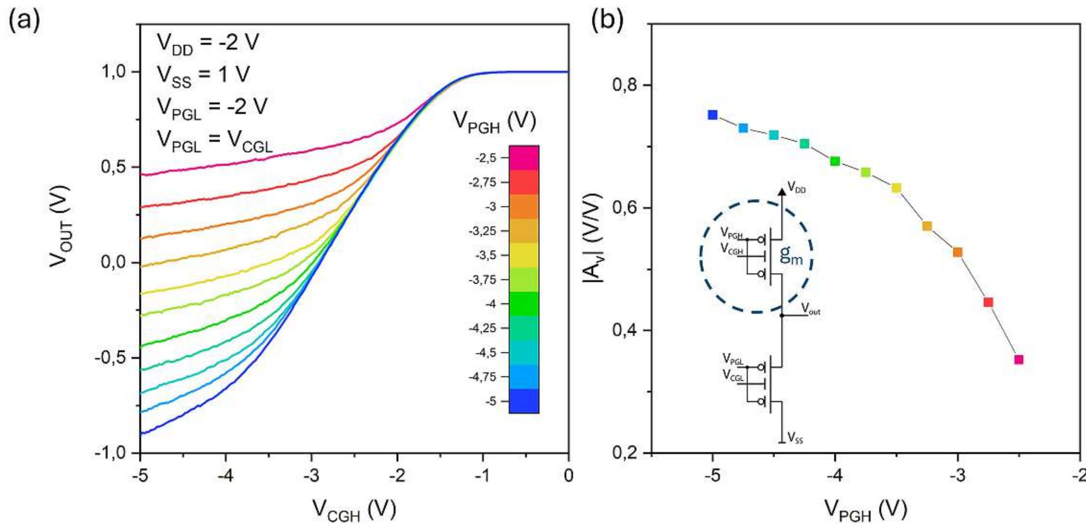


Figure 4.10: *Transfer characteristic of the GeSOI 21 p-mode common drain amplifier showing the g_m variation. The output voltage V_{OUT} is plotted as a function of the control gate voltage V_{CGH} for various program gate voltages V_{PGH} from $-5\ V$ (blue) to $-2.5\ V$ (pink). The circuit was biased at $V_{DD} = -2\ V$ and $V_{SS} = 1\ V$, with the load transistor fixed at $V_{PGL} = -2\ V$. (a) Measured transfer characteristic at room temperature and (b) extracted voltage gain $|A_V|$ as a function of V_{PGH}.*

Fig. 4.10(a) shows the measured transfer characteristics for different values of V_{PGH}. The curves fan out in a clean and well ordered manner without overlap other than the shared diagonal to the positive voltage rail. Both the transition voltage and the slope increase with the magnitude of the program gate voltage. In contrast to the GeSOI 20 generation, no discontinuities or irregularities are observed in the transfer characteristics. A common operating point around $V_{CGH} = -1.5\ V$ can be used for all values of V_{PGH}, which enables consistent and adjustment of the voltage gain without the need for a feedback network to the control gate.

The extracted gain values shown in Fig. 4.10(b) reveal a clear and monotonic trend: larger magnitudes of V_{PGH} result in higher gain. The achievable gain ranges from approximately 0.35 to 0.75, which is more than double the gain obtained with the GeSOI 20 devices, where the corresponding range was only 0.09 to 0.33. The strong and consistent dependence of the gain on the program gate voltage demonstrates that the improved device symmetry and contact engineering of the GeSOI 21 generation directly enhance analog performance

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU Bibliothek Your knowledge hub WIEN

in the common drain configuration.

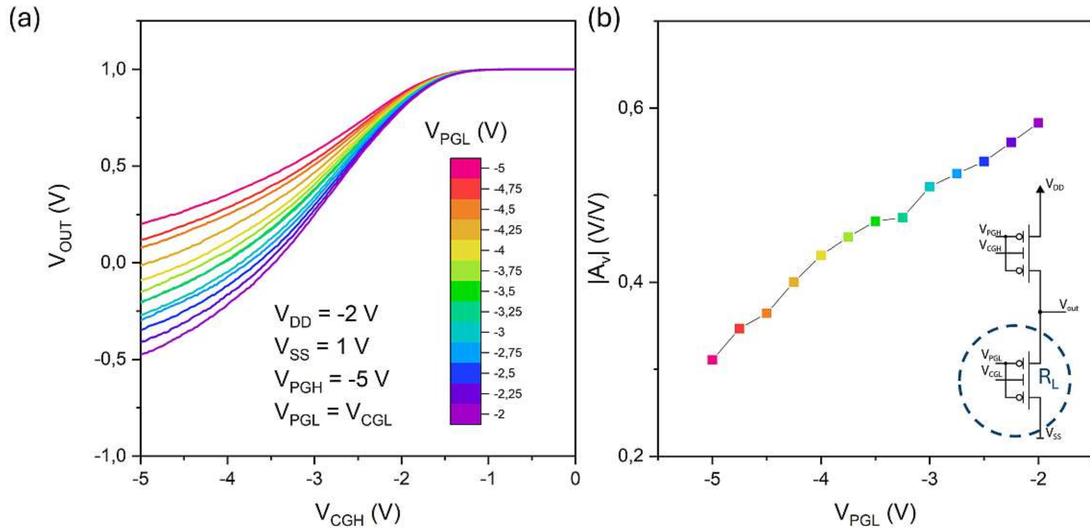


Figure 4.11: *Transfer characteristic of the GeSOI 21 p-mode common drain amplifier showing the R_L variation. The output voltage V_{OUT} is plotted as a function of the control gate voltage V_{CGH} for various program gate voltages V_{PGL} from -5 V (pink) to -2 V (purple). The circuit was biased at $V_{DD} = -2$ V and $V_{SS} = 1$ V, with the control transistor fixed at $V_{PGH} = -5$ V. (a) Measured transfer characteristic at room temperature and (b) extracted voltage gain $|A_V|$ as a function of V_{PGL}.*

The influence of the load transistor is illustrated in Fig. 4.11. In this case, the curves do not shift horizontally but differ primarily in voltage swing. Lower magnitudes of V_{PGL} lead to a larger effective load resistance and therefore a higher voltage swing, while larger magnitudes reduce the load resistance and decrease the swing. This behavior is consistent with the observations in the GeSOI 20 measurements, but the GeSOI 21 amplification performance is significantly improved. The extracted gains shown in Fig. 4.11(b) range from approximately 0.31 to 0.58, which again exceeds the GeSOI 20 values of 0.12 to 0.34. The trend is monotonic and free of outliers, representing the most stable and reproducible gain behavior observed in any common drain configuration within this work.

Overall, the GeSOI 21 common drain amplifier exhibits substantial improvements over the previous generation. The ability to define a fixed operating point for all program gate settings, the clean fanning of the transfer characteristics without discontinuities, and the significantly higher gain values demonstrate the enhanced suitability of the GeSOI 21 platform for analog follower and buffer applications. Combined with the high device symmetry and stable reconfigurable operation observed in the large parameter sweep, these results establish the GeSOI 21 generation as a robust and high performance candidate for complementary and reconfigurable analog circuit design.

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU Bibliothek WIEN Your knowledge hub

4.9 GeSOI 21 Transmission Gate

The reconfigurable transmission gate represents one of the most complex circuit implementations investigated in this work. It combines the bidirectional conduction of complementary RFETs with the independent control of multiple gate electrodes. The fundamental concept and circuit configuration were discussed in Sec. 2.5.4, while the applied measurement procedures are described in Subsec. 3.3.1 and 3.3.6. The setups used were the Karl Suss Needle Prober (Subsec. 3.2.1) and Transient Measurement Setup (3.3.6).The following sections present the experimental results, emphasizing the electrical characteristics, the functional demonstration of reconfigurability, and the tunability achieved through the program and control gates.

4.9.1 Control Gate Dependent Transfer Behavior

The initial characterization of the proposed transmission gate focuses on the dependence of the transfer characteristic on the control gate voltage. The upper transistor RFET1 was operated in n-type mode with $V_{PG1} = 5\ V$, while the lower transistor RFET2 was configured as p-type with $V_{PG2} = -5\ V$. The circuit schematic and measurement configuration are shown in Fig. 4.12(a). Both control gate voltages were varied in an anti-symmetric configuration, such that $V_{CG1} = -V_{CG2}$. This configuration ensures symmetrical switching of both devices. An external load resistance of $R_L = 100\ M\Omega$ was connected to the output node and the input voltage V_{IN} was swept from $-1\ V$ to $1\ V$.

The measured transfer characteristic in Fig. 4.12(b) shows the expected transition between the high-impedance and the transparent state of the transmission gate. For control gate voltages below approximately $V_{CG} = -1.5\ V$, both transistors are non-conductive and the circuit remains in the high-impedance state. With increasing magnitude of V_{CG}, the output signal gradually approaches the input level, indicating a progressive contribution of both transistors to the conduction path. Complete transparency, corresponding to $V_{OUT} \approx V_{IN}$, is achieved for $|V_{CG}| \geq 2\ V$, where both devices are strongly conductive.

Between the blocking and the fully transparent state, an intermediate region exists in which the transmission ratio V_{OUT}/V_{IN} continuously increases with V_{CG}. The slight asymmetry between positive and negative bias directions can be attributed to small variations in the characteristics of the individual transistors, such as threshold voltage and transconductance, as well as to minor bias-dependent effects. The transition region was measured with steps of $0.25\ V$ in V_{CG}, while the outer regions were recorded with steps of $1\ V$. These results confirm the proper operation of the proposed transmission gate and form the basis for the subsequent analysis of input-voltage and program-gate dependence.

4.9.2 Input Voltage Dependent Switching

After establishing the control gate dependence, the next step was to analyze the switching behavior of the transmission gate as a function of the applied input voltage. The circuit

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU WIEN Bibliothek Your knowledge hub

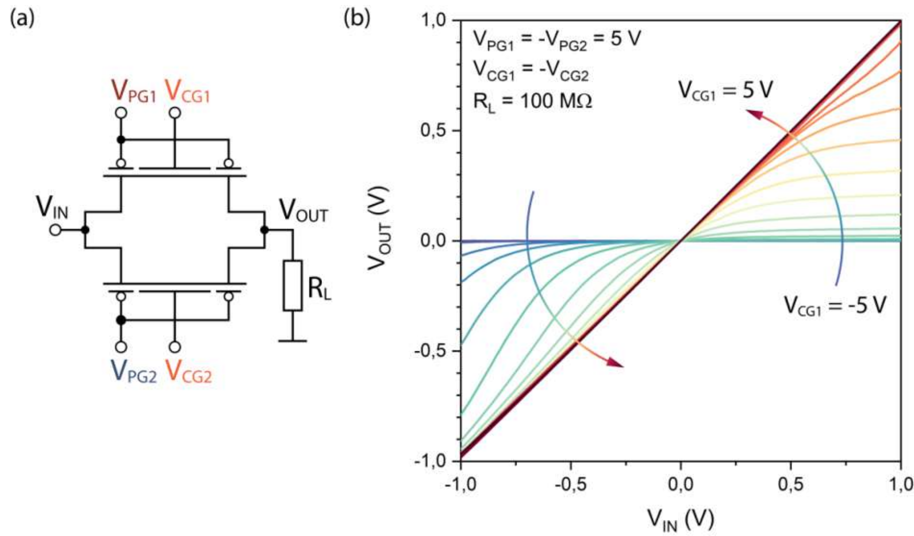


Figure 4.12: *Control gate dependent transmission gate transfer characteristic. (a) Circuit schematic with highlighted parameters V_{CG1} and V_{CG2}, (b) measured transfer characteristic with V_{CG1} varied from $-5\ V$ (blue) to $5\ V$ (red) and $V_{CG2} = -V_{CG1}$, V_{IN} varied from $-1\ V$ to $1\ V$, and $R_L = 100\ M\Omega$.*

schematic and measurement configuration are shown in the schematic inset of Fig. 4.13(a) and Fig. 4.13(b). The measurements were performed by varying the input voltage V_{IN} from $-1\ V$ to $1\ V$ in steps of $0.1\ V$, thus covering both bias directions.

In the configuration shown in Fig. 4.13(a), RFET1 was operated in p-type mode with $V_{PG1} = -5\ V$ and RFET2 in n-type mode with $V_{PG2} = 5\ V$. The measured transfer characteristics reveal that, depending on the input voltage, the control gate voltage V_{CG} has to reach a certain threshold to switch the transmission gate from the high-impedance to the transparent state, in which the output follows the input. This behavior is consistent with the control gate voltage range identified in the previous measurements, confirming that both transistors must be sufficiently biased to enable bidirectional conduction.

When the operation modes of both transistors are inverted, as shown in Fig. 4.13(b), with RFET1 configured as n-type ($V_{PG1} = 5\ V$) and RFET2 as p-type ($V_{PG2} = -5\ V$), the switching behavior remains nearly identical. This indicates that the electrical characteristics of the individual transistors are well balanced in both operation modes. The inversion of the control gate polarity is required to maintain equivalent switching functionality, meaning that V_{CG1} and V_{CG2} must be interchanged in sign. If the same control gate polarity were used for the inverted configuration, the resulting transfer curve would appear mirrored with respect to the control gate axis. This polarity inversion can therefore be exploited as an additional degree of freedom for signal inversion or logic-level functionality within the proposed circuit architecture.

The observed symmetry between both bias directions demonstrates the correct bidirec-

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU WIEN Bibliothek Your knowledge hub

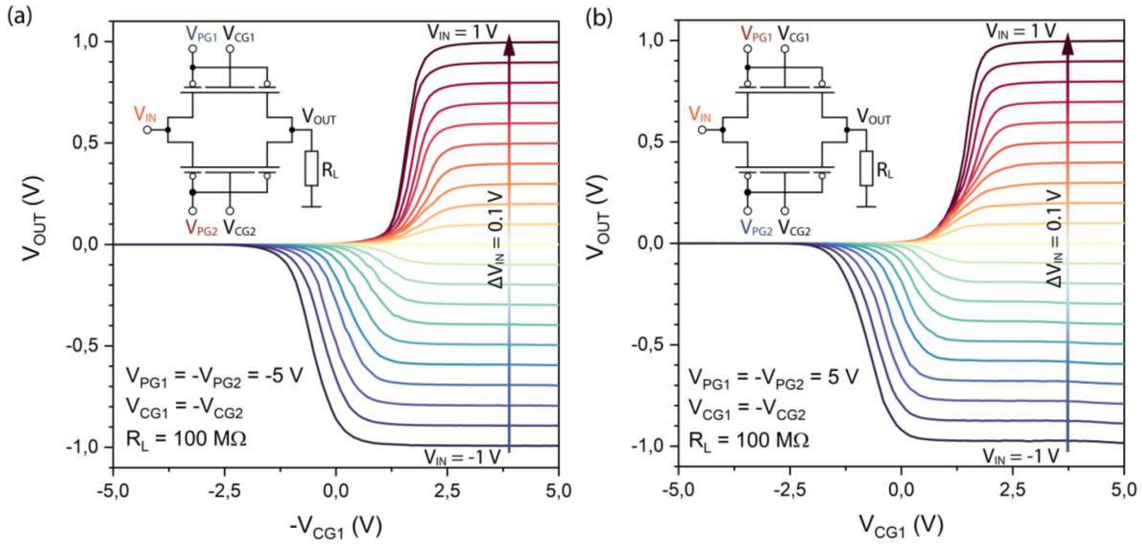


Figure 4.13: *Input voltage dependent transmission gate switching behavior with $R_L = 100\ M\Omega$. (a) RFET1 in p-type mode ($V_{PG1} = -5\ V$) and RFET2 in n-type mode ($V_{PG2} = 5\ V$), (b) inverted configuration with RFET1 in n-type mode ($V_{PG1} = 5\ V$) and RFET2 in p-type mode ($V_{PG2} = -5\ V$). The input voltage V_{IN} was varied from $-1\ V$ (blue) to $1\ V$ (red) in steps of $0.1\ V$ and the corresponding control gate voltages were adjusted anti-symmetrically ($V_{CG1} = -V_{CG2}$).*

tional operation of the transmission gate. The consistent switching characteristics for both transistor configurations confirm the uniformity of the underlying RFET technology and the suitability of the device pair for complementary and reconfigurable circuit applications.

4.9.3 Program Gate Influence

After verifying the control gate related functionality and the input-voltage dependent switching, the next step was to investigate the influence of the program gate voltages on the transmission characteristics. In the following, both asymmetric and symmetric configurations of the program gate voltages are analyzed to assess their impact on the overall circuit performance.

Unequal Program Gate Configuration

To analyze the individual contribution of each transistor, one program gate was kept constant while the other was varied. The corresponding circuit schematic and measurement configuration are shown in Fig. 4.14(a) and Fig. 4.14(b). The control gates were biased anti-symmetrically with $V_{CG1} = 5\ V$ and $V_{CG2} = -5\ V$, ensuring identical switching conditions for both devices.

In the configuration shown in Fig. 4.14(a), RFET1 was operated in n-type mode with $V_{PG1} = 5\ V$, while V_{PG2} of the lower transistor was varied from $5\ V$ to $-5\ V$ in steps of $0.5\ V$. As observed in the measured transfer characteristics, changes in V_{PG2} have only a minor effect on the overall behavior, since RFET1 already provides a low-resistance

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU Bibliothek Your knowledge hub WIEN

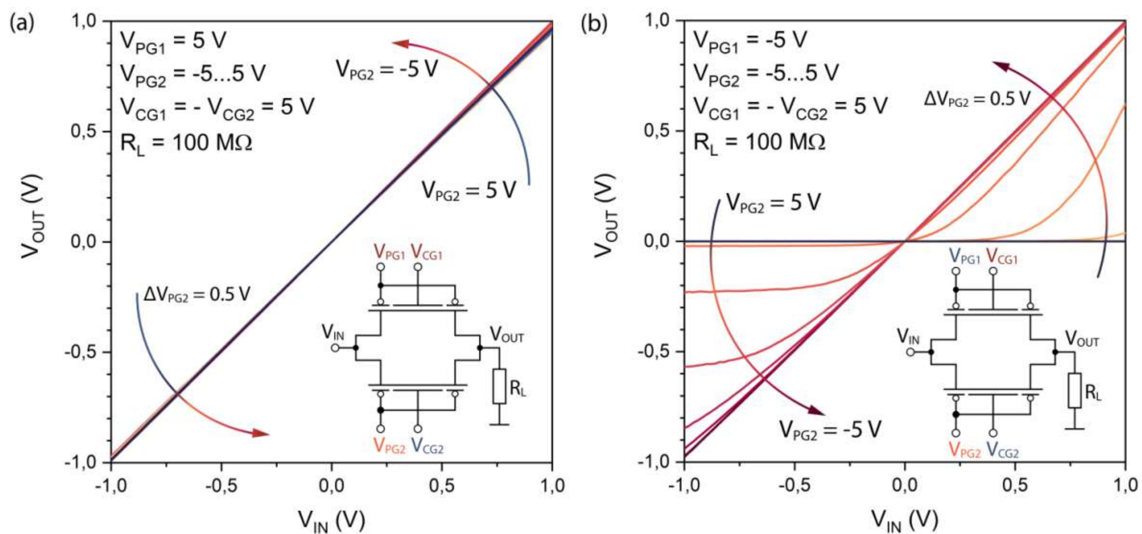


Figure 4.14: *Asymmetric program gate dependent transmission gate transfer characteristics with anti-symmetric control gate bias ($V_{CG1} = 5\ V$, $V_{CG2} = -5\ V$). (a) RFET1 in n-type mode ($V_{PG1} = 5\ V$) and V_{PG2} varied from $5\ V$ (blue) to $-5\ V$ (red) in steps of $0.5\ V$, (b) RFET1 in p-type mode ($V_{PG1} = -5\ V$) and V_{PG2} varied from $5\ V$ (blue) to $-5\ V$ (red) in steps of $0.5\ V$.*

conduction path in its on-state. The circuit remains in the transparent state over the entire sweep range, confirming that the upper transistor dominates the conduction in this configuration.

In contrast, the complementary case shown in Fig. 4.14(b) was measured with RFET1 operated in p-type mode ($V_{PG1} = -5\ V$), which corresponds to the off-state, and RFET2 with a variable V_{PG2} from $5\ V$ to $-5\ V$. In this configuration, the conduction of the transmission gate strongly depends on the state of RFET2. At high positive V_{PG2} values, the transmission gate remains in the high-impedance state, while with decreasing V_{PG2} the conduction gradually increases until full transparency is reached for $V_{PG2} \leq -2\ V$. These measurements clearly demonstrate that the transparency of the circuit can be tuned by the program gate of the individual transistor and that the switching behavior is dominated by the device currently configured for conduction.

Equal Program Gate Configuration and Attenuation

In addition to the independent control of each transistor, both program gates can be varied simultaneously in an anti-symmetric configuration, that is $V_{PG1} = -V_{PG2}$. This configuration allows a balanced adaptation of both transistors and enables control over the overall transmission ratio between input and output. The circuit schematic and measured results are shown in Fig. 4.15(a) and Fig. 4.15(b).

Fig. 4.15(a) shows the transfer characteristic for equally varied program gate voltages from $V_{PG1} = 0.5\ V$ to $5\ V$ in steps of $0.5\ V$. The transparency of the transmission gate increases

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU Bibliothek Your knowledge hub WIEN

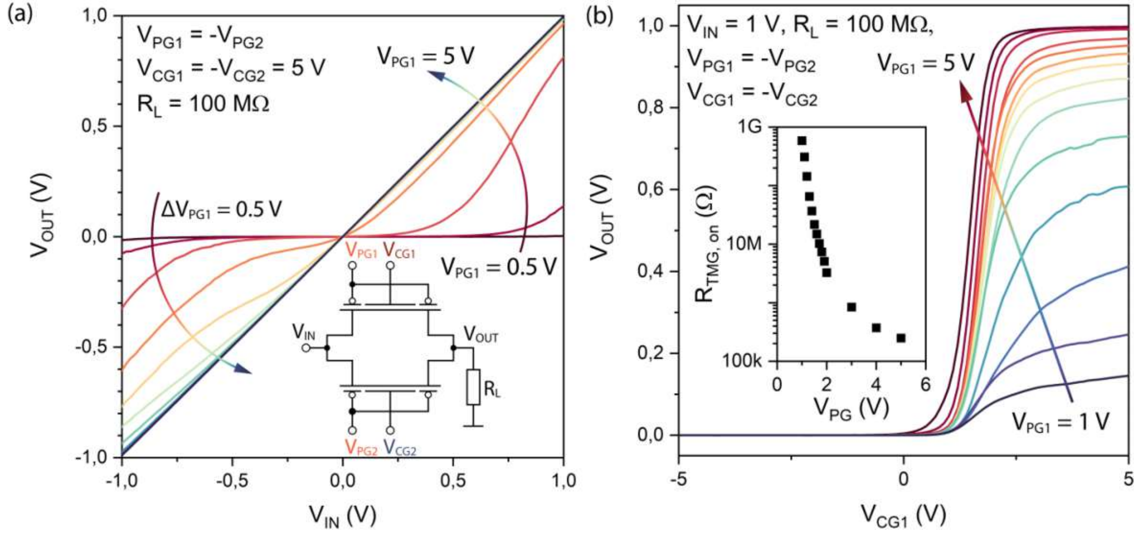


Figure 4.15: *Symmetric program gate dependent transmission gate behavior with anti-symmetric program and control gate bias ($V_{PG1} = -V_{PG2}$ and $V_{CG1} = -V_{CG2}$). (a) Transfer characteristics for V_{PG1} varied from 0.5 V (red) to 5 V (blue) in steps of 0.5 V, (b) attenuation behavior for constant V_{IN} = 1 V and varied program gate voltages from ±1 V (blue) to ±5 V (red), with extracted $R_{TMG,on}$ shown in the inset.*

with higher program gate voltage magnitude until complete transmission ($V_{OUT} \approx V_{IN}$) is reached. Unlike the previous asymmetric configuration, the symmetric sweep results in an almost bias-direction independent behavior.

To further analyze the attenuation behavior, the output-to-input ratio V_{OUT}/V_{IN} was recorded for a constant $V_{IN} = 1\ V$ while varying the program gate voltages equally from $\pm 1\ V$ to $\pm 5\ V$, as shown in Fig. 4.15(b). The output voltage decreases continuously with smaller $|V_{PG}|$, corresponding to an increase in the effective on-state resistance $R_{TMG,on}$. The inset of Fig. 4.15(b) illustrates this relationship, where $R_{TMG,on}$ decreases non-linearly from the $G\Omega$ range down to approximately 100 $k\Omega$. This voltage-dependent attenuation property enables the proposed transmission gate to function as a tunable resistive element, which can be advantageous for analog front-end or feedback networks that require adjustable signal weighting.

4.9.4 Transient Characteristics

In addition to the static transfer measurements, the transient response of the transmission gate was analyzed to evaluate its dynamic behavior and verify the reproducibility of the attenuation property under time-dependent conditions. The schematic measurement configuration is shown in Fig. 4.16(a). During the experiment, RFET1 was configured in p-type mode and RFET2 in n-type mode with $V_{PG1} = -V_{PG2}$, while both control gates were biased anti-symmetrically. A rectangular control input signal with a direct-current level of $V_{DC} = \pm 2.5\ V$ and a peak-to-peak amplitude of $V_{pp} = 5\ V$ at 10 Hz was applied to

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU Bibliothek Your knowledge hub WIEN

the control gates to switch the transmission gate periodically between the high-impedance and the transparent state. The input voltage was kept constant at $V_{IN} = 1\ V$.

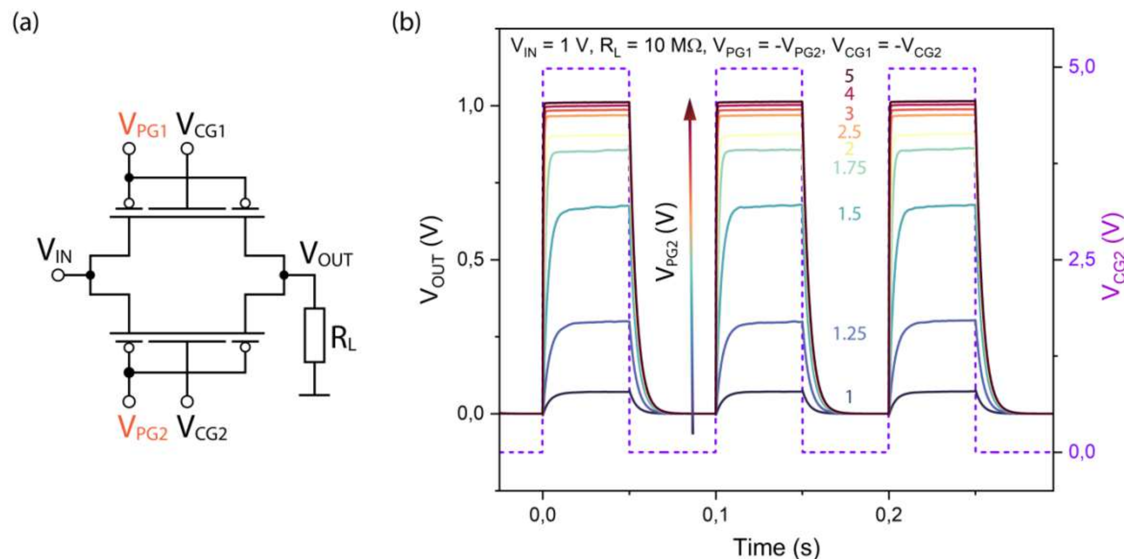


Figure 4.16: *Transient behavior of the transmission gate. (a) Circuit schematic with highlighted constant and varied parameters, (b) measured transient output for anti-symmetric program gate voltages from* $\pm 1\ V$ *(blue) to* $\pm 5\ V$ *(red) with a rectangular control input of* $V_{DC} = \pm 2.5\ V$, $V_{pp} = 5\ V$, *and frequency of* $10\ Hz$. *The load resistance was* $R_L = 10\ M\Omega$ *and the input voltage* $V_{IN} = 1\ V$.

For measurement-related reasons, the external load resistance was reduced from $R_L = 100\ M\Omega$ to $R_L = 10\ M\Omega$, resulting in slightly altered output voltage levels compared to the static characterization. The measured transient response is depicted in Fig. 4.16(b). As can be seen, the transmission gate switches reproducibly between the high-impedance and the transparent state. Within the transparent phase, the output voltage level depends on the applied program gate voltage magnitude. With increasing $|V_{PG}|$, the attenuation decreases, corresponding to a lower on-state resistance $R_{TMG,on}$. This observation confirms the tunable resistive behavior that was already identified in the static measurements.

A closer inspection of the rising and falling signal edges reveals a change in the time constant for different program gate settings. The variation in the transient response can be attributed to the dependence of both channel resistance and junction capacitance on the applied program gate bias. Increasing $|V_{PG}|$ not only enhances the transmission level but also reduces the effective time constant, resulting in faster signal transitions. This property allows the proposed transmission gate to operate as a bidirectional, voltage-controlled delay element. Consequently, such devices can be utilized in applications requiring adjustable signal timing or phase alignment, such as in adaptive sensor front-ends or reconfigurable feedback paths.

The presented measurements confirm the correct operation of the reconfigurable transmis-

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU WIEN Bibliothek Your knowledge hub

sion gate based on complementary RFETs. The circuit demonstrates reliable bidirectional conduction and symmetric switching behavior controlled by the anti-symmetric control gate configuration. The program gate voltages enable fine adjustment of the individual transistor characteristics and allow for precise control of the transmission ratio and the on-state resistance. Furthermore, the transient investigations verify the stability and reproducibility of the attenuation property and reveal a clear correlation between the program gate voltage and the dynamic time constant. Overall, the results validate the functionality and versatility of the proposed transmission gate concept and underline its potential for implementation in adaptive and reconfigurable circuit architectures.

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU WIEN Bibliothek Your knowledge hub

Chapter 5

Summary and Outlook

The presented work demonstrates the evolution of Al-Si-Ge multi-heterojunction reconfigurable field effect transistors from the first generation devices reported by Dobler [10] toward the GeSOI 20 and GeSOI 21 platforms. While the first generation showed strong polarity asymmetry and limited circuit performance, the GeSOI 20 devices achieved improved electrostatic balance due to the Al-Si-Ge multi-heterojunction contact scheme and the SiO2/ZrO2 gate stack. The GeSOI 21 devices further enhanced this behavior. At $T = 323\ K$, the ratio I_{on}^{p}/I_{on}^{n} improved from 4.1 in the first generation and 2.25 in GeSOI 20 to 0.88 in GeSOI 21. The on-to-off ratios increased to approximately six decades for both polarities. Comparable off currents confirm that the Si interlayer effectively centers the Fermi level, resulting in symmetric Schottky barrier modulation for electrons and holes.

Common source and common drain configurations were analyzed across all generations. The first generation achieved maximum gains near unity in n-type common source and below unity in p-type common drain mode. GeSOI 20 introduced fully integrated RFET loads, enabling electrostatic gain control via the program gate. Gains reached approximately 1.1 in common source and 0.5 in common drain configuration, with a stable operating point in the common drain case. The GeSOI 21 devices provided further improvements. The common source amplifier reached gains of approximately 10, while the common drain amplifier achieved gains between about 0.35 and 0.75. In both cases, gain tuning via the program gate was possible, and the common drain configuration maintained a fixed operating point for all program gate settings. These results show the technological progression from early circuits toward high gain and tunable amplifiers.

The reconfigurable transmission gate represents the most complex circuit investigated. Static measurements demonstrated correct bidirectional switching with full transparency for $|V_{CG}| \geq 2\ V$ and tunable attenuation in the intermediate region. Program gate vari-

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU Bibliothek WIEN Your knowledge hub

ations enabled control of the effective on-resistance from the GOhm to the 100 $kOhm$ range, allowing the circuit to operate as a tunable resistive element. Transient measurements confirmed reproducible switching at 10 Hz and showed that the output time constant decreases with increasing $|V_{PG}|$. These results verify that RFET-based circuits support reconfigurable, bidirectional, and continuously tunable signal transmission.

The improvements demonstrated in this work establish the GeSOI 21 RFET as a promising platform for reconfigurable analog and mixed-signal circuits. The symmetric on and off currents, large on-to-off ratios, and high common source gain show that polarity control can be realized without degrading analog performance. Tunable gain and stable operating points in common drain configuration enable reliable biasing strategies. The transmission gate extends these capabilities toward bidirectional routing, programmable attenuation, and adjustable delay.

Limitations arise from charge trapping in the gate stack, which introduces hysteresis and affects reproducibility. The steep transfer characteristic of the GeSOI 21 common source amplifier complicates operating point selection and requires careful bias control. This could be overcome by additional biasing of the device back gate to shift the transfer curve onto the operating point. Dynamic measurements were limited to 10 Hz in this work, although the instrumentation supports substantially higher speeds. In addition, the effective maximum switching frequency was also constrained by the measurement environment: long probe cables and the comparatively large contact pads introduce significant parasitic capacitance, which slows down edge transitions and limit the usable bandwidth at the device terminals. Nonetheless, further improvements in device passivation and dielectric engineering are necessary to fully exploit the device capabilities.

Building on the improved symmetry and tunability demonstrated in this thesis, several advanced circuit concepts become feasible. RFET complementary logic circuits and transmission gates can form the basis of reconfigurable logic cells capable of switching between Boolean functions at runtime. For example, a single RFET-based gate could be configured as NAND, NOR, XOR, or buffer by adjusting the program gate voltages, enabling polymorphic logic blocks with drastically reduced transistor count. Adaptive multiplexers and crossbar networks can benefit from the bidirectional, symmetric behavior of the transmission gate, providing dynamically selectable routing paths in signal-processing chains. Furthermore, adaptive gain amplifier stages could be used in RFET based operational amplifiers to ensure stability over a wide range of temperatures.

In the analog domain, RFET-controlled variable gain amplifiers can be realized by exploiting the continuous gain tuning of the common source configuration. Cascoded RFET stages may achieve enhanced output resistance and higher gain, enabling reconfigurable multi-stage amplifier architectures. Differential pairs using polarity-switchable RFETs could operate in n-n, p-p, or mixed-polarity modes, offering adaptive common-mode ranges and flexible biasing schemes. The tunable on-resistance of the transmission gate allows the

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU WIEN Bibliothek Your knowledge hub

implementation of voltage-controlled resistors suitable for programmable RC filters, variable attenuators, and tunable delay elements. These functionalities point toward adaptive mixed-signal front ends, sensor interfaces, and autonomous analog subsystems.

Measurement-wise, integrating the Zurich Instruments MFLI directly into the Python-based measurement framework via Ethernet would allow synchronized DC, pulsed, and transient characterization, enabling automated transient sweeps at higher frequencies and providing deeper insight into the dynamic RFET behavior.

From a technology perspective, improved passivation targeting reduced charge trapping is expected to enhance stability and reproducibility. Optimized interface treatments and dielectric stacks could suppress slow charge dynamics, decrease hysteresis, and provide more robust operation in extended circuit environments. Together, these developments would further strengthen the potential of RFET technology for reconfigurable electronic systems.

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU Bibliothek WIEN Your knowledge hub

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.

List of Figures

2.1 Lattice structure and band diagram of related materials . . . 6
2.2 Fermi-level pinning for various metals in Si and Ge . . . 9
2.3 Metal-semiconductor transition for n-type and p-type semiconductors . . . 10
2.4 Transport mechanisms in metal-semiconductor transitions . . . 11
2.5 Schematic structure and operation principle of an SBFET . . . 13
2.6 Schematic structure and operation principle of an RFET . . . 15
2.7 Common source amplifier schematic and transfer characteristic . . . 16
2.8 Common drain amplifier schematic and transfer characteristic . . . 18
2.9 Complementary Inverter schematic and transfer characteristic . . . 20
2.10 Transmission gate schematic and truth table . . . 21

3.1 GeSOI wafer and device stack . . . 24
3.2 GeSOI 20 circuit sample . . . 27
3.3 Layout of the Karl Suss Needle Prober setup . . . 28
3.4 Layout of the Cascade setup . . . 31
3.5 Layout of the Semi-Automatic Needle Prober setup . . . 33
3.6 Layout of the Transient Measurement setup . . . 36

4.1 GeSOI 20 reference structure large parameter sweep . . . 46
4.2 GeSOI 20 complementary inverter transfer characteristic . . . 48
4.3 GeSOI 20 p-mode common source gm variation over temperature . . . 50
4.4 GeSOI 20 p-mode common source RL variation over temperature . . . 51
4.5 GeSOI 20 p-mode common drain gm variation over temperature . . . 53
4.6 GeSOI 20 p-mode common drain RL variation over temperature . . . 54
4.7 GeSOI 21 large parameter sweep . . . 56
4.8 GeSOI 21 p-mode common source gm variation . . . 58
4.9 GeSOI 21 p-mode common source RL variation . . . 59
4.10 GeSOI 21 p-mode common drain gm variation . . . 60
4.11 GeSOI 21 p-mode common drain RL variation . . . 61
4.12 Control gate dependent transmission gate transfer characteristic . . . 63
4.13 Input voltage dependent transmission gate switching behavior . . . 64
4.14 Asymmetric program gate dependent transmission gate behavior . . . 65

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU WIEN Bibliothek Your knowledge hub

4.15 Symmetric program gate dependent transmission gate behavior 66
4.16 Transient behavior of the transmission gate 67

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU WIEN Bibliothek Your knowledge hub

Bibliography

[1] J. Bardeen and W. H. Brattain. The Transistor, A Semiconductor Triode. *Phys. Rev.*, 74:230–231, Jul 1948.

[2] Gordon E. Moore. Cramming more components onto integrated circuits, Reprinted from Electronics, volume 38, number 8, april 19, 1965, pp.114 ff. *IEEE Solid-State Circuits Society Newsletter*, 11(5):33–35, Sept 2006. ISSN 1098-4232.

[3] S.M. Sze and K.K. Ng. *Physics of Semiconductor Devices*. Wiley, 2006. ISBN 9780470068304.

[4] E. E. Haller. Germanium: From its discovery to SiGe devices. *Materials Science in Semiconductor Processing*, 9:408–422, Aug 2006. ISSN 13698001.

[5] Sayeef Salahuddin, Kai Ni, and Suman Datta. The era of hyper-scaling in electronics. *Nature Electronics*, 1:442–450, 2018. ISSN 2520-1131.

[6] André Heinzig. *Entwicklung und Herstellung rekonfigurierbarer Nanodraht-Transistoren und Schaltungen*. Dissertation. Technische Universität Dresden, 2014. ISBN 978-3-86247-540-7.

[7] International Roadmap for Devices and Systems (IRDS™) 2021 Edition, Oct 2022. https://irds.ieee.org/editions/2021.

[8] W.M. Weber and T. Mikolajick. Silicon and germanium nanowire electronics: physics of conventional and unconventional transistors. *Reports on Progress in Physics*, 80 (6):066502, Apr 2017.

[9] T. Mikolajick, G. Galderisi, S. Rai, M. Simon, R. Böckle, M. Sistani, C. Cakirlar, N. Bhattacharjee, T. Mauersberger, A. Heinzig, A. Kumar, W.M. Weber, and J. Trommer. Reconfigurable field effect transistors: A technology enablers perspective. *Solid-State Electronics*, 194:108381, 2022. ISSN 0038-1101.

[10] Alexandra Dobler. Al-si-ge multi-heterojunction reconfigurable field-effect transistors for circuit applications. Diploma thesis, Technische Universität Wien, 2024.

[11] W. Martienssen and H. Warlimont. *Springer Handbook of Condensed Matter and Ma-*

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU WIEN Bibliothek Your knowledge hub

terials Data. Springer Handbook of Condensed Matter and Materials Data. Springer Berlin Heidelberg, 2006. ISBN 9783540304371.

[12] W M Haynes, David R Lide, and Thomas J Bruno. *CRC Handbook of Chemistry and Physics 97 th Edition*. CRC Press, Jun 2016. ISBN 9781315380476.

[13] Thomas Prohaska, Johanna Irrgeher, Jacqueline Benefield, John K. Böhlke, Lesley A. Chesson, Tyler B. Coplen, Tiping Ding, Philip J.H. Dunn, Manfred Gröning, Norman E. Holden, Harro A.J. Meijer, Heiko Moossen, Antonio Possolo, Yoshio Takahashi, Jochen Vogl, Thomas Walczyk, Jun Wang, Michael E. Wieser, Shigekazu Yoneda, Xiang Kun Zhu, and Juris Meija. Standard atomic weights of the elements 2021 (IUPAC Technical Report). *Pure and Applied Chemistry*, 94:573–600, May 2022. ISSN 13653075.

[14] G. Fasching. *Werkstoffe für die Elektrotechnik*. Springer Wien New York, 2005. ISBN 9783211221334.

[15] E. Kasper and H.-J. Herzog. 1 - Structural properties of silicon-germanium (SiGe) nanostructures. In Yasuhiro Shiraki and Noritaka Usami, editors, *Silicon-Germanium (SiGe) Nanostructures*, Woodhead Publishing Series in Electronic and Optical Materials, pages 3–25. Woodhead Publishing, 2011. ISBN 978-1-84569-689-4.

[16] N. Mori. 2 - Electronic band structures of silicon-germanium (SiGe) alloys. In Yasuhiro Shiraki and Noritaka Usami, editors, *Silicon-Germanium (SiGe) Nanostructures*, Woodhead Publishing Series in Electronic and Optical Materials, pages 26–42. Woodhead Publishing, 2011. ISBN 978-1-84569-689-4.

[17] NSM Archive - Physical Properties of Semiconductors, Oct 2022. http://www.ioffe.ru/SVA/NSM/Semicond/.

[18] A. Fuchsberger. *Reconfigurable Field-Effect Transistors Based on Aluminium-Silicon-Germanium Heterostructures*. Master's thesis. TU Wien, 2022.

[19] Clemens Winkler. Mittheilungen über das Germanium. *Journal für Praktische Chemie*, 34:177–229, Aug 1886. ISSN 00218383.

[20] Erwin Rosenberg. Germanium: Environmental occurrence, importance and speciation. *Reviews in Environmental Science and Biotechnology*, 8:29–57, Mar 2009. ISSN 15691705.

[21] R. W. Olesinski and G. J. Abbaschian. The Ge-Si (Germanium-Silicon) system. *Bulletin of Alloy Phase Diagrams*, 5(2):180–183, Apr 1984. ISSN 0197-0216.

[22] H W King. Crystal structures of the elements at 25°C. *Bulletin of Alloy Phase Diagrams*, 2:401–402, 1981. ISSN 0197-0216.

[23] Mikhail R Baklanov, Christoph Adelmann, Larry Zhao, and Stefan De Gendt. Advanced Interconnects: Materials, Processing, and Reliability. *ECS Journal of Solid State Science and Technology*, 4:Y1–Y4, Dec 2014.

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU WIEN Bibliothek Your knowledge hub

[24] Baozhen Li, Timothy D Sullivan, Tom C Lee, and Dinesh Badami. Reliability challenges for copper interconnects. *Microelectronics Reliability*, 44:365–380, 2004. ISSN 0026-2714.

[25] Chunlong Fei, Xiangli Liu, Benpeng Zhu, Di Li, Xiaofei Yang, Yintang Yang, and Qifa Zhou. AlN piezoelectric thin films for energy harvesting and acoustic devices. *Nano Energy*, 51:146–161, 2018. ISSN 2211-2855.

[26] Raphael Böckle, Masiar Sistani, Kilian Eysin, Maximilian G. Bartmann, Minh Anh Luong, Martien I. den Hertog, Alois Lugstein, and Walter M. Weber. Gate-Tunable Negative Differential Resistance in Next-Generation Ge Nanodevices and their Performance Metrics. *Advanced Electronic Materials*, 7(3):2001178, 2021.

[27] Raphael Böckle, Masiar Sistani, Boris Lipovec, Darius Pohl, Bernd Rellinghaus, Alois Lugstein, and Walter M. Weber. A Top-Down Platform Enabling Ge Based Reconfigurable Transistors. *Advanced Materials Technologies*, 7(1):2100647, 2022.

[28] Lukas Wind, Masiar Sistani, Raphael Böckle, Jürgen Smoliner, Lada Vukušić, Johannes Aberl, Moritz Brehm, Peter Schweizer, Xavier Maeder, Johann Michler, Frank Fournel, Jean-Michel Hartmann, and Walter M Weber. Composition Dependent Electrical Transport in $Si_{1-x}Ge_x$ Nanosheets with Monolithic Single-Elementary Al Contacts. *Small*, 18:2204178, Sep 2022. ISSN 1613-6810.

[29] Lukas Wind, Raphael Böckle, Masiar Sistani, Peter Schweizer, Xavier Maeder, Johann Michler, Corban G E Murphey, James Cahoon, and Walter M Weber. Monolithic and Single-Crystalline Aluminum-Silicon Heterostructures. *ACS Applied Materials & Interfaces*, 14:26238–26244, Jun 2022. ISSN 1944-8244.

[30] Nicolas Breil, Christian Lavoie, Ahmet Ozcan, Frieder Baumann, Nancy Klymko, Karen Nummy, Bing Sun, Jean Jordan-Sweet, Jian Yu, Frank Zhu, Shreesh Narasimha, and Michael Chudzik. Challenges of nickel silicidation in CMOS technologies. *Microelectronic Engineering*, 137:79–87, 2015. ISSN 0167-9317.

[31] N S Dellas, S Minassian, J M Redwing, and S E Mohney. Formation of nickel germanide contacts to Ge nanowires. *Applied Physics Letters*, 97:263116, Dec 2010. ISSN 0003-6951.

[32] Y.-L. Chao, Y. Xu, R. Scholz, and J.C.S. Woo. Characterization of copper germanide as contact metal for advanced MOSFETs. *IEEE Electron Device Letters*, 27(7):549–551, 2006.

[33] M A Luong, E Robin, N Pauc, P Gentile, M Sistani, A Lugstein, M Spies, B Fernandez, and M I Den Hertog. In-Situ Transmission Electron Microscopy Imaging of Aluminum Diffusion in Germanium Nanowires for the Fabrication of Sub-10 nm Ge Quantum Disks. *ACS Applied Nano Materials*, 3:1891–1899, Feb 2020.

[34] Helmut Mehrer. *Diffusion in Solids*, volume 155. Springer Berlin Heidelberg, 2007. ISBN 978-3-540-71486-6.

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU WIEN Bibliothek Your knowledge hub

[35] Zoltan Balogh and Guido Schmitz. 5 - Diffusion in Metals and Alloys. In David E Laughlin and Kazuhiro Hono, editors, *Physical Metallurgy (Fifth Edition)*, pages 387–559. Elsevier, 2014. ISBN 978-0-444-53770-6.

[36] K.-W. Ang, K. Majumdar, K. Matthews, C. D. Young, C. Kenney, C. Hobbs, P. D. Kirsch, R. Jammy, R. D. Clark, S. Consiglio, K. Tapily, Y. Trickett, G. Nakamura, C. S. Wajda, G. J. Leusink, M. Rodgers, and S. C. Gausepohl. Effective Schottky Barrier Height modulation using dielectric dipoles for source/drain specific contact resistivity improvement. In *2012 International Electron Devices Meeting*, pages 18.6.1–18.6.4, 2012.

[37] Tomonori Nishimura, Koji Kita, and Akira Toriumi. Evidence for strong Fermi-level pinning due to metal-induced gap states at metal/germanium interface. *Applied Physics Letters*, 91:123123, Sep 2007. ISSN 0003-6951.

[38] Robert Clark. Emerging Applications for High K Materials in VLSI Technology. *Materials*, 7:2913–2944, Apr 2014. ISSN 1996-1944.

[39] Manijeh Razeghi. *Fundamentals of Solid State Engineering*. Springer International Publishing, 2019. ISBN 978-3-319-75707-0.

[40] E.H. Rhoderick and R.H. Williams. *Metal-semiconductor Contacts*. Monographs in electrical and electronic engineering. Clarendon Press, 1988. ISBN 9780198593355.

[41] J.M. Larson and J.P. Snyder. Overview and status of metal S/D Schottky-barrier MOSFET technology. *IEEE Transactions on Electron Devices*, 53(5):1048–1058, 2006.

[42] Andreas Fuchsberger, Lukas Wind, Anibal Pacheco-Sanchez, Johannes Aberl, Moritz Brehm, Lilian Vogl, Peter Schweizer, Masiar Sistani, and Walter M. Weber. A schottky barrier field-effect transistor platform with variable ge content on soi. *Solid-State Electronics*, 230:109221, 2025. ISSN 0038-1101.

[43] W.M. Weber, A. Heinzig, J. Trommer, D. Martin, M. Grube, and T. Mikolajick. Reconfigurable nanowire electronics - A review. *Solid-State Electronics*, 102:12–24, 2014. ISSN 0038-1101. Selected papers from ESSDERC 2013.

[44] T Mikolajick, A Heinzig, J Trommer, T Baldauf, and W M Weber. The RFET - a reconfigurable nanowire transistor and its application to novel electronic circuits and systems. *Semiconductor Science and Technology*, 32(4):043001, Mar 2017.

[45] Raphael Böckle, Masiar Sistani, Martina Bažíková, Lukas Wind, Zahra Sadre-Momtaz, Martien I. den Hertog, Corban G. E. Murphey, James F. Cahoon, and Walter M. Weber. Reconfigurable Complementary and Combinational Logic Based on Monolithic and Single-Crystalline Al-Si Heterostructures. *Advanced Electronic Materials*, 9(1):2200567, 2022.

[46] J Trommer, A Heinzig, T Baldauf, T Mikolajick, W M Weber, M Raitza, and M Völp. Reconfigurable nanowire transistors with multiple independent gates for efficient and

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU Bibliothek Your knowledge hub WIEN

programmable combinational circuits. In *2016 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, pages 169–174, 2016. ISBN 1558-1101.

[47] A Chen, X S Hu, Y Jin, M Niemier, and X Yin. Using emerging technologies for hardware security beyond PUFs. In *2016 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, pages 1544–1549, 2016. ISBN 1558-1101.

[48] Peng Wu, Dayane Reis, Xiaobo Sharon Hu, and Joerg Appenzeller. Two-dimensional transistors with reconfigurable polarities for secure circuits. *Nature Electronics*, 4: 45–53, 2021. ISSN 2520-1131.

[49] J H. Bae, H Kim, D Kwon, S Lim, S T. Lee, B G. Park, and J H. Lee. Reconfigurable Field-Effect Transistor as a Synaptic Device for XNOR Binary Neural Network. *IEEE Electron Device Letters*, 40:624–627, 2019. ISSN 1558-0563.

[50] Ch. Schenk U. Tietze. *Halbleiter-Schaltungstechnik*. Springer-Verlag Berlin Heidelberg GmbH, 1999. ISBN ISBN 3-540-64192-0.

[51] R. Jacob Baker. *CMOS: Circuit Design, Layout, and Simulation*. Wiley-IEEE Press, 3rd edition, 2010.

[52] Behzad Razavi. *Design of Analog CMOS Integrated Circuits*. McGraw-Hill Education, New York, 1st edition, 2001.

[53] Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, and Robert G. Meyer. *Analysis and Design of Analog Integrated Circuits*. John Wiley & Sons, Hoboken, NJ, 5th edition, 2009.

[54] Alexander Klös. *Nanoelektronik - Bauelemente der Zukunft, 2. Auflage*. Carl Hanser Verlag GmbH & Co. KG, 2024.

[55] Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic. *Digital Integrated Circuits: A Design Perspective*. Prentice Hall, 2nd edition, 2003.

[56] Andreas Fuchsberger, Masiar Sistani, Lukas Wind, Daniele Nazzari, Lee-Chi Hung, Jose Maria Gonzalez-Medina, Enrique Prado Navarrete, Johannes Aberl, Moritz Brehm, and Walter M. Weber. Enhancing reconfigurable transistors with ultra-thin epitaxial germanium. In *Proceedings of the IEEE*. IEEE, 2024. Conference paper.

[57] Andreas Fuchsberger, Lukas Wind, Daniele Nazzari, Larissa Kühberger, Daniel Popp, Johannes Aberl, Enrique Prado Navarrete, Moritz Brehm, Lilian Vogl, Peter Schweizer, Sebastian Lellig, Xavier Maeder, Masiar Sistani, and Walter M. Weber. A run-time reconfigurable ge field-effect transistor with symmetric on-states. *IEEE Journal of the Electron Devices Society*, 12:83–87, 2024.

[58] Karl Suss KG. *SUSS PSM 6 Submicron Probe Station*. Karl Suss KG, Munich, Germany, 1988. Product Brochure, Document No. 115 000 18, Printed in W-Germany.

[59] Karl Suss GmbH. *SUSS PH150 Micro Positioner*. SUSS MicroTec Test Systems, Garching, Germany, 2000. Technical Data Sheet, PH150 Manual Probehead.

Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.
TU WIEN Bibliothek Your knowledge hub

[60] Hewlett-Packard Company. *HP 4156B Precision Semiconductor Parameter Analyzer*. Test and Measurement Division, Palo Alto, USA, 1997. Technical Data Sheet, Publication No. 5965-9619E.

[61] Cascade Microtech. *Cascade Summit 11000B-AP Probe Station*. FormFactor Inc., Beaverton, USA, 2022. Technical Data Sheet, Summit 11000 Series Manual Probe Systems.

[62] Cascade Microtech. *DCM210 Precision Micropositioner*. FormFactor Inc., Beaverton, USA, 2008. Technical Data Sheet, DCM Series Micropositioners.

[63] Cascade Microtech. *Cascade Microtech 154-001 Probe Tip*. FormFactor Inc., Beaverton, USA, 2015. Technical Data Sheet, DCP-HTR Probe Tip Specifications.

[64] ERS electronic GmbH. *ERS Air Cool SP72 Thermal System*. ERS electronic GmbH, Germering, Germany, 2019. Technical Data Sheet, Air Cool Thermal Chuck Systems.

[65] Keithley Instruments. *Keithley 4200A-SCS Parameter Analyzer*. Tektronix Inc., Cleveland, USA, 2017. User Manual, Document No. 4200A-900-01 Rev. B.

[66] FormFactor Inc. *PA300 Semi-Automatic Probe Station Datasheet*. Cascade Microtech, Beaverton, USA, 2022. Technical Data Sheet, Document No. PA300 Rev. 3.2.

[67] Keithley Instruments. *Model 4225-RPM Remote Pulse Module Instructions*. Tektronix Inc., Cleveland, USA, 2023. Instruction Manual, Document No. PA-1086 Rev. B.

[68] Keithley Instruments. *4200A-KXCI Command Interface Reference Manual*. Tektronix Inc., Cleveland, USA, 2024. Document No. 4200A-KXCI-907-01 Rev. D.

[69] Keithley Instruments. *Model 4225-PMU Ultra-Fast I-V and Capacitance Module*. Tektronix Inc., Cleveland, USA, 2024. Instruction Manual, Document No. 4200A-PMU-900-01 Rev. C.

[70] Zurich Instruments AG. *Zurich Instruments MFLI Lock-In Amplifier*. Zurich Instruments AG, Zurich, Switzerland, 2023. Technical Datasheet and MF-DIG Upgrade Manual.

TU WIEN Bibliothek Your knowledge hub
Die approbierte gedruckte Originalversion dieser Diplomarbeit ist an der TU Wien Bibliothek verfügbar
The approved original version of this thesis is available in print at TU Wien Bibliothek.