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Abstract

Ultrathin aluminum films in the nanometer-thickness regime are of particular interest for nanoscale interconnects and superconducting nanoelectronics, yet their fabrication is limited by discontinuous growth and rapid oxidation. This thesis establishes a CMOS-compatible platform for continuous and electrically stable aluminum films fabricated from silicon-on-insulator wafers using a thermally induced silicon–aluminum exchange reaction combined with controlled thermal oxidation. By means of lithography, the structures are first defined via reactive ion etching in the SOI device layer, and the target thickness is defined by oxidation-based thinning. The remaining silicon is then locally converted into aluminum during a short annealing step. A key advantage of this approach is the intrinsic oxide encapsulation of the ultrathin aluminum, enabling self-passivation and long-term stability even close to the few-monolayer limit.

Two strategies (subtractive vs. additive processing) for the ultrathin regime are implemented, relying on plasma-enhanced chemical vapor deposition and sputtering of sacrificial protective layers. Both approaches are benchmarked in terms of yield and surface quality, identifying a robust, high-yield processing route. The work establishes a quantitative chain from geometry definition to electrical response by combining complementary metrology: ellipsometry, atomic force microscopy to quantify surface roughness, and cross-sectional transmission electron microscopy and scanning transmission electron microscopy to verify continuity, microstructure, and local thickness down to the few-nanometer range. Electrical characterization links these structural metrics to electrical transport properties, current-carrying capacity measurements, low-frequency noise spectroscopy quantified via the standardized $1/f$ noise power spectral density, and low-temperature measurements to investigate the superconducting properties of such fabricated ultrathin aluminum films.

The results demonstrate continuous aluminum films down to thicknesses of ~ 1 nm and reveal a combination of properties that differs from those of conventionally deposited metallic ultrathin aluminum films: (i) below a thickness of 10 nm, the resistivity decreases with decreasing thickness and approaches values of ultrapure, single-crystalline aluminum; (ii) the current-carrying capability increases strongly in the ultrathin limit, reaching critical current densities on the order of 10^{10} A cm^{-2}; (iii) thinner films exhibit suppressed normalized $1/f$ noise; and (iv) the superconducting transition temperature T_c increases systematically with decreasing thickness, reaching $T_c \sim 2.8$ K at an effective thickness of ~ 1.4 nm. These findings provide an experimental basis for discussing size-effect frameworks (Fuchs–Sondheimer surface scattering and Mayadas–Shatzkes grain-boundary scattering) and for quantifying to what extent interface quality, encapsulation, and nanoscale confinement alter classical expectations. Overall, the thesis delivers a reproducible process–structure–property platform for self-passivated aluminum thin films on an SOI platform and motivates refined transport modeling in the extreme thickness regime.

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Kurzfassung

Ultradünne Aluminiumschichten im Nanometer-Dickenbereich sind für nanoskalige Leiterbahnen und supraleitende Nanoelektronik besonders interessant, ihre Herstellung ist jedoch durch diskontinuierliches Wachstum und schnelle Oxidation begrenzt. Diese Arbeit entwickelt eine CMOS-kompatible Plattform für kontinuierliche, elektrisch stabile Aluminiumschichten auf Silizium-auf-Isolator-Wafern, basierend auf einer thermisch induzierten Silizium–Aluminium-Austauschreaktion und kontrollierter thermischer Oxidation. Lithographie und reaktives Ionenätzen definieren die Geometrie, oxidationsbasiertes Dünnen die Zieldicke. Ein kurzer Annealing-Schritt wandelt verbleibendes Silizium lokal in Aluminium um. Die intrinsische Oxidkapselung ermöglicht Selbstpassivierung und Langzeitstabilität.

Für das ultradünne Regime werden zwei Prozessrouten (subtraktiv vs. additiv) umgesetzt, die plasmaunterstützte chemische Gasphasenabscheidung sowie das Sputtern temporärer Siliziumschichten zum Schutz der Kontaktpads während der Oxidation nutzen. Beide Ansätze werden hinsichtlich Ausbeute und Oberflächenqualität verglichen, wodurch eine robuste Prozessroute von hoher Ausbeute identifiziert wird. Die Arbeit etabliert eine quantitative Prozess–Struktur–Eigenschafts-Kette durch die Kombination komplementärer Metrologie: Ellipsometrie zur Dickenbestimmung, Rasterkraftmikroskopie zur Quantifizierung der Oberflächenrauheit sowie (Raster-)Transmissionselektronenmikroskopie im Querschnitt zur Verifikation von Kontinuität, Mikrostruktur und lokaler Dicke bis in den Bereich weniger Nanometer. Die elektrische Charakterisierung verknüpft diese Strukturgrößen mit elektrischen Transporteigenschaften, Messungen der Stromtragfähigkeit, Niederfrequenz-Rauschspektroskopie (quantifiziert über die standardisierte $1/f$-Rauschleistungsdichtespektraldichte) sowie Tieftemperaturmessungen zur Untersuchung der supraleitenden Eigenschaften der hergestellten ultradünnen Aluminiumschichten.

Die Ergebnisse zeigen kontinuierliche Aluminiumschichten bis hin zu Dicken von $\sim 1\,\mathrm{nm}$ und eine Eigenschaftskombination, die sich von konventionell abgeschiedenen ultradünnen Aluminiumfilmen unterscheidet: (i) unterhalb von $10\,\mathrm{nm}$ nimmt die spezifische Resistivität mit abnehmender Dicke ab und nähert sich Werten von hochreinem, einkristallinem Aluminium; (ii) die Stromtragfähigkeit steigt im ultradünnen Grenzfall deutlich an und erreicht kritische Stromdichten in der Größenordnung von $10^{10}\,\mathrm{A\,cm^{-2}}$; (iii) dünnere Schichten weisen ein unterdrücktes normiertes $1/f$-Rauschen auf; und (iv) die supraleitende Übergangstemperatur T_c steigt systematisch mit abnehmender Dicke und erreicht $T_\mathrm{c} \sim 2.8\,\mathrm{K}$ bei einer effektiven Dicke von $\sim 1.4\,\mathrm{nm}$. Diese Befunde liefern eine experimentelle Grundlage zur Einordnung von Größeneffekt-Modellen (Fuchs–Sondheimer-Oberflächenstreuung und Mayadas–Shatzkes-Korngrenzenstreuung) und zur Quantifizierung, in welchem Ausmaß Grenzflächenqualität, Kapselung und geometrische Einengung klassische Erwartungen verändern. Insgesamt stellt die Arbeit eine reproduzierbare Prozess–Struktur–Eigenschafts-Plattform für selbstpassivierte Aluminiumschichten auf einer SOI-Plattform bereit und motiviert eine verfeinerte Transportmodellierung im extremen Dickenregime.

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To my colleagues at TU Wien

To my friends

To my family

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List of abbreviations

Abbreviation	Meaning
AFM	atomic force microscopy
BF-STEM	bright-field scanning transmission electron microscopy
BOE	buffered oxide etch
BOX	buried oxide
DL	device layer
DOS	density of states
EDX	energy-dispersive X-ray spectroscopy
el–ph	electron–phonon
EM	electromigration
FIB	focused ion beam
FS	Fuchs–Sondheimer model
HAADF-STEM	high-angle annular dark-field scanning transmission electron microscopy
HF	hydrofluoric acid
I–V	current–voltage
JJ	Josephson junction
MBE	molecular beam epitaxy
MS	Mayadas–Shatzkes model
PECVD	plasma-enhanced chemical vapor deposition
QSE	quantum size effect
RIE	reactive ion etching
RTA	rapid thermal annealing
SOI	silicon-on-insulator
STEM-EDX	scanning transmission electron microscopy with energy-dispersive X-ray spectroscopy
TEM	transmission electron microscopy
TIER	thermally-induced exchange reaction
UTF	ultrathin film

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Chapter 1

Introduction

Thin films ($<1\,\mu m$) are indispensable in modern technology, whether for optimizing surface coatings [1], fabricating microchips and sensors [2], or validating and extending models from fundamental research [3]. In the literature, the term ultrathin film (UTF) is used with varying thickness criteria. In many works, films thinner than 100 nm are classified as ultrathin [4–7], whereas other studies – particularly those addressing size-quantization and interface-dominated phenomena – apply the term primarily to thicknesses below 10 nm [8–11]. In this thesis, UTF refers to layers thinner than 10 nm, because the measurements presented here indicate that the relevant changes in physical properties become most pronounced in this thickness range. The properties of thin films and UTFs have been under intensive investigation for nearly 90 years [12], and new models and fabrication processes continue to be developed.

The discussion of changes in the physical properties of metallic UTFs, particularly the electrical resistivity, is often grounded in the validated and extended Fuchs–Sondheimer (FS) and Mayadas–Shatzkes (MS) models, which provide a theoretical framework to describe the experimentally observed increase in electrical resistivity when the layers become (ultra)thin [12–17]. Beyond classical descriptions, extended models for UTFs include quantum-effect-based formalisms [18–22], Monte Carlo and atomic-scale simulation approaches [23–25], as well as parameter-augmented models [26–28]. These approaches target key effects in UTFs, most notably quantum interference and size effects, stochastic scattering captured by Monte Carlo/atomistic treatments, and additional surface- or microstructure-related contributions that strongly influence their physical properties [18–28]. Metals frequently analyzed in the literature with regard to their thin film properties are those from groups 10, 11, and 13 of the periodic table, namely platinum, copper, silver, gold, and aluminum (Al). In addition, post-transition metals such as lead, bismuth, and others are often studied for their pronounced superconducting [29–33] and quantum size effects [34–42] in thin-film systems. The models for UTFs discussed in the literature differ in their underlying ap-

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proach (classical, semiclassical, or quantum-mechanical) and in model complexity, i.e., in the number of adjustable parameters, but largely arrive at conclusions similar to those of the classical FS/MS framework, namely that the resistivity increases with decreasing film thickness.

To fabricate ultrathin Al films for characterization and optimization of the models, deposition systems are predominantly used to deposit individual atoms or atomic layers onto a substrate [30, 43]. Classical deposition techniques such as thermal evaporation or sputtering lead to surface roughness, island growth, and grain boundaries [44, 45] and therefore enhanced (surface) scattering events. In established models, this additional scattering contributes to the increase in electrical resistivity in UTFs. In addition, UTFs in the range of several atomic layers are subject to the quantum size effect, which, through geometric confinement, modifies the electron wave function and is thus expected to influence physical properties [46, 47]. Moreover, Anderson localization is expected to occur at grain boundaries within the UTFs [48]. If a perfectly crystalline ultrathin metallic conductor could be realized, the resistivity enhancement typically observed in such conductors would be dramatically reduced [49, 50]. This would constitute an important milestone in reducing power consumption caused by interconnect line resistances in microchips, thereby supporting Moore's law and advancing ultra-large-scale integration applications [51]. Moreover, exploiting the physical properties of UTFs, such as changes in the superconducting transition temperature (T_c), would be advantageous for the scaling and stability of quantum-computing applications, in particular in the context of Josephson junctions [52, 53].

Ultrathin Al is attractive owing to its high electrical conductivity and carrier concentration, and it is widely used as a contact metal in electronic applications [54]. Furthermore, Al is well suited for detailed theoretical analysis and quantitative modeling of crystals and their thermodynamic properties due to its well-studied electronic structure [55–57]. However, in processing Al UTFs, one must account for oxidation [30, 58]. Without suitable passivation, several nanometers of Al at the interface to ambient oxygen are converted into electrically insulating aluminum oxide [59–61], which makes the reproducible production of high-quality, stable, ultrathin Al structures a difficult task. This thesis employs the thermally induced exchange reaction (TIER) process to fabricate Al UTFs [62–65].

Using the processing approaches presented in this thesis, based on silicon-on-insulator (SOI) substrates [66, 67], thermal oxidation [68–77] and TIER, high-quality, crystalline, and self-passivated Al thin films with thicknesses down to 1 nm can be fabricated. An overview of the theoretical fundamentals necessary to understand the processing and the changes in the physical properties of UTFs is provided in chapter 2. To achieve UTFs, three different processing methods are explored and presented in chapter 3. Selected physical properties of the resulting Al structures are characterized and discussed in chapter 4. This work provides a basis for further research on Al UTFs for, e.g., Josephson-junction quantum-computing applications, as discussed in chapter 5.

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Chapter 2

Theory

First, an overview of state-of-the-art methods used to produce UTFs is given, followed by a discussion of the main physico-chemical properties of the elements used in this thesis – Al and Si – which are processed with the aid of SOI wafers to obtain highly crystalline, self-passivated, ultrathin Al films. In the context of the novel processing route presented in this thesis, the associated exchange process, TIER, is then explained in detail. Existing models for predicting the physical properties of UTFs are introduced, and the resulting implications for highly crystalline ultrathin Al are described. The discussion covers electrical resistivity, ampacity, and maximum power density, $1/f$ noise, and superconductivity.

2.1 Material and process fundamentals

The fabrication of ultrathin Al films is typically managed by the deposition of solid materials from the gas phase onto a substrate, forming the desired film [78]. These processes include thermal evaporation, plasma-enhanced chemical vapor deposition (PECVD), atomic layer deposition, molecular beam epitaxy (MBE), (magnetron) sputtering, and others [79, 80]. The various techniques differ in complexity, in the quality of the resulting films, and in the type of precursor materials used. Further details on these processing techniques can be found in comprehensive handbooks [81–85], general review papers [1, 45, 86–90], and research papers focusing specifically on the fabrication of Al films [43, 91–96]. In this thesis, ultrathin Al films are fabricated using SOI wafers as substrates. The device layer (DL) thickness is adjusted by thermal oxidation. This Si thickness is subsequently transferred to Al via TIER. Reference samples are prepared by conventional Al sputter deposition.

2.1.1 Physico-chemical properties of Al, Si, and SOI

In the following, the relevant properties of Al, Si, and the SOI are summarized.

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2.1.1.1 Aluminum

Al is a silvery-white, lightweight, and ductile metal of major technological relevance [97, 98], belonging to group III of the periodic table and having atomic number 13. The main properties are listed in the appendix (see Table C.1). With an average concentration of $\sim 8\,\%$ by mass in the earth's crust, it is the most abundant metal and the third most prevalent element overall, after oxygen and Si [99, 100]. Naturally occurring Al consists almost entirely of the stable isotope ^{27}Al [101]. It has a melting point of approximately 933 K and crystallizes in the face-centered cubic lattice structure with a lattice constant of $a \sim 0.4$ nm [102]. The interatomic spacing along the (111) crystallographic direction is given by $d_{111} = \frac{a}{\sqrt{3}} \approx 0.23$ nm. Pure crystalline Al exhibits an electrical resistivity of approximately $2.7 \times 10^{-6}\,\Omega\,\mathrm{cm}$ and a thermal conductivity of $\sim 240\,\mathrm{W\,m^{-1}\,K^{-1}}$ [103–105]. In terms of electrical conductivity, it ranks fourth among common metals, after silver, copper, and gold [106]. These properties make Al a widely used interconnect material in microelectronics. A key characteristic of Al is its rapid oxidation upon exposure to air, forming a native amorphous Al oxide layer that stabilizes at a thickness of about 5 nm [30, 60]. This oxide layer is dense, adherent, and electrically insulating, protecting the underlying metal from further corrosion and mechanical degradation. In the processing of UTFs, the oxidation of Al is undesirable and must be prevented through appropriate passivation measures, as presented in section 3.3. Optically, bulk Al is highly reflective ($>90\,\%$) in the visible spectral range and beyond [107], and exhibits decreased reflectivity for UTFs [30, 96]. Bulk Al is a type I superconductor with a transition temperature of ~ 1.2 K [108].

2.1.1.2 Silicon

Si is a gray, brittle metalloid and an elemental semiconductor belonging to group IV of the periodic table with the atomic number 14. The main properties are listed in the appendix (see Table C.1). With an average abundance of $\sim 25\,\%$ by weight in the earth's crust, Si is the second most abundant element after oxygen [99, 100]. Naturally occurring Si consists of three stable isotopes, ^{28}Si, ^{29}Si, and ^{30}Si, with approximate relative abundances of 92.2 %, 4.7 %, and 3.1 %, respectively [109]. Si has a melting point of ~ 1683 K and crystallizes in a diamond cubic crystal structure [83]. The arrangement of atoms in a Si wafer is determined by the orientation of the cubic lattice relative to the surface, e.g., Si (100) [110]. Different orientations result in varying surface atomic densities and distinct cleaving behaviors. The lattice spacing between Si atoms in the (100) direction is ~ 0.54 nm [111], while the effective distance between consecutive atomic planes in different directions can be smaller. During Si wafer production, crystal defects such as point defects and dislocations may occur [83]. A key advantage of Si compared to many other semiconductors is its ability to form a stable and high-quality oxide. A native oxide layer with a thickness of up to about 4 nm grows spontaneously in ambient air [74], whereas significantly thicker SiO_2 layers can be grown by thermal oxidation under controlled conditions [69, 70, 112]. By applying the float-zone process, extremely pure Si with a resistivity greater than $1\,\mathrm{k\Omega\,cm}$ can be produced; such Si contains significantly lower concentrations of oxygen, carbon, boron, and

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phosphorus than in Czochralski-grown Si [83]. Furthermore, lightly doped Si exhibits an electron mobility of $\sim 1400\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ and a hole mobility of $\sim 450\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ [113, 114]. Si and its oxide are widely used in optical applications, particularly in photonics and fiber optics, since SiO_2 is transparent in the optical range and beyond (wavelengths between 200 nm to 4000 nm) [115], as well as in modern electronics [116, 117].

2.1.1.3 Silicon-on-insulator

SOI is a semiconductor substrate that is widely used to improve device performance and reduce parasitic effects compared with devices fabricated on conventional bulk Si wafers [67]. An SOI wafer consists of three main layers [66, 118]: a thin crystalline Si layer on top, called the device layer, an insulating buried oxide (BOX) layer in the middle, and a thick Si handle wafer at the bottom, as schematically shown in Figure 2.1.

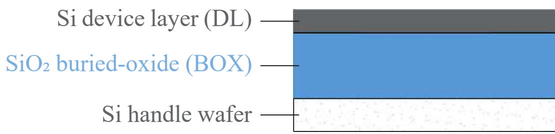

Figure 2.1: *Schematic illustration of the layer stack of a SOI wafer, consisting of the Si device layer (DL), the SiO_2 buried-oxide (BOX), and the Si handle wafer.*

The BOX layer, typically made of SiO_2, electrically isolates the active Si layer from the substrate and suppresses junction leakage [119]. The DL usually has a thickness in the range of 5 nm to 2000 nm with a surface roughness below 1 nm [66, 120], while the BOX thickness commonly ranges between 5 nm to 5000 nm [67]. SOI wafers are fabricated using several key techniques, the most prominent being the *Smart Cut* process, introduced by Bruel at CEA-Leti in the 1990s [121, 122]. The SOI structure offers several electrical and thermal advantages. The presence of the BOX layer reduces parasitic capacitance, leading to higher switching speeds in microchips and lower dynamic power consumption [119]. From a mechanical and thermal perspective, the inclusion of the SiO_2 BOX introduces a thermal barrier that affects heat dissipation, which must be considered in high-power or high-frequency designs [66].

2.1.2 Thermally-induced exchange reaction in the Al–Si system

In this thesis TIER describes a solid-state conversion process in which Si in contact with Al is replaced by Al during a rapid thermal annealing (RTA) treatment. Thermally induced Al–Si exchange is reported in the literature [64, 65] to be a result of asymmetric diffusion behavior and solid solubility. This section summarizes the diffusion concepts and mechanisms of TIER.

2.1.2.1 Fundamentals of solid state diffusion

Diffusion is the thermally activated transport of atoms driven by concentration gradients and caused in random thermal motion. Compared with gases and liquids, diffusion in

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solids is typically slow; however, near the melting point of metals, diffusion rates can reach the order of $1\,\mu\mathrm{m\,s^{-1}}$ but decrease strongly with decreasing temperature.

In crystalline solids, atomic diffusion occurs mainly via point defects. In metals, vacancies are the most common thermally generated defects and diffusion often proceeds by atoms jumping into neighboring vacancies [62, 63]. In addition, diffusion can proceed by the indirect interstitial mechanism [62, 63], a collective process in which an interstitial atom displaces a lattice atom that subsequently becomes interstitial, such that both atoms move in a coupled manner. For Al, and most fcc metals, vacancy-mediated diffusion is the dominant mechanism for self- and interdiffusion. In Si, self-diffusion comprises both vacancy and interstitialcy contributions, with interstitialcy-mediated diffusion dominating at higher temperatures, with a vacancy-mediated diffusion at lower temperatures; the cross-over temperature is near 1163 K. [62, 63]

On the continuum level, diffusion flux is described by Fick's first law,

$$\mathbf{J} = -D\nabla C, \tag{2.1}$$

where $\mathbf{J}$ points opposite to the concentration gradient ∇C and D is the diffusivity. The diffusivity is a material specific parameter and typically follows an Arrhenius-type temperature dependence,

$$D = D_0 \exp\left(-\frac{E_\mathrm{a}}{RT}\right), \tag{2.2}$$

with pre-exponential factor D_0, activation energy E_a, gas constant R, and absolute temperature T. Combined with mass conservation, equation (2.1) yields Fick's second law for time-dependent concentration fields. [63]

For many diffusion-controlled processes, a compact estimate for the characteristic transport length is

$$L \sim \sqrt{2Dt}, \tag{2.3}$$

reflecting the parabolic kinetics expected for diffusion limitation. [63]

In binary systems, the two components generally exhibit different intrinsic diffusivities and therefore different intrinsic diffusion fluxes. This inequality produces a net mass flow during interdiffusion and can shift the apparent interface position, an effect known as the Kirkendall effect. In the diffusion-theory framework, the interface shift is associated with vacancy creation and annihilation required to maintain local site balance as the interdiffusion zone moves. The interface motion can be expressed by the Kirkendall velocity v_K in terms of intrinsic fluxes j_A, j_B and partial molar volumes $\tilde{V}_A$, $\tilde{V}_B$:

$$v_K = -\left(\tilde{V}_A j_A + \tilde{V}_B j_B\right). \tag{2.4}$$

Accordingly, the Kirkendall plane position can evolve parabolically in time, $x_K = K\sqrt{t}$, with a temperature dependent constant K, implying diffusion-controlled behavior, and

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$v_K \equiv dx_K/dt = x_K/(2t)$. The Kirkendall effect is technologically relevant in a range of contexts, including coatings and microelectronic devices. [62, 63]

2.1.2.2 Al–Si exchange: solid-solubility limit and kinetic implications

In the context of TIER, the Kirkendall-type interface shift is consistent with an Al/Si boundary that advances into the Si structure while Si is transported into the Al pad, where it can be accommodated only up to the solid-solubility limit, see Figure 2.2. [62, 63, 123]

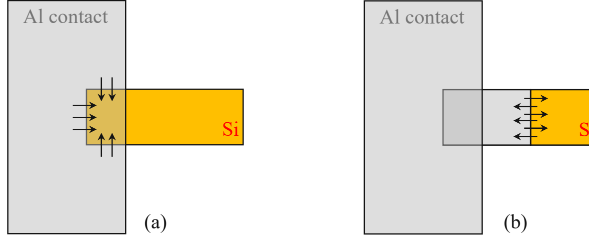

Figure 2.2: *Solid-state Al–Si exchange in a Si nanowire. (a) Al advances from the contact pad with an abrupt front, (b) while Si diffuses into the Al contact. Image adapted and modified from [63].*

The exchange reaction is supposed to stop when the dissolved Si in the Al contacts surpasses its solid solubility limit at about 0.76 % at 773 K, as illustrated in Figure 2.3. The phase diagram of the binary system Al–Si is shown in the range up to 2 % Si.

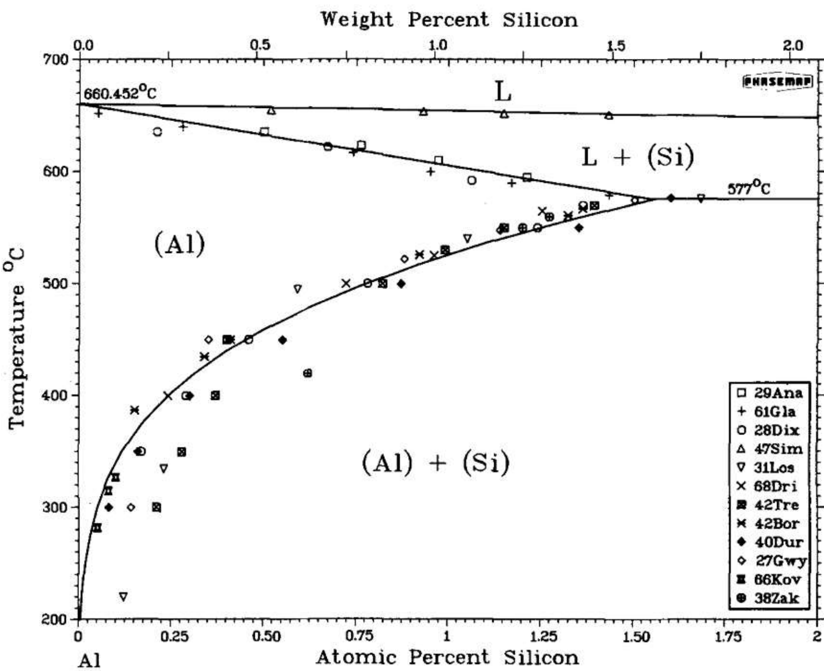

Figure 2.3: *Phase diagram of the Al–Si system. At 773 K (500 °C), the solubility limit of Si in Al is below 1 %. Image adapted from [123].*

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The propagation of an exchange front in thermally activated metal–semiconductor exchange reactions is not necessarily constant in time, because different rate-limiting processes can dominate. Using kinetic analogies (e.g. the Deal–Grove oxidation picture), four limiting cases can be distinguished and their characteristic scaling of the exchanged length L with annealing time t and nanowire radius R can be summarized: metal-reservoir-limited ($L \propto R^{-1}t$), interfacial-exchange-limited ($L \propto t$), volume-diffusion-limited ($L \propto \sqrt{t}$), and surface-diffusion-limited ($L \propto \sqrt{t/R}$). This classification is useful to assess whether an observed TIER propagation is governed primarily by reservoir capacity, interface kinetics, or diffusion pathways. [63]

For Al–Si, Wind *et al.* demonstrate monolithic Al–Si heterostructures formed from Si nanostructures and Al contacts by a thermally induced Al–Si exchange reaction, yielding abrupt and void-free metal–semiconductor interfaces. Their interpretation emphasizes (i) the Al–Si phase diagram, which exhibits a single eutectic point and no solid intermetallic stoichiometry, and (ii) a pronounced diffusion asymmetry: Si diffusion in Al and Al self-diffusion are comparatively high, whereas Al diffusion in Si is reported to be smaller by around 13 orders of magnitude. Consequently, Al atoms can be supplied efficiently through the already exchanged Al segment to sustain the advancing exchange front. In the same context, Si diffusion in Al is discussed assuming interstitial-mediated transport, and Si atoms are suggested to diffuse through the exchanged Al segment and ultimately through the Al pad and/or to the surface, depending on surface passivation. The exchange reaction at $T = 774\,\mathrm{K}$ is considered a solid-state process (below the eutectic temperature), consistent with phase-diagram arguments. [64]

In a related context, Wind *et al.* discuss thermally induced exchange in Al-based metal–semiconductor heterostructures and report that no intermetallic phases are found after exchange, while abrupt, flat, and void-free junctions of high structural quality can be obtained. They attribute this to the combined influence of phase-diagram constraints and diffusion behavior at $T = 774\,\mathrm{K}$. For short annealing durations ($\leq 5\,\mathrm{min}$), certain cross-diffusion processes are argued to be negligible, whereas extended annealing can fully transform the nanosheet into pure Al; this is supported by a reported resistivity of $\rho = (9.7 \pm 4.4) \times 10^{-8}\,\Omega\mathrm{m}$ (fully exchanged layers) and by structural characterization (transmission electron microscopy (TEM)/energy-dispersive X-ray spectroscopy (EDX)) indicating monolithic and single-crystalline heterostructures. [124]

2.2 Electronic transport in ultrathin films

UTFs exhibit electrical behavior that differs from that of bulk films. The following subsections introduce the fundamental principles of electrical resistivity, ampacity, $1/f$ noise, and superconductivity, and explain the behavior of bulk materials compared to UTFs based on the current state of research.

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2.2.1 Resistivity models: classical and quantum approaches

Electrical transport in solids is limited by scattering of conduction electrons, which increases the electrical resistance R. In a simplified picture, R can be viewed as a function of three main scattering contributions: Coulomb scattering at charged defects/impurities, electron–phonon scattering, and surface-roughness scattering. In thin films, the surface-roughness contribution becomes increasingly important as the film thickness approaches the electron mean free path.

Classical thin-film transport theories such as FS [12, 13] and MS [14, 15] predict that the resistivity increases as the film becomes thinner due to enhanced surface and grain-boundary scattering, a trend that is confirmed by further investigations [3, 14, 16, 20, 28, 51, 79, 125–128]. Within the FS framework, the resistivity in the thin-film regime can be approximated by

$$\rho \propto \rho_0 \, f(p) \, \frac{1}{\kappa \, \ln(1/\kappa)}, \qquad \text{with } \kappa \equiv \frac{t}{\lambda_e} \text{ and } \kappa \ll 1. \tag{2.5}$$

Here, ρ_0 denotes the bulk resistivity at the measurement temperature. The factor $f(p)$ encodes the surface-scattering specularity, where $p = 0$ corresponds to fully diffuse and $p = 1$ to fully specular scattering, and $\kappa = t/\lambda_e$ denotes the ratio of film thickness to electron mean free path. Thus, the thin-film limit corresponds to thicknesses t much smaller than λ_e (i.e., $t \ll \lambda_e$), such that decreasing t increases ρ. In addition, the MS model accounts for grain-boundary reflection with a reflection coefficient R_{refl} and the parameter α, which is proportional to the resistivity ρ. Specifically,

$$\rho \propto \alpha, \qquad \alpha = \frac{\lambda_e}{D(t)} \frac{R_{refl}}{1 - R_{refl}} \quad \Rightarrow \quad \rho \propto \frac{\lambda_e}{D(t)} \frac{R_{refl}}{1 - R_{refl}}. \tag{2.6}$$

At the measurement temperature, λ_e denotes the bulk electron mean free path [55, 129], and $D(t)$ denotes the grain-size radius as a function of the film thickness t. When D is reduced, α and hence ρ increase [15].

$$D(t) \sim t \quad \Rightarrow \quad \rho \propto \frac{\lambda_e}{t} \frac{R_{refl}}{1 - R_{refl}}. \tag{2.7}$$

This behavior is consistently observed in metallic UTFs of various compositions and preparation methods (see, e.g., the references cited above) and is exemplified for sputter-deposited Al in Figure 2.4.

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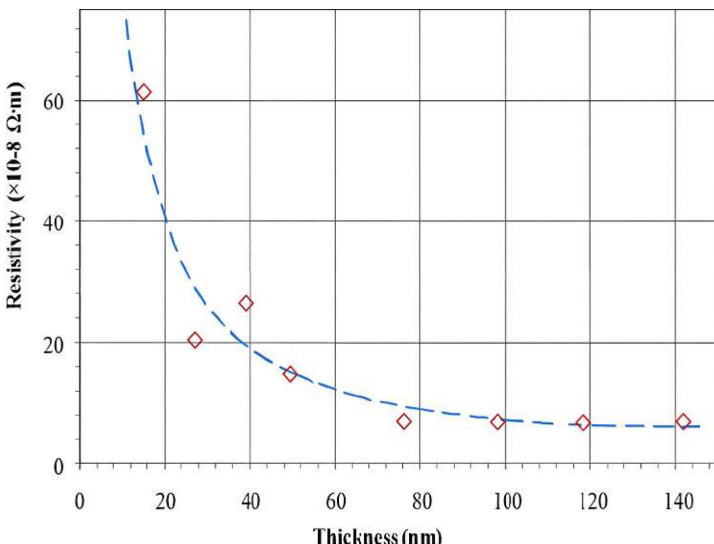

Figure 2.4: *Resistivity of sputtered Al as a function of film thickness. Dots: measured data; dashed line: least-squares fit. Image adapted and modified from [96].*

An extension of the classical models is provided by quantum-theoretical considerations [19–22, 56, 130, 131]. These approaches take into account geometric confinement effects caused by the limited thickness or lateral dimensions of the investigated films, whereby specific states of the electron wave function are restricted. Moreover, the so-called Anderson localization can contribute to changes in the electrical resistance of UTFs [20, 22, 47, 48, 132], in which delocalized electrons, due to their wave-like nature, become localized at grain boundaries as they propagate through the films. Modified electron–phonon (el–ph) [133–135] interactions can also be considered as a contributing factor to the variation of electrical resistance with film thickness, taking into account the electron mean free path λ_e in UTFs [136–138], which, for Al at room temperature, is $\lambda_{e,RT} = 18.9\,\text{nm}$ [137].

It is assumed that, with decreasing film thickness, surface scattering increasingly accounts for the dominant portion of the electrical resistance [19]. However, other simulation studies have shown that grain boundaries exert a significant influence [23, 24] and that multiple scattering events associated with roughness can contribute substantially to the overall resistivity [25]. It should be noted that the crystal orientation can also influence the resistivity of UTFs, as demonstrated for zinc oxide–silver stacks (ZnO/Ag/ZnO) [47], and that both doping [139–141] and overlayers [142] can further modify it. In addition, several studies suggest deviations from conventional model predictions for Al UTFs grown by MBE [30, 92, 95]. In these investigations, the resistivity *decreases* for film thicknesses in the range of 8 nm to 50 nm, which, according to their modeling, is attributed to variable-range hopping and the high structural quality of the fabricated films.

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2.2.2 Ampacity and maximum power density

We define *ampacity* as the maximum sustainable current density J_{crit}, given by the maximum ratio of the electrical current I to the device cross-sectional area A_{dev} with width w and thickness t,

$$J_{\text{crit}}(t) = \max\left(\frac{I}{A_{\text{dev}}}\right), \qquad A_{\text{dev}} = w\,t, \tag{2.8}$$

and the corresponding maximum power density per device cross-sectional area, with the applied voltage V, as

$$P_{\max} = \max\left(\frac{IV}{A_{\text{dev}}}\right) . \tag{2.9}$$

If current and voltage are recorded during an I–V sweep until the device fails due to Joule heating, and the device geometry is known, the corresponding parameters can be obtained by dividing the maximum recorded current at the corresponding applied voltage by A_{dev}. The I–V sweep must therefore be performed sufficiently slowly to ensure that the device remains in thermal equilibrium. Using these current and voltage values, $P_{\max}$ can likewise be calculated via A_{dev}. In Figure 2.5, an overview of the ampacity versus conductivity of various nanocarbons and metals is presented. Previous studies [143] on Al nanowires can be classified into a distinct category next to carbon nanotube–copper composites (CNT–Cu) [144], characterized by both high conductivity and high ampacity.

At high currents and long duration, electromigration (EM) can occur [145–147]. EM refers to the transport of atoms within a conductor driven by the flow of electric current, as shown in Figure 2.6. When the current density exceeds a critical threshold, momentum transfer from electrons cause atoms to detach from their lattice sites and migrate along the current path. This process leads to the formation of atomic voids and hillocks. The growth of voids can eventually disrupt electrical continuity and cause open-circuit failures, whereas the accumulation of material elsewhere can lead to short-circuit formation. The driving forces are the direct electric-field force F_{direct}, arising from the applied macroscopic electric field, and the so-called electron-wind force F_{wind}, which is caused by momentum transfer from conduction electrons to the lattice atoms in the presence of the electric field [145]. In this work, the measured ampacity is limited by Joule-heating-induced failure rather than by electromigration.

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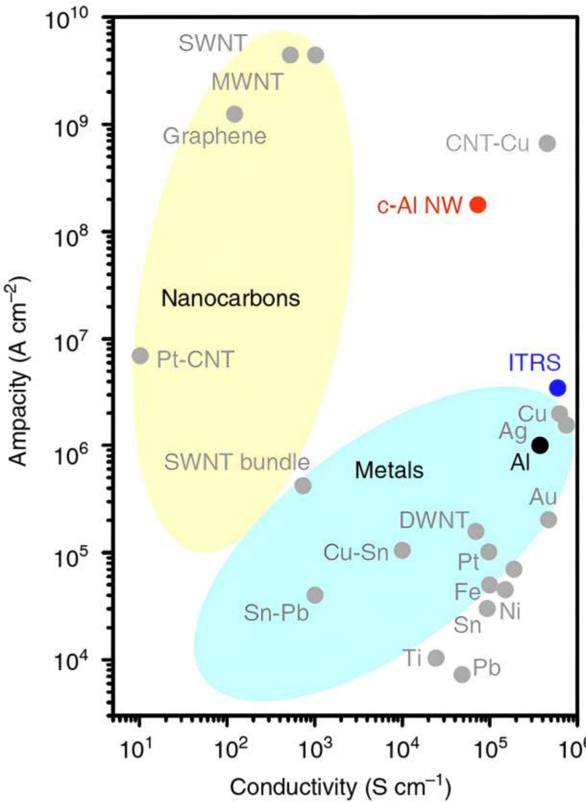

Figure 2.5: *Ampacity vs. conductivity of different materials, where crystalline Al nanowires (c-Al NWs) stand out due to their high ampacity at high conductivity. Image adapted from [143].*

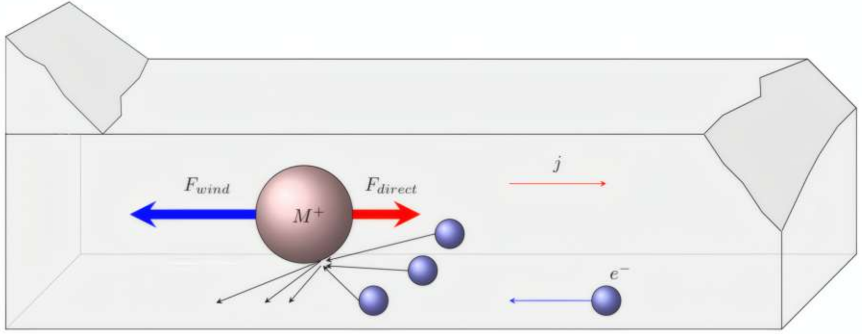

Figure 2.6: *Electromigration in a conductor: metal ions M^+ are driven by the direct force F_{direct} (electric field) and the electron-wind force F_{wind} (momentum transfer from electrons e^-) under a current density j. Image adapted from [145].*

2.2.3 $1/f$ noise: Hooge formalism and normalization

Low-frequency noise serves as a sensitive probe for material quality and reliability, providing insights into defects, interfaces, and charge transport processes [81, 148]. In conductive

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materials at low frequencies, resistivity fluctuations with an approximate $1/f$ dependence are nearly universal [149]. The power spectral density $S(f)$ of $1/f$ noise follows

$$S(f) \propto f^{-\alpha} \tag{2.10}$$

with $0.8 < \alpha < 1.4$. The power spectral density of the resistance fluctuations $S_\mathrm{R}(f)$ at frequency f is empirically described by the Hooge relation [150]

$$\frac{S_\mathrm{R}(f)}{R^2} = \frac{\alpha_\mathrm{H}}{N_\mathrm{c} f}. \tag{2.11}$$

Here, α_H is the empirical Hooge parameter quantifying the noise level, R is the total sample resistance, and N_c denotes the number of charge carriers contributing to conduction [151]. The normalized noise power spectrum $\frac{S_\mathrm{R}(f)}{R^2}$ thus provides a material-specific measure that is independent of the absolute resistance value. The dominant sources of $1/f$ noise are generally bulk-related, including defect motion, el–ph interactions, carrier number fluctuations, and vacancy diffusion [150, 152]. In metals, defect dynamics play a central role [150]. Experiments on polycrystalline Al films indicate that vacancies are mainly generated at grain boundaries, with diffusion lengths comparable to the mean grain size. Accordingly, Al typically exhibits increasing $1/f$ noise with decreasing grain size and, under conventional fabrication routes, also with decreasing film thickness, since thinner films (i) average over a smaller conducting volume (fewer carriers) and (ii) are increasingly dominated by fluctuating scattering at grain boundaries and surfaces/interfaces [150]. To clarify the different forms of the power spectral density in the literature, as seen in Figure 2.7, S_V denotes the *voltage fluctuations*, whereas S_R refers to *resistance fluctuations*. Both quantities are related by $S_\mathrm{V} = I^2 S_\mathrm{R}$ and therefore represent the same $1/f$ noise in different forms. The spectra in Figure 2.7 are measured at 300 K on a MBE-grown Al film of 10 nm thickness with a 3 nm Al_2O_3 cap and a single-crystal sapphire substrate under different bias voltages [153].

The following discussion summarizes the main observations reported in Ref. [150]. The noise level strongly depends on the structural quality of the film. High-purity, annealed Al films with few mobile defects show minimal $1/f$ noise, while films containing numerous microdefects exhibit significantly higher levels. Alloying Al with a small Si content ($\approx 1\,\%$) reduces the noise magnitude compared to pure Al films. The $1/f$ noise is also temperature- and stress-dependent and can evolve over time. Low $1/f$ noise corresponding to $\alpha_\mathrm{H} \approx 2 \times 10^{-3}$ occurs in high-quality films with a low concentration of mobile defects, whose resistivity is comparable to bulk metals. Films with many stable but few mobile defects can also exhibit low noise. The magnitude of $1/f$ noise is often used as an indicator of the EM resistance of thin-film metallizations. For reliable thickness-dependent studies, films with similar concentrations of microdefects and impurities are required, as the noise level

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can vary by orders of magnitude between samples of identical thickness.

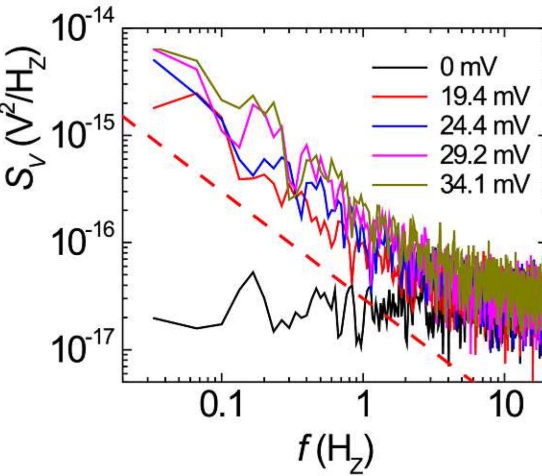

Figure 2.7: *PSD of a MBE-grown Al film of* 10 nm *thickness at* 300 K *under various driving voltages. The dashed line indicates $S_V \propto f^{-1}$ and is a guide to the eye. Image adapted and modified from [153].*

2.2.4 Superconductivity in ultrathin Al layers

Following the discussion in [135], the electrical resistivity in metals is mainly governed by el–ph and electron–electron interactions (see also [154, 155]). As temperature decreases, the phonon population decreases approximately linearly, reducing the el–ph scattering rate and thereby increasing the conductivity. Below a certain critical temperature T_c, some metals transition into the superconducting state, which is characterized by zero resistivity and perfect diamagnetism due to the Meissner effect [110, 156]. In these superconducting materials, there is a drastic change in the behavior of the conduction electrons, characterized within the Bardeen–Cooper–Schrieffer (BCS) theory by the appearance of long-range order, and by an energy gap $E_\Delta \sim 10^{-4}$ eV in their excitation spectrum, with superconductivity arising from a weak attractive interaction between electrons mediated by phonons. The critical temperature T_c depends on the atomic mass (isotope effect), confirming the role of the el–ph coupling. Elements with stronger el–ph interactions, e.g. lead ($T_c = 7.2$ K), exhibit higher transition temperatures [108], whereas noble metals with weaker coupling are poor superconductors. Studies show that the superconducting properties of Al can change in UTFs. In epitaxial Al films approaching the monolayer limit, an increase in T_c is observed, potentially due to additional low-energy excitations such as plasmons [32]. More generally, Al UTFs exhibit a thickness-dependent enhancement of T_c as the film thickness is reduced. Figure 2.8 shows values of $T_c \approx 2.2$ K and $T_c \approx 2.4$ K according to [157] and [33], respectively, i.e., roughly twice the bulk value $T_{c,\text{bulk}} \approx 1.2$ K. Density functional theory calculations link this behavior to surface phonon softening and an increased electronic density of states (DOS), both of which enhance the el–ph coupling. The abrupt decrease in resistivity with decreasing temperature, shown in Figure 2.8 (a), defines the transition temperature. In Ref. [33], the ultrathin epitaxial Al films are grown by solid-source

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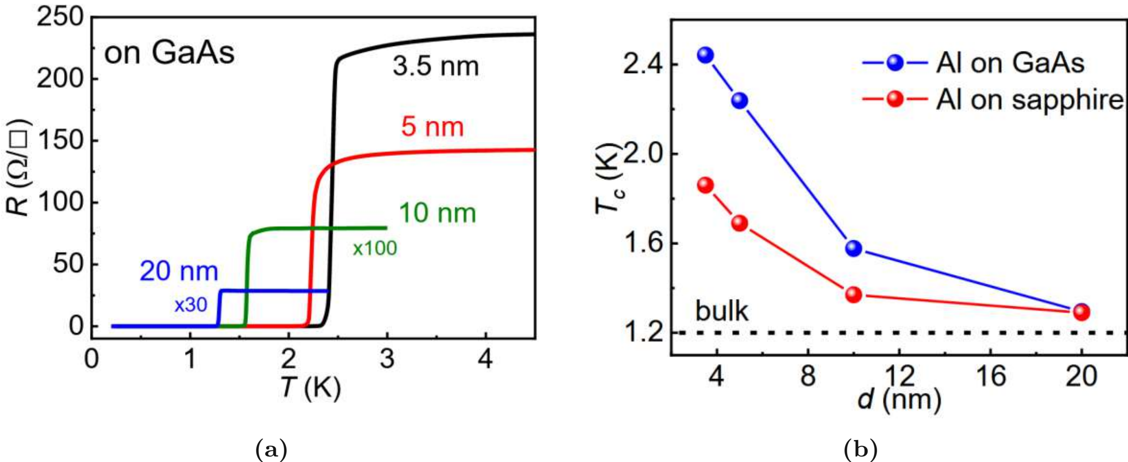
MBE on pretreated substrates, including GaAs(001) and sapphire(0001), with thermal cleaning/oxide removal (and an undoped GaAs buffer layer growth) prior to Al deposition under ultrahigh vacuum.



(a) (b)

Figure 2.8: *(a) Resistivities of different Al layer thicknesses as a function of temperature. The quantity indicated on the y-axis, Ω/□, is referred to by the authors as the normal-state sheet resistance. (b) T_c of Al as a function of layer thickness for two substrates. Images adapted from [33].*

Comprehensive calculations include the renormalization of the chemical potential in thin films and show that the strength of the confining potential is of critical importance. Specifically, strong confinement leads to an enhancement of T_c, whereas weak confinement can suppress it, emphasizing the crucial role of the substrate (e.g., gallium arsenide (GaAs) vs. sapphire in Figure 2.8 (b)) on superconducting properties. A plausible contribution is the substrate phonon spectrum, where GaAs provides more low-frequency phonon modes than sapphire. Such low-energy phonons can couple efficiently to the electrons in the Al film and thereby strengthen the effective electron–phonon interaction, which in turn can increase T_c, consistent with the observed substrate trend [33].

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Chapter 3

Experimental methods

In this chapter, standard deposition techniques are introduced, followed by a novel TIER-based process flow for producing self-passivated Al layers from SOI substrates down to $\sim 1\,\mathrm{nm}$. Subsequently, the metrology and electrical measurement setups employed to verify geometry and quantify key properties (e.g., resistivity, ampacity, and $1/f$ noise) are described.

3.1 Standard fabrication methods for thin layers

Thin layers of Al and Al-based compounds are typically produced by sputtering or thermal evaporation [1, 43, 83]. In thermal evaporation, Al is heated in high vacuum until it evaporates into the gas phase and condenses on a substrate to form a thin film. This process allows control of the film thickness from a few to several hundreds of nanometers. A thickness monitor is used to measure and control the deposition rate, ensuring uniformity and accuracy [43]. In sputtering, energetic plasma ions bombard a solid Al target and eject atoms, which then condense on the substrate. Compared to thermal evaporation, sputtering typically operates at higher working pressures and can yield dense films with good adhesion [1, 83]. The deposition processes employed in this thesis are schematically illustrated in Figure 3.1 for magnetron sputtering and in Figure 3.2 for PECVD. According to [85], the two deposition processes used in this work are summarized below.

3.1.1 Magnetron sputtering

Magnetron sputtering uses a conventional DC magnetron to generate a metal-atom flux, while a plasma between target and substrate ionizes these atoms via electron–metal-atom collisions. This plasma, typically sustained in argon by inductive RF coupling at 13.56 MHz, operates at higher pressures ($> 10\,\mathrm{mTorr}$) than conventional physical vapor deposition and acts as a collimator toward the substrate. The high plasma density ($\sim 1 \times 10^{11}\,\mathrm{cm}^{-3}$)

enables efficient ionization, because the ionization energy of argon (15.7 eV) exceeds that of most metal atoms (< 10 eV). In this work, 5N (99.999 %) Al and Si sputter targets (HMW Hauner GmbH & Co. KG) are used.

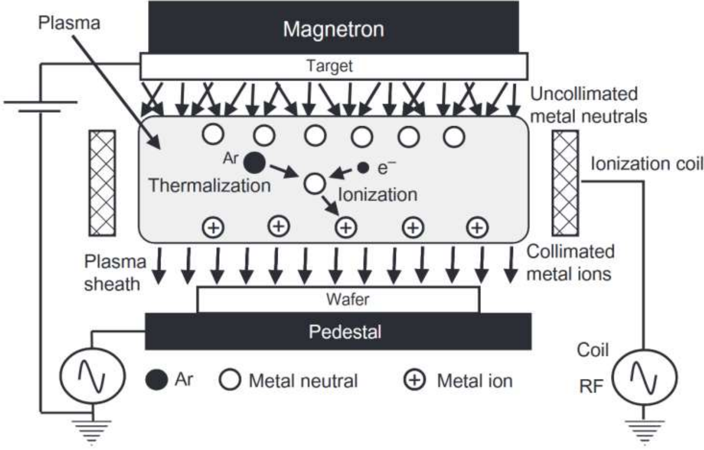

Figure 3.1: *Illustration of magnetron sputtering. Image adapted from [85].*

3.1.2 Plasma-enhanced chemical vapor deposition

For PECVD, film-forming precursor gases are introduced into the reaction chamber via mass-flow-controlled gas lines. Depending on reactor configuration, these gases are dissociated and activated either in a direct plasma above the substrate or in a remote plasma. The reactive species then diffuse to the heated substrate surface, where they undergo chemical reactions that form the solid film. Key deposition parameters include temperature, pressure, plasma power, gas flow rates, and gas composition. Substrate temperature is controlled by a heater to optimize film growth, and by-products are continuously removed by the vacuum pump.

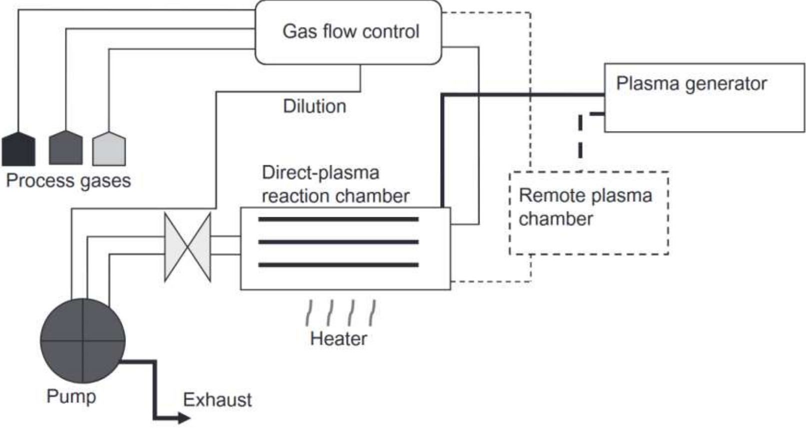

Figure 3.2: *Illustration of plasma-enhanced chemical vapor deposition. Image adapted from [85].*

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3.2 Fabrication routes for thin and ultrathin Al layers based on TIER

This thesis employs a novel fabrication route based on the TIER process, in which Si is replaced by Al at elevated temperatures. The main processing steps are illustrated in Figure 3.3. Starting from an SOI wafer (1), the Si structures are patterned by lithography and RIE (2), and the DL thickness is subsequently adjusted by thermal oxidation (3). During oxidation, a protective SiO_2 layer forms, which is partially removed by wet etching in HF to enable intimate contact with subsequent sputter-deposited Al pads (4). After the excess sputtered Al and the resist have been removed by lift-off in in acetone, assisted by ultrasonication (5), Si is replaced by Al at elevated temperatures in a forming-gas atmosphere, yielding a thin Al film encapsulated by optically transparent SiO_2 (6). This processing approach provides the advantage of a protective SiO_2 capping layer that suppresses oxidation of the Al. Comprehensive descriptions of the fabrication workflow and process parameters are provided in Appendix A, which details the individual processing steps and discusses the identification and mitigation of processing-related artefacts.

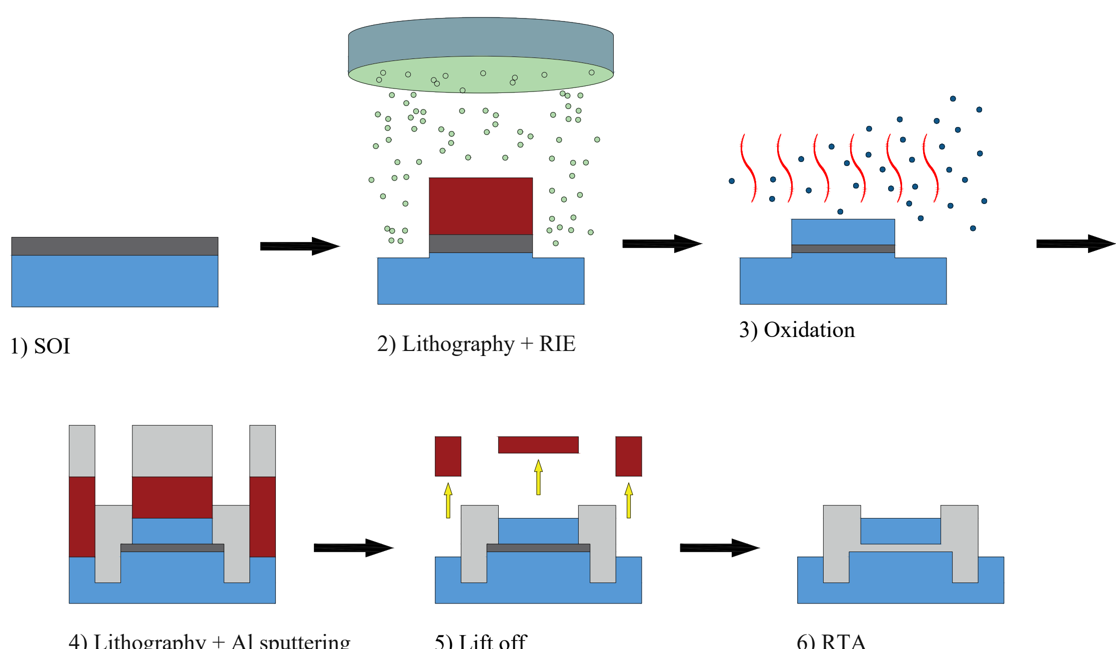

Figure 3.3: *Process flow for fabricating thin Al layers via TIER (handle wafer omitted for clarity): (1) SOI substrate, (2) lithography/RIE patterning, (3) Si thinning by thermal oxidation (SiO_2 cap), (4) contact opening + Al sputter deposition, (5) lift-off, (6) RTA-driven Si–Al exchange (TIER).*

After a sample of roughly 1 cm × 1 cm is cleaved from the corresponding SOI wafer, various structures, including the three structures listed in Table 3.1, are fabricated on the resulting SOI sample in a cleanroom environment by following a step-by-step process flow. The geometry of the particular test structures is systematically varied in terms of length, width,

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and thickness to generate a comprehensive dataset for analysis. However, the employed laser-writer–resist system imposes a limitation on the minimum feature size, which sets the minimum spacing required for processes such as lift-off process to function properly and is on the order of one micrometer. Independently of this, the TIER process imposes a second limitation: the maximum length of the Si structures is restricted to a few tens of micrometers. Within this chapter, a distinction is made between the fabrication of thin and ultrathin structures, as the formation of Al UTFs (< 1.4 nm) requires additional processing steps. The following chapters examine these steps in detail and introduce the relevant parameters that influence the fabrication quality. The process steps include:

- Lithography [83]: application of a patterned resist layer on the wafer to prepare for further process steps, particularly etching and the Al/Si-layer deposition
- RIE [158]: SF_6-based etching of Si
- HF [159]: hydrofluoric acid, used as a buffered oxide etch (BOE; HF : NH_4F = 1 : 7) for etching SiO_2
- PECVD [88]: deposition of a protective SiO_2 layer on the Si structures
- Oxidation [74]: reduction of the Si layer thickness in an oxygen ambient at temperatures of 1173 K to 1273 K
- Sputtering [85]: deposition of Al and/or Si onto the sample
- RTA [64]: replacement of Si by Al through briefly heating the sample

The various processing methods are summarized in the flowchart in Figure 3.4. It distinguishes three fabrication routes, a standard approach, a *subtractive* one (approach 1, shaded red) and an *additive* approach (approach 2, shaded green), which share several common steps. To ensure clear reference throughout the thesis, the individual process steps are labeled consistently as (1, 2, ..., A, B, ..., 6). Although these process steps follow a sequential order, they are independent in time, allowing processing to be paused after any given step. This numbering, including (A, B), is consistently used in the following sections to maintain direct correspondence with the flowchart. In addition, the flowchart groups related steps into higher-level process blocks. In the subtractive approach, two additional process blocks are required, namely *PECVD* and *lithography (oxidation layer, OL) + HF etching*. In contrast, the additive approach requires only a single additional process block, *lithography (silicon layer, SL) + Si sputter deposition*.

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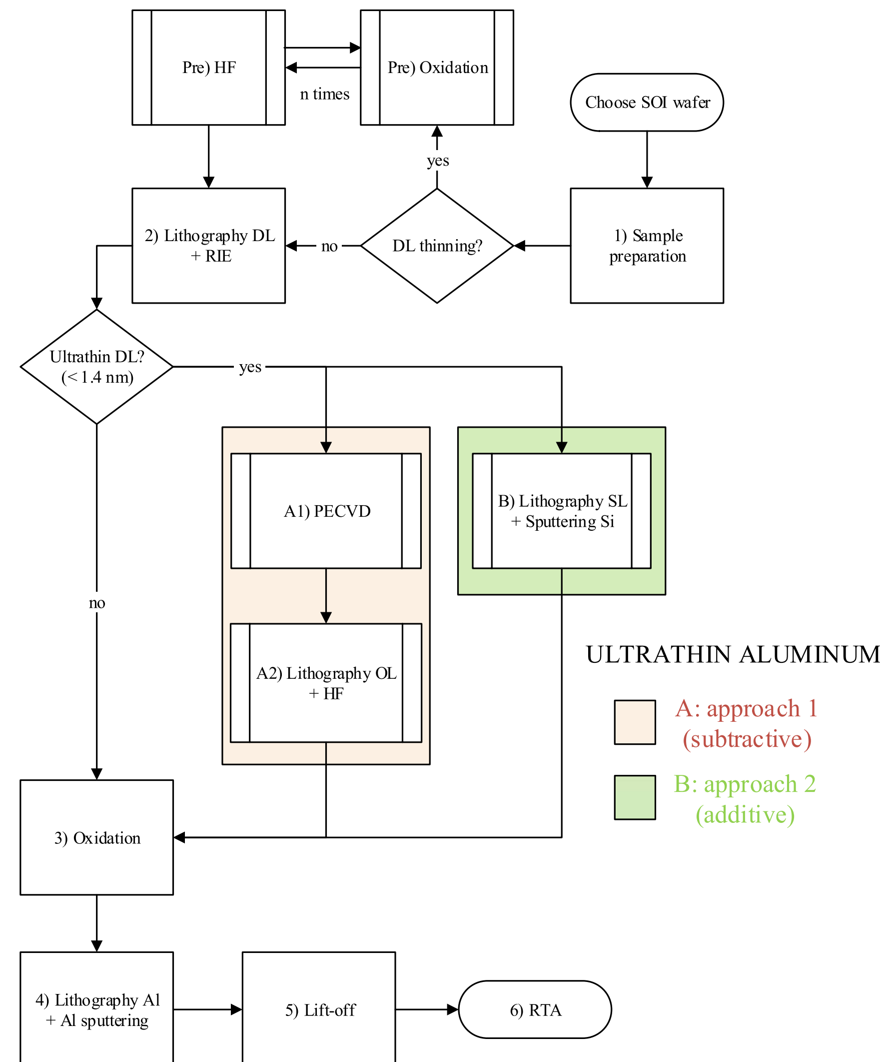

Figure 3.4: *Flowchart illustrating the fabrication of thin and ultrathin Al layers from SOI wafers.*

Following the unshaded path in Figure 3.4, thin Al layers down to, and including, 1.4 nm can be directly obtained using the 189 nm SOI wafer as the base material, although the process yield becomes very low in this regime. For layer thicknesses below 3 nm, contacting the Si structures with sputtered Al is challenging due to the natural oxidation of Si during the processing steps and the HF etch employed to open the contact windows for the Al pads. Therefore, alternative approaches are required. The color-coded paths represent the two selected approaches, which are treated as mutually exclusive processing routes in this thesis. In this ultrathin thickness regime, a 20 nm SOI wafer is used as the starting material in order to reduce the oxidation time that would be required for a 189 nm Si layer and because the 20 nm wafer provides exceptional surface quality.

To produce and electrically characterize Al UTFs, of about 3 nm and below, from an SOI wafer with a DL thickness of 20 nm, the novel combination of individual process steps is used. For electrical characterization, suitable structures must be designed to minimize measurement errors in the actual thin Al layers and to enable standardized comparisons between different Al layer thicknesses and geometries. Among others, the following three test structures are implemented in AutoCAD as part of the preparation for the fabrication process and are shown in Table 3.1 as final structures in optical micrographs.

Table 3.1: *Comparison of different test structures for electrical characterization of UTF Al*

Structure	Top-view micrograph	Characteristics
Dumbbell	10 µm 0	Measurement of electrical resistance, noise, and ampacity
Hall bar	16 µm 0	Four-point resistance measurements and possible monitoring of resistance changes in magnetic fields
Van der Pauw	14 µm 0	Measurement of electrical resistance in external magnetic fields

3.3 Fabrication of thin Al structures

In this section, a novel process based on a thermally induced Al–Si exchange reaction via RTA is presented, which enables the fabrication of thin and self-passivated Al layers, starting from an SOI wafer. The process steps described here form the basis of the subtractive (approach 1) and additive (approach 2) routes used to fabricate Al UTFs with thicknesses below 3 nm in a high-yield process, which are further extended and discussed in section 3.4.

3.3.1 Sample preparation

An SOI substrate with a ⟨100⟩-oriented single-crystal DL on top of a SiO_2 insulator layer and a doped Si handle wafer is used as the base material. The Si DL and BOX layer thicknesses are 189 nm and 382 nm, respectively. Further specifications are listed in Table 3.2.

For ease of reading, only the Si DL and the BOX layer are depicted, while the naturally grown oxide layer and the several-hundred-micrometer-thick Si handle wafer are omitted, as illustrated in Figure 3.5.

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Table 3.2: *Technical data of the SOI wafer with DL thickness of* 189 nm

Manufacturer	IBIS Technology Corporation
Address	32A Cherry Hill Dr, Danvers, MA 01923
Phone / Fax	(978) 777-4247 / (978) 777-6570
Date	October 4, 1999
IBIS Part Number	2PT119-H-068
Purchase Order (PO#)	MO1-4500136321
Sales Order (SO#)	266
Quantity	9
Type	P
Si Thickness (nm)	189
Si Uniformity (Å)	56
SiO_2 Thickness (nm)	382

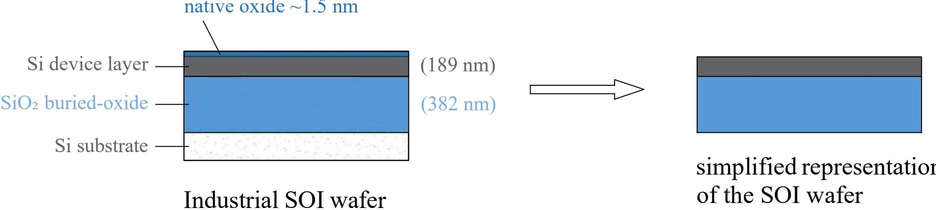

Figure 3.5: *Simplified representation of the SOI wafer used in the subsequent processing steps.*

Prior to processing, a suitable piece of about 1 cm × 1 cm is cleaved from the SOI wafer using a diamond scriber and carefully cleaned by ultrasonication in acetone (Sonorex Digital 10 P, Bandelin) for several tens of seconds at 20 % power, followed by rinsing in isopropanol. This procedure corresponds to step 1 of the flowchart presented in Figure 3.4.

3.3.2 Test pattern formation

Depending on the target DL thickness, the SOI wafer is subjected either to a single-step thermal oxidation for several hours or to a multi-step oxidation process with intermediate HF etching to remove the grown SiO_2, thereby limiting the cumulative oxidation time. Subsequently, laser lithography is employed to define Si test structures. After cleaning the wafer (step 2a in Figure 3.6) with acetone and isopropanol and, if required, ultrasonication for 1 min at 20 % power, a ∼1 µm-thick photoresist layer (AZ 5214-E) is deposited by spin coating (Polos spin coater) at 6000 min^{-1} for 35 s with an acceleration of 4000 min^{-1} (step 2b). The wafer is then soft-baked at 373 K for 60 s on a Präzitherm 2860EB hotplate. The desired patterns (see Appendix B) are exposed using a Heidelberg MLA150 laser-writer system (step 2c) with the following settings: dose 140 mJ cm^{-2}, defocus 0 and high-quality mode. After development in ∼30 mL of AZ 726 MIF (step 2d), the exposed resist regions are removed, whereas the unexposed regions remain. The resulting structures are inspected using an optical microscope (Nikon Eclipse Ni-L) equipped with an Optoteam G5 camera.

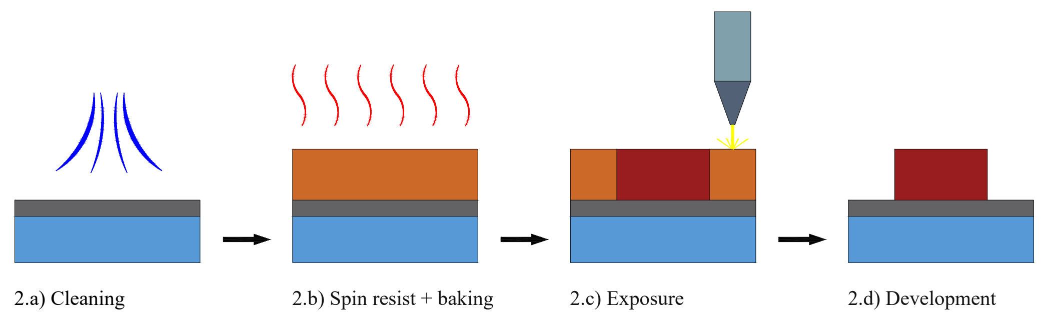

Figure 3.6: *Positive-resist lithography: (a) wafer cleaning, (b) resist coating and bake, (c) laser-writer exposure, (d) development to obtain the desired resist pattern.*

The test structures are defined in the Si DL of the SOI wafer by RIE. The photoresist mask protected the Si in the regions corresponding to the intended structures. During the RIE process, see Figure 3.7, Si removal proceeds via a combination of physical sputtering by energetic ions and chemical etching through reactions with the SF_6 plasma. A Si carrier wafer is used to mount the samples in the reaction chamber. The process parameters are: etch time 30 s to 150 s depending on the Si thickness, $p = 20\,\mathrm{mTorr}$, $T = 308\,\mathrm{K}$, $\Phi_{SF_6} = 50\,\mathrm{sccm}$, $\Phi_{O_2} = 4\,\mathrm{sccm}$, $P_{HF} = 15\,\mathrm{W}$, $V_{DC} \approx 60\,\mathrm{V}$, and He backside cooling flow $\Phi_{He} = 5.3\,\mathrm{sccm}$. The etching rates are approximately $0.3\,\mathrm{nm\,s^{-1}}$ for SiO_2 and $2.5\,\mathrm{nm\,s^{-1}}$ for Si, as determined from the measurements performed in this thesis.

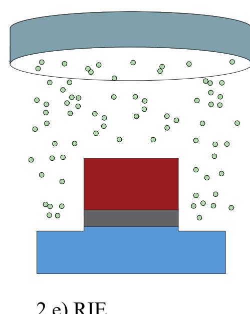

Figure 3.7: *RIE: removal of Si using an SF_6 plasma to define the desired Si structures in the DL.*

3.3.3 Thinning of the Si device layer

The DL of the SOI wafer is thinned in a controlled manner by thermal oxidation in an oxidation furnace (PEO 601) at around 1223 K under an oxygen atmosphere with $\Phi_{O_2} = 50\,\mathrm{sccm}$, with ramp-up and ramp-down carried out in a nitrogen atmosphere. This procedure corresponds to step 3 of the flowchart in Figure 3.4. Wet oxidation is also possible, in which water vapor is introduced into the heating chamber in addition to oxygen [68]. This shortens the oxidation time but increases the roughness of the interface with the grown SiO_2 [74, 160]. The oxidation reaction can be written as

$$\text{Dry oxidation:}\quad \mathrm{Si\,(s) + O_2\,(g) \rightarrow SiO_2\,(s)}. \tag{3.1}$$

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Dry oxidation leads to a smoothing of the Si DL surface [70, 161]. A comparison of the different surface roughness levels and oxidation thicknesses as a function of oxidation time can be found in section 4.1. During oxidation, the positioning of the samples in the oxidation furnace also plays a critical role, as the oxidation rate varies due to variations in oxygen concentration and temperature gradients. The oxidation step forms a self-passivating oxide layer on top of the DL. The thickness of the Si consumed is around 44 % of the total oxide thickness [74].

3.3.4 Al contact pad formation

In order to exchange the Si with Al and enable electrical measurements, the fabricated Si structures must be connected to Al pads. For this purpose, another lithographic mask is prepared, allowing access to the edges of the Si structures. The mask is applied using an image-reversal process [83, 162], which produces a pronounced undercut resist profile and thus enables a reliable subsequent lift-off process. The process flow is shown in Figure 3.8.

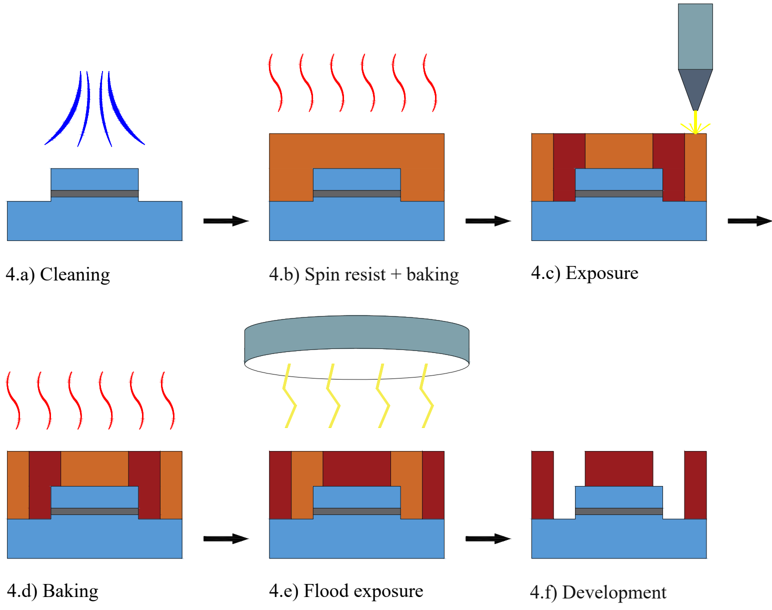

Figure 3.8: *Image-reversal lithography for lift-off: (a) cleaning, (b) spin-coat* 1 µm *resist + bake* (373 K, 60 s)*, (c) laser-writer exposure, (d) reversal bake* (393 K, 70 s)*, (e) UV flood exposure* (35 s)*, (f) final resist profile.*

After cleaning the sample, an approximately 1 µm-thick photoresist layer is deposited by spin coating (step 4b) and soft-baked at 373 K for 60 s. The desired patterns are then exposed using the laser-writer (step 4c). Compared to the laser-writer settings used previously, the exposure dose is reduced to 40 mJ cm^{-2}, while the defocus and high-quality mode are kept unchanged. Subsequently, an additional post-exposure bake at 393 K for 70 s (step 4d) and a flood exposure with UV light using a Karl Süss MJB3 mask aligner

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equipped with a 350 W Hg lamp for 35 s (step 4e) are performed. As discussed above, this sequence modifies the resist edge profile (required for lift-off processing). After development (step 4f), the correspondingly exposed resist regions are retained for subsequent processing. In the next step, the SiO_2 must be etched to achieve contact between the Al and the Si, as shown in Figure 3.9 (4.g). BOE (1:7) is used for this purpose [159, 163]; it removes the SiO_2 layer at an etch rate of approximately $70\,\mathrm{nm\,min^{-1}}$ [164], with a selectivity for SiO_2 over Si on the order of 1000:1 [165–168]. During this step, care must be taken not to etch away the underlying BOX layer completely, as this would lead to undesired contact between the Si handle wafer and the sputtered Al. Further, such over-etching causes the HF step to attack the thin and ultrathin Si pads directly, thereby preventing Si substitution by Al during TIER. The process flows developed for the additive and subtractive approaches overcome this limitation and, in addition, compensate for HF-induced etching damage – affecting mainly the thicker Si pads while preserving the UTFs – as well as for oxidation of the contact pads during air exposure before sputtering. Further details on artefacts caused by HF etching are presented in Appendix Table A.

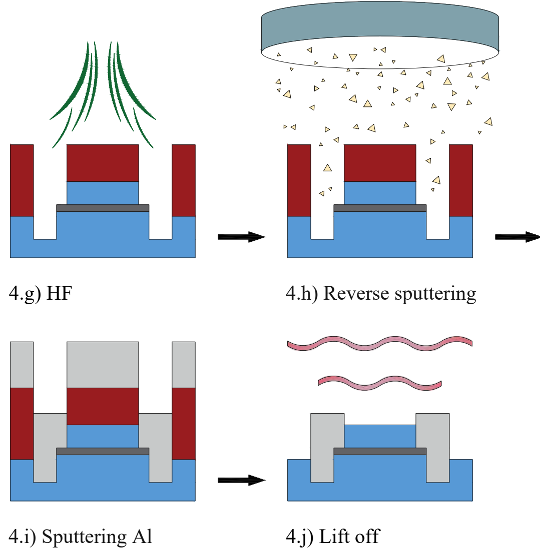

Figure 3.9: *Contact formation: (g) BOE etch of SiO_2 to open Si pads, (h) reverse sputter clean ($<1\,\mathrm{nm}$), (i) Al deposition ($\sim 200\,\mathrm{nm}$), (j) lift-off, yielding intimate Si/Al contact.*

After etching, a surface layer of less than 1 nm is removed from the Si contact areas by reverse sputtering (step 4.h) prior to Al deposition by sputtering in a Creavac system for 60 s at 50 W. An Al film with a thickness of approximately 200 nm is deposited by plasma-enhanced sputtering (step 4i). The deposition sequence consists of ten Al sputter cycles with 1 min cool-down periods between consecutive cycles. Prior to deposition, the Al target is cleaned by a pre-sputter step for 120 s at 100 W with the shutter closed. The process parameters are $P_{\mathrm{reverse}} = 50\,\mathrm{W}$, $t_{\mathrm{reverse}} = 60\,\mathrm{s}$, $P = 60\,\mathrm{W}$, and $t_{\mathrm{tot}} = 600\,\mathrm{s}$. After lift-off – ideally performed in acetone using low-intensity ultrasonication for 30 s to 120 s – the sample is ready for the final process step.

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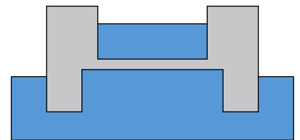
3.3.5 Thermally-induced exchange reaction

Thin Si regions defined by standard lithography and thermal oxidation are locally converted into Al by RTA via the TIER process with adjacent Al pads. The annealing is performed in a UniTemp UTP 1100 at ∼773 K in a forming-gas atmosphere with a flow of 450 l_n/h. During the heat treatment, Si diffuses into the Al pads, while Al atoms migrate into the Si, resulting in a local substitution of Si by Al. To establish well-defined initial conditions, the process chamber is evacuated three times to below 0.1 mbar prior to backfilling and annealing. After the complete exchange, the thin Al layer is protected by SiO_2 formed in the preceding oxidation step, which prevents oxidation of the Al, as illustrated in Figure 3.10. Annealing temperature and duration must be carefully tuned to avoid defects at elevated temperatures due to the melting temperature depression of Al UTFs [169]. The solubility of Si in Al is approximately 1 % at 773 K. The volume of the Al pads is at least 4500 μm^3, while the volume of the largest Si test structures is about 40 μm^3 (see Appendix B). This ensures that all Si can be dissolved in Al without exceeding its solubility limit. The annealing process can stop after a few tens of micrometers from the Si–Al interface, so that the maximum extension of the Al structures is limited. Depending on the Si thickness, the lateral dimensions of the structures, and the selected temperature, the complete replacement typically takes several minutes.



5) Final structure after TIER/RTA

Figure 3.10: *Schematic of a test structure, completely exchanged with Al (grey). The thin Al structure (middle part) is protected by SiO_2 (blue), and the Al pads are exposed for electrical characterization.*

3.4 Fabrication of ultrathin Al structures

This section introduces two fabrication routes for Al UTFs that enable the reliable realization of Al films below 3 nm: a subtractive approach and an additive approach. Both approaches are employed to produce Al UTFs using both an industrial SOI wafer (189 nm) and a high-quality SOI wafer with a DL thickness of 20 nm. The two processes differ in processing complexity, yield, and the interface quality of the resulting structures. The following subsections discuss the challenges of contacting and exchanging of ultrathin Si layers with Al and present the two approaches.

3.4.1 Contacting ultrathin Si with Al pads

The Si DL of the corresponding SOI wafer is thinned by oxidation in order to obtain Si UTFs, which can be replaced by Al. However, contacting the Al pads by sputtering becomes increasingly difficult as the Si layer becomes thinner than 3 nm. In this regime,

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the yield of connecting the Si structures on the SOI wafer to the Al pads becomes very low with the standard fabrication method; thus, additional processing steps are required to protect the contact region and enable reliable contacting for even thinner structures. One reason is that, due to the processing method, HF is used to remove SiO_2 from the Si contacts in order to connect them to the Al pads. This wet-etch step can compromise the ultrathin Si contact regions. Once the protective SiO_2 has been removed, the exposed Si forms a native oxide upon contact with ambient air. Because the oxide formation and the preceding HF-based etch are sensitive to local geometry and mass transport, the resulting material removal is not perfectly uniform across the wafer. Consequently, some features become locally thinner and are therefore more susceptible to further chemical attack during processing and to continued oxidation under ambient conditions.

To reliably fabricate ultrathin Al structures with thicknesses < 3 nm, a high-quality SOI wafer is employed, comprising a 20 nm $\langle 100 \rangle$-oriented single-crystal Si DL on a 100 nm BOX and a 500 µm thick, highly p-doped Si handle wafer.

3.4.2 Approach 1: subtractive pad protection

To protect the Si pads used for Al contacting, an additional subtractive process step is introduced after the RIE process. In this step, the contact-pad regions of the Si structures are coated with a SiO_2 layer deposited via PECVD (PlasmaPro 100 PECVD) such that they remain protected during the subsequent furnace oxidation. In practice, the whole Si structures are coated with SiO_2 immediately after RIE. The PECVD SiO_2 deposition is performed for 3 min at $p = 1000$ mTorr and $T = 573$ K with gas flow rates of $\Phi_{SiH_4} = 425$ sccm and $\Phi_{N_2O} = 710$ sccm, using a plasma power of $P_{CVD} = 20$ W to obtain a SiO_2 layer thickness of 200 nm. In the next step, laser lithography is used to define the central sections of the structures (corresponding to the ultrathin regions) by patterning a positive resist with the OL mask. Using the lithography sequence described in subsection 3.3.2, the resist is patterned such that the contact-pad regions remain covered while the central region is exposed. The exposed SiO_2 is then removed in HF for around 180 s (hence the designation *subtractive pad protection*). After etching and resist removal, the exposed Si re-oxidizes in ambient air, consuming an additional ~0.5 nm of Si, depending on how quickly the sample is further processed, see Figure 3.11 (a). During subsequent thermal oxidation, this central region becomes ultrathin, while the contact pads remain protected from oxidation by the remaining SiO_2, see (b).

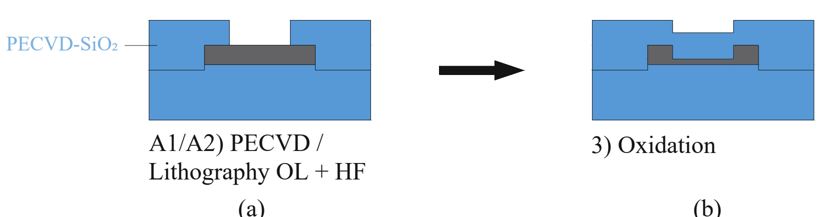

Figure 3.11: *(a) Device with protective SiO_2. (b) Thermal oxidation reduces the Si layer thickness.*

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This subtractive process modifies the surface roughness of the sample and, in addition, slightly reduces the DL thickness due to natural oxidation. Both effects degrade the quality of the DL and reduce the reproducibility of sample fabrication. The subsequent processing steps are the same as for the production of thin Al layers. For thinning the Si by oxidation (see subsection 3.3.3), the PECVD SiO_2 layer suppresses oxidation of the Si contact surfaces. In contrast, the central regions where the SiO_2 has been removed oxidize more rapidly, yielding the desired ultrathin Si section. The protective PECVD SiO_2 layer therefore fulfills its purpose of shielding the contact pads. For contacting the Al pads (see subsection 3.3.4), only the HF etching time is increased, as the SiO_2 layer deposited by PECVD has a thickness of 200 nm and must be removed to enable contact to the sputtered Al pads. It should be noted that the adjacent regions of the structures are also slightly affected by the extended etching process. After annealing (see subsection 3.3.5), an Al UTF is obtained.

3.4.3 Approach 2: additive pad protection

The second approach provides protection for the Si contact regions by means of a sputtered Si layer. A Si layer with a thickness of ~ 6 nm is deposited on the sample – except in the regions that later form the ultrathin areas – as illustrated in Figure 3.12 (a). The sputter parameters are $P = 100$ W, $t_{\text{tot}} = 60$ s, and $V_{\text{bias}} = 393$ V. During oxidation, the sputtered Si acts as a sacrificial layer, causing the Si contact areas on which it is deposited to oxidize more slowly than the untreated central regions of the structures. Upon oxidation, the additional Si layer is converted into SiO_2 and thereby also protects the BOX layer, as illustrated in Figure 3.12 (b). This is advantageous during the subsequent HF etching step used to open the Al contact areas, as slight over-etching does not risk exposing the Si substrate of the SOI wafer. This processing sequence therefore gives rise to the designation *additive pad protection*. Overall, the approach achieves a high process yield, and the ultrathin regions of the structures exhibit excellent structural quality.

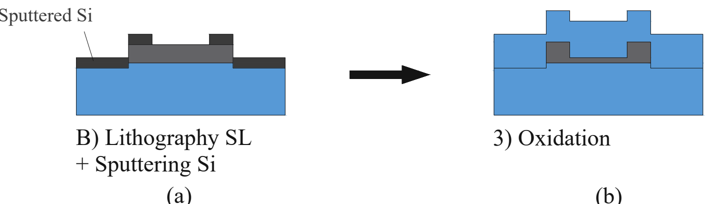

Figure 3.12: *(a) Device with protective Si. (b) Thermal oxidation reduces the Si layer thickness.*

The subsequent processing steps are identical to those used for the fabrication of thin Al layers. During the thinning of the Si (see subsection 3.3.3), the oxidation rates of amorphous and crystalline Si differ [69], which must be taken into account to ensure that the entire sputtered Si layer is removed by oxidation. The sputtered Si layer provides additional protection during oxidation by increasing the amount of Si that must be consumed before oxidation reaches the crystalline Si pads. This effect preserves the crystalline Si contact regions and enables a high yield of reliably contacted Al structures. Through contacting the Al pads (see subsection 3.3.4) and subsequent annealing (see subsection 3.3.5), an Al

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UTF is obtained. The interface and the overall structure exhibit superior quality because the central region remains structurally unaltered.

3.5 Verification of the structures

The geometry of the processed structures is examined using various methods, such as atomic force microscopy (AFM), scanning electron microscopy, and optical microscopy. Furthermore, the thicknesses of the processed Si, SiO_2 and Al layers can be verified using, e.g., ellipsometry or focused ion beam (FIB) cross sectioning followed by TEM imaging. The knowledge gained can lead to optimized processing (e.g., oxidation parameters, etching times). In addition, the Si and SiO_2 thickness measurements obtained by ellipsometry are used to tune the parameters of theoretical models for oxide thickness calculation [75]. Below, the experimental setups for ellipsometry, AFM and TEM/STEM are described.

3.5.1 Ellipsometry

Ellipsometry is the method of choice for measuring optical properties, like the refractive index n and the extinction coefficient k, or layer thicknesses [170]. Measurements can be completed within a few seconds with high accuracy, although the thickness of ultrathin SiO_2 layers can be overestimated due to errors in the refractive index of ultrathin oxides and the effect of interface roughness [171]. As illustrated in Figure 3.13, a light beam with wavelength λ and defined p- and s-polarization (relative to the plane of incidence) impinges on the sample at an angle Θ. The incident electric field is denoted by $E_{f,i}$, and the beam is reflected from the sample. Due to the material properties, the polarization of the incident light is altered.

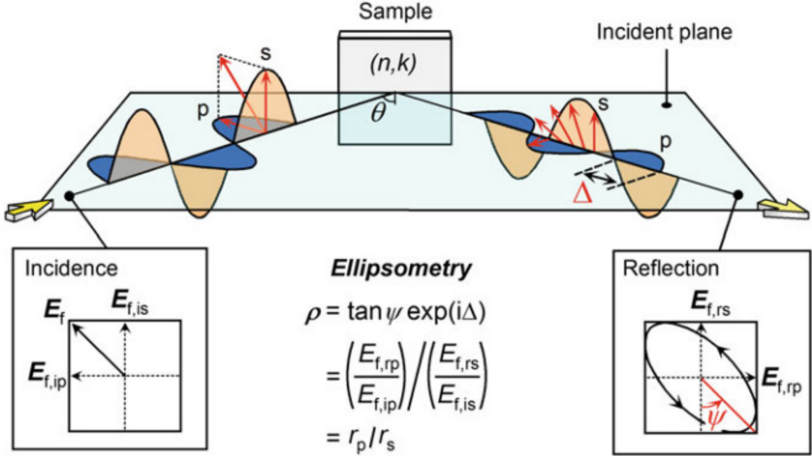

Figure 3.13: *Principle of an ellipsometric measurement. The amplitude ratio Ψ and the phase difference Δ are obtained from the incident light. For multilayer samples, the additional reflections at the interfaces are taken into account accordingly. Image adapted from [172].*

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The amplitudes of the p- and s-polarized waves, as well as their relative phase, are determined by the optical constants (n, k) and the film thickness. As a consequence, the maxima and minima of the reflected p- and s-polarizations no longer coincide, and the resulting vector of the reflected light ($E_f = E_{f,rp} + E_{f,rs}$) undergoes a rotation during propagation. In ellipsometry, the two parameters Ψ and Δ are measured, representing the amplitude ratio Ψ and the phase difference Δ between the p- and s-polarizations. Ellipsometry measurements are performed with a J.A. Woollam *alpha-SE* spectroscopic ellipsometer (rotating-compensator) at an angle of incidence of 70° with an ~ 3 mm beam diameter. The instrument records the parameters $\Psi(\lambda)$ and $\Delta(\lambda)$ over 380 nm to 900 nm (180 wavelengths). Film thicknesses are determined in CompleteEASE by fitting the measured spectra with a multilayer optical model. A full spectrum is acquired in less than 30 s. For a SiO_2 (25 nm)/Si reference at 70° with 10 s averaging, the specified thickness repeatability is $\delta d \approx 0.01$ nm (1σ); the absolute thickness accuracy is limited by the suitability of the optical model and correlations between fit parameters [173]. Figure 3.14 summarizes the evaluation workflow. The analysis starts with constructing an optical stack that reflects the expected layer sequence (e.g., SiO_2/Si/SiO_2/Si) and modeling of the dielectric function.

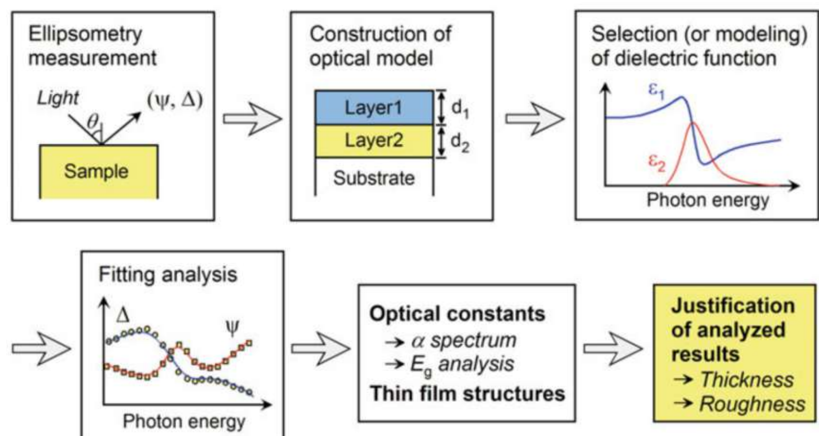

Figure 3.14: *Schematic of the ellipsometric measurement procedure for thin-film thickness determination. The parameters Ψ and Δ are obtained and the layer thickness is calculated from an appropriate optical model. Image adapted from [172].*

The model parameters are optimized by fitting $\Psi(\lambda)$ and $\Delta(\lambda)$, yielding thicknesses (and, if required, optical constants). Reliable results require a physically consistent model and a laterally homogeneous measurement area comparable to the beam diameter (i.e., on the order of a few millimeters). Layer thicknesses are determined by fitting the experimental data to a model, where the best fit corresponds to the lowest Mean Squared Error (MSE). According to [174], an MSE value near 1 represents a fit limited only by experimental noise. For ultrathin films where material properties may deviate from bulk references, MSE values in the range of 10 to 20 are commonly documented as acceptable fits [172, 175]. The resulting MSE of ~ 15 in Figure 3.15 therefore indicates an acceptable fit for the

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investigated test-wafer. This value is primarily attributed to deviations in the optical constants of the ultrathin Si layer compared to bulk reference data, as material properties in the nanometer regime often differ from their macrocrystalline counterparts due to structural variations [174]. The stack was modeled from top to bottom as SiO_2 (Thickness 3) / Si (Thickness 2) / SiO_2 (Thickness 1).

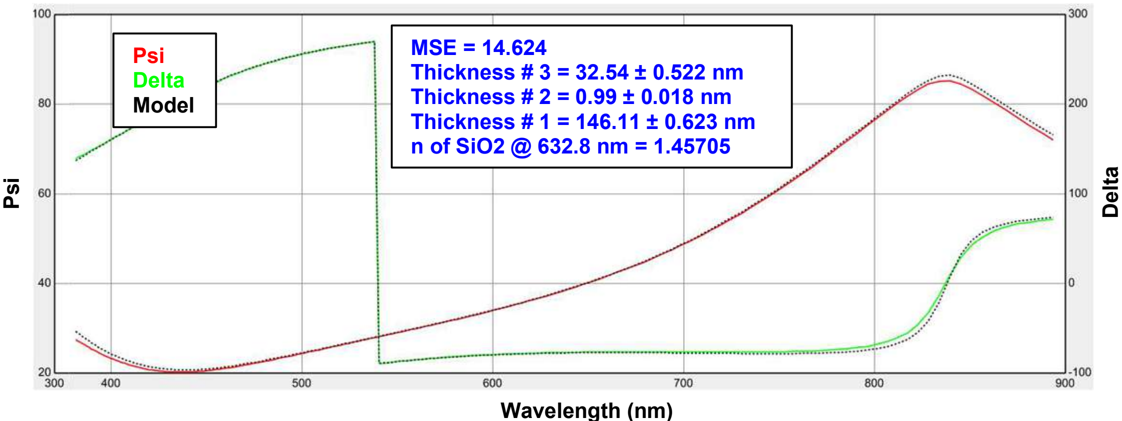

Figure 3.15: *Representative CompleteEASE fit of a Si UTF on a dedicated wafer after oxidation: the 1 nm Si layer remains clearly resolved, with close overlap between measurement (lines) and model (dots).*

3.5.2 Atomic force microscopy

The AFM technique is well suited for visualizing surface topographies over lateral areas of several μm^2 with nanometer-scale vertical resolution [176]. Typical AFMs offer three common imaging modes: contact mode, non-contact mode, and tapping mode [177]. For the purposes of this thesis, all measurements are performed in tapping mode. Analysis of the processed structures allows optimization of the process quality and investigation of the influence of different process steps on the structures. As described in the Veeco application note [177] and illustrated in Figure 3.16, in tapping mode a sharp tip mounted at the end of a cantilever is scanned across the sample surface while the cantilever is driven into oscillation. The cantilever is excited slightly below its resonance frequency with a typical oscillation amplitude in the range of 20 nm to 100 nm. During scanning, the tip intermittently interacts with the surface, making brief contact at the lowest point of each oscillation cycle. A feedback system ensures stable imaging by maintaining a constant root-mean-square value of the oscillation signal, which is monitored by a split photodiode detector. At each lateral coordinate (x, y), the vertical displacement of the scanner required to sustain the predefined setpoint amplitude is recorded, thereby generating a topographical representation of the surface.

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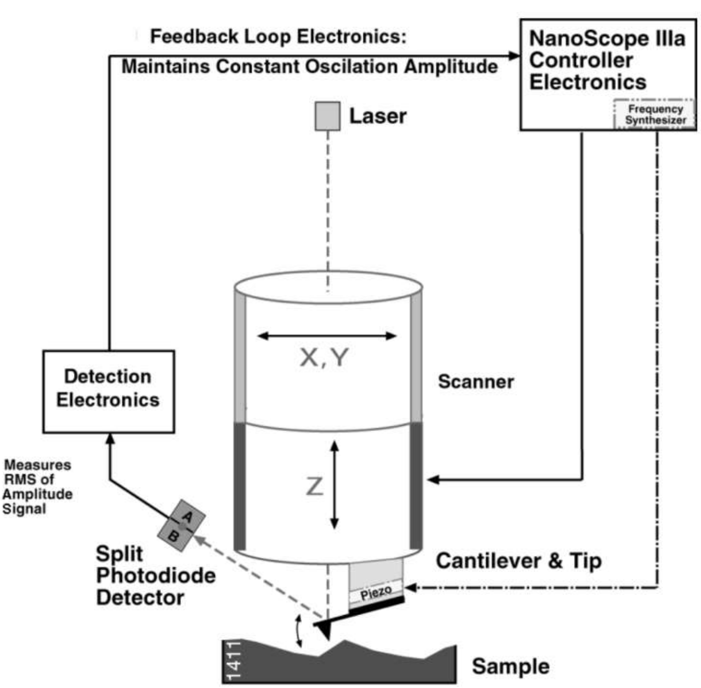

Figure 3.16: *Operating principle of tapping-mode AFM. Image adapted from [177].*

This imaging mode can be employed under ambient conditions. To protect the measurement from environmental influences, the entire experimental setup is placed on a vibration-isolated table and enclosed within a protective cover. For the AFM measurements, the experiment is prepared by initializing the software workspace and mounting the sample securely on the stage. The cantilever tip is positioned above the sample, brought into focus, and aligned with the laser to optimize signal strength. The cantilever is then tuned automatically, after which the measurement area is selected and the surface is brought into focus. A representative sharp Si tip used in AFM measurements is shown in Figure 3.17.

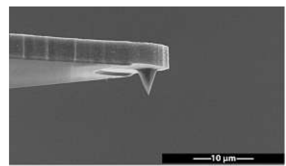

Figure 3.17: *A sharp Si tip used in AFMs. Image adapted from [178].*

The scan parameters (scan speed, resolution) are defined, and the real-time image acquisition is initiated to capture the topography of the sample. AFM measurements are performed with a Veeco/Bruker Dimension V system equipped with a NanoScope V controller. Scan sizes between 5 µm and 15 nm are used with a resolution of 512 samples per line and 512 lines. The scan speed is adjusted between 5.88 $\mu m\, s^{-1}$ and 15 $\mu m\, s^{-1}$. Prior to AFM imaging, all samples are cleaned via ultrasonication. The cantilever is driven close to

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its resonance at a drive frequency of approximately 315 kHz, using a drive amplitude in the range of 20–40 mV. Measuring artefacts and systematic errors such as sample tilt or curvature across large surface areas are corrected using the open-source data analysis software Gwyddion.

3.5.3 TEM/STEM overview and FIB lamella preparation

TEM is a core technique for imaging microstructure and interfaces in thin-film stacks by transmitting a high-energy electron beam through an electron-transparent specimen [82, 179, 180]. Depending on the selected imaging or diffraction condition, contrast can originate from mass–thickness effects, diffraction from crystalline regions and defects, and (in high-resolution operation) phase contrast that can reveal lattice fringes [82, 179, 180]. For cross-sectional TEM, the sample must be thinned to a *lamella* (typically tens of nanometers thick) so that the layer sequence becomes electron-transparent in projection [82, 180]. Site-specific cross-sectional lamellae are typically prepared by FIB milling, often in a dual-beam FIB–SEM instrument [181, 182], as illustrated in Figure 3.18.

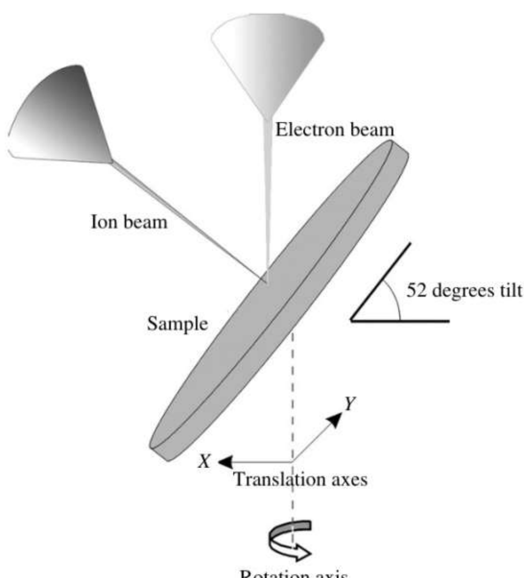

Figure 3.18: *Schematic of FIB milling in a dual-beam FIB–SEM system for lamella preparation. A focused Ga^+ beam sputters material to define a cross-sectional lamella, while the electron beam enables in situ imaging at a tilted stage geometry. Image adapted from [181].*

A region of interest (ROI) is selected, and a protective metal cap (commonly Pt or W) may be locally deposited before ion milling to reduce curtaining, redeposition, and near-surface damage during trenching and thinning [181, 182]. The integrated scanning electron microscope (SEM) is used to image the ROI and to provide geometric context of the structure prior to and during lamella preparation [181]. Typical FIB-related artefacts include ion implantation, amorphization, and redeposition; mitigation strategies include

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stepwise thinning at lower currents/energies and final low-kV cleaning/polishing where available [180–182]. In conventional TEM, the specimen is illuminated by a parallel electron beam and the image is formed simultaneously over the field of view by the post-specimen lens system [82, 179, 180]. Figure 3.19 illustrates two basic TEM imaging modes. In bright-field (BF) TEM, the image is formed primarily from the transmitted (direct) beam, whereas in dark-field (DF) TEM it is formed from a selected diffracted beam, which can enhance the visibility of specific crystalline regions or defect-related scattering [179, 180].

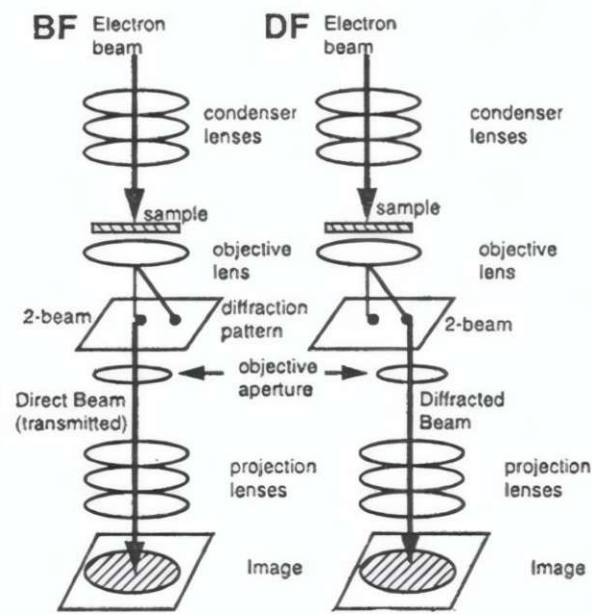

Figure 3.19: *Basic TEM imaging modes. In BF TEM, the image is formed primarily from the transmitted (direct) beam, whereas in DF TEM it is formed from a selected diffracted beam. Image adapted from [82].*

In scanning transmission electron microscopy (STEM), a focused electron probe is raster-scanned across the lamella and transmitted/scattered electrons are collected with dedicated detectors to form an image pixel-by-pixel [180, 182]. In BF-STEM, predominantly low-angle transmitted electrons are detected, yielding contrast that is sensitive to thickness and diffraction-related variations [180, 182]. In annular dark-field STEM, electrons scattered to larger angles are collected; in particular, high-angle annular dark-field (HAADF) STEM often provides robust Z-contrast together with sensitivity to local thickness variations [180, 182]. Chemical analysis is commonly combined with TEM/STEM via EDX, see Figure 3.20, which detects characteristic X-rays generated by electron irradiation [82, 180, 182]. In STEM-EDX, the signal can be recorded as elemental maps ("EDX maps") and as spectra from selected regions, enabling identification and spatial localization of elements such as Al, Si, and O [180, 182]. One-dimensional compositional line scans can be converted into *atomic-fraction profiles* (relative elemental fractions along a line), which are useful for describing compositional motifs such as core–shell-like distributions in cross sections [182].

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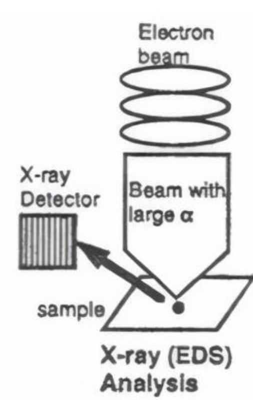

Figure 3.20: *Principle of EDX in (S)TEM. Characteristic X-rays generated under electron irradiation are detected for elemental identification. Image adapted from [82].*

3.6 Electrical measurement setups

Various measurement techniques are employed to investigate the electrical, optical and superconducting properties of the Al samples. The investigated parameters include ampacity, specific resistivity, power density, $1/f$ noise, temperature-dependent electrical resistance, superconducting transition temperature. The following section focuses on the two-point and four-point measurement methods used to determine the fundamental electrical properties. These needles can be precisely positioned onto the contacts of the Al pads using micrometer manipulators.

3.6.1 Basic electrical characterization

For basic electrical characterization, measurements are carried out on a needle probe station. The setup comprises an electrically shielded dark box and a sample stage equipped with multiple independently positionable probe needles, see Figure 3.21.

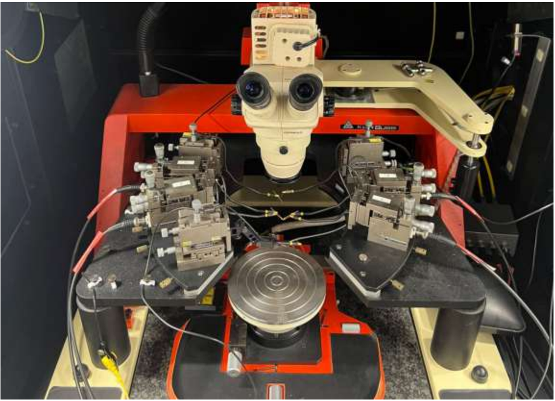

Figure 3.21: *Needle probe station used for electrical characterization of the Al samples, featuring eight micrometer manipulators for probe positioning (two or four used in this work), an inspection microscope, and a movable sample stage inside an electrically shielded dark box.*

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With tip diameters of only a few micrometers, the needles can be accurately aligned under a stationary microscope onto contact pads with lateral dimensions on the order of $100 \times 100\,\mu m^2$. The probe tips placed on the sample are connected via triaxial cables to the supply and measurement electronics, enabling high-resolution current and voltage measurements. The HP 4156B Precision Semiconductor Parameter Analyzer comprises four source-measure units (SMUs) and provides measurement resolutions down to 1 fA and 2 µV [183].

3.6.1.1 Current–voltage (I–V) measurement

The experimental setup follows the two-point configuration shown in Figure 3.22 (a). The measurement needles are positioned on the thick Al pads, and the SMU applies a controlled bias sweep while simultaneously measuring the current. In practice, a voltage V is sourced with a defined current compliance and the resulting current I is recorded. Conceptually, this can be represented equivalently by a current source driving the device and a voltmeter measuring the resulting voltage drop, as illustrated by the equivalent circuit in Figure 3.22 (b). In this circuit, R_{W} denotes the wire resistance, I and V denote the applied current and measured voltage, the resistors R_{C} correspond to the contact resistances, and R_{DUT} denotes the resistance of the device under test (DUT).

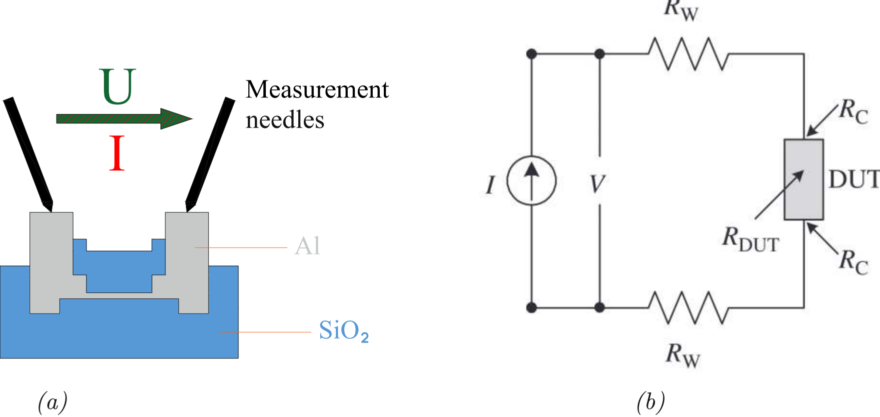

Figure 3.22: *(a) Side view of a two-point measurement on a dumbbell structure; (b) schematic of a two-point electrical measurement. Image adapted from [184].*

For the basic electrical characterization, an I–V curve is recorded, as illustrated in Figure 3.23, for DUT in a two-point configuration using a single forward DC sweep of the drain voltage from -10 to $+10$ mV in 0.1 mV steps. A hold time of approximately 1 s is applied at the start of the sweep to allow the device response to settle, followed by the acquisition of (~ 200) points over the range (± 10 mV) with a per-point delay on the order of (0.2 s) and a medium integration time (~ 20 ms at 50 Hz), resulting in a total measurement duration of about 45 s. A current compliance of ± 3 mA leads to the plateaus for $|V_D| \gtrsim 7$ mV. The current limit is set to the milliampere range to protect the structures from excessive electrical currents that could otherwise destroy the Al UTFs. The electrical

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resistance R is determined from the slope of the I–V characteristic curve according to Ohm's law, and the resistivity ρ is obtained taking into account the geometric dimensions of the sample:

$$R = \frac{\Delta V}{\Delta I}, \qquad \rho = R\,\frac{A}{l}\,, \tag{3.2}$$

where A is the cross-sectional area and l is the total length of the composite current path.

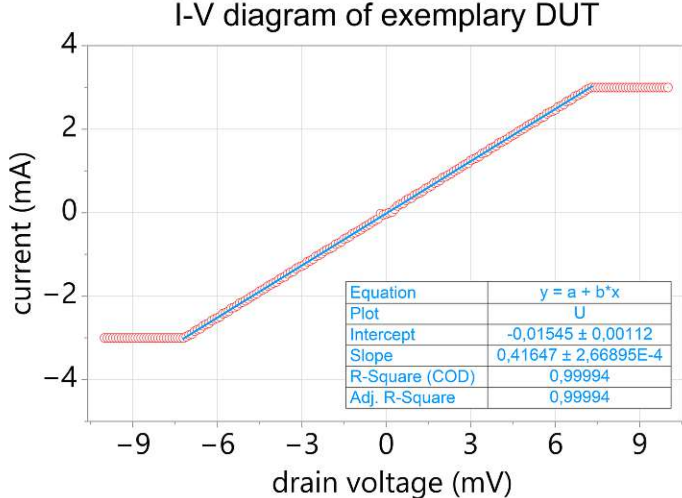

Figure 3.23: *I–V characteristic of DUT measured in a two-point configuration using a single DC sweep of the drain voltage from -10 to $+10\,\mathrm{mV}$ with autorange enabled; the current compliance of $\pm 3\,\mathrm{mA}$ produces the plateaus at $|V_D| \gtrsim 7\,\mathrm{mV}$.*

3.6.1.2 Four-point measurement

Hall-bar test structures are fabricated to enable four-point resistance measurements. In this configuration, two probes contact the current terminals to source and sink the drive current, while two additional high-input-impedance voltage-sensing probes measure the resulting potential drop across the structure, as shown in Figure 3.24 (a). All needles are placed on the thick sputtered Al pads. The current is applied through the outer contacts, and the voltage is recorded at the inner contacts. The equivalent circuit is shown in (b). This configuration is used for low-temperature electrical measurements. The four-point geometry is widely used for resistivity measurements because it largely suppresses the contribution of contact and lead resistances [185]. With the current driven through one pair of contacts and the voltage sensed independently via a separate, high-impedance pair, the measured potential drop predominantly reflects the intrinsic resistance of the sample [184], thereby improving measurement accuracy. It is therefore particularly advantageous when the intrinsic resistance of the device under test is comparable to, or even smaller than, the expected lead and contact resistances.

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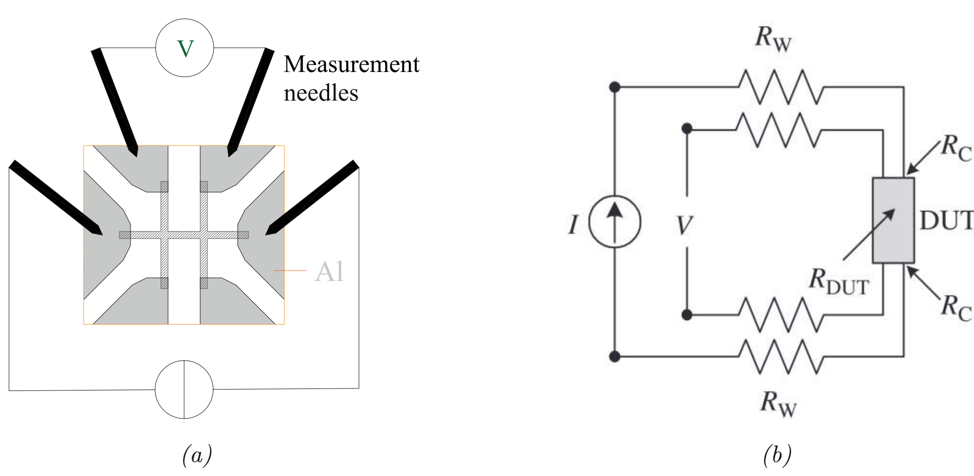

Figure 3.24: *(a) Top view of a Hall bar in a four-point measurement configuration; (b) schematic of a four-point electrical measurement. Image adapted from [184].*

3.6.2 Ampacity measurement

Before determining the ampacity of UTFs, the electrical resistivity ρ is obtained from an I–V measurement to detect possible changes induced by subsequent high current densities. The voltage is then increased stepwise from zero in increments of 1 mV and the current is monitored. To ensure a uniform temperature distribution across the entire device, each voltage level is kept for one second before the next step is applied. Upon reaching a predefined voltage value, the measurement is paused and the actual resistivity is determined again through an additional I–V measurement. After that, the voltage is increased in the next cycle. This is repeated until device breakdown. The ampacity is defined as the last current before breakdown for which the I–V characteristic remains unchanged. The measurement sequence is illustrated in Figure 3.25. For a rectangular cross section ($w \times t$), the area is $A = w\,t$ and the corresponding ampacity as a current density is

$$J_{\mathrm{CCC}} = \frac{I_{\mathrm{CCC}}}{A}. \tag{3.3}$$

The dissipated electrical power is $P = IV$. Averaged over the conductor volume $V_{\mathrm{cond}} = A\,L$, the volumetric power density is

$$p_{\mathrm{vol}} = \frac{P}{A\,L} = \frac{IV}{A\,L}. \tag{3.4}$$

With $J = I/A$ and $E = V/L$, this can be written as $p_{\mathrm{vol}} = J\,E$. For ohmic conduction ($E = \rho J$), one obtains

$$p_{\mathrm{vol}} = \rho J^2, \tag{3.5}$$

and thus at CCC

$$p_{\mathrm{vol,max}} = \rho\,J_{\mathrm{CCC}}^2. \tag{3.6}$$

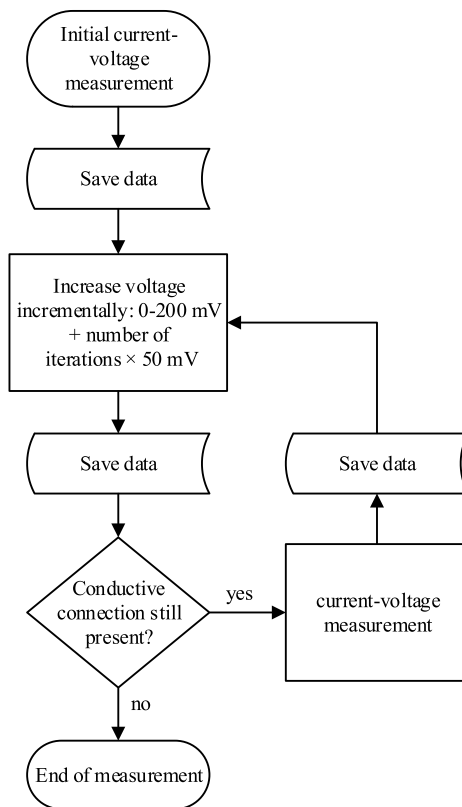

Figure 3.25: *Measurement procedure for determining the ampacity of the Al structures. The voltage is initially increased from* 0 mV *to* 200 mV *in steps of* 1 mV*.*

3.6.3 $1/f$ noise measurement

The processed samples are characterized with respect to their low-frequency $1/f$ noise behavior. The investigated devices comprise line structures with lengths L in the range of 1 µm to 10 µm, nominal widths W of 1 µm to 2 µm, and Al layer thicknesses t between 1 nm and 200 nm. The measurements are carried out using a Zürich Instruments MFLI lock-in amplifier in combination with a LakeShore Cryotronics probe-station measurement setup and a LEICA DM600 M materials microscope. The acquired data are analyzed using dedicated software that calculates the power spectral density as a function of frequency. Figure 3.26 shows the noise measurement apparatus used, featuring a closed sample chamber.

In Table 3.3, the relevant parameters of the measurement program are summarized. The parameter "Drain start value" defines the initial drain voltage at the beginning of the measurement, while "Step width of drain voltage" specifies the voltage increments between successive measurement points. The end of the measurement sequence is determined by the value "Drain stop value". The parameter "Measurement average" indicates the number of measurements per frequency range. The "Settle time" describes the waiting period

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before measuring the compliance current, allowing the system to stabilize and minimizing measurement artefacts.

The compliance current strongly affects the achievable resolution and represents a current-limiting safety setting of the measurement system. The selection of the measurement parameters is guided by two key aspects: preserving the integrity of the structures under investigation and optimizing the measurement resolution. The achieved resolution for the corresponding compliance currents is summarized in Table 3.4.

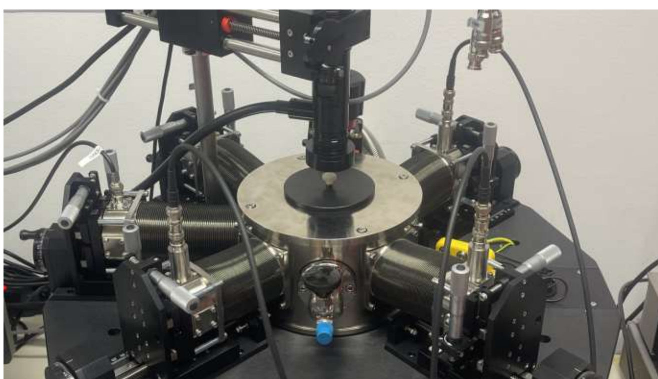

Figure 3.26: *Lake Shore noise-measurement setup, showing the silver cylindrical sample chamber surrounded by five probe tips, positioned via a vertically mounted optical microscope and micrometer manipulators.*

Table 3.3: *Measurement parameters for the drain voltage sweep*

Drain voltage sweep settings			
Parameter	**Value**	**Parameter**	**Value**
Drain start value	1 mV	Measurement average	16
Step width of drain voltage	1 mV	Settle time	30 s
Drain stop value	5 mV		

Table 3.4: *Compliance currents and corresponding measurement resolutions*

Compliance	**Resolution**
1 nA	40 pA
10 nA	40 pA
100 nA	4 nA
10 µA	60 nA
1 mA	2 µA
10 mA	5 µA (Offset: −5 µA)

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Chapter 4

Results and discussion

This chapter presents the outcomes of the different fabrication approaches and the structural and electrical characterization results obtained on the processed samples. This includes analyses by optical microscopy, AFM imaging, ellipsometry, and TEM, as well as electrical characterization using the methods described in chapter 3. Table 4.1 summarizes the different fabrication methods, including comments on the DL preparation and the type of process used to achieve the targeted DL thickness. The samples listed represent a subset of the complete sample set investigated in this thesis.

Table 4.1: *Subset of the processed samples providing fabrication details*

Sample	**DL** (nm)	**DL preparation**	**Processing**	**Comment**
MVII	131	Oxidation + HF	Standard	Wet oxidation
P6	110	Oxidation + HF	Standard	
S5	20	Original wafer	Standard	
S33	5	Oxidation	Additive	
S16	2.5	Oxidation + HF	Subtractive	Oxidation at 1273 K
S25	2	Oxidation + HF	Subtractive	
MA7	1	Oxidation	Additive	

Samples are prepared using different processing approaches in order to obtain the desired layer thickness. Different DL thicknesses are obtained from the respective SOI substrate wafers. The DL thickness is adjusted by (iterative) oxidation and HF treatment of the SOI. The comments in the table provide information on specific aspects of the processing procedure. In addition, different fabrication strategies are employed: (i) a *subtractive* pad protection approach (PECVD + oxidation; see subsection 3.4.2) and (ii) an *additive* pad protection approach (see subsection 3.4.3) for DL thicknesses of about 1 nm. The reported thickness refers to the Si layer, which after annealing corresponds to the thickness of the Al layer. For comparative measurements, reference samples are fabricated by sputtering Al

films with different thicknesses onto SOI substrates. Based on these samples, the following sections first examine how the individual processing steps affect the structural integrity and morphology of the Al layers and structures. Subsequently, the resulting electrical and superconducting properties of Al thin films and UTFs are discussed.

4.1 Processing effects on thickness, roughness, and morphology of Al films

This section presents the structural characterization, beginning with an analysis of the effects of oxidation and HF treatment on the DL thickness, followed by investigations of surface roughness, validation of the RTA process, and determination of the Al layer thickness by TEM. The structural quality of the patterned features is strongly influenced by multiple process parameters; the processing challenges are discussed in Appendix A.

4.1.1 Si DL thickness adjustment

Si DL thickness is adjusted by thermal oxidation at 1173 K to 1273 K. A linearized Massoud oxidation model [75] is used as a reference for the expected Si consumption during thermal oxidation; the corresponding settings are shown in Table 4.2. Ellipsometry measurements are employed to calibrate the oxidation process, which is a critical step for achieving the minimum DL thickness. For this purpose, different pieces of the SOI wafer are oxidized for varying durations, and the Si consumption as a function of oxidation time is recorded. The data obtained from oxidation test series on the SOI wafer with a DL thickness of 189 nm are shown in Figure 4.1.

Table 4.2: *Settings for the oxidation model [75] used for processing* ∼1 nm *samples. With these parameters, the predicted Si DL oxidation (Si consumption) rate is in good agreement with the experimentally determined rate in the furnace oxidation runs.*

Oxidation model settings			
Parameter	**Value**	**Parameter**	**Value**
Ambient	Dry	Initial oxide thickness	15 Å
Partial pressure	1013 hPa	Temperature	1203 K
Model	Massoud	Crystal orientation	(100)

The thickness of the DL of the 189 nm SOI wafer is measured before and after oxidation by ellipsometry. In the target range around an oxidation time of approximately 130 min, a reduction of the Si DL thickness at a rate of 0.11 nm min^{-1} is expected. In practice, however, deviations in the measured Si DL thickness occur between samples oxidized for the same duration in different oxidation runs. These variations are possibly caused by temperature gradients and variations in the oxygen flow within the oxidation chamber, as well as by thickness variations of the initial SOI wafer. The actual oxidation is performed at 1173 K. However, the oxidation model exhibits excellent agreement with the measured

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Si consumption at 1203 K. This corresponds to an oxidation time of about 130 min for the conversion of 20 nm of Si, which is in good agreement with the values reported in [83] in the temperature range around 1203 K for dry oxidation. This also indicates a slightly incorrect temperature reading. The linear fits in Figure 4.1 approximate both the measured and modeled trends.

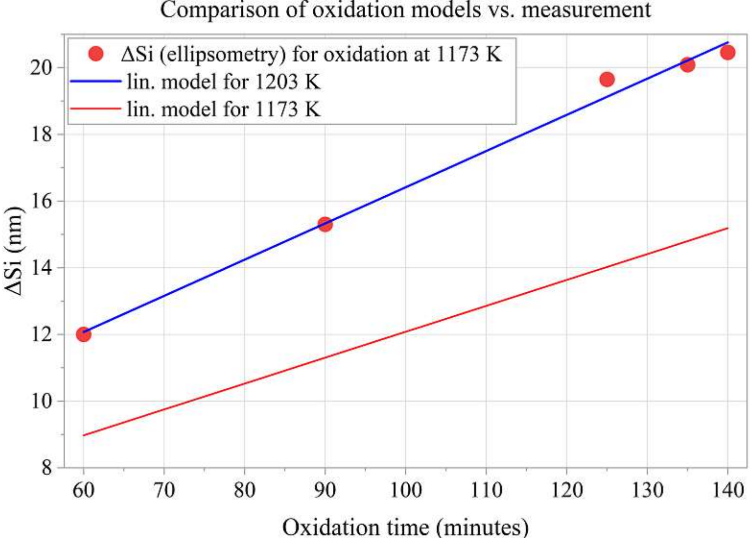

Figure 4.1: *Comparison of different linearized oxidation models with experimental data for the Si converted to silicon dioxide (ΔSi) during thermal oxidation.*

When oxidizing the 20 nm wafer, the measurable limit at which Si can still be detected is reached at ~135 min, as shown in Table 4.3. The table summarizes the ellipsometry results before and after 135 min of oxidation for a representative sample.

Table 4.3: *Ellipsometry results before and after oxidation for* 135 min *of a sample*

Parameter	Before oxidation	After oxidation
Upper SiO_2 layer (nm)	0.80 ± 0.144	48.20 ± 0.337
Si DL (nm)	21.17 ± 0.064	1.08 ± 0.031

4.1.2 Surface roughness of the Si device layer

Thickness adjustment by thermal oxidation and subsequent processing steps can significantly affect the surface roughness and, therefore, the structural integrity of thin and ultrathin regions. In particular HF treatment is known to modify the Si surface. Surface roughness is quantified by AFM using the root-mean-square roughness R_{rms} as a measure. The AFM measurements are performed on SOI wafers subjected to different treatments. The corresponding details are presented below.

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Wafer-to-wafer comparison: The two SOI wafers used in this work, with DL thicknesses of 189 nm and 20 nm, respectively, exhibit markedly different initial roughness levels. As listed in Table 4.4, the 189 nm wafer shows substantially higher roughness ($R_{\mathrm{rms}} = 680$ pm) than the 20 nm wafer ($R_{\mathrm{rms}} = 137$ pm). Thus, the 189 nm wafer provides a less favorable starting surface for fabricating ultrathin structures.

Table 4.4: *Surface-roughness parameter comparison of the two wafers used*

SOI wafer	R_{rms} (pm)
189 nm	680
20 nm	137

Effect of HF treatment on R_{rms}: A short HF dip applied to the 20 nm wafer leads to a further reduction of the measured roughness. According to Table 4.5, R_{rms} decreases from 137 pm to 107 pm after 5 s of HF treatment, corresponding to a reduction of ∼22 %. Within the measurement uncertainty, this indicates that a brief HF step can slightly improve the surface roughness of the SOI wafer with 20 nm DL under the conditions used here.

Table 4.5: *Surface roughness of the* 20 nm *wafer before and after HF treatment*

20 nm **SOI wafer**	R_{rms} (pm)
Original	137
HF treated for 5 s	107

Effect of oxidation on R_{rms}: Repeated thermal oxidation of the 189 nm wafer, performed to reduce the DL thickness down to 25 nm, also improves the surface roughness. As shown in Table 4.6, R_{rms} decreases from 680 pm to 459 pm, corresponding to a reduction of ∼33 %. This trend is consistent with the smoothing effect that can occur during oxidation of Si [70].

Table 4.6: *Surface-roughness parameters before and after oxidation of the* 189 nm *SOI wafer*

189 nm **SOI wafer**	R_{rms} (pm)
Original	680
Multiple oxid. down to 25 nm	459

Implications for the fabrication routes. Although oxidation and short HF exposure can reduce R_{rms}, the surface condition in the ultrathin regions is highly sensitive to the specific process sequence. This is illustrated by the AFM topographies in Figure 4.2. Samples fabricated using the subtractive approach (sample S25) (a), which includes HF

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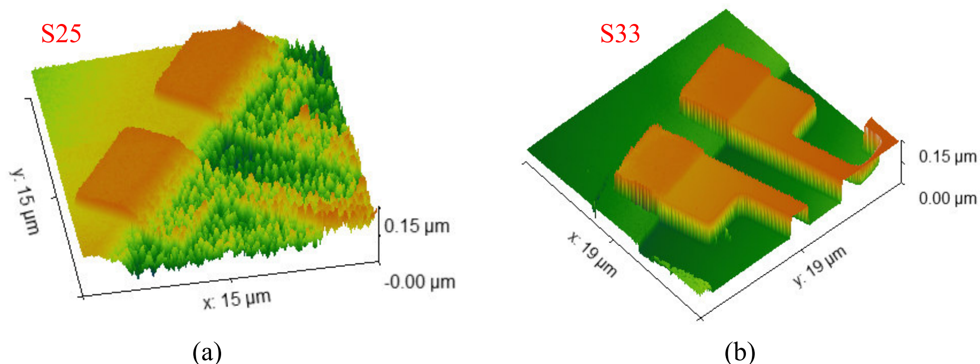

Figure 4.2: *3D AFM surface topographies of samples fabricated via subtractive (a, S25) and additive (b, S33) approaches: the subtractive process strongly roughens the interface in the designated area (area to the right), whereas the additive process yields a much smoother surface.*

etching prior to oxidation in the central region, show pronounced roughening of the ultrathin Si area. In contrast, the additive approach (sample S33) (b), where the pad region is protected and the central region is mainly modified during oxidation, yields an essentially smooth ultrathin surface. These observations indicate that the local exposure history (HF opening, subsequent oxidation, and handling in air) can dominate the final surface quality, even when global roughness trends appear improved.

4.1.3 RTA process verification

The exchange of Si with Al is monitored *ex situ* by optical microscopy. The annealing rates within the observed structures vary between samples with different DL thicknesses and range from 0.1 µm min^{-1} to 1 µm min^{-1}. For structures with DL thicknesses between 20 nm and 200 nm, the most favorable annealing behavior is obtained at ∼773 K. For thinner structures, lower temperatures of about 763 K are optimal to avoid structural damage due to the lowering of the melting point [169]. The visible progression of the annealing front in Figure 4.3, manifested by the boundary between Si and Al, provides information on the progress of the process. In (a), sample S5 is annealed for 2 min at 773 K, and the boundary between Al (gray) and the central Si part (bluish) is visible on both sides of the dumbbell structure. In (b), the fully exchanged sample after several annealing steps is shown.

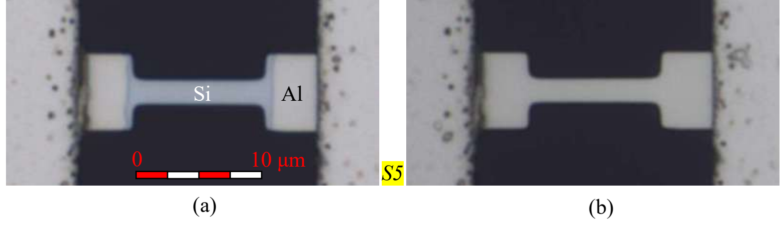

Figure 4.3: *Interface displacement process observed by optical microscopy in sample S5 with a DL of* 20 nm*. (a) Annealed for* 2 min *at* 773 K*. (b) Fully exchanged dumbbell structure.*

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4.1.4 Morphological characterization of Al layers using TEM

Cross-sectional TEM is performed on sample MA7 at ICREA in Barcelona to determine the local thickness and microstructure of the Al UTF for benchmarking the ellipsometer method used for Si thickness evaluation. The TEM lamella is prepared by FIB milling at the ROI indicated in Figure 4.4 (a), and a protective tungsten cap is applied prior to FIB cutting. The corresponding scanning electron microscopy (SEM) image in (b) provides the geometric context of the dumbbell structure and identifies the specific site selected for analysis. HAADF-STEM reveals a pronounced thickness gradient in the exchanged Al layer along the metal film, see Figure 4.5.

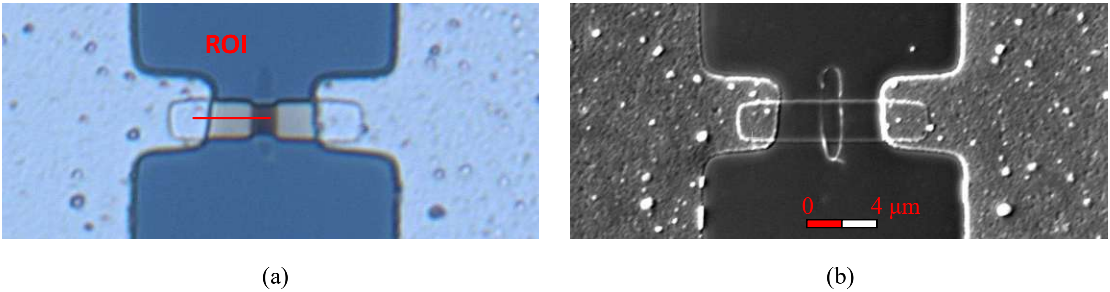

Figure 4.4: *(a) Optical and (b) SEM micrographs of the dumbbell structure in sample MA7. The ROI marks the FIB cross-section position for TEM lamella preparation.*

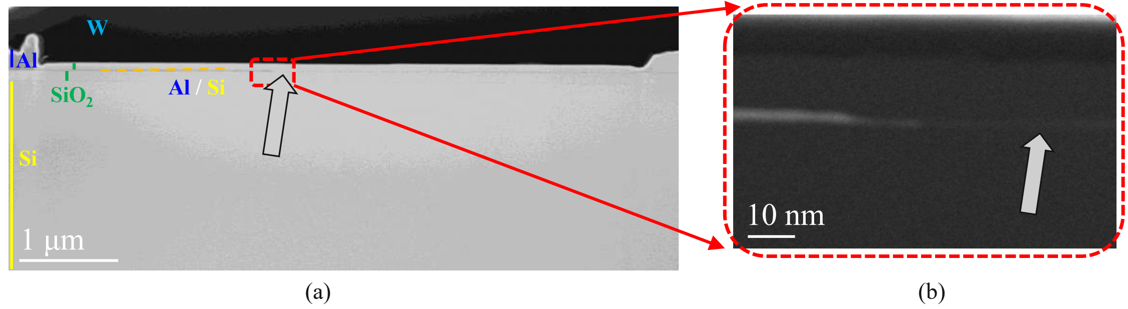

Figure 4.5: *Cross-sectional HAADF-STEM images of sample MA7. (a) Continuous Al layer with a thickness in the range of* 1 nm *to* 200 nm*. (b) Zoomed view of the transition to the thinnest Al region, with a local thickness of about* 1 nm *(arrow).*

The images also resolve the process-induced layer stack, consisting of the oxidized, self-passivated top SiO_2 layer, the Al UTF, the BOX, and the Si handle wafer. In addition, the protective tungsten encapsulation required for FIB cross sectioning is visible in Figure 4.5 (a). Starting from the $\sim$ 200 nm sputtered Al pad on the left, the film forms a continuous $\sim$ 6.5 nm thick layer extending over $\sim$ 1.5 μm. Further along the structure, the layer thickness decreases first to approximately 2 nm and eventually to about 1 nm, as seen in the cross-sectional HAADF-STEM images of sample MA7 in Figure 4.5 (b). This layer thickness

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of about 1 nm corresponds to the ultrathin, central region of the dumbbell structure shown in Figure 4.4. The continuity of the film and the successful formation of the layer by the additive process are confirmed by the HAADF-STEM images.

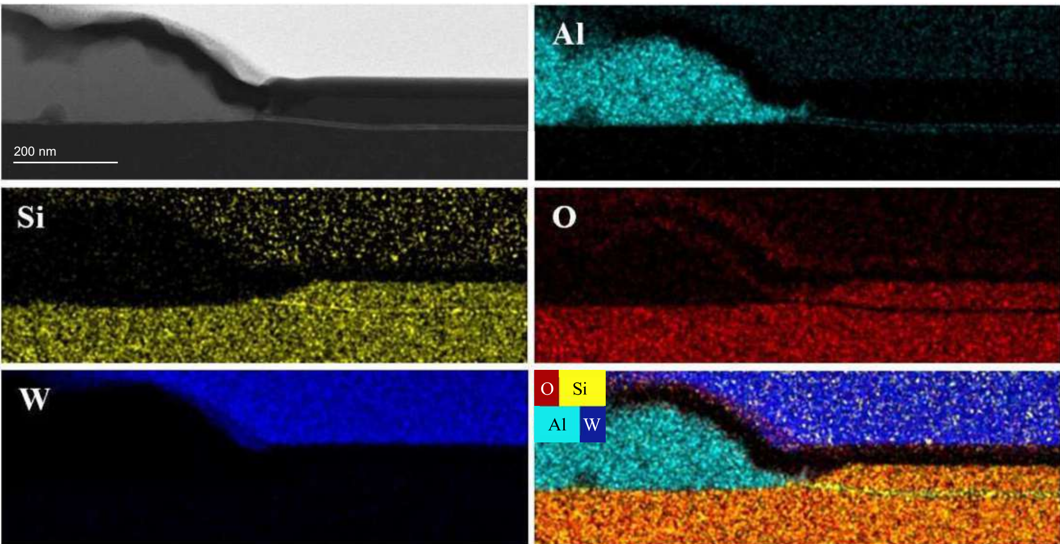

Figure 4.6: *HAADF-STEM image of the deposited and exchanged Al region with corresponding STEM-EDX elemental maps showing the elemental distributions of Al, Si, O, and W (FIB-deposited protective cap), together with their composite overlay. The* 6.5 nm*-thin segment corresponds to the Si/Al layer formed by the additive process due to the protective sputter-deposited Si layer applied.*

EDX maps of the ∼ 200 nm- and 6.5 nm-thick Al segments, as illustrated in Figure 4.6, show that the metallic layer is essentially oxygen-free and, together with the Al and Si distributions, reveal a Si core with an Al shell-like morphology in the 6.5 nm thick segment. A curvature at the transition from sputtered to thin Al is observed and attributed to mechanical stress during oxidation [69, 71, 74, 82, 186]. The associated Al atomic-fraction profile reveals an Al-rich shell of roughly 2 nm thickness. These features persist across regions of varying film thickness, as evidenced by the BF STEM image and corresponding STEM-EDX maps in Figure 4.7, corroborating that the core–shell motif is not confined to the 6.5 nm-thick part of the layer. Further along the structure, in regions where the Al film thickness varies between 0.8 nm to 1.5 nm, Figure 4.8 shows that complementary BF-STEM and STEM-EDX measurements confirm that the metallic layer remains oxygen-free, while the core–shell morphology is no longer observed. The corresponding spectrum exhibits a distinct Al peak, consistent with a local Al film thickness of 0.8 nm to 1.5 nm.

In summary, a lateral thickness evolution from ∼ 200 nm and 6.5 nm down to ∼ 1.5 nm and 0.8 nm over micrometer-scale distances is observed, together with a core–shell-like morphology in which a Si-rich core is encapsulated by Al-rich shells that persist even in the ultrathin regime around ∼ 1.5 nm. A continuous Al layer is observed in segmented regions

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of the ultrathin structures and for thicknesses between 0.8 nm to 1.5 nm, demonstrating that the additive process enables the fabrication of ultrathin, continuous Al films.

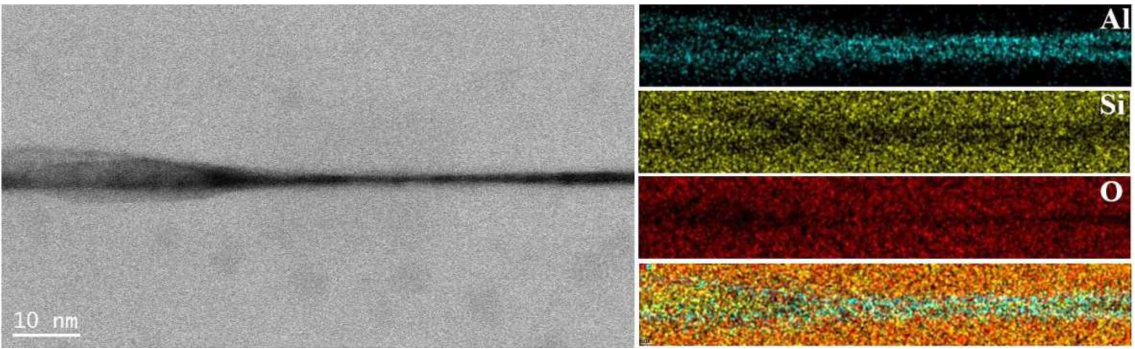

Figure 4.7: *BF-STEM image of the metallic layer across a region where its thickness varies, together with corresponding STEM-EDX elemental maps of Al (cyan), Si (yellow), O (red), and their composite overlay. The layer thickness changes along the structure from* 6.5 nm *to* ∼2 nm.

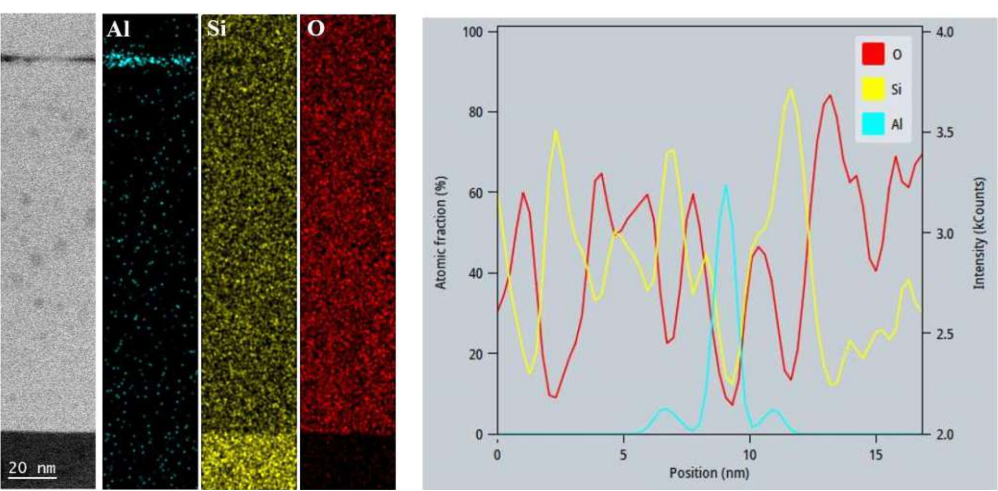

Figure 4.8: *BF-STEM image of a region of sample MA7 where the Al layer thickness varies from* ∼0.8 nm *to* 1.5 nm*, with corresponding STEM-EDX elemental map showing an Al rich core.*

4.1.5 Comparison of the different fabrication methods

The key differences between the two approaches for the fabrication of *ultrathin* samples are the surface quality and the yield. Cross-sections of the two processing routes used to fabricate Al UTFs, together with the *standard processing* procedure for thicker Al films, are compared in Figure 4.9. The yield of *approach 1* (subtractive process), which uses PECVD to protect the contact region, is low at approximately 10 %, and the surface quality is degraded by HF etching and subsequent re-oxidation. In contrast, *approach 2* (additive process) achieves yields above 90 % and provides a stable and reproducible method for

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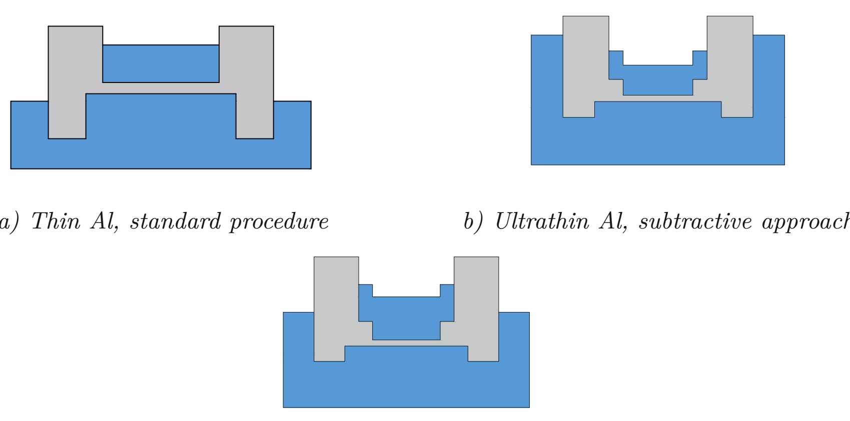
producing high-quality Al structures. An overview of the yield and process characteristics is given in Table 4.7.



a) Thin Al, standard procedure *b) Ultrathin Al, subtractive approach*

c) Ultrathin Al, additive approach

Figure 4.9: *Comparison of processed thin and ultrathin Al structures obtained by the three fabrication routes.*

Table 4.7: *Comparison of fabrication methods for thin and ultrathin Al layers*

Parameter	**Thin films**	**UTF subtractive**	**UTF additive**
Yield	$> 90\,\%$	$\sim 10\,\%$	$> 90\,\%$
Interface quality	Good	Poor	Good
Process complexity	Low	High	Moderate
Reproducibility	High	Low	High

4.2 Physical properties of ultrathin Al layers

The physical properties of Al thin films (10 nm to 200 nm) and UTFs (1 nm to 10 nm) are investigated. Various samples are fabricated using the processing routes described above (standard, additive, and subtractive), and additional reference samples of varying thickness, consisting of conventional sputtered Al films, are prepared for comparison. The investigations include measurements of the electrical resistivity, ampacity, and $1/f$ noise at room temperature, as well as measurements of the critical transition temperature T_c at which the Al structures become superconducting. In the following, the results of the individual measurements are presented and compared with reference values reported in the literature.

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4.2.1 Resistivity of ultrathin Al layers

Figure 4.10 shows a double-logarithmic plot of the resistivity as a function of the Al layer thickness. Reference values for bulk Al and for an Al–Si alloy containing 1 % Si [140, 141] are indicated by horizontal bars for comparison. The measurement repeatability of the setup is better than 0.01 % for an individual data point; however, the plot in Figure 4.10 shows individual samples (including multiple devices at nominally identical film thickness), i.e., no averaging is performed, so the relevant scatter is already represented by the spread of the data points and statistical error bars are omitted. For thicknesses above 10 nm, no thickness dependence of the resistivity is observed. Below 10 nm, the resistivity decreases with decreasing thickness.

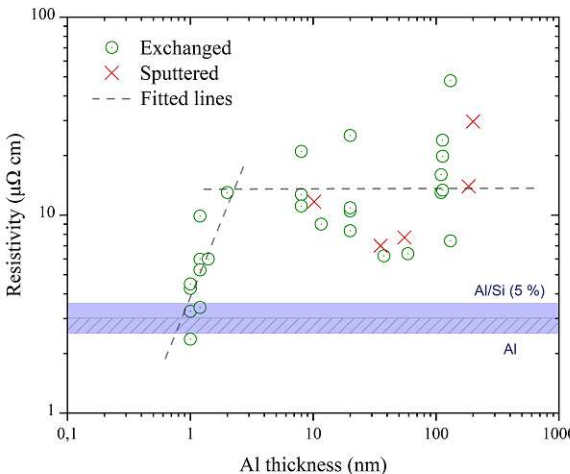

Figure 4.10: *Resistivity of Al films as a function of Al layer thickness on a double-logarithmic scale. The dashed lines serve as a guide to the eye. The blue dashed and blue horizontal bars indicate the bulk resistivity of Al and Al/Si composition (5 % Si).*

Within this range, processed Al UTFs exhibit resistivity values approaching those of bulk Al. In the literature, as discussed in subsection 2.2.1, it is generally reported that the resistivity of UTFs *increases* with decreasing film thickness, consistent with classical size-effect models such as FS and MS. Plausible mechanisms for the counterintuitive behavior observed here include: (i) increasingly ballistic electron transport in the extreme thickness regime, effectively reducing scattering events; (ii) quantum-confinement-induced modifications of the DOS near the Fermi level; and (iii) exceptional interface quality and intrinsic self-passivation due to the buried SiO_2 encapsulation inherent to the solid-state exchange on SOI, which minimizes defect- and oxide-related scattering pathways [187]. These factors jointly provide a possible framework for the observed resistivity decrease, while remaining compatible with classical models in the appropriate (thicker) limits.

At around 1 nm, the conductivity reaches about $4 \times 10^5\,\mathrm{S\,cm^{-1}}$, comparable to values reported for state-of-the-art nanocarbon conductors [144]. Considering only our measured

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data for thicknesses below 10 nm, we find that as the Al UTFs become thinner, their resistivity decreases and approaches the bulk Al resistivity. The observed decrease in resistivity at smaller film thicknesses may be related to an electronic quantum size effect in the thinnest samples. In addition, the localization of charge carriers within individual grains suggests that charge transport is at least partially governed by a hopping mechanism, whose efficiency can change with grain size and morphology in UTFs. With a larger sample size and finer increments in the layer thickness, the behavior could be analyzed in more detail.

4.2.2 Ampacity of ultrathin Al layers

Electrical measurements of Al UTFs reveal that higher currents can be carried before the respective structure fails. In Figure 4.11, (a) shows a systematic increase in ampacity for decreasing structure thickness. For the measurements, the dumbbell structures shown in the optical image in (b) are used. During these ampacity measurements, failure occurred predominantly at geometry transitions and near the positively biased contact as illustrated in (c), consistent with localized Joule heating and electromigration effects in regions of enhanced scattering and supporting the hypothesis of ballistic electron transport. When the film thickness falls below the phonon mean free path in Al ($\sim 10\,\text{nm}$), confinement can reduce electron–phonon scattering, which lowers resistive losses and may therefore enable higher sustainable current densities [187]. For the thinnest films ($t \sim 1\,\text{nm}$), the measured critical current density is $J_{\text{crit}} \sim 10^{10}\,\text{A/cm}^2$. These figures exceed values typical for back-end-of-line Cu in the size-effect regime [142] and approach those of advanced carbon conductors [144].

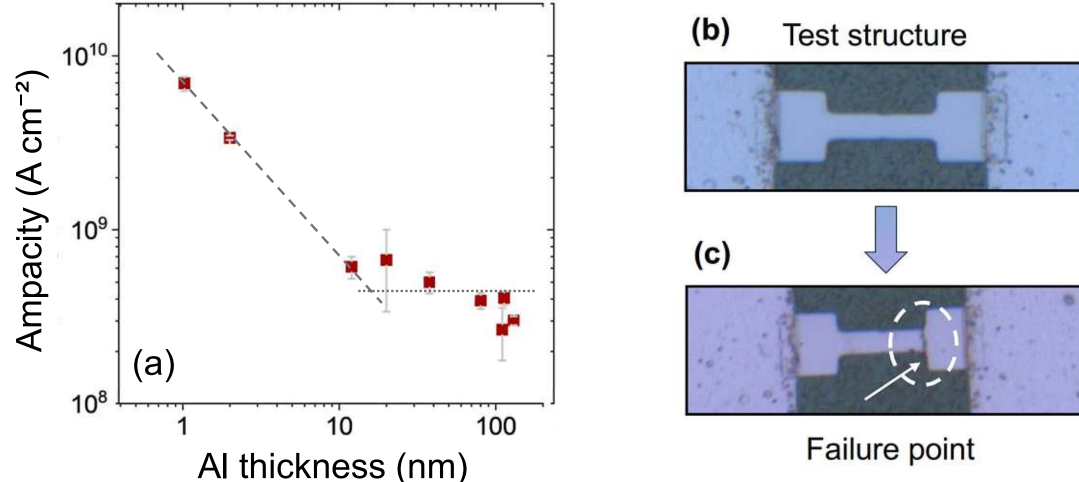

Figure 4.11: *(a) Ampacity versus Al layer thickness; dotted and dashed lines guide the eye, with a steeper trend for Al UTFs down to 1 nm. (b) Dumbbell test structure. (c) Structural failure during ampacity testing. Image adapted and modified from [187].*

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4.2.3 $1/f$ noise of ultrathin Al layers

Figure 4.12 shows the standardized power spectral density (PSD) as a function of frequency for Al films and UTFs with thicknesses ranging from $\sim$1 nm to 200 nm. The low-frequency noise spectra reveal a pronounced reduction in normalized $1/f$ noise as the Al films become thinner. The spectra exhibit a $1/f^{\gamma}$ dependence with $\gamma \approx 1$ over the measured range, while the overall noise magnitude *systematically decreases* with decreasing thickness. The observed trend contrasts with the commonly observed increase of $1/f$ noise in ultrathin metallic films [150]. UTFs typically exhibit *enhanced* $1/f$ noise due to increased surface-, interface-, and defect-assisted scattering [150]. The systematic suppression of $1/f$ noise with decreasing thickness in the ultrathin Al layers suggests a cleaner, more ordered conduction channel with reduced defect participation. This interpretation is consistent with (i) the crystalline quality of the exchanged Al layers evidenced by atomic-resolution (S)TEM, (ii) the lateral continuity and smooth encapsulation of the Al film between the BOX and thermally grown SiO_2, and (iii) transport characteristics indicative of reduced el–ph scattering in the ultrathin limit [187]. The reduced low-frequency noise underlines the suitability of Al UTFs for low-noise nanoelectronics and superconducting/quantum-circuit environments where suppressing $1/f$ fluctuations is critical [149].

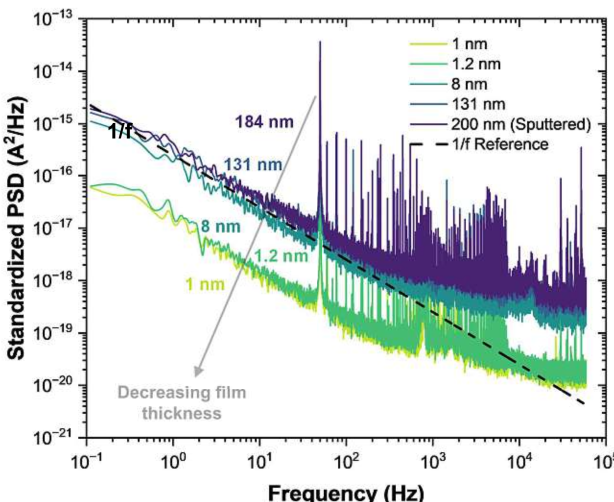

Figure 4.12: *Standardized PSD as a function of frequency for Al films of different thicknesses, measured at* 293 K*. The dashed line indicates the* $1/f$ *reference. Thinner samples exhibit lower noise. Image taken from [187].*

4.2.4 Superconducting transition temperature of ultrathin Al layers

Bulk Al exhibits a superconducting transition around $T_c^{\mathrm{bulk}} = 1.2$ K [108]; in UTFs, T_c can reach 2.4 K [33]. In our devices, low-temperature four-point transport measurements at the partner institute (NEEL, Grenoble) show an *increase* of the transition temperature with decreasing Al layer thickness, as illustrated in Figure 4.13. For Al UTFs, T_c approaches

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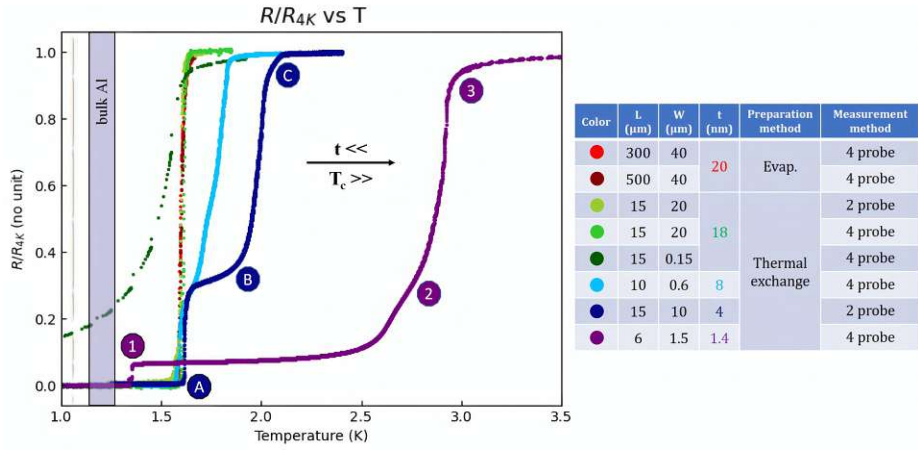
$\sim 2.8\,\mathrm{K}$ at an effective thickness $\sim 1.4\,\mathrm{nm}$, exceeding the bulk value. Superconducting UTFs exhibit an increased T_c primarily due to surface phonon softening and increased electronic DOS from quantum confinement as the film thickness decreases [33]. Furthermore, the substrate influences the phonon spectrum and interfacial coupling [33], modulating the superconducting properties in the ultrathin limit. The features in Figure 4.13 reflect variations in T_c caused by different Al layer thicknesses within the structures (sputtered pads vs. exchanged UTFs) and processing-induced non-uniformity in the ultrathin regime. Consequently, the otherwise sharp resistive transition is broadened and develops steps at the respective T_c values of the individual sections.



Color	L (µm)	W (µm)	t (nm)	Preparation method	Measurement method
red	300	40	20	Evap.	4 probe
dark red	500	40			4 probe
light green	15	20	18	Thermal exchange	2 probe
green	15	20			4 probe
dark green	15	0.15			4 probe
light blue	10	0.6	8		4 probe
dark blue	15	10	4		2 probe
purple	6	1.5	1.4		4 probe

Figure 4.13: *Superconducting transition temperature T_c versus Al layer thickness t for different device geometries, with L ranging from $6\,\mu\mathrm{m}$ to $500\,\mu\mathrm{m}$, W ranging from $0.15\,\mu\mathrm{m}$ to $40\,\mu\mathrm{m}$, and t ranging from $1.4\,\mathrm{nm}$ to $20\,\mathrm{nm}$.*

Point 1/A occurs close to the bulk Al transition and is attributed to relatively thick, almost bulk-like Al regions in the leads and contact pads with up to an additional 1 % Si. Point 2/B marks an intermediate transition likely originating from moderately thinned or partially transformed Al sections, which exhibit an enhanced critical temperature due to reduced thickness and modified microstructure. Point 3/C corresponds to the final transition, where the Al UTF segment itself becomes normal-conducting; this highest effective critical temperature is associated with the thinnest part of the conductor. The observed kinks thus reflect the longitudinal inhomogeneity of the devices, with different portions of the current path undergoing the superconducting-to-normal transition at different temperatures. These effects are less significant for the thicker samples, as T_c is close to the bulk Al value. The markedly different shape of the dark-green curve is attributed to a much smaller width ($W = 0.15\,\mu\mathrm{m}$), effectively turning it into a quasi-one-dimensional nanowire. As a consequence, self-heating and inhomogeneities broaden and shift the superconducting transition, resulting in a more gradual and more extended $R/R_{4\mathrm{K}}(T)$ dependence than that of the wider, more two-dimensional strips.

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Chapter 5

Summary and outlook

Continuous Al UTFs with thicknesses down to ~ 1 nm, corresponding to about three to four layers of Al, were successfully fabricated using the TIER-based processing approach developed in this thesis. The analyses confirmed the continuity and crystallinity of the Al layers, as well as the long-term stability of the resulting structures due to their intrinsic self-passivation. The processed Al UTFs exhibit decreasing resistivity with decreasing thickness, a strongly increased ampacity, suppressed low-frequency $1/f$ noise, and an elevated superconducting transition temperature. The high yield of the fabricated Al UTFs demonstrates the robustness of the process and provides a reproducible route to structurally and electronically well-defined metallic UTFs.

The obtained electrical data indicate a pathway to refine and validate existing theories of electrical conductivity in metallic UTF systems. A larger statistical dataset with varied geometrical and processing parameters (e.g., annealing time) could provide a solid foundation for quantitative modeling based on the processing approach presented in this thesis [188]. Additionally, a finer gradation of processed Al film thicknesses could enable the investigation of quantum oscillations in superconducting structures, as seen for Pb UTFs [189], and spin-orbit-coupled superconductivity [190]. Due to their reduced low-frequency noise, the Al UTFs may be suitable for use in radioelectronic devices and modern microelectronics [150]. Superconducting quantum interference devices, for example, exhibit pronounced $1/f$ noise that can be the dominant noise contribution up to 1 MHz in highly sensitive flux and current detectors [151]. Combined with the high conductivity observed at ~ 1 nm thickness, the results establish Al UTFs as a promising platform for nanoscale interconnects in high-power nanoelectronic devices [2, 149]. In addition to the electrical properties, the optical and thermal properties may also be of interest and merit further investigation [105, 140, 191].

From a process and materials engineering perspective, further optimization may target the

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complete elimination of the HF etching steps by replacing them with reverse sputtering, thereby simplifying the overall workflow. Further experimental directions include the fabrication of multilayer Al stacks on stacked SOI wafers to achieve high-ampacity interconnects. Similarly, alternating Si/Ge stacks could offer a means to study metal–semiconductor exchange reactions, given the different Al diffusion and exchange temperatures [192] in Si and Ge. Furthermore, a more detailed investigation of the crystallinity as a function of the geometric parameters length, width, and thickness [193], which are assumed to be responsible for the improved electrical properties, would be of interest. Additional investigations of magnetoresistive effects [194–196] and spin dependent changes of reflectivity [46] could address potential applications of Al UTF structures as magnetic field sensors, while systematic studies of Al layers with varying thicknesses between 1 nm to 10 nm may reveal resistivity oscillations that are not observed in this work but have been reported for Al, Pt and Bi UTFs [35, 197, 198]. Moreover, x-ray-based analysis and optical reflectivity measurements [91, 199] could clarify the refractive index and demonstrate the potential of high-quality Al UTFs for plasmonic and nanophotonic applications.

In particular, single-material junctions composed solely of Al – in which superconductivity is locally modulated by controlled film thickness – appear highly promising for the realization of qubits [53] or transmons [200]. The fabrication process of Al UTFs presented in this thesis is furthermore ultra-large-scale integration-compatible, providing a possible path to cutting edge quantum computing technology [52] due to a potentially high integration density. Alternatively, ultrathin hybrid Si–Al structures could be explored as a route toward tunable junctions with both metallic and semiconducting properties. Preliminary findings within our research group suggest that Al nanowires fabricated via the TIER process may exhibit monocrystalline growth, which would further enhance their electrical performance, in particular ampacity and noise characteristics, due to the lack of grain boundaries.

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Appendix A

Processing

Process parameters

Table A.1: *Summary of process parameters used for the fabrication of Al UTFs (additive approach)*

#	Process	Comment
1	Measuring DL	Initial DL thickness evaluation via ellipsometry
2	Lithography DL	Corresponding AutoCAD layout, resist AZ 5214E 1 µm thickness, dose 140 mJ cm^{-2}, 22 s development in AZ 726 MIF
3	RIE	40 s with SF_6, parameters: $p = 20$ mTorr, $T = 308$ K, $\Phi_{SF_6} = 50$ sccm, $\Phi_{O_2} = 4$ sccm, $P_{HF} = 15$ W, $V_{DC} = 58.9$ V, $\Phi_{He} = 5.3$ sccm
4	Acetone bath	10 s, removal of resist
5	Lithography Si	Corresponding AutoCAD layout, resist AZ 5214E 1 µm thickness, dose 40 mJ cm^{-2} + flood exposure, 24 s development in AZ 726 MIF
6	Sputtering Si	6 nm, parameters: $P = 100$ W, $t_{tot} = 60$ s, $V_{bias} = 393$ V
7	Lift-off	Via ultrasonic bath + acetone
8	Oxidation furnace	Depending on DL thickness
9	Lithography Al	Corresponding AutoCAD layout, resist AZ 5214E 1 µm thickness, dose 40 mJ cm^{-2} + flood exposure, 24 s development in AZ 726 MIF
10	HF	Depending on oxidation time
11	Sputtering Al	Reverse sputtering etch for 60 s at 50 W; 10 layers of Al, 1 min cool-down periods between consecutive cycles, in total $\sim$ 200 nm, parameters: $P_{reverse} = 50$ W, $t_{reverse} = 60$ s, $P = 60$ W, $t_{tot} = 600$ s, $V_{bias} = 382$ V
12	Lift-off	Via ultrasonic bath in acetone
13	Annealing	763 K, 5 min; check and repeat if needed

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Artefacts during processing

Artefacts originating from lithography, RIE, and HF treatment can significantly alter the structural quality, leading to undesired residues, overetching, or surface damage. Surface roughness is affected by the chosen SOI wafer, oxidation, and HF treatment, with ultrathin samples being particularly sensitive. Furthermore, Si pile-ups formed during Si sputtering and lift-off can compromise contact formation if not properly addressed. Overall, careful control of lithography focus, etching times, and cleaning procedures is essential to ensure reproducible fabrication of high-quality ultrathin Al structures. In the following, characteristic artefacts originating from lithography, RIE, HF, and RTA processes are analyzed, and their influence on surface quality is discussed.

Through the various process steps described in section 3.3 and section 3.4, the quality of the structures is altered in different ways. For example, pattern irregularities can occur in the RIE processes due to unexposed resist areas (streaks in Figure A.1). Due to unexposed areas caused by a focus error of the laser-writer, resist residues (streaks) have remained, underneath which Si from the DL is still present. The optical image of this test sample is taken directly after lithography, prepared for Si sputtering.

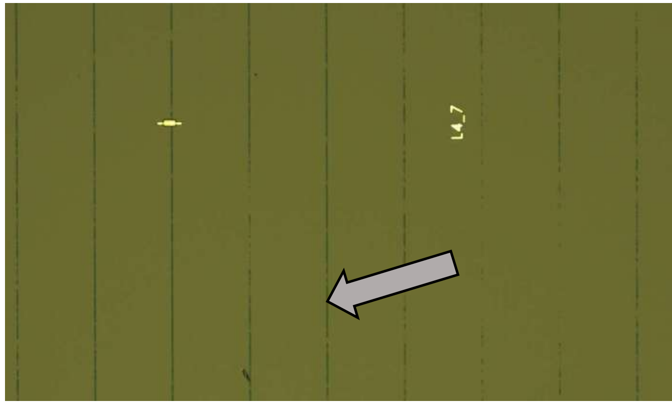

Figure A.1: *Sample area exhibiting RIE-induced pattern irregularities (vertical lines, grey arrow).*

Furthermore, if the RIE process time is chosen too short or the resist is not completely removed, residual Si may remain on the sample and degrade the pattern accuracy. During the subsequent RTA step, this Si can exchange with Al from the contact pads and form an electrically conductive underlayer that may short-circuit the structures under test. It is therefore important to ensure that the lithography has worked properly and that the focus of the laser-writer is correctly adjusted. Likewise, the RIE etching time should be chosen long enough to completely remove the entire Si layer around the desired structures.

Damage due to HF etching can occur when HF seeps underneath the resist (see Figure A.2), for example as a result of resist ageing or improper lithography. In this case, the thermally

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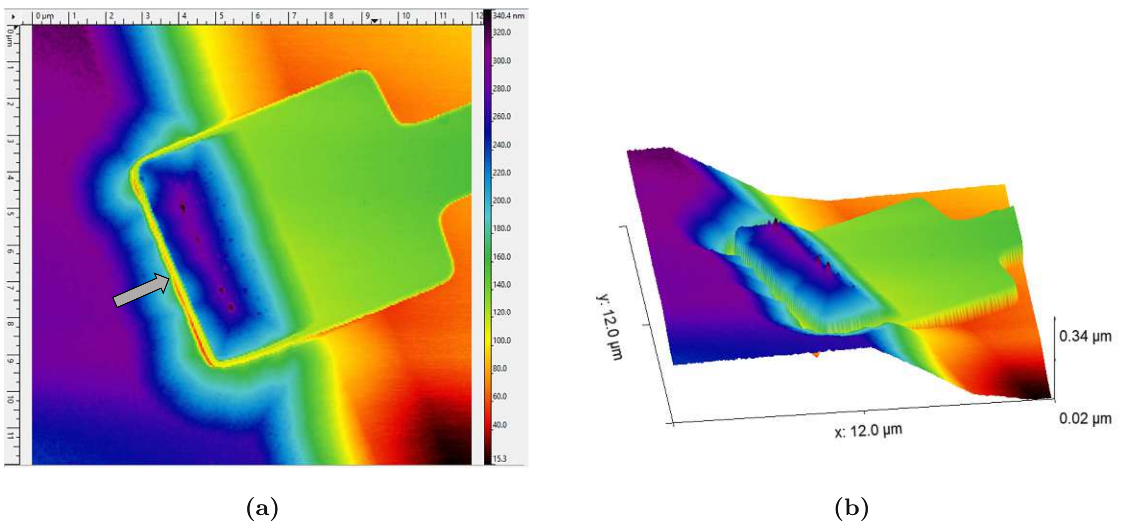
induced Al–Si exchange is suppressed. This issue can be mitigated by using a clean, freshly applied resist layer and keeping the HF etching time as short as possible. In addition, before each oxidation step, it is advisable to clean the wafer and treat it with a HF dip in order to obtain a smoother surface for oxidation and thereby achieve a more uniform oxide growth. Figure A.2 shows AFM images of the ultrathin sample S25 processed using *approach 1* (subtractive) before oxidation: (a) a plan-view AFM topography (height) map and (b) a three-dimensional rendering of the same area. Undesired etching damage caused by the HF treatment is visible, as indicated by the gray arrow in (a). The images show how HF penetrated beneath the large Si pad during etching and undercut the area around the contact point.



(a) **(b)**

Figure A.2: *(a) Plan-view AFM topography (height) map and (b) three-dimensional AFM images of sample S25, showing HF etching damage near the contact pad, as indicated by the gray arrow in (a).*

In addition, care should be taken when immersing the sample into HF to prevent oxygen bubbles from adhering to the surface, which would inhibit etching at those spots - immersing the sample at an angle relative to the HF surface can be advantageous.

- **Very low annealing rate:** Contact with Si underneath the Al pads can occur due to excessive HF etching. Overly long etching times in the etching step can cause direct contact between Al and the BOX layer. Very low rates may also result from insufficient RTA temperatures. Furthermore, the Al–Si exchange rate depends on the DL thickness, since thicker samples require the exchange of a larger amount of Si.

- **Too low RTA temperatures:** At too low temperatures no exchange of Si with Al occurs.

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- **Excessively high annealing temperatures:** At excessively high temperatures, the already exchanged Al retracts from the Si region of the thin structures. Two effects may occur: fracture at the contact site, or retraction of Al. Both effects are shown in Figure A.3.

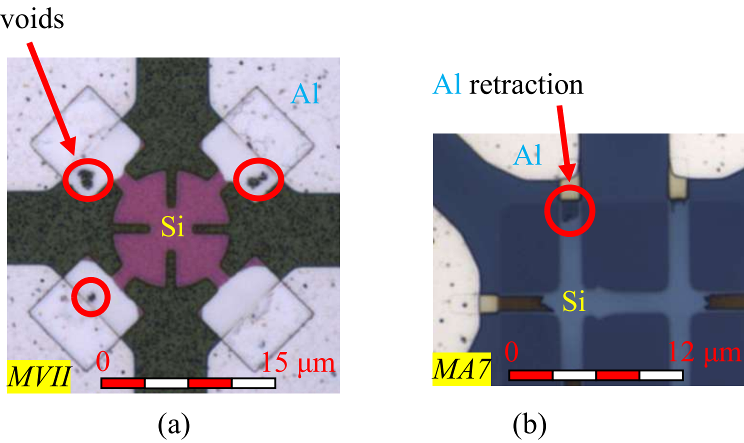

Figure A.3: *RTA result at too high temperatures. Either voids can form in the exchanged Al (a) or the exchange might start but the Al might partially retract from the (ultra-)thin area (b) - the background color (BOX) in these areas specified is visible.*

- **Branching in ultrathin Al:** As oxidation reduces the structural thickness, the Al–Si exchange front becomes increasingly branched and ultimately stops. This effect is accompanied by a transition in the apparent color of the exchanged regions from silvery to brown, together with pronounced branching. Sample MA7 exhibits a DL thickness gradient induced by oxidation; in the thinnest regions, the Al–Si exchange shows strong branching, as observed in Figure A.4.

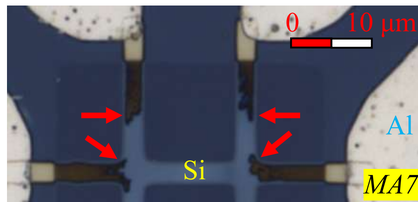

Figure A.4: *Sample MA7: branching of the Al–Si exchange front in the thinnest regions.*

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Appendix B

Designs and geometries

The electrical properties of Al layers can be investigated using test structures with different geometries, allowing the influence of length, width, and thickness on the measured characteristics to be assessed. The shape of the structures (e.g., dumbbell, Hall bar, etc.) has little impact on the manufacturing quality. However, the Si areas to be exchanged by the TIER process should not be too wide ($\gg 10\,\mu m$), as this would hinder the annealing-driven exchange process. Some test structures are present on each sample and are used for alignment and process monitoring. Below, the designs primarily used for fabrication and measurements are presented. The designs evolved throughout the iteration process; therefore, ranges of structural dimensions are provided and accounted for during data evaluation. Since the solubility of Si in Al is approximately 1%, the sputtered Al pads must exceed a minimum size (while larger pads are uncritical). The three AutoCAD designs used for electrical characterization of the Al films are shown below.

Dumbbell

For measurements of electrical resistance (two-point), noise, and ampacity, the dumbbell structure is used. It features a simple design and allows integration of a top gate above the thin central bridge of Si or Al. The various layers are created in AutoCAD and used accordingly for the laser-writer in the respective process steps. The AutoCAD design is parameterized by the length L and width B of the central bridge, with $L = 1\,\mu m$, $3\,\mu m$, $5\,\mu m$ and $10\,\mu m$ and $B = 1\,\mu m$ and $2\,\mu m$. The overlap between Si (yellow-hatched) and Al (solid gray) in Figure B.1 is typically on the order of $3\,\mu m$. This value is determined empirically to compensate for processing inaccuracies while keeping the overlap minimal, thereby reducing the amount of Si exchanged during annealing and shortening the required process time.

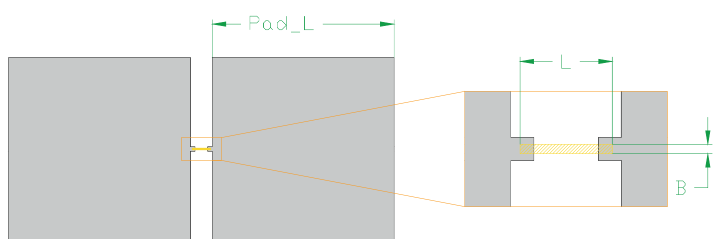

Figure B.1: *AutoCAD layout of a dumbbell structure. Solid gray: Al; yellow-hatched region: Si, exchanged with Al during annealing.* $Pad_L = 196\,\mu m$ *to* $200\,\mu m$, $L = 1\,\mu m$ *to* $20\,\mu m$, $B = 0.6\,\mu m$, $1\,\mu m$ *and* $2\,\mu m$.

Van der Pauw

The Van der Pauw design in Figure B.2 is intended for resistance measurements under an external magnetic field and for Hall-coefficient extraction.

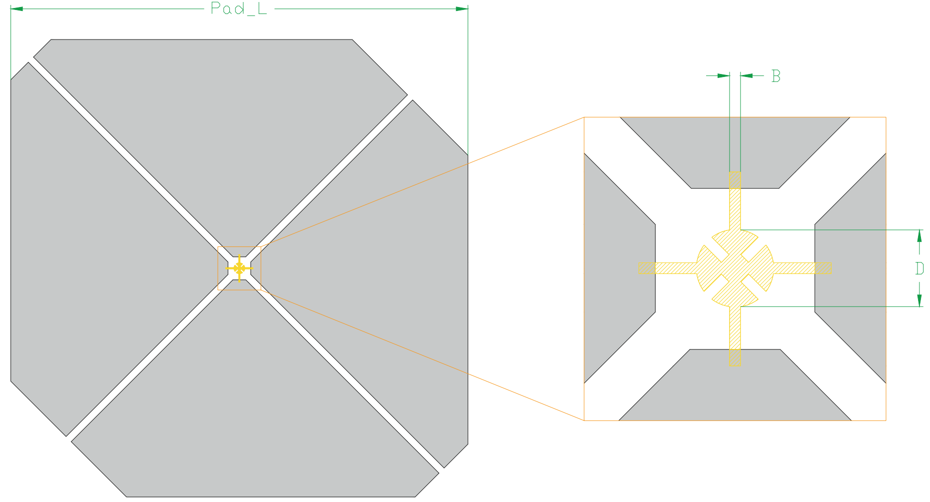

Figure B.2: *AutoCAD layout of a Van der Pauw structure. Gray pads: Al; yellow-hatched region: Si, exchanged with Al during annealing.* $D = 14\,\mu m$, $B = 1\,\mu m$ *and* $2\,\mu m$, $Pad_L = 585\,\mu m$.

Hallbar

The Hall bar design shown in Figure B.3 is used for four-point resistance measurements; in principle, it also enables Hall measurements under an external magnetic field, although this is not implemented in this thesis.

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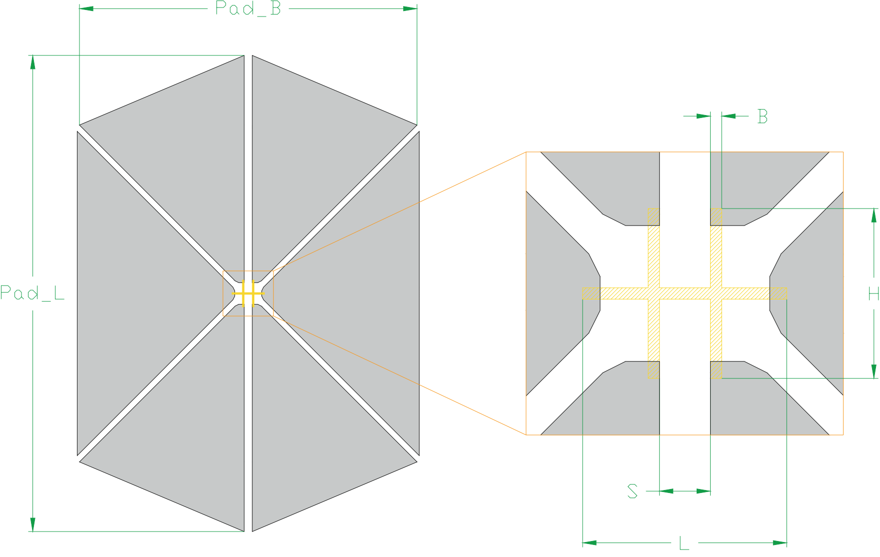

Figure B.3: *AutoCAD layout of a Hall bar structure. Gray pads: Al; yellow-hatched region: Si, exchanged with Al during annealing.* $Pad_B = 528\,\mu m$, $Pad_L = 380\,\mu m$, $B = 2\,\mu m$, $L = 30\,\mu m$.

An overall view of the layout patterned onto the SOI samples can be found in Figure B.4.

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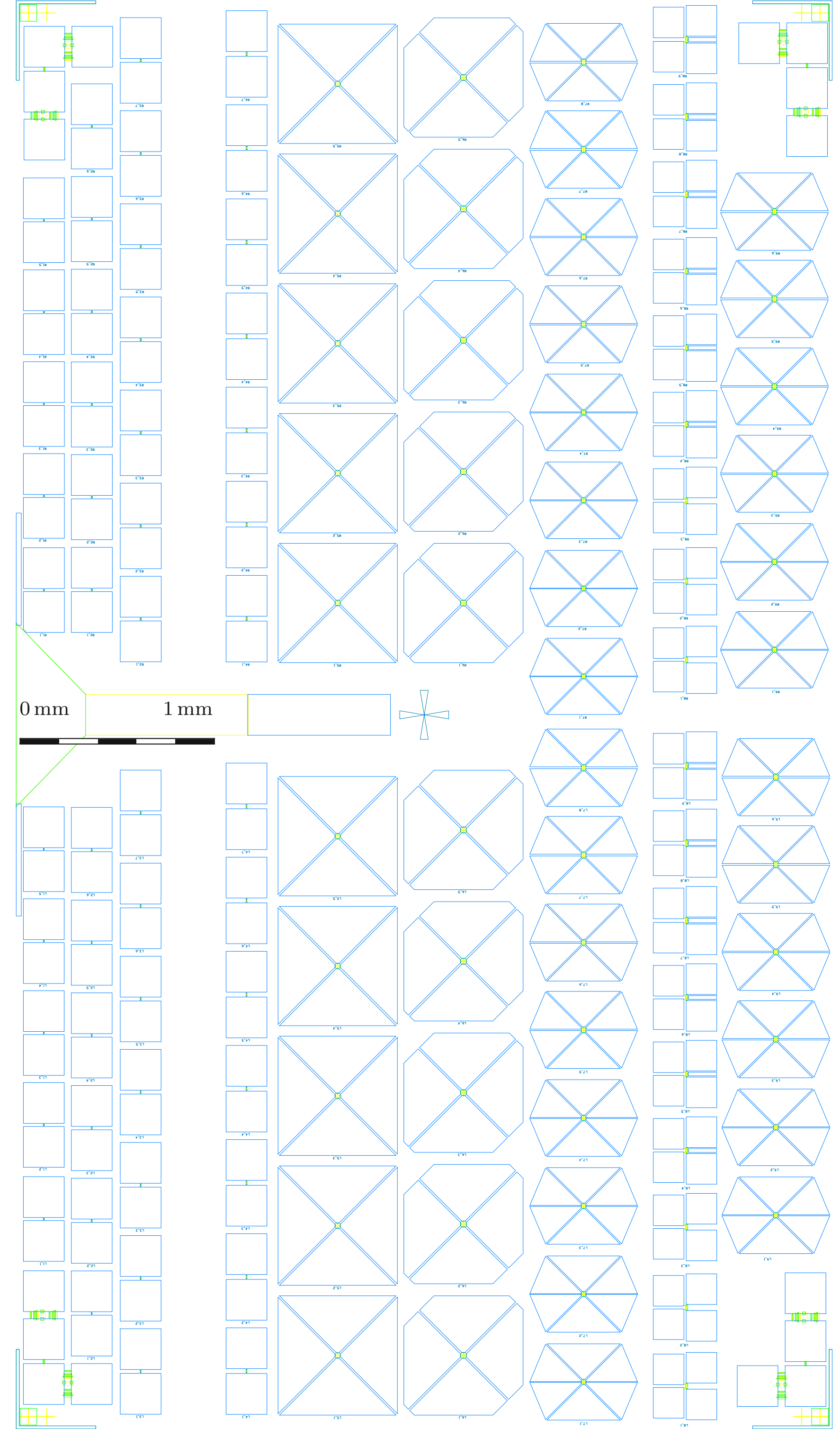

Figure B.4: *Overall layout for fabricating thin Al sheets and Al UTFs, illustrating the individual design layers (color-coded), the range of feature geometries, plus dedicated structural variants and test structures for process diagnostics and layer centering in the middle part and corners.*

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Appendix C

Properties of Al and Si

Table C.1 summarizes key material parameters of Al and Si used throughout this thesis.

Table C.1: *Selected material properties of Al and Si relevant to this work.*

Property	Symbol / unit	Al	Si
Group in periodic table	–	III (metal)	IV (metalloid / semiconductor)
Atomic number	Z	13	14
Crystal structure	–	face-centered cubic (fcc)	diamond cubic
Lattice constant	a (nm)	$\sim$0.4	$\sim$0.54
Dominant stable isotopes	–	^{27}Al	^{28,29,30}Si
Melting point	T_m (K)	$\sim$933	$\sim$1683
Crustal abundance	wt. %	$\sim$8 %	$\sim$25 %
Native oxide type	–	amorphous Al_2O_3	amorphous / thermal SiO_2
Native oxide thickness	t_{ox} (nm)	$\sim$5	$\sim$4
Electrical resistivity	ρ (Ω cm)	$\sim 2.7 \times 10^{-6}$	$> 10^3$ (float-zone, lightly doped)
Thermal conductivity	κ (W m^{-1} K^{-1})	$\sim$240	$\sim$150 (intrinsic)
Superconducting T_c (bulk)	T_c (K)	$\sim$1.2	–
Superconducting T_c (UTFs)	T_c (K)	up to $\sim$2.3–2.4	–
Optical reflectivity (bulk)	R (%)	>90	low (with native SiO_2)
Electron mobility	μ_n (cm^2 V^{-1} s^{-1})	– (metal)	$\sim$1400 (lightly doped)
Hole mobility	μ_p (cm^2 V^{-1} s^{-1})	–	$\sim$450 (lightly doped)
Typical application focus	–	interconnects, contacts, superconducting films	wafers, devices, gate oxides (SiO_2)

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