DIPLOMARBEIT

Formation and Thermoelectric Characterization of Al-Ge-Al Nanowire Heterostructures

zur Erlangung des akademischen Grades

Diplom-Ingenieur

im Rahmen des Studiums

Physikalische Energie- und Messtechnik

eingereicht von

Dominik Ilk
Matrikelnummer 01326218

ausgeführt an der Fakultät für Physik der Technischen Universität Wien
in Zusammenarbeit mit dem Institut für Festkörperelektronik

Betreuer: Ao.Univ.Prof. Dipl.-Ing. Dr.techn. Alois Lugstein

Wien, 22.10.2019 _____ _____
(Unterschrift Verfasser/in) (Unterschrift Betreuer/in)

Statutory Declaration

I declare, that I have authored the present work independently according to the code of conduct, that I have not used other than the declared sources and that I have explicitly marked all material quoted either literally or by content from the used sources.

Erklärung zur Verfassung der Arbeit

Hiermit erkläre ich, dass die vorliegende Arbeit gemäß dem Code of Conduct - Regeln zur Sicherung guter wissenschaftlicher Praxis - ohne unzulässige Hilfe Dritter und ohne Benutzung anderer als der angegebenen Hilfsmittel verfasst wurde. Aus anderen Quellen direkt oder indirekt übernommenen Daten und Konzepte sind unter Angabe der Quelle gekennzeichnet.

Vienna, 22. Oct. 2019 .....

Dominik Ilk

Abstract

Modern society permanently demands more and faster technologies. This leads to the continual improvement and miniaturisation of electronic devices. Due to physical limits and the problem of heat dissipation, scaling becomes increasingly difficult.

Semiconductor nanowires (NWs) are deemed to be one of the most promising building blocks for high-density, ultra-scaled and high-speed microelectronics. NWs are quasi-one-dimensional elongated structures, which are typically only tens of nanometers (nm) in diameter and several µm long. From of the wide range of suitable materials, germanium (Ge) is predicted to be of key interest for future research and technology applications. Ge not only has a more than five times larger exciton Bohr radius compared to silicon (Si), what makes it more likely to study quantum phenomena, it also has a higher carrier mobility, enabling high performance devices.

Furthermore, heterostructured NWs have astonishingly good thermoelectric properties. Thermoelectric devices are capable of transforming heat into energy and vice versa. Because of the one-dimensionality of NWs and their low thermal conductivity, a very high thermoelectric figure of merit (ZT) can be achieved.

In this work, metal-semiconductor-metal (Al-Ge-Al) heterostructured NWs were synthesized with abrupt interfaces and single-crystal aluminum (Al) leads. This was accomplished by using thermally induced diffusion processes between vapour-liquid-solid (VLS) grown mono-crystalline Ge NWs and Al contacts formed by sputter deposition. One of the key strategies for the fabrication of these heterostructured NWs is rapid-thermal-annealing (RTA), because it enables the formation of an ultra-short Ge segment connected by two Schottky-tunnel-barriers. By tuning the process parameters, one is capable of controlling the length of the Ge segment. To secure the Ge from natural oxidation and to confer more mechanical stability, a passivation layer of aluminum oxide (Al_2O_3) was deposited surrounding the wire using atomic layer deposition (ALD).

The electric and thermoelectric characterisation was performed on suspended Al-Ge-Al heterostructured NWs with an average diameter of 50nm at room temperature. The thermoelectric effect was investigated at temperature gradients up to 20K and revealed a Seebeck coefficient of 0,293mV/K.

Kurzfassung

Die Menschheit strebt nach immer schnellerer und leistungsstärkerer Technologie in allen Lebensbereichen. Dieses Streben führt zu einer ständigen Maximierung der Leistung, vor allem durch die Miniaturisierung der elektronischen Bauteile.

Halbleiter Nanowires (NWs) aus Silizium (Si) und Glaiumarsenit (GaAs) werden als vielversprechendstes Basismaterial für ultra-skaliete Hochleistungsbauteile in der Mikroelektronik erachtet. NWs sind quasi-ein-Dimensionale Strukturen mit nur wenigen Nanometer (nm) Durchmesser und ein länge von typischerweise einigen µm. Aus der großen Auswahl an Materialien zeigt sich Germanium (Ge) als besonders interessant für zukünftige Forschungen und industrielle Anwendungen. Der im Vergleich zu Si etwa fünf Mal größeren Excition-Bohr-Radius, ermöglicht die Untersuchung von Quantenphänomenen an größeren Strukturen und damit verminderten Anforderungen an die Prozessierung. Darüber hinaus ermöglicht es die hohe Ladungsträgermobilität, was die Herstellung von Hochleistungsbauteilen ermöglicht.

NW Heterostrukturen haben außerdem erstaunlich gute thermo-elektrische Eigenschaften. Thermoelektrische Bauteile können Wärme in Energie umwandeln und umgekehrt. Wegen der ein-Dimensionalität von NWs, kann eine sehr hohe thermoelektrische figure of merit (ZT) erreicht werden.

Das Thema dieser Arbeit war es, Metall-Halbleiter-Metall (Al-Ge-Al) NW Heterostrukturen zu synthetisieren, welche ein scharfes Interface und monokristallines Aluminum (Al) aufweisen. Dies wurde mittels thermisch induzierten Diffusionsprozessen zwischen Vapour-Liquid-Solid (VLS) gewachsenen monokristallinen Ge NWs und gesputterten Al Kontakten bewerkstelligt. Einer der Kernprozesse der Synthetisierung dieser NW Heterostrukturen ist Rapid-Thermal-Annealing (RTA). Durch gezielte Beeinflussung der Prozessparameter kann die Länge des so erzeugten Ge Segmentes kontrolliert werden. Um das Ge vor Oxidation zu schützen und den NW widerstandsfähiger gegen äußere mechanische Belastungen zu machen, wurde eine Passivierungsschicht mittels Atomic-Layer-Deposition (ALD) aus Aluminumoxide (Al_2O_3) aufgebracht. Die Al-Ge-Al Heterostruktur stellt demnach ein System da, indem ein Halbleitender Ge NW über zwei Schottky-Kontakten, von einkristallinen Al-Zuleitungen kontaktiert ist.

Die elektrische und thermoelektrische Charakterisierung wurde an freihängenden Al-Ge-Al NW Heterostrukturen mit einem mittleren Durchmesser von 50nm bei Raumtemperatur vorgenommen. Aus umfangreichen thermoelektrischen Untersuchungen wurde ein Seebeck Koeffizienten von 0,293mV/K ermittelt.

Acknowledgement

At first I want to thank my supervisor Ao.Univ.Prof. Dipl.-ing.Dr.techn. Alois Lugstein. He incorporated me with open arms in his team, and supported me with good advice every time needed. Also he inspired me with his proclivity for the research with nanowires.

I would also like to express my appreciation to Ao.Univ.Prof.i.R. Univ.Prof. Dipl.-Ing. Dr.techn. Helmut Leeb, Ao.Univ.Prof.i.R. Dr.phil. Herbert Störi and O.Univ.Prof. Dr.phil. Emmerich Bertagnolli, for allowing me to realize my diploma thesis at the Institute of Solide State Electronics.

Furthermore, I want to thank Univ.Prof. Dr.rer.nat Gottfried Strasser for the permission to use the facilities of the Center of Micro- and Nanostructures, particularly the laboratories and the cleanroom. Thereby I want to thank all personal that keeps the cleanroom running, especially OR Dipl.-Ing. Dr.techn. Werner Schrenk for his help and continuous suggestions during the work in the cleanroom.

Special thanks goes to Masiar Sistani and Max Bartmann, who helped me when ever I needed advice. They had every time an open ear for my concerns, find unfailingly the correct words to motivate me, and where there for me when I was in doubt.

Last but not least I want to thank Mr. Clemens Zeiner, who provided me with nanowires, which he had grown.

Most notably, I would like to express my deepest appreciation for my roommates Edi and Wolfi and my great love Jaxi for always being there for me and supported me in every way.

Table of Contents

1. Introduction

Computing systems have a major signification in todays civilization. Sophisticated computing systems open new ways for scientific research, allow faster calculations and continue to push limits further. Since now, more than 50 years ago, Gordon E. Moore published an astonishingly simple prediction, that the number of components, which can be cost-efficiently packed onto a single chip doubles every year, further on well known as Moore´s law [1]. Later he revised his original prediction, stating that the complexity doubles only every two years and probably will continue to do so for at least ten more years [2]. Today the complexity of chips is still growing quite fast and critical voices doubt, that Moore´s law will hold much longer, because several physical limits will be reached.

The looming death of Moor´s law is predict by the increasing significance of thermal noise [3], the fundamental limits of quantum mechanics [4], or the problem of heat dissipation [5], to name just a few of the rising problems. One could say that the laws of quantum mechanics are the ultimately limiting factor in the realisation of classical devices, but they also provide an opportunity for unprecedented computation and communication systems [6].

Today scientists are already diligently working on the groundbreaking concept of quantum computers and are developing novel building blocks, which take advantage of quantum mechanical effects and therefor are capable of achieving classically impossible speed-ups.

Another big problem coming up is the continuously increasing energy demand of the computing systems and information technologies. Not only due to more and faster computing systems, also due to the rapidly growing population and higher technology standards around the world, the total yearly consumption of energy is drastically increasing, which makes it a challenging task to provide sustainable energy suppliers. A new awareness of todays humanity of more efficient usage of the heat loss, is also inspired by the climate change, which gets more and more significance in our all daily lives. It is not only necessary to focus on renewable energy, it is also mandatory to find a solution to increase the power output of our energy harvesting methods. One way to increase the degree of efficiency would be utilizing waste heat from industrial processes. Most of the power plants already started to use their waste heat in form of district heating.

Still there is a big amount of heat disappearing into the atmosphere due to industrial processes. This leads to a revival of thermoelectric application. Thermoelectric materials are creating a link between electrical and thermal energy, hence they are capable of generating a potential difference due to a temperature gradient and vice versa. This behaviour is described by the Seebeck- and Peltier effect [7].

The determination of how suitable a material is for this conversion of energy is delineated by the Seebeck coefficient. However, the typical parameter to benchmark thermoelectric performance of a particular material is the figure of merit, ZT [8]. It is a dimensionless quantity and is determined by $\frac{\alpha^2\sigma}{\kappa}T$. To implement a ZT as large as possible, on one hand a high Seebeck coefficient (α) and electrical conductivity (σ), and on the other hand a low thermal conductivity (κ) are desired.

Astonishing recent research has revealed that for a variety of semiconductors ZT can be improved by down-sizing [9-13]. As a result for NWs, there is a significant reduction in thermal conductivity with only a little attenuation of the Seebeck coefficient and electrical conductivity [14].

NWs are getting more and more important in today research as they have a wide field of applications in microelectronic devise such as high-speed field-effect-transistor´s (FETs) [15] and offer great potential for further research in the field of plasmonics [16], photovoltaics [17], energy harvesting, storage, sensor devices [18] and thermoelectric devices.

There is a variety of different semiconductor materials that can be used for the synthesis of NW e.g. Germanium (Ge), Silicon (Si), Galliumarsenide (GaAs) and Indiumarsenide (InAs). From the wide range of different materials, using Ge is not only motivated by its high carrier mobility, which may paves the way for future high performance devices. Also, Ge could supersede Si, as it has a five times larger Bohr radius compared to Si, so it exhibits quantum confinement effects at larger structural sizes [19].

The goal of this work was to fabricate thermoelectric devices of quasi-one-dimensional nanowires made of Ge and aluminum (Al), and to characterize their electric- and thermoelectric properties.

This involves the fabrication of a measurement device, which requires a complex multi-step fabrication process with high-resolution photolithography, chemical- and reactive-ion etching, multi layer sputter deposition and electron microscopy. Furthermore, atomic layer deposition and a convoluted diffusion process were used to form the heterostructured NWs. Moreover a measurement procedure was conceptualized, which involves a needle probe station and several measurement instruments as source-meters, precision semiconductor parameter analyzer and power supplies. Additionally a switchbox has been fabricated, to minimise the possibility of destroying the sensible NWs by electro-static-discharges (ESD) due to connecting and disconnecting measurement-lines during the measurement procedure.

2. Theory

In the first part of this section the basic principles of NW fabrication, with special focus on the vapour-liquid-solid (VLS) growth method [20] are described. In the mid part the fundamental physico-chemical parameters of the materials Ge, Al and the binary system of Al-Ge are discussed, further the fundamentals of solid state diffusion are reviewed. Further on, the metal-semiconductor interface (Schottky-diode) will be discussed. Finally, the last section of this chapter is covering the thermoelectric effects.

2.1. NW synthesis

The synthesis of NWs can be done by several different techniques such as laser ablation [21] or VLS growth [20]. The VLS mechanism is well known since the 1960s, first introduced by Wagner and Ellis [22].
To synthesize Ge NWs featuring VLS growth mechanism, a thin layer of Au is deposited on a Si wafer. Heating up the sample leads to dewetting of the Au layer and small Au nano droplets are formed. These nano droplets serve as catalytic seeds and define the diameter of the growing NW. Figure 1 shows a schematic illustration of the VLS grows process.

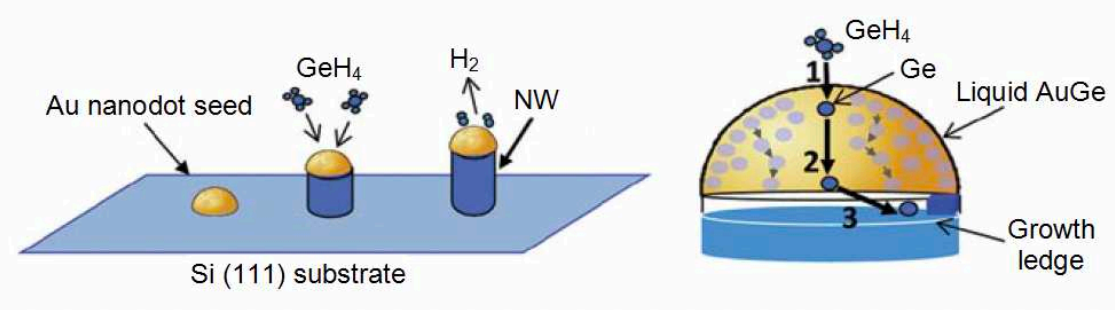


Figure 1: *(left) Schematic illustration of the VLS growth process of Ge NWs, (right) detailed view of the kinetic process of Ge diffusion at the Au-Ge interface during the VLS growth: (1) Adsorption and decomposition of GeH_4 at the Au nanodroplet, (2) Ge diffusion through the AuGe liquid, (3) Ge incorporation at the liquid-solid AuGe interface. Image adapted from [23].*

To initiate the actual growth process the reactor chamber is heated above the eutectic temperature of Au-Ge, which is at 539K [24].

As can be seen in figure 1, a gaseous precursor (GeH_4) is then introduced into the reactor chamber. The Au seeds trigger a kinetic process [25], where they adsorb the GeH_4, followed by a subsequently decomposition into Ge dissolved in catalytic Au particles and gaseous H_2. The non–volatile Ge is diffusing through the liquid AuGe to the liquid-solid interface where it is forming, a vertically solid Ge NW [26]. It is mandatory to ensure stable conditions in the reactor chamber with respect to gas concentration, pressure and temperature in order to prevent kinking along the growth direction [27].
In the last years the applications of NWs have been extended by heterostructures with a sharp atomic interface [28,29]. Since the work at hand is concerning Al-Ge-Al heterostructures consisting of VLS grown Ge NWs, this technique will be explained in detail.

2.2. Quantum confinement in 1D NWs

NWs are elongated nanostructures with a diameter normally lower than 100 nm, and referred as quasi-one-dimensional (1D) materials and are commonly used to study 1D phenomena. They are confining electrons in two dimensions, which leads to a residual movement along only one axis.
Moreover it is possible to observe quantum size effects like confinement of charge carries and photons, and coherent interactions [30]. To understand the 1D of a NW, one have to look at the electronic density of states D(E), which expresses the number of states per unit energy and volume.

To calculate D(E) at first one needs to calculate the available states in the k-space. By considering the electrons in a solid as a free electron gas, with the velocity v, the momentum p and m_e the effective mass, a relation for its energy can be set:

$$E = \frac{1}{2} m_e v^2 = \frac{|p|^2}{2m_e} \tag{1}$$

To establish a wave number, the particle-wave duality from Louise De-Broglie comes in hand.

$$k = \frac{p}{\hbar} \tag{2}$$

Where k represents the base vector in k-space, p the momentum and $\hbar$ the reduced Planck constant. This leads to the energy relation:

$$E = \frac{\hbar}{2m_e}\left(k_x^2 + k_y^2 + k_z^2\right) = \frac{\hbar^2 k^2}{2m_e} \tag{3}$$

Furthermore the time-independent Schrödinger equation (4) has to be solved. Hence the NW has a cylindrical cross-section, the Nabla operator (∇) can be expressed in cylindrical coordinates (r, θ, z). Moreover one can assume plane wave solutions in the z direction. Therefore the z dependence can be excluded (5).

$$\left[-\frac{\hbar^2}{2m}\nabla^2 + V\right]\psi = E\psi \tag{4}$$

$$\left[-\frac{\hbar^2}{2m}\left(\frac{\partial^2}{\partial r^2} + \frac{1}{r}\frac{\partial}{\partial r} + \frac{1}{r^2}\frac{\partial^2}{\partial \theta^2}\right) + V_{(r,\theta)}\right]\psi_{(r,\theta)} = E\psi_{(r,\theta)} \tag{5}$$

Subsequently, the boundary condition (6) has to be set. As the cross-section of the NW can be understood as a 2-D quantum well in polar coordinates with the radial dimension R, the wave function has to vanish outside of the well. Therefore the potential has to be assumed as zero inside and infinite outside of the well.

$$V_{(r,\theta)} = \begin{cases} 0 & \text{for} \quad r < R \\ \infty & \text{for} \quad r > R \end{cases} \tag{6}$$

Furthermore a boundary condition for the wave function has to be set as $\psi(r,\theta = 0) = \psi(r,\theta = 2\pi)$. Since θ is merely present in the second derivative, equation (5) can be reduced to the radial part only. This assumption leads a solution of the Schrödinger equation and a wave function of the form:

$$\psi_{(r)} = C\exp(ik \cdot r) \tag{7}$$

In a quantum well, considering the energy degeneracy, there is only one restricted energy level. With this restriction in k-space, only certain values of k-spaces lead to acceptable electron wave-function solutions.

$$(\Delta k)^d = \left(\frac{2\pi}{L}\right)^d \tag{8}$$

Equation 8 shows the smallest allowed change of k for a particle in a box of the dimension d and a length L. As we are talking about 1-D, two of the k-components are fixed, therefore the area of k-space becomes a length.

$$V_{1D} = \frac{2\pi}{L} \tag{9}$$

Therefor the density of states per unit length in 1-D is given by

$$D_{1D(E)} = \sqrt{\left(\frac{2m_e}{\hbar^2}\right)} \frac{E^{-\frac{1}{2}}}{\pi} \tag{10}$$

where m_e refers to the reduces electron mass, E the energy of an electron and $\hbar$ shows the reduced Plank constant. This leads to sharp spikes of $D_{1D}(E)$ at the sub-band energies [31]. Figure 2 shows the energy distribution of the density of states regarding different dimensionalities. As can be seen the density of states for a 3D system (blue) is continuous, for a 2D system the density of states is discreet, and shows a step function (red). The sharp spikes of $D_{1D}(E)$ are displayed in green. The density of states for a quantum dot is reduced to scalar energy values (black).

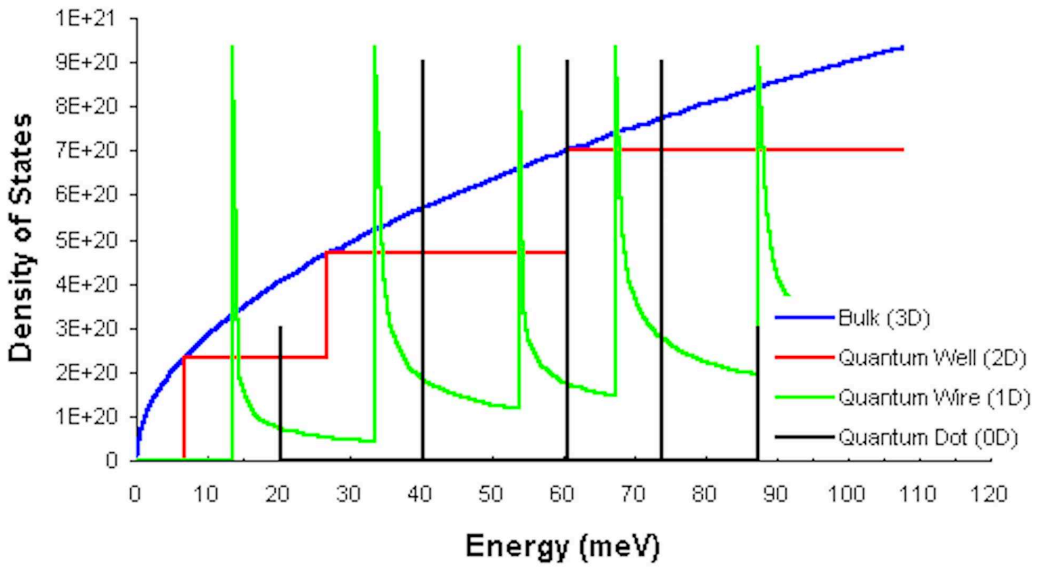


Figure 2: *Density of states for different dimensionalities. Bulk material shows a continuous density of states (blue). A quantum well, which is reduced to 2D, shows a step function (red) and 1D quantum wires show sharp spikes (green). Quantum dots show scalar energy values (black). Taken from [32].*

2.3. The semiconductor germanium

It was first studied in 1886 by Clemens Winkler and named after his homeland Germany. In nature it occurs in mineral compounds like argyrodite or gernabite. At standard condition, it is a lustrous, hard semiconductor with its melting point at 1211K and it boils at 3107K. It is distinguished by the atomic number 32 and a relative atomic mass of 72.64 [33].

Ge is an element in the IV group of the periodic table and a semiconductor with an indirect band-gap of 0.66eV at 300K [34]. Its energy band structure is schematically shown in figure 3.

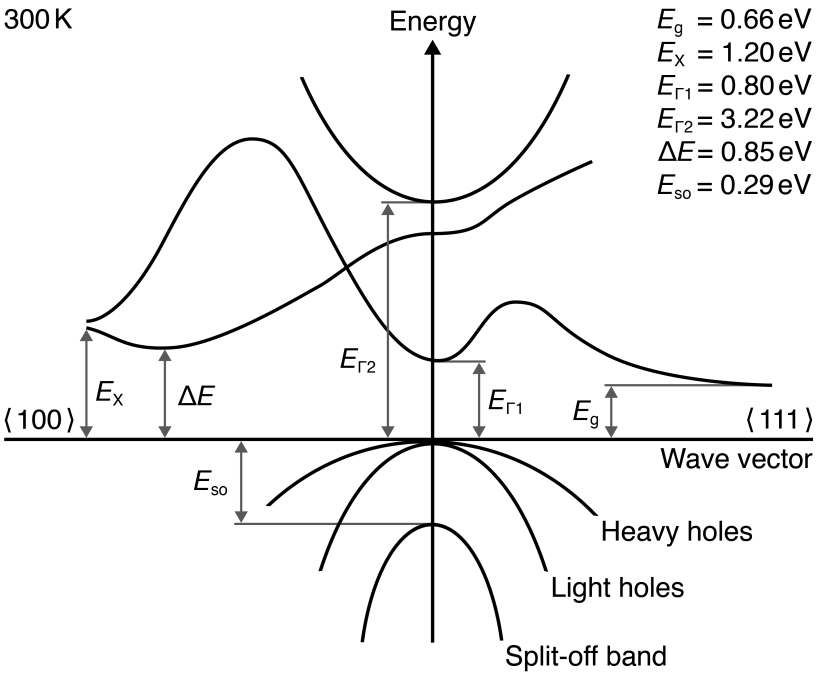


Figure 3: Energy band diagram of Ge at 300K. It shows an indirect band-gap of E_g = 0.66eV. Image adapted from [35].

Like many other semiconductors Ge forms a diamond crystal lattice structure with a lattice constant of a_{Ge} = 0.566nm [36]. The diamond structure is depicted in figure 4. It shows two tetrahedrally bonded atoms in each primitive cell, which are separated by a quarter of the lattice constant in each dimension. The diamond lattice can be viewed as a pair of intersecting face-centered cubic lattices, which are again separated by a quarter of the width of the unit cell. Each atom is surrounded by four equidistant nearest neighbours.

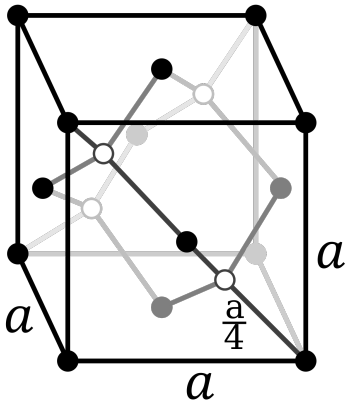


Figure 4: Diamond cubic crystal structure. Taken from [37].

Ge is chemically similar to group IV material Si and Tin (Sn), and naturally reacts and forms complexes with oxygen in nature. One of the most important advantages of Ge comparing to Si is the carrier mobility of $3600 cm^2V^{-1}s^{-1}$ for electrons, which is about twice as high as in Si, and $1800 cm^2V^{-1}s^{-1}$ for holes, what is the highest among all semiconductors [38]. In addition, compared to Si, Ge features the occurrence of quantum confinement effects at much larger structural sizes, because the excitation Bohr radius, which is the distance between the hole and the electron within an excitation, of Ge (a_{BGe} = 24.3nm) is more than five times larger than the one of Si (a_{BSi} = 4.9nm) [36], which is the reason why Ge is more attractive to study quantum confinement effects.

Also Ge and gallium arsenide (GaAs) have a very similar lattice constant, which is the reason why Ge substrates can be used as substrate material for GaAs thin film solar cells [39], that are used for example in the mars exploration rovers.

Beyond the usage in electronic devices, Ge is also used for a variety of different optical systems such as fiber optics and infrared spectrometers [33]. Also Ge-oxides are used for the fabrication of microscope objectives and wide-angle camera lenses, due to its high reflection index and optical dispersion.
It is also used in catalysts for polymerization of polyethylene terephthalate (PET) [40]. Because of the high brilliance of this polyester it is favoured for PET bottles in the marked of Japan.

2.4. The metal aluminum

Al has a very long history on earth. The first written record dates back to the 5th century BC. The ancients used it for dyeing mordant [41]. Attempts to produce aluminum metal date back to 1760, however the first successful attempt was completed by the Danish chemist and physicist Hans Christian Ørsted in 1824 [42]. Nowadays it is extracted of bauxite ore containing between 20 and 30% Al, employing a high energy consuming electrolysis process capable of achieving Al of ≥ 99.99% purity. Also Al has excellent recycle properties where due to secondary production up to 95% of the production energy can be saved compared to the standard electrolysis process. Nowadays up to 30% of the used aluminum is produced with secondary production.

Al is an element in the III group of the periodic table, is designated as a metal and distinguished by the atomic number 13 and relative atomic mass of 26.98 [33]. It is the third most abundant element after oxygen and silicon, and the most abundant metal in the earth crust. By mass, aluminum makes up about 8.3% of the earth's crust [43]. Due to its high chemical reactivity it is most commonly found in minerals, like bauxite ore, granite and feldspar.

At standard condition, Al is a soft, ductile and nonmagnetic metal, with its melting point at 933K and it boils at 2790K. Like many other metals, Al forms a face-centered cubic crystal structure with a lattice constant of a_{Al} = 0.405nm [36]. The crystal structure is depicted in figure 5.

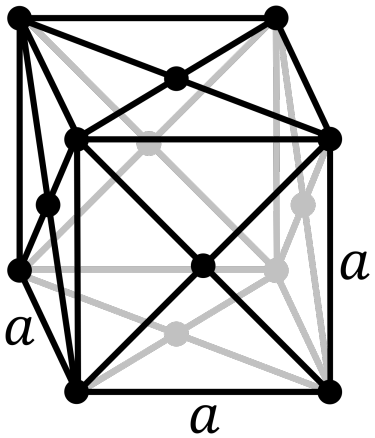


Figure 5: Crystallographic structure of a face-centered-cubic (fcc) cell. Taken from [37].

Al is a good thermal and electrical conductor, showing 59% of the conductivity of copper, while it has a relatively low density of 2.7gcm^{-3} [38], which is 30%

comparing to copper. It is an elementary type-I superconductor with a critical temperature of 1.19K and a critical magnetic field of about 10mT [38].

Today aluminum is the second most used metal after steel, not only because of its favourable electrical properties, also because of its light weight and high corrosion resistance. The high corrosion resistance results from a thin native oxide layer rapidly forming in oxygen-containing atmospheres, what is also the reason for its matt occurring surface [44].

2.5. Binary system Al-Ge

As discussed above, Al is a trivalent and Ge is a tetravalent element. Figure 6 depicts the binary phase diagram of Al-Ge. As can be seen, the eutectic temperature is 420°C (693K). Below the eutectic temperature the solubility is very low, as it is for Ge in Al at about 2% and Al incorporates only about 1,1% into Ge.

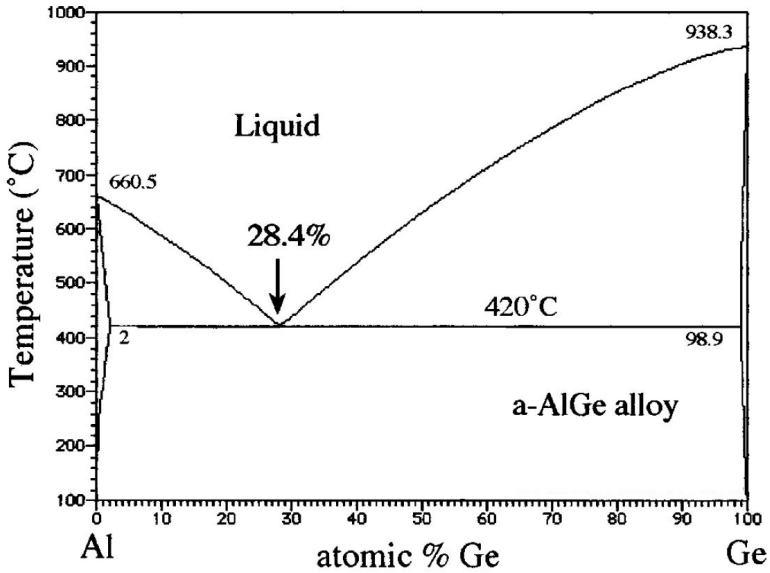


Figure 6: *Phase diagram of Al-Ge. Showing an eutectic temperature of 420°C and an eutectic point at 28.4%. Image taken from [45].*

Hence, it is more likely to find local crystallites rather than intermetallic phases. As it was shown that rapid-thermal-annealing (RTA) of an amorphous thin-film bilayer of Ge and Al deposited on a SiO_2 substrate above the crystallization temperature of Ge, which is at 398K, a metastable amorphous alloy of AlGe is formed in the Ge layer [46].

2.5.1. Solid-state diffusion

The word diffusion derives from the latin word “diffunderes” which can be translated as “ to spread out”, or “to extend”. It plays a fundamental role in a variety of processes in solid-state physics such as thermal oxidation, recrystallization, nucleation of new phases or diffusive phase transformation. Diffusion is a relevant process for a variety of applications, as in solid electrolytes for batteries and fuel cells, diffusion bonding or surface hardening of steel. Moreover diffusion is a fundamental process in semiconductor doping [47].
In terms of classification diffusion is the net movement of atoms or molecules from a region of a higher chemical potential or higher concentration, to a region of lower chemical potential or lower concentration [48]. The driving force is a gradient in chemical potential of the diffusing species. A distinguishing feature of diffusion is the irregular movement of atoms respectively the random walk, which refers to the Brownian motion. This kinetics of microstructural changes results in mixing or mass transport without requiring direct bulk motion. Diffusion not only occurs in solid-states, it also occurs naturally in gases, liquids and amorphous matter.

In crystalline solids the most important diffusion processes are point defects, which will be discussed in detail. In metals point defects appear to be uncharged, whereas point defects in semiconductor can introduce electronic energy levels into their band-gap [47]. The packing density of covalent semiconductor crystals is substantially lower than in close-packed metals, semiconductors are offering considerably more space for self-interstitials [47].
In figure 7 depicts the most common point defect diffusion mechanisms in crystalline materials.

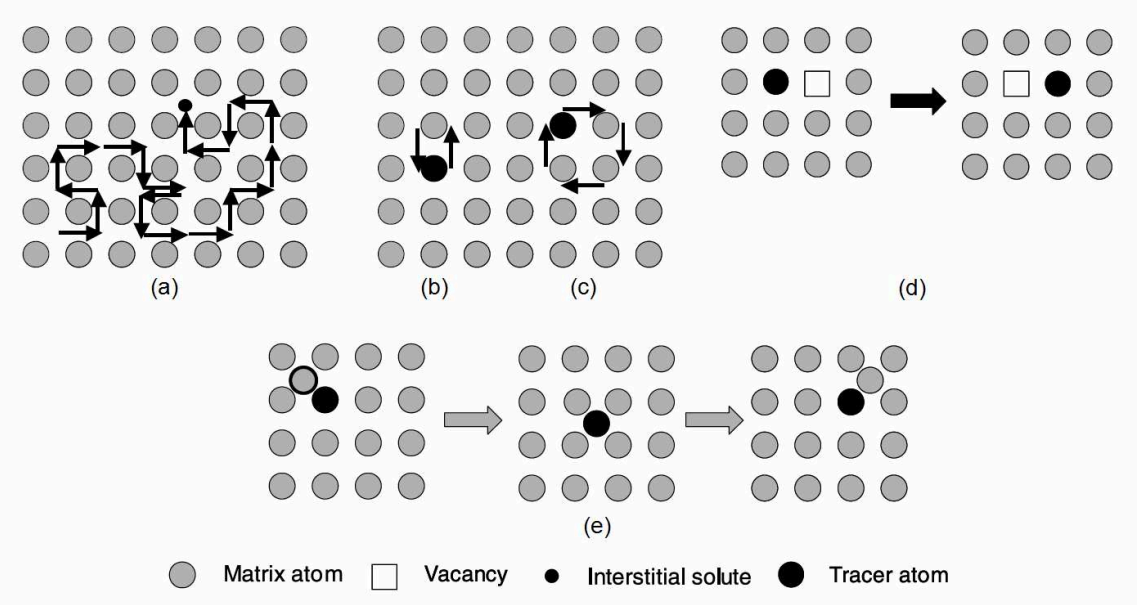


Figure 7: *Point defect - diffusion mechanisms in crystalline solids: (a) Direct interstitial mechanism of diffusion (b) Direct exchange (c) ring diffusion mechanism (d) vacancy assistant mechanism of diffusion and (e) collinear interstitial mechanism of diffusion. Image adapted from [47].*

In figure 7 (a) it can be seen that comparatively small dopant atoms compared to the host lattice atoms are moving throw the host lattice, by jumping between interstitials via random walk till they are incorporated in another interstitial of the host lattice. In case the dopant atoms are more or less equal sized compared to the host atoms, mostly a direct exchange diffusion takes place, as can be seen in (b), or even a direct ring exchange mechanism (c). Further on the most important form of thermally induced atomic defects in crystalline structures are vacancies. Vacancy assistant mechanism of diffusion occurs by jumping of the dopant atoms into a neighbouring vacancy (d). Figure 7 (e) depicts a so-called collinear interstitial mechanism of diffusion, where the dopant atoms are approximately the same size like the host atoms. Both atoms move in unison, which means a self-interstitial replaces an atom on a substitutional site, which then itself is forced to replaces a neighbouring lattice atom. A non-collinear interstitial mechanism of diffusion, where the atoms move at an angle to one another can also occur.

2.5.2. Fick`s law of diffusion

A mathematical description of diffusion processes is given by Fick's first and second law of diffusion [47,48]. The first Fick's law (11) relates the diffusion flux J to the concentration of substance per unit volume, C. It postulates that the flux goes from regions of higher concentration to regions of lower concentration, with a magnitude that is proportional to the concentration gradient. Hence, the diffusion flux J in three-dimensional vector-notation is given by:

$$J = -D\nabla C \tag{11}$$

As can be seen, Fick's first law formulates a direct proportional relation between the flux and the negative concentration gradient, where the proportionality factor between these who parameters is the so-called diffusion coefficient or diffusivity, D. Its dimension is area per unit time, and it is given by:

$$D = D_0 e^{-\frac{E_A}{RT}} \tag{12}$$

where D_0 represents the maximal diffusion coefficient at infinite temperature, E_A is the activation energy to overcome the diffusion barrier, R the universal gas constant and T the temperature [47,48].

To derive Fick's second law, one needs to combine Fick's first law (11) and the mass conservation (13) in absence of any chemical reactions. That means it assumes that the involved species neither have an exchange with internal sources or drains nor undergo any other chemical reactions.

$$\frac{\partial C}{\partial t} + \nabla J = 0 \tag{13}$$

The combining of the two equation (11)&(13) directly yields Fick's second law (14), a linear second-order partial differential equation.

$$\frac{\partial C}{\partial t} = \nabla \cdot (D\nabla C) \tag{14}$$

2.5.3. The Kirkendall effect

In the case of a binary system A-B consisting of two different species of atoms namely Al and Ge, the interdiffusion process can be described with the Kirkendall effect [49,50]. The Kirkendall effect can be understood as the motion of the interface between two crystalline solids that occurs as a consequence of the difference in diffusion rates of the species atoms. Experimentally it can be observed, by placing an insoluble marker at the interface between the two participants, and heating to a temperature at which atomic diffusion is possible. When the temperature is reached, the boundary will move relative to the markers.
The movement of this interface can be mathematically described with the Kirkendall velocity v_K by Darken's first equation (15)[50,51].

$$v_k = (D_A - D_B)\frac{\partial N_A}{\partial x} = (D_B - D_A)\frac{\partial N_B}{\partial x} \qquad (15)$$

D_A and D_B are the diffusion coefficients of the two materials A and B, and N_A and N_B are their respective fractions.

According to the Fick's law (11), the diffusion flux J and the concentration gradient ∇C of both participants must be equal and opposite to each other when a fixed volume axes is considered. Therefor only one parameter is decisive for the description of the behaviour of a binary system diffusion process, the chemical interdiffusion coefficient D_I [48]. The relation between the interdiffusion coefficient D_I of the two participant species and the intrinsic diffusion coefficient is given by Darken's second equation (16)[50,51].

$$D_I = (N_A D_B + N_B D_A) \qquad (16)$$

2.5.4. Diffusion and substitution in the Al-Ge system

Based on the aforementioned fundamentals, the diffusion and substitution behaviour in heterostructures composed of grown Ge NWs connected to Al electrodes was profoundly studied [28,29,52]. It was shown, that Ge of the NW diffuses into the Al when annealed at a temperature between 620K and 700K. That Ge is diffusing into Al and not conversely, accords to the large difference between the diffusion coefficient of Al in Ge and Ge in Al as it is listed in table 1.

	Aluminum in Aluminum	Germanium in Germanium	Aluminum in Germanium	Germanium in Aluminum
E_A (kJ/mol)	123.5	303	332.8	121.3
D_0 (cm^2/s)	0.137	24.8	1000	0.48

Table 1: Al-Ge diffusion paramter. Activation energy E_A and Diffusion coefficient D_0 [53].

The actual diffusion coefficient can be calculated using equation (12). At a temperature of 673K the diffusion coefficient D for Ge or Al in Al is in the area of about 10^{-12} cm^2s^{-1}, as it is for Ge or Al in Ge about 10^{-25} cm^2s^{-1}.
Moreover, the relatively fast substitution of Ge with Al can be explained by the contribution to a quick filling by Al of the vacancies left behind by the diffusion of Ge into the Al rich contact pads where it is dissolved until saturation is achieved. This results in an unreacted pure Ge segment connected by mono-crystalline Al lead, with a sharp atomic interface. Furthermore, metastable alloys are formed at the interface between Ge and Al during the thermal annealing process, which vanish abrupt and form a sharp atomic interface (metal-semiconductor interface) when the temperature is below 500K [28].
With this annealing process it is also possible to manufacture pure mono-crystalline Al NWs, when the annealing process is long enough for the Al to fully exchange all the Ge atoms in the NW.

For the diffusion into solids, vacancies are very important. Grain boundary and atomic imperfections have a very high concentration of vacancies, which is why these regions have a higher diffusivity than the rest of the solid. That's the reason why this microscopic grain boundaries work as trails for the material diffusion [49,54]. It is the same for boundary layers and material surfaces. Because the atoms on the surface have lower boundary force than the inner once, also the activation energy for the surface diffusion is lower [26,49]. At a

high ration of surface to volume, the diffusion process is dominated by surface diffusion.
Figure 8 depicts a schematic illustration of the synthesis of an Al-Ge-Al heterostructure NW coated by an Al_2O_3 passivation layer. This passivation layer infects the diffusion process in no way, it only makes the NW more sustainable against strain and corrosion.

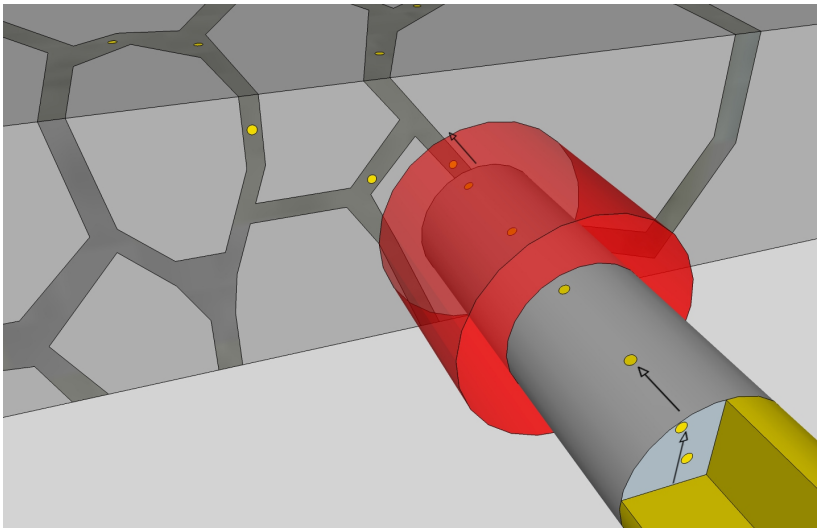


Figure 8: *Schematic illustration of the synthesis of an Al-Ge-Al heterostructure NW with an Al_2O_3 passivation layer (red). The Ge (yellow) diffuses on the surface of the Al-NW (grey) into the Al contact pad and in further consequence along the Al grain boundary (dark-grey). Taken from [52].*

2.6. Metal semiconductor interface (Schottky – diode)

A Schottky-diode is formed by a junction of a metal with a semiconductor. The Schottky-diode, also known as hot-carrier diode, was named after the german physicist Walter H. Schottky. The electric circuit symbol is depicted in figure 9.

Figure 9: *Electric circuit symbol of a Schottky-diode. The left side is metal which acts as the anode and the right side a semiconductor which acts as the cathode.*

However one of the primary features of Schottky-diodes is the rectifying behaviour due to a Schottky-barrier. The height of this barrier is a main characteristic of the Schottky-diode and depends on the material combination and fabrication process. In Figure 10 the Schottky-barrier is denoted by $q\phi_B$ and refers as a potential energy, where q is the electric charge and ϕ_B the electric potential. Figure 10 (a) shows an energy band diagram of a metal and n-type semiconductor and (b) of a metal and n-type semiconductor in contact. The barrier height is predicted by the Schottky-Mott rule, to be proportional to the difference of the metal-vacuum work function ($q\phi_m$) and the electron affinity of the semiconductor ($q\chi$). The vacuum level is defined as the energy level of electrons that are outside the material, as the work function is defined as the energy required, moving an electron from Fermi level (E_F) of a metal to vacuum level. The electron affinity is defined as the energy obtained by moving an electron from the vacuum level to the conduction band (E_C) of the semiconductor.

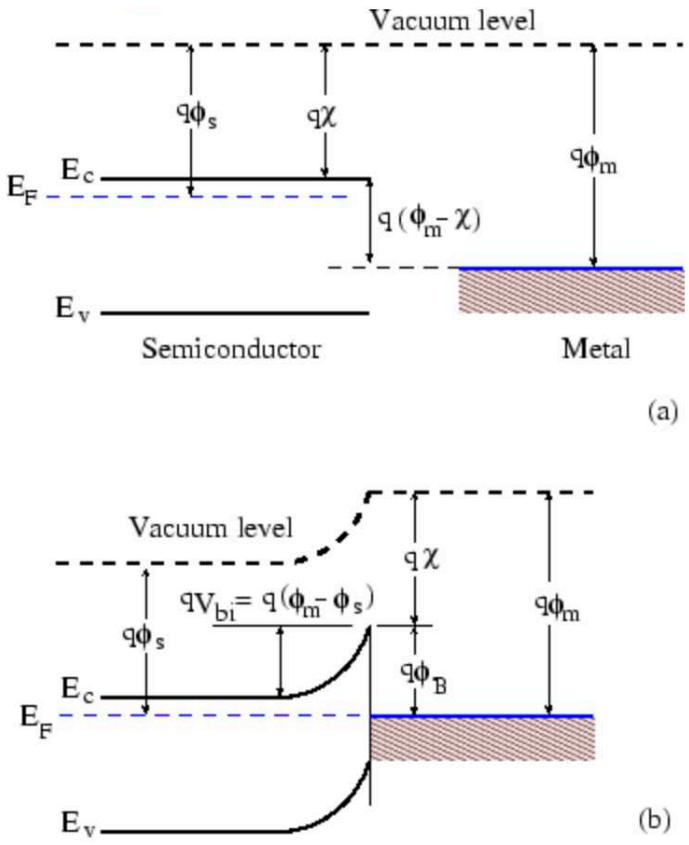


Figure 10: Energie band diagram of a metal adjacent to n-type semiconductor under thermal nonequilibrium condition (a), metal-semiconductor contact in thermal equilibrium (b). Taken from [56].

When a metal and semiconductor are in contact due to charge balancing, the Fermi level of the two materials match at thermal equilibrium. Depending on the relative position of the Fermi levels, respectively the metal work function and semiconductor electron affinity, a Schottky-barrier is formed. In case of an n-type semiconductor, establishing the contact between metal and semiconductor leads to a flow of electrons from the higher level in the semiconductor to the metal. This leads to electron holes in the semiconductor. Hence, a positively charge region, namely the depletion region is formed and results in a deflection of the bands of the semiconductor. Because the electrons in the semiconductor have a higher potential energy than the one from the metal, they are called hot carriers, what is the reason for the name hot-carrier-diode.

When a sufficient high voltage is applied to the Schottky-diode, current starts to flow in the forward direction. Due to the current flow, a small voltage loss occurs across the terminals of the Schottky-diode, the so-called voltage drop. It is the amount of voltage needed to turn on a diode. Standard silicon-diodes show a voltage drop of 0.6 to 0.7 volts, while a standard Schottky-diode has a voltage drop of 0.2 to 0.3 volts [55]. Depending on the material used in the diode the voltage drop can vary. A Schottky-diode has a lower forward voltage drop than a standard p-n junction diode and can be used in high-speed switching applications. Also the Schottky-diode produces less unwanted noise than p-n diodes.

2.7. Thermoelectric effect

The thermoelectric effect is the direct conversion of a temperature gradient to electric power and vice versa. There are three different effects combined in the term thermoelectric effect, namely the Seebeck effect, the Peltier effect and the Thomson effect. When there is a temperature gradient between two sides of the element, due to the Seebeck effect there will be an electrical potential difference. In revers, when there is a voltage applied to the element, heat is transferred from one side to the other, by resulting in a temperature gradient, which is named the Peltier effect. The Thomson effect itself is an extension of the Peltier-Seebeck model and occurs when in materials a spatial gradient in temperature is led to a gradient in the Seebeck coefficient.

According to this work the Seebeck effect will be discussed in more detail. It was first discovered in 1794 by the italian scientist Alessandro Volta [57], and named after the baltic german physicist Thomas Joahnn Seebeck, who independently rediscovered it in 1821. The Seebeck effect at an atomic scale is a result of charge carriers diffusion due to a temperature gradient. It can be explained by the electromotive force (emf). The emf describes the generation of currents even in the absence of an electrical potential difference. The local current density J is given by

$$J = \sigma \cdot (-\nabla \cdot U + E_{emf}) \tag{17}$$

where σ is the local conductivity, U the voltage and E_{emf} the electromagnetic field of the electromotive force. Hence, the Seebeck effect can be understood as a local creation of an electromotive field, E_{emf}.

$$E_{emf} = -S \cdot \nabla T \tag{18}$$

S stands for the Seebeck coefficient, which is a material specific property and ∇T for the temperature gradient. In addition the so-called differential Seebeck coefficient α (also termed as thermo power) is the quantity, which connects the temperature gradient and the voltage.

$$\alpha = \frac{\Delta U}{\Delta T} \tag{19}$$

Due to the thermoelectric effect there is a wide range of possible applications like classification of metals with unknown composition or identify metal alloys. Because thermoelectric elements can convert heat gradients into electricity, or

pump heat by using electricity, it can be used in energy harvesting and solid-state refrigeration. The efficiency of the materials is given by the ZT-value (figure of merit). κ stands for the absolute thermal conductivity of the material. The higher the efficiency of a thermoelectric device, the higher is its ZT value. To gain a maximum ZT one need a high electrical conductivity σ, a large thermal power α and a low thermal conductivity κ.

$$ZT = \left(\frac{\alpha^2 \sigma}{\kappa}\right) T \tag{20}$$

Different thermoelectric materials have different values of ZT, which limit their use to applications at specific temperature range. Figure 11 shows that for lower temperatures (200 to 400K) bismuth telluride (Bi_2Te_3) is preferred, while for temperatures between 600 and 800K, lead telluride (PbTe) is recommended. At higher temperatures (from 800 to 1300K) silicon germanium (SiGe) is used [58].

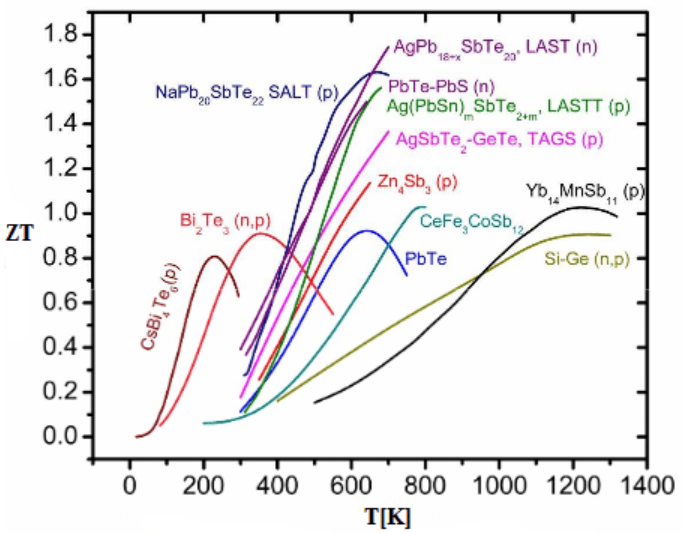


Figure 11: Figure of merit ZT of different thermoelectric materials as a funciton of temperature. Taken from [59].

3. Experimental set up and manufacturing

The following chapter is describing the experimental techniques and processes for the fabrication of Al-Ge-Al heterostructured NWs and the base module on which the wires are placed for proper characterisation. The base module is a macroscopic device, which can be easily handled to allow a sustainable thermoelectrical characterization of the fabricated Al-Ge-Al heterostructured NW. It basically consists of a highly doped Si substrate with a dielectric layer on top with an etched grid. The NWs are located directly over a vertical trench of this grid – so they can be understood as free-hanging wires – via drop-casting. A suitable connection of the NW is given by macroscopic sputtered Al contact pads, which later can be connected with a needle probe station for electric characterization. Further on the base module is capable of heating both sides of the wire separately due to resistive Au heaters. The completed base module with well functioning, connected and measurable Al-Ge-Al heterostructured NWs is called TE test device. In the last part of this chapter the experimental setup and the measurement procedure will be explained. Figure 12 depicts two mesa-pads of the completed TE test device in which between one NW is suspended. One can see the two macroscopic Al contacts and the Au heater structure on each side. The NW is marked in green.

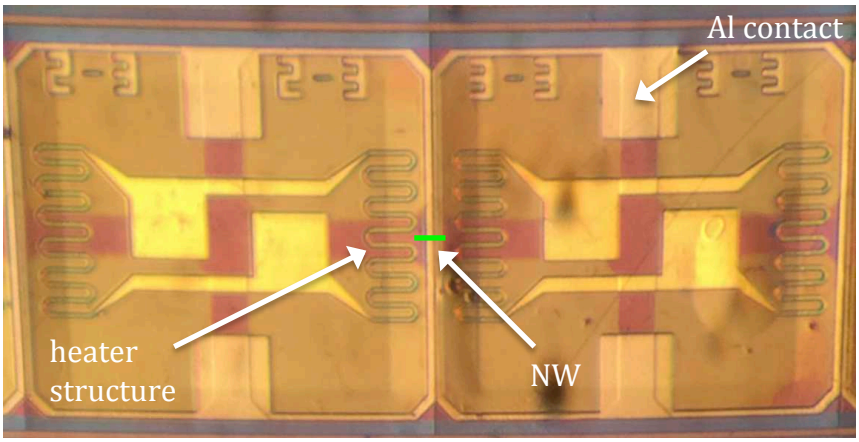


Figure 12: Two mesa-pads of the completed TE test device, in which between one NW is suspended. Image taken with a light-microscope. A NW is symbolized with a green bar.

3.1. Base module

The base module can be understood as mount of the Al-Ge-Al heterostructured NWs for suitable handling and electrical characterization.
It is a 12 x 12 mm^2 device, cleaved from a Si waver. To ensure a measurement of the electrical properties of the wires, without any trap effects, it is mandatory to measure the wires free-hanging. To realise a characterization of a free-hanging NW the base module must have trenches over which the NW is suspended, without any contact to the surface of the base module. Figure 13 depicts one mesa-pad of the base module. One can see the horizontal and vertical trenches. The NWs will be located over the vertical trenches.

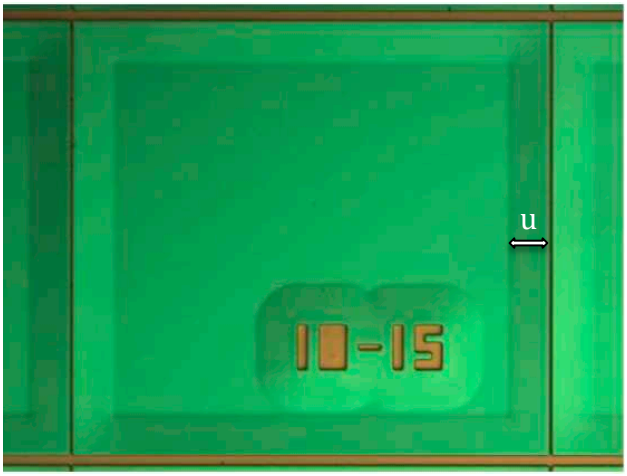


Figure 13: *Mesa-pad geometry. Differential interference contrast light-microscope image of an individual mesa-pad. Showing a vertical trench width of 1µm, a horizontal trench width of 10µm and an undercut u of about 60µm at each pad. Taken from [60].*

Furthermore when they are suspended, a much higher temperature gradient can be achieved along the wire, because there is no thermal dissipation via the base module. An overview of the measurement procedure and a detailed explanation can be found in chapter 3.3.

The manufacturing of the base module is split in 5 steps. Figure 14 gives an overview of these 5 steps, which will be explained in the following sub chapters.

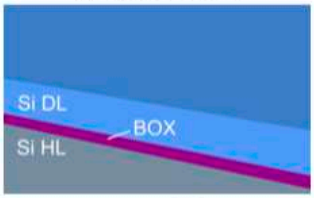
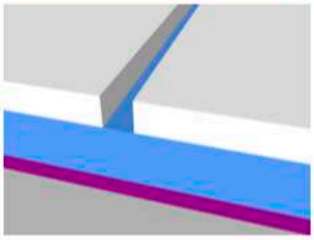
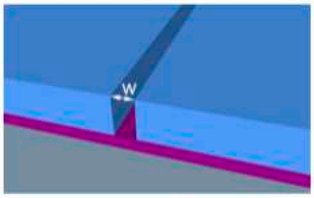
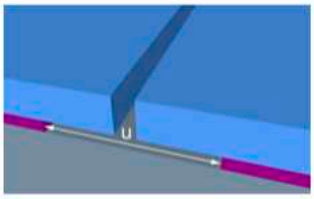
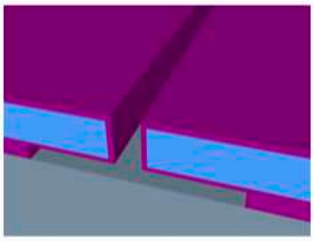
Step	Illustration	Description	Parameters
1		Substrate preparation: Dicing and cleaning	12 × 12 mm SOI (3 µm DL, 1 µm BOX)
2		Etch mask fabrication: Photo-lithography	AZ5214E positive process
3		Trench formation: Reactive-ion etching (RIE) and mask removal	Cryo process SF_6/O_2 -108°C
4		Undercut fabrication: BOX etch and critical-point drying (CPD)	60-120 min 40% HF
5		Pad passivation: Wet thermal oxidation	SiO_2, 300 nm

Figure 14: Schematic presentation of the process steps for manufacturing the base module. Taken from [60].

Step 1 depicts an illustration of the SOI wafer, consisting of a Si handle layer (HL) with a thickness of 500µm, followed by a 1µm buried oxide layer (BOX), with a device layer (DL) of 3µm on top. Step 2 to 5 depicts an illustration of the manufacturing steps needed to form the trenches of the checkerboard patterned grid. After these 5 steps, the base module can be used to manufacture the TE test device (see chapter 3.2).

3.1.1. Substrate preperation and photolithography

As mention before the base module consists of a 12 x 12 mm² device, cleaved from a Si wafer. This wafer consists of a <100> orientated Si DL on top, a Si HL on bottom and a BOX layer in between. Before the checkerboard patterned trenches can be etched via a reactive ion etching (RIE) process (see chapter 3.1.2), a photolithography process using a Cr photomask has to be executed, to predefine the structure of the orientation and location of the trenches.

Prior, the base module is cleaned in acetone and then iso-propanol in a ultrasonic bath (detail process parameter can be found in appendix A). In addition the module will be plasma-ashed with 300W in an oxygen-plasma to remove any organic residues. Subsequently, the module is spin-coated with an image reversal photoresist (AZ5214E). By exposing the photoresist to UV light trough a Cr photomask and subsequently developing in a solution (AZ726MIF), the grid structure was applied onto the base module.
Figure 15 depicts the used Cr photomask for the photolithography process. The vertical trenches have a width of 1µm, and represent the trenches over which the NWs will hang for later characterisation. The horizontal trenches have a width of 10µm.

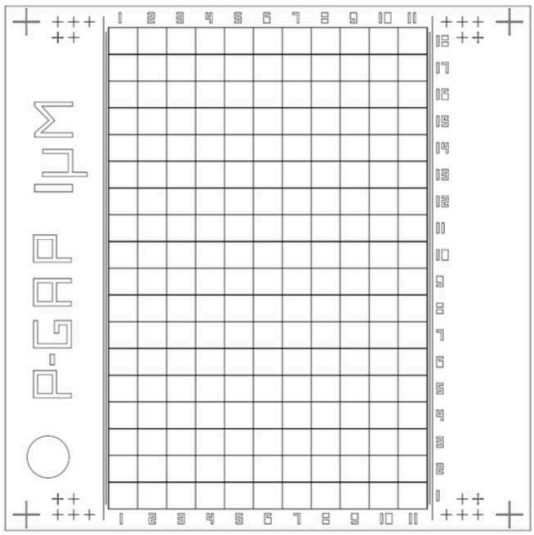


Figure 15: Cr photomask with the checkerboard patterned trenches. The vertical trenches have a width of 1µm and represents the trenches over which the NWs will suspend. The horizontal trenches show a width of 10µm.

After the base module was dipped into the developing solution, the trenches are free of photoresist and the module is ready for step 3, the RIE process where the Si DL layer where etched. Figure 16 depicts a detailed view of the base module with the spin-coated photoresist after the developing process. The grey layer depicts the photoresist defining the 1µm vertical trench.

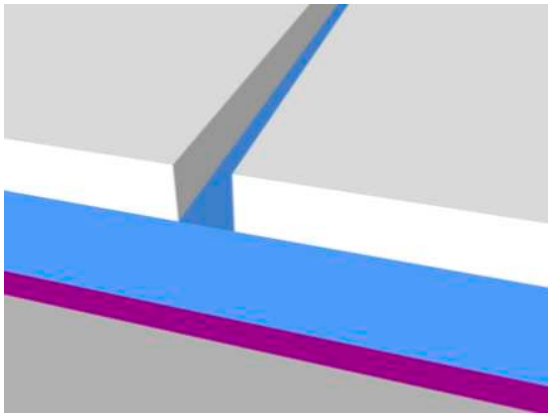


Figure 16: Illustration of the vertical trench formation. The grey layer depicts the photoresist defining a 1µm vertical trench. The blue layer represents the Si DL, which will be etched. Taken from [60].

Photolithography was conducted by using a MJB3 mask aligner from Karl Süss MicroTec AG. The MJB3 mask aligner system features a 275W mercury short-arc lamp exposing light with 450nm. The resolution Re of the minimal achievable feature size [61] for photolithography systems is given by:

$$\mathrm{Re} = k_1 \cdot \left(\frac{\lambda}{\mathrm{NA}}\right) \tag{21}$$

The determining parameters are the wavelength of the exposed light λ, the numerical aperture of the used lens system NA and the factor k_1 depending on various process parameters. Related to equation 21 the actual system allows a minimal feature size of about 0.8µm.

3.1.2. Trench formation with reactive-ion etching

To etch the trenches in the Si DL layer, a RIE process is applied. The trench width is predefined by the photoresist grid, while the depth depends on the etching time. The formation is executed by cryogenic RIE at -108°C in SF_6/O_2 atmosphere. After the etching process the photoresist has to be removed with aceton. For etch depth control, an interferometer has been used. It is mandatory that the whole DL was etched, otherwise the following etching process of the BOX layer with HF will be impeded. Figure 17 depicts an illustration of the trench formation in the DL.

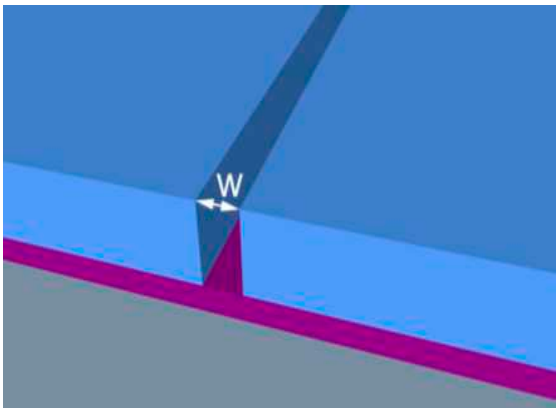


Figure 17: Illustration of the vertical trench formation in the DL. The width of the vertical trench is W = 1µm. Taken from [60].

3.1.3. Forming the mesa-pad structure

After it is ensured that the Si DL layer is completely etched till the BOX layer, the HF etching can be executed. To form the undercut, the BOX layer is selectively etched in 40% HF with an etch rate of about 800nm/min. The length of the undercut for the actual device is u = 121µm. Figure 18 depicts an illustration of the under-etched mesa pads.

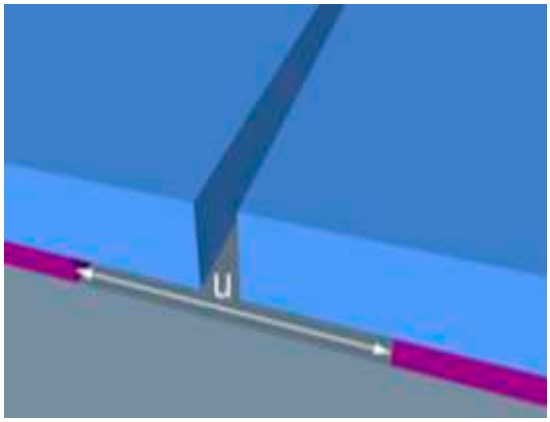


Figure 18: Illustration of the under-etched mesa-pads. The length of the undercut is represented by u. Taken from [60].

After the desired undercut length u is accomplished, the TE test device is dipped into deionized water to stop the etching process. To avoid stitching a critical point drying process is executed. This is necessary to avoid the free-hanging cantilevers from the mesa-pad structure, from bending downwards during the evaporization of the DIW. To finalise the manufacturing of the base module a passivation layer is deposited. Therefore the base module is thermally oxidized with a 300nm thick SiO_2 layer, which is illustrated in figure 19.

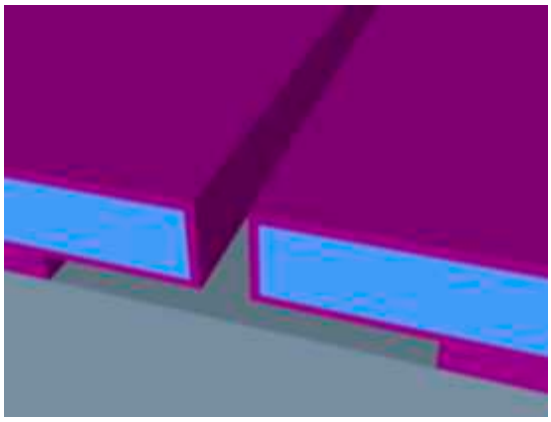


Figure 19: Illustration of the passivated base module due to wet thermal oxidation, with a 300nm layer of SiO_2 (purple). Taken from [60].

After the passivation, the base module is finished and can be used for the TE test device fabrication. Figure 13 depicts an image taken with a light-microscope from an individual mesa-pad with a vertical trench width of 1µm, horizontal trench-width of 10µm and an undercut of 60µm below each pad.

3.2. TE test device fabrication

This chapter is describing how the pre manufactured base module becomes the TE test device. The TE test device is capable of measuring and characterisation of the Al-Ge-Al heterostructured NWs. Furthermore, an explanation of the experimental techniques and process parameters for the fabrication of the TE test device will be given. Figure 20 gives an overview of the 3 steps that are needed to manufacture the TE test device, which will be explained in the following sub chapters.

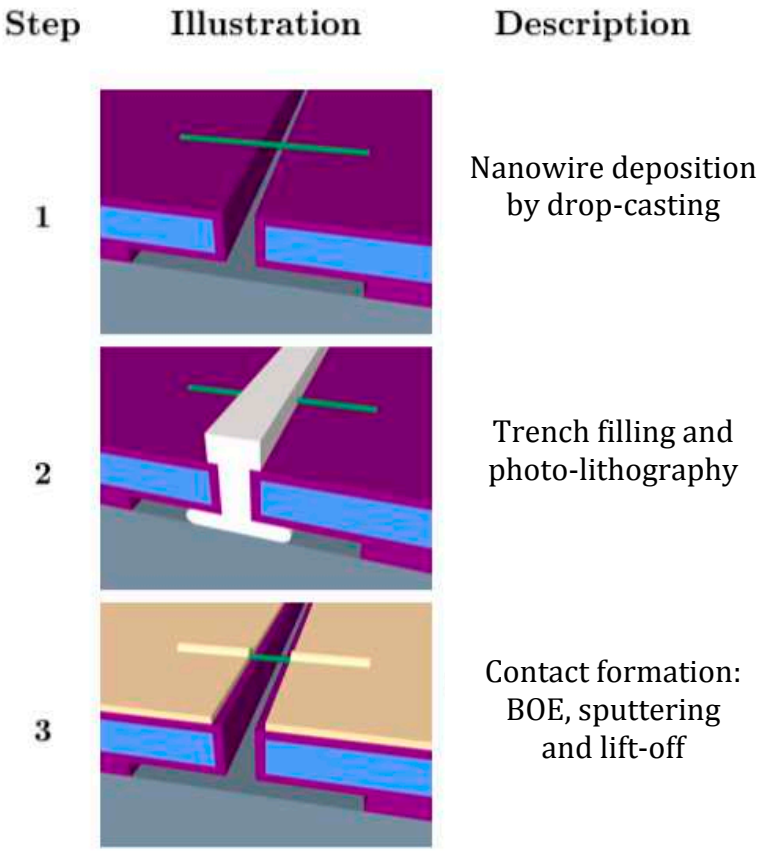


Figure 20: *Schematic presentation of the process steps for manufacturing the TE test device. Taken from [60].*

Anyhow before the NWs can be integrated to the base module by drop casting, they have to be passivated which will be explained in the next section. After the passivation the NWs have to be removed from the growth substrate.

3.2.1. Passivation of the NWs

The Ge wires were grown by the former PhD student Clemens Zeiner at TU Vienna via VLS mechanism (see chapter 2.1.), vertically grown on a Si substrate. They have an average diameter of 50nm and a length of about 8µm. To achieve a higher mechanical stability of the wires and prevent them from oxidation, they are passivated with a 20nm thick Al_2O_3 layer. The passivation were done with an atomic layer deposition (ALD) process [62], carried out with a Cambridge NanoTech Savannah 100. In figure 21 there can be seen (a) the grown NWs on the Si substrate and (b) a schematic of the passivated NWs.

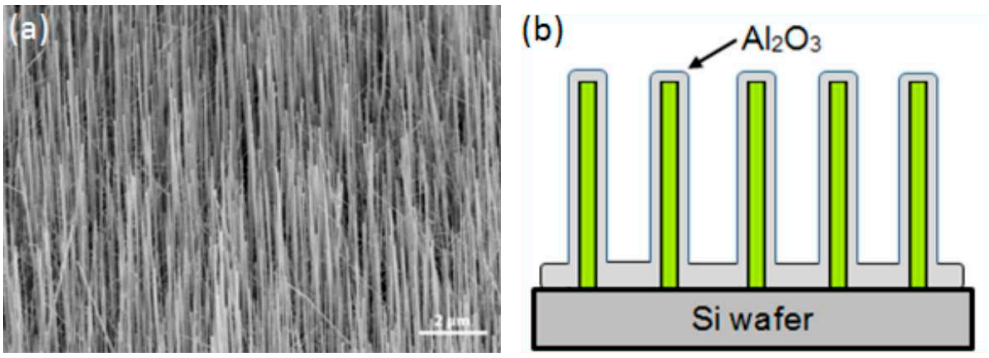


Figure 21: a) Ge NWs grown via VLS process on a Si substrate. Image was taken with a secondary electron microscope (SEM), b) passivated Ge NWs (green) on Si substrate with 20nm Al_2O_3 deposited via ALD. Images taken from [63].

ALD is a gas phase deposition method, which has emerged as an important technique for conformal depositing of thin films for a variety of applications. Due to its sequential, self-limiting surface reactions, it is used for fabrication of continuous and pinhole-free ultrathin films [64], while it allows thickness control on a monolayer scale. Moreover it is used for depositing todays high quality high-k gate oxides such as hafnium oxide (HfO_2), titanium oxide (TiO_2), zirconium oxide (ZrO_2) and Al_2O_3. Furthermore, ALD is used for highly scaled deep trench DRAM capacitors [64] and fabrication of copper diffusion barriers in backend interconnects [65].
In figure 22 you can see a schematic process overview of the binary reaction sequence occurring during the ALD process. The ALD process takes place in a temperature controlled evacuated camber. To begin the process, precursor A (in this case C_3H_9Al) is introduced to the working chamber, where a chemisorption of the introduced gas takes place on the surface of the sample. That leads to an entirely coverage of the surface of the sample by a monolayer, of material A. To start the second step, the working chamber must be evacuated

to remove all residuals of the precursor material A. Subsequently, precursor B (vaporous H_2O) is introduced to the working chamber, where a chemical reaction with the first layer takes place. This reaction results in the formation of a monolayer of the desired material (Al_2O_3). After that step, the working chamber must be evacuated again to remove all residuals of the used process gases. The whole process has to be repeated until the required layer thickness is deposited.

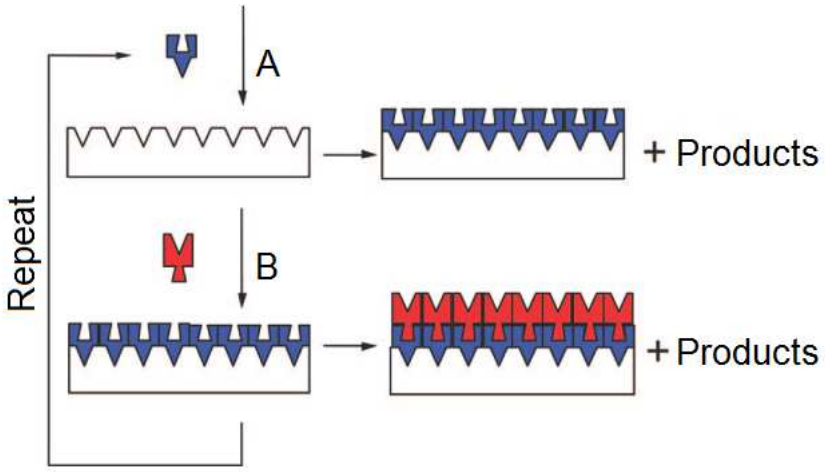


Figure 22: *Schematic process overview of the binary reaction sequence of an ALD process: By introducing process gas A into the working chamber, a monolayer composed of material A will be formed on the surface of the sample. After evacuation to remove all residuals of precursor A, precursor B is introduced to the working chamber, where a chemical reaction with the first layer takes place to form a monolayer of the desired material. In order to remove all residuals of the used process gases, the working chamber needs to be evacuated again. The whole process has to be repeated until the required layer thickness is deposited. Image taken from [62].*

3.2.2. NW harvesting and NW device integration

After the passivation of the Si wafer with the Ge NWs on top, a piece of approximately 2 x 2 mm^2 is cleaved and dispersed in iso-propanol. To harvest the NW from the substrate the iso-propanol solution with the Si growth substrate of Ge NWs was put into an ultrasonic bath. The sonic waves are cutting the wires on the bottom from the Si wafer piece. In order to integrate

these passivated Ge NWs into the base module, 4µL of the NW containing iso-propanol solution were drop-casted on the base module using a micropipette. During drop-casting, a continuous stream of N_2 was applied perpendicular to the small vertical trenches to achieve a high yield of NWs bridging the gap. The deposition process of the NWs was repeated until the NW density, located over the vertical trench on the base module was adequate. The density and orientation of the NWs was observed by using a light microscope.

3.2.3. Deposition of Al contacts

In the next step the TE test device can be prepared for the lithography for the sputtering of the Al contact pads.
In order to prevent the cantilevers from the mesa-pad structure from bending downwards during the spin-coating of the photoresist (AZ5214E), at first the trenches had to be filled with a LOR varnish (LOR 3A). It is necessary to use the LOR vanish before applying the photoresist, because the surface tension of photoresist hampers the resist to funnel into the trench and under the cantilevers. If the photoresist will be applied directly, without the forgoing LOR vanish, the weight of the resist will bend the cantilevers downwards and may lead to a major damage of the NWs. After the spin-coating of the LOR vanish and the photoresist, the TE test device is introduced to the MJB3 mask aligner from Karl Süss MicroTec AG, where it is exposed to UV light through a Cr photomask, which predefines the photolithographically structured outcome and subsequently developed in a solution (AZ726MIF). After this step the whole TE test device is covered with photoresist, except the contacts, which have been cleared during the developing process.
For better navigation on the TE test device, all fields of the checkerboard pattern grid have an assigned number starting in the top left edge with 1-1, where the first number represents the row and the second the column. The field to the bottom right side is assigned to the number 11-18, as there are 198 fields onto the TE test device. Figure 23 depicts an illustration of the TE test device prepared for Al sputter deposition, with the trenches filled by LOR vanish and developed photoresist (grey).

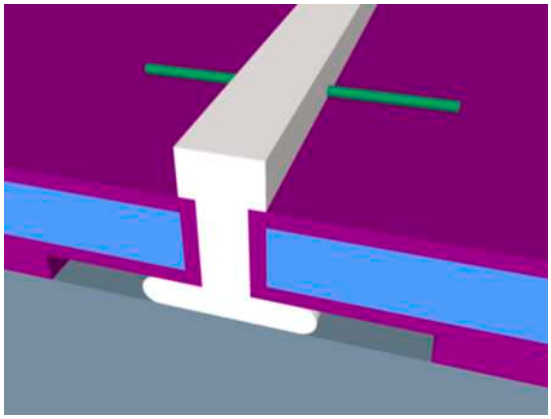


Figure 23: *Illustration of the TE test device prepared for Al sputter deposition. A NW (green) is located over a vertical trench, which is filled by LOR vanish (grey). Image taken from [60].*

Before the TE test device can be introduced into sputter deposition process, to ensure an electrical connection between the Ge NWs and the Al metallization, at first the passivation layer (Al_2O_3) and the native Ge-oxide layer of the NWs have to be removed by buffered oxide etching (BOE). In order to prior remove the Al_2O_3 passivation layer, a 1:7 buffered BHF dip was executed. Due to the photoresist layer the NW was only exposed to the BHF at the area where the Al will be deposited. Furthermore, when exposed to ambient air, Ge is forming a native oxide layer, consisting of germanium dioxide (GeO_2) and germanium monoxide (GeO). Because this native oxide layer avoids an electric contact between the Ge NW and the Al contacts, it has to be removed. While GeO_2 is soluble in water, the GeO layer requires an etching with hydroiodic acid (HI). To remove the native oxide layer of the Ge NWs, there was preformed a dip in a 14% diluted HI [66]. In an oxygen containing environment the native oxide layer of Ge is growing quite fast, therefor the TE test device was immediately introduced into the evacuated working chamber of the sputter system.
The sputter process was done with the VonArdenne LS320 S sputter system, featuring a 300W RF-powered sputter source. It is capable of holding up to 6 different sputter targets, with which multilayer deposition is possible. Furthermore, the system is equipped with reactive gas inlets and a substrate heater. The max. sample size of the system, is limited to 2” devices.
The VonArdenne LS320 S sputter system is working with a magnetron sputtering process, which is one of the most frequently used deposition tools for fabricating thin films. A schematic illustration of a magnetron sputter system is depicted in figure 24.
In a magnetron sputter system, the target and the sample holder are connected to opposing terminals of a high-voltage power supply, which permit the Argon (Ar) ions and the target atoms to move in a defined direction inside the

working chamber. The working chamber is usually a low-pressure environment, in order to increase the mean free path of the ejected target atoms, so they have a higher possibility to reach the substrate. By combing both a magnetic and electric field, magnetron sputtering is applied to enhance the ionization [67]. First of all, the working chamber has to be pumped, to remove all residual gases. The base pressure is in a 10^{-5}-10^{-6}mbar regime, and is accomplished by using a turbomolecular pump. When a set working pressure is reached, Ar is introduced to the working chamber and the high frequency generator is turned on to ignite the Ar plasma. Due to the plasma in the working chamber there is a working pressure of 8 * 10^{-3}mbar adjusted automatically. The ignition of the plasma triggers a gas discharge, which leads to a bombardment of the target material with high energetic Ar ions. Due to the bombardment atoms from the target material are ejected and subsequently moving to the substrate where they form a thin film consisting of the material of interest [68].

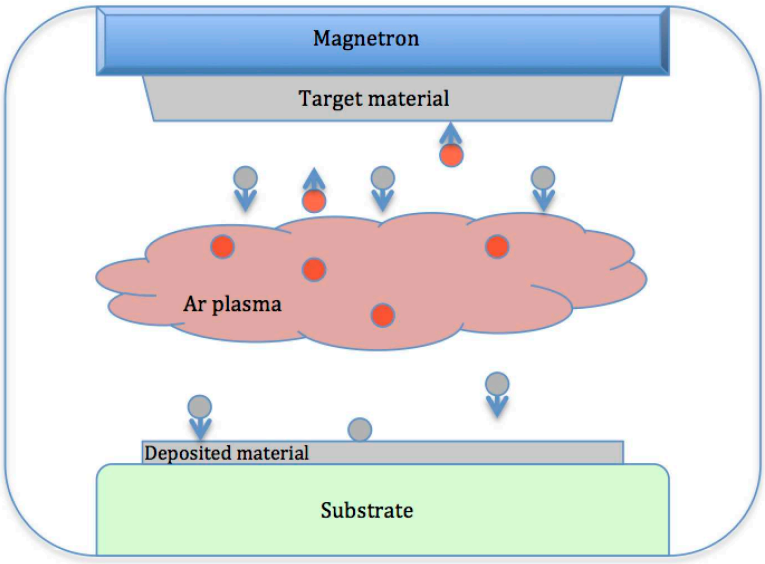


Figure 24: *Schematic illustration of magnetron sputtering: In the working chamber Ar plasma (red), whose ions are accelerated towards the target consisting of the material of interest (grey), where they eject atoms upon impact. As a result the ejected atoms from the target are moving to the substrate (green), and forming a deposition layer of a thin film consisting of the target material on the substrate.*

After the sputter deposition of the Al contact pads with a thickness of 200nm was completed, a lift-off process has to be done. The lift-off process was executed with dimethyl sulfoxide (DMSO) at a temperature of 363.15K, to remove the excess metal, the photoresist and the LOR vanish. Figure 25 depicts

a SEM image of the TE test device with the Al contacts and the macroscopic Al contact pads.

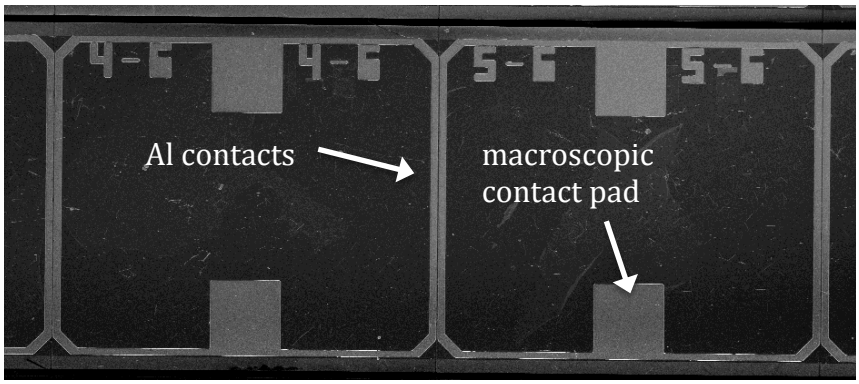


Figure 25: TE test device with Al contacts and macroscopic Al contact pads. Image taken using the Zeiss NEON 40Esb CrossBeam.

3.2.4. Formation of Al-Ge-Al heterostructured NWs

After the Ge NWs were successfully contacted with the Al contact pads, the fabrication of the Al-Ge-Al heterostructured NWs can be done. The formation of the heterostructure was achieved by thermal induced substitution of Ge by Al. The controlled diffusion process was activated by an annealing process conduced in a rapid-thermal-annealing (RTA) system. The main reason why RTA was used for the diffusion process, is the high rate at which the temperature can be ramped up, which leads to relatively short processing times in the order of seconds to minutes.
The used RTA system is a UniTemp UTP 1100 RTA oven, which uses 18kW infrared lamps, with which the system can achieve a maximum temperature of 1200K and maximum ramp up rates of up to $75Ks^{-1}$ [69]. The oven of the system consists of a quartz chamber and can be hermetically sealed. The system is capable of handling up to 4" wafers, manually loaded through a quartz tray. To ensure a clean and well controllable process area, the quartz chamber is evacuated prior to the actual RTA process and subsequently purged with nitrogen and forming gas. After this mandatory cleaning process a user-defined RTA routine can be executed. Subsequently the chamber was heated to a temperature of 673K to ensure a stable diffusion process. For a controlled stopping of the diffusion process, the temperature of the oven is rapidly ramped down assisted by flushing the chamber with nitrogen. The average diffusion rate of Al into Ge NWs appeared to depend on the diameter and

surface roughness of the NWs and was experimentally determined between 2.5nms^{-1} and 4nms^{-1}.
To verify the fabricated length of the Ge segment in the Al-Ge-Al heterostructured NWs, a scanning electron microscopy (SEM) was used. Figure 26 depicts an image taken with the Zeiss NEON 40Esb CrossBeam, from a fabricated Al-Ge-Al heterostructured NW.

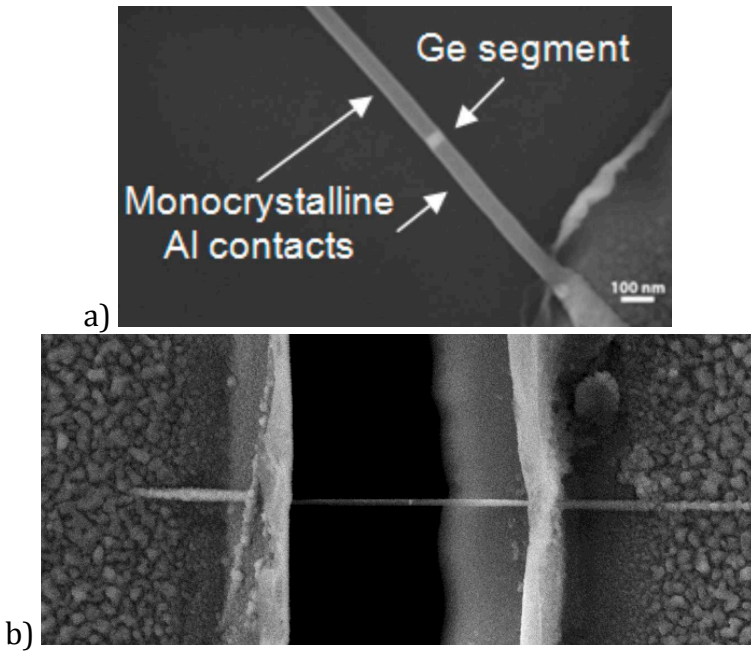


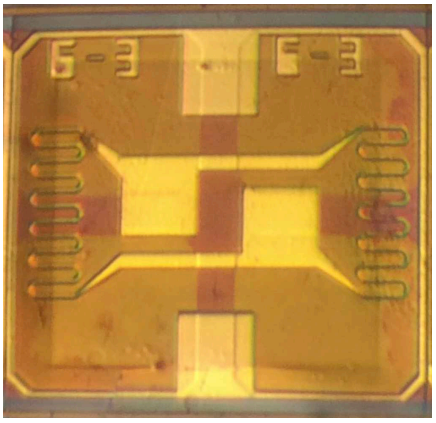
Figure 26: SEM image of an a) Al-Ge-Al heterostructured NW located on a Si substrate, b) Al-Ge-Al heterostructured NW located over a vertical trench. Image taken using the Zeiss NEON 40Esb CrossBeam.

3.2.5. Fabrication of the resistive Au heater

As a last step the Au heater has to be integrated. The Au heater is produced more or less in the same way like the Al contacts, with the help of photolithography, subsequently followed by a sputter deposition process, in combination with a lift-off process. In order to do so, at first the trenches of the TE test device has to be filled up with LOR vanish (LOR 3A). After the TE test device is spin-coated with LOR vanish, it can be spin-coated with photoresist (AZ5214E). Subsequently the TE test device is exposed to UV light trough a Cr photomask, which defines the structure of the Au heater. After that, the TE test device is developed in a solution (AZ726MIF), to get rid of the resist on the desired areas. The photolithography process was conducted by using the MJB3

mask aligner from Karl Süss MicroTec AG. After the photolithography process, the TE test device can be introduced to the Au sputter deposition process. The sputter deposition process was done again with the VonArdenne LS320 S sputter system, with which a thickness of 180nm Au was deposited onto a 5nm adhesion layer of Ti. After the deposition process a lift-off process has to be done. The lift-off process was executed again with DMSO at a temperature of 363K, to remove the excess metal, the photoresist and the LOR vanish. Figure 27 depicts a single mesa-pad of the TE test device with the Au heater structure with macroscopic connection pads on it (a) and a CAD drawing of the used Cr photomask for the heater structure (b).

a)



b)

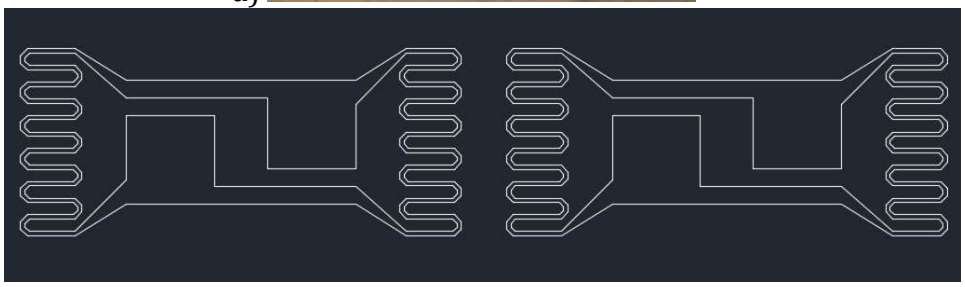


Figure 27: *a) Single mesa-pad of the TE test device with a deposited Au heater structure with macroscopic contact pads. Image taken with light microscope. b) CAD drawing of the Cr photomask for the heater structure.*

After the successful production of the Au heater the TE test device has to be examined with a SEM to find suitable NWs for electrical characterization. The examination was done by using the Zeiss NEON 40Esb CrossBeam. Suitable NWs have to show a Ge segment in the middle of the wire. Furthermore, the investigation has to be done to categorize the NWs in their position, length and diameter. Because of the randomness of the drop-cast process, with which the NWs where introduced to the TE test device, it is possible to find more than one wire between two mesa-pads of the TE test device. This makes a clear electrical

characterization impossible, because current will flow through both wires in a parallel circuit configuration. Therefor it is mandatory that a characterised wire is located with out any artefacts between two mesa-pads. If there is more then one wire between two mesa-pads, it has to be ensured that only one that should be measured will remain. The termination of the artefacts is executed by vaporization with a high-energy laser (40µW). Figure 28 shows a light-microscope image of two mesa-pads of a completed TE test device.

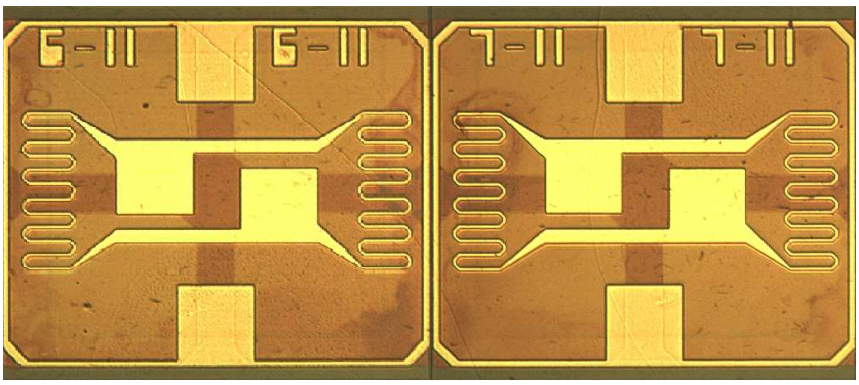


Figure 28: Two mesa-pads of the completed TE test device, in which between one NW should be suspended. Image taken with a light-microscope.

After all suitable NWs have been located, theirs electrical functionality have to be checked. To control the electrical contact a needle probe station in combination with the HP 4156B Precision Semiconductor Parameter Analyzer was used.

3.3. Experimental setup – evaluation of the electric and thermoelectric properties

The final TE test device design consists of an Au heater structure and a resistive Al thermometer, mirrored at the middle of the nanowire. To characterize the electric and thermoelectric properties of the NWs a needle probe station will be used to connect the macroscopic contact pads of the TE test device with the measurement devices. Special care had to be taken to protect the NWs from ESD, which may lead to immediate melting induced failure due to Joule heating. Due to their low resistivity, Al NWs were especially sensitive to ESD and had to be handled with extreme caution.

3.3.1. Electrical characteristics

All measurements were performed with a needle probe station. In addition to minimize the influence of electromagnetic fields as well as ambient light on the TE test device during the measurement, the needle probe station was placed into a dark box. The electrical measurements were realized by using the HEWLETT PACKARD (HP) 4156B Precision Semiconductor Parameter Analyzer in combination with two independent source measure units (SMUs) using two needle probes. To ensure a precise established connection between the macroscopic Al and Au pads with the needle probes, a stereoscope was used. Figure 29 depicts a photo of the used needle probe station in combination with the dark box, as well as a rack on the right hand side, where the HP 4156B Precision Semiconductor Parameter Analyzer, the TTi EL302P PROGRAMMABLE PSU and the two-channel KEITHLEY 2612A SYSTEM SourceMeter are located. The TTi EL302P PROGRAMMABLE PSU was used to power the heater and the two-channel KEITHLEY 2612A SYSTEM SourceMeter was used to monitor the temperature gradient along the NW. A detail explanation of the general measurement procedure can be found in chapter 3.3.6.

Figure 29: Photo of the used needle probe station which is located in a dark box. On the right hand side there can be seen a rack where the HP 4156B Precision Semiconductor Parameter Analyzer, the two-channel KEITHLEY 2612A SYSTEM SourceMeter and the TTi EL302P PROGRAMMABLE PSU are located (marked with red squares).

All measurements were carried out at room temperature and ambient atmosphere, as 2-point (2T) measurements.

3.3.2. I/V characteristic

In order to measure the current-voltage (I/V) characteristic of an Al-Ge-Al heterostructured NW, one needle was set on the macroscopic Al contact pad on each side of the NW, which will be later referred to as source and drain contact. One of the two contacts (drain) was forced to ground level, while the other one (source) was swept from [-1 ; +1] V and [-0.10 ; +0.10] V, the source-drain current was measured accordingly using the HP 4156B Precision Semiconductor Parameter Analyzer. Figure 30 depicts a measurement of the I/V characteristic from [-1 ; +1] V, of a 48nm thick and 4.3µm long wire with a 720nm long Ge segment, at room temperature.

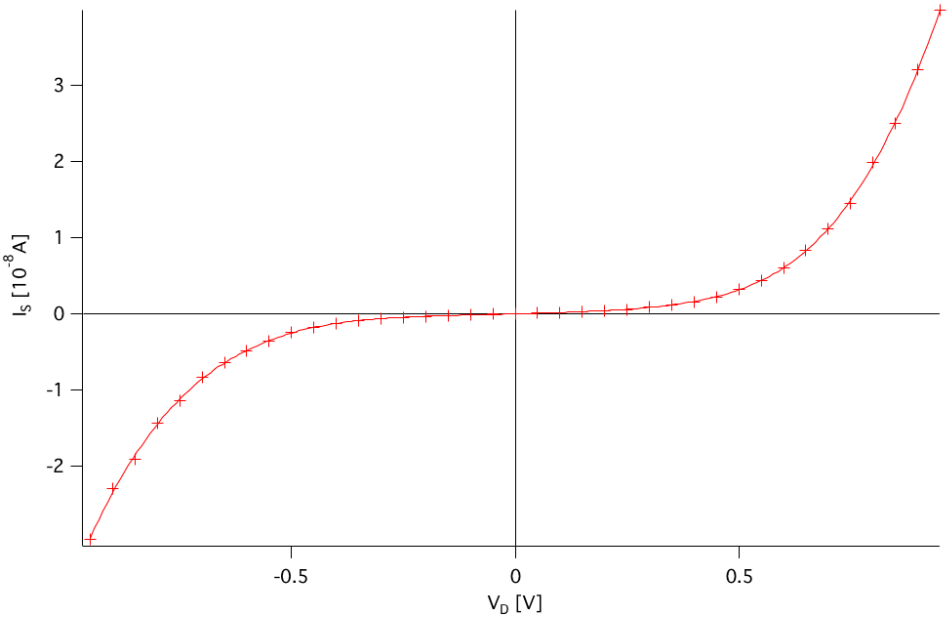


Figure 30: I/V characteristic of an 48nm thick and 4,3µm long Al-Ge-Al heterostructured NW, with a 720nm long Ge segment, measured at room temperature.

In addition, the resistivity of the measured NW can be determined by the slope of the I/V characteristic line, and the specific dimensions of the NW as represented in equation 22.

$$\rho = R_\Omega \cdot \frac{A}{L} \tag{22}$$

In equation 22 the specific dimensions are given by, A which represents the cross section and L the overall length of the NW. ρ represents the specific resistance and R_Ω the ohmic resistance. Since only 2T measurements were performed, it has to be taken into account that the measured data contains parasitic contact series resistance. The serial resistance is consisting of the Al contacts and the Al-Ge-Al heterostructured NW, consisting of mono-crystalline Al leads contacting the Ge segment.

3.3.3. Calibration of resistive Al temperature sensor

Since thermoelectric elements are strongly dependent on the temperature, it is mandatory to have an accurate determination of the thermal gradient over the NW. To measure the temperature gradient along the NW, a resistive thermometer was used on each side. These thermometer was realized with the Al contacts of the NW. Due to the temperature dependent resistance of Al, it can be used as an accurate temperature sensor when it is calibrated correctly. To calibrate the Al temperature sensor, at first the whole TE test device was heated up from approximately 303K to 373K in steps of 10K. The heating process was realized with an external heater element located below the TE test device. To have a precise reference temperature sensor, a PT100 element was placed on the top of the ceramic plate beside the TE test device. Figure 31 depicts a photo of the external heater element located between two white ceramic plates, powered via the two black cables, and the PT100 element on the top with the two white connection lines to measure its resistance.

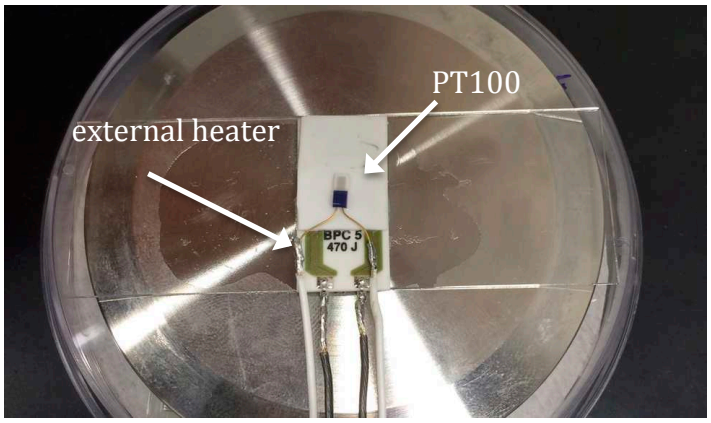


Figure 31: External heater (brown) between two ceramic plates and a PT100 element (blue) on top.

The PT100 element is a calibrated temperature sensor, which measures temperature due to resistance changes. The resistance of the PT100 was measured with a Keithly 2612A SYSTEM SourceMeter. Once the actual resistance of the PT100 is known, one can compare the value to a table to find the proper temperature. Table 2 represents the values for the PT100 from 303K to 373K in 10K steps.

Temperature [K]	303	313	323	333	343	353	363	373
Resistance [Ω]	111.88	115.81	119.73	123.64	127.54	131.42	135.50	139.16

Table 2: Temperature dependence of the resistance from the PT100 temperature sensor. Adapted from [70].

During the ramping of the temperature in 10K steps, two needle probes were placed to the Al contact pads and an I/V curve was measured with the HP 4156B Precision Semiconductor Parameter Analyzer. The I/V curve was monitored in a range of [-5 ; +5]mV, in addition a compliance of 100µA was set, to prevent the wire from destroying due to any over current. Hence, each of the 8 measured I/V curves represent a certain temperature of the TE test device. Exemplarily two of them at T = 303K and T = 373K, are depicted in figure 32.

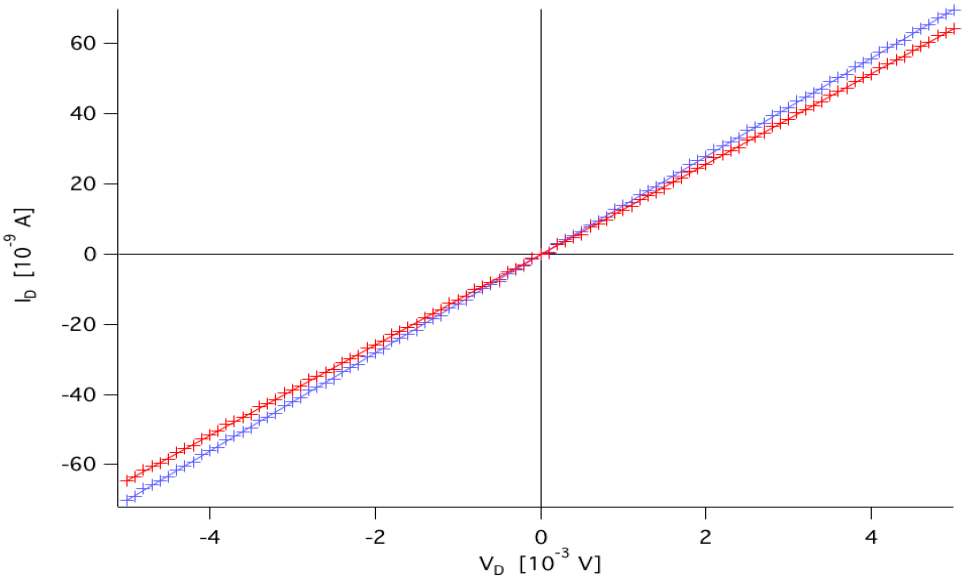


Figure 32: I/V curves of the Al temperature sensor measured at T = 303K and T = 373K.

The slope in figure 32 represents the reciprocal resistance of the Al temperature sensor. Figure 33 depicts the temperature dependence of the resistance of the Al temperature sensor. Furthermore, a linear fit was executed to calculate an accurate value of the slope.

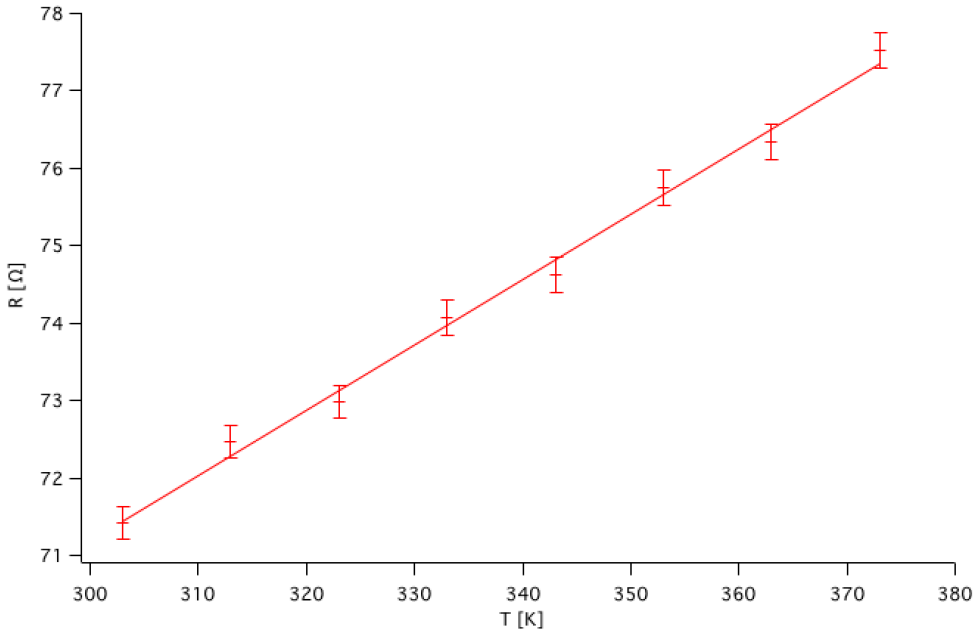


Figure 33: Temperature dependence of the resistance R of the Al temperature sensor. Resistance R vs Temperature T.

After the calculation of the slope of 87 mΩ/K, the Al temperature sensor is fully calibrated, and the temperature of each side of the wire can be determined, and thereby the temperature gradient along the NW.

3.3.4. Temperature gradient along the NW (Au heater structure)

The temperature gradient along the NW was achieved by implementing a Au heater structure on each side of the wire (see figure 28). To achieve a temperature gradient along the wire, only one heater is needed. To determine the temperature gradient, the temperature on both sides of the NW was measured with the resistive Al temperature sensor.

3.3.5. Determination of the Seebeck coefficient

The determination of the thermo-voltage was done analysing the shift of the I/V characteristic line. An I/V curve was measured each temperature step at equilibrium. Thermal equilibrium was assumed, 2 minutes after the temperature on the heated side has reached the set value. This measurement technique was performed following the work of [71, 72]. To exemplify the desired outcome of this measurement procedure figure 34 depicts an I/V characteristic for a heavily doped Si NW. At this example the applied heating voltage was modified in 1V steps from 0 to 4V, accordingly. As can be seen in the inset, the intersection at $I_D = 0$ shifts with applied thermal bias. This enables to identify V_{th} for each heating voltage.

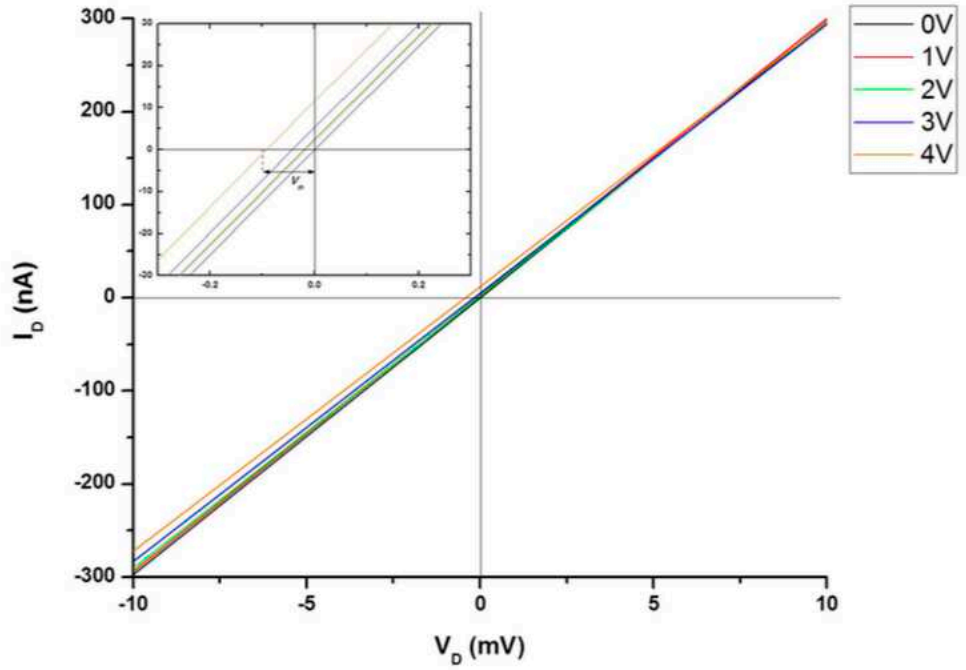


Figure 34: *I/V characteristics for a heavily doped silicon NW for 4 different heating voltages applied. Inset: Zoom in on the intersection at $I_D = 0$ and marking of thermo-voltage V_{th} for $V_{Heat} = 4V$ on one side of the wire. Image taken from [73].*

3.3.6. General measurement procedure

For the measurement procedure overall 6 needle probes have to be placed on the TE test device. Figure 35 depicts a circuit layout with two mesa-pads of the TE test device. The 6 needle probes where labelled from 1 to 6.

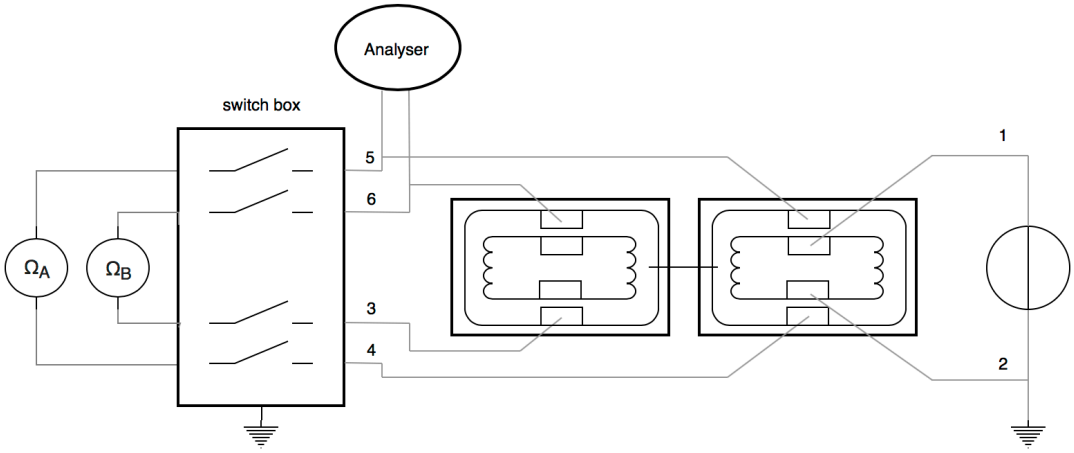


Figure 35: *Schematic circuit layout of the general measurement procedure*.

The actual measurement procedure is divided in 4 steps listed below. At first one side of the NW was heated with the Au heater, to create a temperature gradient ΔT along the NW. After two minutes, to ensure the temperature is stable, ΔT can be determined. As a next step an I/V characteristic can be acquired according to the ΔT. At last the next heating step can be preapared.

Heating
Needle probe 1 and 2 were placed on the two macroscopic contact pads of the Au heater on one side of the wire. These two needle probes were connected to the TTi EL302P PROGRAMMABLE PSU. With this power supply unit a certain power can be supplied to the heater to heat preferably one side of the NW.

Determination of the temperature gradient ΔT
To determine the temperature gradient ΔT along the NW, the temperature on both sides of the NW has to be measured. To measure the temperature on one side of the NW, two needle probes were placed on the two macroscopic Al contact pads on one side of the NW. These two needle probes were connected via a switch box to the two-channel KEITHLEY 2612A SYSTEM SourceMeter. The switchbox consist of simple switches, which are capable of closing or opening the circuit between the needle probes and the SourceMeter. This SourceMeter has two channels A and B, to measure two values at the same time. With this instrument the resistance of the Al and respectively the

temperature on one side of the NW can be measured (chapter 3.3.3). When the temperature is measured all switches of the switch box have to be set to GND (closed). A photo of the switch box is depicted in figure 36. As depicted in figure 35, needle probe 4 and 5 were placed to the Al contacts on the right side of the NW and needle probe 3 and 6 were placed to the Al contacts on the left side of the NW.

I/V characteristic

To measure the I/V characteristic of the NW at a certain ΔT, needle probe 5 and 6 were used. These needle probes are forked before their connection to the switch box and were connected via two SMUs to the HP 4156B Precision Semiconductor Parameter Analyzer. Before one can measure the I/V characteristic of the NW, all switches of the switch box have to be set to OPEN. Now both channels of the SourceMeter are disconnected and an I/V characteristic of the NW can be acquired. The I/V curve was captured in a range from [-10 ; +10]mV and a compliance of 100µA was set.

Preparation of the next heating step

Before the next heating step can be initialized, the measurement of the I/V characteristic has to be completed and all switches of the switch box have to be set to GND. Then both channels of the SourceMeter are connected and therefor the temperature gradient along the NW can be monitored again.

Figure 36: *Photo of the switchbox, labeled the connections on top with 3 to 6 (measurement lines) and on bottom A and B for the two-channel SourceMeter to measure the temperature gradient along the NW.*

4. Results and Discussion

This chapter presents all important results regarding the manufacturing of the base module, the preparation of the TE test device, the formation of the Al-Ge-Al heterostructured NWs, and the corresponding electrical and thermoelectric characterization at room temperature and ambient atmosphere.

4.1. Ge NW synthesis

The Ge NWs were manufactured according to the VLS growth mechanism. The Ge NWs have been provided by the former PhD student Clemens Zeiner at TU Vienna and have an average diameter of 50nm and a length of about 8µm. Because the Ge naturally reacts under ambient condition with the oxygen, which will negatively effect the electrical properties of the NWs, a passivation layer of 10nm Al_2O_3 was deposited with ALD. Furthermore the passivation of the NWs not only prevents them from oxidation, it also improves the mechanical stability and makes it more sustainable.
For further use of the NWs they have to be harvested form the Si substrate. The harvesting was done by dissolving the Si substrate in iso-propanol and subsequently introduced into an ultrasonic bath. After this process the passivated Ge NWs are disconnected from the Si substrate and a solution of iso-propanol and Ge NWs has been formed. This solution will be used to introduce the Ge NWs onto the TE test device via a drop-cast process. Figure 37 depicts a Ge NW with an Al_2O_3 passivation layer, drop-casted onto a Si substrate.

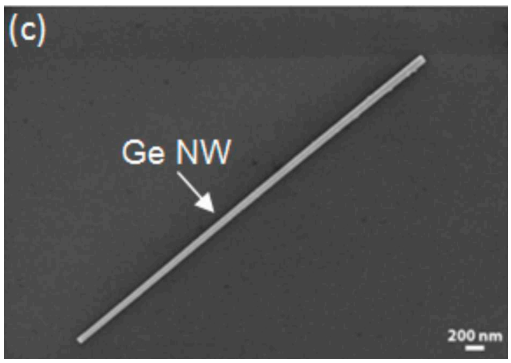


Figure 37: Ge NW grown via the VLS mechanism and coated with an Al_2O_3 passivation layer via ALD and drop-casted onto a Si substrate. Taken from [63].

4.2. Manufacturing of the base module

The base module is fabricated using a SOI substrate with a 500µm thick HL, a DL of 3µm and a BOX layer thickness of 1µm diced into squares of 12 x 12 mm². It has a total of 180 mesa-pads separated by vertical trenches. The width of the vertical trenches is 1µm and thereby small enough to support fixation of NWs aligned horizontally during the integration process (see chapter 3.2.2). Furthermore the mesa-pads have a 60µm undercut. In addition after the trench etching processes a thermal wet oxidation process is executed to grow a 300nm thick $Si0_2$ layer. Figure 38 shows an illustration of a vertical trench on the left side and an optical image of a single undercuted mesa-pad on the right side.

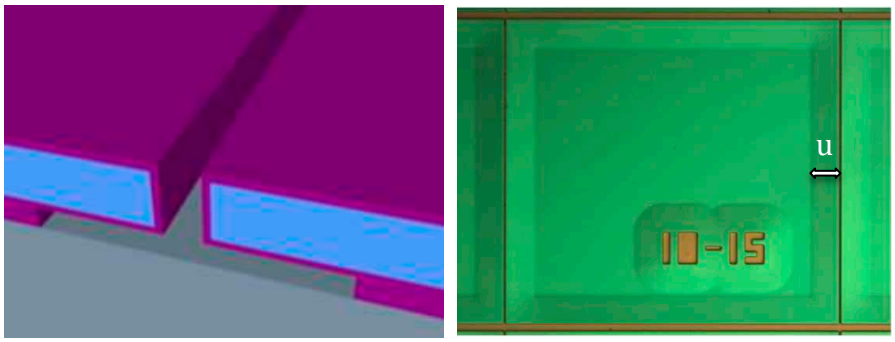


Figure 38: Left side: Illustration of a vertical trench with an undercut. The Si DL is blue and the SiO_2 layer is purple. Right side: Differential interference contrast light-microscope image of an individual mesa-pad with 300 x 300 µm² and with a vertical trench width of about 1µm and an undercut u of about 60µm. The horizontal separation of the pads is 10µm. Taken from [60].

4.3. Preparation of the TE test device

First of all the Ge NWs with the Al_2O_3 passivation layer have to be integrated onto the base module via a drop-cast process. After the wires are deposited on the TE test device, they have to be electrically connected to ensure a macroscopic connection for electric and thermoelectric characterisation. Using photolithography in combination with a sputter deposition process, 200nm thick Al contacts with a macroscopic connection pads were formed (see chapter 3.2.3). Figure 39 depicts a SEM image of the TE test device with connected NWs and the macroscopic Al contacts.

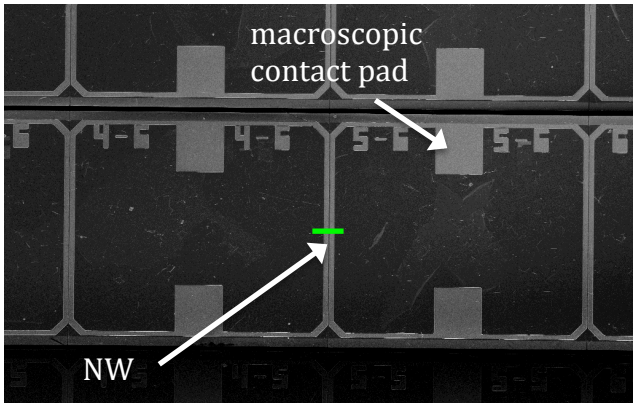


Figure 39: SEM image of the TE test device. Al contact with macroscopic contact pads (grey). A NW is symbolized with a green bar.

4.4. Formation of Al-Ge-Al heterostructured NWs

After the electrical contacting of the Ge NWs with Al contacts, the formation of the Al-Ge-Al heterostructured NWs can be initiated. The formation of the heterostructure was achieved by thermal induced substitution of Ge in the NWs by Al from the contacts. To accomplish a controlled diffusion process, an annealing process was executed. The annealing process was realized with an RTA system at a temperature of 673K. To realize specified length of the Ge segment, the annealing temperature and time is decisive. Furthermore, the average diffusion rate of Ge into Al is depending on the geometry and the surface roughness of the NW, and was experimentally determined between $2.5 nms^{-1}$ and $4 nms^{-1}$. After the formation process of the Al-Ge-Al heterostructured NWs, the TE test device has to be investigated with a SEM to determine the length of the Ge segment of each NW. However, this annealing process leads to a heterostructured NW of Al-Ge-Al with a pure Ge segment, connected via a sharp atomic interface with mono-crystalline Al. Figure 40 depicts a SEM image of an Al-Ge heterostructures interface.

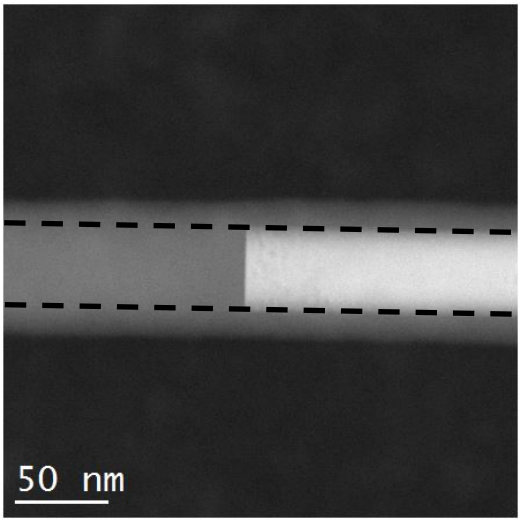


Figure 40: SEM image of an Al-Ge heterostructure. The pure Ge segment (light-grey) is connected with monocrystalline Al (dark-grey), surrounded by an Al_2O_3 passivation layer (separated by the dashed line). Taken from [52].

4.5. Manufacturing of the heater structure

The heater structure is implemented on each mesa-pad to be able to create a temperature gradient along each NW on the TE test device. The heater structure is produced employing photolithography process, followed by a sputter deposition of 180nm Au onto a 5nm adhesion layer of Ti. The heater structure also shows macroscopic connection pads. Figure 41 depicts one mesa-pad of the TE test device with a Au heater structure.

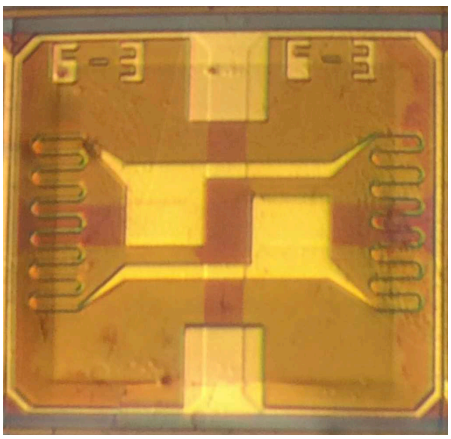


Figure 41: Light-microscope image of a complete mesa-pad with a Au heater structure and Al contacts.

4.6. Electric and thermoelectric characterization

To perform a proper electric and thermoelectric characterisation of the TE test device, needle probes had been placed on the macroscopic contact pads of the Al contacts and the Au heater. Overall 6 needle probes have been used. The needle probe station was located in a dark box to minimise the influence of electromagnetic fields as well as ambient light on the device during the measurement. The measurement instruments involved were a HEWLETT PACKARD (HP) 4156B Precision Semiconductor Parameter Analyzer in combination with two independent source measure units (SMUs) and a two-channel KEITHLEY 2612A SYSTEM SourceMeter. In addition to drive the Au heater structure a TTi EL302P PROGRAMMABLE PSU was used. All measurements were carried out at room temperature and ambient atmosphere, as 2T measurements. A general measurement procedure explained in detail can be found in capture 3.3.

4.7. Basic electric characterization

Figure 30 shows a non linear I/V characteristic of a typical Al-Ge-Al heterostructured NW. The non linearity is an effect of Schottky contacts. The electrical conductivity σ is the inverse specific resistance and can be calculated using equation (22). The electrical conductivity of a Ge segment with a length of about 720nm and a cross-section of about 1808nm^2 is about 0.2Sm^{-1} at 300K. In comparison, Ge bulk material exhibits an electrical conductivity of about 2Sm^{-1} [43].

4.8. Determination of the Seebeck coefficient

Figure 42 depicts the I/V characteristic of an Al-Ge-Al heterostructured NW with a thickness of 48nm, a length of 4.3µm and a Ge segment length of 720nm. It shows how the thermo-voltage V_{th} is determined from the I/V characteristic line, as described in capture 3.3.5. To do so, the applied heat voltage was modified in 0.5V steps from 1.5V to 4V. As can be seen in figure 42, the intersection at I_D = 0A shifts with the applied thermal bias to the right. This shift represents the thermo-voltage V_{th} for each temperature gradient [71, 72].

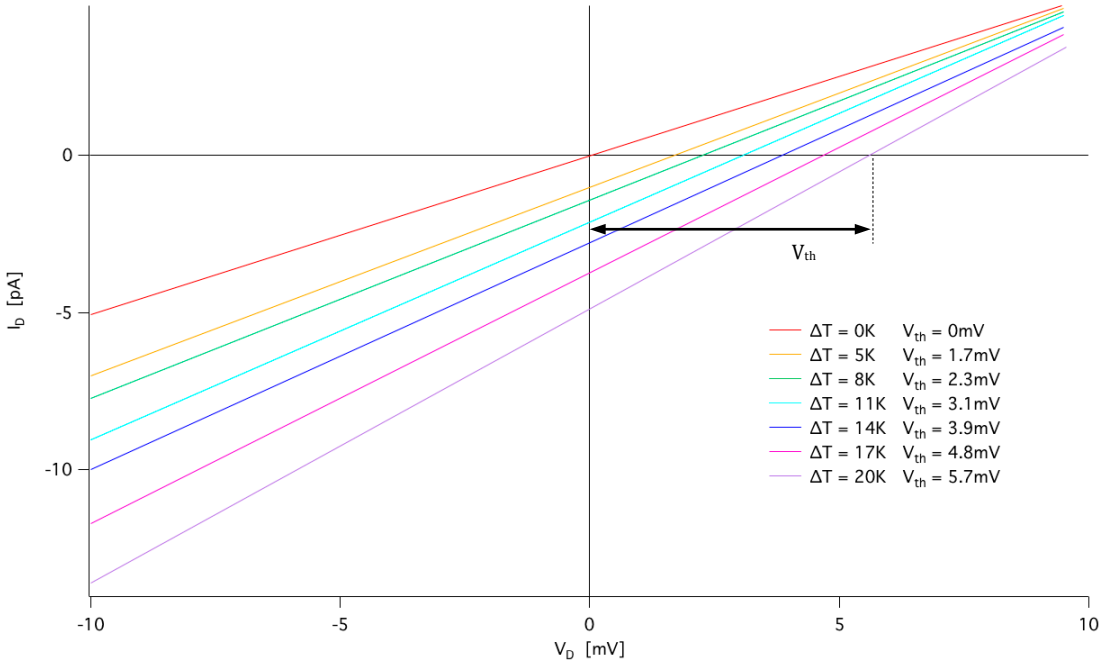


Figure 42: I/V characteristic of an Al-Ge-Al heterostructured NW with a thickness of 48nm, a length of 4.3µm and a Ge segment length of 720nm, showing a thermo-voltage V_{th} due to applied temperature gradient ΔT.

To get a better impression of how the thermo-voltage V_{th} is connected with the temperature gradient ΔT, figure 43 depicts the thermo-voltage V_{th} as a function of the temperature gradient ΔT. One can see that the thermo-voltage V_{th} has a linear dependence on the temperature gradient ΔT, as expected.

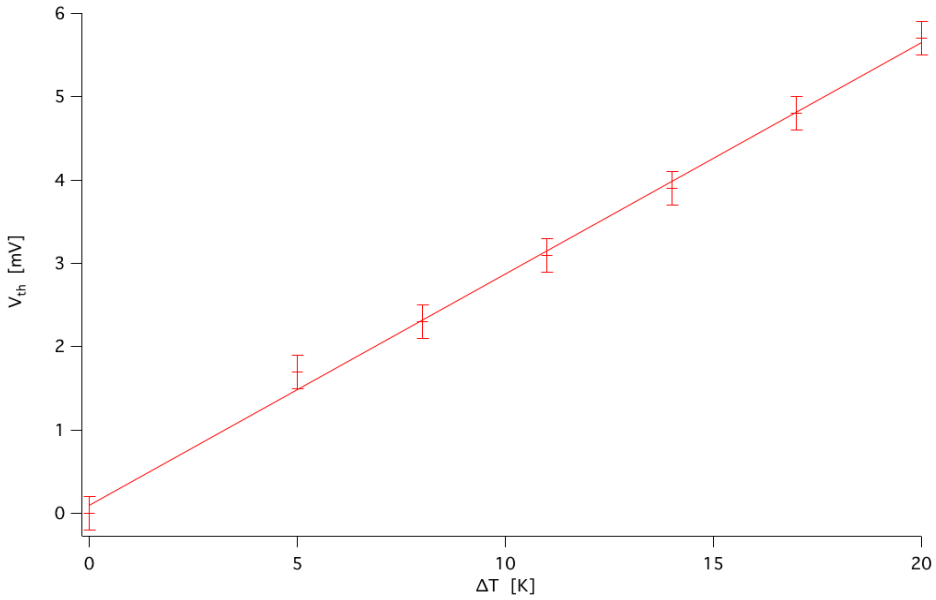


Figure 43: Thermal voltage as a function of the temperature gradient ΔT.

Furthermore, by the use of equation (19) the thermo power (differential Seebeck coefficient) can be calculated. Figure 44 depicts the calculated thermo power α for each temperature gradient ΔT.

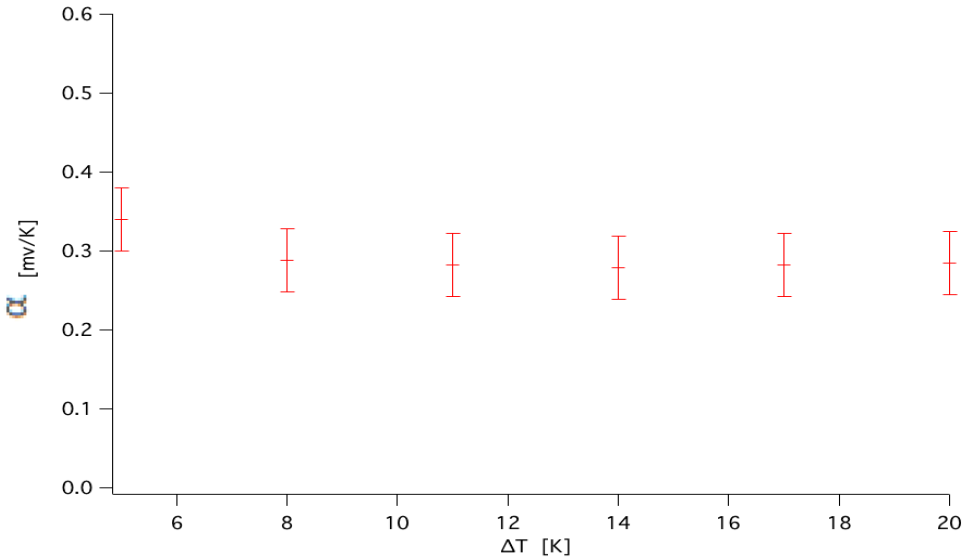


Figure 44: Calculated thermo power α for each temperature gradient ΔT.

The mean of the calculated thermo power α for the Al-Ge-Al heterostructured NW with a thickness of 48nm, a length of 4.3µm and a Ge segment of 720nm is α = 0,293 mV/K and shows a standard deviation of 15,6µV/K.

4.9. Determination of the figure of merit

The figure of merit is calculated using equation (20) and a thermal conductivity κ for Ge bulk material, which is about 60$Wm^{-1}K^{-1}$ [43]. By taking into account that the thermal conductivity for NWs is predicted to be much smaller [74] the calculated ZT represents a lower boundary and is about 4.8 * 10^{-3}. Although the thermo power α is comparable with that one from bulk Ge [43] the ZT is rather small. This can be explained by the much lower charge carrier mobility of NW [75] and thereby a much lower σ compared to bulk material.

5. Conclusion and Outlook

Mono-crystalline Ge wires with an average diameter of about 50nm and Al contacts have been successfully used to produce quasi one-dimensional Al-Ge-Al heterostructured NWs with an average length of 4.3µm. The formation of the heterostructure was accomplished with a thermal induced diffusion process at 675K executed via a RTA process. The length of the Ge segment can be controlled with the time and temperature of the Al-Ge exchange process, while a diffusion rate was experimentally determined between 2.5nms^{-1} and 4nms^{-1}, depending on the wire geometry and surface roughness.

Furthermore a TE test device has been designed for proper handling of the NWs. It consists of a 12x12mm^2 Si wafer with a checkerboard pattern grid with 180 fields. Each field is separated by the next with vertical trenches of about 1µm and horizontal trenches of about 10µm. The fields have a 60µm undercut and form a mesa-pad structure. The TE test device basically allows the material of interest, to be measured suspended from one mesa-pad to another. Measuring a material of interest in a suspended condition brings several advantages, like avoiding trapping effects and achieving a higher temperature gradient along the material of interest. It is capable of providing the Al-Ge-Al heterostructured NWs with macroscopic Al contact pads, to allow a connection via a needle probe station to external measurement instruments. Furthermore the TE test device comes up with a Au heater structure on each side of the NW to generate a temperature gradient up to 20K along the Al-Ge-Al heterostructured NWs.

The results of this work show that with an Al-Ge-Al heterostructured NW with a diameter of 48nm, a length of 4.3µm and a Ge segment length of 720nm a thermo power of 0,293 mV/K with a standard deviation of 15,6µV/K can be achieved. This measurement paved the way for a lot of possible projects in the future. It is to expect that with a shorter Ge segment, especial under 50nm, a much higher thermo power can be achieved, due to ballistic transport [64]. Furthermore, the measurements can be executed while the Al-Ge-Al heterostructured NW experiences a strain along its wire axis. This could be interesting because Ge changes its resistivity by deforming its energy band structure, while it experiences a strain [62].

6. Reference

[1] K. Rupp and S. Selberherr, “The Economic Limit to Moore’s Law,” in IEEE Transactions on Semiconductor Manufacturing, vol. 24, pp. 1–4, IEEE, (2011)

[2] G. E. Moore, “Cramming more components onto integrated circuits (Reprinted from Electronics, pg 114-117, April 19, 1965),” Proceedings Of The IEEE, vol. 86, pp. 82–85, Apr. 1998.

[3] L. B. Kish, “End of Moore’s law: Thermal (noise) death of integration in micro and nano electronics,” Physics Letters, Section A: General, Atomic and Solid State Physics, vol. 305, no. 3-4, pp. 144–149, 2002.

[4] V. V. Zhirnov, V. V. Zhirnov, I. I. I. Ralph K. Cavin, I. I. I. Ralph K. Cavin, J. a. Hutchby, J. a. Hutchby, G. I. Bouriano , and G. I. Bouriano , “Limits to Binary Switch Scaling—A Gedanken Model,” in Proceedings of the IEEE, vol. 91, pp. 1934–1939, Nov. 2003.

[5] J. R. Powell, “The quantum limit to Moore’s law,” in Proceedings of the IEEE, vol. 96, pp. 1247–1248, IEEE, Aug. 2008.

[6] C.H. Bennett, D.P. DiVincenzo, “Quantum information and compution”. In Nature 404,247-255 (2000). doi: https://doi.org/10.1038/35005001

[7] H. J. Goldsmid. Introduction to Thermoelectricity. 2nd ed. Berlin, Heidelberg: Springer- Verlag, 2016, pp. 339–357. ISBN: 978-3-662-49255-0.

[8] Snyder, G.J. (2017). "Figure of merit ZT of a thermoelectric device defined from materials properties". Energy and Environmental Science. 10: 2280. doi:10.1039/C7EE02007D.

[9] T. H. Geballe and G. W. Hull. “Seebeck effect in silicon”. Phys. Rev. 98.4 (1955), pp. 940–947.

[10] G. Pennelli and M. Macucci. “Optimization of the thermoelectric properties of nanos- tructured silicon”. In: J. Appl. Phys. 114.21 (2013).

[11] W. Liu, K. Etessam-Yazdani, R. Hussin, et al. “Modeling and Data for Thermal Conductivity of Ultrathin Single-Crystal SOI Layers at High Temperature”. In: IEEE Trans. Electron Devices 53.8 (2006).

[12] J. Yu, S. Mitrovic, D. Tham, et al. “Reduction of thermal conductivity in phononic nanomesh structures”. In: Nat Nanotechnol. 5 (2010), pp. 718–721.

[13] J. H. Lee and J. C. Grossman. “Thermoelectric properties of nanoporous Ge”. In: Appl. Phys. Lett. 95.1 (2009), pp. 93–96.

[14] N. Mingo, L. Yang, D. Li, et al. “Predicting the Thermal Conductivity of Si and Ge Nanowires”. In: Nano Lett. 3.12 (2003), pp. 1713–1716.

[15] T. Burchhart, A. Lugstein, C. Zeiner, Y. J. Hyun, G. Hochleitner, and E. Bertagnolli. Nanowire-metal heterostructures for high performance MOSFETs. Elektrotechnik und Informationstechnik, 127(6):171–175, 2010. ISSN 0932-383X. doi: 10.1007/ s00502-010-0739-9.
URL http://dx.doi.org/10.1007/s00502-010-0739-9.

[16] C. Cho, C.O. Aspetti, J. Park, and R. Agarwal. Silicon coupled with plasmon nanocavities generates bright visible hot luminescence. Nat Photon, 7(4):285–289, Apr 2013. ISSN 1749-4885.
doi: 10.1038/nphoton.2013.25.
URL http://dx.doi. org/10.1038/nphoton.2013.25.

[17] J.Greil, S. Birner, E. Bertagnolli, and A. Lugstein. Nanowires enabling strained photovoltaics. Applied Physics Letters, 104(16):163901, 2014.
doi: http://dx.doi.org/10. 1063/1.4871458.
URL:http://scitation.aip.org/content/aip/journal/apl/104/16/10.1063/1.4871458.

[18] A. Cao, E. Sudhölter, and L. de Smet. Silicon nanowire-based devices for gasphase sensing. Sensors, 14(1):245, 2013. ISSN 1424-8220.
doi: 10.3390/s140100245.
URL http://www.mdpi.com/1424-8220/14/1/245.

[19] Y. Wu and P. Yang. Germanium nanowire growth via simple vapor transport. Chemistry of Materials, 12(3):605–607, 2000. doi: 10.1021/cm9907514.
URL http: //dx.doi.org/10.1021/cm9907514.

[20] Heon-Jin Choi, Springer-Verlag Berlin Heidelberg 2012, "Vapor-Liquid-Solid Growth of Semiconductor Nanowires" : https://www.google.at/url?sa=t&rct=j&q=&esrc=s&source=web&cd=3&ved=2ahUKEwiu86vSyZffAhWnNOwKHelFCb4QFjACegQIARAC&url=https%3A%2F%2Fwww.springer.com%2Fcda%2Fcontent%2Fdocument%2Fcda_downloaddocument%2F9783642224799-c1.pdf%3FSGWID%3D0-0-45-1262259-p174132261&usg=AOvVaw3Y1oBf7UA-Mjh1dipFtWBV

[21] A. Morales and C. Lieber. "A laser ablation method for the synthesis of crys- talline semiconductor nanowires". Science, 279(5348):208–211, 1998.
doi: 10.1126/ science.279.5348.208. URL http://www.sciencemag.org/content/279/5348/208. abstract.

[22] R.S. Wagner and W.C. Ellis. "Vapor-liquid-solid mechanism of single crystal growth". Applied Physics Letters, 4(5):89–90, 1964.
doi: http://dx.doi.org/10.1063/1. 1753975.
URL http://scitation.aip.org/content/aip/journal/apl/4/5/10.1063/1.1753975.

[23] S.T. Picraux, S. Dayeh, P. Manandhar, D. Perea, and S. Choi. "Silicon and ger- manium nanowires: Growth, properties, and integration". JOM, 62(4):35–43, 2010. ISSN 1047-4838.
doi: 10.1007/s11837-010-0057-z. URL http://dx.doi.org/10.1007/s11837-010-0057-z.

[24] H. Adhikari, A.F. Marshall, I. A. Goldthorpe, C. Chidsey, and P.C. McIntyre. Metastability of Au-Ge liquid nanocatalysts: Ge vapor-liquid-solid nanowire growth far below the bulk eutectic temperature. ACS Nano, 1(5):415–422, 2007.
doi: 10.1021/nn7001486.
URL http://dx.doi.org/10.1021/nn7001486.

[25] S. Kodambaka, J. Tersoff, M.C. Reuter, and F.M. Ross. Growth kinetics of Si and Ge nanowires. Proc. SPIE, 7224:72240C–72240C–11, 2009.
doi: 10.1117/12.810672.
URL http://dx.doi.org/10.1117/12.810672.

[26] V. Schmidt and U. Gösele. How nanowires grow. Science, 316(5825):698–699, 2007. doi: 10.1126/science.1142951. URL http://www.sciencemag.org/content/316/ 5825/698.short.

[27] P. Madras, E. Dailey, and J. Drucker. Kinetically induced kinking of vapor-liquid- solid grown epitaxial Si nanowires. Nano Letters, 9(11):3826–3830, 2009. doi: 10. 1021/nl902013g. URL http://dx.doi.org/10.1021/nl902013g. PMID: 19860454.

[28] S. Kral. Herstellung und Charakterisierung von monolithischen Germanium- Nanodraht-Bauelementen mit Metall-Halbleiter-Heteroübergang. Master's thesis. TU Wien, 2014.

[29] S. Kral, C. Zeiner, M. Stöger-Pollach, E. Bertagnolli, M. I. Den Hertog, M. Lopez- Haro, E. Robin, K. El Hajraoui, and A. Lugstein. Abrupt schottky junctions in Al/Ge nanowire heterostructures. Nano Letters, 15(7):4783–4787, 2015. doi: 10.1021/acs.nanolett.5b01748. URL http://dx.doi.org/10.1021/acs.nanolett. 5b01748. PMID: 26052733.

[30] G. Gu, M. Burghard, G. S. Kim, P. W. Chiu, V. Krstic, S. Roth, and W. Q. Han. Growth and electrical transport of germanium nanowires. Journal of Applied Physics, 90(11):5747–5751, 2001. doi: 10.1063/1.1413495. URL http://scitation.aip.org/content/aip/journal/jap/90/11/

[31] M. Whitby and N. Quirke, Handbook of Nanophysics: Nanotubes and Nanowires. CRC Press, 1 ed., Sept. 2008.

[32] Das, Mukunda. (2010). Mesoscopic systems in the quantum realm: Fundamental science and applications. Advances in Natural Sciences: Nanoscience and Nanotechnology. 1. 043001. 10.1088/2043-6262/1/4/043001.

[33] W.M. Haynes. CRC Handbook of Chemistry and Physics, 93rd Edition. CRC Hand- book of Chemistry and Physics. Taylor & Francis, 2012. ISBN 9781439880494. URL https://books.google.at/books?id=-BzP7Rkl7WkC.

[34] S. Kasap and P. Capper, Springer Handbook of Electronic and Photonic Materials, vol. 10. Springer Science and Business Media, 2006.

[35] B. Yu, X. H. Sun, G. A. Calebotta, G. R. Dholakia, and M. Meyyappan, “One-dimensional Germanium Nanowires for Future Electronics,” Journal of Cluster Science, vol. 17, pp. 579–597, Dec. 2006.

[36] S.M. Sze and K.K. Ng. Physics of Semiconductor Devices. Wiley, 2006. ISBN 9780470068304. URL https://books.google.at/books?id=o4unkmHBHb8C.

[37] S.M. Sze and M.K. Lee. Semiconductor Devices: Physics and Technology, 3rd Edition: Physics and Technology. John Wiley & Sons, 2012. ISBN 9781118139837. URL https://books.google.at/books?id=WdcbAAAAQBAJ.

[38] C. Kittel. Introduction to Solid State Physics. Wiley, 1996. ISBN 9780471111818. URL https://books.google.at/books?id=1X8pAQAAMAAJ.

[39] Bailey, Sheila G.; Raffaelle, Ryne; Emery, Keith (2002). "Space and terrestrial photovoltaics: synergy and diversity". Progress in Photovoltaics: Research and Applications. 10 (6): 399–406. doi:10.1002/pip.446. hdl:2060/20030000611.

[40] Thiele, Ulrich K. (2001). "The Current Status of Catalysis and Catalyst Development for the Industrial Process of Poly(ethylene terephthalate) Polycondensation". International Journal of Polymeric Materials. 50(3): 387–394. doi:10.1080/00914030108035115.

[41] Drozdov, Andrey (2007). Aluminium: The Thirteenth Element. RUSAL Library. ISBN 978-5-91523-002-5.

[42] Richards, Joseph William (1896). Aluminium: Its history, occurrence, properties, metallurgy and applications, including its alloys (3 ed.). Henry Carey Baird & Co.

[43] R. C. Weast, CRC handbook of chemistry and physics. CRC Press, Mar. 1986.

[44] Martienssen and H. Warlimont. Springer Handbook of Condensed Matter and Materials Data. Springer Handbook of Condensed Matter and Materials Data. Springer Berlin Heidelberg, 2006. ISBN 9783540304371. URL https://books. google.at/books?id=TnHJX79b3RwC.

[45] F.Katsuki,K.Hanafusa,M.Yonemura,T.Koyama,andM.Doi,“ Crystallizationof amorphous germanium in an al/a-ge bilayer film deposited on a sio 2 substrate,” Journal of Applied Physics, vol. 89, no. 8, pp. 4643–4647, 2001.

[46] F. Katsuki, K. Hanafusa, M. Yonemura, T. Koyama, and M. Doi. Crystallization of amorphous germanium in an AlGe bilayer film deposited on a SiO2 substrate. Journal of Applied Physics, 89(8):4643–4647, 2001. doi: 10.1063/1.1359149.

[47] H. Mehrer. Diffusion in Solids: Fundamentals, Methods, Materials, Diffusion- Controlled Processes. Springer Series in Solid-State Sciences. Springer, 2007. ISBN 9783540714880. URL https://books.google.at/books?id=IUZVffQLFKQC.

[48] J. Patterson and B. Bailey. Solid-State Physics: Introduction to the Theory. SpringerLink: Springer e-Books. Springer Berlin Heidelberg, 2007. ISBN 9783540349334. URL https://books.google.at/books?id=uRQg87Mb6DoC.

[49] A. Paul, “The kirkendall effect in solid state diffusion,” Laboratory of Materials and Interface Chemistry, 2004.

[50] H. Bracht and N.A. Stolwijk. Diffusion in Semiconductors. Landolt-Börnstein - Group III Condensed Matter. Springer Berlin Heidelberg, 1998. ISBN 978-3-540- 60964-3. doi: 10.1007/b53031.

[51] L. S. Darken, “Diffusion, mobility and their interrelation through free energy in binary metallic systems,” in Trans. AIME, vol. 175, p. 184, 1948.

[52] D. Graf, “Synthese und Charakterisierung von verdrahteten Germanium Quantenpunkten”, Diplomarbeit, Wien, Techn. Univ., 2018

[53] W.F. Gale and T.C. Totemeier. Smithells Metals Reference Book. Elsevier Sci- ence, 2003. ISBN 9780080480961. URL https://books.google.at/books?id= zweHvqOdcs0C.

[54] “University of Cambridge, Dissemination of IT for the Promotion of Materials Science (DoITPoMS).” [Online]. Available: www.doitpoms.ac.uk/tlplib/ diffusion/microstructure.php 91

[55] R. Sauer, Halbleiterphysik: Lehrbuch für Physiker und Ingenieure. Oldenbourg Verlag, 2010.

[56] T. Ayalew, " SiC Semiconductor Devices Technology, Modeling, and Simulation" Dissertation, Wien, Techn. Univ., 2004

[57] Goupil, Christophe; Ouerdane, Henni; Zabrocki, Knud; Seifert, Wolfgang; Hinsche, Nicki F.; Müller, Eckhard (2016). "Thermodynamics and thermoelectricity". In Goupil, Christophe. Continuum Theory and Modeling of Thermoelectric Elements. New York, New York, USA: Wiley-VCH. pp. 2–3. ISBN 9783527413379.

[58] T.M Tritt, H. Bottner, L. Chen, "Thermoelectrics: direct solar thermal energy conversion", MRS Bull, Vol. 33, pp. 3668, 2008

[59] A Novel Identification Method of Thermal Resistances of Thermoelectric Modules Combining Electrical Characterization Under Constant Temperature and Heat Flow Conditions - Scientific Figure on ResearchGate. Available from: https://www.researchgate.net/figure/Figure-of-merit-ZT-of-different-thermoelectric-materials-performing-a-function-of_fig2_310470558 [accessed 16 Oct, 2019]

[60] S. Glaßner, "Tuning the optical properties of silicon nanowires by ultra-high strain and plasmonic coupling ", PhD thesis, Wien, Techn. Univ., 2018

[61] L.R. Harriott. Limits of lithography. In Proceedings of the IEEE, pages 366–374, 2001.

[62] Steven M.G. Atomic layer deposition: An overview. Chemical Reviews, 110(1):111– 131, 2010. doi: 10.1021/cr900056b. URL http://dx.doi.org/10.1021/cr900056b. PMID: 19947596.

[63] M. Sistani, "Ballistic Transport Phenomena in Al-Ge-Al Nanowire Heterostructures", Diplomarbeit, Wien, Techn. Univ., 2014

[64] O. Sneh, R. Clark-Phelps, A. Londergan, J. Winkler, and T.E. Seidel. Thin film atomic layer deposition equipment for semiconductor processing. Thin Solid Films, 402(1-2):248 – 261, 2002. ISSN 0040-6090. doi: http://dx.doi.org/10. 1016/S0040-6090(01)01678-9. URL http://www.sciencedirect.com/science/ article/pii/S0040609001016789.

[65] The International Technology Roadmap for Semiconductors (ITRS), System Drivers, 2009, http://www.itrs.net/.

[66] B. Onsia, T. Conard, S. De Gendt, M. Heyns, I. Hoflijk, P. Mertens, M. Meuris, G. Raskin, S. Sioncke, and I. Teerlinck. A study of the influence of typical wet chemical treatments on the germanium wafer surface. Solid State Phenom, 103 (104):27–30, 2005. doi: 10.4028/www.scientific.net/SSP.103-104.27.

[67] H.S. Nalwa. Handbook of Thin Film Materials: Deposition and Processing of Thin Films. Elsevier Science & Technology Books, 2001. ISBN 9780125129084. URL https://books.google.at/books?id=6P5QAUno-PgC.

[68] K. Wasa, I. Kanno, and H. Kotera. Handbook of Sputter Deposition Technology: Fun- damentals and Applications for Functional Thin Films, Nano-materials and MEMS. William Andrew, 2012. ISBN 9781437734836. URL https://books.google.at/ books?id=6TYMTZdyWO4C.

[69] UniTempGmbH,"RapidThermalProcessOvenModellUTP1100."Datasheet.

[70] Resitive Temperature Sensore: PT100 datasheept

[71] L. Dobusch, M. M. Furchi, A. Pospischil, et al. "Electric field modulation of thermo- voltage in single-layer MoS2". In: Appl. Phys. Lett. 105.25 (2014).

[72] S. Roddaro, D. Ercolani, M. A. Safeen, et al. "Giant thermovoltage in single InAs nanowire field-effect transistors". In: Nano Lett. 13.8 (2013), pp. 3638–3642.

[73] S. Benter, "Synthesis and Thermoelectric Characterization of Metal-Semiconductor NW Heterostructures ", Diplomarbeit, Aalborg, Aalborg Univ., 2018

[74] N. Mingo, L. Yang, et al. "Predicting the Thermal Conductivity of Si and Ge Nanowires". In: Nano Lett. 3.12 (2003), pp. 1713–1716.

[75] J. Xiang, W. Lu, "Semiconductor Nanowires: From Next-Generation Electronics to Sustainable Energy". Royal Society of Chemistry (2014) ISBN: 9781782625209

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

1D	one dimensional
2D	two dimensional
2T	two point
Ag	Silver
Al	Aluminum
Al_2O_3	Aluminum oxide
ALD	Atomic layer deposition
Ar	Argon
Au	Gold
BHF	Buffered hydro-fluoric acid
BOE	Buffered oxide etching
BOX	Buried oxide layer
Cr	Chrome
DMSO	Dimethyl sulfoxide
DL	Device layer
ESD	Electro static discharge
Fcc	Face-centered cubic
FET	Field effect transistor
GaAs	Galliumarsenide
Ge	Germanium
GeO	Germanium monooxide
GeO_2	Germanium dioxid
GeH_4	Germane
H_2	Hydrogen
H_2O	Water
HF	Hydro-fluoric acid
HfO_2	Hafnium oxide
HI	Hydrogen iodide
HL	Handle layer
I/V	Current-voltage
InAs	Indiumarsenide
NW	Nanowire
N_2	Nytrogen
PET	Polyethylene terephthalate
RIE	Reactive ion etching
RTA	Rapide thermal annealing
SEM	Scanning electron microscope
Si	Silicon
SiO_2	Silicon oxide
TiO_2	Titanium oxide
UV	Ultra violet
VLS	Vapor liquid solid
Zn	Tin
ZrO_2	Zirconium oxide

LIST OF SYMBOLS

m_e	Effective mass
v	Velocety
p	Momentum
k	Base vector in k-space
$\hbar$	Planck constant
Δ	Laplace operator
∇	Nabla operator
V	Volume
D(E)	Electronic density of states
r, θ, z	Cylindric coordinates
ψ	Wave function
π	Pi
i	Imaginary unit
L	Length
a	Lattice constant
J	Diffusion flux
D	Diffusivity
D_0	Maximal diffusion coefficient at infinite temperature
E_A	Activation energy
T	Temperatur
R	Universal gas constant
∇C	Conzentration gradient vector
t	Time
N	Respective fraction
D_I	Interdiffusion coefficient
J_c	Emission current density
A_G	Specific correction factor
W	Work function
k_B	Boltzmann constant
E_{emf}	Electromagnetic field electromotive force
S	Seebeck coefficient
σ	Electrical conductivity
α	Differential Seebeck coefficient (thermo power)
U	Local voltage
ZT	Figure of merit
λ	Wave length
Re	Resolution
κ	Thermal conductivity
NA	Numerical aperture
A	Cross section
ρ	Specific resistance
R_Ω	Ohmic resistance

Appendix A

Process Parameters

A.1. Fabrication of the base module

Substrate preparation

The substrate, which was used for the production of the base module and further on for the TE test device, was a highly p-doped <100>-orientated Si wafer with a device layer-thickness of 500um, and a 100nm thick thermally grown SiO_2 layer on top. The wafer was cut in 15 x 15mm^2 pieces, by using a diamond scribe.

Substrate cleaning

Prior the photolithography steps, the following cleaning procedures were preformed, to ensure a clean surface.

- Ultrasonic cleaning in acetone for 120s at 100%
- Ultrasonic cleaning in isopropanol for 120s at 100%
- Blow drying with nitrogen

Photolithography

Process procedures needed for the checkerboard pattern grid on the base module:

- Spin coating of image reversal resist (AZ 5214) at 9000 rpm for 30s (ramp-up constant 3)
- Softbake at 373K for 60s
- Alignment for Cr photomask DI_V3
- Exposure for 8s (Karl Süss MicroTec MJB3)
- Dip in developer solution (AZ 726 MIF) for 80s
- Dip in DI water for 15s (to stop developer)
- Blow drying with nitrogen

Reactive iron etching (RIE)

- Process parameter from RIE
- 280s etching at 80K

HF DIP

- concentrated HF dip for 50min
- stopping of the etching with DI water
- critical point drying
- Dip acetone for 120s

A.2. Fabrication of the TE test device

Substrate cleaning

- Dip in isopropanol for 120s
- Plasma ashing in O_2 plasma at 300W for 300s

Introduction of the NW

- Drop-casting 4uL of NW consisting isopropanol solution onto TE test device
- Carefully blow drying with nitrogen orthogonally to trench

Photolithography

Process procedures needed for the Al contacts:

- Spin coating LOR (LOR 3A) at 1500 rpm for 30s (ramp-up constant 3)
- Softbake at 473K for 120s
- Spin coating LOR (LOR 3A) at 2000 rpm for 30s (ramp-up constant 3)
- Softbake at 473K for 120s
- Spin coating LOR (LOR 3A) at 3000 rpm for 30s (ramp-up constant 3)
- Softbake at 473K for 300s
- Spin coating of image reversal resist (AZ 5214) at 9000 rpm for 30s (ramp-up constant 3)

- Softbake at 373K for 60s
- Alignment for Cr photomask DI_V4
- Exposure for 4s (Karl Süss MicroTec MJB3)
- Hardbake at 373K for 100s
- Flood Exposure for 12s (Karl Süss MicroTec MJB3)
- Dip in developer solution (AZ 726 MIF) for 80s
- Dip in DI water for 15s (to stop developer)
- Blow drying with nitrogen

Al Sputtering

Prior the Al sputtering the following etching procedure has to be executed, to ensure an electrical contact between the NW and the Al contacts:

- Buffered HF (1:7) dip for 15s
- Dip in DI water 30s
- Blow drying with nitrogen
- Dip in HI (14%) for 5s
- Dip in DI water 15s

The sputter rate for deposition Al was experimentally determined to 0.42nms^{-1} at 50W. The sputter parameter where set as the following:

- Base pressure: 3 x 10^{-5}mbar
- Working pressure: 8 x 10^{-3}mbar
- Al cleaning procedure: 2 x 60s at 100W

- 100nm deposition of Al: 4 x 60s at 50W
- Wait 10min to cool the TE test device
- 100nm deposition of Al: 4 x 60s at 50W

Lift-Off

- Immerse TE test device in DMSO and heat to a temperature of 353K
- After 60min, rinse the TE test device carefully with DMSO inside the 353K Dip
- Dip in isopropanol for 120s
- Blow drying with nitrogen

Rapid Thermal Annealing

To form heterostructured NW, RTA was employed with the following process steps and parameters:

- Open working chamber and place TE test device on quartz tray
- Pump 120s to reach 2mbar
- Flush 120s with nitrogen
- Pump 120s to reach 2mbar
- Flush 120s with nitrogen
- Pump 120s to reach 2mbar
- Flush 120s with forming gas
- Heat to 573K with 75Ks^{-1} temperature ramping in forming gas atmosphere (no use of top-heat)

- Heat to 673K with 50Ks^{-1} temperature ramping in forming gas atmosphere (no use of top-heat)
- Hold temperature for 130s in forming gas atmosphere (no use of top-heat)
- Cool to ambient temperature with a nitrogen flush
- Open working chamber and remove TE test device from quartz tray

Photolithography

Process procedures needed for the Au heater structure:

- Spin coating LOR (LOR 3A) at 1500 rpm for 30s (ramp-up constant 3)
- Softbake at 473K for 120s
- Spin coating LOR (LOR 3A) at 2000 rpm for 30s (ramp-up constant 3)
- Softbake at 473K for 120s
- Spin coating LOR (LOR 3A) at 3000 rpm for 30s (ramp-up constant 3)
- Softbake at 473K for 300s
- Spin coating of image reversal resist (AZ 5214) at 9000 rpm for 30s (ramp-up constant 3)
- Softbake at 373K for 60s
- Alignment for Cr photomask DI_V5
- Exposure for 4s (Karl Süss MicroTec MJB3)
- Hardbake at 373K for 100s
- Flood Exposure for 12s (Karl Süss MicroTec MJB3)
- Dip in developer solution (AZ 726 MIF) for 80s

- Dip in DI water for 15s (to stop developer)
- Blow drying with nitrogen

Au Sputtering

The sputter successfully Au on a Si substrate, prior a layer of 10nm Ti as an adhesion promoter has to be deposited. The empirically determined sputter rates are 0.17nms^{-1} at 50W for Ti and 1.6nms^{-1} at 50W for Au.

- Base pressure: 3 x 10^{-5}mbar
- Working pressure: 8 x 10^{-3}mbar
- Ti cleaning procedure: 2 x 60s at 100W
- 10nm deposition of Ti: 1 x 60s at 50W
- 200nm deposition of Au: 2 x 60s at 50W

Lift-Off

- Immerse TE test device in DMSO and heat to a temperature of 353K
- After 60min, rinse the TE test device carefully with DMSO inside the 353K Dip
- Dip in isopropanol for 120s
- Blow drying with nitrogen