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DISSERTATION

Study and Development of a novel Silicon Pixel Detector for the Upgrade of the ALICE Inner Tracking System

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Kurzfassung

Das ALICE-Experiment wurde speziell zur Untersuchung von Schwerionen-Kollisionen im Large Hardon Collider (LHC) am CERN konstruiert. Während des zweiten langen Wartungsstops (LS2) des LHC in 2019/20 plant ALICE die Durchführung einer umfassenden Erneuerung und Verbesserung des existierenden Detektorsystems. Ein wichtiger Punkt ist dabei die Installation eines neuen, hochauflösenden Spurdetektors - des Inner-Tracking-Systems (ITS). Das neue ITS wird aus sieben konzentrische Lagen bestehen, mit einer Fläche von insgesamt circa $10\,\mathrm{m}^2$, die mit monolitischen, aktiven Pixelsensoren (MAPS) ausgestattet werden. Die Auswahl dieser Sensortechnologie wurde aufgrund der strengen Anforderungen an die Strahlungslänge des Materials von $0.3\,\%\ x/X_0$ pro Lage in den drei innersten Lagen getroffen, und unterstützt durch die starke Weiterentwicklung im Bereich von MAPS in den vergangenen Jahren.
Die Pixelchips werden im 180 nm CMOS Prozess von TowerJazz hergestellt, auf Wafer mit einer hochresistiven Epitaxialschicht, welche zur Sammlung der durch die durchgehenden Teilchen erzeugten Ladungsträger dient. Um im vollen Umfang ein spezielles Merkmal dieses Fertigungsprozesses, eine tiefe p-implantierte Lage (P-well), auszunutzen, wurden während der Forschungs- und Entwicklungsphase des neuen Pixelchips diverse Chiparchitekturen untersucht. Der tiefe P-well ermöglicht die Verwendung von umfangreichen CMOS-Schaltungen innerhalb der Pixelmatrix, ohne dass es dabei zu Auswirkungen auf die Effizienz der Ladungssammlung im Sensor kommt. Zusammen mit der kleinen Strukturgröße erlaubt dies die Implemetierung einer dauerhaft aktiven Frontend-Schaltung innerhalb jedes Pixels und die Verwendung einer Ausleselogik, die ohne alle Pixel lesen zu müssen, nur die Adressen von getroffenen Pixeln an die Chipperipherie sendet. Dieses Konzept wird im Besonderen vom sogenannten ALPIDE-Design verfolgt, das als ein weiteres Erkennungsmerkmal die Möglichkeit bietet, eine erhöhte Sperrvorspannung über das Wafersubstrat anzulegen. Dies ermöglicht eine signifikante Vergrößerung der Raumladungszonen um die Ladungssammlungs-Elektroden und erlaubt daher einen größeren Teil der Ladungsträger über weitere Strecken per Drift zu sammeln. Dies hat Vorteile in der Ladungssammlungszeit, und damit im Zusammenhang, in der Ladungssammlungs-Effizienz nach Bestrahlung durch eine verringerte Rekombinationswahrscheinlichkeit.

Diese Arbeit wurde im Rahmen der Forschung und Entwicklung des neuen Pixelchips für das ALICE ITS Upgrade durchgeführt, mit besonderem Augenmerk auf das ALPIDE-Design. Die Arbeit lässt sich dabei großteils in zwei Teile gliedern:

- Die Modellierung und Charakterisierung der sensitiven Schicht und der Ladungssammlungs-Elektrode des Pixelchips, mit einem Hauptaugenmerk auf das Q/C-Verhältnis, dem Verhältnis zwischen gesammelter Ladung in einem Pixel und der Pixel-Eingangskapazität.
- Die Charakterisierung des ersten ALPIDE-Prototypen im finalen Format ($3 \times 1.5\,\mathrm{cm}^2$), mit einem Hauptaugenmerk auf die Funktionsweise der neuen Frontend-Schaltung.

Um die Eigenschaften der sensitiven Schicht und der Ladungssammlungs-Elektrode zu untersuchen, wurden mehrere kleinformatige Prototypen mit analoger Auslese entworfen und produziert. Diese Chips enthalten diverse Pixeldesigns mit verschiedenen Pixelgrößen, Epitaxialschichten und Anordnungen der Ladungssammlungs-Elektrode. Den Einfluss dieser Parameter, auch im Zusammenhang mit der über das Wafersubstrat angelegten Sperrvorspannung, auf den Ladungssammlungs-Vorgang und die Eingangskapazität der Pixel habe ich umfassend unter Verwendung von Röntgenphotonen einer ^{55}Fe-Quelle untersucht. Zusätzlich habe ich maßgeblich zu verschiedenen Messungen in hochenergetischen Teilchen-Teststrahlen beigetragen. Um den Einfluss von strahlungsinduzierten Schäden zu quantifizieren, wurden die Studien sowohl vor, als auch nach Bestrahlung der Chips durchgeführt. Einhergehend mit den Messungen habe ich auch die Ladungssammlung im Sensor, abhängig von der Größe der Raumladungszonen um die Ladungssammlungs-Elektroden, modelliert und simuliert.
Nach einer Serie von kleinformatigen Prototypen wurde der erste ALPIDE-Prototyp im finalen Format, der pALPIDE-1, produziert. Für diesen Chip habe ich ausführliche Labormessungen zum Verhalten des analogen Teils der Frontend-Schaltung durchgeführt. Weiters habe ich auch für den pALPIDE-1 wesentlich zu den Messungen an Teststrahlen beigetragen. Die Messungen in Labor und Teststrahlen erlauben eine umfassende Bewertung von entscheidenden Leistungsparametern des Chips, wie Detektionseffizienz, Rauschtreffer-Rate und Ortsauflösung, und haben die Realisierbarkeit und Attraktivität des ALPIDE-Designs demonstriert.

Diese Arbeit stellt einen wesentlichen Beitrag zur Charakterisierung und Optimierung der ALPIDE-Entwicklung dar, die im ALICE ITS-Upgrade zur Anwendung kommen wird. Die intensiven Forschungs- und Entwicklungsarbeiten innerhalb des ALICE ITS-Upgrade Projekts haben dabei zu einer maßgeblichen Weiterentwicklung der Technologie von MAPS im Hinblick auf Energieverbrauch, Auslesegeschwindigkeit, Ladungssammlungs-Zeiten und Strahlungshärte geführt.

Abstract

ALICE (A Large Ion Collider Experiment) is the heavy-ion experiment at the CERN Large Hadron Collider (LHC). As an important part of its upgrade plans, the ALICE experiment schedules the installation of a new Inner Tracking System (ITS) during the Long Shutdown 2 (LS2) of the LHC in 2019/20. The new ITS will consist of seven concentric layers, covering about $10\,\mathrm{m}^2$ with Monolithic Active Pixel Sensors (MAPS). This choice of technology has been guided by the tight requirements on the material budget of $0.3\,\%\ x/X_0$ per layer for the three innermost layers and backed by the significant progress in the field of MAPS in recent years.
The pixel chips are manufactured in the TowerJazz 180 nm CMOS process on wafers with a high-resistivity epitaxial layer on top of the substrate. During the R&D phase several chip architectures have been investigated, which take full advantage of a particular process feature, the deep p-well, that allows for full CMOS circuitry within the pixel matrix while retaining full charge collection efficiency. Together with the small feature size, this allows to implement a continuously active front-end into each pixel and using a sparsified readout scheme that only sends the addresses of hit pixels to the periphery - an approach followed by the so-called ALPIDE design. As another distinguishing feature, the ALPIDE design provides the possibility to apply a reverse bias voltage via the substrate, which allows to significantly increase the depletion regions around the charge collection diodes.

This thesis is carried out within the framework of the R&D on the pixel chip for the ALICE ITS upgrade, and in particular the ALPIDE design. The work can be categorized in two main parts:

- The modeling and characterization of the sensitive layer and the charge collection electrode of the pixel chip, with a particular focus on the Q/C ratio, that is, the ratio of the collected charge in a single pixel and the pixel input capacitance.

- The characterization of the first final-size ($3 \times 1.5\,\mathrm{cm}^2$) ALPIDE prototype, with a particular focus on the functionality of its novel low-power front-end.

To study the characterisitics of the sensitive layer and the collection electrode, various small-scale prototypes with analogue readout were produced. These prototypes contain many pixel designs with varying pixel pitch, epitaxial layer properties and collection electrode geometry. Exploiting X-rays from an ^{55}Fe source, I performed extensive studies on the influence of all these parameters, and furthermore the reverse substrate bias voltage,

on the charge collection process and the pixel-input capacitance. In addition, I significantly contributed to various measurements using particle beam tests. In order to quantify the radiation induced effects on the sensor performance, the studies were performed before and after irradiation. Along with the measurements, I also modeled the charge collection in the partially depleted sensitive layer characteristic for the used technology.
After a series of small-scale prototypes, a first final-size ($3 \times 1.5\,\mathrm{cm}^2$) prototype of the ALPIDE, the so-called pALPIDE-1, was submitted. For this prototype, I performed comprehensive lab-studies on the behaviour of the analogue part of the front-end circuit. Furthermore, also for the pALPIDE-1 I significantly contributed to the measurements employing particle test beams. The lab and test beam measurements allowed an assessment of decisive chip performance parameters as detection efficiency, fake hit rate, and position resolution, and demonstrated the feasibility and attractiveness of the ALPIDE design.

This work represents a key contribution to the characterization and optimization efforts towards the final design of the pixel chip for the new ALICE ITS. The intensive R&D carried out within the framework of the ALICE ITS upgrade led to a significant advancement of the technology of MAPS regarding power consumption, readout speed, charge collection time and radiation hardness.

Contents

1. Introduction

ALICE (A Large Ion Collider Experiment) [1] is one of the experiments at the CERN Large Hadron Collider (LHC) [2] and is specifically designed to study the physics of strongly interacting matter, in particular, the characteristics of *quark-gluon plasma* (QGP). For the time after the second long shutdown (LS2) of the LHC, ALICE is preparing a major upgrade of its apparatus targeting both an improvement of the measurement precision, as well as an increase of the event readout rate. A key element of the upgrade is a new, ultra-light, high-resolution Inner Tracking System (ITS), equipped with monolithic silicon pixel sensors. This thesis is carried out within the development efforts towards the new pixel chip for the upgraded ITS in the so-called ALPIDE design.
This chapter provides an overview of the ALICE physics program, highlighting heavy flavour probes, which are the primary scope of the upgraded ITS. Furthermore, it presents an overview of the current layout of the ALICE experiment and its upgrade plans.

1.1. Quark-gluon plasma

Quantum Chromodynamics (QCD) (see e.g. [3]) is part of the Standard Model of particle physics and describes the strong interaction, the fundamental interaction between quarks and gluons. It explains the dependency of the intensity of the interaction, i.e. the strong coupling constant α_S, on the transferred momentum Q.
At small momentum transfers Q, the strong coupling constant is large ($\alpha_S > 1$) and quarks are bound in either mesons ($q\bar{q}$) or baryons (qqq)[1]. The property, that no free quarks are observed, is known as *confinement*. At large momentum transfers Q^2, α_S decreases until the quarks are quasi-free particles, a condition known as *asymptotic freedom*.
QCD moreover predicts that when finite size hadrons begin to overlap at very high temperatures or densities, quarks and gluons form a deconfined phase of matter, which is referred to as *quark-gluon-plasma* (QGP) [5]. It is assumed that this phase existed in the early universe, some 10 ps after the Big Bang lasting for about 10 µs. At low baryochemical potential μ_B[2], the critical temperature T_c for the transition from the familiar, confined hadron phase to the QGP phase of matter is estimated to be in the order of 100 MeV to 200 MeV[3] [6]. In the laboratory, QGP is created in ultra-relativistic heavy-ion

[1] Recently, also pentaquarks have been discovered [4].
[2] The baryochemical potential is a measure for the net baryon density and quantifies the energy needed for adding an additional baryon to the partcle ensemble.
[3] For reference, a temperature of 100 MeV corresponds to 1.16×10^{12} K.

collisions.
The LHC allows to accelerate and collide protons and Pb-nuclei to unprecedented center-of-mass energies, of so far up to $\sqrt{s} = 13\,\text{TeV}$ for protons and up to $\sqrt{s_{NN}} = 2.76\,\text{TeV}$ per nucleon pair for Pb-nuclei[4]. Compared to previous heavy-ion experiments at the CERN SPS or BNL RHIC, this represents a large increase in beam energy with the associated larger cross sections for hard probes [5] and higher particle densities and creates a "hotter, larger, and longer living" QGP [7]. The LHC thus offers a unique opportunity to carefully study the properties of the QGP.

Characterizing the QGP

The characterization of the QGP is carried out using various probes emerging from ultra-relativistic nucleus-nucleus (A-A) collisions at unprecedented energies. In order to provide reference data, in addition to A-A collisions, ALICE also performs precision measurements using proton-proton (pp) and proton-nucleus (p-A) collisions.
Determining the properties of the QGP is, however, challenging due to its short life time and the fact that it is only indirectly observable after its transition to hadronic matter. In general, during a heavy-ion collision, a short-lived, non-spherical hot *fireball* is created [8]. The precise shape and size of the fireball will thereby depend on the overlap of the nuclei during the collision, also referred to as the collision's *centrality*.
A first crucial question is to what extent the created system, that is the fireball, behaves like a phase in the thermodynamic sense, and not like a group of individual elementary particles. To be able to refer to a phase, the system must consist of many particles and needs to reach a local equilibrium, so that variables such as temperature, pressure, energy or entropy and the relation of these quantities are defined and can be studied. Indeed, the fireball was found to behave like a strongly interacting, almost perfect fluid. It is opaque and absorbs much of the energy of high-$p_\perp$ [6] quarks an gluons traversing it and shows hydrodynamic flow effects as it reacts to pressure gradients [9, 10, 7]. Moreover, also high-precision measurements of hadron yield ratios in heavy-ion collisions, in particular the high abundance of hyperons[7] [11], represent a strong argument for the existence of a thermally and chemically equilibrated state. This argument is substantiated by the fact that in e^+e^- or p-p collisions such an equilibrium is not observed [8].

[4] Plans are to increase these energies to the LHC design values of $\sqrt{s} = 14\,\text{TeV}$ and $\sqrt{s_{NN}} = 5.5\,\text{TeV}$, respectively [2].
[5] *Hard processes* in QCD refer to scattering processes with momentum transfers Q at scales $Q \gg \Lambda_{QCD}$, Λ_{QCD} being the QCD scale parameter. Accordingly, the term *hard probe* refers to heavy quark-anti-quark pairs ($m_q \gg \Lambda_{QCD}$) or large $p_\perp$ partons ($p_\perp \approx Q$), which are created in initial hard scattering events in a heavy ion collision.
[6] $p_\perp$ is the transverse momentum of a particle, i.e. the component of its momentum perpendicular to the beam line.
[7] *Hyperon* refers to a baryon containing one or more strange quarks, but no charm, beauty, or top quark.

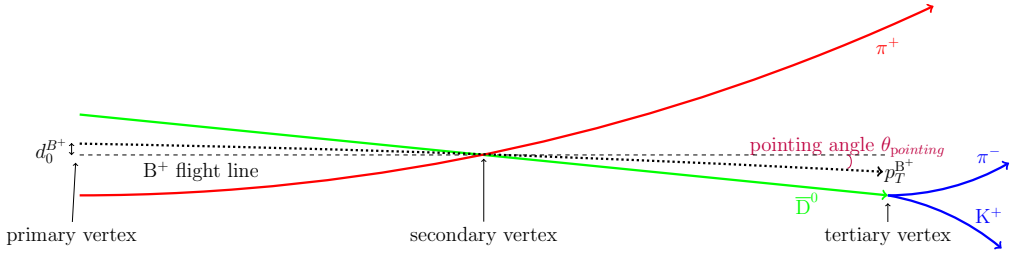


Figure 1.1.: Topology of the decay $B^+ \to \bar{D}^0\pi^+$ and subsequent decay of $\bar{D}^0 \to K^+\pi^+$. The reconstructed transverse momentum $p_\perp^{B^+}$, the impact parameter d_0^B and the pointing angle $\theta_{pointing}$ are shown [16].

Heavy-flavour probes The temperature of the QGP can be inferred from direct photon measurements. Measurements by PHENIX at RHIC with Au-Au collisions at $\sqrt{s_{NN}} = 200\,\mathrm{GeV}$ yield a QGP temperature of the order of 220 MeV [12], whereas measurements performed by ALICE at the LHC at higher energies obtain a value of about 300 MeV [13]. While these temperature scales allow to create *light quark* pairs ($u\bar{u}$, $d\bar{d}$ and also $s\bar{s}$), they are assumed to be too low to allow the creation of *heavy quark* pairs (essentially $c\bar{c}$ and $b\bar{b}$ [8]). Consequently, it is assumed that heavy quarks are dominantly produced in hard processes, which occur before the creation of the QGP phase. For such processes, the initial-state production can be predicted using perturbative QCD (pQCD) [15]. The QGP life time is estimated to be of the order of 10 fm/c, which corresponds to about 3.3×10^{-23} s. In comparison, the life time of charmed and beauty hadrons are of the order of 1×10^{-12} s [14]. Thus, the time until they decay weakly is large compared to the QGP life time, and after their creation heavy quarks will preserve their identity while propagating through the medium. Since the energy loss ΔE is expected to depend on medium properties (e.g. density, interaction strength), the path length inside the medium, but also the quark mass and color charge, they represent rich probes for microscopic studies of the QGP [8].

After the transition from the QGP phase to hadronic matter - also referred to as *chemical freeze out* - the heavy quarks can be found in different hadrons, mainly with a single heavy quark (e.g. D^0, D^{*+}, D_s^+ and Λ_c^+ for charm quarks, or B, B^+ and Λ_b for beauty quarks), but also to a smaller extent in $c\bar{c}$ or $b\bar{b}$ pairs (e.g. J/ψ or Υ). As can be seen in Tab. 1.1, all these particles have in common that they are short-lived (i.e. have a short decay length). Moreover, they are produced scarcely compared to the overall expected pseudorapidty[9] densities of charged particles, $\mathrm{d}N_{ch}/\mathrm{d}\eta$, of about 1800 in the 5 % most-central Pb-Pb collisions at mid-pseudorapidity for $\sqrt{s_{NN}} = 5.5\,\mathrm{TeV}$ [17][10].

[8] *Current quark* masses [14]: $m_u \approx 2\,\mathrm{MeV}$, $m_d \approx 5\,\mathrm{MeV}$, $m_s \approx 100\,\mathrm{MeV}$, $m_c \approx 1.3\,\mathrm{GeV}$, $m_b \approx 4.2\,\mathrm{GeV}$, $m_t \approx 174\,\mathrm{GeV}$.

[9] Pseudorapidity η is a measure for the particle direction, where $\eta = -\ln(\theta/2)$, θ being the polar angle with respect to the beam direction.

[10] For Pb-Pb collisions at a centre-of-mass energy of $\sqrt{s_{NN}} = 2.76\,\mathrm{TeV}$ per nucleon pair the density of primary charged particles was measured to be about 1600 at mid-pseudorapidity [18].

Table 1.1.: Expected production yields (total and per unit of rapidity at mid-rapidity) for charm and beauty particles (+ anti-particles) in minimum-bias and 0 % to 10 % events for central Pb–Pb collisions at 5.5 TeV, mean proper decay length and branching ratios to the relevant decay channels [16, 14].

Part.	Yield m.b., 0-10 %	$\mathrm{d}N/\mathrm{d}\eta\|_{\eta=0}$ m.b., 0-10 %	$c\tau$ [µm]	decay channel	branching ratios
D^0	23, 100	2.3, 11	≈ 120	$\mathrm{K}^-\pi^+$	3.8 %
D^{*+}	9, 44	0.9, 4.4	≈ 0	$\mathrm{D}^0\pi^+$	67.7 %
D_s^+	4.3, 20	0.4, 2.0	≈ 150	$\Phi(\rightarrow \mathrm{K}^+\mathrm{K}^-)\pi^+$	4.4 %($\times$ 49 %)
Λ_c^+	2.9, 14	0.29, 1.4	≈ 60	$\mathrm{pK}^-\pi^+$	5.0 %
				$\mathrm{p}\overline{\mathrm{K}}^0(\mathrm{K}_S^0 \rightarrow \pi^+\pi^-)$	1.15 %($\times$ 69.2 %)
				$\Lambda\pi^+(\rightarrow p\pi^-)$	1.1 %($\times$ 63.9 %)
B	1.3, 6.2	0.2, 0.9	≈ 500	$\mathrm{J}/\psi(\rightarrow e^+e^-) + X$	1.2 %($\times$ 6 %)
				$\mathrm{D}^0(\rightarrow \mathrm{K}^-\pi^+) + X$	60 %($\times$ 3.8 %)
				$e^+ + X$	10.9 %
B^+	0.6 2.7	0.1, 0.4	≈ 500	$\overline{\mathrm{D}}^0(\rightarrow \mathrm{K}^+\pi^-)\pi^+$	0.5 %($\times$ 3.8 %)
B^0	0.6 2.7	0.1, 0.4	≈ 500	$\mathrm{D}^{*-}(\rightarrow \mathrm{K}^+\pi^-\pi^-)\pi^+$	0.3 %($\times$ 2.6 %)
Λ_b^0	0.1 0.5	0.015, 0.07	≈ 400	$\Lambda_c^+(\rightarrow \mathrm{pK}^-\pi^+) + e^- + X$	9.9 %($\times$ 5 %)
				$\Lambda_c^+(\rightarrow \mathrm{pK}^-\pi^+) + \pi^-$	0.6 %($\times$ 5 %)

A heavy flavour analysis therefore needs to rely on very efficient selection criteria and strongly benefits from increased statistics. The selection criteria are typically based on a recipe involving the kinematic variables and particle identification (PID) of decay particles, and a subsequent search for secondary or even tertiary *vertices*[11] compatible with the decay topology of the considered particles (cf. Fig. 1.1).

1.2. The ALICE detector

The focus of ALICE on heavy-ion collisions led to requirements very different from the other LHC experiments. The high particle densities present in central Pb-Pb collisions[12] led to the design of a highly granular detector. For the measurement of total particle yields (i.e. integrated over $p_\perp$), tracking and vertexing down to very low transverse momenta, where particles are produced most abundantly, is required. Particle identification (PID) is of great importance to study e.g. the composition of the set of produced particles.

[11] In particle physics, the *interaction point* (IP) of colliding beam particles is also referred to as *primary vertex*. Accordingly, a particle decay vertex outside the interaction point is called *secondary vertex* [19].

[12] ALICE was designed to allow for track reconstruction with pseudorapidity densities of charged particles up to $\mathrm{d}N_{ch}/\mathrm{d}\eta \approx 8000$ [20].

In addition, high-$p_\perp$ probes, e.g. jets[13], require good tracking resolution up to high momenta.

The ALICE experiment measures 26 m in length and 16 m in height. It can be subdivided into a central detector part - also called the central barrel - and a muon spectrometer in forward direction, along with smaller detectors for trigger and event characterization. Both the central barrel, as well as the muon arm, are composed of several sub-detectors each serving a particular purpose [1, 21].
The central barrel is located inside the L3 magnet with a solenoidal field strength of 0.5 T. The detectors in the central barrel are mainly dedicated to vertex reconstruction, tracking and PID. Ordered by increasing radial distance from the beam pipe, the main components of the apparatus are (cf. Fig. 1.2) [1]:

- **Inner Tracking System (ITS) -** The present ALICE ITS [1] consists of six cylindrical layers of position sensitive silicon detectors, covering a radial distance between 39 mm and 436 mm. It is built using three different technologies: hybrid Silicon Pixel Detectors (SPD) for the two inner layers, Silicon Drift Detectors (SDD) for the two middle layers and Silicon Strip Detectors (SSD) for the two outer layers. Its main purpose is the precise determination of primary and secondary vertices and high granularity, low $p_\perp$ tracking. The analogue read-out of the four outermost layers moreover allows PID via specific energy loss in the non-relativistic $1/\beta^2$ region.

- **Time Projection Chamber (TPC) -** The TPC [22] is ALICE's main detector for tracking and particle identification via specific energy loss. It is a gaseous detector in the shape of a hollow cylinder with a length of 5 m in beam direction, an inner radius of approximately 57 cm and an outer radius of 278 cm, comprising an active gas volume of 88 m^3.

- **Time-Of-Flight detector (TOF) -** The TOF [23, 24] consists of multi-gap resistive plate chambers (RPC) at a radial distance of 370 cm from the beam line. It is designed for PID by measuring the flight time from the interaction point.

Both the ITS and especially the TPC, as a gaseous detector, are very light in terms of radiation length. Among the four large experiments at the LHC, ALICE is the one with the lowest material budget and magnetic field in the central rapidity region[14]. This combination allows ALICE to perform tracking down to a $p_\perp$ of about 150 MeV/c [21] and

[13] A *jet* refers to a norrow cone of hadrons that is produced by the hadronization of a high-$p_\perp$ quark or gluon.

[14] A particle in ALICE has to cross about 13 % of radiation length until it leaves the TPC, which is about third of case in ATLAS [25] or CMS [26] before their calorimeters [27]. Moreover, ATLAS and CMS use magnetic fields of 2 T and 3.8 T, respectively.

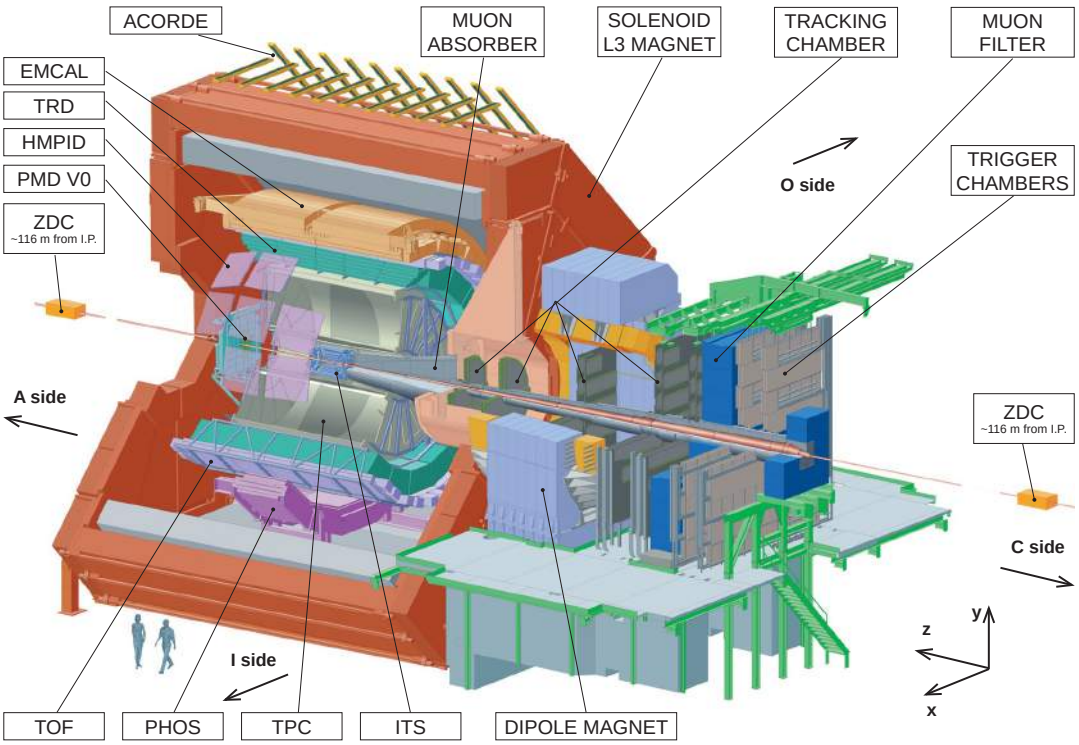


Figure 1.2.: Current layout of the ALICE experiment with its main subdetectors [1].

translates into excellent momentum resolution at low $p_\perp$. Employing the sub-detectors listed above, ALICE furthermore provides excellent capabilities for PID from very low $p_\perp$ to values up to 20 GeV/c. These two features are of great importance for the measurements of the $p_\perp$-differential yields of heavy-flavour hadrons, since they help to drastically reduce the combinatorial background and most of their daughter particles are found at low $p_\perp$.

1.3. ALICE upgrade plans

After its first years of running, ALICE already proved to provide very good performance for heavy ion collisions. It confirmed the basic picture of the nature of the QGP drawn by earlier experiments at the SPS and RHIC, however, exceeding their precision and kinematic reach at all significant probes [28]. Despite this success, there are several frontiers, including high precision measurements of rare probes at low transverse momenta, which are out of reach for the present experimental setup.
The ALICE long-term physics goals and the according experimental strategies are discussed in detail in the ALICE Upgrade Letter of Intent [29]. Topics to be addressed include heavy flavour hadrons, quarkonia and low-mass dileptons at low transverse momenta.

By upgrading key detector elements and an increase in statistics, the capability to study these processes will be greatly enhanced. ALICE is therefore developing a major upgrade of its apparatus, planned for installation during the Long Shutdown 2 (LS2) of the LHC in 2019/20.

Upgrade strategy

The upgrade strategy is based on a combination of detector upgrades and a large increase of the LHC luminosity for Pb-Pb collisions, reaching $\mathcal{L} = 6 \times 10^{27}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ at an event rate of about 50 kHz. In the proposed plan, the ALICE detector will be upgraded to enable the readout of all interactions, accumulating more than $10\,\mathrm{nb}^{-1}$ of Pb-Pb collisions after LS2. Since the majority of the rare probes in Pb-Pb collisions cannot be selected with a trigger due to a very high combinatorial background, it is required to take minimum-bias data. For these measurements the upgrade will provide an increase of statistics of about a factor 100 with respect to the program defined until LS2. For the measurements that are currently based on rare triggers, the increase in statistics will be a factor 10 [16]. Moreover, the intended measurements ask for a significant improvement in vertexing and tracking efficiency at low $p_\perp$. In summary, the detector upgrade consists of [29]:

- A reduction of the beam pipe radius from 29.8 mm to 19.2 mm;
- New high resolution, low material silicon trackers:
  - Inner Tracking System (ITS) [16] covering mid pseudorapidity ($-1.2 < \eta < 1.2$);
  - Muon Forward Tracker (MFT) [30] covering forward pseudorapidity ($-3.6 < \eta < 2.45$) to add vertexing capabilities to the current Muon Spectrometer;
- Upgrade of the Time Projection Chamber (TPC) [31], consisting of the replacement of the wire chambers with GEM detectors and new pipelined readout electronics allowing for continuous readout;
- Upgrade of the readout electronics of the Transition Radiation Detector (TRD), Time-Of-Flight (TOF) detector, and Muon Spectrometer to enable the operation at increased rates;
- Upgrade of the online and offline reconstruction and analysis framework [32].

Physics objectives for the ALICE ITS upgrade

Measurements of heavy flavour interactions with the QGP medium are the primary scope of a new ITS with largely improved tracking and readout-rate capabilities [16]. In this regard, the two main open questions and the related experimental handles are:

- The study of the thermalization and hadronization of heavy quarks in the QGP medium. This will be possible by measuring the heavy flavour baryon/meson ratio for charm (Λ_c/D) and for beauty (Λ_b/D), and the azimuthal anisotropy v_2 [15] for charm and beauty mesons.
- The study of the in-medium energy loss of heavy quarks and its mass dependence. This can be performed by measuring the nuclear modification factors R_{AA} [16] as function of $p_\perp$ for D and B mesons in a wide momentum range, as well as the heavy flavour production associated with jets.

Additionally, the new ITS will provide an essential contribution for a detailed measurement of electromagnetic radiation from the QGP, including thermal photons detected as low-mass dielectrons.

This thesis is conducted within the R&D project on the new pixel chip for the upgraded ALICE ITS. The upgrade of the ITS, including its motivation and the requirements on the pixel chip derived therefrom, are discussed in detail in the following chapter (Chap. 2). The two chapters thereafter (Chaps. 3 and 4) describe the technology and working principle of the sensor. Furthermore, measurement results on various small-scale prototypes with analogue readout are discussed, which have been used to guide the optimization of the sensor design. In the final chapter (Chap. 5), the characterization results on the first final-size prototype are presented.

[15] v_2 is the second order Fourier coefficient of the azimuthal distribution of particles w.r.t. the reaction plane.

[16] R_{AA} factor relates the particle production yield in A-A collisions to that expected for a superposition of independent nucleon-nucleon collisions.

2. Upgrade of the ALICE Inner Tracking System

As an important cornerstone of its upgrade plans, ALICE schedules the installation of a new Inner Tracking System (ITS), consisting of seven concentric layers of Monolithic Active Pixel Sensors (MAPS), fabricated in the TowerJazz 180 nm CMOS technology. This chapter lines out the upgrade concept and presents the general layout of the new ITS. Based on the related requirements on the detector, the choice of technology for the pixel chip is motivated. The later part of the chapter is devoted to the R&D on the new pixel chip, which provides the framework for this thesis. Special focus is thereby given to the ALPIDE development. Starting from the state of the art before the R&D within the ALICE ITS upgrade, the development approach for the ALPIDE design, including the prototypes discussed in later chapters, is explained.

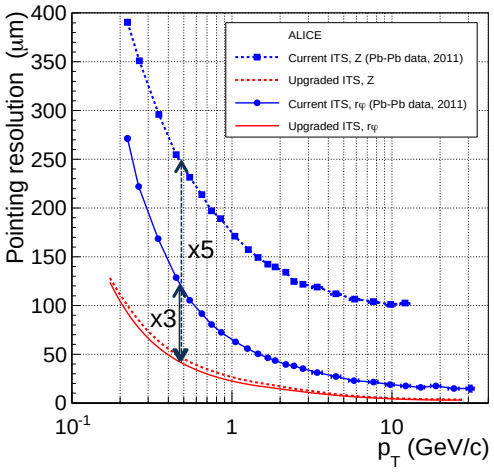
2.1. Present ITS and limitations

An important element of the proposed ALICE physics program for the time after LS2 is the high precision measurement of processes including heavy flavour quarks. An essential part of the analysis of these processes is the identification of secondary vertices with the respective decay topologies. By distinguishing the decay vertices of heavy-flavour hadrons from the primary vertex, background signals can be strongly suppressed. A key parameter in this context is the decay length

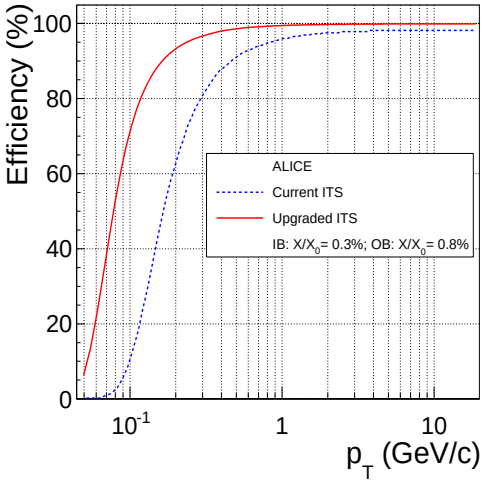
$$\lambda_{decay} = \beta c \tau_0 \gamma, \tag{2.1}$$

where βc is the velocity of the decaying particle, τ_0 its proper life time, and γ the Lorentz factor. Thus, in order to allow to apply the according selection criteria, the detector system has to provide a track resolution close to the interaction point (IP)- also known as *pointing resolution* - which is better than the decay lengths of the particles to be measured.

Concerning heavy flavour measurements, the present ALICE ITS has significant limitations [16]. First, it can only operate a maximum readout rate of 1 kHz, irrespective of the detector occupancy. For the physics channels that cannot be selected by a trigger, this represents a crucial limitation since the Pb-Pb collision rate that can presently be



(a) Pointing resolution as a function of transverse momentum.



(b) Tracking efficiency as a function of transverse momentum.

Figure 2.1.: Performance (for primary charged pions) of the current ITS compared to expected performance of the upgraded ITS [16].

delivered by the LHC is 8 kHz. It is also clearly inadequate to perform measurements at the envisaged readout rates for the time after the LS2.
Secondly, the pointing resolution of the present ITS restricts the range of measurements that are accessible: while it is adequate for the study of charm and beauty mesons in particular decay channels (e.g. $D^0 \to K\pi$ and $D^+ \to K\pi\pi$) at transverse momenta above 1 GeV/c, at lower transverse momenta the statistical significance becomes insufficient for currently achievable data sets. Moreover, the detection of charmed baryons is currently not feasible in Pb-Pb collisions. The most abundantly produced charm baryon, the Λ_c, has a mean proper decay length of only 60 µm, which is lower than the pointing resolution of the current ITS (cf. Fig. 2.1a) in the $p_\perp$-range of most of the Λ_c daughter particles (< 1 GeV/c). Also the study of baryons containing a beauty quark or more than one heavy quark is beyond reach of the current detector [16]. Overall, a decrease of the measurement uncertainty - obtained both by means of increased statistics and an improved experimental setup - would allow to greatly enhance the understanding of the interaction of heavy-flavour quarks with the QGP, and consequently the QGP properties [29].

2.2. Upgrade concept

The objectives for the ITS upgrade are to record Pb-Pb collisions at up to 100 kHz and pp collisions at 400 kHz, while improving the pointing resolution by a factor three in $r\varphi$ and a factor five in z at $p_\perp = 500$ MeV/c with respect to the present ITS (cf. Fig. 2.1a) [16].

The pointing resolution σ_p is mainly determined by two aspects:

- First, by the error σ_p^x of the geometrical extrapolation from measured points along the particle's track to the interaction point (IP). This contribution is mainly determined by the intrinsic resolution $\sigma_{x,i}$ and the positions r_i of the detector elements i.

- Secondly, by the uncertainty σ_p^{ms} introduced by multiple coulomb scattering occurring in the beam pipe and the detector layers themselves, especially the one closest to the IP. The distribution of the angular deflection due to scattering can roughly be described by a Gaussian with RMS width θ_{RMS} [14]:

$$\theta_{RMS} = \frac{13.6\,[\text{MeV}]}{\beta cp} z\sqrt{x/X_0}\,[1 + 0.038\,\ln(x/X_0)]\,, \tag{2.2}$$

  where p, βc, and z are the momentum, velocity and charge of the incident particle, and x/X_0 is the thickness of the material in terms of radiation length X_0 [1].

In order to assess the influence of these parameters on the pointing resolution of a tracking system, already the simple example of a two-layer detector provides valuable insights [33] [2]. Considering a configuration with the inner layer at radius r_1 and the outer layer at r_2, featuring a spatial resolution of σ_1 and σ_2, respectively, the contribution σ_p^x yields

$$\sigma_p^x = \sqrt{\left(\frac{r_2}{r_2 - r_1}\sigma_1\right)^2 + \left(\frac{r_1}{r_2 - r_1}\sigma_2\right)^2}. \tag{2.3}$$

The multiple scattering causes a deviation from zero pointing resolution due to θ_{RMS} over the lever arm r_1 (or the beam pipe radius), which is $\sigma_p^{ms} \approx r_1\theta_{RMS}$. For a track at angle ϕ with respect to the detection layer surface, this expression is increased by two effects: first, because the amount of material to be crossed increases, $x \to x/\sin\phi$, and second because the level arm is larger, $r_1 \to r_1/\sin\phi$. In summary, for a particle with unit charge and neglecting the logarithmic term in Eq. (2.2), the contribution of multiple scattering to σ_p can be written as

$$\sigma_p^{ms} \approx \frac{r_1}{\sin^{3/2}\phi}\frac{13.6\,[\text{MeV}]}{\beta cp}\sqrt{x/X_0} \tag{2.4}$$

The pointing resolution σ_p is then obtained by summing the two contributions in quadrature

$$\sigma_p \approx \sigma_p^x \oplus \sigma_p^{ms} \tag{2.5}$$

[1] The radiation length X_0, typically expressed in g/cm^2, is a characteristic value for a material. It is both the mean distance over which a high energy electron loses all but $1/e$ of its energy by bremsstrahlung, and 7/9 if the mean free path for pair production by a high energy photon [14].

[2] A detailed treatment of the topic can be found in [34].

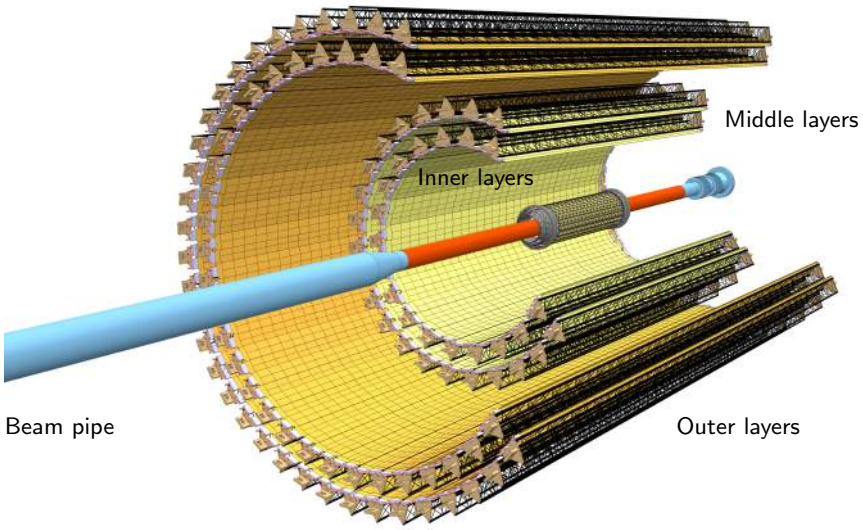


Figure 2.2.: Layout of the new ITS [16].

This simple treatment indicates that a better pointing resolution is mainly achieved by small inner radii (r_1) and low material budget (x/X_0), especially for the innermost layer and the beam pipe. The position resolution at the inner radius is weighted by the outer radius, so precision at the inner layer is paramount.
Indeed, for the ITS upgrade detailed simulations have been performed to determine the optimum design parameters. In summary, the following design objectives were defined:

- Reducing the distance between the first layer and the interaction point from 39 mm to 22 mm;
- Reducing the material budget from 1.14 % to 0.3 % x/X_0 per layer for the innermost layers and to 1.0 % x/X_0 per layer for the outer layers;
- Reducing the pixel size from 50 µm × 425 µm to about 30 µm × 30 µm;
- Increasing the number of layers from currently six to seven; this will also improve the standalone tracking efficiency and $p_\perp$-resolution at low transverse momenta.
- Increasing the readout rate from currently maximum 1 kHz to up to 100 kHz for Pb-Pb collisions and 400 kHz for pp collisions;
- Implementation of the possibility for an efficient insertion and removal of detector parts during the yearly shutdown period;

Table 2.1.: Layout parameters of the new ITS [16].

	Inner Barrel			**Outer Barrel**			
	Inner Layers			Middle Layers		Outer Layers	
	Layer 0	Layer 1	Layer 2	Layer 3	Layer 4	Layer 5	Layer 6
Length [mm]		271		843		1475	
Radial position [mm]	22.4	30.1	37.8	194.4	243.9	342.3	391.8
Nr. pixel chips	108	144	180	2688	3360	8232	9408
Nr. modules	12	16	20	384	480	1176	1344
Nr. staves	12	16	20	24	30	42	48
Chip size [mm^2]				15×30			

2.2.1. Layout of the upgraded ITS

To achieve the design objectives, the present ITS will be fully replaced by a new detector consisting of seven layers equipped with monolithic silicon pixel detectors (cf. Fig. 2.2). The layers are grouped into two separate barrels. The *Inner Barrel* (IB) consists of the three innermost layers, while the *Outer Barrel* (OB) contains the two middle and two outer layers.
The radial positions of the layers were tuned to obtain the optimum combined performance in terms of pointing resolution, $p_\perp$-resolution and tracking efficiency at a maximum hit density of about 19 hits/cm^2/event for minimum bias events in the innermost layer. The longitudinal extensions of the layers were chosen to provide a pseudorapidity coverage of $|\eta| < 1.22$ over 90 % of the most luminous beam interaction region. The detailed layout parameters are presented in Tab. 2.1. In total, the new ITS will cover a surface of 10.3 m^2 with about 12.5×10^9 pixels with binary readout. The size of a single pixel chip is 15 mm $\times$ 30 mm. In order to reduce the material budget, it will be thinned down to 50 µm. The expected radiation levels at the innermost layer, including a safety factor of ten, is 2.7 Mrad (TID) and 1.7×10^{13} 1 MeV n_{eq}/cm^2 (NIEL). Using water cooling, the new ITS will be operated at a temperature of 30 °C.

Staves The layers are azimuthally segmented in mechanically independent elements named *staves*. Even though the inner and outer barrel staves have different geometries, they have the same basic structure consisting of the following elements:

- *Space frame* - The space frame is the mechanical support element. It has a truss-like structure based on carbon fiber material.

- *Cold plate* - The cold plate is a carbon ply that embeds the cooling pipes.

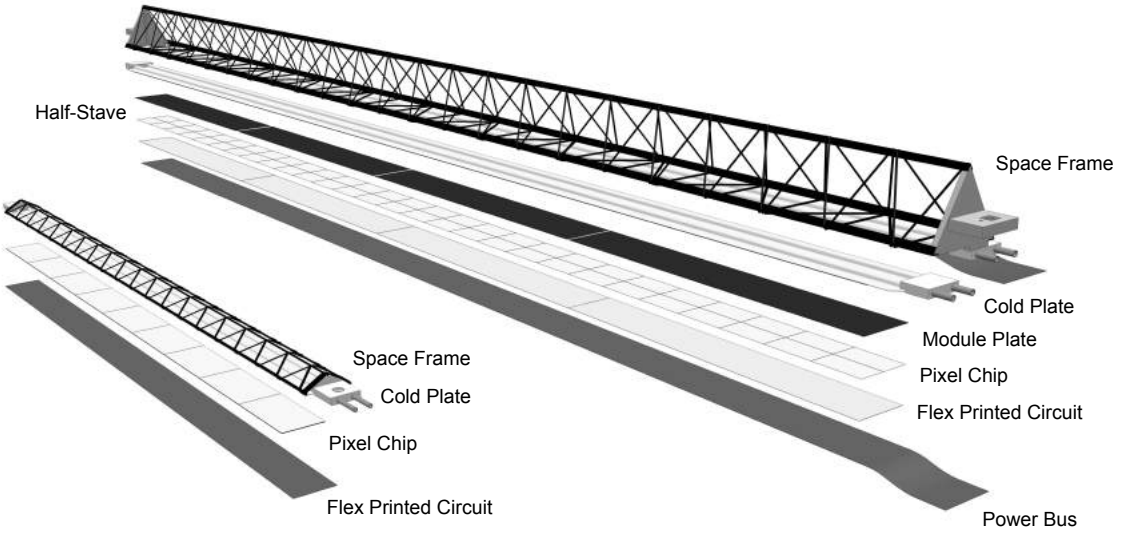


Figure 2.3.: Schematic drawing of the inner barrel (left) and the outer barrel (right) staves [16].

- *Hybrid integrated circuit (HIC)* - The hybrid integrated circuit is an assembly of a polyimide Flexible Printed Circuit (FPC) which interconnects several pixel chips and contains additional passive components. A novel feature of the ITS pixel chip is that all connection pads are distributed over its full top surface[3]. The bonding to the FPC is performed using a laser soldering technique specially adopted for this project.

The inner barrel stave hosts a single HIC integrating nine pixel chips. In contrast, the outer barrel staves are further segmented in azimuth into two halves extending over the full stave length, called *half-staves*. Each half-stave, in turn, is subdivided in longitudinal direction into a number of modules (cf. Fig. 2.5). The modules form separate entities, each consisting of a single HIC integrating two rows of seven pixel chips. An additional power bus, soldered to the FPC, is added to improve the power distribution over the full length of the staves.
The staves are fixed to a support structure, shaped in the form of a half-wheel, forming half-layers. Two half layers, top and bottom, are mounted separately around the beam pipe. Cooling and cabling infrastructure for the staves are routed only from one side of the detector through a service barrel. The total number of pixel chips, staves and modules for all layers are presented in Tab. 2.1.

Material budget The requirements on the material budget of 0.3 % x/X_0 per layer for the inner layers are particularly challenging. They will be achieved by the following measures:

[3] See Sec. 5.1 for details.

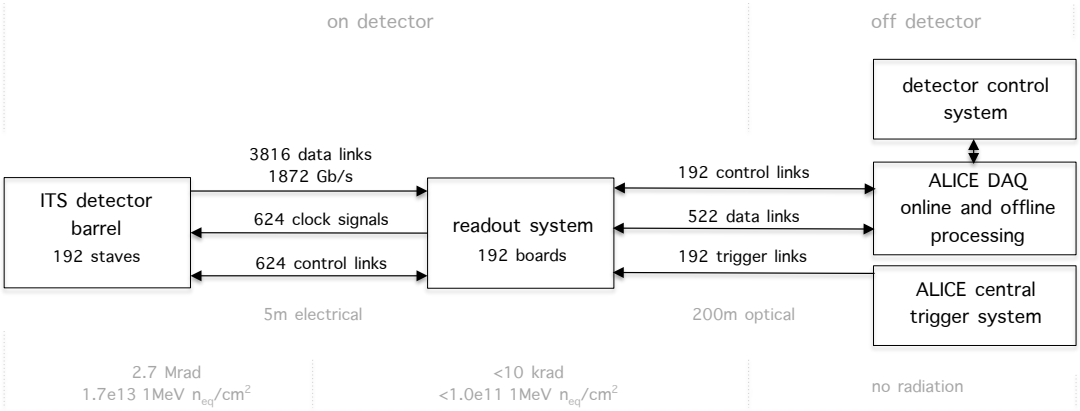


Figure 2.4.: Conceptual layout of the ITS readout system. The expected radiation levels in terms of TID and NIEL are also indicated.

- The use of monolithic silicon pixel sensors (cf. Sec. 2.2.2), consisting of only a single layer of silicon of a total thickness of 50 µm, allows the silicon material budget per layer to be reduced by a factor of seven in comparison to the present ITS. Additionally, the power consumption can be significantly reduced by a careful optimization of the analogue front-end and readout architecture. This will allow to reduce the material budget for electrical power and signal cables and the cooling infrastructure.
- No glue and wire bonding are used to interconnect the pixel chips to the FPCs. The connection is solely realized by the bonds distributed over the chip surface. Furthermore, compared to the present pixel detector, only a double sided instead of multi-layer FPC is used.
- A minimization of the dead area of the pixel chip allows to reduce the overlap of the staves.
- Ultra-light materials are used for the mechanical support structure and cooling pipes.

Detector readout

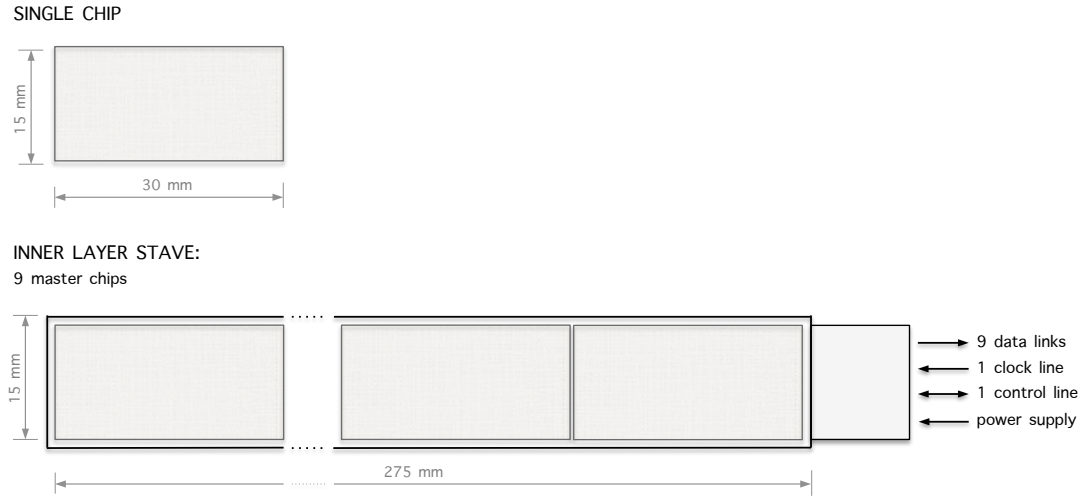
In general, it will be possible to operate the new ITS in two modes: the *triggered mode* and the *continuous mode*. In the triggered mode, the sensors will be read out upon the arrival of the ALICE level zero (L0) trigger, which has a latency of about 1.2 µs [1]. In continuous mode, data will be continuously read out and transmitted off-chip.
The emerging data volume is directly related to the pixel hit density in the detector, which in turn is determined by the experimental running conditions, i.e. the collision system (Pb-Pb or pp) and beam interaction rate. E.g. the maximum hit densities at mid-rapidity

estimated for minimum bias Pb-Pb events at the innermost layer are 19 hits/cm^2 [16]. In the outer layers where the hit density is significantly lower, fake hits caused by electronic noise will contribute significantly to the data rate and can become dominant. The implications of the different operation modes and conditions on the design of the pixel chip is discussed in Chap. 5.

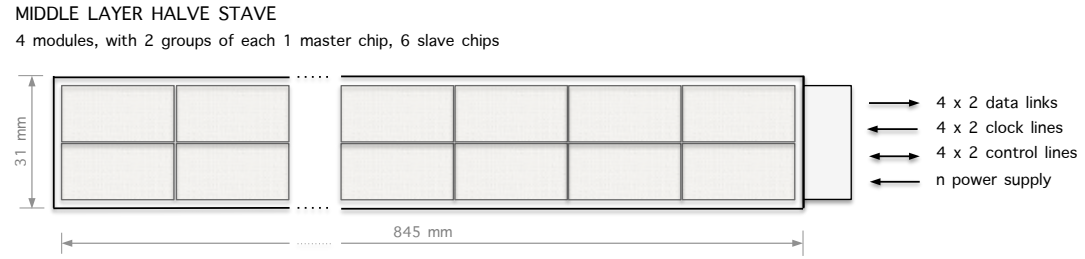
The conceptual layout of the ITS readout system is presented in Fig. 2.4: the staves are housed inside the detector barrel and connected via electrical signal connections and power cables to the readout and power units, respectively, placed in the ALICE miniframe. There, the ITS on-detector electronics are interfaced with the data acquisition (DAQ), trigger and detector control systems (DCS) of ALICE.
Due to the substantially different hit densities in the IB and OB layers, the readout is realized in different ways, making use of two different configuration options implemented in the pixel chip. In the inner barrel (cf. Fig. 2.5a), each pixel chip has an independent data output via a single link of 1.2 Gbit/s which is directly connected to the Readout Unit (RU). In the outer barrel staves, being composed of modules integrating 14 pixel chips placed in two rows, a different approach is followed. Here, one chip in each row is configured as a master chip which manages the communication to the RU. The other chips in the row share the local bus to send out their data, where the master chip serves as pass-through with a bandwidth of 400 Mbit/s.

2.2.2. Pixel chip

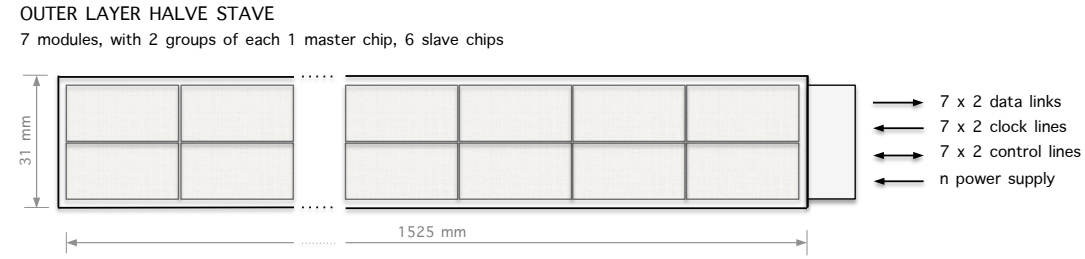
The design objectives together with the operation environment of the upgraded ITS led to the requirements on the pixel chip as presented in Tab. 2.2. In summary, the upgraded ITS has to be equipped with very thin sensors, providing a high granularity; the radiation levels (1.7×10^{13} 1 MeV n_{eq}/cm^2 (NIEL) and 2.7 Mrad (TID) for the innermost layers) and collision rates (50 kHz for Pb-Pb) are moderate compared to other experiments at the LHC. Furthermore, a considerably large area of about 10 m^2 has to be be covered with pixels. This led to the choice of CMOS *Monolithic Active Pixel Sensors* (MAPS) as the technology for all layers.
MAPS have shown a significant progress in recent years, the first large scale application being represented by the STAR PXL detector at RHIC, which is equipped with the ULTIMATE chips [36]. This chip, produced in the AMS 0.35 µm technology, however, does not meet the requirements for the ALICE ITS upgrade in terms of readout time, power consumption and radiation hardness [16]. In order to overcome these limitations, the ALICE ITS upgrade project has chosen a process with smaller feature size and additional process options - the 180 nm CMOS technology by TowerJazz.



(a) Inner layer module.



(b) Middle layer modules and half-staves.



(c) Outer layer modules and half-staves.

Figure 2.5.: Connection of the inner (a), middle (b) and outer layer (c) (halve) staves [35].

Monolithic silicon pixel sensors In present large scale high-energy particle physics experiments, silicon based *hybrid* pixel sensors are applied for the vertexing and tracking in the innermost regions. The term hybrid refers to the physical separation of the sensitive layer, i.e. the *sensor*, from the CMOS based readout chip, which are attached to each other by use of fine pitch bumb-bonding (cf. Fig. 2.6).
The advantage of this technology is that the sensitive layer and the chip containing the front-end and readout logic can be optimized separately. Even other materials than silicon, e.g. GaAs or diamond, can be used as sensitive layer. In addition, large bias voltages

Table 2.2.: General specifications of the ITS pixel chip [16].

Parameter	**Inner Barrel**	**Outer Barrel**
Chip dimension	$15 \times 30\,\mathrm{mm}^2$ ($r\phi \times z$)	
Max. silicon thickness	50 µm	
Max. power density	$300\,\mathrm{mW/cm}^2$	$100\,\mathrm{mW/cm}^2$
TID radiation hardness[a]	2.7 Mrad	10 krad
NIEL radiation hardness[a]	$1.7 \times 10^{13}\,1\,\mathrm{MeV\,n_{eq}/cm}^2$	$3 \times 10^{10}\,1\,\mathrm{MeV\,n_{eq}/cm}^2$
Operation temperature	20 °C to 30 °C	
Max. integration time	30 µs	
Max. relative dead time	10 % at 50 kHz Pb-Pb	
Min. detection efficiency	99 %	
Max. fake hit rate	10^{-5}/event/pixel	
Spatial resolution	5 µm	30 µm

[a] This includes a safety factor of ten and has been updated with respect to the reference.

can be applied to the sensitive layer, allowing for its full depletion with large electric fields, leading to an efficient and fast charge collection and large radiation tolerance [4].
However, hybrid pixel sensors also present limitations. They are rather complex to construct due to the bump-bonding and therefore costly. Moreover, they typically yield a relatively large material budget[5].
Monolithic silicon pixel sensors allow for very thin detectors as the sensor and the readout electronics are integrated inside the same silicon die, completely avoiding bum-bonding bonding. CMOS MAPS, of which a schematic cross section is shown in Fig. 2.6, are a particular development in the field of monolithic silicon pixel sensors. For the production of MAPS, standard CMOS processes can be used, which make them potentially very cost effective. So far, compared to hybrid pixel sensors, the main disadvantages have been radiation hardness and charge collection time [39]. For heavy-ion experiments as ALICE, however, the requirements in this regard are less demanding and novel developments as described in this thesis allow to design faster and more radiation hard monolithic chips.

TowerJazz 180 nm CMOS technology The general constituents of a MAPS fabricated in the TowerJazz 180 nm CMOS process are schematically shown in Fig. 2.6. The base layer, i.e. substrate, is a highly doped, low resistivity (in the order of $10\,\Omega\,\mathrm{cm}$)[6] p-type silicon wafer.
On top of it, a high-resistivity (1 kΩ cm to 10 kΩ cm) p-type epitaxial layer with a thickness

[4] Hybrid pixels are proven radiation hard to $1 \times 10^{15}\,1\,\mathrm{MeV\,n_{eq}/cm}^2$ [37].
[5] E.g. the recently installed Insertable B-Layer (IBL) of ATLAS exhibits 1.54 % x/X_0 [38]. The current ALICE Silicon Pixel Detector (SPD) of ALICE exhibits 1.14 % x/X_0 per layer.
[6] Silicon wafers manufacturers usually specify the resistivity ρ of the material, which is related to the doping concentration N by $\rho = \frac{1}{N\mu q}$, where μ is the mobility of the respective carrier.

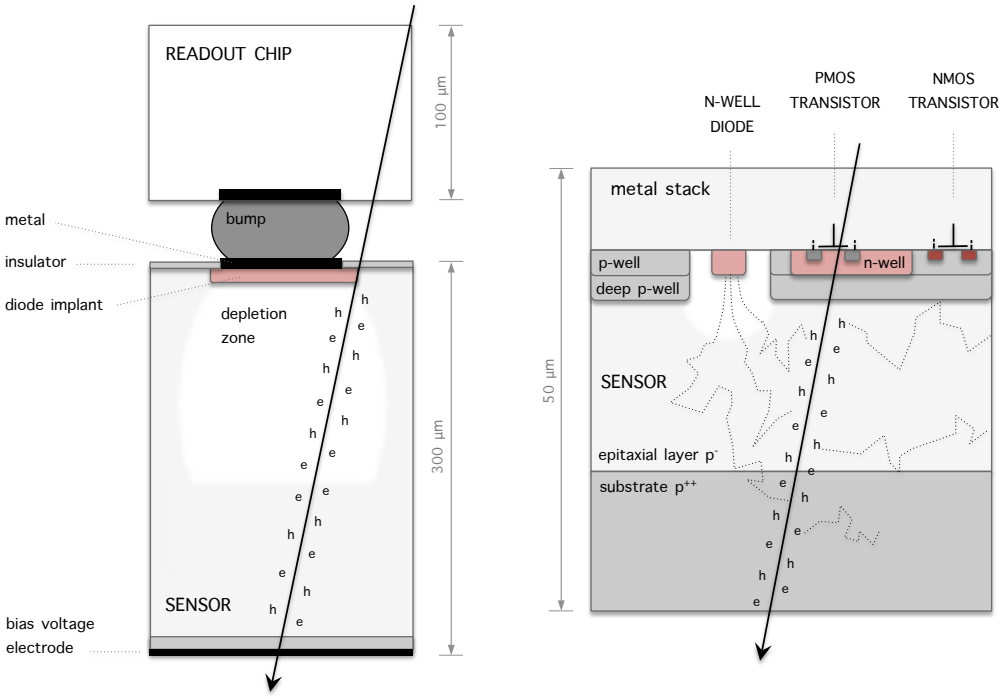


Figure 2.6.: Schematic cross sections through pixel sensors realized in different technologies. Left: *hybrid pixel sensor* - the sensor and the readout chip are separate components. Each charge collection diode (pixel cell) in the sensor is connected via micro-bump bonds to the corresponding cell in the readout chip. Right: *monolithic pixel sensor* - The sensor and the readout circuit are integrated in the same silicon die. The deep p-well is a feature of the TowerJazz 180 nm CMOS process.

in the order of 20 µm is grown by chemical vapour deposition [40][7]. The epitaxial layer, typically only partially depleted, acts as the sensitive layer of the pixel chip. There, the generated charge is constrained by potential barriers at the boundary until it reaches the collection diodes, which are formed between n-wells and the p-type epitaxial layer.
Additional n-well and p-well implantations at the top of the epitaxial layer serve as bulk for the PMOS and NMOS transistors, respectively, of the CMOS circuit. The source and drain of the transistors are formed by diffusion implantations with a higher doping than the wells in which they are embedded into. Metal lines insulated by silicon oxide layers connect the different silicon structures to form the front-end and readout circuits.
In summary, the 180 nm CMOS technology by TowerJazz offers several features that make it particularly suitable for its application in the ITS upgrade [16]:

- **Deep p-well -** In standard CMOS processes, n-wells form the bulk material for PMOS transistors. In the pixel area, however, these n-wells compete with the n-

[7] For uniform charge collection, it is important that the grown epitaxial layer does not exhibit crystal defects in the layer itself nor at the interface with the substrate, i.e. the crystal has to be continuous.

wells intended for charge collection. As indicated in Fig. 2.6, a deep p-well allows to circumvent this problem by shielding the n-wells hosting the PMOS transistors. The availability of a deep p-well hence is a key feature of the process, enabling the implementation of full CMOS logic within the pixel matrix.

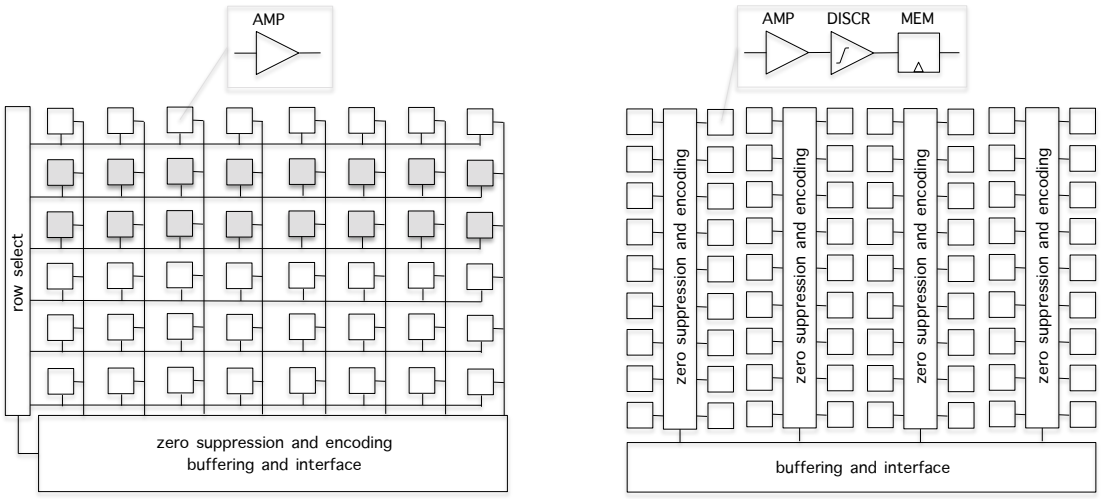
- **Feature size -** The transistor feature size of 180 nm and a gate-oxide thickness of 3 nm makes the process expectedly more resistant to the total ionizing dose (TID) effects [41].

- **Up to six metal layers -** The process allows for up to six metal layers, which in addition to the small feature size allows for the implementation of a high-density, low-power circuitry within the pixel matrix. Furthermore, this permits to reduce the insensitive area of the digital circuitry located at the periphery of the chip.

Even though the process is used as a commercial standard for imaging sensors, its applicability for a use in high-energy physics, and in particular the ALICE ITS upgrade, has to be assessed. In imaging sensors, where visible light is absorbed very close to the top of the sensor, a significant fraction of the sensor surface has to be reserved for the photo-sensitive elements, i.e. photodiodes[8]. Moreover, it is typically desired to read out a full image, i.e. the complete pixel matrix. The charge is typically integrated during the opening of a shutter.
On the contrary, high-energy charged particles generate charge over the full silicon thickness. This allows to employ the full epitaxial layer for charge collection and to cover a large part of the sensor surface with circuitry. Furthermore, it is desired to read out only the pixels hit by a traversing particle. In this context, the image is very sparse, with very low hit densities in the order of a few tens of hits/cm^2 compared to the about 1×10^5 pixels/cm^2 for the new pixel chip of the ITS. The use in ALICE also requires a radiation tolerance of the technology up to levels presented in Tab. 2.2 and the design of efficient circuits that minimize readout time and power consumption.

2.3. Pixel chip R&D

The R&D was started in 2011 with the goal to fully qualify the TowerJazz 180 nm CMOS technology for the ALICE ITS upgrade. This section gives an overview of the the different R&D stages towards the final design of the pixel chip.



(a) MISTRAL. **(b)** ALPIDE.

Figure 2.7.: Schematic layout of the two proposed pixel chip architectures.

2.3.1. The ALPIDE development

The state of the art of MAPS before the start of the pixel chip R&D within the ALICE ITS upgrade is represented by the ULTIMATE sensor for STAR [42], fabricated in the AMS 0.35 µm process. It includes a pixel array of 928 rows and 960 columns with 20.7 µm pixel pitch, covering a sensitive area of about 3.8 cm^2. The ULTIMATE was designed to be radiation tolerant up to levels of 3×10^{12} 1 MeV $\mathrm{n_{eq}}/\mathrm{cm}^2$ (NIEL) and 150 krad (TID) and exhibits a power dissipation of about 150 $\mathrm{mW}/\mathrm{cm}^2$. The chip is based on an architecture referred to as *rolling shutter readout*, where the columns of the pixel matrix are read out in parallel row by row. The discriminators to obtain binary information and the zero-suppression logic are integrated into the end-of-column circuitry.

The advantages of this architecture are the very small number of transistors needed inside each pixel and that it can be implemented with transistors of the same type (NMOS or PMOS). The latter is a requirement in standard CMOS imaging sensor processes as the AMS 0.35 µm (no deep p-well available).

A disadvantage is that the analogue signals from the pixels have to be driven along the columns until the discrimination stage. A further limitation of the rolling shutter architecture is that the time to read out the pixel matrix is fundamentally coupled to the number of rows the shutter (i.e. the row select sequencer) has to pass before returning to the same. For the ULTIMATE chip, having 928 rows and a shutter clock frequency of 5 MHz, the readout time results in 185.6 µs, which does not satisfy the requirements set by the ITS upgrade. Ways to improve this are an increase of the clock frequency for the

[8] The fraction of the surface covered by photo-sensitive elements is referred to as *fill factor*.

row selection, less pixels per column, or reading multiple rows at the same time.
Such an approach is followed by the MISTRAL [43] development (cf. Fig. 2.7a), which takes advantage of the smaller feature size provided by the TowerJazz 180 nm CMOS technology and reads out two rows at once.

The potential of the TowerJazz 180 nm CMOS technology offering the deep p-well and therefore allowing full CMOS circuitry within the pixel matrix, can be further exploited by moving the discriminator into the pixel cell. The advantage of such an approach is that the analog signal is no longer driven over the column lines, hence allowing to reduce power consumption and increase readout speed. The realization of in-pixel discriminators also offers the opportunity of a sparsified readout, in which the digital outputs of the pixels are scanned by an encoder circuit that directly produces the address of hit pixels as output. The circuit works in a way that the pixel hit register is reset after the read operation, whereupon the circuit will move on to the next hit pixel to encode its address. The procedure is iterated until the full pixel matrix is read out. This approach is followed by the ALPIDE [44, 45] development (cf. Fig. 2.7b), which has been selected as the project baseline design. The features of the final ALPIDE chip are presented in Tab. 2.3.

Table 2.3.: Design features of the ALPIDE chip.

Architecture (discriminator, readout)	in-pixel, in-matrix sparsification
Chip dimensions	$15.3\,\text{mm} \times 30\,\text{mm}$
Pixel dimensions	$26.88\,\mu\text{m} \times 29.24\,\mu\text{m}$
Number of pixels (rows × columns)	512×1024
Time resolution	$2\,\mu\text{s}$
Power consumption[a]	$39\,\text{mWcm}^{-2}$
Dead area	$1.1\,\text{mm} \times 30\,\text{mm}$

[a] for the IB layers.

In contrast to MISTRAL, the ALPIDE operates in a *global shutter* mode, which is steered by a global strobe signal. As long as the strobe signal is active, the output of the discriminators will be stored into the local hit register. As soon as the strobe signal is deactivated, the readout of the pixel matrix is initiated. Thereby the encoder circuit only becomes active, i.e. it only consumes power, when hits are present. In general, the strobe can either be activated for a certain time by an external trigger signal, e.g. the ALICE level-zero (L0) trigger, or continuously be kept open. In continuous-integration mode the strobe is only deactivated to advance to the next event. Additional in-pixel hit buffers will allow to acquire consecutive events while the readout of the previous event is still ongoing.
Besides the sparsified readout, an additional distinctive feature of the ALPIDE design is

the possibility to apply an additional reverse bias voltage via the substrate. This allows to significantly increase the depletion zones around the collection diodes, leading to a more efficient charge collection and a reduction of the pixel input capacitance with respect to earlier MAPS.

Low power design The requirement for the material budget of the upgraded ITS (0.3 % x/X_0 for the inner barrel and 1.0 % x/X_0 for the outer barrel) is very challenging. Since the amount of material that is used for the power distribution and cooling directly contributes to the overall material budget of the detection layers, low power consumption is the key to a low material detector.
The contributions to the power consumption of the pixel chip can be attributed to the analogue front-end, the digital circuits for the on-chip data processing and the off-chip data transmission. In terms of the power consumption of the analogue front-end, with a required signal-to-noise ratio (SNR) at a given bandwidth, the ratio Q/C of the collected signal charge and the pixel input capacitance has been identified as a key parameter [39][9], and given special focus during ALPIDE development efforts [46, 44, 47, 48].
However, to fully benefit from a power reduction of the analogue front-end, also the other (digital) contributions are optimized. Currently the contribution for data transmission represents the ultimate limit, as particle hit information, requiring a certain data volume independent of the detector type, has to be transmitted[10].

R&D approach Due to the complexity of the device, the R&D approach has been largely based on exploratory prototypes rather than on simulations. In this context, various small [49, 50, 51, 46, 52] and large scale prototypes [44, 53] have been designed and submitted, each focusing on the optimization of single or few aspects of the final chip.
An overview of the prototypes for the ALPIDE architecture and their purpose and major novel features within the chip development are presented in Fig. 2.8. Since the sensor designs still has to be fully optimized, the R&D phase will continue until the end of 2015. The engineering design review will take place in October 2015, whereupon the start of the mass production of the pixel chips is planned for mid 2016.

[9] The SNR for a given bandwidth is not an exclusive performance criterion, e.g. slew rate can be a speed limitation and may require an increased power consumption.
[10] The power consumption of the data transmission unit also depends on the environment the chip has to operate in, e.g. longer cables involve a larger power consumption.

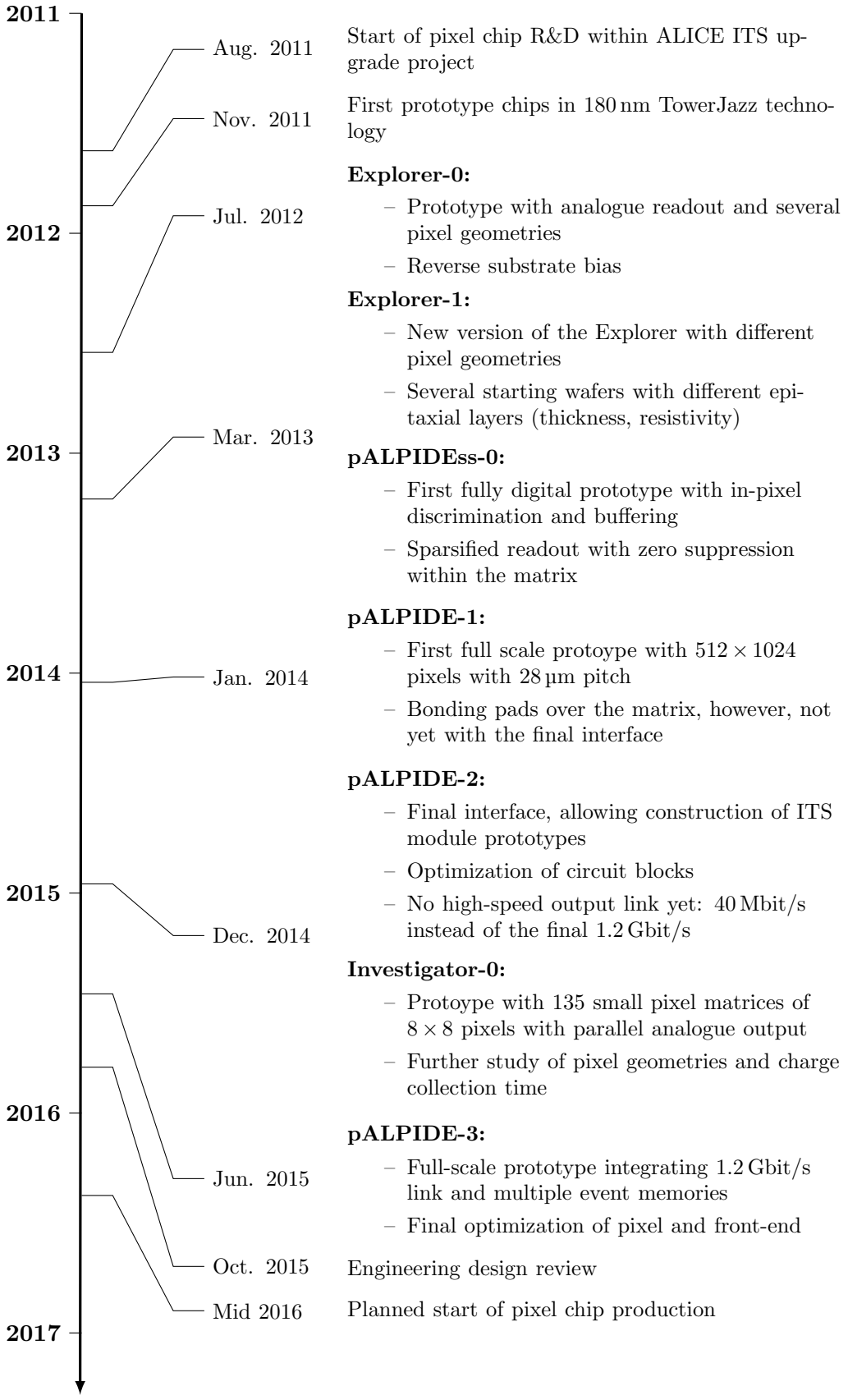


Figure 2.8.: Time line of the R&D for the new ITS pixel chip including the most important prototypes for the ALPIDE architecture.

3. CMOS Monolithic Active Pixel Sensors for the ALICE ITS upgrade

This thesis is built around the development of the monolithic silicon pixel chip for the new ALICE ITS, named ALPIDE, which will be implemented in the 180 nm CMOS process by TowerJazz. This chapter is devoted to the description of the underlying principles of the generation of charge carriers and their collection within the sensitive layer. Furthermore, the formation of a signal at the output of the charge collection electrodes is discussed.

The first part of the chapter is dedicated to a review of the energy-loss mechanisms of charged particles and electromagnetic radiation in silicon. Subsequently, the sensitive layer, including the charge collection elements, i.e. diodes, are described in a quantitative fashion. Further into the chapter, the attainable position resolution of the sensor and radiation damage effects are discussed.
The sensitive layer in the ALPIDE design is only partially depleted, that is, it is only depleted in regions around the collection electrodes. Diffusion therefore plays an important role in the charge collection process. To study the charge collection characteristics of such a partially depleted sensor as function of the pixel and depletion region geometry, a simplified model has been developed, the so-called depletion approximation. The last section of this chapter describes this model and the obtained results from the simulation.

3.1. Charge generation in silicon

The principle of solid state detectors is based on the energy loss of traversing particles or radiation in the sensor material. Part of the energy lost is used for the generation of free electron-hole (e-h) pairs, which by their motion induce a signal current on their respective collection electrodes.
For silicon, the mean energy w required to create a single e-h pair is about 3.6 eV [14], which is in fact more than three times larger than the band gap (1.12 eV). The difference goes into the generation of phonons and eventually will dissipate as thermal energy.
Due to the varying fractions of deposited energy used for charge carrier and phonon generation, the variance of the number of e-h pairs $N_{\text{e-h}}$ generated by a deposited energy

E is reduced by the *Fano factor* F [54] according to

$$\langle \Delta N_{\text{e-h}}^2 \rangle = F N_{\text{e-h}} = F \frac{E_i}{w}. \tag{3.1}$$

For most semiconductors being in the order of 0.1, the Fano factor determines the best possible energy resolution of semiconductor sensors.

3.1.1. Energy loss of charged particles

Charged particles crossing material deposit part of their energy by means of scattering processes with the electrons of the medium, causing an approximately uniform ionization along the path. For particles heavier than electrons, this process is described by the *Bethe-Bloch* formula [14]

$$-\frac{1}{\rho}\left\langle \frac{\mathrm{d}E}{\mathrm{d}x} \right\rangle = 4\pi N_A r_e^2 m_e c^2 z^2 \frac{Z}{A}\frac{1}{\beta^2}\left(\frac{1}{2}\ln\left(\frac{2m_e c^2 \beta^2 \gamma^2 T_{max}}{I^2}\right) - \beta^2\right) \tag{3.2}$$

with:

N_A: Avogrado's number;

z: charge of the traversing particle in terms of unit charge;

Z: atomic number of the absorption medium (14 for silicon);

A: atomic mass of the absorption medium (28 g/mol for silicon);

$m_e c^2$: rest energy of the electron;

r_e: classical electron radius;

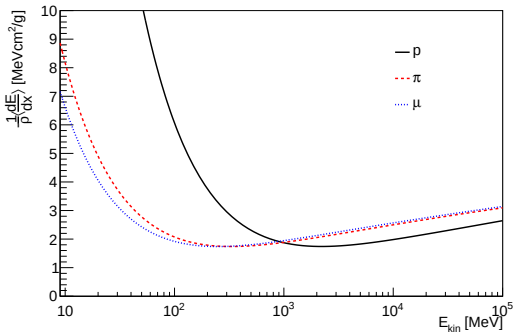
β: velocity of the traversing particle in units of c;

γ: Lorentz factor $1/\sqrt{1-\beta^2}$;

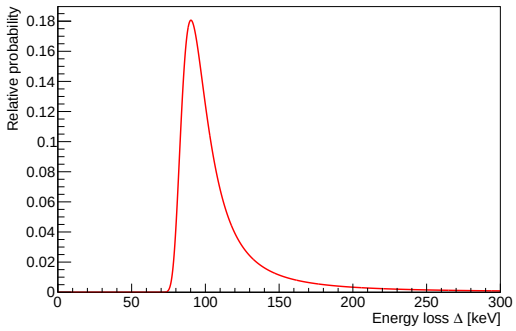
I: mean excitation energy (137 eV for silicon);

$T_{max} = \frac{2m_e c^2 \beta^2 \gamma^2}{1+2\gamma m_e/M+(m_e/M)^2}$: maximum energy loss for a particle with mass M in a single collision;

Eq. (3.2) represents the average differential energy loss per mass surface density, typically expressed in $\left[\frac{\text{MeV}}{\text{g/cm}^2}\right]$. There exist additional correction terms to Eq. (3.2) as the density correction for high particle energies and the shell correction for lower energies [14]. For electrons and positrons additional modifications to the Bethe-Bloch formula are required due to their low mass and the fact that they interact with identical particles (i.e. electrons) while traversing the medium. Furthermore, additional energy-loss mechanisms such as bremsstrahlung have to be considered.



(a) $\frac{1}{\rho}\langle \mathrm{d}E/\mathrm{d}x \rangle$ according to Eq. (3.2) as a function of E_{kin} for protons, pions and muons. The density correction is not considered.

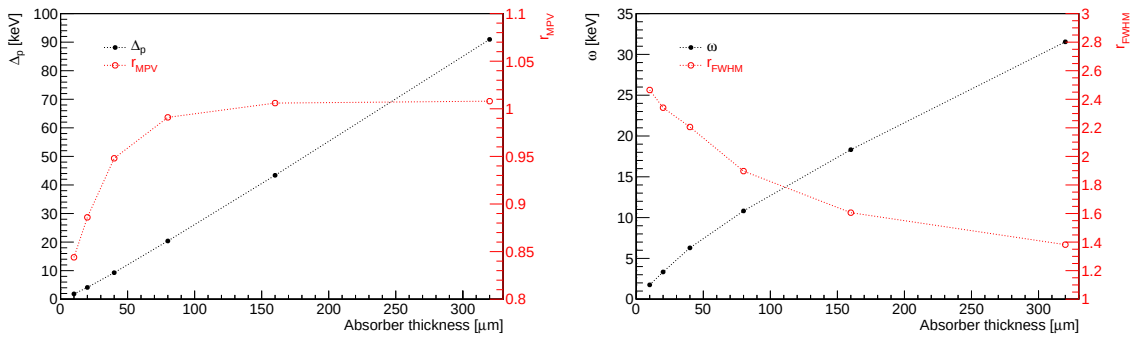


(b) Landau distribution of the energy loss of highly relativistic particles ($\beta\gamma \gg 100$) in a silicon layer of 320 µm thickness.

Figure 3.1.: Energy loss of charged particles.

The dependence of Eq. (3.2) on the properties of the absorbing material is rather weak. At non-relativistic energies, $\mathrm{d}E/\mathrm{d}x$ is dominated by the factor $1/\beta^2$ and decreases with increasing velocity until $\beta \approx 0.96$ (or $\beta\gamma \approx 3$), where a minimum is reached. As can be seen in Fig. 3.1a, the minimum value for $\mathrm{d}E/\mathrm{d}x$ is very similar for all particles of the same charge and therefore particles at this point are generally referred to as *minimum ionizing particles* (MIPs). At larger energies $\mathrm{d}E/\mathrm{d}x$ rises again due to the logarithmic dependence of Eq. (3.2). This *relativistic rise* is eventually flattened, however, by the density correction, leading to a plateau [14].

Landau distribution The Bethe-Bloch formula only provides the mean energy loss $\langle \Delta \rangle$ suffered by a charged particle passing through a layer of material. The amount of energy lost Δ for a particle in a single crossing, however, is subject to statistical fluctuations because of the variations in the number of collisions and in the energy transferred in each collision. The probability density function of the energy loss (*straggling function*) depends on the thickness of the absorbing medium [55]: for sufficiently thick layers such that the number of collisions is large the central limit theorem is applicable and the distribution shows a Gaussian shape around the mean energy loss. In thin layers with less collisions occurring, the situation changes and the fluctuations become larger. Landau was the first to calculate this [56] and hence the probability density function $f(\Delta)$ of the energy loss in thin layers is often only referred to as *Landau distribution*. The Landau distribution shows a long upper tail due to rare, but highly ionizing knock-on or δ-electrons, which obtain sufficient energy during the interaction to become ionizing particles themselves (cf. Fig. 3.1b). As a result of this tail, the mean energy loss $\langle \Delta \rangle$ is larger than the most probable value for the energy loss (MPV or Δ_{MPV}). The scale factor between Δ_{MPV} and the mean energy loss depends on the particle energy, but is typically around 1.3.



(a) MPV. **(b)** FWHM.

Figure 3.2.: Most probable value Δ_p (a) and the full width at half maximum ω (b) of the Bichsel function as a function of the silicon absorber thickness. The graphs with red open symbols show the ratios $r_{\mathrm{MPV}} = \Delta_{\mathrm{p}}/\Delta_{\mathrm{MPV},Landau}$ and $r_{\mathrm{FWHM}} = \omega/\omega_{\mathrm{FWHM},Landau}$ comparing the values resulting from the Bichsel and Landau theories. The graphs are reproduced from data presented in [57] (table V and VI), valid for all particles with charge ± 1 and $\beta\gamma > 500$.

The signal amplitude, i.e. the number $N_{\text{e-h}}$ of electron-hole pairs generated by a traversing particle, can be obtained by dividing the deposited energy by the mean energy needed for ionization (3.6 eV in silicon). The mean deposited energy, however, can differ from the mean energy loss. E.g. in case of thin layers, the deposited energy is less than predicted since a fraction is carried off by δ-electrons leaving the sensor. This effect is described by a modified version of the Bethe-Bloch formula, referred to as *restricted energy loss*.

Very thin absorbers Moreover, for very thin sensor layers ($\lesssim 300\,\mu$m for silicon), as used in MAPS, the Landau model fails to describe the energy loss accurately [14]. In such cases an improved model by Bichsel can be used, which provides good agreement with experimental data down to 10 µm [57]. Fig. 3.2 presents the most probable value Δ_p and the full width at half maximum ω of the *Bichsel function*[1] as a function of the silicon absorber thickness, together with the ratios r_{MPV} and r_{FWHM} comparing the values resulting from the Bichsel and Landau theories. For a silicon layer with a thickness of 20 µm the Bichsel model yields $\Delta_p = 4.12$ keV, corresponding to 1140 e-h pairs or about 60 e-h pairs per µm, and $\omega = 3.34$ keV. The Landau model overestimates the MPV of the energy-loss distribution for thicknesses below about 160 µm (cf. Fig. 3.2a), but significantly underestimates its width (cf. Fig. 3.2b). The broadening can be approximated quite well by the convolution of a Landau density with a Gaussian density with variance δ_2 [58, 59].

[1] According to [57], Δ_p (in eV) is approximated to within 1.2 % for $\beta\gamma > 100$ by $\Delta_p = t(100.6 + 35.35\ \ln t)$ for thickness t between 13 µm and 110 µm. For the same $\beta\gamma$ values the following approximations (within 2 %) are presented for the ω (FWHM): $11 < t < 30$: $\omega = t(174.7 - 2.72\ \ln t)$; $30 < t < 260$: $\omega = t(259.6 - 28.41\ \ln t)$; t in µm.

3.1.2. Energy loss of electromagnetic radiation

Electromagnetic radiation interacts with material mainly via three processes: photoelectric effect, Compton effect, and pair production [14, 60]. In these interactions photons are either scattered by relatively large angles (Compton) or completely absorbed in a single process (photoelectric effect, pair production), the latter being a major difference to the interaction with charged particles. In summary, a monochromatic photon beam traversing a layer of material is not modified in energy but attenuated in intensity according to

$$I(x) = I_0 e^{-x/\lambda} \tag{3.3}$$

where I_0 and $I(x)$ are the beam intensity before and after traversing a medium of thickness x, respectively. The attenuation length, λ is a characteristic property of the material and depends on the photon energy. From the three contributions, the photoelectric effect dominates at energies up to a few tens of keV, whereupon the Compton effect dominates around 1 MeV. For larger energies, pair production becomes dominant.
The primary electron emitted after a photoelectric absorption of an X-ray will generate further e-h pairs along its path. For energies below 10 keV (soft X-rays) the range of the primary electron in silicon ($< 1\,\mu$m for a 6 keV electron [61]) is however small compared to the dimensions of the sensor and the process can be considered rather point-like.
The average number of electron-hole pairs $N_{\text{e-h}}$ generated by a photon with energy E_{ph} can be obtained by considering the average energy necessary to produce a single electron-hole pair, w (3.6 eV in silicon):

$$N_{\text{e-h}} = \frac{E_{ph}}{w} \tag{3.4}$$

In case the electron released through the photoelectric effect does not escape the sensor, photons with a known energy (e.g. from an X-ray source as ^{55}Fe) suit very well for calibration purposes a sensor.

3.2. Sensitive layer and charge collection electrode

3.2.1. Collection diode

As essentially in all silicon sensors, the basic building block of an ALPIDE pixel is a reversely biased diode, i.e. a p-n junction, at which a depletion layer is formed. In the depletion layer, a large electric field is built up that allows the collection of signal charge. In case of the ALPIDE design, the collection diode is realized as a junction between the p-type epitaxial layer (p^-, $N_A \approx 1 \times 10^{12}\,\text{cm}^{-3}$) and an n-well ($n^+$, $N_D \approx 1 \times 10^{17}\,\text{cm}^{-3}$) on its top (cf. Fig. 3.3).

In the following, the behaviour of a p-n junction is introduced by the example of an abrupt, planar junction with constant doping concentration on both sides. It should be kept in mind, however, that for the ALPIDE pixels this represents a strong simplification[2].

At thermal equilibrium, the built up electric field in a p-n junction can be characterized by the so-called *built-in voltage* V_{bi}, which for an abrupt planar p-n junction with constant doping concentration on both sides can be expressed as

$$V_{bi} = \frac{k_B T}{q} \ln\left(\frac{N_D N_A}{n_i^2}\right) \tag{3.5}$$

where N_D and N_A are the effective concentration of donors (n-type) and acceptors (p-type), respectively, n_i is the intrinsic carrier concentration, k_B is the Boltzman constant, q is the unit charge, and T the temperature. The width d of the depletion zone is depending on the doping concentrations on both sides of the junction and can be enlarged by applying an external *reverse bias* voltage V_{RB}. With the same assumptions as used above, one obtains

$$\begin{aligned} d &= d_n + d_p \\ &= \sqrt{\frac{2\epsilon}{q}\frac{N_A}{(N_A+N_D)\,N_D}\,(V_{bi}-V_{RB})} + \sqrt{\frac{2\epsilon}{q}\frac{N_D}{(N_A+N_D)\,N_A}\,(V_{bi}-V_{RB})} \\ &= \sqrt{\frac{2\epsilon}{q}\left(\frac{1}{N_A}+\frac{1}{N_D}\right)(V_{bi}-V_{RB})} \end{aligned} \tag{3.6}$$

where d_n and d_p are the width of the depletion zone in the n- and p-doped region, respectively, and $\epsilon = \epsilon_0\epsilon_{Si}$ is the dielectric constant in silicon[3]. Since the doping concentrations differ by order of magnitudes, the term $1/N_D$ in (3.6) can be neglected, implying that the depletion zone reaches far deeper into the lower doped side of the junction, i.e. the epitaxial layer.
Manufactures of silicon wafers usually specify the resistivity ρ of the material, which is related to the doping concentration N by

$$\rho = \frac{1}{N\mu q} \tag{3.7}$$

where μ is the mobility of the respective carrier[4]. Consequently it follows from Eq. (3.6)

[2] Indeed, the collection n-well diameter is typically much smaller than the pixel pitch and it extends into the epitaxial layer. Moreover, the junction is not abrupt but gradual, exhibiting a certain doping profile.
[3] $\epsilon = \epsilon_{Si}\epsilon_0 = 11.6 \times 8.854 \times 10^{-12}\,\mathrm{F/m} = 1.05 \times 10^{-10}\,\mathrm{F/m}$.
[4] In silicon, the hole mobility is $480\,\mathrm{cm}^2/(\mathrm{Vs})$ [60]. Consequently, p-type material with $\rho = 1\,\mathrm{k\Omega\,cm}$ has an acceptor concentration N_A of about $1.3 \times 10^{13}\,\mathrm{cm}^{-3}$.

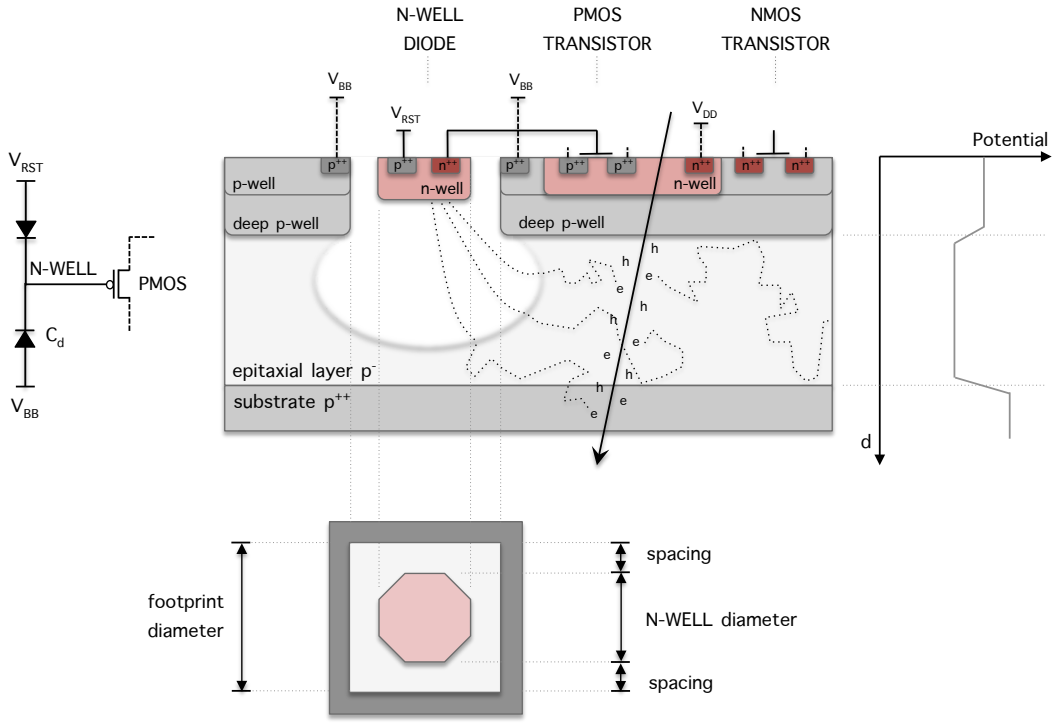


Figure 3.3.: Center top: Schematic cross section of a pixel in the ALPIDE design. Left: equivalent circuit of the input net with a resetting diode, including the charge collection diode and the input transistor. Right: Schematic representation of the potential barriers seen by electrons at the borders of the epitaxial layers formed by three differently p-doped layers p^{++} substrate — p^- epitaxial layer — p^+ p-well. Center bottom: definition of n-well and footprint diameter and spacing to the surrounding p-well.

that

$$d \propto \sqrt{\rho \left(V_{bi} - V_{RB} \right)} \tag{3.8}$$

and hence the depletion region can be enlarged by increasing the reverse bias voltage V_{RB} or increasing the resistivity ρ.

Each reversely biased p-n junction with depletion layer thickness d also constitutes a capacitance C, which is important for the gain and noise behaviour of the sensor. For a planar p-n junction the capacitance can be estimated according to the formula for a parallel plate capacitor by

$$C = \epsilon \frac{A}{d} = A \sqrt{\frac{\epsilon q N_A}{2 \Delta V}} \tag{3.9}$$

with $\Delta V = V_{bi} - V_{RB}$, and is thus determined by the junction area A, the dielectric constant of the sensor material and the depletion layer width[5]. It is important to note

[5] The inverse square root dependence of the junction capacitance on the reverse bias ΔV in the case of an ideal abrupt junction becomes an inverse cube root dependence for a linearly graded doping profile across the junction. In a real junction it typically ranges between these two extremes.

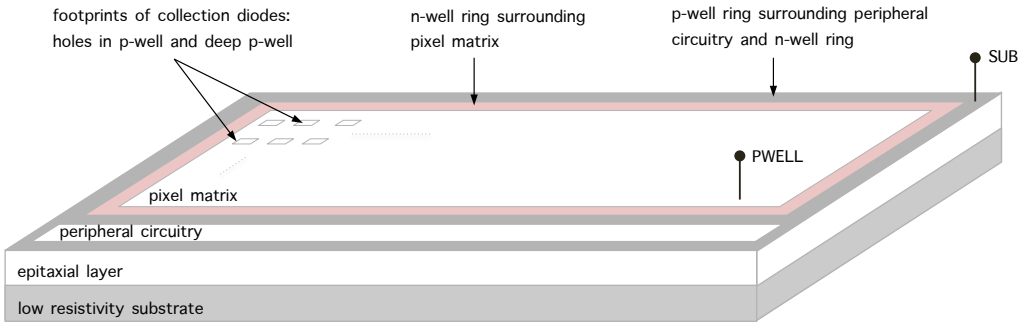


Figure 3.4.: Schematical illustration of matrix isolation and the application of the reverse substrate bias in the ALPIDE design.

that an increase in the reverse bias voltage leads to a decrease in capacitance, as does a decrease of the junction area.

Leakage current If free charge carriers as generated by ionizing radiation enter the depletion region of a reversely biased diode, they will be collected by the respective electrodes by means of drift in the electric field. However, also in absence of radiation there always is a steady current referred to as *leakage current*. It stems from various components, one being the diffusion of free charge carriers from the undepleted sensor volume into the depletion region. The more important contribution, however, is the thermal generation of charge carriers at generation-recombination centers in the depleted volume. Since this contribution is proportional to the depleted volume it is referred to as volume generation current J_{vol}. The volume generation current has a strong temperature dependence [60]

$$J_{vol} \propto T^2 e^{-E_g(T)/2k_BT} \tag{3.10}$$

where E_g is the energy gap defined as the difference between the lower edge of the conduction band and the upper edge of the valence band [6].

3.2.2. Reverse substrate bias in the ALPIDE design

As shown in Fig. 3.3 (left), in case of the ALPIDE design and its prototypes discussed in this work, the total reverse bias voltage V_{RB} on the collection diode is formed by the pixel reset voltage V_{RST}, which also fixes the working point of the input transistor, and the reverse substrate bias voltage V_{BB} applied via the substrate: $V_{RB} \approx V_{\mathrm{RST}} + V_{BB}$ [7].

[6] A useful rule of thumb is that J_{vol} doubles about every 8 K.

[7] In the presented schematic in Fig. 3.3, voltage drops across the reset diode have to be taken into account.

The technical implementation of the reverse substrate bias is illustrated in Fig. 3.4. An n-well ring provides the isolation of the pixel matrix from the rest of the chip. The low resistivity (of the order of 10 Ω cm) substrate is biased through the high resistivity (of the order of 1 kΩ cm to 10 kΩ cm) epitaxial layer by a p-well ring (cf. Fig. 3.4, *SUB*) , which is surrounding the n-well ring and the peripheral circuitry[8]. The p-well and deep p-well within the matrix are biased separately (cf. Fig. 3.4, *PWELL*). However, depending on to which extent the epitaxial layer is depleted, the following cases have to be considered:

- Without full depletion (cf. Fig. 3.5, top and center), as is the case for the chips discussed in this work, there also exists an ohmic connection through the epitaxial layer between the low-resistivity substrate and the p-well. Consequently the in-matrix p-well and the substrate are approximately on the same potential, i.e. V_{BB}.
- In case of a full depletion of the epitaxial layer (cf. Fig. 3.5, bottom), the in-matrix p-well is isolated from the substrate. This allows to apply different potentials.

In case of non-fully depleted epitaxial layer, the reverse substrate bias is also seen by the NMOS transistors in the pixels implemented in the in-matrix p-well (cf. 3.3), forming their bulk terminal. This has a consequence on their operational characteristics, including a threshold voltage shift depending on V_{BB}, which has to be considered in the circuit design. In contrast to the in-matrix circuitry, the peripheral circuitry is implemented in a so-called triple well structure where the n-wells and p-wells are placed inside a deep n-well, and is therefore isolated from the substrate by the deep n-well (connected to $VDDA = 1.8\,\mathrm{V}$) to epitaxial layer (connected to $SUB \lesssim 0\,\mathrm{V}$) diode. The characteristics of the peripheral circuitry are thus not influenced by changes of the reverse substrate bias V_{BB}. Within the matrix the deep n-well cannot be applied, as it would compete with the collection n-wells for the collection of charge carriers.

Maximum reverse substrate bias In prototype measurements, the maximum applicable reverse substrate bias has been observed to be about $-8\,\mathrm{V}$. Above this voltage, breakdowns of reversely biased p-n junctions within the well structures[9] occur. To ensure a safe operation, measurements have only been performed to a V_{BB} up to $-6\,\mathrm{V}$. However, depending on the collection diode geometry, already at this value a significant fraction of the epitaxial layer can be depleted.

[8] In the ALPIDE, the p-well ring covers about 2 % of the die area. Consequently, the resistance $R_{\text{ring-sub}}$ between the p-well ring and the substrate can be estimated by

$$R_{\text{ring-sub}} = \rho_{\text{epi}} \frac{d_{\text{epi}}}{A_{\text{p-ring}}} \approx 10\,\mathrm{k\Omega\,cm} \frac{25\,\mu\mathrm{m}}{0.02 \times 4.5\,\mathrm{cm}^2} \approx 220\,\Omega. \tag{3.11}$$

Thus, with a conservatively assumed leakage current of 10 pA per pixel, i.e. only about 5 µA over the complete matrix, a resistive voltage drop across the epitaxial layer is negligible and the substrate is indeed biased to the *SUB* potential, i.e. V_{BB}.

[9] E.g. the p-n junction formed by the n^{++} implant of an NMOS transistor and its p^{+} (p-well) bulk.

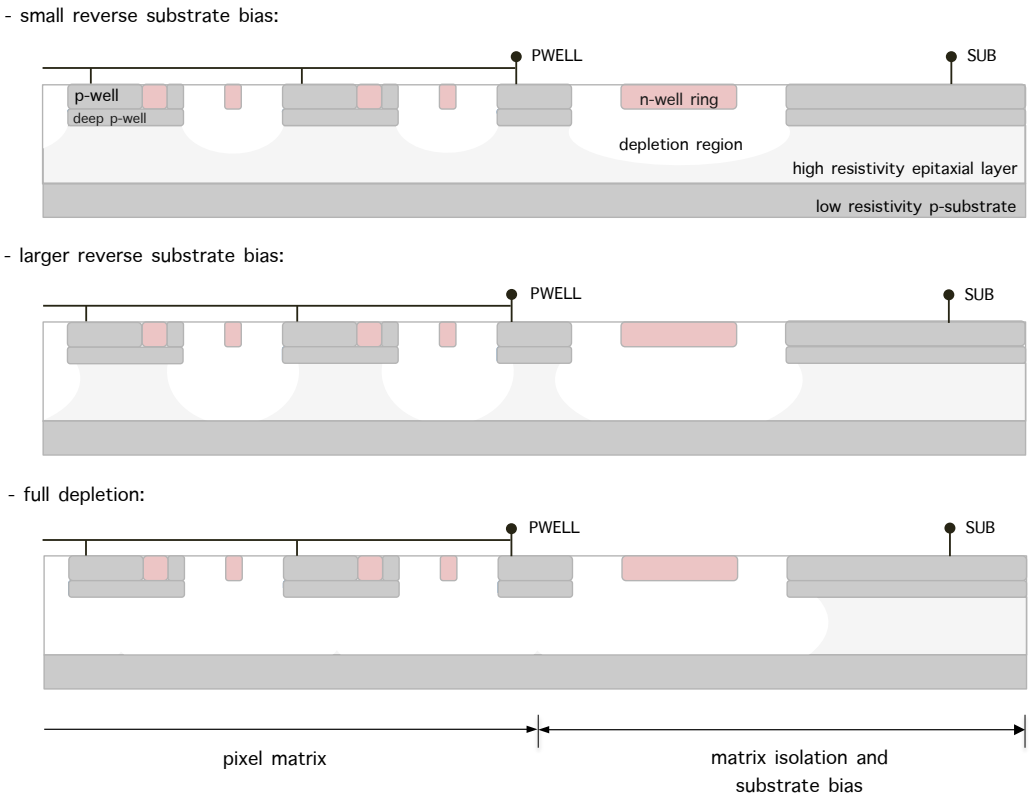


Figure 3.5.: Schematical cross sections through the ALPIDE die for different values of the reverse substrate bias.

3.2.3. Sensitive layer

In the ALPIDE pixels the signal charge is collected by n-well implants, around which a depleted region is formed; an increase of the reverse bias voltage induces an enlargement of the depletion volume. However, in the current architecture the fraction of the pixel area covered by the CMOS circuitry is too large to fully deplete the sensitive layer at reverse bias voltages below $-8\,\mathrm{V}$. Hence, diffusion plays an important role in the charge collection process. Thereby, the relatively long lifetime of the charge carriers in the epitaxial layer of about 1 ms [62][10] is exploited.

A sandwich structure formed by three differently p-doped layers (p^{++} substrate — p^- epitaxial layer — p^+ p-well) is used to guide the diffusing electrons to the depletion regions around the collection n-wells. The central high-resistivity epitaxial layer acts as the sensitive volume, the p^+-p^- junctions at its boundaries forming electric fields that act as reflective barriers (cf. Fig. 3.3, right). Similar to Eq. (3.5), the electric fields can be

[10]The carrier lifetime deteriorates after irradiation, see Sec. 3.5.

characterized by the respective built-in voltages

$$V_{bi} = \frac{k_B T}{q} \ln\left(\frac{N_{A,p^+}}{N_{A,p^-}}\right). \tag{3.12}$$

The factor $k_B T/q$ in Eq. (3.12) is also often referred to as *thermal potential* and yields 25.6 mV at 300 K. In order for the charge carriers to be reflected by a potential barrier, it has to be higher than $k_B T/q$. Therefore the factor $\ln\left(N_{A,p^+}/N_{A,p^-}\right)$ is of interest. For the two potential barriers at both sides of the epitaxial layers the following values are obtained:

- Substrate — epitaxial layer: in the substrate the effective doping concentration is about $N_{A,sub} \approx 1 \times 10^{19}\,\mathrm{cm}^{-3}$, while in the epitaxial layer $N_{A,epi} \approx 1 \times 10^{12}\,\mathrm{cm}^{-3}$, resulting in $\ln\left(N_{A,p^+}/N_{A,p^-}\right) \approx 16.1$.
- Epitaxial layer — p-well: in the p-well the effective doping concentration is about $N_{A,p-well} \approx 1 \times 10^{16}\,\mathrm{cm}^{-3}$, resulting in $\ln\left(N_{A,p^+}/N_{A,p^-}\right) \approx 9.2$.

Both interfaces can thus indeed be assumed to act as perfect mirrors for electrons which diffuse at thermal velocities. They will therefore continue diffusing in the epitaxial layer until they happen to approach a collection n-well (or get trapped). Entering the depletion region, the electric field causes them to drift towards the collection electrode whereupon they are stored on the pixel-input capacitance.
In addition to the electrons generated in the epitaxial layer, also part of the electrons produced in the highly doped substrate will be able to reach the epitaxial layer. Thereby, the probability depends on the lifetime in the substrate[11] and the path length to reach the epitaxial layer [63].
Since diffusion plays an important role in the charge collection process, the charge carriers created by an ionizing particle crossing the sensor are usually shared among several collection diodes (i.e. pixels), even for particles tracks perpendicular to the sensor surface[12]. The characteristics of the charge sharing effects are thereby determined by the geometry of depletion volume, i.e. the regions where the charge carriers are essentially only collected by means of drift.

The working principles lined out above were based on simplified models assuming abrupt, planar junctions between the regions with different doping concentrations. Fig. 3.6 presents the effective doping concentration (N_{eff}) profiles as a function of the wafer depth for various wafer types used throughout the ITS pixel chip R&D. The wafers were fully processed, i.e. with a p-well and a deep p-well on top of the epitaxial layer. As can be

[11] Related to the large doping concentration present, the lifetime in the substrate is typically very small, in the order of 10 ns [63].
[12] Besides due to diffusion, charge sharing may occur due to capacitive coupling, Lorentz shift or simply because of inclined tracks [60].

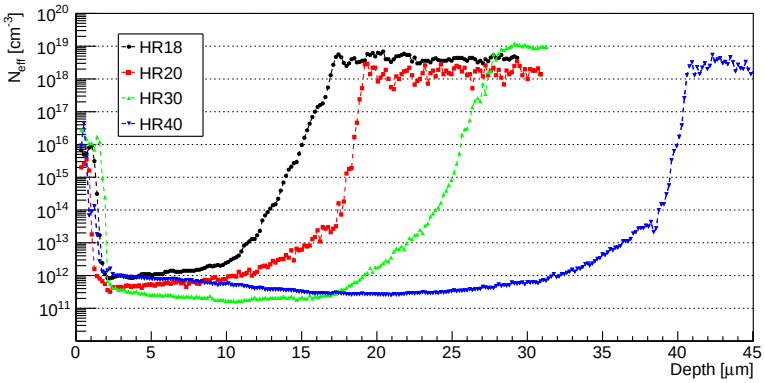


Figure 3.6.: Effective doping concentration N_{eff} profiles as estimated from a Spreading Resistance Profiling (SRP) measurement of the resistivity [64]. Data are presented for various wafers types used within the ITS upgrade pixel chip R&D. The nominal epitaxial layer thicknesses are 18 µm (HR18), 20 µm (HR20), 30 µm (HR30) and 40 µm (HR40), respectively. The wafers were fully processed, i.e. with a p-well and a deep p-well. It should be noted that the SRP probe used for the measurement was only fully calibrated for resistivities below 1 kΩ cm, i.e. $N_{eff} \gtrsim 1.3 \times 10^{13}\,\mathrm{cm}^{-3}$.

observed, there is no abrupt, but a rather gradual change in N_{eff}, especially at the interface between the epitaxial layer and the substrate. Therefore, depending on the gradient of N_{eff}, reflective electric fields[13] at the interfaces may extend far into the epitaxial layer, reducing the field-free diffusion region from approximately the thickness of the epitaxial layer to a layer with an effective thickness d_{eff}. Such a reduced effective diffusion layer thickness is expected to lead to smaller charge collection times compared to the case of abrupt junctions, and less charge sharing between the pixels.

[13] For the p-type epitaxial layer, an expression for the electric field $\boldsymbol{E}$ as a function of a doping concentration gradient can be derived reminding that Eq. 3.16 is also valid for describing the carrier motion in a semiconductor at equilibrium. Considering however, that at equilibrium the net current is zero and substituting p with $N_{eff}(z)$, z being the wafer depth, the equation for the z component E_z yields

$$J_z = 0 = q\mu_h N_{eff}(z) E_z(z) - qD_h \frac{\partial N_{eff}(z)}{\partial z}, \tag{3.13}$$

and using the Einstein relation it follows that

$$E_z(z) = \frac{k_B T}{q} \frac{1}{N_{eff}} \frac{\partial N_{eff}(z)}{\partial z}. \tag{3.14}$$

3.3. Transport of charge carriers and signal generation

3.3.1. Description of charge carrier transport

As lined out in the previous section, the transport of free charge carriers in silicon occurs by means of *diffusion* and *drift*. In the absence of external electric fields, the carriers can be considered as free particles moving in random directions and scattering with silicon lattice or impurity atoms. Their mean free path is in the order of 0.1 µm, corresponding to a mean free time between two collisions of about 1 ps [60]. In silicon at room temperature, the mean thermal velocity of electrons is about 1×10^5 m/s. In equilibrium, the traveled distance, averaged over many charge carriers, is zero. However, in case of a gradient of the carrier concentration $\boldsymbol{\nabla} q$, as it can be introduced by ionizing radiation, the random motion will yield a net transport of the charge carriers. This diffusion process hence results in a net current in the direction opposite to the concentration gradient.
The presence of an external electric field $\boldsymbol{E}$ leads to an additional drift of the carriers with a velocity $\boldsymbol{v}$ determined by

$$\boldsymbol{v} = \mu \boldsymbol{E} \tag{3.15}$$

where μ is the carrier mobility[14]. The carrier flow due to drift and diffusion in summary gives rise to current densities for electrons and holes that can be expressed as

$$\boldsymbol{J}_n = q\mu_e n \boldsymbol{E} + qD_e \boldsymbol{\nabla} n \quad \text{and} \quad \boldsymbol{J}_p = q\mu_h p \boldsymbol{E} - qD_h \boldsymbol{\nabla} p \tag{3.16}$$

where $\boldsymbol{J}_n$ and $\boldsymbol{J}_p$ are the net current densities for electron and holes, respectively, and n and p are the electron and hole concentrations. The first part each in Eq. (3.16) describes the drift current, the second part the diffusion current. D_n and D_p are the diffusion constants of electrons and holes, respectively, which are related to the mobility by the Einstein relation [65]

$$D = \frac{k_B T}{q} \mu. \tag{3.17}$$

3.3.2. Signal generation

The formation of a signal at the output of the charge collection electrode is described by the Ramo theorem [66], according to which the instantaneous current i induced on an

[14] $\mu = q\tau_c / m_{eff}$, where τ_c is the mean free lifetime and m_{eff} is the effective mass of the respective carrier (electron or hole). In silicon electrons and holes have a mobility of $1415\,\mathrm{cm}^2/(\mathrm{Vs})$ and $480\,\mathrm{cm}^2/(\mathrm{Vs})$, respectively [60]. Electrons are thus almost three times more mobile than holes, which makes the holes more prone to trapping, particularly in irradiated material.

electrode by the movement of a charge e with velocity $\boldsymbol{v}$ is given by

$$i = e\boldsymbol{E}_w \cdot \boldsymbol{v} \tag{3.18}$$

where $\boldsymbol{E}_w$ is the so-called *weighting field*[15]. In contrast to the electric field $\boldsymbol{E}$, which determines the drift velocity $\boldsymbol{v}$, the weighting field describes the coupling of the induced current by a moving charge to the respective electrode. Therefore, a signal is already measurable before the first charge carriers are collected on the readout electrodes.
However, when all the charge has arrived at the collection electrodes, the integral of the induced signal current at a single electrode equals the charge collected Q_{col} at the respective electrode. This fact is of practical interest for sensors with integration times much larger than the charge collection times, as is the case for the sensor discussed in this work[16].

In the ALPIDE design, the first stage of the amplification circuit relies on a small capacitance, the so-called *pixel-input capacitance* C_p. It is predominantly formed by the junction capacitance of the collection diode C_d, and parasitic contributions of the routing lines and input transistor, summarized in C_{rt}. During operation, this capacitance is initially charged to a potential V_{RST}. If subsequently the collection diode collects a certain amount of charge Q_{col}, a discharge of the capacitance will take place, leading to a voltage drop

$$\Delta V_{\mathrm{col}} = \frac{Q_{\mathrm{col}}}{C_p}. \tag{3.19}$$

A more precise analysis also has to include the change of the collection diode capacitance C_d during the charge collection. The bias dependency of C_d gives rise to a non-linearity of the *charge-to-voltage conversion gain* as a function of the collected charge Q_{col}. However, this non-linearity is reduced to some extent by the contribution C_{rt}, which exhibits a linear behaviour. Furthermore, the change in the reverse bias voltage ΔV_{col} has to be put in perspective to the total reverse bias voltage. In summary, the following considerations can be made for the pixels of ALPIDE prototype sensors:

- The contribution C_{rt} is typically in the order of 1.5 fF.
- At zero reverse substrate bias, the total reverse bias of the collection diode consists only of V_{RST}, which is typically set to values between 0.7 V and 0.8 V (at maximum 1.8 V). The total input capacitance for such bias conditions is in the order of 5 fF. Considering, e.g. the collection of all 1640 electrons created by a 5.9 keV X-ray from

[15] The weighting field $\boldsymbol{E}_w$ is calculated by setting electrode k to unit potential and all others to zero and solving the corresponding Laplace equation. It is related to the *weighting potential* Φ_w by $\boldsymbol{E}_w = \Delta\Phi_w$.
[16] The integration time of the ALPIDE architecture is in the order of 2 µs, whereas charge collection times can reach values up to several hundreds of ns (see Sec. 3.6.3 and [63]).

an ^{55}Fe source, the voltage drop ΔV_{col} yields approximately 50 mV. Combining Eq. (3.8) and Eq. (3.9)[17], it follows that $C_d \propto 1/\sqrt{V_{bi} - V_{RB}}$. Hence the voltage drop of 50 mV at a total reverse bias of 0.7 V would lead to an increase of the junction capacitance by approximately 3.5 %.

- At −6 V reverse substrate bias, the total input capacitance can be as low as 2 fF. For this case, similar considerations as above yield a voltage drop ΔV_{col} of approximately 130 mV, leading to an increase of the junction capacitance by approximately 1 %.

Thus, the change of the collection diode capacitance C_d following the collection of charge generated by impinging particles can in good approximation be neglected.

Optimizing the ratio Q_{col}/C_p ratio is the main design goal of the small-scale prototype sensors with analogue readout discussed in Chap. 4.

3.4. Position resolution

The position resolution, i.e. the mean error of the position reconstruction, of a pixel sensor is depending on the pixel pitch p, the type of readout (analogue or binary) and the charge sharing characteristics of the sensor.
In the case of a binary readout, only the hit information is available. Thereby, the number of pixels that register a hit also depends on the threshold applied for the signal discrimination. If the configuration is such that only single pixels register a crossing particle[18], the position resolution σ_p is given by[19]:

$$\sigma_p = \frac{p}{\sqrt{12}}, \tag{3.20}$$

which for sensor with a pitch of 30 µm results in $\sigma_p = 8.7$ µm. The position resolution can be improved if in case of charge sharing the configuration allows several adjacent pixels to register a hit, their number and topology depending on the impact position of the ionizing particle.
A further improvement of the position resolution can be obtained with an analogue readout of the sensor that provides a signal proportional to the collected charge in each pixel. Assuming the charge sharing is linearly dependent on the impact position, a center of gravity algorithm can be used for its reconstruction. However, if this assumption is not accurate, as is for instance the case for pixels of the ALPIDE development, the use of more

[17] It should be kept in mind that Eq. (3.8) and Eq. (3.9) are based on the assumption of a planar abrupt p-n junction.
[18] At this point it is assumed that the responding pixel is the one crossed by the impinging particle
[19] In fact, this is only true for a uniform distribution of the particle impact positions within the pixel, which is typically the case.

elaborate interpolation methods, e.g. the η-algorithm [67] is beneficial. The precision of the interpolation methods is a function of the signal-to-noise ratio (SNR) of the detector.

3.5. Radiation damage effects

Pixel sensors are used in tracking devices in the innermost regions of high energy physics experiments. As such, the high particle fluence related to high collision rates and track densities can lead to considerable damage of the sensors and electronics. Radiation induced effects are usually subdivided into bulk and surface defects. The former are induced by the displacement of lattice atoms due to non-ionizing energy loss, while the latter include the effects of ionizing radiation on the dielectrics and the silicon-dielectric interface at the sensor surface.

The following radiation induced effects are expected to occur in the ALPIDE:

- **Bulk damage -** Bulk damage is caused by the inelastic displacement of nuclei in the sensor, producing imperfections in the crystal structure that introduce additional energy levels within the silicon bandgap that may change the properties of the material. This type of radiation damage is related to hadrons. To allow a comparison of the damage caused by different particle types with different energies, bulk radiation damage is scaled using the *non-ionizing energy loss* (NIEL)[20]. The main effects of radiation induced bulk defects are the following:

  - **Leakage current -** The radiation induced lattice defects lead to an increase of the volume-related leakage current across a p-n junction (cf. Sec. 3.2.1) that is strictly proportional to the equivalent fluence Φ_{eq}

    $$\Delta I = \alpha \Phi_{eq} V \tag{3.21}$$

    where V is the depleted volume and α the *current-related damage rate*[21], which is independent of the type and initial resistivity and the material [60]. An increase of the leakage current leads to an increase of the shot noise, as well as a larger power dissipation of the sensor.

  - **Effective doping concentration -** If the impurity atoms used as doping are involved in the radiation induced crystal defects, it may happen that they become electrically inactive, hence losing their function as donors or acceptors.

[20] Neutrons of 1 MeV are commonly used as reference particles. The damage due to a fluence Φ_{phys} of another particle has therefore to be related to the equivalent fluence Φ_{eq} of 1 MeV neutrons causing the same damage. The energy dependent conversion factor is called *hardness factor* [60].

[21] For silicon at 20 °C α is about 3.9×10^{-17} A/cm.

At the same time, new acceptor or donor states may be created during the radiation induced generation of defects. A quantity describing the difference of all donor and acceptor-like states is the *effective doping concentration* N_{eff}, for which the following fluence dependence is expected:

$$N_{eff}\left(\Phi_{eq}\right) = N_{A,0} \cdot e^{-c_A \Phi_{eq}} - N_{D,0} \cdot e^{-c_D \Phi_{eq}} + b_A \Phi_{eq} - b_D \Phi_{eq} \tag{3.22}$$

with $N_{A,0}$ and $N_{D,0}$ donor and acceptor concentration before irradiation and c_A, c_D, b_A, and b_D constants to be determined experimentally [33].

– **Charge trapping and carrier lifetime -** Crystal defects introduce states that act as trapping centers for charge carriers. As a carrier moves through the sensor material, the probability of encountering a trap is proportional to the elapsed time. A parameter to describe trapping is therefore the carrier lifetime τ[22]. Given a carrier lifetime τ, a certain initial amount of charge generated in a single point, Q_0, will decay so that after a time t the remaining charge is given by

$$Q(t) = Q_0 e^{-t/\tau} \tag{3.23}$$

Thus, if the carrier lifetime decreases to the order of the charge collection time, part of the signal charge gets lost, manifesting itself in a degradation of the charge collection efficiency (CCE) of the sensor.

Bulk damage adds additional traps with a concentration proportional to the equivalent fluence Φ_{eq}. Considering this, the lifetime can be written as

$$\frac{1}{\tau} = \frac{1}{\tau_0} + \frac{\Phi_{eq}}{K} \tag{3.24}$$

where τ_0 is the initial carrier lifetime before irradiation and K is the *silicon damage constant*, which is in the order of $2 \times 10^6\,\mathrm{s/cm^2}$ [33].
This effect is of particular importance in the design of the sensors of the ALPIDE where, depending on the depleted fraction of the sensitive volume, diffusion plays an important role in the charge collection process and collection times may be relatively long (up to several hundred of ns, cf. Sec. 3.6.3, [63]).

- **Surface defects -** Ionizing radiation is scaled in with the *total ionizing dose* (TID). It essentially affects the surface oxide layers as well as the lateral isolation oxides of MOSFET transistors through positive charge carriers trapped in the insulation layers (usually SiO_2) and the generation of interface states at the SiO_2-Si interface.

[22] An underlying assumption is that the thermal velocity $\boldsymbol{v}_{th}$ is large compared to the drift velocity, so that during charge collection the integrated path length is proportional to $\boldsymbol{v}_{th}$.

ct, as discussed in For CMOS pixel sensors, this results in a shift of threshold voltages, an increase of $1/f$ noise and parasitic leakage currents.

Beside the bulk and surface damage, also the following radiation induced effects may occur in the ALPIDE design:

- **Single event upset -** A single event upset (SEU) occurs when sufficient charge is deposited close to a sensitive node in a micro-electronic device, causing e.g. a bit flip in a memory cell or register. This can be the result of a high local ionization by a recoil fragment generated by a nuclear interaction[23].
- **Single event latchup -** Under certain circumstances, an SEU can cause a single event latchup (SEL), a parasitic short circuit that leads to a state of abnormal high-current. This can lead to a loss of device functionality or even a destruction of the circuit by overcurrent.

In order to ensure the full functionality of the ITS pixel chip for the expected radiation environment, comprehensive radiation studies have been carried out using various prototype structures fabricated in the TowerJazz 180 nm technology. A test chip (TID_TJ180) was developed in order to investigate the effects of TID on the threshold voltage and leakage current of various transistor designs. Studies showed no relevant degradation of transistor performance up to 250 Mrad, which is much beyond the values expected for the ALICE ITS upgrade [69]. In addition, a dedicated test chip (SEU_TJ180) has been designed to evaluate the SEU and SEL sensitivity of the technology. First results are reported in [16]. The effect of NIEL on the sensor performance has been characterized using the analogue sensor prototypes of the Explorer and Investigator chip families (cf. Sec. 2.3). The results are presented in detail in Chap. 4.

3.6. A case study - Charge collection in the depletion approximation model

Based on the structure of the MAPS for the ALICE ITS upgrade discussed in the previous sections a simplified model was developed that will be further referred to as *depletion approximation*. In this model it is assumed that the epitaxial layer can be separated into two distinct types of regions (cf. Fig. 3.7): depleted regions around the collection n-wells, and the rest of the epitaxial layer, where no electric field is present and the motion of the charge carriers is purely determined by diffusion.

[23] An important issue related to SEU is also that Phase Locked Loops (PLL) can lose lock, causing the circuit to lose its clock and synchronization with the rest of the system. Since the time to recover from this is expected to be significant [68], it is important to protect the circuit against such SEU.

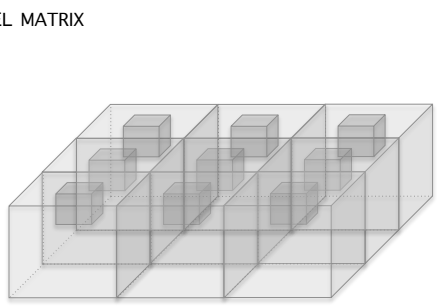


Figure 3.7.: Simulation volume of $n \times n$ pixels, which is divided into depleted regions and diffusion regions.

The model allows a first study of the effects of geometrical parameters as the pixel pitch and the epitaxial layer thickness, and furthermore the depletion volume underneath the collection n-well. The latter is mainly determined by the collection n-well size and the spacing to the surrounding p-well, the reverse substrate bias voltage V_{BB}, and also the epitaxial layer resistivity. Moreover, the simulation results provide a valuable reference for the interpretation of the measurement results presented in Chap. 4.

3.6.1. Model

In the depletion approximation the two regions are attributed with the following characteristics:

- *The depleted part* - This volume is found around the collection n-wells. Within the depleted region the electrical field is strong and points away from the closest n-well. Thus, once entering this region the electrons are instantaneously collected by the corresponding n-well[24].

[24] This can be assumed to be a reasonable approximation, since the transit time of a carrier in the depletion region is much shorter than the times involved with the diffusion process, and the probability for recombination is hence negligible.
To support this, an estimate for the collection time of the electrons by drift shall be given here: the transit time Δt_{trans} can be roughly estimated by considering the depletion zone depth d, as given by Eq. 3.6, and the mean drift velocity $v_{\text{drift}} = \mu_e \langle E \rangle$, where $\mu_e \approx 1415\,\text{cm}^2/(\text{Vs})$ is the electron mobility in silicon and $\langle E \rangle$ is the mean electric field within the depletion zone. Substituting Eq. 3.6 with the values $N_D = 1 \times 10^{17}\,\text{cm}^{-3}$, $\Delta V = 6\,\text{V}$, $\epsilon = 1.05 \times 10^{-10}\,\text{F/m}$, results in $d \approx 89\,\mu\text{m}$, which is larger than the typical epitaxial layer thickness of about 30 µm. The mean electric field can thus be approximated by the reverse bias voltage ΔV and the epitaxial layer thickness d_{epi} to $\langle E \rangle \approx \Delta V / d_{\text{epi}} = 2\,\text{kV/cm}$. With this, the drift velocity results in $v_{\text{drift}} \approx 2.9 \times 10^6\,\text{cm/s}$ and the transit time is consequently given by

$$\Delta t_{\text{trans}} \approx \frac{d_{\text{epi}}}{v_{\text{drift}}} \approx \frac{30\,\mu\text{m}}{2.9 \times 10^6\,\text{cm/s}} \approx 1\,\text{ns}.$$

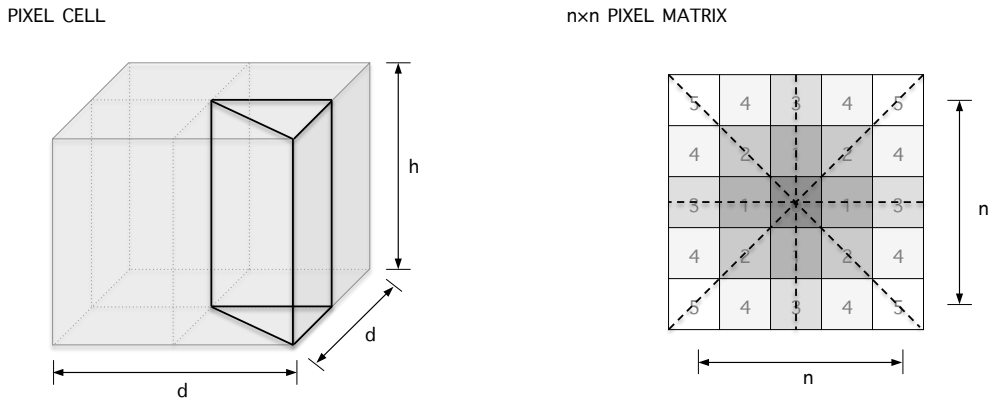


Figure 3.8.: Schematical representation of the employed symmetries. Left: pixel cell, right: $n \times n$ pixel matrix.

- *The rest* - Here no electrical field is seen by the electrons and their motion is described purely by diffusion. Furthermore the epitaxial layer is confined by the substrate on the bottom and the deep p-wells on the top. Both are reflecting.

In summary, in the model the diffusing electrons arriving to the depletion region are simply counted as a function of time, neglecting the Ramo theorem discussed in Sec. 3.3. However, this approximation is reasonable when considering the *small pixel effect* [60]: for pixel detectors where the size of the collection electrode is comparable or even smaller than the sensitive layer thickness, it occurs that the smaller collection electrode size gets, the larger becomes the region in which the weighting potential becomes zero. This is the case for the pixels of the devices discussed in this work, where the epitaxial layer thickness is in the range of 18 µm to 40 µm, while the collection n-well diameter is in the order of only a few µm. This leads to the fact that very little signal is induced on the collection electrode while the charge is moving, while most of the signal is induced in the very last part of the carrier's path. Furthermore charge carriers moving toward the sensor back plane do not contribute significantly to the signal.
The small pixel effect also becomes important in case of irradiated sensors, when a significant part of the charge carriers gets trapped. If the trapping probability is uniform over the sensitive volume, most of the charge gets trapped before reaching regions with a non-zero weighting potential, consequently not being able to induce signal.

3.6.2. Computation

As mentioned above, the motion of the electrons within the epitaxial layer is described purely by diffusion, i.e. the evolution of the electron density n is determined by the

diffusion equation in three dimensions:

$$\frac{\partial n(x,y,z,t)}{\partial t} = D\nabla^2 n(x,y,z,t), \tag{3.25}$$

where D is the diffusion coefficient[25], while obeying the boundary conditions of the model (reflection at epitaxial layer boundary and instantaneous collection at the depletion region boundary).
The model was solved based on a simple discretisation on a uniform grid using the *finite difference method* [70]. In doing so, the electron density $n(x,y,z,t)$ is represented by its values $n^n_{i,j,k}$ at the discrete set of points x_i, y_j, z_l at time t_n

$$\begin{aligned} x_i &= x_0 + i \cdot \Delta l, & i &= 0,\ 1,\ ...\ I \\ y_j &= y_0 + j \cdot \Delta l, & j &= 0,\ 1,\ ...\ J \\ z_k &= z_0 + k \cdot \Delta l, & k &= 0,\ 1,\ ...\ K \\ t_n &= t_0 + n \cdot \Delta t, & n &= 0,\ 1,\ ...\ N \end{aligned} \tag{3.26}$$

where Δl is the *grid spacing* and Δt is the *time step*. With this, Eq. (3.25) can be substituted with the finite difference representation

$$\frac{n^{n+1}_{i,j,k} - n^n_{i,j,k}}{\Delta t} = D\left[\frac{n^n_{i+1,j,k} + n^n_{i,j+1,k} + n^n_{i,j,k+1} - 6n^n_{i,j,k} + n^n_{i-1,j,k} + n^n_{i,j-1,k} + n^n_{i,j,k-1}}{\Delta l^2}\right] \tag{3.27}$$

and $n^{n+1}_{i,j,k}$ results in

$$n^{n+1}_{i,j,k} = \frac{D\Delta t}{\Delta l^2}\left[n^n_{i+1,j,k} + n^n_{i,j+1,k} + n^n_{i,j,k+1} + n^n_{i-1,j,k} + n^n_{i,j-1,k} + n^n_{i,j,k-1}\right] + \left[1 - \frac{6\Delta t D}{\Delta l^2}\right] n^n_{i,j,k}, \tag{3.28}$$

where for stability the coefficient of $n^n_{i,j,k}$ must be non-negative.
For calculations presented in this work $n^n_{i,j,k}$ was set to zero, and consequently the relation of the time step Δt to the grid spacing Δl results in

$$\Delta t = \frac{\Delta l^2}{6D}. \tag{3.29}$$

The same result can also be obtained in a more intuitive way when reconsidering the equivalence of the brownian motion (i.e. random walk) of a particle and a diffusion process [71]. Considering a random walk on a grid for which every time interval Δt each carrier moves by a distance Δl in random direction. After $N = t/\Delta t$ steps, the mean

[25] The diffusion coefficient is related to the mobility μ by the Einstein relation $D = \mu k_B T/q$. Substituting the low field mobility for silicon yields $D_n = 36.6\,\mathrm{cm}^2/\mathrm{s}$ and $D_p = 12.2\,\mathrm{cm}^2/\mathrm{s}$ for electrons and holes, respectively.

square distance from the starting point is

$$\langle r^2 \rangle = N\Delta l^2 \tag{3.30}$$

Comparing this with the well known result of the diffusion equation Eq. (3.25) with the boundary condition $n(x, y, z, t) = n(\mathbf{r}, t) \to 0$ as $x, y, y \to \pm\infty$ and the initial condition $n(\mathbf{r}, 0) = \delta(\mathbf{r})$

$$n(\mathbf{r}, t) = \frac{1}{\sqrt{2\pi\sigma(t)}} e^{\left(\frac{-|\mathbf{r}|^2}{2\sigma(t)^2}\right)}, \text{ with } \sigma(t) = \sqrt{6Dt} \tag{3.31}$$

where $\sigma(t)$ is the mean square carrier displacement as a function of time. Equating it with the result from Eq. (3.30) yields

$$\Delta t = \frac{\Delta l^2}{6D} \tag{3.32}$$

which is the equivalent expression as obtained in Eq. (3.29)[26].

A matrix of 5×5 pixels has been simulated. Considering the available symmetries, the model only has to be solved for one eighth of the grid points of the central pixel (cf. Fig 3.8). Finally, the data obtained from the model is the fraction $Q_\mathrm{i}/Q_\mathrm{tot}$ of the injected charge Q_tot collected in each pixel i of the matrix as a function of time t_n, depending on the position of the charge injection. For the results presented in the following, the least favourable position of charge injection in terms of charge collection and collection time for the central pixel has been considered, i.e. at the bottom of the epitaxial layer, close to the corner between four pixels (cf. Fig. 3.9).

3.6.3. Simulation of charge collection time

The charge collection process has been studied as function of the geometry of the pixels (pixel pitch, epitaxial layer thickness) and the depletion region (volume, width, depth). The details of the in total twelve simulated geometries are schematically shown in Fig. 3.10. All of them approximate realistic cases in the ALPIDE design:

- The depletion volume for a given pixel pitch and epitaxial layer can be varied by varying the reverse substrate bias voltage V_{BB}, the epitaxial layer resistivity, the spacing between the n-well and surrounding p-well, and also the collection n-well size.

[26] The results presented in the next section are computed using a grid spacing of 1 µm, for which the time step for the electron diffusion results in $\Delta t \approx 46.3$ ps.

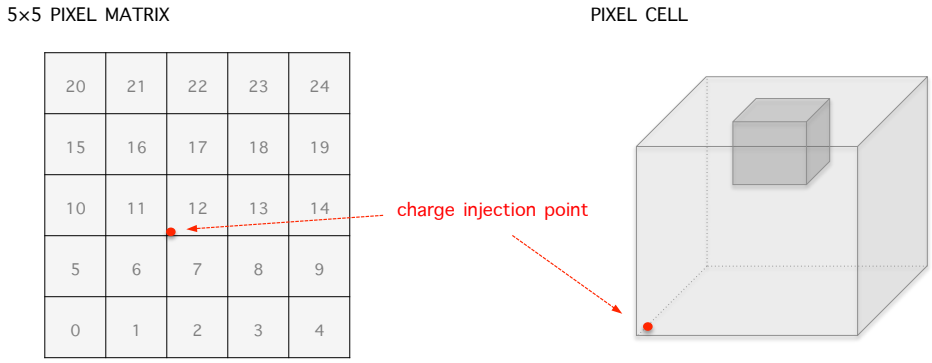


Figure 3.9.: Schematical representation of the position of charge injection, i.e. at the bottom of the epitaxial layer close to the corner between four pixels. Left: position within the pixel cell, right: position within the 5×5 pixel matrix.

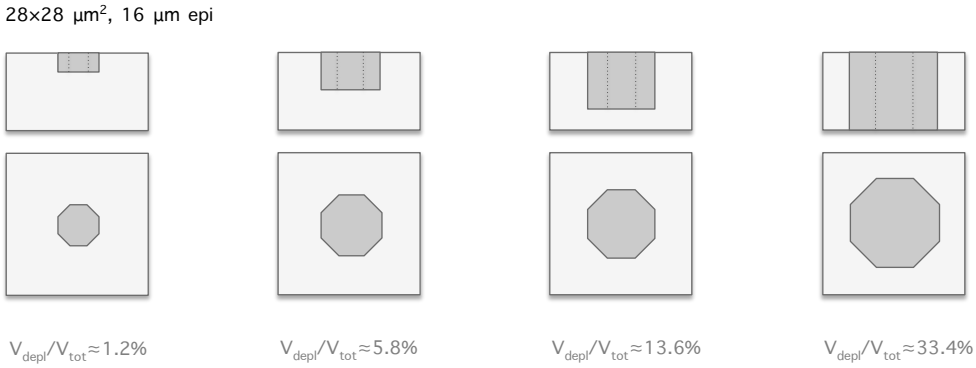
- The simulated epitaxial layer thicknesses of 16 µm, 27 µm and 39 µm are the effective thicknesses extracted from Fig. 3.6 for the wafers with a nominal epitaxial layer thickness of 18 µm, 30 µm and 40 µm, respectively. To study the effects of wafers with a reduced effective diffusion layer thickness, also the case of $d_{\mathrm{epi}} = 8\,\mu\mathrm{m}$ was considered.

- Pixels with the simulated pitches of 20 µm, 24 µm and 28 µm are available in the analogue sensor prototypes discussed in Chap. 4.

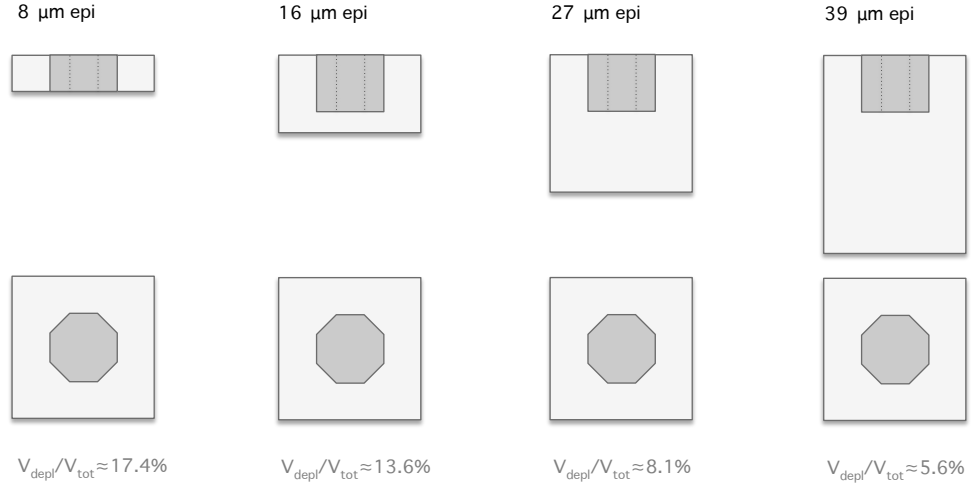
The figures in the left column show the fraction of charge $Q_{\mathrm{seed}}/Q_{\mathrm{tot}}$ collected by the seed pixel as a function of time after the charge injection. The charge collection time, defined as the time required to rise from 20 % to 95 % of the total collected charge in a pixel, is denoted in the legends. The figures in the right column show the corresponding current at the collection n-well of the seed pixel as function of time after the charge injection. The simulation results are discussed in the following:

- Figures 3.11a and 3.11b show the simulation results for different depletion volumes, however, keeping pixel pitch (28 µm) and epitaxial layer thickness (16 µm) constant. As to be expected, both the charge collection process is faster and the fraction of charge collected is larger in case of an increased depletion volume. In case of a relative depletion volume of about 33 %, the obtained charge collection time τ_{coll} is only 21 ns and more than 25 % of the injected charge is collected within the seed pixel. The situation gradually worsens when reducing the depletion volume, where for a relative depletion volume of about 1 % τ_{coll} reaches 171 ns and only about 16 % of the injected charge is collected within the seed pixel.

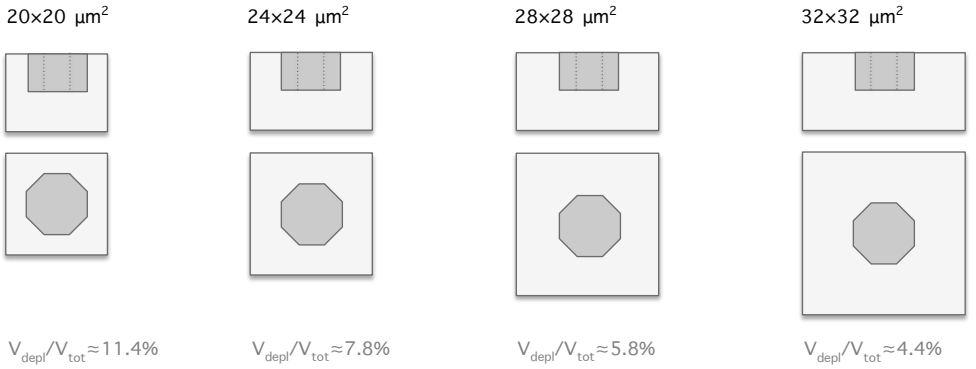
- Figures 3.11c and 3.11d show the results for different epitaxial layer thicknesses d_{epi},



(a) Schematic representation of the simulated pixels with equal pitch (28 µm) and epitaxial layer thickness (16 µm), but different depletion volumes.

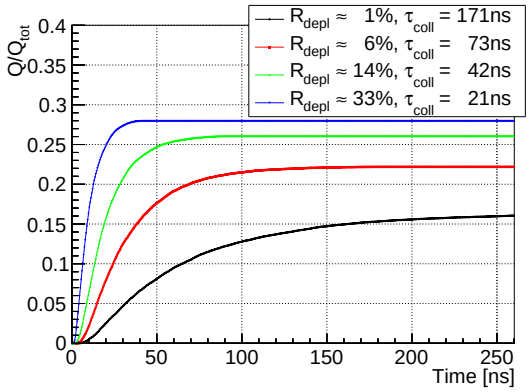


(b) Schematic representation of the simulated pixels with equal pitch (28 µm) and depletion volumes, but different epitaxial layer thicknesses.

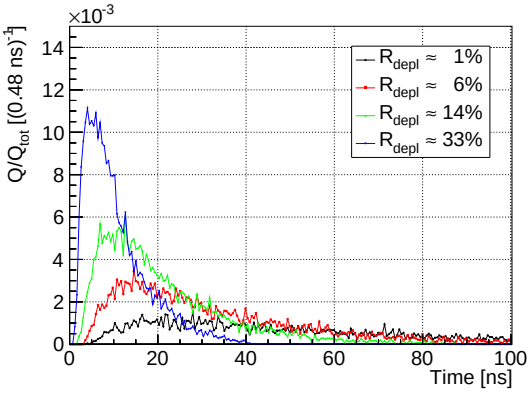


(c) Schematic representation of the simulated pixels with equal epitaxial layer thickness (16 µm) and depletion volume, but different pitch.

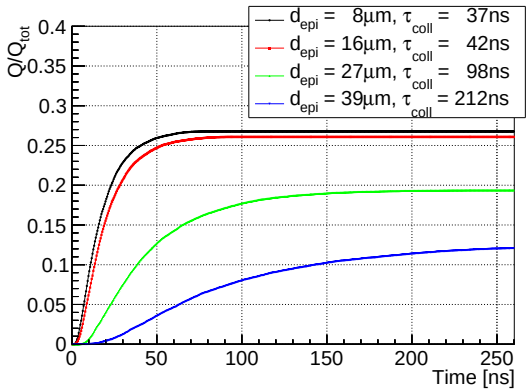
Figure 3.10.: Schematic representation of the simulated pixel volumes.



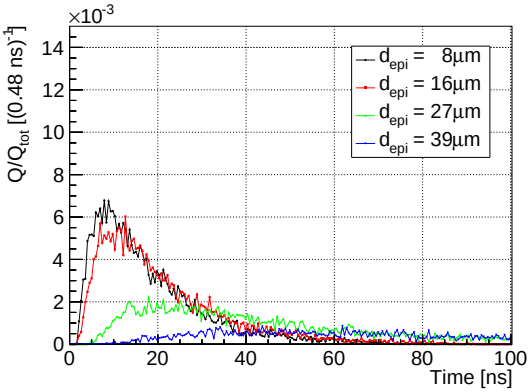
(a) Integrated charge for the different cases presented in Fig. 3.10a.



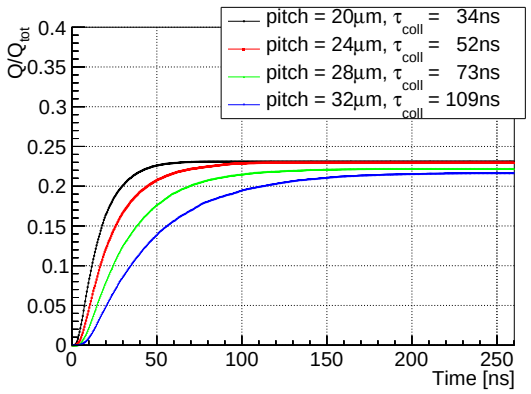
(b) Current for the different cases presented in Fig. 3.10a.



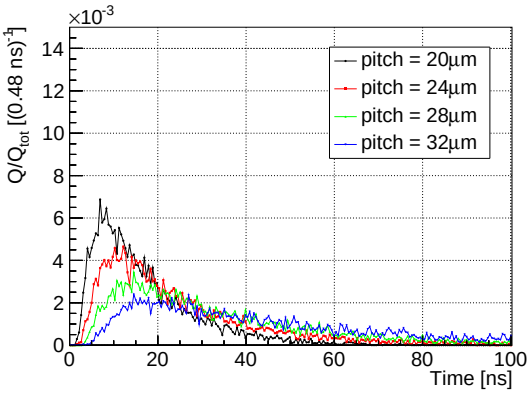
(c) Integrated charge for the different cases presented in Fig. 3.10b.



(d) Current for the different cases presented in Fig. 3.10b.



(e) Integrated charge for the different cases presented in Fig. 3.10c.



(f) Current for the different cases presented in Fig. 3.10c.

Figure 3.11.: Integrated charge and current as a function of time after the charge injection. The charge collection time, defined as the time required to rise from 20 % to 95 % of the total collected charge in a pixel, is noted in the legend of the figures in the left column.

however, retaining the pixel pitch (28 µm) and (absolute) depletion volume. Thus, when varying d_{epi}, simultaneously the relative depletion volume is changed. With increasing epitaxial layer thickness, a larger part at the bottom of the epitaxial layer becomes undepleted, increasingly allowing the charge carriers to diffuse sidewards over long distances before being collected. This effect can clearly be observed, as for $d_{\mathrm{epi}} = 39\,\mu\mathrm{m}$ the charge collected in the seed pixel is about half and the charge collection time is about a factor six larger compared to the case of $d_{\mathrm{epi}} = 16\,\mu\mathrm{m}$.

- Figures 3.11e and 3.11f present the results for different pixel pitches, however, keeping the depletion volume and epitaxial layer thickness (16 µm) constant. For the studied cases with pixel pitches between 20 µm to 32 µm, it can be observed that the fraction of charge collected within the seed pixel is almost constant. However, while the obtained charge collection time is 34 ns for the pixel pitch of 20 µm, it is increased to 109 ns for the pitch of 32 µm.

The distribution of the integrated charge over the pixels of the 5×5 pixel matrix after the completion of the charge collection process is presented in Appendix C. In case of the selected point of charge injection (cf. Fig. 3.9), a large part of the charge is almost equally divided between the four pixels adjoining the point of charge injection. However, depending on the pixel and depletion volume geometry, a significant part of the charge can also diffuse to pixels further away, or even reach the walls of the simulation volume, indicating that in the real case it may get lost for detection.

As mentioned above, this simulation based on the depletion approximation model provides a guidance for the effects to be expected when varying sensor parameters. The related measurement results on the analogue prototype sensors will be discussed in detail in Chap. 4.

4. Optimization of sensitive layer and charge collection electrode

In the ALPIDE design, the sensor and the readout circuits are integrated into the same silicon die, together forming the pixel chip. Even though a physical distinction of the two elements is no longer provided, in the ALPIDE development attempts have been made to optimize the sensor, i.e. the sensitive layer and the charge collection electrode, independently of the readout circuit. In this context, the following parameters have been identified to mainly determine the characteristics and performance of the pixels:

- Pixel pitch
- Epitaxial layer thickness and resistivity
- Collection n-well size
- Spacing between the collection n-well and the surrounding p-well
- Reverse bias voltage on the collection diode

The detailed study of the influence of these parameters on the pixel input capacitance and charge collection process, and subsequently the Q/C ratio, both before and after irradiation, is described in this chapter.
The tools for this study are represented by two dedicated small-scale prototypes with analogue readout - the Explorer-1 and the Investigator-0. These chips provide a large variety of pixel designs (18 in the Explorer-1 and 134 in the Investigator-0) and were processed on different wafers with an epitaxial layer thickness ranging between 18 µm and 40 µm and a resistivity between 1 kΩ cm and 7.5 kΩ cm. A distinctive feature of the Investigator-0 design is that the pixels can be directly connected to the respective output pads, allowing for continuous parallel signal sampling and hence measurements of the charge collection time.

The first part of the chapter is devoted to the common aspects of the prototypes, that are the very front-end part of the readout circuit, including the pixel reset mechanism of the sensing node, and noise sources. This is followed by a part dedicated to the description of the prototype circuits and the methods to calculate the sensor signal and noise. Subsequently, an overview of the sensor characterization methods and observables is given. The later part of the chapter presents the measurement results.

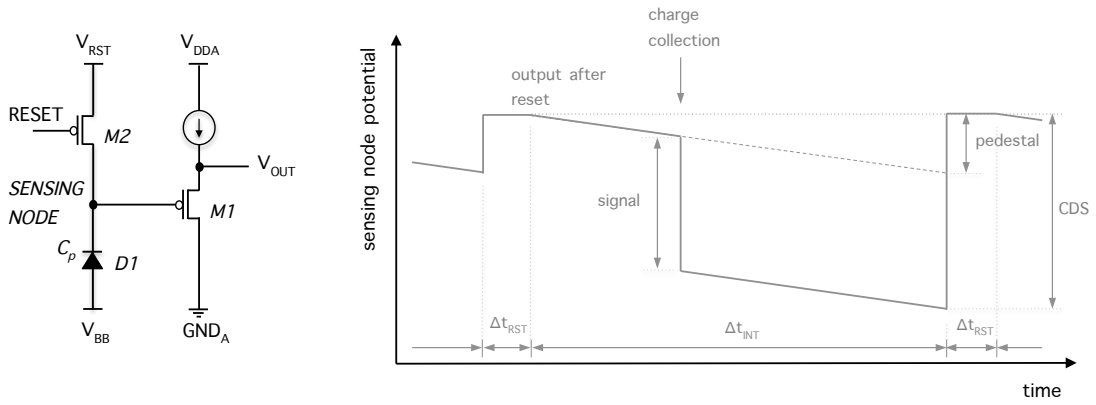


Figure 4.1.: Active reset.

4.1. Common aspects of the small-scale prototypes with analogue readout

4.1.1. Input net

The prototype chips discussed in this chapter share the same very front-end part of the readout circuit, the so-called *input net*, which is formed by the collection diode (D1), a source follower transistor (M1) and a reset transistor (M2). The node connecting the three elements is also referred to as the *sensing node*.

The first source follower (SF) transistor (M1) acts as a buffer, which isolates the sensing node from the readout circuit. The SF gain g_S is approximately unity and ideally the output voltage is proportional to the input voltage: $V_{OUT} = g_S V_{IN}$.
The sensing node is initially set to a potential V_1, that has to be chosen according to the working point of the SF and the subsequent circuitry. Corresponding to the potential V_1, the pixel input capacitance C_p is charged to $Q_1 = C_p V_1$. If subsequently a particle passes the sensor and the collection diode collects a certain amount Q_{col} of the created charge, a discharge of the capacitor will take place. Consequently, the charge stored in C_p will be reduced to $Q_2 = Q_1 - Q_{col}$ and the potential at the sensing node will drop by $\Delta V_{col} = Q_{col}/C_p$ to a value $V_2 = V_1 - \Delta V_{col} = Q_2/C_p$. As a result, assuming constant g_S and C_p, the potential difference at the output of the input net can be expressed as

$$\Delta V_{OUT} = g_S V_1 - g_S V_2 = g_S \frac{(Q_1 - Q_2)}{C_p} = g_S \frac{Q_{col}}{C_p}. \tag{4.1}$$

The output voltage difference is therefore ideally also proportional to the collected charge. Typically, the signal of a pixel is sensed twice, at a time t_1 and after a certain period a

second time at t_2. Within this period, the pixels integrate all collected charge into their capacitance. The period $\Delta t_{INT} = t_2 - t_1$ is therefore also referred to as *integration time*.

4.1.2. Reset of the sensing node potential

There are two processes responsible for the discharge of the sensing node: leakage current and the collection of charge generated by a traversing particle. Since a too strong discharge may bring the sensing node to a voltage outside the operational margin of the readout circuit, mechanisms must be applied to retain stable conditions.
In case of a circuit with an *active reset*, as presented in Fig. 4.1, this is achieved by turning on the reset transistor (M2) and hence connecting the sensing node to the reset potential V_{RST}. This phase is referred to as *reset phase*. If its duration Δt_{RST} is sufficiently long to fully recharge of the pixel capacitance C_p, the sensing node will be at the potential V_{RST}[1]. After the reset phase, the sensing node discharges (due to leakage currents) until the next reset phase, where the potential is restored anew to V_{RST}. The possible collection of charge deposited by a traversing particle is observed as an additional potential drop[2]

4.1.3. Noise

Noise in MAPS is separated into the two categories of *random noise*, or temporal noise (TN), and (fixed) *pattern noise* (FPN). FPN is the spatial variation in pixel output values under uniform stimulus due to device and interconnect parameter variations (mismatches) across the sensor. FPN consists of offset and gain components. However, since FPN exhibits a systematic behaviour it can typically be isolated. For sensors with analogue readout as discussed in this chapter, offline correction methods can be applied (see Appendix D). Temporal noise in MAPS has various sources at all stages of the readout chain [72, 63]. For the prototype chips with analogue readout discussed in this chapter, the main TN contributions can be attributed to their different operation phases, that are reset, integration and readout phase:

- **Reset phase:** The noise introduced by the pixel reset operation - kTC, or thermal noise - is the main contribution to the total noise.

[1] A detailed analysis of the circuit shows that when turning off the reset transistor, a significant amount of charge is injected onto the sensing node. Depending on the pixel capacitance C_p, this leads to the fact that the actual potential at the sensing node after the reset is up to 100 mV larger than V_{RST} for the sensors discussed in this work. See also Fig. D.1.
[2] It should be noted that the described circuit is insensitive to particles during the reset phase.

If the reset phase is sufficiently long to reach equilibrium conditions, its mean square value can be expressed as

$$\langle V_{\mathrm{rst}}^2 \rangle = \frac{k_B T}{C_p}. \tag{4.2}$$

However, if no equilibrium is reached, it can be shown [72] that the expression in Eq. (4.2) is reduced by a factor two.
For the prototypes discussed in this chapter, *kTC* noise can be effectively mitigated by employing a technique referred to as *Correlated Double Sampling* (CDS) [73, 74]. CDS is based on a comparison of two samplings following the reset phase and therefore independent of the noise introduced by the reset operation.

- **Integration phase:** The dominant noise source during the integration phase are leakage currents onto and off the sensing node. Manifesting as shot noise, its mean square value can be expressed as

$$\langle V_{\mathrm{int}}^2 \rangle = \frac{q I_{\mathrm{leak}}}{C_p^2} \Delta t, \tag{4.3}$$

where q is the electric unit charge, $I_{\mathrm{leak}} = \sqrt{\sum_i I_i}$ is the root of the summed squares of the leakage current contributions I_i, C_p is the pixel input capacitance, and Δt the integration time. The leakage current increases after irradiation, consequently leading to a larger contribution of this noise source.

- **Readout phase:** The source follower and switching transistors in the in-pixel circuitry, as well as the column and chip-level circuitry contribute to $1/f$ and thermal noise during the readout [72].

During the integration and readout phase also *random telegraph signal* (RTS) noise [75] in the first (MOSFET) source follower transistors can play an important role. RTS noise originates from modifications of the field applied in field-effect transistors, caused by the presence of defects in the oxide layer. An individual defect can change its charge state by electron/hole capture and emission processes and thereby create an additional field.
In a transistor connected as a source follower, it manifests itself as discrete changes of the pixel output between two or more levels (cf. Fig. 4.2), modulated on top of the previously described noise. While the amplitudes are typically well defined, the period is random and may reach from µs up to minutes. RTS noise depends on various parameters, including temperature [76, 77], and the size [78][3], gate voltage and oxide thickness and type (NMOS

[3] RTS noise is reduced with increasing transistor size. This effect has also been observed at the development step of the front-end circuit design from Explorer-0 to Explorer-1, where the input transistor size was reduced. While for the Explorer-0 the total noise was found to be Gaussian for more than 99.9 %, in the Explorer-1 RTS noise appeared as a significant noise source, affecting a few percent of the pixels [16].

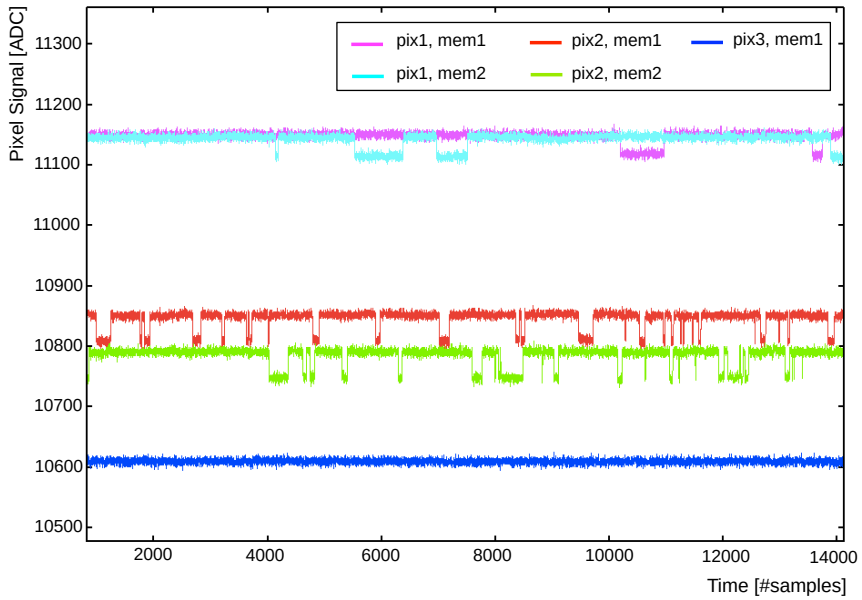


Figure 4.2.: Output signals for selected pixels of the Explorer-1. The discrete changes of the output signals can be attributed to RTS noise.

or PMOS) of a MOSFET transistor [77, 43].

Furthermore, predominantly during the integration, but also during the readout phase *common-mode noise* can occur. Unlike the sources listed above, the common mode is not considered as a noise of individual pixels. It is often dominated by pickup from sources outside the chip.

It should be noted at this point that the front-end circuit of the ALPIDE architecture, differs substantially from the circuits employed in the prototype chips with analogue readout discussed in this chapter: In view of the optimization of the ALPIDE design, the characterization of the total noise performance of the small-scale prototype chips is thus of limited significance. The part of the circuit that is very similar to that of the ALPIDE, however, is the input net. In this context, the assessment of the leakage currents at the sensing node was the main focus of the noise measurements of the prototypes discussed in this chapter.

4.2. Explorer-1

The Explorer-1, an improved version of its predecessor Explorer-0 [46], is intended to further optimize the sensor geometry, as well as to study the effect of applying the reverse substrate bias via the substrate to the collection diode. The chip is segmented into two

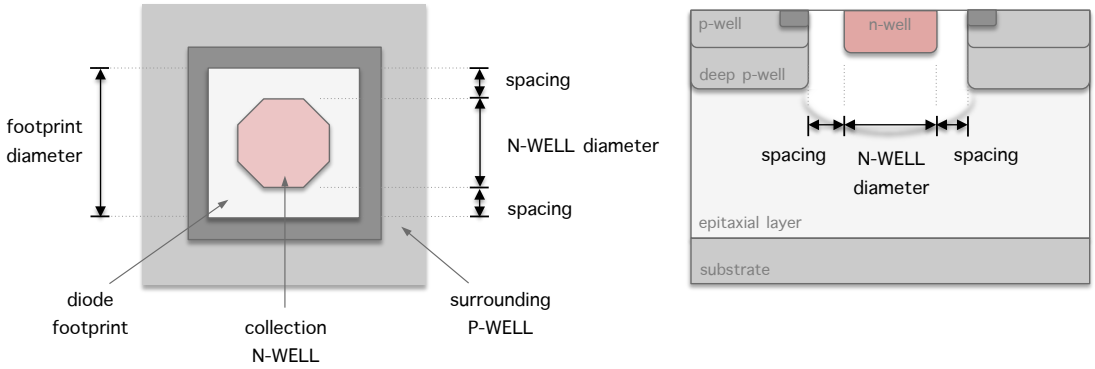


Figure 4.3.: Schematical representation of the collection diode. The p-well opening is referred to as footprint.

Table 4.1.: Comparison of the collection diode geometries of the nine sectors of the Explorer-0 and Explorer-1. The geometries are equivalent for the two pixel pitches.

Explorer-0				Explorer-1			
Sector	Shape	Diameter [µm]	Spacing [µm]	Sector	Shape	Diameter [µm]	Spacing [µm]
1		2	0	1		1.13	3.035
2		3	0	2		2	2.6
3		4	0	3		3	2.1
4		3	0	4		1.13	3.035
5		3	0.6	5		2	2.6
6		3	1.04	6		3	2.1
7		2	1.54	7		1.13	0.635 (top)
8		3	0	8		1.13	0.635 (top)
9		3	1.04	9		2	2.6

Table 4.2.: Features of the epitaxial layers of the different wafer types.

Wafer Type	**Epi Thickness** [µm]	**Epi Resistivity** [kΩ cm]
HR-18	18	> 1
HR-20	20	6.2
HR-30	30	≈ 1
HR-40A	40	≈ 1
HR-40B	40	7.5

pixel matrices with pixel pitches of 20 µm and 30 µm, respectively. Each pixel matrix, in turn, is subdivided into nine sectors with pixels consisting of different collection electrode geometries in terms of collection n-well area and shape and spacing to the surrounding p-well (cf. Fig. 4.3 and Tab. 4.1). The architecture of the Explorer-1 allows to fully decouple the integration and readout time.
In summary, the Explorer-1 allows to characterize the sensor performance depending on the following parameters:

- **Reverse substrate bias of the collection diode:** The Explorer-1 circuitry allows to apply a reverse substrate bias to the collection diode of up to $-6\,\mathrm{V}$[4].

- **Pixel pitch:** The Explorer-1 consists of matrices with pixels of two different pitches: 20 µm and 30 µm.

- **Geometry of the collection diode:** The Explorer-1 pixel matrices consist of nine sectors with each a different collection diode geometry (cf. Fig. 4.1).

- **Epitaxial layer properties:** The Explorer-1 was produced on five different wafers types, each with a different epitaxial layer thickness and resistivity in the range of 18 µm to 40 µm and 1 kΩ cm to 7.5 kΩ cm, respectively.

- **Bulk damage:** A set of Explorer-1 sensors was irradiated with neutron fluences of $2.5 \times 10^{12}\,1\,\mathrm{MeV\,n_{eq}/cm^2}$ and $1 \times 10^{13}\,1\,\mathrm{MeV\,n_{eq}/cm^2}$.

The characterization results are presented in Sections 4.5 and 4.7.

[4] In fact, as discussed in Sec. 3.2.2, the value of reverse substrate bias where breakdowns start to occur is about $-8\,\mathrm{V}$. However, to ensure a safe operation, measurements have only been performed to a V_{BB} up to $-6\,\mathrm{V}$.

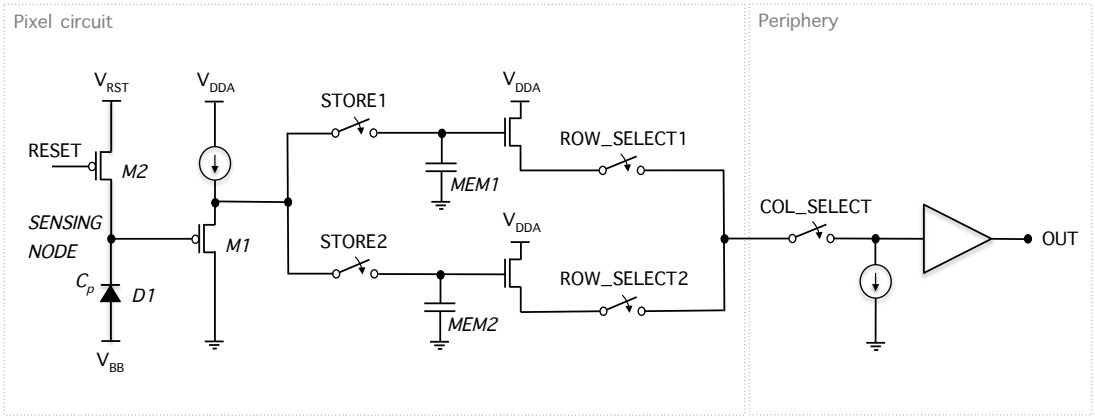


Figure 4.4.: Simplified schematic of the Explorer-1 front-end circuitry.

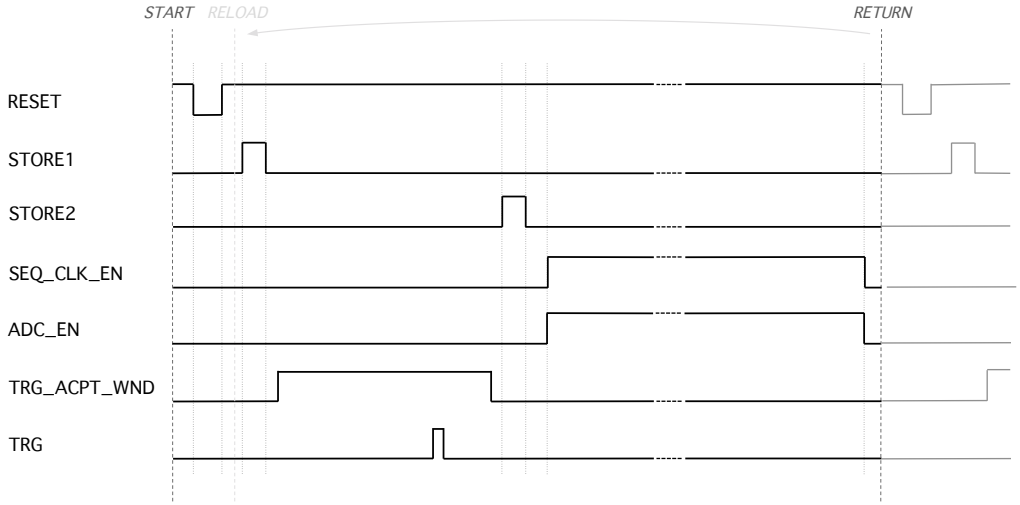


Figure 4.5.: Sequence of the steering signals for the Explorer-1 readout. The sequence is based on a single counter. For each of the signals, a counter value for activation and deactivation can be defined. Initially the sequence is started at the counter value zero (*START*) and runs until the counter reaches the *RETURN* value, whereafter the counter is reset to the *RELOAD* value. From this value, which can be set arbitrarily, but is by default set to zero, the sequence is repeated periodically. The default steering sequence is as follows: first the *RESET* signal (active low) is activated to reset the pixel. Shortly after the reset phase, the *STORE1* and *STORE2* signals are activated to store the potential at the sensing node into the analogue memory cells. The duration between the two *STORE* signals defines the integration time. After the *STORE2* is deactivated, the *SEQ_CLK_EN* signal is activated to enable the start of the sequencer that consecutively connects the pixel memories to the output pad of the chip. Simultaneously, also the ADC is enabled by the *ADC_EN* signal to sample the corresponding signals stored in the memories. In addition to the steering signals of the chip, an additional signal *TRG_ACPT_WND* is introduced that defines the period within which a trigger for the respective event is accepted.

4.2.1. Principle of operation

A simplified schematic of the Explorer-1 front-end circuitry is presented in Fig. 4.4. The input net is formed by the collection diode (D1), a PMOS source-follower (SF) transistor (M1) and a PMOS resetting transistor (M2). After the source follower, each pixel contains two independent analogue memory cells *MEM1* and *MEM2*, implemented to allow for correlated double sampling (CDS). Each of the two memory cells is followed by a second (NMOS) source-follower stage. At the periphery, a sequencing circuit is implemented to read out the memories pixel-by-pixel.
From the functional point of view, the pixel circuit operates as follows (cf. Fig.4.5): the potential at the sensing node, i.e. at the gate of the SF transistor, is first set to a well-defined value (V_{RST}) by activating the *RESET* signal, i.e. turning on the reset transistor (*reset operation*). Immediately after the reset, the potential at the sensing node is stored in the first memory cell *MEM1* by applying the switch *STORE1*. After the integration time Δt_{INT}, which is by default set to 28.8 µs[5], the potential at the sensing node is stored in the second memory cell *MEM2* by applying the switch *STORE2*. The assertion of the *RESET*, *STORE1* and *STORE2* is performed globally, i.e. simultaneously for all pixels. Subsequently to the assertion of *STORE2*, the analogue memory cells of all pixels are read out sequentially (by a combined switching of *ROW_SELECT1* or *ROW_SELECT2* and *COL_SELECT*). The digitization and CDS calculation take place off-chip.

4.2.2. Calculation pixel signal, pedestal and noise

The pixel signal for the Explorer-1 chip is calculated using the method of CDS, employing the signals stored in the two analogue memory cells *MEM1* and *MEM2*, where

$$\mathrm{CDS}_n = MEM1_n - MEM2_n \tag{4.4}$$

is the CDS value for pixel n.
Ideally, in the absence of hits, the CDS value for each pixel is zero. However, due to manufacturing tolerances in the chip production, the CDS value is non-zero even without impinging particles. Given a sample of N events, the mean value of the CDS distribution is called *pedestal*:

$$\mathrm{Pedestal}_n = \frac{1}{N}\sum_{i=1}^{N} \mathrm{CDS}_{n,i} \tag{4.5}$$

[5] This value was chosen close to the maximum tolerable integration time of 30 µs for the final pixel chip for the ALICE ITS upgrade (cf. Tab. 2.2).

The (temporal) noise is then defined as the RMS of the CDS distribution:

$$\text{Noise}_n = \sqrt{\frac{1}{N-1}\sum_{i=1}^{N}(\text{CDS}_{n,i} - \text{Pedestal}_n)^2} \tag{4.6}$$

In fact, the reset phase noise (kTC noise), which is introduced by the resetting transistor, is removed by this technique.
Once the pedestal and the noise values are estimated from a separate measurement, the pixel *signal* for an event i and pixel n is defined by:

$$\text{Signal}_{n,i} = \text{CDS}_{n,i} - \text{Pedestal}_n \tag{4.7}$$

The principle of operation of the Explorer-1 has, beside its advantage of being very versatile, also a downside: after the application of the reset and then *STORE1* and *STORE2* signals, the analogue memory cells are read out sequentially one after another. For the full pixel matrix this operation lasts more than 2 ms at the default sequencer clock frequency (10 MHz). At these time scales, the effects of leakage currents in the memory cells become significant, leading to experimentally observed lower signal and larger noise values for pixels connected later in the readout steering sequence.
To mitigate these effects, a correction procedure, the so-called *gain correction*, based on the measured transfer functions of the front-end circuits of each of the pixels has been developed. In addition, also a procedure to correct for common-mode noise has been implemented. The methods are presented in detail in Appendix D. For the Explorer-1 results presented in this chapter, both corrections have been applied.

4.2.3. SRS test system

The DAQ system for the Explorer chip family is based on the Scalable Readout System (SRS) of the CERN RD51 collaboration. It consists of the following components:

- **Hybrid board:** The Explorer-1 chip is wire-bonded on top of the hybrid board, that provides mechanical and electric interfacing to the proximity board.
- **Proximity board:** The proximity board is a custom design for the testing of the Explorer and other prototype chips for the pixel chip of the new ALICE ITS. It contains 16 analog channels with amplification as well as 64 digital channels with level shifters. Furthermore, it provides multiple supply voltages, bias DACs and a ADCs for chip monitoring purposes.

- **SRS system:** The SRS system itself consists of two so-called Front-End Concentrator (FEC) cards, which are paired with an ADC card and an LVDS-IO card, respectively. The FEC cards each contain an FPGA and communicate with the DAQ PC via Gigabit-Ethernet. The master FEC with the LVDS-IO card sends the steering signals to the Explorer-1 and controls its biasing via the proximity board. Furthermore, it controls the second FEC, which takes care of the digitisation of the analogue Explorer-1 output signal. This is performed with a 12 bit ADC at 10 MHz.
- **PC with DAQ software:** The SRS system is connected to DAQ PC. The DAQ software allows to configure the steering sequence for the chip and the bias DACs. Furthermore it handles the data processing, including an online zero-suppression, and allows for data monitoring. For test beam purposes also the EUDAQ framework[6] was used.

4.3. Investigator-0

The design of the Investigator-0 was motivated by the desire to obtain a more direct access to each pixel, avoiding the in-pixel memories of the Explorer chip family, and allowing for the study of the charge collection time within a cluster.
As listed in Tab. 4.3, the Investigator-0 chip consists of in total 134 pixel matrices with different pixel pitches ranging from 20 µm to 50 µm. The matrices are of 10×10 pixels in size, of which only the central 8×8 pixels are active. The outermost pixel rows and columns contain dummy-pixels, which are implemented to reduce edge effects in the pixel matrix. They are biased similarly to the central pixels, but have no connection to the chip periphery. Due to the small size of the pixel matrices they are also referred to as *mini-matrices* (MM).
Apart from different pixel pitches and collection-diode geometries, the various mini-matrices feature different implementations of the pixel reset (active or continuous), different deep p-well coverage under the matrix, different input-transistor locations (inside or outside the collection n-well) and different source follower configurations [47]. In this chapter, only results for pixels with active reset and a standard source follower are presented.

4.3.1. Principle of operation

A simplified schematic of the Investigator-0 chip, based on a sequence of PMOS and NMOS source followers, is presented in Fig. 4.6. The mini matrices - one at the time - can be

[6] `https://eudaq.github.io/`

Table 4.3.: Mini matrix identifier numbers and according pixel pitches in the Investigator-0.

MM identifier	**Pixel pitch** [µm]	**Number of MM** (per pitch)
0-35	20	36
36-57	22	22
58-67	25	10
68-103	28	36
104-111	30	8
112-123	40	12
123-134	50	10

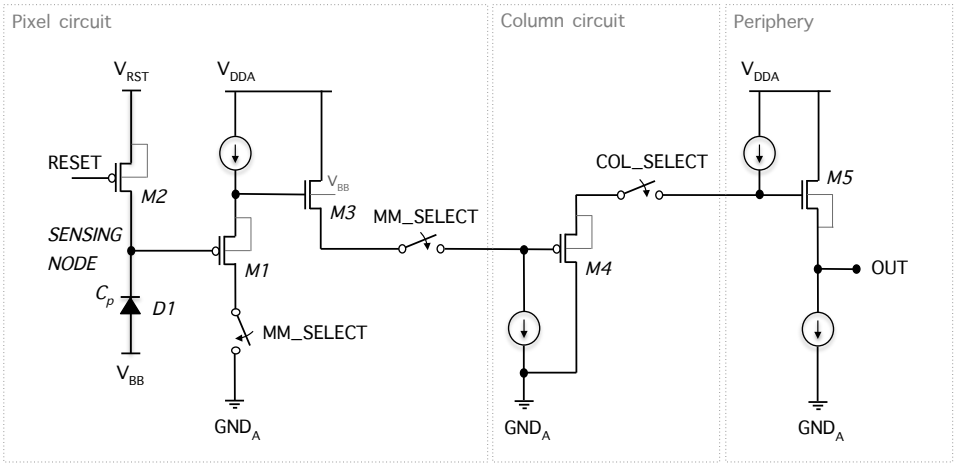


Figure 4.6.: Simplified schematic of the Investigator-0 chip.

selected by activating the according *MM_SELECT* switches. Indeed, the *MM_SELECT* switches directly connect each of the 64 pixels of the respective MM to the corresponding output pads of the chip, allowing for a continuous parallel sampling of the output signals of the pixels.

The steering sequence for the Investigator-0 is presented in Fig. 4.7. Similarly to the readout steering sequence for the Explorer-1 chip (cf. Fig. 4.5), it is based on a single counter, based on which for each of the steering signals a value for activation and deactivation can be defined. The default steering sequence is as follows: first the *RESET* signal (active low) is asserted to reset the pixel. Shortly after the reset phase, the *ACQ_WND* signal is asserted to enable the signal sampling[7]. In addition to the steering signals for the chip, an additional signal *TRG_ACPT_WND* is introduced that allows to define the period within which a trigger for the respective event is accepted.

[7]By default, the duration of the *ACQ_WND* is set to 1024 samples, which corresponds to a duration of 15.75 µs at the sampling frequency of 65 MHz.

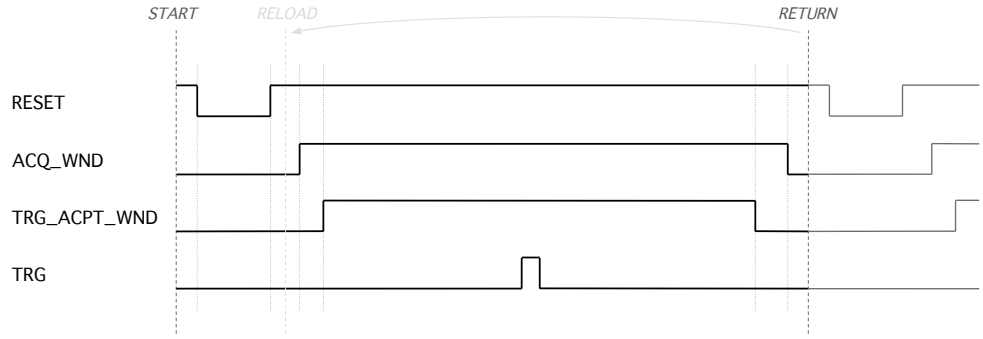


Figure 4.7.: Sequence of the steering signals in the Investigator-0 readout.

4.3.2. Calculation of pixel signal

Within the acquisition window, the output of each of the 64 pixels of a MM is sampled in parallel at a rate of 65 MHz. The sampled output waveforms for an array of 3×3 pixels out of the 8×8 pixels of a mini matrix is presented in Fig. 4.8. The arrangement of figures matches the pixel positions wihtin the pixel matrix. The presence of a hit and the associated generation and collection of signal charge is represented by a drop of the output signal of several pixels, clearly showing the charge sharing between the pixels. To determine the total amount of charge collected in each pixel in an event, the following approach has been followed:

- First, a search for the largest signal drop between two subsequent samples in the waveforms of any pixel of the MM is performed. The sample after which the largest signal drop occurs is referred to as *hit sample*. The pixel in which it was found is considered as seed-pixel candidate.

- After the hit sample is determined, the baseline signal $V_{\mathrm{OUT,b}}$ is estimated by calculating the mean value of N samples situated N_b samples before the hit sample. Correspondingly, the signal after the hit $V_{\mathrm{OUT,s}}$ is estimated by calculating the mean value of N samples situated N_s samples after the hit sample. The pixel signal ΔV_{OUT} consequently is the difference between the two mean values: $\Delta V_{\mathrm{OUT}} = V_{\mathrm{OUT,b}} - V_{\mathrm{OUT,s}}$.

- If the signal ΔV_{OUT} of the seed pixel candidate exceeds the threshold set for the seed pixel signal, it is considered to be the seed pixel of a cluster.

- After a seed pixel is found, the pixel signal of each pixel in an $n \times n$ pixel matrix around the seed pixel is calculated according to the procedure described above, using the same hit sample.

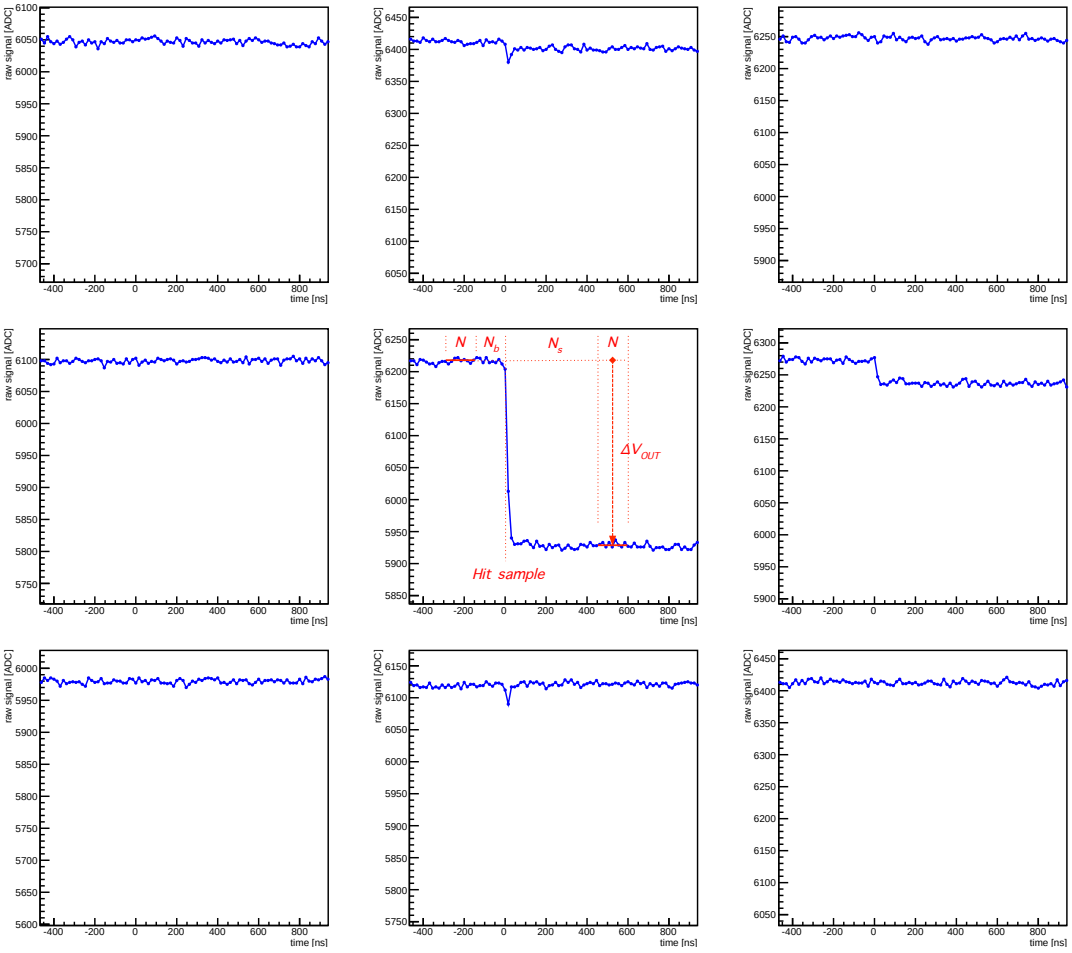


Figure 4.8.: Sampled output of nine of the 64 pixels of a mini matrix. The arrangement of figures matches the pixel positions in the array.

The signal of each of the pixels is moreover corrected for the differences of the gain of the respective channels of the readout system (INVROS), which are in the range of a few percent. A correction for the pixel-to-pixel variations of the on-chip circuitry gain is not possible for the Investigator-0 (cf. Appendix D.2)[8].

4.3.3. INVROS test system

The INVROS test system is a custom design for the Investigator chip family. It consists of the following components:

- **Chip carrier card:** The Investigator-0 chip is wire-bonded to the chip carrier card that provides both mechanical and electric interface to DAQ unit.

[8] However, compared to the Explorer-1 the variations are expected to be small as no on-chip analogue memory cells are employed.

- **Data acquisition (DAQ) unit:** The 64 analogue outputs from the Investigator chip are received by the DAQ unit. After conditioning in the analogue front-ends, each consisting of a voltage-follower and a differential driver, they are digitized by ADCs (14 bit at 65 MHz). The DAQ card is equipped with an FPGA, DACs providing the chip bias currents and voltages, and a unit for measuring the chip's power consumption. The sampled data is sent to a PC via a USB 3.0 interface.

- **PC with DAQ software:** The INVROS is connected to the PC running the DAQ software. The software allows to configure the readout system, including the steering sequence of the chip, the bias DACs and the mini matrix to be measured, request data and handle the data processing. Furthermore it contains a framework for the data analysis.

The data request is performed via a trigger signal. The following trigger modes are available:

- *Internal trigger:* this trigger is implemented in the FPGA on the DAQ unit. The trigger is issued when the signal of at least one pixel drops below a threshold to be defined with respect to the baseline signal of the pixel.

- *External trigger:* the trigger is issued upon the arrival of a signal from an external device to the DAQ unit.

- *Software trigger:* the trigger is issued by software, acquiring any data at the maximum achievable rate.

4.4. Sensor characterization

The characterization of the ALPIDE prototypes is mainly carried out using soft X-ray sources or minimum ionizing particles (MIPs) from test beam facilities as provided at CERN or DESY. X-rays and MIPs both lead to very characteristic signal and cluster shape distributions which can be deduced from the characteristics of the process of their energy loss and conversion: whereas X-rays are absorbed in a single point-like region by photoelectric conversion, MIPs in general cross the thin sensor, generating e-h pairs approximately uniformly along their track.
For the discussion of the measurements the following definition of terms is used:

- **Cluster:** The charge created by ionizing radiation in the sensor may be shared by several pixels. The group of pixel which shows a signal above a certain threshold is called a *cluster*.

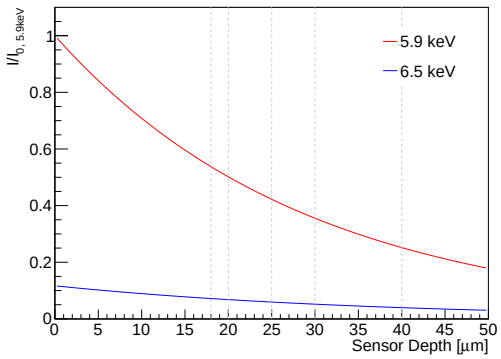
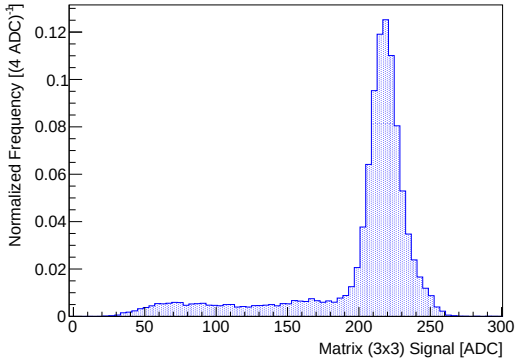


Figure 4.9.: Relative intensity as a function of sensor depth in silicon for both the 5.9 keV and 6.5 keV X-ray emission modes of ^{55}Fe. Both intensities are normalized to the intensity of the 5.9 keV line at the sensor surface. Nominal epitaxial layer thicknesses for chips discussed in this work are indicated.

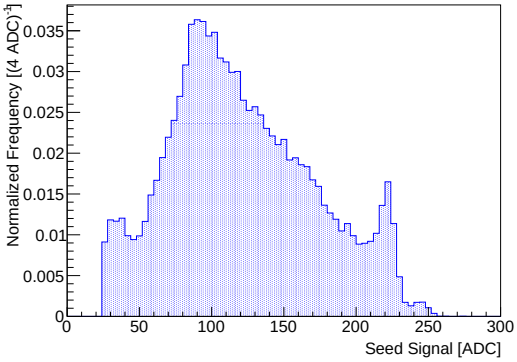
- **Seed pixel:** The pixel in the cluster with the largest signal is called the *seed pixel*.
- **Seed signal:** The signal obtained in the seed pixel is called the *seed signal*.
- **Cluster signal:** The sum of the signals of all pixels assigned to a cluster is called *cluster signal*. It is strongly dependent on the choice of the thresholds used for the assignment.
  Assuming that the noise of individual pixels is uncorrelated, the noise of the cluster signal depends on the number N of pixels involved. Further assuming identical RMS noise n_p on each pixel, the RMS cluster noise n_c is obtained by $n_c = \sqrt{N} n_p$.
- **Matrix signal:** The sum of the signals of an $n \times n$ pixel matrix, centered around the seed pixel is called *matrix signal*. The size of the matrix is to be chosen, but usually 3×3 pixels (*first crown*) or 5×5 pixels (*second crown*). With the same assumptions as for the cluster noise the RMS matrix noise n_m yields $n_m = 3n_p$ or $n_m = 5n_p$, respectively, depending on the crown.
- **Cluster multiplicity:** The number of pixels assigned to a cluster is called *cluster multiplicity*. As the cluster signal, it is strongly depending on the choice of thresholds.

4.4.1. X-ray source tests

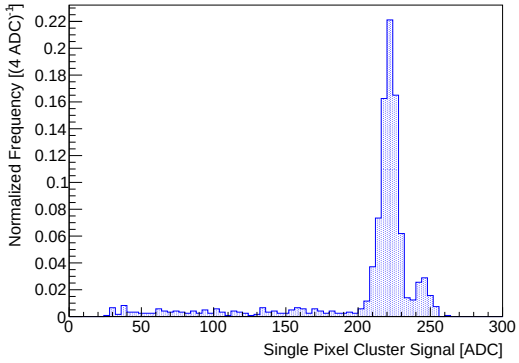
Soft X-rays ($E_{ph} < 10\,\text{keV}$) interact with silicon predominantly via the photoelectric effect, and generate $N_{\text{e-h}} = E_{ph}/w$ electron-hole pairs in a small point-like spatial region. For the characterization of the protoypes from the ALPIDE development, it is beneficial to exploit a source that offers a photon energy close to the most probable energy loss of a MIP, which is about $\Delta_p = 4.12\,\text{keV}$ in a sensor of 20 µm thickness. An isotope that



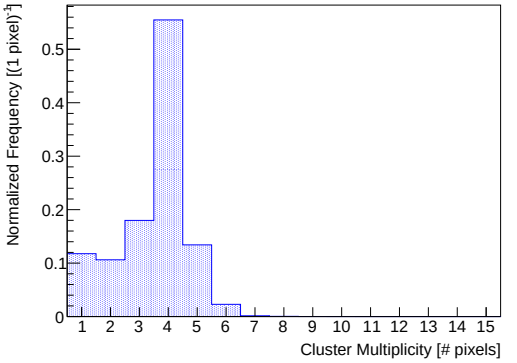
(a) Matrix signal distribution.



(b) Seed signal distribution.



(c) Single pixel cluster signal distribution.



(d) Cluster multiplicity distribution.

Figure 4.10.: Typical response of a prototype chip from the ALPIDE development to X-rays from an ^{55}Fe source.

offers this is ^{55}Fe, which emits photons in two emission modes with energies of 5.9 keV and 6.5 keV, with a probability of 24.40 % and 2.85 %, respectively [79][9]. The attenuation lengths of these photons in silicon are 29 µm and 37 µm [81], respectively, and therefore sufficient to allow a full penetration of the sensitive layer of the chips discussed in this work (cf. Fig. 4.9).

Typical signal and cluster-multiplicity spectra for X-rays originating from an ^{55}Fe source are shown in Fig. 4.10. The matrix signal distribution (cf. Fig. 4.10a) shows one significant peak. It can be related to events where the X-ray conversion occurred within the reflective boundaries of the epitaxial layer and almost all generated charge carriers are collected in the $n \times n$ pixel matrix. The tail to lower signal values can be attributed to events where the photon was absorbed in the substrate and thus not all generated charge is able to the reach the epitaxial layer.

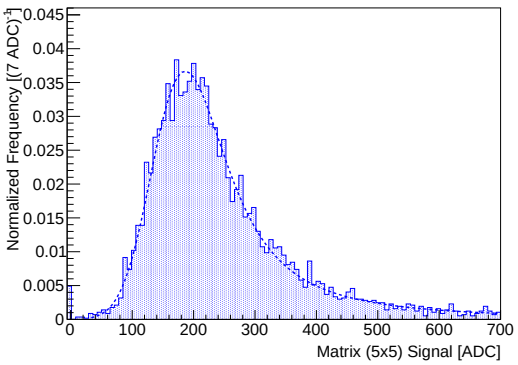
The seed signal distribution, shown in Fig. 4.10b, shows two significant peaks: The most prominent one, also called *collection peak*, represents the MPV of the charge collected by

[9] See also discussion in [80].

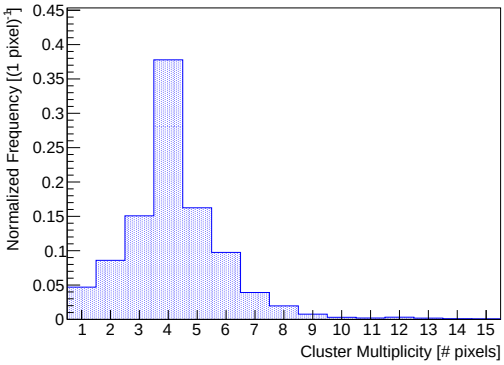
the seed pixel in case of charge sharing. For the sensors discussed in this thesis, this is typically in the range of 35 % to 50 % of the total deposited charge. The smaller peak to large signal values in the spectrum represents the cases in which the total charge deposited by the 5.9 keV photons is collected in the seed pixel. Since a 5.9 keV photon will in average generate approximately 1640 e-h pairs, this peak can be used for an absolute charge calibration. It is therefore often referred to as *calibration peak*. The additional small peak on the left of the spectrum follows from the events in which the photo conversion took place in the substrate. The relative distinctness of the collection peak and the calibration peak depends on the extension of the depletion regions around the collection diodes.
Selecting only such clusters with the total charge collected in a single pixel results in the *single-pixel cluster signal* distribution, as presented in Fig. 4.10c. Fig. 4.10d presents the cluster-multiplicity distribution, in this example obtaining an MPV of the cluster multiplicity of four.

4.4.2. High-energy charged particle test beams

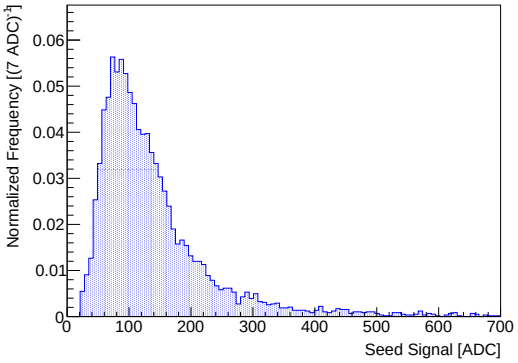
Sensor tests with high-energy charged particles (e.g. electrons or positrons, protons or pions) with a range of energies can be performed in test beam facilities, as existing at e.g. CERN or DESY.
Charged particles crossing the thin silicon layer of the sensor generate e-h pairs approximately uniformly along their track. The number of e-h pairs generated in a single event, $N_{\text{e-h}}$, is thereby a stochastic quantity, subject to large fluctuations, of which the probability density function is best characterized by its most probable value (MPV). The MPV is approximately proportional to the sensor thickness d (about 60 e-h pairs per µm, cf. Fig. 3.2a).
Typical signal and cluster-multiplicity distributions due to relativistic charged particles are shown in Fig. 4.11. The matrix signal distribution is presented in Fig. 4.11a. If full charge collection within the $n \times n$ matrix is provided, the matrix signal represents the deposited energy. Thus, it can be well fitted by a Landau distribution convoluted with a narrow normal distribution, modeling the broadening of the energy-loss distribution for very thin sensors and electronic noise. The seed signal distribution, shown in Fig. 4.11c, still resembles a Landau distribution. In fact, however, it is shaped by a convolution of the energy-loss distribution and a distribution representing the charge sharing effects. The relative amount of the total deposited charge collected in the seed pixel, i.e. the *relative seed signal*, averaged over all clusters, is presented in Fig. 4.11d. As can be observed for this example, the MPV is about 45 %, which also leads to an MPV of the seed signal that is about 45 % of the MPV of the matrix signal. Fig. 4.11b presents the cluster-multiplicity distribution, which compared to the distribution for ^{55}Fe X-rays, obtains a higher probab-



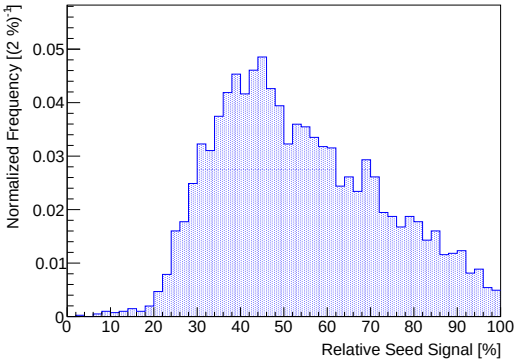
(a) Matrix signal distribution.



(b) Cluster multiplicity distribution.



(c) Seed signal distribution.



(d) Relative seed signal distribution.

Figure 4.11.: Typical response of a prototype chip from the ALPIDE development to MIPs.

ility for larger clusters. This effect can be attributed to the large-signal tail of the Landau distribution. As for X-rays, the shape of the seed signal and cluster-multiplicity distributions depends on the extension of the depletion regions around the collection diodes.
With high-energy charged particles also more elaborate setups can be applied, including so-called *beam telescopes*. Beam telescopes consist of several layers of position sensitive particle detectors and thus enable particle tracking, allowing for measurements of the detection efficiencies and position resolution of the sensor under test.

4.4.3. Observables and methods

The following observables have been used in order to assess the performance of prototypes from the ALPIDE development:

- **Equivalent noise charge (ENC):** In order to allow a convenient comparison with the signal charge, the noise is often expressed in units of electrons, also referred to as *equivalent noise charge* (ENC).

For the sensors with analogue readout discussed in this chapter, the ENC can be experimentally determined by using the calibration peak from the ^{55}Fe seed signal spectrum:

$$\text{ENC} = \frac{\text{Noise [V]} \times 1640e^-}{\text{Calibration Peak [V]}} \tag{4.8}$$

- **Signal to noise ratio (SNR):** The signal to noise ratio (SNR) is defined as the ratio of the MPV of the pixel signal and its noise value. An important value for the sensor charactization is also the SNR of the seed pixel, i.e. the Seed SNR.

- **Charge collection efficiency (CCE):** The CCE is defined as the ratio of the detected charge and the charge produced by an impinging particle and is an important measure to characterize the charge collection performance of the pixels.
  In practice, the CCE is measured using X-rays. Thereby it is assumed that in case the X-ray conversion occurs inside or near the depleted volume, most or all charge is collected by a single pixel. In other cases the photoelectric conversion occurs far from the depleted volume and the charge will be shared by several pixels. Some charge carriers may even get lost for detection, resulting in a CCE smaller than unity. Experimentally, the following estimates for the CCE can be defined:

  - **Cluster CCE:** The cluster CCE is defined as the ratio of the MPV of the cluster-signal distribution and the MPV of the single-pixel cluster signal distribution. As the cluster signal, the cluster CCE depends on the choice of thresholds for the assignment of the pixels to a cluster.

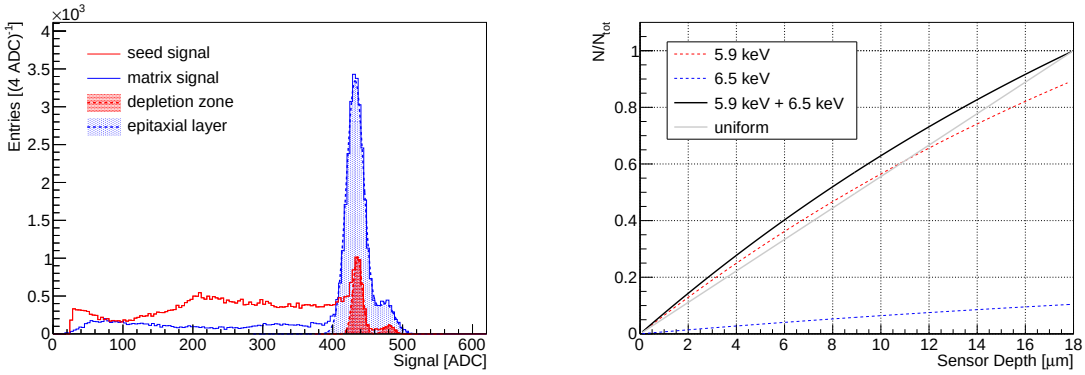
  - **Matrix CCE:** To obtain an observable that is independet of thresholds, the matrix CCE was introduced. It is defined as the ratio of the MPV of the matrix signal distribution and the MPV of the single-pixel cluster signal distribution.

- **Pixel input capacitance:** The pixel input capacitance C_p can be estimated from the pixel response to the 5.9 keV X-rays from an ^{55}Fe source. The calculation is performed using the signal value obtained for the calibration peak $V^{\text{gc}}_{\text{calib}}$, corrected for the gain of the on-chip circuitry and the readout system[10]:

$$C_p = \frac{1640\, e^-}{V^{\text{gc}}_{\text{calib}}} \tag{4.9}$$

- **Relative depletion volume:** The characteristics of the X-ray interaction also allow for a study of the depletion volume, however, only for the *relative depletion volume*, not for its precise shape. The depleted fraction of the sensor volume is of interest regarding the charge collection times and consequently the radiation

[10] See Appendix D.1.1 for details.



(a) **(b)**

Figure 4.12.: Estimation of the relative depletion volume and systematic error estimation: (a) fits to seed and matrix signal distribution and (b) cumulative distribution of the X-ray absorption over the sensor depth, for the example of an 18 µm thick epitaxial layer.

hardness of the sensor.

The calibration peak is assumed to be formed by N_{depl} events in which the X-ray conversion took place within the depletion volume and therefore all deposited charge is collected by a single pixel. By contrast, the matrix signal peak is formed by N_{tot} events in which the photo conversion occurs within the epitaxial layer. Consequently, the ratio $r_{\text{depl}} = N_{\text{depl}}/N_{\text{tot}}$ of the integrals below each of the peaks represents an estimate for the relative depletion volume. In practice, the values for N_{depl} and N_{tot} are estimated by fitting the peaks in the corresponding distributions by a function constructed of two overlapping Gaussian distributions, accounting for both of the ^{55}Fe emission lines. Fig. 4.12a shows example matrix and seed signal distributions, in which the peak fits are highlighted.

Taking just the ratio $N_{\text{depl}}/N_{\text{tot}}$, however, holds the implicit assumption that the X-rays are uniformly converted along the sensor depth. In fact, however, the intensity profiles of the X-rays according to the attenuation lengths λ_i have to be taken into account (cf. Fig. 4.9). To obtain an estimate for the systematic error made due to the assumption, the two extreme (unrealistic) cases that the depletion volume is either fully situated in a layer at the top, or at the bottom of the epitaxial layer, are considered in the following.

Correctly normalized, the intensity profiles represent the probability density function (PDF) for an X-ray conversion at a given sensor depth z for each of the emission modes of 5.9 keV and 6.5 keV, respectively[11]. Reconsidering Eq. (3.3), the PDF

[11] This is actually only valid when the conversion probability is uniform over the sensor depth. Then the PDF for a photo conversion in a given sensor depth is determined by the intensity profile of the X-ray beam.

$f_{X,i}(z)$, $0 < z < d$, d being the sensor depth, of emission mode i can be written as

$$f_{X,i}(z) = c_i e^{-z/\lambda_i}, \tag{4.10}$$

where c_i is a normalization constant so that

$$\int_0^d f_{X,i}(z)\,\mathrm{d}z = 1, \tag{4.11}$$

The corresponding cumulative distribution function (CDF) consequently is

$$F_{X,i}(z) = \int f_{X,i}(z)\,\mathrm{d}z = c_i d\left(1 - e^{-z/\mu_i}\right), \tag{4.12}$$

where the factor d follows from the condition $F_{X,i}(z = 0) = 0$. The summed CDF for both emission modes for a sensor with a nominal thickness of $d = 18\,\mu\mathrm{m}$ is shown in Fig. 4.12b. For comparison also the CDF $F_X(z) = z/d$ of a uniform PDF is plotted. Using the inverse function F_X^{-1} of the summed CDF, the depleted volume related to the observable $N_{\mathrm{depl}}/N_{\mathrm{tot}}$ is

$$r_{\mathrm{depl,top}} = \frac{F_X^{-1}\left(N_{\mathrm{depl}}/N_{\mathrm{tot}}\right)}{d} \tag{4.13}$$

for the extreme case in which the depletion volume is assumed to be situated in a layer at the top of the epitaxial layer.
Resulting from Eq. (4.12), the $r_{\mathrm{depl,top}}$ expressed in Eq. 4.13 is smaller than in the case of a uniform PDF. Accordingly, assuming the extreme case in which the depletion volume is fully situated in a uniform layer at the bottom of the epitaxial layer, the relative depletion volume is estimated as

$$r_{\mathrm{depl,bottom}} = \frac{F_X^{-1}\left(1 - N_{\mathrm{depl}}/N_{\mathrm{tot}}\right)}{d}, \tag{4.14}$$

which results in larger than value in the case of a uniform PDF.
The systematic error estimate obtained in this way depends on the thickness of the epitaxial layer. For an epitaxial layer of 18 µm thickness, the relative error amounts to about 20 %.

4.5. Charge collection efficiency and pixel input capacitance as function of sensor parameters

In this section, experimental results on the performance of the sensor are discussed depending on the sensor parameters, i.e. the pixel pitch, collection electrode geometry and the properties of the epitaxial layer (thickness and resistivity). Furthermore, the influence of the reverse-substrate bias voltage is discussed.

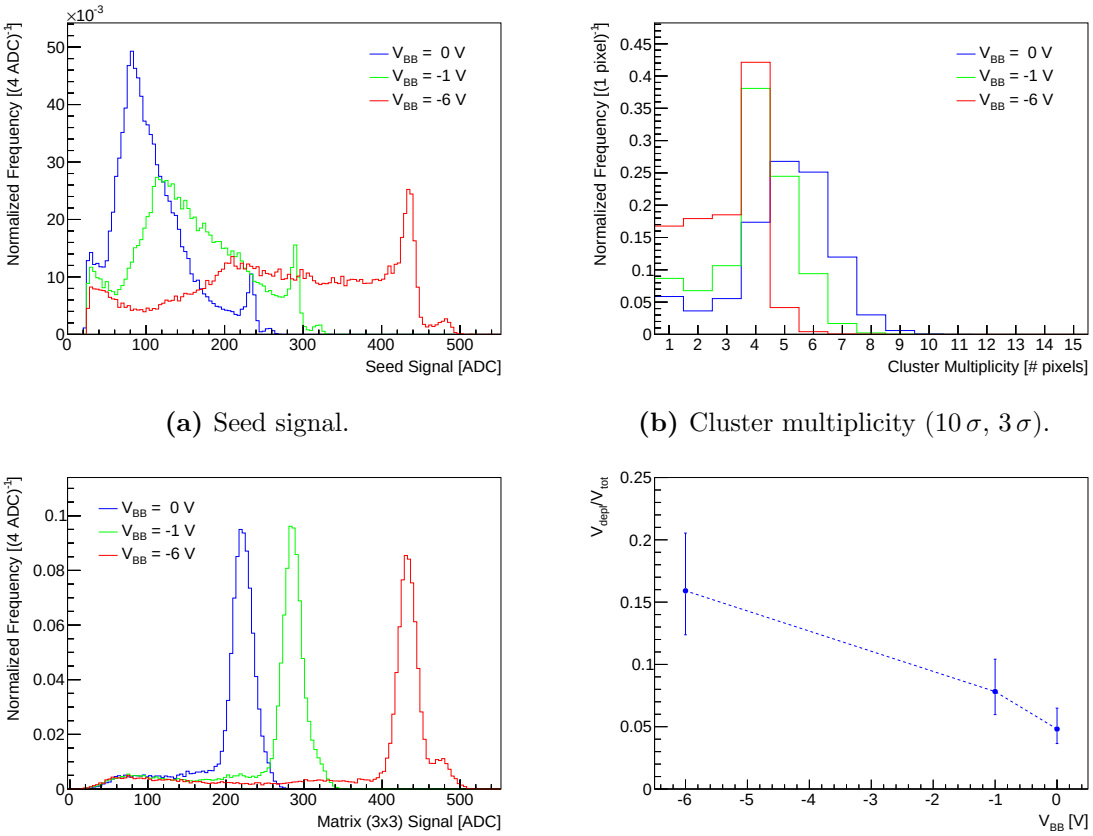
4.5.1. Reverse substrate bias of the collection diode

The reverse-substrate bias voltage V_{BB} has an influence on the extension of the depletion region, with a direct effect on the pixel input capacitance and the efficiency of the charge collection process and hence the Q/C ratio of the sensor.

^{55}Fe distributions A way to characterize the influence of an increased reversed bias voltage on the collection diode is to study the signal- and cluster-multiplicity distributions for X-rays originating from an ^{55}Fe source, as introduced in Sec. 4.4.1.
Fig. 4.13a presents the seed signal distribution for sector 5 of the Explorer-1 for the three reverse substrate bias values of 0 V, −1 V and −6 V, respectively. Two main changes can be noted as V_{BB} is increased: first, the collection peak is shifted to higher signal values, and second the distinctness of the calibration peak is enhanced with respect to the collection peak. Both changes can be understood by an enlargement of the depletion volume, which leads to a reduction of the pixel input capacitance and a more efficient charge collection process:

- The calibration peak is assumed to be formed by events in which the total charge generated by an X-ray conversion is collected by a single pixel. The signal shift must therefore originate from a reduction of the pixel input capacitance. This interpretation is supported by the fact that also the matrix signal peak is shifted similarly to the calibration peak. The observation that the matrix signal peaks (cf. Fig. 4.13c) and the corresponding calibration peaks are found at approximately the same signal values moreover indicates that the charge collection efficiency (CCE) is close to 100 %. The CCE is discussed in more detail in view of bulk damage effects in Sec. 4.7.

- An enlargement of the depletion volume leads to a larger relative number of events in which the X-ray conversion takes place within the depletion region. As a consequence, for enlarged depletion volumes the calibration peak becomes more prominent. Moreover, as the depletion regions are enlarged, the generated charge is in



(a) Seed signal.

(b) Cluster multiplicity ($10\,\sigma$, $3\,\sigma$).

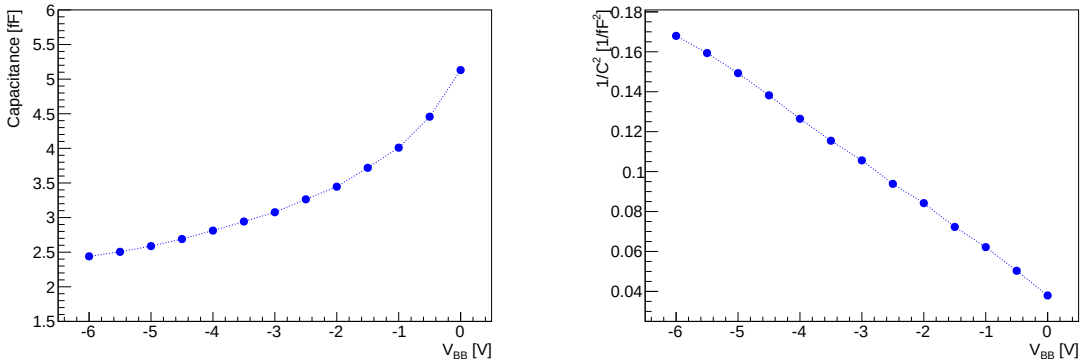
(c) Matrix signal.

(d) Relative depletion volume.

Figure 4.13.: Comparison of the Explorer-1 response for V_{BB} values of 0 V, −1 V and −6 V to X-rays from an ^{55}Fe source for a $20\,\mu m \times 20\,\mu m$ pixel with a $3.31\,\mu m^2$ octagonal n-well electrode and 2.6 µm spacing between the n-well and the surrounding p-well (sector 5) on an HR18 wafer. The seed signal (a), cluster multiplicity (b), matrix signal (c) distributions, and furthermore the relative depletion volume as function of V_{BB} (d) are shown. The error bars in (d) represent systematic uncertainties estimated using Eq. (4.13) and Eq. (4.14). Statistical errors are not included, but have been found to be in the order of 10 %.

average shared by less pixels. The effect is directly visible in Fig. 4.13a, where the probability for clusters with smaller multiplicity is shown to be strongly increased at higher reverse bias. The resulting effect on the collection peak, which in fact represents the most probable seed signal in case of charge sharing, is that it becomes less prominent and gets shifted to larger signal values with respect to the calibration peak. E.g. for $V_{BB} = 0\,V$ the collection peak is very dominant and situated at approximately 30 % of the calibration peak. In contrast, at $V_{BB} = -6\,V$ it no longer dominates and situated at approximately 50 % of the calibration peak.

Fig. 4.13d presents quantitative estimates of the relative depletion volume as a function of the reverse substrate bias. For the pixel under study, at $V_{BB} = 0\,V$ a relative depletion volume of the order of 5 % is obtained, which is more than tripled when increasing V_{BB}



(a) Pixel input capacitance. **(b)** $1/C^2$.

Figure 4.14.: C/V-characteristics of a 20 µm × 20 µm Explorer-1 pixel with a 3.31 µm^2 octagonal n-well electrode and a 2.6 µm spacing between the n-well and the surrounding p-well (sector 5) on an HR18 wafer.

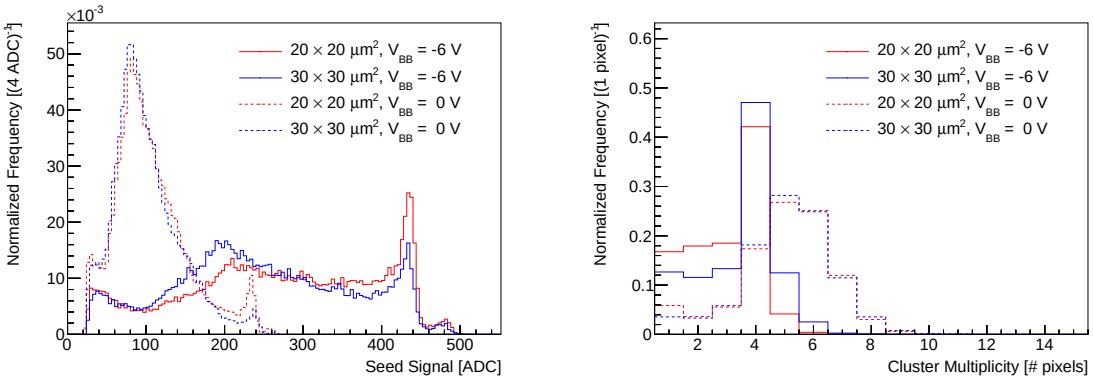
to −6 V. It should be noted, however, that the size of the depletion region is not only depending on the reverse bias, but also on geometrical parameters such as collection n-well size and spacing between the n-well and the surrounding p-well, and consequently the collection-diode footprint. The related effects will be discussed in Sec. 4.5.3.

Pixel input capacitance Fig. 4.14a shows the pixel input capacitance C_p as a function of V_{BB}, estimated using Eq. (4.9). As expected, it can be observed that increasing the reverse bias leads to a reduction of the pixel input capacitance. As introduced in Sec. 3.3.2, the capacitance of the sensing node can be subdivided into the contributions of the input routing lines and transistor, C_{rt}, and the collection-diode junction, C_d. Indeed, increasing the reverse bias voltage reduces the junction capacitance. For the pixel under study, a cumulative value of approximately 5 fF is reached for $V_{BB} = 0$ V which is reduced by 50 % to about 2.5 fF for $V_{BB} = -6$ V. Moreover, Fig. 4.14b reveals that the pixel input capacitance is approximately an inverse quadratic function of V_{BB}.

4.5.2. Pixel pitch

When maintaining the collection electrode geometry and epitaxial layer properties, the relative depletion volume can be expected to decrease with increasing pixel pitch[12]. At the same time, the mean diffusion path length will be increased.
Fig. 4.15 presents the seed signal and cluster multiplicity distributions for pixels with the same collection electrode but two different pixel pitches (20 µm and 30 µm). It can be clearly seen that the calibration peak position remains identical for the different pixel

[12] Cases in which the depletion region reaches the lateral limits of the pixel volume are negelegted here.



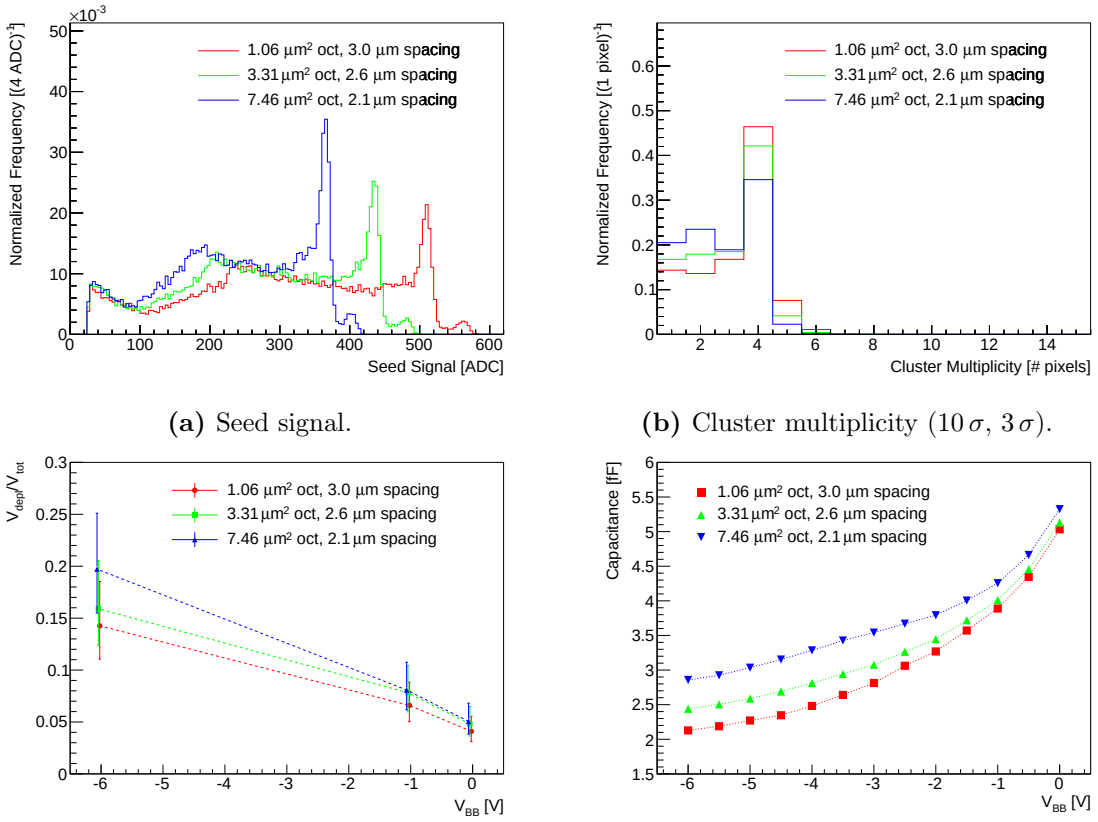
(a) Seed signal. **(b)** Cluster multiplicity.

Figure 4.15.: Investigator-0 response to X-rays from an ^{55}Fe source for two different pixel pitches: seed signal distribution (a) cluster multiplicity distribution (b) (cuts 10σ, 3σ) . The results are shown for a pixel with a $3.31\,\mu m^2$ octagonal n-well electrode and $3\,\mu m$ spacing between the n-well and the surrounding p-well at $V_{BB} = 0\,V$ and $V_{BB} = -6\,V$ on an HR18 wafer.

pitches. This indicates that the pixel pitch has no effect on the pixel input capacitance. However, the relative distinctness of the collection peak with respect to calibration peak is reduced when increasing the pixel pitch. The effect is accompanied with a shift of the collection peak to smaller signal values, indicating more pronounced charge sharing effects. This is also represented in the cluster multiplicity distributions, where the probability for clusters with larger multiplicity is shown to be increased for larger pixels.
The observed trends with increasing pixel pitch resemble the effects of a reduction of the reverse bias as discussed in the previous section, which could be explained by the size of the depletion region. However, it should be noted, that even in case of equal relative depletion volumes for two different pixel pitches, the mean diffusion path is longer for larger pixels. This has a direct effect on the charge collection time and consequently the CCE, in particular after irradiation when the charge carrier lifetime is reduced. Thus, when maintaining the collection electrode geometry, smaller pixels can be expected to be less sensitive to bulk damage. The related results are discussed in Sec. 4.7.

4.5.3. Collection electrode geometry

The collection diode geometry is determined by the *collection n-well size* and the *spacing* to the surrounding p-well. The total area within the p-well opening is also referred to as *footprint* (cf. Fig. 4.3).
As shown Fig. 4.1, for the study of the influence of the collection n-well geometry, the Explorer-1 chip provides pixels with equal footprint, but different n-well sizes, and consequently different spacings. In particular, sectors four, five and six, offer pixels with an



(a) Seed signal.

(b) Cluster multiplicity ($10\,\sigma$, $3\,\sigma$).

(c) Relative depletion volume.

(d) Pixel input capacitance.

Figure 4.16.: Explorer-1 response to X-rays from an ^{55}Fe source for pixels with 20 µm pitch and three different octagonal n-well electrodes (sector 4, 5 and 6), at a $V_{BB} = -6\,\mathrm{V}$ on and HR18 wafer. The seed signal(a) and cluster multiplicity (b) distributions are shown. Furthermore the relative depletion volume (c) and the pixel input capacitance (d) as function of V_{BB} for the same pixels are presented.

octagonal n-well with a diameter of 1.1 µm, 2.0 µm and 2.6 µm, and a spacing of 3.0 µm, 2.6 µm and 2.1 µm, respectively.

Fig. 4.16a presents the seed signal distributions from ^{55}Fe X-rays for the three different pixel types at $V_{BB} = -6\,\mathrm{V}$. Two main trends can be noted:

- The calibration peak is more prominent for pixels equipped with a larger collection n-well. This effect is compatible with the idea that a larger collection n-well results in a larger depletion volume, despite equal footprints and the expectation that at $V_{BB} = -6\,\mathrm{V}$ the lateral expansion of the depletion region is sufficiently large to fully fill the footprint area at the top of the sensor. Fig. 4.16c shows the estimated relative depletion volume for the three different pixels as a function of the reverse substrate bias. It can be clearly recognized that increasing the n-well size leads to an enlargement of the depletion volume for all studied V_{BB} values. The observations are further substantiated by the cluster multiplicity distributions presented in

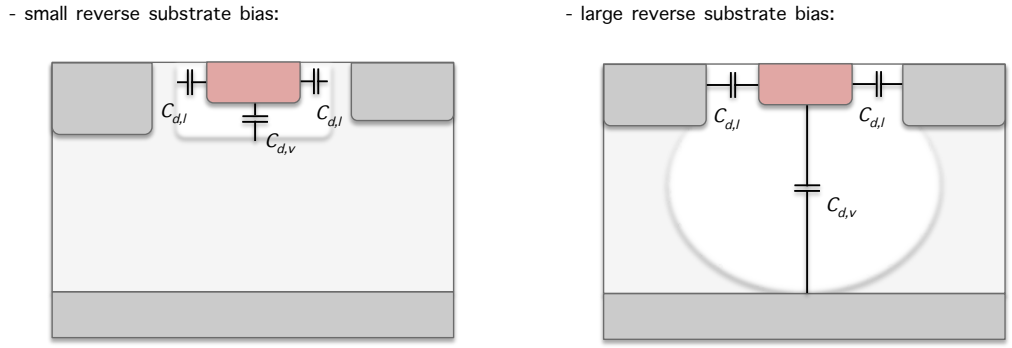


Figure 4.17.: Simplified model for subdivision of the junction capacitance C_d. Qualitative effects of increasing V_{BB} are indicated.

Fig. 4.16b, where the probability for clusters with smaller multiplicity is shown to be enhanced for larger collection n-wells.

- The calibration peak is obtained at higher signal values for pixels featuring a smaller n-well size and larger spacing. This indicates a change of the pixel input capacitance C_p.

Fig. 4.16d shows the estimated pixel input capacitances as a function of V_{BB} for the three different pixel types. As to be expected from the observations on the calibration peak positions in Fig. 4.16a, one can observe a clear trend, that is, the capacitance is lower for pixels with smaller collection n-well and larger spacing.
As previously discussed, the capacitance of the sensing node can be separated into the contributions of the input routing lines and transistor, C_{rt}, and the collection diode, C_d. As the input transistors and routing line lengths are equal for the three studied pixel types, the contribution C_{rt} cannot explain the behaviour of the total pixel input capacitance C_p. Therefore, the characteristics of the contribution collection diode, C_d, are further reviewed. Following the simplified model presented in Fig. 4.17, it can be subdivided into two contributions:

- The first is formed by the lateral contribution between the collection n-well and the surrounding p-well $C_{d,l}$,
- The second is formed by the vertical contribution between the n-well and the epitaxial layer $C_{d,v}$.

Both contributions are expected to be a monotonically decreasing function of the depletion layer extension in the respective directions. At low reverse bias, the extension can be expected to be equal at in all directions. However, at large reverse bias the situation changes. Due to the fact that the doping concentration in the p-well is orders of magnitude larger than in the epitaxial layer, the lateral extension of the depletion region at the top

of the sensor is essentially limited by the p-well. Consequently, for V_{BB} values sufficiently large to fully deplete the footprint area, the lateral contribution $C_{d,l}$ is saturated. On the contrary, in the vertical direction, the depletion region can further extend to the bottom of the epitaxial layer. Thus, considering that the spacing is typically significantly smaller than the epitaxial layer thickness, it can be expected that at large reverse bias the diode capacitance C_d is dominated by the lateral contribution $C_{d,l}$. The observation from Fig. 4.16d that the input capacitance of pixels with a larger n-well and smaller spacing saturates at larger values can hence most probably be attributed to the smaller spacing[13].

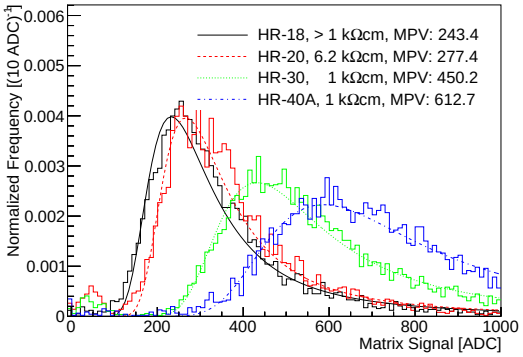
4.5.4. Epitaxial layer properties

The Explorer-1 chip was produced on five different wafer types with different epitaxial layer thicknesses and resistivities (cf. Tab. 4.2). The corresponding characterization of the pixel performance depending on the epitaxial layer properties is discussed in the following.

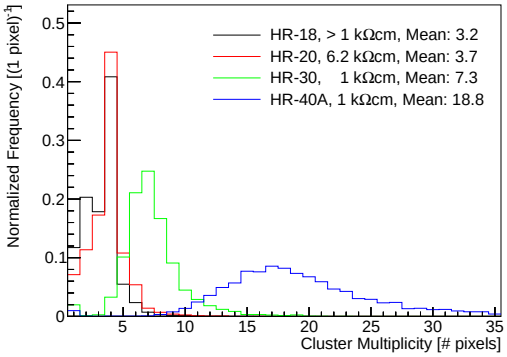
Epitaxial layer thickness

The motivation to study additional wafers featuring different epitaxial layer thicknesses results from the fact that the amount of e-h pairs created by traversing charged particles is expected to be approximately proportional to the thickness of the sensitive layer. However, when increasing the epitaxial layer thickness, at the same time also the diffusion volume is enlarged. The achieved benefit will therefore depend on the magnitude of the charge sharing effects.
The influence of the epitaxial layer properties was studied in a test beam at DESY with a 3.2 GeV positron beam, comparing the wafer types HR-18, HR-20, HR-30 and HR-40A. The summary for the 20 µm × 20 µm pixels of sector 5 of the Explorer-1 is shown in Fig. 4.18c. As expected, it is observed that the MPV of the matrix signal, representing the total deposited charge in the sensor, is approximately proportional to the epitaxial layer thickness (also see Fig. 4.18a), exhibiting an average charge generation between 70 e^-/µm and 75 e^-/µm[15].

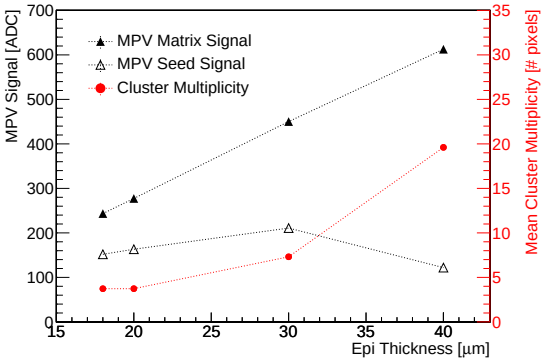
[13] Contributions from the larger n-well size can however not be fully excluded with the data available from the Explorer-1 chip. The Investigator-0 chip with its 134 pixel matrices may offer the possibility to disentangle the effects of varying collection n-well size, spacing and footprint.
[14] Due to the different cluster sizes for the different epitaxial layer thicknesses different sizes of the $n \times n$ pixel matrix were applied: n = 5 for HR-18 and HR-20, n = 7 for HR-30, n = 9 for HR-40A and HR-40B.
[15] These values have been estimated using the nominal thickness of the epitaxial layer. The difference between these values and the value expected from theory, i.e. about 60 e^-/µm (cf. Sec. 3.1.1) may be explained by the contribution from the substrate.



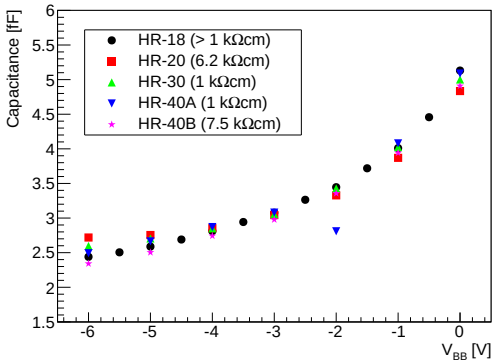
(a) Matrix signal[14] for $V_{BB} = -6\,\mathrm{V}$.



(b) Cluster multiplicity for $V_{BB} = -6\,\mathrm{V}$.



(c) The MPV of the matrix signal and seed signal distributions, and the mean cluster multiplicity (red) for $V_{BB} = -6\,\mathrm{V}$ as a function of the epitaxial layer thickness.



(d) Pixel input capacitance for the different epitaxial layer types evaluated from the pixel response to 5.9 keV X-rays from an ^{55}Fe source as a function of the reverse bias.

Figure 4.18.: Comparison of measurement results for different wafer types. The data shown are taken with an Explorer-1 pixel with a 3.31 µm^2 octagonal n-well electrode and a 2.6 µm spacing between the n-well and the surrounding p-well.

However, at the same time the mean cluster multiplicity shows a strong non-linear increase as a function of the epitaxial layer thickness. These two effects have a competing influence on the process that determines the amount of charge that is collected in each pixel, i.e. also the seed pixel. Since measurements confirmed no significant difference in noise for the studied wafer types, for V_{BB}= −6 V this results in the fact that while the seed signal-to-noise ratio (SNR) increases for epitaxial layer thicknesses up to 30 µm, it is again reduced at a thickness of 40 µm.

Epitaxial layer resistivity

An increased epitaxial layer resistivity is, similarly to the biasing of the collection diode, expected to cause an increase of the depletion volume and therefore a reduction of the

pixel capacitance.
The effect of the epitaxial layer resistivity on the pixel performance was studied measuring the input capacitance of the Explorer-1 pixels on different epitaxial layers. Fig. 4.18d shows the results for the pixel capacitance for $20\,\mu m \times 20\,\mu m$ pixels of sector 5 of the Explorer-1 as a function of reverse bias for five different epitaxial layers. The effects are very similar for all wafer types, indicating only a very weak influence of the epitaxial layer resistivity. This compatible with the previously discussed idea that the junction capacitance C_d is dominated by the lateral contribution between the collection n-well and the surrounding p-well with respect to the vertical contribution between the n-well and the epitaxial layer (cf. Fig. 4.17). Since doping concentrations of both n-well and p-well are not modified for the various wafer types, it can be assumed that also the lateral contribution to C_d and consequently the overall junction capacitance do not vary significantly depending on the epitaxial layer resistivity.
It should be noted, however, that the results obtained with the available pixels do not exclude benefits of an increased epitaxial layer resistivity for other pixel designs, in particular for designs including larger spacings.

4.5.5. Combined effects

In some cases, variations of the parameters discussed in the previous sections have shown a competing influence on the Q/C ratio, i.e. the ratio of the collected signal charge in a pixel and the pixel input capacitance. For instance, increasing the n-well size increases the efficiency of the charge collection process a single pixel, but reduces the pixel input capacitance. In order to allow for a more complete picture of the effects, example parameter combinations will be discussed in the following.

In Fig. 4.19 the effect of an increasing epitaxial layer thickness in combination with different values of V_{BB} can be observed. The data for $V_{BB} = -6\,V$ has already been presented separately in Fig. 4.18c, for which the largest seed signal and hence the optimum epitaxial layer thickness (for the pixel under study) was obtained at $30\,\mu m$.
In addition to this, Fig. 4.19 also shows the results for $V_{BB} = -1\,V$ (dashed lines). As for the reverse substrate bias of $-6\,V$, the MPV of the matrix signal is observed to increase proportionally to the epitaxial layer thickness. However, the obtained values for $V_{BB} = -1\,V$ are significantly lower than for $V_{BB} = -6\,V$. Indeed, this difference can be attributed to the increased pixel input capacitance for lower reverse bias.
Moreover, at $V_{BB} = -1\,V$ the cluster multiplicity shows a much stronger increase as function of the epitaxial layer thickness. This results in the fact that for $V_{BB} = -1\,V$ the largest seed signal is obtained with an epitaxial layer thickness of $20\,\mu m$. For pixels with

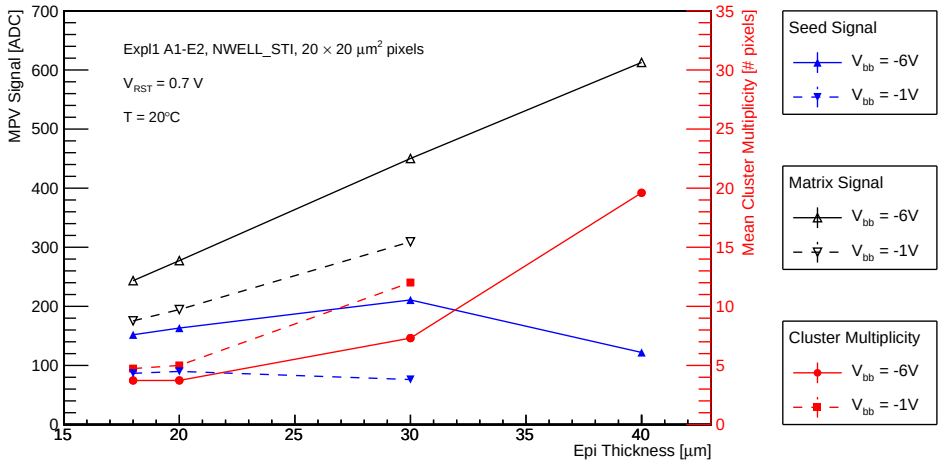


Figure 4.19.: Combined effect of the reverse substrate bias and the epitaxial layer thickness on the signal studied with a 3.2 GeV e^+ beam. The MPV of the matrix signal (black) and seed signal (blue), and the mean cluster multiplicity (red) are presented as function of the epitaxial layer thickness. The data are measured with an Explorer-1 pixel with a 3.31 µm^2 octagonal n-well electrode and 2.6 µm spacing between the n-well and the surrounding p-well (sector 5) and at two V_{BB} values of −1 V (dashed lines) and −6 V (solid lines).

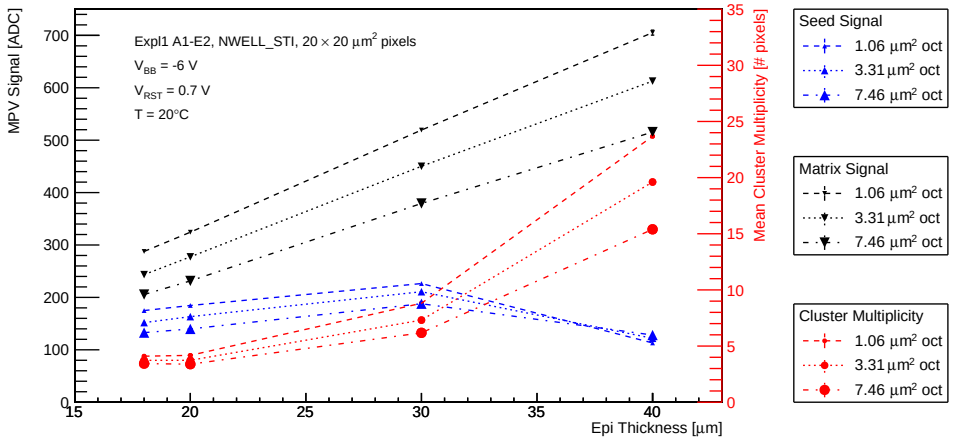


Figure 4.20.: Combined effect of the collection diode geometry and the epitaxial layer thickness on the signal studied with a 3.2 GeV e^+ beam. The MPV of the matrix signal (black) and seed signal (blue), and the mean cluster multiplicity (red) are presented as function of the epitaxial layer thickness. The data are measured with three Explorer-1 pixels featuring different collection diode geometries (sectors 4, 5 and 6) at $V_{BB} = -6$ V.

a pitch of 30 µm very similar results were observed for the same sector of the Explorer-1 and the studied reverse subsrate bias voltages.

Fig. 4.20 illustrates the effect of an increasing epitaxial layer thickness in combination with different collection diode geometries. The results for the same pixels as discussed in Sec. 4.5.3, featuring different n-well sizes and spacing but equal footprint, are presented for $V_{BB} = -6\,\mathrm{V}$.
The offset and different slopes of the curves for the MPV of the matrix signal of the different pixels can be attributed to different pixel input capacitances. Furthermore, it can be clearly recognized that the increase of the cluster multiplicity for thicker epitaxial layers is mitigated for the pixels with larger n-well size. This leads to the fact that for an epitaxial layer thickness of 40 µm the largest seed signal is obtained for the pixel type with the largest collection n-well and smallest spacing, despite its larger capacitance. The larger capacitance must thus be overcompensated by the collection of more charge, i.e. by a larger depletion volume. These observations show that epitaxial layers thicker than 30 µm may be beneficial for pixels with large collection n-well sizes and possibly larger spacing.

4.5.6. Summary of the influence of the sensor parameters

Summarizing the presented measurements, the following trends have been observed:

- All studied Explorer-1 pixel designs provide the required charge collection efficiency.
- A large reverse bias on the collection diode yields a better Q/C ratio due to both a decreased pixel input capacitance and less charge sharing as a result of an enlarged depletion volume.
- With increasing pixel pitch the charge is shared over more pixels due to the involved increase of the non-depleted volume in the epitaxial layer.
- Pixels with a small collection n-well and large spacing between the collection n-well and the surrounding p-well gain more from an increase of the reverse substrate bias in terms of pixel input capacitance.
- A smaller collection n-well yields a smaller pixel input capacitance. However, as a competing effect the depletion volume and thus the charge collection efficiency is reduced. This effect becomes particularly visible for very thick epitaxial layers.
- For pixel layouts available in the Explorer-1 and the considered epitaxial layer resistivities (between 1 kΩ cm to 7.5 kΩ cm), the epitaxial layer resistivity only shows a minor influence.

5	4	3	4	5
4	2	1	2	4
3	1	0	1	3
4	2	1	2	4
5	4	3	4	5

Figure 4.21.: Definition of the pixel and signal groups for the analysis of the charge collection time. Pixel group 0 corresponds to the seed pixel.

The benefit of an increased epitaxial layer thickness depends on the charge collection efficiency in a single pixel. Only at larger reverse bias voltages, i.e. large depletion regions, an advantage from the larger amount of signal charge generated in a thicker epitaxial layer is observed. Then, however, the increase of the seed SNR is substantial.
The study of the effects of the different collection diode geometries provided by the Explorer-1, however, also indicates that the depletion volumes may be enlarged by enlarging the collection n-well and/or the footprint[16].

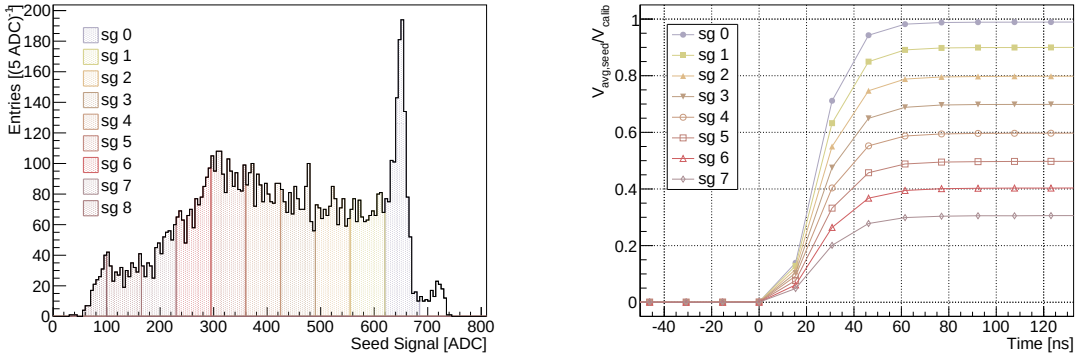
4.6. Charge collection time as function of sensor parameters

The continuous parallel sampling of the output signal of each pixel in case of the Investigator-0 chip allows the characterization of the duration of the charge collection process, i.e. the *charge collection time* (CCT). Moreover, with its variety of pixels, the Investigator-0 chip provides a great opportunity to study the CCT as function of the different sensor design parameters.

4.6.1. Analysis approach

The studies have been performed in the laboratory using X-rays from an ^{55}Fe source. Indeed, for X-rays no information is available about the actual position of the X-ray conversion within the pixel. However, the fraction of the total deposited charge collected in the seed pixel can be used as a measure for the distance of the conversion point from the seed pixel's collection n-well. In case of a lower relative seed signal, the charge carriers are expected to have a longer diffusion path and therefore a larger charge collection time. Therefore, the collection time is studied according to different groups of pixels of a cluster,

[16] Enlarging the footprint may allow to extend the depletion volume without the penalty of an increased capacitance involved with an enlargement of the junction area.



(a) Signal groups for pixel group 0.

(b) Average waveforms.

Figure 4.22.: Definition of the signal groups for the analysis of the charge collection time (a) and average waveforms for each signal group, normalized to the calibration peak signal (b) for an Investigator-0 pixel with a pitch of 30 µm, a 3.31 µm^2 octagonal n-well electrode and 3.0 µm spacing between the n-well and the surrounding p-well (MM 110) at $V_{BB} = -6$ V.

and in turn, for different groups (bins) of pixel signals. In detail, the groups are defined as follows:

- As presented in Fig. 4.21, the pixels in an $n \times n$ pixel matrix around the seed pixel are grouped according to their distance from the seed pixel, the group identifier being increased with increasing distance. The seed pixel itself is defined as pixel group 0.

- As presented in Fig. 4.22a, ten signal groups are defined. The grouping is performed with respect to the calibration peak obtained from the seed signal histogram. Signal group 0 is centered around the calibration peak, the group identifier being reduced towards lower signal. An identical signal grouping is applied to the other pixel groups.

For each group average waveforms are calculated[17]. Since with X-rays the actual time of the X-ray conversion cannot be determined, the necessary temporal alignment of the waveforms is performed with respect to the hit sample. Furthermore, the different offsets of the baseline signal level obtained for each pixel are subtracted. Fig. 4.22b presents the average waveforms for each of the signal groups presented in 4.22a, normalized to the signal obtained for the calibration peak.

[17] The statistics in each group strongly depend on the charge collection performance of the pixel under study, i.e. on the characteristics of the charge sharing.

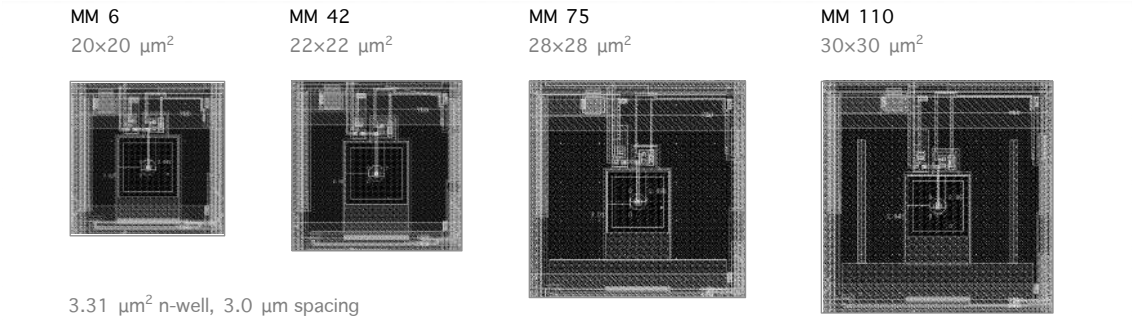


Figure 4.23.: Specifications of the pixels considered in the charge collection time study.

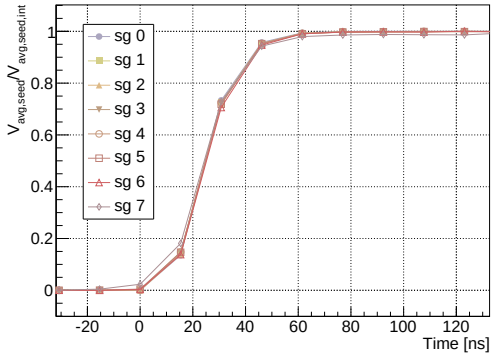
4.6.2. Results

A detailed characterization of the charge collection time depending on the pixel pitch, the reverse substrate bias V_{BB}, and the collection diode geometry (n-well size, spacing, footprint) has been performed. Fig. 4.24 shows results for pixels with different pixel pitches, but identical collection diode geometry, for different values of V_{BB}. The detailed specifications of the regarded pixels are presented in Fig. 4.23: all pixels feature an $3.31\,\mu m^2$ octagonal n-well with 3.0 µm spacing between the n-well and the surrounding p-well, while the pitch ranges from 20 µm to 30 µm. Thus, while the footprint area is constant, the pixel area is more than doubled. As a conseqence, the non-depleted sensor volume will be significantly enlarged[18].

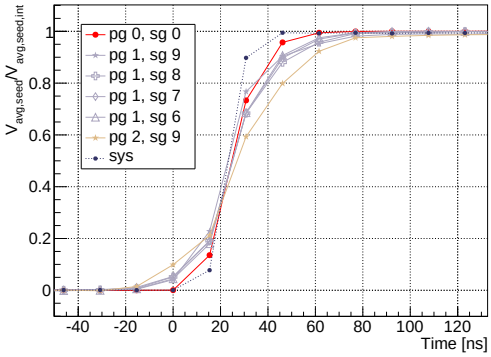
Results are shown in Figures 4.24a to 4.24f. To highlight the changes in the charge collection time, the average waveforms are further normalized to their asymptotic value (i.e. after charge collection). The plots in the left column present the waveforms for the different signal groups of pixel group 0, i.e. for the seed pixel. In contrast, the plots in the right column present the average waveforms for the signal groups of the remaining pixel groups. Only groups with sufficient statistics are represented[19]. For the pixel with 20 µm pitch at $V_{BB} = 0\,V$, contrary to expectations, no dependency of the charge collection time on the relative amount of charge collected in the seed pixel can be recognized (cf. Fig. 4.24a). Moreover, the time required for the average waveforms to rise from 20 % to 95 %, further referred to as the charge collection time (CCT) is in the order of 30 ns. Since, however, for events in which the X-ray conversion takes place within the depletion volume a CCT below 1 ns is expected (cf. Sec. 3.6.1), the contribututions of systematic effects related to the chip and the readout system were further investigated.

[18] This can be expected since for typical pixels and reverse bias voltages the pixel pitch only has a minor influence on the depletion volume compared to the collection diode geometry.

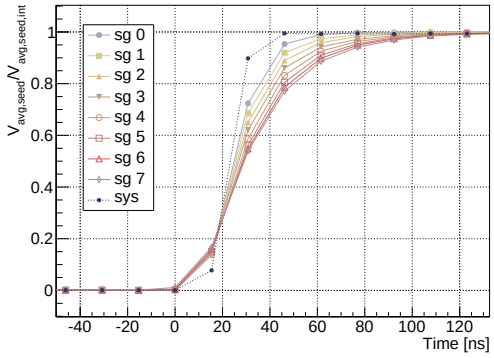
[19] Since by definition most of the charge is collected in the seed pixel, for the pixel groups of the neighbour pixels only the signal groups with a large group identifier, representing a smaller fraction of charge collected in the respective pixels, are populated.



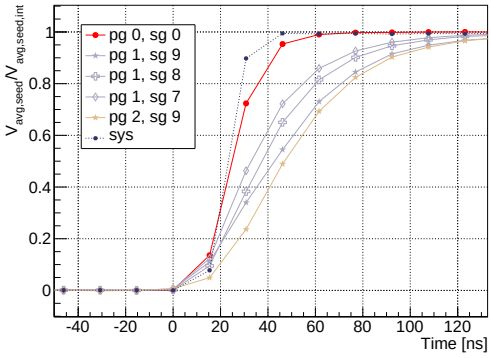
(a) 20 µm pitch, $V_{BB} = 0\,\mathrm{V}$.



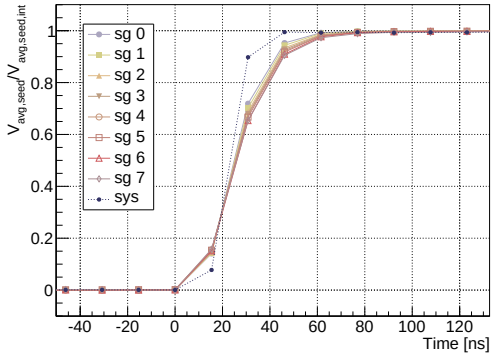
(b) 20 µm pitch, $V_{BB} = 0\,\mathrm{V}$.



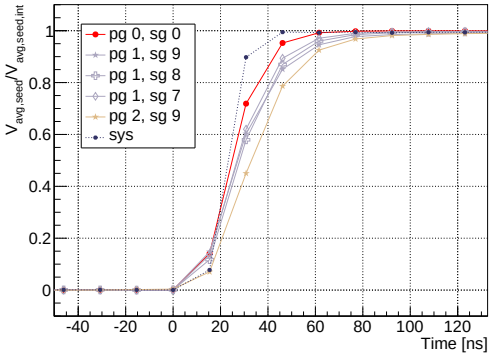
(c) 30 µm pitch, $V_{BB} = 0\,\mathrm{V}$.



(d) 30 µm pitch, $V_{BB} = 0\,\mathrm{V}$.



(e) 30 µm pitch, $V_{BB} = -6\,\mathrm{V}$.



(f) 30 µm pitch, $V_{BB} = -6\,\mathrm{V}$.

Figure 4.24.: Normalized average waveforms for Investigator-0 pixels with different pixel pitches but identical collection diode geometries (3.31 µm^2 octagonal n-well electrode and 3.0 µm spacing between the n-well and the surrounding p-well), and in addition for different values of V_{BB}. For reference, the average waveform measured with the INVROS for a step function with a rise time with 10 ns is plotted alongside in each plot (named *sys*).

Systematic effects The behaviour of the readout system has been studied according to the following approach:

- First, a step function with an amplitude of 70 mV and a rise time of 10 ns was applied to the input of the analogue front-ends of the INVROS. In analogy to the measurements with X-rays, this signal was supplied at random times without correlation to the ADC clock.

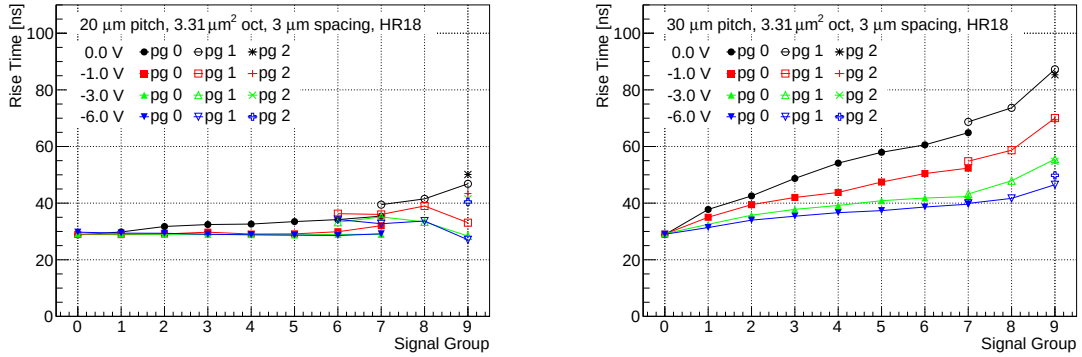
- Subsequently, the data was analyzed using the same procedure as for the data obtained with the Investigator-0. The result is an average waveform similar to the ones obtained for the Investigator-0.

The resulting average waveform is drawn alongside in each plot (referred to as *sys*). As can be clearly recognized, it exhibits a rise time in the order of 20 ns and is thus shorter than for all waveforms obtained with the Investigator-0.
The remaining discrepancy can be attributed to the rise time inherent to the Investigator-0 chip, for which device simulations yield a value in the order of 15 ns [82].

In summary, the results obtained from Fig. 4.24a (for the seed pixel) are compatible with a CCT in the in the order of a few ns. As expected, however, Fig. 4.24b shows that the CCT is increased for the neighbour pixels, i.e. pixel groups with a larger group identifier. By comparing the waveforms of pixel groups 1 and 2, it can be observed that the collection time is furthermore increased for the neighbour pixels with a larger distance from the seed pixel, an effect that can be attributed to the increased diffusion path lengths.

Influence of the pixel pitch and reverse substrate bias Contrary to the pixel with 20 µm pitch, for the pixel with 30 µm pitch, at $V_{BB} = 0\,\mathrm{V}$, the dependency of the charge collection time on the signal group becomes clearly visible (cf. Fig. 4.24c). For the events in which less charge is collected by the seed pixel and thus the X-ray conversion is assumed to occur further from the depletion region, the charge collection time is significantly increased.i In Fig. 4.24d it can be observed that similar effects, but even more pronounced, occur in the pixel groups of the neighbouring pixels. Figures 4.24e and 4.24f show that the increased CCT involved with the increased pixel pitch can be largely compensated by increasing V_{BB} to $-6\,\mathrm{V}$.

Fig. 4.25 presents a summary of the average waveform rise times for the two pixel pitches of 20 µm and 30 µm and four reverse substrate bias voltages of 0 V, −1 V, −3 V and −6 V. The data is presented as a function of the signal group, i.e. the relative amount of charge collected in the pixels, where an increasing signal group identifier corresponds to less charge collected. Correspondingly, signal group 0 represents the events in which the X-ray conversion is assumed to occur within the depletion volume and hence all charge is



(a) 20 µm pitch.

(b) 30 µm pitch.

Figure 4.25.: Summary of the charge collection time measurements for a pixel with a 20 µm pitch (a) and a pixel with 30 µm pitch (b) at different V_{BB} values, as function of the signal group. Both pixels consist of a 3.31 µm^2 octagonal n-well electrode and 3.0 µm spacing between the n-well and the surrounding p-well.

collected with the seed pixel.
In summary, the following observations can be made:

- Regarding Fig. 4.25a, for the pixel with 20 µm pitch only for $V_{BB} = 0$ V a weak increase of the rise time as a function of the signal group is observable. For larger reverse bias, the rise time measured for the seed pixel (pg = 0) appears constant at the minimum resolvable value of 30 ns. As previously discussed, this value is compatible with charge collection times (CCT) of the order of a few ns. For the neighbouring pixels (pg > 0), the rise times of the waveforms are only slightly increased.

- The situation changes for the pixel with 30 µm pitch, where the rise times, and consequently the CCT, show a clear dependency on the reverse bias and the signal groups:

  - As expected, for the case that the X-ray conversion occurs in the depletion region and all charge is collected within the seed pixel, i.e. pg 0 and signal group 0, the curves for different reverse substrate bias match in a single point[20].

  - In case that lower fractions of charge are collected within the seed pixel (i.e. signal groups > 0), the rise times measured in the seed pixel (pg = 0) for $V_{BB} = 0$ V reach values up to 70 ns, while in the neighbouring pixels (pg > 0) reach up to 90 ns. The rise times are gradually mitigated with increasing reverse bias,

[20] Indeed, for this case, i.e. signal group 0 and pixel group 0, even the curves for the different pixel pitches match in a single point. This result is to be expected, as in first approximation the charge collection time within the depletion region does not vary as function of the pixel pitch and revere bias voltage.

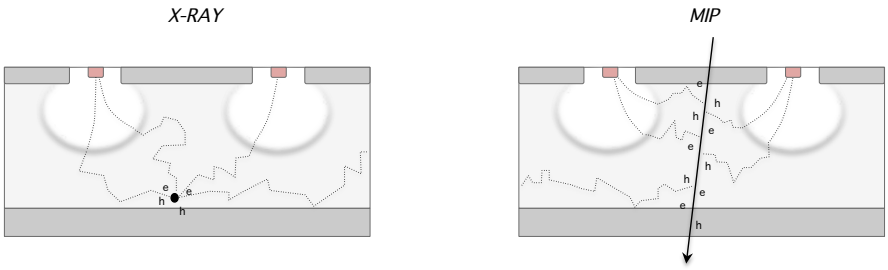


Figure 4.26.: Schematic representation of the difference of the charge generation process between X-rays and MIPs.

so that for $V_{BB} = -6\,\mathrm{V}$, for the seed pixel, the maximum obtained value is reduced to 40 ns, and to 50 ns for the neighbouring pixels.

Discussion of the results Reducing the CCT is beneficial as it decreases the probability for the charge to be trapped and therefore increases the tolerance to radiation induced bulk damage in the sensor.
All observations above indicate that the collection time is reduced by an enlargement of the depletion volume and the involved enhancement of the charge collection efficiency. As discussed in Sec. 4.5.3, beside increasing the reverse bias, the depletion region may be extended by tuning the geometry of the charge collection diode.
In the context of the sensitivity of the sensor performance to bulk damage, also the observed correlation between the collection time and the distance of the X-ray conversion from the collection n-well is of interest. It can be expected to results in the effect that the amount of charge lost due to trapping is depending on the impact position of the ionizing particles, i.e. the further the ionization occurs from the collection n-well, the more charge gets trapped. Moreover considering that the charge is shared among more pixels if the ionization happens further from the collection n-well, regions of decreased detection efficiency may be created.

It should be noted, however, that the final application of the ALPIDE chip is the measurement of MIPs rather than X-rays. As discussed in Sec. 4.4, both types of radiation have very different characteristics of the charge generation process: whereas X-rays are absorbed in a single point-like region by photoelectric conversion, MIPs generate e-h pairs approximately uniformly along their track. Thus, as illustrated in Fig. 4.26, while for X-rays events occur where *all* charge is generated far from the collection n-well, for MIPs a part of the charge will always be generated in a comparably short distance to the boundary of the depletion volume and thus exhibiting small collection times. The situation will even be improved for inclined tracks. The detection efficiency for MIPs may therefore be expected to be less sensitive to bulk damage than for X-rays.

Another point to be noted is that, except for the case where the X-ray conversion occurs within the depletion volume and the charge is dominantly collected by drift, the measured charge collection times are significantly shorter than predicted by the depletion approximation model presented in Sec. 3.6. A possible explanation is that the assumption of a completely field-free epitaxial layer (except for the depletion regions around the collection n-wells) is not fulfilled. Here also fields created by doping concentration gradients in the epitaxial layer are expected to play a role[21].

4.7. Sensor performance after neutron irradiation

The study of the sensor performance after neutron irradiation is based on results obtained with the Explorer-1, of which a sample was irradiated at the TRIGA MarkII Reactor at JSI in Ljubljana with equivalent fluences of $2.5 \times 10^{12}\,1\,\mathrm{MeV\,n_{eq}/cm^2}$ and $1 \times 10^{13}\,1\,\mathrm{MeV\,n_{eq}/cm^2}$.

4.7.1. Leakage current and noise

Fig. 4.27 shows the total noise[22], averaged over all pixels in sector 5 of the Explorer-1, in units of ADC counts (a) and as ENC (b), as a function of the equivalent fluence and for three different V_{BB} values. The noise in terms of ADC counts for the non-irradiated chip is observed almost independent of the reverse substrate bias. Considering the fact that the pixel input capacitance C_p is reduced by more than half when decreasing V_{BB} from 0 V to −6 V, this indicates that the noise is largely dominated by the contributions from the readout circuit. After irradiation, the noise shows a strong increase, which is even more pronounced for larger reverse substrate bias. In terms of ENC, the noise is observed to range between 10 and 18 electrons for the non-irradiated pixels, depending on the reverse bias, and between 20 and 25 electrons after irradiation with $1 \times 10^{13}\,1\,\mathrm{MeV\,n_{eq}/cm^2}$.

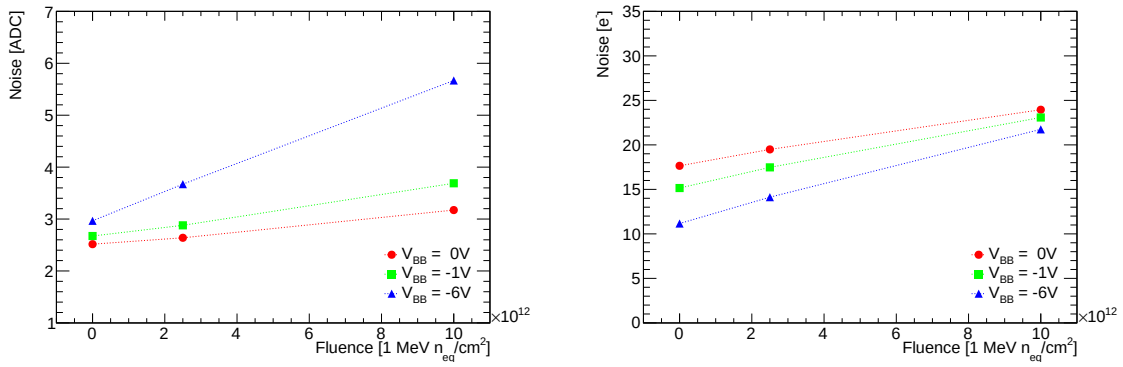
The contribution of the leakage current to the total noise was studied separately before and after irradiation and for different V_{BB}. It is estimated by measuring the voltage change $\Delta V(t)$ at the sensing node as function of time, which is related to a charge variation $\Delta Q(t)$ in the pixel input capacitance C_p by[23]:

$$\Delta V(t) = \frac{\Delta Q(t)}{C_p}, \tag{4.15}$$

[21] See also discussion in Sec. 3.2.3.

[22] The presented values are calculated using Eq. (D.4), i.e. they represent the signal corrected for common-mode noise.

[23] All measurements were performed at 30 °C and $V_{\mathrm{RST}} = 0.7\,\mathrm{V}$.



(a) Total noise. **(b)** Total noise (ENC).

Figure 4.27.: Total noise in terms of measured voltage (a) and ENC (b) of the Explorer-1, sector 5, presented as a function of neutron fluence for the three V_{BB} values 0 V (red), −1 V (green) and −6 V (blue). The pixels consists of a 2.0 µm diameter octagonal n-well electrode with 2.6 µm spacing.

where the charge variation $\Delta Q(t)$ as function of time is, in turn, depending on the leakage currents[24].

This indirect method, however, cannot be taken as an absolute leakage current measurement of the collection diode, since the leakage current of the collection diode may be compensated by contributions of other sources of leakage current present at the input net. A schematical representation of the input net including the sensing node is presented in Fig. 4.28. For the Explorer-1 chip - when the reset transistor is turned off - the main secondary contribution originates from the p-n junction formed by the p^{++} implant for the drain terminal of the reset transistor and the n-well it is placed in[25]. For leakage current studies, after closing the reset transistor, the input net can hence be modeled by two reversely biased diodes (n-well/p^--epi and p^{++}/n-well, cf. Fig. 4.28 right side), exhibiting the leakage currents I_1 and I_2, respectively.

Following this model, the change of the sensing node potential as a function of time after

[24] The measurement is realized by changing the default steering sequence of the Explorer-1 (cf. Fig. 4.5) as follows: the row and column sequencer is stopped at the desired pixel memory, whereafter the pixel reset is performed, the corresponding *STORE* signal is activated and ADC is enabled for sampling. The *RELOAD* value of the sequence is set right before the activation of the *RESET* signal, so that the later part of the sequence is repeated periodically while the same pixel memory is kept being connected to the output pad.

[25] Possible additional sources as the channel and gate leakage currents of the reset transistor (M2), and the gate leakage current of the source follower transistor (M1) can be neglected [83]: - Gate leakage currents: for the gate leakage current, the a maximum value of 8 fA µm^2 is specified. In case of the Explorer-1 the size of the input transistor is $W/L = 0.22\,\mu m/0.1\,\mu m$, whereas reset transistor is $W/L = 1.0\,\mu m/0.3\,\mu m$, thus resulting in maximum expected gate leakage currents in the range of fA. - Channel leakage currents: when the reset transistor is switched off, its source terminal is at $V_{RST} = 0.7$ V, while the potential at its gate terminal is set to $V_{DDA} = 1.8$ V, resulting in $V_{gs} = -1.1$ V. At this level, the gate leakage current is expected to be below 1 fA.

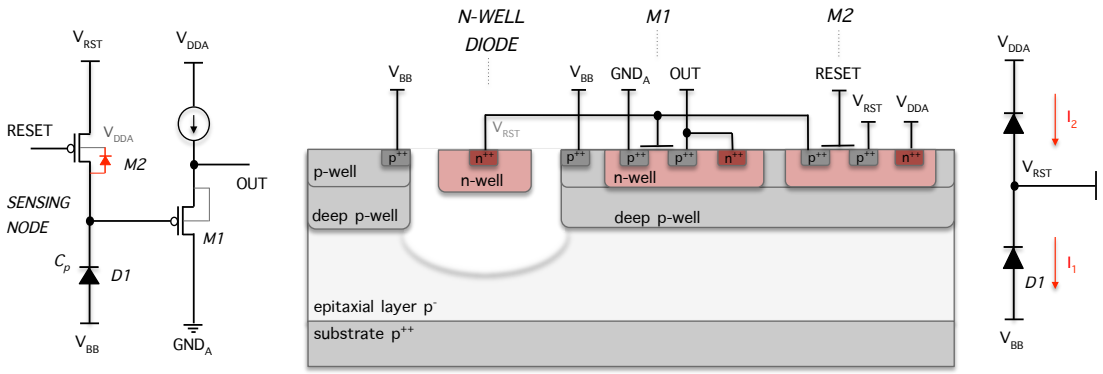


Figure 4.28.: Schematical representation of the input net.

the reset $\Delta V(t)$ can be expressed as

$$\Delta V(t) = \frac{(I_1 - I_2)\, t}{C_p}, \tag{4.16}$$

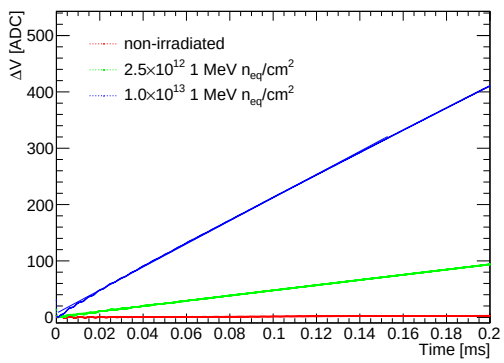
and is therefore proportional to the net leakage current $I_{net} = I_1 - I_2$. Moreover, according to Eq. (4.3) the mean square value of the noise sampled on the pixel input capacitance at time t is given by[26]

$$\langle \Delta V(t)^2 \rangle = \frac{q\sqrt{I_1^2 + I_2^2}\; t}{C_p^2}. \tag{4.17}$$

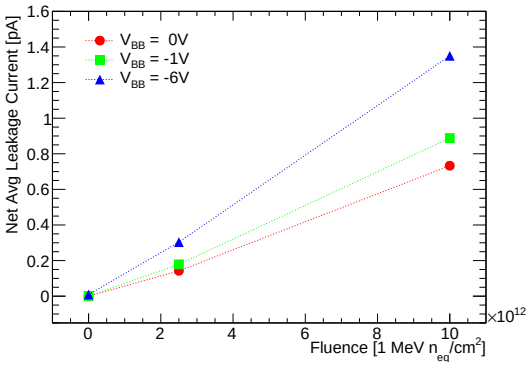
Results on the change of the sensing node potential as a function of the time after the reset are presented in Fig. 4.29a. The data shown are for a single pixel only, averaged over 1000 events. Correlated double sampling (CDS), i.e. the subtraction of the first sample of all subsequent samples is performed offline.
While for the non-irradiated sensor no change of the sensing node potential can be observed, there is a strong linear decrease of ΔV for increased irradiation levels. The direction of the potential change reveals a dominance of the leakage current through the collection diode, which is enhanced after irradiation.

A summary of the results on the net leakage currents plotted as a function of the equivalent fluence for different reverse substrate bias voltages is shown in Fig. 4.29b. The values presented are estimated applying Eq. (4.16), using the pixel input capacitance C_p evaluated from ^{55}Fe signal spectra according to Eq. (4.9). For the non-irradiated sensor, the net leakage current is below 1 fA, independent of the reverse substrate bias.
For the irradiated sensors the net leakage current shows strong increase. In addition, the

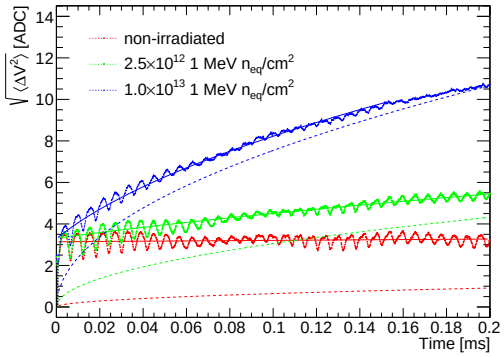
[26] A more precise analysis should also include the change of the collection diode capacitance during the sensing node discharge. For typical integration times in the order of tens or hundreds of µs, however, the discharge due to leakage currents does never exceed the one obtained after, i.e. the hit of a MIP. Therefore, based in the discussion in Sec. 3.3, this is considered to be a negligible effect.



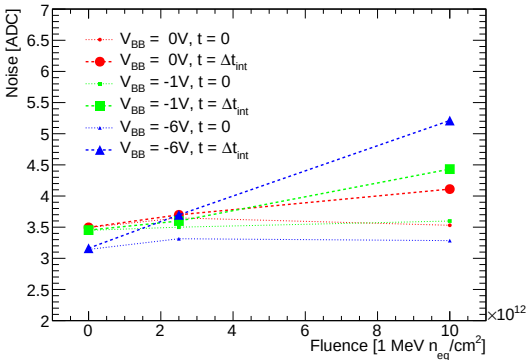
(a) Sensing node discharge $\Delta V(t)$.



(b) Average net leakage current.



(c) $\sqrt{\langle \Delta V(t)^2 \rangle}$.



(d) Noise after reset and integration time.

Figure 4.29.: Sensing node discharge $\Delta V(t)$ (a) and its RMS deviation $\sqrt{\langle \Delta V(t)^2 \rangle}$ (c) as a function of time after the reset measured for a single pixel (pixel 4004, *MEM1*) at $V_{BB} = -6\,\mathrm{V}$. Furthermore noise at different times after the reset (d) and the average net leakage current (b) for the same pixel are presented as a function of neutron fluence for the three V_{BB} values $0\,\mathrm{V}$ (red), $-1\,\mathrm{V}$ (green) and $-6\,\mathrm{V}$ (blue). The pixel consists of a $2.0\,\mu\mathrm{m}$ diameter octagonal n-well electrode with $2.6\,\mu\mathrm{m}$ spacing.

net leakage current also increases for larger reverse bias of the collection diode. This can be understood by reconsidering Eq. (3.21), according to which the volume related leakage current is directly proportional to the product $\Phi_{eq} \cdot V$ of the equivalent fluence Φ_{eq} and the depleted volume V, which in turn is an increasing function of the reverse bias. Consequently, the largest net leakage current, amounting to approximately $1.4\,\mathrm{pA}$ (for the pixel under study), is obtained for $V_{BB} = -6\,\mathrm{V}$ and a fluence of $1 \times 10^{13}\,1\,\mathrm{MeV\,n_{eq}/cm^2}$.

The RMS deviation of the sampled sensing potential as a function of the time after the reset is presented in Fig. 4.29c. The data shows a behaviour that can be parametrized with a function of the form

$$f(t) = \sqrt{\alpha^2 + \beta t}. \tag{4.18}$$

Since CDS is applied, the factor α represents the noise of the readout circuit, whereas by

a comparison with Eq. (4.17) the factor β can be identified as the shot noise contribution from the leakage currents: $\beta = q\sqrt{I_1^2 + I_2^2}/C_p^2$. The sole shot noise contribution is plotted separately for each of the irradiation levels. Beside the overal progression of the data according to Eq. (4.18) one can also clearly recognize a superimposed oscillation. This effect can be traced back to a ringing introduced on the input net by turning off the reset transistor.
Simultaneously measuring the sensing node discharge $\Delta V(t)$ and its RMS deviation $\sqrt{\langle \Delta V(t)^2 \rangle}$ in principle allows for a disentanglement of the two leakage current contributions I_1 and I_2 by combining Eq. (4.16) and Eq. (4.17). The results have not been fully conclusive, however, only indicating that the collection diode leakage current is the dominating contribution.

Fig. 4.29d presents a summary of the noise right after the reset (i.e. factor α, the noise of the readout circuit) and after the integration time, determined from fits as presented in Fig. 4.29c, as a function of the neutron fluence and for three different values of V_{BB}. It can be clearly observed that while the noise contribution of the readout circuit is almost independent of the irradiation level, the total noise after the default integration time (28.8 µs) is strongly increased.
In summary, the example data presented for a single pixel in Fig. 4.29 indicates that a large part of the increase of the total noise presented in Fig. 4.27 results from an increase of the leakage current at the input net.

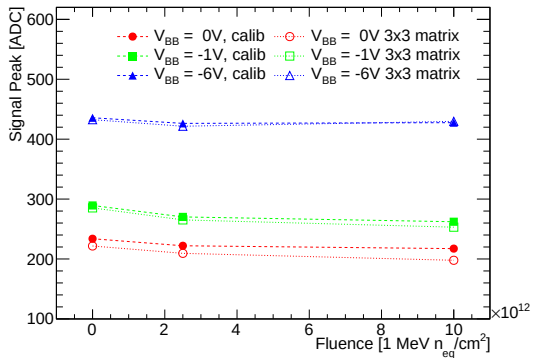
4.7.2. Charge collection efficiency

The influence of bulk damage following on the charge collection efficiency (CCE) has been studied by the characteristic signal spectra, i.e. the spectra for the seed-, matrix-, and single-pixel cluster signal for ^{55}Fe X-rays[27]. In order to mitigate effects from changes of the working point and the differential gain of the front-end circuit after irradiation, a gain correction of the signal spectra was performed (cf. Sec. D.1.1).

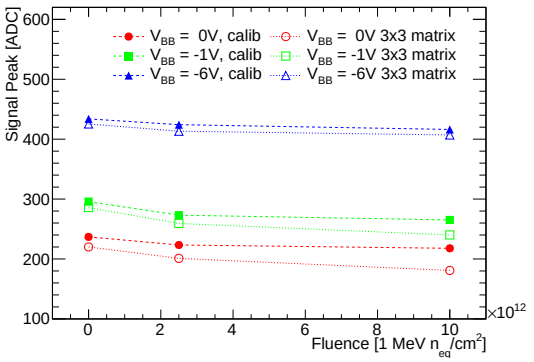
Figures 4.30a and 4.30b show the signal value of the calibration peak and the matrix signal peak, measured for Explorer-1 pixels with two different pitches, before and after irradiation with neutrons, and for three reverse substrate bias voltages.
Two main effects can be observed:

- The first effect is that the signal for the calibration peak is slightly reduced with increasing radiation. Since a correction for changes of the gain of the readout circuit has been applied, and the charge collected in the events forming the calibration peak is not assumed to be reduced, the observed decrease of the signal is expected to

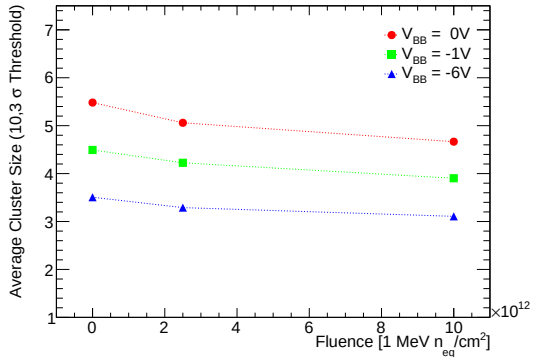
[27] The details of the method have been described in Sec. 4.4.3.



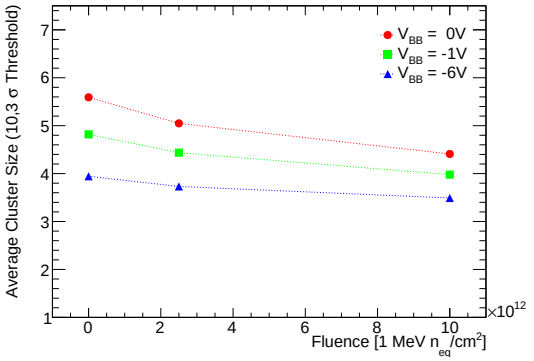
(a) Signals, 20 µm pitch.



(b) Signals, 30 µm pitch.



(c) Cluster multiplicity, 20 µm pitch.



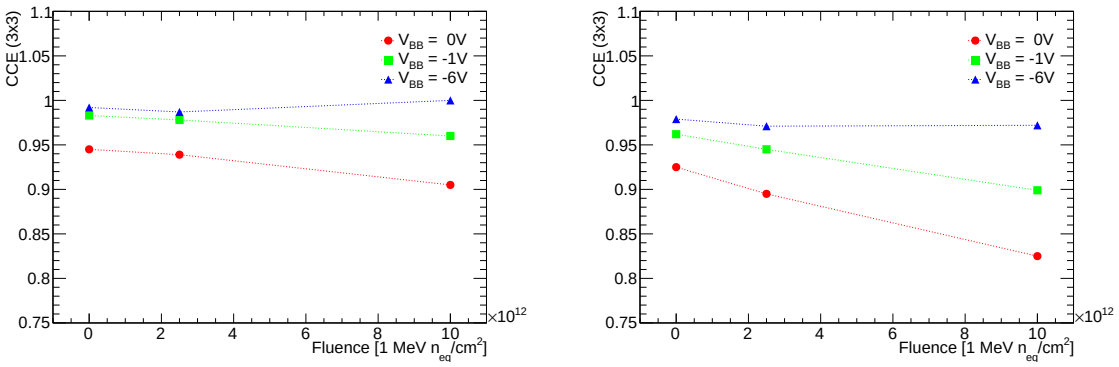
(d) Cluster multiplicity, 30 µm pitch.

Figure 4.30.: MPV of the matrix and single pixel cluster signal (a, b), and cluster multiplicities ($10\,\sigma$, $3\,\sigma$) (c, d) due to X-rays from an ^{55}Fe source for a pixel with a 2.0 µm diameter octagonal n-well electrode with 2.6 µm spacing on an HR18 wafer. The data is presented as a function of neutron fluence for the three V_{BB} values 0 V (red), −1 V (green) and −6 V (blue).

have its origin in a slight increase of the pixel input capacitance after irradiation. A possible explanation for this effect are changes of the effective doping concentrations at the junction.

- The second effect that can be observed is that the offset between the signal for the calibration peak and the matrix signal peak is increased as a function of the neutron fluence. Alongside, as shown in Fig. 4.30c and Fig. 4.30d, the cluster multiplicity is reduced. It can be clearly recognized that the effects are more pronounced at lower reverse bias and larger pixel pitch, indicating a deterioration of the matrix CCE.

The results for the matrix CCE are presented in Figures 4.31a and 4.31b. As expected from the observations above, the matrix CCE shows a strong dependency on the neutron fluence, in particular at large pixel pitches and low reverse bias, whereas the use of −6 V leaves the matrix CCE almost unchanged at about 100 %.
In regard of a pixel chip with binary readout (e.g. the ALPIDE), these results on the



(a) Matrix CCE, 20 µm pitch.

(b) Matrix CCE, 30 µm pitch.

Figure 4.31.: Matrix CCE for Explorer-1 pixels with two different pitches (20 µm (left) and 30 µm (right)), but equivalent collection electrode geometries (2.0 µm diameter octagonal n-well electrode with 2.6 µm spacing). The data is presented as a function of neutron fluence for the three V_{BB} values 0 V (red), −1 V (green) and −6 V (blue).

matrix CCE have to be put into context to the detection efficiency. In order to obtain 100 % detection efficiency, it is required that at least a single pixel, i.e. the seed pixel, shows a signal above threshold. Hence, it is of larger interest by which extent the charge collection efficiency within the seed pixel, i.e. the seed CCE, deteriorates due to bulk damage. Indeed, based on the discussion of the results on the charge collection time (cf. Sec. 4.6), it can be expected that the seed CCE is less sensitive to bulk damage than the matrix CCE.

The effects of bulk damage on the detection efficiency have been studied in detail using the first full-scale ALPIDE prototype, the so-called pALPIDE-1. The results of this study are presented in the next chapter (Sec. 5.3).

4.8. Summary

A summary on the results of the influence of each of the sensor design parameters and the reverse substrate bias on the sensor performance before irradiation has been presented in Sec. 4.5.6.

In general, the charge collection process was found to be improved by an enlargement of the (relative) depletion volume. It has been shown that this can be achieved by reducing the pixel pitch, increasing the reverse substrate bias, and optimizing the layout of the collection diode. For the studied pixels of the Explorer-1 with 20 µm pitch on an 18 µm thick epitaxial layer, the relative depletion volume is about 5 % for $V_{BB} = 0$ V, while it can be increased to up to about 20 % for $V_{BB} = -6$ V. For pixels with the same collection diode footprint, the increase is larger for pixels with a larger collection n-well.

When varying the collection diode geometry parameters, however, also effects on the pixel input capacitance have to be taken into account. The capacitance is typically increased for a larger collection n-well. A reduction of the pixel capacitance by increasing the reverse substrate bias has been observed to be limited by the spacing between the n-well and the surrounding p-well. For the pixels of the Explorer-1, an input capacitance of approximately 5 fF is reached for $V_{BB} = 0\,\mathrm{V}$, which can be reduced to about 2.0 fF when increasing V_{BB} to $-6\,\mathrm{V}$.
The leakage currents for non-irradiated sensors were found to be negligible, below a fA per pixel. RTS noise has been observed and is strongly dependent on the input transistor size, affecting a few percent of the pixel in the Explorer-1 chip [16].

The charge collection time has been studied for pixels with a pitch of 20 µm and 30 µm, respectively, an epitaxial-layer thickness of 18 µm and a collection-diode footprint of $7.2 \times 7.2\,\mu\mathrm{m}^2$. For the pixels with 20 µm pitch, the charge collection time was found to be in the order of a few ns, independent of the applied reverse substrate bias and the position of the X-ray conversion. For the pixels with 30 µm pitch and $V_{BB} = 0\,\mathrm{V}$, the collection time becomes dependent on the distance of the X-ray conversion from the collection n-well. However, this effect can be almost fully compensated by increasing V_{BB} to $-6\,\mathrm{V}$.

The effects of bulk damage have been studied for fluences, Φ_{eq}, up to $1 \times 10^{13}\,1\,\mathrm{MeV\,n_{eq}/cm^2}$. It has been shown that a deterioration of the charge collection efficiency can be fully compensated by an increase of the reverse substrate bias to $-6\,\mathrm{V}$. After irradiation, however, leakage currents become notable and show a strong dependency on the reverse substrate bias, reaching values up to a few pA per pixel for $V_{BB} = -6\,\mathrm{V}$ and $\Phi_{\mathrm{eq}} = 1 \times 10^{13}\,1\,\mathrm{MeV\,n_{eq}/cm^2}$. Leakage currents at the input net hence can become a significant noise source. It should be noted, however, that even at the largest reverse bias voltage and irradiation level, the total ENC of the Explorer-1 chip does not exceed $30\,e^-$ after an integration time of approximately 30 µs.

The results discussed in this chapter represent a valuable input for the ALPIDE development, as they provide a detailed overview of the trends involved with the variation of geometrical paramaters and the reverse substrate bias. In general, however, the optimal combination also depends on constraints imposed by the overal chip design, such as a fixed pixel pitch or a maximum allowable collection diode footprint. Therefore, along with the improvements of the readout circuitry [48], also the sensitive layer and the collection electrode remain subject to optimization towards the final ALPIDE design.

5. pALPIDE-1 - First full-scale ALPIDE prototype

The pALPIDE-1 represents the first full-scale prototype within the ALPIDE development. It contains the novel low-power front-end and the sparsified readout architecture characteristic for the ALPIDE design. For optimization purposes its pixel matrix integrates four pixel types with differing collection diode geometries and reset mechanisms.

The first part of this chapter is dedicated to a description of the ALPIDE architecture, with particular focus on the operating principle of the low-power front-end circuit. The second part of the chapter will discuss the characterization results on the behaviour of the front-end depending on the respective bias parameters and pixel type. The interpretation of the results is largely based on the results obtained on the small-scale prototypes discussed in the previous chapter. It will be shown that working points of the pALPIDE-1 can be obtained for which the detection efficiency, position resolution and fake-hit rate are in line with, or even surpassing, the requirements set by the ALICE ITS upgrade, leaving a satisfying operational margin also after irradiation with an equivalent fluence of $1 \times 10^{13}\,1\,\mathrm{MeV\,n_{eq}/cm^2}$.

5.1. pALPIDE-1

The active area of the pALPIDE-1 consists of 524288 pixels with a pitch of 28 µm, arranged in 1024 columns and 512 rows, in total covering $28.7\,\mathrm{mm} \times 14.3\,\mathrm{mm}$. The chip periphery is placed along the long edge of the die, with a height of approximately 1 mm, leading to a total die size of $30\,\mathrm{mm} \times 15.3\,\mu\mathrm{m}$. The total thickness of the chip, including the metal stack, the epitaxial layer and the substrate amounts to 50 µm.

The design exploits all six metal layers offered by the TowerJazz 180 nm technology (cf. Sec. 2.2.2). To ensure for a solid power distribution, the top two layers are mainly used for power routing lines. For the same reason, in total 72 power pads are placed over the pixel matrix. In order to reduce the coupling between the analogue and digital circuitry in the chip, the respective power domains (all at a nominal voltage of 1.8 V) are kept separate.
In the ALPIDE design only the information whether a pixel was hit or not is read out. The hit discrimination is implemented at the pixel level, while the threshold settings for

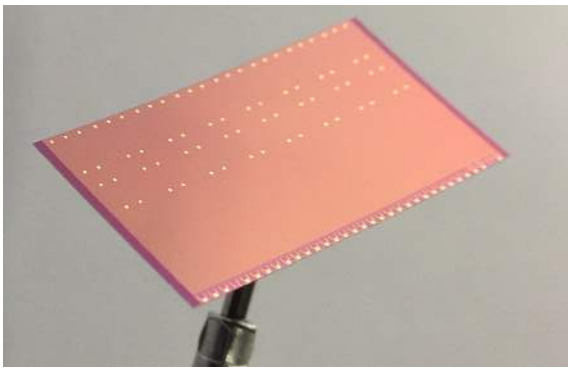


Figure 5.1.: The pALPIDE-1 chip with a die size of 30 mm × 15.3 µm and a total thickness of 50 µm.

the discriminators are provided globally. The digital pixel outputs are connected to a digital circuit, called AERD (Address-Encoder Reset-Decoder) [84], which is arranged in the center of a pair of columns, the so-called *double columns*. Following a toplogical priority this circuit sequentially provides the addresses of hit pixels to the digital periphery of the chip. The circuit is implemented in a way that the hit register of the respective pixel is reset after the read operation, whereupon the AERD moves to the next hit pixel. This procedure is iterated until all hit pixels within a double column are read out.
Overall, the pixel matrix is organized in 32 regions, each of them consisting of 16 double columns. The regions are each read out by a *region readout unit* (RRU), which buffers the hit data. The *top readout unit* (TRU) combines the data from the 32 RRU's and transmits it through an 8 bit wide CMOS data port at 40 MHz. A top-level control block, interfaced by JTAG, enables access to the control and status registers in the periphery, as well as to the memories in the RRUs.

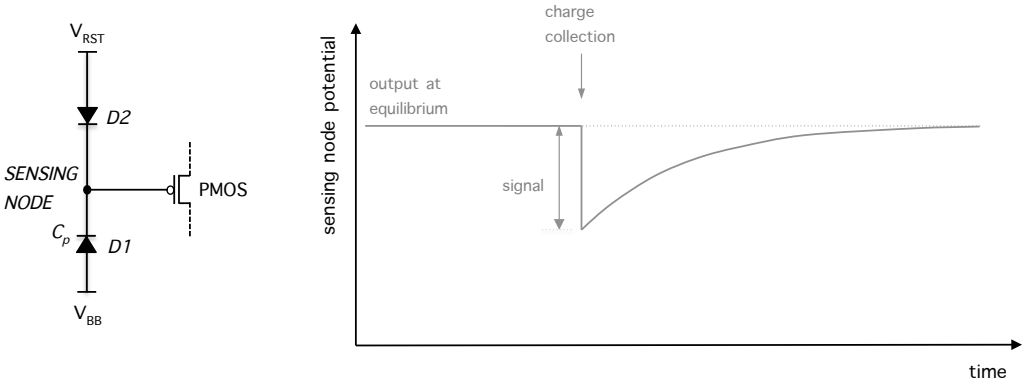
The following sections describe the main building blocks of the pALPIDE-1, highlighting the low-power front-end of the chip. It should be kept in mind, however, that the pALPIDE-1 is the first full-scale prototype of the ALPIDE. As such, the focussed was laid on the performance of the pixel matrix with its novel low-power front-end and the in-pixel digital circuitry. However, it does not yet contain the final interface, the high-speed output link and the in-pixel multi event buffer. As outlined in Sec. 2.2.2, these building blocks will be implemented and characterized in later prototypes.

5.1.1. Pixel matrix

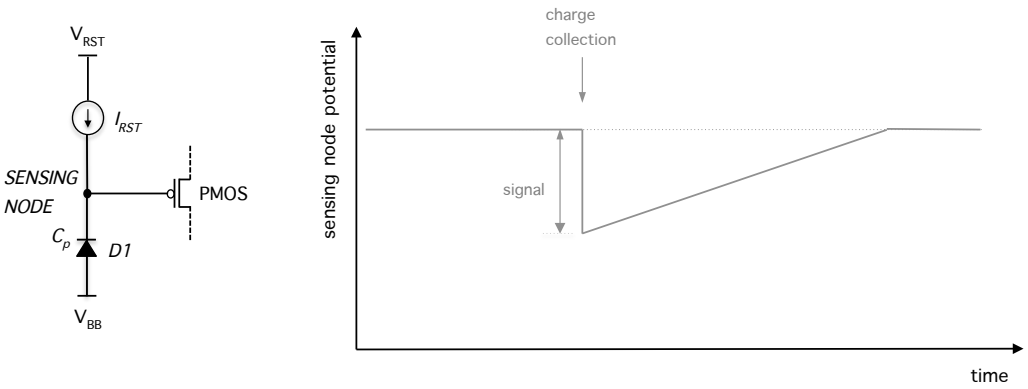
The pixel matrix is subdivided into four submatrices of 256 × 512 pixels also referred to as *sectors*. Each sector is composed of different pixels types. The four pixel types differ

Table 5.1.: Characteristics of the four different pixel types of the pALPIDE-1.

Sector	Columns	N-well diameter	Spacing	Footprint diameter	Reset type
0	0 - 255	2 µm	1 µm	4 µm	PMOS
1	256 - 511	2 µm	2 µm	6 µm	PMOS
2	512 - 767	2 µm	2 µm	6 µm	diode
3	768 - 1023	2 µm	4 µm	10 µm	PMOS



(a) Diode reset.



(b) PMOS reset.

Figure 5.2.: Simplified schematics of the pALPIDE-1 pixel reset mechanisms.

by the geometry of the collection diode and the implementation of the reset mechanism for the sensing node, the details being presented in Tab. 5.1.

As presented in Fig. 5.2, two different reset mechanisms are applied, either via a diode (a) or via a PMOS transistor (b). In both cases the sensing node is reset continuously with a nominal time constant in the order of a ms. In contrast to the active reset employed in

the prototype circuits discussed in the previous chapter, the reset mechanisms applied in the pALPIDE-1 have no intrinsic dead time.
In case of the circuit with a reset diode (D2), as presented in Fig.5.2a, the reset of the potential of the sensing node is achieved by a forward bias current. The current I_D across a diode is described by the Shockley diode equation [85] as

$$I_D = I_S \left(e^{\frac{V_D}{nV_T}} - 1 \right), \tag{5.1}$$

where V_D is the voltage across the diode, I_S is the diode saturation current, n is the ideality factor and $V_T = k_B T/q$ is the thermal potential. In the absence of traversing particles, the small forward current passing through the diode compensates the leakage currents, continuously recharging the pixel-input capacitance C_p. When the sensing diode collects charge deposited by an impinging particle, the potential on the sensing node drops. This causes the forward current to increase, leading to a recovery of the sensing node potential. According to Eq. 5.1, the conductance of a diode can be expressed as

$$g_D = \frac{\mathrm{d}I_D}{\mathrm{d}V_D} = \frac{I_S}{nV_T} e^{\frac{V_D}{nV_T}}. \tag{5.2}$$

The diode conductance thus increases exponentially with increasing voltage across the diode V_D, and increasing I_S, e.g. after irradiation. In the input net of the front-end circuit an increase of V_D can be caused by leakage currents and the collection of signal charge.
Indeed, an increase of the conductance is correlated with a faster recharge time sensing node. Therefore, when employing a diode reset, the following considerations have to be taken into account:

- While the recharge current allows to bring the pixel back to its equilibrium, it also compensates the signal charge. Detecting a hit is thus only possible if the recharge process is sufficiently slow, i.e. much slower than the response time of the front-end circuit.

- The circuit reacts to larger voltage drops ΔV at the sensing node by an exponential increase of the instantaneous recharge current. Large voltage drops can on the one hand be caused by single hit with a large charge deposit in the sensitive layer, e.g. by a delta-ray, or a series of hits with a period of less than the recharge time constant. In this context, the characteristics of the diode conductance in principle imply an intrinsic limit on the hit frequency within a single pixel.

In case of the PMOS reset, the maximum reset current $I_{\mathrm{RESET}}^{\mathrm{max}}$ can be adjusted by varying the respective bias DAC. To avoid a total discharge of the sensing node, it has to be ensured that $I_{\mathrm{RESET}}^{\mathrm{max}}$ is set sufficiently high to compensate increased leakage currents,

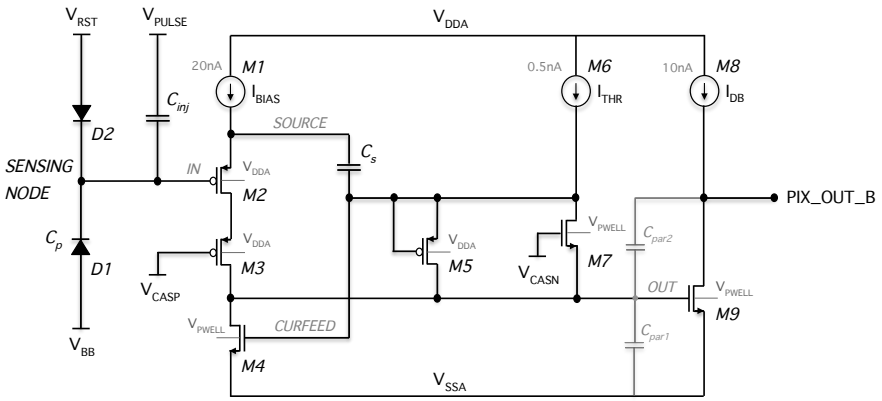


Figure 5.3.: Simplified schematic of the analogue part of the pALPIDE-1 front-end.

e.g. after irradiation. On the other hand, $I_{\mathrm{RESET}}^{\mathrm{max}}$ has to be limited in order to avoid that the collected signal charge is compensated too fast.

5.1.2. Front-end circuit

The in-pixel front-end circuitry of the pALPIDE-1 consists of an analogue part where the signal is shaped and discriminated, and a digital part containing the hit register and additional logic for testing and disabling (masking) the pixel. The details are presented in the following.

Analogue part

A simplified schematic of the analogue part of the pALPIDE-1 front-end is presented in Fig. 5.3. It can be observed that the input net consists of the familiar components and an additional small capacitance C_{inj} (160 aF[1]). This allows testing the front-end response by applying a negative voltage step through the V_{PULSE} node, which can be driven from the digital part of the front-end.
The subsequent analogue front-end circuit can be roughly subdivided into two stages: the first stage, also referred to as the *gain stage*, consists of two branches related to the current sources I_{BIAS} and I_{THR}. The second stage, also referred to as the *discrimination stage*, is related to the current source I_{DB}. In detail, the analogue front-end working principle is as follows:

[1] This is about an order of magnitude lower than the typical total pixel-input capacitance C_p and thus does not influence the performance of the circuit. The injection capacitance is designed such that a voltage step of -1 mV will lead to a charge injection of $1\,e^-$.

- *Static behaviour* - In the absence of perturbations the potential at the *SOURCE* node (and consequently the charge in the capacitance C_s) is defined by the equilibrium potential at the sensing node[2] and the I_{BIAS} current. The current I_{BIAS} flows through the transistors M2, M3, and furthermore M4, defining the voltages at the source terminal of M3 (together with V_{CASP}) and the gate terminal of M4. Together with the input transistor M2, transistor M3 forms a PMOS cascode, ensuring a capacitive decoupling of the *IN* and the *OUT* node. The potential at the *OUT* node is defined by the current I_{THR} and the voltage V_{CASN} applied to the gate of the NMOS cascode transistor M7. The I_{THR} current path passes through the transistors M7 and M4.

- *Dynamic behaviour* - When the sensing node potential drops within a time much shorter than the time constant at the *SOURCE* node, e.g. due to the collection of charge generated in the sensor by a traversing particle, the V_{sg} of the PMOS input transistor will be increased[3]. This consequently leads to an additional current I_s through M2 and furthermore M3[4]. For this additional current to be allowed to pass M4, the voltage at its gate, that is the *CURFEED* node, would have to adjust. However, since this is only happening to small extent and with a certain delay due to the presence of C_s, the current I_s will charge the *OUT* node, creating a positive voltage pulse.
  After the onset of the pulse, the *OUT* node is restored to its baseline by the following mechanism: as soon as the *OUT* node is charged to a sufficiently large potential, $V_{gs} = V_{\mathrm{CASN}} - V_{\mathrm{OUT}}$ of M7 approaches zero, largely reducing its conductance. The current I_{THR} will hence be redirected and start charging the *CURFEED* node, leading to the gate potential of M4 to be increased. This consequently allows the current through M4 to be increased and the *OUT* node to be discharged, so that M7 becomes conductive again and the *OUT* and furthermore the *CURFEED* node potential are restored to their baseline value. Thus, while the baseline potential at the *OUT* node can be adjusted by varying V_{CASN}, the duration of the restoration process and the (relative) pulse height and width can be reduced by increasing I_{THR}.
  The peak height and the pulse width for the circuit presented so far are larger for greater amounts of collected charge. However, in order to limit the pulse duration in

[2] As discussed in Sec. 4.1.1, the potential at the sensing node is defined by V_{RST} and possible voltage drops across the reset diode or transistor.

[3] V_{sg} is the source-to-gate voltage of the transistor. In a source follower circuit, the input transistor source follows the gate voltage. In pALPIDE-1 front-end circuit, the capacitance C_s is introduced in order to obtain a certain time constant τ_{SOURCE} at the *SOURCE* node, which consequently leads to an AC-behaviour of the circuit. The larger the value of C_s, the longer is the reaction time of the front-end circuit. In this pALPIDE-1, a compromise on the layout area fixed C_s to approximately 350 fF.

[4] The charge related to the current I_s is provided by C_s.

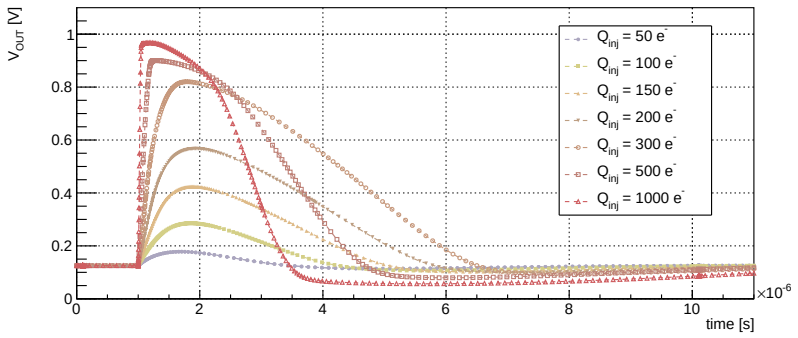


Figure 5.4.: Simulated response of the analogue front-end at nominal bias: the voltage at the *OUT* node is presented as a function of time after a charge injection (at $t = 1\,\mu s$) at the sensing node. Data taken from [83].

case of very large collected charges, a *clipping transistor* (M5) is introduced, that in DC operation functions as a reversely biased diode. As the voltage at the *OUT* node exceeds the one at the *CURFEED* node by the threshold voltage of M5, however, M5 is forced into conduction, resulting in current flowing from *OUT* to *CURFEED* and consequently a faster restoration of the baseline.
The simulated response of the analogue front-end circuit is presented in Fig. 5.4, where the voltage at the *OUT* node is shown as a function of time after a charge injection (at $t = 1\,\mu s$) at the sensing node. The simulated rise time for the lower injected charges is about $1\,\mu s$, whereas it is largely reduced for $Q_{\text{inj}} \gtrsim 300\,e^-$. The effect of the clipping transistor M5 can be clearly observed for large injected charges Q_{inj} (i.e. $500\,e^-$ and $1000\,e^-$), where the pulse duration is more reduced for higher pulse amplitudes.

- *Pulse discrimination* - As can be seen in Fig. 5.3, the *OUT* node is further connected to the gate of transistor M9. During the time the pulse amplitude at the *OUT* node exceeds a certain critical voltage $V_{\text{c,M9}}$, as indicated in Fig. 5.5, M9, being an NMOS transistor, will be forced into conduction. Consequently, if the current through M9 surpasses I_{DB}, the node *PIX_OUT_B* will be driven low[5]. When the pulse at node *OUT* returns to the baseline and goes below $V_{\text{c,M9}}$, transistor M9 will stop conducting and the node *PIX_OUT_B* will be driven high again. As will be discussed in the next section, the *PIX_OUT_B* node is connected to the digital part of the front-end circuitry and used to set the state register for the hit.

Charge threshold In summary, the analogue front-end circuit is AC-sensitive to voltage drops at the sensing node, after which a pulse is shaped that is fed to a discrimination stage. A smaller pixel-input capacitance increases the voltage excursion at the sensing

[5] The *PIX_OUT_B* signal is hence active low.

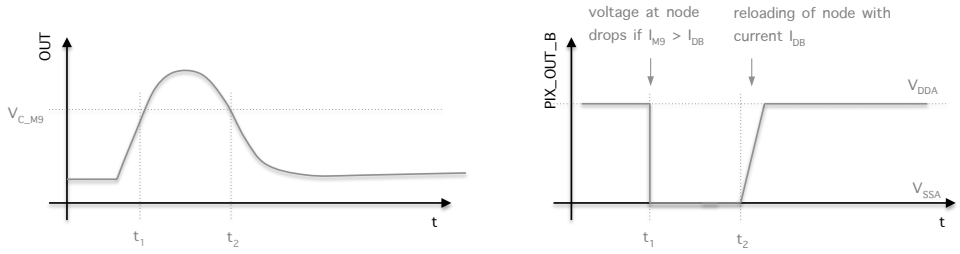


Figure 5.5.: Simplified response of the pALPIDE-1 analogue front-end. Left: analogue pulse; right: discriminated output.

node for a given collected charge, i.e. the charge-to-voltage conversion gain of the circuit (cf. Q/C ratio, Sec. 3.3), and subsequently leads to a larger pulse height within the front-end. Since the discrimination stage is based on a voltage comparison (cf. $V_{\mathrm{c,M9}}$ in Fig. 5.5), a smaller pixel-input capacitance reduces the charge threshold[6]. The threshold is further determined by a combination of I_{THR} and V_{CASN}, where in first approximation I_{THR} controls the pulse shape (i.e. relative height and width), and V_{CASN} determines the pulse baseline. Increasing I_{THR} leads to a reduced pulse height and width, whereas increasing V_{CASN} leads to an increased baseline voltage, bringing it closer to the critical voltage $V_{\mathrm{c,M9}}$ for driving the output node. Consequently, the charge threshold is increased by rising I_{THR}, while it is reduced by rising V_{CASN}. For large pulse amplitudes, the pulse duration is limited by the clipping mechanism, where the clipping effect is the larger, the larger the pulse height. The time resolution of the circuit is defined by the rise time, which is $\lesssim 1\,\mu\mathrm{s}$ by simulation. The shaping time is relatively long ($> 5\,\mu\mathrm{s}$) and therefore the front-end can be employed as an analogue memory.

Front-end biasing The bias to the pixels is provided by eleven on-chip 8 bit DACs placed in the chip periphery (six bias voltages and five bias currents). Their reference voltage is supplied externally by a dedicated pad ($V_{\mathrm{REF}} = 1.8\,\mathrm{V}$) positioned at the edge of the sensor[7]. The *nominal* DAC settings are presented in Tab. 5.2. The values are derived from device simulations and provide a first working point for the front-end circuit, however, they do not present the *optimum* DAC settings. These have to be obtained from a detailed characterization of the chip and may be different for future prototypes or the final design. The values presented in Tab. 5.2[8], including V_{BB} set to 0 V, will be further referred to as *nominal bias settings*.

[6] The charge threshold is here defined as the charge Q_{thr} that is required to be collected at the sensing node to produce a hit at the output of the front-end circuit with probability of 50 %.

[7] The output of the DACs can be monitored by two analogue monitoring pads. The same pads can also be used to override either one of the voltage DACs, one of the current DACs, or to override the internal reference current used by all current DACs.

[8] The reason to not have the nominal parameters at midscale between 0 and 255 is to increase the margin to larger values.

Table 5.2.: Nominal DAC values and related values as seen by the pixels [86]. Each DAC can be varied from 0 up to a value of 255.

DAC	nominal setting	nominal value
I_{BIAS}	64	20 nA
I_{THR}	51	0.5 nA
I_{DB}	64	10 nA
I_{RESET}	50	5 pA
V_{CASN}	57	400 mV
V_{CASP}	86	600 mV
V_{RESET}	117	1.2 V
V_{AUX}	117	1.2 V

Table 5.3.: Nominal V_{CASN} DAC settings used for different reverse substrate bias voltages.

V_{BB} [V]	V_{CASN} [DAC]	V_{CASN} [mV]
0.0	57	400.8
-3.0	135	949.2

Influence of reverse substrate bias on behaviour of front-end circuit It should be noted that the bulk terminal of the NMOS transistors M4, M7 and M9 is represented by the p-well, which is connected to the reverse substrate bias voltage V_{BB}. Changing V_{BB} therefore has a direct consequence on the characteristics of these transistors, most notably as a shift of the threshold voltage V_t. The effect on the operation of the front-end can be largely compensated by adjusting V_{CASN}, that is, V_{CASN} has to be increased for increased V_{BB}.

A rough calibration of the working point has been performed by increasing V_{CASN} until the fake-hit rate of the chip reaches a value similar to the one obtained for nominal bias settings. The values of V_{CASN} obtained for the different values of V_{BB}, further referred to as the respective *nominal* values, are presented in Tab. 5.3. Again, it should be noted that these values do not necessarily represent the optimum settings, as this has to be determined from a detailed characterization of the chip. Measurement results on the front-end response as a function of the bias settings are presented in Sec. 5.2.

Digital part

Fig. 5.6 presents the digital part of the pALPIDE-1 front-end circuit. It contains three registers: a *state register*, a *mask register* and a *pulse register*. Combinatorial gates allow

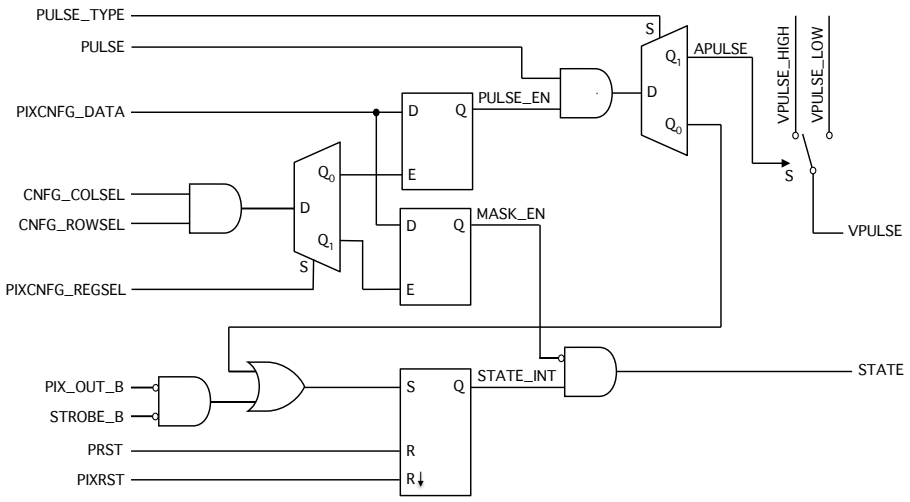


Figure 5.6.: Simplified schematic of the digital part of the pALPIDE-1 front-end.

these registers to be addressed and set from the digital periphery.

- **State register -** The *PIX_OUT_B* signal from the analogue front-end is put in coincidence with the *STROBE_B* signal provided by the digital periphery of the chip. If the *PIX_OUT_B* is driven low due to a hit detected by the sensor while the *STROBE_B* is asserted, the hit information will be stored in the state register. The state register can then either be reset by a *PIX_RST* pulse generated by the AERD or a global *PRST* pulse.

- **Mask register -** If the mask register is set, a one in the state register will not be propagated to the AERD. This allows the readout not to be loaded by malfunctioning or excessively noisy, i.e. so-called *hot* pixels.

- **Pulse register -** The pulse register enables the possibility to access each pixel for testing of the front-end response and the functionality of the state register. That is, if the pulse register is set to one, the test pulse (analogue or digital) will be propagated to the pixel. The tests can be performed by two different pulse modes, where in both cases the global *PULSE* signal, applied to the respective chip pad, steers the test pulse:

  – *Analogue pulsing* - The analogue pulsing allows the injection of a test charge Q_{inj} into the sensing node by the capacitance C_{inj}. The amplitude of the applied pulse and consequently the injected test charge Q_{inj} is defined by the difference between *VPULSE_HIGH* and *VPULSE_LOW*, both to be set on the respective DAC. It should be noted that both edges of the *PULSE* signal lead to charge

injections of different polarity, where the leading edge causes a discharge of the sensing node similar to a traversing particle.

– *Digital pulsing* - The digital pulsing allows to stimulate the state register, bypassing the analogue front-end and the *STROBE_B* signal. Subsequent to the assertion of the *PULSE* signal, the *STATE* signal must go high provided the state register is functioning properly and the pixel is not masked.

5.1.3. Sparsified readout

As discussed in the previous section, the output of the in-pixel front-end of each pixel is the digital *STATE* signal, which provides the information whether the pixel is hit or not. Since not each pixel output can be routed to the chip periphery, a suitable architecture for the readout of the matrix has to be found. In case of low hit densities, a sparsified readout approach can offer a low readout time and power consumption.
In the ALPIDE design, the pixel matrix is read by 512 separate circuits called AERD, each integrated into a double column. Each AERD performs a sparsified readout of the related double column and provides the address of hit pixels.

Address-Encoder Reset-Decoder (AERD) The AERD is an asynchronous combinatorial circuit, consisting of a fast *OR* logic, a priority address encoder and a one-hot reset decoder [84, 45]. As input, an AERD takes the 1024 *STATE* signals of the pixels of the related double column and generates 10 bit addresses[9] of the hit pixels as follows: if at least one pixel is hit in the respective double column, the *VALID* signal, generated by the fast *OR* logic, is set high. The digital periphery subsequently asserts the *SELECT* signal, which is propagated through the reset decoder in the various layers[10] to the hit pixel with the lowest address (highest priority). The forward propagation of the *SELECT* signal activates the generation and backward propagation of the respective pixel address to the digital periphery. Once the digital periphery has read the address, the *SELECT* signal is deasserted and the pixel is reset. This procedure is iterated until all hit pixels connected to the AERD are read, that is, when the *VALID* signal is set low. It should be noted that in general no activity takes place in the circuitry if no hit is present, i.e. there is no free running clock present in the matrix.

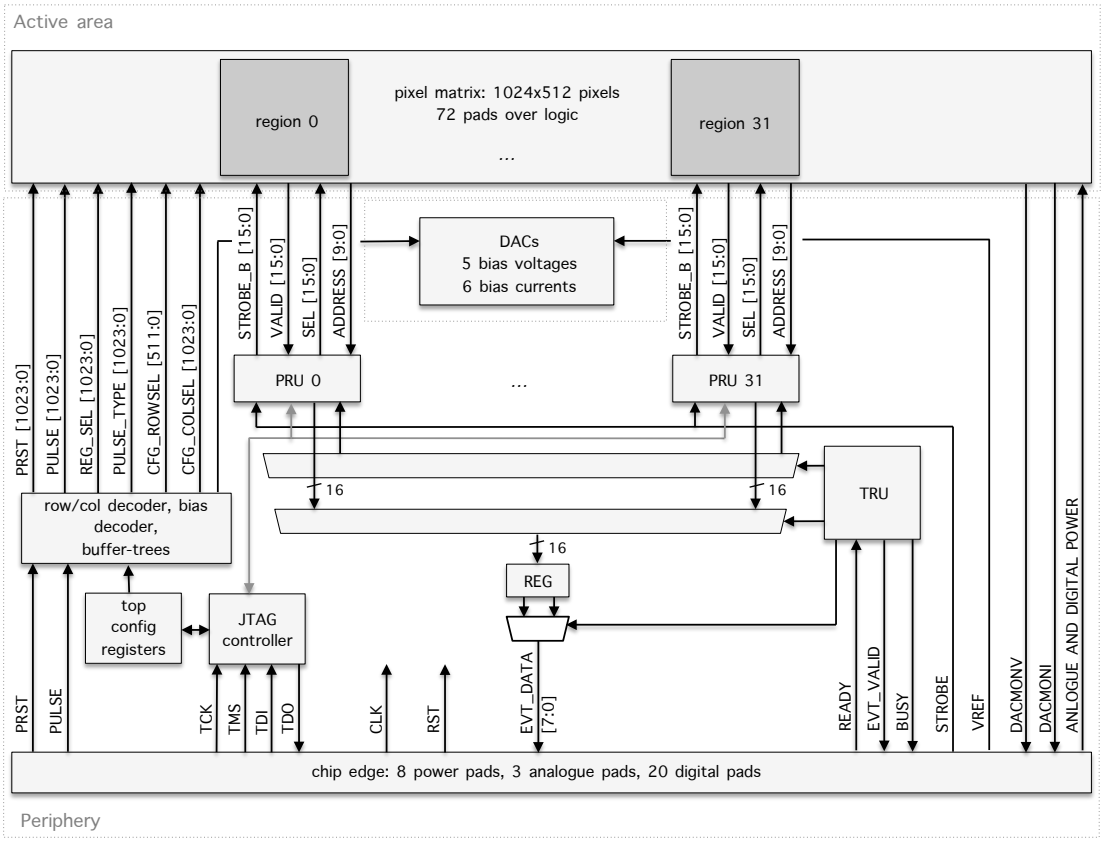


Figure 5.7.: Simplified block-diagram of the pALPIDE-1.

5.1.4. Chip periphery

As presented in Fig. 5.7, the periphery of the pALPIDE-1, located at the long edge of the sensor, can roughly be subdivided into the bias block and the digital periphery.
The digital periphery comprises the 32 RRUs and the TRU for the readout of the pixel matrix. Moreover, it contains a total of 64 memories, two per RRU[11], and 78 configuration and status registers. It communicates with the off-chip electronics through 20 CMOS pads. To the core side of the chip, it interfaces to the bias block and the pixel matrix. A JTAG interface is implemented to read or write registers and to access memories for test purposes.

Region Readout Units (RRU) Each RRU contains configuration registers, two memories (a 16×16 DPRAM and a 256×16 DPRAM as event-info buffers and multi-event data

[9] In the pALPIDE-1, the addresses are generated within four clock cycles.
[10] This allows for saving power as only the branch which leads to the respective pixel is activated.
[11] 32 16×16 and 32 256×16 DPRAM memories as event-info buffers and multi-event data buffers, respectively.

buffers, respectively) and the logic to steer the 16 double columns of a region, including the readout of the respective part of the pixel matrix. Generally, the readout sequence can be subdivided into two phases: the *integration phase* and the *readout phase*, where the former is defined by the time the *STROBE_B* is asserted. During the readout phase the state registers are read by the AERD circuits. The off-chip data transmission is immediately started after the completion of the data transfer from the matrix to the memory blocks in the RRUs.
In the pALPIDE-1, two different readout sequences are implemented:

- **Continuous integration mode -** In the continuous integration mode (readout mode A) the *STROBE_B* signal is kept continuously asserted until the arrival of an external *STROBE* pulse. After this, the *STROBE_B* is deasserted, causing the pixels to stop latching the discriminator outputs into the state register and the readout of the pixel matrix to be initiated. Once the matrix readout is completed, the integration phase is restarted by an automatic reassertion of *STROBE_B*[12].

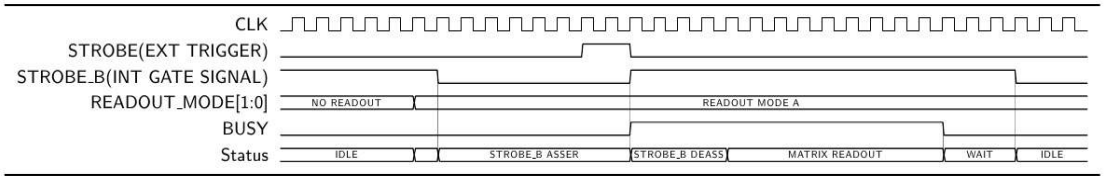


Figure 5.8.: Sequence of the continuous integration mode (readout mode A) [86].

  In this sequence, the pixels continuously integrate all discriminated hits during the assertion of *STROBE_B*, while the *STROBE* pulse effectively operates a start of the readout. Since the system is unable to process any other *STROBE* signals during the readout phase, the *BUSY* signal of the chip is set high.

- **Triggered integration mode -** Contrary to the continuous readout mode, in the triggered readout mode (readout mode B) the *STROBE_B* signal is initially deasserted. Only upon the arrival of an external *STROBE* pulse the *STROBE_B* signal is asserted for a fixed time, whereafter the readout of the pixel matrix is initiated[13].

  In this sequence, the *STROBE* pulse effectively operates as the start of a fixed-duration integration time. The *BUSY* is set high after receiving the *STROBE* pulse until the completion of the data transfer from the matrix to the memory blocks.

[12] Both the delay between deassertion of *STROBE_B* and start of the readout and completion of the readout and reassertion of *STROBE_B* are programmable.
[13] The duration of the *STROBE_B* signal and the delay between its deassertion and the start of the readout are programmable.

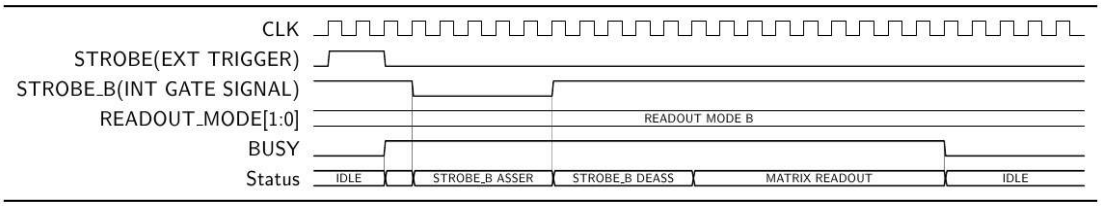


Figure 5.9.: Sequence of the continuous integration mode (readout mode B) [86].

Readout of the regions After the integration phase, a combinatorial *OR* of the 16 *VALID* signals provided by the AERDs is used to evaluate whether or not to read out the region. In case the *OR* is set, a priority encoder provides the address (4 bit) of the first double column containing a hit pixel. After all hit pixels of the double column are read, the priority encoder in the RRU generates the address of the next hit double column. This procedure is iterated until the combinatorial *OR* of the *VALID* signal goes low.
The readout scheme provides a unique identifier for the hits inside a region, since for each pixel address provided by a given AERD (i.e. double column), ther RRU priority encoder provides the related double column address. The pixel and double column address are combined into a 16 bit data word which is saved into the 256×16 memory, that is, the multi event buffer. Once the readout of the double columns is terminated, a header word of 16 bits is saved into the 16×16 memory, i.e. the event info buffer. This word contains the address of the RRU (5 bits) and the number of data words (event depth) that were written into the multi-event buffer during the preceding readout phase[14].

Top Readout Unit (TRU) When at least one header word is written into the multi-event buffers, i.e. when at least one RRU stores a complete event, the TRU is initiated to scan the 32 RRUs in sequence. From each RRU, the header word is read to extract the event depth, which is used to read the correct number of data words from the multi-event buffer. Subsequently, both the 16 bit header and the data words are separated into two bytes and sent off-chip through the 8 bit wide data port.

5.1.5. Considerations on the chip performance

In this section, the performance of the pALPIDE-1 regarding readout time, power consumption and dead time is discussed.

- **Matrix readout time -** Due to the sparsified readout scheme of the ALPIDE architecture, the total readout time depends on the hit density and the cluster

[14] The multi-event buffers also act as derandomizer, allowing to decouple the matrix readout phase from the data transmission off-chip.

size. Considering the expected maximum hit density of about 19 hits/cm^2/event [16] for a minimum bias Pb-Pb collision at mid-rapidity in the innermost layer, which corresponds to about 2.5 hits, or about 10 hit pixels (assuming 4-pixel clusters), per region and event, the average readout time of the matrix is about 1 µs.

- **Power consumption -** The overall power consumption of the pALPIDE-1 chip can be attributed to the in-pixel analogue front-end circuits, the AERD circuits and the digital periphery:

  – *In-pixel analogue front-ends* - The contribution of the analogue front-end circuit is independent of the hit density and dominated by the I_{BIAS} current, which by default is 20 nA per pixel. In total, for the 524288 pixels in the matrix, this results in an analogue current consumption of about 10.5 mA. Considering the supply voltage is 1.8 V, the total power consumption yields approximately 20 mW.

  – *AERD circuits* - The power consumption of the AERD depends on the average pixel hit density and the event trigger rate. Assuming the values previously presented for the hit density and cluster multiplicity and a trigger rate of 100 kHz, the total power consumption of all 512 AERD circuits is about 3 mW[15].

  – *Digital periphery* - The digital periphery represents the largest contribution to the total power consumption and is dominated by the internal consumption of the memory blocks and the switching of the clock tree [86]. For the pALPIDE-1, this contribution has been measured to be approximately 260 mW [87]. It should be noted however, that for the pALPIDE-1 no low-power techniques as disabling the memories or clock gating have yet been applied.

  Summarizing the contributions discussed above, the total power consumption of the chip is below 300 mW (70 mW/cm^2) and largely dominated by the digital periphery. The power consumption of this part, however, still has a large potential for optimization and will be addressed in future prototypes towards the final ALPIDE chip[16].

- **Data rates and dead time -** The working principle of the ALPIDE front-end circuit in the triggered readout mode can be summarized as presented in Fig. 5.10: within each pixel, the output of the analogue front-end is fed to the discrimination stage. Due to the relatively long pulse duration the front-end acts as an analogue

[15] The estimation of this value is based on simulations, from which the total energy used by an AERD circuit to read the address of single hit pixel yields 90 pJ [45].

[16] For the final ALPIDE the power consumption is foreseen to be less than 20 mW/cm^2 for the middle and outer layers, and about a factor two larger for the inner layers [68].

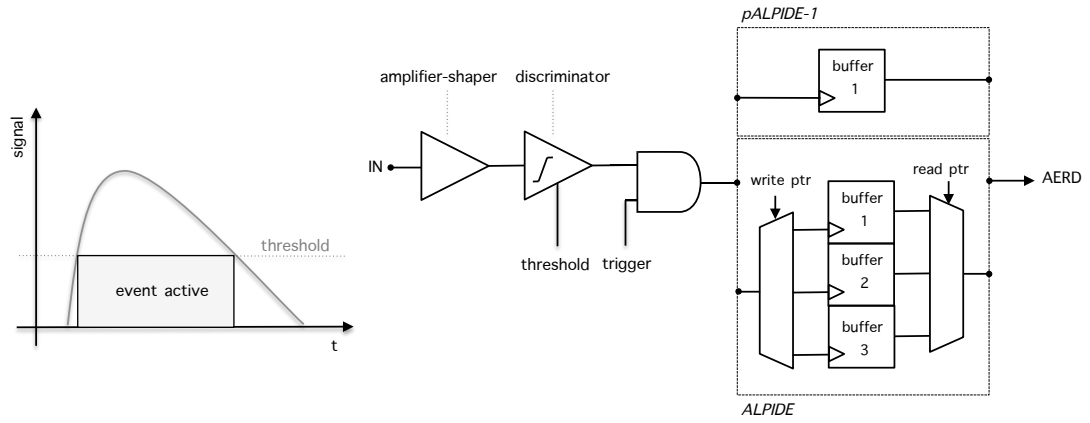


Figure 5.10.: Schematic representation of the working principle of the ALPIDE front-end.

memory. Each trigger signal (*STROBE*) opens an acquisition window for the recording of the discriminator outputs into the in-pixel hit buffers (state registers) and a subsequent readout of the matrix.

As previously discussed, the pALPIDE-1 prototype, containing only a single memory cell, is unable to process additional triggers while reading the matrix, hence potentially causing dead time. To reduce this, it is planned to include three in-pixel memory cells in the final ALPIDE chip. However, as indicated in Fig. 5.11, with such an arrangement physics events closer in time than the pulse duration in the analogue front-end may be recorded multiple times, possibly leading to a larger data rate[17]. In the continuous readout mode, the assertion of the trigger (*STROBE*) is asynchronous from the physics events with a programmable period. Similarly to the triggered mode, if physics events occur at the boundary of two acquisition windows, they will be recorded multiple times.

Consequently, the data rate is not only determined by the event-trigger rate, but also by the duration of the front-end output pulse. A pulse duration larger than the trigger signal delay, but smaller than the acquisition window (for continuous readout) or the average event interval (for triggered readout) is thus desirable.

To study the effects in detail, the ITS performance has been simulated under various running conditions using a SystemC model, for which the results are reported in [35]. The measurement results on the pulse duration for the pALPIDE-1 as a function of the front-end bias parameters and the collected charge are presented in Sec. 5.2.2.

[17] Moreover, if a pixel shows hits in consecutive events, it is difficult to distinguish whether a single hit was recorded several times or whether the pixel was hit several times. The probability for the latter is, however, expected to be neglibible.

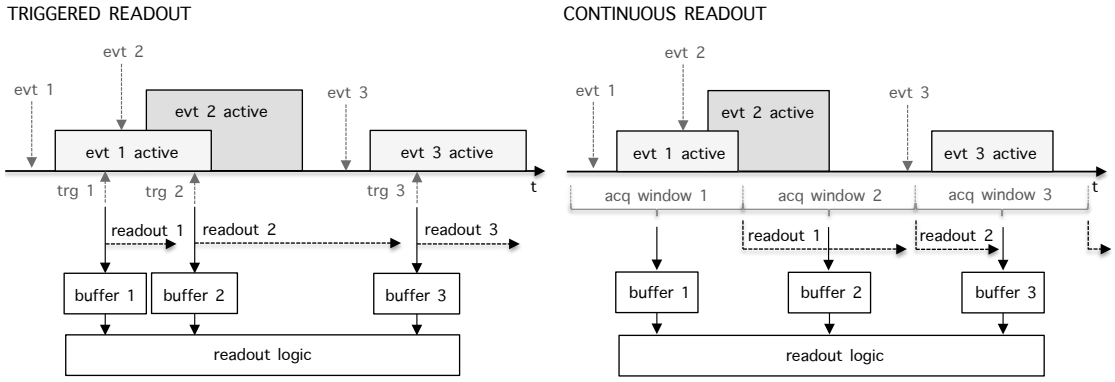


Figure 5.11.: Principle of the triggered readout mode (left) and continuous readout mode (right) in case of three in-pixel memory cells. Figure reproduced from [35].

5.2. Chip characterization

In a characterization campaign towards the beginning of 2015, the performance of the pALPIDE-1 has been assessed in view of the requirements on the pixel chip specified in Sec. 2.2.2. In this section, the results on the charge threshold, shaping time, fake-hit rate, detection efficiency and the position resolution will be presented and discussed.

5.2.1. Threshold, threshold RMS and temporal noise

The threshold has an important effect on most of the performance parameters of the sensor: a lower threshold will increase the detection efficiency, but also increase the fake-hit rate. Furthermore, an increased threshold results in a decreased cluster multiplicity, with a direct consequence on the position resolution.

As was introduced in the description of the analogue front-end circuit (Sec. 5.1.2), the charge threshold for pALPIDE-1 is mainly determined by the pixel-input capacitance C_p (i.e. the charge-to-voltage conversion gain) and the front-end bias parameters, that is, mainly I_{THR} and V_{CASN}. For a given bias setting it can be measured using the analogue pulsing. For this, a range of test charges Q_{inj}[18] is injected N times each into a selected pixel[19]. Subsequently, for each test charge the ratio between the number of times the

[18] The charge Q_{inj} injected by the capacitance C_{inj} depends on the amplitude of the voltage pulse, which in turn is defined by the difference between *VPULSE_HIGH* and *VPULSE_LOW*. Both voltages are generated by internal DACs on the chip, which provide a resolution of 256 steps over $V_{\mathrm{REF}} = 1.8\,\mathrm{V}$ and hence approximately 7 mV per step. Considering the fact that the injection capacitance C_{inj} by design is 160 aF, the calibration factor between the injected charge and one DAC step results in approximately $7\,e^-$/DAC step.

[19] In order not to overstress the pulsing circuit, only one pixel per region is pulsed at a time.

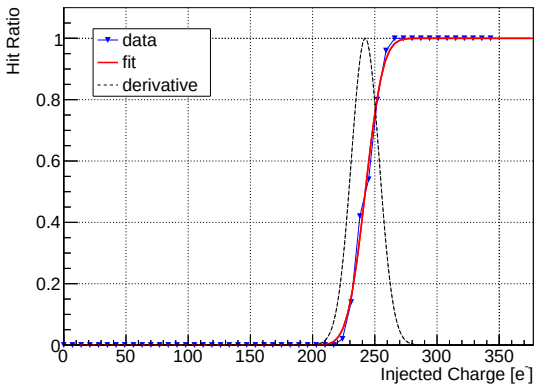


Figure 5.12.: S-curve measurement: hit ratio $r(Q_{\text{inj}})$ as a function of Q_{inj} for a pALPIDE-1 pixel at nominal bias settings and $V_{BB} = 0\,\text{V}$.

pixel has registered a hit, N_{hit}, and the total number of charge injections N is measured. The result is the response function $r(Q_{\text{inj}})$ of the front-end circuit:

$$Q_{\text{inj}} \rightarrow r(Q_{\text{inj}}) = \frac{N_{\text{hit}}(Q_{\text{inj}})}{N}. \tag{5.3}$$

For a functional pixel, only affected by Gaussian noise, $r(Q_{\text{inj}})$ is described by a shifted and scaled error function of the form

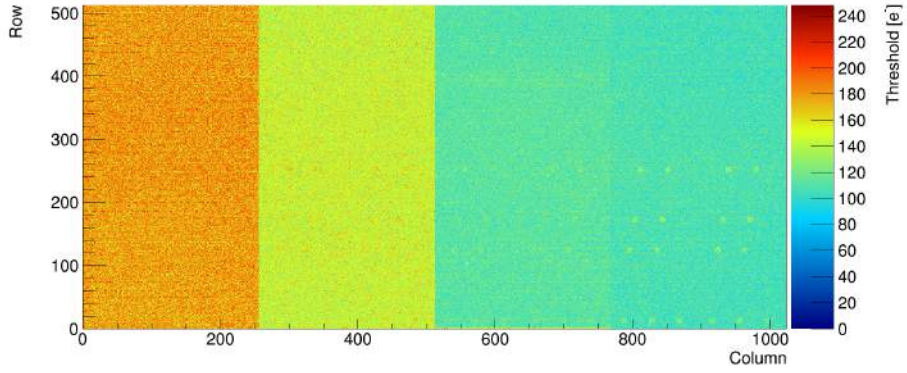
$$f(Q_{\text{inj}}) = \frac{1}{2}\left[1 + \text{erf}\left(\frac{Q_{\text{inj}} - Q_{\text{thr}}}{\sqrt{2}\sigma}\right)\right], \tag{5.4}$$

where Q_{thr} is the charge threshold, i.e. the charge value for which a pixel registers a hit with a probability of 50 %. The parameter σ describes the temporal noise[20]. Indeed, it is the standard deviation of the derivative of $f(Q_{\text{inj}})$, that is, a Gaussian function. Since there may be other noise sources (e.g. RTS noise) present, experimentally obtained response functions are more generally referred to as *s-curves*, due to their resemblance to the letter *S*.

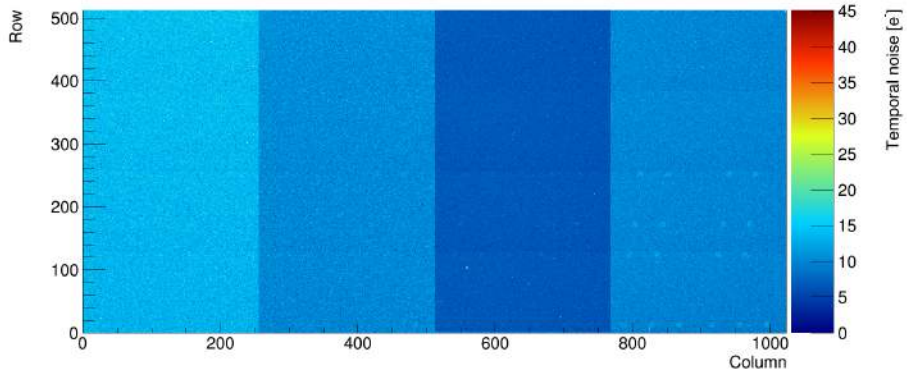
In the pALPIDE-1, the threshold measurement can be performed for each pixel of the matrix[21]. Fig. 5.13, shows the spatial distribution of the charge threshold (a) and the temporal noise (b) of a pALPIDE-1 for $V_{BB} = -3\,\text{V}$, $I_{\text{THR}} = 20\,\text{DAC}$ counts and nominal V_{CASN} for the respective V_{BB}. The four sectors containing the four different pixel types can be clearly distinguished. Within each sector, both the threshold and the temporal noise values can be observed to be evenly distributed, except for the pixels which are covered by the pads over the matrix, where the threshold and noise values are slightly

[20] The noise value obtained in such a way indeed the sum of both the fluctuations on the injected signal and the fluctuations on the threshold itself.

[21] Typically only a sample, e.g. of 1 % of the pixels, evenly distributed over the matrix, was measured.

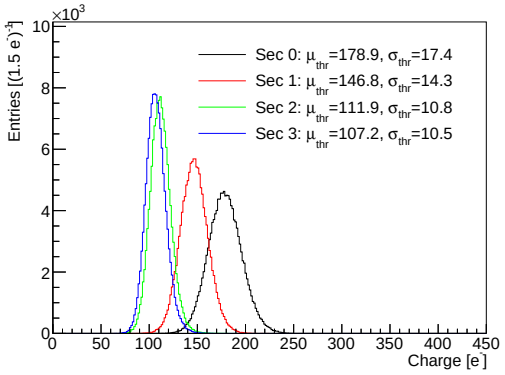


(a) Threshold map.

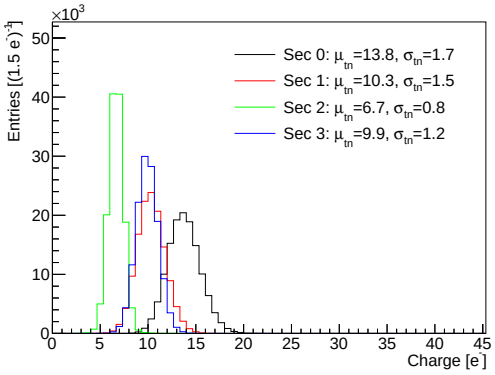


(b) Temporal noise map.

Figure 5.13.: Threshold (a) and temporal noise (b) map for a pALPIDE-1 at $V_{BB} = -3\,\mathrm{V}$, $I_{\mathrm{THR}} = 20\,\mathrm{DAC}$ counts, and nominal V_{CASN} for the respective reverse substrate bias.



(a) Threshold.



(b) Temporal noise.

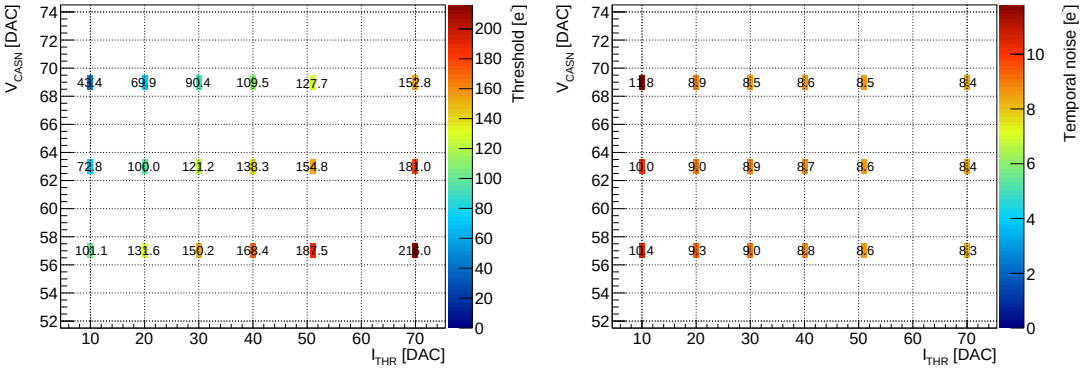
Figure 5.14.: Threshold and temporal noise distributions (including all pixels) for a pALPIDE-1 chip at the $V_{BB} = -3\,\mathrm{V}$, $I_{\mathrm{THR}} = 20\,\mathrm{DAC}$ counts, and nominal V_{CASN}.

increased (most prominently in sector 3). This effect, however, can most probably be explained by a change in the pulsing capacitance C_{inj} for these pixels [87].

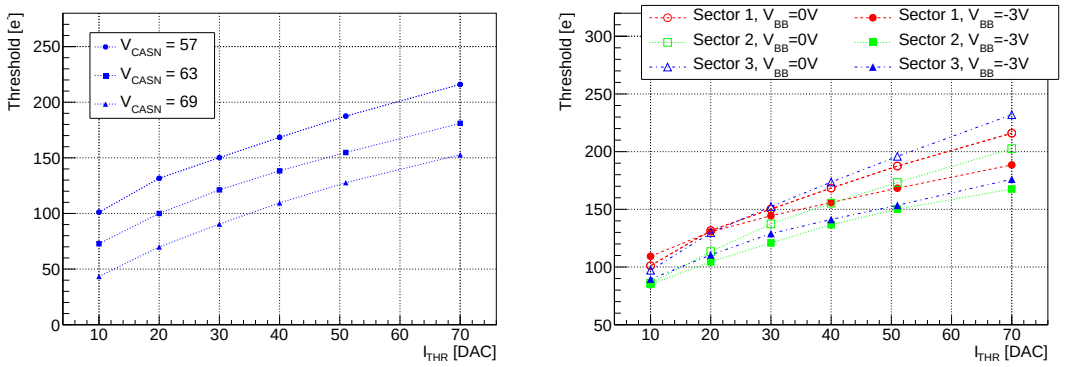
Threshold and temporal noise distributions Fig. 5.14, shows the pixel-to-pixel variations for the threshold and temporal noise, separately for each sector, and for two different reverse substrate bias voltages. Both threshold and temporal noise distributions resemble a Gaussian distribution. However, it should be noted at this point, that for most chips a few pixels can be found that do not exhibit a response function that is well described by Eq. (5.4). As will be discussed in Sec. 5.2.3, it are these pixels that dominate the fake-hit rate if not masked.
Comparing the threshold distributions for the pixels with PMOS reset (sectors 0, 1 and 3), a trend according to the spacing between the collection n-well and the surrounding p-well can be noticed, where pixels with an increased spacing exhibit a smaller threshold[22]. A possible explanation for this effect is that the pixel input capacitance C_p of the pixels with larger spacing is reduced more with increasing reverse substrate bias[23]. A smaller pixel-input capacitance leads to a larger charge-to-voltage conversion gain and consequently a lower charge threshold.
For $V_{BB} = -3\,\text{V}$, the diode-reset pixels of sector 2 show threshold values very similar to the PMOS-reset pixels the largest spacing (4 µm) of sector 3. The thresholds of the pixels of sector 2 are thus significantly lower compared to the PMOS-reset pixels with the exact same spacing (2 µm) of sector 1. A possible explanation for this effect is that the parasitic contribution to the pixel-input capacitance related to the reset mechanism is lower for the diode reset than for the PMOS reset[24]. Regarding the temporal noise distibutions in Fig. 5.14b, the diode-reset pixels of sector 2 show the lowest value. Between the PMOS-reset pixels, the lowest temporal noise is obtained for sector 3 with the largest spacing.

Influence of $\mathbf{I_{THR}}$ and $\mathbf{V_{CASN}}$ The threshold can be adjusted by varying the front-end bias parameters I_{THR} and V_{CASN}. Results for sector 1 as a function of both bias parameters for $V_{BB} = 0\,\text{V}$ are presented in Fig. 5.15a. The projection of the data along the V_{CASN}-axis is shown in Fig. 5.15c.
It can be observed that the threshold increases almost linearly with increasing I_{THR}. Furthermore, the threshold decreases with increasing V_{CASN}. It is therefore important to note that similar thresholds can be obtained with different combinations of I_{THR} and

[22] As presented in Tab. 5.1: sector 0: 1 µm spacing, sector 1: 2 µm spacing, sector 3: 4 µm spacing.
[23] That an increased spacing indeed allows a stronger reduction of the pixel-input capacitance as function of the reverse substrate bias was shown in Sec. 4.5.3.
[24] Indeed, this is expected [39].



(a) Threshold. **(b)** Temporal noise.



(c) Threshold as function of I_{THR}. **(d)** Thresholds for different sectors and V_{BB}.

Figure 5.15.: Mean threshold (a) and temporal noise (b) as function of I_{THR} and V_{CASN} for sector 1, and its projection along the axis of V_{CASN} (c) at $V_{BB} = 0\,\mathrm{V}$. Thresholds as function of I_{THR} for the different pixel types (sectors) of the pALPIDE-1 (d) for two values of V_{BB}, each at nominal V_{CASN}. The presented data is obtained from 1 % of the pixels of a single chip.

V_{CASN}[25]. When increasing the reverse substrate bias from 0 V to −3 V (cf. Fig. 5.15d), the slope of the treshold as function of I_{THR} is reduced.
Fig. 5.15b shows that the temporal noise is reduced with increasing I_{THR}, while it is almost uninfluenced by V_{CASN}.

Chip-to-chip variations The chip-to-chip variations of the threshold and temporal noise have been studied by comparing the data of in total 49 pALPIDE-1 chips. A summary of the results is presented in Tab. 5.4. As can be noted, the chip-to-chip fluctuation

[25] It should be kept in mind here that V_{CASN} determines the baseline voltage at the *OUT* node within the analogue front-end. If the baseline voltage at the *OUT* node, connected to the gate of transistor M9 (cf. Fig. 5.3), exceeds a certain critical voltage $V_{\mathrm{c,M9}}$ for which the current through M9 surpasses I_{DB}, the *PIX_OUT_B* node of the pixel is driven continuously low (active). This represents a limitation when trying to decrease the threshold by increasing V_{CASN}. Accordingly, also the pixel-to-pixel variations within the front-end (e.g. V_t-spread of M9) have to be considered.

is relatively large, with an RMS around 10 % and some chips differing by a up to 30 %. Possible sources for these variations have been studied, however, no conclusive explanation has yet been found. No systematic effects between wafers have been observed. Effects of the voltage DACs and injection capacitance related to analogue pulsing have been excluded [87]. Moreover, the varying thresholds have been observed to be reflected in the results for the detection efficiency [88].

Table 5.4.: Chip-to-chip variations of the threshold and temporal noise for nominal bias settings and $V_{BB} = 0\,\mathrm{V}$. The presented values have been calculated from the data of in total 49 pALPIDE-1 chips.

Sector	**Threshold**			**Temporal noise**		
	Mean [e^-]	RMS [e^-]	RMS [%]	Mean [e^-]	RMS [e^-]	RMS [%]
0	195.8	16.8	8.6	9.6	0.5	5.2
1	178.4	16.6	9.3	7.6	0.6	7.9
2	165.3	21.5	13.0	4.0	0.5	12.5
3	177.3	17.3	9.6	6.4	0.5	7.8

5.2.2. Shaping time

In the ALPIDE design the analogue pulse is employed as an analogue memory. In this context, the pulse duration can affect the data rate (cf. Sec. 5.1.5). It is hence of interest to characterize the shape of the pulse within the pALPIDE-1 front-end and the ways to control it.

The pALPIDE-1 solely consists of pixels with digital output. As such, only the information whether the amplitude of the pulse on the *OUT* node exceeds the voltage threshold ($V_{\mathrm{c,M9}}$) during the time the *STROBE_B* signal is asserted is accessable. That is, the circuit only allows to measure the *time-over-threshold* (ToT).
The measurements were performed as a sequence of threshold scans, where between each scan the delay between the charge injection and the assertion of *STROBE_B*, i.e. the *STROBE_B* window, was increased (cf. Fig 5.16). To minimize smearing effects, the *STROBE_B* duration was fixed to the shortest possible time, that is, 100 ns. To limit the measurement duration, only one pixel per region, i.e. eight pixels per sector, were measured. Fig. 5.17 presents an example result of a scan for a single pixel, where the hit ratio, i.e. $N_{\mathrm{hit}}(Q_{\mathrm{inj}})/N$, is shown as a function of the injected charge Q_{inj} and the *STROBE_B* delay. The area where the hit ratio is equal to one (red area) represents the region within which the pulse amplitude exceeds the threshold. Two characteristic points are indicated:

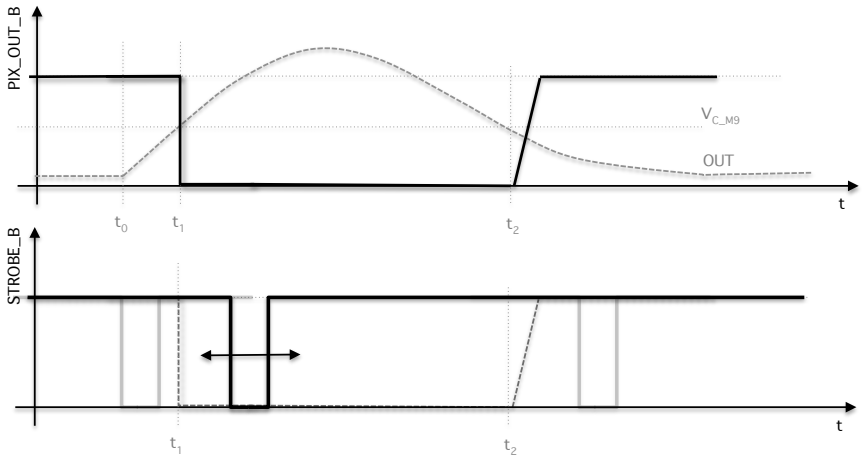


Figure 5.16.: Principle of pALPIDE-1 pulse duration measurement: an analogue pulse is applied at t_0, which leads to the creation of a voltage pulse at the *OUT* node. As long as the pulse amplitude exceeds a certain critical voltage $V_{c,M9}$, the digital output signal of the front-end *PIX_OUT_B* is driven low (active). In the digital front-end, this signal is then put in coincidence with the *STROBE_B* signal. When both are simultaneously active, a hit is registered. The time-over-threshold of the analogue pulse can thus be scanned by moving the *STROBE_B* active window with respect to the injection time. To avoid smearing effects, the *STROBE_B* duration must be set to a value much shorter than the pulse duration.

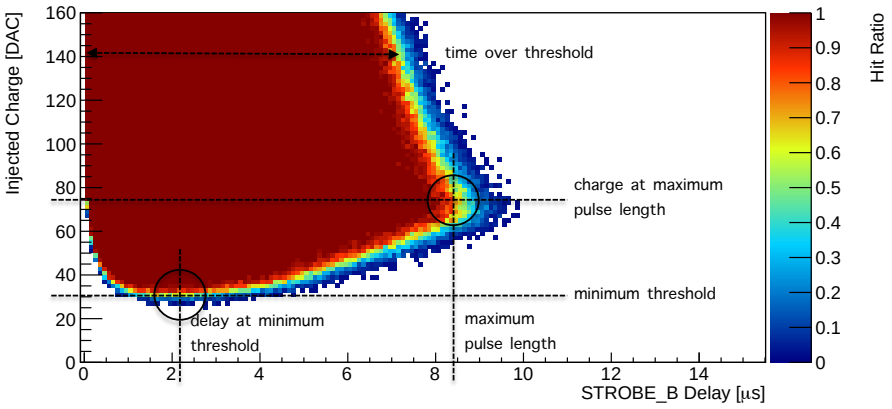


Figure 5.17.: Hit ratio as a function of Q_{inj} and the *STROBE_B* delay for a pALPIDE-1 pixel with PMOS reset at nominal bias settings and $V_{BB} = 0\,\text{V}$. The characteristic points of the *minimum threshold* and the *maximum pulse duration* are indicated.

- *Point of minimum threshold* - Fig. 5.17 shows that if the *STROBE_B* duration is set to values much shorter than the pulse duration, the measured charge threshold of the pALPIDE-1 is a function the *STROBE_B* delay. The point of minimum threshold is defined by the lowest value of injected charge $Q_{\text{THR,min}}$ for which the peak of the related analogue pulse exceeds the voltage threshold ($V_{c,M9}$). For the case presented in Fig. 5.17, this occurs at $Q_{\text{inj}} \approx 210\,e^-$ (30 DAC counts), for which

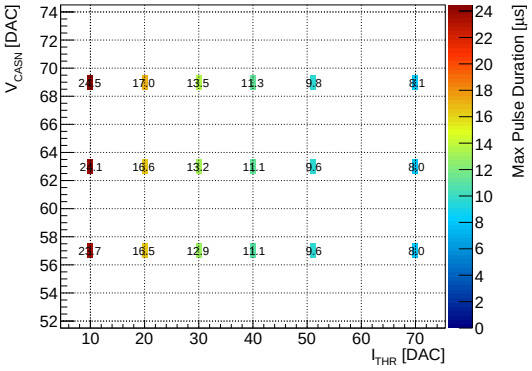
the peak position of the pulse $t_{\mathrm{THR,min}}$ is observed at about 2.2 µs. In order to obtain the most sensitive operation of the front-end, the active window of the *STROBE_B* signal must include this value. The peaking time $t_{\mathrm{THR,min}}$ furthermore defines the time resolution of the pALPIDE-1.

- *Point of maximum pulse duration* - For injected charges larger than $Q_{\mathrm{THR,min}}$, the ToT can be observed to increase - both due to a faster rise time[26] and a longer duration of the pulse. It can thereby be noted that the pulse duration τ_{p} increases almost linearly with increasing Q_{inj} up to a point where it reaches a maximum $\tau_{\mathrm{p,max}}$. For the presented case, this point is found at about 8.5 µs at $Q_{\mathrm{inj}} \approx 75\,\mathrm{DAC}$ counts $\approx 525\,e^-$. After the maximum, the ToT decreases with increasing injected charge - an effect that can be attributed to the clipping mechanism within the analogue front-end (cf. Fig. 5.3, transistor M5 and related text). The measuring range in terms of injected charge is limited by the related DACs to $Q_{\mathrm{inj}} \approx 1120\,e^-$, which is close to the MPV charge created by a MIP traversing a sensitive layer of 18 µm thickness.

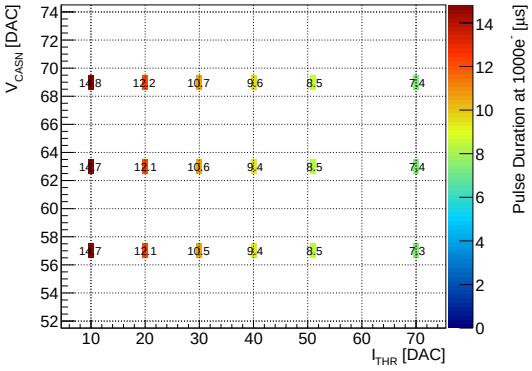
In addition to the two characteristic points, the time-over-threshold can be obtained as a function of the injected charge (cf. Fig. 5.17).

Influence of $\mathbf{I_{THR}}$ and $\mathbf{V_{CASN}}$ The shape of the analogue pulse at the *OUT* node is expected to be mainly influenced by I_{THR} (cf. Sec. 5.1.2). This is reflected in Fig. 5.18a, which shows the maximum pulse duration $\tau_{\mathrm{p,max}}$ as a function of I_{THR} and V_{CASN} for sector 1 of the pALPIDE-1 at $V_{BB} = 0\,\mathrm{V}$: $\tau_{\mathrm{p,max}}$ can be observed to be almost independent of V_{CASN}, while being a strong function of I_{THR}, e.g. for $I_{\mathrm{THR}} = 10\,\mathrm{DAC}$ counts the maximum pulse duration is about 24 µs, while it is reduced to about 8 µs at $I_{\mathrm{THR}} = 70\,\mathrm{DAC}$ counts. For reference, Fig. 5.18b presents the pulse duration at an injected charge of $1000\,e^-$, $\tau_{\mathrm{p},1000\,e^-}$, which is significantly shorter than $\tau_{\mathrm{p,max}}$ at low values of I_{THR}. Reconsidering the charge threshold values as a function of I_{THR} and V_{CASN} and relating them to the results obtained for the pulse durations, it can be noted that towards larger values of I_{THR} and V_{CASN} the pulse duration can be significantly reduced while maintaining a constant charge threshold.
Fig. 5.18c and Fig. 5.18d present the delay at minimum threshold $t_{\mathrm{THR,min}}$ (i.e. the time resolution of the circuit), and the injected charge $Q_{\mathrm{p,max}}$ for which the maximum pulse duration is observed (i.e. the clipping point), respectively. As the pulse duration, the delay at minimum threshold is decreasing as a function of I_{THR} and almost independent of V_{CASN}. It is about 3.1 µs for $I_{\mathrm{THR}} = 20\,\mathrm{DAC}$ counts and can be reduced to 1.8 µs when increasing I_{THR} to 70 DAC counts.
The charge at which the clipping mechanism starts acting shows a very similar behaviour

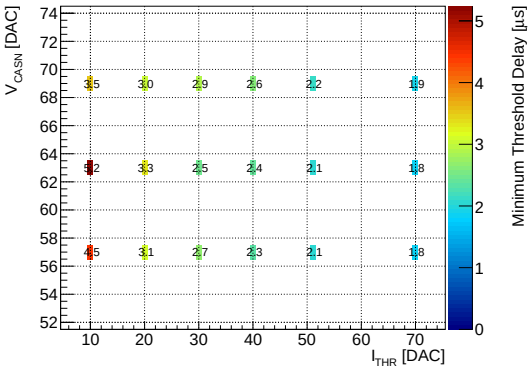
[26] The phenomenon that the time at which the pulse crosses the threshold depends on the pulse height is also referred to as *time walk* [33].



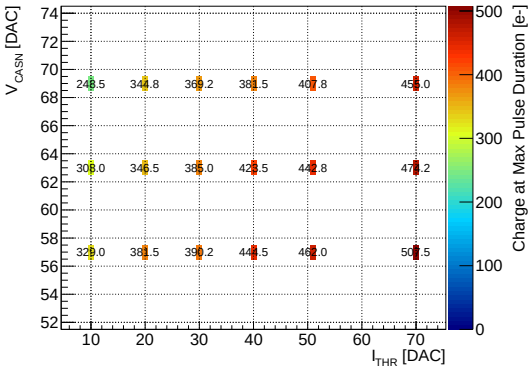
(a) Maximum pulse duration.



(b) Pulse duration at $Q_{\mathrm{inj}} = 1000\,e^-$.



(c) Delay at minimum threshold.



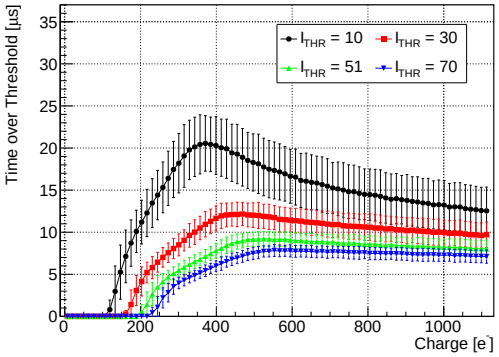
(d) Q_{inj} at maximum pulse duration.

Figure 5.18.: Mean values for maximum pulse duration $\tau_{\mathrm{p,max}}$ (a), pulse duration $\tau_{\mathrm{p},1000\,e^-}$ for $Q_{\mathrm{inj}} = 1000\,e^-$ (b), delay at minimum threshold $t_{\mathrm{THR,min}}$ (c) and injected charge at maximum pulse duration $Q_{\mathrm{p,max}}$ (d) as a function of I_{THR} and V_{CASN}. The data presented are for sector 1 of pALPIDE-1 at $V_{BB} = 0\,\mathrm{V}$.

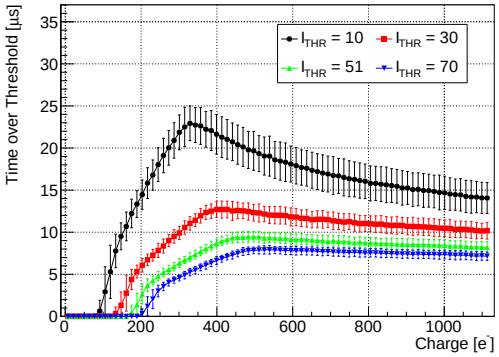
to the charge threshold as function of I_{THR} and V_{CASN}. This observation can be explained by the fact that, as the discrimination stage, the clipping mechanism is based on a voltage threshold.

Influence of reset mechanism and collection electrode geometry The influence of the reset mechanism and collection electrode geometry can be inferred from a study of the four different pixel types of the pALPIDE-1. As an example, the results for the time-over-threshold as a function of the injected charge for $V_{BB} = 0\,\mathrm{V}$ are presented in Fig. 5.19. Regarding the PMOS-reset pixels (i.e. sectors 0, 1 and 3), a very similar behaviour of the curves can be noted, where due to the clipping mechanism the pulse duration is significantly decreased after reaching its maximum. However the pixel types each exhibit different pulse durations and clipping points, i.e. charge at maximum pulse length.

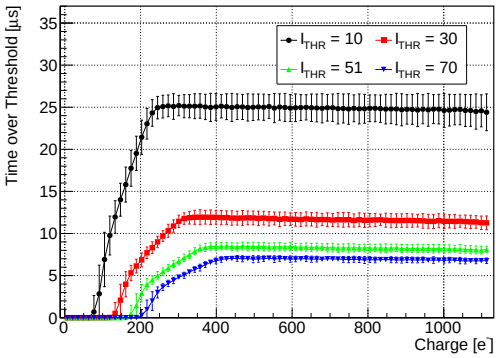
In a first approximation, the analogue pulse height and therefore the clipping mechan-



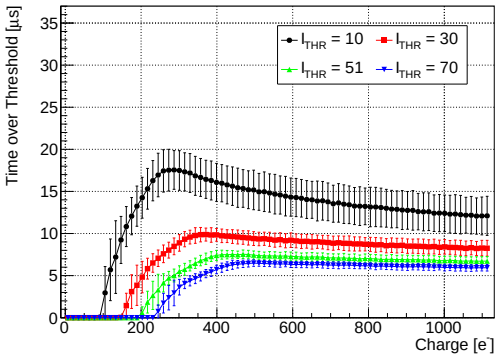
(a) Sector 0: 1 µm spacing, PMOS reset.



(b) Sector 1: 2 µm spacing, PMOS reset.

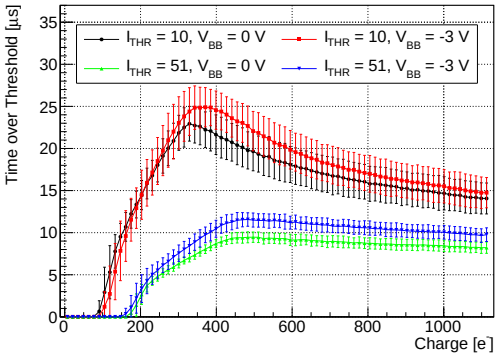


(c) Sector 2: 2 µm spacing, diode reset.

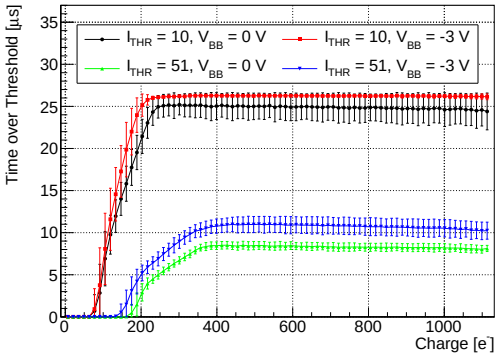


(d) Sector 3: 4 µm spacing, PMOS reset.

Figure 5.19.: Average time-over-threshold as function of the injected charge Q_{inj} for the different pixel types of pALPIDE-1 at various I_{THR}, $V_{BB} = 0\,\mathrm{V}$ and nominal V_{CASN}.



(a) Sector 1: 1 µm spacing, PMOS reset.



(b) Sector 2: 2 µm spacing, diode reset.

Figure 5.20.: Average time-over-threshold as function of the injected charge Q_{inj} for the different pixel types of pALPIDE-1 at various I_{THR} and V_{BB}, each at nominal V_{CASN}.

ism can be assumed to be solely determined by the voltage drop at the sensing node, i.e. the ratio of the collected charge Q_{col} and the pixel-input capacitance C_p (cf. Q/C ratio, Sec. 3.3). Consequently, as the reduced pixel-input capacitance C_p involved with larger spacing (cf. Sec. 4.5.3) leads to a larger pulse height, the clipping threshold voltage is reached at lower collected charge. This explains the observation that the pixels of sector 3 with the largest spacing (4 µm) show the lowest charge at maximum pulse length.
However, following this assumption, it also has to be expected that the pulse duration at the clipping point is independent on the pixel-input capacitance. It therefore cannot explain the observation that sector 3 with 4 µm spacing shows a significantly shorter pulse duration than e.g. sector 1 with 2 µm spacing.
For this, a possible explanation is a mechanism related to the contribution to the pixel-input capacitance formed between the sensing node (i.e. gate terminal of the input transistor) and the source terminal of the input transistor, C_{gs}. In the absence of perturbations, this capacitance C_{gs} is almost uncharged since the potential difference between the source and the gate terminal V_{sg} is approximately zero (cf. *static behaviour* in Sec. 5.1.2). When subsequently the potential at the sensing node drops due to the collection of signal charge, V_{sg} will be instantaneously increased. Indeed, as V_{sg} is now non-zero, part of the collected charge will be stored in the capacitance C_{gs}. When, with a certain delay, the source terminal starts to follow the sensing node (cf. *dynamic behaviour* in Sec. 5.1.2), the charge stored in C_{gs} will be gradually restituted to the rest of the pixel-input capacitance, leading to an additional voltage drop at the sensing node that is the larger, the smaller the capacitance. The additional voltage drop, amplifies the pulse height within the front-end, which in turn enhances the clipping effect and results in a smaller pulse duration.

Compared to the PMOS-reset pixels, the diode-reset pixels of sector 2 (i.e. Fig. 5.19c) exhibit an almost constant pulse duration after reaching the maximum. The behaviour can be attributed to the fact that the forward biased diode employed for the reset of the sensing node potential itself exhibits a clipping effect, which is related to its conductance g_D (cf. Eq.5.2). Accordingly, the instantaneous reset current increases with increasing injected charge, effectively limiting the voltage excursion for large amounts of collected charge. The effect is not present for the PMOS reset, since in this case the maximum reset current is limited by the I_{RESET} DAC setting.

Influence of V_{BB} The influence of the reverse substrate bias voltage V_{BB} on the pulse shape can be observed in Fig. 5.20. It shows the ToT as a function of the injected charge for various values of V_{BB} and I_{THR}. It can be noted that varying V_{BB} does not affect the overall pulse shape. However, when increasing V_{BB} from 0 V to −3 V, for injected charges above the clipping point the pulse duration is increased by about 2 µs for the diode-reset pixels and by about 1 µs for the PMOS-reset pixels. The exact reason for this effect is difficult to determine since an increase of V_{BB} not only leads to a decrease of the

pixel-input capacitance, but also has an effect on the operation of the NMOS transistors within the front-end circuit.

Influence of I_{DB} Additionally to the previously discussed parameters, also I_{DB} has shown to have an influence on the pulse duration, as it is responsible for recharging the *PIX_OUT_B* node after a hit (cf. Fig. 5.5). Since this node gets totally discharged to V_{SSA} (except for few pulses that reach a peak height just at the threshold) the recharge time can be assumed to be a constant that is added to actual pulse duration. Indeed, it was measured that the pulse duration is decreased by about 0.5 µs when increasing I_{DB} by a factor three, independent of the other bias settings.

5.2.3. Fake-hit rate

As it can strongly affect the tracking performance and output data rate of a tracking device, the fake-hit rate, i.e. the rate at which pixels show a hit in the absence of ionizing particles, is an important figure of a pixel chip. As presented in Tab. 2.2, the ALICE ITS upgrade requires a value below 10^{-5}/event/pixel[27], which corresponds to about five fake-hits per event per chip. The fake-hit rate increases for larger integration time, as this increases the probability to register a typically randomly occurring (fake) hit. In this context, for the pALPIDE-1 the fake-hit rate has been observed to increase as function of the *STROBE_B* width [45].

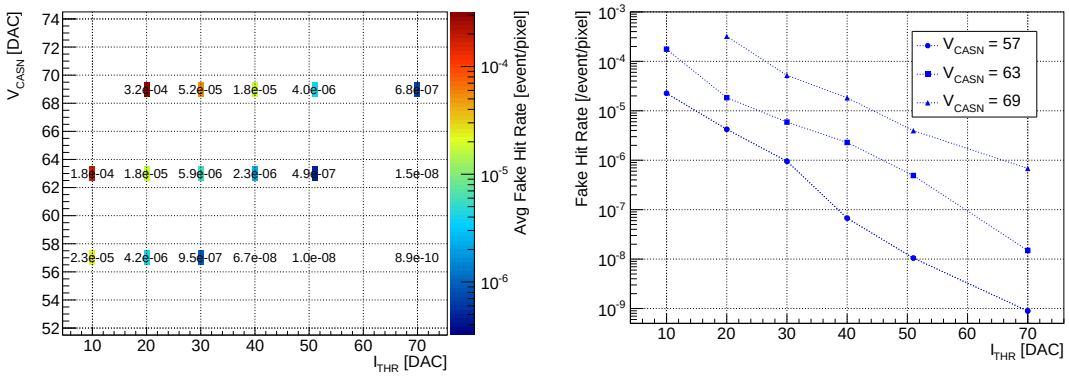
For the fake-hit rate measurement, a number of N random triggers is sent to the chip in absence of radiation. Subesequently, the resulting total number of hit pixels N^i_{fh} in each sector i is counted. The average fake-hit rate R^i_{fh} is then obtained according to

$$R^i_{fh} = \frac{N^i_{fh}}{N^i_{\mathrm{pix}} N}, \tag{5.5}$$

where N^i_{pix} is the number of pixels in a sector i (i.e. 256×512).
Since the R^i_{fh} is expected to be strongly influenced by the threshold, and moreover the threshold dispersion and temporal noise, the fake-hit rate measurements were performed as a function of different parameters as I_{THR}, V_{CASN}, V_{BB} and temperature. For all results presented presented in the following the *STROBE_B* width was set to 500 ns.

Influence of I_{THR} and V_{CASN} Fig. 5.21a shows results for the fake-hit rate as function of I_{THR} and V_{CASN} for sector 1 of a single pALPIDE-1 chip, measured at $V_{BB} = 0\,\mathrm{V}$ and $T = 28\,^{\circ}\mathrm{C}$. Reconsidering these results in view of the threshold values as a function of

[27] This value is motivated by the data rate in the outer layers.



(a) R^i_{fh} as function of I_{THR} and V_{CASN}. **(b)** R^i_{fh} as function of I_{THR}.

Figure 5.21.: Average fake-hit rate R^i_{fh} for sector 1 of a single pALPIDE-1 chip as function of I_{THR} and V_{CASN} for $V_{BB} = 0\,\mathrm{V}$, and zero pixels masked (a) and its projection along the axis of V_{CASN} (b). All presented data was measured at 28 °C with the *STROBE_B* width set to 500 ns.

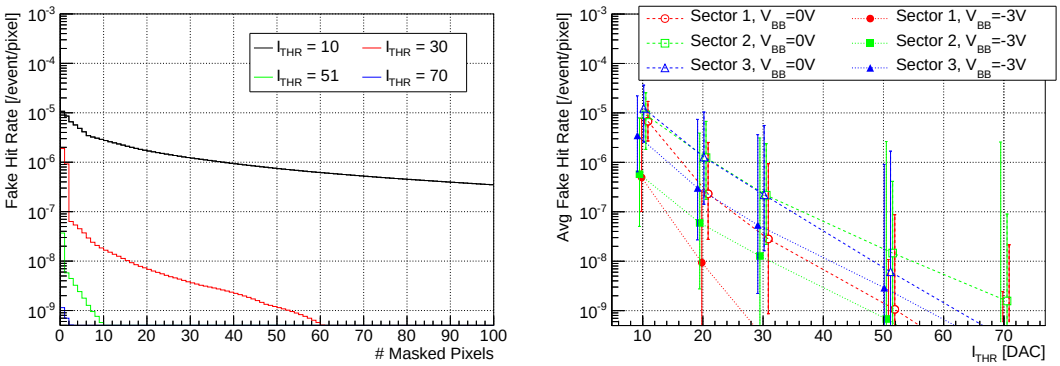
I_{THR} and V_{CASN} (cf. Fig. 5.15a) reveals a clear correlation, as combinations with similar charge threshold exhibit similar values for the fake-hit rate[28].

Masking pixels A more detailed analysis shows that the fake-hit rate is dominated by a few, so-called *hot* pixels, rather than by Gaussian noise. These pixels show a reproducable behaviour, producing fake hits with an increased, for each pixel characteristic probability. The behaviour can most probably explained by RTS noise in the input transistor, which also has been observed in the small-scale prototypes with analogue readout[29].
Masking the hot pixels allows to reduce the fake-hit rate of the pALPIDE-1 significantly. While the values presented in Fig. 5.21a are obtained without masking any pixel, it can be observed in Fig. 5.22a that by masking less than 100 pixels (which is less than 1 ‰ of the pixels in a sector), the fake-hit rate can be reduced by orders of magnitude, where this effect is more pronounced at larger thresholds.

Influence of reset mechanism, collection electrode geometry and V_{BB} Fig. 5.22b presents the fake-hit rate as a function of I_{THR} for two values of V_{BB} and three pixel types, which either differ by reset mechanism (sectors 1 and 2) or by spacing between the collection n-well and the surrounding p-well (sectors 1 and 3). The presented data points

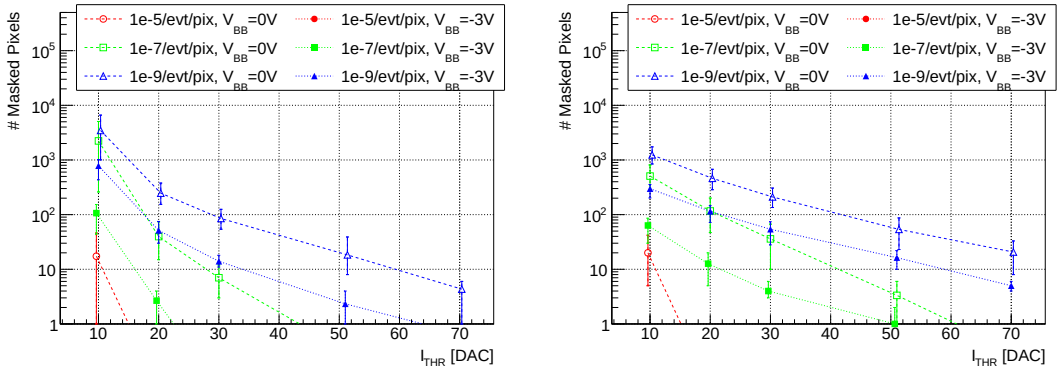
[28] As previously discussed, V_{CASN} influences the baseline at the *OUT* node, which is connected to the gate of the transistor controlling the output stage (cf. M9 in Fig. 5.3) and the signal *PIX_OUT_B*. Consequently, if V_{CASN} is increased in such a way that the *OUT* node exceeds a certain critical voltage $V_{\mathrm{c,M9}}$, all pixels outputs will be constantly activated (i.e. a fake-hit rate equal to one), leading to a non-functioning of the chip. E.g. for $V_{BB} = 0\,\mathrm{V}$, this limit for V_{CASN} is found around 70 DAC counts, corresponding to approximately 490 mV.

[29] This hypothesis has recently been substantiated by measurements on the pALPIDE-2, i.e. the successor of the pALPIDE-1, where in one sector the input transistor size was increased. For this sector, the fake hit rate was found to be reduced by about two orders of magnitude [87].



(a) R^i_{fh} as function of $N^{\text{masked}}_{\text{pix}}$. **(b)** R^i_{fh} as function of I_{THR}.

Figure 5.22.: Average fake-hit rate R^i_{fh} as function of the number of masked pixels $N^{\text{masked}}_{\text{pix}}$ for sector 1 of a single chip, measured at $V_{BB} = 0\,\text{V}$ and nominal V_{CASN} (a) and the average fake-hit rate as a function of I_{THR} for three different pixel types and various values of V_{BB}, each at nominal V_{CASN} (b). The data for the latter graph is averaged over three different pALPIDE-1 chips and after masking the 20 hottest pixels, where the error bars represent the average fake-hit rate obtained after either masking zero or the 100 hottest pixels. All presented data was measured at 28 °C with the *STROBE_B* width set to 500 ns.

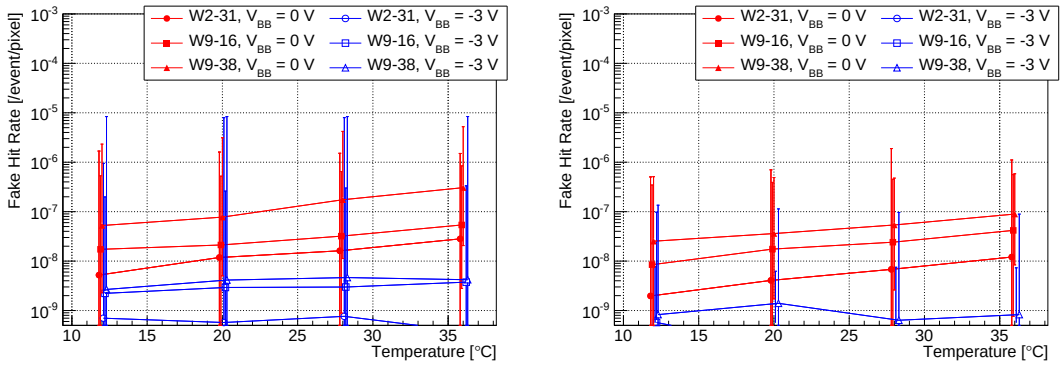


(a) Sector 1: 2 µm spacing, PMOS reset. **(b)** Sector 2: 2 µm spacing, diode reset.

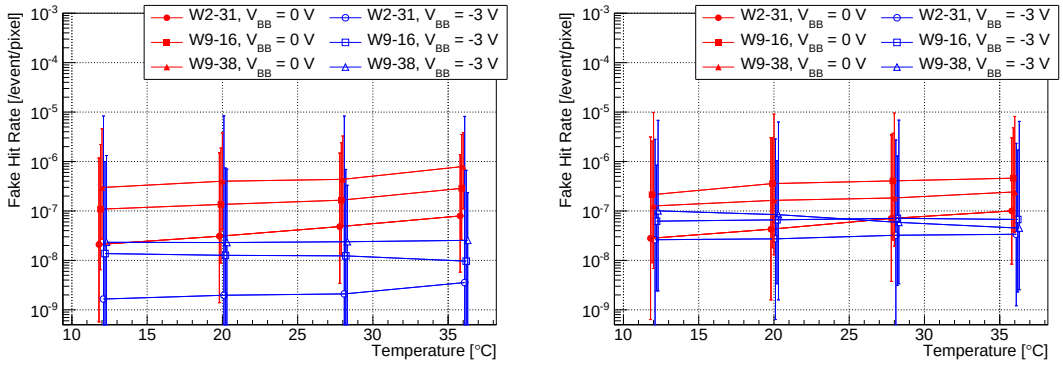
Figure 5.23.: Average number of pixels to be masked in order to obtain a certain fake-hit rate R^i_{fh} for various values of V_{BB}, each at nominal V_{CASN}. The data are averaged over three different pALPIDE-1 chips, where the error bars represent the minimum and maximum number of pixels to be masked between the chips to reach the respective R^i_{fh}. All presented data was measured at 28 °C with the *STROBE_B* width set to 500 ns.

are averaged over three chips and after masking the 20 hottest pixels, whereas the error bars represent the values after masking between zero and up to the 100 hottest pixels. Differences between the sectors can be observed, which are, however, not significant as equal fake-hit rates are attainable by masking a few more or less pixels.

An increase of V_{BB} from 0 V to −3 V can be observed to yield a reduction of the fake-hit rate. The benefit of applying a reverse substrate bias voltage can also be recognized in Fig. 5.23, showing the average number of pixels to be masked in order to obtain a certain



(a) Sector 0. **(b)** Sector 1.



(c) Sector 2. **(d)** Sector 3.

Figure 5.24.: Average fake-hit rate as a function of temperature for the four sectors of pALPIDE-1 at $I_{\mathrm{THR}} = 30\,\mathrm{DAC}$ counts for different chips and V_{BB} values at nominal V_{CASN} each. The presented data points are obtained by masking the 20 hottest pixels, whereas the error bars represent the values obtained when masking between zero up to the 100 hottest pixels. The *STROBE_B* width was set to 500 ns.

fake-hit rate[30], as a function of I_{THR} for sectors 1 and 2, at $V_{BB} = 0\,\mathrm{V}$ and nominal V_{CASN}. The number of pixels to be masked for $V_{BB} = -3\,\mathrm{V}$, compared to $V_{BB} = 0\,\mathrm{V}$, to reach a certain fake-hit rate is about a factor ten less. More generally it can be observed that the required fake-hit rate of 10^{-5}/event/pixel is obtained for all chips without masking any pixel for $I_{\mathrm{THR}} > 20\,\mathrm{DAC}$ counts, while a value of 10^{-9}/event/pixel is reached for all chips for $I_{\mathrm{THR}} \gtrsim 30\,\mathrm{DAC}$ counts and masking less than 2 ‰ of the pixels.

Influence of other parameters Fig. 5.24 presents a summary of the fake-hit rate results as a function of temperature for all four sectors of the pALPIDE-1, three different chips

[30] It should be reminded that a masking of pixels is only appropriate if they exhibit a reproducible behaviour, e.g. due to RTS noise. This is no longer guaranteed for $I_{\mathrm{THR}} \lesssim 20\,\mathrm{DAC}$ counts for nominal V_{CASN}. Furthermore, it is not reasonable to mask more than 1 % of the pixels, which for one sector of the pALPIDE-1 corresponds to approximately 1310 pixels, a number which is not reached in Fig. 5.23 for $I_{\mathrm{THR}} \gtrsim 20\,\mathrm{DAC}$ counts.

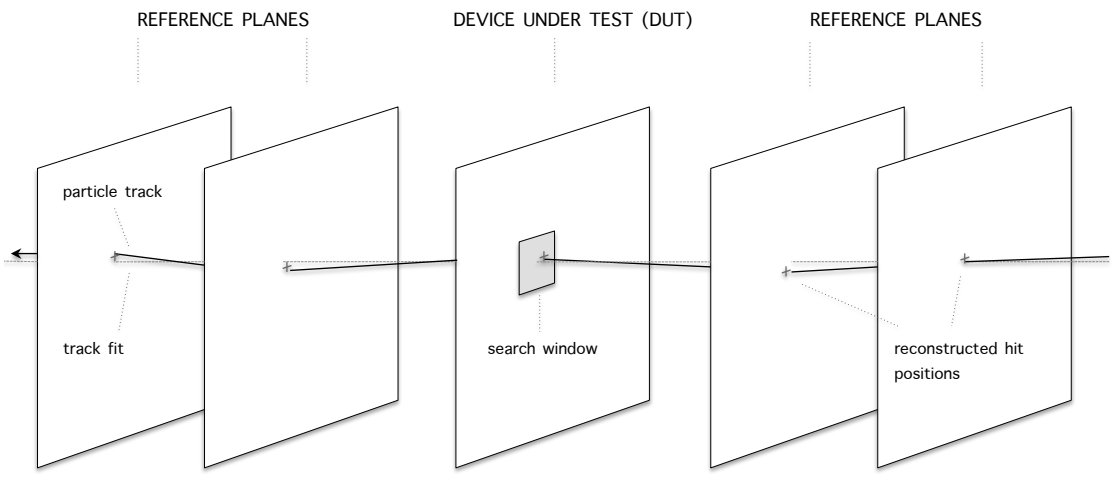


Figure 5.25.: Principle of a beam telescope and the particle track fitting.

and two V_{BB} values, measured at $I_{\mathrm{THR}} = 30\,\mathrm{DAC}$ counts and nominal V_{CASN}.
It can be noted that for $V_{BB} = 0\,\mathrm{V}$ an increase of temperature from 12 °C to 36 °C yields an increase of the fake-hit rate of about a factor ten, while for $V_{BB} = -3\,\mathrm{V}$ it stays almost constant. No significant difference is observed between the different pixel types for the temperature dependency of the fake-hit rate. The chip-to-chip variations are about a factor ten when masking the same number of pixels.
Comparing the observed trends with the results of the threshold measurements as presented in Appendix E.1, it can be noted that the temperature dependency of the fake-hit rate follows the temperature dependency of the threshold values, while trends of the threshold RMS and temporal noise are not reflected. This is consistent with the fact that the fake-hit rate is not dominated by Gaussian noise, but rather by a few pixels strongly affected by RTS noise.

5.2.4. Detection efficiency

The detection efficiency ϵ_{det} represents the probability of a sensor to detect traversing particles. It is determined by two effects: first, the charge collected in the seed pixel (and the related distribution) and hence by the sensor geometry, the reverse substrate bias and the particle type and energy, and second, the charge threshold. Consequently, lowering the threshold is beneficial for the detection efficiency, which is however limited by the involved increase of the fake-hit rate as discussed in the previous section. Hence, a trade-off has to be found.
The detection efficiency is measured using MIPs from a test beam facility and a so-called *beam telescope*, of which the principle is schematically shown in Fig. 5.25. A beam

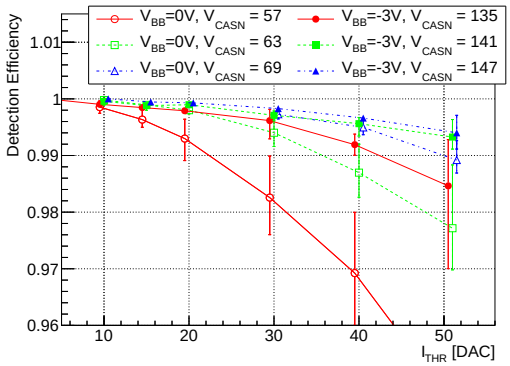
telescope is a particle tracking device, formed by several high-resolution position sensitive detectors, the so-called *reference planes*. The *device-under-test* (DUT) is typically placed in the center of the telescope.
The results on the detection efficiencies presented in the following have in most cases been obtained with a telescope of seven planes equipped with pALPIDE-1 chips, where the central three planes were treated as DUTs [88]. Indeed, in this case the distinction between reference planes and DUTs is only defined by the applied bias settings during the measurements (for the reference planes the settings are kept at fixed values, while for the DUTs they are varied) and the treatment during the analysis (only the hit information from the reference planes is considered for track fitting). The analysis of the data has been performed using the Eutelescope framework [31], using a broken-line fit that considers multiple-scattering effects in the all planes. Details on the optimization of the telescope configuration and data analysis are presented in [88].

Fig. 5.26 presents the results for the detection efficiency (left column) and average cluster multiplicity (right column) as a function of I_{THR} for sectors 1 (2 µm spacing, PMOS reset), 2 (2 µm spacing, diode reset), and 3 (4 µm spacing, PMOS reset), for two values of reverse substrate bias, measured with a 6 GeV pion beam from the CERN PS. For each reverse bias, the curves for three different values of V_{CASN} are presented, that is, the respective nominal values, and two larger values (yielding lower thresholds).

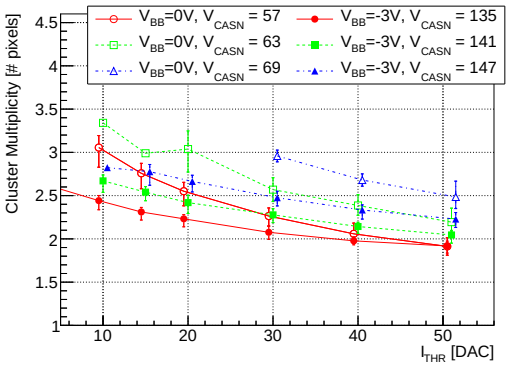
Influence of I_{THR} and V_{CASN} The dependency of the detection efficiency ϵ_{det} on the charge threshold can clearly be recognized, as it decreases for all curves with increasing I_{THR} and increases with increasing V_{CASN}. Since the front-end bias settings have no influence on the charge collection process, similar values of ϵ_{det} can be observed for different combinations of I_{THR} and V_{CASN}. Similar trends can be noticed for the average cluster multiplicity.

Influence of V_{BB} The reverse substrate bias voltage V_{BB} influences the extension of the depletion zone, with a direct effect on the junction capacitance C_d and the characteristics of the charge collection process (cf. Sec. 4.5.1). Therefore, an increase of V_{BB} has a direct, positive effect on the Q/C ratio of the sensor and consequently on the detection efficiency. The effect can be clearly observed in Fig. 5.26, where for all pixel types (sectors) and front-end bias combinations the detection efficiency is significantly larger when increasing V_{BB} from 0 V to −3 V, exceeding the required value of 99 % for almost all presented settings. The effects of an increased reverse bias is also reflected in the results for the average cluster multiplicity (cf. right column of Fig. 5.26). At small V_{BB} (e.g. $V_{BB} = 0$), the charge collection process is less efficient, enhancing charge sharing effects, thus allowing more pixels to collect signal charge. This also means, however, that in average each pixel

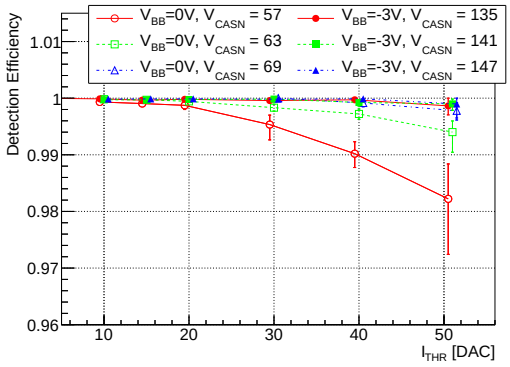
[31] `http://eutelescope.web.cern.ch`



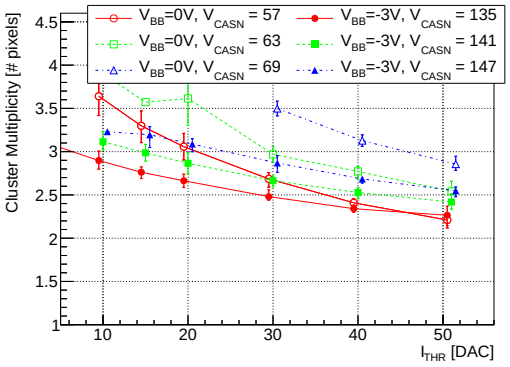
(a) Sector 1, detection efficiency.



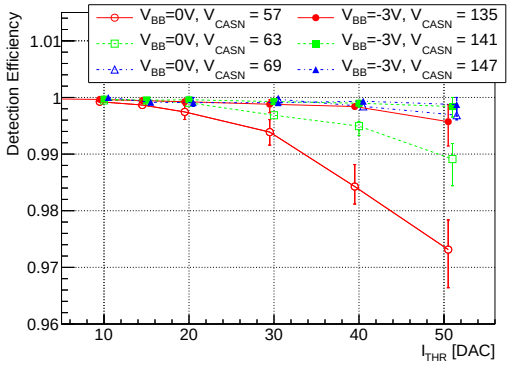
(b) Sector 1, average cluster multiplicity.



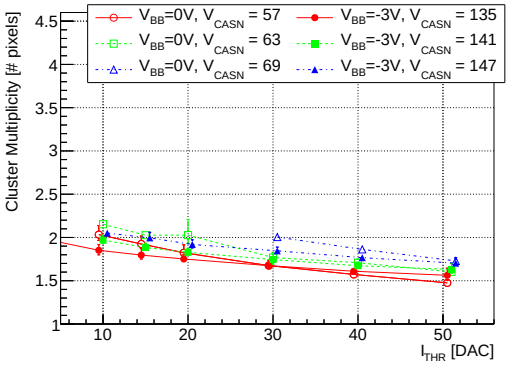
(c) Sector 2, detection efficiency.



(d) Sector 2, average cluster multiplicity.



(e) Sector 3, detection efficiency.



(f) Sector 3, average cluster multiplicity.

Figure 5.26.: Detection efficiency ϵ_{det} and average cluster multiplicity as a function of I_{THR}, averaged over three pALPIDE-1 chips, for different pixels types (sectors), reverse substrate bias voltages and values of V_{CASN}. All data was measured at the CERN PS with 6 GeV pions with the *STROBE_B* delay set to 2.2 µs. Data points taken from [88].

in a cluster collects less charge and, depending on the threshold, the probability for a single pixel to exceed the threshold and show a hit is decreased. At lower thresholds, the cluster multiplicity is therefore typically larger for low reverse bias, whereas at higher thresholds it can become larger for increased reverse bias, the exact behaviour depending on the pixel geometry.

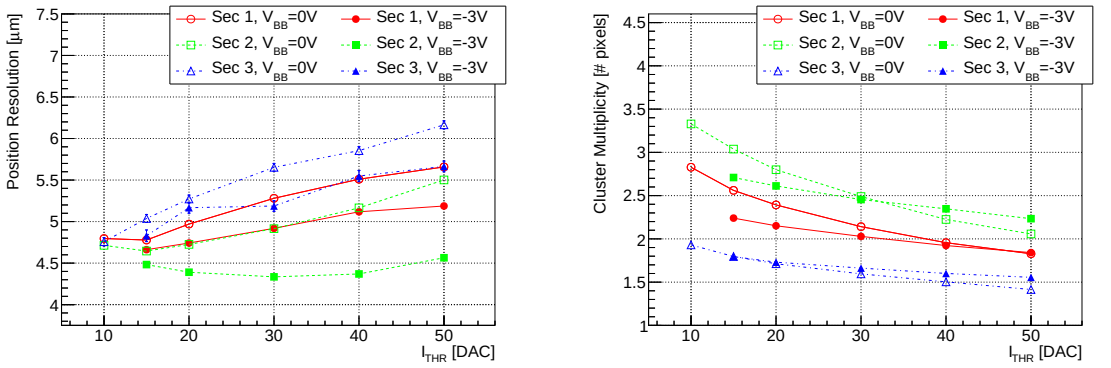
Indeed, at this point it should be reconsidered that the charge threshold itself is influenced by V_{BB} (cf. Fig. 5.15d)[32], as on the one hand the lower pixel-input capacitance related involved with increased V_{BB} leads to a reduced charge threshold, and on the other hand the operation of the NMOS transistors within the analogue front-end is altered. Hence, when interpreting the observed behaviour of the detection efficiency in Fig. 5.26, also the involved behaviour of the threshold has to be considered. While plotting the detection efficiency against the charge threshold would allow better insights into the physics processes, the presentation of the results as function of the front-end bias parameters reveals more information about the operational margin of the circuit.

Influence of reset mechanism The influence of the reset mechanism can be inferred from a comparison of sectors 1 and 2, featuring pixels with PMOS reset and diode reset, respectively, while having identical collection electrode geometry (i.e. collection n-well size and spacing between the collection n-well and the surrounding p-well). The depletion volumes and consequently the charge collection properties and junction capacitance C_d can therefore be assumed to be equal. What however differs is the parasitic contribution to the pixel-input capacitance C_p related to either PMOS or diode reset.
Regarding Figures 5.26a and 5.26c, it can be observed that for the same front-end bias settings, the diode-reset pixels show a significantly larger detection efficiency. This can be attributed to a lower pixel-input capacitance, which is expected for the diode reset [39]. The reduced capacitance involved with the diode reset is also reflected in the results for the average cluster multiplicity (cf. Figures 5.26b and 5.26d), which is generally larger for sector 2 (diode reset), while showing a very similar behaviour as function of the front-end biasing.

Influence of collection electrode geometry The influence of the collection electrode geometry can be inferred from a comparison of sectors 1 and 3[33], featuring pixels with

[32] In Fig. 5.15d, it was observed that for increased reverse substrate bias the threshold is less sensitive to changes in I_{THR} and typically lower for $V_{BB} = -3\,\mathrm{V}$ compared to $V_{BB} = 0\,\mathrm{V}$ at the respective nominal V_{CASN}. As was pointed out in the introduction of the analogue part of the front-end (cf. Sec. 5.1.2), the presented nominal values of V_{CASN} are not necessarily the optimum values. As V_{CASN} is one of the main control handles for the threshold, but also has to be readjusted when changing V_{BB}, an absolute comparison of the charge threshold for the different values of V_{BB} is difficult.

[33] The results for sector 0 (1 µm spacing, PMOS reset) are not presented here since in terms of detection efficiency it is strongly outperformed by the sectors with larger spacing, particularly at low reverse substrate bias.



(a) Position resolution.

(b) Average cluster multiplicity.

Figure 5.27.: Position resolution σ_{pos} and average cluster multiplicity as a function of I_{THR}, for different pixel types and reverse substrate bias, each at nominal V_{CASN}. All data was measured with a single pALPIDE-1 chip at the CERN PS with a 6 GeV pion beam. For all measurements at $V_{BB} = -3\,\text{V}$, V_{AUX} was adjusted from 117 DAC counts to 160 DAC counts. Data points taken from [88].

2 µm and 4 µm spacing, respectively, but equal reset mechanism (PMOS). In this case, the parasitic contribution to the pixel-input capacitance C_p related to reset mechanism can be assumed to be equal. By contrast, now the depletion volumes and consequently the charge collection properties and junction capacitance C_d differ, where the Q/C ratio is larger for the pixels with larger spacing (i.e. sector 3).
In Figures 5.26a and 5.26e, it can be observed that for the same settings of the front-end bias, the pixels with larger spacing show a significantly larger detection efficiency. The less pronounced charge sharing effects involved with increased spacing is also represented in the results for the average cluster multiplicity (cf. Figures 5.26b and 5.26f), which is significantly reduced for the pixels with larger spacing and also less sensitive to changes in threshold. This is the case despite the fact that the pixel-input capacitance is simultaneously reduced, which naturally leads to larger cluster multiplicities.

In summary, the pALIDE-1 shows excellent detection efficiencies for various parameter combinations. The performance can significantly be improved by increasing the reverse bias voltage on the collection diode. Furthermore, the results show that applying a diode reset and/or increasing the spacing between the collection n-well and the surrounding p-well are favourable[34].

5.2.5. Position resolution

As the detection efficiency, the *position resolution* of the DUT, i.e. the RMS deviation σ_{pos} of the reconstructed hit position from the real hit position, was measured using a beam telescope [88]. Indeed, the quantity directly accessible in such a measurement is the RMS deviation σ_{res} of the reconstructed hit position with respect to the extrapolated track crossing position, that is the *track residuals*. σ_{res} contains contributions from the position resolution of the DUT, but also the track resolution σ_{track} at the DUT. From the residual distribution, the position resolution of the DUT can be estimated by

$$\sigma_{\text{pos}}^2 = \sigma_{\text{res}}^2 - \sigma_{\text{track}}^2. \tag{5.6}$$

The track resolution σ_{track} at the DUT in turn depends on the intrinsic resolution of the telescope planes σ_i and the uncertainties involved with multiple scattering σ_{ms} (cf. Eq. 2.2). Details on the data analysis of the results discussed in this section, including the estimation of the track resolution σ_{track} of the used beam telescope, are presented [88].

The results obtained for the position resolution σ_{pos} for three different pixel types of the pALPIDE-1 (sectors 1, 2 and 3) and two different values of V_{BB}, each at nominal V_{CASN}, are presented in Fig. 5.27. It can generally be observed that the position resolution deteriorates with increasing I_{THR} as the average cluster multiplicity decreases (cf. Fig. 5.27b). Furthermore, it can be noticed that increasing the reverse substrate bias from 0 V to −3 V improves the position resolution, particularly at larger thresholds, despite the fact that the charge sharing effects are reduced.
Regarding the different pixel types, it can be clearly recognized that the pixels of sector 2 (diode reset, 2 µm spacing) show the best performance, exhibiting a position resolution of well below the required value of 5 µm at V_{BB} =−3 V for all presented values of I_{THR}. This can be attributed to an increased charge sharing effect obtained with 2 µm spacing and the reduced pixel-input capacitance involved with the diode reset.
The worst position resolution is observed for the pixels of sector 3 with the largest spacing (4 µm spacing) and PMOS reset. For this pixel type the depletion volume is larger and hence the charge sharing effects less pronounced. This leads to smaller average cluster multiplicities (cf. Fig. 5.27b) of between 1.5 and 2 (for nominal V_{CASN}), and a significant fraction of single pixel clusters. Nevertheless, the pixels of sector 3 reach a position resolution of about 5.5 µm for $V_{BB} = -3$ V and 6 µm for $V_{BB} = 0$ V at $I_{\text{THR}} = 51$ DAC counts. The results are thus significantly better than the value expected for a sensor with only single pixels responding to particle crossings (cf. Eq. 3.20), which is approximately 8 µm for a pixel pitch of 28 µm. The results can be furthermore expected to be improved by increasing V_{CASN}, i.e. lowering the charge threshold.

[34] These statements are based on data obtained with non-irradiated chips.

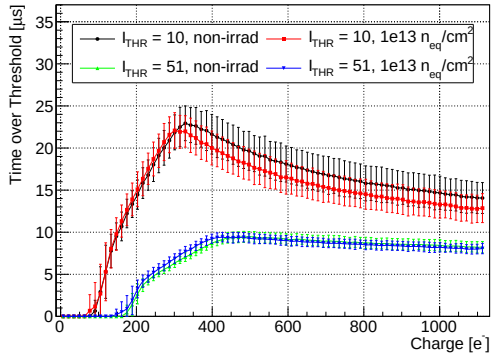
5.3. Post irradiation performance

In this section, studies on the effects of bulk damage on the chip performance parameters will be discussed. For this study, a sample of pALPIDE-1 chips was irradiated at the TRIGA MarkII Reactor at JSI in Ljubljana with neutron fluences of 1×10^{13} 1 MeV n_{eq}/cm^2. As has been shown in the previous chapter, bulk damage leads to a decreased charge collection efficiency, particularly if the (relative) depletion volume is small, and an increased leakage current in the collection diode. Both the depletion volume and the leakage current depend on the reverse substrate bias voltage V_{BB} (cf. Sec. 4.8).
Special attention also has to be paid to the input net and the operation of the reset mechanism. For the PMOS reset, it has to be ensured that the maximum reset current $I^{\max}_{\mathrm{RESET}}$ is sufficiently large to compensate the collection-diode leakage current (cf. Sec. 5.1.1)[35]. For the diode reset, the forward current will naturally increase with increased leakage currents at the input net. However, it also has to be considered that after irradiation the behaviour of the reset diode itself is influenced by the involved increase of the diode saturation current I_S (cf. Eq. (5.1)). Most prominently, this leads to a increase of the conductance and consequently a faster reset.

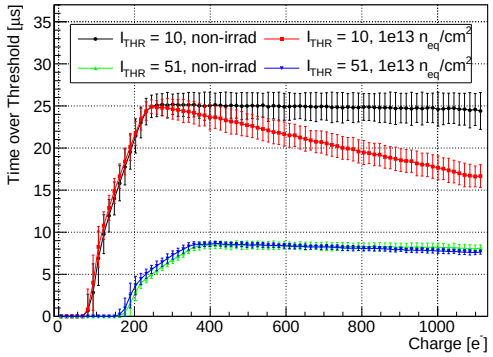
5.3.1. Shaping time

Fig. 5.28 presents the time-over-threshold (ToT) as a function of the injected charge for sector 1 (PMOS reset) and sector 2 (diode reset) before and after irradiation at two values of I_{THR} and V_{BB}, each at nominal V_{CASN}.
For the PMOS-reset pixels it can be observed that the pulse shape remains almost unchanged, the pulse duration only being slightly reduced for low values of I_{THR}. By contrast, significant effects can be observed for the diode-reset pixels. Whereas before irradiation the ToT was observed to be constant as function of the injected charge Q_{inj} after reaching its maximum, after irradiation the ToT decreases almost linearly with increasing Q_{inj}. Thereby the relative decrease of the ToT with respect to the maximum ToT is larger for smaller values of I_{THR}. Furthermore, the effect is more prominent (i.e. the slope increased) with increased reverse substrate bias.
Reconsidering the discussions in Sec. 5.2.2, the almost constant ToT after reaching its maximum was mainly attributed to the clipping effect inherent to the reset diode itself. This effect limits the voltage excursion at the sensing node for large amounts of collected charge. Accordingly, the behaviour after irradiation can be attributed to the same mechanism, however, with a decreased diode conductance and therefore an increased reset

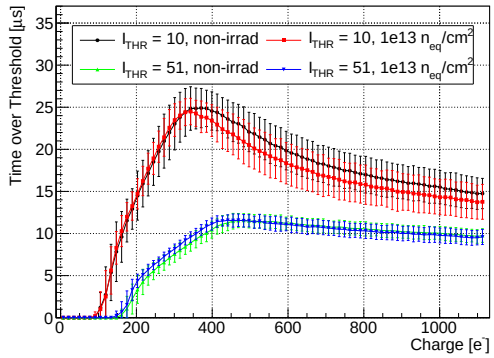
[35] The nominal maximum reset current of 5 pA (cf. Tab. 5.2), which represents a suitable value before irradiation, is therefore increased.



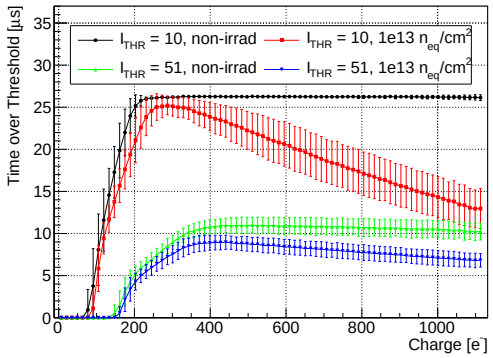
(a) $V_{BB} = 0\,\mathrm{V}$, Sector 1 (PMOS reset).



(b) $V_{BB} = 0\,\mathrm{V}$, Sector 2 (diode reset).



(c) $V_{BB} = -3\,\mathrm{V}$, Sector 1 (PMOS reset).



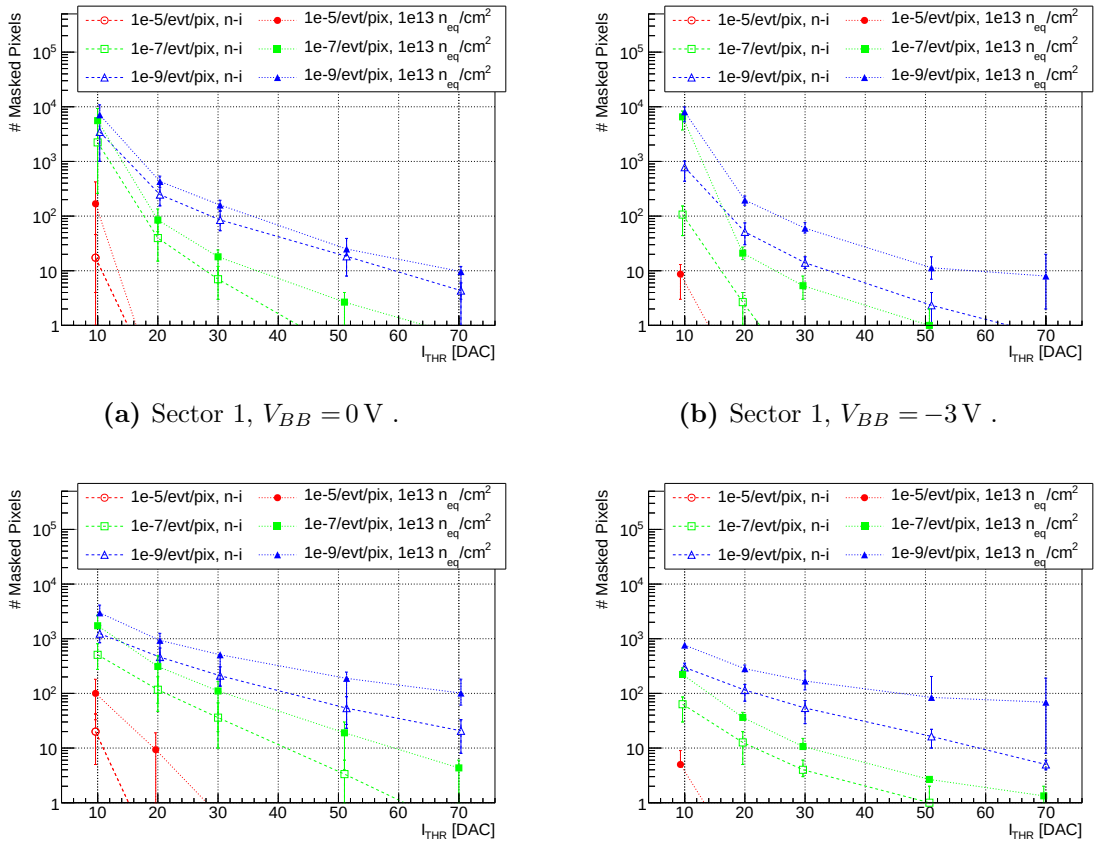
(d) $V_{BB} = -3\,\mathrm{V}$, Sector 2 (diode reset).

Figure 5.28.: Comparison of the ToT measured for non-irradiated chips and chips irradiated with a fluence of $1 \times 10^{13}\,1\,\mathrm{MeV\,n_{eq}/cm^2}$, for various I_{THR} and V_{BB}, at nominal V_{CASN}. It should be noted that for the irradiated chips at $V_{BB} = -3\,\mathrm{V}$ the changes of the working point due to increased leakage currents were compensated by adjusting V_{RESET} and V_{AUX} from 117 DAC counts to 125 DAC counts. The error bars represent the pixel to pixel variation.

current. In fact, the observed decrease of the pulse duration with increasing Q_{inj} after irradiation indicates that the dynamic reset current becomes sufficiently large to limit the voltage drop at the sensing node to values for which the clipping mechanism in the front-end circuit is not even activated.

5.3.2. Fake-hit rate

Despite the increased temporal noise (cf. Appendix E.2), also after irradiation with a neutron fluence of $1 \times 10^{13}\,1\,\mathrm{MeV\,n_{eq}/cm^2}$ the fake-hit rate can be observed to be dominated by a low fraction of the pixels. However, when masking the same number of pixels, the average fake-hit rate is increased by up to a factor ten.
Fig. 5.29 presents the average number of pixels to be masked in order to obtain a certain



(a) Sector 1, $V_{BB} = 0\,\mathrm{V}$.

(b) Sector 1, $V_{BB} = -3\,\mathrm{V}$.

(c) Sector 2, $V_{BB} = 0\,\mathrm{V}$.

(d) Sector 2, $V_{BB} = -3\,\mathrm{V}$.

Figure 5.29.: Average number of pixels to be masked in order to obtain a certain fake-hit rate R^i_{fh} as a function of I_{THR} before and after irradiation with a neutron fluence of $1 \times 10^{13}\,1\,\mathrm{MeV\,n_{eq}/cm^2}$ for sector 1 (2 µm spacing, PMOS reset) (a, b) and sector 2 (2 µm spacing, diode reset) (c, d) at various V_{BB} values, each at nominal V_{CASN}. The data is averaged over three different pALPIDE-1 chips, where the error bars represent the minimum and maximum values obtained between the chips. All presented data was measured at nominal V_{VCASN}, 28 °C and with the *STROBE_B* width set to 500 ns.

fake-hit rate R^i_{fh} as a function of I_{THR}, before and after irradiation, for sector 1 (PMOS reset) and sector 2 (diode reset) at various V_{BB} values and nominal V_{CASN}. Between the two reset types, no signifant difference in behaviour after irradiation can be observed, as the number of pixels that have to be masked for a certain fake-hit rate is in both cases increased by up to a factor ten. The required fake-hit rate of 10^{-5}/event/pixel can be obtained for all chips without masking any pixel for $I_{\mathrm{THR}} \gtrsim 30\,\mathrm{DAC}$ counts, while a value 10^{-9}/event/pixel can be reached for all chips for $I_{\mathrm{THR}} \gtrsim 30\,\mathrm{DAC}$ counts and masking about 5 ‰ of the pixels.

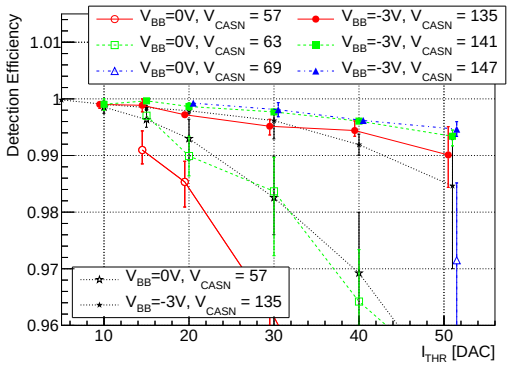
The chip-to-chip variations remain about a factor ten when masking the same number of pixels. The temperature behaviour of the fake-hit rate after irradiation, presented in Appendix E.2, shows no significant changes.

5.3.3. Detection efficiency

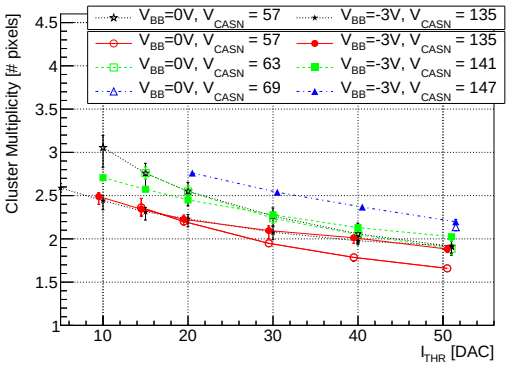
The chip performance in terms of detection efficiency before and after irradiation with a neutron fluence of $1 \times 10^{13}\,1\,\mathrm{MeV\,n_{eq}/cm^2}$ is shown in Fig. 5.30. Similarly to the data presented for the non-irradiated chips, it shows the detection efficiency (left column) and average cluster multiplicity (right column), averaged over three chips, as a function of I_{THR} for sectors 1 (2 µm spacing, PMOS reset), 2 (2 µm spacing, diode reset), and 3 (4 µm spacing, PMOS reset) for two values for reverse substrate bias V_{BB}. For each value of V_{BB}, the curves for three different values of V_{CASN} are presented.
Indeed, the detection efficiency is expected to be influenced on the one hand by a deteriorated charge collection effiency, and on the other hand by a change of behaviour of the circuit, including the pixel reset mechanism.
The effects related to the reset mechanism can be inferred from a comparison of sectors 1 and 2. For the PMOS-reset pixels (sector 1), at $V_{BB} = -3\,\mathrm{V}$, the detection efficiency, as well as the average cluster multiplicity remains unchanged. On the contrary, at $V_{BB} = 0\,\mathrm{V}$, the detection efficiency, and the average cluster multiplicity clearly drop. The results of the non-irradiated chips for nominal V_{CASN} can, however, be reproduced by increasing V_{CASN} from 57 DAC counts to 63 DAC counts, i.e. by lowering the charge threshold by about $30\,e^-$.
The performance of the pixels with diode reset (sector 2) is affected more. At $V_{BB} = 0\,\mathrm{V}$, the decrease of the detection efficiency is stronger than for the PMOS-reset pixels, as is the decrease of the average cluster multiplicity. Since the pixels of sectors 1 and 2 have identical collection diode geometries, it can be assumed that they exhibit an identical charge collection performance. Thus, the larger sensitivity to irradiation of the diode-reset pixels must be attributed to the reset mechanism. At $V_{BB} = -3\,\mathrm{V}$, the detection efficiency is not significantly affected, however, in contrast to the PMOS-reset pixels, the average cluster multiplicity is decreased.
The benefit of an increased spacing and the associated improved charge collection efficiency can be observed by comparing the results for sectors 1 and 3. Regarding the detection efficiency, the pixels of sector 3 (with 4 µm spacing) are clearly less affected by NIEL irradiation, now being the best performing pixel type. Besides, the average cluster multiplicity remains almost constant, also for zero reverse substrate bias.

5.3.4. Position resolution

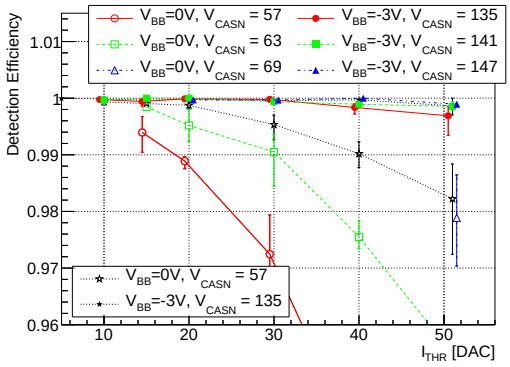
Fig. 5.31 presents a comparison of the position resolution and average cluster multiplicity as function of I_{THR} before and after irradiation, for three pixel types (sectors 1, 2, and 3) and two values of reverse substrate bias, each at nominal V_{CASN}. At $V_{BB} = 0\,\mathrm{V}$, as to be



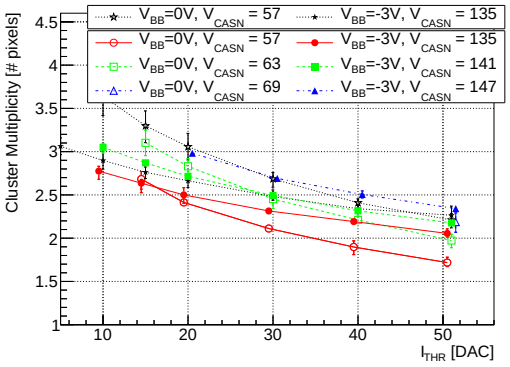
(a) ϵ_{det} sector 1.



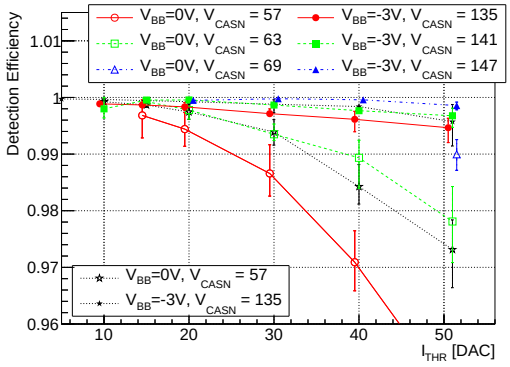
(b) Average cluster multiplicity sector 1.



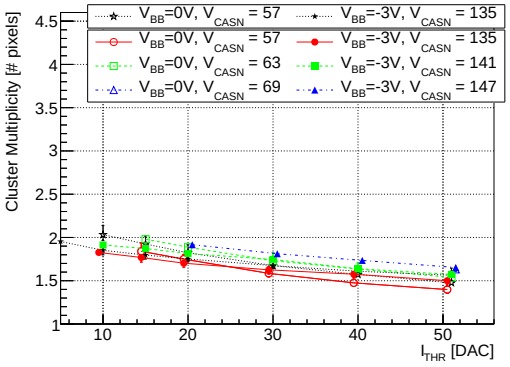
(c) ϵ_{det} sector 2.



(d) Average cluster multiplitcity sector 2.

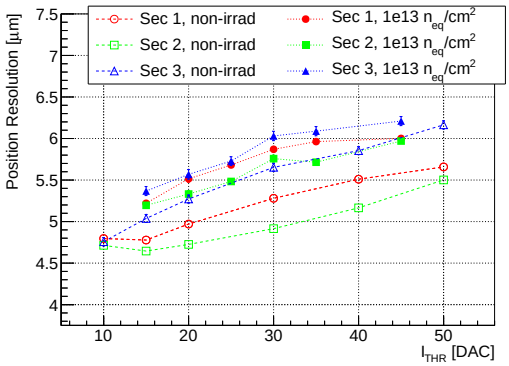


(e) ϵ_{det} sector 3.

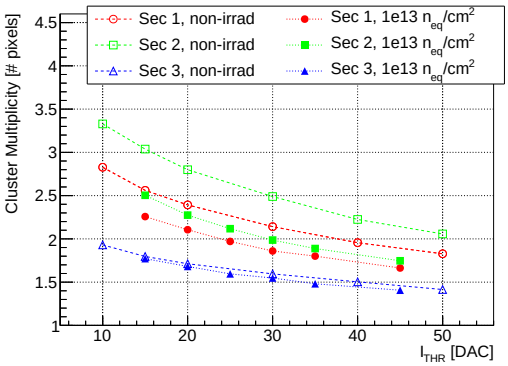


(f) Average cluster multiplicity sector 3.

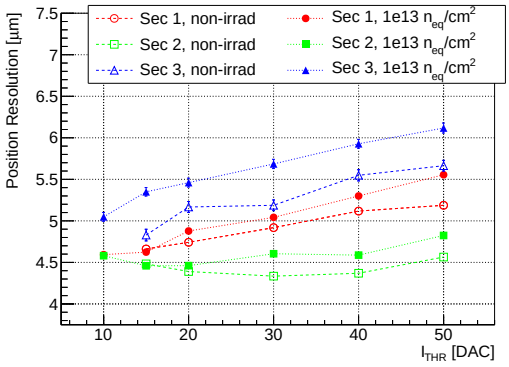
Figure 5.30.: Detection efficiency ϵ_{det} and average cluster multiplicity as a function of I_{THR}, averaged over three pALPIDE-1 chips irradiated with a fluence of 1×10^{13} 1 MeV $\text{n}_{\text{eq}}/\text{cm}^2$, for different pixels types, reverse substrate bias and values of V_{CASN}. For reference, also the values for the non-irradiated chips at nominal V_{CASN} are shown (black lines). All data was measured at the CERN PS with 6 GeV pions with the *STROBE_B* delay set to 2.2 µs. It should be noted that for the irradiated chips at $V_{BB} = -3$ V the changes of the working point due to increased leakage currents were compensated by adjusting V_{RESET} and V_{AUX} from 117 DAC counts to 125 DAC counts. Data points taken from [88].



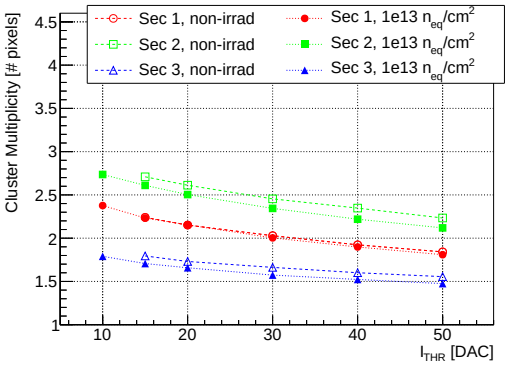
(a) Position resolution, $V_{BB} = 0\,\mathrm{V}$.



(b) Average cluster multiplicity, $V_{BB} = 0\,\mathrm{V}$.



(c) Position resolution, $V_{BB} = -3\,\mathrm{V}$.



(d) Average cluster multiplicity, $V_{BB} = -3\,\mathrm{V}$.

Figure 5.31.: Position resolution σ_{pos} and average cluster multiplicity as a function of I_{THR} (for a single pALPIDE-1 chip) before and after irradiation with a fluence of $1 \times 10^{13}\,1\,\mathrm{MeV\,n_{eq}/cm^2}$, for different pixels types and reverse substrate bias, each at nominal V_{CASN}. All data was measured at the CERN PS with a 6 GeV pion beam. For all measurements at $V_{BB} = -3\,\mathrm{V}$, V_{AUX} was adjusted from 117 DAC counts to 160 DAC counts. Data points taken from [88].

expected from the observations on the cluster multiplicity (cf. Fig. 5.31b), the diode-reset pixel with 2 µm spacing (sector 2) is most affected by irradiation, remaining only slightly superior to the PMOS-reset pixel with the same spacing (sector 1). The PMOS-reset pixels with 4 µm spacing of sector 3 show the smallest deterioration of the position resolution, along with the smallest change of the cluster multiplicity. Overall, for $V_{BB} = 0\,\mathrm{V}$ (and the presented front-end bias settings), all three pixel types show a comparable performance in terms of position resolution after irradiation, which ranges between 5.5 µm for $I_{\mathrm{THR}} \approx 20$ DAC counts and increases to about 6.5 µm for $I_{\mathrm{THR}} \approx 50$ DAC counts.
At $V_{BB} = -3\,\mathrm{V}$, the enhanced charge collection performance of the sensor, in particular for the pixels with 2 µm spacing, leads to less significant changes of the position resolution. In this case, the diode-reset pixel (sector 2) remains the best performing with a position resolution well below the required 5 µm also after irradiation.

5.4. Summary

The pALPIDE-1 is the first full-scale demonstrator of the ALPIDE design, combining a novel low-power front-end with a sparsified readout. In order to investigate the effects of different reset mechanisms (i.e. PMOS reset and diode reset), and collection-diode geometries (i.e. collection n-well diameter and spacing between the collection n-well and the surrounding p-well), it was designed with four different pixel types.
In this chapter, the studies of the different pixel types were combined with a characterization of the operational behaviour of the analogue part of the front-end, where the primary focus was put on the influence of the two bias parameters I_{THR} and V_{CASN}. The main performance parameters of the pixels were considered, that is the detection efficiency, the fake-hit rate and the position resolution. Since in the ALPIDE design the front-end is employed as an analogue memory, also the pulse duration has been studied in detail. In detail, the following points can be noted:

- Both front-end bias parameters I_{THR} and V_{CASN} can be used to adjust the charge threshold, where an increase of V_{CASN} reduces the threshold, while an increase of I_{THR} increases the threshold. Hence, different combinations of the bias parameters can be applied which result in an equal threshold. Alongside, however, an increase of I_{THR} reduces the pulse duration, while it is almost independent of V_{CASN}. In this context, combinations of I_{THR} and V_{CASN} towards larger values, but constant threshold, are favourable.

- The application of a reverse substrate bias voltage on the collection diode has shown to improve the sensor performance in terms of all regarded parameters, particularly after irradiation. This can be attributed to an increased Q/C ratio, which increases the charge-to-voltage conversion gain of the circuit, inherently reducing the charge threshold.

- The fake-hit rate both before and after irradiation is dominated by a small fraction of hot pixels, which exhibit a reproducible behaviour, being affected by RTS noise. Overall, the pALPIDE-1 shows an excellent fake-hit rate performance, as the required value of 10^{-5}/event/pixel can be safely reached for thresholds equivalent to $I_{\mathrm{THR}} \gtrsim 30\,\mathrm{DAC}$ counts and nominal V_{CASN} for the respective V_{BB} value without masking any pixel. Moreover, a fake-hit rate below 10^{-8}/event/pixel, also after irradiation, can be obtained for $I_{\mathrm{THR}} \gtrsim 30\,\mathrm{DAC}$ when masking about 1 ‰ of the pixels.

- Before irradiation, the pixel of sector 2, featuring a diode reset and 2 µm spacing is the best performing pixel in terms of detection efficiency and position resolu-

tion [88], which can be attributed to benefits from charge sharing and a reduced parasitic contributions to the pixel-input capacitance from the reset mechanism. However, the diode-reset mechanism is observed to be significantly more sensitive to irradiation than the PMOS reset due to an increased diode saturation current and consequently an increased conductance. This leads to increased instantaneous reset currents subsequent to the collection of signal charge that limit the voltage excursion at the sensing node, an effect that has been prominently observed in the pulse shape measurements. Therefore, after irradiation the diode reset can only be applied with caution.

Taking these considerations into account, the pixel of sector 3, featuring a PMOS reset and 4 µm spacing, is considered as the most favoured pixel, particularly at low reverse substrate bias. For this pixel, at $V_{BB} = 0\,\mathrm{V}$ and nominal V_{CASN}, the detection efficiency after irradiation stays above 99 % for $I_{\mathrm{THR}} \lesssim 30\,\mathrm{DAC}$ counts, where the maximum pulse duration is about 13 µs. This is, however, significantly larger than the desired value of $\leq 5\,\mu\mathrm{s}$. The situation can be improved by increasing V_{CASN} or, for a far larger improvement, by increasing the reverse substrate bias voltage.

At $V_{BB} = -3\,\mathrm{V}$ and nominal V_{CASN}, the detection efficiency after irradiation stays 99 % for all studied values of I_{THR}, assumingly up to $I_{\mathrm{THR}} \approx 70\,\mathrm{DAC}$ counts, where the maximum pulse duration is reduced to about 8 µs. Moreover, at this level of I_{THR}, a fake-hit rate below 10^{-7}/event/pixel can be safely obtained without masking any pixel. The position resolution for this setting, however, is in the order of 6.5 µm.

- The time resolution of the circuit is determined by the peaking time of the lowest pulse exceeding the threshold. As the pulse duration, it is depending on I_{THR}. It was measured to be about 3.1 µs for $I_{\mathrm{THR}} = 20\,\mathrm{DAC}$ counts and can be reduced to 1.8 µs when increasing I_{THR} to 70 DAC counts. The maximum pulse duration has been observed to be longer than expected from simulations (cf. Fig. 5.4), as it is about 8 µs even at very large values of I_{THR}.

In summary, the results show that working points of the pALPIDE-1 can be obtained for which the detection efficiency, position resolution and fake-hit rate are in line with the requirements set by the ALICE ITS upgrade, leaving sufficient margin after irradiation with an equivalent fluence of $1 \times 10^{13}\,1\,\mathrm{MeV\,n_{eq}/cm^2}$ (NIEL). Also validating a very low power consumption of $70\,\mathrm{mW/cm^2}$ and a time resolution of around 2 µs, the pALPIDE-1 has demonstrated the feasibility and attractiveness of the ALPIDE design. The performed measurements furthermore allowed to identify a strategy for the optimization of the pixel design in terms of reset type and collection electrode geometry, as well as for an optimal set of operational parameters as the reverse substrate bias voltage V_{BB} and the front-end bias parameters.

6. Summary and Outlook

During the Long Shutdown 2 of the LHC in 2019/20, the ALICE experiment plans the installation of a novel Inner Tracking System. It will have significantly improved tracking and vertexing capabilities, as well as readout rate, and will replace the current six layer detector system with seven layers of Monolithic Active Pixel Sensors (MAPS).

The pixel chip will be fabricated in the TowerJazz 180 nm CMOS process on wafers with a high resistivity epitaxial layer on top of the substrate, with a total thickness amounting to only 50 µm. Thereby, the epitaxial layer, which is typically only partially depleted, acts as the sensitive layer.
In this thesis, the development of the ALPIDE design has been discussed, which has two main distinguishing features: first, it consists of a low-power (40 nW) binary front-end and a sparsified readout, and second it allows to apply a reverse substrate bias to the charge collection diodes. The latter allows to significanlty enlarge the depletion regions around the charge collection diodes, with positive effects on the charge collection process and pixel-input capacitance, and consequently the Q/C ratio of the pixels.
Using small-scale prototypes with analogue readout, these effects have been quantified. For a reverse substrate bias voltage of -6 V, charge collection times in the order of a few ns have been obtained for pixels with a pitch of up to 30 µm, an epitaxial-layer thickness of 18 µm and a collection-diode footprint of $7.2 \times 7.2\,\mu\text{m}^2$. For this case, the charge collection effieciency was shown to be unaffected by an equivalent fluences of 1×10^{13} 1 MeV $\text{n}_{\text{eq}}/\text{cm}^2$ (NIEL). Leakage currents at this irradiation level reach up to a few pA per pixel.
The pixel-input capacitance has shown to strongly benefit from the implementation of a spacing between the collection n-well and the surrounding p-well, particularly at large reverse substrate bias. For the studied pixels, an input capacitance of approximately 5 fF is reached for $V_{BB} = 0$ V, which can be reduced by more than 50 % to about 2.0 fF when increasing V_{BB} to -6 V. For the different wafer types with epitaxial layer resistivities ranging between 1 kΩ cm and 7.5 kΩ cm, only minor differences were found.
Earlier studies on a dedicated test chip showed no relevant degradation of transistor performance up to 250 Mrad (TID), which is much beyond the values expected for the ALICE ITS upgrade [69].

The first final-size ($3 \times 1.5\,\text{cm}^2$) demonstrator of the ALPIDE design is represented by the pALPIDE-1. The characterization of this chip validated working points for which the detection efficiency, position resolution and fake hit rate are in line with, or even

surpassing, the requirements set by the ALICE ITS upgrade, with a satisfying operational margin also after irradiation with an equivalent fluence of $1 \times 10^{13}\,1\,\mathrm{MeV\,n_{eq}/cm^2}$. Moreover validating a very low power consumption of $70\,\mathrm{mW/cm^2}$ and a time resolution of about 2 µs, the pALPIDE-1 has demonstrated the feasability and attractiveness of the ALPIDE design. Overall, the results obtained represent a significant advancement of the technology of MAPS regarding power consumption, readout speed, charge collection time and radiation hardness.

However, the characterization also revealed room for optimizations. Recent observations indicate that the fake hit rate drops by orders of magnitude when using a larger input transistor, without penalties on the charge-to-voltage conversion gain [48]. The power consumption is foreseen to be reduced to less than $40\,\mathrm{mW/cm^2}$ for the inner layers. In the outer layers, where the hit densities, and therefore also the data rates are lower, a power consumption of $20\,\mathrm{mW/cm^2}$ is expected to be achievable [39].

The further optimization and implementation of additional building blocks will be adressed in later ALPIDE prototypes. At the same time also tests of detector module prototypes will take place. The start of the mass production of the final pixel chip is planned for mid 2016. The full detector will be commissioned at surface throughout 2019 and will be installed during the LS2 in 2020 in the ALICE cavern.

A. Acknowledgements

First and foremost I want to thank Manfred Krammer, who agreed to supervise me on this thesis and enabling me to participate in this exciting field. Secondly, I have to express my profound gratitude to my supervisor at CERN, Petra Riedler. Thank you very much for your guidance and help in all matters, it has been a pleasure to work with you. Special thanks also go to Luciano Musa. I have enjoyed all the discussions with you, they have been a great source of inspiration. I also would like to thank Magnus Mager for critically reflecting all my work and being a reference for testing new ideas. I sincerely appreciate all your advice. My warm thanks also go to Chris Fabjan for some reassuring conversations throughout the period of my PhD.

The work described in this thesis is the result of a collaboration with many people involved in the ALICE ITS upgrade project. Here, most of all, I have to mention Felix Reidt, with whom I have been working together in almost every project. Thank you very much for all your precious help, especially related to computing. Many thanks also go to Krzysztof Sielewicz for his hard work on the INVROS, that enabled me to include the results of the charge collection time in this thesis. I want to thank Monika Kofarago, for sharing the office, and always having an open ear for all the ideas that came into my mind throughout the days, some good, some worse. I would like to thank Miljenko Suljic, for all the creative conversations, particularly on the charge collection process and the related simulation. I owe many thanks to the participants in all the beam tests at CERN and DESY, particularly to Paolo Martinengo as our test-beam coordinator. My thanks also go Alberto Collu, with whom I have been working since the very early days of my PhD, for introducing me to the operation of readout systems. I want to thank Markus Keil for his help during the measurements on the pALPIDE-1. Furthermore, I would like to express my gratitude to Hartmut Hillemanns for proof-reading this thesis, already at its very early stages. I also would like express my gratitude to Walter Snoeys and Thanushan Kugathasan for always finding some time to discuss my questions on the functionality of all the many chips I have worked on.

My life during the past three years would not have been as enjoyable as it was without the people around me in Geneva and at CERN. In particular I want to thank the following list of people - in no particular order: Marc, for sharing *your* appartment, for the all the deep conversations over a beer, but most of all for motivating me to bike and run up mountains so much faster. It has been a pleasure. Amyina, for making particularly the early days in Geneva much more pleasant, and all the concerts. Francesco, for sharing your thoughts

on *mud* and many other things since then. The people of the KK - Francesco, Katie, Pier, Sue, for all the amazing moments. Felix, first, for simply being a great colleague, and then, for all the climbing. I hope it will continue - both. Krzysztof, for running up *some* mountain so many times with me and spending all those weekends on our little project. It has been great fun. Andres, Torsten, Jens, Alex, Jochen, Christian, and Johannes, for all the discussions and chats during lunch, and over the coffee after.

Then, major thanks go to my family. I know you did not appreciate my absence, but I received a lot of support from you nevertheless. Thank you.
Finally, my warmest thanks go to Marina. Thank you so much for your endless patience while I was working on this thesis. It is finished now.

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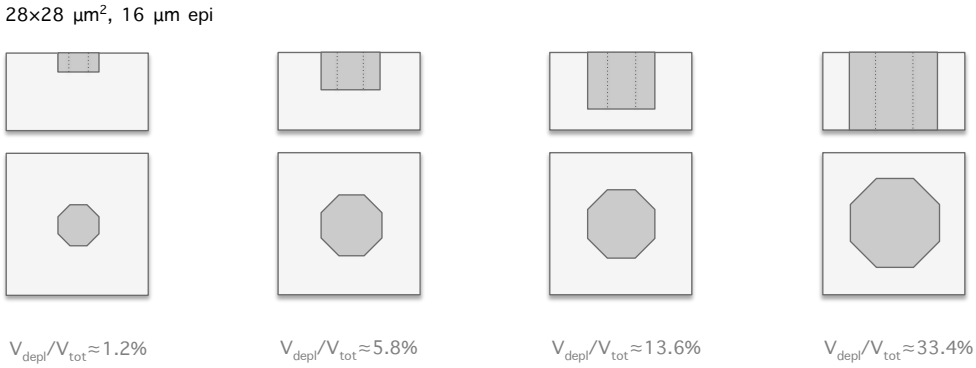
B. Acronyms

ADC	Analog-to-Digital Converter
AERD	Adress-Encoder Reset-Decoder
ALICE	A Large Ion Collider Experiment
ALPIDE	ALICE PIxel DEtector
ATLAS	A Toroidal LHC ApparatuS
BNL	Brookhaven National Laboratory
CERN	Conseil Européen pour la Recherche Nucléaire
CCE	Charge Collection Efficiency
CCT	Charge Collection Time
CDF	Cumulative Distribution Function
CDS	Correlated Double Sampling
CMC	Common Mode Correction
CMOS	Complementary Metal-Oxide Semiconductor
DAC	Digital-to-Analog Converter
DAQ	Data AcQuisition
DCS	Detector Control System
DESY	Deutsches Elektron-SYnchrotron
DUT	Device Under Test
ENC	Equivalent Noise Charge
FPC	Flex Printed Circuit
FPN	Fixed Pattern Noise
FPGA	Field-Programmable Gate Array
GC	Gain Correction
HIC	Hybrid Integrated Circuit
IB	Inner Barrel
INVROS	INVestigator ReadOut System
ITS	Inner Tracking System
IP	Interaction Point
LHC	Large Hadron Collider
LVDS	Low-Voltage Differential Signaling
LS2	Long Shutdown 2
MAPS	Monolithic Active Pixel Sensor
MFT	Muon Forward Tracker
MIP	Minimum Ionising Particle

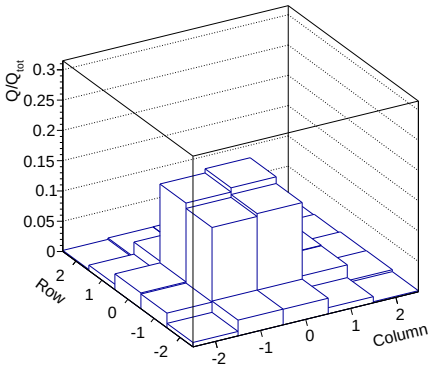
MM	Mini Matrix
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
MPV	Most Probable Value
NIEL	Non-Ionizing Energy Loss
NMOS	n-channel MOSFET
NPR	Non-Permanent Reset
OB	Outer Barrel
PDF	Probability Density Function
PID	Particle Identification
PMOS	p-channel MOSFET
PR	Permanent Reset
QCD	Quantum Chromodynamics
QGP	Quark-Gluon Plasma
RHIC	Relativistic Heavy Ion Collider
RMS	Root Mean Square
RPC	Resistive Plate Chamber
RRU	Region Readout Unit
RTS	Random Telegraph Signal noise
RU	Readout Unit
SDD	Silicon Drift Detectors
SEL	Single Event Latchup
SEU	Single Event Upset
SF	Source Follower
SNR	Signal-to-Noise Ratio
SPD	Silicon Pixel Detector
PS	Proton Synchrotron
SPS	Super Proton Synchrotron
SSD	Silicon Strip Detector
STAR	Solenoidal Tracker at RHIC
TID	Total Ionizing Dose
TN	Temporal Noise
TOF	Time-of-Flight detector
ToT	Time-over-Threshold
TPC	Time-Projection Chamber
TRD	Transition Radiation Detector
TRU	Top Readout Unit

C. Depletion approximation - Charge collection efficiency

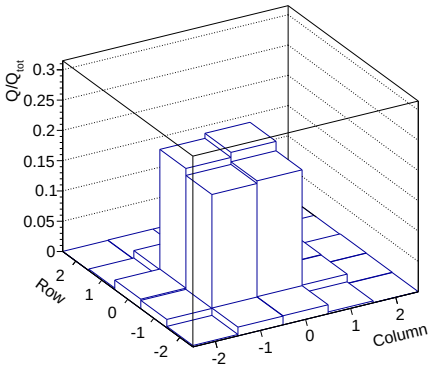
The figures in this section show the distribution of the integrated charge over the pixels of the 5×5 pixel matrix after the completion of the charge collection process. The presented pixel and depletion volume geometries are the same as discussed in Sec. 3.6.3.



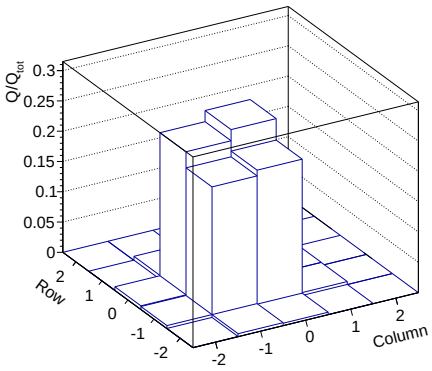
(a) Schematic representation of the simulated pixels with equal pitch (28 µm) and epitaxial layer thickness (16 µm), but different depletion volumes.



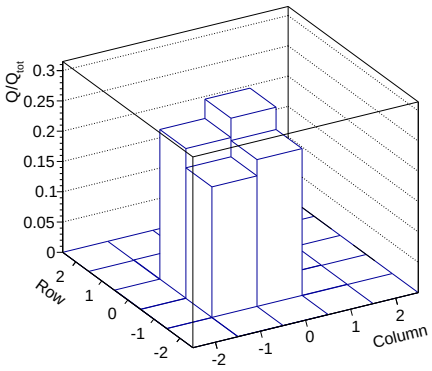
(b) Integrated charge for the case of $V_{depl}/V_{tot} = 1.2\,\%$.



(c) Integrated charge for the case of $V_{depl}/V_{tot} = 5.8\,\%$.

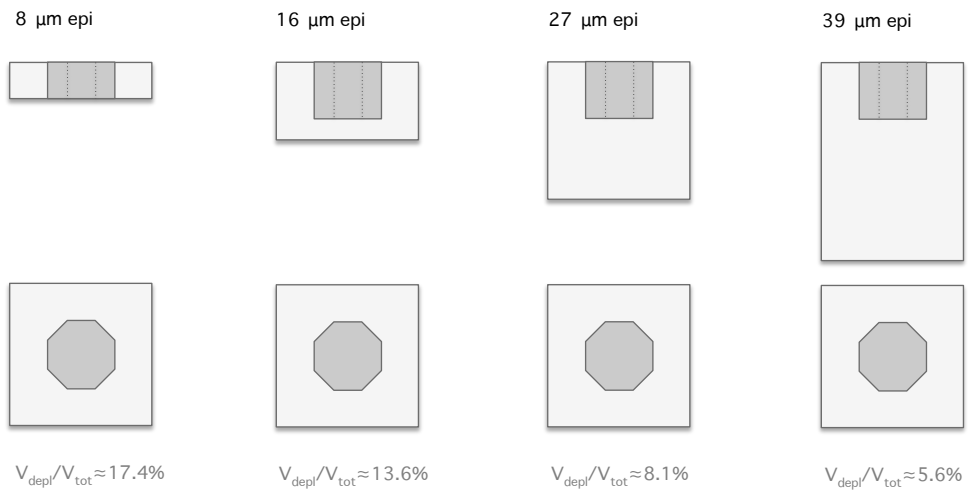


(d) Integrated charge for the case of $V_{depl}/V_{tot} = 13.6\,\%$.

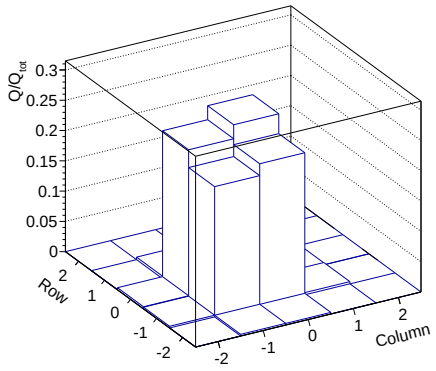


(e) Integrated charge for the case of $V_{depl}/V_{tot} = 33.4\,\%$.

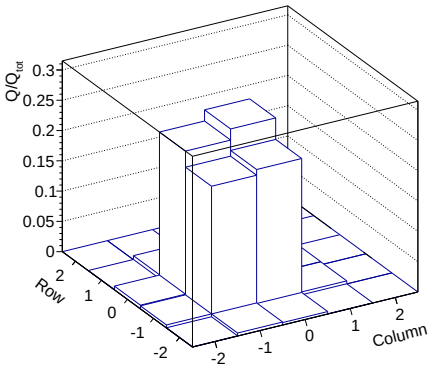
Figure C.1.: Integrated charge for different relative depletion volumes, but equal pitch (28 µm) and epitaxial layer thickness (16 µm).



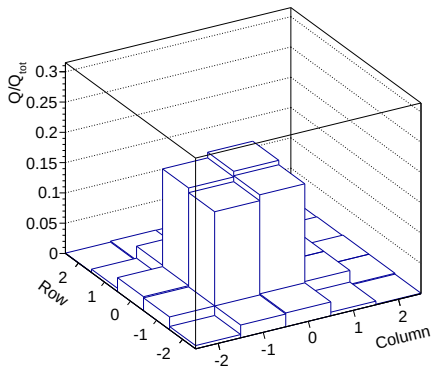
(a) Schematic representation of the simulated pixels with equal pitch (28 µm) and depletion volumes, but different epitaxial layer thicknesses.



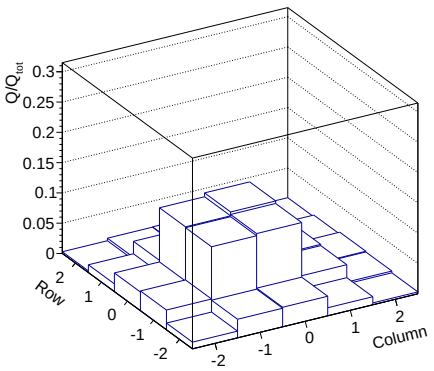
(b) Integrated charge for the case of $d_{epi} = 8\,\mu\text{m}$ ($V_{depl}/V_{tot} = 17.4\,\%$).



(c) Integrated charge for the case of $d_{epi} = 16\,\mu\text{m}$ ($V_{depl}/V_{tot} = 13.6\,\%$).

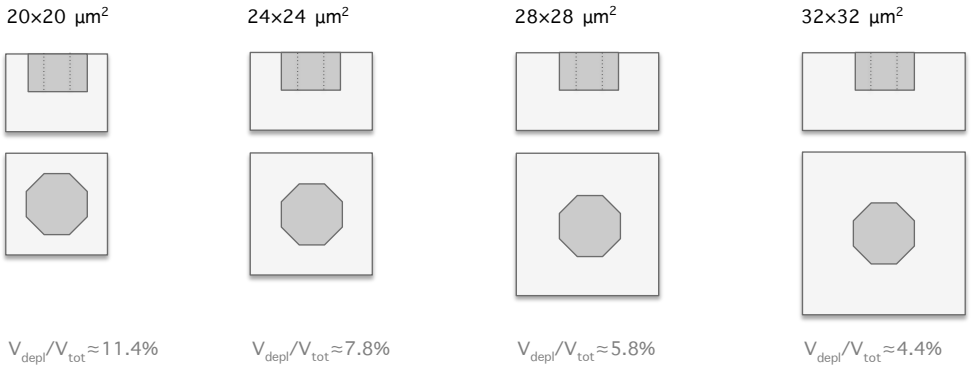


(d) Integrated charge for the case of $d_{epi} = 27\,\mu\text{m}$ ($V_{depl}/V_{tot} = 8.1\,\%$).

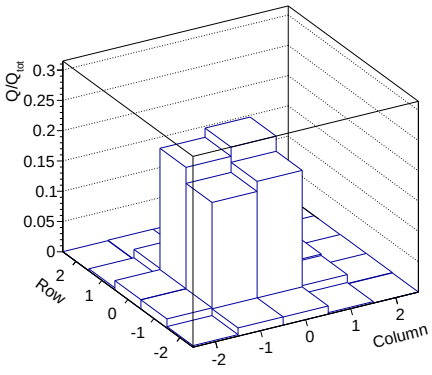


(e) Integrated charge for the case of $d_{epi} = 39\,\mu\text{m}$ ($V_{depl}/V_{tot} = 5.6\,\%$).

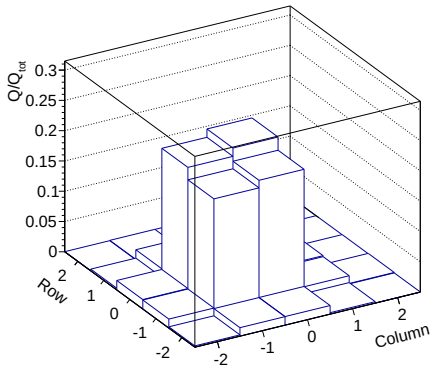
Figure C.2.: Integrated charge for pixels with equal pitch (28 µm) and depletion volumes, but different epitaxial layer thicknesses.



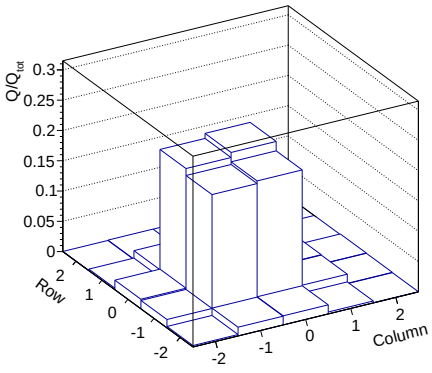
(a) Schematic representation of the simulated pixels with equal epitaxial layer thickness (16 µm) and depletion volume, but different pitch.



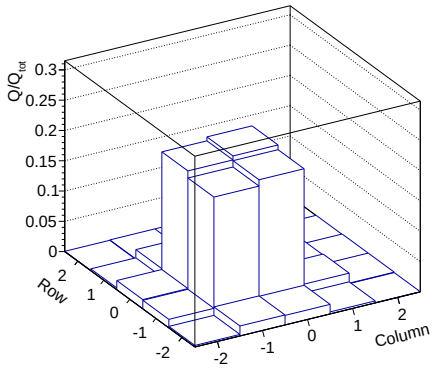
(b) Integrated charge for the case of a pixel pitch of 20 µm ($V_{depl}/V_{tot} = 11.4\,\%$).



(c) Integrated charge for the case of a pixel pitch of 22 µm ($V_{depl}/V_{tot} = 7.8\,\%$).



(d) Integrated charge for the case of a pixel pitch of 24 µm ($V_{depl}/V_{tot} = 5.8\,\%$).



(e) Integrated charge for the case of a pixel pitch of 28 µm ($V_{depl}/V_{tot} = 4.4\,\%$).

Figure C.3.: Integrated charge for pixels with equal depletion volume and epitaxial layer thickness (16 µm), but different pixel pitch.

D. Signal correction

D.1. Explorer-1

D.1.1. Gradient of in-pixel gain

As lined out in Sec. 4.2.2, the operating principle of the Explorer-1 readout architecture leads to lower signal and larger noise values for pixels connected later in the readout sequence. To mitigate these effects, a correction procedure based on the measured transfer function of the front-end circuit of each pixel has been developed. The details of the correction are illustrated in this section.

The reason for the experimentally observed lower signal values can be found in non-linearities of the transfer function $f_\mathrm{T} = V_\mathrm{OUT}(V_\mathrm{IN})$ of the front-end circuit, which is mainly originating from two effects: firstly, saturation effects in the PMOS source follower stage at the sensing node and the NMOS source follower stage after the memory cells and secondly, the fact that the leakage currents in the memory cells depend on the saved potential value, i.e. a larger potential involves a faster discharge rate. Generally, the differential gain g_n[1] of the readout circuit of a pixel n can be defined as the derivative of its transfer function:

$$g_n = \frac{\mathrm{d}f_{\mathrm{T},n}}{\mathrm{d}V_{\mathrm{IN},n}} = \frac{\mathrm{d}V_{\mathrm{OUT},n}}{\mathrm{d}V_{\mathrm{IN},n}} \tag{D.1}$$

where V_IN is the potential at the sensing node and V_OUT the corresponding output voltage measured at the readout system. Experimentally, f_T can be obtained by varying V_RST, therefore changing the voltage at the sensing node and measuring the corresponding output voltage V_OUT. This measurement is performed for two different steering sequences of the chip, differing in the application of the *RESET* signal:

- **Non-permanent reset (NPR):** The NPR sequence represents the default steering sequence for measurements with the Explorer-1 chip. The reset transistor is only kept open for sufficiently long time to recharge the sensing node to the equilibrium potential, whereafter it is closed to allow the circiut for charge detection. The resulting transfer function for the NPR sequence will be further referred to as $f_\mathrm{T,NPR}$. As a detailed analysis of the circuit shows, however, the closing the reset transistor

[1] The term *gain* may be misleading here, since in fact the progression of the transfer function is not only determined by the gain of the buffer and amplifier stages in the readout chain, but also strongly influenced by the discharge of the analogue memory cells.

also injects a significant amount of charge Q_{inj} onto the sensing node. Depending on the pixel capacitance C_p, this leads to the fact that the actual potential at the sensing node after the reset is larger than the equilibrium potential, hence causing a distortion of the transfer function. The transfer function $f_{\mathrm{T,NPR}}$ thus actually represents the exact working point $V_{\mathrm{RST,eff}} = V_{\mathrm{RST}} + Q_{\mathrm{inj}}/C_p$ of the circuit for a given V_{RST} value.

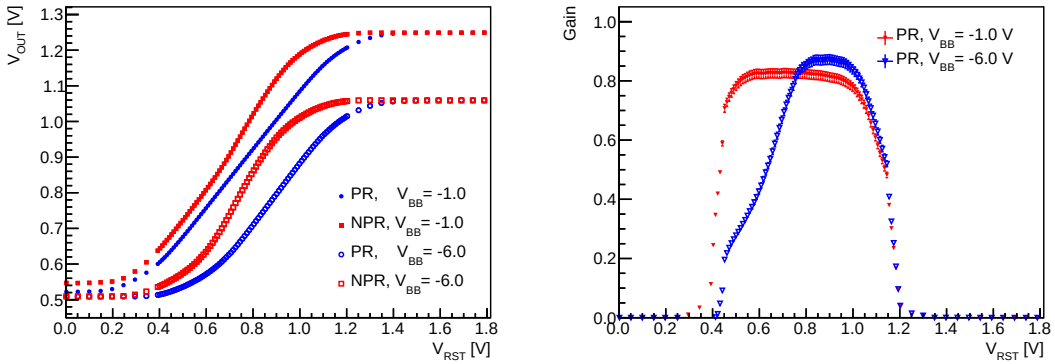
- **Permanent reset (PR):** To obtain a non-distorted transfer function of the readout circuit, measurements with a second steering sequence with a permanent reset are performed. For this, all steering signals are kept identical to the NPR sequence, except for the *RESET*, which is kept continuously asserted, hence eliminating the charge injection. The resulting transfer function for the PR sequence will be further referred to as $f_{\mathrm{T,PR}}$.

Fig. D.1a (left) shows the resulting transfer functions for *MEM1* of the first pixel in the readout sequence (pixel 0), for both PR and NPR, and furthermore for two different V_{BB} values of $-1\,\mathrm{V}$ and $-6\,\mathrm{V}$. The observations that can be made are the following:

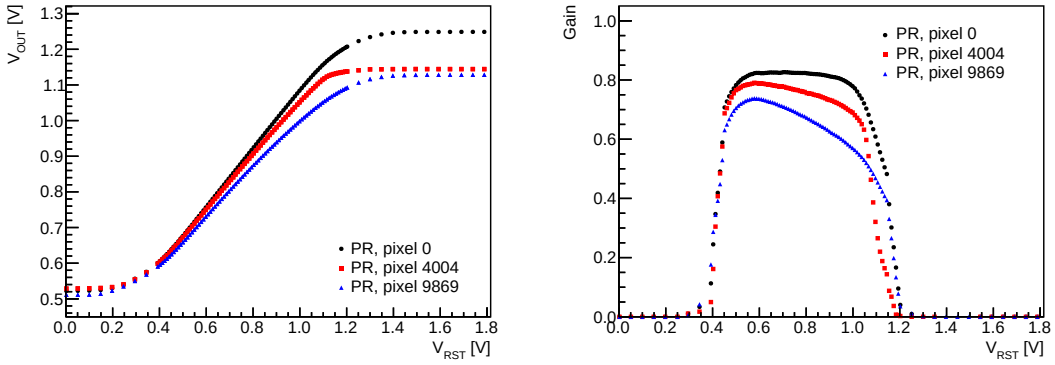
- All the transfer functions show saturation effects both at regions of low and high values of V_{RST}. The saturation at high V_{RST} (approaching $V_{\mathrm{DDA}} = 1.8\,\mathrm{V}$) can be attributed to the PMOS source follower stage at the sensing node, whereas the saturation at low V_{RST} (approaching GND) can be attributed to the NMOS source follower stage after the analogue memories.
  Furthermore, an offset between the curves for the different reverse substrate bias voltages can be observed. This effect can be attributed to the fact that the bulk terminal of the NMOS transistor is connected to the p-well potential, which is identical to V_{BB}. This causes a change of the characteristics of the NMOS transistors, including a threshold voltage shift depending on V_{BB}, that in turn entails different offsets after the NMOS source follower stage. Since for most of the PMOS transistors the bulk terminal is connected to the n-well potential, which is identical to V_{DDA}, their threshold voltage is not affected by changes of V_{BB}[2].

- The offset between the NPR and PR transfer functions as a function of V_{RST} for each V_{BB} value is related to the charge injected on the sensing node by closing the reset transistor: $\Delta V_{\mathrm{inj}} = Q_{\mathrm{inj}}/C_p$. It can be observed that ΔV_{inj} increases as V_{RST} is increased and furthermore that ΔV_{inj} is larger for larger values of V_{BB}, leading to cases where ΔV_{inj} reaches values up to $150\,\mathrm{mV}$.
  Indeed increasing V_{RST} and V_{BB} leads to a decrease of C_p and therefore expectedly

[2] In some pixel designs, the bulk terminal of the PMOS transistors can be connected differently (e.g. to the source terminal), or the n-well potential can be different from V_{DDA}. In these cases, this will be explicitly mentioned.



(a) Left: Transfer function f_{T} for an Explorer-1 pixel (pixel 0, *MEM1*) at $V_{BB} = -1\,\mathrm{V}$ and $-6\,\mathrm{V}$. The curves for permanent reset (PR) and non-permanent reset (NPR) are compared. Right: Gain curves for $V_{BB} = -1\,\mathrm{V}$ and $-6\,\mathrm{V}$ derived from the PR transfer functions in the left figure.



(b) Left: Transfer functions $f_{\mathrm{T,PR}}$ for *MEM1* of different Explorer-1 pixels at $V_{BB} = -1\,\mathrm{V}$. Right: Gain curves derived from the transfer functions on the left.

Figure D.1.: Transfer functions of the Explorer-1 sensor.

to an increase of ΔV_{inj}. However, also an increase of Q_{inj} with increasing V_{RST} and V_{BB} is conceivable, and up to date no detailed study has been performed to disentangle the effects.

Fig. D.1a (right) shows the differential gain of the readout circuit as a function of V_{RST} for two different V_{BB} values of $-1\,\mathrm{V}$ and $-6\,\mathrm{V}$, derived from the corresonding PR transfer functions on the left. For $V_{BB} = -1\,\mathrm{V}$ it can be observed that for V_{RST} values between the saturation regions, i.e. $0.5\,\mathrm{V} \lesssim V_{\mathrm{RST}} \lesssim 1.0\,\mathrm{V}$, there exists a plateau of approximately constant differential gain. For increased V_{BB} values, as can be observed from the curve for $V_{BB} = -6\,\mathrm{V}$, the width of the plateau is reduced from the side of lower V_{RST} values, now starting at $V_{\mathrm{RST}} \approx 0.8\,\mathrm{V}$ - an effect that can be attributed to the previously mentioned dependency of the characteristics of the NMOS transistor on V_{BB}.

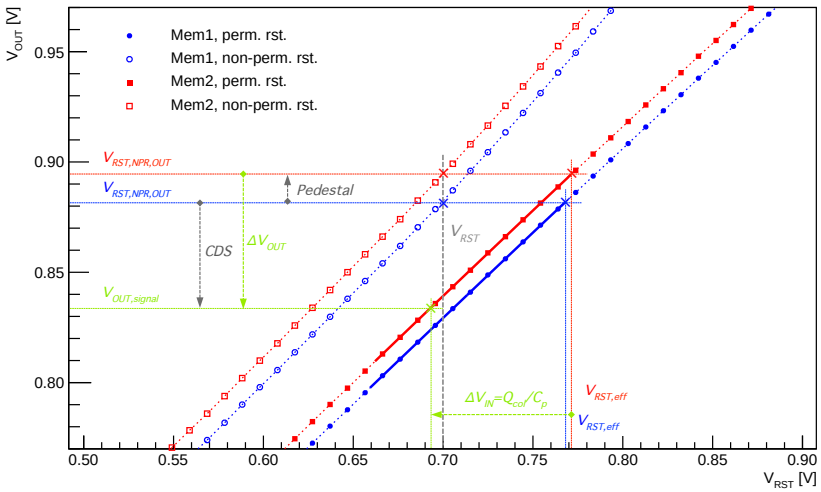


Figure D.2.: Graphical representation of the calcuation of the pedestal, signal and CDS values. Furthermore $V_{\mathrm{RST,NPR,OUT}}$ and $V_{\mathrm{RST,eff}}$ for both *MEM1* and *MEM2* are indicated.

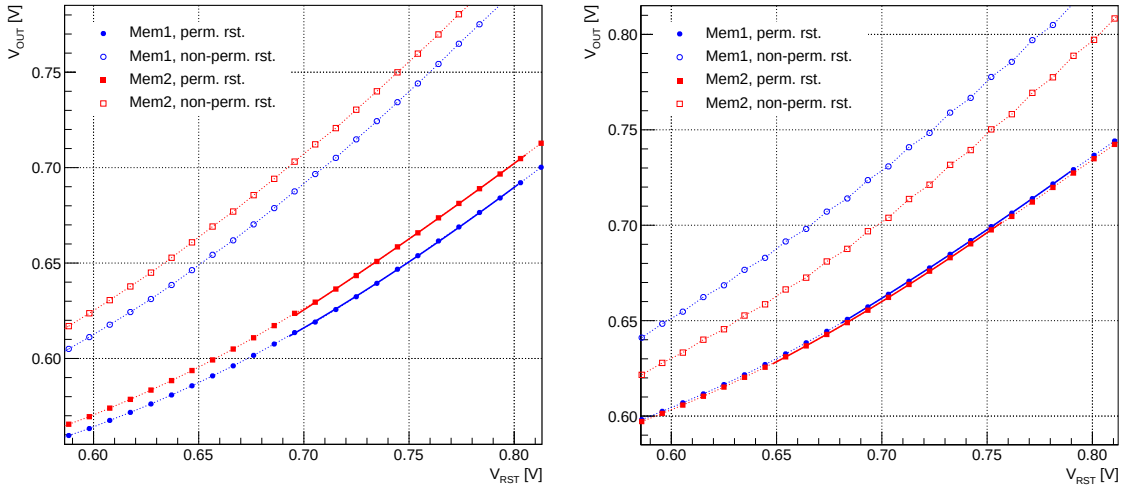
This observation has to be taken into account when choosing the working point (i.e. V_{RST}) of the circuit, which ideally should be placed in a region of constant differential gain. Since in order to allow for hit detection the Explorer-1 chip has to be operated with the NPR steering sequence, a second effect to be considered in this context is the charge injection, leading to an effective reset potential $V_{\mathrm{RST,eff}}$ typically larger than the applied reset voltage V_{RST}. Taking into account both effects, a V_{RST} value of 0.7 V was found to be suitable for all reverse substrate bias voltages and therefore used for all source and test beam measurements.

The influence of the leakage currents in the analogue memory cells can be observed in Fig. D.1b, in which the PR transfer function of three different pixels (with positions 0, 4004 and 9869 in the readout sequence[3]) is presented. As can be seen in Fig. D.1b (right), the differential gain is generally lower for pixels that are read out later. In addition, the plateau of appoximately constant differential gain as a function of V_{RST} observed for pixel 0 is deformed for later pixels: for higher V_{RST} values the gain is gradually decreasing until the saturation region. This effect can be explained by larger leakage currents at larger values of V_{RST}, of which the effects are increasingly pronounced at later readout times.

Gain correction

The objective of the gain correction (GC) is to obtain a correct estimate for the potential difference at the sensing node ΔV_{IN} corresponding to a measured potential difference

[3] Pixel 0 is the first pixel to be read in the readout sequence, pixel 4004 is the central pixel of the 20 µm × 20 µm pixel matrix, and pixel 9869 is the central pixel of the 30 µm × 30 µm pixel matrix.



(a) Non-irradiated Explorer-1 chip.

(b) Explorer-1 chip after NIEL irradiation with $1 \times 10^{13}\,1\,\mathrm{MeV\,n_{eq}/cm^2}$.

Figure D.3.: Zoom in of the transfer functions $f_{\mathrm{T,NPR}}$ and $f_{\mathrm{T,PR}}$ for both *MEM1* and *MEM2* of an Explorer-1 pixel measured at $V_{BB} = -6\,\mathrm{V}$ from (a) a non-irradiated chip and (b) a chip after NIEL irradiation of $1 \times 10^{13}\,1\,\mathrm{MeV\,n_{eq}/cm^2}$.

ΔV_{OUT}. This can be achieved using the inverse of the experimentally obtained transfer function: $f_{\mathrm{T}}^{-1} = V_{\mathrm{IN}}(V_{\mathrm{OUT}})$. Assuming the sensing node is at the effective equilibrium potential $V_{\mathrm{RST,eff}}$ before the hit, the gain corrected value for $\Delta V_{n,\mathrm{OUT}}$ measured at pixel n can be expressed as:

$$\begin{aligned}\Delta V_{\mathrm{IN},n} &= \int_{V_{\mathrm{RST,NPR,OUT},n} - \Delta V_{\mathrm{RST,NPR,OUT},n}}^{V_{\mathrm{OUT,\,RST},n}} g_n^{-1}\,\mathrm{d}V_{\mathrm{OUT},n} \\ &= f_T^{-1}(V_{\mathrm{RST,NPR,OUT},n}) - f_T^{-1}(V_{\mathrm{RST,NPR,OUT},n} - \Delta V_{\mathrm{OUT},n}) \end{aligned} \tag{D.2}$$

where g_n^{-1} is the inverse of the differential gain derived from $f_{\mathrm{T,PR}}^{-1}$ and $V_{\mathrm{RST,NPR,OUT},n}$ is the voltage measured at the output for a given V_{RST} when operating the chip with the NPR sequence.

In case of the Explorer-1 chip, the pedestal, CDS and signal values are calculated employing the two analogue memory cells *MEM1* and *MEM2* (cf. Fig. D.2). The details of the implementation of the gain correction procedure are presented in the following (cf. Fig. D.2). During the measurements, V_{RST} is set to 0.7 V. The corresonding voltages measured at the output for each memory when operating the chip with the NPR sequence ($V_{\mathrm{RST,NPR,OUT}}$) are indicated. According to Eq. (4.5) the pedestal is defined as the mean difference of these values. Projecting the $V_{\mathrm{RST,NPR,OUT}}$ values to the PR transfer functions yields the effective equilibrium potentials $V_{\mathrm{RST,eff}}$. If charge is collected at the sensing node within the integration time, the output value of *MEM2* will decrease accordingly, whereas the output of *MEM1* is not affected. Consequently, the CDS value will change

and a signal value $\Delta V_{\mathrm{OUT}} = \mathit{CDS} - \mathit{Pedestal}$ different from zero will be obtained.
Since it is the output value of *MEM2* that changes when signal charge is collected, it is the inverse transfer function of *MEM2* that is employed for the GC according to Eq. (D.2). The tranfser functions are fitted with a cubic function in the range from $V_{\mathrm{RST,eff}} - \Delta V_{\mathrm{sig}}$ up to $V_{\mathrm{RST,eff}}$, where ΔV_{sig} is the maximum expected voltage drop due to signal charge collection[4]. The fit parameters for each pixel and memory of the chip are then saved for availability in the GC processing.

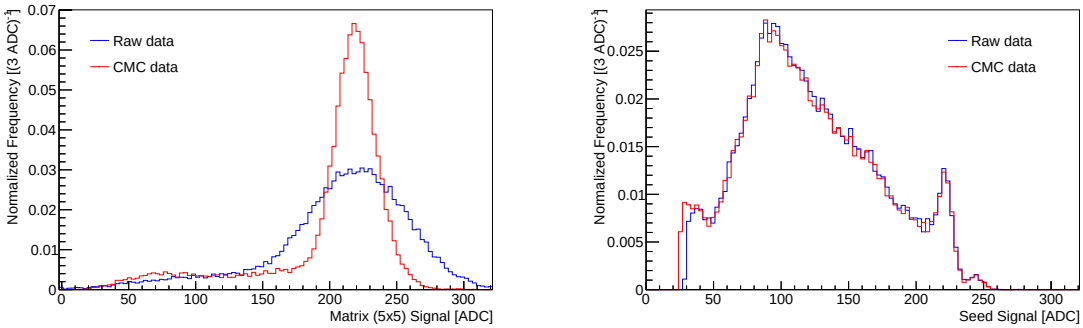
It should be noted that since the potential at the sensing node is saved to *MEM2* only after the integration time Δt_{INT}, the corresponding value $V_{\mathrm{RST,NPR,OUT}}$ is also influenced by leakage currents. An example of the effect is presented in Fig. D.3a and Fig. D.3b, where the transfer functions are shown for a pixel of a non-irradiated and an irradiated Explorer-1 chip, respectively, for a V_{BB} value of $-6\,\mathrm{V}$[5]. It can be observed that for the non-irradiated chip, both the PR and NPR transfer functions of *MEM2* lie above the corresponding transfer functions of *MEM1*, with very similar offsets for both PR and NPR. The situation changes significantly for the irradiated chip, where the leakage current at the collection diode is strongly increased: the NPR transfer function for *MEM2* now lies below the transfer function of *MEM1*. Due to the discharge of the sensing node related to the leakage current, a large part of the charge injected by the reset operation is already compensated, reducing the measured offset between the NPR and PR transfer function for *MEM2*.
The observed effects after irradiation lead to a shift of the working point of the circuit, particularly for *MEM2*. This has to be taken into account when measuring irradiated Explorer-1 chips.

D.1.2. Common-mode noise

A more detailed analysis of the pixel signals revealed common event by event deviations of the CDS values of all pixels in a sector or the entire pixel matrix from their pedestal value. If not corrected for, these common-mode fluctuations represent an additional noise source. As the main source of the common-mode fluctuations the noise on the supply of the V_{BB} could be identified. Furthermore, as another but less influential source, a non-periodic readout sequence of the chip could be identified. Even though the effect of these sources has been mitigated, for a better estimation of the characteristic parameters of the pixels that is almost independent of the appearence of common-mode fluctuations,

[4] Assuming a maximum charge of 2500 electrons to be generated and a pixel input capacitance of 2.5 fF, ΔV_{sig} results in 160 mV.

[5] The expample of a chip irradiated with $1 \times 10^{13}\,1\,\mathrm{MeV\,n_{eq}/cm^2}$ NIEL and $V_{BB} = -6\,\mathrm{V}$ was chosen since for this combination the largest leakage currents are expected.



(a) Matrix signal distribution. **(b)** Seed signal distribution.

Figure D.4.: Explorer-1 response to X-rays from an ^{55}Fe source for a pixel with a 7.6 µm^2 octagonal n-well electrode and 2.1 µm spacing between the n-well and the surrounding p-well (sector 5), $V_{BB} = -1$ V on and HR18 wafer. The raw data is compared to the CMC data. Where to be applied, the cuts are $10\,\sigma$ on for the seed signal and $3\,\sigma$ on the neighbouring pixels.

an offline correction method was developed.

Common-mode correction

In the procedure for the common-mode correction CMC, the common-mode fluctuation of the pixels of a sector in a particular event is estimated by calcuating the winsorized mean WM [6] of their CDS values.

The signal, pedestal and noise values are then redefined in the following way: The pedestal value for a pixel n is redefined as the mean value of the deviation of its CDS value from the winsorized mean WM_{sec} of the CDS values of all pixels in the corresponding sector. For a given set of N events it can be expressed as

$$\text{Pedestal}_{cmc,n} = \frac{1}{N}\sum_{i=1}^{N}(\text{CDS}_{n,i} - WM_{sec,i}) \tag{D.3}$$

for wich the expectation value is zero.

The noise value of a pixel n is redefined as the RMS of the distribution of the deviation

[6] The winsorized mean is a winsorized statistical measure, similar to the truncated mean. It involves the calculation of the mean after replacing given parts of a probability distribution or sample at the high and low end with the most extreme remaining values, typically doing so for an equal amount of both extremes; often 10 to 25 percent of the ends are replaced.

of the CDS values from WM_{sec}.

$$\text{Noise}_{cmc,n} = \sqrt{\frac{1}{N-1}\sum_{i=1}^{N}(\text{CDS}_{n,i} - WM_{sec,i} - \text{Pedestal}_{cmc,n})^2} \tag{D.4}$$

Once the pedestal and the noise values are estimated from a separate run, the pixel signal for an event i and pixel n is defined by:

$$\text{Signal}_{cmc,n,i} = \text{CDS}_{n,i} - WM_{sec,i} - \text{Pedestal}_{cmc,n}. \tag{D.5}$$

The effect of the CMC is shown in Fig. D.4, where the matrix signal and seed signal distributions for X-rays from ^{55}Fe source are shown for raw data and CMC data. The improvement after the CMC can be most clearly observed for the matrix signal distribution since it represents the distribution of the sum of the signals of 5×5 pixels, whereas no significant change for the seed signal is observed. In summary, the CMC allows a more precise estimation of several observables, in particular the charge collection efficiency for an $n \times n$ pixel matrix.

D.2. Transfer functions of the Investigator-0 front-end circuit

During the first measurements of the Investigator-0 chip, large currents[7] at the V_{RST} and V_{BB} supply lines were observed, that are depending on the V_{RST} potential provided to the chip. Furthermore the large currents are only observed when measuring mini-matrices (MM) containing PMOS reset pixels.
The cause could be identified in a design error of the dummy-pixels of the mini-matrices where the input transistor is placed inside the collection n-well. The schematic design of the in-pixel circuit of both the central pixel and the dummy-pixel for this MM is presented in Fig. D.5. A parasitic forward biased diode is created between the p-type implant for the source terminal of the input transistor and the collection n-well, which acts as the transistor bulk. In equilibrium the collection n-well, and thus the gate terminal of the input transistor, is approximately at the V_{RST} potential. In case of the central pixel design, the source potential always follows the gate potential and the forward bias of the parasitic diode is never sufficiently high to allow a significant forward current. In case of the dummy pixel design, however, the source terminal of the input transistor is directly connected to V_{DDA}. Consequently, if the value of V_{RST} reaches below $V_{\text{DDA}} - V_{\text{d,thr}}$, $V_{\text{d,thr}}$ being the diode threshold voltage, a significant current starts to flow from the V_{DDA} to

[7] Currents of the order of mA instead of pA were observed for lower V_{RST} values and when measuring mini-matrices with transistor reset.

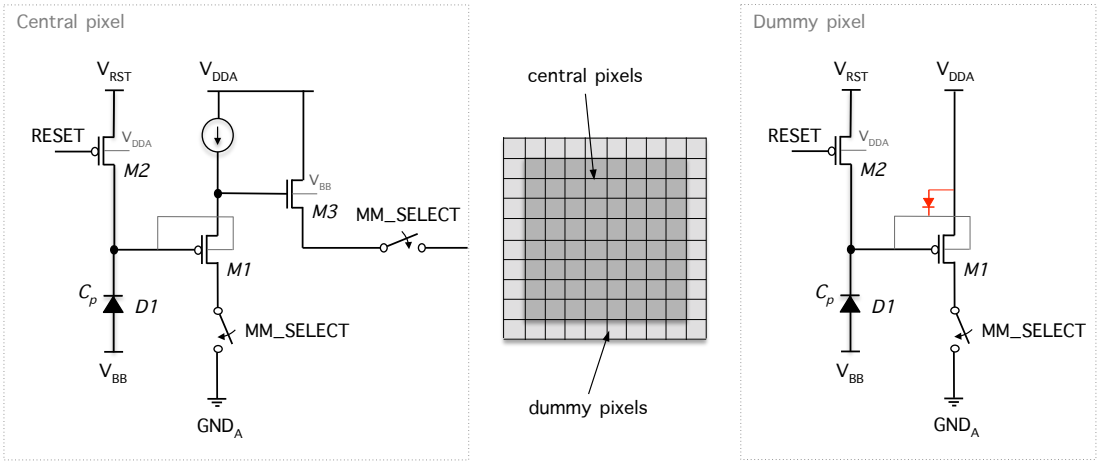


Figure D.5.: Schematic pixel circuit of the mini-matrix with PMOS reset and the input transistor placed inside the collection n-well. The fact that the input transistor is placed inside the collection n-well is represented in the schematic by the connection of the bulk terminal to the sensing node. In this design, a parasitic diode forward-biased diode is created between the p-type implant for the source terminal of the input transistor and the collection n-well.

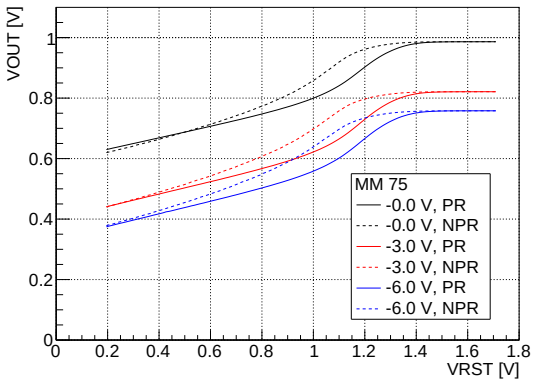


Figure D.6.: Measured transfer functions for a transistor (active) reset pixel of the Investigator-0. The curves are presented for the V_{BB} values of 0 V, −3 V and −6 V.

the V_{RST} supply net.

The characteristics of the circuit are however such that the current only flows if the reset transistor is opened. If it is kept closed, as is the case when measuring during the integration phase or in general when measuring other mini-matrices which contain a diode reset pixel, no increase of current is visible[8].

One effect of the high currents can be observed in the measured transfer functions[9] for the

[8] For the diode reset pixels with the input transistor placed inside the collection n-well the strong increase of current is suppressed by the fact as soon as current starts flowing from the V_{DDA} node to the sensing node, the reset diode gets reversely biased.

[9] See Sec. D.1.1 for a definition and the measurement principle.

transistor reset pixels of the Investigator as presented in Fig. D.6: whereas at large V_{RST} values the curve behaves as expected with a slope close to unity, below the saturation region at $V_{\mathrm{RST}} \approx 1.2\,\mathrm{V}$, the slope changes to smaller values for $V_{\mathrm{RST}} \lesssim 1.1\,\mathrm{V}$, giving the impression of a decreased differential gain. However, if the large current start flowing from the V_{DDA} to the V_{RST} supply net across the parasitic diode in the affected dummy-pixels, resistive voltage drops in the V_{RST} supply net occur. Consequently, since the V_{RST} supply net is same for all mini-matrices, the reset voltage provided to *all* pixels is no longer (approximately) equal to the V_{RST} voltage provided to the chip. Hence, the measured transfer function for *all* pixels in the region of $V_{\mathrm{RST}} \lesssim 1.1\,\mathrm{V}$ does no longer represent the gain of the circuit and can no longer be used for a gain correction of the pixel signals.
That meaningful results, however, can still be obtained can be understood when reconsidering the following points:

- The large current only flows in dummy-pixels of certain mini-matrices, for $V_{\mathrm{RST}} \lesssim 1.2\,\mathrm{V}$, and only if the reset transistors are kept open, i.e. during the reset phase.
- The large curent leads to a resistive voltage drop in the V_{RST} supply net, which is connected to all pixels. Therefore also pixel not affected by the large current, i.e. all pixel except the affected dummy-pixels, are no longer supplied with the V_{RST} voltage provided to the chip. The precise working point of the front-end circuit is thus unknown, however within limits that can be estimated.

In summary, all central pixels are properly functioning, however, for the pixels with active reset the working point is slightly unkknown and no gain correction procedure can be applied. In this context, for observables as the charge collection time and relative depletion volume no signifant limitations are expected. However, regarding other observables the following issues have to be kept in mind:

- Pixel-to-pixel variations of the gain of the on-chip circuitry within a single mini-matrix are expected to be negligible. However, comparisons between the pixels of different mini-matrices have to be based on the assumption that the respective front-end circuits exhibit the same gain. In particular for mini-matrices with the same front-end design this assumption is very reasonable.
- A precise estimation of the pixel input capacitance is not possible without the gain correction of the output signal (see Sec. 4.5.1).
- In case of the Explorer-1, the gain correction was also used to correct for non-linearities of the transfer functions that lead to uncertainties of a few percent for observables based on signal comparisons, such as the charge collection efficiency. For the Investigator-0 these unceratainties remain.

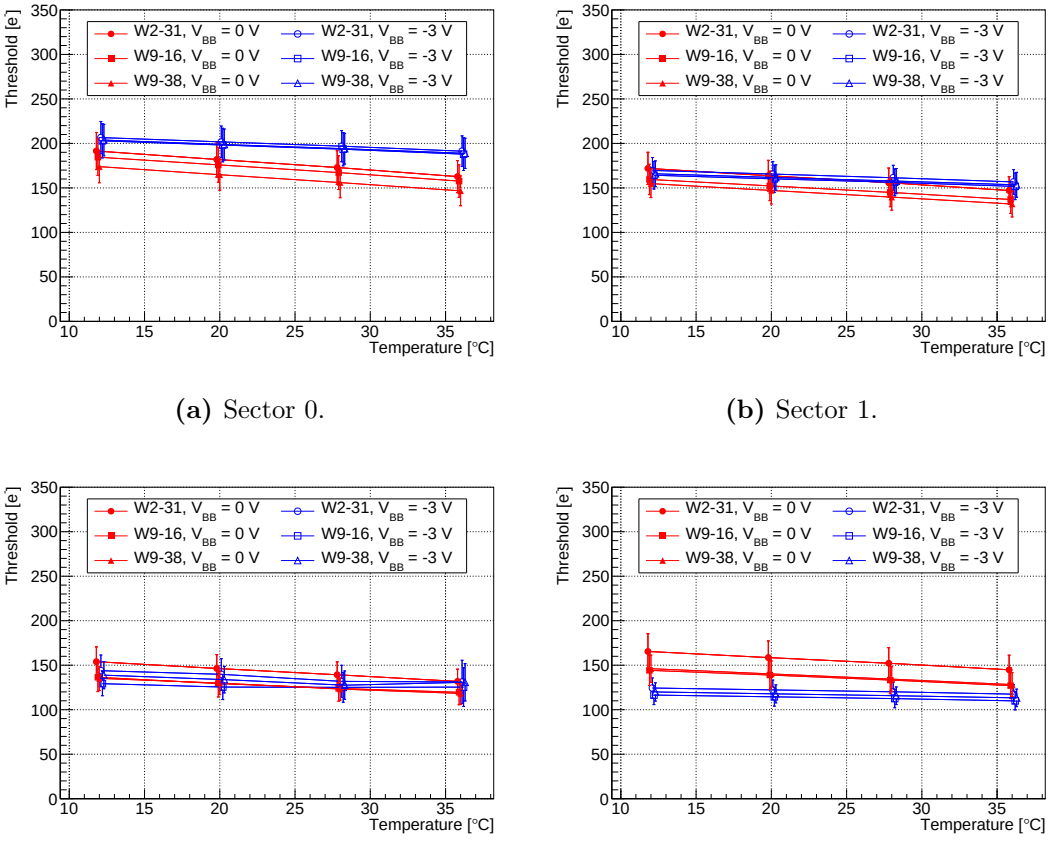
E. Threshold measurement summary

E.1. Non-irradiated chips

The plots in the following present a summary of the measurements of the threshold, threshold RMS and temporal noise as a function of temperature, for different chips and V_{BB} values. Measurements for a range of values of I_{THR}, have been performed, however, as an example only results for $I_{\mathrm{THR}} = 30\,\mathrm{DAC}$ counts are presented. The V_{CASN} DAC was set to the nominal value for the respective V_{BB}.

Thresholds The results of the threshold measurements are presented in Fig. E.1. It should be noted that the generally observed change of the charge threshold obtained when applying V_{BB} is not only caused by the changes in V_{BB}, but also depends on the respective (nominal) setting of V_{CASN}. In general, the following points, separately for each V_{BB} value, can be noted:

- $V_{BB} = 0\,\mathrm{V}$:
  - An increase of temperature from 12 °C to 36 °C yields a decrease of the threshold in the order of $20\,e^-$.
  - The behaviour is similar for all sectors.
  - The chip-to-chip variation is about $20\,e^-$ and constant as function of temperature.
  - The threshold distributions from which the data points are obtained are symmetric and resemble a Gaussian.
- $V_{BB} = -3\,\mathrm{V}$:
  - The temperature dependency of the threshold values is less pronounced, however, a decrease of threshold with increasing T can still be observed.
  - The behaviour is similar for all sectors.
  - The chip-to-chip variation is observed to be decreased to about $10\,e^-$ remaining constant as function of temperature.
  - The threshold distributions from which the data points are obtained are Gauss-like, and symmetric for the PMOS reset pixels (sectors 0, 1, 3), while the for diode reset sector a tail to larger threshold values can be observed. A more



(a) Sector 0. **(b)** Sector 1.

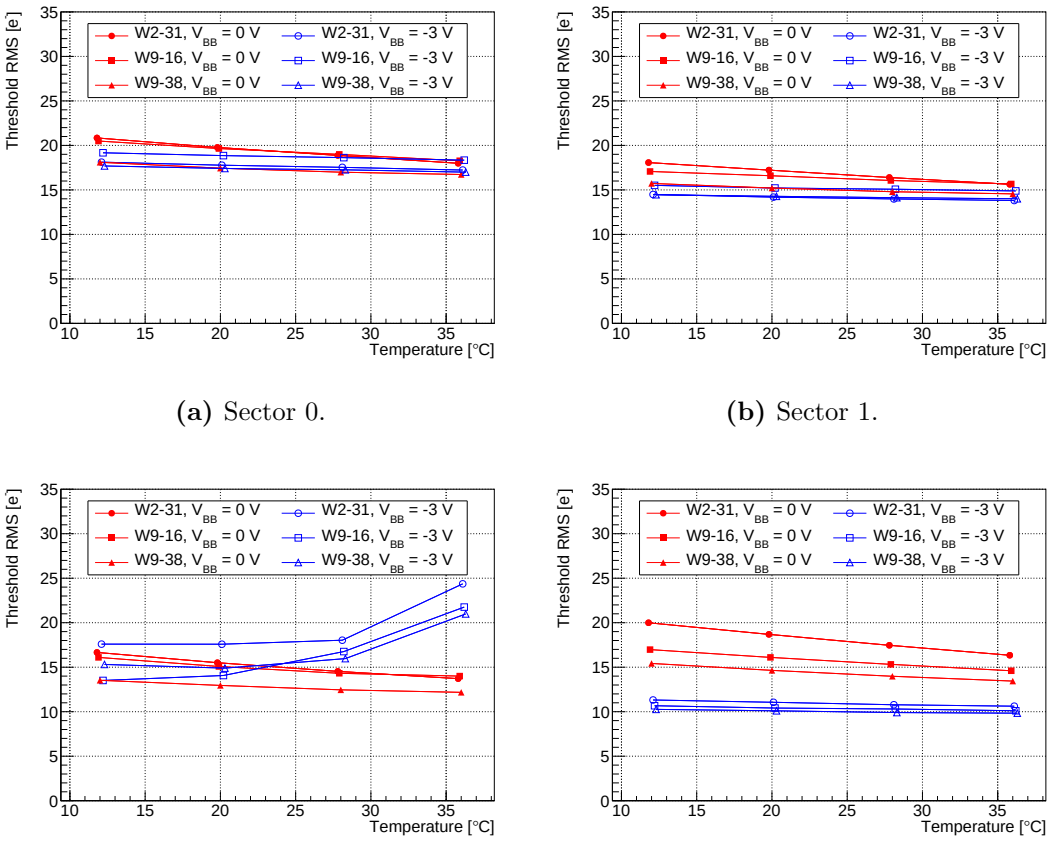
(c) Sector 2. **(d)** Sector 3.

Figure E.1.: Threshold as a function of temperature for the four sectors of pALPIDE-1 at $I_{\mathrm{THR}} = 30\,\mathrm{DAC}$ units for different chips and V_{BB} values at nominal V_{CASN} each. The error bars represent the pixel to pixel variation, i.e. the threshold RMS.

detailed analysis, however, showed that this tail is caused by pixels in row zero only [89].

Thresholds RMS The results of the threshold RMS are presented in Fig. E.2. The following points, separately for each V_{BB} value can be noted:

- $V_{BB} = 0\,\mathrm{V}$:
  - The threshold RMS is slightly decreasing with increasing temperature.
  - The behaviour is very similar for all sectors.
- $V_{BB} = -3\,\mathrm{V}$:
  - For the PMOS reset sectors (0, 1, 3), the threshold RMS is less dependent on the temperature and the chip-to-chip variation is reduced.
  - For the diode reset sector (2), the threshold RMS rises with increasing tem-



(a) Sector 0.

(b) Sector 1.

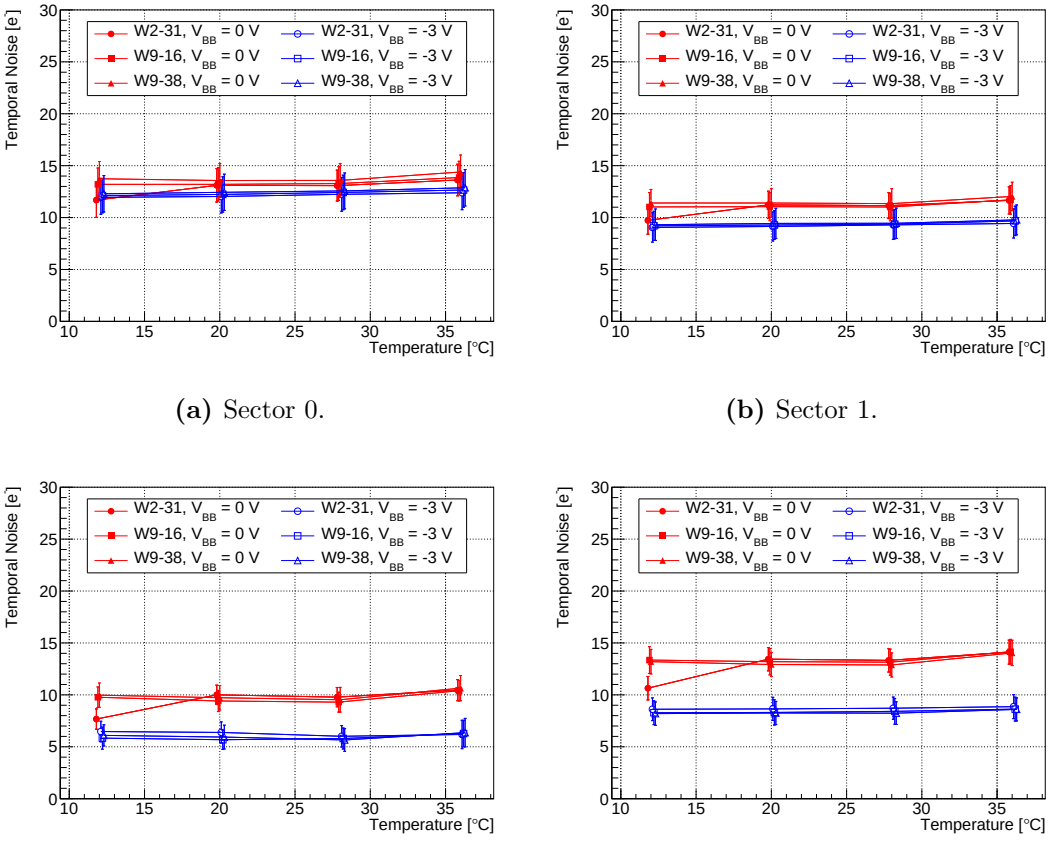
(c) Sector 2.

(d) Sector 3.

Figure E.2.: Threshold RMS as a function of temperature for the four sectors of pALPIDE-1 at $I_{\mathrm{THR}} = 30\,\mathrm{DAC}$ units for different chips and V_{BB} values at nominal V_{CASN} each.

perature, a fact that can be attributed to the tail observed in the threshold distributions. As previously noted, this tail is caused by pixels in row zero only [89].

Temporal noise The results of the temporal noise are presented in Fig. E.3. It can be noted that the temporal noise is almost constant as a function of temperature, and it is decreased for all sectors for larger values of reverse substrate bias.



(a) Sector 0. **(b)** Sector 1.

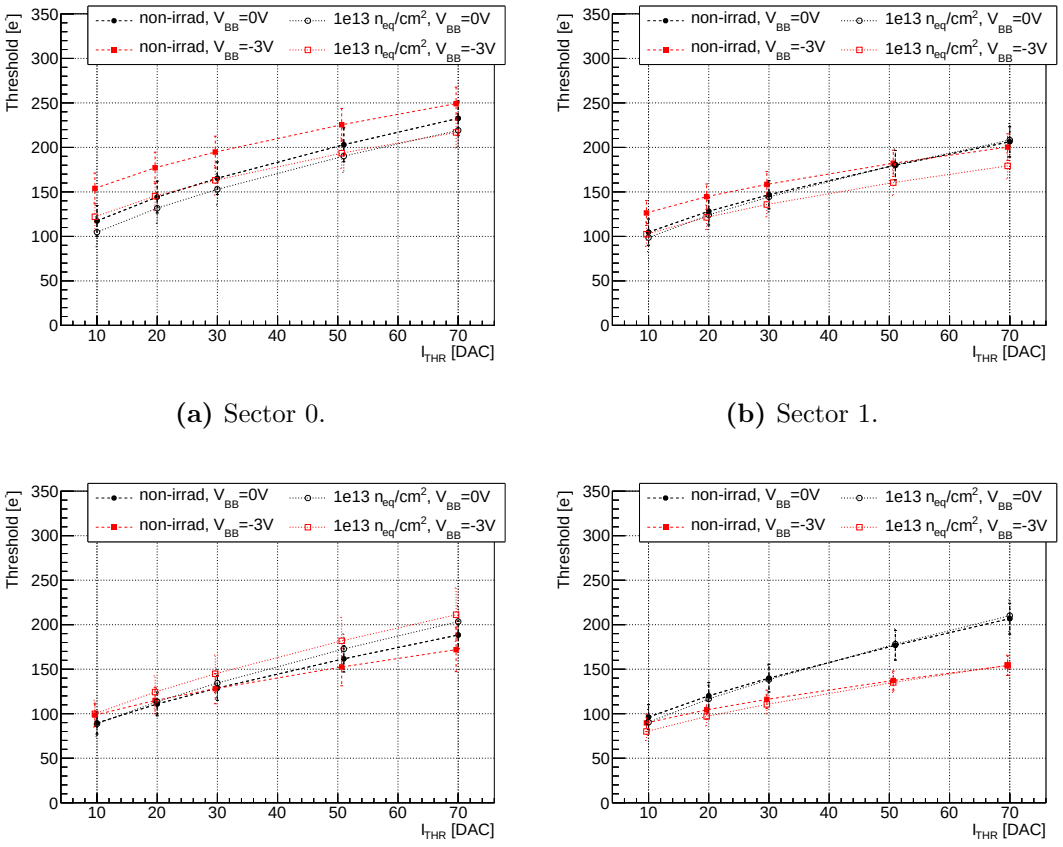
(c) Sector 2. **(d)** Sector 3.

Figure E.3.: Temporal noise as a function of temperature for the four sectors of pALPIDE-1 at $I_{\mathrm{THR}} = 30\,\mathrm{DAC}$ units for different chips and V_{BB} values at nominal V_{CASN} each. The error bars represent the pixel to pixel variation.

E.2. Irradiated chips

Thresholds Fig. E.4 presents a summary of the irradiation effects on the charge threshold when the front-end bias settings are kept constant. It shows the threshold as function of I_{THR} for the four pixel variants of pALPIDE-1 before and after irradiation with a fluence of $1 \times 10^{13}\,1\,\mathrm{MeV\,n_{eq}/cm^2}$ at 28 °C for different values of V_{BB}, each at the respective nominal value of V_{CASN}. The following points can be noted:

- The changes of the thresholds after irradiation are clearly more pronounced for increased values of V_{BB}.
- For the PMOS reset pixels (sectors 0, 1 and 3), the threshold curves before and after irradiation differ by an offset, where the threshold after irradiation is observed to be reduced. Considering the different values of spacing between the n-well and the



(a) Sector 0. **(b)** Sector 1.

(c) Sector 2. **(d)** Sector 3.

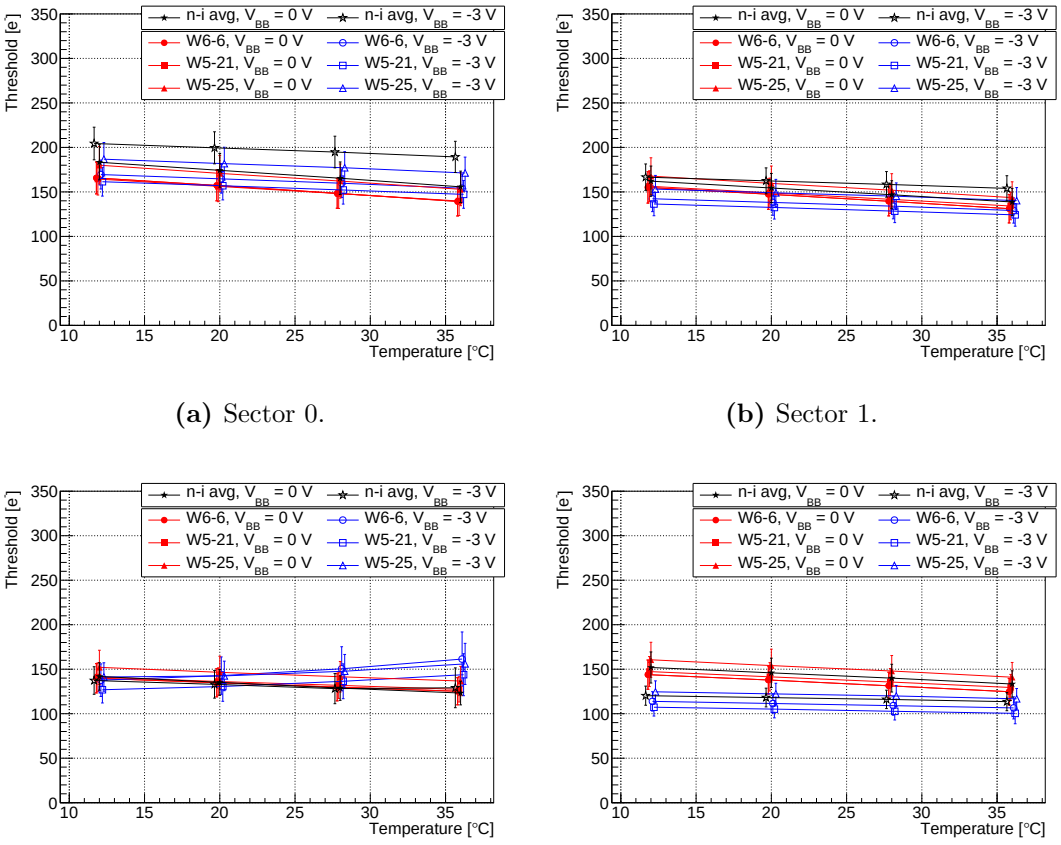
Figure E.4.: Mean threshold, each averaged over three chips, as a function of I_{THR} for the four sectors of pALPIDE-1 before and after irradiation with a fluence of $1 \times 10^{13}\,1\,\mathrm{MeV\,n_{eq}/cm^2}$ at 28 °C for different V_{BB} values at the respective nominal V_{CASN}. The error bars represent the pixel to pixel variation, i.e. the threshold RMS.

surrounding p-well between the sectors, a trend can be observed, that is, the offset increases with decreasing spacing. For sector 3 with the largest spacing, the offset is almost negligible.

For the diode reset pixel (sector 2), the threshold curves before and after irradiation exhibit a different slope, where the curves meet at low I_{THR}.

The threshold results after irradiation as function of temperature are presented in Fig. E.5. For the PMOS reset pixels no significant change in the temperature behaviour can be observed at both presented values of V_{BB}. For the diode reset pixels the situation changes: while for $V_{BB} = 0\,\mathrm{V}$ the temperature dependence is not notably influenced, at $V_{BB} = -3\,\mathrm{V}$ the threshold now clearly inceases with increasing temperature.

Threshold RMS The results for the threshold RMS, i.e. the pixel-to-pixel variation of the threshold after irradiation as function of temperature are presented in Fig. E.6. As for



(a) Sector 0.

(b) Sector 1.

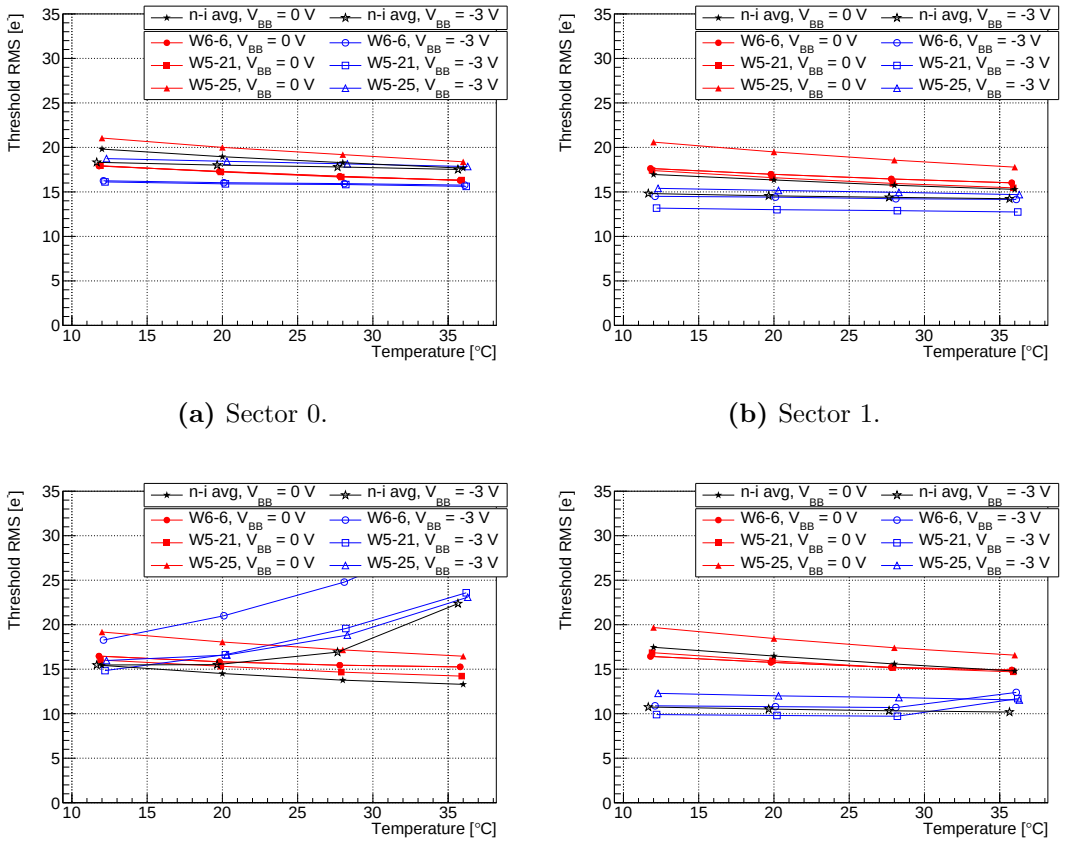
(c) Sector 2.

(d) Sector 3.

Figure E.5.: Threshold as a function of temperature for the four sectors of pALPIDE-1 after irradiation with a fluence of $1 \times 10^{13}\,1\,\mathrm{MeV\,n_{eq}/cm^2}$ at $I_{\mathrm{THR}} = 30\,\mathrm{DAC\,units}$ for different chips and V_{BB} values at nominal V_{CASN} each. The error bars represent the pixel to pixel variation, i.e. the threshold RMS. For reference, also the average values for the non-irradiated chips are shown (black lines).

the threshold itself, for the PMOS reset pixels no significant change in the temperature behaviour can be observed at both presented values of V_{BB}. Also for the diode reset pixels no change in the progression as function of temperature can be observed after irradiation, however, the absolute values are slightly increased.

Temporal noise The results for the temporal noise after irradiation as function of temperature are presented in Fig. E.7. For the PMOS reset pixels, no notable changes of the temperature dependency can be observed. For the same observation applies to the the diode reset pixel at $V_{BB} = 0\,\mathrm{V}$, whereas at $V_{BB} = -3\,\mathrm{V}$ the temporal noise now slightly increases as funciton of temperature. In contrast to the temperature dependence, however, the absolute values increase significantly after irradiation, where for the PMOS reset the increase correlates with the spacing, and accordingly with the pixel input capacitance.



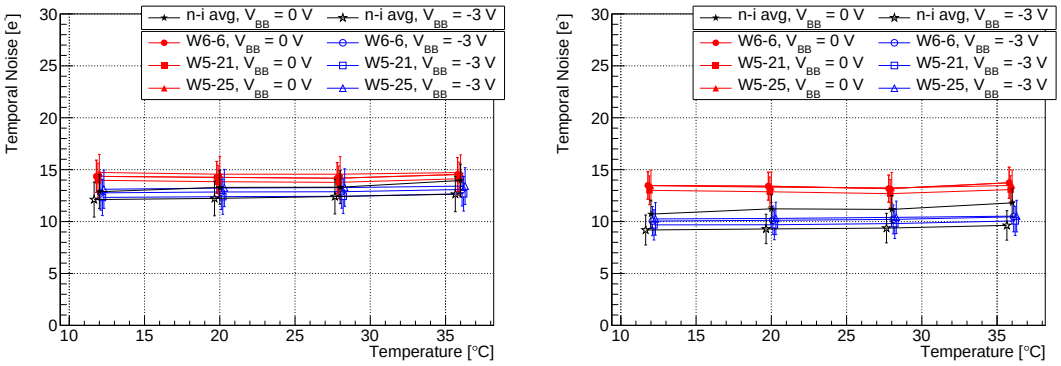
(a) Sector 0. **(b)** Sector 1.

(c) Sector 2. **(d)** Sector 3.

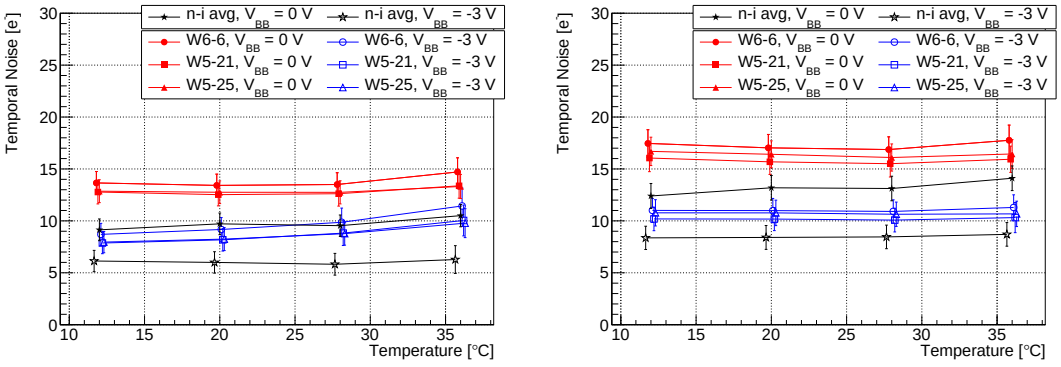
Figure E.6.: Threshold RMS as a function of temperature for the four sectors of pALPIDE-1 after irradiation with a fluence of 1×10^{13} 1 MeV n_{eq}/cm^2 at $I_{THR} = 30$ DAC units for different chips and V_{BB} values at nominal V_{CASN} each. For reference, also the average values for the non-irradiated chips are shown (black lines).

Fake hit rate Fig. E.8 presents an example summary of the results for the fake hit after irradiation as function of temperature for all four sectors of the pALPIDE-1, for three different chips and two V_{BB} values, measured at $I_{THR} = 30$ DAC counts, each at nominal V_{CASN}. The presented data points are obtained after masking the 20 hottest pixels, whereas the error bars represent the values obtained after masking between zero and up to the 100 hottest pixels. For reference, the average values for the non-irradiated chips are shown.
The following points can be noted:

- Masking the same number of pixels, the fake hit rate after irradiation is increased by up to a factor ten, where this factor is almost constant as function of temperature.
- As before irradiation, the chip-to-chip variation after irradiation is about a factor ten when masking the same number of pixels.



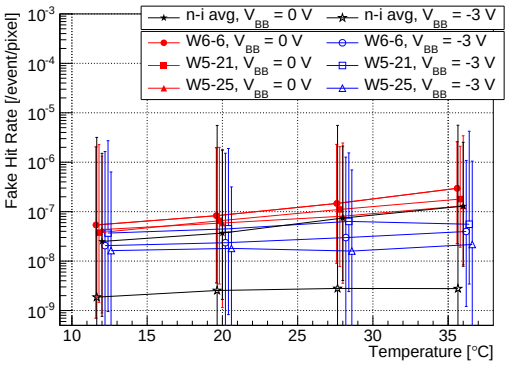
(a) Sector 0. **(b)** Sector 1.



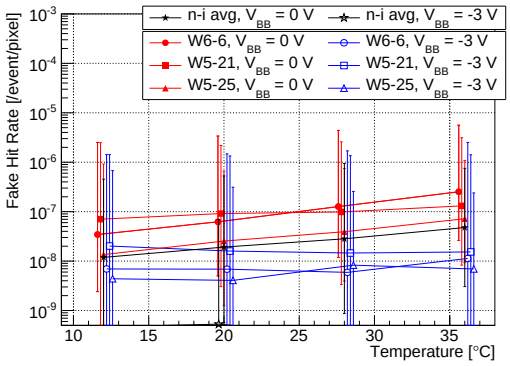
(c) Sector 2. **(d)** Sector 3.

Figure E.7.: Temporal noise as a function of temperature for the four sectors of pALPIDE-1 after irradiation with a fluence of $1 \times 10^{13}\,1\,\mathrm{MeV\,n_{eq}/cm^2}$ at $I_{\mathrm{THR}} = 30\,\mathrm{DAC\,units}$ for different chips and V_{BB} values at nominal V_{CASN} each. The error bars represent the pixel to pixel variation. For reference, also the average values for the non-irradiated chips are shown (black lines).

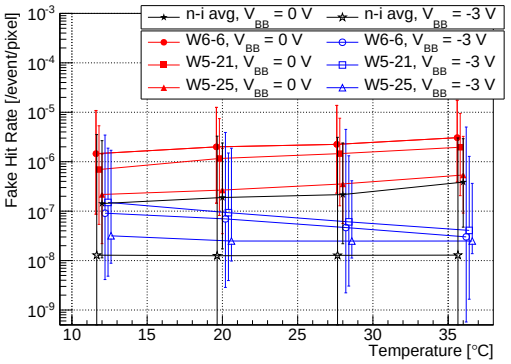
- For $V_{BB} = 0\,\mathrm{V}$ an increase of temperature from 12 °C to 36 °C yields an increase of the fake hit rate of about a factor ten, while for $V_{BB} = -3\,\mathrm{V}$ it stays almost constant. Furthermore, by increasing the additonal reverse bias from 0 V to −3 V, the fake hit rate can be reduced by about a factor ten.
- No significant difference is observed between the different pixel variants for the temperature dependency of the fake hit rate, as similar values can be obtained by masking a few more or less pixels.
- Overall, also after irradiation, most of the chips show a fake hit rate below the required value of 10^{-5}/event/pixel for the case of masking zero pixels, while in the case of masking the 100 hottest pixels it can be reduced to values around 2×10^{-7}/event/pixel and far below.



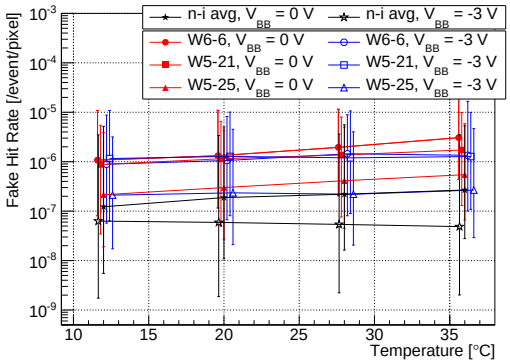
(a) Sector 0: 1 µm spacing, PMOS reset.



(b) Sector 1: 2 µm spacing, PMOS reset.



(c) Sector 2: 2 µm spacing, diode reset.



(d) Sector 3: 4 µm spacing, PMOS reset.

Figure E.8.: Fake hit rate after irradiation as a function of temperature for the four sectors of pALPIDE-1 at $I_{\mathrm{THR}} = 30$ DAC counts for various chips and V_{BB} values, at nominal V_{CASN} each. For reference, also the average values for the non-irradiated chips are shown (black lines). The presented data points are obtained after masking the 20 hottest pixels, whereas the error bars represent the values obtained after masking between zero up to the 100 hottest pixels. The *STROBE_B* width was set to 500 ns.

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G. Curriculum Vitae

Jacobus Willem van Hoorne

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Birthdate/place:	31st January 1986 in Giessenlanden, Netherlands
Citizenship:	Netherlands

Education

2012 – present	PhD candidate at TU Vienna, Austria Topic: *Study and Development of a novel Silicon Pixel Detector for the Upgrade of the ALICE Inner Tracking System*
09/2012 – 08/2015	Participation in the CERN Doctoral Student Program, Geneva, Switzerland
2009 – 2012	Master's program in Technical Physics, TU Vienna, Austria Graduation with highest distinction in June 2012 Title of diploma thesis: *Cherenkov fibers for beam loss monitoring at the CLIC Two Beam Module*
06/2011 – 04/2012	Participation in the CERN Technical Student Program, Geneva, Switzerland
07/2010 – 09/2010	Participation in the HEPHY@CERN Summer Student Program, Geneva, Switzerland
2006 – 2009	Bacherlor's program in Technical Physics, TU Vienna, Austria Graduation with highest distinction in September 2009
2005 – 2006	Master's program in Architecture, Academy of fine Arts Vienna, masterclass of Nasrine Seraji, AA DIPL RIBA
2000 – 2005	HTBLuVA Mödling, Austria, Departement for Civil Engineering Graduation with highest distinction in June 2005

Professional experience and internships

2000 – 2012	Schilfdachdeckermeister A. van Hoorne, Weiden am See, Austria
06/2013 – 07/2003	Internship at Architekt DI Kandelsdorfer, Neusiedl am See, Austria

Teaching experience

2010	Tutor for Statistical Physics at TU Vienna, Austria

Conferences and workshops

05/2014	*The upgrade of the ALICE Inner Tracking System - status of the R&D on monolithic silicon pixel sensors.* Talk at the conference for Technology and Instrumentation in Particle Physics (TIPP) 2014 in Amsterdam, Netherlands
12/2011	*Investigations on optical fibers for beam loss measurements - simulations and measurements.* Talk at the 7th DITANET topical workshop on beam loss monitoring at DESY, Hamburg, Germany

Skills

Languages	- Mother tongue	Dutch
	- Others	German, English (fluent), French (B1)
Computing	- Languages	C, C++, Python, shell scripting
	- Analysis/simulation	ROOT, Matlab, FLUKA
	- Others	several CAD softwares

Honours

2010	Participation in TUtheTop, the high potential program of TU Vienna as group leader of the OMV group
2005	Golden ring of honor from HTBLuVA Mödling for outstanding performance
2005	2. place at the youth innovation award of the federal state of Niederösterreich, Austria

List of publications

As a member of the ALICE collaboration I am co-author of all physics publications since 01/2013. A complete and up to date list can be found on inSPIRE-HEP at:
`http://inspirehep.net/author/profile/J.W.Van.hoorne.1`
The following list consists of selected additional publications that I have contributed to.

2015 L. Musa (for the ALICE collaboration). *Upgrade of the ALICE Silicon Tracker Using CMOS Pixel Sensors.* to be published in JINST (2015). talk presented at TWEPP 2015.

2015 D. Kim et al. *Front end Optimization for the Monolithic Active Pixel Sensor of the ALICE Inner Tracking System Upgrade.* to be published in JINST (2015). talk presented at TWEPP 2015.

2015 C. Gao et al. *A Novel Source-Drain Follower for Monolithic Active Pixel Sensors.* to be published in NIM A (2015). poster presented at HSTD10.

2015 M. Mager (for the ALICE collaboration). *ALPIDE - the Monolithic Active Pixel Sensor for the ALICE ITS upgrade.* to be published in NIM A (2015). talk presented at Elba2015

2015 A. Szczepankiewicz (for the ALICE collaboration). *Readout of the upgraded ALICE ITS.* to be published in NIM A (2015). talk presented at Elba2015

2015 M. Kofarago (for the ALICE collaboration). *The Upgrade of the Inner Tracking System of ALICE.* PoS (VERTEX2015) 009.

2015 P. Yang et al. *Low-power priority Address-Encoder and Reset-Decoder data-Driven readout for Monolithic Active Pixel Sensors for tracker system.* NIM A 785 (2015) 61-69.

2014 P. Yang et al. *MAPS development for the ALICE ITS upgrade.* JINST, Volume 10 (2015) C03030.

2014 M. Keil et al. *Upgrade of the ALICE Inner Tracking System.* JINST, Volume 10 (2015) C03012.

2014 A. Collu (for the ALICE collaboration). *A Monolithic Active Pixel Sensor for the Upgrade of the ALICE ITS.* PoS (TIPP2014) 337.

2014 J. W. van Hoorne (for the ALICE collaboration). *The upgrade of the ALICE Inner Tracking System – Status of the R&D on monolithic silicon pixel sensors.* PoS (TIPP2014) 125.

2014 F. Reidt (for the ALICE collaboration). *Upgrade of the ALICE ITS.* PoS (VERTEX2014) 007.

2014 C. Cavicchioli et al. *Design and characterization of novel monolithic pixel sensors for the ALICE ITS upgrade.* NIM A 765 (2014) 177-182.

2013 L. Musa et al. *Technical Design Report for the Upgrade of the ALICE Inner Tracking System.* J. Phys. G (2014) 087002.

2013 H. Hillemanns et al. *Radiation hardness and detector performance of new 180 nm CMOS MAPS prototype test structures developed for the ALICE Inner Tracking System.* NSS/MIC, 2013 IEEE.

2013 T. Kugathasan et al. *Explorer-0: A Monolithic Pixel Sensor in a* 180 nm *CMOS process with an* 18 µm *thick high resistivity epitaxial layer.* NSS/MIC, 2013 IEEE.

2013 W. Snoeys et al. *Monolithic active pixel sensor development for the upgrade of the ALICE Inner Tracking System.* JINST, Volume 8 (2013) C12041.

2012 C. Irmler, M. Friedl, J. W. van Hoorne and H. Steininger. *Efficient signal conditioning by a FIR filter for analog signal transmission over long lines.* JINST, Volume 7 (2012) C01082.

2010 A. Di Mauro et al. *R&D results on a CsI coated triple thick GEM-based photodetector.* NIM A 639 (2011) 126-129.

27th October 2015