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Characterization and Modeling of Charged Defects in Silicon and 2D Field-Effect Transistors

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Abstract

This work has been conducted at a time when scaling of Si MOSFETs according to Moore's Law is close to its end. Hence, the research focus is shifting from nanoscale Si MOSFETs to next-generation transistors based on 2D materials. Although these technologies are dramatically different from one another, the question of reliability is essential for both types of devices. However, the typical dimensions of modern nanoscale Si MOSFETs are already far below 100 nm, while the channel lengths of next-generation 2D FETs are still in the micrometer range. Hence, in the former case the reliability is dominated by single discrete defects and in the latter case one has to deal with the impact of continuously distributed defects.

In the course of this dissertation we characterize the reliability of both nanoscale Si MOSFETs and next-generation 2D FETs with graphene and molybdenum disulphide (MoS_2) channels.

First we study the impact of charged traps and random dopants on the performance of nanoscale Si MOSFETs. Based on the results of TCAD simulations, we introduce a precise technique which allows for evaluation of the lateral trap position from the experimental data obtained using time-dependent defect spectroscopy. While our method fully accounts for the impact of random dopants, the typical uncertainty is several percents of the channel length.

Next we switch our attention to graphene FETs and analyze their reliability with respect to bias-temperature instabilities (BTI) and hot carrier degradation (HCD). Our analysis shows that the degradation/recovery dynamics of BTI and some HCD mechanisms can be captured using the models previously developed for Si technologies. Also, we show that HCD in graphene FETs can either accelerate or suppress BTI degradation, depending on the bias condition. In some cases this leads to a non-trivial impact on charged trap density and carrier mobility, both of which are correlated to each other.

Finally, we study the reliability of MoS_2 FETs, which are more suitable for applications in digital circuits compared to graphene transistors. While analyzing the hysteresis and BTI in these devices, we demonstrate that our MoS_2 FETs are more stable compared to their previously reported counterparts. Moreover, we show that use of hexagonal boron nitride as a gate insulator significantly improves the reliability of MoS_2 FETs, especially at lower temperatures. Lastly, we introduce the proof of concept for modeling of the reliability characteristics of MoS_2 FETs using advanced simulation software previously developed for Si MOSFETs.

The results obtained for 2D FETs allow for a general understanding of their reliability at the beginning stage of research. However, sooner or later circuit integration of these new devices will request considerable scaling of their dimensions and dramatical improvement of the technology level. As so, reliability of 2D FETs will be also dominated by single defects. Thus, we can expect that our trap location technique developed for nanoscale Si MOSFETs, as well as the described modeling approach, can be applied for next-generation 2D FETs in future.

Zusammenfassung

Gemäß des Moorschen Gesetzes steht die weitere Skalierung von konventionellen Si MOSFETs kurz vor einer fundamentalen Grenze. Der Forschungsschwerpunkt verschiebt sich daher immer weiter in Richtung Transistortechnologien, welche auf 2D Materialen basieren. Obwohl diese Technologien grundlegend verschieden sind, bleibt die Analyse der Zuverlässigkeit beider Bauteile ein essentieller Bestandteil der Forschung. Allerdings ändert sich durch die unterschiedlichen Bauteilabmessungen die Beschreibung der Degradationsprozesse. Während bei modernen Si MOSFETs im Nanometerberich diskrete Defekte das Verhalten dominieren, beeinflusst ein kontinuerliches Defektspektrum die Funktionalitt von 2D FETs mit Kanallängen im Mikrometerbereich.

In diesem Kontext befasst sich die vorliegende Dissertation mit der Charakterisierung der Zuverlässigkeit beider Technologien, state-of-the-art SI MOSFETs sowie Graphene- und Molybdän Disulfid- (MoS_2) FETs.

Im ersten Teil dieser Arbeit analysieren wir den Einfluss diskreter geladender Defekte und zufällig verteilten Dopanden auf das Verhalten von Si MOSFETs im Nanometerbereich. Mit Hilfe von TCAD Simulationen entwicklen wir eine präzise Methode die laterale Position eines Defektes aus TDDS (time-dependent defect spectroscopy) Experimenten zu extrahieren. Durch die Berücksichtigung von random dopants bewegt sich die Unsicherheit dieser Technik im Bereich weniger Prozente der Kanallänge.

Als nächstes richten wir unsere Aufmerksamkeit auf Graphen-FETs und untersuchen deren Zuverlässigkeit bezüglich Bias Temperature Instabilities (BTI) und Hot Carrier Degradation (HCD). Unsere Analyse zeigt, dass das dynamische Verhalten von BTI und HCD grötenteils durch bestehende, Silizium basierte, Modelle korrekt wiedergeben werden kann. Weiteres wird deutlich, dass die Wechselwirkung zwischen HCD und BTI zu einem nicht-trivialen Verhalten führen kann. Abhängig von den Bias Bedingungen kann HCD in Graphen-FETs den Effekt von BTI verstärken oder unterdrücken. In machen Fällen führt dies zu einer komplexen Korrelation zwischen geladener Defektdichte und Ladungsträgermobilität.

Im letzten Kapitel beschäftigen wir uns mit einer zweiten, in digitalen Schaltungen gebräuchlicheren, Art von 2D-FETs, MoS_2-FETs. Bei der Analyse des Hysterese- und BTI-Verhaltens stellt sich heraus dass diese Bauteile stabiler als ihre Graphene Pendants sind. Darüber hinaus zeigen wir dass der Einsatz von hexagonalem Bornitrid als Gateisolator die Zuverlässigkeit von MoS_2-FETs maßgeblich verbessert, speziell bei niedrigen Temperaturen. Mittels modernen Simulationssoftware, entwickelt fr Si MOSFETs, erbringen wir schließlich den positiven Machbarkeitsbeweis MoS_2-FETs hinsichtlich ihrer Zuverlässigkeit zu modellieren.

Die Resultate dieser Arbeit erlauben ein allgemeines Verständnis und ersten Einblick in das Degradationsverhalten von 2D FETs. Um diese Strukturen allerdings in bestehende Schaltungen zu integrieren muss sowohl die Skalierung der Bauteile als auch die Technologie drastisch verbessert werden. Dadurch wird, analog zu modernen Si MOSFETs, der Einfluss von einzelnen Defekten die Funktionalität dominieren. Es ist daher zu erwarten dass sowohl unsere Methode zur Bestimmung der lateralen Defektposition als auch die vorgestellten Modelle bei zukünftigen 2D Technologien zum Einsatz kommen.

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> The work of the individual still remains the spark that moves mankind ahead even more than teamwork
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> Igor Sikorsky

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Contents

1 Introduction

Since the beginning of mass production of silicon (Si) metal-oxide-semiconductor field-effect transistors (MOSFETs), the dimensions of these devices have been continuously scaling according to Moore's Law. Hence, already in the nineties the typical channel lengths reached sub-100 nm range, which opened a new era of nanoscale MOSFETs. Their integration into the digital and analog circuits allowed for a significant miniaturization of the final products of the modern microelectronics industry. However, the probability of functional failure of these devices is larger, since scaling has made the impact of single defects on the channel electrostatics more crucial. Therefore, investigation of device reliability has become essential. The main ingredients of any reliability study of modern nanoscale MOSFETs are experimental characterization and modeling of charging/discharging of individual defects, both of which typically lead to a drift in the device characteristics. However, investigation of reliability is not possible without accounting for device-to-device variability, which is also very important in scaled devices. In this context, the first part of this work deals with modeling of the impact of the position of single defects on the reliability of nanoscale MOSFETs in the presence of randomly distributed discrete dopants, which are considered one of the main sources of variability. Comparison of the simulation results with the experimental data will allow for the derivation of a technique suitable for the evaluation of the lateral positions of these single defects.

Although the International Technology Roadmap for Semiconductors (ITRS)[84] requires further scaling of modern MOSFETs down to 5 nm channel lengths, simultaneous achievement of high transistor performance targets with these devices is extremely complicated. Therefore, in the meantime the device research community has a clear understanding that scaling of conventional Si MOSFETs according to Moore's Law is close to its end. Extension of these limits requires switching of attention to principally new transistor technologies, which could fulfill the requirements on miniaturization and high device performance simultaneously. A very interesting approach is the implementation of new two-dimensional (2D) semiconductors as channel materials for next-generation transistors. This idea has been intensively developed since 2004, when the electric field effect in high-mobility graphene was discovered by K. Novoselov and A. Geim[133]. The first practical step in this direction was taken in 2007, when the group of M. Lemme reported the first graphene field-effect device[108]. This triggered the introduction of numerous next-generation 2D FETs. However, although within the next few years a number of other successful attempts at fabricating graphene FETs were undertaken, it has been clear since the beginning that graphene devices are only suitable for integration into analog circuits. The reason for this is the lack of a bandgap in graphene, which does not allow for the high on/off ratio necessary for digital circuits to be reached. Hence, research attention has shifted to other 2D semiconductors with sizable bandgap allowing for the limitations of graphene to be overcome. The most widely used is molybdenum disulphide (MoS_2), which was shown to be suitable for use as a channel material in 2011, when the first MoS_2 FET was reported by A. Kis and colleagues[141]. Subsequent studies have shown that graphene FETs can be outperformed by MoS_2 devices with respect to transconductance and on current value, despite significantly smaller mobility. However, the level of fabrication technology of next-generation 2D FETs is obviously below the standards for Si technologies. Hence, contrary to modern nanoscale Si

MOSFETs, the typical channel length of both graphene and MoS_2 FETs are in the micrometer range. While the characterization of reliability of these devices is extremely important, the impact of single defects on their performance is not yet the most crucial issue (as it was for Si technologies in the seventies and eighties). Therefore, the building of methodology for a reliability study for these new devices has to be started from scratch, while also dealing with the issues of Si MOSFETs that have been known for decades. Thus, in the second part of this work a detailed analysis of the reliability of both graphene and MoS_2 FETs will be performed. A majority of attention will be paid to experimental analysis of the impact of bias-temperature instabilities (BTI) and hot-carrier degradation (HCD) on the performance of next-generation 2D FETs. However, the experimental results will be supported by simulations.

The period of time in which this dissertation has been written falls exactly within the overlap between the era of ultra-scaled Si MOSFETs and the era of next-generation 2D FETs. While characterization of reliability is of key importance for both types of devices, in the former case one has to deal with the impact of single defects, while in the latter continuously distributed multiple defects are in the meantime more crucial. Therefore, both these questions will be touched upon in the course of this work.

The structure of this dissertation is organized as follows. The first three chapters contain a description of the theoretical background and an overview of previous research. Inclusion of such information is necessary to understand the results obtained by the author. Namely, Chapter 2 presents a brief description of the main approaches used for the simulation of the charged carrier transport through the channel of modern nanoscale Si MOSFETs in the presence of individual defects and randomly distributed discrete dopants. Basic information about the Boltzman transport equation (BTE), drift diffusion (DD) and density gradient (DG) models will be provided. In addition, the main principles of the time-dependent defect spectroscopy (TDDS), which is now used as the main experimental technique to characterize single defects in nanoscale MOSFETs, will be discussed. Chapter 3 provides an overview of the main reliability issues in modern Si MOSFETs, followed by a description of the analytical models used for their modeling. Most essential in the context of this work are the universal relaxation model, the capture/emission time (CET) map model, and the four-state non-radiative multiphonon (NMP) model, all of which are discussed in detail. The main idea is that although the described models have been previously developed for Si MOSFETs, they will be useful for understanding of BTI and HCD in next-generation 2D technologies. In Chapter 4 a brief review of 2D materials (graphene, MoS_2, hexagonal boron nitride [hBN] and others) and their properties will be provided. This will be accompanied by an overview of previous research on graphene and MoS_2 FETs and their reliability. The next three chapters describe the results obtained within this work. Chapter 5 is devoted to characterization and modeling of single defects in modern nanoscale Si MOSFETs. The simulation results obtained for similar devices with a single trap and a number of configurations of randomly distributed discrete dopants are discussed. Based on comparison of these results with experimental data obtained using TDDS, a technique allowing for the evaluation of the lateral trap position with a high accuracy is derived. Chapter 6 includes a detailed analysis of BTI and HCD in graphene FETs. The experimentally measured stress/recovery data for both issues are shown to agree with universal relaxation and CET map models developed for Si technologies. Moreover, a detailed classification of HCD mechanisms in graphene FETs is provided, in particular with the help of the adjusted DD model. The results on hysteresis stability and BTI analysis in MoS_2 FETs with SiO_2 and hBN insulators can be found in Chapter 7. While BTI results are accompanied by modeling using the universal relaxation model, it is also shown that the reliability characteristics of MoS_2 FETs can be reproduced using our simulator Minimos-NT employing the four-state NMP model. Finally, the main results are summarized.

2 Charged Carrier Transport and Single Defects in Si FETs

The first part of this work will be devoted to the characterization of preexisting defects in Silicon metal-oxide-semiconductor field-effect transistors (MOSFETs), and evaluation of their lateral positions. This study requires both modeling of charged carrier transport through the device channel in the presence of random dopants and single defects, and experimental analysis. Information on main simulation and experimental techniques used will be provided within this chapter.

2.1 Charged Carrier Transport: General Equations and Models

2.1.1 Single-Particle Schroedinger Equation

The channel of modern Silicon MOSFETs typically presents a multi-particle system with randomly distributed dopants and defects. This system can be described by the time-dependent Schroedinger equation, which generally reads [14]

$$\begin{aligned}\Big(-\frac{\hbar^2}{2m_0}\nabla^2_{\boldsymbol{r}} - \frac{\hbar^2}{2M_0}\nabla^2_{\boldsymbol{R}} + \boldsymbol{H}_{\mathrm{ee}}(\boldsymbol{r})\\ + \boldsymbol{H}_{\mathrm{ii}}(\boldsymbol{R}) + \boldsymbol{H}_{\mathrm{ei}}(\boldsymbol{r},\boldsymbol{R}) + \ldots\Big)\boldsymbol{\Psi}(\boldsymbol{r},\boldsymbol{R}) = i\hbar\frac{\partial\boldsymbol{\Psi}(\boldsymbol{r},\boldsymbol{R})}{\partial t},\end{aligned} \tag{2.1}$$

where m_0 and M_0 are the masses of electrons and ions, respectively. While $\boldsymbol{r}$ expresses the positions of electrons and $\boldsymbol{R}$ the positions of ions, $\boldsymbol{H}_{\mathrm{ee}}(\boldsymbol{r})$, $\boldsymbol{H}_{\mathrm{ii}}(\boldsymbol{R})$ and $\boldsymbol{H}_{\mathrm{ei}}(\boldsymbol{r},\boldsymbol{R})$ denote electron-electron scattering and the interactions of ions with other ions and electrons, respectively.

However, the solution of the multi-particle Equation 2.1 is extremely complicated. Therefore, by separation of wave functions for electrons and holes, and using Hartree-Fock and Slater approximations [119], it is typically transferred into a single-particle Schroedinger equation for electrons

$$\Big(-\frac{\hbar^2}{2m_0}\nabla^2_x + V(\boldsymbol{x}) + V_{\mathrm{ext}}(\boldsymbol{x},t) + H_{\mathrm{sc}}(\boldsymbol{x},\boldsymbol{k})\Big)\Psi(\boldsymbol{x},\boldsymbol{k},t) = i\hbar\frac{\partial\Psi(\boldsymbol{x},\boldsymbol{k},t)}{\partial t}, \tag{2.2}$$

where $\Psi(\boldsymbol{x},\boldsymbol{k},t)$ is the wave function of a single electron, $V_{\mathrm{ext}}(\boldsymbol{x},t)$ is the external electrostatic potential and $H_{\mathrm{sc}}(\boldsymbol{x},\boldsymbol{k})$ is a scattering Hamilton operator which combines other interactions between different particles. The quantities $\boldsymbol{k}$ and $V(\boldsymbol{x})$ denote the reciprocal wave vector and ionic potential [119], respectively. Furthermore, another Hamilton operator

$$H_{\mathrm{m}}(-i\nabla_x) = -\frac{\hbar^2}{2m_0}\nabla^2_x + V(x) \tag{2.3}$$

is introduced, where

$$H_{\mathrm{m}}(-i\nabla_x)\Psi(\boldsymbol{x},\boldsymbol{k}) = H_{\mathrm{m}}(\boldsymbol{k})\Psi(\boldsymbol{x},\boldsymbol{k}) \tag{2.4}$$

and $H_{\mathrm{m}}(\boldsymbol{k})$ presents a dispersion relation in the m-th band, which allows for the inclusion of the full band structure of the semiconductor (i.e. all conduction and valence bands) [119]. This dispersion relation is given by the type of channel material [14].

2.1.2 Boltzmann Transport Equation and Method of Moments

The single-particle Schroedinger Equation 2.2 can be used to derive the Boltzmann Transport Equation (BTE), which describes electron transport in a semiconductor. While the detailed step-by-step derivation of BTE can be found in [119, 14], in general form this equation reads [14]

$$\frac{\partial f^{\mathrm{m}}(\boldsymbol{x},\boldsymbol{k},t)}{\partial t} + L\{f^{\mathrm{m}}(\boldsymbol{x},\boldsymbol{k},t)\} = Q\{f^{\mathrm{m}}(\boldsymbol{x},\boldsymbol{k},t)\}, \tag{2.5}$$

where $f^{\mathrm{m}}(\boldsymbol{x},\boldsymbol{k},t)$ is the carrier distribution function in the m-th band, $Q\{f^{\mathrm{m}}(\boldsymbol{x},\boldsymbol{k},t)\}$ is the operator describing scattering processes from a statistical point of view and $L\{f^{\mathrm{m}}(\boldsymbol{x},\boldsymbol{k},t)\}$ is a free-streaming operator given as

$$L\{f^{\mathrm{m}}(\boldsymbol{x},\boldsymbol{k},t)\} = v_{\mathrm{gr}}^{\mathrm{m}}(\boldsymbol{x},\boldsymbol{k}) \cdot \nabla_x f^{\mathrm{m}}(\boldsymbol{x},\boldsymbol{k},t) - \frac{\boldsymbol{F}(\boldsymbol{x},t)}{\hbar} \cdot \nabla_k f^{\mathrm{m}}(\boldsymbol{x},\boldsymbol{k},t). \tag{2.6}$$

Here $v_{\mathrm{gr}}^{\mathrm{m}}(\boldsymbol{x},\boldsymbol{k})$ is the group velocity in the m-th band and $\boldsymbol{F}(\boldsymbol{x},t)$ is an external force given by the gradient of $V_{\mathrm{ext}}(\boldsymbol{x},t)$ from Equation 2.2.

Thus, BTE describes both electron scattering by $Q\{f^{\mathrm{m}}(\boldsymbol{x},\boldsymbol{k},t)\}$ and free transport of electrons in between scattering events by $L\{f^{\mathrm{m}}(\boldsymbol{x},\boldsymbol{k},t)\}$, and can be written for any of the conduction or valence bands. A self-consistent solution of the BTE for electrons and holes coupled with the Poisson equation allows for a detailed analysis of charged carrier transport through the MOSFET channel. However, discretization of the original BTE 2.5 leads to a multidimensional system of equations which requires significant computational resources. Therefore, most typically used carrier transport models are obtained by simplification of this system. This can be done using the method of moments [162]. This method denotes j^{th}-order moments of the carrier distribution function $f(\boldsymbol{x},\boldsymbol{k},t)$ as

$$\langle \chi_j \rangle = \int \chi_j f(\boldsymbol{x},\, \boldsymbol{k},\, t) d^3k \tag{2.7}$$

with χ_j being the j^{th}-order weight function. Hence, using $\chi_1 = 1$ leads to the first moment of the distribution function, which is either electron or hole concentration (n and p, respectively). The second moment is obtained by using $\chi_2 = \boldsymbol{k}$ and denotes the average drift velocity of carriers $\langle v_{\mathrm{n}} \rangle = \boldsymbol{J}_{\mathrm{n}}/q$ or $\langle v_{\mathrm{p}} \rangle = \boldsymbol{J}_{\mathrm{p}}/q$, with $\boldsymbol{J}_{\mathrm{n}}$ and $\boldsymbol{J}_{\mathrm{p}}$ being the current density for electrons and holes, respectively. Weighting of the distribution function with $\chi_3 = E(\boldsymbol{k})$ leads to the third moment, which presents the average energy for electrons ($\langle E_{\mathrm{n}} \rangle$) or holes ($\langle E_{\mathrm{p}} \rangle$). Although the higher order moments can be obtained in a similar manner, these first three are typically enough for the derivation of the most widely used carrier transport models.

2.1.3 Drift-Diffusion Model

The drift-diffusion (DD) model is one of the carrier transport models that can be derived from BTE using the method of moments. The main equations of the DD model are the continuity equations for electrons and holes

$$\nabla \boldsymbol{J}_{\mathrm{n}} = q\Big(R + \frac{\partial n}{\partial t}\Big), \tag{2.8}$$

$$\nabla \boldsymbol{J}_{\mathrm{p}} = -q\Big(R + \frac{\partial p}{\partial t}\Big), \tag{2.9}$$

which present the first two moments of the BTE, and the Poisson equation

$$\nabla(\varepsilon(\boldsymbol{x})\nabla\psi) = q(n - p + C). \tag{2.10}$$

Here R is the recombination rate, ε is the dielectric constant and C denotes the concentration of fixed charges. The unknown quantities are the carrier concentrations n and p and the electrostatic potential ψ, while the electron and hole current densities are given by

$$\boldsymbol{J}_{\mathrm{n}} = qn\mu_n F + qD_n\nabla n, \tag{2.11}$$

$$\boldsymbol{J}_{\mathrm{p}} = qp\mu_p F - qD_p\nabla p, \tag{2.12}$$

where the drift term is associated with the electric field F and the diffusion term is given by the concentration gradient. μ_{n}, μ_{p} and D_{n}, D_{p} are the electron and hole mobilities and diffusion coefficients, respectively.

Since the DD model incorporates only the first two moments of the BTE, it can not capture energy transport. Nevertheless, the self-consistent solution of equations 2.8- 2.10 allows for a reliable description of charged carrier transport through the device channel at reasonable computational costs. Therefore, the DD model is typically employed to reproduce the device electrostatics for its implementation into reliability models, especially when studying bias-temperature instabilities [60, 15].

The DD model is incorporated into our deterministic TCAD simulator Minimos-NT [83], which will be used when performing simulations of the output characteristics of Si MOSFETs and when studying the impact of single defects on their performance. Also, an attempt to extend the DD model for the case of graphene FETs will be made within this work, although without implementation into professional simulation software.

It should be noted that some more complex models, e.g. the hydrodynamic transport model employing three moments of the BTE, are also incorporated into Minimos-NT [83]. However, their consideration is beyond the scope of this work.

2.2 Modeling of Random Dopants and Discrete Traps

The Poisson equation 2.10 generally accounts for all charged particles in the device channel by regarding their macroscopic densities (e.g. the density of ionized impurities is described by their concentration C). However, this approach is only applicable for Si MOSFETs with large enough channel lengths. At the same time, for nanoscale MOSFETs with channel lengths of around 100 nm and smaller, the amount of charged impurities can be small [9, 11, 153]. Hence, one has to deal with randomly distributed discrete dopants [15], which for brevity can be denoted as "random dopants". They can originate, for example, from doping of semiconductor substrates using ion implantation.

In nanoscale devices, random dopants can severely impact the channel electrostatics, which are one of the main sources of device-to-device variability [9]. Namely, they can perturb the channel potential [9] and form a percolation path for the current[15]. This leads to different values of the threshold voltage V_{th} for nominally identical devices with different configurations of random dopants. Hence, accounting for the impact of random dopants on the device electrostatics is extremely important when simulating charge carrier transport through the channel. As will

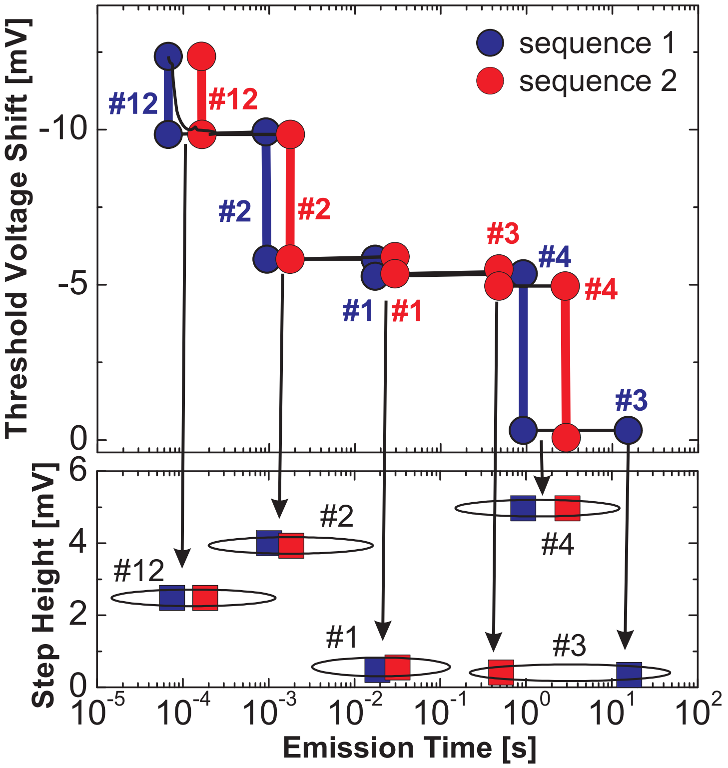

Figure 2.1: Two typical threshold voltage shift recovery traces measured using TDDS on the same nanoscale p-MOSFET (reproduced from [67]) contain discrete steps (top). They can be attributed to discharging of single defects. The extracted step heights and emission times form a spectral map containing fingerprints of each individual defect (bottom).

become clear from the analysis below, this is the key figure of merit for the characterization of preexisting defects in nanoscale MOSFETs and evaluation of their lateral positions.

Placement of random dopants into the device channel is typically done by discretizing the macroscopic channel doping concentrations (N_D for n-MOSFET or N_A for p-MOSFET) and using the Monte Carlo algorithm [187] to calculate the position of each particular dopant (details can be found in [14]). However, the accuracy of this method is strongly dependent on the mesh spacing of the simulation grid used. Nevertheless, the authors of [9, 11] have shown that a spacing smaller than 1 nm is typically sufficient to capture the magnitude of device-to-device variability in nanoscale MOSFETs.

A randomly placed dopant presents a point charge with the Coulomb potential, which can be screened by numerous carriers having discrete energies [14]. Hence, a classical or semi-classical description would lead to a failure of numerical solution for the Poisson equation. Therefore, modeling of random dopants using a semi-classical simulator incorporating the DD model typically requires accounting for a quantum correction of the Coulomb potential. The most suitable methodology for this is the density gradient (DG) model [9, 11, 184, 19], which allows to obtain quantum corrected drift-diffusion equations (see [14]).

Another source of device-to-device variability in nanoscale MOSFETs is associated with charged traps [121], which also have a discrete distribution along the channel. Their electrostatical interactions with random dopants can lead to variations of the threshold voltage, while the proximity of a charged trap to the dominating percolation path formed by random dopants strongly impacts the drain current [15]. In the course of this work we perform our simulations either for perturbed device with a single discrete trap placed right at the channel/oxide interface or for unperturbed device.

2.3 Characterization of Preexisting Defects Using Time-Dependent Defect Spectroscopy

The channel of a modern nanoscale MOSFET contains a number of preexisting defects introduced during fabrication. Charging/discharging of these defects may significantly impact device reliability and also lead to a time-dependent variability [167]. Hence, characterization of preexisting defects is extremely important.

Time-dependent defect spectroscopy (TDDS) [67, 68, 181] is one of the most versatile methods for characterization of individual defects in nanoscale MOSFETs. The typical TDDS experiment includes charging of traps at a higher gate voltage followed by their discharging at a lower voltage. During this the subsequent charge-emission transient is recorded. Multiple repetitions of these charging/discharging sequences allow one to obtain good statistics on capture and emission times for each individual trap.

A typical evolution of the threshold voltage after charging of preexisting defects using TDDS is shown in Figure 2.1. Clearly, the recovery consists of a number of discrete steps, while each of these steps is attributed to discharging of an individual trap. Since this behaviour is reproducible when using subsequent TDDS sequences on the same device, one can extract the corresponding step heights and emission times and build a spectral map (Figure 2.1(bottom))[67]. This spectral map contains unique fingerprints for each of the defects in the device channel. Also, repetition of TDDS measurements at different drain voltages allows for the extraction of $\Delta V_{\mathrm{th}}(V_{\mathrm{d}})$ characteristics, which will be analyzed within this work. In particular, we will clearly show that the dependence of step height on the drain bias contains the full information on the lateral defect position.

3 Main Reliability Issues in Si MOSFETs and Their Modeling

A significant part of this work will be devoted to reliability studies of next-generation 2D FETs. Since so far no reliability theory has been developed for these new technologies, we will start by using general models previously developed for Si MOSFETs. Hence, in this chapter a brief background of the main reliability issues in Si technologies and their modeling will be provided.

3.1 Overview of Reliability Issues

Understanding of reliability models requires basic knowledge on the main reliability issues observable in modern Si MOSFETs. The related information will be provided in this section.

3.1.1 Negative Bias-Temperature Instability

Negative bias-temperature instability (NBTI) is one of the most crucial degradation mechanisms observed in modern CMOS devices. Pure NBTI degradation typically occurs if the device is examined at high enough temperatures and if considerable negative gate voltages are applied when the source and drain terminals are grounded. While leading to a shift of the threshold voltage and variation of the subthreshold swing, NBTI may significantly impact device performance. If the device operates in extrem working conditions[1], the impact of NBTI can be very strong. However, when the stress is removed, the device parameters tend to return back to their initial values, i.e. NBTI degradation is recoverable. During the last decade investigation of NBTI has attracted a considerable amount of attention [89, 59, 80, 60, 65, 66, 79, 76, 7, 58]. One of the main reasons for this is the agressive scaling of the devices, which requires the use of thinner gate oxides, thereby leading to larger oxide fields.

The impact of NBTI on the device characteristics is associated with the trapping of carriers by oxide traps [173, 63] (e.g. E' centers and switching oxide traps), which can exchange charges with the channel, and interface states [61] (e.g. P_b centers). The positive charge variation associated with oxide traps is

$$\Delta Q_\mathrm{ox}(t) = q \int\int \Delta D_\mathrm{ox}(x,\, E_\mathrm{t},\, t) f_\mathrm{ox}(x,\, E_\mathrm{t},\, t)(1 - x/d_\mathrm{ox}) dx\; dE_\mathrm{t}, \tag{3.1}$$

where $f_\mathrm{ox}(x, E_\mathrm{t}, t)$ is the occupancy of oxide traps, $\Delta D_\mathrm{ox}(x, E_\mathrm{t}, t)$ is the density of states in the oxide and d_ox is the oxide thickness. Since oxide traps are located in the oxide bulk and have larger time constants, their occupancy can not follow the Fermi level. Conversely, the charging and discharging of interface states is very fast. Hence, the captured variation of positive charge

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[1] The typical operation ranges of modern MOSFETs are the temperatures between 0 and 200 °C and gate oxide fields up to 10 MV/cm.

follows the Fermi level E_F and can be given by

$$\Delta Q_\mathrm{it}(t) = q \int \Delta D_\mathrm{it}(E_\mathrm{t},\, t) f_\mathrm{it}(E_\mathrm{F},\, E_\mathrm{t},\, t) dE_\mathrm{t}, \tag{3.2}$$

where $f_\mathrm{it}(E_\mathrm{F}, E_\mathrm{t}, t)$ is the occupancy of interface states and $\Delta D_\mathrm{it}(E_\mathrm{t}, t)$ the time-dependent density.

The strongest impact of NBTI is observed for p-MOSFETs, which typically operate at negative gate voltages. However, some NBTI degradation, although less significant, can be observed for n-MOSFETs [34, 80] (in that case negative gate voltage corresponds to the accumulation region).

3.1.2 Positive Bias-Temperature Instability

Positive bias-temperature instability (PBTI) is a counterpart of NBTI which occurs at positive gate voltages. Although this degradation issue is expected to impact n-MOSFETs, it has already been shown in [34, 80] that for SiON devices threshold voltage shifts induced by PBTI in n-MOSFETs can be several orders of magnitude smaller than NBTI shifts in p-MOSFETs. Moreover, they are even smaller than PBTI shifts in p-MOSFETs, which correspond to accumulation stress voltage and hence are not of any practical interest. Therefore, investigation of PBTI in Si MOSFETs with SiON insulators is much less intensive compared to NBTI studies. However, PBTI is often reported to be a serious reliability issue in Si MOSFETs with high-k gate insulators[75, 175]. Furthermore, it will be shown that this degradation issue can be very crucial in next-generation 2D FETs.

3.1.3 Hot-Carrier Degradation

Hot-carrier degradation (HCD) is a reliability issue which takes place if a non-zero voltage is applied at the drain. Since most device operation conditions assume some voltage applied at the gate, HCD typically occurs in conjuction with NBTI or PBTI [1].

HCD is associated with defects situated closely to the channel/oxide interface and becomes more pronounced for larger drain voltages. During device operation this interface is bombarded by highly-energetic (i.e. “hot”) carriers, which leads to a rupture of hydrogene (Si-H) bonds and the formation of dangling bonds, i.e. interface states [1, 172, 171]. These interface states are inhomogeneously distributed along the channel with a maximum density in the proximity of the drain [171, 16]. The latter occurs because the electric field near the drain is largest, making carrier energies higher.

Trapping of carriers by interface states created by HCD leads to a shift of the threshold voltage. On the other hand side, scattering of carriers on charged interface states reduces transconductance and mobility. However, contrary to NBTI and PBTI, HCD in Si MOSFETs is typically non-recoverable, since only a strong permanent component associated with a number of dangling bonds is present.[2]

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[2] Some recent papers (e.g. [194]) show that HCD in Si MOSFETs tends to recover at higher temperatures. However, the underlying physical mechanisms require more detailed understanding.

3.1.4 Other Reliability Issues

Other reliability issues which are typically observed in Si MOSFETs are time-dependent dielectric breakdown (TDDB), random telegraph noise (RTN) and $1/f$ noise. However, they will not be studied in the course of this work.

TDDB is a degradation mechanism which leads to the failure of the gate dielectric resulting from operation for a long time [155, 156].[3] Obviously, in real device operation conditions, TDDB usually acts in conjuction with BTI and/or HCD.

RTN is observed in extremely scaled devices, where the capture and emission of carriers by individual traps results in a discrete modulation of the drain current at fixed drain or gate voltage. Contributions of multiple traps may lead to a multi-level RTN [78]. However, this is not an issue for large devices with a great number of defects.

$1/f$ noise (or flicker noise) is the counterpart of RTN which is characterized by a continuous spectral density behaving as 1 over frequency ($1/f$) [154, 186]. Contrary to RTN, it can be observed in large area devices.

3.2 Modeling of BTI in Si MOSFETs

In this section we will provide information on general models which are employed to describe BTI degradation/recovery dynamics in Si MOSFETs. In the following chapters these models will be adjusted to characterize the reliability of next-generation 2D FETs.

3.2.1 Universal Relaxation Model

The universal relaxation model [61, 64] has been derived for fitting of NBTI degradation/recovery in Si technologies. In order to distinguish between the degradation during the stress and relaxation phases, the authors of [61] operate with the degradation magnitude accumulated during the stress $S_0(t_\mathrm{s})$ and relaxation magnitude $R_0(t_\mathrm{s}, t_\mathrm{r})$. It is assumed that the relaxation starts as soon as the stress voltage is removed. Hence, the relaxation magnitude is treated as a function of both stress time t_s and relaxation time $t_\mathrm{r} = t - t_\mathrm{s}$.

However, most experimental techniques typically introduce some measurement delay t_M between the end of the stress and the beginning of recovery observation. Since the recovery of NBTI degradation starts faster than microseconds after the BTI stress is removed [146], some fraction of recovery is lost.[4] Hence, one has to operate with $R_\mathrm{M}(t_\mathrm{s}) = R_0(t_\mathrm{s}, t_\mathrm{M})$ and $S_\mathrm{M}(t_\mathrm{s}) = S_0(t_\mathrm{s}, t_\mathrm{M})$ [61] when normalizing the obtained recovery data by the first measurement point. Also, a fractional recovery $r_\mathrm{f}(t_\mathrm{s}, t_\mathrm{r}) = R_0(t_\mathrm{s}, t_\mathrm{r})/R_\mathrm{M}(t_\mathrm{s})$ can be introduced [146, 61].

According to [33], the normalized NBTI recovery obtained using different stress times has the same dependence on the normalized relaxation time $\xi = t_\mathrm{r}/t_\mathrm{s}$. However, the recovery of NBTI is typically not complete, and has some permanent component $P(t_\mathrm{s}) = S_0(t_\mathrm{s}) - R_0(t_\mathrm{s}, 0)$ [143, 62, 58]. Therefore, in the spirit of [33] and taking into account the permanent component, the

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[3] Obviously, a very strong oxide field would lead to an immediate breakdown of the gate dielectric. However, the critical oxide fields are typically known and hence this issue can be avoided.

[4] Below it will be shown that this measurement delay can be very important when characterizing BTI and HCD recovery in graphene FETs.

authors of [61] have introduced a general universal relaxation function, which is given by

$$r(\xi) = \frac{R_0(t_\mathrm{s},\, t_\mathrm{r})}{S_0(t_\mathrm{s}) - P(t_\mathrm{s})} = \frac{R_0(t_\mathrm{s},\, t_\mathrm{r})}{R_0(t_\mathrm{s},\, 0)}. \tag{3.3}$$

After a number of attempts have been made to empirically find the exact form of universal relaxation function [2, 169, 170], in [61] it has been demonstrated that the one suitable for the whole spectra of experimental data available for NBTI is

$$r(\xi) = \frac{1}{1 + B\xi^{\beta}}, \tag{3.4}$$

where B and β are the fitting parameters which have to be adjusted for each particular case[5], while $r_\mathrm{f}(t_\mathrm{s}, t_\mathrm{r}) = r(\xi)/r(\xi_\mathrm{M})$ with $\xi_\mathrm{M} = t_\mathrm{M}/t_\mathrm{s}$. Equation 3.4 can be successfully applied to fit normalized NBTI recovery in Si technologies and also to predict time to failure of the device. However, one should note that in [61] equation 3.4 has been empirically derived assuming a zero permanent component. At the same time, according to equation 3.3, $P(t_\mathrm{s})$ has to be subtracted from the experimental data before analyzing universality.

Another important consequence following from the universal relaxation model is that it allows for the extrapolation of the degradation magnitude at a zero measurement delay. While the degradation magnitude is expected to follow a power law $S_0(t_\mathrm{s}) = At_\mathrm{s}^\mathrm{n}$, in [61] it has been shown that experimentally observed threshold voltage shifts measured at $t = t_\mathrm{M}$ can be expressed by

$$S_\mathrm{M}(t_\mathrm{s}) = S_0(t_\mathrm{s})r(t_\mathrm{s},\, t_\mathrm{M}) = \frac{At_\mathrm{s}^\mathrm{n}}{1 + B\xi_\mathrm{M}^{\beta}}, \tag{3.5}$$

with B and β given by equation 3.4. This expression allows to combine experimental data measured with different delays t_M.

One should note that although the universal relaxation model was originally developed for NBTI in p-MOSFETs, in [64] it was also found to be suitable for capturing both NBTI and PBTI in p- and n-MOSFETs.

3.2.2 Capture/Emission Time Map Model

The capture/emission time (CET) map model [69] assumes that BTI is due to both interface states and oxide traps which can exchange charges with the channel. Each of these defects is assumed to have two stable states, i.e. charged and neutral. The charge exchange events between different states are treated as first-order non-radiative multiphonon (NMP) processes [66] with the capture and emission times given by

$$\tau_\mathrm{c} = \tau_0 \exp\left(\frac{E_\mathrm{c}}{k_\mathrm{B}T}\right), \tag{3.6}$$

$$\tau_\mathrm{e} = \tau_0 \exp\left(\frac{E_\mathrm{e}}{k_\mathrm{B}T}\right). \tag{3.7}$$

Here τ_0 is the effective time constant which weakly depends on BTI stress conditions, and E_c and E_e are capture and emission energy barriers, respectively.

In the CET map model, BTI is assumed to be the collective response of different oxide traps and interface states, while capture and emission are considered as thermally activated processes [66, 147]. Hence, the distributions of E_c and E_e are employed to obtain CET maps using

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[5] According to [61], the typical values for B are within 0.3–3 and for β within 0.15–0.2.

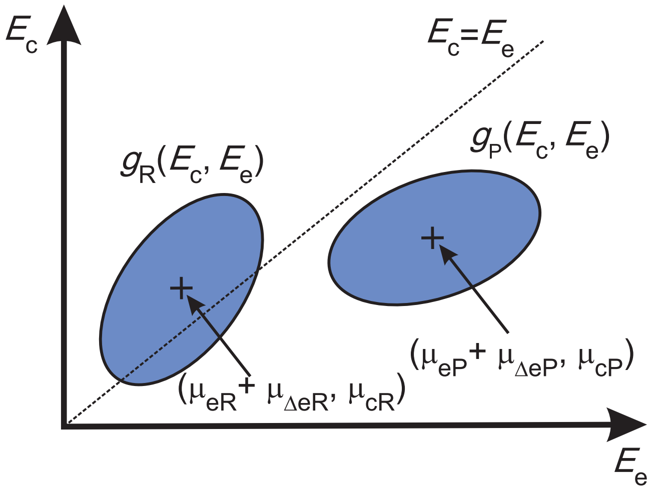

Figure 3.1: Schematic representation of two Gaussian distributions used in the CET map model. One ($g_{\mathrm{R}}(E_{\mathrm{c}}, E_{\mathrm{e}})$) is for the recoverable component and the other ($g_{\mathrm{P}}(E_{\mathrm{c}}, E_{\mathrm{e}})$) is for the permanent component.

equations 3.6–3.7. This allows to avoid direct modeling of widely distributed time constants τ_{c} and τ_{e} and also leads to a built-in temperature dependence of the model. At the same time, the dependence on stress voltage has to be introduced by adjusting model parameters [69].

Initially, the CET maps were extracted numerically by differentiating the obtained recovery traces for threshold voltage shift [147]. The analysis of the results obtained at different temperatures has shown that the capture and emission times are correlated. Namely, a decrease of the emission time at higher temperature leads to a reduced capture time [96] and vice versa. Therefore, it was suggested to express this correlation by linking the activation energies of capture and emission processes as $E_{\mathrm{e}} = E_{\mathrm{c}} + \Delta E_{\mathrm{e}}$, with ΔE_{e} being an uncorrelated part of E_{e}. Since many experimental features of BTI degradation/recovery dynamics could be captured by a Gaussian distribution, the authors of [69] assume that the quantities E_{e}, E_{c} and ΔE_{e} are normally distributed with the mean values μ_{e}, μ_{c} and $\mu_{\Delta\mathrm{e}}$, and standard deviations σ_{e}, σ_{c} and $\sigma_{\Delta\mathrm{e}}$, respectively. This allows for the constructing of a bivariate Gaussian distribution, which is given by

$$g(E_{\mathrm{c}},\, E_{\mathrm{e}}) \;=\; \frac{1}{2\pi\sigma_{\mathrm{c}}\sigma_{\Delta\mathrm{e}}}\exp\Big(-\frac{(E_{\mathrm{c}}-\mu_{\mathrm{c}})^2}{2\sigma_{\mathrm{c}}^2}-\frac{(E_{\mathrm{e}}-(E_{\mathrm{c}}+\mu_{\Delta\mathrm{e}}))^2}{2\sigma_{\Delta\mathrm{e}}^2}\Big). \tag{3.8}$$

Obviously, the marginal distributions $g(E_{\mathrm{e}})$ and $g(E_{\mathrm{c}})$ can be obtained by integrating $g(E_{\mathrm{c}}, E_{\mathrm{e}})$ over E_{c} and E_{e}, respectively. At the same time, the main parameters of $g(E_{\mathrm{e}})$ can be expressed by $\mu_{\mathrm{e}} = \mu_{\mathrm{c}} + \mu_{\Delta\mathrm{e}}$ and $\sigma_{\mathrm{e}}^2 = \sigma_{\mathrm{c}}^2 + \sigma_{\Delta\mathrm{e}}^2$.[6]

However, fitting of the BTI recovery in Si technologies typically requires two bivariate Gaussian distributions given by equation 3.8. As shown in Figure 3.1, one ($g_{\mathrm{R}}(E_{\mathrm{c}}, E_{\mathrm{e}})$) is necessary to express the contribution of the recoverable component and the other is used for the permanent component ($g_{\mathrm{P}}(E_{\mathrm{c}}, E_{\mathrm{e}})$). Typically, the mean values and standard deviations for these two distributions are different, i.e. one has to operate with μ_{cR}, μ_{cP}, σ_{cR}, σ_{cP} and so on.

Taking into account equations 3.6– 3.7, which link the time constants with corresponding activation energies, bivariate Gaussian distributions of E_{c} and E_{e} can be used to calculate the CET map. Obviously, this CET map will present nothing else than a combination of two bivariate

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[6] Below we will see that this correlation between σ_{e} and σ_{c} can be readjusted, which will allow to fit HCD recovery in graphene FETs.

Gaussian distributions for τ_c and τ_e. Hence, the threshold voltage shift can be obtained by integrating these distributions over all defects with $\tau_\mathrm{c} < t_\mathrm{s}$ and $\tau_\mathrm{e} > t_\mathrm{r}$, and reads

$$\Delta V_\mathrm{th} = A_\mathrm{R} \int_{-\infty}^{t_\mathrm{s}} \int_{t_\mathrm{r}}^{\infty} g_\mathrm{R}(\tau_\mathrm{c}, \tau_\mathrm{e}) d\tau_\mathrm{c}\, d\tau_\mathrm{e} + A_\mathrm{P} \int_{-\infty}^{t_\mathrm{s}} \int_{t_\mathrm{r}}^{\infty} g_\mathrm{P}(\tau_\mathrm{c}, \tau_\mathrm{e}) d\tau_\mathrm{c}\, d\tau_\mathrm{e}, \tag{3.9}$$

where A_R and A_P are the fitting parameters which express the magnitudes of the contributions associated with the recoverable and permanent components, respectively.

However, in some cases it is more convenient to integrate the original distributions obtained for the activation energies. Thus the equation 3.9 can be rewritten as

$$\Delta V_\mathrm{th} = A_\mathrm{R} \int_{-\infty}^{a_\mathrm{R}} \int_{b_\mathrm{R}}^{\infty} g_\mathrm{R}(E_\mathrm{c}, E_\mathrm{e}) dE_\mathrm{c}\, dE_\mathrm{e} + A_\mathrm{P} \int_{-\infty}^{a_\mathrm{P}} \int_{b_\mathrm{P}}^{\infty} g_\mathrm{P}(E_\mathrm{c}, E_\mathrm{e}) dE_\mathrm{c}\, dE_\mathrm{e}, \tag{3.10}$$

where $a_\mathrm{R|P}$ and $b_\mathrm{R|P}$ are obtained by recalculating the integration limits using equations 3.6– 3.7 and given by

$$a_\mathrm{R|P} = k_\mathrm{B} T \log\Big(\frac{t_\mathrm{s}}{t_\mathrm{0R|P}}\Big), \tag{3.11}$$

$$b_\mathrm{R|P} = k_\mathrm{B} T \log\Big(\frac{t_\mathrm{r}}{t_\mathrm{0R|P}}\Big). \tag{3.12}$$

In general, integration in equations 3.9– 3.10 has to be done numerically. However, in [69] one can find an analytical approximation.

According to the description above, the CET map model allows for the simulation of $\Delta V_\mathrm{th}(t_\mathrm{r})$ recovery traces for different stress times. Hence, by adjusting the distribution widths and positions (i.e. mean values and standard deviations) one can approximate the measured BTI recovery. Moreover, extrapolation of ΔV_th at zero measurement delay is possible, similarly to the universal relaxation model. However, a significant advance of the CET map model compared to the universal relaxation model is that the former incorporates a temperature dependence, which results in more stable fits.

3.2.3 Four-state NMP Model

The models described above allow for the fitting of a wide range of NBTI and PBTI stress/recovery characteristics. However, they are not always consistent with a number of features which have been extracted from TDDS measurements when characterizing single defects. The most important of them is associated with significant differences in emission times for the defects with similar capture times as well as bias dependence of emission times for some defects. Hence, a more general four-state NMP model was derived in [66].

The four-state NMP model considers interaction of a single carrier with an individual defect. Contrary to the two-state CET map model, this defect is assumed to have four different states. Namely, both neutral and charged configurations of the defect are characterized by one stable and one metastable state. In Figure 3.2 this situation is illustrated for the case of hole trapping. One can see that there are eight different transitions which may occur. While all the transitions between stable and metastable states of one configuration (11', 22', 1'1 and 2'2) are associated with structural relaxation of the defect, transitions between the states with different configurations (12', 2'1, 1'2, 21') correspond to a charge exchange between the defect and the device channel. Also, each of these transitions is described by a certain transition rate k_{ij}. These transition rates are calculated by assuming that the defect time dynamics can be

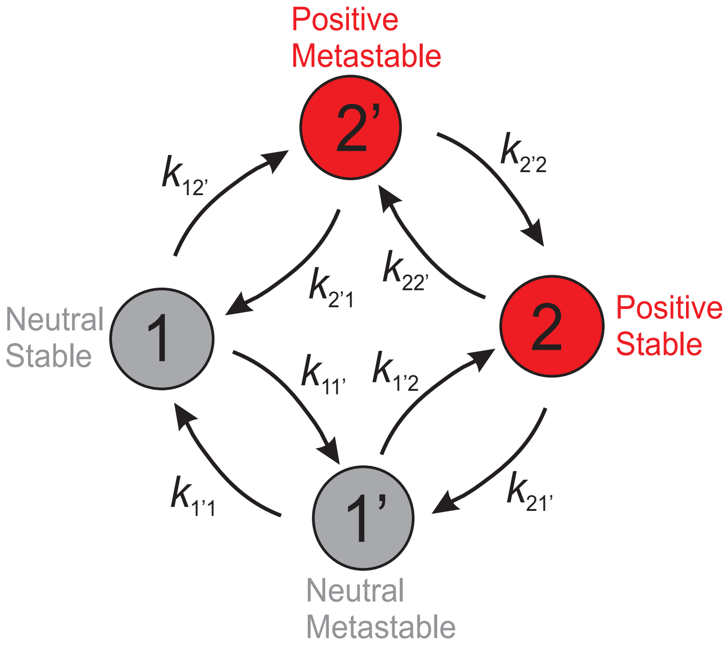

Figure 3.2: Schematic configuration of a single defect assumed in the four-state NMP model (the case of hole trapping is considered). Charging and discharging of the defect occurs through a metastable state. For example, in the positive metastable state 2' the defect can either go through a structural relaxation and become stable (state 2) or emit a hole and return back to neutral stable state 1. In a neutral metastable state 1' it can either capture a hole and become positively charged and stable (state 2) or return back to state 1 by experiencing structural relaxation. The transitions between two stable or two metastable states are disregarded.

described using a continuous-time Markov process $X(t)$ [55], i.e. the defect can only be in one state at a certain point in time. Hence, the probability of finding the defect in a certain state $p_i(t) = P\{X(t) = i\}$ and $\Sigma_i p_i(t) = 1$, where $i = 1, 1', 2, 2'$. Following the theory of Markov processes described in [55], the authors of [66] derived a master equation for all four probabilities $p_i(t)$, which reads

$$\frac{\partial p_i(t)}{\partial t} = \sum_{j=1}^{4} \Big(p_j(t) k_{ji} - p_i(t) k_{ij} \Big). \tag{3.13}$$

The rates for each of the transitions marked in Figure 3.2 can be calculated using NMP theory[7]. It has been found that the transition rates for the transitions between stable states and metastable states of opposite configurations depend on the applied gate voltage and can be given by

$$k_{12'} = \sigma_\mathrm{p}\, v_\mathrm{tp}\, p \exp\Big(-\frac{\varepsilon_{12'}}{k_\mathrm{B} T} \Big), \tag{3.14}$$

$$k_{1'2} = \sigma_\mathrm{p}\, v_\mathrm{tp}\, p \exp\Big(-\frac{\varepsilon_{1'2}}{k_\mathrm{B} T} \Big), \tag{3.15}$$

$$k_{2'1} = \sigma_\mathrm{p}\, v_\mathrm{tp}\, p \exp\Big(-\frac{\varepsilon_{12'}}{k_\mathrm{B} T} \Big) \exp\Big(-\frac{E_\mathrm{T} - E_\mathrm{F} - \varepsilon_{\mathrm{T}2'}}{k_\mathrm{B} T} \Big), \tag{3.16}$$

$$k_{21'} = \sigma_\mathrm{p}\, v_\mathrm{tp}\, p \exp\Big(-\frac{\varepsilon_{1'2}}{k_\mathrm{B} T} \Big) \exp\Big(-\frac{E'_\mathrm{T} - E_\mathrm{F}}{k_\mathrm{B} T} \Big). \tag{3.17}$$

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[7] The details can be found in [56].

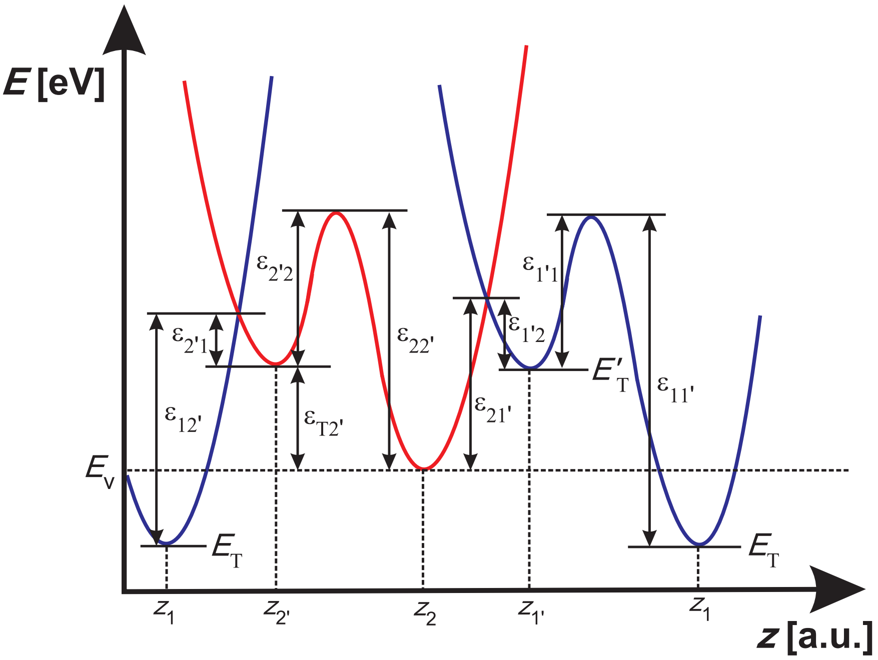

Figure 3.3: Definition of potential barriers used in the four-state NMP model. The adiabatic potentials describing different states are plotted versus a reaction coordinate. The potential describing neutral states (1 and 1') is plotted twice, since the transitions between 1⟷2' and 2⟷1' are characterized by different reaction coordinates.

Furthermore, the transitions between stable and metastable states of one configuration are only activated by temperature and can be written as[8]

$$k_{11'} = v_0 \exp\Big(-\frac{\varepsilon_{11'}}{k_\mathrm{B}T}\Big), \tag{3.18}$$

$$k_{1'1} = v_0 \exp\Big(-\frac{\varepsilon_{1'1}}{k_\mathrm{B}T}\Big), \tag{3.19}$$

$$k_{22'} = v_0 \exp\Big(-\frac{\varepsilon_{22'}}{k_\mathrm{B}T}\Big), \tag{3.20}$$

$$k_{2'2} = v_0 \exp\Big(-\frac{\varepsilon_{2'2}}{k_\mathrm{B}T}\Big). \tag{3.21}$$

Here σ_p is a hole capture cross-section, $v_0 \approx 10^{13}\,\mathrm{s}^{-1}$ is the attempt frequency [56], and p and v_tp are hole concentration and thermal velocity, respectively[9]. The trap levels in neutral stable and metastable states are given by E_T and $E_\mathrm{T}^{'}$, while ε_{ij} are the activation barriers. The configuration of these parameters is shown in Figure 3.3, where the adiabatic potentials for different states of the defect are plotted versus the reaction coordinate z.

The bias dependent barriers $\varepsilon_{12'}$ and $\varepsilon_{1'2}$ are calculated by quadratic expansion of the adiabatic potentials around the minima corresponding to different states (z_i), while the other barriers are obtained as explicit parameters [66]. Then the calculated transition rates can be used to express individual contributions of each defect state to the time constants [66].

Although originally the four-state NMP model was developed to capture the experimental features of single defects observed in TDDS data, its complexity allows for a reliable description

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[8] Similarly to equations 3.6– 3.7.

[9] Trapping of electrons is considered by four-state NMP model in a similar manner.

of a wide spectrum of effects related to the trapping of carriers in the device channel. Hence, PBTI and NBTI can be properly modeled using this approach. Also, a major advantage of the four-state NMP model compared to the CET map model and other previously used approaches is that it can be coupled with DD simulations. This allows its implementation into professional simulation software and makes the four-state NMP model potentially suitable for the simulations of next-generation 2D FETs reliability. Although a number of further efforts still have to be undertaken to adjust this model to 2D channel geometries, in this work the validity of this approach will be illustrated on an example of MoS_2 FETs.

It should be noted that although in Si technologies modeling of HCD requires a separate description[10], we assume that in 2D technologies the absence of dangling bonds makes BTI and HCD more similar. Therefore, according to our current understanding, the models derived for BTI in Si MOSFETs, after some adjusting, should be suitable to capture the dynamics of both BTI and HCD in 2D FETs. Especially valuable in this context is the four-state NMP model.

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[10] The most advanced models currently used are based on the solution of the BTE using a spherical harmonic expansion method [16]. This avoids the time-consuming Monte-Carlo simulations of non-equilibrium distribution functions, and increases the accuracy.

4 Next Generation FETs Based on 2D Materials

A significant portion of this work will be devoted to the characterization of the reliability of next-generation FETs based on 2D materials, which are currently being intensively studied. Therefore, in the course of this chapter a brief review of 2D materials from graphene and beyond, which are suitable for applications in modern micro- and nanoelectronic devices, will be provided. Also, an overview of research on transistors with graphene and MoS_2 and their properties will be provided. This information will be useful for understanding the results described in the following chapters.

4.1 Overview of 2D Materials: Graphene, MoS_2 and Beyond

The term “2D materials” combines a wide range of crystalline materials with exciting electrophysical, magnetic and optical properties [20, 71]. Although the first studies of 2D materials are known since the late sixties [123, 185], an intensive research in this direction has started only in the last decade [195, 22, 99, 182]. The main reason for this is the understanding that sooner or later conventional scaling of Si devices, as known from Moore’s Law, will come to an end. This creates a demand to go beyond conventional CMOS technology by using principally different material systems. In particular, the primary advantage of 2D materials, i.e. the creation of atomically thin channel layers below 1 nm and the stacking of them in versatile ways, has introduced an extremely rich spectrum of new possibilities in modern science and technology [22].

Based on literature reports [133, 21, 3, 130, 12, 18, 22, 32, 35, 49, 126, 190, 135, 87, 138, 51, 88, 91, 99, 182, 20], the major fraction of 2D materials can be classified into three main subclasses. The first and the largest of them is 2D chalcogenides, which include such semiconducting transition metal dichalcogenides (TMDs) as MoS_2, WS_2, WSe_2, $MoSe_2$ [3, 35, 49, 51, 91], metallic dichalcogenides like $NbSe_2$, TaS_2, $NiSe_2$, NbS_2 [22, 35, 49] and layered semiconductors (GaSe, GaTe, InSe, etc)[49]. The second subclass combines graphene-like materials, including graphene itself[133, 12, 18, 88, 28], its derivatives (e.g. wide bandgap fluorographene[130]), boron carbon nitride (BCN)[87], hexagonal boron nitride (hBN) [32, 126, 182] and graphene oxide [138]. Finally, 2D oxides like, e.g. metallic oxides (MoO_3, WO_3, TiO_2, etc)[135], Perovskite-type oxides ($LaNb_2O_7$, $Ca_2Ta_2TiO_{10}$, etc) [135] and hydroxides ($Ni(OH)_2$, $Eu(OH)_2$, etc.) [49] form the third class of 2D materials. Also, research attention has now shifted to principally new 2D materials, like phosphorene [115, 145], silicene [179, 38, 85] and germanene [31].

Since in the course of this work we are dealing with next-generation 2D FETs, those 2D materials suitable for application either as a device channel or gate dielectric are of the largest interest. Therefore, the following detailed description will be mainly devoted to such channel materials as graphene and semiconducting TMDs (mainly MoS_2). Although devices based on phosphorene, silicene and germanene will not be studied in this work, some brief information about these materials will be provided. This should be useful for understanding of the future development

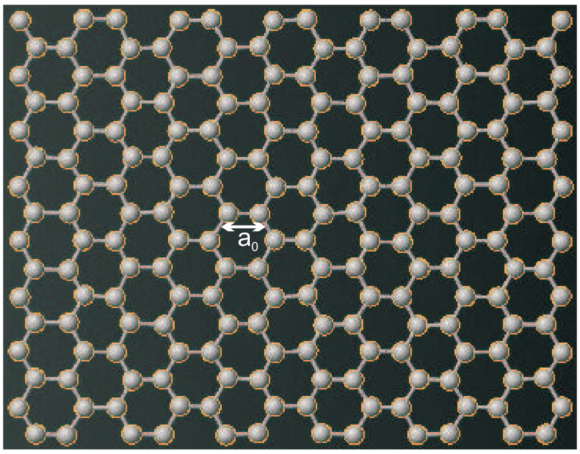

Figure 4.1: 2D hexagonal structure of graphene formed by carbon atoms (reproduced using QuantumWise Virtual Nanolab). The lattice constant $a = \sqrt{3}a_0 = 2.46\,\text{Å}$.

of 2D transistor technologies in general. In addition, the properties of hBN, which is now considered as a next-generation 2D gate insulator [126], will be briefly discussed.

4.1.1 Graphene: Structure and Main Properties

Graphene was already theoretically predicted in 1969 [123], when a detailed analysis of previously published low-energy electron diffraction (LEED) data from single-crystal metallic substrates exposed to hydrocarbons [72, 128] was performed. However, the field effect in highly-stable graphene layers was first reported only in 2004 [133]. Since then graphene has attracted considerable attention due to its unique physical and electrical properties, such as an extremely high room-temperature carrier mobility [50, 133] and high saturation velocity [36].

Graphene is a 2D crystalline allotrope of carbon with a hexagonal lattice structure consisting of a single layer of carbon atoms (Figure 4.1). Each of these atoms has three σ-bonds with its closest neighbours and one π-bond with an orientation outside the 2D plane of graphene. The former is associated with a combination of s, p_x and p_y orbitals of carbon atoms, while the latter is made by the last p_z electron. Thus, sp^2 bonding of carbon atoms, together with their tight packing in hexagonal lattice (distance between two closest neighbours is just $a_0 = 1.42\,\text{Å}$), leads to an extremely high stability of graphene layers. On the other hand side, hybridization of π-bonds leads to the formation of π- and π^*- bands. These bands make free transport of carriers possible, leading to most of the fascinating electrical properties of graphene [28].

The band structure of graphene can be calculated from the solution of the Schroedinger equation using the tight binding approach [180], which takes into account only the interactions between the closest neighbours. The resulting energy dispersion expressed using the x and y components of the wave vector k reads

$$E(k_\text{x}, k_\text{y}) = \pm\gamma\sqrt{1 + 4\cos\Big(\frac{\sqrt{3}ak_\text{y}}{2}\Big)\cos\Big(\frac{ak_\text{x}}{2}\Big) + 4\cos^2\Big(\frac{ak_\text{x}}{2}\Big)}, \tag{4.1}$$

where $\gamma = 3\,\text{eV}$ is a tight binding parameter and $a = \sqrt{3}a_0 = 2.46\,\text{Å}$ is the lattice constant. This energy dispersion is shown in Figure 4.2. Clearly, at the edges of the Brillouin zone the conduction and valence bands touch each other, which means that the bandgap of graphene is equal to zero. The corresponding energy is conventionally known as the Dirac point, or

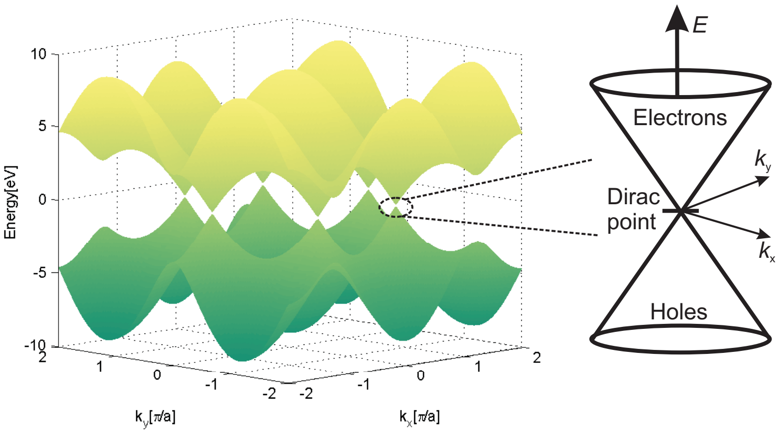

Figure 4.2: Left: Band structure of graphene reproduced based on the dispersion relation 4.1 following from the solution of the Schroedinger equation using the tight binding approach. Right: Schematic representation of the linear energy dispersion (equation 4.2) in the proximity of the Dirac point.

charge neutrality point[132]. When an intrinsic graphene is in equilibrium, its Fermi level is alligned at the Dirac point, which corresponds to the middle of the bandgap in conventional semiconductors.

Near the Dirac point, equation 4.1 can be approximated as

$$E(k) = \pm \hbar v_{\mathrm{f}} k, \tag{4.2}$$

where $\hbar$ is the Planck constant, $v_{\mathrm{f}} = 10^8$ cm/s is the Fermi velocity in graphene [132] and k is the absolute value of the wave vector having the components k_{x} and k_{y}. This linear dispersion law is similar to that of photons. Therefore, electrons and holes in the proximity of the graphene Dirac point have zero effective mass, while their velocity is independent of the energy. This is in contrast to parabolic dispersion laws containing an effective mass, which are typical for most other systems.

While in a conventional 2D electron gas with a parabolic dispersion law the density of states is independent of energy, in the case of graphene the linear dispersion law leads to a linear dependence of the density of states versus energy [6]

$$D(E) = \pm \frac{g_{\mathrm{s}} g_{\mathrm{v}} E}{2\pi \hbar^2 v_{\mathrm{f}}^2}, \tag{4.3}$$

where $g_{\mathrm{s}} = g_{\mathrm{v}} = 2$ are spin and valley degeneration degrees, respectively. Therefore, at zero energy no carriers are present.[1] At the same time, electrons and holes in graphene have to be considered as fermions with zero effective mass, which leads to the following equations for their concentrations n and p, respectively [196]

$$n = \int_0^{\infty} \frac{D(E)}{1 + \exp\left(\frac{E - E_{\mathrm{F}}}{k_{\mathrm{B}} T}\right)} dE, \tag{4.4}$$

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[1] Here the energy is equal to zero at the Dirac point (sometimes referred as E_{cv}), while being larger than zero for electrons (conduction band) and smaller for holes (valence band). Thus in equations 4.1– 4.3 "+" should be taken for electrons and "-" for holes.

$$p = \int_{-\infty}^{0} \frac{D(E)}{1+\exp\left(\frac{E_\mathrm{F}-E}{k_\mathrm{B}T}\right)} dE. \tag{4.5}$$

Also, since the momentum k in equation 4.2 is related to the concentration of electrons as $k = \sqrt{\pi n}$, the Fermi level E_F and carrier concentrations can be modulated by applying an external electric field. This is typically done by varying the gate voltage of graphene FETs.

The unique 2D structure of graphene results in this material having a number of outstanding properties. The main and most attractive of them is an extremely high carrier mobility at room temperature, which can reach $100000\,\mathrm{cm}^2/\mathrm{Vs}$ [17]. Another important property of graphene is a considerable saturation velocity. According to [36], it can exceed $3\times10^7\,\mathrm{cm/s}$ at low carrier concentrations. Furthermore, the saturation velocity of graphene remains larger than those of Si within the whole range of carrier concentrations at which FETs typically operate (1×10^{12}–$1\times10^{13}\,\mathrm{cm}^{-2}$). This is especially valuable for application of graphene in short channel devices. In addition, graphene has an Ohmic contact resistance with metallic electrodes, while its magnitude can be just $50\,\Omega\times\mu\mathrm{m}$ [189]. This allows to achieve high carrier mobilities in graphene devices. Finally, graphene has a high mechanical stability [102], optical transparency [129] and thermal conductivity [157]. These properties are also essential for application of this material in next-generation electronics devices.

Currently, graphene layers can be successfully synthesized using a large number of different methods [39]. However, the zero bandgap of graphene significantly limits the potential of its practical applications. In particular, this disadvantage makes fabrication of high on/off ratio graphene-based transistors impossible, though such devices are required for application in digital circuits. Although several attempts have been undertaken to artificially open the bandgap in graphene (e.g. by using dopants [144] or create nanoribbons [73, 111]), this typically leads to a considerable decrease in mobility, the most fascinating property of graphene. Therefore, in addition to intensive graphene research, alternative 2D materials are being sought.

4.1.2 MoS_2 as a Further Step Beyond Graphene

Molybdenum disulfide (MoS_2) is one of the transition metal dichalcogenides now considered a promising candidate for future device applications. This material has a layered structure consisting of S-Mo-S monolayers, which are formed by hexagonally arranged Mo and S atoms. In MoS_2 crystals these layers are stacked together by weak van-der-Waals interactions, while the thickness of a single layer is 6.5 Å [141]. The geometry of MoS_2 layers reproduced using QuantumWise Virtual Nanolab is shown in Figure 4.3.

A long time ago it was found that bulk MoS_2 crystals exhibit semiconducting properties, while having an indirect bandgap of 1.2 eV [92]. Owing to recent technological progress [134, 174], single-layer MoS_2 has become an interesting semiconducting counterpart of graphene, which has a similar 2D hexagonal structure but no bandgap. The first-principles calculations of the electronic structure of single-layer MoS_2 was performed in [91], where the authors employed the Kohn-Sham density functional theory [77]. These simulations reapproved [120] that single-layer MoS_2 is a direct bandgap semiconductor with a sizable bandgap of 1.79 eV. This allows the main limitation of graphene to be overcome, making MoS_2 suitable for application in logic devices. At the same time, a single-layer MoS_2 has a parabolic dispersion relation in the proximity of the valence band maximum and conduction band minimum (K-point), while having considerable effective masses ($m_\mathrm{e}^* = 0.54\,m_0$ and $m_\mathrm{h}^* = 0.44\,m_0$ for electrons and holes [91], respectively).

Another important property of thin MoS_2 layers is a high intensity of the photoluminescence

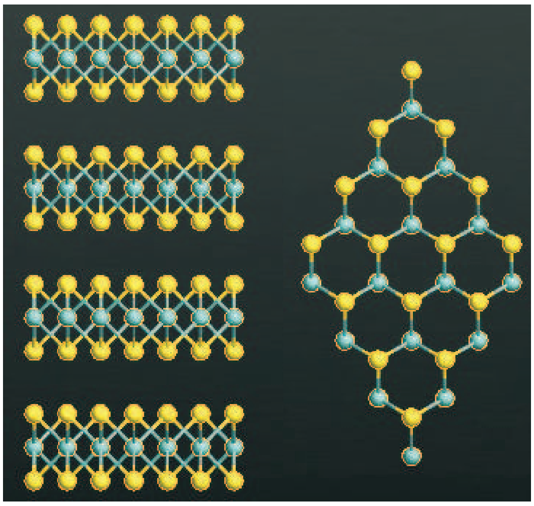

Figure 4.3: Left: Geometry of four MoS_2 layers stacked together by van-der-Waals forces. Right: Cross-section view of the hexagonal arrangement of Mo (blue) and S (yellow) atoms in S-Mo-S monolayer. The distance between the two closest neighbours (atoms of different type) is 2.383 Å, while the closest atoms of the same type are separated with 3.122 Å.

signal [120], which originates from the direct optical transitions at the K point [91]. Therefore, this material is now being successfully applied in optical detectors [118] and electroluminescence devices [163].

A significant disadvantage of MoS_2 compared to graphene is a considerably lower mobility. The room temperature values for bulk MoS_2 crystals are 200–500 cm^2/Vs [44], which is limited by phonon scattering. However, for single-layer MoS_2 on SiO_2 substrates, these values are typically reduced to 0.1–10 cm^2/Vs [104, 140]. Nevertheless, further development of MoS_2 device technologies has significant potential to go far beyond these small values. The two main directions in this context are the use of non-SiO_2 substrates, such as hBN [104], and the engineering of metallic contacts with low resistance (e.g. molybdenum [95]). The most realistic goal would be to outperform graphene with an artificially introduced bandgap.[2]

As for the fabrication of single-layer MoS_2, currently the most wide spread techniques are mechanical exfoliation [134] and chemical vapour deposition (CVD) [174]. However, mechanical exfoliation allows for the obtainment of high quality crystals of single-layer MoS_2 with small grain sizes, typically below 10 μm. Conversely, the grain sizes of CVD MoS_2 crystals can be as large as 120 μm [174]. Therefore, the second technique is more suitable for mass production.

Although MoS_2 has attracted a considerable amount of attention, this is only one material from a wide range of 2D TMDs. At the same time, it has been shown that many other TMDs with similar properties (e.g. TiS_2, TaS_2, WS_2, $MoSe_2$, WSe_2) outperform the bandgapless graphene in many ways, especially in FETs for digital applications [122]. Thus, intensification of research in this direction is expected in the near future.

4.1.3 Phosphorene, Silicene and Germanene: New Era in Semiconductor Science

Phosphorene is an almost unexplored 2D counterpart of bulk black phosphorous, which was only reported in 2014 [115, 145]. First calculations performed in [115] show that this material has a direct bandgap, which depends on the number of layers and also the in-layer strain. Phosphorene

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[2] In graphene with artificially introduced bandgap of 0.15 eV the mobility can be around 200 cm^2/Vs [111].

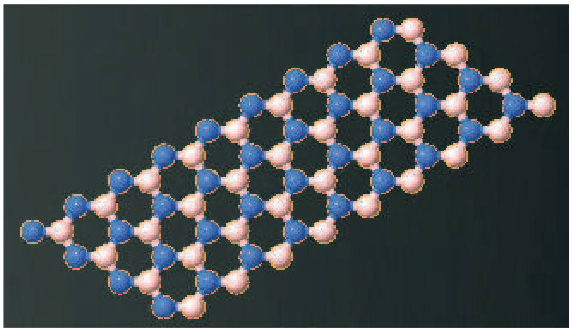

Figure 4.4: Geometry of hBN monolayer formed by alternating B (blue) and N (white) atoms linked by covalent B-N bonds (reproduced using QuantumWise Virtual Nanolab).

is now considered a promising material capable of outperforming graphene in digital device applications. At the same time, its comparably high hole mobility (286 $\mathrm{cm}^2/\mathrm{Vs}$) [115] makes phosphorene a promising candidate as a channel material in p-FETs. This allows limitations of MoS_2, which typically acts as an n-channel material [142], to be overcome. Finally, the high flexibility of phosphorene allows its mechanical exfoliation [183] to be performed, which significantly simplifies fabrication of device prototypes.

Further research for 2D materials capable of overcoming the limitations of graphene has led the research community to the 2D counterparts of Silicon (silicene) [179, 38, 85] and Germanium (germanene) [31]. Together with phosphorene, these, and perhaps other 2D counterparts of well-known semiconductors, may open a new era in sub-Silicon semiconductor device technologies in the near future.

4.1.4 Hexagonal Boron Nitride as a Next-Generation 2D Insulator

Hexagonal boron nitride (hBN) [136, 32, 182] is one of the most widely used phases of boron nitride, and is also known as “white graphene”. As shown in Figure 4.4, the structure of the hBN layer presents a set of hexagonal honeycombs similar to that of graphene. However, alternating atoms of boron and nitrogen are linked by highly polar covalent B-N bonds, in contrast to non-polar C-C bonds in a graphene sheet. At the same time, different layers in multi-layer structures are stacked by van-der-Waals interactions.

Although hBN belongs to the graphene family of 2D materials, its electrical properties are dramatically different. The most important in the context of this work is that hBN has a wide direct bandgap of around 5.9 eV[136]. Together with a crystal structure, that is similar to that of most widely used 2D semiconductors, and the absence of dangling bonds, this makes hBN a promising candidate for the use as a gate insulator in next-generation 2D FET technologies [32, 126, 104].

Initially, hBN insulating layers attracted a considerable amount of attention in attempts to improve the performance of graphene FETs (GFETs) [32, 126]. In particular, in [32] it was shown that the mobility achieved in GFETs made on hBN substrates is considerably larger compared to similar devices on SiO_2. However, in the meantime hBN has been successfully applied as a gate insulator in MoS_2 FETs, also leading to a significant improvement in mobility [104].

While being extremely stable, hBN monolayers can be produced using the same methods as many other 2D materials. Namely, either mechanically or via liquid phase exfoliation as well as CVD can be used [182]. This makes simple assembly of hBN into technological processes used for

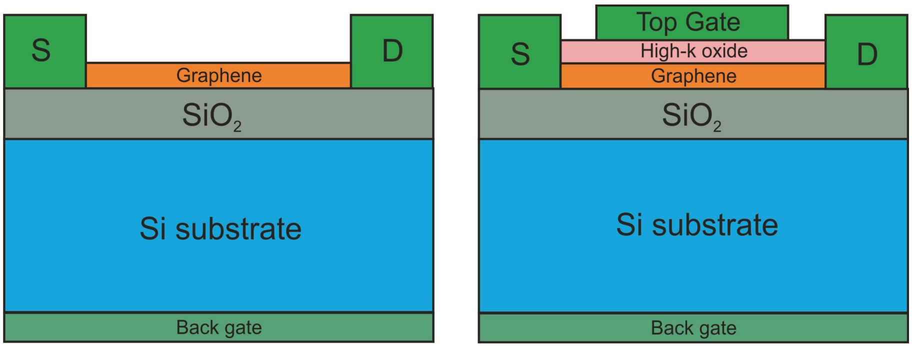

Figure 4.5: Schematic configurations of back-gated (left) and top-gated (right) GFETs. In back-gated devices the graphene channel is typically placed on top of SiO_2, while the gate contact is connected to a Si substrate. In top-gated devices graphene is sandwiched between two gate insulators.

manufacturing of next-generation 2D devices possible. For example, creation of hBN/MoS_2/hBN stacks is possible [103].

4.2 Properties of Graphene FETs

The discovery of an electric field effect in graphene in 2004 [133] allowed this material to be considered as a new building block for modern FETs. Therefore, already in 2007 the first field-effect device with a graphene channel was reported [108]. Since then, many successful attempts at fabricating GFETs [112, 98, 127, 126, 82, 32, 74, 125, 40, 117] and related electronic devices, such as graphene barristors [192] and graphene hot electron transistors [176], have been undertaken.

4.2.1 Different Realizations of GFETs

Depending on the device configuration, GFETs known from the literature are either back-gated [126, 82, 32, 74, 117] or top-gated [108, 112, 127, 98, 40], see Figure 4.5. In back-gated GFETs, the graphene channel is situated on top of the Si/SiO_2 substrate (Figure 4.5(left)). Therefore, the SiO_2 layer, which is obtained by thermal oxidation of Si [112, 82, 74, 117], serves as a gate insulator, while Si is employed as a gate electrode. The graphene channel is typically made by mechanical exfoliation on top of SiO_2 [32] or by CVD [74], while the latter method leads to significant uniformity of the film [74]. The source/drain electrodes (e.g. TiAu) can be created by using electron-beam lithography followed by a lift-off process [117]. Also, for convenience during measurements, a metallic electrode connected to a Si substrate can be added. However, back-gated devices are quite complicated for integration into circuits, and their performance is limited by large parasitic capacitances and the detrimental impact of the environment on the non-covered graphene layer [117]. Therefore, they are mostly suitable for use as test benches when investigating the carrier transport processes in graphene. Thus, devices required for circuit applications have to be equipped with a top gate.

In top-gated devices, the graphene channel is sandwiched between a back gate insulator (SiO_2) and a top gate insulator (typically high-k) with the top gate electrode placed on top (Figure 4.5(right)). Obviously, realization of top-gated GFETs requires additional technological steps compared to their back-gated counterparts. First, after transferring graphene on top of

SiO_2, the high-k top gate oxide (e.g. HfO_2 or Al_2O_3) is grown by atomic layer deposition (ALD) [112, 40]. Second, additional lithography steps are necessary to create the top gate electrode and make the device electrically accessible [40]. Also, since top-gated devices typically have two gate contacts, they can be referred to as "double-gated" (in particular, in this work).

The schematic plots in Figure 4.5 illustrate those realizations of GFETs which in the meantimes are the most commonly used. However, in the literature one can find GFETs with more exotic configurations. For example, the authors of [32, 126] report on back-gated devices with hBN gate insulators. The top-gated GFETs described in [127] are made on the SiC substrate with the graphene channel epitaxially grown on top of it, with no back gate SiO_2 layer. Finally, in [40] Si_3N_4 is used as a back gate insulator. Obviously, all these realizations introduce new technological steps to standard GFETs fabrication techniques, while targeting an improvement of device performance.

4.2.2 Operation and Reliability

As has been mentioned, the position of Fermi level in graphene can be modulated by an external electric field. By varying the voltages applied at the gates (i.e. potential difference between the channel and gates) one can change the carrier concentrations and even the conductivity type of the GFET channel. The latter is due to the zero bandgap of graphene, which leads to the ambipolar behaviour of GFETs. The change of the GFET conductivity type takes place when the Fermi level is aligned at the Dirac point (E_{cv}). Obviously, this is realized when the potential difference between the channel and gates is equal to work fuction difference. In the general case of double-gated GFETs, this is equivalent to a zero effective gate voltage [196], which reads

$$V_{\mathrm{g}}^{\mathrm{eff}} = \frac{C_{\mathrm{tg}}(V_{\mathrm{tg}} - V_{\mathrm{NP}}^{\mathrm{tg}}) + C_{\mathrm{bg}}(V_{\mathrm{bg}} - V_{\mathrm{NP}}^{\mathrm{bg}})}{C_{\mathrm{tg}} + C_{\mathrm{bg}}}, \tag{4.6}$$

where C_{tg} and C_{bg}, and V_{tg} and V_{bg} are the top and back gate capacitances and voltages, respectively. The quantities $V_{\mathrm{NP}}^{\mathrm{tg}}$ and $V_{\mathrm{NP}}^{\mathrm{bg}}$ have the physical meanings of charged neutrality biases (Dirac points) of uncorrelated devices with only a top gate and only a back gate. They are given as

$$V_{\mathrm{NP}}^{\mathrm{tg}} = W_{\mathrm{tg}} - \chi_{\mathrm{gr}} - \frac{qN_{\mathrm{T}}^{\mathrm{tg}}}{C_{\mathrm{tg}}}, \tag{4.7}$$

$$V_{\mathrm{NP}}^{\mathrm{bg}} = W_{\mathrm{bg}} - \chi_{\mathrm{gr}} - \frac{qN_{\mathrm{T}}^{\mathrm{bg}}}{C_{\mathrm{bg}}} \tag{4.8}$$

with W_{tg}, W_{bg} and χ_{gr} being the work functions of the top gate, back gate and graphene. $N_{\mathrm{T}}^{\mathrm{tg}}$ and $N_{\mathrm{T}}^{\mathrm{bg}}$ are the concentrations of charged traps in the top gate and back gate oxides, respectively. Therefore, the top gate Dirac point voltage at fixed V_{bg} reads

$$V_{\mathrm{D}}^{\mathrm{tg}} = -\frac{C_{\mathrm{bg}}}{C_{\mathrm{tg}}}(V_{\mathrm{bg}} - V_{\mathrm{NP}}^{\mathrm{bg}}) + V_{\mathrm{NP}}^{\mathrm{tg}}. \tag{4.9}$$

Similarly, if the device is tested at constant V_{tg} while sweeping V_{bg}, the back gate Dirac point voltage[3] is

$$V_{\mathrm{D}}^{\mathrm{bg}} = -\frac{C_{\mathrm{tg}}}{C_{\mathrm{bg}}}(V_{\mathrm{tg}} - V_{\mathrm{NP}}^{\mathrm{tg}}) + V_{\mathrm{NP}}^{\mathrm{bg}}. \tag{4.10}$$

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[3] In the chapters describing our experimental results, it will be clear whether the device is examined at fixed V_{bg} or V_{tg}. Thus, for simplicity, the charged trap density and Dirac point voltage will be called N_{T} and V_{D}, respectively.

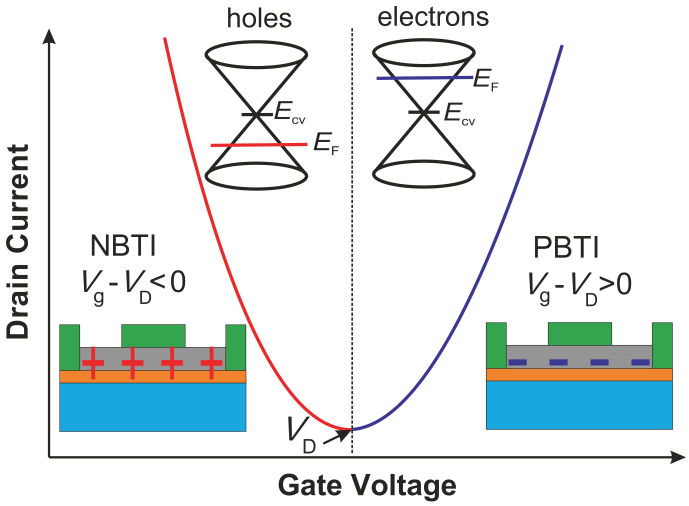

Figure 4.6: Typical I_d-V_g characteristic of GFETs. If the applied V_g is smaller than V_D, the Fermi level is situated in the valence band of graphene and the channel is of p-type. Conversely, if the applied V_g is above V_D, the device operates as an n-FET.

Therefore, one of the main parameters which determines the position of the Dirac point is the density of charges in the corresponding oxide. This quantity is also responsible for the dielectric reliability and typically changes during stress, which make this correlation extremely important for the interpretation of our experimental results below. Also, it is worth noting that if the back gate oxide is much thicker than its top gate counterpart, $V_D^{tg} \approx V_{NP}^{tg}$. Since variations of work functions and gate capacitances during device operation (stress) are negligible, for devices with a thick back gate, N_T^{tg} is the only dynamic parameter responsible for the Dirac point position. Also, equations 4.9– 4.10 show that in double-gated GFETs the Dirac point can be modulated by the voltage applied at the opposite gate electrode.

One should note that in general the top and back gate capacitances used above may differ from geometric capacitances. This originates from the 2D nature of graphene, which leads to a limited density of states $D(E)$ (equation 4.3). Thus, it is necessary to account for the quantum capacitance $C_q = q^2D(E)$ [42]. This quantum capacitance is connected in series with the geometric capacitance $C_g = \varepsilon_g/d_g$, with the gate dielectric constant ε_g and oxide thickness d_g. However, since the typical oxide thicknesses used in GFETs are quite large, the contribution of C_q in most cases is not very significant. Nevertheless, it always worth estimating the impact of the quantum capacitance.

The typical transfer (I_d-V_g) characteristic of a GFET is shown in Figure 4.6. It has a parabolic-like shape with a minimum of the drain current at the Dirac point. Hence, if the applied gate bias is below V_D, the Fermi level lies in the valence band of graphene. This leads to a hole conductivity type of the channel. In contrast, at V_g above the Dirac point the Fermi level is inside the conduction band of graphene, leading to electron transport. In the context of device reliability, this behaviour means that NBTI corresponding to $V_g - V_D < 0$ is associated with hole trapping, while PBTI at $V_g - V_D > 0$ leads to electron trapping. Therefore, in the former case the created defects are positively charged, while in the latter case negatively charged defects are introduced.

However, the symmetric transfer characteristic sketched in Figure 4.6 corresponds to an ideal GFET. In reality, the difference between the electron and hole mobility and the impact of the contact resistance may lead to a considerable asymmetry between the behaviour left and right from the Dirac point [191]. In addition to limitations introduced by device fabrication, this significantly complicates simulations of GFETs. Nevertheless, several compact models allowing for the reproduction of the main characteristics of GFETs have been reported [98, 164, 4, 165, 196]. The most interesting in the context of this work is the paper by Ancona [4], in which an attempt to adjust the drift-diffusion model to the case of GFETs has been undertaken. This idea will be further developed in the course of this work, which will help in the interpretation of our experimental results.

Another interesting property following from the ambipolar nature of graphene is that, contrary to Si FETs, there is no pinch-off behaviour. Instead, if the drain bias V_d is large enough, the device channel can be of an ambipolar nature [125]. Namely, while a considerable part of the channel is n-type, at high V_d the conductivity type of some near-drain regions can change to p-type. As will be shown (Figure 6.2), this typically leads to some signs of the second linear region (“kinks”) on the output (I_d-V_d) characteristics.

We assume that, similarly to Si MOSFETs, the main reliability issues in GFETs should be NBTI, PBTI and HCD. Obviously, recent successes in fabrication of GFETs have created a demand for a detailed study of these phenomena. However, only a few attempts to describe BTI in GFETs have so far been reported [82, 113, 116, 117]. While basic concepts of the BTI origin in GFETs have been understood, there are no systematic studies of this issue. At the same time, nothing at all has been reported about HCD in GFETs. Thus, in the context of this work, a lack of understanding of the reliability of GFETs opens wide a new area of investigation.

4.3 MoS_2 FETs: an Important Step Beyond GFETs

Practical realization of high-performance devices based on 2D materials is a very attractive idea. However, limitations of graphene due to the zero bandgap do not allow for the creation of GFETs with a high on/off current ratio. Therefore, implementation of MoS_2 as a new building block for next-generation FETs has become a must. The first transistor with MoS_2 was reported in 2011 [141]. While having a single-layer MoS_2 channel, this device could exhibit an on/off ratio as high as 10^8 and a mobility of $200\,\mathrm{cm}^2/\mathrm{Vs}$.[4] In the same year an attempt to estimate the potential limits of the performance of MoS_2 FETs was undertaken [195]. By performing self-consistent simulations of quantum transport through a MoS_2 layer, the authors of [195] have shown that MoS_2 FETs can reach a transconductance as large as $4.4\,\mathrm{mS}/\mu\mathrm{m}$ and an on/off ratio of $>10^{10}$, together with an excellent short-channel behaviour. These advances resulted in a more intensive investigation of MoS_2 properties. Thus, numerous groups succeeded at fabricating MoS_2 FETs in the next few years [30, 140, 101, 52, 104, 43, 110, 193, 95, 24, 100].

The absolute majority of MoS_2 FETs known from the literature are of a back-gated configuration [30, 140, 101, 52, 104, 43, 110, 193, 95, 24, 100]. Similarly to GFETs, they are typically fabricated on Si/SiO_2 substrates with thermally grown SiO_2, which serves as a gate insulator. However, in some devices Al_2O_3 grown by ALD right on the Si substrate is employed [24, 95]. Also, the use of transferred hBN as a back gate insulator is possible, while leading to a significant mobility increase [104]. The MoS_2 channel is typically fabricated by mechanical exfoliation from bulk crystals on top of a back gate insulator (e.g. [43, 100]), while being covered by an Al_2O_3 passivation layer in some cases [43]. The source-drain contacts are made by e-beam evaporation and patterned using ultra-violet photolithography, while the most widely used material is TiAu (e.g. [101, 104, 100]). But, contrary to graphene, MoS_2 forms a Schottky contact at the

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[4] According to [46], the mobility value reported in [141] is significantly overestimated. The real mobility for these devices is just a few $\mathrm{cm}^2/\mathrm{Vs}$.

interface with metals. Thus, in some cases a large Schottky barrier may lead to considerable contact resistances, while reducing the overall device performance. Also, in [30] it was claimed that the interface between MoS_2 and the metal is strongly impacted by Fermi level pinning close to the conduction band of MoS_2. Therefore, the authors of [30] suggest using metals with lower work functions as source and drain contacts for MoS_2 FETs. In particular, devices with Sc contacts show a significantly reduced contact resistance, while exhibiting a transconductance of $4.7\,\mu S/\mu m$. Another work [95] reports that the use of Mo contacts also leads to a lower Schottky barrier with MoS_2, which significantly improves transistor performance.

The first MoS_2 FET reported in [141] had a top-gated configuration and employed ALD grown HfO_2 as a top gate insulator. However, direct deposition of a top gate dielectric onto a MoS_2 channel still presents a technological issue. This is because direct ALD of HfO_2 on MoS_2 is not uniform, and no covalent bonding is formed between the two materials [124]. This significantly limits the possibility of integration of MoS_2 FETs in top-gated configuration. Nevertheless, estimation of device performance limits made in [195] have been done for the top-gated geometry which is similar to [141]. Moreover, simulations made by the authors of [23] have shown that the output characteristics of top-gated MoS_2 FETs can exhibit negative differential resistance. Together with a better compatibility of top-gated devices with integrated circuit technology, this makes practical realization of high-performance top-gated MoS_2 FETs the next technological task. One of the first steps in this direction was made in [197], where the use of an ultra-thin (1 nm) metal oxide (e.g. Y_2O_3) as a buffer layer between MoS_2 and HfO_2 was suggested. This resulted in a MoS_2/HfO_2 interface with smaller defect density, while leading to excellent device performance (e.g. a mobility of $63.7\,cm^2/Vs$ and an on/off ratio exceeding 10^8). However, according to a literature review conducted for the purposes of this thesis, the attempts to fabricate the top-gated MoS_2 FETs are still lacking, leaving more detailed studies of top-gated MoS_2 FETs for the near future.

Another important advantage of MoS_2 FETs is that they have a superior immunity to short channel effects [114]. In particular, a high saturation velocity ($2.8\times10^6\,cm/s$) makes MoS_2 channels highly suitable for nanoscale applications [43]. However, MoS_2 devices have been reported to exhibit n-type behaviour, while their transfer characteristics have a shape similar to Si n-MOSFETs [141, 46]. Since for low-power circuits the use of p-FETs is more favourable, other 2D TMDs are now being studied in this context. For example, in [41] WSe_2 p-FETs with reasonable performance are reported. The authors of [29] claim that the use of different electrodes (Ni as a source and Pd as a drain) leads to ambipolar behaviour of WSe_2 FETs.

At the current stage of research the main reliability issue of MoS_2 FETs is associated with the hysteresis appearing on the transfer characteristics due to charging/discharging of fast oxide traps. As shown in [101, 140, 110, 104, 24], the hysteresis can be considerable, especially when measuring in the ambient [101]. However, the use of gate insulators other than SiO_2, namely Al_2O_3 [24] and especially hBN [104], significantly improves the hysteresis stability of MoS_2 FETs.

Other degradation issues which have already been observed for MoS_2 FETs are NBTI [26, 193] and PBTI [26, 139]. Similarly to GFETs, both issues can be observed on the same device, leading to extremely large threshold voltage shifts [26]. The presence of HCD in MoS_2 FETs was declared in [139], although without detailed interpretation. However, reliability studies of MoS_2 FETs are still lacking compared to a great number of papers reporting various device realizations. Also, such studies do not report analysis of BTI recovery, and have been conducted on devices with SiO_2 which lack perfect performance. Therefore, a detailed reliability study on more advanced MoS_2 FETs, in particular with hBN insulator, is a crucial task of this work.

5 Impact of Charged Traps and Random Dopants on the Performance of Si MOSFETs

Charged traps near the oxide/silicon interface and in the oxide bulk can have a dramatic impact on the characteristics of MOSFETs [107, 37, 109, 10, 105, 65, 159, 90, 63, 168, 166]. Although nanoscale transistors contain very few defects [90], each can significantly disturb the channel electrostatics and affect device performance. Particularly, the lifetime of a device [166, 37] is ultimately determined by the time-dependent variability of the transistor characteristics. Such time-dependent variability is caused by the creation/annealing and/or the charging/discharging of interface and oxide traps. Consequently, one must study device reliability from a statistical point of view. Therefore, recently much information on the energy levels of border traps [45, 168, 166] and their depth distribution in the oxide film [105] has been presented. However, the information on the lateral defect position is also important since this would allow for understanding of the role of each single trap in its contribution to the device performance. That is because charged traps situated in different regions of the device may have a significantly different impact on the channel electrostatics, depending on the applied bias conditions and the distribution of random dopants along the channel. Nevertheless, there is no study which would fully describe the impact of the lateral defect position in the presence of random dopants. Thus in the course of this chapter we will perform a detailed analysis of this issue and introduce a new method allowing for a precise evaluation of the lateral trap coordinate.

5.1 Previous Descriptions and their Disadvantages

The impact of the lateral position of a single defect on the device performance was first reported in [10]. The authors of [10] showed that the amplitude of random telegraph noise (RTN) associated with the charging/discharging of a single trap is strongly correlated with the lateral coordinate and reaches its maximum when the trap is situated in the middle of the channel. While the impact of random dopants has been accounted for in their 3D atomistic simulations, the main goal of [10] was to demonstrate that single defects have a dramatic impact on the performance of ultra-scaled devices. At the same time, in [10] no significant attention was paid to the experimental evaluation of the lateral defect coordinate. Nevertheless, the idea to determine the lateral trap position from the analysis of the RTN signal was further developed in the works [105, 93, 25, 137, 78, 94]. The authors of [105] attempt to extract lateral and depth positions of the traps from the analysis of gate and drain current RTN. However, the equation which is used for the estimation of the lateral trap position does not account for the impact of border traps and random dopants on the shape of the potential profile. In Figure 5.1 we demonstrate that this effect may significantly affect the shape of the channel barrier, making the results questionable. A similar methodology disregarding the impact of random dopants is used in [93, 25, 137, 94], while the authors of [78] introduce a 2D trap profiling technique based on the drain-induced barrier lowering (DIBL) effect [78]. This method employs a relation between the position of the channel barrier peak and the magnitude of RTN. However, the perturbations of the surface potential induced by traps and random dopants (Figure 5.1) are also

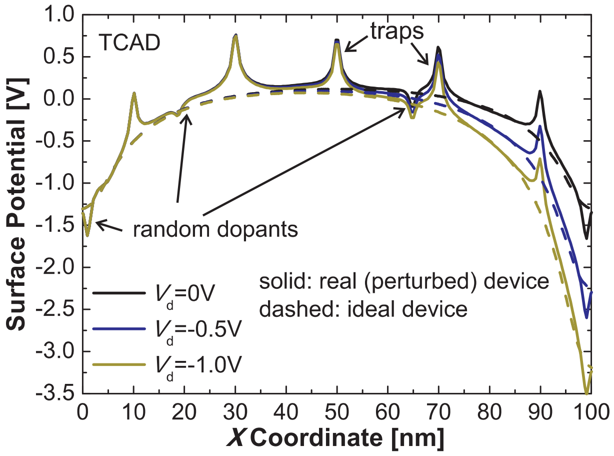

Figure 5.1: The surface potential distribution along the interface of the investigated device with five traps situated exactly at the interface and randomly distributed dopants overlaid on the similar distribution for an ideal device, i.e. without traps and random dopants. The TCAD simulations have been performed in the weak inversion regime ($V_{\mathrm{g}} = \text{-}0.2\,\mathrm{V}$). The source corresponds to $x = 0\,\mathrm{nm}$ and the drain to $x = 100\,\mathrm{nm}$.

disregarded. This would make the relation for the peak position evaluated in [78] inapplicable, independently of the magnitude of the DIBL effect.

In the following we will present a new approach which exploits the fact that the impact of the lateral defect coordinate X_{T} on the drain bias dependence of the threshold voltage shift ΔV_{th} induced by a single charged trap is stronger than the impact of random dopants. Accounting for the effect of random dopants is the key feature of our method since it allows us to estimate the evaluation uncertainty for each of the extracted lateral trap positions. Next we will introduce a compact model allowing us to understand the underlying physical nature. Finally, we will present a simple equation, which with reasonable accuracy allows for the estimation of the lateral trap position directly from the experimental data given in Figure 5.2.

5.2 Experimental Technique

p-MOSFETs with a channel length of $L = 100\,\mathrm{nm}$, a width of $W = 150\,\mathrm{nm}$ and a 2.2 nm thick SiON gate insulator have been characterized using TDDS [68, 67, 181]. This technique is based on alternatively charging and discharging preexisting border traps in order to study their capture and emission times. While having the same properties as newly created defects [70], in p-MOSFETs these traps are responsible for the recoverable component of the NBTI. By analyzing the TDDS results, the threshold voltage shift ΔV_{th} induced by each particular trap can be individually traced versus the applied drain bias V_{d}. Results for three different devices and nine defects are summarized in Figure 5.2. One can see that the $\Delta V_{\mathrm{th}}(V_{\mathrm{d}})$ characteristics of every single trap have dramatically different shapes. Since the trap depth and energy level have no significant impact on the drain bias dependence of ΔV_{th} [57], this indicates that the traps responsible for the threshold voltage shift are located in different regions of the device [10]. Based on this assumption, we perform a parameterization of the $\Delta V_{\mathrm{th}}(V_{\mathrm{d}})$ curves and demonstrate that they can be perfectly approximated by a cubic polynomial function $\Delta V_{\mathrm{th}}(V_{\mathrm{d}}) = \sum_i p_i V_{\mathrm{d}}^i$. As will be shown later, the corresponding parameterization coefficients are unique for each particular trap position. Therefore, this unique set of coefficients can be treated as the defect signature and used for a precise evaluation of the lateral defect coordinate.

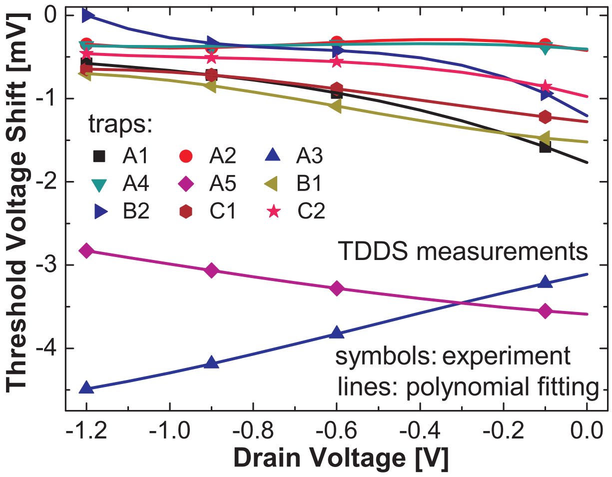

Figure 5.2: $\Delta V_{\mathrm{th}}(V_{\mathrm{d}})$ characteristics of nine individual traps obtained from time-dependent defect spectroscopy (TDDS) measurements [68, 67, 181] on p-MOSFETs with $L/W = 100\,\mathrm{nm}/150\,\mathrm{nm}$ and 2.2 nm thick SiON film employed as a gate insulator. The results can be perfectly fitted using the cubic polynomial function $\Delta V_{\mathrm{th}}(V_{\mathrm{d}}) = \sum_i p_i V_{\mathrm{d}}^i$.

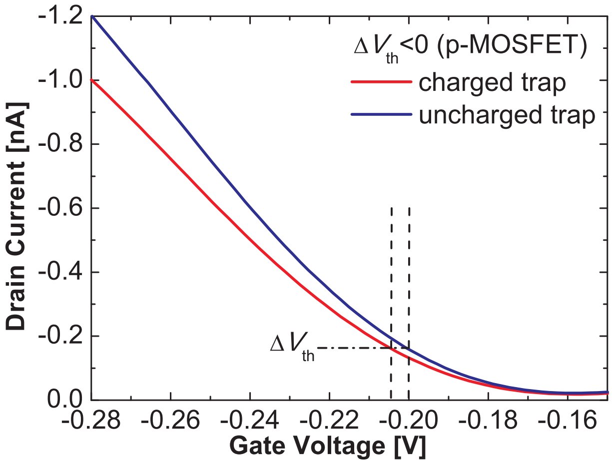

Figure 5.3: Gate transfer (I_{d}-V_{g}) characteristics simulated using TCAD for an ideal device and a device with a single charged defect. ΔV_{th} is defined with respect to I_{d} reached for the unperturbed device at $V_{\mathrm{g}} = -0.2\,\mathrm{V}$.

5.3 TCAD Simulations

We apply our TCAD simulator Minimos-NT, which considers random discrete dopants using the established methodology pioneered by Asenov [9] with a density gradient model [5] to account for the quantum correction of the Coulomb potential [19]. This simulator has already been successfully applied to assess the reliability of modern nanoscale devices [15, 16]. TCAD simulations were carried out for one hundred p-MOSFETs with identical architectures but with different configurations of random dopants. Initially we performed the simulations for a fixed coordinate along the oxide/silicon interface (X_{T}) and different trap positions in the direction perpendicular to the source-bulk-drain plane (W_{T}). The ΔV_{th} values induced by the traps situated in each particular position were evaluated as a function of V_{d} for all 100 devices using I_{d}-V_{g} curves simulated with and without charged traps. As shown in Figure 5.3, ΔV_{th} was determined using a standard method [89] for a fixed drain current I_{d} corresponding to $V_{\mathrm{g}} \leq V_{\mathrm{th}}$, i.e. weak

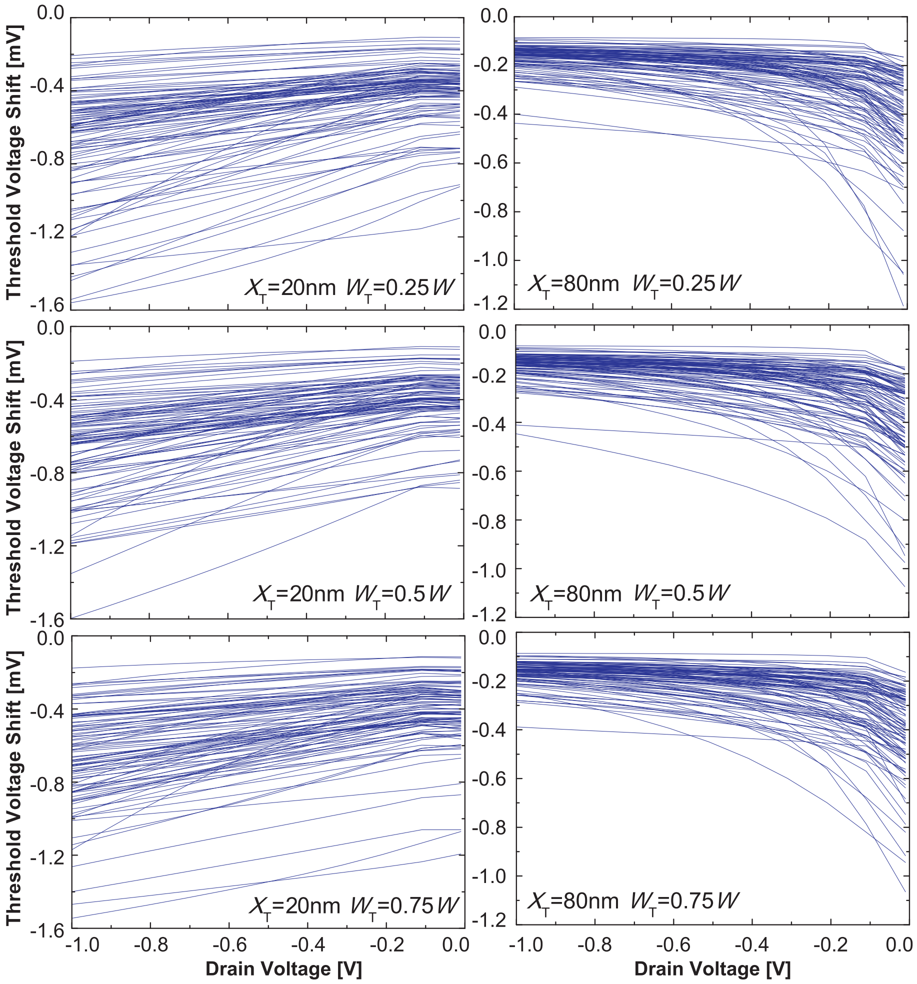

Figure 5.4: $\Delta V_{\mathrm{th}}(V_{\mathrm{d}})$ characteristics for devices with one hundred different random dopant configurations and three different trap coordinates across the channel W_{T} simulated using TCAD for traps close to the source (left) and the drain (right). For any fixed X_{T} the shape of the $\Delta V_{\mathrm{th}}(V_{\mathrm{d}})$ curves is almost independent of W_{T}. Thus all the following TCAD simulations were performed using $W_{\mathrm{T}} = W/2$.

inversion. In Figure 5.4 it is shown that the position across the channel W_{T} has no significant impact on the shape of the $\Delta V_{\mathrm{th}}(V_{\mathrm{d}})$ curves, which implies that W_{T} can not be extracted using our methodology. At the same time, a weak dependence of the results on W_{T} together with an insignificant impact of the vertical trap position on the $\Delta V_{\mathrm{th}}(V_{\mathrm{d}})$ dependence [57] means that the impact of shallow trench isolation [106] on our results is also negligible. Therefore, in all the following simulations we used $W_{\mathrm{T}} = W/2$. The lateral defect coordinate X_{T} was varied from the source to the drain using 10 nm steps to provide the benchmark for our trap location technique.

The obtained $\Delta V_{\mathrm{th}}(V_{\mathrm{d}})$ curves show a cubic behavior, just like their experimental counterparts. In Figure 5.5 one can clearly see that the shape of these curves has a stronger dependence on the lateral defect coordinate X_{T} than on the distribution of random dopants. For example, if a trap is situated at the source side of the channel ($X_{\mathrm{T}} = 20$ nm and $X_{\mathrm{T}} = 40$ nm), ΔV_{th} versus V_{d} increases independently of the configuration of random dopants. However, for a trap situated at the drain side ($X_{\mathrm{T}} = 80$ nm) ΔV_{th} versus V_{d} decreases. When a trap is located in the middle of the channel ($X_{\mathrm{T}} = 50$ nm), the situation becomes more complicated. Although for most of

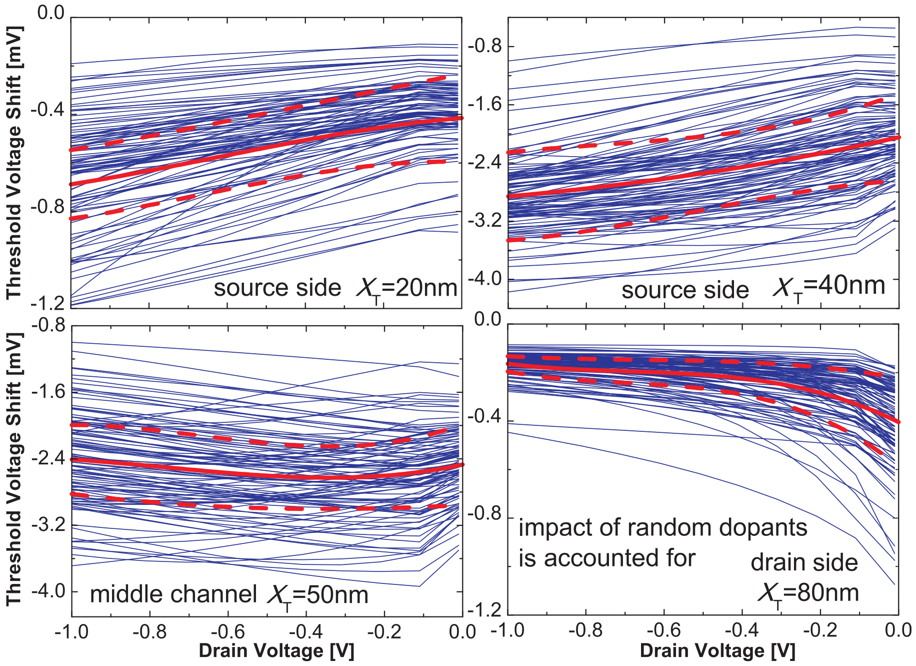

Figure 5.5: $\Delta V_{\mathrm{th}}(V_{\mathrm{d}})$ characteristics for devices with one hundred different random dopant configurations and four different lateral trap coordinates X_{T} simulated using TCAD. The red lines indicate the characteristics with average (solid) and plus/minus one standard deviation cubic parameterization coefficients (dashed). Clearly, the shape of the $\Delta V_{\mathrm{th}}(V_{\mathrm{d}})$ curves is more strongly affected by the lateral trap position than by the random dopant distribution which impacts mostly the absolute value. Therefore, it can be used as a defect fingerprint and allows us to evaluate the lateral defect coordinate.

the random dopant configurations the dependence of ΔV_{th} on V_{d} is mostly dominated by the higher order polynomial terms, for some of them ΔV_{th} increases versus V_{d} while for others it decreases. This is because the transition between the two possible types of $\Delta V_{\mathrm{th}}(V_{\mathrm{d}})$ dependence takes place for trap positions close to the middle of the channel, although the exact point is determined by the random dopant configuration.

The observed correlation between the $\Delta V_{\mathrm{th}}(V_{\mathrm{d}})$ characteristics and the lateral trap position is the key result of our TCAD simulations. This outcome is in agreement with the experimental results (Figure 5.2). Therefore, this feature introduces the working principle of our trap location technique. At the same time, the obtained results allow us to conclude that the expected accuracy of our technique for the central traps is lower because the dependence of the $\Delta V_{\mathrm{th}}(V_{\mathrm{d}})$ behavior on the random dopant configuration is strongest.

5.4 Compact Model

The use of TCAD allows for the simulation of the reference data for the trap location technique with rather high accuracy. However, a physical explanation of the results is not obvious. Therefore, we attempted to reproduce the observed behaviour of the $\Delta V_{\mathrm{th}}(V_{\mathrm{d}})$ curves for different X_{T} using a physics based compact model.

Our compact model exploits the fact that the impact of a charged trap on the device electrostatics is equivalent to a local perturbation of the majority carrier concentration (electrons in the case of p-MOSFETs). This feature is included by perturbing the surface potential and treating it as

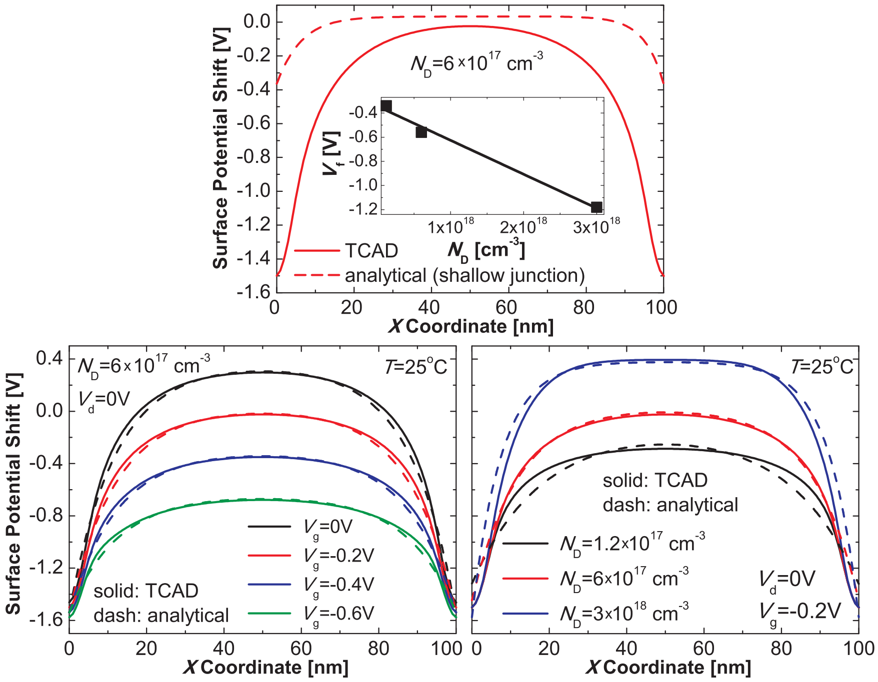

Figure 5.6: The surface potential distributions $\psi_s^0(x)$ obtained using an analytical model overlaid on the related results simulated with TCAD. A direct implementation of the model [188] does not lead to a reasonable agreement (top). However, use of fitting parameters allowed us to neutralize the shallow depth approximation and fit the analytical results with their TCAD counterparts for different V_g and N_D (bottom). While the scaling factor b, which is used to modify the built-in potential, was found to be universal, the fitting parameter V_f employed to adjust the flat band voltage is a linear function of N_D (inset).

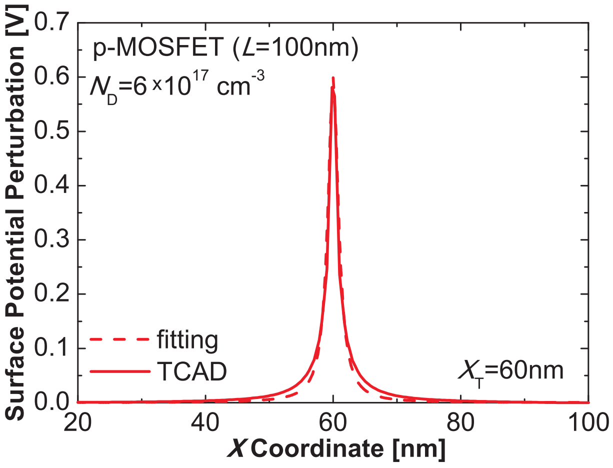

Figure 5.7: The trap-induced perturbation of the surface potential $\psi_s^{T0}(x)$ has a universal shape and can be reasonably fitted using a Voigt-like peak function centered at the trap position X_T. The peak height is slightly dependent on N_D and should be adjusted using an appropriate calibration factor V_0 in order to match the experimentally measured ΔV_{th}.

a local abrupt increase of the channel doping level ΔN_D. The shift of an electron concentration induced by a charge at zero drain bias can be written as

$$\Delta N_e(x) = \Delta N_D(x) = N_D e^{\frac{\psi_s^0(x)}{kT}}\left(e^{\frac{\psi_s^{T0}(x)}{kT}} - 1\right), \tag{5.1}$$

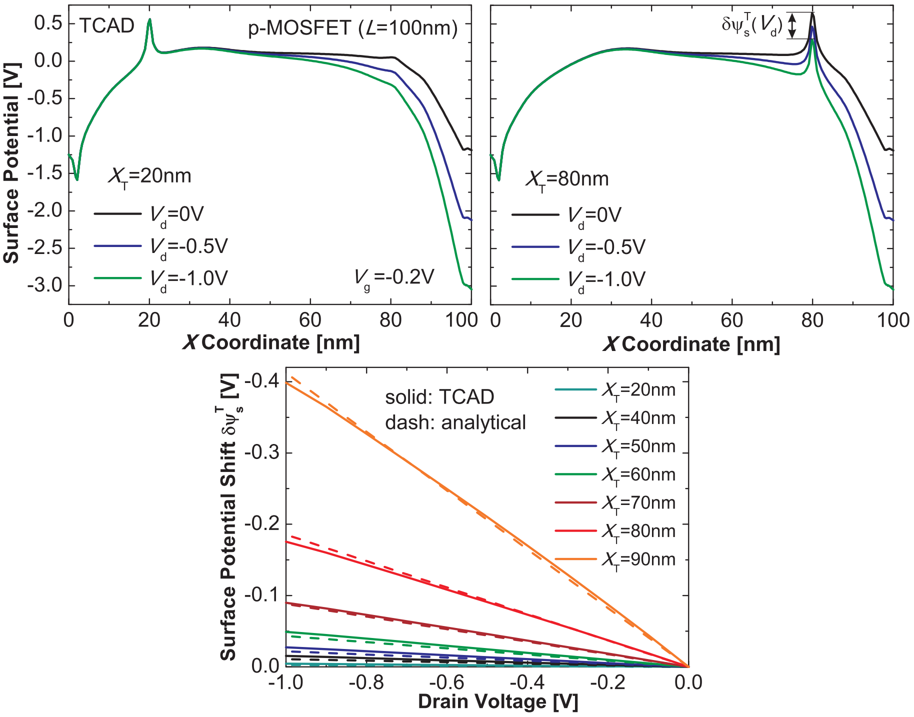

Figure 5.8: Our TCAD simulations show that the V_{d} dependence of the surface potential perturbation $\delta\psi_{\mathrm{s}}^{\mathrm{T}}(X_{\mathrm{T}}, V_{\mathrm{d}})$ is linear and becomes more significant if the trap is situated at the drain side of the channel. This behaviour can be captured analytically with the model of [86] adjusted for the case of a single defect in the perturbed channel region.

where $\psi_{\mathrm{s}}^{0}(x) = \psi_{\mathrm{s}}(x, V_{\mathrm{d}} = 0)$ is the surface potential along the interface in the absence of a charged defect and $\psi_{\mathrm{s}}^{T0}(x) = \psi_{\mathrm{s}}^{T}(x, V_{\mathrm{d}} = 0)$ is a peak function centered at $x = X_{\mathrm{T}}$ which describes the local shift of $\psi_{\mathrm{s}}^{0}(x)$ in the presence of a charged trap (these are the spikes illustrated in Figure 5.1).

The surface potential distribution $\psi_{\mathrm{s}}^{0}(x)$ in the absence of the charged trap is calculated using an analytical model [188]. This model assumes that both source and drain junction depths are negligibly small, which allows us to avoid a numerical solution of the Poisson equation and derive an analytical expression for the surface potential. However, $\psi_{\mathrm{s}}^{0}(x)$ obtained using the original expression from [188], is significantly flattened compared to its counterpart simulated with TCAD (Figure 5.6). Therefore, we adjusted the model [188] for the case of a deep junction by neutralizing the shallow junction depth approximation. This was done by artificially substituting the flat band voltage as $V_{\mathrm{fb}} = V_{\mathrm{f}} \text{ - } V_{\mathrm{g}}$ and multiplying the built in potential V_{bi} by factor $b = 3.1$, which is equivalent to an increase in the junction depth y_{d}. As shown in Figure 5.6, this allowed us to obtain reasonable fits of the surface potential distribution to our TCAD results for different N_{D} and V_{g}. Also, the fitting parameter b was found to be independent of N_{D}, V_{g} and V_{d}, while V_{f} linearly decays for larger N_{D} (inset).

The trap-induced perturbation $\psi_{\mathrm{s}}^{T0}(x)$ was found to have a universal shape for each device. As shown in Figure 5.7, it can be accurately fit using a Voigt-like peak function:

$$\psi_{\mathrm{s}}^{T0}(x) = \pm \frac{V_0}{1 + \left(\frac{x - X_{\mathrm{T}}}{x_0}\right)^2}. \tag{5.2}$$

Here a plus sign must be taken for a p-MOSFET and a minus sign for an n-MOSFET; the normalization factor is $x_0 = 1\,\mathrm{nm}$. The calibration parameter V_0 which determines the spike

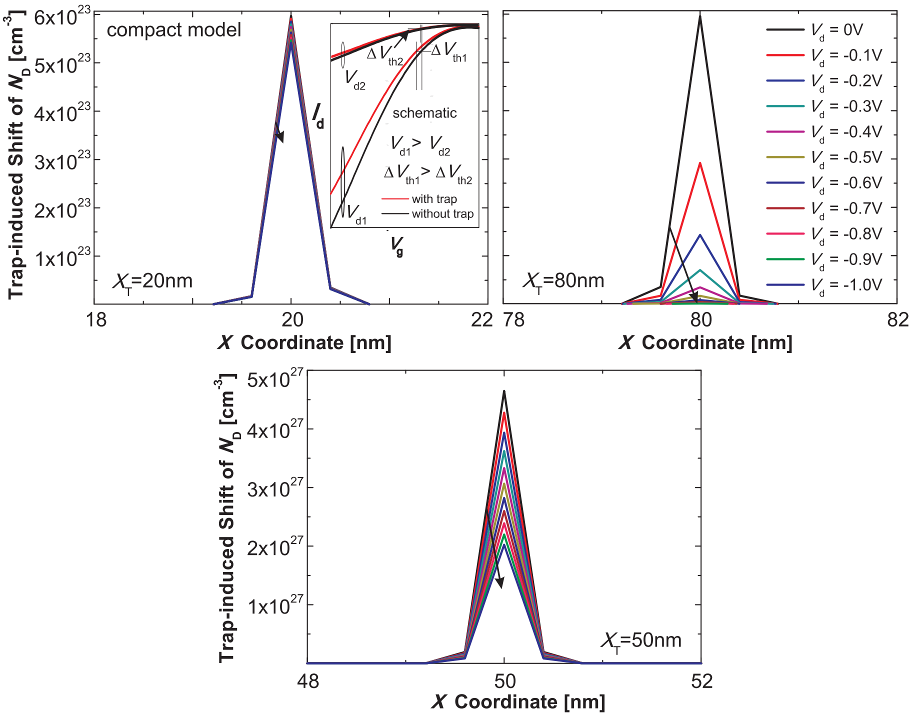

Figure 5.9: In our compact model the impact of a charged border trap is treated as an artificial δ-like local increase of the channel doping level N_D. Its magnitude can be calculated for any X_T using the surface potential distribution along the channel. When the trap is situated at the source side of the channel the concentration shift has a weak dependence on V_d. Therefore, the behaviour of the $\Delta V_{th}(V_d)$ curves is mainly determined by I_d-V_g vs. V_d dependence (inset) which leads to a positive slope. Conversely, a strong decrease of the concentration shift induced by the traps situated at the drain side versus V_d leads to $\Delta V_{th}(V_d)$ curves going down. At the same time, the charged trap in the middle of the channel is equivalent to a larger concentration shift which leads to a bigger ΔV_{th}. These dependences are introduced into the simulations based on the Enz-Krummenacher-Vittoz (EKV) model [8] to obtain the I_d-V_g characteristics.

height is independent of X_T and V_d and has to be adjusted to match the obtained ΔV_{th} with their experimental or TCAD counterparts. By performing the TCAD simulations for different N_D we found that typical values of V_0 lie within the range of $0.4-1\,\mathrm{V}$.

The description above corresponds to the case of zero drain voltage, while simulations of the $\Delta V_{th}(V_d)$ curves require incorporation of a V_d dependence into the compact model. In the case of an unperturbed surface potential $\psi_s(x, V_d)$ can be reasonably described using the model [188] which has been used to calculate $\psi_s^0(x)$. However, the channel doping shift ΔN_D is an exponential function of the surface potential. Therefore, its V_d dependence is mainly determined by the behaviour of the total shift of the surface potential $\psi_s^T(x, V_d) = \psi_s^{T0}(x) + \delta\psi_s^T(X_T, V_d)$, where $\delta\psi_s^T(X_T, V_d)$ is the V_d-induced surface potential perturbation. The behaviour of $\delta\psi_s^T(X_T, V_d)$ can be captured analytically using the approach proposed in [86], which considers the surface potential distribution in the MOSFET channel with perturbed region. In order to do this, we adjusted the model [86] to the case of a single defect by assuming that the dimension of the perturbed area is equal to the lateral size of the trap (see the details in [11]). As shown in Figure 5.8, this allowed us to reasonably reproduce both X_T and V_d dependences of $\delta\psi_s^T$ simulated with TCAD. Namely, the dependence of $\delta\psi_s^T$ on V_d is linear and becomes more pronounced if the trap is situated at the drain side of the channel.

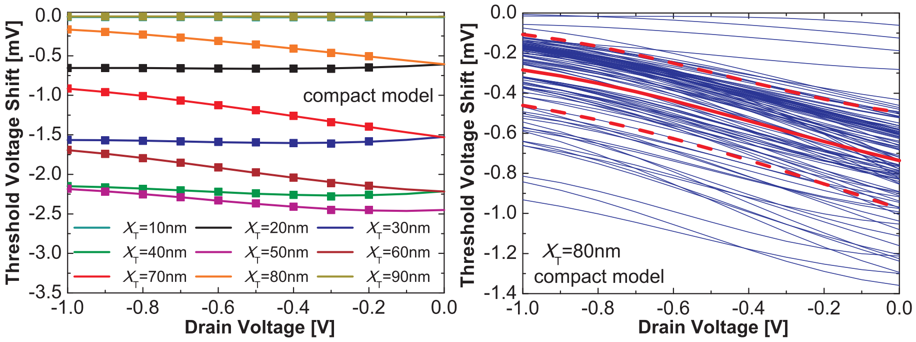

Figure 5.10: Left: The $\Delta V_{\mathrm{th}}(V_{\mathrm{d}})$ curves simulated using our compact model for different X_{T} (symbols) and fitted using cubic polynomials (lines). The characteristics show all typical features known from TCAD results. Namely, the threshold voltage shift induced by the trap situated in the middle of the channel is the largest. Also, the dependence of ΔV_{th} versus V_{d} has a positive slope if the trap is located at the source side of the channel and negative if it is situated at the drain side. As follows from our description, this originates from the drain bias dependence of the perturbed surface potential which can be treated as an equivalent channel doping shift (Figure 5.9). Right: The $\Delta V_{\mathrm{th}}(V_{\mathrm{d}})$ curves obtained using the compact model for $X_{\mathrm{T}} = 80\,\mathrm{nm}$ and a hundred different configurations of random dopants. The impact of random dopants was incorporated by adding random perturbations to the surface potential distributions used in the simulations.

As was shown above, the quantities $\psi_{\mathrm{s}}^{0}(x)$, $\psi_{\mathrm{s}}^{T0}(x)$ and $\delta\psi_{\mathrm{s}}^{\mathrm{T}}(X_{\mathrm{T}}, V_{\mathrm{d}})$ can be calculated analytically. Therefore, the equivalent doping level shift is[1]

$$\Delta N_{\mathrm{D}}(x,\, V_{\mathrm{d}}) = N_{\mathrm{D}}\left(\mathrm{e}^{\frac{\psi_{\mathrm{s}}(x,\, V_d)+\psi_{\mathrm{s}}^{T0}(x)+\delta\psi_{\mathrm{s}}^{T}(X_T,\, V_d)}{kT}} - \mathrm{e}^{\frac{\psi_{\mathrm{s}}(x,\, V_d)}{kT}}\right). \tag{5.3}$$

The doping level profiles obtained for three different trap positions are shown in Figure 5.9, where one can see that ΔN_{D} heights and V_{d} dependences are strongly linked to the lateral trap position. For example, the impact of traps situated in the middle of the channel ($X_{\mathrm{T}} = 50\,\mathrm{nm}$) is equivalent to a much higher doping level shift than it would be for traps situated closer to the electrodes. At the same time, the concentration shifts, which correspond to traps situated symmetrically with respect to the middle of the channel ($X_{\mathrm{T}} = 20\,\mathrm{nm}$ and $X_{\mathrm{T}} = 80\,\mathrm{nm}$), are comparable at $V_{\mathrm{d}} = 0$. However, their drain bias dependences are very different. This originates from the fact that the V_{d} dependence of $\delta\psi_{\mathrm{s}}^{\mathrm{T}}$ is stronger when the trap is situated near the drain. Hence, the concentration shift corresponding to traps situated at the source side of the channel is almost independent of the drain bias. Conversely, traps situated at the drain side induce a concentration shift which strongly decreases at higher V_{d}.

The obtained doping level profiles were implemented into the Enz-Krummenacher-Vittoz (EKV) model [8], which allowed us to simulate the I_{d}-V_{g} characteristics with and without ΔN_{D} as required for the extraction of $\Delta V_{\mathrm{th}}(V_{\mathrm{d}})$. Finally, as was the case for the TCAD simulations, our compact model allows for the incorporation of the impact of random dopants. This is done by artificially adding random perturbations to the surface potential distributions, which are used to calculate ΔN_{D} versus X_{T}. This consequently impacts the ΔV_{th} magnitude and introduces standard deviations.

The $\Delta V_{\mathrm{th}}(V_{\mathrm{d}})$ characteristics simulated using our compact model for different X_{T} are shown in Figure 5.10. These curves exhibit similar behaviour to their counterparts simulated with

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[1] Obviously, the drain bias dependence of the unperturbed channel potential can be neglected, i.e. $\psi_{\mathrm{s}}^{0}(x)$ can be used instead of $\psi_{\mathrm{s}}(x, V_{\mathrm{d}})$.

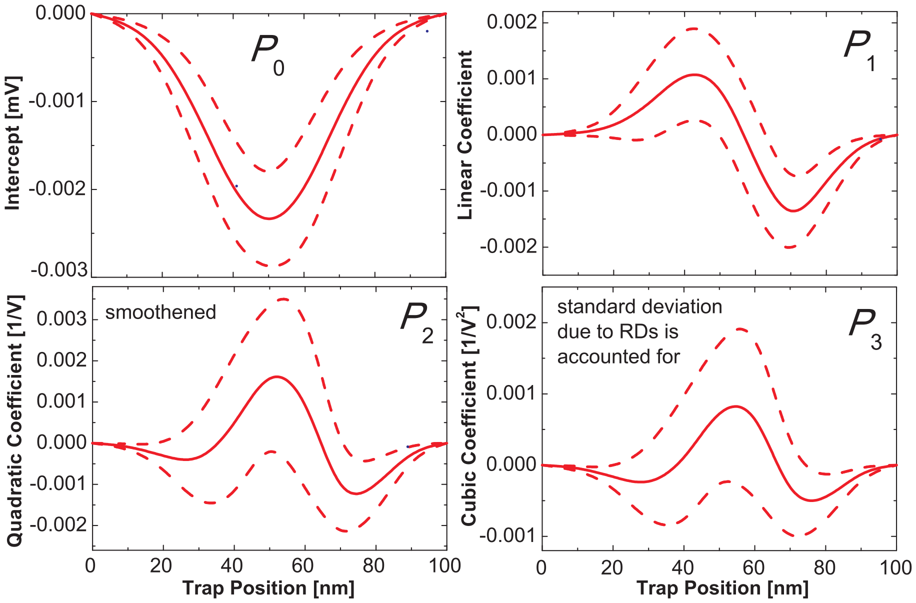

Figure 5.11: The dependences of the polynomial parameterization coefficients of the $\Delta V_{\mathrm{th}}(V_{\mathrm{d}})$ characteristics on X_{T} simulated with TCAD (interpolation using 0.1 nm steps and smoothing is done). The impact of random dopants is accounted for; the solid lines reproduce the average values and the dashed ones the average plus/minus σ_i. Clearly, the behavior of the $\Delta V_{\mathrm{th}}(V_{\mathrm{d}})$ curves is different for different lateral defect coordinates. For example, the slope changes sign near the middle of the channel. The intercept P_0 is symmetric with respect to the middle of the channel where it reaches the highest absolute values, in agreement with [10, 53, 54]. Also, the coefficients P_2 and P_3 are larger in the middle of the channel.

TCAD for different X_{T}, and can be well fitted with cubic polynomials. Moreover, the analytical approach allows us to understand the origin of this behaviour. For example, the threshold voltage shift induced by a trap in the middle of the channel is the largest. This is fully consistent with the results from Figure 5.9 which state that the impact of such traps is equivalent to a concentration shift increase by several orders of magnitude. Furthermore, this agrees with previous literature reports [10, 53, 54]. The sign of the $\Delta V_{\mathrm{th}}(V_{\mathrm{d}})$ dependence (i.e. slope P_1) is explained by the interplay between the two contributions. On the one hand, at lower V_{d} the magnitude of the threshold voltage shift should be lower which originates from the behaviour of I_{d}-V_{g} characteristics versus V_{d} (Figure 5.9(inset)). However, this is relevant only if the drain bias dependence of the concentration peak is not significant, which is the case for traps situated at the source side of the channel (Figure 5.9(left)). Therefore, a positive slope P_1 is obvious for these traps. On the other hand, for traps situated closer to the drain, the contribution introduced by the abrupt decrease of the concentration shift at larger V_{d} (Figure 5.9(right)) is more pronounced, making the values of P_1 negative. In the middle of the channel both contributions nearly compensate each other and therefore the linear term in $\Delta V_{\mathrm{th}}(V_{\mathrm{d}})$ dependence is small (i.e. P_1 changes sign). The results provided in Figure 5.10(right) show that the model allows for a reasonable reproduction of the fluctuations introduced by random dopants. This means that our compact model can be applied to simulate the reference data for the trap location technique, which would allow for the avoidance of time-consuming TCAD simulations.

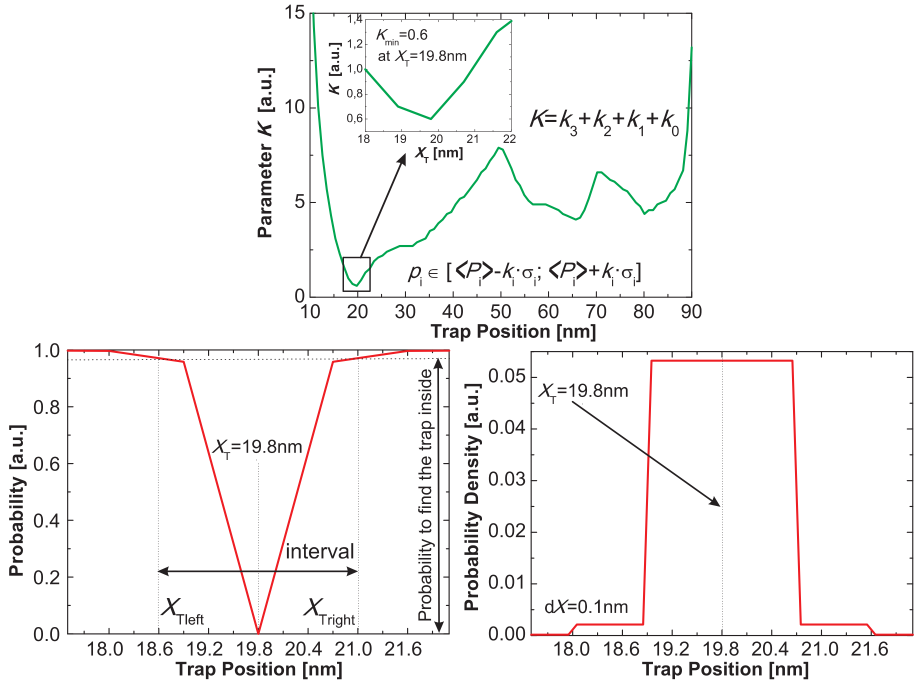

Figure 5.12: Illustration of the working principle of our trap location algorithm for $X_\mathrm{T}=20\,\mathrm{nm}$. The proximity of the experimental $\Delta V_\mathrm{th}(V_\mathrm{d})$ to the mean curve simulated using TCAD or the compact model is determined by the parameter K. A typical $K(X_\mathrm{T})$ dependence shows that K_min is observed at X_T=19.8 nm, which is the most likely extracted lateral defect position. The probability of finding the trap inside several intervals around an extracted X_T is equivalent to the probability with which the points $X_{\mathrm{T}_\mathrm{left}}$, X_T and $X_{\mathrm{T}_\mathrm{right}}$ can be separated with respect to the narrowest intervals $[\langle P_i\rangle$-$k_i\sigma_i$; $\langle P_i\rangle$+$k_i\sigma_i]$ selected at each point. The probability density corresponding to the interval $\mathrm{d}X=0.1\,\mathrm{nm}$ presents a distribution around X_T, which originates from the uncertainity introduced by the random dopants.

5.5 Extraction of the Lateral Trap Position

5.5.1 Method Description and Verification

The results provided above introduce the concept of our trap location technique, which is based on the observation that the impact of the lateral trap position X_T on the shape of $\Delta V_\mathrm{th}(V_\mathrm{d})$ curves is typically stronger than the fluctuations induced by random dopants. Thus in order to extract the lateral trap position from the experimental data, we parameterize the results of the TCAD simulations using a cubic polynomial function $\Delta V_\mathrm{th}(V_\mathrm{d})=\sum_i P_i V_\mathrm{d}^i$ and determine the coefficients P_i for each random dopant configuration corresponding to a certain X_T. The mean TCAD coefficients $\langle P_i\rangle$ and $\langle P_i\rangle\pm\sigma_i$, with σ_i being the standard deviations induced by the random dopants, are subsequently calculated. Their dependences on the lateral defect position are shown in Figure 5.11. Note that although in the simulations X_T has been varied using 10 nm steps, the values of P_i have been then interpolated at all intermediate X_T points using 0.1 nm steps. The lateral trap position was evaluated according to an algorithm which compares the cubic parameterization coefficients p_i, obtained from the experimental data (e.g. Figure 5.2) to those P_i which have been simulated using TCAD.

The working principle of our trap location technique is illustrated in Figure 5.12. For each X_T one can find a minimum k_i which guarantees that p_i lies inside the interval $[\langle P_i\rangle$-$k_i\sigma_i$;

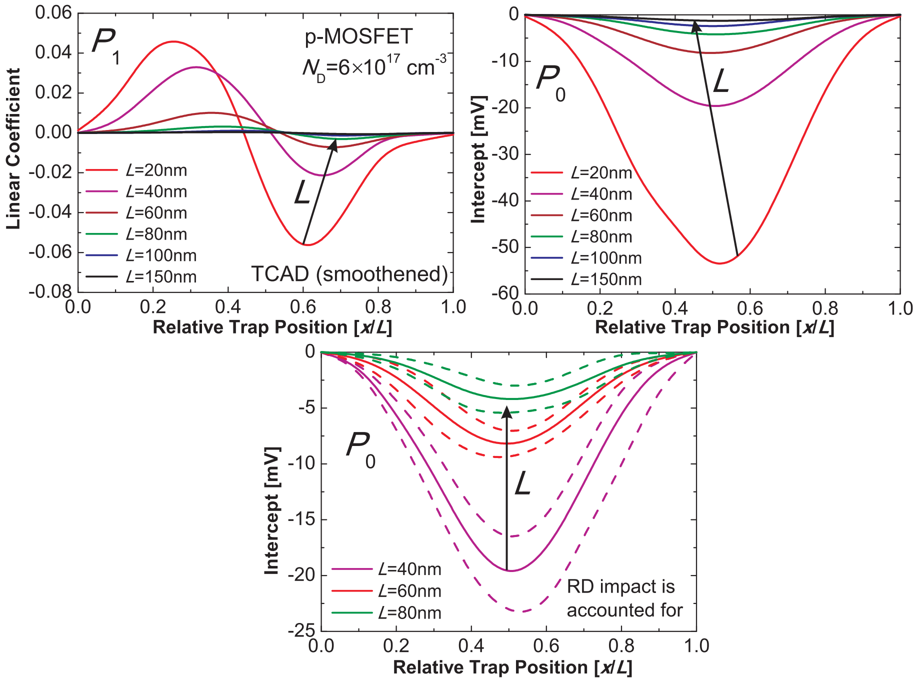

Figure 5.13: The dependences of the slope and the intercept of the $\Delta V_{\mathrm{th}}(V_{\mathrm{d}})$ characteristics on X_{T} simulated with TCAD for devices with different channel lengths. Clearly, for smaller L the impact of the lateral trap position on the magnitude and drain bias dependence of ΔV_{th} increases more significantly than the magnitude of random dopant fluctuations (bottom plot). Therefore, although in ultra-scaled devices the impact of random dopants is more pronounced [9], device scaling will even lead to an improvement in the accuracy of our trap location technique.

$\langle P_i \rangle + k_i\sigma_i]$. Therefore, the proximity between experimental and TCAD data will be reflected by the sum $K = \sum_i k_i$. The parameter K is a function of the lateral defect coordinate X_{T} which reaches its minimum value when the combination of p_i lies closest to the corresponding $\langle P_i \rangle$ (Figure 5.12(top)). Since it is supposed that the $\Delta V_{\mathrm{th}}(V_{\mathrm{d}})$ curve obtained from TDDS measurements is associated with an individual defect, the corresponding value of X_{T} is considered the most likely lateral position of this defect.

After the lateral defect position is evaluated, the probability that all four intervals $[\langle P_i \rangle$-$k_i\sigma_i$; $\langle P_i \rangle + k_i\sigma_i]$ obtained for the extracted X_{T} do not simultaneously overlap with their counterparts for neighboring points, X_{Tleft} and X_{Tright}, is determined. This probability is interpreted as the probability that the trap is situated inside the interval $[X_{\mathrm{Tleft}}, X_{\mathrm{Tright}}]$ centered at the extracted X_{T} (Figure 5.12(bottom)). Then, the obtained probability can be replotted in terms of a normalized density, which is calculated for each X_{T} and $\mathrm{d}X$ as a probability to find the trap inside the fixed interval $[X_{\mathrm{T}}$-$\mathrm{d}X$; $X_{\mathrm{T}}+\mathrm{d}X]$. Note that the consideration of all four coefficients results in high accuracy of the lateral trap position evaluation. This is because the proximity of the experimental coefficients to their TCAD counterparts is determined more reliably. Thus the neighbouring points can be separated with a higher probability, which increases the spatial resolution.

As follows from the above description, the accuracy of our trap location technique depends on the impact of the random dopants on the shape of $\Delta V_{\mathrm{th}}(V_{\mathrm{d}})$. Since the impact of random dopants is known to be stronger in devices with smaller L [9], one could expect the method to not allow an accurate extraction of X_{T} in ultra-scaled devices. However, the results of our

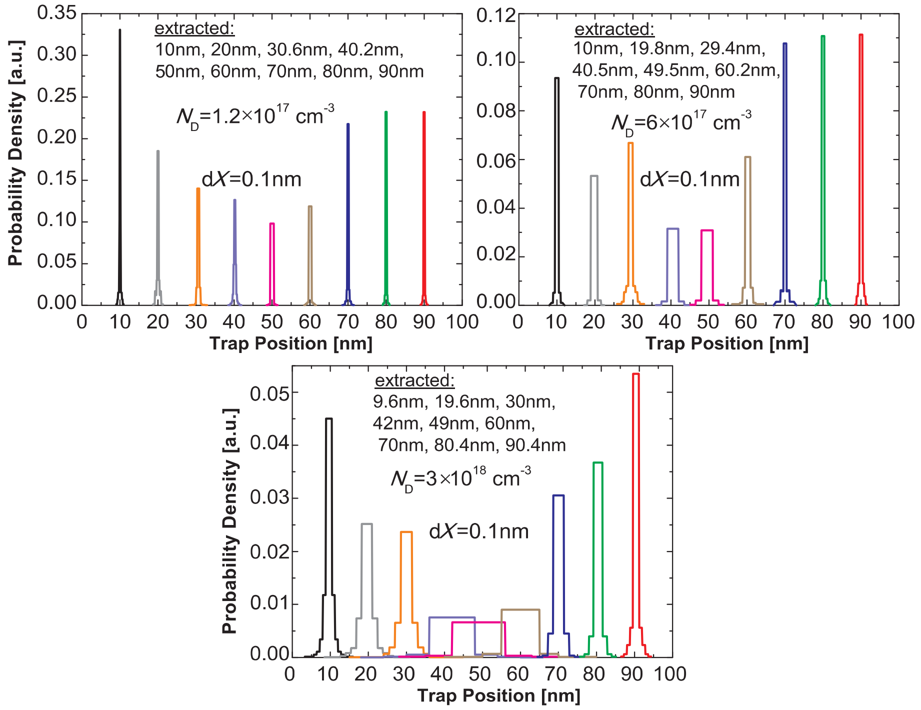

Figure 5.14: The probability densities obtained for similar MOSFETs with $L = 100\,\text{nm}$ and three different channel doping levels. The algorithm is applied to the $\Delta V_{\text{th}}(V_{\text{d}})$ characteristic closest to the mean TCAD curve. Therefore, the results reflect the best accuracy which can be achieved with our trap location technique for different sections of the device channel (benchmark X_{T} is varied between 10 nm and 90 nm using 10 nm steps). In all cases the impact of random dopants is stronger in the middle of the channel. The best overall accuracy is reached for the device with the lowest N_{D}.

TCAD simulations (Figure 5.13) show that the magnitude and drain bias dependence of ΔV_{th} are considerably more sensitive to X_{T} if a device with smaller L is considered. Moreover, the increase in the magnitude of the $\Delta V_{\text{th}}(V_{\text{d}})$ versus X_{T} dependence is stronger compared to the increase in the magnitude of the random dopant fluctuations. This will lead to an even higher precision for ultra-scaled devices. Therefore, below we operate with a relative accuracy given as a percentage of L.

In order to verify the correct functionality of the described trap location technique, we check if the reverse algorithm reproduces the benchmark X_{T}. For this purpose we select one of the $\Delta V_{\text{th}}(V_{\text{d}})$ curves simulated by TCAD for a certain configuration of random dopants. Initially, we examine the curve which is closest to the mean for the considered benchmark X_{T}. This characteristic is used as experimental data for our algorithm. In this way, the optimum accuracy of the method can be evaluated. The procedure has been repeated for numerous lateral defect coordinates along the channel. First we examined devices with different channel doping levels N_{D} and $L = 100\,\text{nm}$. The obtained results, plotted in terms of probability densities, are given in Figure 5.14. In all cases the error in the extracted X_{T} rarely exceeds 2 % of L. However, for the traps located near the middle of the channel, the distributions are broader and their heights lower. This is because the fluctuations of ΔV_{th} induced by random dopants are more significant [27]. The observed behaviour of the probability density can be well described by a Gaussian distribution. The reason for a small deviation is that the precision of the algoritm is limited by several percents of L, especially in the middle of the channel. Another important feature is that the accuracy of our technique decreases with increasing channel doping. This originates from a weaker $\Delta V_{\text{th}}(V_{\text{d}})$

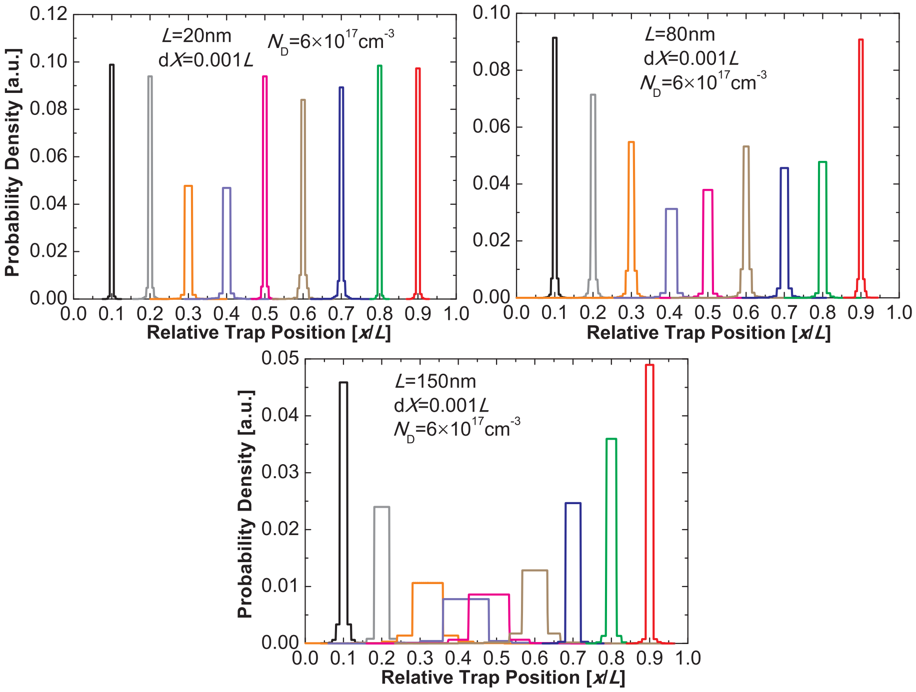

Figure 5.15: The probability densities obtained for similar MOSFETs with $N_\mathrm{D} = 6 \times 10^{17}\,\mathrm{cm}^{-3}$ and three different channel lengths. Similarly to Figure 5.14, the algorithm is applied to the $\Delta V_\mathrm{th}(V_\mathrm{d})$ characteristic which is closest to the mean TCAD curve, while the benchmark trap position is varied in $0.1L$ steps. Also, a small interval $\mathrm{d}X = 0.001\,L$ is used to calculate the probability density. Clearly, the best overall accuracy is reached for the device with the smallest L.

dependence observed for devices with high N_D. Therefore, the impact of random dopants is more pronounced, which leads to a broadening of the distributions.

As a further verification step we attempt to capture the impact of the channel length on the accuracy of our technique by performing a similar procedure for the devices with $N_\mathrm{D} = 6 \times 10^{17}\,\mathrm{cm}^{-3}$ and different L. For a more detailed comparison, in all cases the lateral trap position is varied in $0.1L$ steps, while the probability density is calculated using a small interval $\mathrm{d}X = 0.001\,L$. The obtained results are shown in Figure 5.15. Clearly, the best accuracy is reached for the device with the smallest $L = 20\,\mathrm{nm}$, while for its counterpart with $L = 150\,\mathrm{nm}$ the technique is significantly less accurate. This is because the $\Delta V_\mathrm{th}(V_\mathrm{d})$ dependence becomes significantly stronger for ultra-scaled devices, while the impact of random dopants increases only marginally (cf. Figure 5.13). Also, for the central traps the accuracy is more sensitive to variations of L.

Finally, we examine the device with $L = 100\,\mathrm{nm}$ and $N_\mathrm{D} = 6 \times 10^{17}\,\mathrm{cm}^{-3}$ and repeat the procedure with characteristics which strongly deviate from the mean. In such a case the $\Delta V_\mathrm{th}(V_\mathrm{d})$ curves are considerably displaced from the mean curve, i.e. the deviation of the parameterization coefficients from $\langle P_i \rangle$ is stronger. The obtained probability density distributions are plotted in Figure 5.16. They correspond to border traps situated at $X_\mathrm{T} = 20\,\mathrm{nm}$ (left) and $X_\mathrm{T} = 50\,\mathrm{nm}$ (right). The $\Delta V_\mathrm{th}(V_\mathrm{d})$ characteristics with $P_i = \langle P_i \rangle \pm \sigma_i$ and $\langle P_i \rangle \pm 3\sigma_i$ were examined. One can see that the uncertainty in the extracted lateral trap position for coefficients spread within $[\langle P_i \rangle$-$\sigma_i,\ \langle P_i \rangle$+$\sigma_i]$, which is the most common for the considered devices, does not exceed 5 %. For the case of an extremely strong impact of random dopants, when the $\Delta V_\mathrm{th}(V_\mathrm{d})$ shape strongly deviates from the mean (i.e. $[\langle P_i \rangle$-$3\sigma_i,\ \langle P_i \rangle$+$3\sigma_i]$), the error rarely exceeds 10 %, even if the trap is situated in the middle of the channel. This is still better than our knowledge about

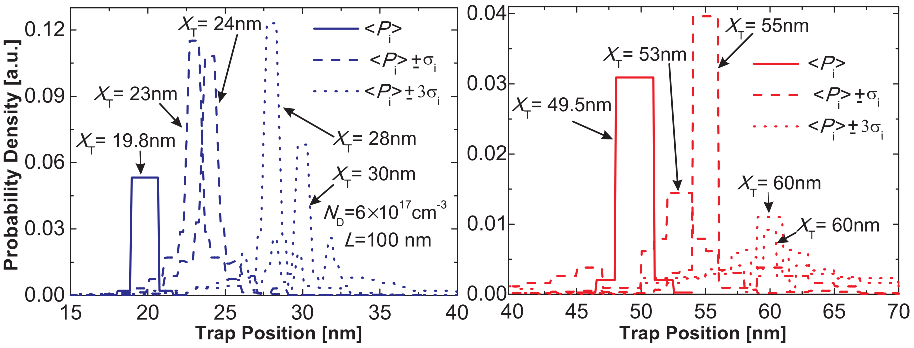

Figure 5.16: The dependence of the accuracy of our trap location technique on the deviation of the $\Delta V_{\text{th}}(V_{\text{d}})$ curve from the mean, i.e. the severity of random dopant configuration. The plotted probability densities ($\text{d}X = 0.1\,\text{nm}$) correspond to border traps situated at $X_{\text{T}} = 20\,\text{nm}$ (left) and $X_{\text{T}} = 50\,\text{nm}$ (right). The lateral defect coordinate extracted for the ideal case ($P_i = \langle P_i \rangle$) is nearly the same as the benchmark X_{T}. For a stronger impact of random dopants ($P_i = \langle P_i \rangle \pm \sigma_i$) the uncertainity is around 3-5 %, and for extremely severe random dopant configurations ($P_i = \langle P_i \rangle \pm 3\sigma_i$) it is around 8-10 %.

technological parameters of the transistors, such as doping profiles, and thus sufficient for the practical application of our method to characterize industrial MOSFETs.

5.5.2 Simplified Technique

The use of TCAD allows for the simulation of the reference data for the trap location technique with rather high accuracy. However, the technique requires substantial computational resources. Therefore, initially we attempted to reproduce the observed behaviour of the $\Delta V_{\text{th}}(V_{\text{d}})$ curves for different X_{T} using a compact model described above. In the next step we found an even more efficient way to simplify our trap location algorithm without a significant loss of accuracy.

This further simplification of our technique is based on the realization that the main information regarding the lateral trap coordinate is given by the slope P_1 and the intercept P_0 of the $\Delta V_{\text{th}}(V_{\text{d}})$ curve. The sign of the former determines whether the trap is at the source or at the drain side of the channel and the magnitude of the latter is responsible for the proximity of the trap to one of the electrodes. Knowing that the mean dependence of P_0 on the lateral trap position X_{T} has a universal shape which is symmetric with respect to the middle of the channel (e.g. our simulations (Figure 5.11) or Refs. [10, 27]), we can approximate it using a Gaussian function (Figure 5.17):

$$P_0(X_{\text{T}}) = P_{0\text{max}} \exp\Big(- \frac{(X_{\text{T}} - \frac{L}{2})^2}{2\sigma^2} \Big), \tag{5.4}$$

where it is assumed that $P_{0\text{max}} = P_0(X_{\text{T}} = L/2)$ and $P_0(X_{\text{T}} = 0) = P_0(X_{\text{T}} = L) = 0$. Based on TCAD simulations performed for devices with different L, the standard deviation σ is found to be proportional to the channel length L as $\sigma = \alpha L$ with $\alpha \approx 0.17$ (Figure 5.17, inset). Therefore, the relative lateral trap position can be estimated by

$$\frac{X_{\text{T}}}{L} = \frac{1}{2} - \text{sign}(P_1)\sqrt{2\alpha^2 \log\Big(\frac{P_{0\text{max}}}{P_0}\Big)}. \tag{5.5}$$

Interestingly, the gate oxide thickness d and channel doping N_{D} mainly impact the values of $P_{0\text{max}}$ which have to be determined experimentally. At the same time, the parameter α is almost independent of these quantities (Figure 5.18).

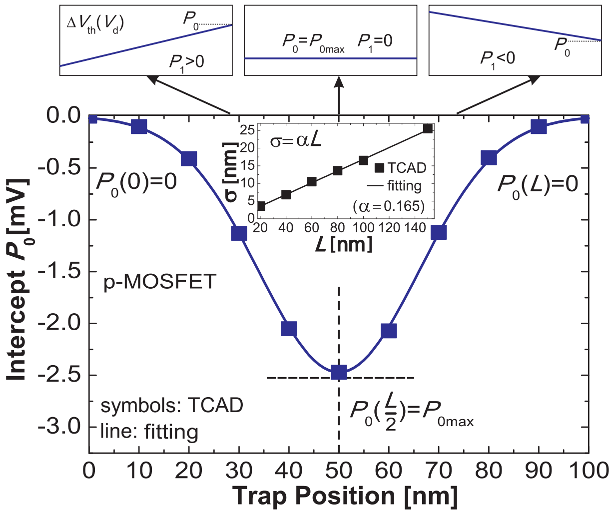

Figure 5.17: Knowing that the intercept $P_0 = \Delta V_{\mathrm{th}}(V_{\mathrm{d}} = 0)$ is zero near the electrodes and has a maximum in the middle of the channel, one can approximate the mean TCAD simulated dependence $P_0(X_{\mathrm{T}})$ with a Gaussian and derive a simple relation for the relative lateral trap position (equation 5.5). The standard deviation σ (equation 5.4) is empirically found to be proportional to L with a coefficient of α (inset). The input data necessary to estimate X_{T} are the value of $P_{0\mathrm{max}}$, which is extracted for the $\Delta V_{\mathrm{th}}(V_{\mathrm{d}})$ curve belonging to a trap situated in the middle of the channel (top center plot), and the values of P_0 for all other curves together with the corresponding slope signs (top right and left plots). Although the mean $P_0(X_{\mathrm{T}})$ curve can be fitted almost exactly, for devices which deviate from the mean some uncertainty is introduced by random dopants.

However, an exact Gaussian fitting of the $P_0(X_{\mathrm{T}})$ dependence is possible only for the case $P_0 = \langle P_0 \rangle \pm n\sigma_0$ with σ_0 being a standard deviation and n constant along the channel. In reality, for each channel coordinate the values of P_0 can be randomly distributed within the interval $[\langle P_0 \rangle$-$3\sigma_0$; $\langle P_0 \rangle$+$3\sigma_0]$ due to the impact of random dopants. Therefore, for some configurations of random dopants, the shape of the $P_0(X_{\mathrm{T}})$ dependences may deviate from a Gaussian, thus introducing some uncertainty. In Figure 5.19 it is illustrated that this uncertainty δX decreases from below 25% for $L = 100\,\mathrm{nm}$ to below 5% for $L = 20\,\mathrm{nm}$. This is because the increase of the magnitude and coordinate dependence of P_0 for devices with smaller L is more significant than the increase of the magnitude of the random dopant fluctuations (cf. Figure 5.13). Therefore, our simplified technique is even more suitable for ultra-scaled devices.

One should note that the exact point at which P_1 changes its sign is also affected by the random dopants and can deviate within 5% from the middle of the channel (cf. Figure 5.11). This may lead to a wrong determination of the channel side at which the trap is situated, but only for central traps. Therefore, some additional uncertainty of around 10% has to be expected for these traps.

The input data necessary to estimate the lateral trap position X_{T} using equation 5.5 can easily be extracted from the experimental results. The value of $P_{0\mathrm{max}}$ is determined only once for each device from the $\Delta V_{\mathrm{th}}(V_{\mathrm{d}})$ characteristic corresponding to the middle of the channel ($X_{\mathrm{T}} = L/2$). This curve typically has a near-zero slope P_1 and the largest among all other values for the intercept P_0; therefore it can easily be discerned. Knowing the value of $P_{0\mathrm{max}}$, one can analyze all other $\Delta V_{\mathrm{th}}(V_{\mathrm{d}})$ curves from the considered dataset in order to extract P_0 and sign(P_1) (Figure 5.17(top)) and then apply equation 5.5 to estimate X_{T}.

The necessary condition for the successful application of the simplified version of our trap lo-

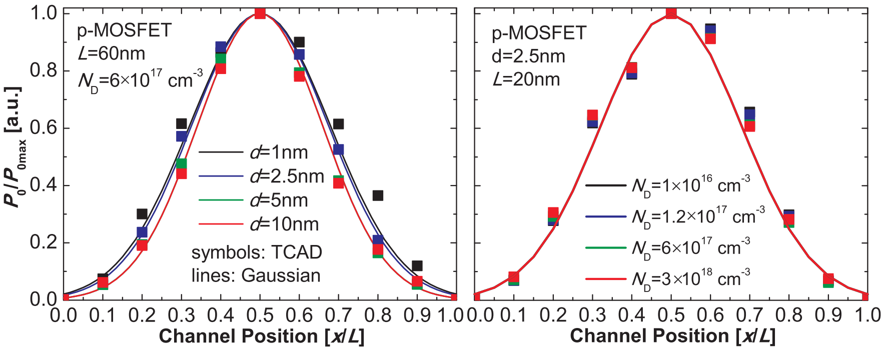

Figure 5.18: Gaussian fitting of the mean TCAD simulated dependences $P_0(X_\mathrm{T})$ normalized to $P_{0\mathrm{max}}$ for different gate oxide thicknesses (left) and doping concentrations (right) allows us to conclude that the parameter α is almost independent of d and N_D which mainly impact the magnitude of $P_{0\mathrm{max}}$.

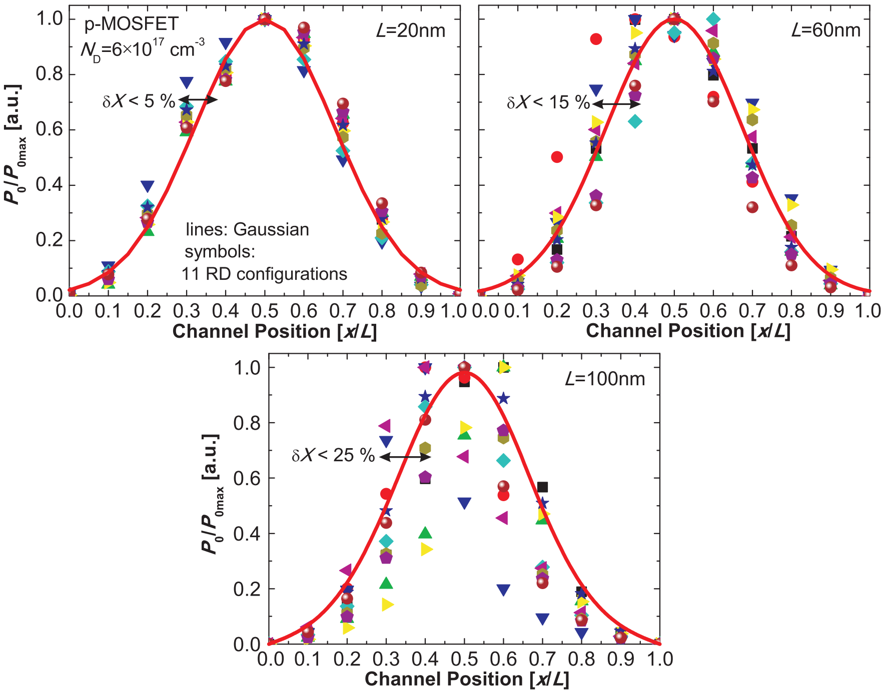

Figure 5.19: Gaussian fitting of the mean TCAD simulated dependences $P_0(X_\mathrm{T})$ normalized to $P_{0\mathrm{max}}$ and overlaid on the related dependences obtained with TCAD for certain random dopant configurations. Clearly, with smaller L the uncertainty is significantly smaller. This makes our simplified technique even better suited for the characterization of border traps in ultra-scaled devices.

cation technique is to have at least one $\Delta V_\mathrm{th}(V_\mathrm{d})$ curve corresponding to $X_\mathrm{T} = L/2$ within the experimental dataset (i.e. with $P_0 = P_{0\mathrm{max}}$ and $P_1 = 0$). However, taking into account that modern nanoscale MOSFETs may contain only a limited number of defects [90], one can imagine a situation when such a curve is not available. In particular, this is the case for our experimental dataset provided in Figure 5.2. In such a case one can perform a visual analysis of all measured $\Delta V_\mathrm{th}(V_\mathrm{d})$ curves in order to find the one which corresponds to the trap situated closest to the middle of the channel. Such a curve will have the largest P_0 and at the same time the smallest P_1. In the case of Figure 5.2, this will be trap A5. Then, this $\Delta V_\mathrm{th}(V_\mathrm{d})$ curve must be used to determine the value of $P_{0\mathrm{max}}$, which allows us to extract the positions of all other traps using

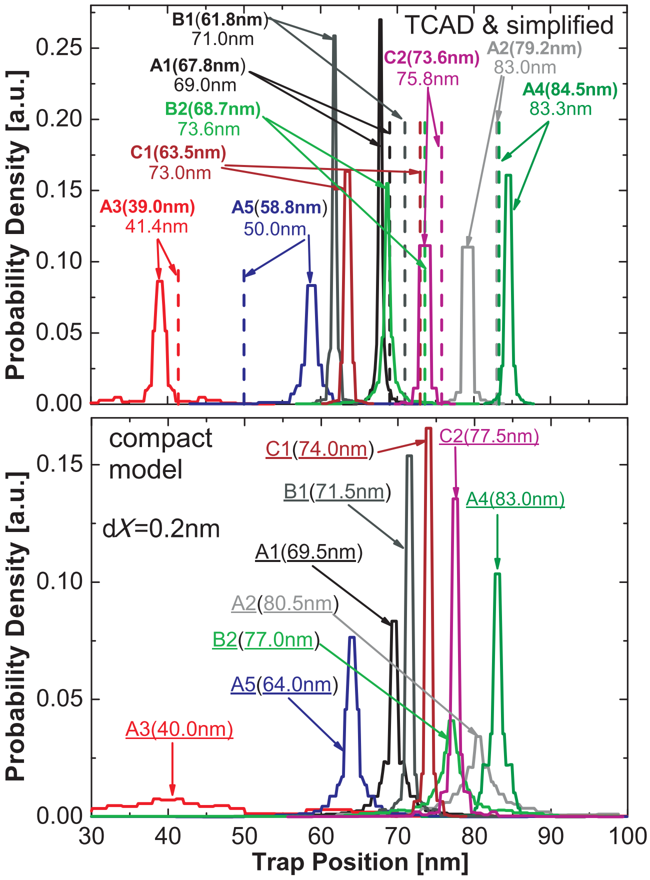

Figure 5.20: The probability densities of the lateral trap position calculated for small intervals $\mathrm{d}X = 0.2\,\mathrm{nm}$ for the experimental data given in Figure 5.2. Top: The results obtained using TCAD data (solid lines) are compared to the estimations done using the simplified method (dashed). The difference in the extracted values of X_T is always below 10 % of the channel length (100 nm). Bottom: Similar distributions obtained by substituting the TCAD data with compact model results in our trap location algorithm. The deviation of the extracted X_T from their counterparts obtained using TCAD results is also less than 10 % of L in most cases.

equation 5.5. Although some additional inaccuracy may be introduced, it will not be significant for the case where the reference curve used to extract $P_{0\mathrm{max}}$ corresponds to a trap situated not very far from the middle of the channel. Also, one should note that in a particular situation of Figure 5.2 the trap A3 could also be used as a reference to extract P_0. However, the universality of equation 5.5 requires the selection of the trap which has a maximum intercept P_0.

Alternatively, one can perform a visual qualitative analysis of the experimental traces (e.g. Figure 5.2) and immediately recognize the $\Delta V_\mathrm{th}(V_\mathrm{d})$ curves which correspond to traps situated at the source side ($P_1 > 0$) and the drain side ($P_1 < 0$) of the channel. Moreover, traps with a larger P_0 are situated closer to the middle of the channel while those with a smaller P_0 are closer to the contact regions.

5.5.3 Results and Discussions

We have applied our trap location technique to the experimental results given in Figure 5.2 (p-MOSFET, $L \approx 100\,\mathrm{nm}$, $N_\mathrm{D} \approx 6 \times 10^{17}\,\mathrm{cm}^{-3}$) and extracted the positions of all nine detected individual traps. First, we employed the results of our TCAD simulations as a reference. The obtained probability density distributions are plotted in Figure 5.20(top). The results show that the traps can be located with a rather high accuracy inside narrow intervals. The width of these intervals is typically related to the impact of the random dopants. For this reason, the obtained distributions are broader for traps close to the middle of the channel where the device is more sensitive to random dopants. In the same plot, the values of X_T estimated using our simplified trap location method (equation 5.5) are given. The value of $P_{0\mathrm{max}}$ has been estimated from the $\Delta V_\mathrm{th}(V_\mathrm{d})$ curve corresponding to the trap A5 which is the closest to $X_\mathrm{T} = L/2$. Although the simplified technique does not allow for any probability calculations and leads to a single value of X_T, the results are very similar to those obtained using TCAD data. The typical difference in the extracted X_T values in all cases is below $10\,\%$ of the channel length, while accuracy is expected to improve for smaller devices. Therefore, taking into account that the TCAD simulations require several weeks of cluster simulations and that the simplified algorithm gives the results in several minutes, we conclude that the substitution of the precise algorithm with the simplified one is quite appropriate if one needs to increase efficiency.

Another possibility to simplify the entire trap location procedure is to replace the TCAD simulations by the compact model in our general algorithm (Figure 5.20(bottom)). However, this still requires some computational resources, while the results are typically similar to those obtained using the simplified technique. Therefore, we conclude that the use of the compact model is reasonable mostly for the physical interpretation of the TCAD and experimental results.

Finally, we remark that although the entire above description is based on the results obtained for p-MOSFETs, it is obvious that our trap location technique can be used for n-MOSFETs as well. The main point to note is that in the case of n-MOSFETs, ΔV_th is positive. However, the dependences of the parameterization coefficients of $\Delta V_\mathrm{th}(V_\mathrm{d})$ curves versus X_T are similar to those observed for p-MOSFETs.

5.6 Chapter Conclusions

We have presented a detailed analysis of the impact of charged single defects on the performance of modern nanoscale MOSFETs. Based on the obtained results a precise method for the extraction of the lateral position of traps in nanoscale MOSFETs has been suggested. The main advantage of our technique compared to the ones reported previously is that it fully accounts for the impact of random dopants. Our approach exploits the fact that the slope and curvature of the trap-induced threshold voltage shift versus drain bias of a single trap is considerably less sensitive to the random dopants as opposed to the lateral trap position. Therefore, we have demonstrated that the lateral defect coordinate can be estimated with a precision of several percents of the channel length. In addition, we have proposed a compact model that allows for the capture of the essence of the impact of charged trap on the device performance and is also suitable for calculation of the reference data for the algorithm without running time-consuming TCAD simulations. Moreover, we have introduced a simple expression which allows for the estimation of the lateral trap position directly from the experimental data and have demonstrated that the extraction uncertainty decreases for devices with smaller channel length. Therefore, the simplified version of our trap location technique allows us to avoid both time-consuming TCAD simulations and the compact model. This considerably increases the efficiency of the entire procedure. Finally, we have demonstrated the applicability of all modifications of our trap location technique using experimental TDDS data.

6 Reliability of Graphene FETs

Miniaturization of modern MOSFETs with simultaneous improvement of their performance presents a crucial problem for modern microelectronics. Searching for a solution to this problem creates a high demand for next-generation channel materials capable of being used as alternatives to Silicon. In the meantime, special attention is being paid to 2D materials capable of maintaining both a decrease in the dimensions and improvement in the main characteristics of industrial MOSFETs. Within these materials, graphene has attracted the most considerable amount of attention. This is due to its unique physical and electrical properties, such as an extremely high room-temperature carrier mobility [50, 133] and a high saturation velocity [36]. Moreover, graphene is remarkably compatible with standard CMOS technology [177]. This is especially important for enhancement of the performance and functionality of advanced microelectronic devices and, consequently, silicon integrated circuits. At the same time, practical realization of devices based on any new material creates a demand for characterization of their reliability. Therefore, this chapter is devoted to the investigation of the reliability of graphene FETs. Similarly to the case of Si MOSFETs described above, this study will be associated with the analysis of the impact of charged traps on device performance. However, the typical dimensions of graphene field effect transistors (GFETs) are still in the micrometer range, while the technology of their fabrication is still far below Si standards. Hence, reliability of these devices is determined by the impact of continuously distributed charged traps rather than single discrete defects.

6.1 Introduction

Since the discovery of graphene in 2004 [133], many successful attempts at fabricating GFETs [108, 112, 127, 126, 74, 40] and related electronic devices [176, 192] have been undertaken. Beyond such demonstrations of device functionality for potential applications, process integration issues, such as low resistance electrical contacts and reliable dielectric interfaces with graphene, are urgent topics requiring further research to assess the true potential of graphene technology. In particular, a rigorous method for the quantification of dielectric quality and reliability in terms of the charged trap density is needed. Few attempts have been made to try to describe dielectric reliability in terms of bias-temperature instability (BTI) [82, 113, 116, 117], one of the key figures of merit for reliability in Si MOSFETs [80, 7]. However, despite significant advances in the overall understanding of GFET reliability, none of these works reports a systematic method to benchmark BTI dynamics in GFETs. Also, no analysis has been attempted with respect to hot-carrier degradation (HCD), which is another key reliability issue in Si MOSFETs [171].

In the course of this work we perform a detailed study of both BTI and HCD on the high-k top gate of double-gated GFETs and compare the dynamics of these phenomena. We demonstrate that despite the defect densities measured for GFETs are still considerably larger than those known from Si technologies, the dynamics of BTI are in general comparable. This allows us to understand BTI in GFETs using standard methods previously developed for Si technologies if the degradation dynamics are expressed in terms of a Dirac point voltage shift as opposed to an ill-defined threshold voltage shift. Moreover, for some stress conditions HCD in GFETs can also be benchmarked using the same methods which allows for quantitative estimation of the graphene/dielectric interface quality. Also, we compare the BTI dynamics on the high-k top gate and SiO_2 back gate of double-gated GFETs. Finally, we study the impact of HCD with different polarity of HC and bias components on defect density and mobility, and investigate the temperature dependence of the related interaction between different defects. Based on these findings, we show that the resulting changes in the charged trap density and carrier mobility are correlated.

6.2 Investigated Devices: Fabrication and Basic Characteristics

We perform our studies on double-gated GFETs with Al_2O_3 as a top gate insulator and SiO_2 as a back gate insulator. The channel length L of these devices is either 1, 2 or 4 μm, while the width W can vary between 4 and 80 μm. The oxide thickness is 25 nm for Al_2O_3 and 1800 nm for SiO_2. However, in some devices 92 nm thick back gate oxide was used, which allowed us to observe back gate BTI at reasonable stress voltages. An isometric view and a schematic cross-section of the devices used as test benches are given in Figure 6.1.

The GFETs were fabricated at the group of Prof. Max Lemme on thermally oxidized silicon chips with a given silicon dioxide thickness. First, a contact hole to the substrate (i.e. back gate) was etched through the SiO_2 using reactive ion etching, and subsequently filled with aluminum using thermal evaporation and a self aligned lift-off process. Contact pads were then embedded into the SiO_2 layer in order to form source and drain contacts as well as two extra contact pads for contact and sheet resistance measurements. The contact pads were made of gold (Au) and evaporated titanium (Ti) to improve adhesion to the SiO_2 layer. Chemical vapour deposited (CVD) graphene was then transferred from copper foil to the chip using a well-developed wet graphene transfer process [177]. For this, a polymer layer was first spun onto the graphene on one side of the copper. The graphene was etched from the other side of the copper using O_2 plasma. The remaining copper foil with graphene and polymer was then placed, copper side down, into ferric chloride. This etched away the copper layer leaving the graphene and polymer floating on the surface. Next, the graphene was further processed by fishing it out of the ferric chloride using a dummy wafer and placing it into a series of water and hydrochloric acid (HCl) solutions. After cleaning, the graphene was transferred in a similar manner onto the chip and the polymer layer was removed with chloroform. Once the graphene was transferred to the wafer, transistor channels were structured using standard photolithography and O_2 plasma. The top gate dielectric was formed by atomic layer deposition (ALD), utilizing an evaporated aluminum seed layer of 3 nm which was oxidized to form a 5 nm layer of Al_2O_3. A 20 nm thick film of Al_2O_3 was then deposited on top of the seed layer using ALD. The Al_2O_3 was etched using buffered hydrofluoric acid (BHF) in the areas of the contact pads. Finally, Ti/Au top gate electrodes were deposited onto the devices using metal evaporation and a lift-off process.

For the initial check of the device performance, we investigated the output and transfer characteristics of our GFETs. As shown in Figure 6.2, these basic device characteristics correspond to those published previously [82]. In particular, the top gate transfer characteristics measured at different back gate biases exhibit a modulation of the Dirac point voltage V_D by the back gate bias V_bg. Also, a hysteresis related to charging/discharging of fast oxide traps is present on the I_d-V_tg curves. The output characteristics measured at different top gate biases V_tg show a rather strong saturation at high drain bias V_d and also exhibit some kinks for negative V_tg. The origin of the latter is associated with a change of the conductivity type in some channel regions,

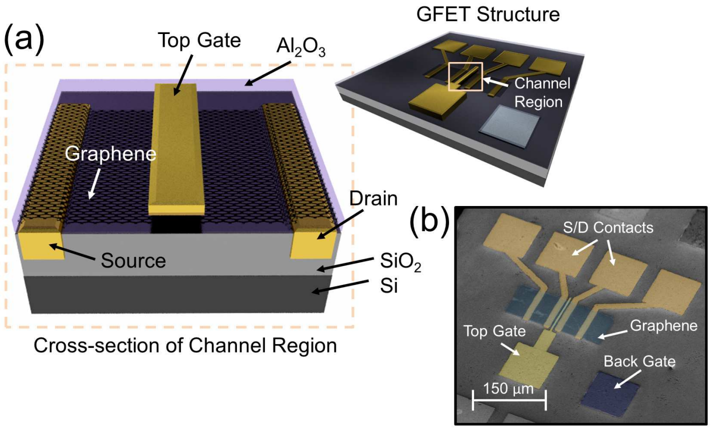

Figure 6.1: (a) Schematic layout of the double-gated single-layer GFET and a cross-section of the channel region. The graphene channel is sandwiched between Al_2O_3 as a top gate insulator and SiO_2 as a back gate insulator. (b) Top view of the investigated double-gated GFET obtained using scanning-electron microscopy (SEM). The top gates and source/drain pads are made of Ti/Au and the back gates of Al.

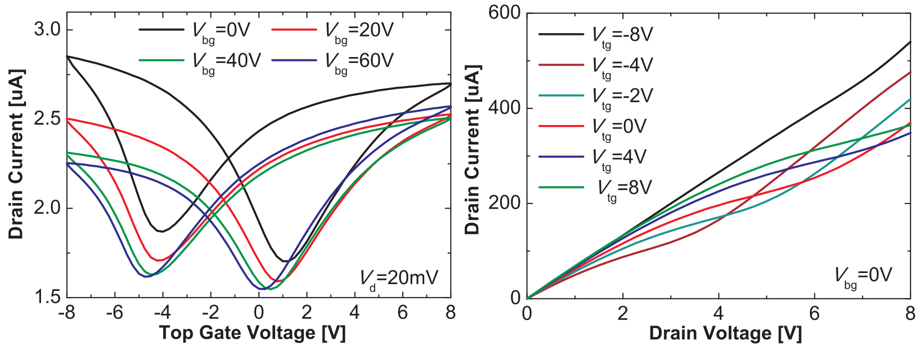

Figure 6.2: Left: The top gate transfer (I_d-V_tg) characteristics of the double gated GFETs show a hysteresis due to charging/discharging of fast traps as well as a modulation of the Dirac point position by V_bg, in agreement with literature [82]. Right: Similarly to [125], the output (I_d-V_d) characteristics show signs of saturation at high V_d and some kinks related to ambipolar channel effects at negative V_tg.

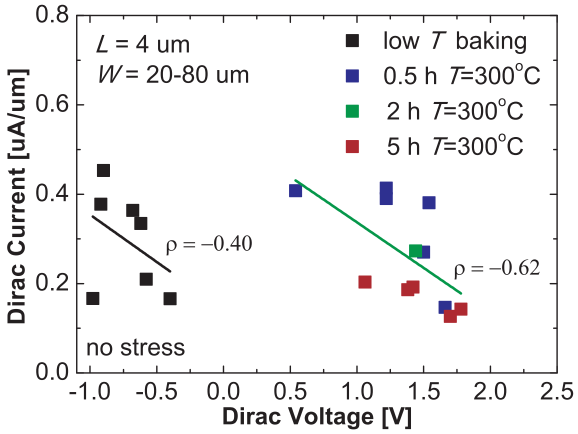

Figure 6.3: Device-to-device variability is determined by the distribution of the current normalized to W and voltage values at the Dirac point. After baking the devices at 300 °C in a H_2/He mixture, variability is reduced and the absolute value of the correlation coefficient ρ increases.

which is known as ambipolar channel behaviour [125] and presents a counterpart of pinch-off behaviour in Si MOSFETs.

However, in our first measurements significant device-to-device variability could be observed which prevented a systematic reliability study. This variability is determined by the distribution of the current normalized to the channel width W and voltage values at the Dirac point. It can be described by the trend line with a certain correlation coefficient ρ (Figure 6.3). In the spirit of the standard forming-gas anneal of Si MOSFETs [116], the devices were baked at $T = 300\,^\circ\mathrm{C}$ in a H_2/He mixture. As shown in Figure 6.3, this allowed us to obtain a significant decrease in device-to-device variability. Namely, after baking, the distribution of the current and voltage at the Dirac point becomes narrower, while the correlation coefficient increases. At the same time, V_D is shifted towards positive values, which suggests a change in the charged trap density. As such, this thermal treatment before electrical characterization appears to be essential for reliability studies, which require the comparison of degradation data taken on various devices. Also, to the best of the author's knowledge, such small variability has so far not been reported for GFETs.

6.3 Experimental Technique

Our experimental technique for benchmarking reliability issues in GFETs is based on the measurements of the gate transfer characteristics, which are known to be sensitive to the detrimental impact of the environment[117, 160]. Therefore, all measurements were performed in a vacuum (5×10^{-6}–10^{-5} torr).

First we studied the impact of BTI stress on the top gate transfer characteristics in order to benchmark the BTI dynamics in GFETs. Thus, according to our technique, a constant BTI stress V_tg applied on the top gate for a certain stress time t_s is followed by measuring the transfer characteristics corresponding to different recovery stages, which are measured as a function of the relaxation time t_r. Taking into account the logarithmic time dependence of the BTI degradation and recovery, the number of experimental points used is larger within the first minutes after the stress. As will be discussed below, we express the BTI dynamics in terms of a horizontal shift of the Dirac point ΔV_D rather than an ill-defined threshold voltage V_th [113, 116, 117]. The main technical features of our method are the following: first, the voltages V_bg and V_d are set to zero during stress and narrow (2–3 V) V_tg intervals are used during the I_d-V_tg measurements. This is necessary to minimize the impact of any additional degradation factors (e.g. hot carrier degradation). Second, the results for different stress conditions and temperatures are obtained either on the same device or on a group of devices with negligible variability. For this reason subsequent measurement rounds are separated by an intermediate baking step of the devices in a H_2/He mixture at $T = 300\,^\circ\mathrm{C}$, which in most cases leads to almost complete recovery and also decreases device-to-device variability. Third, because of large magnitudes of ΔV_D, the measurements on each device are repeated using increasing stress times $t_\mathrm{s} = 1$, 10, 100, 1000 and 10000 s while keeping $V_\mathrm{tg} - V_\mathrm{D}(t_\mathrm{s}) \approx$ const. The latter is necessary to sustain an approximately constant oxide field during all experiments, making the obtained results easier to interpret. Also, to further simplify the analysis, the gate transfer characteristics were always measured at $V_\mathrm{d} = 20\,\mathrm{mV}$.

However, the use of $V_\mathrm{tg} - V_\mathrm{D}(t_\mathrm{s}) \approx$ const should be essential when the waiting time between the experiments with different t_s is not enough for a nearly complete recovery after the previous stress. In this case the difference between the sets of BTI recovery traces measured using the stress conditions $V_\mathrm{tg}(t_\mathrm{s}) = \mathrm{const}$ and $V_\mathrm{tg} - V_\mathrm{D}(t_\mathrm{s}) \approx$ const can be significant. Conversely, if the

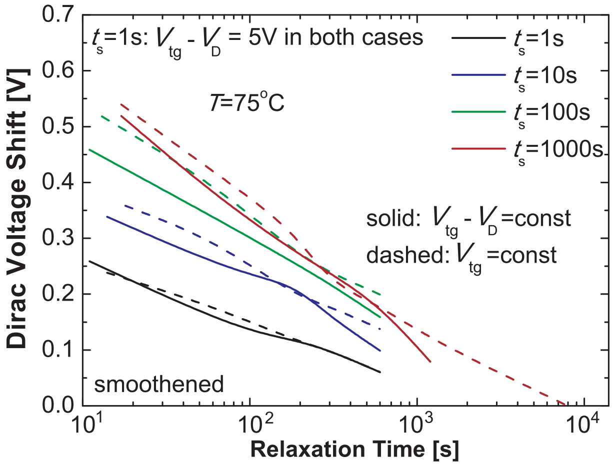

Figure 6.4: The PBTI recovery traces measured on the same device using two different stress bias conditions. A significant saturation at larger t_s is clearly visible for the case of $V_{tg}(t_s) = \text{const}$. This is why the use of V_{tg} - $V_D(t_s) \approx \text{const}$ is essential when the recovery is not complete, making our technique universal and suitable for application even for short-term BTI experiments.

waiting time in between the experiments with different t_s is large enough for a significant degree of recovery, the use of just $V_{tg}(t_s) \approx \text{const}$ should be enough.

In order to compare the two stress conditions and justify our statement about the universality of using V_{tg} - $V_D(t_s) \approx \text{const}$, we performed the following experiment. First, a typical set of PBTI traces was measured using $V_{tg}(t_s) = \text{const}$. Next, similar measurements using V_{tg} - $V_D(t_s) \approx \text{const}$ were performed on the same device. The temperature $T = 75\,^\circ\text{C}$ was maintained during all experiments, which in around two hours resulted in complete recovery after the first set of measurements, even without high-temperature baking. To highlight the difference between the two techniques, recovery after PBTI stress with a certain t_s was monitored only for 10 minutes.

The results given in Figure 6.4 demonstrate the difference between the two techniques which is due to incomplete recovery on each step. A nearly complete reproducibility of the first trace is obvious because the initial stress conditions in the two experiments were identical (i.e. V_{tg} - $V_D = 5\,\text{V}$, $t_s = 1\,\text{s}$). However, at larger t_s, the distances between the traces obtained using the technique with $V_{tg}(t_s) = \text{const}$ show some saturation. The reason is that in this case the resulting oxide field ($F_{ox} = (V_{tg}$ - $V_D)/d_{tg}$) decreases due to incomplete recovery. This is contrary to the case when V_{tg} - $V_D(t_s) \approx \text{const}$ is readjusted on each t_s step. Another important feature which testifies to the decrease in F_{ox} in the case of $V_{tg}(t_s) = \text{const}$ is that the corresponding recovery traces lie higher than for V_{tg} - $V_D(t_s) \approx \text{const}$. This suggests slower recovery in the former case, which is typical for lower stress biases (note that $t_r = 0$ extrapolation is not done here). Therefore, the use of the V_{tg} - $V_D(t_s) \approx \text{const}$ condition makes our experimental technique universal and suitable for application even if the recovery is rather weak. Use of this condition should allow us to avoid distortion of the experimental results and simplify benchmarking of BTI dynamics in GFETs using general models developed for Si technologies.

However, some of our studies require investigation of the dependence of the BTI dynamics on the stress oxide field. In this case subsequent stress/recovery rounds with constant t_s and either increasing V_{tg} - V_D and $V_{bg} = 0$ (top gate BTI) or increasing V_{bg} - V_D and $V_{tg} = 0$ (back gate BTI) were used.

The experimental technique described above was also extended for benchmarking the dynamics of HCD in GFETs. This was done simply by using constant non-zero V_d during each of the stress rounds. However, in some cases we employed a similar technique with a constant t_s and subsequent stress/recovery rounds with increasing $V_\mathrm{d} = 0...\pm 12\,\mathrm{V}$. This was necessary to capture the dependence of the degradation/recovery dynamics on the magnitude of the HCD component. In the spirit of our general technique with increasing t_s, V_tg - $V_\mathrm{D}(V_\mathrm{d}) \approx$ const and $V_\mathrm{bg} = 0$ were maintained for all stress rounds.

Therefore, our experimental technique allows us to study the degradation/recovery dynamics under different magnitudes and polarities of hot carrier and bias stress contributions. Similarly to NBTI and PBTI, the impact of hot carrier contribution with $V_\mathrm{d} > 0$ is designated as PHCD, while its counterpart with $V_\mathrm{d} < 0$ is called NHCD. If both hot carrier and bias stress contribution act in conjuction, one can have NBTI-PHCD, NBTI-NHCD, PBTI-PHCD or PBTI-NHCD. The impact of all these issues on the device performance are studied below using our experimental technique.

6.4 Modeling of Carrier Distribution in GFET Channel

A precise modeling of carrier transport in GFETs is significantly different compared to Si technologies. This is because graphene is a 2D material with zero bandgap and linear band edge profiles, which requires radical modifications of the general models used in modern device simulators. Therefore, most of the literature reports provide only quite simplified compact models, allowing for the reproduction of basic characteristics of GFETs [98, 196]. However, interpretation of the experimental reliability characteristics requires more general information on the channel distribution of the surface potential and carrier concentrations during the stress. In this context, implementation of the drift-diffusion (DD) model for the case of GFETs is quite appropriate. The first attempt to adjust generally known DD equations for GFETs was done in [4]. However, the authors of [4] consider a number of non-trivial issues which significantly complicate the model, while at the same time are particularly important for devices based on graphene with artificially created bandgap. On the other hand side, in [4] there is a lack of information on the boundary conditions used, while the motivation of [4] is not linked to a reliability study.

In the following, we provide a simple implementation of the DD model for GFETs, allowing for qualitative analysis of the surface potential distributions and carrier concentrations under different stress conditions. At the same time, we introduce and discuss different types of boundary conditions for carrier concentrations corresponding to different stress configurations. This is especially important for the linking of our simulation results with the experimental reliability study of GFETs.

The DD equations for electron and hole current densities, J_n and J_p are

$$J_n = qD_n\frac{dn}{dx} - qn\mu_n\frac{d\psi}{dx} = qD_n\frac{dn}{dx} + qn\mu_nF \tag{6.1}$$

and

$$J_p = -qD_p\frac{dp}{dx} - qp\mu_p\frac{d\psi}{dx} = -qD_p\frac{dp}{dx} + qp\mu_pF, \tag{6.2}$$

where n, p, μ_n and μ_p are the electron and hole concentrations and mobilities, respectively, F and ψ are the channel electric field and electrostatic potential, respectively, and the coordinate x expresses the position along the graphene channel. For the diffusion coefficients D_n and D_p

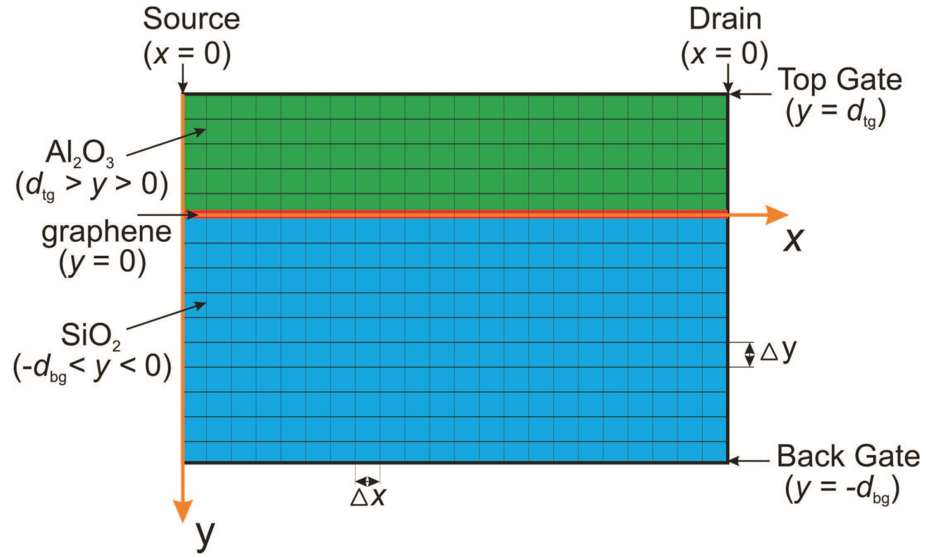

Figure 6.5: Schematic representation of double-gated GFET meshed for application of the Scharfetter-Gummel scheme [13].

we use the definition from [196] which reads

$$D_n = D_p = \frac{v_F^2 \tau_{tr}}{2} = \frac{v_F l}{2} \tag{6.3}$$

with $v_\mathrm{F} = 10^8$ cm/s being the Fermi velocity in graphene and $\tau_\mathrm{tr} = 10$ ps the transport relaxation time, which determines the carrier mean free path $l = v_\mathrm{F}\tau_\mathrm{tr}$. Contrary to a more general definition of the diffusion coefficient in graphene given in [4], here the dependence of the diffusion coefficients on carrier concentrations is not accounted for. However, according to our experience, this significantly improves the convergence while still leading to reasonable qualitative results.

The corresponding continuity equations read

$$\frac{dJ_n}{dx} = \frac{np - n_\mathrm{eq}p_\mathrm{eq}}{n + p + 2\sqrt{n_\mathrm{eq}p_\mathrm{eq}}} \tag{6.4}$$

and

$$\frac{dJ_p}{dx} = -\frac{np - n_\mathrm{eq}p_\mathrm{eq}}{n + p + 2\sqrt{n_\mathrm{eq}p_\mathrm{eq}}}. \tag{6.5}$$

Here the terms on the right account for the thermal generation of carriers [4] and the equilibrium carrier concentrations are

$$n_\mathrm{eq} = p_\mathrm{eq} = \frac{\pi}{6}\left(\frac{k_\mathrm{B}T}{\hbar\, v_\mathrm{F}}\right)^2. \tag{6.6}$$

According to the drift-diffusion theory, the equations above have to be solved self-consistently with the Poisson equation, which in our case is

$$\frac{d^2\psi}{dx^2} + \frac{d^2\psi}{dy^2} = -\frac{qD_\mathrm{f}(y)}{\varepsilon(y)}. \tag{6.7}$$

Obviously, the concentration of fixed charges D_f and dielectric constant ε depend on the device segment, which is determined by the coordinate y perpendicularly to the channel.

In order to solve equations 6.4, 6.5 and 6.7, we perform their discretization using the Scharfetter-Gummel scheme [13]. The schematic layout of the meshed device is shown in Figure 6.5. The coordinate grid used in our simulations is created by discretizing the x and y coordinates as follows:

$$x_i = i\frac{L}{N_{\mathrm{X}}}, \qquad i = 0\ldots N_{\mathrm{X}}; \tag{6.8}$$

$$y_j = -d_{\mathrm{bg}} + j\frac{d_{\mathrm{bg}}}{N_{\mathrm{Ybg}}}, \qquad j = 0\ldots N_{\mathrm{Ybg}}; \tag{6.9}$$

$$y_j = (j - N_{\mathrm{Ybg}})\frac{d_{\mathrm{tg}}}{N_{\mathrm{Ytg}}}, \qquad j = N_{\mathrm{Ybg}}\ldots \mathrm{N}_{\mathrm{Ybg}} + N_{\mathrm{Ytg}}. \tag{6.10}$$

Therefore, N_{X}+1 is the number of x points, while N_{Ybg}+1 and N_{Ytg}+1 are the numbers of y points within the back and top gate oxides, respectively. Taking into account a significant difference in the oxide thicknesses d_{bg} and d_{tg}, we adjust N_{Ybg} and N_{Ytg} so as to make the discretization step $\Delta y = y_{\mathrm{i+1}}$-$y_{\mathrm{i}}$ constant. At the same time, the step $\Delta x = x_{\mathrm{i+1}}$-$x_{\mathrm{i}}$ is not necessarily equal to Δy.

Thus, the Poisson equation is discretized as follows:

$$\begin{aligned}
\frac{\psi_{i+1,j} - \psi_{i,j}}{\Delta x^2} + \frac{\psi_{i,j+1} - 2\psi_{i,j} + \psi_{i,j-1}}{\Delta y^2} &= -\frac{qD_{\mathrm{bg}}}{\varepsilon_{\mathrm{SiO2}}},\\
i = 0, \qquad j &= 1\ldots N_{\mathrm{Ybg}} - 1;\\
\frac{\psi_{i+1,j} - 2\psi_{i,j} + \psi_{i-1,j}}{\Delta x^2} + \frac{\psi_{i,j+1} - 2\psi_{i,j} + \psi_{i,j-1}}{\Delta y^2} &= -\frac{qD_{\mathrm{bg}}}{\varepsilon_{\mathrm{SiO2}}},\\
i = 1\ldots N_{\mathrm{X}} - 1, \qquad j &= 1\ldots N_{\mathrm{Ybg}} - 1;\\
\frac{\psi_{i-1,j} - \psi_{i,j}}{\Delta x^2} + \frac{\psi_{i,j+1} - 2\psi_{i,j} + \psi_{i,j-1}}{\Delta y^2} &= -\frac{qD_{\mathrm{bg}}}{\varepsilon_{\mathrm{SiO2}}},\\
i = N_{\mathrm{X}}, \qquad j &= 1\ldots N_{\mathrm{Ybg}} - 1;
\end{aligned} \tag{6.11}$$

$$\begin{aligned}
\frac{\psi_{i+1,j} - \psi_{i,j}}{\Delta x^2} + \frac{\psi_{i,j+1} - 2\psi_{i,j} + \psi_{i,j-1}}{\Delta y^2} &= -\frac{qD_{\mathrm{tg}}}{\varepsilon_{\mathrm{Al2O3}}},\\
i = 0, \qquad j &= N_{\mathrm{Ybg}} + 1\ldots N_{\mathrm{Ybg}} + N_{\mathrm{Ytg}} - 1;\\
\frac{\psi_{i+1,j} - 2\psi_{i,j} + \psi_{i-1,j}}{\Delta x^2} + \frac{\psi_{i,j+1} - 2\psi_{i,j} + \psi_{i,j-1}}{\Delta y^2} &= -\frac{qD_{\mathrm{tg}}}{\varepsilon_{\mathrm{Al2O3}}},\\
i = 1\ldots N_{\mathrm{X}} - 1, \qquad j &= N_{\mathrm{Ybg}} + 1\ldots N_{\mathrm{Ybg}} + N_{\mathrm{Ytg}} - 1;\\
\frac{\psi_{i-1,j} - \psi_{i,j}}{\Delta x^2} + \frac{\psi_{i,j+1} - 2\psi_{i,j} + \psi_{i,j-1}}{\Delta y^2} &= -\frac{qD_{\mathrm{tg}}}{\varepsilon_{\mathrm{Al2O3}}},\\
i = N_{\mathrm{X}}, \qquad j &= N_{\mathrm{Ybg}} + 1\ldots N_{\mathrm{Ybg}} + N_{\mathrm{Ytg}} - 1;
\end{aligned} \tag{6.12}$$

$$\begin{aligned}
(\varepsilon_{\mathrm{Al2O3}} + \varepsilon_{\mathrm{SiO2}})\frac{\psi_{i+1,j} - 2\psi_{i,j} + \psi_{i-1,j}}{2\Delta x^2} + \varepsilon_{\mathrm{Al2O3}}\frac{\psi_{i,j+1} - \psi_{i,j}}{\Delta y^2} + \varepsilon_{\mathrm{SiO2}}\frac{\psi_{i,j-1} - \psi_{i,j}}{\Delta y^2} &=\\
-q(D_{\mathrm{tg}} + D_{\mathrm{bg}} + p_{\mathrm{eq}} - n_{\mathrm{eq}}), \qquad i = 1\ldots N_{\mathrm{X}} - 1, \qquad j &= N_{\mathrm{Ybg}}.
\end{aligned} \tag{6.13}$$

Equations 6.11, 6.12 and 6.13 correspond to the back gate oxide, the top gate oxide and the graphene channel, respectively. The quantities D_{bg} and D_{tg} express 2D densities of fixed charges at the graphene/SiO$_2$ and graphene/Al$_2$O$_3$ interfaces. A difference compared to implementation in [4] is that we consider the full discretization of the Poisson equation in graphene (equation 6.13) instead of using just a first order differential equation relating the electrostatics across the channel.

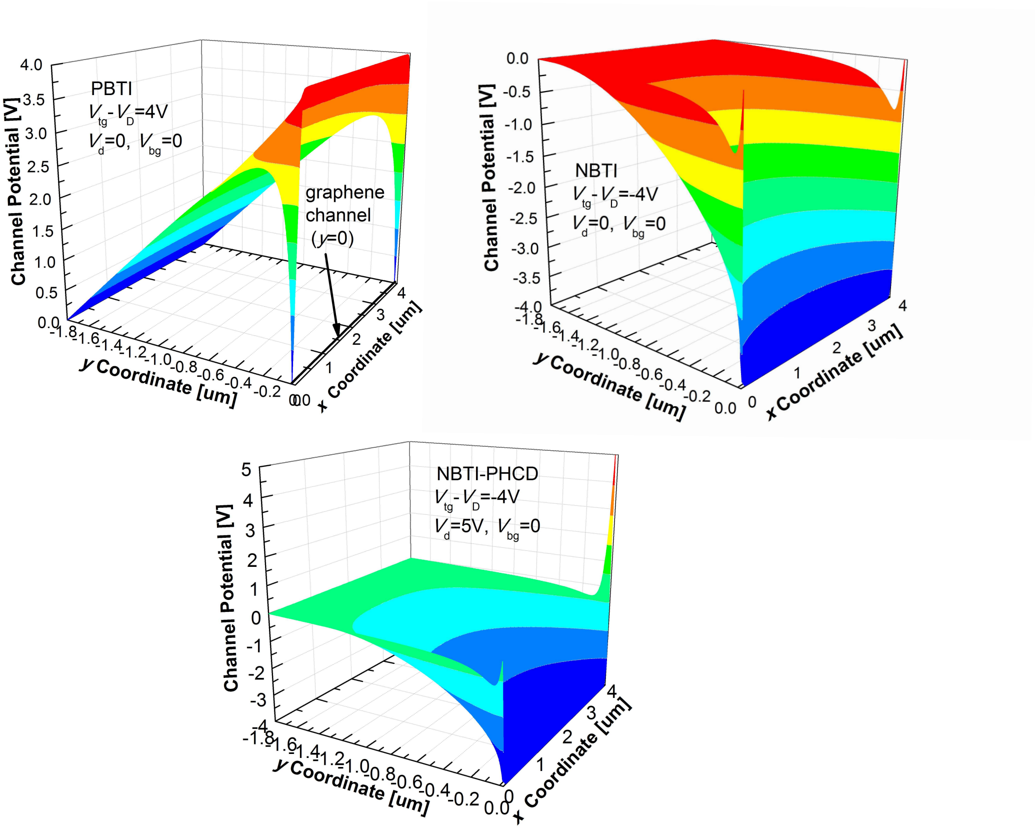

Figure 6.6: Potential distributions simulated for double-gated GFET with $L = 4\,\mu\text{m}$, $d_{\text{bg}} = 1.8\,\mu\text{m}$ and $d_{\text{tg}} = 25\,\text{nm}$. The results correspond to PBTI, NBTI and NBTI-PHCD stress conditions.

In order to solve equations 6.11, 6.12 and 6.13, we employ the following Dirichlet boundary conditions

$$\begin{aligned} \psi_{0,N_{\text{Ybg}}} &= 0, \qquad \psi_{N_{\text{X}},N_{\text{Ybg}}} = V_{\text{d}}; \\ \psi_{i,0} = V_{\text{bg}}, \qquad \psi_{i,N_{\text{Ybg}}+N_{\text{Ytg}}} &= V_{\text{tg}} - V_{\text{D}}, \qquad i = 0 \ldots N_{\text{X}}. \end{aligned} \tag{6.14}$$

Therefore, we obtain the potential distribution within the graphene channel and gate oxides for various combinations of V_{tg}-V_{D}, V_{bg} and V_{d}, i.e. different stress conditions. The simulation results for PBTI, NBTI and NBTI-PHCD shown in Figure 6.6 look quite reasonable. However, the distributions of carrier concentrations along the channel would allow for a more intuitive qualitative explanation of our experimental results.

We proceed with the discretization of the continuity equations 6.4 and 6.5. According to Scharfetter-Gummel scheme, the current densities at the intermediate points are discretized as

$$\begin{aligned} J_{n(i+1/2)} &= J_n(x_{i+1/2}) = \frac{qD_n}{\Delta x}\Big(B\Big(\frac{\mu_n(\psi_{i+1}-\psi_i)}{D_n}\Big)n_{i+1} - B\Big(-\frac{\mu_n(\psi_{i+1}-\psi_i)}{D_n}\Big)n_i\Big); \\ J_{p(i+1/2)} &= J_p(x_{i+1/2}) = -\frac{qD_p}{\Delta x}\Big(B\Big(-\frac{\mu_p(\psi_{i+1}-\psi_i)}{D_p}\Big)p_{i+1} - B\Big(\frac{\mu_p(\psi_{i+1}-\psi_i)}{D_p}\Big)p_i\Big), \\ & \qquad\qquad i = 1 \ldots N_{\text{X}}-1, \end{aligned} \tag{6.15}$$

where $B(t) = t/(e^t - 1)$ is the Bernoulli function and $x_{i+1/2} = (x_i + x_{i+1})/2$. The index

$j = N_{\mathrm{Ybg}}$ (i.e. graphene channel) is skipped for simplicity. Therefore, the continuity equations read

$$\begin{aligned} J_{n(i+1/2)} + J_{n(i-1/2)} &= \frac{n_i p_i - n_{\mathrm{eq}} p_{\mathrm{eq}}}{n_i + p_i + 2\sqrt{n_{\mathrm{eq}} p_{\mathrm{eq}}}} \Delta x; \\ J_{p(i+1/2)} + J_{p(i-1/2)} &= -\frac{n_i p_i - n_{\mathrm{eq}} p_{\mathrm{eq}}}{n_i + p_i + 2\sqrt{n_{\mathrm{eq}} p_{\mathrm{eq}}}} \Delta x, \\ & \qquad\qquad i = 1 \dots N_{\mathrm{X}} - 1. \end{aligned} \tag{6.16}$$

Obviously, solution of these equations requires boundary conditions for both carrier concentrations. However, a significant complication compared to the case of Si technologies is that the conductivity type of the graphene channel is determined by the applied stress rather than by the type of artificially introduced dopants. Moreover, for some combinations of gate and drain biases the conductivity type can vary along the channel, i.e. the channel can be ambipolar [125]. In order to account for this behaviour, we suggest two possible types of boundary conditions. Type I is used if the graphene channel is of electron conductivity type and reads

$$\begin{aligned} n_i &= n_{\mathrm{eq}} - \frac{C_{\mathrm{tg}}(\psi_{i,N_{\mathrm{Ybg}}} - \psi_{i,N_{\mathrm{Ybg}}+N_{\mathrm{Ytg}}})}{q}; \\ p_i &= \frac{n_{\mathrm{eq}}^2}{n_i}, \qquad i = 0 \quad \text{or} \quad i = N_{\mathrm{X}}. \end{aligned} \tag{6.17}$$

Type II is for the hole conductivity type of the channel and can be written as

$$\begin{aligned} p_i &= p_{\mathrm{eq}} + \frac{C_{\mathrm{tg}}(\psi_{i,N_{\mathrm{Ybg}}} - \psi_{i,N_{\mathrm{Ybg}}+N_{\mathrm{Ytg}}})}{q}; \\ n_i &= \frac{n_{\mathrm{eq}}^2}{p_i}, \qquad i = 0 \quad \text{or} \quad i = N_{\mathrm{X}}. \end{aligned} \tag{6.18}$$

Therefore, the concentration of majority carriers close to the source and drain is determined by the potential difference between graphene and the gate electrode, while its counterpart for minority carriers is calculated using the carrier balance law.

However, equations 6.17 and 6.18 correspond to the case when the bias component is applied on the top gate of double gated GFETs. Obviously, for back gate BTI one would get

$$\begin{aligned} n_i &= n_{\mathrm{eq}} - \frac{C_{\mathrm{bg}}(\psi_{i,N_{\mathrm{Ybg}}} - \psi_{i,0})}{q}; \\ p_i &= \frac{n_{\mathrm{eq}}^2}{n_i}, \qquad i = 0 \quad \text{or} \quad i = N_{\mathrm{X}} \end{aligned} \tag{6.19}$$

for Type I, and

$$\begin{aligned} p_i &= p_{\mathrm{eq}} + \frac{C_{\mathrm{bg}}(\psi_{i,N_{\mathrm{Ybg}}} - \psi_{i,0})}{q}; \\ n_i &= \frac{n_{\mathrm{eq}}^2}{p_i}, \qquad i = 0 \quad \text{or} \quad i = N_{\mathrm{X}}. \end{aligned} \tag{6.20}$$

for Type II. Since in our case the oxide thicknesses are large enough, the impact of the quantum capacitance can be neglected and therefore C_{tg} and C_{bg} express geometric capacitances of the top gate and back gate oxides, respectively. Also, all the potential quantities which contribute to equations 6.17 – 6.20 are known and given by V_{tg}-V_{D}, V_{bg}-V_{D} and V_{d}.

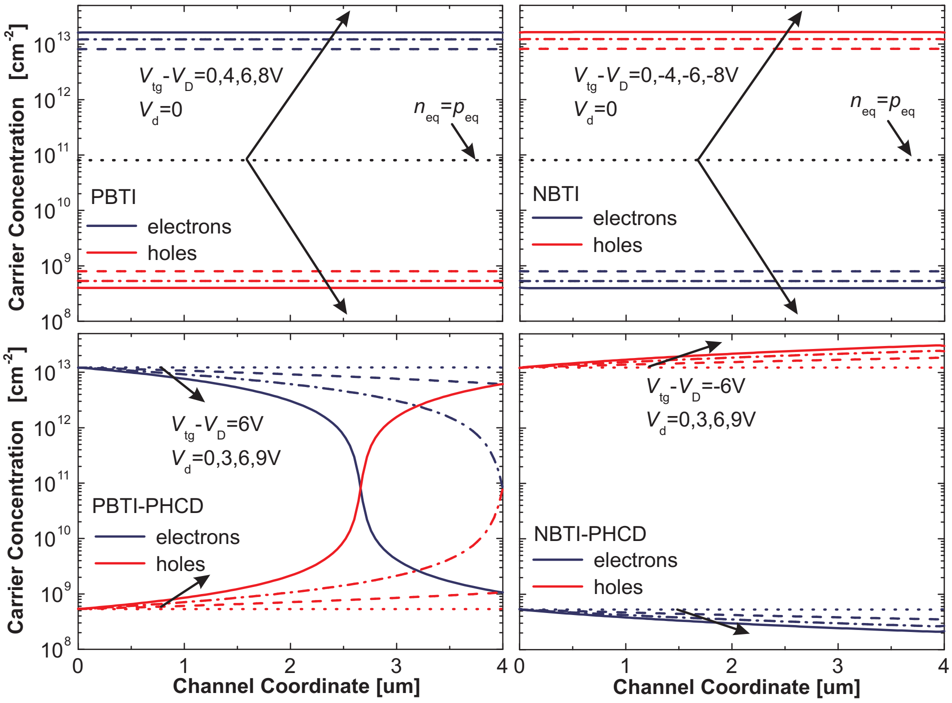

Figure 6.7: Examples of the carrier concentration distributions along the channel simulated using our implementation of the DD equations for PBTI, NBTI, PBTI-PHCD and NBTI-PHCD in GFETs. While in the case of PBTI and NBTI the carrier concentration along the channel is nearly constant, for NBTI-PHCD the concentration of holes increases and the concentration of electrons decreases toward the drain. At the same time, PBTI-PHCD may lead to ambipolar channel behaviour if the drain bias is large enough.

As follows from the description above, in the case of the GFETs, selection of appropriate boundary conditions depends on the polarity of applied BTI and HCD stress components. Therefore, since PBTI corresponds to the electron conduction region of GFET, one has to use Type I boundary conditions at both electrodes. Conversely, for NBTI, Type II boundary conditions have to be used. Activation of PHCD would lead to an additional increase of the hole concentration close to the drain, while the NHCD component would increase the electron concentration in the proximity of the drain. Thus in the case of PBTI-NHCD and NBTI-PHCD, the HCD component should not change the channel conductivity type. As such, one has to use the boundary conditions of Type I and Type II, respectively.

However, setting of the boundary conditions for PBTI-PHCD and NBTI-NHCD is more complicated, since these two stress configurations may lead to ambipolar channel behaviour. For example, in the case of PBTI-PHCD, one should always use Type I at the source, where the electron conductivity type is associated with the PBTI component. At the same time, the PHCD component comes into play close to the drain. If V_d is not large enough, this simply reduces the electron concentration near the drain, while the overall electron conductivity type is conserved. Therefore, the boundary condition of Type I has to be used at the drain as well. But a strong PHCD component can reverse the conductivity type of graphene near the drain and make hole transport dominating. In this case the Type II boundary condition has to be employed at the drain. Similarly, for NBTI-NCD, the boundary condition of Type II at the source and either Type II or Type I at the drain have to be used. The former corresponds to the case of small V_d, while the latter is for large V_d, leading to ambipolar behaviour. For both PBTI-PHCD and NBTI-HNCD the transition between the different types of boundary conditions at the drain can

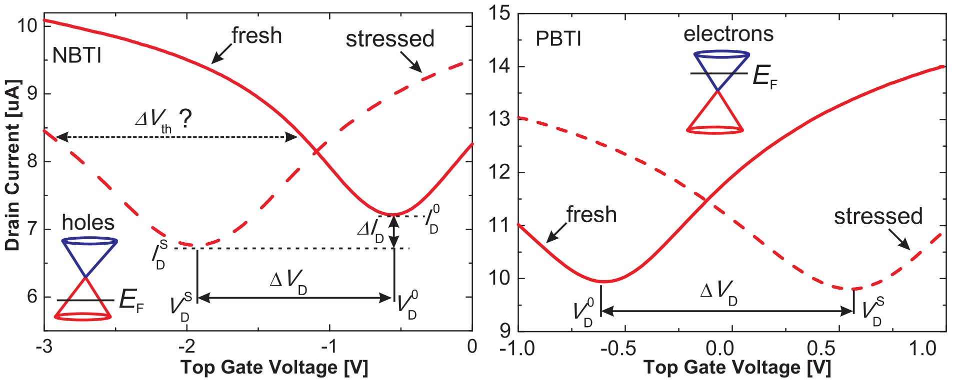

Figure 6.8: The typical impact of NBTI (left) and PBTI (right) stress on the top gate results in a vertical shift of the Dirac point ΔV_D in opposite directions. Also, a horizontal shift of the Dirac point ΔI_D is present in both cases. Thus, the frequently used definition of V_th at which $I_\mathrm{d} = (I_\mathrm{dmax} + I_\mathrm{dmin})/2$ [113, 116, 117] will see a mixture of electrostatics, mobility degradation, and contact resistance. For a correct estimate of the trapped charge density we suggest the use of the shift of the Dirac point voltage ΔV_D.

be easily captured empirically, since setting of a wrong type (e.g. Type I for PBTI-PHCD with large V_d) always leads to unfeasible results.

Exemplary carrier concentration profiles along the channel simulated for different stress configurations are shown in Figure 6.7. Clearly, the concentration of both electrons and holes are nearly constant for PBTI and NBTI, while the channel conductivity types are different. An increase of V_tg-V_D makes the concentration of majority carriers larger, while reducing the amount of minority carriers. At the same time, activation of the PHCD component acting in conjuction with NBTI increases the concentration of holes and decreases the concentration of electrons toward the drain, making hole conductivity more pronounced. Obviously, this trend is stronger for larger V_d. If a PHCD component acts in conjuction with PBTI, the concentration of electrons, which are the majority carriers close to the source, also decreases toward the drain. Therefore, at a certain V_d the concentration of holes at the drain side becomes larger than the concentration of electrons, i.e. the channel becomes ambipolar.

Although implementation of graphene into the simulators allowing for the quantitative capture of the carrier trapping dynamics remains complicated, the obtained concentration profiles are suitable for a qualitative interpretation of the experimental results. This is because the information on the carrier concentrations in a certain channel segment allows us to make a conclusion on whether electron or hole trapping is more favourable. Moreover, the dependence of the carrier distributions on the magnitude and polarity of the applied stress can be qualitatively reproduced.

6.5 Bias-Temperature Instabilities on the High-k Top Gate

The major part of our experimental studies on BTI in GFETs have been performed by applying either positive (PBTI) or negative (NBTI) bias stress on the high-k top gate of double gated GFET. The obtained results and their interpretation using the general models previously developed for Si MOSFETs are discussed in this section.

6.5.1 Typical Impact on the Device Performance and Reproducibility

Based on our knowledge of GFET operation and the DD simulation results above, we can conclude that NBTI is associated with positively charged traps, which appear as a result of hole trapping. Conversely, in the case of PBTI we are dealing with negatively charged traps, i.e. electron trapping. Hence, the charged trap density shift ΔN_T is positive for NBTI and negative for PBTI. Obviously, any variation of N_T would lead to a shift of the Dirac point voltage, which can be expressed as $\Delta V_\mathrm{D} = \mathrm{q}\Delta N_\mathrm{T}/C_\mathrm{tg}$. Therefore, the simplest way to capture the impact of BTI on the performance of GFET consists in comparison of the gate transfer characteristics measured before and after the stress. The results given in Figure 6.8 show that BTI stress results mainly in a horizontal shift of the Dirac point voltage V_D. However, some vertical drift of the characteristics ΔI_D is also present. The latter is most likely related to a change in the device electrostatics and mobility, which are affected by variation of N_T.

Since I_d depends on other factors (e.g. the contact resistance) and I_dmax is determined by the width of the V_tg interval, the presence of ΔI_D makes the frequently used (but somewhat arbitrary) definition [113, 116, 117] of the threshold voltage V_th as the gate bias at which $I_\mathrm{d} = (I_\mathrm{dmax}+I_\mathrm{dmin})/2$ questionable. Thus, we suggest using the Dirac point shift $\Delta V_\mathrm{D} = |\, V_\mathrm{D}^0 - V_\mathrm{D}^\mathrm{S} \,|$[1] as the main quantity for expressing GFET reliability, since it is directly linked to the variation of charged traps ΔN_T and also independent of other factors. As for the vertical shift of the Dirac point ΔI_D, use of this quantity for expressing BTI degradation/recovery dynamics is also unfeasible. That is because evaluation of the link between ΔI_D and ΔN_T is complicated, since the vertical shift is most likely contributed by both carrier trapping and mobility variation. Also, ΔI_D is impacted by contact resistance, especially if ΔV_D is large.

Experimental results illustrating the time evolution of transfer characteristics during and after NBTI stress at $T = 25\,^\circ\mathrm{C}$ and $T = 75\,^\circ\mathrm{C}$ are shown in Figure 6.9. As expected, a longer NBTI stress causes a stronger shift of ΔV_D towards more negative voltages. Also, significant drifts are recorded even at very low stress biases, corresponding to about 1 MV/cm (compare to the typically used 4 – 8 MV/cm stress in Si technologies). During the recovery, ΔV_D returns back to its initial position which happens faster at a higher temperature. We thus can extract V_D for each of the measured characteristics and obtain the recovery traces versus the relaxation time. Analysis is provided below.

The transfer characteristics shown in Figure 6.9 were measured by sweeping V_tg from positive to negative values (V^- sweep mode). However, it has been observed that when the measurements are performed from negative to positive V_tg (V^+ sweep mode), the initial NBTI degradation is more severe, which is due to charging of fast traps during the stress. The fast trap component associated with these defects is also responsible for the pronounced hysteresis and becomes stronger for larger ΔV_D, while recovering within about 100 s (Figure 6.10). However, contrary to NBTI, the magnitude and recovery of PBTI degradation are independent of the sweep direction.

Figure 6.11(left) illustrates that high-temperature baking at 300 °C for 2 hours leads to a nearly complete recovery of NBTI degradation. This allows us to minimize the impact of device-to-device variations by performing numerous measurements on the same device. In Figure 6.11 (right) one can see the two sets of recovery traces measured for the same device at $T = 25\,^\circ\mathrm{C}$, with an intermediate baking step at $T = 300\,^\circ\mathrm{C}$ for 2 hours. The results are well reproducible, despite the presence of both fast and slower trap components. Therefore, the reliability characteristics measured on the same device using different stress conditions should be easier to interpret.

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[1] In the some cases, e.g. comparison of NBTI and PBTI on one plot, we will take into account the sign of ΔV_D. Then it is "+" for NBTI (hole trapping) and "-" for PBTI (electron trapping).

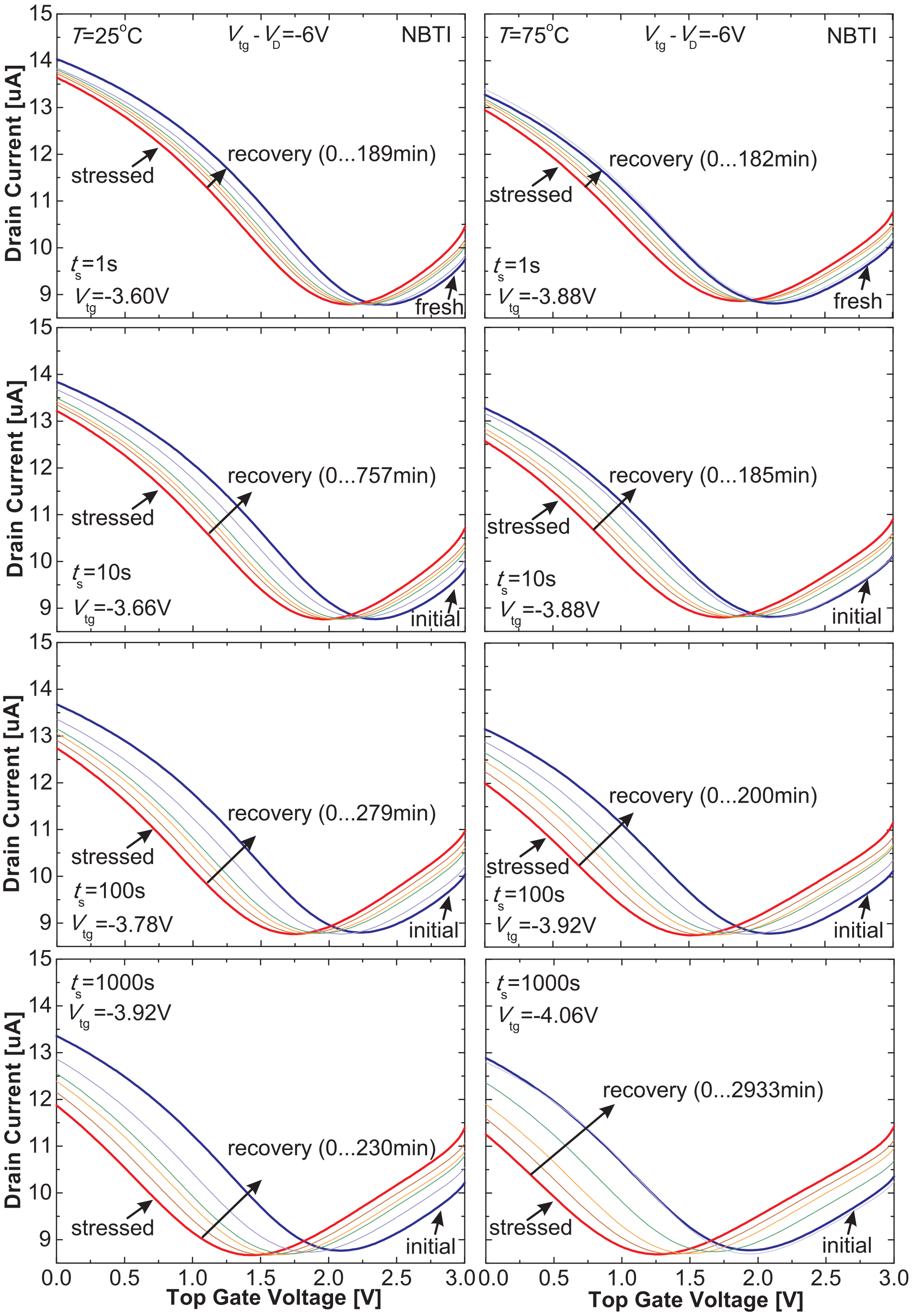

Figure 6.9: Time evolution of the top gate transfer characteristics after NBTI stress ($t_s = 1$ s, 10 s, 100 s, and 1000 s) with V_{tg} - $V_D(t_s) \approx$ const for $T = 25$ °C (left) and $T = 75$ °C (right). The degradation magnitude and the recovery rate strongly correlate with the stress time and the temperature of the sample. For example, at a higher temperature the degradation is stronger and the recovery proceeds faster. Note that narrow V_{tg} intervals were used during I_d-V_{tg} measurements in order to minimize additional BTI stressing/relaxation.

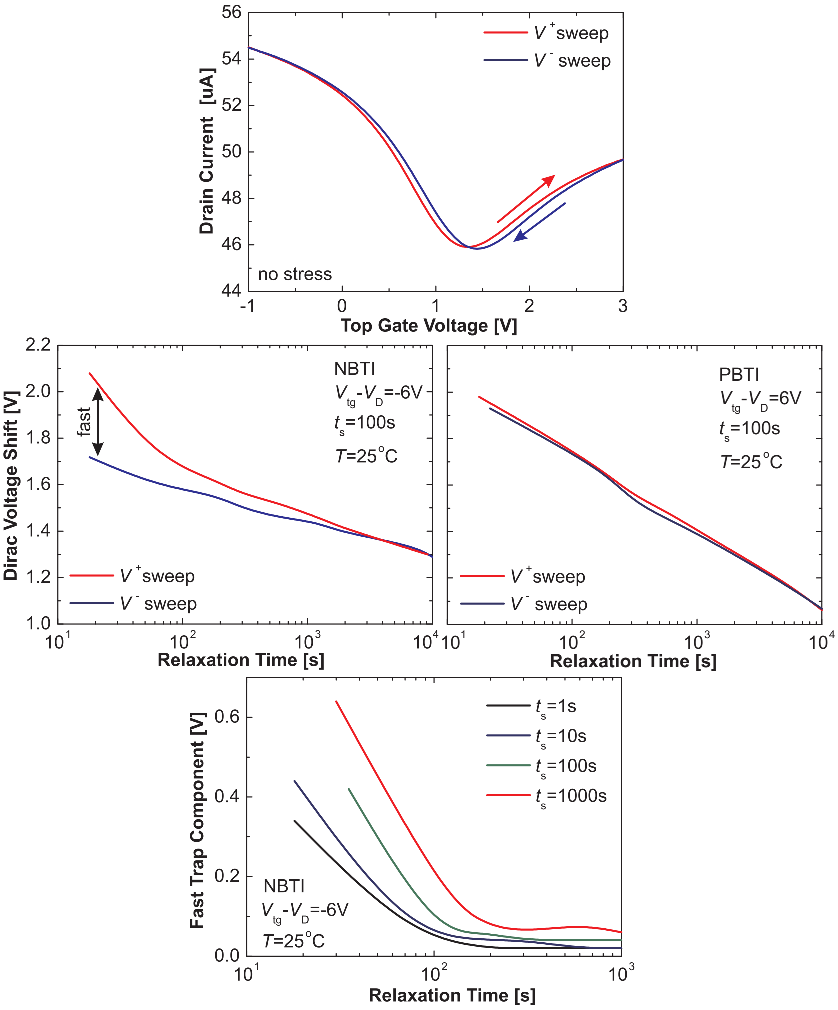

Figure 6.10: The presence of the fast trap component leads to a hysteresis-like impact on the transfer characteristics (top). Recovery traces measured after NBTI-like stress in V^+ sweep mode also contain a fast trap component, while their counterparts corresponding to PBTI do not depend on the sweep direction (center). The NBTI-like fast trap component strongly depends on the degradation magnitude and recovers within approximately the first 100 seconds after the stress (bottom).

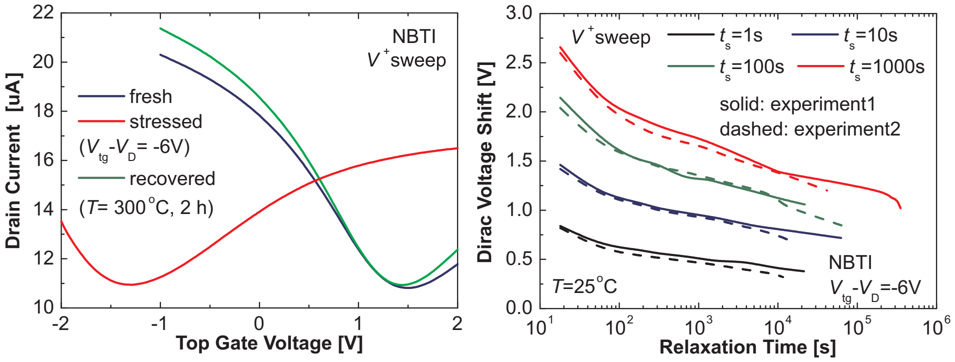

Figure 6.11: Left: Baking of the device at $T = 300\,^\circ\mathrm{C}$ for 2 hours leads to a near complete recovery of NBTI degradation. Right: The recovery traces obtained for the same device after baking are well reproducible, including the fast trap impact observed when using V^+ sweep mode. This allows us to reuse the same device several times for different stress conditions.

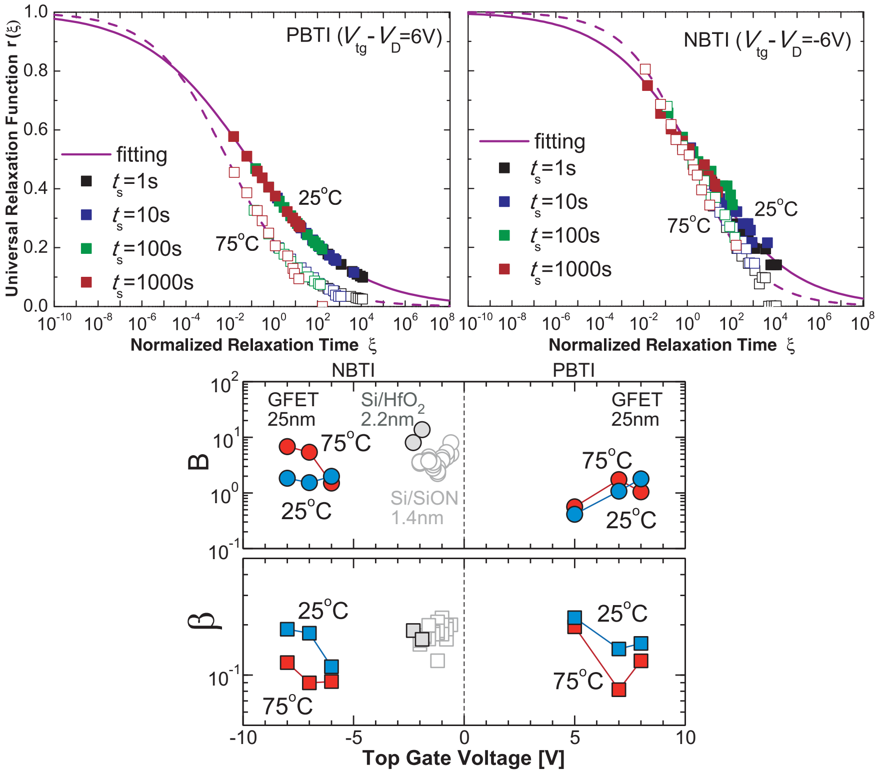

Figure 6.12: In Si technologies, it has been observed that the normalized BTI recovery follows a universal relaxation relation [61, 64] $r(\xi) = 1/(1 + B\xi^{\beta})$ with the normalized relaxation time $\xi = t_{\mathrm{r}}/t_{\mathrm{s}}$, and B and β being empirical fitting parameters. We demonstrate that this is also the case for PBTI and NBTI recovery in GFETs. Quite remarkably, the parameters used for fitting of GFET traces (bottom) are very similar to those required to fit silicon data. This indicates a similarity in the underlying physical degradation processes.

6.5.2 Temperature Dependence and Fitting with CET Map and Universal Models

The fast trap component observed when monitoring the NBTI recovery using the V^+ sweep mode makes the interpretation of the resulting ΔV_{D} recovery traces more complicated. Moreover, the slow long-term degradation/recovery dynamics are more suitable for comparison with Si technologies than the hysteresis behaviour. Therefore, the results measured using the V^- sweep mode (e.g. Figure 6.9) will be analyzed in detail below.

First we attempt to fit the ΔV_{D} recovery traces measured without the fast trap component using the universal relaxation relation previously developed for Si technologies [61, 64]. As has been discussed in Section 3.2, this universal relation reads $r(\xi) = 1/(1 + B\xi^{\beta})$ with the normalized relaxation time $\xi = t_{\mathrm{r}}/t_{\mathrm{s}}$ and empirical fitting parameters B and β. In Figure 6.12 we show that perfect fits can be obtained for both PBTI and NBTI at $T = 25\,°\mathrm{C}$ and $T = 75\,°\mathrm{C}$. Moreover, the parameters B and β employed for fitting are very similar to those obtained from Si data, confirming the similarity in the underlying physical degradation processes. However, contrary to Si technologies, no permanent ('dangling bond') component needs to be taken into account during the extraction.

For a final comparison with Si technologies, we show that the obtained recovery traces can be fitted with the capture/emission time (CET) map model [69] for both PBTI and NBTI. The CET map model assumes that BTI is the collective response of independent defects which exchange charges with the channel, each following a first-order non-radiative multiphonon process. Con-

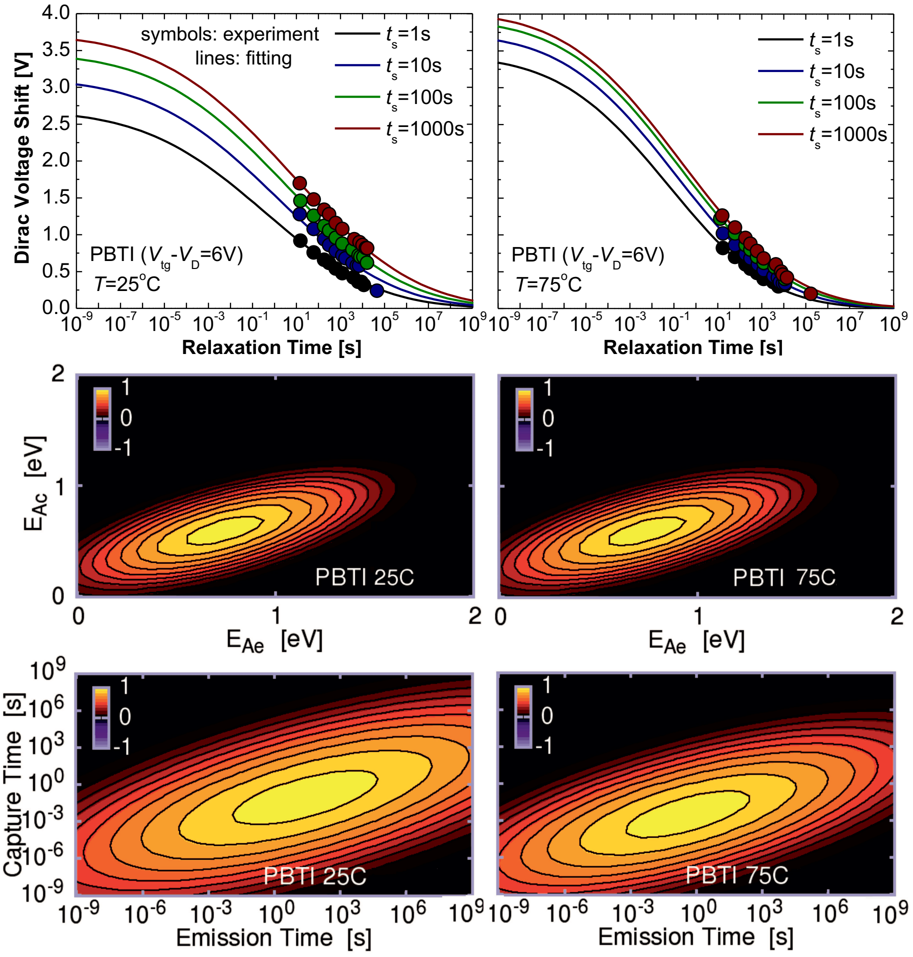

Figure 6.13: The ΔV_{D} recovery traces for PBTI at $T = 25\,°\mathrm{C}$ and $T = 75\,°\mathrm{C}$ fitted with the CET map model. The dependence of the degradation on temperature is clearly visible, i.e. stronger initial degradation and faster recovery for higher T. The simulations using the CET map model [69] are in good agreement with our experimental data. The underlying Gaussian distributions for activation energies and time constants closely resemble those for Si technologies [69]. This also testifies to the usefulness of the model for GFETs.

firmed by extensive Si datasets, the essential ingredients of the model are the widely distributed, correlated, and temperature dependent capture and emission times. These quantities can be well described using bivariate Gaussian distributions of the respective activation energies. The sets of experimental ΔV_{D} recovery traces fitted with the simulation results, and corresponding CET map distributions are given in Figure 6.13 and Figure 6.14 for PBTI and NBTI, respectively. In both cases the same absolute value of V_{tg} - V_{D} and two different temperatures ($T = 25\,°\mathrm{C}$ and $T = 75\,°\mathrm{C}$) were used. The typical initial values of the charged trap density shift ΔN_{T} for GFETs are around $10^{12}\,\mathrm{cm}^{-2}$ which is still considerably larger than for Si technologies.

In our first studies the measurements were performed without an intermediate high-temperature baking/recovery step. Therefore we had to investigate the BTI dynamics for various stress conditions on different devices. In that case simultaneous fits of data for different stress conditions were often difficult to obtain because of the detrimental effects of variability (cf. Figure 6.3) which are not considered in the CET map model. However, the experimental results measured on the same devices (Figures 6.13 – 6.14) are fully consistent with the theory. Similarly to Si technologies, for both PBTI and NBTI the degradation is stronger and recovery is faster at

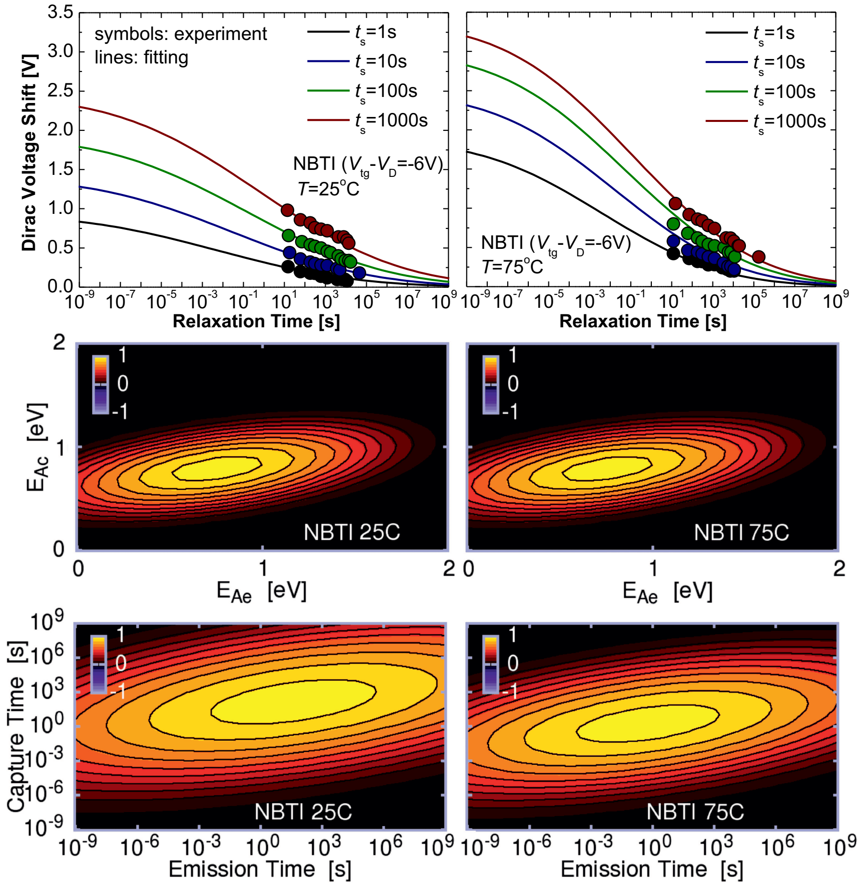

Figure 6.14: The ΔV_D recovery traces for NBTI at $T = 25\,°\mathrm{C}$ and $T = 75\,°\mathrm{C}$ fitted with the CET map model. Similarly to the case of PBTI, stronger degradation and faster recovery are observed at higher T. Also, the extracted CET distributions are similar to their counterparts for Si technologies [69]. This finally underlines the similarities in BTI degradation/recovery dynamics in GFETs and Si MOSFETs.

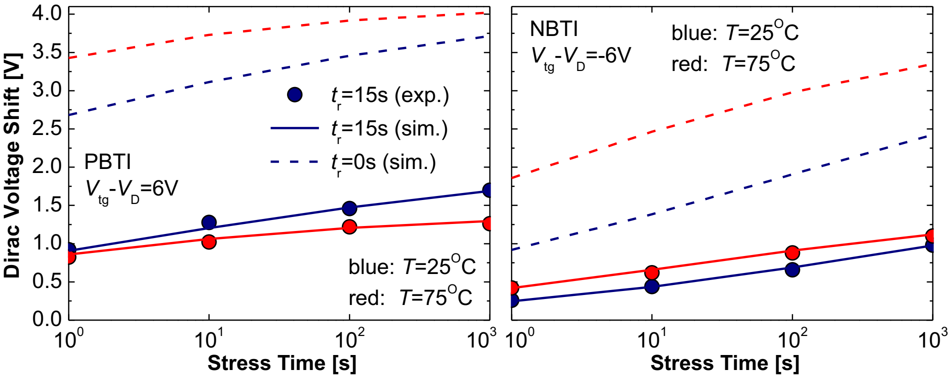

Figure 6.15: Back-extrapolation to zero measurement delay using the CET map model for PBTI (left) and NBTI (right). In both cases the values of $\Delta V_\mathrm{D}(t_\mathrm{r} \approx 0)$ obtained for $T = 75\,°\mathrm{C}$ are significantly larger than those measured for $T = 25\,°\mathrm{C}$. This suggests that the lower degradation at higher T previously observed for PBTI with $t_\mathrm{r} = 15\,\mathrm{s}$ measurement delay is an artefact.

higher T. Also, the dependence of the degradation magnitude on stress time is well reproduced. Finally, the obtained CET distributions for activation energies and time constants are very similar to the ones extracted for Si MOSFETs [69]. This means that the degradation/recovery dynamics of BTI in GFETs and Si technologies are very similar.

In some cases, as a consequence of the relatively large measurement delay caused by the full I_d-V_tg sweeps, the degradation appears to be lower at higher T, in agreement with previous results [113, 117]. However, in Figure 6.15 we show that the measurement delay can be extrapolated to $t_\mathrm{r} \approx 0$ using the CET map model. The values of $\Delta V_\mathrm{D}(t_\mathrm{r} \approx 0)$ obtained for $T = 75\,^\circ\mathrm{C}$ are always larger than their counterparts for $T = 25\,^\circ\mathrm{C}$. This confirms that a lower degradation at higher temperature is an artefact, which appears due to a significant measurement delay and faster recovery at $T = 75\,^\circ\mathrm{C}$. This artefact is typically more pronounced for PBTI than for NBTI because the recovery of PBTI is faster, especially at higher temperatures.

In Si technologies, two Gaussian distributions have to be used to describe the NBTI recovery data [161, 57]. The first dominates the experimentally observed recovery and has mean activation energies for capture and emission slightly below 1 eV, just like our GFETs. The second distribution has mean activation energies at about 1.5 eV/2 eV for capture and emission, respectively. This second distribution has been tentatively assigned to dangling bonds (P_b centers) which are responsible for the permanent component. Interestingly, this distribution is absent in our graphene transistors, which is consistent with the Van der Waals bonding between graphene and $\mathrm{Al_2O_3}$. Nevertheless, we can conclude that the CET map model established for Si MOSFETs can be successfully applied to GFETs as well.

Overall, we can conclude that our BTI assessment methodology based on the models used for Si technologies is suitable for quantifying the quality and reliability of GFETs and graphene/dielectric interfaces in general. This is because the BTI degradation/recovery dynamics in GFETs and Si MOSFETs are similar despite the absence of dangling bonds and larger defect density shifts in the former case.

6.6 Bias-Temperature Instabilities on the $\mathrm{SiO_2}$ Back Gate

Although in the course of this work we have mostly dealt with BTI on the high-k top gate, some BTI measurements on the $\mathrm{SiO_2}$ back gate were also performed. However, investigation of the back gate BTI on our standard devices was not possible, since no visible degradation of the 1800 nm thick back gate oxide could be caused using stress voltages below 100 V. Therefore, similar devices with 92 nm thick $\mathrm{SiO_2}$ layers have been fabricated, allowing us to observe back gate BTI at reasonable stress voltages. The results obtained on these devices are discussed below.

6.6.1 Stress Oxide Field Dependence and Recovery

In Figure 6.16 we show the measured evolution of the back gate transfer characteristics after subsequent NBTI and PBTI stresses with $V_\mathrm{bg} - V_\mathrm{D}$ varied from 0 to ± 60 V in ± 5 V steps. Clearly, the typical impact of BTI is similar to what is observed on the high-k top gate. Therefore, we express the degradation magnitude in terms of a Dirac point voltage shift $\Delta V_\mathrm{D} = q\Delta N_\mathrm{T}/C_\mathrm{bg}$. The resulting dependences of ΔV_D on the stress oxide field $F_\mathrm{ox} = (V_\mathrm{bg} - V_\mathrm{D})/d_\mathrm{bg}$ are plotted in Figure 6.17 for the stress times $t_\mathrm{s} = 10\,\mathrm{s}$ and $t_\mathrm{s} = 100\,\mathrm{s}$. Contrary to Si technologies, in both cases PBTI degradation is stronger than its NBTI counterpart. Moreover, there is a significant difference between PBTI and NBTI with respect to the dependence of the observed

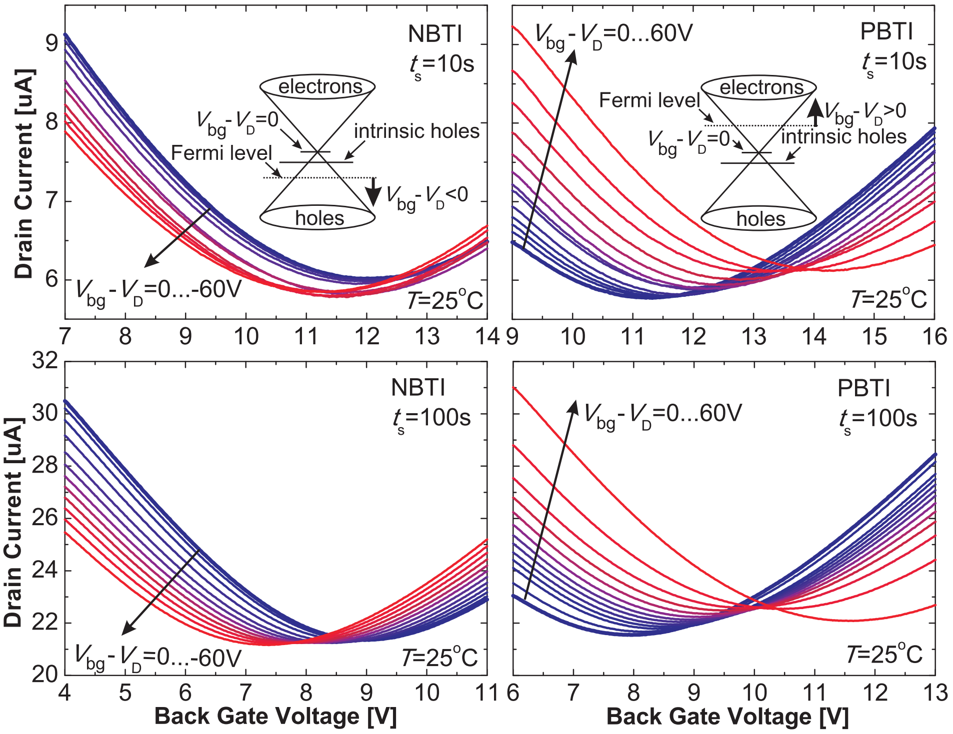

Figure 6.16: Evolution of the back gate transfer characteristics after subsequent stresses with increasing V_{bg} - V_{D} and two different stress times for NBTI (left) and PBTI (right).

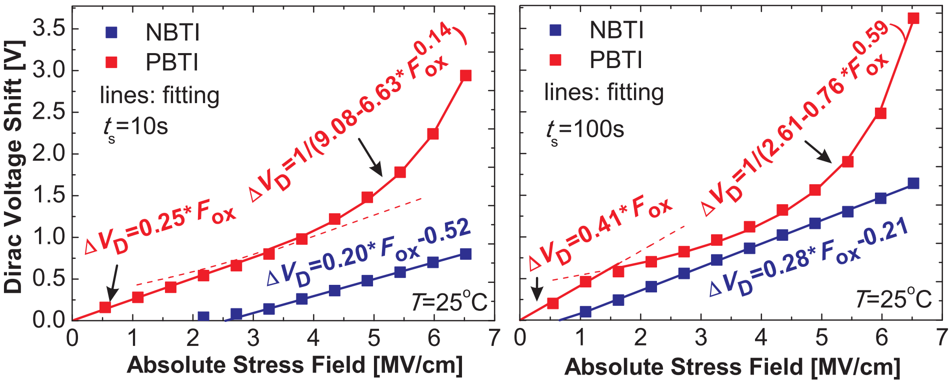

Figure 6.17: Comparison of the PBTI and NBTI V_{D} shifts versus stress oxide field at $t_{\mathrm{s}} = 10\,\mathrm{s}$ (left) and $t_{\mathrm{s}} = 100\,\mathrm{s}$ (right).

Dirac voltage shifts on the stress oxide field. While the NBTI shift linearly increases versus F_{ox}, growth of the PBTI shift is linear only at small F_{ox} and can be fitted with a Langmuir power law $f(x) = 1/(a - bx^c)$ at larger oxide fields. At the same time, for both NBTI and PBTI the slopes in the linear regions increase versus t_{s}. This is because the probability of carrier trapping becomes larger for longer stresses.

Interestingly, transition of PBTI curves to a Langmuir-like behaviour takes place at smaller F_{ox} if t_{s} is larger. This leads to a smaller difference between PBTI and NBTI shifts at moderate t_{s}, although PBTI still remains stronger than NBTI (Figure 6.17(right)). Since in GFETs PBTI is associated with electron trapping and NBTI is due to hole trapping, we assume that the main reason for the observed behaviour is the difference in the kinetics of the two processes as well as the energetic alignment of the defect bands with the Fermi level in the graphene channel.

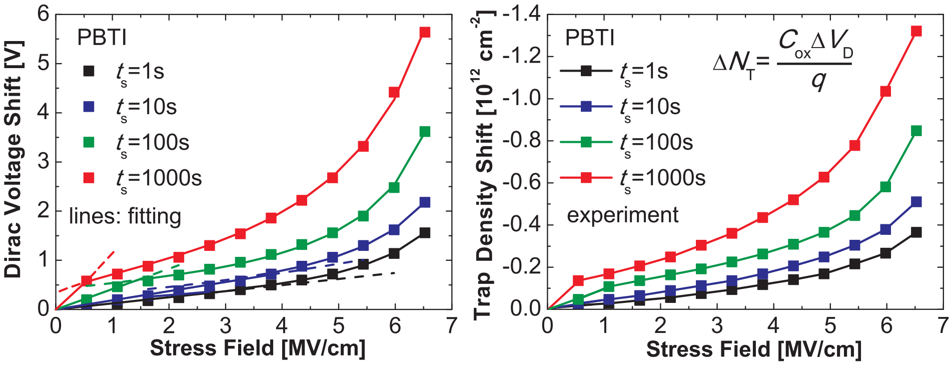

Figure 6.18: Stress field dependence of the ΔV_D (left) and ΔN_T (right) after PBTI stresses with different stress times. $\Delta N_T < 0$ means electron trapping.

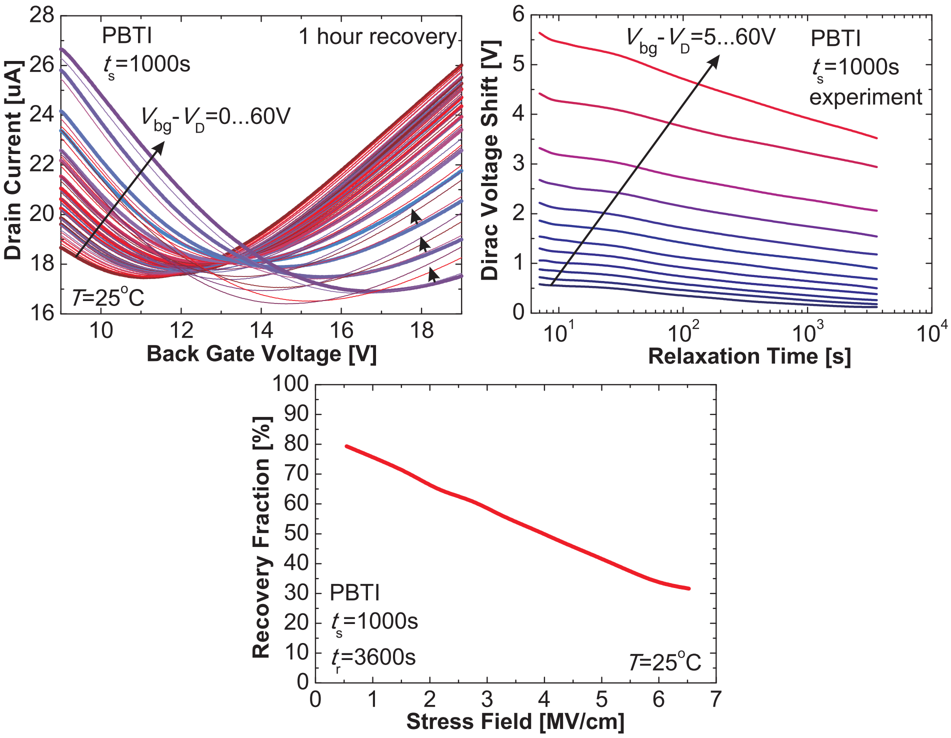

Figure 6.19: Top: Time evolution of the back gate transfer characteristics after subsequent PBTI stress/recovery rounds with increasing V_{bg} - V_D and the corresponding $\Delta V_D(t_r)$ recovery traces. Bottom: The recovery fraction measured one hour after the stress decreases versus the stress oxide field.

Another issue which contributes to the asymmetry between NBTI and PBTI is the positive initial values of V_D, which are typical for all our GFETs. This means that our graphene is p-doped, i.e. some intrinsic holes are present even if $V_{bg} = 0$. Most likely, trapping of these intrinsic holes is less efficient, especially if the stress time is small. Therefore, NBTI degradation is weak at small F_{ox}, when $-V_D < V_{bg} - V_D < 0$, i.e. the applied voltage is not enough to shift the Fermi level below the intrinsic level (Figure 6.16(inset)).

Contrary to NBTI, PBTI is independent of the intrinsic hole level position, since any stress with $V_{bg} - V_D > 0$ introduces extrinsic electrons and shifts the Fermi level into the conduction band. This is why some PBTI degradation is clearly visible even after a stress with $t_s = 1$ s and

$F_{\text{ox}} < 1\,\text{MV/cm}$ (Figure 6.18(left)). However, the dependence of the magnitude of the PBTI shifts on the stress oxide field is strongly correlated with the stress time. For example, if t_{s} is small, the PBTI shift moderately increases in a linear manner up to a quite large F_{ox}. Conversely, in the case of long stresses, a strong linear dependence of ΔV_{D} on F_{ox} is observed only in a very narrow range of small F_{ox}, and is immediately substituted by a Langmuir-like behaviour. Obviously, the same type of oxide field dependence is typical for the charged trap density shift ΔN_{T}, which is proportional to ΔV_{D} (Figure 6.18(right)). However, the values of ΔN_{T} observed for GFETs are 10^{11}–$10^{12}\,\text{cm}^{-2}$, which is significantly larger than for Si technologies (10^{10}–$10^{11}\,\text{cm}^{-2}$) [59].

Next we examine the time evolution of the back gate transfer characteristics after the PBTI stress. In order to do so, we fix a comparably large $t_{\text{s}} = 1000\,\text{s}$ and monitor recovery during the one hour after the end of stress with a certain $V_{\text{bg}}\text{-}V_{\text{D}}$. The time evolution of the transfer characteristics and resulting $\Delta V_{\text{D}}(t_{\text{r}})$ recovery traces are shown in Figure 6.19. Clearly, the back gate BTI degradation in GFETs is recoverable, similarly to its counterpart observed on the high-k top gate and also for Si technologies [76, 151, 158]. Remarkably, after the stress with smaller oxide field, the recovery is faster, while the fraction of recovered degradation is larger (Figure 6.19, bottom). The latter observation is also similar to Si technologies [158]. At the same time, the distances between the recovery traces increase versus $V_{\text{bg}}\text{-}V_{\text{D}}$, following the Langmuir-like dependence which is typical for PBTI with $t_{\text{s}} = 1000\,\text{s}$ (cf. Figure 6.18).

6.6.2 Comparison with Top Gate BTI

In Figure 6.20 we compare the results for PBTI degradation obtained on the SiO_2 back gate and Al_2O_3 top gate of the same GFET. Clearly, the direction of the Dirac point voltage shift is the same, which means that electron trapping takes place independently of whether the PBTI stress is applied on the top or back gate of GFET. At the same time, the Dirac point current is shifted in opposite directions, which is most likely because the negatively charged traps situated in SiO_2 and Al_2O_3 interfacial layers impact the carrier mobility in a different manner.

However, the significant difference in the oxide thicknesses requires us to operate with a normalized Dirac point voltage shift $\Delta V_{\text{Dn}} = \Delta V_{\text{D}}/d_{\text{ox}}$ (cf. [148])[2] when making a quantitative comparison of the degradation magnitudes on the top and back gates. As shown in Figure 6.20, the magnitude of PBTI degradation on the top gate is considerably larger. This is similar to Si technologies, where the reliability of high-k oxides also presents an important issue [149]. At the same time, the dependence on F_{ox} in the case of top gate PBTI is purely Langmuir-like, while an abrupt linear increase is expected only close to $F_{\text{ox}} = 0$ so as to maintain zero degradation at zero oxide field. This is despite $t_{\text{s}} = 10\,\text{s}$, which leads to a significant linear region in the case of back gate PBTI. In other words, the behaviour of the top gate PBTI degradation versus F_{ox} observed using $t_{\text{s}} = 10\,\text{s}$ is similar to those which has been measured on the back gate with significantly larger stress times (Figure 6.17). Also, the resulting charged trap density shift is larger for the top gate PBTI. Therefore, we can conclude that the high-k top gate is considerably less stable with respect to BTI than the SiO_2 back gate.

To conclude, we have shown that there is a considerable asymmetry between back gate NBTI and PBTI in terms of degradation magnitude and its dependence on the stress parameters. At the same time, the recovery of the back gate BTI has been shown to be similar to those previously reported for Si technologies and for the high-k top gate BTI in GFETs. Finally, the back gate BTI degradation dynamics are similar to those observed on the high-k top gate,

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[2] Here d_{ox} is either d_{bg} or d_{tg}.

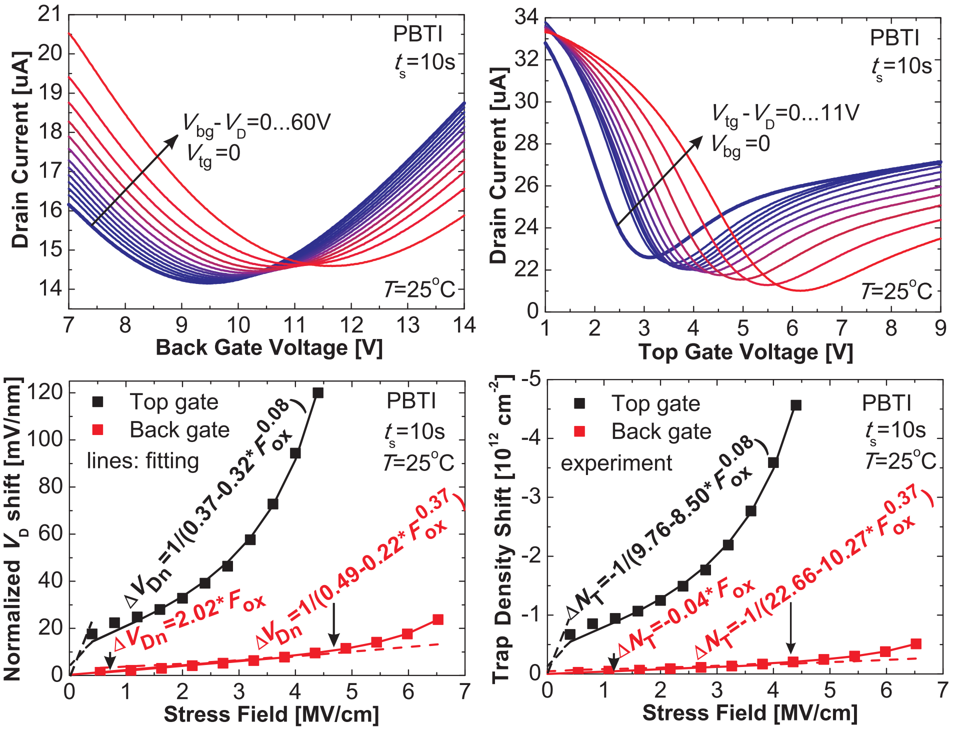


Figure 6.20: Top: Evolution of the back gate and top gate transfer characteristics after subsequent PBTI stresses with increasing F_{ox}. Bottom: Comparison of the resulting ΔV_{Dn} and ΔN_{T}.

although the magnitude in the latter is significantly larger. Therefore, we can conclude that the BTI stability of the SiO_2 back gate is better compared to the high-k top gate.

6.7 Hot-Carrier Degradation

The results discussed in the previous sections allowed us to understand the degradation/recovery dynamics of BTI in GFETs. However, in real device operation conditions, a non-zero drain bias is typically applied. Therefore, an additional degradation due to the impact of hot carriers is expected. In this section we discuss the results of the HCD dynamics obtained on the high-k top gate of similar double-gated GFETs.

6.7.1 First Observations and Typical Impact on the Device Performance

In order to observe HCD in GFETs and obtain an initial understanding of its dynamics, we have performed measurements using a fixed $V_{\mathrm{d}} = 5\,\mathrm{V}$ (i.e. PHCD) and three different $V_{\mathrm{tg}} - V_{\mathrm{D}}$ corresponding to NBTI ($V_{\mathrm{tg}} - V_{\mathrm{D}} < 0$), a zero bias component ($V_{\mathrm{tg}} - V_{\mathrm{D}} = 0$) and PBTI ($V_{\mathrm{tg}} - V_{\mathrm{D}} > 0$). The resulting time evolution of the top gate transfer characteristics after subsequent stress/recovery rounds with increasing t_{s} is depicted in Figure 6.21. Clearly, if the bias stress $V_{\mathrm{tg}} - V_{\mathrm{D}}$ is set to zero (Figure 6.21a), the pure PHCD ($V_{\mathrm{d}} > 0$) stress shifts the Dirac point in an NBTI-like manner. However, if a rather small negative $V_{\mathrm{tg}} - V_{\mathrm{D}}$ is applied in conjuction with PHCD (i.e. NBTI-PHCD), the shift of Dirac voltage towards more negative values is more considerable, while some vertical drift ΔI_{D} is observed (Figure 6.21b). Interestingly, in both cases hot carrier degradation is recoverable. At the same time, a small positive $V_{\mathrm{tg}} - V_{\mathrm{D}}$ (i.e. PBTI-PHCD) accompanied by the PHCD component has only a negligible impact on the

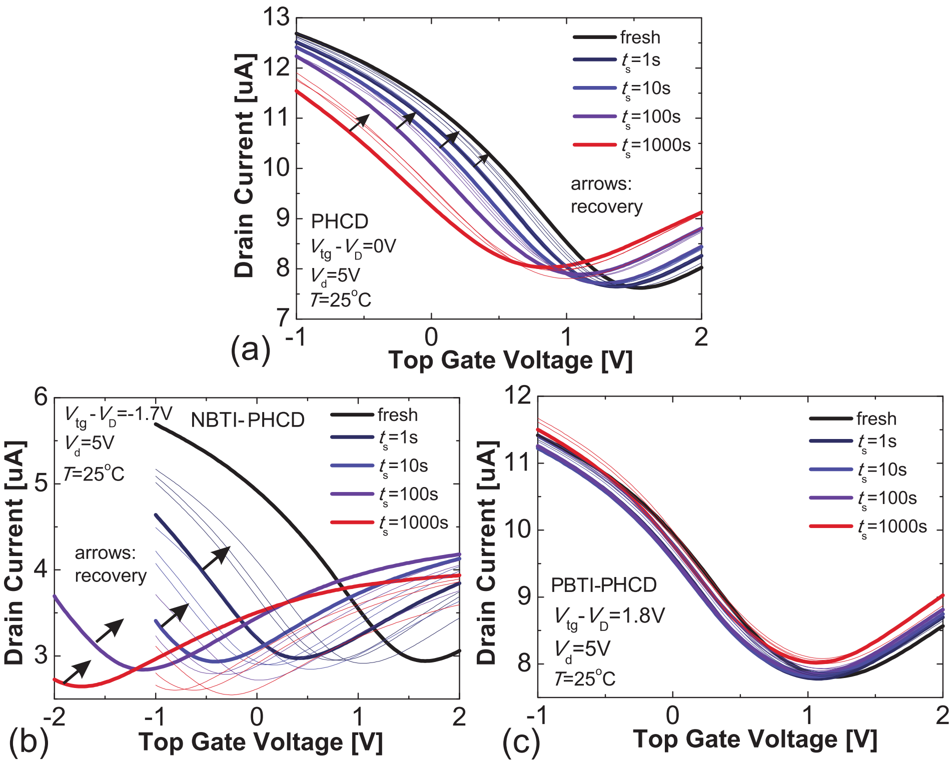


Figure 6.21: Time evolution of the top gate transfer characteristics after pure PHCD (a), NBTI-PHCD (b) and PBTI-PHCD (c). Clearly, the PHCD component having an NBTI-like nature leads to a significant acceleration of NBTI degradation even if the applied negative V_{tg} - V_{D} is rather small. At the same time, the PBTI degradation caused by positive V_{tg} - V_{D} of the same absolute magnitude is almost completely compensated by the PHCD component.

transfer characteristics (Figure 6.21c). Therefore, in our GFETs the impact of NBTI stress becomes more severe if accompanied by a PHCD component. Conversely, PBTI degradation is reduced by an accompanying PHCD component.

Overall, the typical impact of HCD on the performance of GFETs is similar to BTI. Namely, the degradation is associated with both a vertical (ΔI_{D}) and horizontal (ΔV_{D}) shift of the Dirac point and also with a transformation of the shape of the transfer characteristics. However, the vertical shift ΔI_{D} and transformation of the shape are typically stronger than for pure BTI and become more pronounced after stress with a stronger HCD component. Therefore, the use of ΔV_{D} to express degradation/recovery dynamics is especially important in the case of HCD in GFETs.

However, as shown in Figure 6.21, the typical impact of HCD on the device performance also depends on the magnitudes and polarities of the hot carrier and bias stress components contributing to the applied stress. This behaviour can be understood based on our drift-diffusion simulations for the carrier distributions along the channel (Figure 6.7) and band diagrams given in Figure 6.22. If a pure NBTI stress is applied (Figure 6.22(top)), the holes are transferred from graphene and trapped by the oxide traps. As a result the density of positively charged states at the graphene/$\mathrm{Al_2O_3}$ interface N_{T} increases which leads to an NBTI-like shift of the Dirac point. On the contrary, the pure PBTI stress acting in the electron conduction region (Figure 6.22(bottom)) leads to electron trapping. At the same time, the carrier concentration is constant along the channel for both pure BTI issues. As shown by our drift-diffusion simulations, activation of the PHCD component increases the hole concentration closely to the drain,

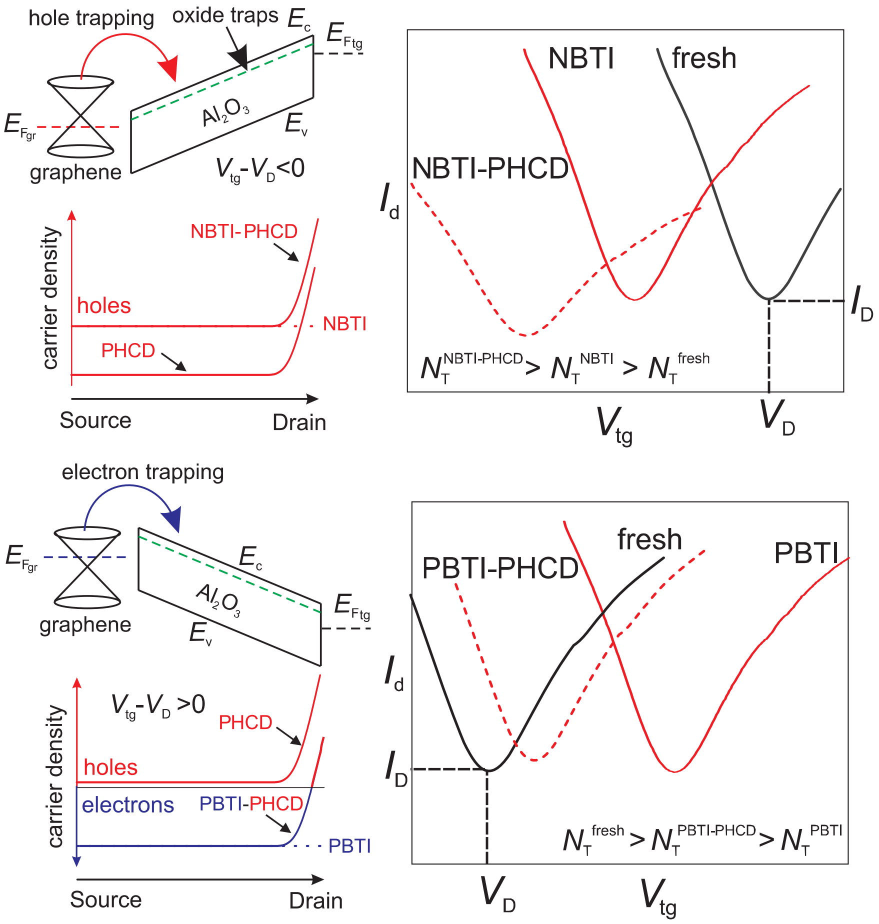
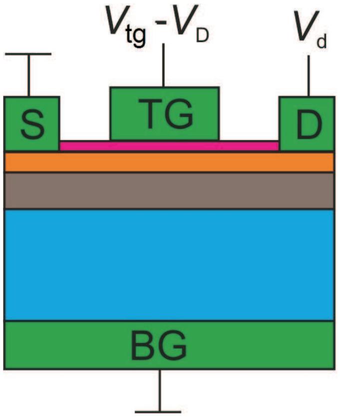


Figure 6.22: Top: Band diagram of the top gate cross-section of a GFET, sketch of the carrier distribution based on our drift-diffusion simulations and a schematic evolution of the transfer characteristic in the case of V_{tg} - $V_D < 0$ (NBTI-like stress). The holes are trapped by the oxide traps. Thus the density of a positive trap charge N_T at the oxide/graphene interface increases and the Dirac voltage determined by -qN_T/C_{tg} is shifted towards more negative values (NBTI). As follows from our drift-diffusion simulations, the PHCD component creates positively charged defects close to the drain, which leads to an additional increase of N_T and acceleration of NBTI (NBTI-PHCD). Bottom: Similar plots for V_{tg} - $V_D > 0$ (PBTI-like stress). The electrons are transferred from graphene to the oxide and become trapped. Thus N_T decreases and the Dirac point is shifted towards more positive values (PBTI). The PHCD component creates positively charged defects which partially compensate for the negative charge introduced by PBTI, making the V_D shift less pronounced (PBTI-PHCD). In both cases the shape of the characteristics is modified because of the change in mobility.

independent of the polarity of the bias stress. Therefore, PHCD introduces additional positively charged defects and accelerates NBTI degradation. Conversely, suppression of PBTI degradation by PHCD originates in the compensation of negatively charged defects introduced by the former by positively charged defects associated with the latter. In this case the negative charges are concentrated at the source side of the channel, while the positive charges are situated close to the drain. In other words, the hot carrier component introduces non-uniformity into the charge distribution along the channel.



Issue	V_{tg}-V_D	V_d
PBTI	>0	0
NBTI	<0	0
PHCD	0	>0
NHCD	0	<0
PBTI-PHCD	>0	>0
PBTI-NHCD	>0	<0
NBTI-PHCD	<0	>0
NBTI-NHCD	<0	<0

Figure 6.23: General classification of reliability issues in GFETs for different polarities of bias and hot carrier stress components.

6.7.2 Degradation under Different Polarities of HC and Bias Components

Although the first observation of HCD in GFETs was done using positive drain bias, it is obvious that $V_d < 0$ would lead to a different reliability issue designated as NHCD. Therefore, in Figure 6.23 we suggest a general classification of reliability issues in GFETs. In addition to pure PBTI and NBTI, there are six degradation mechanisms containing HCD, which are determined by the polarity of the bias and hot carrier components of the applied stress. The detailed analysis of the related degradation/recovery dynamics are provided below.

First we attempt to compare the degradation dynamics of pure PHCD and NHCD with different magnitudes. In Figure 6.24(top) we show the transformation of the top gate transfer characteristics after subsequent pure PHCD and NHCD stresses with increasing V_d and $t_s = 10\,\mathrm{s}$. Clearly, the impact of HC stress on the device performance depends on the polarity of V_d, which introduces some asymmetry between the two issues. PHCD shifts V_D in an NBTI-like manner and also leads to a deformation and vertical drift of the transfer characteristics. However, NHCD is of PBTI-like nature at smaller V_d and NBTI-like at larger V_d while the transition at moderate V_d is associated with a current increase. The resulting ΔN_T versus V_d dependences (Figure 6.24(bottom)) allow us to conclude that PHCD leads to the creation of positively charged defects, while NHCD introduces a negative charge at smaller V_d and a positive charge at larger V_d. At the same time, an increase of t_s makes PHCD more pronounced while in the case of NHCD this leads to a stronger interplay between the defects of different signs. Another interesting observation is that after the stresses with larger V_d the magnitude of ΔN_T tends to decrease. This is most likely because of the disappearance of some positively charged defects, which also occurs in Si technologies [69].

However, since under real operation conditions the hot carrier and bias stress components typically act in conjunction, the analysis of the last four HCD issues mentioned in Figure 6.23 is of an even higher interest. Therefore, at the next stage of our research we analyze PHCD and NHCD overlaid on either PBTI or NBTI with V_{tg} - $V_D = \pm 4\,\mathrm{V}$ and $t_s = 1000\,\mathrm{s}$. While using our experimentral technique with constant t_s and increasing V_d, we also monitor the recovery.

In Figure 6.25 the results for PBTI-PHCD are depicted. The degradation/recovery dynamics

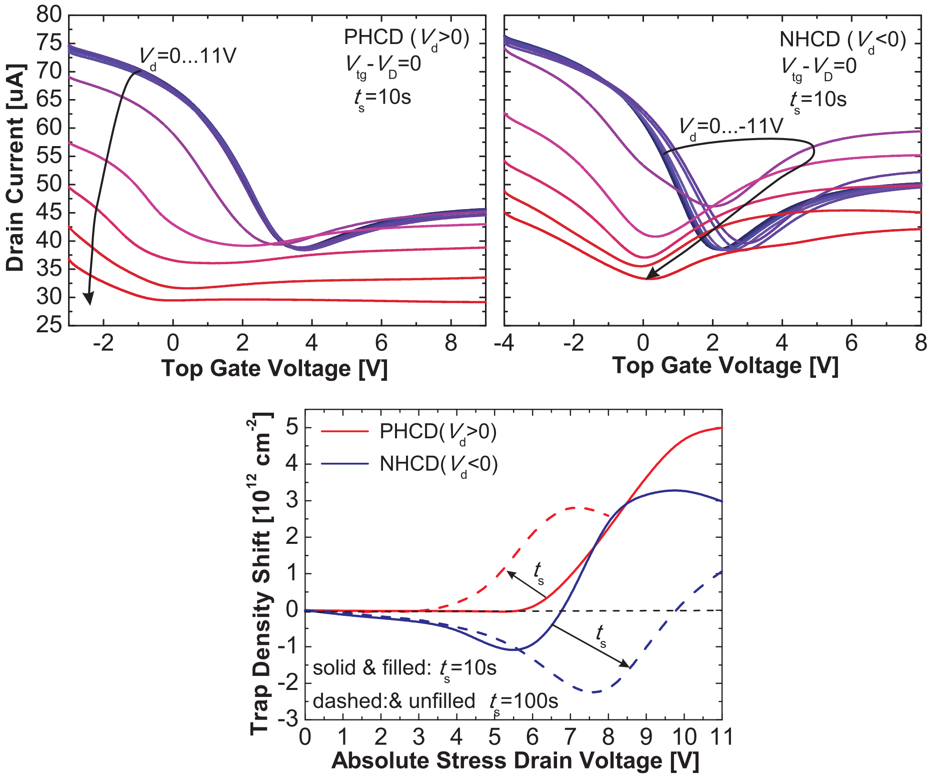


Figure 6.24: Top: Top gate transfer characteristics measured after subsequent stresses with $t_s = 10\,\mathrm{s}$ and increasing V_d for pure PHCD and NHCD. Bottom: Variation of charged trap density shift ΔN_T for PHCD and NHCD; results corresponding to $t_s = 10\,\mathrm{s}$ and $100\,\mathrm{s}$ are plotted. A PHCD stress is able to create only positively charged defects while an NHCD stress creates negatively charged defects at smaller V_d and positively charged ones at larger V_d. Interestingly, positively charged defects may tend to disappear after a stress with larger V_d, similarly to Si technologies [69].

strongly correlate with the magnitude of the applied HC stress. At smaller V_d a PBTI-like shift of the Dirac point is observed which means that the impact of bias stress dominates. However, at larger V_d an NBTI-like PHCD first reduces the Dirac point shift and then introduces an NBTI-like fast trap shift which is similar to pure NBTI in GFETs. The total ΔV_D (Figure 6.25b) can be separated into strongly recoverable and weakly recoverable parts; for convenience each is plotted in the units of charged trap density shift ΔN_T. The strongly recoverable part (Figure 6.25c,d) at smaller V_d is mainly associated with bias stress while at larger V_d PHCD reduces it and also supplements an NBTI-like fast trap. Interestingly, the slow trap behaviour remains PBTI-like and thus originates from the bias stress independently of the HC stress magnitude. The weakly recoverable part (Figure 6.25e) at smaller V_d originates from the bias stress and reflects the presence of a negative charge which is then compensated by PHCD at larger V_d. Moreover, an extra positive charge appears after strong HC stresses which leads to over-recovery of PBTI-like degradation.

The related results for PBTI-NHCD are plotted in Figure 6.26. A PBTI-like nature of the NHCD component at smaller V_d results in a significant acceleration of the PBTI degradation while its NBTI-like nature at larger V_d leads to its suppression. However, contrary to the previous case, a more significant negative charge density prevents a complete suppression of PBTI-like behavior. Thus, the strongly recoverable part remains PBTI-like within the whole V_d range and no NBTI-like fast trap appears (Figure 6.26c,d). The behavior of the weakly recoverable

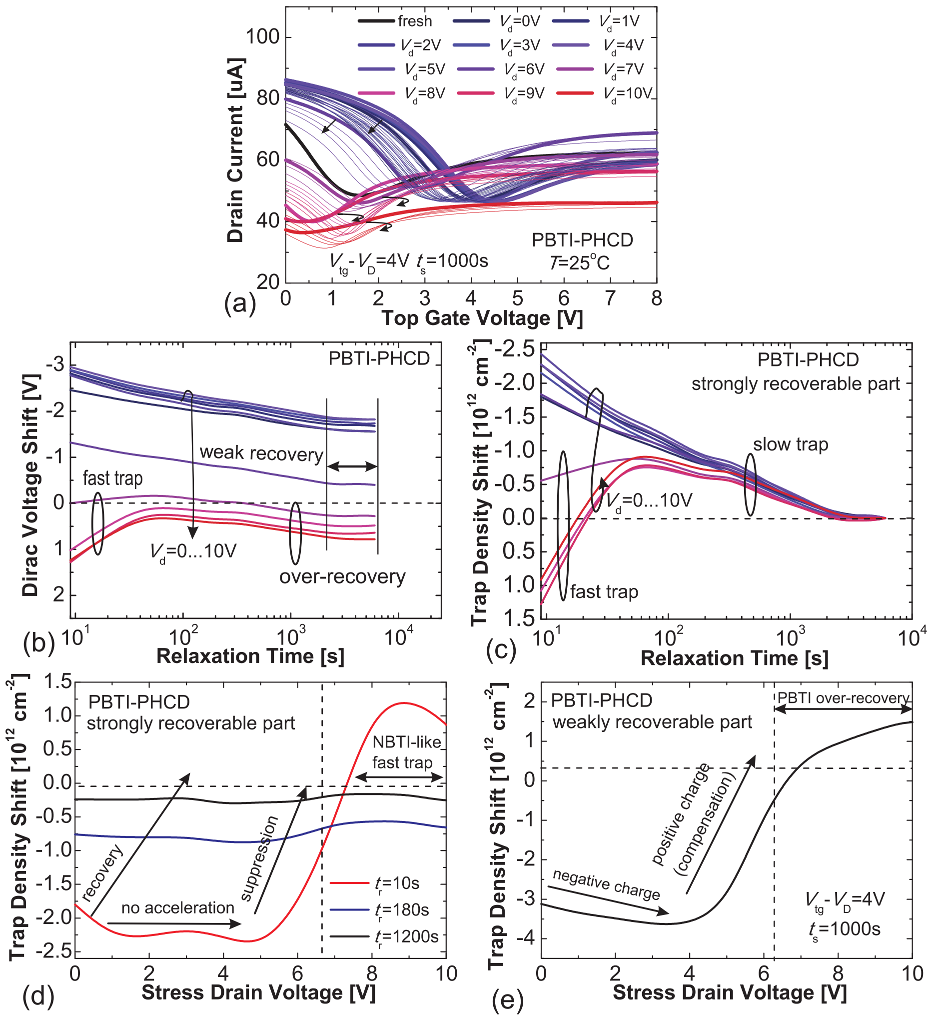


Figure 6.25: (a) Time evolution of the top gate transfer characteristics after subsequent PBTI-PHCD stresses. (b) The corresponding ΔV_D recovery traces contain both strongly recoverable (c,d) and weakly recoverable (e) parts. At low V_d the former has a PBTI-like nature and thus is mainly associated with bias stress, being almost independent of V_d. The presence of a strong V_d leads to a suppression of the strongly recoverable part and introduces NBTI-like fast trap contribution which is also typical for pure NBTI in GFETs. Interestingly, the slow trap behaviour remains PBTI-like (c). The weakly recoverable part (e) is associated with negatively charged defects created by PBTI at smaller V_d and with positive charge introduced by PHCD at larger V_d. The presence of an extra positive charge at larger stress V_d (e) leads to an over-recovery of PBTI-like degradation (b).

part (Figure 6.26e) is similar to PBTI-PHCD, although an increase of negative charge density obviously proceeds faster. Nevertheless, an extra positive charge leading to over-recovery of PBTI-like degradation is present at larger V_d.

In Figure 6.27 one can see the results for NBTI-PHCD. Obviously, in this case both the HC and the bias component are able to create only positively charged defects. Thus the degradation is NBTI-like within the whole V_d range and no over-recovery is observed (Figure 6.27b). However, a strong transformation of the shape of the characteristics (Figure 6.27a) does not allow us to perform a reliable extraction of ΔV_D for the largest V_d. The strongly recoverable part (Figure 6.27c,d) initially increases versus V_d and shows the presence of an NBTI-like fast trap shift. However, the stresses with larger V_d lead to a decrease of the degradation which indicates that

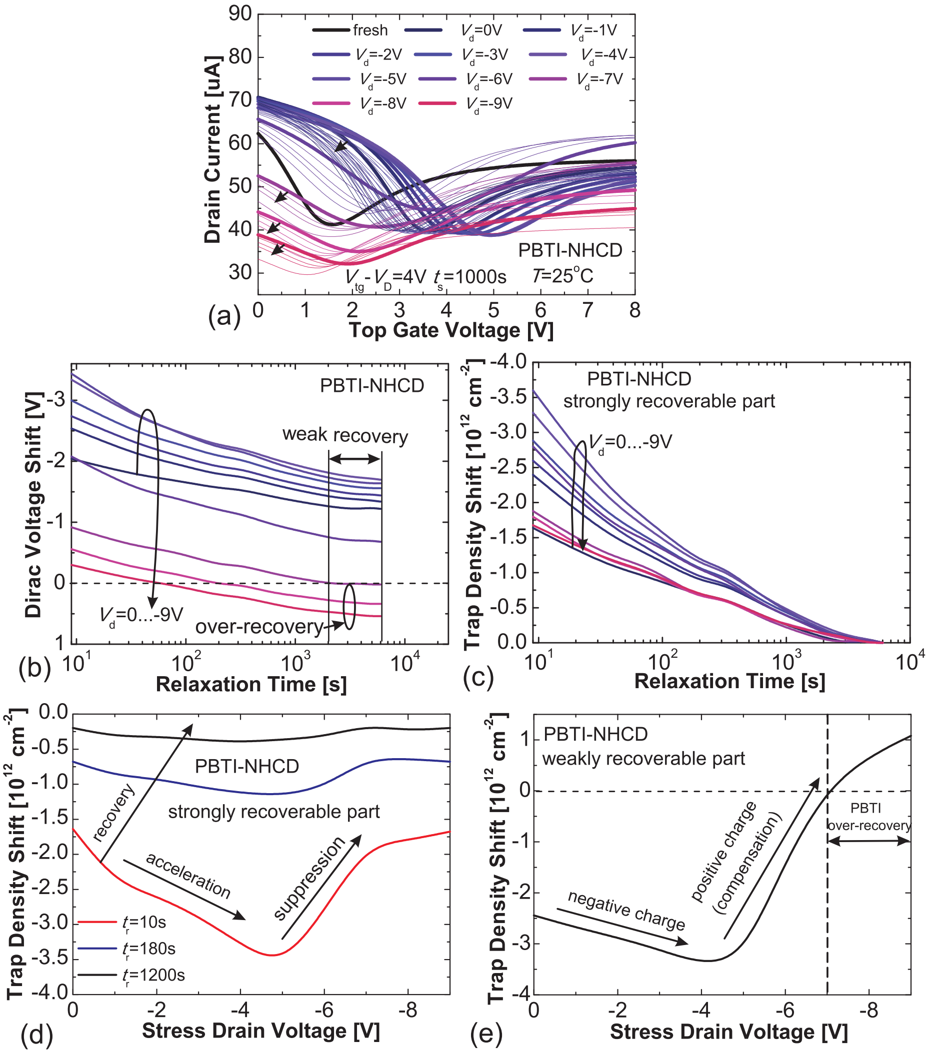


Figure 6.26: (a) Time evolution of the top gate transfer characteristics after subsequent PBTI-NHCD stresses. (b) Contrary to Figure 6.25, the PBTI-like degradation at smaller V_d is significantly accelerated by NHCD which is able to create a negative charge. However, this is mainly associated with the strongly recoverable part of the recovery traces (c,d). At larger V_d the strongly recoverable part is suppressed by NHCD but remains PBTI-like due to the presence of a larger negative charge density (d), unlike Figure 6.25. The weakly recoverable part (e) is similar to the previous case, although an increase of negative charge density obviously proceeds faster. The presence of an extra positive charge at larger V_d leads to over-recovery of PBTI (b).

positively charged defects disappear, similarly to Si technologies [69]. The weakly recoverable part (Figure 6.27e) behaves in the same manner which suggests the absence of any interplay between the defects with different signs in the considered case.

Figure 6.28 presents the related results for NBTI-NHCD. In this case the bias component is suppressed by the PBTI-like NHCD component at smaller V_d and becomes significantly pronounced at larger V_d when NHCD is NBTI-like. Interestingly, in all cases except $V_\mathrm{d} = 0$ (pure NBTI) the strongly recoverable part (Figure 6.28c,d) in addition to the NBTI-like fast trap contains a PBTI-like slow trap contribution which is obviously associated with NHCD. This means that despite the overall NBTI-like nature at larger V_d, NHCD creates some negatively

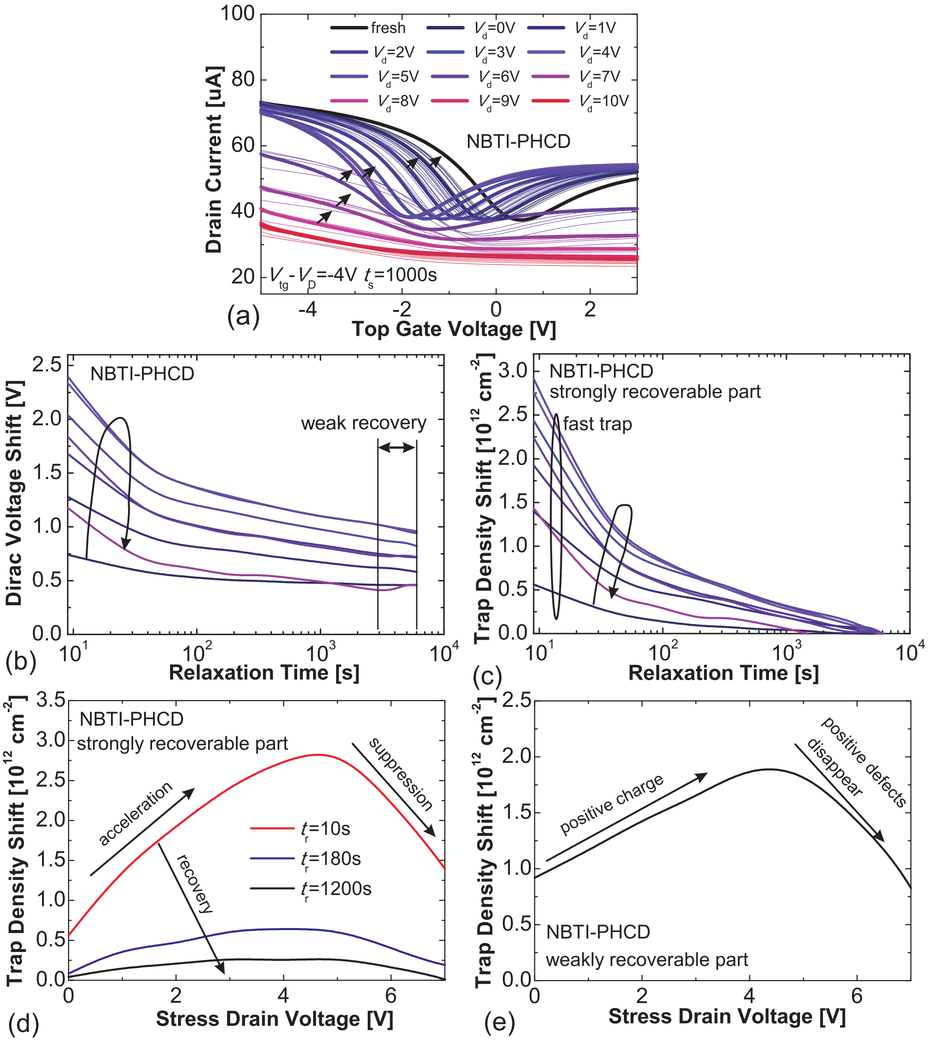


Figure 6.27: (a) Time evolution of the top gate transfer characteristics after subsequent NBTI-PHCD stresses. (b) In contrast to the previous two cases, both the HC and the bias component create positively charged defects. Thus, the degradation/recovery dynamics are completely NBTI-like and the recovery traces contain some kinks associated with fast traps, similarly to pure NBTI in GFETs. Interestingly, both strongly (c,d) and weakly (e) recoverable parts have similar behavior versus V_d. At smaller V_d they increase, showing that the HC and the bias components create defects of the same sign. However, at larger V_d the degradation in terms of ΔN_T becomes less pronounced, suggesting the disappearance of some positively charged defects, similarly to Si technologies [69]. Also, strong transformation of the curve shape does not allow for reliable extraction of ΔV_D for the largest V_d.

charged defects. The weakly recoverable part (Figure 6.28e) at smaller V_d is associated with an insignificant amount of negative charges which leads to over-recovery of NBTI-like degradation. At larger V_d the positive charge results in incomplete recovery.

The results above show that in the case of NBTI-PHCD we are dealing only with positively charged defects, while NBTI-NHCD introduces a large amount of positive charges and some insignificant amounts of negatively charged defects. At the same time, PBTI-PHCD and PBTI-NHCD are associated with a strong interaction between defects with opposite signs introduced by the bias and hot carrier components. In order to study this interaction in more detail, we repeat our experiments for the latter two issues at $T = 120\,^\circ\mathrm{C}$.

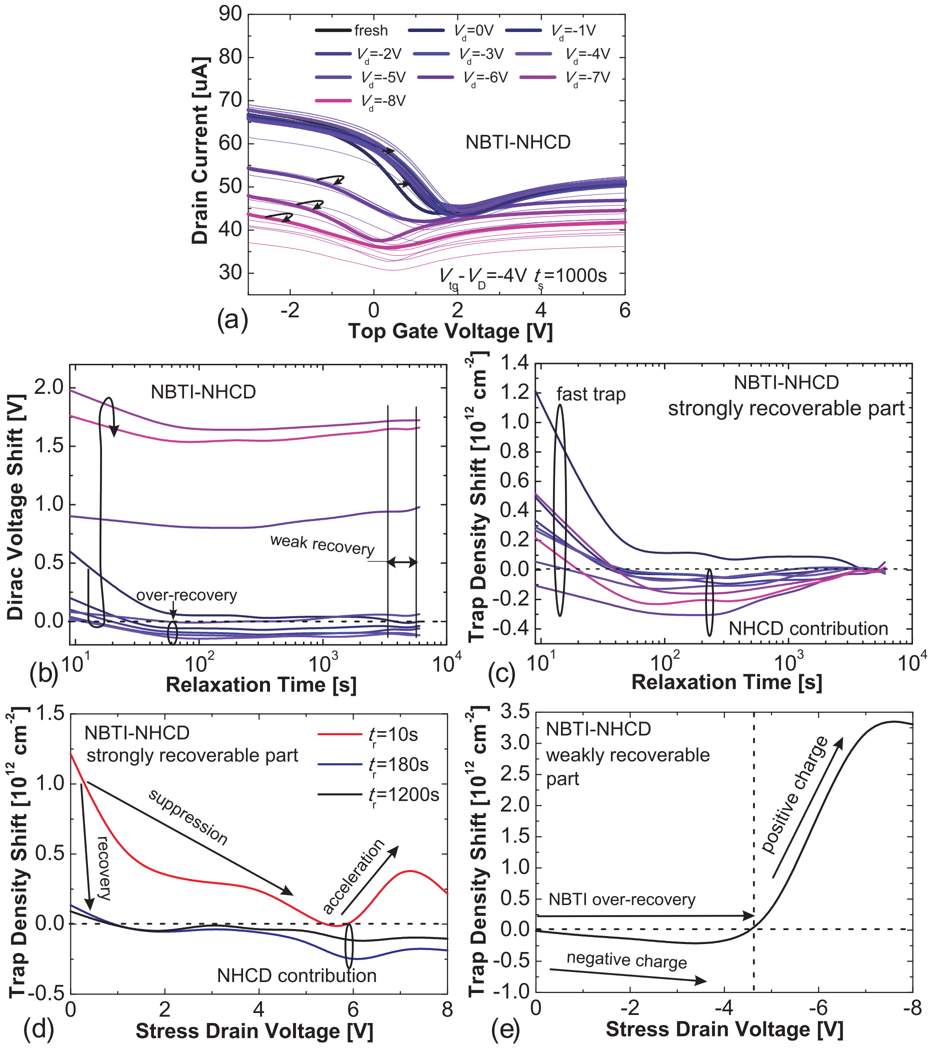


Figure 6.28: (a) Time evolution of the top gate transfer characteristics after subsequent NBTI-NHCD stresses. (b) At smaller V_d, NBTI-like degradation is suppressed by the NHCD component, creating negatively charged defects. However, at larger V_d an NBTI-like degradation is observed because both the HC and the bias component create positively charged defects. The strongly recoverable part (c,d) for all non-zero V_d consists of an NBTI-like fast trap and PBTI-like contribution of NHCD (slow trap). The presence of the latter at larger V_d means that NHCD is able to create some negatively charged defects even at large V_d. The weakly recoverable part (e) is contributed to by a NHCD-induced negative charge at smaller V_d and a positive charge created by both the HC and the bias component at larger V_d. The former is not very significant and thus leads to only a slight over-recovery of NBTI-like degradation.

In Figure 6.29 we compare the ΔV_D recovery traces for PBTI-PHCD measured at $T = 25\,^\circ\mathrm{C}$ and $T = 120\,^\circ\mathrm{C}$. Clearly, at both temperatures we observe a strong suppression of PBTI degradation by the PHCD component and over-recovery as well as an NBTI-like fast trap response supplemented at larger V_d. However, comparison of the results obtained at different temperatures shows that at $T = 120\,^\circ\mathrm{C}$ compensation of PBTI degradation by the PHCD contribution becomes pronounced starting at smaller V_d, while NBTI-like fast traps also appear earlier. Therefore, we conclude that the PHCD component is accelerated at a higher temperature. The related results for PBTI-NHCD are shown in Figure 6.30. Contrary to the previous case, the NHCD component

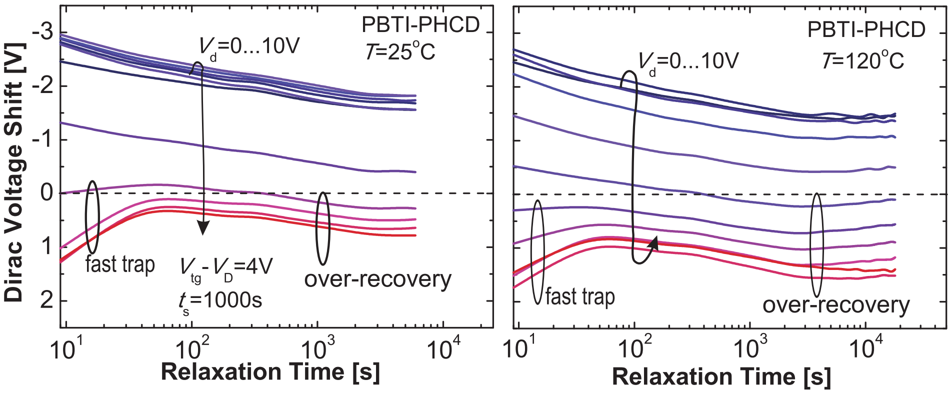


Figure 6.29: The ΔV_D recovery traces measured after subsequent PBTI-PHCD stresses with increasing PHCD component at $T = 25\,°C$ (left) and $T = 120\,°C$ (right). In both cases PBTI degradation is compensated by the PHCD component. The latter introduces additional weakly recoverable positively charged defects which lead to over-recovery beyond the initial Dirac point and also add an NBTI-like fast trap response. At a higher temperature these effects become more pronounced, which means that the PHCD component is accelerated by temperature.

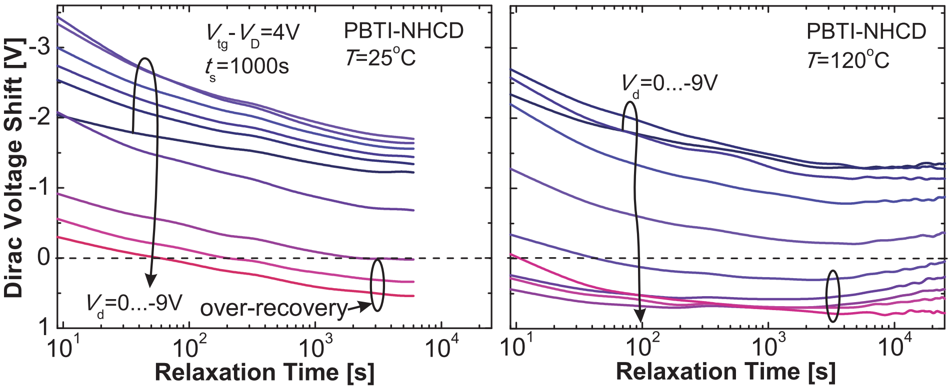


Figure 6.30: The ΔV_D recovery traces measured after subsequent PBTI-NHCD stresses with an increasing NHCD component at $T = 25\,°C$ (left) and $T = 120\,°C$ (right). At $T = 25\,°C$, PBTI degradation is first accelerated and then suppressed by the NHCD component, while at $T = 120\,°C$ the compensation takes place independently of the NHCD magnitude. Therefore, the NHCD component is able to introduce some negative charges, contrary to its PHCD counterpart. However, at higher temperature this asymmetry is significantly less pronounced and consists only in the absence of NBTI-like fast traps in the case of PBTI-NHCD.

is able to introduce some negative charges at smaller V_d. This leads to acceleration of the PBTI component at $T = 25\,°C$. Conversely, a strong NHCD component acts in the same manner as PHCD and leads to a compensation of the PBTI degradation and over-recovery. As for the case of $T = 120\,°C$, the NHCD component compensates PBTI independently of V_d. However, NBTI-like fast traps are not present, which suggests that some asymmetry between the PHCD and NHCD components is still pronounced at $T = 120\,°C$. Interestingly, for both PBTI-PHCD and PBTI-NHCD the weakly recoverable positive charges introduced by the hot carrier components tend to recover at high T, i.e. the Dirac point starts to return back to its original value.

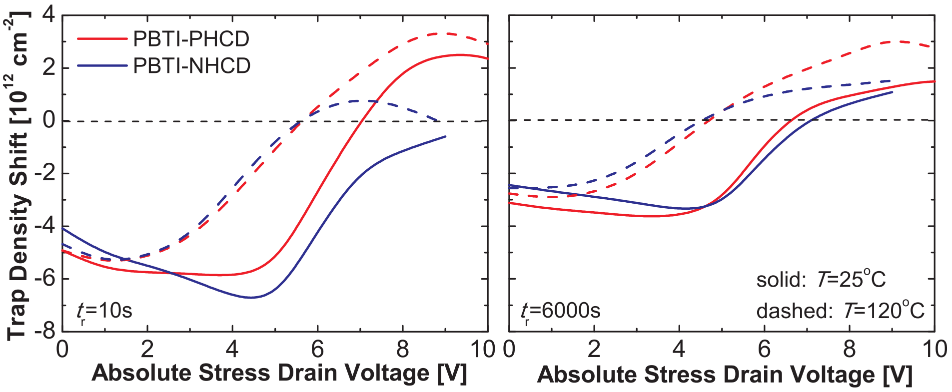


Figure 6.31: Defect density shifts vs. V_d for PBTI-PHCD and PBTI-NHCD at two different relaxation time points: $t_\mathrm{r} = 10\,\mathrm{s}$ (right) and $t_\mathrm{r} = 6000\,\mathrm{s}$ (left). The results corresponding to $T = 25\,°\mathrm{C}$ and $T = 120\,°\mathrm{C}$ are plotted. At $T = 120\,°\mathrm{C}$ the charge compensation region is wider and the concentration of weakly recoverable positive charges is larger. Also, the significant difference between PBTI-PHCD and PBTI-NHCD visible at $T = 25\,°\mathrm{C}$, especially 10 s after the stress, becomes less pronounced at higher temperatures.

6.7.3 Impact of HCD on Charged Trap Density and Carrier Mobility

The top gate transfer characteristics measured at different stress/recovery stages for various HCD issues in GFETs contain the information on both charged trap density and carrier mobility. The former is associated with the Dirac point voltage shift, while the latter can be captured by analyzing the shape of the I_d-V_tg curve at a certain recovery stage. Therefore, we can now perform a more detailed analysis of the experimental results provided in Figures 6.25– 6.30, and study the variation of the charged trap density and mobility after HCD stresses with different polarities. Also, a correlation between the two quantities can be analyzed.

In Figure 6.31 we depict the resulting charged trap density shifts extracted from the recovery traces given in Figures 6.29– 6.30. Clearly, the asymmetry between PBTI-PHCD and PBTI-NHCD observed 10 s after the stresses at $T = 25\,°\mathrm{C}$ almost disappears at $T = 120\,°\mathrm{C}$ (Figure 6.31(left)). The only conserved trend is that a strong PHCD component introduces more positive charges than the NHCD component of the same magnitude, while the difference is mainly due to NBTI-like fast traps. The related results obtained after 6000 s recovery (Figure 6.31(right)) show that both PHCD and NHCD components of large magnitude introduce weakly recoverable positive charges. Obviously, the concentration of these defects is larger at a higher temperature, leading to a stronger over-recovery (cf. Figures 6.29– 6.30). Also, the range of stress V_d within which the charge compensation takes place is wider at $T = 120\,°\mathrm{C}$. The reason for this is that not only the hot carrier, but also the bias component becomes more pronounced at a higher temperature. Therefore, at $T = 120\,°\mathrm{C}$ a strong interplay between defects with opposite signs introduced by the PBTI and HCD components starts at smaller V_d.

Analysis of the transfer characteristics given in Figures 6.25– 6.26 allows us to determine the transconductance G_m and extract electron and hole mobility [178] at all PBTI-PHCD and PBTI-NHCD stress/recovery phases. In Figure 6.32, the obtained values related to the mobilities measured before the stress (typically 20–60 $\mathrm{cm}^2/\mathrm{Vs}$ for electrons and 90–150 $\mathrm{cm}^2/\mathrm{Vs}$ for holes) are plotted versus stress V_d. One can see that in both cases the electron mobility increases with respect to its initial value, an effect which becomes more pronounced at $T = 120\,°\mathrm{C}$. At both temperatures the electron mobility maximum is located within the V_d range corresponding to the charge compensation region (cf. Figure 6.31). This behaviour is more likely related to

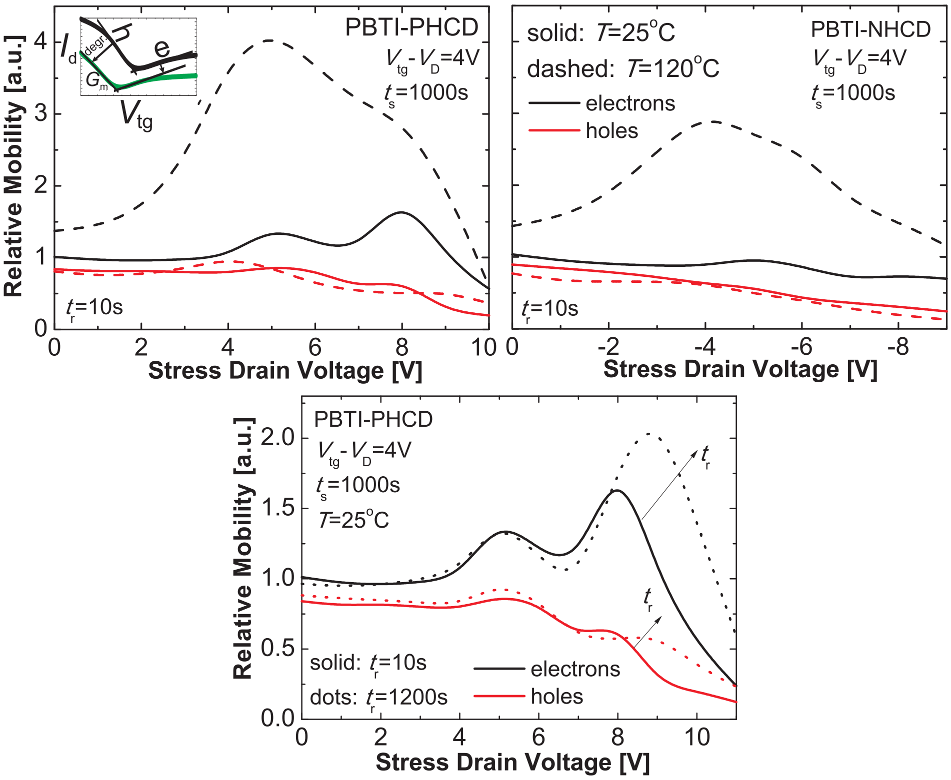


Figure 6.32: Top: Relative mobility vs. V_d for PBTI-PHCD (left) and PBTI-NHCD (right) at two different temperatures. In both cases the electron mobility increases with respect to its initial value, which is likely associated with screening effects and becomes more visible at $T = 120\,°C$. The position of the electron mobility maximum corresponds to the charge compensation region, which is also more pronounced at higher temperatures (Figure 6.31). Therefore, the mobility and charged trap density variations are correlated. Bottom: Relative mobility vs. V_d for PBTI-PHCD measured at $T = 25\,°C$ for $t_r = 10\,s$ and $t_r = 1200\,s$. After the recovery of the NBTI-like fast traps ($t_r = 1200\,s$) the electron mobility maximum becomes larger, since the concentration of the positively charged defects decreases and the impact of screening effects becomes more important.

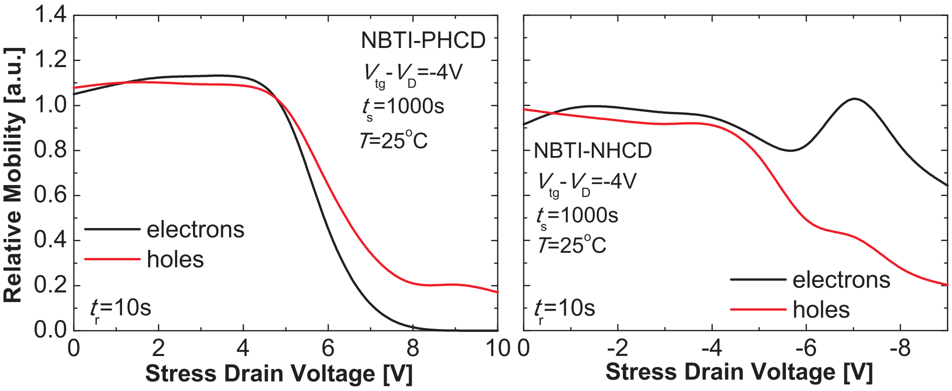


Figure 6.33: Relative mobility versus V_d for NBTI-PHCD (left) and NBTI-NHCD (right). At smaller V_d the created charge is insufficient for a mobility degradation. At larger V_d the degradation of electron and hole mobility is nearly symmetric in the case of NBTI-PHCD. This suggests that scattering at neutral imperfections dominates [131, 97]. However, the electron mobility degrades considerably more, which is likely due to the presence of positively charged defects acting as attractive scattering centers for electrons. For NBTI-NHCD, screening effects reduce degradation of electron mobility.

screening effects [97] which accompany the interplay between the defects with opposite signs. Obviously, at higher temperatures charge compensation starts at smaller V_d but proceeds more slowly, making the interplay between different defects and, consequently, the electron mobility maximum more pronounced. Moreover, the relative decrease in electron mobility after the maximum is stronger than for holes. This is because of the presence of additional positively charged defects. Such defects cause electrons and holes to experience attractive scattering and repulsive scattering, respectively. Furthermore, attractive scattering is known to be stronger than repulsive scattering [131]. Conversely, at small V_d, when negatively charged defects dominate, the relative degradation of the hole mobility is stronger. At the same time, in the case of PBTI-PHCD at $T = 25\,^\circ\mathrm{C}$ there are two maxima: the first one corresponds to the beginning of charge compensation and the second one appears near the transition point and significantly increases after the recovery of the fast trap component (Figure 6.32(bottom)). The latter indicates that the positive charge introduced by the fast traps contributes to the attractive scattering of electrons. Therefore, we can conclude that the observed mobility change not only correlates with a variation of the charged trap density, but also agrees with the attractive/repulsive scattering asymmetry reported in [131]. At the same time, the impact of screening effects on the mobility means that an interaction between the defects with opposite signs introduced by bias and hot carrier components takes place in terms of both their charges and potentials, while being considerably more pronounced at higher temperatures.

In Figure 6.33 the related results for NBTI-PHCD and NBTI-NHCD measured at $T = 25\,^\circ\mathrm{C}$ (cf. Figures 6.27– 6.28) are provided. In both cases the charge created at smaller V_d is insufficient to cause significant mobility degradation because the defects are mainly introduced by the bias component and therefore situated at a considerable distance from the graphene channel. In the case of NBTI-PHCD, larger V_d causes a nearly symmetric decrease of the electron and hole mobilities. This suggests scattering at neutral imperfections [131, 97] which most likely substitute disappearing positive defects (cf. Figure 6.27d,e). However, the degradation of electron mobility is stronger, which is due to the presence of positive charges. Most likely, at larger V_d these defects are situated in the proximity of the graphene channel, which makes their contribution to attractive scattering of electrons more significant. The results for NBTI-NHCD show that at moderate V_d the electron mobility is affected by screening, similarly to PBTI-PHCD and PBTI-NHCD. However, the magnitude of screening effects in the case of NBTI-NHCD is significantly smaller, since the concentration of negatively charged defects is not enough for a considerable compensation of positive charges (Figure 6.28).

6.7.4 Similarities to BTI and Fitting with General Models

The results for HCD discussed above were obtained using the V^+ sweep mode when measuring the top gate transfer characteristics. That is why in the case of NBTI-like degradation, the presence of the fast trap response on the $\Delta V_\mathrm{D}(t_\mathrm{r})$ recovery traces is obvious. However, in the case of pure BTI, the suppression of the fast trap contribution using the V^- sweep mode allowed us to fit the experimental ΔV_D recovery with the capture/emission time (CET) map model [69] and the universal relaxation function [61, 64] previously developed for Si technologies. Taking into account the similarities between BTI and HCD in GFETs, which are mostly associated with the absence of dangling bonds, we proceed with applying these general models to fit the HCD dynamics in GFETs. In order to do so, we have performed similar HCD experiments using our experimental technique which employs subsequent stress/recovery rounds with constant V_d and increasing t_s, while using the V^- sweep mode when measuring the transfer characteristics.

As mentioned above, the CET map model [69] assumes that charge exchange associated with

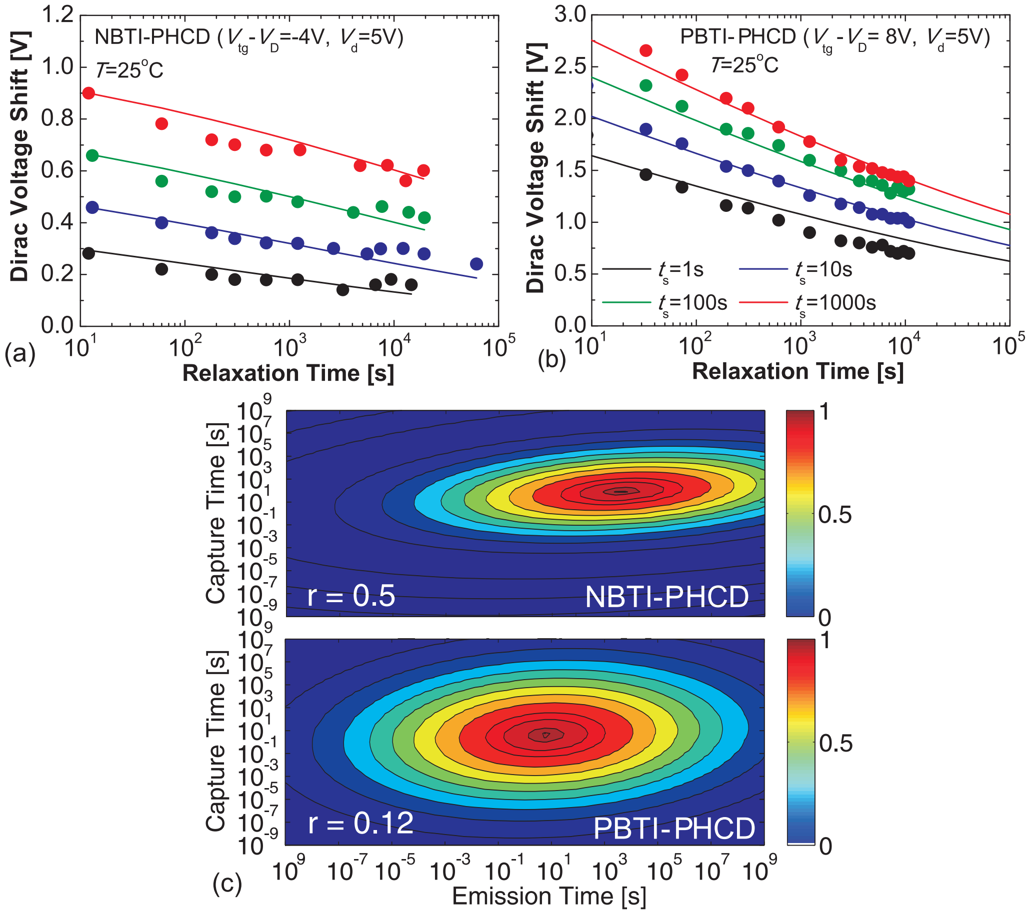


Figure 6.34: Similarly to the case of pure BTI, recovery traces measured after both NBTI-PHCD (a) and PBTI-PHCD (b) stress can be fitted with the CET map model [69] using a single bivariate Gaussian distribution. This, however, only works if the degradation is mainly due to defects of one sign, which is either the case for NBTI-PHCD or PBTI-PHCD with large V_{tg} - V_{D}. Under these conditions the dynamics of HCD are similar to BTI, possibly because of the absence of dangling bonds in GFETs, making the defects responsible for BTI and HCD similar. (c) Underlying CET distributions obtained using the optimized CET map model are similar to those obtained for BTI in GFETs (cf. Figures 6.13– 6.14).

BTI degradation/recovery is thermally activated, while the correlated activation energies can be described using bivariate Gaussian distributions. The main parameters of the model are the mean values (μ_{c} and μ_{e}) and the standard deviations (σ_{c} and σ_{e}) of the capture and emission energies E_{c} and E_{e}, respectively. In addition, an uncorrelated part of the emission energy ΔE_{e} and the corresponding $\mu_{\Delta\mathrm{e}}$ and $\sigma_{\Delta\mathrm{e}}$ are considered. However, it was found that the use of the original model [69] not always produces reasonable results, especially when trying to fit HCD recovery traces in GFETs. This is most likely because V_{D} shifts in GFETs are significantly larger than threshold voltage shifts in Si technologies. Therefore, we suggest modifying the model [69] by changing the implict correlation between the standard deviations $\sigma_{\mathrm{e}}^2 = r\sigma_{\mathrm{c}}^2 + \sigma_{\Delta\mathrm{e}}^2$ with r being a new model parameter which can be varied between 0 and 1, while in [69] r was equal to 1. Thus the distribution is given by:

$$g(E_{\mathrm{c}},\,E_{\mathrm{e}}) = \frac{1}{2r\pi\sigma_{\mathrm{c}}\sigma_{\Delta\mathrm{e}}}\exp\Big(-\frac{(rE_{\mathrm{c}}-\mu_{\mathrm{c}})^2}{2r^2\sigma_{\mathrm{c}}^2}-\frac{(E_{\mathrm{e}}-(rE_{\mathrm{c}}+\mu_{\Delta\mathrm{e}}))^2}{2\sigma_{\Delta\mathrm{e}}^2}\Big). \tag{6.21}$$

The results obtained for NBTI-PHCD and PBTI-PHCD are shown in Figure 6.34. While only

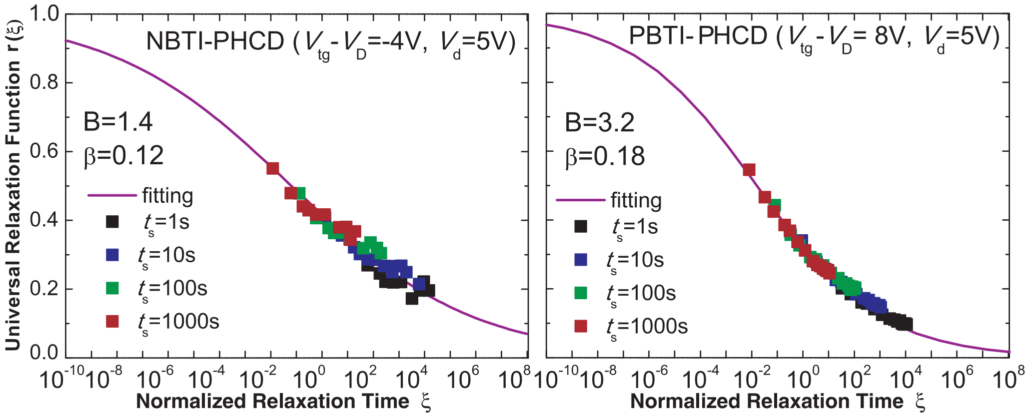


Figure 6.35: HCD in GFETs can be fitted using the universal relaxation relation [61, 64] $r(\xi)=1/(1+B\xi^{\beta})$, while the parameters B and β remain similar to their counterparts for BTI in both GFETs and Si technologies (cf. Figure 6.12). However, the limitations are the same as in the case of the CET map model.

a single Gaussian distribution corresponding to a more recoverable component has been used, the fits (Figure 6.34a,b) of the recovery traces are rather reasonable. This underlines the similarity between HCD and BTI dynamics in GFETs. The underlying CET map distributions (Figure 6.34c) are also similar to those obtained for BTI in GFETs (cf. Figures 6.13– 6.14). Moreover, the dynamics of HCD in GFETs can be also described by the universal relaxation model [61, 64] (Figure 6.35). Remarkably, the parameters B and β given in the plots are similar to their counterparts obtained from BTI data for both GFETs and Si technologies (Figure 6.12). This further confirms the similarity in the physical mechanisms underlying degradation/recovery dynamics.

However, the described analysis is typically only possible if both HC and bias components introduce defects of the same sign (e.g. NBTI-PHCD). Otherwise, if the two contributions have opposite signs (e.g. PBTI-PHCD), fitting is only possible for stress conditions under which the bias component dominates. At the same time, the dynamics of PBTI-PHCD with comparable HC and bias components (e.g. Figure 6.29) are more complicated and therefore can not be described using such simple models [61, 64, 69].

6.8 Chapter Conclusions

In summary, we have performed a detailed study of both BTI and HCD dynamics in GFETs. First, we found that high-temperature baking of devices leads to a decrease in device-to-device variability, which either allows us to perform numerous measurements on the same device or obtain consistent results for different stress conditions on similar devices. Together with an optimized experimental technique, in which a constant oxide field is sustained during all measurements, this allowed us to obtain experimental results for BTI in GFETs which are fully consistent with Si technologies. Thus, the BTI assessment methodology suggested in this chapter is generally suitable for quantifying the quality and reliability of graphene FETs and graphene/dielectric interfaces. Furthermore, we have demonstrated that the BTI dynamics on the back gate of our GFETs are similar to those on the high-k top gate, although the latter is less stable with respect to BTI. Next, we have classified those reliability issues in GFETs which are associated with HCD and investigated their impact on device performance. In particular, it was shown that the interplay between the bias and the hot carrier stress components is stronger if the HC stress acts in conjuction with PBTI, while the qualitative drift-diffusion simulations allowed us to understand the origin of this behaviour. Moreover, we have demonstrated that HCD impacts both the charged trap density shift and the mobility which are correlated, while the mobility variation agrees with the previously reported attractive/repulsive scattering asymmetry[131]. Finally, we have demonstrated that, similarly to pure BTI in both GFETs and Si technologies, for some stress conditions the long-term HCD data can be well fitted with the CET map model and also with the universal relaxation relation. Therefore, our systematic method for benchmarking new graphene technologies was extended to the case of HCD.

7 Reliability of MoS_2 FETs

Limitations of graphene associated with the lack of a bandgap do not allow for the creation of GFETs with a high on/off ratio, thus making integration of these devices into digital circuits impossible. Therefore, alternative 2D materials with considerable bandgaps are currently being sought. One of these materials is MoS_2, which is already being successfully applied as a 2D channel in next-generation FETs. However, similarly to the case of GFETs, the level of technology is still far below Si standards and requires further improvement. Hence, the characterization of reliability of MoS_2 FETs, i.e. the subject of this chapter, is essential. Moreover, the band structure of MoS_2 is more similar to conventional semiconductors rather than graphene. This allows comparably simple implementation of this material into professional simulation software, such as Minimos-NT. Some of these simulation results are discussed at the end of this chapter.

7.1 Introduction

Since the first practical realization of MoS_2 FETs in 2011 [141], a number of other attempts at fabricating related devices with either SiO_2 [141, 30, 140, 101, 43, 52, 139, 26, 110, 193, 100], Al_2O_3 [95, 24] or hBN [104] as a gate insulator have been undertaken. Although one could expect each of these attempts to be accompanied by at least some reliability analysis, papers which address the question of MoS_2 FETs reliability are still lacking [101, 140, 110, 104, 139, 26, 193, 24]. Moreover, even these few studies are mostly restricted to the observation of a hysteresis in the gate transfer characteristics for different measurement conditions [101, 140, 104, 24, 110], while typically reporting extremely poor hysteresis stability of the analyzed devices. At the same time, attempts to analyze BTI in MoS_2 FETs are rare [26, 139, 193]. All are limited to MoS_2/SiO_2 FETs, while reporting large enough threshold voltage shifts and not providing any detailed analysis of BTI degradation/recovery dynamics. Also, no analysis of BTI characteristics have been reported for MoS_2 FETs with hBN gate insulators.

In the course of this chapter we perform a detailed study of both the hysteresis and BTI in single-layer MoS_2 FETs with SiO_2, hBN/SiO_2 and hBN insulators, and capture the correlation between these phenomena. As shown below, the devices analyzed within this work significantly outperform their previously reported counterparts with respect to both hysteresis and BTI stability. Also, contrary to all previous BTI studies of MoS_2 FETs, we attempt to capture the observed degradation/recovery dynamics using the models previously developed for Si technologies. While employing the universal relaxation relation as the simplest starting approach, we also provide results simulated using the four-state NMP model, which was adjusted to the case of MoS_2 FET. The latter approach allows us to perform a more detailed analysis of experimentally observed reliability features.

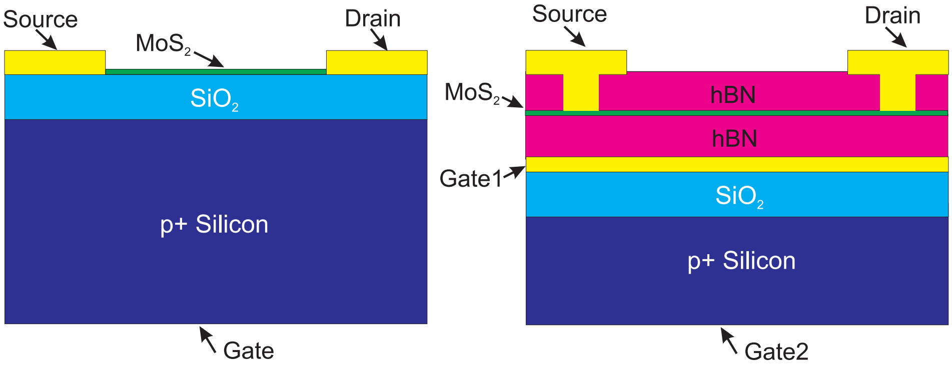


Figure 7.1: Schematic layout of our two single-layer MoS_2 FETs with SiO_2 (left) and hBN (right). The insulator thickness is around 90 nm for both SiO_2 and hBN. The MoS_2/hBN device has two gate contacts: one through the highly doped Si substrate and the other through a Ti/Au pad in between the SiO_2 and hBN layers. This allows us to use either the hBN or the hBN/SiO_2 stack as a gate insulator. The drain and source contacts are made of Ti/Au.

7.2 Investigated Devices: Fabrication and Basic Characteristics

We examine single-layer MoS_2 FETs with SiO_2 and hBN as a gate insulator fabricated by our collaborators at Prof. Mueller's group [47]. The channel length of these devices is around 1 μm, while the width for different FETs can vary between 4 μm and 8 μm. In our MoS_2/SiO_2 devices (Figure 7.1(left)) a MoS_2 channel is situated on top of a 90 nm thick SiO_2 layer. In the second transistors, MoS_2 is sandwiched between two 90 nm thick hBN layers (Figure 7.1(right)). In order to allow for a more detailed analysis of hBN vs. SiO_2, we added an additional Ti/Au gate between the hBN and the SiO_2 layer. Thus, we can operate these devices either with a hBN gate insulator when contacting the Ti/Au plate or with a hBN/SiO_2 stack through the highly doped Si substrate.

The MoS_2/SiO_2 devices were fabricated on double side polished and thermally oxidized Si substrates with a resistivity of $1-5\,\Omega\times$cm and SiO_2 thickness of 90 nm. MoS_2 flakes were mechanically exfoliated from a natural bulk crystal on top of a SiO_2 layer using the method [48]. After, the flakes with the optimal quality were selected using an optical microscope and their final thickness was determined by Raman spectroscopy. This was done in order to identify those with single-layer MoS_2 thickness (i.e. around 6.5 $\mathring{A}$). Then Ti/Au electrodes were created by electron beam lithography and metal evaporation techniques (e.g. [101]).

In the case of MoS_2/hBN devices, a 22 nm thick Ti/Au back gate pad was evaporated on top of a 90 nm thick SiO_2 layer. Next, the hBN/MoS_2/hBN stack produced using the stacking method [103] was placed on top of the Ti/Au pad. The essential ingredients of this stack are mechanically exfoliated single-layer MoS_2 flakes and two 90 nm thick hBN layers, also obtained from bulk hBN crystals[1] using mechanical exfoliation. While single-layer MoS_2 flakes were identified using Raman spectroscopy, the thickness and quality of hBN flakes were controlled using atomic-force microscopy. Also, those hBN flakes which were used as the uppermost layer were pre-structured by electron beam lithography and reactive ion etching in order to create the slots for source and drain contacts. Finally, Ti/Au electrodes were created using electron beam lithography and metal evaporation.

For the primary check of the performance of our devices we measured their gate transfer (I_d-V_g) and output (I_d-V_d) characteristics. The results obtained for MoS_2/SiO_2 and MoS_2/hBN FETs

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[1] The hBN crystals have been bought from HQ Graphene.

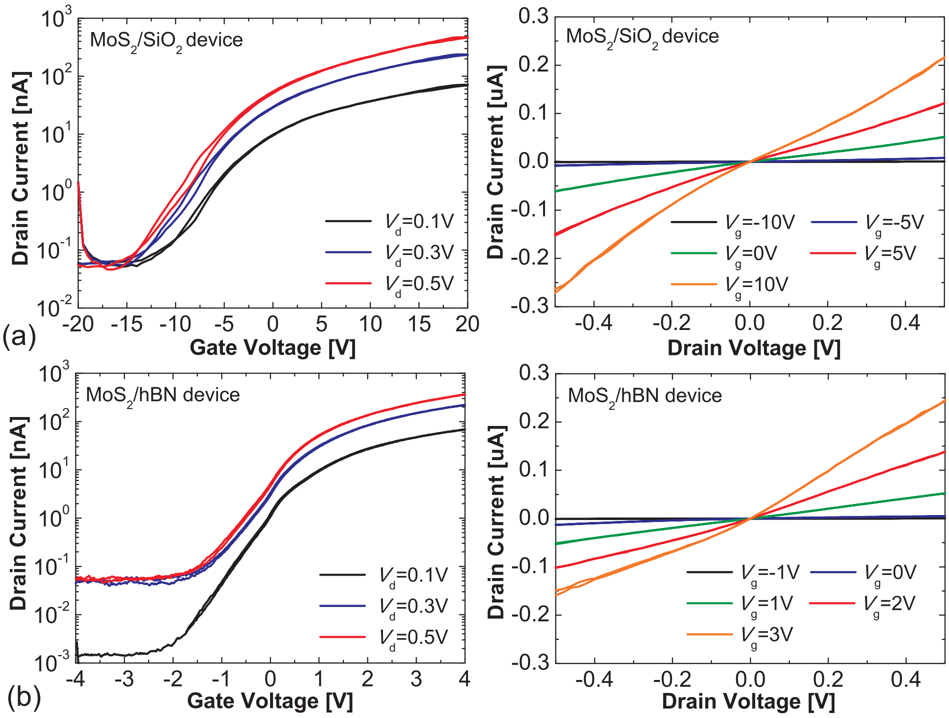


Figure 7.2: The gate transfer (I_d-V_g) and output (I_d-V_d) characteristics of our MoS$_2$ FETs with SiO$_2$ (a) and pure hBN (b). In agreement with [101, 104], the transfer characteristics show some hysteresis due to charging/discharging of fast traps. For MoS$_2$/hBN devices the hysteresis is considerably smaller (cf. [104]). The output characteristics show a quasi-linear current increase within the narrow V_d range used.

are shown in Figure 7.2. Similarly to [101, 104], the gate transfer characteristics of our devices exhibit the behaviour typical for n-FETs with some hysteresis. The latter is associated with charging/discharging of fast traps. Interestingly, for the devices with hBN, the hysteresis is significantly smaller than for their counterparts with SiO$_2$, which is in agreement with [104]. At the same time, the output characteristics of both types of our devices show a quasi-linear behaviour, which is a consequence of the narrow drain voltage intervals [101, 104]. The estimated mobility can reach $1\,\mathrm{cm}^2/\mathrm{Vs}$ for MoS$_2$/SiO$_2$ FETs and $3\,\mathrm{cm}^2/\mathrm{Vs}$ for MoS$_2$/hBN devices. This is larger than for devices with a small number of MoS$_2$ layers and similar channel length [140], while the on/off ratio measured with high current resolution can exceed 10^5.

7.3 Experimental Technique

Similarly to GFETs, the devices with MoS$_2$ are very sensitive to the detrimental impact of the environment [101]. Therefore, all our measurements were performed in a vacuum (5×10^{-6}–10^{-5} torr), while the temperature was either 25°C or 85°C.

The hysteresis was investigated by measuring the I_d-V_g characteristics using $V_\mathrm{d} = 0.1\,\mathrm{V}$ and different sweep rates S. In order to capture the full frequency range of the fast traps responsible for the hysteresis, $S = V_\mathrm{step}/t_\mathrm{step}$ was varied between 0.04 and 8000 V/s by adjusting the step voltage V_step and the sampling time t_step.

The BTI behaviour of MoS$_2$ devices was studied using an experimental technique similar to those previously employed for our GFETs. Namely, subsequent stress/recovery cycles with

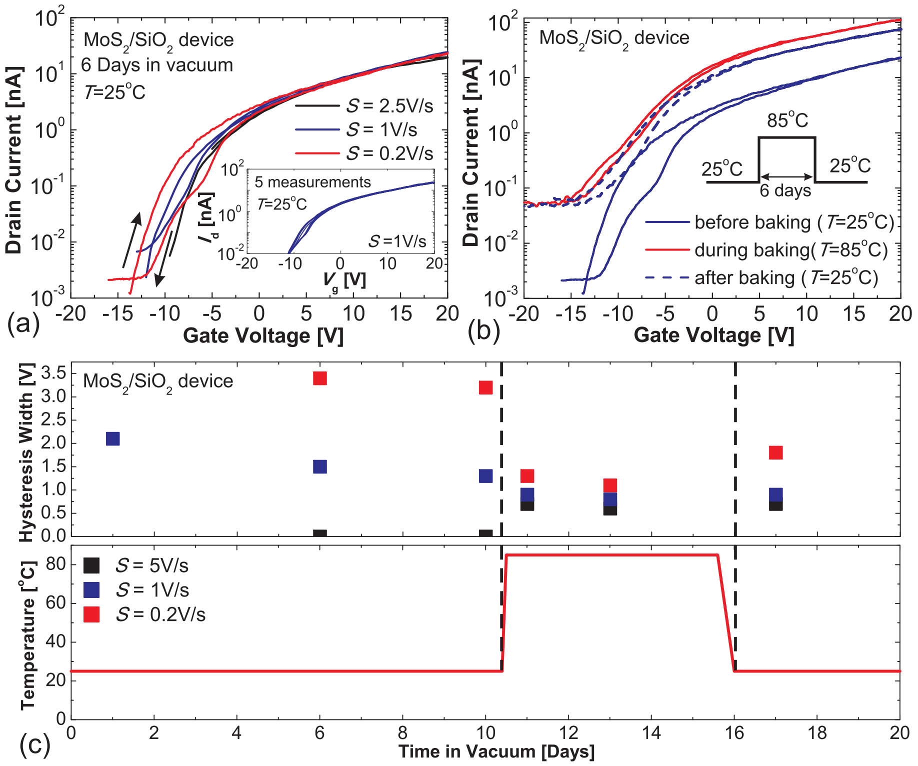


Figure 7.3: (a) The I_d-V_g characteristics of the $\mathrm{MoS_2/SiO_2}$ FET measured with different sweep rates S. Clearly, the hysteresis becomes more pronounced with smaller S, revealing an increasing contribution of slower traps. At the same time, at constant S the hysteresis is stable and well reproducible (inset). (b) At $T = 85°\mathrm{C}$ the drain current is larger, while the slow sweep hysteresis is significantly reduced. After returning back to $T = 25°\mathrm{C}$ following six days of measurements, I_d was considerably larger and ΔV_H considerably reduced. (c) Evolution of ΔV_H measured for the $\mathrm{MoS_2/SiO_2}$ device versus time in the vacuum. During the first days at $T = 25°\mathrm{C}$, a hysteresis is only observed for slow sweeps and decreases with time. At $T = 85°\mathrm{C}$, ΔV_H for small S decreases abruptly. However, the hysteresis suddenly becomes pronounced at larger S. Finally, when T is returned back to 25°C, the slow sweep ΔV_H slightly increases, while nearly no change is seen for fast sweeps. This means that a number of slower traps were annealed at the higher temperature.

either increasing stress time t_s or gate voltage V_g were used for a detailed analysis of BTI degradation/recovery dynamics. By measuring the full I_d-V_g characteristics of our devices at each recovery stage, we were able to extract the threshold voltage shift ΔV_th at a fixed drain current, and express the BTI dynamics in terms of $\Delta V_\mathrm{th}(t_\mathrm{r})$ recovery traces.

7.4 Hysteresis Stability

According to previous literature reports [101, 140, 104], hysteresis stability presents a serious reliability issue for $\mathrm{MoS_2}$ FETs at this early stage of research. Hence, we start our reliability analysis with a detailed study of the hysteresis behaviour of our devices with $\mathrm{SiO_2}$, $\mathrm{hBN/SiO_2}$ and hBN insulators.

An initial check of our $\mathrm{MoS_2/SiO_2}$ devices shows that the I_d-V_g characteristics exhibit some hysteresis even after several days in a vacuum at $T = 25°\mathrm{C}$. While being reproducible at a constant sweep rate, similarly to [101], this hysteresis becomes larger when S is decreased (Figure 7.3a).

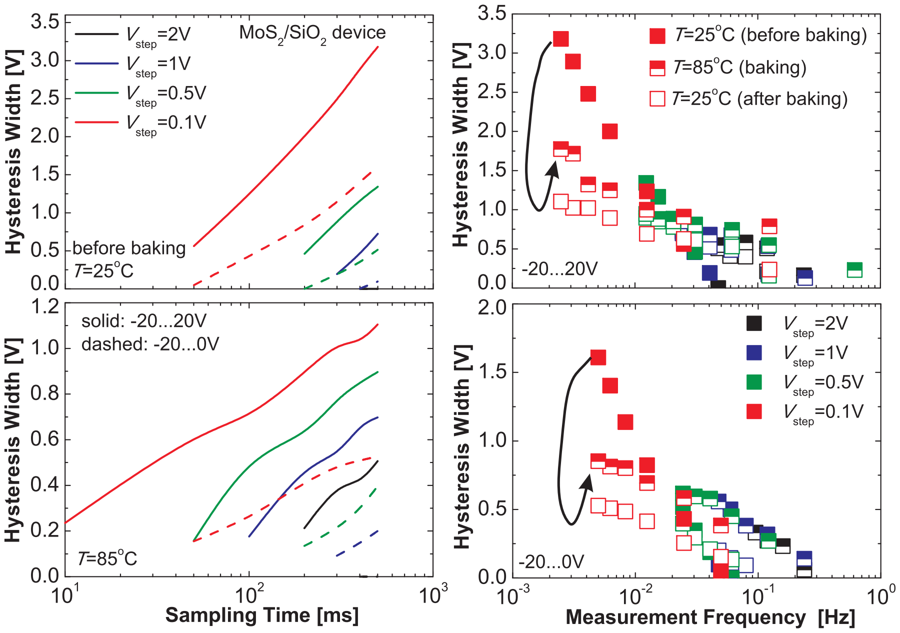


Figure 7.4: Left: The dependence of the hysteresis width on the sampling time t_{step} for different step voltages V_{step} for the MoS_2/SiO_2 device at $T = 25°C$ before baking (top) and at $T = 85°C$ (bottom). During baking at $T = 85°C$ ΔV_{H} is significantly smaller. In agreement with the literature [110], narrower sweep ranges (dashed lines) lead to a scaling of ΔV_{H} for both temperatures. Right: The resulting dependence of ΔV_{H} versus measurement frequency for the sweep ranges -20...20 V (top) and -20...0 V (bottom). The three datasets correspond to the results obtained before, during and after six days at $T = 85°C$. The behaviour of $\Delta V_{\mathrm{H}}(f)$ versus T allows us to conclude that slower traps are annealed and faster ones activated during baking.

When the temperature is increased to 85°C, the drain current increases (Figure 7.3b). At the same time, the hysteresis width ΔV_{H} measured using a very small S significantly decreases. However, when after six days the temperature is changed back to 25°C, both drain current and hysteresis width show only insignificant trends toward their initial values. Hence, after baking, the device exhibits better performance in terms of both I_{d} and ΔV_{H}. The evolution of the hysteresis for our MoS_2/SiO_2 devices at different S versus time in the vacuum and temperature is shown in Figure 7.3c. During the first 10 days at $T = 25°C$, a large hysteresis was observed for small S, while being reduced versus time in the vacuum. At the same time, no significant hysteresis was present when using fast sweeps. However, when increasing the temperature to 85°C, ΔV_{H} measured with small S was significantly reduced, while a considerable hysteresis appeared for large S. Back at 25°C, some increase in hysteresis width measured with small S is pronounced. However, ΔV_{H} did not return to its initial values. This implies that in our MoS_2/SiO_2 FETs, baking anneals a considerable fraction of slower traps, while also introducing some faster traps. Most likely, slower traps are associated with water molecules [101], which can be evaporated from an uncovered MoS_2 surface either during a long time in the vacuum or at higher temperatures. Obviously, in the latter case, annealing of these traps is more intensive, leading to a larger decrease in ΔV_{H}.

We proceed with a detailed analysis of the dependence of the hysteresis width versus sweep rate for our MoS_2/SiO_2 devices. In Figure 7.4 (left) the dependences of ΔV_{H} versus t_{step} and V_{step} for different voltage sweep intervals $V_{\mathrm{gmin}} \ldots V_{\mathrm{gmax}}$ and temperatures are shown. Clearly, in all cases ΔV_{H} increases for larger t_{step} and smaller V_{step}, i.e. smaller $S = V_{\mathrm{step}}/t_{\mathrm{step}}$. By

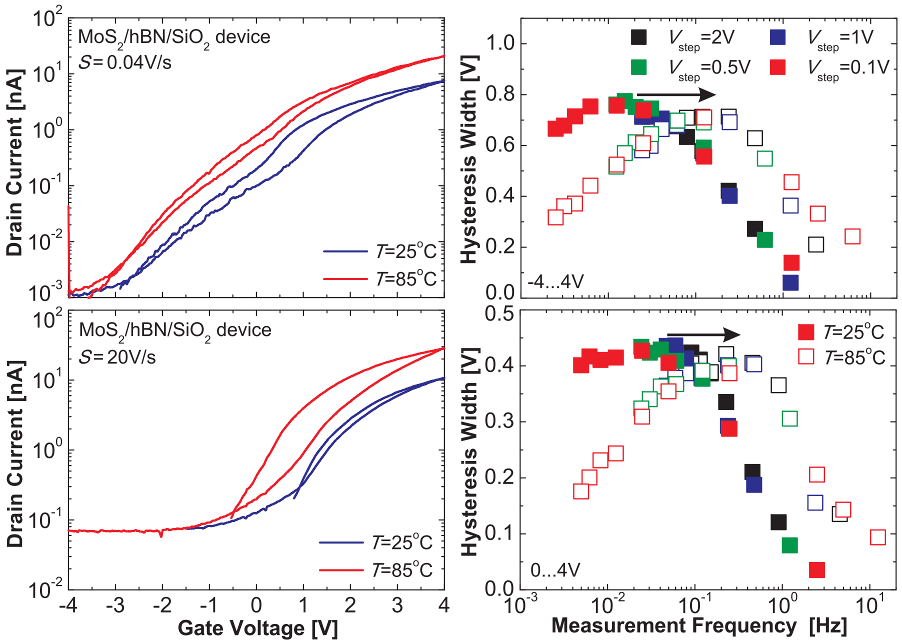


Figure 7.5: Left: The transfer characteristics of the MoS_2 FET with the hBN/SiO_2 stack measured at different temperatures. For small S (top), at $T = 85°C$ the hysteresis is smaller than at $T = 25°C$. However, for larger sweep rates (bottom), ΔV_H becomes significantly larger at higher T, showing a thermally activated behavior of ultra-fast traps. Left: The resulting dependence of ΔV_H versus measurement frequency for the sweep ranges $-4\ldots4\,V$ (top) and $0\ldots4\,V$ (bottom). In both cases we observe a maximum of ΔV_H, which is reduced for narrower sweep ranges. At $T = 85°C$ the maximum is shifted toward higher frequency, which means that the hysteresis becomes dominated by faster traps.

introducing the measurement frequency $f = 1/(Nt_{\text{step}})$ with the number of points $N = 2((V_{\text{gmax}}$-$V_{\text{gmin}})/V_{\text{step}}+1)$, we demonstrate in Figure 7.4 (right) that the obtained experimental points form a universal frequency dependence of ΔV_H. This behaviour depends strongly on T at low frequencies, confirming that slower traps disappear during baking. For higher frequencies, the dependence becomes more pronounced during and after baking, suggesting that defects with smaller capture times become active. Interestingly, the same trends are observed independently of the sweep range, although ΔV_H becomes smaller for narrower sweep ranges (cf. [110]). Thus, in our MoS_2/SiO_2 FETs the temperature treatment reduces the amount of slower traps and activates faster traps.

In Figure 7.5 we show the transfer characteristics measured at different S and temperatures, and $\Delta V_H(f)$ dependences for $MoS_2/hBN/SiO_2$ device. Similarly to MoS_2/SiO_2 devices, ΔV_H measured using a small S is reduced at higher temperatures, while the fast sweep hysteresis becomes significantly larger. However, the hysteresis is pronounced up to larger S, which suggests the existence of a larger contribution of faster traps compared to MoS_2/SiO_2 devices. The resulting frequency dependence contains a maximum of ΔV_H, which shifts towards higher frequency at $T = 85°C$. As such, the temperature dependence is similar to MoS_2/SiO_2 FETs. Figure 7.6 shows the related results for MoS_2/hBN devices. Contrary to the previous two cases, the hysteresis is not present at very small S and can be observed only when using extremely fast sweeps. The frequency dependence confirms that the hysteresis in hBN devices is dominated by ultra-fast traps, while the contribution of slower traps is negligible. Hence, the maximum of ΔV_H is most likely at even higher frequencies outside our measurements range. Also, an increase in ΔV_H at $T = 85°C$ is visible for wider sweep range.

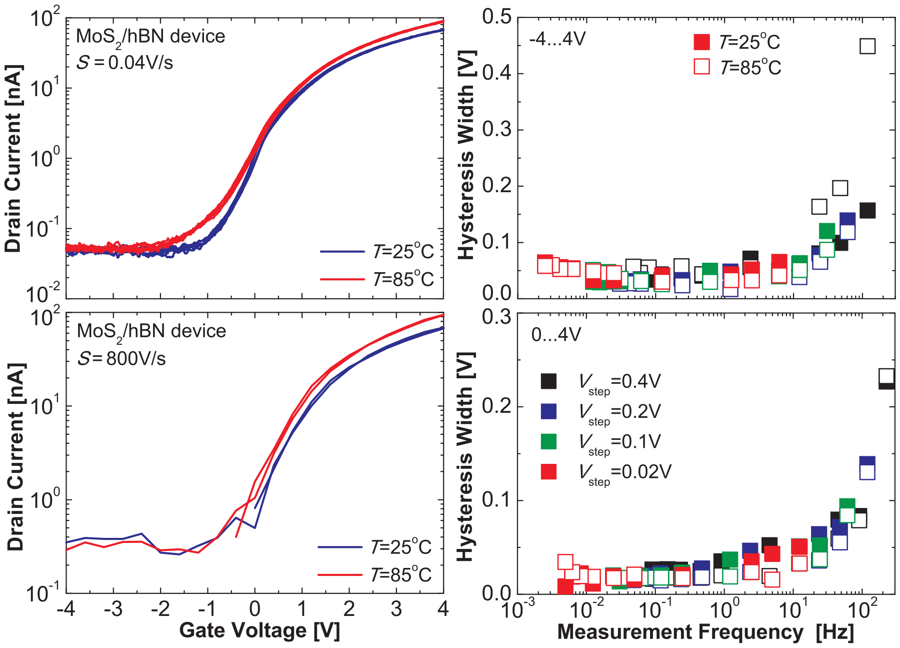
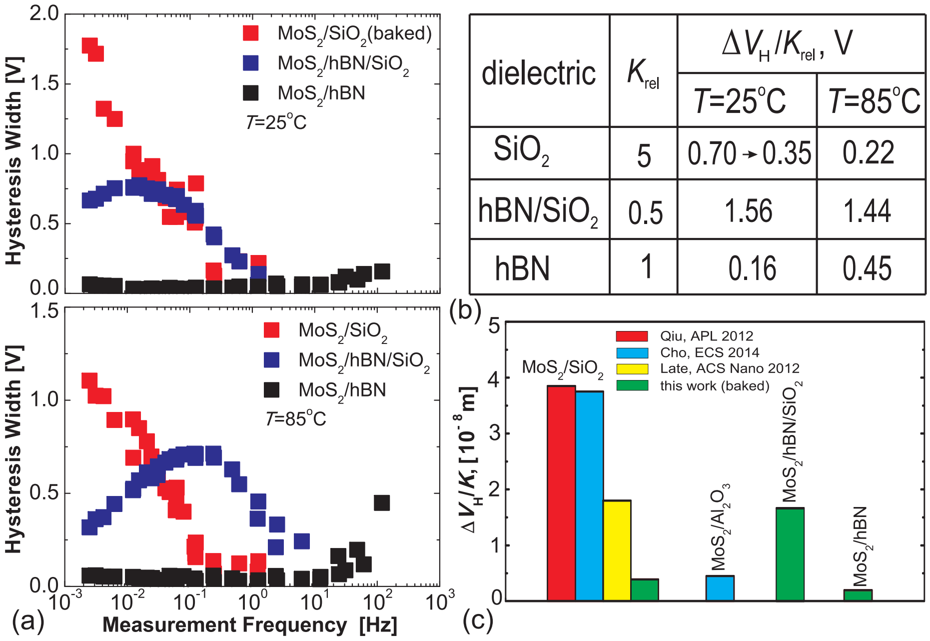


Figure 7.6: Left: The transfer characteristics of the MoS_2 FET with the hBN gate insulator measured at different temperatures. Contrary to the previous two insulators, almost no hysteresis is observed for slow sweeps (top). Conversely, some hysteresis is present for extremely large S (bottom), while becoming larger at $T = 85°C$. Right: The resulting frequency dependence confirms that the fraction of slower traps in these devices is negligible. We observe only some extremely fast traps, which are activated at higher T and are also sensitive to the sweep range.

The results obtained for MoS_2 FETs with different gate insulators allow for a comparison of our finding (see Figure 7.7). While for MoS_2/SiO_2 FETs the hysteresis is mostly dominated by slower traps, for hBN/SiO_2 stacks an increased contribution of faster traps is observed. Hence, in the latter case the maximum of ΔV_H lies within our experimental range. At the same time, in MoS_2/hBN devices the hysteresis is purely related to ultra-fast traps. Interestingly, in all three cases the temperature dependence is similar. Namely, the contribution of slower traps is reduced and the contribution of faster traps is increased at higher T, leading to a shift of the ΔV_H dependence to higher f. In order to compare the maximum values of ΔV_H, we normalize them by the scaling factor $K_{\mathrm{rel}} = K/K_{\mathrm{hBN}}$ with $K = (V_{\mathrm{gmax}}\text{-}V_{\mathrm{gmin}})/d_{\mathrm{ox}}$. This allows to account for the differences in the sweep ranges and insulator thicknesses used for different devices. As shown in Figure 7.7b, our hBN devices exhibit the best hysteresis stability at $T = 25°C$. However, their performance deteriorates at higher temperatures, where they are even outperformed by MoS_2/SiO_2 FETs. Finally, in Figure 7.7c we compare the maximum hysteresis widths ($T = 25°C$) normalized by K obtained within this work with the results from [140, 101, 24]. In all cases the measurements have been performed in vacuum because measurements in the ambient show considerably larger ΔV_H [101]. Although the hysteresis strongly depends on the temperature, the sweep rate and the gate bias sweep range, we can conclude that our MoS_2/SiO_2 and MoS_2/hBN FETs exhibit the best hysteresis stability. As for the $MoS_2/hBN/SiO_2$ devices, they are outperformed only by MoS_2/SiO_2 devices reported in [24].



dielectric	K_{rel}	$\Delta V_H/K_{rel}$, V	
		T=25°C	T=85°C
SiO_2	5	0.70 → 0.35	0.22
hBN/SiO_2	0.5	1.56	1.44
hBN	1	0.16	0.45

Figure 7.7: (a) Comparison of the frequency dependence of ΔV_H for our three devices at $T = 25°C$ (top) and $T = 85°C$ (bottom). In MoS_2/SiO_2 FETs the hysteresis is due to slower traps, while faster traps contribute to the $MoS_2/hBN/SiO_2$ device. Finally, MoS_2 transistors with pure hBN apparently contain mostly ultra-fast traps. In all cases the contribution of slower traps is reduced by temperature. Conversely, the impact of faster traps is thermally activated. (b) Comparison of the maximum ΔV_H normalized by the scaling factor K_{rel} relative to the MoS_2/hBN value. Clearly, MoS_2/hBN FETs exhibit the best performance at $T = 25°C$, and MoS_2/SiO_2 devices at $T = 85°C$. (c) Comparison of the normalized hysteresis width ΔV_H of our MoS_2 FETs with literature results measured in vacuum at $T = 25°C$ [140, 101, 24]. The values obtained for our MoS_2/SiO_2 and MoS_2/hBN devices are the smallest.

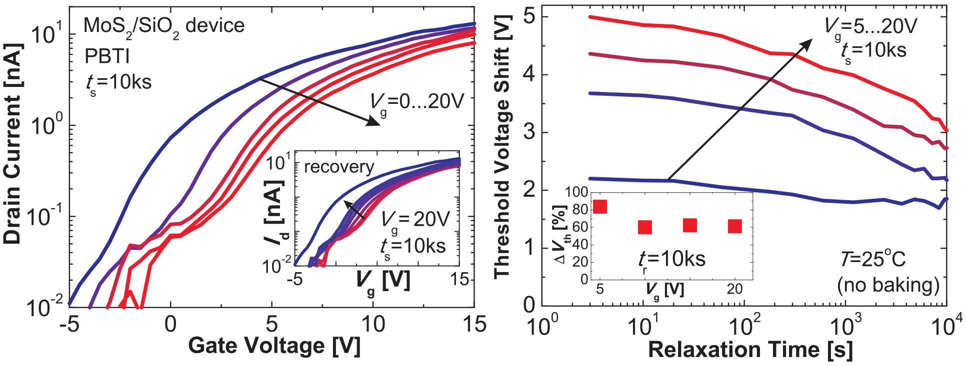


Figure 7.8: Left: Degradation of the gate transfer characteristics of the MoS_2/SiO_2 FET after subsequent PBTI stresses with stress time $t_s = 10$ ks and increasing V_g. The inset shows the time evolution of the I_d-V_g characteristics during recovery. Right: The resulting recovery traces for the threshold voltage shift ΔV_{th}. The degradation is partially recoverable and strongly increases with increasing stress V_g. While for the stress with $V_g = 5$ V the relative ΔV_{th} remaining after a relaxation time $t_r = 10$ ks is around 85% of the initially measured value, for stronger stresses it is close to 60%. Note that the measurements of the full I_d-V_g sweep at each recovery point introduce a delay of about 3 s.

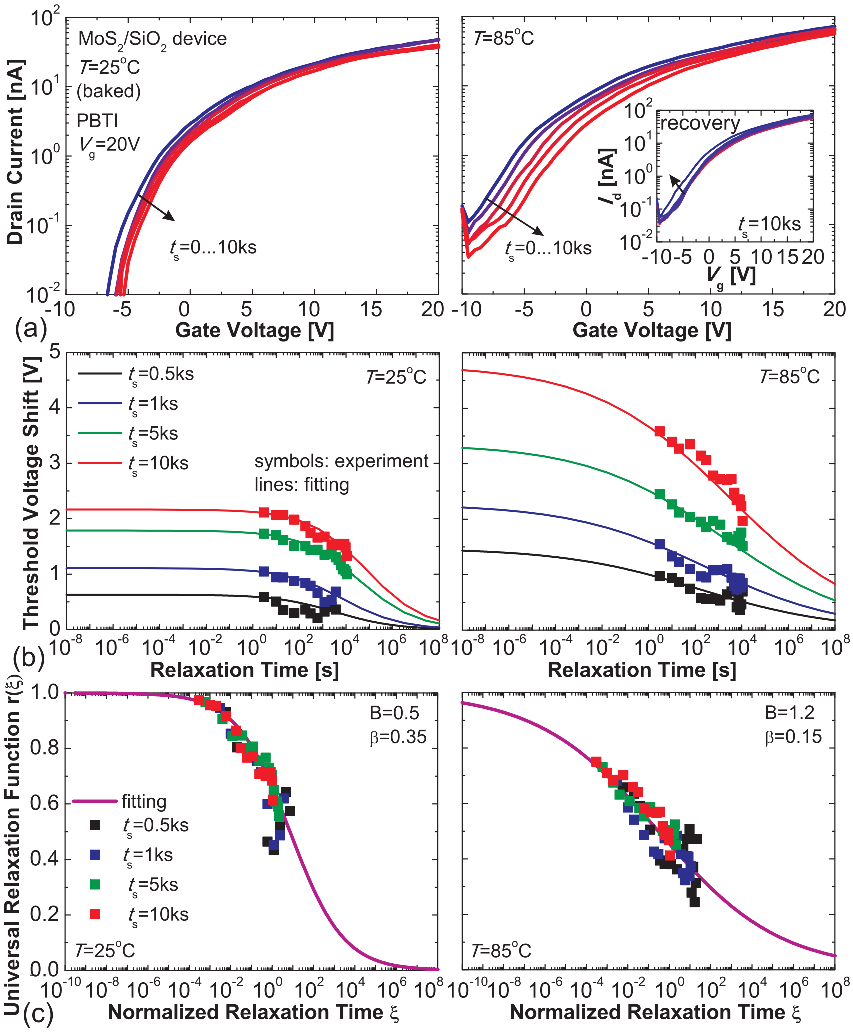


Figure 7.9: (a) Degradation of the gate transfer characteristics of the MoS$_2$/SiO$_2$ FET after subsequent PBTI stresses with $V_\mathrm{g} = 20\,\mathrm{V}$ and increasing t_s at $T = 25°\mathrm{C}$ (left) and $T = 85°\mathrm{C}$ (right). (b) The resulting ΔV_th recovery traces can be fitted using the universal relaxation model [61, 64]. (c) Normalized recovery traces follow a universal relaxation relation. Similarly to Si technologies, at higher T, degradation is stronger and the degree of recovery is larger. This agrees with our hysteresis measurements, which show that at higher T, traps become faster (Figures 7.4 and 7.7). The parameters B and β are very similar to those obtained from Si data (Figure 7.13), which confirms the similarity in the underlying physical degradation processes.

7.5 Analysis of Bias-Temperature Instabilities

Another degradation mechanism which has been reported for MoS$_2$ FETs [26, 139, 193] is associated with bias-temperature instabilities known from Si technologies. Hence, we proceed with characterization of BTI for our MoS$_2$/SiO$_2$ and MoS$_2$/hBN FETs, which have shown the best hysteresis stability.

First we examine our MoS$_2$/SiO$_2$ FETs by applying subsequent PBTI stresses with stress time $t_\mathrm{s} = 10\,\mathrm{ks}$ and increasing V_g. The resulting evolution of the I_d-V_g characterestics is shown in Figure 7.8(left). Clearly, the degradation is recoverable, while being more pronounced for larger V_g. Contrary to GFETs and similarly to Si technologies, the BTI degradation/recovery dynamics

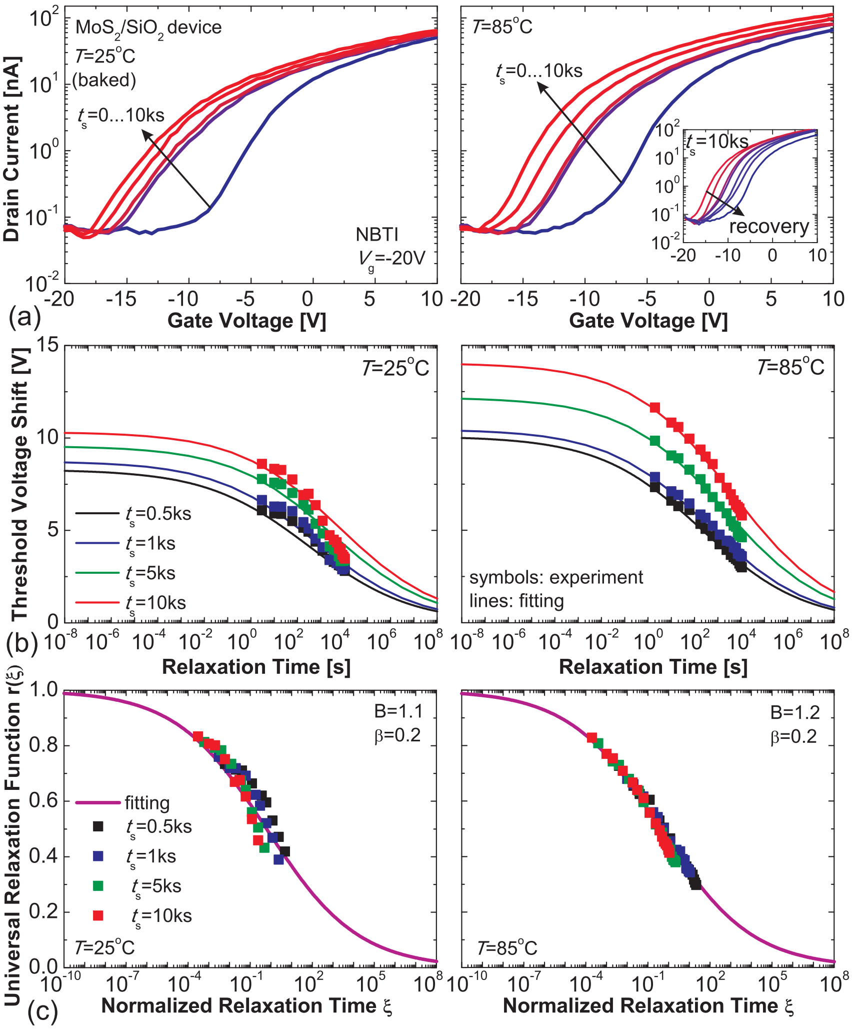


Figure 7.10: (a) Degradation of the gate transfer characteristics of the MoS$_2$/SiO$_2$ FET after subsequent NBTI stresses with $V_\mathrm{g} = -20\,\mathrm{V}$ and increasing t_s at $T = 25°\mathrm{C}$ (left) and $T = 85°\mathrm{C}$ (right). The observed threshold voltage shifts are significantly larger than for PBTI, while the recovery is also stronger. This is most likely associated with the difference in the energy levels of the defects involved in the underlying charge trapping processes. (b) Similarly to Figure 7.9, the recovery traces for ΔV_th can be reasonably fitted using the universal relaxation model. The temperature dependence of the degradation/recovery dynamics is similar to the case of PBTI. Namely, larger shifts and stronger recovery are observed at higher T, which is also the case for Si technologies. (c) The normalized recovery again follows the universal relaxation relation.

can be expressed using the threshold voltage shift ΔV_th versus the relaxation time t_r traces (Figure 7.8(right)). Their analysis shows that the relative ΔV_th remaining after $t_\mathrm{r} = 10\,\mathrm{ks}$ decreases from 85 % of the initially measured ΔV_th for $V_\mathrm{g} = 5\,\mathrm{V}$ toward 60 % for stronger stresses, i.e. for larger V_g the degradation is stronger and more recoverable. This is similar to Si technologies.

We proceed with an analysis of the degradation/recovery dynamics in MoS$_2$/SiO$_2$ FETs at different temperatures. Figure 7.9 shows the results obtained using subsequent PBTI stress/recovery cycles with increasing t_s. In order to compare the BTI degradation/recovery dynamics with Si technologies, we use the universal relaxation model [61, 64]. All recovery traces for our MoS$_2$/SiO$_2$ devices can be reasonably fitted (Figure 7.9b), since the normalized recovery is

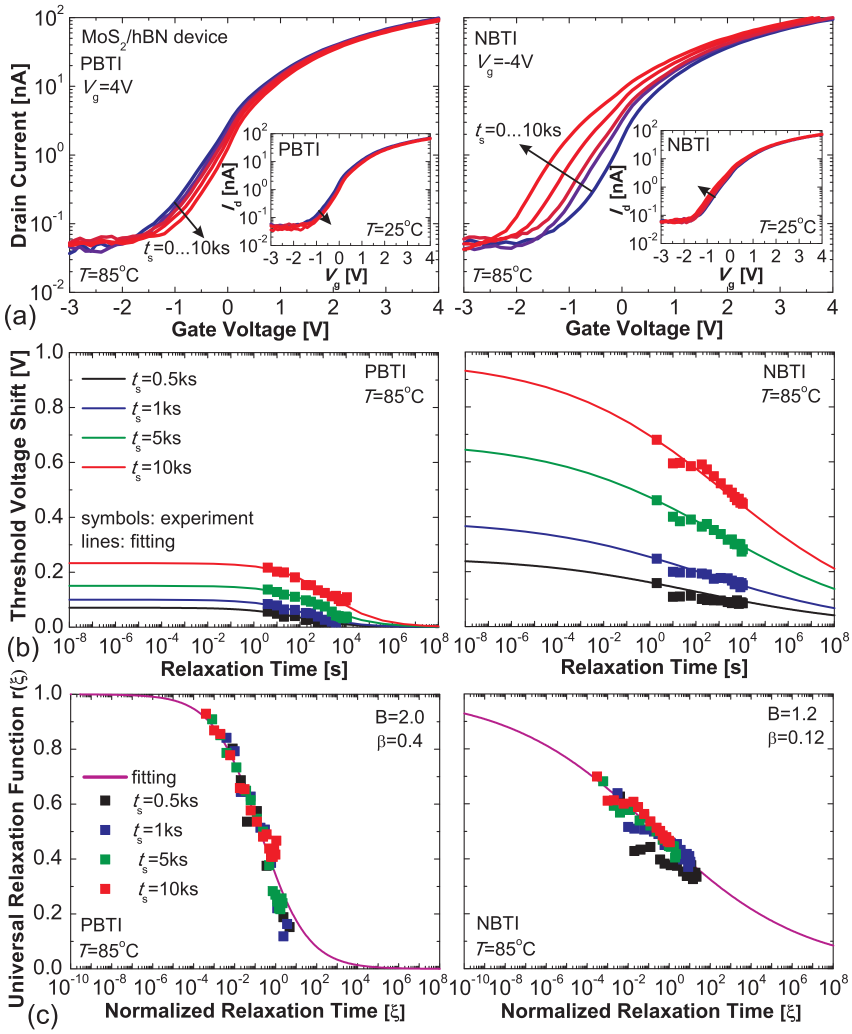


Figure 7.11: (a) Degradation of the gate transfer characteristics of the MoS_2/hBN FET after subsequent PBTI (left) and NBTI (right) stresses at $T = 85°C$. The insets show that the degradation observed after both PBTI and NBTI at $T = 25°C$ is significantly smaller. (b) The ΔV_{th} recovery traces at $T = 85°C$ can again be well fitted using the universal relaxation model as the normalized recovery is universal (c). Similarly to MoS_2/SiO_2 devices, the threshold voltage shifts are larger for NBTI than for PBTI and more recoverable. Also, the significant increase in the drifts of the MoS_2/hBN devices at higher T agrees with the increased hysteresis (Figure 7.6).

universal (Figure 7.9c). Just like in Si technologies, stronger degradation and faster recovery are observed at higher T, which is due to the thermally activated nature of carrier trapping [57]. However, MoS_2 FETs are known to exhibit both PBTI and NBTI on the same device [26, 193]. The related results for NBTI in MoS_2/SiO_2 FETs are provided in Figure 7.10. While V_{th} is shifted in the opposite direction, the observed shifts are larger than for PBTI. This is likely due to a difference in the energy levels of the involved traps. Nevertheless, the recovery traces can be well fitted by the universal relaxation model, which confirms a similarity of the two phenomena. Moreover, the temperature dependence of NBTI degradation is similar to PBTI. Namely, stronger shifts and faster recovery are observed at $T = 85°C$.

Next we repeat similar measurements for our MoS_2/hBN FETs. The results for PBTI and NBTI are shown in Figure 7.11. While these devices exhibit a negligible degradation at $T = 25°C$, at

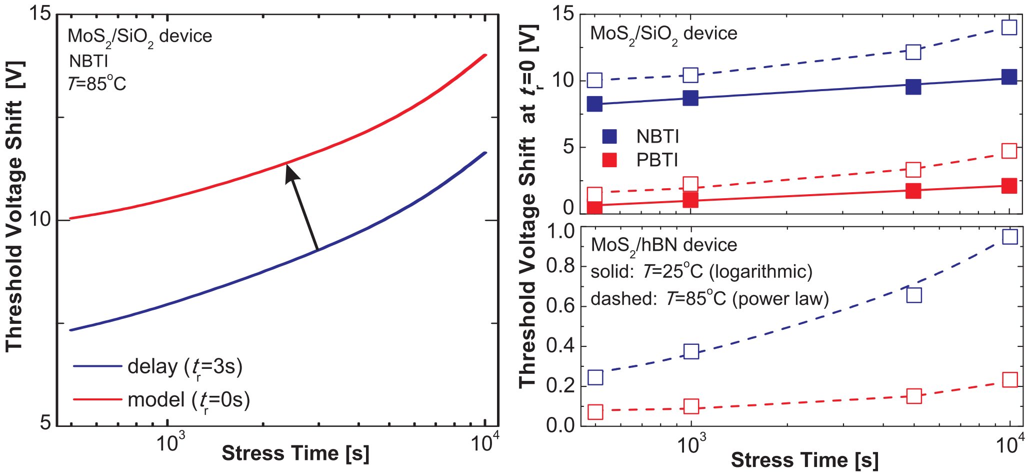


Figure 7.12: Left: Fitting of the recovery traces using the universal relaxation model allows us to estimate a recovery-free $\Delta V_{\text{th}}(t_{\text{r}} = 0)$, which is not experimentally accessible. Right: For both SiO_2 (top) and hBN (bottom) FETs the dependences of $\Delta V_{\text{th}}(t_{\text{r}}=0)$ versus t_{s} are logarithmic at $T = 25$°C and power law at 85°C. This again confirms the strong thermal activation of carrier trapping.

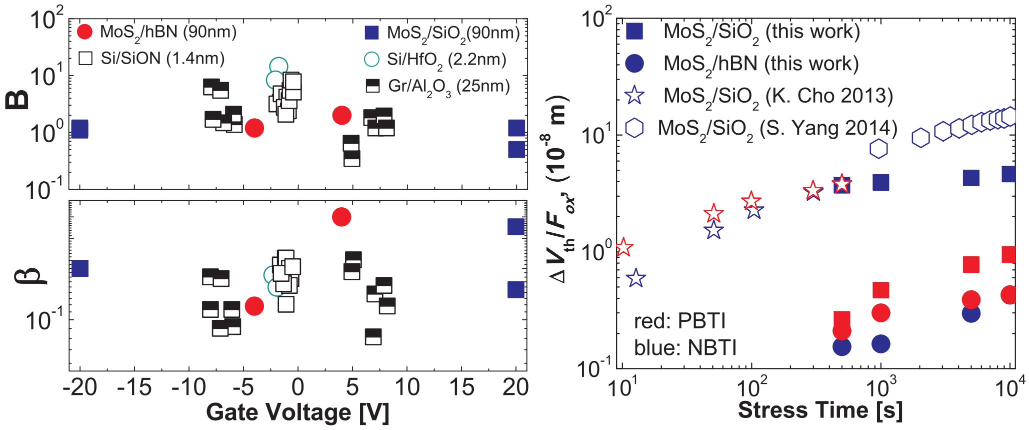


Figure 7.13: Left: The empirical parameters B and β, which have been used for fitting the recovery traces of our MoS_2/SiO_2 and MoS_2/hBN FETs, are very similar to those previously used for Si technologies and graphene FETs. This indicates a similarity in the physical processes related to BTI degradation/recovery dynamics. Right: Comparison of ΔV_{th} normalized by the oxide field F_{ox} for our devices against literature data [26, 193] at different t_{s}. While the NBTI shifts are comparable for our MoS_2/SiO_2 FETs, PBTI is significantly weaker in our devices. Finally, our MoS_2/hBN devices show superior reliability with respect to both PBTI and NBTI.

$T = 85$°C, both PBTI and NBTI shifts become more pronounced and agree with the universal model. Interestingly, NBTI in MoS_2/hBN devices is stronger than PBTI, which is similar to MoS_2/SiO_2 FETs. Also, use of the universal relaxation model allows us to extrapolate initial shifts $\Delta V_{\text{th}}(t_{\text{r}}=0)$ for both MoS_2/SiO_2 and MoS_2/hBN FETs. The results provided in Figure 7.12 show that $\Delta V_{\text{th}}(t_{\text{r}}=0)$ follow a $\log(t_{\text{s}})$ dependence at $T = 25$°C and exhibit a power law dependence at $T = 85$°C.[2] This further confirms that, similarly to Si technologies, carrier trapping in our MoS_2 FETs is thermally activated [57].

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[2] In the case of MoS_2/hBN FETs only the results for $T = 85$°C have been analyzed, since both PBTI and NBTI shifts at $T = 25$°C are negligible.

Hence, we have shown that both PBTI and NBTI recovery in our MoS_2 FETs can be reasonably described using the universal relaxation model. Moreover, in Figure 7.13(left) it is shown that the parameters B and β which have been used for fitting of the recovery traces of our MoS_2 FETs with SiO_2 and hBN are very similar to those previously used for Si technologies and GFETs. This indicates a similarity in the physical processes underlying the BTI dynamics. In Figure 7.13(right) we compare the normalized ΔV_{th} measured within this work with the results from [26, 193]. Clearly, our MoS_2/SiO_2 FETs show better stability with respect to PBTI stress, while the V_{th} shifts caused by NBTI are comparable to previous literature reports. At the same time, hBN devices exhibit superior BTI reliability. This is in agreement with our hysteresis results, showing that the amount of slow traps in MoS_2/hBN FETs is small and that the main reliability issue of these devices is associated with ultra-fast traps. It is also worth noting that, contrary to Si technologies, the degradation in these 2D FETs does not have a permanent component, likely due to the absence of dangling bonds at the interface.

7.6 Modeling of BTI Characteristics Using Minimos-NT

The results above show that the BTI dynamics in our MoS_2 FETs are very similar to those in Si technologies. Hence, at the next stage we attempted to perform more sophisticated simulations using the four-state NMP model coupled with the DD model. These simulations were done using our deterministic simulator Minimos-NT[83], which was first applied to describe carrier transport and trapping dynamics in the transistors with 2D channels.

In order to demonstrate the proof of concept, we have created a simulation template with the device geometry of our MoS_2/SiO_2 FET (Figure 7.1(left)) and a number of traps placed into the gate oxide. The real device dimensions and barrier parameters known from the literature (e.g. [150]) were implemented into the simulations. However, since Minimos-NT was originally developed for modeling of traditional Si MOSFETs, adjusting of this advanced simulator to the case of next-generation 2D technologies presents a complicated trick. Hence, in our first attempt, MoS_2 is treated as a conventional material with the thickness of several angstroms. Also, the density of states in the MoS_2 channel is described using the standard approach for conventional semiconductors rather than the one employed for 2D electron gas.

In Figure 7.14 we show the results simulated for stress and recovery dynamics of both NBTI and PBTI in MoS_2/SiO_2 FETs at two different temperatures. Despite several approximations having been done, our Minimos-NT simulations can reasonably reproduce the measured recovery traces and all related trends. In particular, an asymmetry between NBTI and PBTI as well as stronger degradation and faster recovery at higher temperatures fully agree with the four-state NMP model. Remarkably, the activation barriers of different transitions and other model parameters were the same for all four considered cases. Moreover, they are very similar to those previously used for modeling of NBTI in Si MOSFETs[152].

However, in the meantime a reasonable fitting of the experimental results is mostly possible for very long PBTI and NBTI stresses (all traces in Figure 7.14 correspond to $t_{\mathrm{s}} = 10\,\mathrm{ks}$). Nevertheless, in some particular cases we can properly reproduce the traces measured for different t_{s} using the same set of parameters. An example of the most successful results for NBTI at $T = 85°\mathrm{C}$ is shown in Figure 7.15. Again, the similarity of the model parameters to the case of Si technologies[152] allows us to conclude that the BTI dynamics in our MoS_2 FETs are similar to Si technologies. However, in our simulations for MoS_2 devices we consider only the recoverable component of BTI, while the permanent component is neglected. This is similar to the case of GFETs, and most likely associated with the absence of dangling bonds.

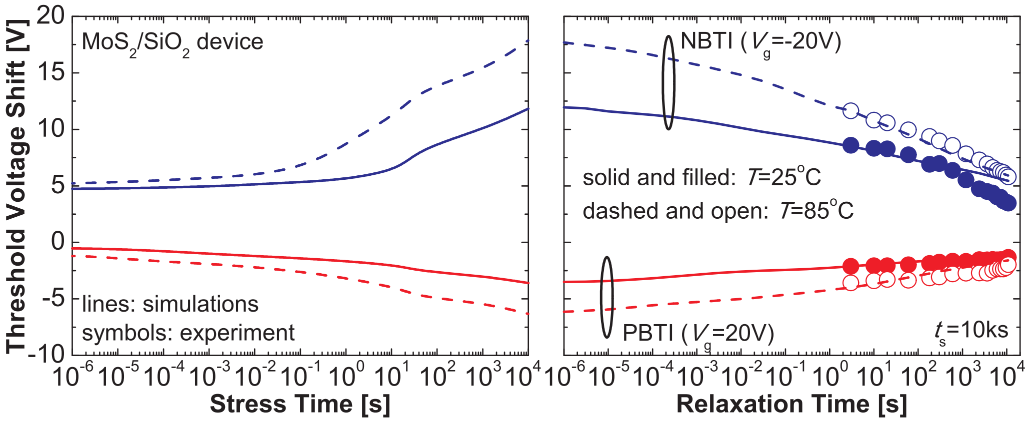

Figure 7.14: Left: The dynamics of PBTI and NBTI degradation in our MoS_2/SiO_2 FETs at $T = 25°C$ and $T = 85°C$ simulated using Minimos-NT. Right: The measured recovery traces can be reasonably fitted with simulation results. The same set of four-state NMP model parameters was used for all four cases corresponding to $t_s = 10\,ks$.

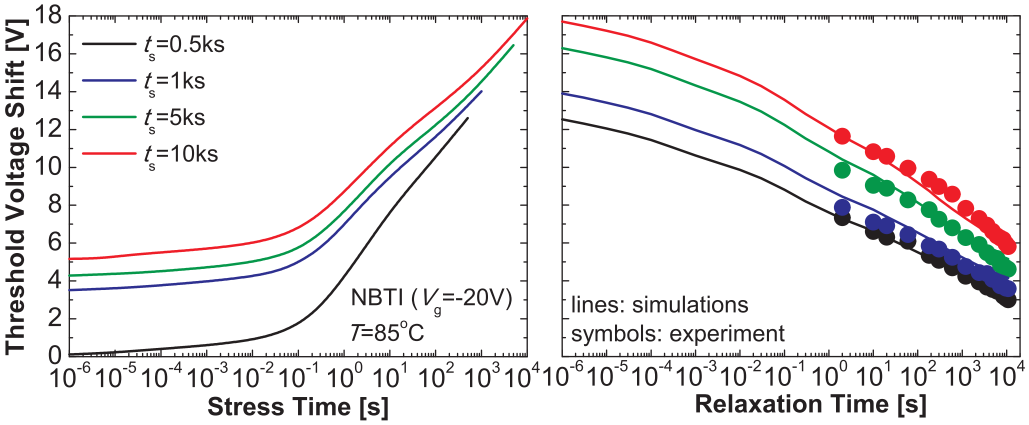

Figure 7.15: Left: The simulated dynamics of NBTI degradation in our MoS_2/SiO_2 FETs at $T = 85°C$ and four different stress times. Right: The recovery traces measured for different t_s can be reasonably fitted with the simulation results obtained using the same set of the four-state NMP model parameters.

Although some reasonable results on modeling of BTI in MoS_2 FETs have already been obtained, this simulation technique requires further adjustment. Nevertheless, demonstration of the proof of concept for these simulations, which were done for the first time in the course of this work, is extremely valuable.

7.7 Chapter Conclusions

In the course of this chapter we have demonstrated that our MoS_2 FETs with SiO_2 and hBN exhibit a smaller hysteresis and better BTI stability than similar devices reported by other groups. Moreover, hBN as a gate insulator reduces the impact of slow traps and improves BTI reliability. While the main reliability issue in MoS_2/hBN FETs is associated with ultra-fast traps, we have shown that at higher T the BTI reliability of hBN is reduced due to thermally activated charge trapping. Also, we have demonstrated that the BTI recovery traces measured for all our MoS_2 FETs follow the universal relaxation relation previously developed for Si technologies. Finally, we presented a proof of concept for the modeling of BTI characteristics of our MoS_2/SiO_2 FETs with Minimos-NT. Although this work requires further efforts, some reasonable results were obtained with the four-state NMP model parameters similar to those previously used for Si MOSFETs. Together with the results for GFETs described in the previous chapter, this underlines that the BTI degradation/recovery dynamics in next-generation 2D FETs are similar to their counterparts in Si technologies. However, no proof of the impact of the permanent component of BTI has been found for 2D devices so far, most likely because of the absence of dangling bonds.

8 Conclusions and Outlook

In the course of this work we have considered the most important reliability aspects in modern nanoscale Si MOSFETs and new transistors with graphene and MoS_2 channels. While in the former case scaling of device dimensions leads to a significant impact of individual defects on device performance, in the latter case one has to deal with a continuous number of charged defects. Below the main results of this work are summarized.

- The impact of individual defects on the performance of nanoscale Si MOSFETs in the presence of random dopants was studied in detail. The results of our TCAD simulations showed that the impact of a single charged trap on the threshold voltage shift versus drain bias dependence is strongly correlated with the lateral position of this trap. Based on this, a precise algorithm allowing us to evaluate the lateral trap position directly from TDDS data was developed. While our technique fully accounts for the impact of random dopants, the uncertainty of the lateral trap position evaluation does not exceed several percents of the channel length. Moreover, the accuracy was shown to increase for devices with smaller channel lengths.
- A detailed study of PBTI and NBTI in GFETs was first performed. It was shown that the BTI dynamics in GFETs can be reasonably fitted with the CET map model and universal relaxation model known from Si technologies. This allowed us to conclude that the mechanisms of BTI degradation and recovery in GFETs and Si MOSFETs are similar. However, no permanent component of BTI was found for GFETs, likely due to the absence of dangling bonds.
- The presence of HCD was first reported for GFETs. Contrary to Si technologies, HCD in GFETs was found to be recoverable and more similar to BTI. For some stress conditions, this allowed us to capture the dynamics of HCD in GFETs with the CET map and universal relaxation models.
- The mechanisms of HCD in GFETs were classified with respect to the polarities of bias and hot carrier stress components. A detailed experimental analysis of all HCD issues was performed, while qualitative simulations using the DD model adjusted for GFETs allowed for an interpretation of the results. In particular, it was found that PBTI and HCD stress components acting in conjuction lead to a non-trivial recovery of the degradation accompained with thermally activated mobility increase. Moreover, variations of the charged trap density and mobility resulting from HCD are correlated, while being consistent with previously reported attractive/repulsive scattering asymmetry.
- The first detailed characterization of hysteresis and BTI was performed for MoS_2 FETs with SiO_2 and hBN insulators. It was shown that the devices studied within this work exhibit better reliability compared to their previously reported counterparts. Namely, the hysteresis and BTI shifts in our MoS_2 devices are smaller. Furthermore, use of hBN as a gate insulator improves the device reliability at room temperature, although it considerably decays at higher temperatures.
- The first attempt to reproduce the BTI degradation dynamics in MoS_2 FETs with SiO_2

using the four-state NMP model coupled with the DD model was performed. The demonstrated proof of concept opens wide possibilities for modeling of reliability characteristics of next-generation 2D FETs using the simulators developed for Si technologies.

The trap location technique developed in this work can be very useful in application by industrial specialists when conducting primary characterization of nanoscale Si MOSFETs. Moreover, this method is potentially suitable to be applied for characterization of future 2D FETs, when the dimensions of these devices become small enough. At the same time, the information about reliability of the devices with graphene and $\mathrm{MoS_2}$ obtained in this dissertation can be very useful for the understanding of future trends in 2D technologies. Moreover, the described experimental and simulation approaches can be applied to capture the reliability of the transistors with other 2D materials, such as phosphorene, silicene and germanene, which will be studied in the near future. Especially important is that the reliability characteristics of 2D FETs can be predicted using the models previously developed for Si technologies. This allows us to adjust the conventional Si device simulators, in particular those developed at our institute, to the case of 2D devices. Hence, one of the main directions for future research on 2D materials can be a more accurate adjustment of the four-state NMP and DD models for transistors with various 2D materials from the “beyond graphene” range. Another important step could be realization and a detailed reliability study of top-gated FETs with $\mathrm{MoS_2}$, phosphorene and other 2D channels. Also, attention needs to be paid to devices with 2D insulators, such as hBN. Advanced modeling of their reliability coupled with experimental analysis would present a very interesting research topic.

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Own Publications

Publications Related to this Dissertation

[1] Y. Illarionov, M. Waltl, A. Smith, S. Vaziri, M. Ostling, M. Lemme, and T. Grasser. Bias-Temperature Instability on the Back Gate of Single-Layer Double-Gated Graphene Field-Effect Transistors. *Japanese Journal of Applied Physics*, 2016. accepted.

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[6] Y. Illarionov, M. Waltl, A. Smith, S. Vaziri, M. Ostling, M. Lemme, and T. Grasser. Interplay between Hot Carrier and Bias Stress Components in Single-Layer Double-Gated Graphene Field-Effect Transistors. In *Proceedings of 45th European Solid-State Device Research Conference (ESSDERC)*, pages 172–175, 2015.

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Other Publications

[1] Y. Illarionov. *Tunnel Carrier Transport and Related Physical Phenomena in Gold - Calcium Fluoride - Silicon (111) Structures.* Dissertation, Ioffe Physical-Technical Institute, 2015. in Russian.

[2] Y. Illarionov, M. Vexler, V. Fedorov, S. Suturin, N. Sokolov, and T. Grasser. Characterization of Epitaxial Calcium Fluoride as a Dielectric Material for Ultra-Thin Barrier Layers in Silicon Microelectronics. In *Extended Abstracts of the 2015 International Conference on Solid State Devices and Materials(SSDM)*, pages 330–331, 2015.

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Curriculum Vitae

Personal Information

Name	Yury Illarionov
05 June 1988	Born in Leningrad (now St-Petersburg), Russia
Nationality	Russian
Languages	Russian (Mother Tongue) English (Advanced) French (Basic) German (Beginner)

Education

1995 – 2005	School Education (Gymnasium 107, Lyceum 597), St-Petersburg, Russia
June 2005	Finished with Honors ("Gold Medal" Award)
2005 – 2011	St-Petersburg State Polytechnical University, Faculty of Physics and Technology, Department of Solid State Physics
June 2009	Received B.Sc. Degree in Engineering and Technology (with Honors)
June 2011	Received M.Sc. Degree in Engineering and Technology (with Honors)
2010 – 2012	Erasmus Mundus FAME Master Program (Awarded with a Scholarship by the EC) Grenoble INP, France University of Augsburg, Germany
October 2012	Received Double European M.Sc. Degree in Advanced Material Science
2011 – 2015	Ioffe Physical-Technical Institute, Division of Solid-State Electronics
January 2015	Recieved Ph.D Degree in Semiconductor Physics
July 2015	Degree Approved by the Higher Attestation Commission
February 2013	Enrolled at TU Wien as a Ph.D Student

Work Experience

2007 – present	Ioffe Physical-Technical Institute (Russia)
October 2007	Part-time Bachelor Student (not employed)
October 2009	Laboratory Assistant
November 2011	Senior Laboratory Assistant
February 2015	Junior Researcher
May–July 2011	CNRS IRCELYON (France) Summer Internship
February–July 2012	Singapore Institute of Manufacturing Technology (Singapore) Diploma Internship
February 2013 – present	Institute for Microelectronics (TU Wien, Austria), Reliability Group (Headed by Prof. Tibor Grasser)