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Transport in ultra-scaled Ge quantum dots embedded in Al-Ge-Al nanowire heterostructures

PhD thesis by
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Abstract

Metal-semiconductor-metal heterostructures are attractive for both fundamental studies of low-dimensional nanostructures as well as for future high-performance low power dissipating nanoelectronic and quantum devices. Most notably, they bear enormous potential for a vast array of key components for quantum computing such as SQUIDs, oscillators, mixers and amplifiers. In this context, combining high carrier mobilities and leveraging strong quantum confinement effects due to a more than five times larger exciton Bohr radius compared to Si, Ge occupies an exceptional position for the development of novel quantum devices in the post Si era. Within this thesis, it is shown that utilizing a thermally induced exchange reaction between single-crystalline Ge nanowires and Al pads, monolithic Al-Ge-Al nanowire heterostructures with ultra-small Ge segments contacted by self-aligned, quasi-1D, crystalline Al leads can be fabricated without lithographic constraints. High-resolution transmission electron microscopy and energy dispersive X-ray spectroscopy proved the composition and perfect crystallinity of the entire nanowire heterostructure. Integrating such Al-Ge-Al nanowire heterostructures as active channels in electrostatically gated field-effect transistor devices, provides a platform for the systematic investigation of electrical transport mechanisms in ultra-scaled Ge nanowires. In contrast to common short channel devices, the 1D monolithic metal-semiconductor-metal architecture effectively prevents the screening of the gate electric field by lithographically defined contacts and thus enables perfect electrostatic control of ultra-scaled Ge channels. Based on these structures, ballistic transport as well as quantum ballistic transport phenomena were systematically investigated depending on the Ge channel length and nanowire diameter. Resistivity and gate-dependent conductance measurements as well as detailed bias spectroscopy studies in the temperature range between 5 K and 300 K revealed a current transport through spin-degenerate 1D sub-bands in ultra-scaled Ge channels up to room temperature. The second part of the thesis is dedicated to the transport effects in the temperature range from 10 K to 2 K, where a small Ge channel reveals the characteristic of a single hole-transistor. Systematic investigations of single-hole tunnelling through Ge quantum dots revealed a complex charge trapping related multi-dot system near the pinch-off gate-voltage that evolves into a single-dot regime. The third set of experiments investigated the temperature regime from 1.5 K to 400 mK, where an ultra-scaled Ge channel coupled to superconducting Al leads, reassembles a Josephson field-effect transistor. The experimental proof of exchanging Cooper pairs between the superconducting Al leads and a gate-tunable Ge channel, mediated by the superconducting proximity effect enabled the first demonstration of superconductivity induced in a pure Ge channel. Gate-dependent transport measurements revealed a tunable critical supercurrent in the Ge quantum dot from zero to approximately 20 nA.

Kurzfassung

Metall-Halbleiter-Metall Heterostrukturen sind für grundlegende Untersuchungen von niedrigdimensionalen Nanostrukturen und der Erforschung zukünftiger hochleistungsfähiger Nanoelektronik- und Quantenbauelemente attraktiv. Insbesondere bieten sie ein enormes Potenzial für eine Vielzahl von Schlüsselkomponenten von Quantencomputern wie beispielsweise SQUIDs, Oszillatoren, Mischern und Verstärkern. In diesem Zusammenhang nimmt Ge, durch die Kombination hoher Ladungsträgermobilitäten und ausgeprägterer Quanten-Confinement-Effekte, eine Sonderstellung für die Entwicklung neuartiger Quantenbauteile in der Post-Si-Ära ein. In der vorliegenden Arbeit wird gezeigt, dass unter Verwendung einer thermisch induzierten Austauschreaktion zwischen einkristallinen Ge-Nanodrähten und Al-Kontakten, Al-Ge-Al Nanodraht-Heterostrukturen mit ultra-kurzen Ge-Segmenten und kristallinen quasi-1D Al-Zuleitungen, ohne lithografische Einschränkungen, hergestellt werden können. Hochauflösende Transmissionselektronenmikroskopie und energiedispersive Röntgenspektroskopie belegten dabei die perfekte Kristallinität aller Komponenten der Nanodraht-Heterostruktur. Durch die Integration ultrakurzer Ge Segmente als aktive Kanäle in elektrostatisch gesteuerten Feldeffekttransistoren wurde eine Plattform für die systematische Untersuchung elektrischer Transportmechanismen in ultra-skalierten Ge-Nanodrähten geschaffen. Im Gegensatz zu herkömmlichen Kurzkanalbauelementen verhindert die quasi-1D Metall-Halbleiter-Metall Architektur eine Abschirmung des elektrischen Feldes der Gate-Elektrode durch die Anschlusskontakte und ermöglicht somit eine perfekte elektrostatische Steuerung von ultra-skalierten Ge-Kanälen. Basierend auf diesen Strukturen wurden ballistische und quantenballistische Transportphänomene in Abhängigkeit der Kanallänge und dem Nanodrahtdurchmesser untersucht. Temperaturabhängige Messungen des spezifischen Widerstands und Gate-abhängige Leitfähigkeitsmessungen im Bereich zwischen 5 K und 300 K, haben einen quantisierten Stromtransport durch einzelne quasi-1D Subbänder nachgewiesen. Darüber hinaus, wurden die Transporteffekte im Temperaturbereich von 10 K bis 2 K untersucht. Hier war es möglich zu zeigen, dass ein kurzer Ge-Kanal die Charakteristik eines Single-Hole Transistors aufweist. Systematische Untersuchungen des Tunnelns einzelner Löcher ergaben ein Multi-Quantum-Dot System innerhalb des Ge-Segments, welches sich über die Gate-Spannung in ein Single-Quantum-Dot System überführen ließ. Des Weiteren, wurde das Temperaturregime von 1.5 K bis 400 mK untersucht, in dem ein ultra-skalierter Ge-Kanal, der an supraleitende Al-Zuleitungen gekoppelt ist, einem Josephson-Feldeffekttransistor entspricht. Hier konnte der experimentelle Nachweis für den Austauschs von Cooper-Paaren zwischen den supraleitenden Al-Kontakten durch den Gate-kontrollierbaren Ge-Kanal basierend auf dem supraleitenden Proximity-Effekt erbracht werden. Die Transportmessungen ergaben dabei einen einstellbaren kritischen Superstrom im Ge-Quantenpunkt bis zu ca. 20 nA.

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Contents

Chapter 1

Introduction

Over the last decades, following Moore's law,[1] the continuous down-scaling of the Si based, planar integrated circuit technology has been the main driving force to reduce size, power consumption and cost of modern microelectronic devices. The most recent evolution steps of scaling the minimum feature size of the Si based transistor technology are shown in figure 1.1.

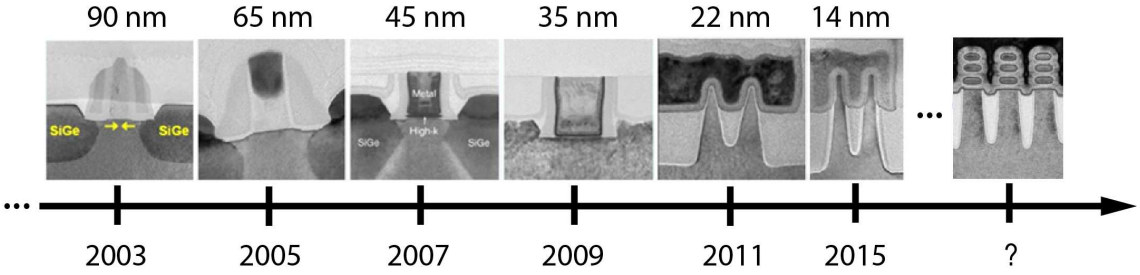

Figure 1.1: *Timeline of the recent evolution steps of the Si based transistor technology. Images adapted from the Intel development roadmap 2015.*

The timeline reveals that the down-scaling of the minimum feature size required the implementation of new materials such as SiGe to enhance carrier mobilities (2003) or high-κ dielectrics to decrease the gate leakage (2007). Most notably, scaling beyond the 35 nm node required a radical change in the device architecture towards a 3D tri-gate design (2011). Although it was possible to reach the 14 nm technology node

in 2015, physical limits and the dramatic repercussions of short-channel effects[2] forced a shift of research efforts towards the integration of new materials and device architectures.[3]

Thus, substantial research interest has been triggered to manipulate matter on the nanometer scale to tune material properties beyond those of their bulk counterparts. However, according to the relatively high effective masses that limit the application of single-electron tunneling and quantum ballistic transport in group IV based devices to ultra-small structural sizes or ultra-low temperatures, III-V semiconductors[4–6] have been extensively studied.

Most notably, all materials foreseen to displace Si, exhibit much larger exciton Bohr radii (a_B^*) and significantly longer scattering mean free paths and thus feature quantum confinement effects at much larger structural sizes compared to Si. Accordingly, a shift from diffusive to quantum ballistic transport and single-electron tunneling will pave the way for novel nanoelectronic devices with superb performance and efficiency providing a platform for the implementation of complex functionality with a minimum number of multi-valued logic gates and ultra-fast solid-state drives.[7, 8]

Further, the pronounced structural surface roughness in top-down architectures, motivated the development of bottom-up fabricated nanostructures, which emerged as a promising platform to overcome the limitations of conventional planar architectures. Consequently, considerable effort has been devoted on bottom-up fabricated low dimensional nanostructures such as single-walled carbon nanotubes (SWCNTs)[9] and vapor-liquid-solid (VLS) grown nanowires (NWs).[10, 11] Although SWNT based quantum devices[12–15] have revealed themselves as promising platform for the investigation of novel transport phenomena, problems with respect to purity, uniformity and the fabrication of reliable contacts are the main limiting factors toward wafer-scale integration.[9, 16] Further, the electrical characteristic of SWCNTs is mainly determined by the diameter and by chirality. This requires a time-consuming process of selecting particular nanotubes prior to device fabrication.[9] In contrast, there is no need for a distinction between metallic or semiconducting NWs, because their properties are determined by the material they are consisting of. One of the most significant advantages of NWs is the ability to customize their morphology, geometry, composition, crystal orientation and size by tuning the growth conditions. Further, a large variety of semiconductor materials, such as e.g. Si, Ge, GaAs, GaN

and InAs are available for NW growth.[17] Moreover, the combination of a quasi-1D structure, enabling electrical transport through discrete sub-bands and significant advantages with respect to contacting compared to quantum dots, make NWs attractive for both fundamental studies of low-dimensional as well as key components for future ultra-scaled hybrid nanoelectronics and quantum devices.[18–21] Especially, the ability to synthesize heterostructures of dissimilar materials with unique structure-property relationships and interactions originating from the contributions of individual low-dimensional components may give rise to unique electronic or photonic characteristics outclassing or even unattainable those of planar geometries.[22] Providing large exciton Bohr radii and long scattering mean free paths of charge carriers, investigations of quantum ballistic transport in NWs are almost exclusively based on group III-V NWs.[23–26] Despite the vast body of pioneering experimental work on GeSi[27, 28] and Ge-Si core-shell structures,[19, 20] on single-hole tunneling and gate-tunable Josephson junctions, the investigation of ballistic and quantum ballistic transport in pure group-IV based nanostructures is still evasive. This is mainly associated to limitations of fabricating reliable contacts to ultra-scaled Ge nanostructures, which requires sophisticated nanofabrication techniques and precise lithography. Regarding this problematic, intense research on thermal diffusion of metals into Si and Ge NWs was carried out to form scilicide and germanide contacts, respectively.[29–33] In contrast to common short channel devices, applying these silicide/germanide-semiconductor based heterostructures, effectively prevents screening of the gate electric field by lithographically defined contacts and thus enables perfect electrostatic control of ultra-scaled channels.[34] Nevertheless, the resistivity of these quasi-metallic structures is still significantly higher compared to pure metals. Hence, material combinations with no intermetallic phase formation, such as Al-Ge system, enabling true metal-semiconductor heterostructures with abrupt interfaces received a considerable amount of attention.[35–37]

Motivated by the potential of ultra-scaled Ge NWs as ultra-scaled hybrid nanoelectronics, the scope of this thesis is the fabrication of axial Al-Ge-Al NW heterostructures comprising an ultra-small Ge channel contacted by self-aligned, quasi-1D, crystalline Al (c-Al) leads. The integration of such NW heterostructures as active channels in electrostatically gated field-effect transistor devices, served as a platform for a systematic investigation of electrical transport mechanisms in ultra-scaled Ge

NWs in the temperature range between 400 mK and 300 K.
Starting with the fundamental physico-chemical parameters of Al and Ge, general properties and applications of Ge NWs as well as thermally induced diffusion of Al in Ge NWs, chapter 2 provides a theoretical overview of the Al-Ge material system. Additionally, theoretical aspects of transport phenomena in ultra-scaled Ge quantum dots including quantum ballistic transport, Coulomb blockade and the Josephson field-effect are addressed.
Chapter 3, concerns the fabrication process for embedding Ge NWs in a back-gated FET architecture and the setups as well as the measurement procedures for conducting electrical measurements of Al-Ge-Al NW heterostructures at room-temperature as well as cryogenic temperatures.
Based on high-resolution transmission electron microscopy (HRTEM) and energy-dispersive X-ray (EDX) spectroscopy, chapter 4 discusses the morphological study of Al-Ge-Al NW heterostructures. The investigations proved the composition and perfect crystallinity of heterostructure devices with ultra-short Ge channels. The main part of the chapter focuses on transport measurements discussing the experimental observation of ballistic and quantum ballistic transport in the temperature range between 5 K and 300 K. Further, DC spectroscopy measurements conducted in the temperature range between 400 mK and 1.5 K revealed the ability to tune the Ge segment from a completely insulating regime, through a low conductive regime, that exhibits properties of a single-hole transistor, to a superconducting regime, resembling a Josephson field effect transistor with a maximum critical current of approximately 20 nA.
Finally, chapter 5 provides a summery of the thesis as well as an outlook for further investigations concerning transport measurements on ultra-scaled Ge transistors.

Chapter 2

Theory

The following chapter is divided in four sections. First, the fundamental physico-chemical parameters of Al and Ge are discussed. Next, the motivation, general properties and applications of NWs are addressed. Further, theoretical aspects of NW synthesis techniques with a special focus on the VLS growth are given. The third section provides a brief overview of different contact geometries to nanoscale semiconductors. Thereby, a special focus was set on the thermally induced diffusion of Al in Ge NWs to fabricate quasi-1D metallic leads to the Ge quantum dots. The last section discusses theoretical aspects of transport phenomena in ultra-scaled Ge quantum dots including quantum ballistic transport, Coulomb blockade and the Josephson field-effect.

2.1 Materials

2.1.1 Aluminum

Al is a metal, located in the 3rd group of the periodic table of elements. It has the atomic number 13 and a relative atomic mass of 26.98. The melting- and boiling points are 933 K and 2790 K, respectively. Al crystallizes in a face-centered cubic structure with a lattice constant of $a_{Al} = 0.405\,\text{nm}$. The crystallographic structure of Al is shown in figure 2.1. Although with 8.1 % Al is the most abundant metal in the earth's crust, pure Al is never found in nature, due to its high reactivity. It only occurs in compounds like feldspar, granite and bauxite core. Today, Al is mainly extracted from the ore bauxite via highly energy-consuming electrolysis, achieving Al of approximately 99.99 % purity.[38]

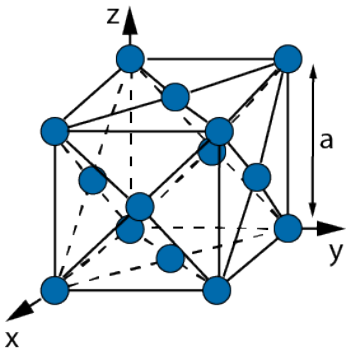

Figure 2.1: *Crystallographic structure of Al:*
Schematic illustration of the fcc Al cell. The lattice constant is indicated with a.

With a density of $2.7\,\text{g}\,\text{cm}^{-3}$ and an electrical conductivity of about $36\,\text{mS}\,\text{mm}^{-2}$, Al features an excellent combination of mechanical and electrical properties. Due to these favorable properties, Al is the second most widely used metallic material today.[39] Further, Al is an elementary type-I superconductor with a bulk transition temperature of $T_c = 1.19\,\text{K}$.[40] As Al forms a thin high-quality native oxide film in oxygen-containing atmospheres, it is routinely used for resonators and other superconducting quantum circuits.[21] For microelectronic devices, Al was mainly used as metalization and interconnect material in integrated circuits.[41] Although, Al rather than other interconnect metals like Au or Cu, is not causing deep traps

in Si or Ge, the high current densities of modern microelectronic devices lead to unacceptable electromigration in Al interconnects. Consequently, Al was replaced by Cu as preferred interconnect metal in 1997.[42] Further, with a work function of $q\phi_m = 4.1\,\text{eV}$, Al is used for electrodes and integrated transducers.[41]

2.1.2 Germanium

Ge is a semiconductor, located in the 4th group of the periodic table of elements. It has the atomic number 32 and a relative atomic mass of 72.64. The melting- and boiling points are 1211 K and 3107 K, respectively. Ge crystallizes in a diamond structure, that can be considered as two interpenetrating fcc lattices with a lattice constant of $a_{Ge} = 0.566\,\text{nm}$. In this structure, each atom is surrounded by four equidistant nearest neighbors, which lie in the corners of a tetrahedron.[38] The crystallographic structure of Ge is shown in figure 2.2(a). In nature, Ge occurs only in mineral compounds like argyrodite, germanite, zinc ors or coal. Ultra-high purity Ge where only one part in 10^{10} is an impurity, which is required for the semiconductor industry, is mainly produced by zone-refining techniques.[38]

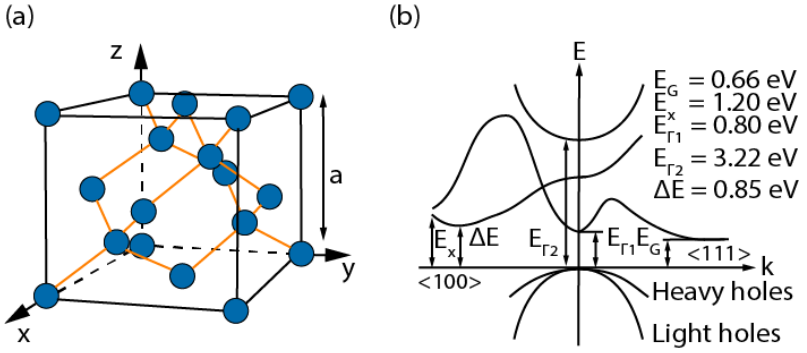

Figure 2.2: *Crystallographic structure and band diagram of Ge:*
(a) Schematic illustration of the diamond cell of Ge. The lattice constant is indicated with a. (b) Energy band diagram of Ge at a temperature of 300 K *showing an indirect band gap at the L-point minimum* $E_G = 0.66\,\text{eV}$ *and a direct band gap at the* Γ*-point* $E_\Gamma = 0.8\,\text{eV}$.

Figure 2.2(b) shows the band structure of Ge at a temperature of 300 K, indicating an indirect band gap at the L-point minimum $E_G = 0.66\,\text{eV}$ and a direct band gap at the Γ-point $E_\Gamma = 0.8\,\text{eV}$.[41] As the indirect band-gap is smaller than the direct one, Ge is referred to as indirect semiconductor. Consequently, incident photons can

only excite an electron over the band gap, for photon energies $E_{ph} = h\nu \geq E_G$. Accordingly, in indirect semiconductors, the momentum required to excite an electron from the valence band maximum in the Γ-point to the conduction band minimum in the L-valley is much larger than the momentum of the photon. Thus, the assistance of a phonon interaction is required. Such a multiple particle processes have a significantly lower probability compared to absorption in the direct semiconductor.[41] As Ge nearly is almost a direct band gap semiconductor, it was shown that alloying with Sn [43] or applying high uniaxial tensile strain in suspended Ge structures can be used to achieve Ge based lasers[44]. Moreover, compared to Si, Ge exhibits significantly higher carrier mobilities of electrons $\mu_n = 3800\,\mathrm{cm^2\,V^{-1}\,s}$ and holes $\mu_p = 1820\,\mathrm{cm^2\,V^{-1}\,s}$.[45] According to this advantageous properties, the first transistors, fabricated by Shockley Bardeen and Brattain, in 1947 were based on Ge.[46]
Despite all these numerous advantages, Ge played only a minor role in transistor technology in the past decades. Beside the higher fabrication cost, this is mainly attributed to the fact that Si, in contrast to Ge, forms a high-quality native oxide, which serves as a good insulator and naturally passivates dangling bonds on the semiconductor-oxide interface. A high quality oxide such as silicon oxide is highly preferable, because it is not soluble in water, stable at high temperatures, can be used as diffusion mask and forms a low defect density interface to silicon.[41] In contrast to Si, the surface properties of Ge are mainly determined by the quality of the oxide at the interface.[47, 48] Beside, Ge dioxide (GeO_2) and Ge monoxide (GeO), there two further oxide species present, namely Ge_2O_3 and Ge_2O. It was shown that the the electrical properties of the interface strongly dependent on the composition of those sub-oxides. Due to the higher quality of the GeO_2/Ge interface, the formation of GeO_2 is highly favorable to reduce surface trapping. However, as non of these oxide species remains stable at ambient conditions, a permanent change of oxide composition has significant influence on the electrical and optical properties of Ge.[49] However, with the introduction of high-κ dielectrics as gate-oxides in sub-45 nm technology nodes, the advantage of a high quality native oxide was no longer crucial and Ge became a potential semiconductor material for future high performance devices again.[50] Further, Ge features a a_B^* of 24.3 nm much larger compared to Si ($a_B^* = 4.9\,\mathrm{nm}$). This makes Ge especially attractive to study quantum confinement effects up to room temperature such as quantum ballistic transport.[51]

Regarding optoelectronic applications, the high absorption coefficient of Ge in the wavelength range between 800 nm and 1550 nm makes it a highly interesting candidate for IR photo detectors[52] as well as efficient IR absorbers for tandem solar cells.[53] Besides the usage in microelectronic and optoelectronic devices, Ge is also a common material for different optical systems such as infrared spectrometers and fiber optics. Further, Ge-oxides are used for the fabrication of wide angle camera lenses and microscope objectives due to a high index of reflection and dispersion.[38]

2.2 Nanowires

NWs are rod-like nanostructures with diameters below 100 nm that can exhibit aspect ratios far beyond 1:1000.[54] This inherently high surface to volume ratio causes the properties of NWs to be strongly dependent on by the surface area rather than the material itself. Hence, NWs provide a platform to study the influence of surface effects on electronic transport phenomena or optical effects.[55] Especially for very thin group-IV NWs and lower doping concentrations, acceptor-like traps reside on the interface and in the oxide, which cause the surface potential to be positive and the bands to bend upward. Although the NW is intrinsic or even moderately n-type doped, this effect is denoted surface doping and can result in a shift of the energy band structure throughout the whole cross section of the NW, causing a significant p-type behavior.[56–58] Further, a very important advantage of NWs is that a large variety of semiconductor materials, such as e.g. Si, Ge, GaAs, GaN and InAs are available for NW growth.[17] As these materials are exhibiting different electrical and optical properties, NWs not only have attracted intense research interest for future microelectronic devices such as ultra-scaled transistors,[11] but exhibit an enormous potential to be important building blocks of future photonic[59] plasmonic,[60] photovoltaic,[61] solar energy harvesting,[62] or sensor devices.[63] Recently, band-structure engineering by controlled epitaxial growth of core-shell NWs provoked the investigation of one-dimensional hole-gas systems.[64, 65] Further, as for very thin NWs, the momentum of an electron is confined in two dimensions and thus the movement of charge carriers is only possible in one dimension, they are often referred to as quasi-1D nanostructures. As a result, unique size dependent effects drastically change the electrical, chemical, and mechanical properties.[9] The possi-

bility to customize the morphology, geometry, composition or crystal orientation of NWs, combined with their enormous potential for future devices triggered intense research interest in the field of NW synthesis and led to the exploration of a large variety of different technologies such as electron beam lithography [66], laser ablation, [67] template,[68], VLS [10] and vapor-solid-solid (VSS) [69] based NW growth.[70] A SEM image showing a growth substrate with VLS grown Ge NWs is supplied in figure 2.3.

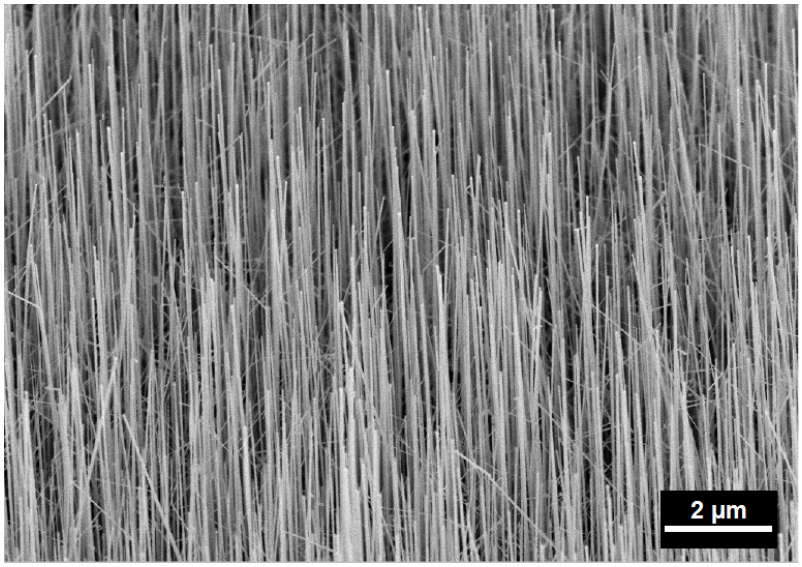

Figure 2.3: *SEM image of VLS grown Ge NWs:*
The shown NWs are approximately 7 µm *long and exhibit diameters between* 25 nm *and* 70 nm*. The image was recorded at a magnification of approximately 20.000x.*

2.2.1 Vapor-liquid-solid growth of Ge nanowires

Today, catalytic NW growth by the VLS mechanism is the most frequently used growth technique for the bottom-up fabrication of semiconductor NWs. Inspired by the pioneering work of R.S. Wagner and W.C. Ellis in the 1960s, [10] intense research archived a continuous improvement of this synthesis method allowed better insight into growth dynamics, kinetics and morphology control of VLS grown NWs.[71] The name VLS derives from the aggregate states the semiconductor material supplied by the precursor gas has to cycle before it is incorporated into the NW. A schematic illustration of the VLS growth mechanism is shown in figure 2.4. First, a thin metal

layer, mostly Au, is deposited on a Si wafer. The successive annealing of the wafer forces a dewetting of the Au layer and the formation of nano-droplets. These nano-droplets serve as catalytic seeds and define the diameter of the NWs. To initiate the NW growth, the substrate is heated above the eutectic temperature of the Au-Ge material system (539 K) and a gaseous precursor (GeH_4) is introduced. This triggers a process, starting with absorption of GeH_4 on the Au nano-droplet. At the vapor-liquid interface, a decomposition of the precursor into volatile H_2 and Ge takes place. Ge is diffusing through the AuGe liquid to reach the liquid solid interface between the nano-droplet and the Si substrate. Finally, supersaturation drives the incorporation of Ge forming a vertically growing solid quasi one-dimensional NW. The length of the NW is determined by the temperature, partial pressure and the process time.[17] In order to prevent kinking along the growth direction, it is mandatory to ensure stable conditions for pressure, temperature and gas concentration. The growth temperature further determines the morphology of the NW. While elevated temperatures result in a non-catalytic growth and consequently to an increased tapering of the NW, lower temperatures suppress non-catalytic growth, but also decrease the NW growth rate. Further, partial pressure of precursor gas is a very important parameter as it influences the nucleation rate and NW growth direction. Further, high pressures can result NW growth in random directions. In contrast, a low pressure results in short and sparse NW growth.[72]

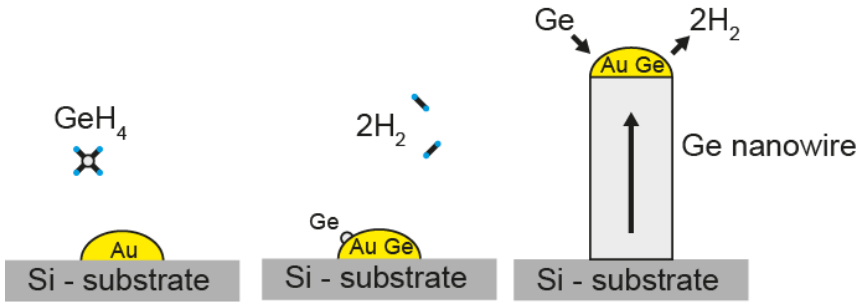

Figure 2.4: *VLS growth mechanism for the synthesis of Ge NWs:*
(left) Formation of the catalytic Au nano-droplet after annealing of the Au film. Subsequently the precursor gas GeH_4 is introduced, (middle) Adsorption and decomposition of the GeH_4 precursor at the vapor-liquid interface of the nano-droplet, (right) Incorporation of Ge at the liquid-solid interface of the nano-droplet and supersaturation driven vertical NW growth.

2.3 The Al-Ge material system

2.3.1 Physico-chemical properties of the Al-Ge system

In terms of classification, Al is a trivalent and Ge is a tetravalent element. There is no stable stoichiometric compound of Al and Ge.
The binary phase-diagram of the Al-Ge material system, shown in figure 2.5, reveals a melting point of Al and Ge at 933 K and 1211 K respectively.[73] The eutectic point of the material system can be found for a Ge composition of 29.5 % with a solid liquid transition at 693 K. As below the eutectic temperature the solubility of Ge in Al is very low, only about 2 % of Ge can be incorporated into Al. The solubility of Al in Ge is with even less than 1 %. Thus, the formation of only local crystallites is much more likely compared to intermetallic phases.[73]

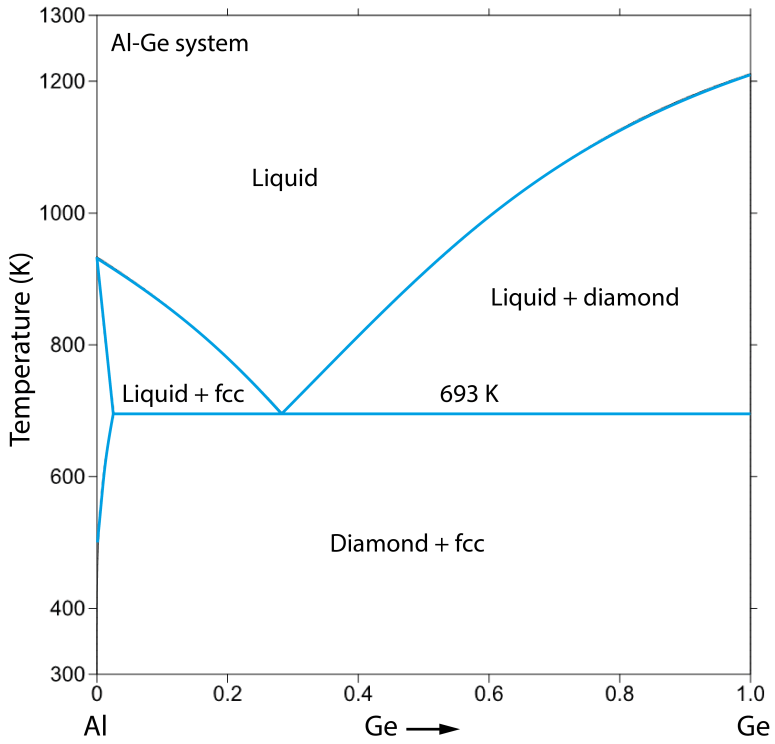

Figure 2.5: *Phase diagram of the Al-Ge material system.*
The eutectic point of the material system reveals a solid liquid transition at 693 K *for a Ge composition of* 29.5 %*. Image based on [73].*

Further, table 2.1 shows the diffusion coefficients of the Al-Ge material system for a temperature of 623 K. As can be seen, the listed values show an pronounced asymmetric behavior. The self-diffusion of Al and the diffusion of Ge in Al are orders of magnitude higher compared to the self-diffusion of Ge and the diffusion of Al in Ge.

Material	**Al** ($cm^2\,s^{-1}$)	**Ge** ($cm^2\,s^{-1}$)
Al	6.0 x 10^{-12}	1.3 x 10^{-25}
Ge	3.2 x 10^{-11}	9.9 x 10^{-25}

Table 2.1: *Diffusion coefficients of the Al-Ge material system: The Diffusion coefficients are shown for a temperature of* 623 K.*[74]*

2.3.2 Al diffusion in Ge nanowires

Diffusion is a fundamental process in solid-state physics. The origin of diffusion is the irregular movement of atoms, denoted as Brownian motion.[75]
This behavior is e.g. relevant for the kinetics of microstructural changes occurring during material processing, such as nucleation of new phases, diffusive phase transformations, recrystallization and thermal oxidation. As diffusion and electrical conduction phenomena in ionic conductors are closely related, technological applications of diffusion processes include e.g. solid electrolytes for batteries and fuel cells, surface hardening of steel through carburisation or nitridation, diffusion bonding, or sintering.[75]
In microelectronics, the fabrication of integrated interconnects is a crucial step towards the integration of reliable future ultra-scaled devices and requires sophisticated nanostructure formation techniques and precise lithography. Regarding this problematic, intense research on thermal diffusion of metals into Si and Ge NWs was carried out to form scilicide and germanide contacts, respectively.[29–33] However, the resistivity of these quasi-metallic structures is still significantly higher compared to pure metals. Hence, material combinations with no intermetallic phase formation, such as the Al-Ge system, enabling true metal-semiconductor heterostructures with abrupt interfaces received a considerable amount of attention.[35–37]
Using Joule heating, the diffusion of Al in Ge NWs was studied in-situ using TEM. This was achieved by both passing a current through a buried heating spiral be-

neath a Si_3N_4 membrane as well as localized Joule heating of an Al contact to a Ge NW.[36] For the following investigations, Ge NWs were contacted by Al pads. Upon heating with temperatures in the range between 250 K and 603 K, the strong asymmetry of the diffusion behavior in the Al-Ge material system (see table 2.1), a formation of an c-Al-Ge heterostructure can be initiated. The following diffusion mechanism was proposed [36]:
As shown in figure 2.6, Ge is diffusing out of the overlapping part and is replaced by Al. The black and green arrows indicate the replacement of Ge by Al from the contact pad. Further annealing results in the formation of a diffusion front gradually progressing along the quasi-1D NW resulting in an c-Al-Ge heterostructure (figure 2.6(b)). Using a 3D chemical reconstruction model based on EDX the chemical composition of the cross-section of the reacted part of the NW was generated.[36, 76] The analysis revealed the formation of a core-shell structure after the exchange of Al by Ge. A pure c-Al core is encapsulated by two Ge containing shells and a further Al_2O_3-shell. The first shell consists of pure Ge and is approximately 2 nm thick. It was demonstrated that the Al propagation in the Ge NW is governed by the Al self-diffusion through the created Al segment as Ge diffuses through a surface channel to the Al reservoir (see figure 2.6(c)). The second shell is only 1 nm thin and consists of a mixture of Ge and Al_2O_3. The whole structure is encapsulated by a 3 nm thick Al_2O_3-shell. A schematic of the entire core-shell structure is shown in figure 2.6(d). This cross-section was obtained at the location of the dashed black rectangle seen in figure 2.6(c). Remarkably, detailed EDX measurements neither showed Al contamination in the unreacted Ge NW nor Ge contamination in the core of the reacted part of the NW. In the investigated temperature range between 523 K and 603 K a parabolic growth behavior was found:

$$L_{c-Al} = \sqrt{2Dt} \tag{2.1}$$

where L_{c-Al} is the length of exchanged c-Al part of the NW (nm), D is the diffusion constant ($nm^2\,s^{-1}$) of Al in Ge and t is the process time (s).[36] This growth behavior appeared to be similar to the formation of Ni silicide thin films on a Si substrates.[77]

Further, investigations determining the influence of the Ge NW diameter in the range between 127 nm and 150 nm revealed an increase of the diffusion rate with decreasing NW diameter.[36] Similar results were obtained by Kral et al.[35] where ex situ investigations by rapid thermal annealing (RTA) also revealed an size-dependent Al-Ge exchange process. However, it has be noted that the Al-Ge propagation rates can only be correctly interpreted if the reaction initiates in all Ge NWs simultaneously, which is known to be unlikely for the used ex situ approach and underlines the importance of in situ experiments. Another important factor influence the diffusion rates could also be strain in bent or kinked Ge NWs. Moreover, it was found that the start of the Al diffusion was different for each NW, which most likely is due to variations of the Al-Ge contact at the overlap between the Ge NW and the Al metalization. However for successive annealing steps the rates appeared to be much more constant.[36]

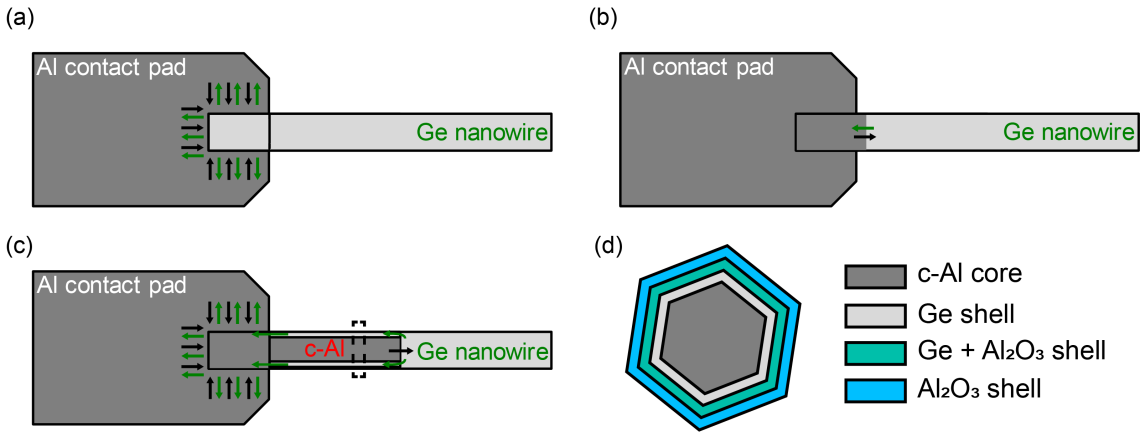

Figure 2.6: *Mechanism of Al diffusion in Ge nanowires:*
(a) Ge NW contacted by an overlapping Al pad. Upon heating at $T = 623\,\mathrm{K}$, Ge is diffusing out of the overlapping part of the Ge NW. The black and green arrows indicate the replacement of Ge by Al from the contact pad. (b) Further annealing results in the formation of a diffusion front gradually progressing along the quasi-1D nanowire resulting in an c-Al-Ge heterostructure. (c) Detailed schematic showing the diffusion of Ge into the Al pad. (d) Schematic of the cross-section obtained at the location of the dashed black rectangle after the thermally induced exchange of Ge by Al. The cross-section is indicating a core-shell structure comprising a c-Al core with several Ge containing shells wrapped around.

2.4 Transport in ultra-scaled 1D nanostructures

Over recent years, intense research facilitated a rapid down-scaling of nanoelectronic devices, enabling the observation of a shift from diffusive to ballistic and further on quantum ballistic transport.[78] A schematic illustration based on a quasi-1D channel with a length (L) and a diameter (d) is shown in figure 2.7.

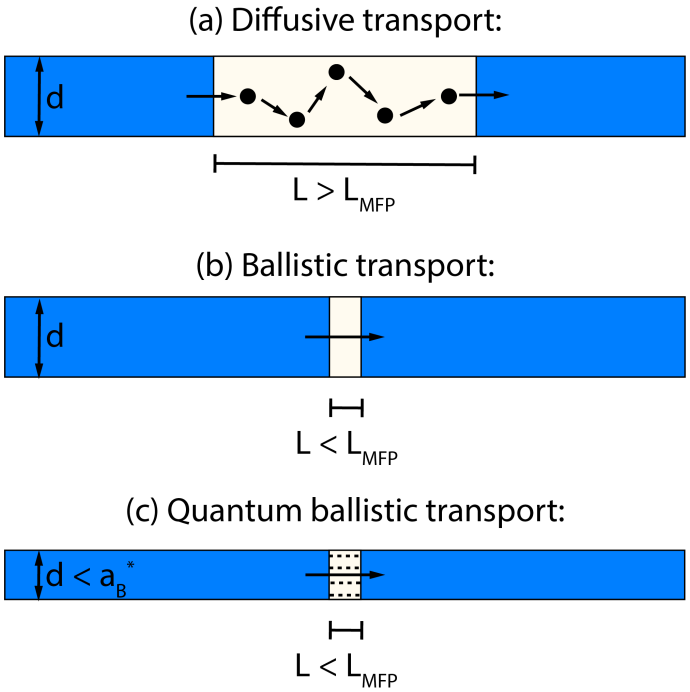

Figure 2.7: *Transport phenomena in channels of the length L and diameter d: (a) Diffusive transport: charge carriers scatter with phonons, crystal defects, impurities or grain boundaries, (b) Ballistic transport: charge carriers traverse through the channel without scattering, (c) Quantum ballistic transport: for $d < a_B^*$ the conduction- and valence-band of the channel are composed of equally spaced sub-bands.*

As shown in figure 2.7(a), in the case of diffusive transport, traversing charge carriers encounter collisions (scattering) with phonons, crystal defects, impurities or grain boundaries. Consequently, upon propagation, the charge carriers loose energy to the crystal lattice, which results in parasitic effects like heating, degradation, limited carrier velocities and a significant temperature dependence of the conductivity.[41] In contrast, the channel length of a ballistic conductor is below the scattering mean free path of the charge carriers (L_{MFP}) and is defined as the average distance charge

carriers can traverse through a channel without scattering (see figure 2.7(b)). [9] The L_{MFP} is material and temperature dependent and ranges at room-temperature from several manometers in group-IV semiconductors to micrometers in SWCNT and group-III-V compound semiconductors.[9, 12, 79] In the absence of scattering events, charge carriers accelerated by an electric field gain energy without losing it to the lattice. Thus, charge carriers can traverse through a channel exceeding the saturation velocity.[41] Applications utilizing the significant advantages of ballistic conduction, include transistors operating at the upper limit of ON-state conductance and ultra-fast solid-state drives. [8, 25] Finally, as schematically shown in figure 2.7(c), the quantum ballistic transport regime can be accessed by scaling d of a ballistic channel below a_B^*, which is material and temperature dependent and is defined as the distance between the electron and the hole within an exciton.[78] Below a_B^*, the conductance and valance band are not continuous anymore, but are composed of a discrete number of equally spaced sub-bands (modes, conductance channels). The energetic spacing of these sub-bands is material dependent.[79] Based on this characteristic, quantum ballistic devices are foreseen to enable multi-value logic devices capable of implementing complex functionalities with a minimum number of gates.[7] In the following subsections, the origins of ballistic and quantum ballistic transport will be discussed in more detail.

2.4.1 Ballistic transport

The investigation of transport effects in a ballistic conductor requires a coupling to 3D electron reservoirs. The L_{MFP} of the ballistic conductor depends on the effective mass m^*, the carrier density n and the momentum relaxation time τ_m[78]:

$$L_{MFP} = \frac{\hbar}{m^*}\sqrt{2\pi n}\tau_m \tag{2.2}$$

An schematic illustration of such an arrangement with a ballistic conductor coupled to macroscopic contacts is shown in figure 2.8.

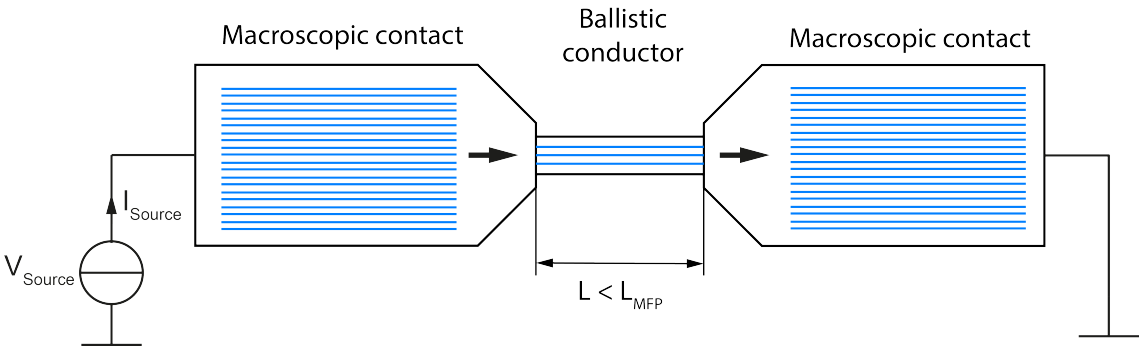

Figure 2.8: *Schematic illustration of a contacted ballistic conductor: Inside the macroscopic contacts the current is carried by a continuous conduction band, while conduction through the ballistic conductor occurs via a discrete number of sub-bands (blue lines). As indicated by the black arrows, conduction through this arrangement requires a redistribution of the current that causes a contact resistance.*

Taking into account the effective mass of holes in Ge $m^*_{Ge} = 0.041m_0$, a carrier density of $n_{Ge} = 5 \times 10^{20}\text{cm}^{-3}$ and a momentum relaxation time of $\tau_{mGe} = 0.26\,\text{ps}$, the scattering mean free path of Ge calculates to $l_{mGe} = 37.2\,\text{nm}$.[80]
Further, as in this model macroscopic metallic contacts are assumed, the current in this structures is carried by a large number of sub-bands with negligible energetic spacing, resulting in continuous bands, implied by the dense blue lines.[79] In contrast, conduction through the ballistic conductor occurs via a discrete number of sub-bands. Further, the resistance is not depending on the conductivity of the material σ and the width to length ratio (d/L) anymore, but on the redistribution of the current from the macroscopic contacts to the ballistic conductor (black arrows) that causes a contact resistance. Although momentum conservation is assumed, due to reflections at the interface between the macroscopic contacts and the ballistic conductor, only a small intersection of modes below the Fermi energy can propagate into the ballistic conductor.[78]
For the calculation of the contact resistance due to a redistribution of the current from the macroscopic contacts to the ballistic conductor, the electron velocity $\nu = \frac{1}{\hbar}\frac{\partial E(k)}{\partial k}$, the carrier transit time $t_t = \frac{L}{\nu}$ and the microscopic current $I = \frac{e}{t_t}$ are required. [78, 81] Inserting ν and t_t in the equation of I yields:

$$I = \frac{e}{L} \sum_{l,k} \frac{1}{\hbar} \frac{\partial E(k)}{\partial k} [f(E - E_{F1}) - f(E - E_{F2})] \tag{2.3}$$

In the next step, the sum over k is converted to an integral. Further, a spin degeneracy of two and the inverse of the level spacing $L/2\pi$ is introduced:

$$I = \frac{e}{L} \frac{2L}{2\pi} \sum_{l} \int dk \frac{1}{\hbar} \frac{\partial E(k)}{\partial k} [f(E - E_{F1}) - f(E - E_{F2})] \tag{2.4}$$

$$I = \frac{2e}{h} \int dE [f(E - E_{F1}) - f(E - E_{F2})] N(E) \tag{2.5}$$

where $N(E)$ denotes the number of conductance channels as a function of energy.

Assuming $N(E)$to be constant over the integration range yields:

$$I \approx \frac{2e^2}{h} N \frac{[E_{F1} - E_{F2}]}{e} \tag{2.6}$$

where $\frac{[E_{F1} - E_{F2}]}{e}$ can be identified as the voltage V between the electrodes. Thus, the quantized contact resistance of a ballistic conductor as a function of N can be formulated as follows:

$$R_C = \frac{V}{I} = \frac{h}{2e^2} \frac{1}{N} \tag{2.7}$$

Thus, assuming perfect interfaces between the macroscopic contacts and a ballistic channel with conduction through only one sub-band, the contact resistance is $R_C = \frac{h}{2q^2}$, which is denoted as the quantum resistance $R_Q = 12.9\,\mathrm{k\Omega}$. Moreover, for opening up a further sub-band participating to conduction, the resistance is reduced by a factor two. It is important to note, that R_C is not related to quantum mechanical effects, but can be attributed to the redistribution of the current and the channel length of the conductor ($L < L_{MFP}$). [78, 79, 81]

2.4.2 Quantum ballistic transport

By integrating a ballistic conductor, fulfilling the condition $d < a_B^*$, into a transistor architecture, the occupation of sub-bands can be controlled by applying a gate-voltage. A schematic illustration of such an arrangement is shown in figure 2.9(a). The accessible sub-bands are indicated by the dashed black lines.
In such an architecture, for particular materials at sufficiently low temperatures, the conductance reveals a regular step function with a step-height of G_0, as the gate-voltage is varied. G_0 is the conductance quantum that is obtained by $G_0 = 1/R_C = 2e^2/h$. Thus, plotting the conductance in units of G_0 reveals the number of sub-bands participating to current transport.[79, 82] A schematic illustration of the $G - V_G$ characteristic is shown in figure 2.9 (b).
However, the observation of conductance quantization in actual devices is rather difficult, because of a strong suppression of disorder, which often originates from structural imperfections of the channel.[83] Further, studying conductance quantization in most materials is restricted to low temperatures and requires sophisticated nanostructure formation techniques and precise lithography for contact formation as well as a low-noise measurement setup.

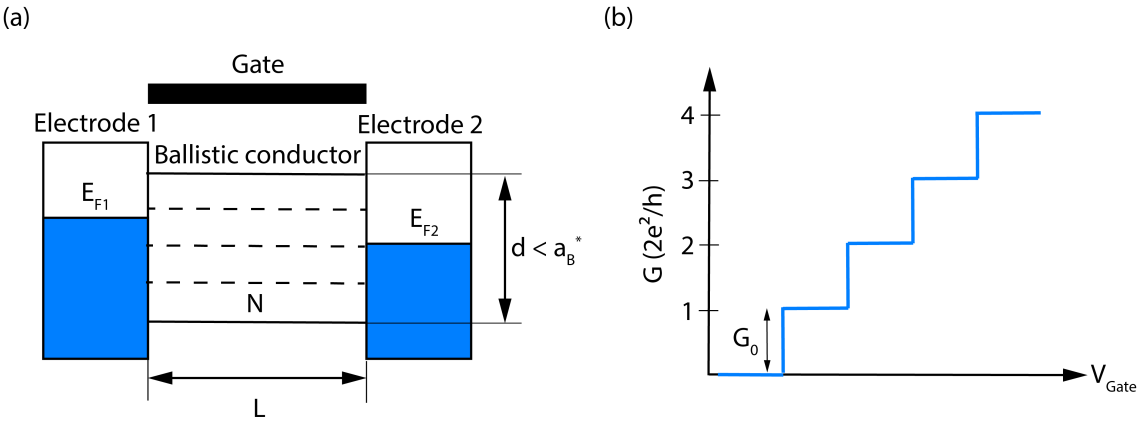

Figure 2.9: *Quantum ballistic transport:*
(a) A ballistic conductor of the length L is connected to two electrodes with the Fermi energies E_{F1} and E_{F2}, respectively. N is the number of conductance channels for charge carriers to traverse through the channel, which can be controlled via the gate-electrode (dashed black lines). (b) Conductance of a dimensional channel as a function of the gate-voltage V_G showing a regular step function with a step-height of G_0.

The maximum number of sub-bands (N) in a gated ballistic conductor can be calculated assuming a saddle potential confining the charge carriers in the y-direction transverse to the channel axis forming potential barrier at the saddle minimum along the x-direction of current flow. As the gate-voltage is varied, the potential evolves smoothly, with the saddle minimum rising and falling in energy with respect to the polarity of the gate-voltage.[79] In this case the charge carrier potential energy reassembles a parabolic form:

$$V(x,y) = V_0 - \frac{1}{2}m^*\omega_x^2 x^2 + \frac{1}{2}m^*\omega_0^2 y^2 \tag{2.8}$$

where V_0 is the saddle-barrier height, m^* is the effective mass, and ω_x and ω_0 are the characteristic oscillator frequencies.[79]

As the parabolic potential reassembles a harmonic-oscillator potential, the motion in the direction of confinement can be assumed to be quantized into a set of equally spaced energies.[79] Thus, the resulting electron dispersion relation (with energy measured relative to the conduction-band edge) is then given by:

$$E_n = [n + \frac{1}{2}]\hbar\omega_0 + \frac{\hbar^2 k_x^2}{2m^2}, \quad n = 1, 2, 3, ... \tag{2.9}$$

As shown in figure 2.10, only sub-bands with an energy threshold at $k_x = 0$ below the Fermi level will be populated and thus can contribute to current through the ballistic conductor.

To finally obtain the expression of N, the effective diameter at E_F has to be concerned:

$$E_F = \frac{1}{2}m^*\omega_0^2\frac{d^2}{4} \tag{2.10}$$

Rearranging this equation results in the expression for d:

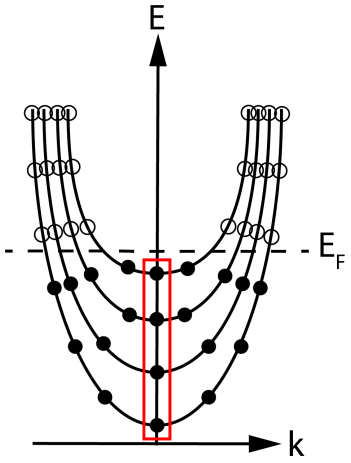

Figure 2.10: *E-k diagram of a quantum ballistic conductor: A gate-voltage was applied to raise the Fermi level to promote a filling of electron states in the first four sub-bands. The red rectangle indicates the the populated sub-bands at $k_x = 0$. Image adapted from [79].*

$$d = \frac{2\hbar k_F}{m^* \omega_0} \tag{2.11}$$

where E_F was expressed using $p = \hbar k$ and $E = \frac{p^2}{2m^*}$.

Next, the expression for the Fermi level can be formulated as:

$$E_F > (N - \frac{1}{2})\hbar\omega_0 \tag{2.12}$$

Rearranging this equation, the number of sub-bands N can be expressed as:

$$N = Int[\frac{1}{2} + \frac{E_F}{\hbar\omega_0}] \approx \frac{E_F}{\hbar\omega_0} = \frac{k_F d}{4} = \frac{\pi d}{2\lambda_F} \tag{2.13}$$

where λ_F is the Fermi wavelength:

$$\lambda_F = \frac{h}{\sqrt{2m^* E_F}} \tag{2.14}$$

Inserting the bulk values for the effective mass of holes in intrinsic Ge $m^*_{Ge} = 0.041m_0$, the Fermi wavelength calculates to $\lambda_{FGe} = 10.67\,\text{nm}$.[80]

Finally, assuming an square-well potential the expression for N simplifies to:

$$N = \frac{2d}{\lambda_F} \tag{2.15}$$

Using the calculated λ_{FGe}, the number of possible sub-bands of a Ge channel with $d = 25\,\text{nm}$ equal to a^*_B calculates to $N = 4$. Further, the energetic spacing between the conductance channels is on the order of $\frac{h^2}{m^* d^2}$.[21]
Thus, the energetic spacing between the sub-bands of a Ge channel with $d = 25\,\text{nm}$ further calculates to $\Delta E = 117.4\,\text{meV}$. Due to thermal broadening, the observation of a quantized conductance in two terminal devices is only possible for $\Delta E > 3.5 k_B T$ (full-width at half-maximum of the derivative of the Fermi-Dirac distribution).[79] Otherwise thermal fluctuations would excite carriers to the vicinity of the Fermi level, washing out the step-function of the $G - V_G$ characteristic.[21, 79]
As the calculated value of ΔE for a Ge channel of $d = 25\,\text{nm}$ is fulfilling the aforementioned condition for two terminal devices, a discrete number of 1D sub-bands should be observable, even at room temperature.

Further, the experimental observation of quantum ballistic transport at nonzero temperatures requires to take a combination of thermal broadening of the electron distribution in the sub-bands and disorder broadening at the sub-band edges into account [79]. The combination of these effects are descried by the following thermal broadening function [24]:

$$F(E) = \frac{\partial f(E)}{\partial E} = \frac{1}{4k_B T}\ sech^2(\frac{E}{2k_B T}) \tag{2.16}$$

where, $f(E)$ denotes the Fermi function and $sech = \frac{1}{cosh(x)}$.

Hence the total number of populated sub-bands taking thermal and disorder broadening into account is:

$$N(E_F) = \int N(E)F(E - E_F)G(E - E_F)dE \tag{2.17}$$

$$G(E) = \frac{1}{c\sqrt{2\pi}} \exp(\frac{-E^2}{2c^2}) \tag{2.18}$$

where c is the variance of the Gaussian distribution function.

The combination of both thermal and disorder broadening should result in a shift from abrupt steps to rounded and often smeared out conduction plateaus for nonzero temperatures.[24]

2.4.3 Coulomb blockade

Coulomb blockade is a fundamental transport effect of a quantum dot reassembling an isolated charge island containing localized electrons coupled to two electron reservoirs via tunnel junctions.[79, 84]
For sufficiently small dimensions of the quantum dot and low temperatures, the corresponding capacitances of the arrangement are small. A schematic equivalent circuit diagram showing a capacitive coupling of the quantum dot to metallic leads is depicted in figure 2.11(a). In such a system, electron-electron or hole-hole interactions based on the electrostatic capacitive charging energy are observed. Consequently, the tunneling of electrons / holes in out of the quantum dot is suppressed by the Coulomb repulsion of charges on the quantum dot.[79] Thus, the energy for putting an additional charge onto the quantum dot requires the so called charging energy:

$$E_C = \frac{e^2}{2C} \tag{2.19}$$

where C is the capacitance of the quantum dot.

Consequently, the Coulomb blockade effect allows to control the tunneling of electrons across a quantum dot by applying a sufficiently high bias voltage. The resulting I/V characteristic for applying a source voltage (V_{Source}) and setting the drain voltage (V_{Drain}) to ground is depicted in figure 2.11(b).
As can be seen, due to the charging energy of the quantum dot, a Coulomb gap has opened, where no electrons can tunnel onto or out of the quantum dot and the current flow is zero ($|V_{Source}| < e/2C$). By surpassing this threshold voltage, the Coulomb repulsion energy is exceeded and electrons can tunnel across the arrangement generating a current flow.

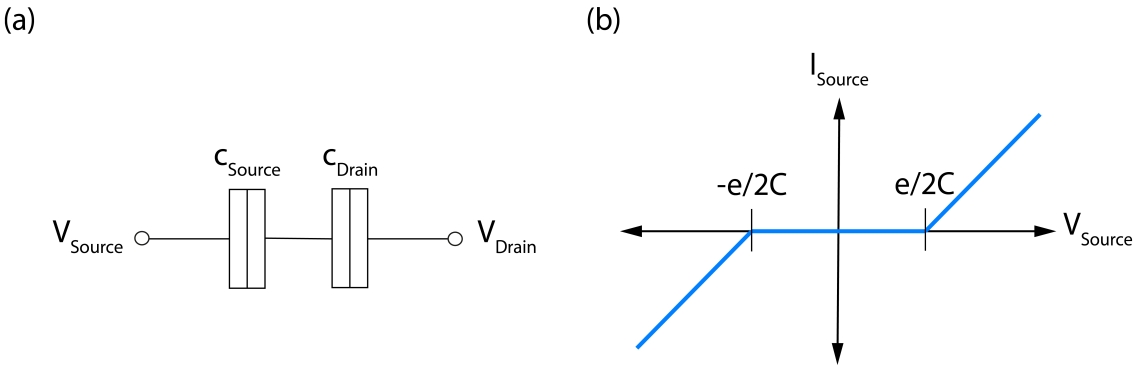

Figure 2.11: *Coulomb blockade:*
(a) Equivalent circuit diagram of an isolating island capacitively coupled to metallic leads. (b) Typical I-V characteristic for applying a voltage across an isolating island. Due to Coulomb repulsion, the current is blocked for $|V_{Source}| < e/2C$.

In addition to the formation of an isolated charge island connected to electron reservoirs by tunnel junctions, three conditions have to be fulfilled to observe Coulomb blockade effects:

First, V_{Source} has to be lower than the elementary charge divided by the self-capacitance of the island:

$$V_{Source} < \frac{e}{C} \tag{2.20}$$

Second, the thermal energy has to be smaller than the charging energy, otherwise

Coulomb blockade effects would be washed out by thermal noise:

$$k_B T < \frac{e^2}{2C} \tag{2.21}$$

Third, based on Heisenberg's uncertainty principle, the resistance of the tunnel barriers coupled to the quantum dot have to be larger than the quantum resistance:

$$\Delta E \Delta t \geq \frac{h}{2} \tag{2.22}$$

where ΔE is the charging energy and Δt is the time constant of the system:

$$\Delta E = \frac{e^2}{C} \tag{2.23}$$

$$\Delta t = RC \tag{2.24}$$

Finally, inserting these two expressions into $\Delta E \Delta t$ gives the condition for the tunnel resistance:

$$R = \frac{h}{e^2} \tag{2.25}$$

Further, it is important to note that the the small size of the quantum dot results in a quantization of charge. The energy level spacing of electron states increasing indirectly proportional to the square of the quantum dot size (d):

$$E_N = \frac{1}{2m^*}(\frac{hN}{2d})^2 \tag{2.26}$$

where N is the number of charges on the quantum dot.

For a further discussion of Coulomb blockade effects, the confinement potential of a quantum dot revealing a quantization of charges is schematically shown in figure 2.12. Depending on the applied bias voltage, the resulting chemical potentials of the source (μ_{Source}) and drain (μ_{Drain}) enable two possible configurations:
First, in case there are no available energy levels on the dot in the bias window, the number of charges on the quantum dot is fixed to N and there is no current flow. This configuration is depicted in figure 2.12(a). Second, as can be seen in figure 2.12(b), changing the chemical potentials to align with μ_N, the number of electrons on the quantum dot alternates between N and N-1 and the device is in single-electron tunneling mode.[21]

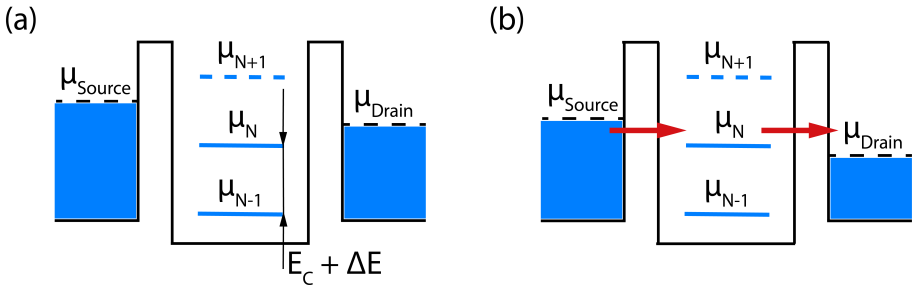

Figure 2.12: *Confinement potential of an isolated island:*
(a) Blocking state: There is no available level in the bias window. The number of electrons on the island is fixed to N. (b) Single electron tunneling state: The chemical potentials of the source and drain align with the level μ_N. The number of electrons is alternating between N and $N-1$.

Further, by extending the arrangement of figure 2.11(a) of the quantum dot coupled to metallic electron reservoirs with a gate-electrode, capacitively coupled to the quantum dot a single-electron transistor (SET) can be reassembled.[21, 79] An equivalent circuit diagram of a SET is shown in figure 2.13(a). In such a device, applying a gate-voltage can now be used to shift the whole ladder of electrochemical potential levels up or down.[21] Thus, the coupling strength between the quantum dot and the metallic electron reservoirs can be periodically lifted as a function of the gate-voltage. This characteristic behavior gives rise to applications like extremely sensitive charge detectors,[85] single electron/hole spectroscopy[86] or low power dissipating nanoelectronics[87].
The stability diagram of a SET can be obtained by sweeping V_{Source} as a function of

the gate-voltage V_{Gate} and measuring the current through the SET, which depends on the principle of resonant tunneling.[79] A schematic illustration of a typical stability diagram showing diamond like structures is depicted in figure 2.13(b). Inside the diamond-shaped regions, the current flow is suppressed and the number of electrons on the quantum dot is constant, due to the Coulomb blockade. The Coulomb blockade is maximized any time the charge on the gate-voltage is an integer multiple of the charge of an electron.[21] The edges of these Coulomb diamonds mark the onset of current flow and correspond to a level in the bias-window being resonant with either source or drain, which results in single-electron tunneling. From such a bias spectroscopy, one can directly read off E_C as the height of the diamonds from zero voltage. Further, based on the periodicity and the slopes of the Coulomb diamonds the capacitances of the entire system can be obtained.[84]

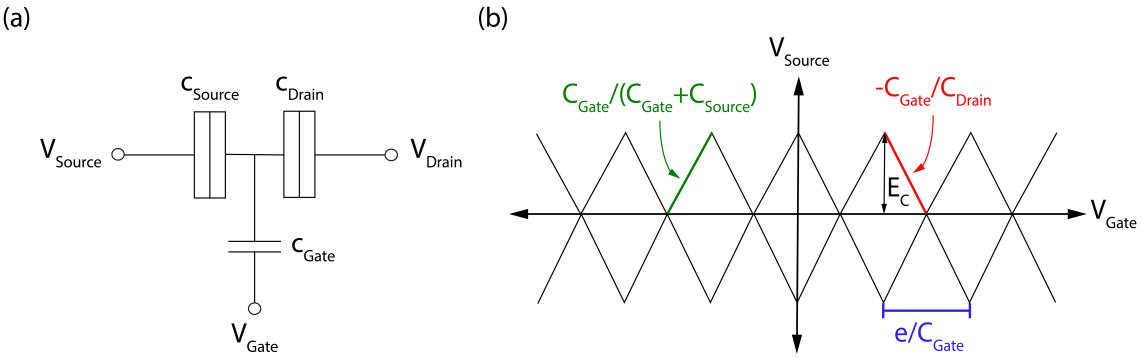

Figure 2.13: *Single electron transistor:*
(a) Equivalent circuit diagram of a SET showing the capacitive coupling of a semiconducting island to metallic leads. (b) Stability diagram of a SET showing a periodic lifting of the Coulomb blockade effect as a function of the gate-voltage. The capacitances shown in the equivalent circuit diagram of the SET can be extracted from the slopes and spacing of the diamonds. E_C can be obtained from the height of the diamonds form zero voltage.

2.4.4 Josephson junction

An arrangement of two superconductors coupled via a sufficiently thin insulating barrier, which can be either an isolator, a semiconductor or a non-superconducting metal, is denoted a Josephson junction.[82, 88] In such an arrangement superconductivity may be induced into the isolating barrier. Consequently, Cooper pairs can be coherently exchanged from one superconductor to the other via tunneling, which

results in a dissipationless current flow across the device up to a certain threshold value, referred as "critical current" or Josephson current (I_c). The working principle of Josephson tunneling is schematically depicted in figure 2.14.

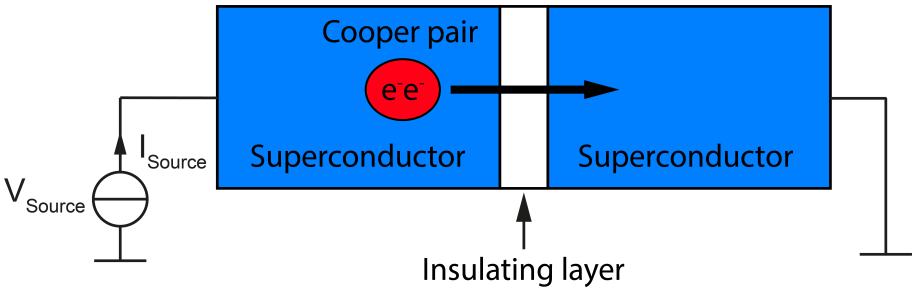

Figure 2.14: *Working principle of Josephson tunneling:*
An arrangement of two superconductors separated by a thin barrier enables the exchange of cooper pairs between the superconductors via tunneling.

Besides fundamental investigations of transport in mesoscopic systems, the concept of Josephson junctions bear great potential for a vast array of possible applications in analog and digital electronics, such as superconducting quantum interference devices (SQUIDs), oscillators, mixers and amplifiers.[89–91]
The underlying mechanism of Josephson tunneling is the proximity effect[92], which describes that the non-locality of the Cooper pairs can not be abruptly revoked at a superconductor - normal conductor (S-N) interface. This results in "leaking" of Cooper pairs from the superconductor into the normal conductor. Thus, Cooper pairs are able to "diffuse" a certain distance before they decay via scattering. Consequently, the maximum thickness of the insulating barrier depends on the proximity length or coherence length that denotes the penetration depth of the Cooper pairs into the insulating layer:[88]

$$\xi_N = \sqrt{\hbar D_N / 2\pi k_B T_c} \tag{2.27}$$

where D_N is the material and temperature dependent diffusion constant of Cooper pairs and T_c is the critical temperature of the superconductor.

The underlying mechanism of the proximity effect in a superconductor - normal conductor - superconductor (S-N-S) arrangement is closely related to a scattering based retroreflection mechanism occurring at interfaces between a superconductor and a normal state material, denoted Andreev reflections.[88, 93]
Figure 2.15(a), shows a schematic illustration of the Andreev reflection mechanism. In a superconductor the energy gap Δ is a region of suppressed density of states around the Fermi energy E_F, indicating the energy gain for two electrons upon the formation of a Cooper pair. Consequently, for electrons with $E < \Delta$, traversing from the normal conductor in the superconductor, no quasi-particle states are provided in the superconductor and thus transmission is excluded. Further, as there is no energetic barrier present at the interface that can absorb the momentum difference, a normal reflection is also not possible. However, if a second electron from the normal conductor is involved in the process, a Cooper pair can be formed. Consequently, a hole is formed in the normal conductor to maintain the charge neutrality and satisfy momentum conservation. As the hole takes the same path as the incident electron, but in reverse direction, this process is called a retroreflection. According to the opposite charge and group velocity of electrons and holes, the measured conductance of the junction is twice as large as for an ideal normal transmission through the interface.[88] According to reflections between the two interfaces, multiple Andreev reflections (MARs) contribute to the formation of "Andreev channels" to open up in the junction at bias voltages below the superconducting energy gap 2Δ. These channels are observable as kinks in the I/V characteristic and appear when the sum of the energy gain equals 2Δ, which results in a resonant enhancement in the conductance.[20] Repeating cycles of Andreev reflections on both sides of a Josephson junction cause Andreev bound states, which are described as the effect of the phases of the holes and electrons circulating around the Fermi level of the junction (see figure 2.15(b)). As the phases of the holes and electrons are equal to $2n\pi$, energy discretization takes place.[94] Considering the case of an incident electron with $E > \Delta$, quasi-particles can be excited in the superconductor. Thus, in addition to an Andreev reflection, normal secular electron reflection takes place.[88, 95]

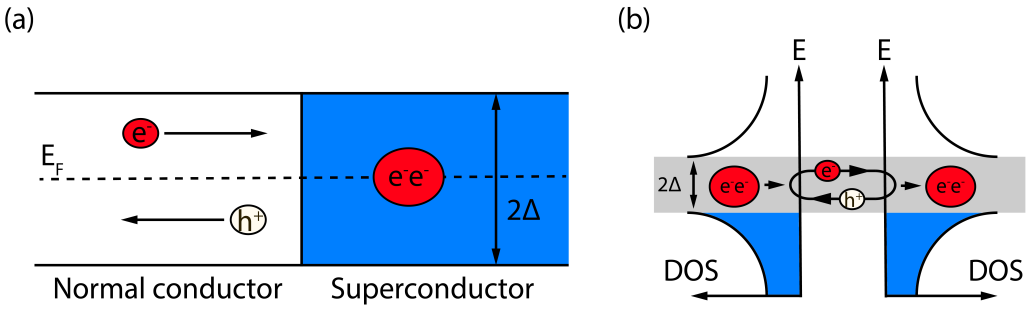

Figure 2.15: *Schematic illustration of the Andreev reflection mechanism: (a) An incident electron from the normal-conductor is retroreflected, resulting in the formation of a Cooper pair in the superconductor. (b) Schemtaic illustration of Andreev bound states traversing through a Josephson junction*

As schematically depicted in figure 2.16(a), Josephson tunneling can be quantum mechanically understood as an overlap of the wavefunctions (Ψ_1, Ψ_2) of the two superconductors separated by the thin insulating layer. Consequently, the dynamics of the two wavefunctions can be determined by the following coupled Schrödinger equations:

$$i\hbar\frac{\partial\Psi_1}{\partial t} = \mu_1\Psi_1 + K\Psi_2 \tag{2.28}$$

$$i\hbar\frac{\partial\Psi_2}{\partial t} = \mu_2\Psi_2 + K\Psi_1 \tag{2.29}$$

where the coupling across the junction is represented by K and μ_1 and μ_2 are the lowest energetic states on both side of the junction.

Within one superconductor and in the absence of a current, all Cooper pairs can be described by a single wavefunction because all the pairs have the same phase, which is denoted as phase coherence.[96] Thus, considering an arrangement of two superconductors separated by an isolating layer with thickness below the proximity length, the wavefunctions of the Cooper pairs in the superconductors are exponential like the free particle wavefunction:

$$\Psi_1 = \sqrt{n_1} e^{i\theta_1} \tag{2.30}$$

$$\Psi_2 = \sqrt{n_1} e^{i\theta_2} \tag{2.31}$$

where n_1, n_2 are the densities of Cooper pairs in the superconductors and θ_1, θ_2 are the respective phases. The wavefunctions of Cooper pairs on each side of the junction penetrating into the insulating region are "locking together" in phase, resulting in a current flow through the junction in the absence of an applied voltage (DC Josephson effect).[96] A typical I-V characteristic of a Josephson junction showing a critical current in the insulating barrier is depicted in figure 2.16(b).

Finally, the equations of the Josephson effect can be obtained by substituting the equations 2.30 and 2.31 into 2.28 and 2.29:

$$\hbar \frac{\partial n_1}{\partial t} = -\hbar \frac{\partial n_2}{\partial t} = 2K\sqrt{n_1 n_2}\, sin(\theta_2 - \theta_1) \tag{2.32}$$

$$-\hbar \frac{\partial}{\partial t}(\theta_2 - \theta_1) = \mu_2 - \mu_1 \tag{2.33}$$

Applying a voltage across the Josephson junction, the term $\frac{\partial n}{\partial t}$ describes a charge transport denoted as Josephson current. Further, applying a voltage V_{12} across the junction would shift the energy levels according to $\mu_2 - \mu_1 = 2eV_{12}$:

$$I = 2K\sqrt{n_1 n_2}/\hbar\, sin(\theta_1 - \theta_2) = I_0 sin(\delta) \tag{2.34}$$

$$\frac{\partial \delta}{\partial t} = \frac{2eV_{12}}{\hbar} \tag{2.35}$$

where I_0 substitutes $2K\sqrt{n_1 n_2}/\hbar$ and δ substitutes $\theta_1 - \theta_2$.

The equations 2.34 and 2.35 describe the dynamics governing a Josephson junction and thus are denoted Josephson or weak-link current-phase relation and superconducting phase evolution equation respectively.[88]

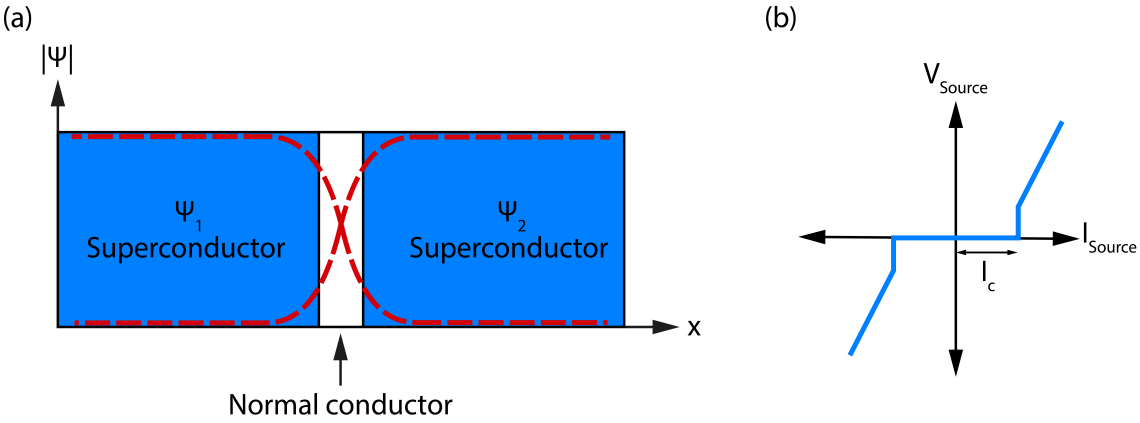

Figure 2.16: *Schematic illustration of a Josephson junction:*
(a) Schematic showing the decay of the wavefunctions of the left and right superconductor inside the normal conductor. For sufficiently thin normal conductors the wavefunctions overlap and tunneling of cooper pairs across the junction is possible. (b) Typical I-V characteristic of a Josephson junction showing a supercurrent in the insulating layer.

The concept of modulating the charge carrier concentration in a semiconductor by the means of the field effect mediated by applying a voltage to a gate-electrode is one of the main foundations of modern microelectronics.[88] Interestingly, by extending a superconductor - semiconductor - superconductor arrangement by an isolated gate-electrode, the concepts of a Josephson junction and a field-effect transistor can be combined to realize a Josephson field-effect transistor (JoFET).[88]. A schematic illustration of a JoFET is shown in figure 2.17(a). Such a three-terminal device features a gate-tunable semiconducting channel that enables the exchange of Cooper pairs between two superconductors mediated by the superconducting proximity effect.[97] As the proximity length depends on the electron concentration of the semiconductor, which can be controlled by the electric field set by the gate-voltage, the critical current of a JoFET can be effectively controlled.[98] A typical I-V characteristic of a JoFET enabling a gate-tunable critical current in the semiconducting channel is shown in figure 2.17(b).

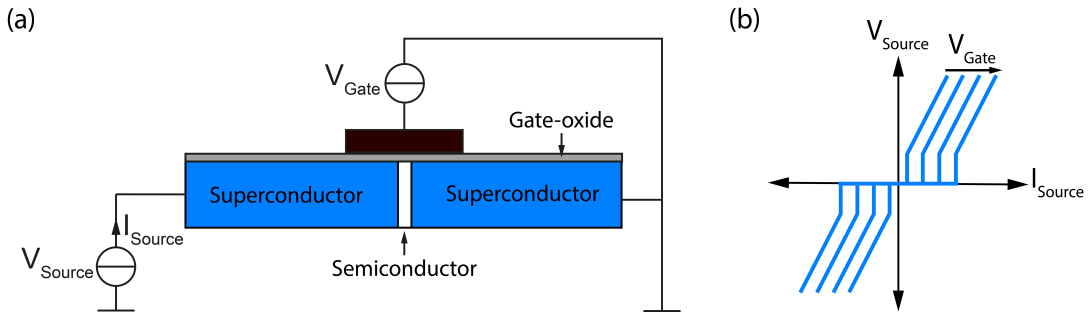

Figure 2.17: *Josephson field-effect transistor:*
(a) Schematic illustration of a Josephson field-effect transistor comprising a S-N-S arrangement extended by an isolated gate-electrode. (b) Typical I-V characteristics of a Josephson field-effect transistor for different gate-voltages enabling a gate-tunable supercurrent in the semiconducting channel.

Dover et al.[99] described the dependence of the critical current on the gate-voltage for a JoFET with a channel length $L < \xi_N$ as follows:

$$I_c = {R_N}^{-1} \frac{\pi \Delta^2}{2ek_B T_c} \frac{\rho_N m_e}{\rho_s m_N^*} A^2 f^2 \frac{L}{\xi_N} e^{-L/\xi_N} \tag{2.36}$$

where ρ_S and ρ_N represent the gate-voltage dependent resistivities of the superconductor and normal conductor, respectively. Further, f is the ratio of the order parameter at the interface to its bulk value and A is the factor by which the order parameter changes on crossing the interface.[88]

With respect to the temperature dependence of the critical current, the Likharev model[100] can be applied:

$$I_c(T) = I_{c,0} e^{-L/\xi_N(T)} \tag{2.37}$$

Besides applications such as charge qubits, sensitive magnetometers or as fast low power dissipating logic, JoFETs also bear a high potential for the fundamental investigation of Fabry-Pérot-like interference patterns of the critical current or mesoscopic fluctuations and localization effects, directly demonstrating the wave nature of the electrons in a conductor.[88, 91, 101]

Chapter 3

Experimental techniques

This chapter discusses the experimental methods for the fabrication and electrical characterization of Al-Ge-Al NW heterostructures.
The first section describes the fabrication of a measurement module and the integration of Al-Ge-Al NW heterostructures in a back-gated FET architecture. Further, the fabrication of a Si_3N_4 based membrane chip for the structural analysis of Al-Ge-Al NW heterostructures is discussed. The second part of this chapter focuses on the measurement setups and the procedures for conducting electrical measurements at room-temperature as well as cryogenic temperatures are discussed. Finally, the measurement setups used for the low-temperature ($T < 1\,K$) characterization of the Al-Ge-Al NW heterostructures are addressed.

3.1 Nanowire device integration

In order to gain the ability to measure Ge NW based devices a sophisticated measurement module with macroscopic contact pads was designed. These contacts are needed for measurements with a cryostat setup, which requires wire bonds from the macroscopic pads to a printed circuit board (PCB). For device integration, Al contacts were used to connect the Ge NWs with the macroscopic bond pads on the measurement module. The entire fabrication process is schematically depicted in figure 3.1. As can be seen in figure 3.1(a), the substrate material for the measurement module is a highly p-type doped 500 µm thick Si <100> wafer with 100 nm of thermally grown SiO_2 on top. Next, a two step photolithography process using a Cr hardmask, image reversal resist (AZ5214) and developer solution (AZ726MIF) was used to pattern contacts onto the measurement module to get access to the backgate. In the first photolithography step, the vias for the substrate contacts were patterned. To complete the first step, the SiO_2 layer was etched using a buffered hydrofluoric acid (BHF). This shown in figure 3.1(b). In the second photolithography step, the contacts on top of the SiO_2 layer were patterned. To finalize the measurement module, the macroscopic Au pads were fabricated by Ti/Au deposition via magnetron sputtering with the "VonArdenne LS320 S" sputter system. Subsequently, a lift-off process was used to remove the excess metal. A schematic illustration of the completed measurement module is shown in figure 3.1(c). The detailed process parameters for the fabrication of the measurement module can be found in appendix A.1.

Next, Ge NWs with diameters between 20 nm and 30 nm encapsulated in a 20 nm Al_2O_3 shell were transferred onto the measurement module by the drop-casting method using a micropipette (figure 3.1(d)). Parameters regarding NW growth and passivation can be found in appendix A.3. To contact individual Ge NWs with the macroscopic bond pads, electron beam lithography (Raith e_LiNE), a positive PMMA based resist (AR-P 679.04) and a developer solution (AR 600-56) were used. In order to fabricate connections between the Ge NWs and the Al contacts, a two step etching process was used. First the ALD grown Al_2O_3-shell was removed by etching with BHF. Exposed to ambient air, Ge forms native oxide layer (see section 2.1.2). Thus, this oxide layer has to be removed prior to the Al sputter deposition in

the next step to form an adequate contact between the Al metallization and the Ge NWs. This was accomplished using a 14 % diluted hydroiodic acid (HI).[102] The fabrication of contacts to individual Ge NWs was finalized by Al deposition using a "VonArdenne LS320S" sputter system and lift-off techniques. In this configuration, the devices reassemble a Ge NW based back-gated FETs (figure 3.1(e)). A detailed listing of the process parameters for the Ge NW device integration on the measurement module can be found in appendix A.4.

To define Ge channel lengths without any lithographic limitations, a thermally induced heterostructure formation method was applied.[35] The controlled diffusion of Al from the contacts into Ge NWs was activated by an annealing process conducted in a "UniTemp UTP 1100" RTA system at a temperature of 624 K. Average diffusion rates of Al into the Ge NWs were experimentally determined between 2.5 nm s^{-1} and 15 nm s^{-1} depending on the applied annealing temperature, the diameter of Ge NWs and the material of the passivating shell. The process parameters of the heterostructure formation are listed in appendix A.5.

Applying this process results in Al-Ge-Al NW heterostructures with abrupt metal-semiconductor interfaces contacted by quasi-1D c-Al leads. The length of the remaining Ge segment can be controlled by the annealing time and temperature. Further, by lithographically defining different gaps between the Al contacts, it is possible to fabricate samples with Al-Ge-Al NW heterostructures featuring Ge segment lengths between 10 nm and 500 nm by applying just one annealing step. Moreover, as the diffusion of Al in the Ge NWs can be restarted upon further heating, by applying consecutive annealing steps, the Ge segment length can be reduced in a controlled manner. Thus, ultra-short channel lengths can be fabricated without any lithographic restrictions. The schematic illustration of the completed Al-Ge-Al NW heterostructure device is schematically shown in figure 3.1(f).

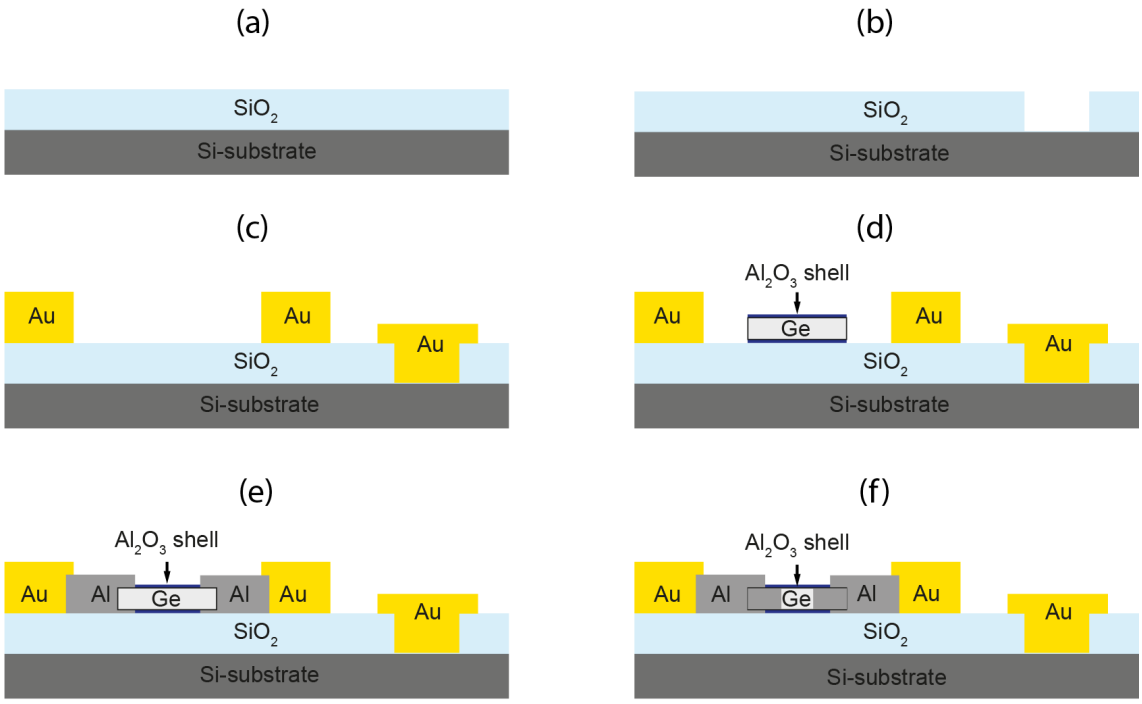

Figure 3.1: *Schematic illustration of the Al-Ge-Al NW heterostructure fabrication: (a): Highly p-doped Si substrate with* 100 nm *SiO_2 on top, (b) Via opening to contact the substrate, (c) Fabrication of Au contacts on top of the SiO_2 and to the Si substrate, (d) NW transfer to the measurement module, (e) Fabrication of Al contacts connecting the Ge NWs to the macroscopic Au bond pads of the measurement module, (f) Thermally induced Al-Ge-Al heterostructure formation to fabricate FETs with ultra-scaled Ge channels.*

3.2 TEM sample preparation

For the structural analysis of the crystal structure and the interfaces of Al-Ge-Al NW heterostructures, the device fabrication scheme discussed in section 3.1 needed to be transferred to an electron beam transparent substrate. Hence, the fabrication was performed on arrays of 40 nm thick Si_3N_4-membranes with window sizes of 200 µm x 200 µm. Additionally, the device fabrication was also performed on arrays of 140 nm thick membranes with holes, in order to obtain suspended devices enabling EDX mapping of the composition of the heterostructure devices. Both types of membrane chips were fabricated by Martien den Hertog (Institut NEEL CNRS, Grenoble, France).[103]

For the device processing on the membrane-chips several precautions must be taken.

Prior to the fabrication of Al-Ge-Al NW heterostructures, the membrane chips were mounted on a highly p-doped Si carrier wafer using PMMA as glue. This process step was necessary to prevent the membranes from being damaged during the spin-coating of resist required for the patterning of individual contacts to Ge NWs by electron beam lithography. To enable electron beam lithography on the membranes with holes, a thicker layer of resist was necessary to fill the holes and to achieve a uniform resist layer. The exposure parameters also needed to be optimized due to the lack of reflecting electrons from the underlying substrate. As a consequence of the thicker resist, the development time needed to be increased.
Figure 3.2 shows a schematic illustration of an Al-Ge-Al NW heterostructure device fabricated on the 40 nm thick Si_3N_4-membrane. A detailed listing of all process parameters for the fabrication of the membrane-chips and sample preparation for the electron beam lithography process is supplied in appendix A.2.
The structural analysis of the heterostructure devices fabricated on the membrane-chips was performed by TEM and EDX investigations. High-angle annular dark-field (HAADF) scanning transmission electron microscopy (STEM) was performed on a probe-corrected FEI Titan Themis working at 200 kV equipped with four silicon drift detectors for EDX analysis and a Fischione ultra narrow gap tomography sample holder. Further, for high-resolution imaging, a DENSsolutions 6 contact double tilt holder was used.[37]

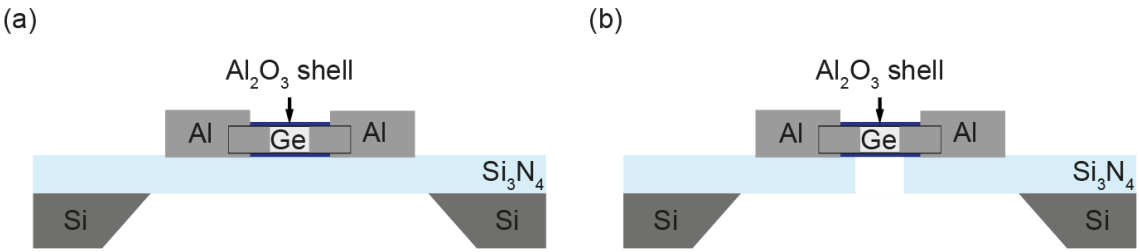

Figure 3.2: *Schematic illustrations of heterostructure devices on Si_3N_4-membranes: Al-Ge-Al NW heterostructure fabricated on a (a)* 40 nm *and (b)* 140 nm *thick Si_3N_4-membrane with holes required for the structural analysis of freestanding Al-Ge-Al NW heterostructure devices by TEM and EDX.*

3.3 Electrical characterization

For the electrical characterization of the fabricated Al-Ge-Al NW heterostructures, the measurement module was mounted on a Cu-substrate. For electrical insulation, a Kapton tape was glued between the measurement module and the Cu-substrate using silver conductive paste. Further, a PCB with a soldered on socket strip was glued on the Cu-substrate using an epoxy resin based glue. Wire bonding was used to connect the macroscopic bond pads of the measurement module with contacts on the PCB. In order to conduct electrical measurements, low-noise source measure units (SMUs) of a semiconductor parameter analyzer (Keysight B1500A) were connected to the PCB via coaxial cables. The resolution limit of the used setup is 500 fA. In comparison, the measured leakage currents between the back-gate and the Ge channels of the investigated devices was approximately 1 pA. For detailed analysis, the measured data were transferred to a PC via a GPIB connection. A schematic illustration of the complete measurement setup for the electrical characterization of Al-Ge-Al NW heterostructures is shown in figure 3.3.

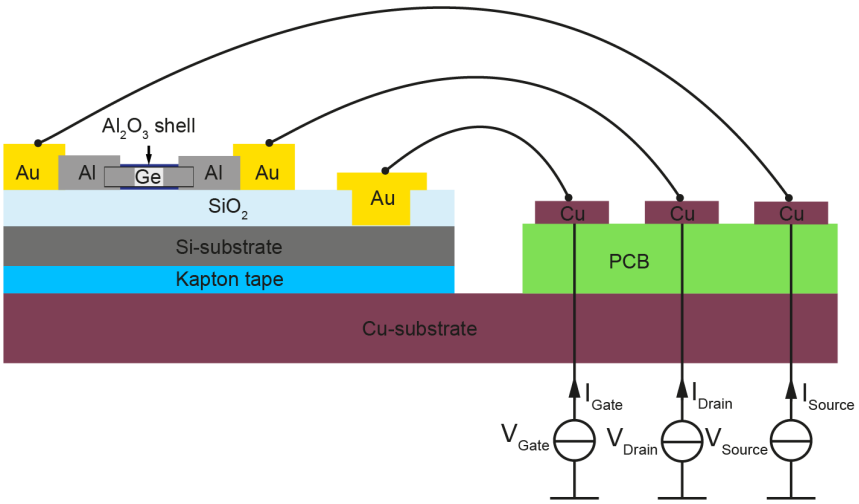

Figure 3.3: *Schematic illustration of the measurement configuration: Al-Ge-Al NW heterostructure fabricated on the measurement module glued to a Cu-substrate using silver conductive paint. For electrical insulation, an adhesive Kapton tape was used to insulate the measurement module from the Cu-substrate. To provide electrical contacts, a PCB was fixed to the Cu-substrate using an epoxy resin based adhesive. Au wire bonding was used to connect the Al-Ge-Al NW heterostructure as well as the global back-gate to the PCB. For electrical measurements, the contact pads on the PCB were connected to SMUs.*

3.3.1 I/V measurements

To investigate the contact properties and resistivity of Al-Ge-Al NW heterostructures, two terminal (2T) current-voltage (I/V) sweeps were performed. As only 2T measurements were conducted, the measured data contain a parasitic series resistance originating from the measurement setup and Al contacts between the Au pads and the Al-Ge-Al NW heterostructure as well as the c-Al leads contacting the Ge segment. However, as the resistance of the Ge segment is in the range 4.3 kΩ < R < 10 MΩ, the series resistance (≈700 Ω) is negligible for most of the measurements. To avoid any influences from radiation or ambient air, the I/V measurements were performed in vacuum at a background pressure of approximately 2.5×10^{-5} mbar in a cryostat (Cryo Industries CRC-102), featuring 12 electrical vacuum feedthroughs. For the I/V measurement of Al-Ge-Al NW heterostructures a voltage sweep was applied to the source (V_{Source}) or drain (V_{Drain}) contact of the device while simultaneously recording both the source (I_{Source}) and drain (I_{Drain}) current. Depending on the Ge segment length of the Al-Ge-Al NW heterostructures, the I/V characteristics of the devices was investigated in the measurement range between 10 mV and 1 V considering the breakdown field strength of $E_{Ge,max} = 10\,\mathrm{mV\,nm^{-1}}$. By additionally applying a voltage to the global back-gate (V_{Gate}),[41] the conductivity of the devices can be electrostatically modulated. Back-gate voltages in the measurement range of +/- 40 V were investigated. A schematic illustration of the measurement configuration is shown in figure 3.3. Based on the I/V measurements, the transport properties of Al-Ge-Al NW heterostructures were investigated by calculating the resistivity of devices with different Ge segment lengths. While devices with ultrashort Ge segment lengths show a linear I/V characteristic, heterostructures with Ge segment lengths longer than 45 nm reassemble back-gated Schottky barrier FETs, with $I \propto exp(eV/kT)$, due to two back-to-back Schottky contacts.[41] Thus, the resistance (R) of these devices needed to be calculated by fitting the measured current in the linear regime according to $R = \Delta V/\Delta I$. The resistivity of the heterostructure devices was calculated as follows:

$$\rho = \frac{RA_{Ge}}{L_{Ge}} = \frac{R\frac{d_{Ge}^2\pi}{4}}{L_{Ge}} \tag{3.1}$$

where the geometry of the Ge segment is considered by the length (L_{Ge}), the diameter (d_{Ge}) and the area (A_{Ge}). The transport properties of ultra-short Ge segments were further investigated via bias spectroscopy. This was accomplished by measuring I/Vs for different gate voltages from which the differential conductance $g = dI/dV$ was directly obtained and plotted as a function of the applied bias voltage. To further study the electrical transport through ultra-scaled Ge channels in the temperature regime between T = 5 K and 400 mK, a combination of a custom-built pumped ^{3}He cryostat (see section 3.4) and a low-noise electrical setup as used. The measurements were conducted at the institute Neel, CNRS Grenoble. The heterostructure devices were probed using both voltage and current biasing techniques with a National Instruments PCI DAC/ADC high frequency card. In the voltage biasing scheme, a voltage divider consisting of a ratio of 50 kΩ/50 Ω was used to reduce the amplitude of the voltage source. A Femto variable gain transimpedance amplifier (DCPCA-200) was used to convert and amplify the induced current to a voltage signal measured by the National Instruments card. In the current biasing scheme, a 10 MΩ resistor was used to convert the voltage signal to a current signal with a maximum amplitude of 1 µA. The current was applied to one contact of the sample while the other one was grounded. The potential difference across the sample was amplified by two NF Electronic Instruments low noise preamplifiers (LI-75A) connected in series, each of a gain of 100. The back-gate was biased using a Yokogawa programmable voltage source.

3.3.2 Transfer measurements

Al-Ge-Al NW heterostructures integrated on the measurement module reassemble back-gated p-type accumulation FETs.[35, 104] Hence, modulating the gate-voltage (V_{Gate}) and simultaneously applying a fixed bias on the source (V_{Source}) or drain (V_{Drain}) contact, the carrier concentration can be modulated and thus, the electrical transport through the Ge channel can be investigated. In detail, back-gate voltages in the measurement range of +/- 40 V were investigated. To avoid any influences from radiation or ambient air, the transfer measurements were also performed in vacuum at a background pressure of approximately 2.5×10^{-5} mbar using a cryostat (Cryo Industries CRC-102). A schematic illustration of the measurement

configuration is shown in figure 3.3.
To insure reliable measurements, the currents I_{Source}, I_{Drain} and I_{Gate} were recorded and analyzed. Depending on the Ge segment length of the Al-Ge-Al NW heterostructures, the applied bias voltages were fixed between 1 mV and 10 mV. In order minimize charging effects of parasitic capacities during the measurements, an initial hold-time of 5 s as well as a 250 ms delay-time between the measurement points were set. To investigate the influence of the sweep direction of the gate-voltage, double sweeps were conducted to examine the hysteresis effects due to charge carrier trapping. Ultra-short Ge channels show a transport through a discrete number of sub-bands, observable by a step-like increase of the conductance for sweeping the gate-voltage. Thus, the conductance $G = I/V$ was directly obtained from transfer measurements and plotted in units of the fundamental conductance G_0 as a function of the gate voltage.

3.4 Low-temperature setup

In addition to measurements at room-temperature, a detailed analysis of the transport effects of ultra-scaled Ge quantum dots requires low-temperature measurements to ensure stable measurement conditions as well as to reduce noise due to thermal fluctuations and charge carrier trapping related effects. Further, cryogenic measurements enable to investigate the origins of electrical transport effects. Measurements in the temperature range between 5 K and 300 K were performed in a continuous flow liquid ^{4}He cryostat (Cryo Industries CRC-102). To prevent damaging the devices by freezing, the measurement chamber of the cryostat was evacuated at a pressure of approximately 2.5×10^{-5} mbar. For temperature monitoring, the cryostat features a highly accurate sensor located in the immediate vicinity of the sample holder. The measurement temperatures were adjusted using a "Cryo Con 32B temperature controller". To ensure a proper thermalization of the sample, a hold time of 10 min was set before the measurements were executed. For the low-temperature transport measurements, the sample configuration schematically shown in figure 3.3 was used. To investigate low-temperature transport effects such as superconductivity, Coulomb blockade and the Josephson field-effect, it was also necessary to conduct measurements in the temperature range between 300 mK and 2 K. This was accom-

plished using a pumped ^{3}He cryostat (Institute Neel, CNRS Grenoble).[105] As low temperature transport effects are very sensitive to noise, π-filters and thermal coax lines of approximately 1 m length were put in series with the sample. The resistance of the setup was independently measured to be 370 Ω at 400 mK. The cryostat first cools down to approximately 4.5 K using a continuous flow of ^{4}He. As the boiling temperature of a liquid is a function of its vapor pressure, the temperature was further lowed to approximately 1 K by pumping ^{4}He through the cryostat. To achieve even lower temperatures, a sorption pump was used to direct ^{4}He from the main bath through a heat exchanger. A schematic illustration of the working principle of the sorption pumped ^{3}He cryostat is shown in figure 3.4. The flow rate of ^{4}He is controlled by a valve in the pumping line. An additional vessel (1 K pot) filled with ^{4}He from the main bath, operated by a needle valve, is used to condense ^{3}He gas. During condensation, the sorption pump is warmed above 40 K. As at this temperature ^{3}He can not be absorbed anymore, the ^{3}He condenses on the 1-K pot and cools down the sample holder to approximately 1.2 K (see figure 3.4(a)). After the condensation the needle valve of the 1-K pot is closed. Next, the sorption pump is cooled, which reduces the vapor pressure of the ^{3}He, resulting in a further decrease of the sample holder temperature to approximately 300 mK (see figure 3.4(a)).[106, 107]

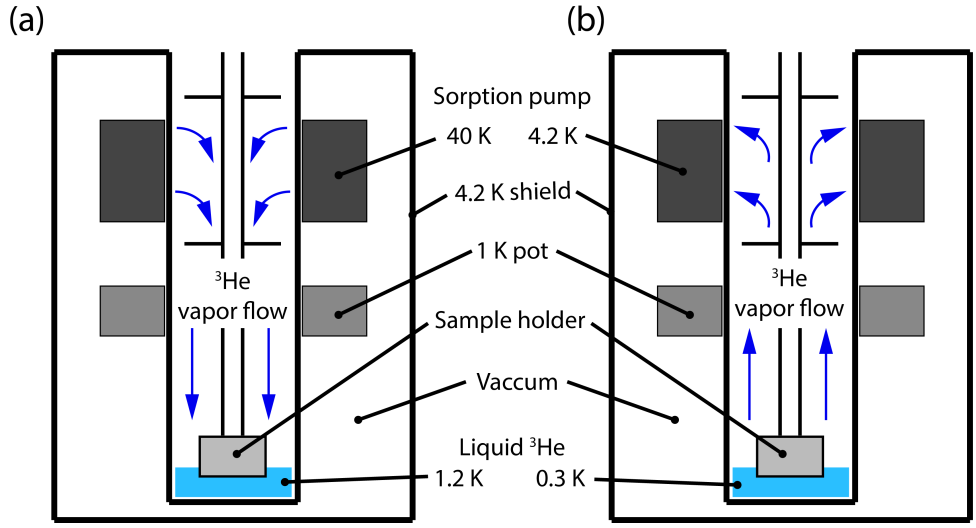

Figure 3.4: *Schematic illustration of a sorption pumped ^{3}He cryostat: (a) Condensing of ^{3}He on the 1 K pot to cool the sample down to* 1.2 K*, (b) Cooling of the sorption pump to reach the base temperature. The schematic is based on [106].*

Chapter 4

Results and discussion

In this chapter, the experimental results regarding the controlled formation of Al-Ge-Al NW heterostructures comprising ultra-short Ge segments are discussed. HRTEM and EDX investigations proved the composition and perfect crystallinity of these ultra-scaled metal-semiconductor NW heterostructures. Prior to the actual discussion of transport effects in ultra-scaled Ge channels embedded in Al-Ge-Al NW heterostructures, the charge carrier injection barriers of passivated and unpassivated heterostructure devices are addressed with a special focus on the influence of surface traps on charge carrier transport. Based on this systematic analysis, measurements conducted in the temperature range between 400 mK and 300 K, the experimental observation of quantum ballistic transport, single-hole tunneling and superconductivity induced in ultra-scaled Ge channels are addressed.

4.1 Al-Ge-Al nanowire heterostructures

4.1.1 Structural analysis by TEM and EDX

As described in section 3.1, the annealing of Ge NWs contacted by Al pads results in monolithic Al-Ge-Al NW heterostructures comprising Ge segments contacted to self-aligned, quasi-1D, crystalline Al leads.
Most notably, this fabrication scheme enables to apply consecutive annealing steps to tune the Ge channel length (L_{Ge}) beyond lithographic limitations (see section 4.1.2). Although, in contrast to common short channel devices, the 1D monolithic metal-semiconductor-metal architecture effectively prevents screening of the gate electric field by lithographically defined contacts[34] and thus enables perfect electrostatic control of field effect devices, Al-Ge-Al NW heterostructures with Ge segments below 10 nm showed no response anymore to the applied back-gate voltages. With respect to this problem, the heterostructure formation process was tuned to fabricate devices with large lithographic contact gap und Ge segments in the range between 15 nm and 40 nm. The thermally induced diffusion of Al in Ge NWs is discussed in section 2.3.2. A schematic illustration of the Al-Ge-Al NW heterostructure enwrapped in a 20 nm Al_2O_3-shell and integrated in a back-gated field-effect transistor architecture is shown in figure 4.1(a). To investigate the crystal structure as well as the Al-Ge interface of the heterostructure devices TEM samples were prepared as described in section 3.2. A detailed view of an Al-Ge-Al NW heterostructure integrated into the measurement module is depicted in figure 4.1(b). The HAADF STEM image shows a heterostructure device with a 220 nm long Ge segment connected to Al contact pads. Further, a compilation of HAADF STEM images showing Al-Ge-Al NW heterostructures with different Ge segments lengths between 15 nm and 600 nm is depicted in figure 4.1(c).

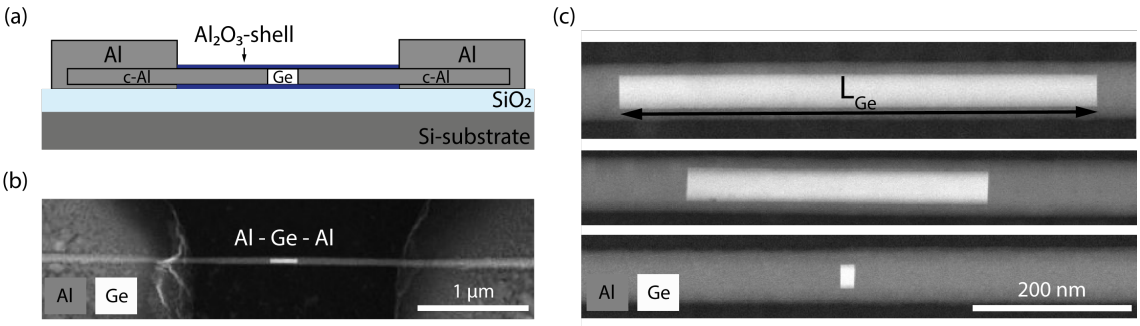

Figure 4.1: *Al-Ge-Al NW heterostructures:*
(a) Schematic illustration showing the completed Al-Ge-Al NW heterostructure integrated in a back-gated field-effect transistor architecture. (b) HAADF STEM of an actual heterostructure device with a channel length of $L_{Ge} = 220\,\text{nm}$. *(c) Zoomed-in HAADF STEM images showing Al-Ge-Al heterostructures with different Ge channel lengths of* $L_{Ge} = 600\,\text{nm}, 270\,\text{nm}$ *and* $15\,\text{nm}$.

To discuss the structural properties of ultra-short Ge segments, figure 4.2 shows further HRTEM and EDX images of an Al-Ge-Al NW heterostructure with a 15 nm long Ge channel. An overview HAADF STEM image of the heterostructure device with indicated Al_2O_3-shell is shown in figure 4.2(a). Further, a zoom-in HAADF STEM at the left Al-Ge interface oriented along the [110] direction of observation of the Ge crystal is shown in figure 4.2(b). As the contrast in the HAADF STEM image is related to both the sample thickness and the mean atomic number, thicker regions and/or those with a higher atomic number scatter more electrons on the annular detector and appear brighter. Since the diameter of the VLS grown Ge NWs is quite uniform, even after the exchange reaction with Al, the darker segment extending from the Al contact pads corresponds to the Al substituted part and the brighter segment to the unreacted Ge NW part.[37] The metal-semiconductor interface appeared to be abrupt and defect-free. The Ge lattice oriented along the [110] direction can be clearly observed in the right part of figure 4.2(b). On the left side, a crystalline Al part is observed, but in this NW the Al part is not oriented along the same crystallographic direction as Ge and therefore the lattice is not visible. In general, looking at many of such NWs not a single epitaxial relationship between the Ge and Al part was found.[36] Further, figure 4.2(c) shows the corresponding Fourier Transformation (FT) of the image shown in figure 4.2(b) with indexed reflections in the Ge crystal, indicating the (111) reflection both in the Ge and c-Al part. In good agreement with tabulated literature values, the FT shows the <111> growth plane

in the Ge diamond cubic structure with a lattice spacing of 0.33 nm.[108] Further, the extra peak indicated by the left arrow shows the presence of a family of planes with a smaller lattice spacing of around 0.23 nm, which is in good agreement with the theoretical interplanar spacing of Al face center cubic for <111> planes.[109] The Al [111] plane is observed to be parallel to the Ge (111) growth plane, while the perpendicular reflection $(2\bar{2}0)$ is only visible in the Ge crystal, indicating that the Al crystal is not seen along the same direction. Indeed, the Al crystal is rotated by approximately 6° around the NW axis with respect to the Ge crystal (image not shown) in this NW heterostructure. The interface appears to be very abrupt, regardless of the large lattice mismatch between Al and Ge. No crystal defects are observed along the interface. To confirm the composition of the heterostructure device, EDX maps were recorded in STEM mode in the vicinity of the ultra-short Ge segment. The EDX maps in figure 4.2(d-f) confirm that the reacted part (blue) of the NW is pure c-Al, while the unreacted part (yellow) is pure Ge. In good agreement with previous findings, a very low Ge concentration of a few atomic percent was detected, which should correspond to a very thin (2 nm or less) radial shell around an Al core.[35, 36] Moreover, detailed in-situ investigations of the thermally induced diffusion of Al in Ge NWs has shown, that a substitution of Ge by Al rather than the formation of new phases is dominating the diffusion process in the investigated Al-Ge material system.[36] Most notably, it was shown that the exemplary selective replacement of Ge by Al in Ge-Si core-shell NWs represents a general approach for the elaboration of radial and axial metal-semiconductor heterostructures in various Ge-semiconductor heterostructures.[37]

4.1.2 Formation of ultra-short Ge channels

To actually fabricate ultra-short Ge channels embedded in Al-Ge-Al NW heterostructures, consecutive annealing cycles were applied to tune the Ge channel length below L_{MFP}. For some heterostructure devices a sequence of more than 10 annealing cycles were applied. It was found that there is no correlation between the number of annealing steps and a degraded electrical characteristic of the heterostructure devices. However, in case every annealing cycle is followed by SEM observations, carbon deposition and charging of high-energetic traps due to the interaction of the

electron beam with the Ge segment, was observed to alter the electrical characteristic of the heterostructure devices.[110] The negative influence of these effects was also supported by in-situ observations of Al diffusion in Ge NWs using SEM. Hence, the diffusion rates for an annealing temperature of $T = 624\,\mathrm{K}$ were systematically investigated and analyzed to reduce the number of annealing cycles.

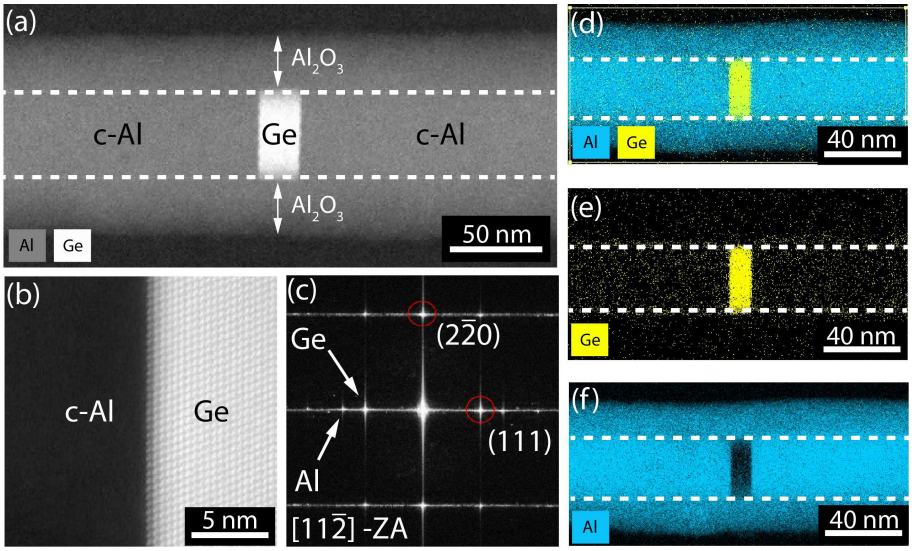

Figure 4.2: *Structural analysis of Al-Ge-Al heterostructures: (a) HAADF STEM image of an Al-Ge-Al NW heterostructure with an ultra-scaled Ge segment. (b) FFT patter showing (111) planes in both Al and Ge parts with spacings of* 0.23 nm *and* 0.33 nm*, respectively. (c) High-resolution HAADF STEM images recorded at the Al-Ge interface. (d-f) EDX mappings of the Al-Ge-Al NW heterostructure.*

Figure 4.3 shows the evaluation of the experimentally determined diffusion rates for annealing times between $t = 15\,\mathrm{s}$ and $150\,\mathrm{s}$ for Ge NWs with approximately 25 nm diameter all-around passivated with a 20 nm thick Al_2O_3 shell. The annealing procedure was executed in two steps. First, depending on the contact-gap of the lithographically defined Al contacts, annealing times between $t = 180\,\mathrm{s}$ and $120\,\mathrm{s}$ were used. In the second step, the Ge channel length of the devices were tuned applying a sequence of annealing cycles between $t = 15\,\mathrm{s}$ and $50\,\mathrm{s}$. As can be seen, for $t = 180\,\mathrm{s}$, $150\,\mathrm{s}$ or $120\,\mathrm{s}$, the variation of diffusion rates is much larger compared to the smaller annealing times. The origin of this effect was investigated using in-situ TEM investigations of the diffusion process.[36] It was observed that the quality of the material contact between the Al metalization and the Ge NW, has

a significant influence on the start of the diffusion process. After this individual starting phase, the diffusion rate of Al in Ge appeared to be relatively stable.[36] To further illustrate the capability of consecutive annealing steps in order to obtain ultra-scaled Ge channel lengths beyond lithographic limitations, an example for the down-scaling of the Ge channel length of an Al-Ge-Al NW heterostructure is shown in the inset. For the actual heterostructure device, the first annealing time was set to $t = 180\,\mathrm{s}$ to obtain a Ge channel length of 50 nm. Two subsequent annealing cycles for $t = 30\,\mathrm{s}$ and 15 s resulted in Ge channel lengths of 25 nm and 15 nm respectively.

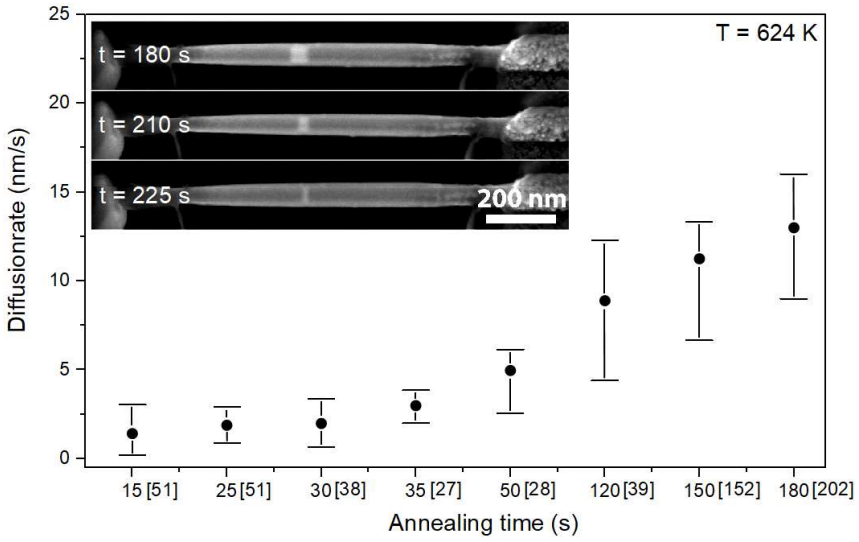

Figure 4.3: *Diffusion rates for annealing at* $T = 624\,\mathrm{K}$*:*
The diagram shows the experimentally determined diffusion rates for annealing times between $t = 15\,\mathrm{s}$ *and* 180 s *for Ge NWs with approximately* 25 nm *diameter, all-around passivated with a* 20 nm *thick* Al_2O_3 *shell. The mean diffusion rates for each temperature are indicated by black dots. The numbers in square brackets correspond to the number of investigated devices. The inset shows an example for tuning the Ge channel length of an Al-Ge-Al NW heterostructure by applying consecutive annealing steps for* $t = 180\,\mathrm{s}$, 30 s *and* 15 s*. The respective Ge segment lengths are* 50 nm, 25 nm *and* 15 nm*.*

4.2 Transport in ultra-scaled Ge channels

4.2.1 Al-Ge Schottky contact

Al-Ge junctions are known to form Schottky contacts exhibiting very strong Fermi-level pinning close to the valence band, regardless of the doping concentrations.[111–113] According to simulations of the electric field distribution in Ge NWs by Kim et al.,[114] the importance of this effect is significantly increasing for thin NWs, where the depletion regions approach each other. In this context, the influence of the Al-Ge-Al NW heterostructure formation on the electrical characteristic of ultra-thin Ge NWs integrated in a back-gated FET architecture was investigated. Figure 4.4 shows a comparison of the I/V characteristic of a bare Ge NW with a diameter of 25 nm contacted by Al pads before and after the heterostructure formation.

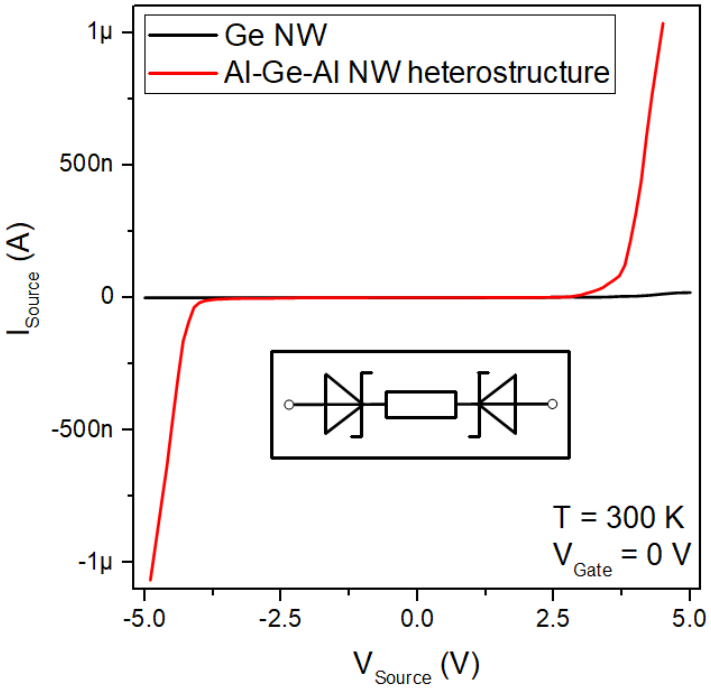

Figure 4.4: *I/V characterization of Ge NWs and Al-Ge-Al NW heterostructures: Comparison showing the I/Vs of a* 1500 nm *long bare Ge NW contacted by Al pads integrated in a back-gated FET architecture before (back) and after (red) thermally induced Al-Ge-Al NW heterostructure formation. Upon annealing the Ge channel length was reduced to* $L_{Ge} = 550\,\text{nm}$. *The data were recorded for* $V_{Gate} = 0\,\text{V}$ *at ambient conditions. The equivalent circuit diagram of Al-Ge-Al NW heterostructures is shown in the inset.*

The I/V measurement of the Ge NW device prior to the annealing procedure shows a strongly asymmetric I/V characteristic that indicates two different Schottky contacts. This could possibly be associated with a parasitic serial resistance originating from interface- or oxide-states located in a residual parasitic oxide-layer on the contact area between the Ge NW and the Al pads.[115]
Upon annealing, the Ge channel length of the heterostructure device was reduced from initially $L_{Ge} = 1500\,\text{nm}$ to 550 nm. This resulted a moderate decrease of the resistivity in the linear I/V regime of about 75 %, which we dedicate to a combined effect of the reduction of the Ge channel length and a change of the contact architecture from the Al pad atop of the Ge NW to a quasi 1D monolithic Al-Ge contact. Importantly, it was found that the applied thermally induced heterostructure formation contributed essentially to more reliable and reproducible Al-Ge contacts, which might be attributed to the absence of the aforementioned parasitic serial resistance. As the Ge channel of the Al-Ge-Al NW heterostructures is connected via two Schottky barriers, the observed characteristic of the annealed device can be explained based on two back-to-back Schottky diodes (see inset of figure 4.4) biased in reverse direction. Assuming thermionic emission, the room temperature Schottky barrier height of the Al-Ge interface was experimentally determined to be $\phi_B = 361\,\text{meV}$.[35] At low bias, the space-charge region of the diode is increasing, which results in low current levels and a linear I/V regime. As the bias is increasing, hot electrons release their energy gained from the electric field by creating electron-hole pairs, which are subsequently split by the increasing electric field. The continuation of this process with increasing bias voltages initiates an avalanche-like increase of the current causing the non-linear I/V behavior distinctive for impact ionization.[41]

4.2.2 Influence of surface traps

Prior to the actual discussion of transport effects in ultra-scaled Ge channels embedded in Al-Ge-Al NW heterostructures, it is mandatory to address the charge carrier injection barriers of passivated and unpassivated heterostructure devices. Considering to the unstable native oxide of Ge and the large surface-to-volume ratio of NWs, adsorbates and surface traps have a significant impact on the electrical characteristics of Ge NW based devices.[55, 57, 116] Thus, heterostructure devices passivated

with an all-around high-κ dielectric (20 nm Al_2O_3, see section 3.1) were explored based on the analysis of the I/V and transfer characteristics of various Al-Ge-Al NW heterostructures with different Ge segment lengths. In order to exemplary show the impact of a high quality passivation on the electrical properties of Al-Ge-Al NW heterostructures, figure 4.5 depicts a comparison of I/Vs for a $L_{Ge} = 77\,\text{nm}$ long, back-gated Ge NW heterostructure device at $V_{Gate} = 0\,\text{V}$ without (black) and with (red) a passivating shell. The drastic change of the electrical characteristics is due to a superposition of several effects, which are discussed below.[104]

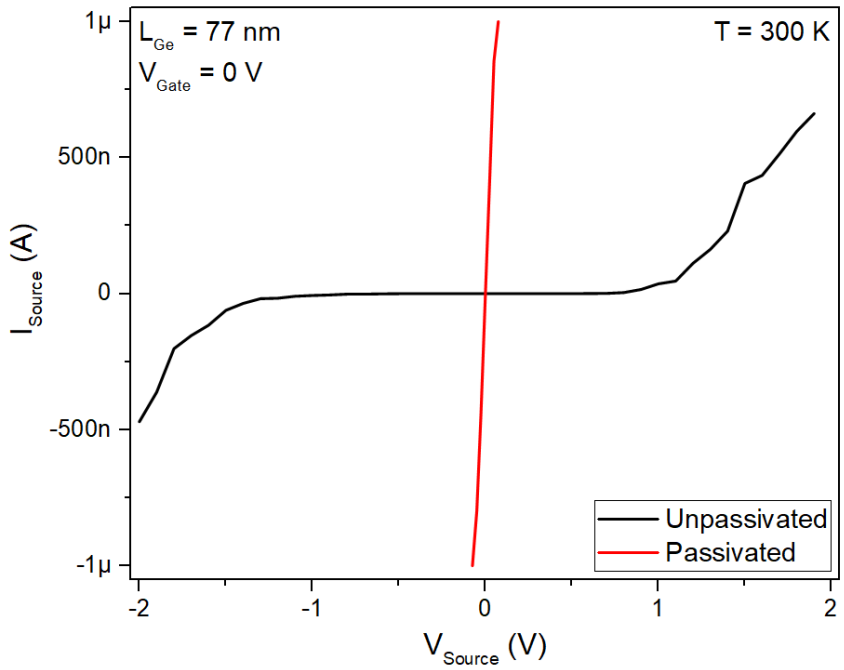

Figure 4.5: *Influence of a passivating Al_2O_3 – shell on the I/V characteristics: Comparison of I/V measurements for $V_{Gate} = 0\,\text{V}$ between an unpassivated (black) and a passivated Al-Ge-Al NW heterostructure (red) with a channel length of $L_{Ge} = 77\,\text{nm}$. The measurements were recorded at room-temperature and ambient conditions. Image adapted from [104].*

First, in accordance with the work of Korgel et al.[55], traps in the native oxide accumulate charges on the NW surface and interband trap levels, dominating the electrical characteristic and thus have a huge impact on the electrical transport phenomena. In equilibrium, trap states below the Fermi level are filled, while those above the Fermi level remain empty. As electrons are negatively charged, the channel

feels a "effective" negative gate, which results in the commonly observed p-type behavior of intentionally intrinsic Ge NWs.[117] By applying a negative gate-voltage, the conductivity is increased by an additional accumulation of holes, which discharge trapped charge carriers. However, as surface states in Ge can exhibit time constants up to several minutes, this is a rather slow process.[118] During the discharging process of the traps, the "effective" gate becomes more and more positive, due to less and less negative charges present at the surface. Hence, the current through the device is decaying exponentially over time. This transient behavior is shown in figure 4.6.[55]

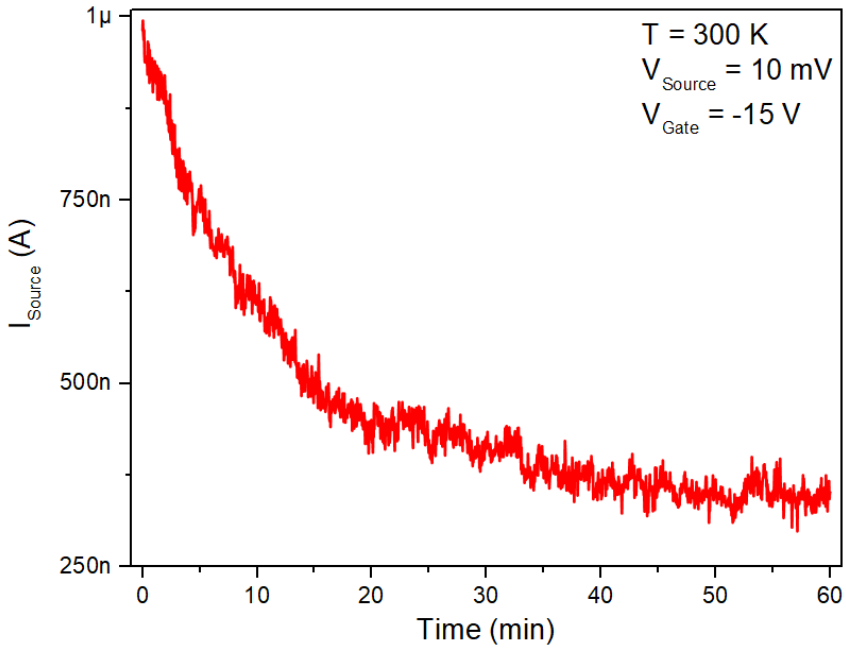

Figure 4.6: *Transient behavior of Al-Ge-Al NW heterostructures: Time dependence of the current of a passivated heterostructure device with a channel length of* $L_{Ge} = 150\,\text{nm}$ *for* $V_{Gate} = -15\,\text{V}$ *and a bias of* $V_{Source} = 10\,\text{mV}$*. The data were recorded at room-temperature and ambient conditions. Image adapted from [104].*

Further, it was shown that despite of the high-quality passivation, a GeO_x-shell will always be present at the Ge surface, due to the ALD process of growing the Al_2O_3-shell.[119] Consequently, due to a multi-exponential time dependence, indicating a significant spread in the spatial and energetic distribution of the surface trap states as well as kinetic limitation by either a diffusion barrier or a tunnel barrier at the NW surface, charging and discharging of trapped surface states will be present

in all transport measurements. It was further demonstrated that trap charging and neutralization prozesses in Ge are relatively slow processes.[55] Thus, the passivating Al_2O_3-shell only ensures reliable and reproducible measurements by avoiding any influence of adsorbates rather than eliminating charge trapping due to dangling bonds on the GeO_x/Ge interface. As can be seen in figure 4.6, for the actual device geometry and under the given experimental conditions, a steady state is reached after approximately 1 h of applying a V_{Gate} = -15 V and a bias of V_{Source} = 10 mV. This transient behavior has to be taken into account to achieve reliable transport measurements.[104] Further, with respect to hysteresis effects, the transfer characteristics of passivated and unpassivated Al-Ge-Al NW heterostructures were analyzed. The transfer characteristics in Figure 4.7 compares a bare Ge NW channel and one covered by an Al_2O_3-shell demonstrating the necessity of passivation layer to achieve reliable device characteristics.

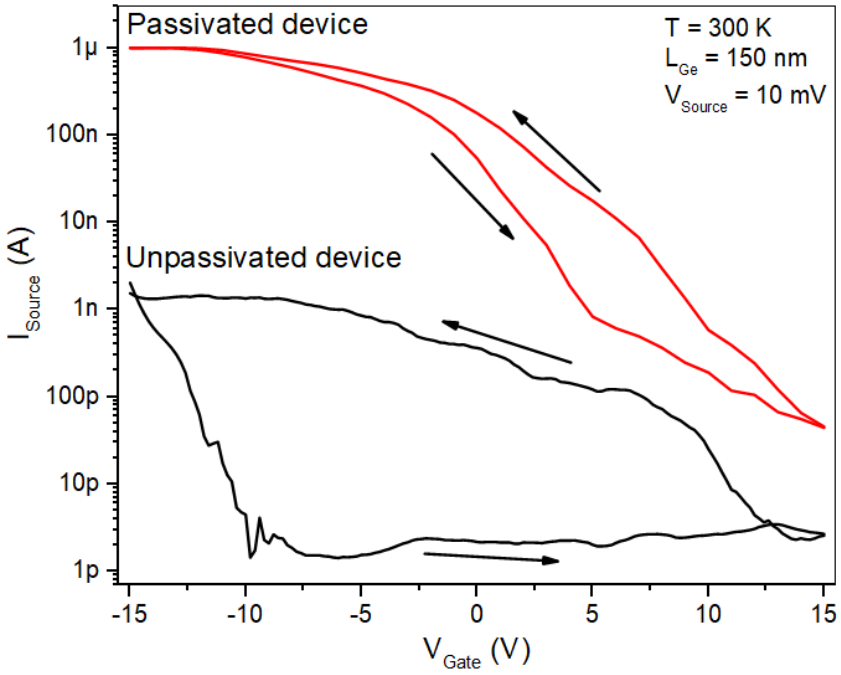

Figure 4.7: *Hysteresis effects of the transfer characteristics: Comparison of passivated and unpassivated heterostructure devices showing hysteresis effects. The measurements were recorded for back-gated FET devices with Ge segment lengths of L_{Ge} = 150 nm in the gate-voltage range between V_{Gate} = -15 V and 15 V for a bias of V_{Source} = 10 mV. The black arrows indicate the direction of measurement. The data were recorded at room-temperature and ambient conditions. Image adapted from [104].*

In agreement with previous reports,[116, 120] using a high-κ passivation layer results in less pronounced hysteresis effects. In addition, the ON-current and the I_{ON}/I_{OFF} ratio of the passivated Al-Ge-Al based FET devices increases by more than two orders of magnitude. Although intrinsic VLS-grown Ge NWs were used, the discussed negative surface charges accumulating in interband trap levels[55] contribute to an overall p-type behavior of the back-gated FET device for both the bare as well as the Al_2O_3 passivated NWs. Further, as adsorbates influence the electrical behavior of Ge-NW-based devices,[121, 122], it was mandatory to passivate the Ge NWs prior to the heterostructure formation to reduce interface traps and surface disorder,[123, 124] and thus ultimately gain the ability to investigate transport phenomena in ultra-scaled Ge quantum dots embedded in Al-Ge-Al NW heterostructures.

4.2.3 Ballistic transport

In a first experiment, two-terminal I/V measurements of Al-Ge-Al NW heterostructure devices with different Ge segment lengths were recorded at room-temperature and ambient conditions. Due to the unstable native Ge oxide shell around the Ge channel, the surface trap density at the GeO_x/Ge interface is not constant and additional charges originate at the surface due to the adsorption of various gases.[104, 117, 125] Therefore, the heterostructure devices were wrapped in a 20 nm thick Al_2O_3-shell, effectively passivating the surface. The measurement data shown in figure 4.8 reveal a clear transition from a nonlinear behavior to an almost linear characteristic with decreasing channel lengths.
In this context, it can be assumed that heterostructure devices with $L_{Ge} > 45\,\text{nm}$, due to two distinct back-to-back Schottky diodes operate in the space-charge limited current regime. Consequently, the current through the Ge channel is dominated by charge carrier injection from the contacts, with the I/V characteristic being quadratic ($\text{I} \approx \text{V}^2$).[41] As the L_{MFP} of Ge was calculated in section 2.4.1 to be approximately 37 nm, it can be assumed that the linear I/V-characteristic of the devices with $L_{Ge} < 45\,\text{nm}$ is a first indication for the shift from diffusive to ballistic transport. Thus, a part of the charge carriers start to travel ballistically through the channel without scattering.[104]

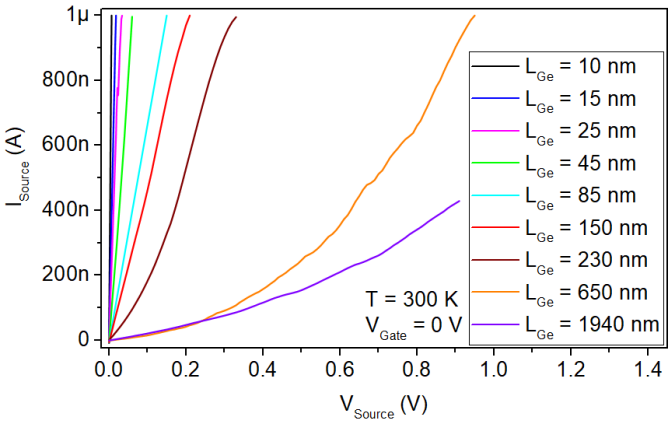

Figure 4.8: *I/V characterization of Al-Ge-Al NW heterostructures: Comparison of I/Vs of heterostructure devices with different Ge segment lengths integrated in back-gated FET devices. The data were recorded for $V_{Gate} = 0\,\mathrm{V}$ at room-temperature and ambient conditions. Image adapted from [104].*

For further interpretation of the data provided by the two terminal I/V measurements, the thereof calculated resistance as a function of Ge segment length normalized with respect to the NW cross-section was analyzed and displayed in figure 4.9. The resistance of long channel devices is directly proportional to the Ge segment length consistent with Ohm's law with a resistivity of $\rho = 0.75\,\Omega\,\mathrm{cm}$. This is also consistent with previously reported resistivities of nominally undoped Ge NWs.[55, 57] In contrast, heterostructure devices with $L_{Ge} < 45\,\mathrm{nm}$ reveal a resistance independent of the Ge segment length. As the diameter of all devices equaled the a_B^* of Ge, quantum confinement effects, resulting in band structure being composed of multiple 1D sub-bands can be assumed. Thus, for current transfer across the heterostructure, the current carried by continuous bands in the c-Al contact leads needs to be redistributed to a maximum of four 1D conductance channels inside the Ge segment (see section 2.4.2). However, as can be seen in the inset of figure 4.9, the resistance of heterostructure devices with ultra-scaled Ge channels, is approaching the fundamental contact resistance of $R_C = 12.9\,\mathrm{k}\Omega$. This suggests that under the given experimental conditions ($V_{Gate} = 0\,\mathrm{V}$) only one conductance channel can be accessed in the Ge segment.

The inset of figure 4.9 actually illustrates the modification of the transmission coefficient as a function of the channel length for the first conductance channel and suggests a L_{MFP} of approximately 45 nm at room temperature.[104]

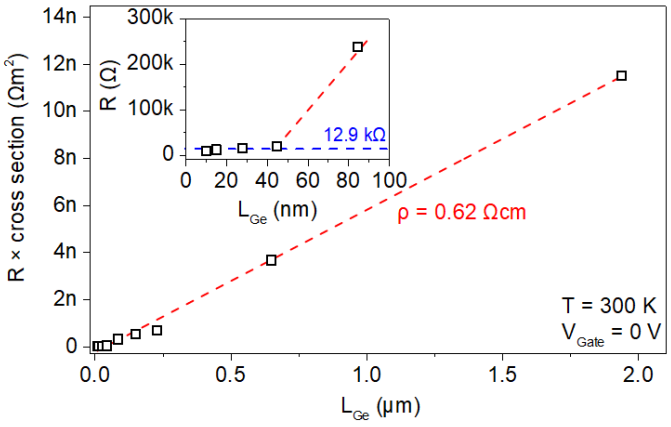

Figure 4.9: *Normalized resistance as a function of the Ge channel length: Calculated resistance as a function of Ge segment length normalized with respect to the NW cross-section. The inset shows an enlarged view of the resistance of heterostructure devices with $L_{Ge} < 100\,\text{nm}$. Image adapted from [104].*

4.2.4 Quantum ballistic transport

To provide further proof for quantum ballistic transport in Al-Ge-Al NW heterostructures with ultra-scaled Ge channels, the temperature dependency of the resistivity was investigated. This was done by performing two terminal I/V measurements at $V_G = 0\,\text{V}$ on heterostructure devices with different Ge segment lengths between 500 nm and 10 nm in the temperature range between 300 K and 5 K. The thereof calculated resistivity is plotted in figure 4.10. The resistivities were obtained according to section 3.3.1. As only two terminal measurements were conducted, the resistivity includes a series resistance originating from the c-Al leads of the heterostructures. To determine the influence of this series resistance, the resistivity of a 2 µm long and a diameter of 25 nm long c-Al NW was measured in two terminal configuration. Based on this measurement, a resistivity ρ_{c-Al} of 20 µΩ cm was calculated, which is approximately 7.5 times larger than the bulk value of Al.[126] This behavior is attributed to an increased influence of surface scattering in 1D nanostructures with dimensions approaching L_{MFP}.[79] Further, upon cooling, the resistivity of the c-Al NW is decreasing, which is associated with a decrease of phonon scattering at lower temperatures and is typical for a metal.[127] However, as the resistance of a c-Al NW is approximately three orders of magnitude smaller compared to ultra-short Ge

quantum dots, the parasitic resistance of the c-Al leads should be negligible. With respect to the calculated resistivity of the investigated Al-Ge-Al NW heterostructures, two different regimes were identified, depending on the Ge segment length. Firstly, indicating diffusive transport, the resistivity of heterostructure devices with $L_{Ge} > 45\,\text{nm}$ reveals a distinct temperature dependency. In such long Ge channels, the charge carriers travel a distance equal to the L_{MFP} in a ballistic manner. However, as the channel length exceeds L_{MFP}, scattering with phonons, crystal defects and impurities results in an added series resistance that increases with longer channel lengths. Thus, the distinct temperature dependence of long channel devices can be associated with a gradually freeze out of charge carriers, which is consistent with the behavior of intrinsic semiconductors where the resistivity is increasing with decreasing temperatures.[126, 128] Secondly, the resistivity of heterostructure device with $L_{Ge} \leq 45\,\text{nm}$ remains almost constant over the investigated temperature range. Such devices comprise a channel length that even at room temperature is smaller than L_{MFP}. Thus, there is no scattering related series resistance and the charge carriers can traverse through the entire Ge channel ballistically. Consequently, there is no temperature dependence of the resistivity anymore.

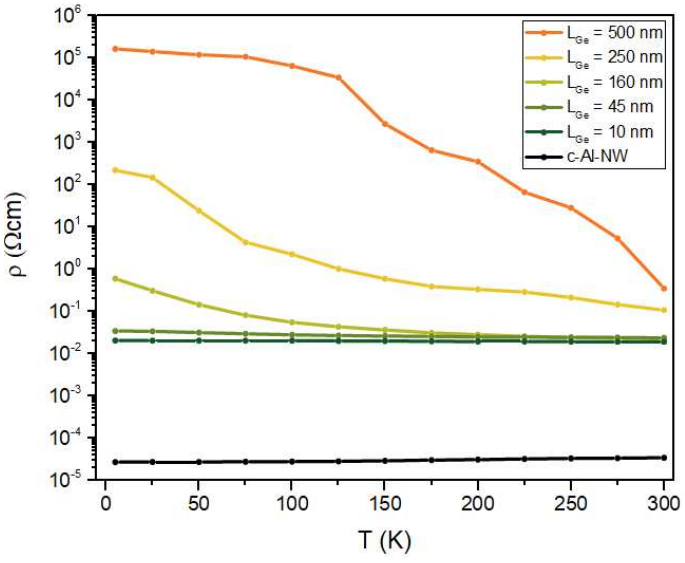

Figure 4.10: *Temperature dependence of the resistivity of Al-Ge-Al NW heterostructures: Comparison between heterostructure devices with different Ge segment lengths with a c-Al NW in the temperature range between* $T = 300\,\text{K}$ *and* $5\,\text{K}$.

To further discuss quantum ballistic transport in ultra-scaled Ge quantum dots embedded in Al-Ge-Al NW heterostructures, the modulation capability of the structures was determined by measuring the transfer characteristics of Al-Ge-Al NW heterostructures with a diameter of 30 nm depending on the Ge segment length.
The discussion is based on the comparison of the transfer characteristic of heterostructure devices with Ge channel lengths of 15 nm and 2000 nm integrated in back-gated FET architecture, shown in figure 4.11.
Considering the transfer characteristic of the device with the 2000 nm long Ge segment, applying a back-gate voltage, the Fermi level of the Ge NW can be effectively shifted. Consequently, the charge carrier concentration and therefore the conductivity in the channel can be modulated over more than four orders of magnitude. Thus, long channel devices reassemble the behavior of a Schottky barrier FETs.[129, 130] At $V_{Gate} = 0\,\mathrm{V}$ the channel is moderately p-type and the resulting current is consequently relatively low. By reducing V_{Gate}, the Fermi level is shifted towards the valence band, which increases the hole concentration, resulting in a higher current through the channel. In contrast, by increasing V_{Gate}, the Fermi energy approaches the band gap center and the conductivity decreases until a certain level, where the intrinsic Fermi level is reached. From there on, inversion takes place and the current starts to increase again as electron transport is dominating in this regime. This ambipolar behavior was only observed in heterostructure devices with $L_{Ge} > 1000\,\mathrm{nm}$ and is commonly observed in semiconductor NWs.[131] Although it was shown that passivating the Ge channel with an all-around Al_2O_3-shell increases the ON-current and the I_{ON}/I_{OFF} ratio, a distinct hysteresis is still observable in the transfer characteristic. These kinetic effects are mostly attributed to the high density of surface traps in the Ge channel.[104, 116]

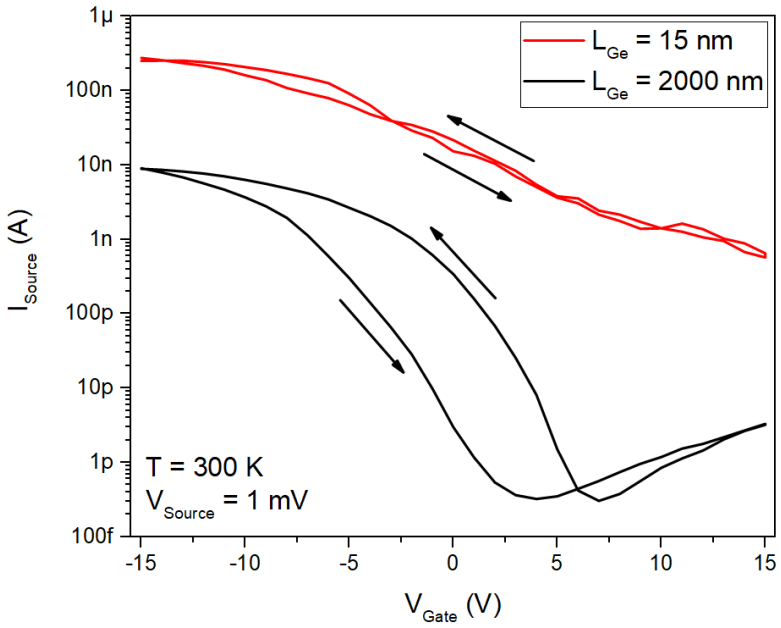

Figure 4.11: *Transfer characteristics of passivated Al-Ge-Al NW heterostructures: Comparison between heterostructure devices with* L_{Ge} = 15 nm *and* 2000 nm *integrated in back-gated FET devices showing the electrostatic control depending on the channel length and the respective hysteresis effects. The black arrows indicate the direction of the voltage sweep. The data were recorded for a bias voltage of* V_{Source} = 1 mV *at room-temperature and ambient conditions.*

Based on the transfer characteristics of the heterostructure device with only 15 nm channel length, the huge potential of Al-Ge-Al NW heterostructures with respect to gate-modulability is revealed. While the gate electric field of common back-gated short channel devices is often screened by large lithographically defined source/drain contacts, the quasi-1D contact leads of the monolithic metal-semiconductor-metal architectures enables a perfect electrostatic control of ultra-scaled channels.[132] Further, despite the surface to volume ratio is approximately a factor of two larger for the 15 nm Ge channel, compared to the 2000 nm Ge segment, the transfer characteristics of ultra-scaled Ge channel reveals a diminished hysteresis compared to the the long channel device. This should mostly be attributed to a lower number of surface traps present in ultra-scaled channels. Moreover, as L_{Ge} is smaller than the room-temperature L_{MFP} of Ge, there is no scattering related series resistance in the channel. Thus, the charge carriers can traverse through the entire Ge channel in a ballistic manner. Consequently, the ON-current of the heterostructure device with

15 nm channel length is more than one order of magnitude larger compared to the 2000 nm device. Thus, integrating Al-Ge-Al NW heterostructures as active channels in electrostatically gated field-effect transistor devices, should provide a platform for the systematic investigation of electrical transport mechanisms in ultra-scaled Ge quantum dots embedded in Al-Ge-Al NW heterostructures.

As already discussed, charge carrier trapping has to be taken into account in the investigation of quantum ballistic transport in ultra-scaled Ge quantum dots embedded in Al-Ge-Al NW heterostructures. Figure 4.12 exemplary shows a schematic illustration of the 1D dispersion relation $E(K)$ and respective density of states $D(E)$ of a Ge NW with a diameter close to a_B^*, for different trap filling levels. In such a system, quantum confinement results in a band structure being composed of multiple 1D sub-bands. In the model, the axis of the Ge NW is oriented along the x-direction. According to the quantum confinement in the $y-z$ direction, the respective dispersion relation for holes of such a quantum wire provokes the corresponding quantization of conductance,[133] with each 1D sub-band contributing a quantum unit of conductance of G_0.[25]

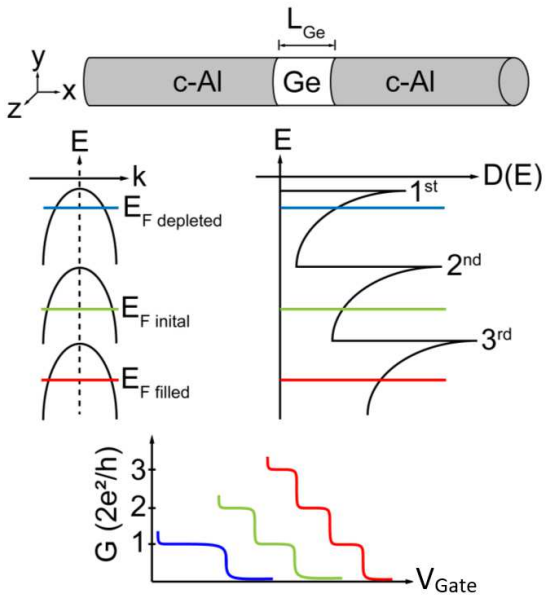

Figure 4.12: *Schematic illustration of the 1D dispersion relation and density of states: The Fermi level and the expected $G-V_{Gate}$ characteristics for NWs with filled and depleted surface traps are sketched. Image adapted from [104].*

To discuss the influence of charge carrier trapping on quantum ballistic transport, figure 4.13 shows the transient behavior of the conductance of three Al-Ge-Al NW heterostructure devices with Ge channel lengths of L_{Ge} = 15 nm, 45 nm and 150 nm recorded for applying a gate-voltage of V_{Gate} = -15 V and a bias voltage of V_{Source} = 1 mV. For the discussion of ballistic transport phenomena, the conductance was plotted in integer multiples of the quantum conductance G_0.

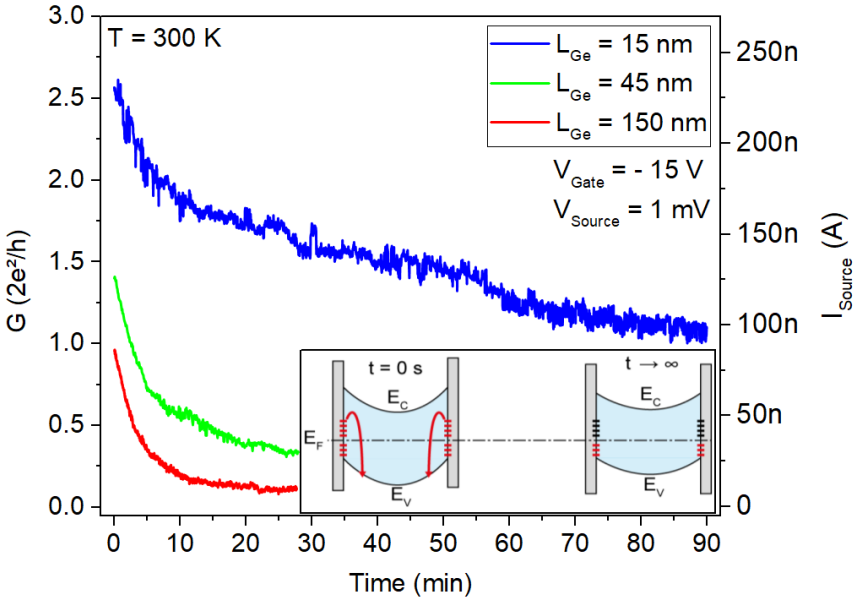

Figure 4.13: *Time-dependent $G - V_{Gate}$ behavior for Al-Ge-Al NW heterostructure devices with Ge channel lengths of L_{Ge} = 15 nm, 45 nm and 150 nm. All measurement data were recorded for a bias of V_{Source} = 1 mV and V_{Gate} = -15 V at T = 300 K in vacuum. The conductance was directly obtained from the measured current according to $G = I_{Source}/V_{Source}$. The inset provides schematic illustrations of band diagrams showing the discharging of traps due to an accumulation of holes by applying a negative V_{Gate}. Image adapted from [104].*

For the ballistic 15 nm long Ge channel, an initial conductance of 2.5 x G_0 indicates a redistribution of the current from the continuous bands of Al leads to two conductance channels inside the ultra-scaled Ge segment. This case would correspond to the Fermi level and $G - V_{Gate}$ characteristics that is schematically depicted by the green line in the schematic of figure 4.12. As for the whole experiment, the gate-voltage was kept constant at V_{Gate} = -15 V, the traps are continuously discharged resulting in less "effective" gating. This mechanism is schematically depicted in the

inset of figure 4.13. Finally, after approximately 80 min of trap depletion, the Fermi level adjusts close to the edge of the first conductance channel, schematically depicted by the blue line of figure 4.12. With respect to Al-Ge-Al NW heterostructures with longer Ge segments, in the steady state, the conductance level is decreased to approximately 0.25 x G_0. Representative for heterostructure devices with Ge channel lengths in the diffusive transport regime, the measurement of the $L_{Ge} = 150\,\text{nm}$ device revealed a conductance level that is further decreased below 0.1 x G_0. To further support the proposed model, figure 4.14(a) shows the transfer characteristics of a heterostructure device with a channel length of $L_{Ge} = 15\,\text{nm}$ for different trap filling levels at room-temperature and vacuum atmosphere.

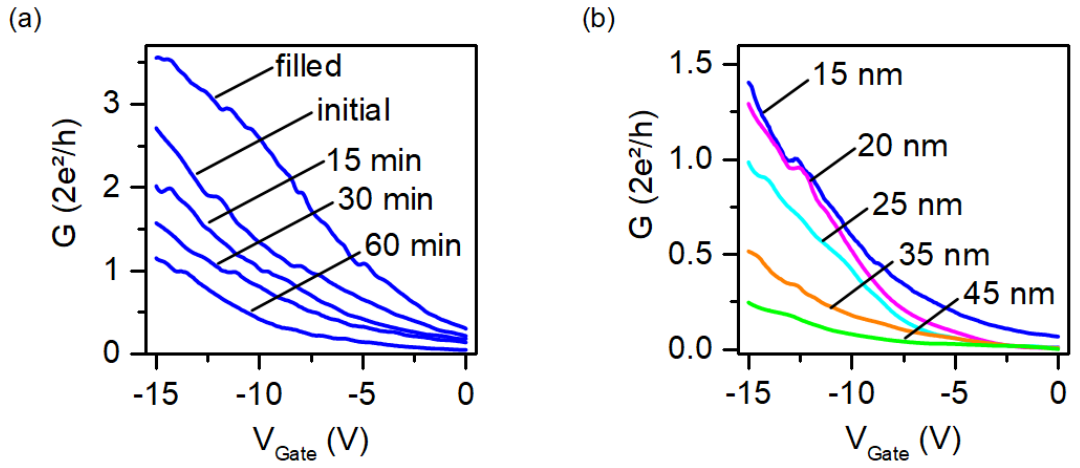

Figure 4.14: *$G - V_{Gate}$ characteristic for different trap-filling levels: (a) Fast $G-V_{Gate}$ measurements were performed after the given time intervals recorded for a heterostructure device with a* 15 nm *long Ge segment for V_{Gate} =* -15 V*. (b) Experimental $G - V_{Gate}$ behavior of Al-Ge-Al NW heterostructures with varying Ge segment lengths with depleted traps. All measurement data were recorded for V_{Source} = 1 mV at T =* 300 K *in vacuum. The conductance was directly obtained from the measured current $G = I_{Source}/V_{Source}$. Image adapted from [104].*

Initially, without any depletion or filling of the traps, sweeping V_{Gate} from 0 V to -15 V, two distinct step-like features are observed at 1 x and 2 x G_0. Due to the quantization of the density of states, each step is attributed to the population of a single spin-degenerated 1D sub-band. As the step-like features appear exactly at integer multiples of G_0, a negligible contact resistance can be assumed. Accordingly, the injection barriers also appeared to be negligible, indicating effective carrier injection

with hole tunneling at the sharp and high-quality Al-Ge interface.[25] However, with the gate voltage kept constant at V_{Gate} = -15 V, the traps are discharged, resulting in less effective gating. Thus, $G - V_{Gate}$ measurements conducted for different trap depletion times between 15 min and 60 min show that due to gradually trap depletion, the Fermi level shifts upward, and thus, only the first sub-band contributes to ballistic current transport. This is indicated by a step-like feature at G_0. In contrast, applying a positive gate voltage of V_{Gate} = 15 V, provokes the filling of traps below the Fermi energy, resulting in a more negative "effective" gate. This process continues until equilibrium is reached, having a higher number of trap states filled, which results in a Fermi level slightly below the edge of the third sub-band. The respective measurement showing the heterostructure operating with filled traps is shown by the curves labeled with "filled". According to step-like features in the $G - V_{Gate}$ characteristics at 1 x, 2 x and 3 x G_0 conductance quantization can be assumed. Consequently, the presented transient experiments show, that the Fermi level shifts with respect to the trap-filling level, and the conductance quantization persists.[104] To further investigate the influence of Ge channel length of ultra-scaled Al-Ge-Al NW heterostructures on quantum ballistic transport, figure 4.14 depicts a compilation of steady-state $G - V_{Gate}$ measurements of heterostructure devices with Ge segment lengths L_{Ge} between 15 nm and 45 nm with fully depleted traps. As can be seen, with increasing channel length, the G_0 conductance plateau is shifted to lower conductance, corresponding to an added series resistance due to an increasing number of scattering events. Investigations on numerous devices revealed that for heterostructure devices with Ge segment lengths above L_{Ge} = 45 nm, all signs of conductance quantization at room temperature vanish.[104]

In order to finally investigate conductance quantization, the $G - V_{Gate}$ behavior of heterostructure devices with diameters of approximately 25 nm close to a_B^* and Ge segment lengths between 15 nm and 35 nm were analyzed in the temperature range between 5 K and 300 K. Although conductance quantization up to room-temperature was observed in more than 10 Al-Ge-Al NW heterostructures with ultra-scaled Ge segment lengths, the following discussion is based on a heterostructure device comprising a 15 nm Ge channel. The respective measurement showing the the $G - V_{Gate}$ characteristic of the device for V_{Source} = 1 mV is depicted in figure 4.15. The measured $G - V_{Gate}$ characteristics show a distinct plateau-like feature

at G_0 over the entire temperature range, which is a clear indication for transport through individual spin degenerate 1D sub-bands in ultra-scaled Ge quantum dots up to room-temperature. This conductance plateau can even be better observed in the inset of figure 4.15, which shows the $G - V_{Gate}$ characteristic shifted in V_{Gate} for presentation clarity. Although trap induced surface disorder, blurring out the sub-band profile,[24] should be significantly reduced by using a passivating Al_2O_3-shell wrapped around the heterostructure device, this effect should have an impact on the overall size and shape of the measured conductance plateaus. Further, backscattering at the atomically sharp Al-Ge interface should be an intrinsic limitation of measuring conductance quantization in Al-Ge-Al NW heterostructures. This effect provides an explanation for the rounded appearance of the conductance plateaus.[79] In addition to the G_0-plateau a further conductance feature could clearly be observed at approximately 0.85 x G_0 up to a temperature of 200 K. The origin of this sub-G_0 conductance feature is assumed to be a result of spin effects.[133] All further observed plateau-like features are fading for higher temperatures above 5 K. Such conductance anomalies are assumed to be dedicated to tunneling resonances,[134] single-electron charging effects,[4] or geometric transmission resonances[135] arising from impurities. Moreover, due to the ballistic nature of the 15 nm Ge quantum dot, neither the overall conductance nor the steepness of the conduction plateaus changes with increasing temperatures.

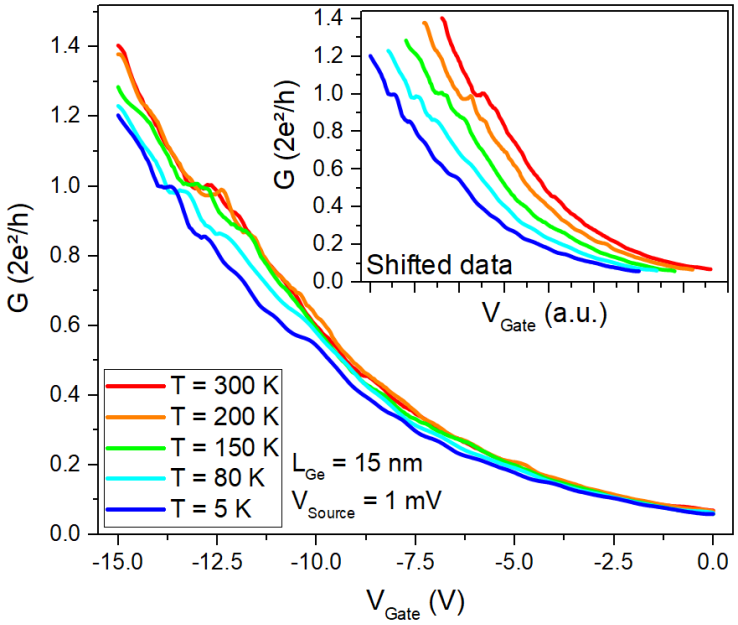

Figure 4.15: *$G - V_{Gate}$ characteristics of an ultra-scaled heterostructure device: Temperature dependent $G - V_{Gate}$ measurements of an Al-Ge-Al NW heterostructure with $L_{Ge} = 15\,\text{nm}$ for temperatures between $T = 5\,\text{K}$ and $300\,\text{K}$. The measurement was conducted for $V_{Source} = 1\,\text{mV}$. The inset shows the $G - V_{Gate}$ characteristics shifted in V_{Gate} for presentation clarity. Image adapted from [104].*

Although the $G - V_{Gate}$ characteristic provided first pronounced signs of quantum ballistic transport in ultra-scaled Ge dots, further investigations were necessary. As the total scattering matrix of a quantum ballistic system is depending on the exact location of impurities and boundary fluctuations, slightly different impurity configurations can have a huge impact on the conductance. Thus, despite the conductance of a quantum ballistic system in theory increases in G_0-steps (see section 2.4.2), sub-G_0 anomalies are possible.[79, 136] Consequently, bias spectroscopy measurements at a temperature of 70 K were conducted to investigate conductance quantization in a regime without trap induced surface disorder, blurring out the sub-band profile. The respective bias spectroscopy is shown in figure 4.16. The measurement is based on I/Vs recorded for different gate voltages. For analysis of the bias depending conductance quantization behavior, the bias spectroscopy shows curves corresponds to dI_{Source}/dV_{Source} versus V_{Source}. In the low-bias region, dense regions appear at integer multiples of G_0, which indicate quantized conductance plateaus consistent with individual spin degenerate 1D sub-bands. Thus, in this region the influence of

the gate voltage on dI_{Source}/dV_{Source} is negligible.[20] The second regime evolves for larger bias voltages and reveals an evolution of dI_{Source}/dV_{Source} from integers multiples of G_0 to intermediate values at $\pm$ 10 mV. Such half-plateaus arise when the chemical potentials of the source and drain occupy different sub-bands and were previously reported in various QPCs.[20, 137, 138] Additionally, the bias spectroscopy clearly revealed a conductance feature at approximately 0.7 x G_0, which is an intrinsic low-temperature sub-G_0 feature of mesoscopic systems. This conductance anomaly is assumed to originate from many-body physics and was the first conduction anomaly that turned out to be independent of the material system.[139–141] In conclusion, the bias spectroscopy revealed transport through single 1D-subbands even at room-temperature for ultra-scaled Ge quantum dots. Further, as all sub-G_0 conductance features observed in the $G - V_{Gate}$ characteristics, except for the 0.7 x G_0 anomaly, were absent in the bias spectroscopy their origin is most likely dedicated to charging-effects induced by the gate-voltage sweep.[104]

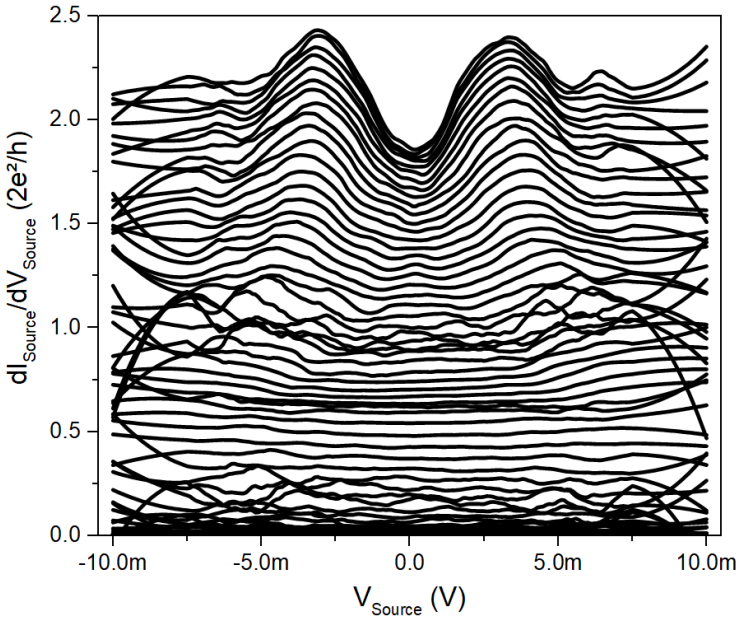

Figure 4.16: *Bias spectroscopy of an ultra-scaled heterostructure device: Differential conductance $dI_{Source}I/dV_{Source}$ showing the 1D sub-band structure for an Al-Ge-Al NW heterostructure with L_{Ge} = 15 nm at a temperature of T = 70 K. The dI_{Source}/dV_{Source} values were directly obtained from I/V measurements at different gate-voltages and is plotted in units of G_0. Image adapted from [104].*

4.2.5 Quantum ballistic photo-detection

The extraordinary high photo-sensitivity of Ge NWs [142] motivates the investigation of ultra-high gain quantum ballistic Ge photo-detectors potentially paving the way towards advanced photo-electric devices with quasi-zero off-state current and high spatial resolution, which are fully compatible with today's CMOS technology. Such a device was investigated by illuminating the quantum ballistic Ge channel of an Al-Ge-Al NW heterostructure integrated into a back-gated FET architecture, using a focused green laser exciting at $\lambda_{ex} = 532\,\text{nm}$. The experimentally obtained room-temperature $G - V_{Gate}$ characteristics of a heterostructure device with a Ge channel length of only $L_{Ge} = 18\,\text{nm}$ is shown in figure 4.17.

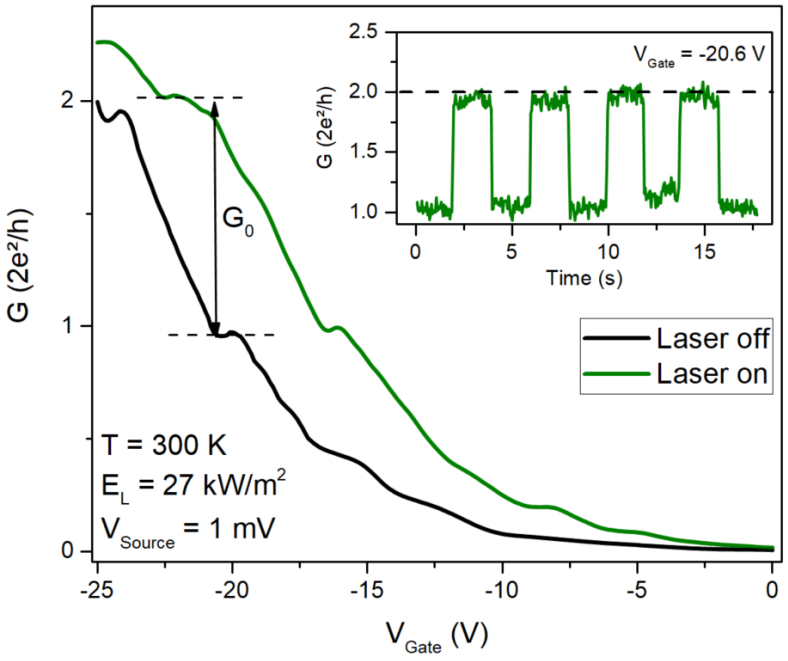

Figure 4.17: *Quantum ballistic photo-detection:*
$G - V_{Gate}$ characteristics of a heterostructure device with an Ge channel length of L_{Ge} = 18 nm without (black) and with (green) laser illumination (λ_{ex} = 532 nm, E_L = 27 kW m^{-2}, 30 µm spot size). The inset shows a time resolved measurement at V_{Gate} = -20.6 V and periodically switching the laser light on and off (λ_{ex} = 532 nm, E_L = 27 kW m^{-2}, 865 nm spot size) with a period of f_{mod} = 0.25 Hz. The conductance was directly obtained from the measured current according to $G = I_{Source}/V_{Source}$. All measurements were obtained at room-temperature and vacuum conditions. Image adapted from [143].

The black characteristics shows an increase of the conductance in integer multiples up to 2 x G_0 indicating quantum ballistic transport in the investigated gate-voltage range between $V_{Gate} = 0\,\mathrm{V}$ and -25 V. For exciting the heterostructure device with the laser, the green curve reveals a shift in the threshold voltage to a more positive gate voltage, preserving conductance quantization. As for the photo-conductive effect,[144] a constant current increase is expected, such a shift of the threshold voltage is emphasized to be a unique feature of the photo-gating effect.[143] The origin of this behavior is charge carrier trapping of photo-generated carriers, which enhances the sensitivity of field-effect based photo-detectors.[114, 145–147] Consequently, the device behavior implied, that under illumination, the current through the ultra-scaled Ge channel increases by opening an additional transfer channel, which effectively allows for controlling the sub-band population by light exposure. Thus, as can be seen in the inset of figure 4.17, for a particular back-gate voltage, the transmission via the second sub-band can be modulated, as the laser is switched on and off causing an effective quantization of the obtained photo-current. These investigations show, that the sensitivity of a photo-detector, operating in the quantum ballistic regime, significantly enhances through a high transconductance originating from the steep current increase in-between individual conductance plateaus. Remarkably, considering the spatial footprint of the sensing element of less than 500 nm^2, for the actual heterostructure device, a photo-conductive gain of approximately 2 x 10^4 was calculated.[143]

4.2.6 Single-hole tunneling

As the Ge channel of Al-Ge-Al nanowire heterostructures is defined by abrupt metal-semiconductor interfaces at sufficiently low temperatures, the system should reassemble a quantum dot isolated by the two Al-Ge Schottky tunnel barriers. Hence, the coupling strength between the Ge island and the Al leads should be tunable as function of the gate-voltage. As the Ge channel behaves like a p-type semiconductor, the device should reassemble a singe-hole transistor (SHT). In order to investigate single-hole tunneling and Coulomb blockade effects in Al-Ge-Al heterostructures, more than 20 heterostructure devices with Ge channel lengths between 40 nm and 800 nm with diameters of approximately 30 nm were investigated. In good agreement

with the work of Bjork et al.,[148] for heterostructure devices with Ge channel length below $L_{Ge} = 100\,\text{nm}$, the behavior changes from a SHT to a few-hole quantum dot. Associated with this transition, it was observed, that the reduced dimensionality of ultra-scaled Ge channels gives rise to pronounced resonant tunneling in ultra-scaled Ge channel devices. To describe the behavior of heterostructure devices with Ge channel lengths exceeding $L_{Ge} = 100\,\text{nm}$, figure 4.18 exemplary shows the stability diagram of a 160 nm long Ge channel embedded in an Al-Ge-Al NW heterostructure for temperatures between T = 420 mK and 10 K.

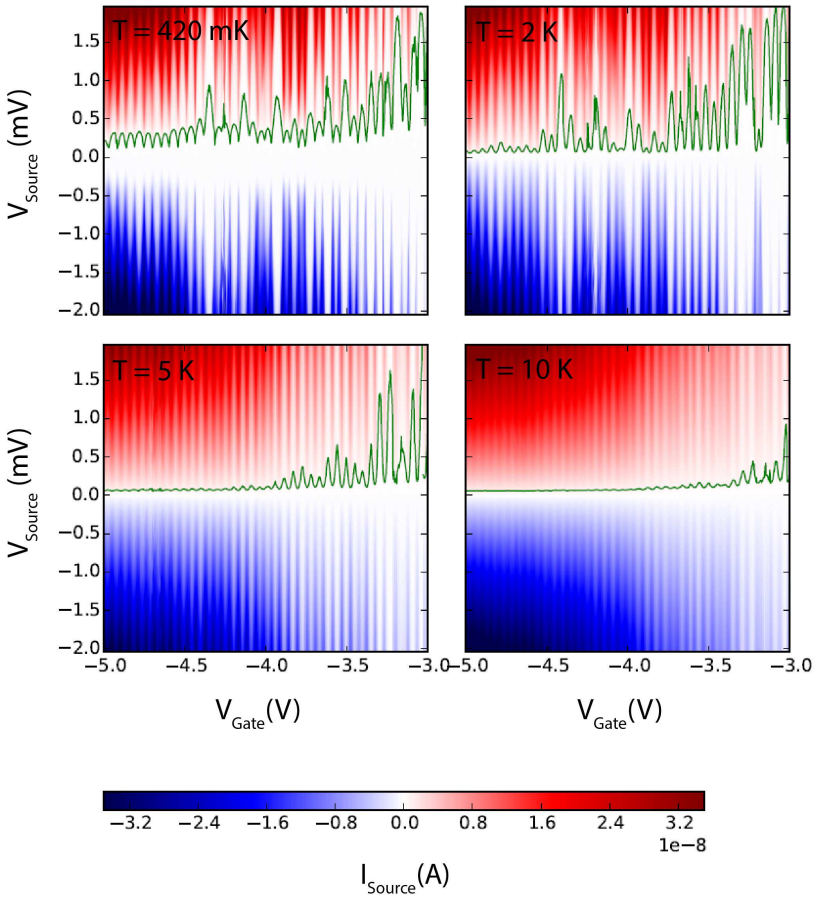

Figure 4.18: *Temperature dependency of Coulomb blockade effects:*
The stability diagrams show the measured source current as a function of the source and gate-voltage of an heterostructure device with an Ge channel length of $L_{Ge} = 160\,\text{nm}$ *recorded for temperatures between* $T = 420\,\text{mK}$ *and* $10\,\text{K}$. *Green lines are iso-current curves extracted from the stability diagrams for a source current of* $0.5\,\text{nA}$.

All stability diagrams show a clear evidence of Coulomb blockade, indicated by the appearance of diamond-like structures as the gate-voltage is swept. Thus, the Al-Ge-Al NW heterostructure can be interpreted as a SHT with the Ge segment modeled as a short semiconducting island connected via two tunnel junctions to two c-Al contact leads. For the measurement at a temperature of T = 420 mK, which is below the superconducting transition temperature of Al (T_c = 1.19 K[40]), the diamonds do not close at zero bias voltage, which is due to the superconducting gap of the c-Al leads. However, at all temperatures, the stability diagrams clearly show two different regimes.

First, between V_{Gate} = -5 V and -4.5 V, the height of the Coulomb diamonds is relatively constant with a stable charging energy of a single intrinsic quantum dot.

Second, as the gate-voltage is increased towards V_{Gate} = -3 V, a more complex stability diagram is observed revealing a large variation of the height of the Coulomb diamonds, that indicates a change of the source and drain capacitances with the gate-voltage.[34] In this regime, the charging energy is decreasing from E_C = 2.43 meV to 0.26 meV as V_{Gate} decreases. It is also observed, that the diamonds overlap with each other, which could be an indication for the formation of multiple islands along the length of the Ge segment.[34, 149] It is most likely, that this phenomenon is caused by defects and fluctuations of the potential in the NW environment, which create charge traps at the bottom of the Ge potential well. Thus, charge transfer from source to drain occurs by tunneling through a chain of islands rather than through a single quantum dot. This is supported by the observation of similar Coulomb oscillations in small semiconductor quantum dots[150] and SWCNT quantum dots,[151] where each peak height varies resulting in an non-uniform peak spacing.

To study the transition from a multi-dot regime to a single-dot system for all investigated temperatures, the iso-current curves showing the variation of the source-voltage as a function of the gate-voltage for constant current of 0.5 nA, were extracted and added to the respective stability diagrams. The iso-current curves reveal significant oscillations versus the gate-voltage with the same periodicity as the current or conductance peaks for a constant source-voltage. The amplitude of these oscillations versus the gate-voltage is correlated to the charging energy of the system. In the gate-voltage regime between V_{Gate} = -3 V and -4.5 V the oscillations show a significant beating that can be associated with an addition of multiple Coulomb

effects related to the different dots along the Ge segment. As can be seen, the amplitude of the beating of the oscillations in the single-dot regime are strongly reduced with increasing temperatures. Nevertheless, the Coulomb oscillations in the multi-dot regime around V_{Gate} = -3 V are still clearly visible up to T = 10 K. The absence of the multi-dot regime is correlated with more pronounced thermal fluctuations that significantly reduce the sensitivity of the system to corrugations at the bottom of the Ge channel potential.

To further discuss Coulomb blockade effects in ultra-scaled Ge channels, the following study is based on a heterostructure device with a 40 nm long Ge channel. The stability diagram of figure 4.19 obtained at T = 420 mK, clearly shows that for gate-voltages higher than V_{Gate} = -2.2 V, the Ge channel is completely pinched off and thus is in insulating state.

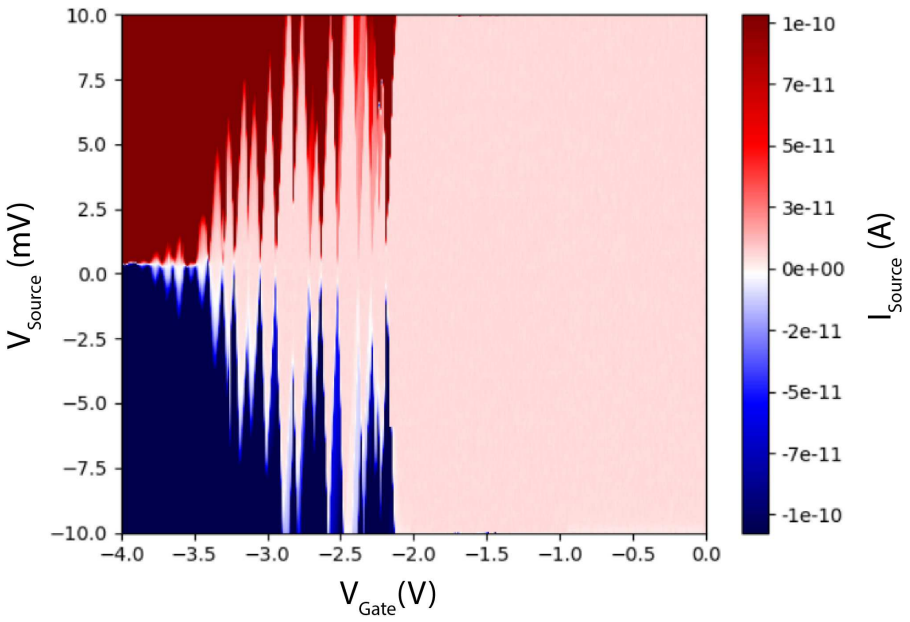

Figure 4.19: *Few-hole quantum dot regime:*
Stability diagram showing the measured source current versus the source voltage and the gate-voltage of an heterostructure device with L_{Ge} = 40 nm recorded at a temperature of T = 420 mK. While gate-voltages higher than V_{Gate} = -2.2 V result in an insulating state, the device clearly shows the characteristics of a few-hole quantum dot for more negative gate-voltages.

As the gate-voltage is becoming more negative, oscillations related to Coulomb blockade phenomena appear. As it was possible to resolve the insulating regime,

each of the shown Coulomb diamonds correspond to a further hole being added to the Ge quantum dot. For all heterostructure devices with $L_{Ge} < 200\,\text{nm}$, the diamonds were found to be distorted. A possible reason for this phenomenon could be offset charges associated with sudden changes in the electrostatic environment of the island, resulting in a gate-voltage offset.[21, 34, 148] Figure 4.20 shows a zoomed-in view of the Coulomb diamonds in the gate-voltage regime between V_{Gate} = -2.35 V and -3.1 V.

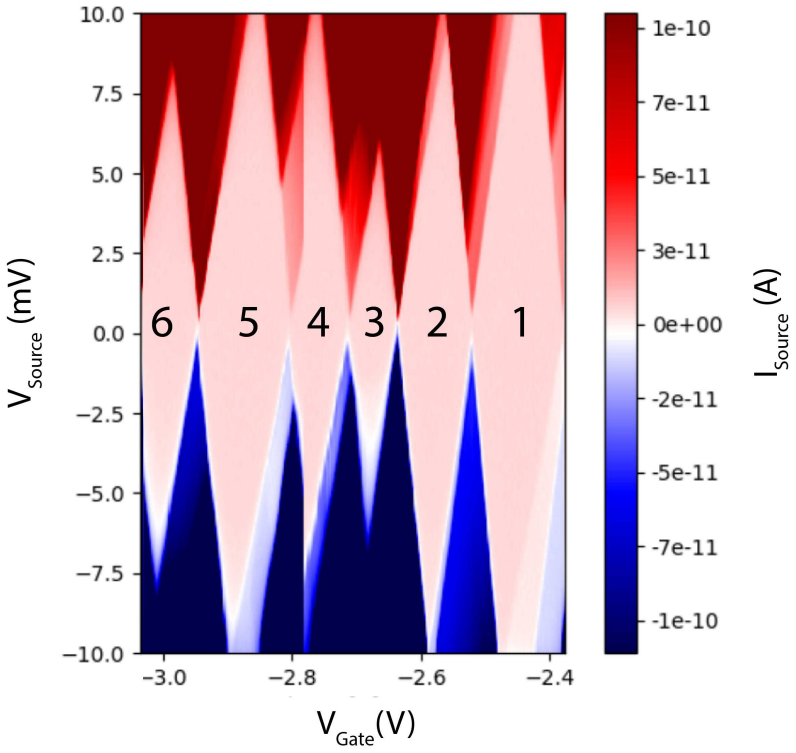

Figure 4.20: *Single-hole tunneling:*
Stability diagram showing a zoom-in at the gate-voltage regime between V_{Gate} = -2.35 V *and* -3.1 V *showing a sequence of Coulomb diamonds with varying heights. The number of holes on the quantum dot is indicated. The data were recorded at a temperature of* T = 420 mK.

The height difference of the Coulomb diamonds indicates a variation of the source and drain capacitances that influence the charging energy. However, as clearly shown in figure 4.19, the overall charging energy is decreasing as V_{Gate} becomes more negative. As discussed in section 2.4.3, modeling the Ge channel as a short metallic island connected via two tunnel junctions to two superconducting reservoirs allows

for the extraction of the capacitances of the system (C_{Source}, C_{Drain}, C_{Gate}) from the Coulomb diamonds. Applying a gate-voltage allows to shift the quasi Fermi level inside the Ge segment and thus change the electric charge of the quantum dot via capacitive coupling. From the periodicity of the diamonds as a function of the gate-voltage, the gate capacitance was calculated to be $C_{Gate} = 0.45\,\text{aF}$. Further, deduced from the slope of the Coulomb diamonds, the source and drain capacitances were extracted to be $C_{Source} \approx C_{Drain} = 2.2\,\text{aF}$. The charging energy of the first diamond was calculated to be $E_C = 16.5\,\text{meV}$. As the gate-voltage is getting more negative, the Ge well potential is becoming larger. Consequently, the tunnel barrier height is decreasing and becomes thinner. Hence, the conductance of the overall system rises and the Coulomb blockade oscillation disappears. This can be explained by a reduction of the height of the tunnel barrier of the Al-Ge arrangement, leading to an increase of the junction transparency. The charging energy of the last Coulomb diamonds was found to be as low as $E_C = 0.5\,\text{meV}$.

4.2.7 Josephson field-effect transistor

To study the superconducting proximity effect in ultra-scaled Ge quantum dots, the Al-Ge-Al NW heterostructure device with a channel length of $L_{Ge} = 40\,\text{nm}$ was again cooled below the superconducting transition temperature of the Al contacts ($T_c = 1.19\,\text{K}$).[40] In this temperature regime and considering the ultra-short Ge channel length of the heterostructure device, a sufficiently low gate-voltage should enable to tune the carrier concentration inside the Ge channel to enable an overlap of the wavefunctions of the Cooper pairs of the superconducting c-Al leads inside the Ge channel. This would allow an exchange of Cooper pairs between the superconducting c-Al leads mediated by superconducting proximity effect.[88]
Measurements of the differential resistance dV_{Source}/dI_{Source} revealed that passing through the quantum dot regime an intermediate coupling regime with moderate conductivity evolves, where transport is governed by the interplay between superconductivity and Coulomb interactions.[152, 153] A DC spectroscopy measurement showing the intermediate coupling regime in the gate-voltage range between V_{Gate} = -3.7 V and -5 V is supplied in figure 4.21. At the beginning of this regime at approximately V_{Gate} = -4 V, Coulomb diamond like conductance dips are surrounded

by conductance peaks, showing a height of approximately G_0. As the gate-voltage is becoming more and more negative, the charge carrier concentration in the Ge channel increases. Consequently, the coupling strength increases and the conductance dips are gradually disappearing. Finally, a further decrease of the gate-voltage forces the conductance dips to evolve to conductance peaks around $V_{Source} = 0\,\mathrm{V}$, marking a shift towards to the high coupling regime, where proximity induced superconductivity in the Ge channel is expected.

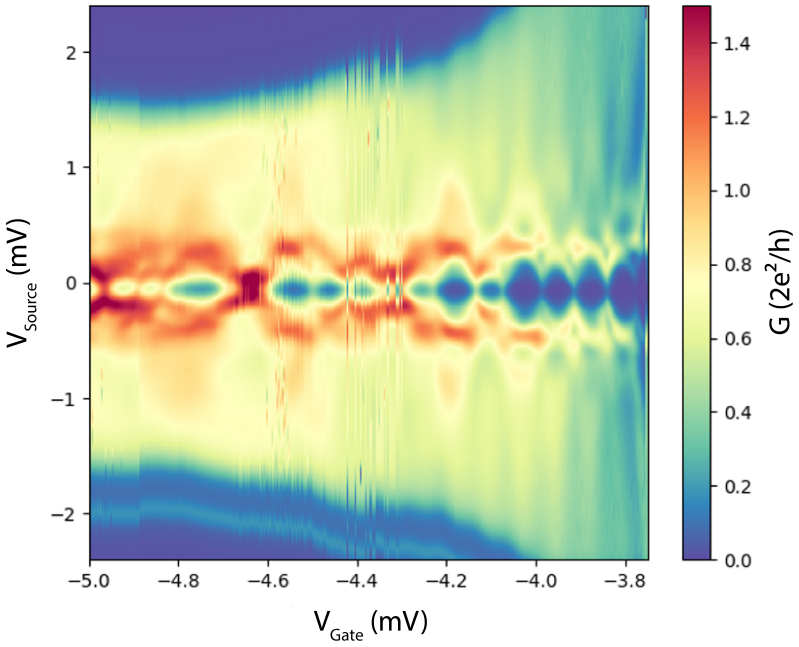

Figure 4.21: *DC spectroscopy of the Intermediate coupling regime: Differential conductance dI_{Source}/dV_{Source} for sweeping the source voltage between I_{Source} = -2.5 mV and 2.5 mV and measuring I_{Source} plotted in units of the quantum conductance versus V_{Source} and V_{Gate}. In this gate-voltage regime, a moderate conductance showing an interplay between superconductivity and Coulomb interactions was found. The data were recorded at a temperature of $T = 420\,\mathrm{mK}$.*

Further beyond V_{Gate} = -10 V, an increasingly negative gate-voltage results in a strongly decreasing resistance of the device. As can be seen in the DC spectroscopy shown in figure 4.22, with V_{Gate} = -10 V, the zero-bias resistance of the heterostructure device is dramatically dropping and finally vanishes completely, resulting in a clear dissipationless supercurrent observable in the Ge channel (blue). This is a clear indication for a gate-voltage mediated proximity effect enabling the tunnel-

ing of Cooper pairs across the Ge quantum dot.[20, 88, 154] The gate-dependent transport measurements revealed a tunable critical supercurrent in the Ge quantum dot from zero to approximately 20 nA at V_{Gate} = -30 V, significantly lower than the theoretical maximum $I_{c,max} = e\Delta/\hbar = 57$ nA.[101]

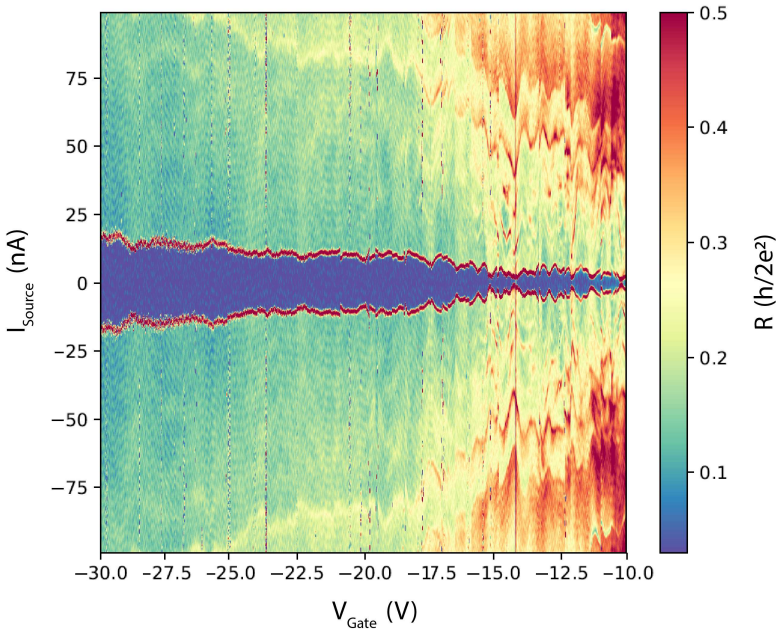

Figure 4.22: *DC spectroscopy of the superconducting regime: Differential resistance dV_{Source}/dI_{Source} for sweeping the source current between I_{Source} = -100 nA and 100 nA and measuring V_{Source} plotted in units of the quantum resistance versus I_{Source} and V_{Gate}. The blue regions correspond to zero resistance and indicate a gate-tunable critical current mediated by the superconducting proximity effect. The data were recorded at a temperature of T = 420 mK.*

To show the dependence of the critical current on the gate-induced electric field, figure 4.23, depicts the I/V characteristics of the heterostructure device for particular gate-voltages illustrating the ability to tune the critical current reassembling a JoFET. As the Ge channel shows the characteristics of a p-type semiconductor, a more negative gate-voltage increases the number of conductance channels contributing to current transport, resulting in higher critical current and an increased conductance in the normal state.[20] For currents exceeding I_C, the I/V curve abruptly switches to dissipative conduction with a finite slope indicating the normal resistance of the system to be R_N = 2.5 kΩ.

These results indicate, that the superconductive coupling strength of the system can be tuned with the change of the carrier density inside the Ge channel, providing an additional experimental knob not available in conventional superconductor-normal-superconductor junctions based on metallic weak links.[20, 155]

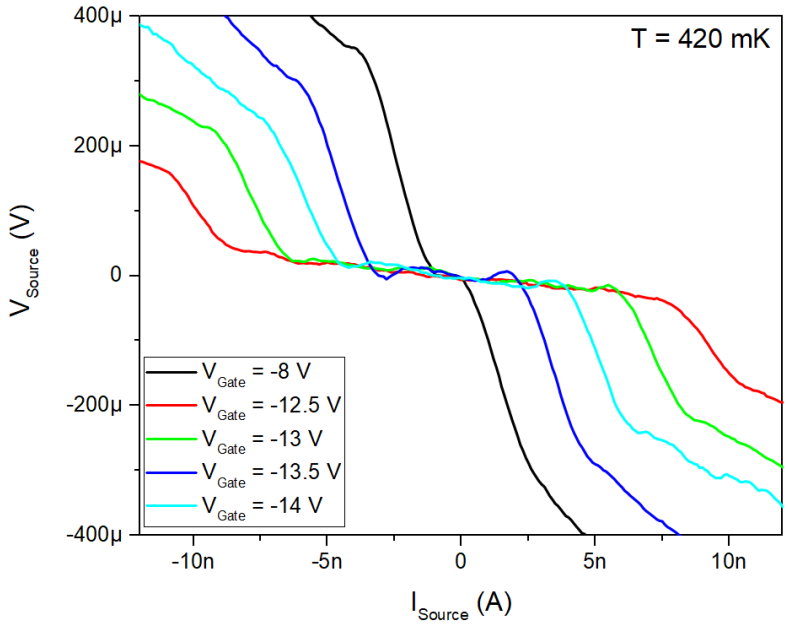

Figure 4.23: *I/V characteristic of a JoFET:*
I/Vs of a JoFET recorded for gate-voltages between V_{Gate} = -8 V *and* -14 V *revealing a gate-tunable critical current. The I/Vs were recorded by sweeping* I_{Source} *from positive to negative. The data were recorded at a temperature of* $T = 420\,\mathrm{mK}$.

To further investigate the exchange process of Cooper pairs across the Al-Ge-Al arrangement, figure 4.24 shows a map of the differential resistance measured for sweeping the source current between I_{Source} = -400 nA and 400 nA. This measurement enables to investigate the subharmonic energy-gap structure caused by MARs, which can be observed symmetrically around $V_{Source} = 0\,\mathrm{V}$ as a family of wavy lines visible at increased resistance in the dissipative state. These features arise from a progressive increase of the incident carrier energy as the carrier reflects between the two interfaces and thus mark Andreev channels present in in superconductor-normal-superconductor junctions for applying bias voltages below the superconducting gap. The lines occur for $V_{Source} = 2\Delta/n$, where n is integer denoting the MAR order. Using the BCS relation $\Delta = 1.76 k_B T_c$,[154] we calculated the superconducting gap

of the connecting c-Al leads to be 0.18 meV. Hence, within our measurement resolution and limits of thermal broadening considering the relatively high temperature close to T_c the measurement was recorded, n = 1,2,3 could be clearly and reproducible identified. As a point of reference, $n = 3$ indicates that a charge carrier gets 3 times reflected between the Al-Ge interfaces without being scattered inside the channel.[20] The clear observation of MARs over a wide gate-voltage range in Al-Ge-Al NW heterostructures with ultra-scaled Ge channels is a further experimental proof for the sharp defect-free Al-Ge interface of the devices and indicates a high junction transparency for highly negative gate-voltages. Although, traces of higher order MARs were found, the accurate identification of these highly sensitive superconducting features would most probably require to conduct transport measurements at even lower temperatures.

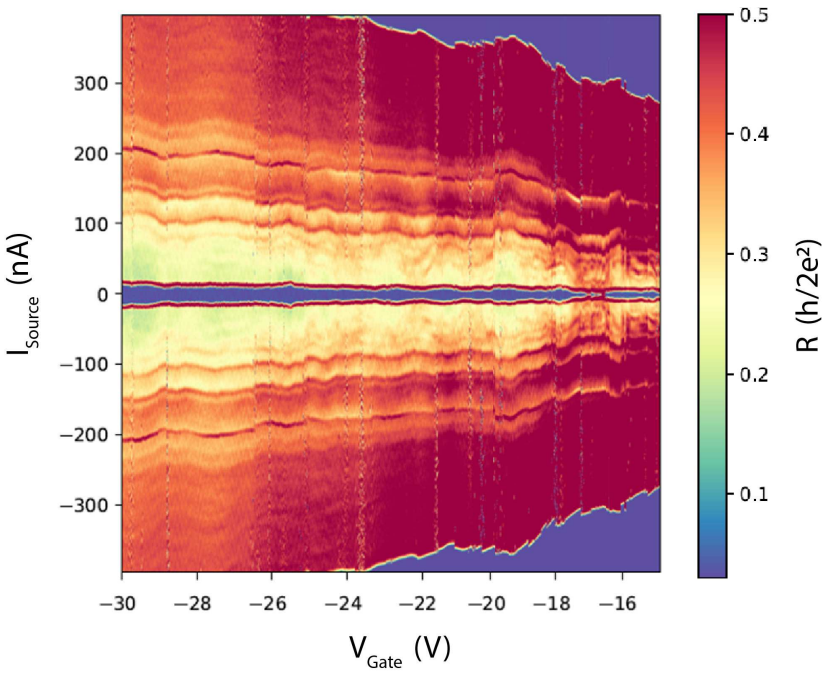

Figure 4.24: *DC spectroscopy measurement showing MARs: Differential resistance dV_{Source}/dI_{Source} for sweeping the source current between I_{Source} =* -400 nA *and* 400 nA *plotted in units of the quantum resistance versus I_{Source} and V_{Gate}. The blue regions correspond to zero resistance and indicate a gate-tunable critical current mediated by the superconducting proximity effect. The wavy pattern of lines present for the dissipative state indicates subharmonic energy-gap structures caused by MARs. The data were recorded at a temperature of T = 420 mK.*

Chapter 5

Summary and outlook

The thesis at hand provides a systematical investigation of the controlled formation and extensive electrical characterization of quasi-1D Ge channels embedded in axial Al-Ge-Al NW heterostructures, fabricated utilizing a thermally induced exchange reaction between single-crystalline Ge nanowires and Al pads. Applying this fabrication scheme, it was possible to form ultra-scaled Ge channels without lithographic constraints connected via self-aligned, quasi-1D, c-Al leads. To provide a platform for the systematic investigation of the electrical transport phenomena in ultra-scaled Ge segments, the Al-Ge-Al NW heterostructures were integrated as active channels in electrostatically gated FETs.

In order to elaborate a profound discussion on the transport in ultra-scaled Ge channels embedded in Al-Ge-Al NW heterostructures the first chapter provided a general introduction to transport phenomena in ultra-scaled Ge devices and the motivated their potential applications. The second chapter started with the fundamental physico-chemical parameters of Al and Ge, and discussed the general properties and applications of NWs. Further, theoretical aspects of NW synthesis techniques with a special focus on the VLS growth were given. Thereby, a special focus was set on the thermally induced diffusion of Al in Ge NWs to fabricate quasi-1D metallic leads to the Ge quantum dots. The last section of chapter two discussed the theoretical aspects of transport phenomena in ultra-scaled Ge quantum dots including

quantum ballistic transport, Coulomb blockade and the Josephson field-effect. The experimental methods for the fabrication and electrical characterization of Al-Ge-Al NW heterostructures were provided in the third chapter. Starting with the fabrication of a measurement module and the embedding of Ge NWs in a back-gated FET architecture a special focus was dedicated to the setups as well as the measurement procedures for conducting electrical measurements at room-temperature as well as cryogenic temperatures. In the last chapter, the experimental results regarding the formation of Al-Ge-Al NW heterostructures comprising ultra-short Ge segments were discussed. Based on HRTEM and EDX investigations the composition and perfect crystallinity of these ultra-scaled metal-semiconductor NW heterostructures was shown. Prior to the actual discussion of transport effects in ultra-scaled Ge channels embedded in Al-Ge-Al NW heterostructures the charge carrier injection barriers of passivated and unpassivated heterostructure devices were addressed with a special focus on the influence of surface traps on charge carrier transport. Based on this systematic analysis, measurements in the temperature range between 400 mK and 300 K demonstrated the experimental observation of quantum ballistic transport up to room-temperature. Further low-temperature investigations showed that for heterostructure devices with Ge channel length below $L_{Ge} = 100$ nm the behavior changes from a SHT to a few-hole quantum dot. Associated with this transition, it was observed that the reduced dimensionality of ultra-scaled Ge channels gives rise to pronounced resonant tunneling in ultra-scaled Ge channel devices. Finally, measurements in the temperature range between 1 K and 400 mK revealed that ultra-scaled Ge channels coupled to superconducting Al leads, reassemble a JoFET. The experimental proof of exchanging cooper-pairs between the superconducting Al leads and a gate-tunable Ge channel, mediated by the superconducting proximity effect enabled the first demonstration of superconductivity induced in a pure Ge channel. Gate-dependent transport measurements revealed a tunable critical supercurrent in the Ge quantum dot from zero to approximately 20 nA.

In conclusion, the experimental results discussed in this thesis revealed the high quality of ultra-scaled Ge channels embedded in axial monolithic Al-Ge-Al NW heterostructures and demonstrate their versatility for novel nanoelectronic devices based on quantum confinement effects. Importantly, the selective replacement of Ge by Al could present a general approach for the realization of radial and axial

metal-semiconductor heterostructures in various Ge-semiconductor heterostructures enabling quasi-1D coaxial metal-semiconductor architectures, attractive for novel photonic and plasmonic devices.

Most notably, the demonstration of the controlled formation of ultra-short Ge channels may motivate the large scale integration of Al-Ge-Al NW heterostructures based on arrays of Ge NWs structured in the device layer of GeOI chips. This would enable highly uniform (in diameter and length) quasi-1D Ge nanostructures, which can be placed perfectly aligned at predetermined sites. Such structures would enable quantum ballistic logic gates, circuits or sensor arrays. Therefore, the findings of this thesis provide a platform for the exploration of ultra-scaled devices based on Ge NWs and are an important step toward the practical applications of quantum ballistic transport at room-temperature. Most notable, they may contribute to the development of novel quantum devices of the post Si era. Further, the investigations on low-temperature transport in ultra-scaled Ge channels contacted by superconducting Al leads revealed an enormous potential for a vast array of key components for quantum computing such as SQUIDs, oscillators, mixers or amplifiers.

Curriculum Vitae

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List of figures

List of abbreviations

Al	Aluminum
ALD	Atomic layer deposition
Au	Gold
BCS	Bardeen-Cooper-Schrieffer theory
BHF	Buffered hydrofluoric acid
DI	Deionized water
EDX	Energy-dispersive X-ray spectroscopy
ESD	Electrostatic discharge
FET	Field-effect transistor
FT	Fourier transformation
Ge	Germanium
GeOI	Germanium on insulator
HAADF	High-angle annular dark field
HF	Hydrofluoric acid
HI	Hydroiodic acid
HRTEM	High-resolution transmission electron microscopy
I/V	Current-Voltage
JoFET	Josephson field-effect transistor
MAR	Multiple Andreev reflections
MOSFET	Metal-oxide-semiconductor field-effect transistor
NW	Nanowire

PCB	Printed circuit board
PMMA	Polymethylmethacrylat
QPC	Quantum point contact
RTA	Rapid thermal annealing
Si	Silicon
SSD	Solid-state-drive
SEM	Scanning electron microscopy
SET	Single-electron transistor
SHT	Single-hole transistor
SMUs	Source measure units
SQUIDs	Superconducting quantum interference devices
STEM	Scanning transmission electron microscopy
Ti	Titanium
VLS	Vapor-liquid-solid

List of symbols

a_B^*	Exciton Bohr radius
D	Diffusion coefficient
E_C	Charging energy
E_F	Fermi energy
G	Conductance
g_S	Spin degeneracy
g_V	Valley degeneracy
Γ_E	Level spacing
h, $\hbar$	Planck constant, reduced Planck constant
$h\Gamma$	Level broadening
k	Wavenumber
k_B	Boltzmann constant
l_m	Scattering mean free path
λ_F	Fermi wavelength
N	Number of conductance channels
m^*	Effective mass
μ	Electrochemical potential
n	Electron density
ρ	Resistivity
σ	Conductivity
T	Temperature
τ_m	Momentum relaxation time

Appendix A

Process parameters

A.1 Measurement module

Substrate preparation

The substrate, used for the fabrication of the measurement module, was a highly p-doped 500 µm thick <100>-oriented Si wafer with 100 nm thermally grown SiO_2 on top. Typical sample size was 15 mm x 15 mm, which were manually cleaved from the wafer.

Substrate cleaning

Prior to the patterning of the measurement module, the following cleaning procedures were performed:

- Ultrasonic cleaning for 120 s at 100 % power in acetone
- Ultrasonic cleaning for 120 s at 100 % power in isopropanol
- Drying the sample with nitrogen

Photolithography

Process procedures needed for the patterning the structures on the measurement module:

- Spin coating of image reversal resist (AZ5214) at 9000 RPM
- Softbaking at 373 K for 60 s
- Mask alignment for the back-gate contacts on the substrate
- Exposure for 5.5 s (Karl Süss MicroTec MJB3)
- Immersing sample 30 s in developer (AZ726MIF)
- Immersing sample 35 s in deionized water (DI)
- Drying the sample with nitrogen
- BHF dip (7:1) for 130 s
- Immersing sample 10 s in DI
- Drying the sample with nitrogen
- Resist stripping with acetone
- Diping the sample in isopropanol
- Drying the sample with nitrogen
- Spin coating of image reversal resist (AZ5214) at 9000 RPM
- Softbaking at 373 K for 60 s
- Alignment of metalization mask and back-gate structures on the substrate

- Exposure for 4 s (Karl Süss MicroTec MJB3)
- Reversal baking at 394 K for 60 s
- Flood exposure for 20 s (Karl Süss MicroTec MJB3)
- Immersing the sample 30 s in developer solution (AZ726MIF)
- Immersing the sample 35 s in DI
- Drying the sample with nitrogen
- BHF dip (7:1) for 5 s
- Immersing sample 10 s in DI
- Drying the sample with nitrogen

Ti/Au sputtering

The empirically determined sputter rates are 0.17 nm s^{-1} at 50 W for Ti and 1.6 nm s^{-1} at 50 W for Au. The following procedures were executed to deposit a 10 nm Ti adhesion layer and a 100 nm Au layer:

- Base pressure: 2×10^{-5} mbar
- Working pressure: 8×10^{-3} mbar
- Ti cleaning procedure: 60 s, 100 W
- 10 nm Ti deposition: 1x60 s, 50 W
- 200 nm Au deposition: 2x60 s, 50 W

Lift-off

Subsequent to the sputter deposition, the excess metal was removed by the lift-off procedure listed below:

- Ultrasonic cleaning with 80 % power in acetone
- After 5 min, rinse the sample carefully with acetone
- Isopropanol dip
- Drying the sample with nitrogen

A.2 TEM sample fabrication

TEM membrane fabrication

For the structural analysis of the crystal structure and the interfaces of Al-Ge-Al NW heterostructures, the device fabrication was performed on arrays of 40 nm thick Si_3N_4-membranes. The process steps for the fabrication of a chip comprising an 8 x 8 array of membranes are listed below:

- Dicing of a 450 µm thick Si (100) wafer with a 200 nm thick layer of thermally grown SiO_2 into 25.6 mm x 24 mm pieces
- 5 min ultrasonic cleaning with 80 % power in acetone
- Isopropanol dip
- Deposition of 40 nm thick layer of stoichiometric Si_3N_4 on each side of the chip by low-pressure chemical vapor deposition (LioniX BV)
- Windows on one side of the chip were opened using UV lithography
- Reactive ion etching was performed to locally remove the Si_3N_4 and SiO_2 layers

- Si was etched through the backside of the chip using a potassium hydroxide (KOH) bath at 353 K for several hours until the opposite Si_3N_4 layer was reached
- The membrane arrays were cleaned in 65 % HNO_3 at 353 K for 1 h
- Bond pads and marker structures were patterned on the top side of the membrane using photolithography
- Electron beam assisted evaporation of Ti and Au was used for contact and marker formation

TEM sample preparation

Prior to the fabrication of Al-Ge-Al NW heterostructures, the membrane chip was mounted on a highly p-doped Si carrier wafer using PMMA as glue. This process step was necessary to prevent the membranes from being damaged during the spin-coating of resist required for the patterning of individual contacts to Ge NWs by electron beam lithography. The used procedure is listed below:

- Cleaving of the highly p-doped carrier wafer
- 5 min ultrasonic cleaning with 80 % power in acetone
- Isopropanol dip
- Drying the sample with nitrogen
- Spin coating of PMMA (AR-P 679.04) for 35 s at 1200 RPM
- Mounting membrane chip on carrier wafer
- Baking the sample for 120 s at 364 K
- Baking the sample for 900 s at 444 K

A.3 Ge nanowire growth

The Ge NWs were grown on Si <100> substrates using the VLS process with germane (GeH_4, 2 % diluted in He) as precursor and a 2 nm thick sputtered Au layer as growth promoting catalyst. The actual growth was performed using a home built low pressure hot wall CVD chamber at 50 mbar and a gas flow of 100 sccm for both, the precursor gas and H_2 as carrier gas. After the pressure and precursor flow is stable, the temperature was ramped up at a rate of 60 K min^{-1} to the target temperature of 614 K. The rather high growth temperature ensures uniform catalyst diameter and good NW epitaxy. After a 10 min nucleation phase, the temperature is lowered to 573 K. Typical growth duration of 60 min result in about 8 µm long NWs with uniform diameters of about 40 nm. Subsequently to the growth, the NWs were uniformly coated with 20 nm Al_2O_3 by atomic layer deposition (Cambridge NanoTech Savannah 100).

A.4 Electrical contact formation

Electron Beam Lithography

The electron beam lithography pattering of individual contacts between the macroscopic Au pads and the deposited NWs was done by the following procedures:

- To avoid charging effects of the sample, the thermally grown SiO_2 layer was carefully removed from one macroscopic back-gate contact by using a diamond scribe
- Placing the sample on sample holder
- Inserting the sample holder via the loadlock into the working chamber of the EBL-system
- Executing the coordinate system alignment procedure
- Executing the writefield alignment procedure

- Searching for NWs in the vicinity of the macroscopic Au contacts and saving the respective coordinates of the NWs
- Removing the sample via loadlock
- Spin coating of PMMA (AR-P 679.04) for 35 s at 4000 RPM
- Baking sample for 900 s at 444 K
- Spin coating of PMMA (AR-P 679.04) for 35 s at 6000 RPM (only for membrane devices)
- Baking the sample for 900 s at 444 K (only for membrane devices)
- Drawing of contacts with a spacing between 1.2 µm and 1.6 µm
- Placing the sample on sample holder and inserting the sample holder via loadlock into the working chamber
- Measuring the electron beam current with Faraday cup
- Calculate dwell times
- Executing the coordinate system alignment procedure
- Executing the writefield alignment procedure
- Start exposure process
- Removing the sample via loadlock
- Developing for 35 s (+5 s for membrane devices) (AR 600-56)
- Immersing the sample for 35 s in stopper solution (AR 600-60)
- Drying the sample with nitrogen

BHF dip

At the contact area between the Al contacts and the Ge NWs, the ALD grown Al_2O_3 was removed by applying the following BHF etching procedure:

- Dipping sample for 23 s in BHF (7:1) (etch rate approximately 1 nm s^{-1})
- Dipping the sample for 10 s in DI
- Drying the sample with nitrogen

HI dip

Prior to the Al sputter deposition, the native GeO_2 layer on the NWs was removed by dipping the sample in diluted HI:

- Dilution: one part 57 % HI was diluted with three parts DI
- Dipping sample for 5 s in 14 % diluted HI (etch rate approximately 1 nm s^{-1})
- Dipping the sample for 20 s in DI
- Drying the sample with nitrogen

Al sputtering

The sputter rate for the deposition of Al was empirically determined as 0.42 nm s^{-1} at 50 W. The following sputter parameter were used to deposit 100 nm of Al:

- Base pressure: 2×10^{-6}mbar
- Working pressure: 8×10^{-3}mbar
- Al cleaning procedure: 2x60 s, 100 W RF power
- 100 nm Al deposition: 4x60 s, 50 W

Lift-off

To finalize the fabrication of the Al contacts, the excess metal was removed from the sample by a lift-off procedure:

- Immersing the sample in acetone at 326 K
- After 30 min, rinse the sample carefully with acetone
- Isopropanol dip
- Drying the sample with nitrogen

A.5 Rapid thermal annealing

The RTA procedure for the formation of Al-Ge-Al NW heterostructures is listed below:

- Opening the working chamber and placing the sample onto a carrier wafer
- Pumping 120 s to approximately 1 mbar
- Flushing 120 s with nitrogen
- Pumping 120 s to approximately 1 mbar
- Flushing 120 s with nitrogen
- Pumping 120 s to approximately 1 mbar
- Flushing 120 s with forming gas
- Heating to 574 K with a 75 $\mathrm{K\,s^{-1}}$ temperature ramp in forming gas atmosphere (no top-heat)
- To prevent a temperature overshoot, execute a 50 $\mathrm{K\,s^{-1}}$ temperature ramp to

624 K in forming gas atmosphere (no top-heat)

- The annealing time depends on the desired Ge segment length (no top-heat).
- Executing the cool-down procedure to room-temperature
- Opening the working chamber and remove sample from quartz tray

A.6 Preparations for cryostat measurements

In detail, the following steps were executed for adapting the measurement module to the sample holder of the cryostat:

- Cleaning a Cu substrate (15 mm x 30 mm) with isopropanol
- Soldering a socket strip onto the PCB with ten conducting paths for wire bonding
- Gluing a PCB on the Cu substrate using a epoxy resin
- Gluing a piece of cigarette paper on the Cu substrate using PMMA resist
- Gluing the measurement module on cigarette paper using PMMA resist
- Using wire bonding (K&S iBond5000-Wedge) to connect the devices on the measurement module with the PCB
- Short-cut the used conducting paths on the PCB using ultrasonic wire bonding to prevent damaging the devices by electrostatic discharge (ESD)
- Inserting and connecting sample with the holder on the cryostat finger
- Connecting the cryostat with the measurement system
- Connecting the cryostat with the temperature controller

- Removing the short-circuiting wire bonds carefully using a tweezer
- Testing the functionality of the arrangement before inserting the finger into the cryostat
- As the Al-Ge-Al NW heterostructures are very sensitive to ESD and voltage peaks, it is necessary to wear a protective ESD wrist strap during bonding and device handling
- While connecting the cables of the SMUs to the device, run a "zero-voltage" program, that applies 0 V to all used outputs with a current compliance of 100 nA for each channel
- Mounting the finger into the cryostat
- Connecting the vacuum pump with the cryostat
- After a pressure of 10^{-5} mbar, is reached, the cooling process is started by connecting the He/LN_2 dewar to the cryostat
- A temperature controller and the He/LN_2 flow valve of the dewar were used to adjust the desired temperature

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