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DIPLOMARBEIT

Ballistic Transport Phenomena in Al-Ge-Al Nanowire Heterostructures

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unter der Leitung von

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Abstract

So far, continuous miniaturization of classical planar electronic devices has been the main driving force behind the advancement of modern integrated circuit technology. However, due to physical limits and dramatic repercussions of short channel effects, scaling becomes increasingly difficult. Hence, a shift towards the adoption of new materials and novel design architectures is predicted to insure further improvement of integration densities, power dissipation and performance.
Semiconductor nanowires (NWs) are predicted to be one of the most promising building blocks for future ultra-scaled high-speed microelectronics. Out of the wide range of NWs, germanium (Ge) occupies an exceptional position, because it combines a high carrier mobility, enabling high performance devices, with a more than five times larger exciton Bohr radius compared to silicon (Si). Hence, Ge is especially interesting for the development of novel quantum devices.
Dedicated to the small feature sizes required, until now it was not possible to show ballistic transport in group IV semiconductor NW based devices at temperatures above 20 mK.
The scope of the diploma thesis at hand was to synthesize axial Al-Ge-Al NW heterostructures with abrupt interfaces and monocrystalline aluminum (Al) leads. This was achieved by using a thermally initiated exchange reaction between vapor-liquid-solid (VLS) grown single-crystalline Ge NWs and Al contact pads. Applying rapid thermal annealing (RTA) for the formation of Al-Ge-Al NW heterostructures is one of the key advantages of the fabrication strategy, because it enables the formation of a Ge nanodot without requiring precise lithographic alignment of the contacts, which is one of the most challenging issues of fabricating nanodot based devices. The capability to control the size of the Ge segment connected by two Schottky tunnel barriers was achieved by fine tuning of the process parameters. Thus, it was possible to fabricate Al-Ge-Al NW heterostructures featuring ultrashort Ge segments down to 10 nm, which can be operated as back-gated field-effect transistors (FETs).
Based on NW heterostructures with ultrasmall Ge segments, a systematic investigation of ballistic transport phenomena was carried out by electrical characterizations at room temperature as well as cryogenic temperatures down to 5 K. In order to allow interpretation and to gain a better insight into the measurement results of the conducted transport measurements, the diameter dependence of quantum confinement effects in Ge NWs was investigated by simulations based on the 2D Schrödinger equation. By comparing the experimental data and simulation results, evidence of ballistic transport for Al-Ge-Al NW heterostructures with Ge segment lengths varying between 10 nm and 30 nm at room-temperature is presented.

Kurzfassung

Bis jetzt war die kontinuierliche Miniaturisierung klassisch planarer Transistorarchitekturen die treibende Kraft für den Fortschritt der Mikroelektronik. Eine weitere Miniaturisierung wird durch das Erreichen physikalischer Grenzen immer komplizierter. Um sowohl eine weitere Steigerung der Integrationsdichte und Schaltgeschwindigkeit als auch eine Verringerung der Leistungsaufnahme von Transistoren gewährleisten zu können, verschiebt sich der Forschungsschwerpunkt zunehmend in Richtung neuer Prozessorarchitekturen und der Integration von neuen Materialien.
Die Integration von Nanodrähten ist eine der vielversprechendsten Konzepte für eine zukünftige Generation von ultraschnellen Transistoren. Auf Grund der vorteilhaften Kombination aus hohen Ladungsträgermobilitäten und einem mehr als fünfmal größeren Exziton Bohr-Radius im Vergleich zu Silizium (Si) ist die Integration von Germanium (Ge) basierten Nanodrähten sowohl für die Entwicklung von high-speed Transistoren als auch für die Erforschung von "Quantum-Confinement-Effekten" interessant.
Bis jetzt ist es nicht gelungen, ballistischen Transport in Gruppe IV Halbleiter basierten Bauelementen über einer Temperatur von 20 mK zu zeigen.
Das Ziel der vorliegenden Diplomarbeit war es daher, axiale Al-Ge-Al Nanodraht Heterostrukturen mit abrupten Metall-Halbleiter-Übergängen und einkristallinen Aluminium (Al) Kontakten herzustellen und ballistischen Transport nachzuweisen.
Die Herstellung der Al-Ge-Al Nanodraht Heterostrukturen wurde durch eine thermisch induzierte Austauschreaktion zwischen einkristallinen Ge Nanodrähten und deren Al Kontakten realisiert. Da dieses Herstellungsverfahren kein präzises lithographisches Ausrichten der Kontakte benötigt, stellt es einen der bedeutendsten Vorteile des Fertigungsprozesses dar. Die Herstellung von Al-Ge-Al Nanodraht Heterostrukturen mit ultrakurzen Ge Segmenten verbunden durch Zwei Schottky Tunnelbarrieren wurde durch eine Feinabstimmung der Prozessparameter erreicht. Die hergestellten Heterostrukturen wurden für die durchgefürten Transportuntersuchung als Back-Gate gesteuerte Feldeffekttransistoren betrieben.
Basierend auf der elektrischen Charakterisierung im Temperaturbereich zwischen 5 K und 300 K wurden Al-Ge-Al Nanodraht Heterostrukturen mit ultrakurzen Ge Segmentlängen systematisch in Hinblick auf ballistische Transportphänomene untersucht. Um den Einfluss des Nanodraht-Durchmessers auf "Quantum-Confinement-Effekte" zu untersuchen, wurden Simulationen basierend auf der 2D-Schrödinger-Gleichung durchgeführt. Durch einen Vergleich der experimentellen Messdaten und der simulierten Eigenenergien war es möglich ballistischen Transport bei Al-Ge-Al Nanodraht Heterostrukturen mit Ge Segmentlängen zwischen 15 nm und 30 nm für Temperaturen bis 300 K zu zeigen.

Acknowledgement

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Chapter 1

Introduction

After decades, following Moore's law [1] by continuously shrinking the feature sizes of classical planar integrated circuit technology, physical limits and the dramatic repercussions of short channel effects [2] forced a shift of research efforts towards the integration of new materials and device architectures [3].
One of the most promising building blocks predicted to overcome the aforementioned limitations are quasi one dimensional nanostructures denoted NWs. In contrast to e.g. carbon nanotubes [4], there is no need for a distinction between metallic or semiconducting NWs, because their properties are determined by the material they are consisting of. In addition, today a large variety of different semiconductor materials, such as e.g. silicon (Si), germanium (Ge), gallium arsenide (GaAs), gallium nitride (GaN) or indium arsenide (InAs) are available for NW growth [5]. Decades of advances in the field of NW synthesis are culminating in highly sophisticated growth processes capable to even fabricate e.g. 2 mm long and only 100 nm thick NWs, exhibiting enormous aspect ratios [6]. The astonishing potential to enable ultra-scaled high performance and low power consuming nanoelectronic devices encouraged enormous research interest for future microelectronic [2, 7], photonic [8], plasmonic [9], photovoltaic [10], solar energy harvesting [11], energy storage [12] and sensors [13] based on NWs.
Out of the wide range of NWs, using Ge is motivated by its high carrier mobility, which may paves the way for future high performance devices. Further on, with a more than five times larger exciton Bohr radius compared to Si, Ge exhibits quantum confinement effects at larger structural sizes [14, 15]. The unique combination of these advantageous properties makes Ge interesting for the development of novel quantum devices [16, 17]. According to the small difference between the direct and indirect band gap energy, Ge is also a promising candidate for investigating strain-driven band structure engineering and its impact on the electrical and optical properties [18].
Fabricating reliable electrical contacts is one of the main issues to ensure highly reliable future nanoelectronic devices based on NWs. Common metal contacts are formed by

using a combination of electron beam lithography (EBL), metal deposition and lift-off techniques. However, metal contacts often reveal large Schottky barriers [19]. Regarding this problematic, intense research on studying thermal diffusion processes of metals into Si and Ge NWs was carried out to form silicides and germanides respectively. In recent years, various materials including nickel (Ni) [20], cobalt (Co) [21], platinum (Pt) [22], manganese (Mn) [23] and copper (Cu) [24] have been investigated as diffusion sources. Moreover, it was successfully demonstrated that NW heterostructures with abrupt interfaces can weaken the Fermi-level pinning effect [25]. Since native defects on Ge surfaces are resulting in high density interface states [19], this technique enabled the possibility to diminish the Fermi-pinning effect, which was one of the main obstacles for fabricating Ge NW based devices in the past. Furthermore, by using Cu as source material, it was demonstrated, that germanide regions can be used as source/drain contacts for novel NW based field-effect transistors (FETs), allowing channel lengths below 50 nm without using high-coast masks and photolithography technology [24]. According to recent publications, NW heterostructures also show a huge potential to pave the way for entirely new nanoelectronic device concepts such as impact ionization FETs [26]. In addition, the evidence of negative differential resistance (NDR) behavior in Al-Ge-Al NW heterostructures may lead to novel static memory cells, fast switching logic circuits or high-frequency oscillators [27]. The motivation for using 1D nanostructures like NWs for future nanoelectronic devices featuring ballistic transport is associated with the intrinsic problem of planar nanoelectronic device architectures, which due to etching often exhibit pronounced structural surface roughnesses. Therefore, top-down fabrication of quantum dots is often resulting in multiple dots connected in series. It was demonstrated, that this problem is not present in ballistic nanoelectronic devices fabricated based on VLS grown NWs [28].

The scope of this diploma thesis is to investigate ballistic transport phenomena in axial Al-Ge-Al NW heterostructures featuring ultrasmall Ge segments with abrupt metal-semiconductor interfaces and monocrystalline Al leads. The heterostructure devices were formed by a RTA initiated exchange reaction between VLS grown single-crystalline Ge NWs and Al contacts. Starting with a theoretical overview of the used materials, chapter 2 discusses NW synthesis by the VLS method. In addition, the possibilities for using NWs in microelectronics are addressed. Further on, diffusion and substitution processes in the Al-Ge material system are explained based on the fundamentals of solid state diffusion. After that, the theoretical aspects of ballistic transport phenomena and their possible applications for future microelectronic devices are discussed. Chapter 3 is describing the experimental techniques for the formation of Al-Ge-Al NW heterostructures featuring ultrasmall Ge segment lengths. In addition, the process flow for the fabrication of a measurement module suitable for conducting electrical characterizations is discussed. By comparing the measurement results from electrical characterizations at room temperature and at cryogenic temperatures with simulations based on the 2D Schrödinger equation concerning the diameter dependence of the eigenenergies in Ge NWs, chapter 4 discusses ballistic transport in Al-Ge-Al NW heterostructures with Ge segment lengths between 10 nm and 30 nm. Finally, chapter 5 provides a summery of the thesis as well as an outlook for further investigations concerning Al-Ge based NW heterostructures.

Chapter 2

Theory

The following chapter discusses the fundamental physico-chemical parameters of the materials Al and Ge, needed for the fabrication of Al-Ge-Al NW heterostructures. In the second part of the chapter, various NW synthesis techniques, with special focus on the VLS method will be reviewed. Further on, the advantageous properties and possibilities for using NWs in future microelectronic devices are discussed. After that, the fundamentals of solid state diffusion are addressed. Moreover, diffusion and substitution processes in Al-Ge material systems are described. Further on, theoretical aspects of ballistic transport phenomena and their possible applications for future nanoelectronic devices are discussed. Finally, the last section of this chapter is considering theoretical aspects of the fabrication techniques required for the formation of Al-Ge-Al NW heterostructures.

2.1 Materials

In order to undertake a profound discussion on Al-Ge-Al NW heterostructures fabricated for the investigation of ballistic transport phenomena, it is mandatory to address the fundamental properties and parameters of the involved materials. Therefore this chapter focuses on the structural, mechanical and electronical properties of Al and Ge.
In terms of classification, Al is a trivalent and Ge is a tetravalent element. Further on, there is no possible stoichiometric compound of Al and Ge.
Fig. 2.1 depicts the binary phase diagram of Al-Ge. As can be seen, below the eutectic temperature of 693 K, the solubility is very low. Only about 2 % of Ge are incorporated into Al. The solubility of Al in Ge is with about 1 % also very small. Hence, it is much more likely that there are only local crystallites rather than intermetallic phases.

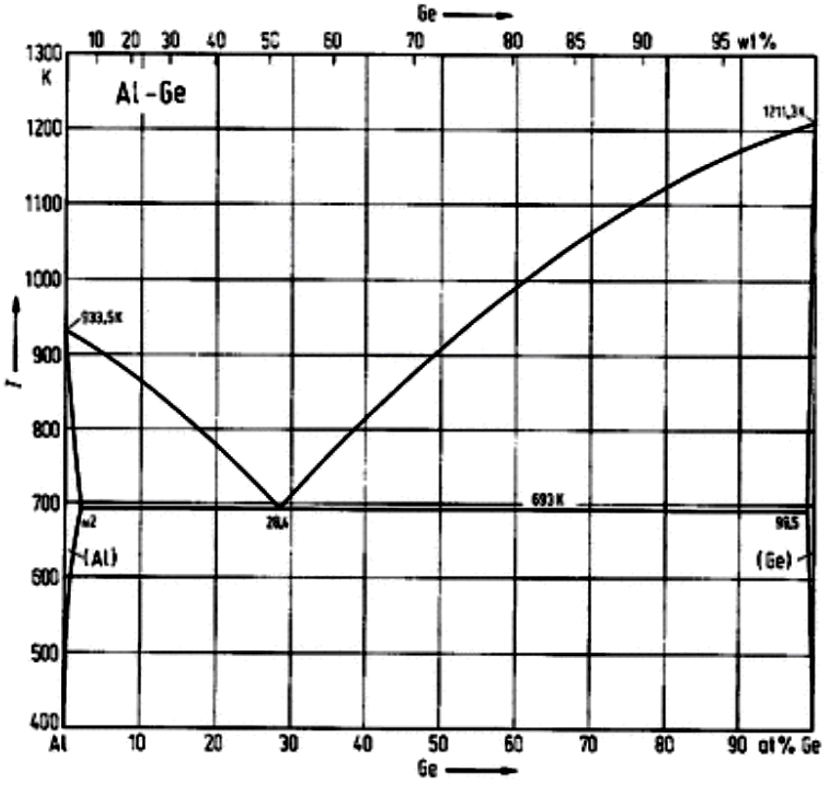

Figure 2.1: *Al-Ge phase diagram revealing an eutectic temperature of* 693 K. *Image taken from [29]*

Moreover, it was demonstrated that RTA of a thin film bilayer consisting of Al and Ge deposited on a SiO_2 substrate above the crystallization temperature of Ge at 399 K results in a metastable AlGe alloy formed in the Ge layer. After the RTA procedure, the amorphous AlGe alloy was converted to a polycrystalline film. [30].

2.1.1 Aluminum

Al is a metal, in the 3rd group of the periodic table of elements and has the atomic number 13 as well as a relative atomic mass of 26.98. Its melting- and boiling point are 933 K and 2790 K, respectively. As most metals, Al crystallizes in a face-centered cubic (fcc) structure with a lattice constant of $a_{Al} = 0.405\,\text{nm}$. The crystallographic structure of Al is depicted in fig 2.2. According to its high reactivity, it often occurs in compounds like feldspar, granite and bauxite core. Although pure Al is never found in nature, with 8.1 %, Al is the most abundant metal in the earth's crust [31, 32].

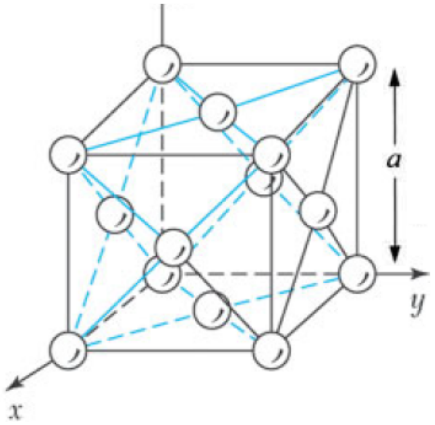

Figure 2.2: *Face-centered-cubic (fcc) cell. Image taken from [33]*

For the most part, Al is produced by using an energy intensive electrolysis process capable of achieving Al of $\geq$ 99.99 % purity. The base material for this process is bauxite ore containing between 20 and 30 % Al. Due to the excellent recycling properties of Al, today up to 95 % of the energy compared to the aforementioned electrolysis process can be saved by secondary production e.g. recycling scrap and waste material. The amount of recycled Al has nowadays reached up to 30 % of the total production [32]. Due to its excellent combination of mechanical and electrical properties, such as a low density of $2.7\,\text{g}\,\text{cm}^{-3}$ [32] and an good electrical conductivity of about $36\,\text{mS}\,\text{mm}^{-2}$ [32], Al is the second most widely used metallic material today [32]. In addition to these favorable properties, Al is universally used because of its good machinability, light weight and high corrosion resistance, which results from a fast formation of a thin native oxide film in oxygen-containing atmospheres [32]. In terms of usage in microelectronic devices, Al is i.e. successfully applied as metalization and interconnect material in integrated circuits. This is especially attributed by the fact that Al rather than other metals like Au or Cu is not causing deep traps in Si or Ge, that could act as recombination centers for charge carriers (fig. 2.3) [34].

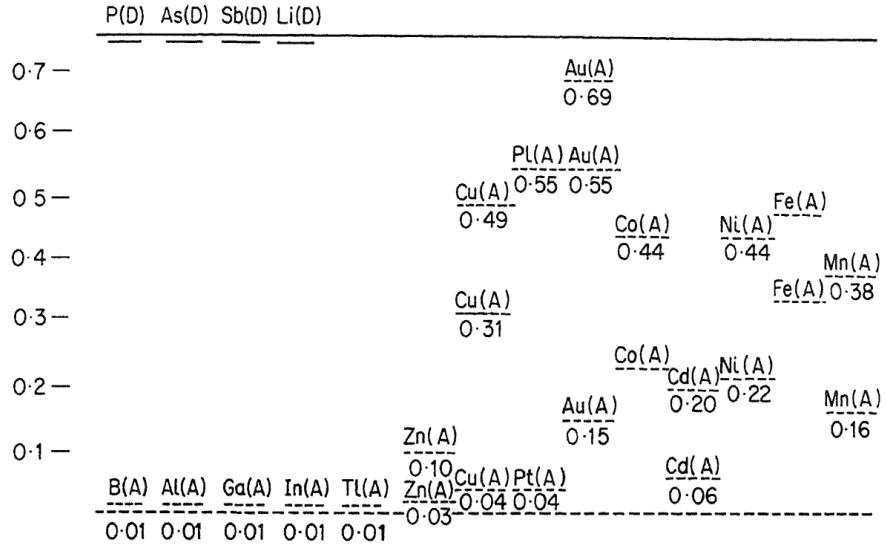

Figure 2.3: *Energy levels of various impurities in Ge. Image taken from [34]*

Beside these advantageous properties, the ever increasing current densities of modern microelectronic devices lead to unacceptable electromigration in Al interconnects. Thus, starting with the development of Cu interconnects in 1997, Al was successively replaced as preferred metalization material [35]. Furthermore with a work function of $q\phi_m = 4.1\,\mathrm{eV}$ [32], Al is one of the most frequently used materials for metal electrodes and integrated transducers [36].

2.1.2 Germanium

Ge is an elementary semiconductor with an indirect band-gap in the 4th group of the periodic table, which exhibits the atomic number 32 and a relative atomic mass of 72.64 [31, 32]. Its melting- and boiling point are 1211 K, 3107 K respectively [31, 32]. As many important semiconductors Ge forms a diamond crystal lattice structure with a lattice constant of $a_{Ge} = 0.566\,\text{nm}$, that can be considered as two interpenetrating fcc lattices. In such a structure, each atom is surrounded by four equidistant nearest neighbors, which lie in the corners of a tetrahedron (fig. 2.4) [36].

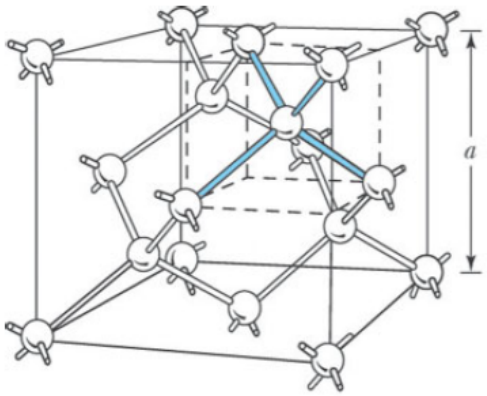

Figure 2.4: *Diamond lattice structure. Image taken from [33]*

In nature the occurrence of Ge is restricted to mineral compounds like argyrodite, germanite, zinc ors or coal. The production of crystalline Ge suitable for the fabrication of electronic devices requires a degree of purity to extent where only one part in 10^{10} is an impurity. Such ultra-high purity Ge is today mainly produced by zone-refining techniques [32]. Fig. 2.5 depicts the band structure of Ge, that reveals an indirect band-gap of $E_g = 0.66\,\text{eV}$ at a temperature of 300 K. Since Ge nearly has a direct band-gap, it was shown that alloying with tin (Sn) [37] or creating high uniaxial tensile stress in suspended Ge structures can be applied to fabricate Ge based lasers [38]. One of the most important advantages of using Ge over other semiconducting materials, such as Si, is the extremely high carrier mobility for both electrons and holes. Ge exhibits a electron mobility of $3600\,\text{cm}^2\,\text{V}^{-1}\,\text{s}^{-1}$ [39] about twice as high as the one of Si. Furthermore, Ge exhibits by far the highest hole mobility of $1800\,\text{cm}^2\,\text{V}^{-1}\,\text{s}^{-1}$ [39] among all semiconductors. Regarding this advantageous properties, the first transistors were fabricated using Ge [40, 41]. Despite the beneficial carrier mobilities of Ge, Si was dominating the microelectronic industry until CMOS scaling reached the 45 nm technology node, which firstly applied high-k dielectrics as gate-oxide. As a result of this advancement, the main advantage of Si having a high quality thermal oxide was no longer crucial and Ge became again a potential semiconductor material for future high performance devices [42]. In addition, Ge features the occurrence of quantum confinement effects, such as ballistic transport phenomena, at

much larger structural sizes than e.g. Si. This can be attributed to the fact that the exciton Bohr radius (the distance between the electron and the hole within an exciton) of Ge $a^*_{BGe} = 24.3\,\text{nm}$ is more than five times larger than the one of Si $a^*_{BSi} = 4.9\,\text{nm}$ [14, 15]. Hence, Ge is a more attractive candidate to study quantum confinement effects.

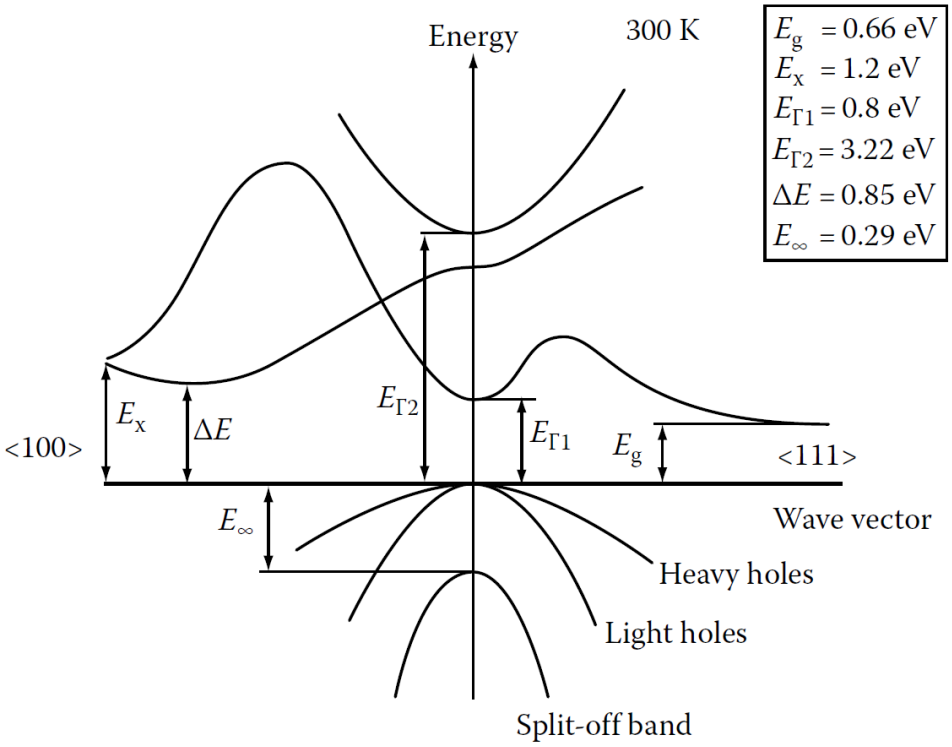

Figure 2.5: *Energy band diagram of Ge showing an indirect band-gap of* $E_g = 0.66\,\text{eV}$ *at a temperature of* 300 K. *Image taken from [4]*

Beyond the usage in electronic devices, Ge is also the base material for a large variety of different optical systems such as infrared spectrometers and fiber optics [31]. Due to a high index of reflection and dispersion, Ge-oxides are used for the fabrication of wide angle camera lenses and microscope objectives. Further on, Ge can also be applied as e.g. an alloying agent, as a phosphor in fluorescent lamps and as a catalyst [31].

2.2 Nanowires

Nanowires are elongated quasi 1D nanostructures with tunable diameters at the nanometer length scale, that can exhibit aspect ratios far beyond 1:1000 [6]. Fig. 2.6 depicts a TEM image of VLS grown Ge NWs on a Si substrate.

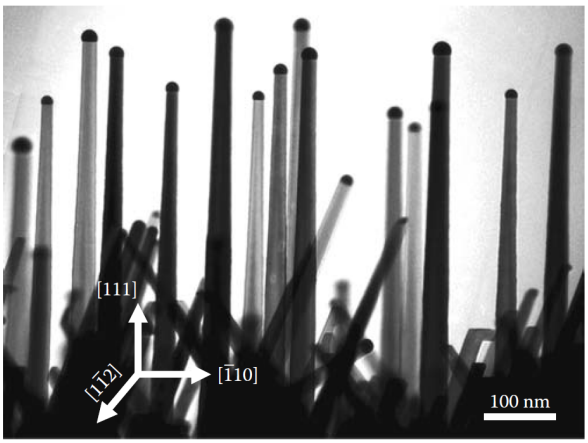

Figure 2.6: *TEM image of VLS grown Ge NWs on a Si substrate. Image taken from [43]*

The motivation for using NWs arises from the fact that they are one-dimensional nanostructures, with properties like e.g. 1D transport of charge carriers, that cannot be observed in bulk materials [44]. Attributed to the fact that the structure of NWs is exposing a larger surface to volume ratio compared to bulk materials, their surface atoms have a different coordination. In addition, interfaces between nanostructures exhibit e.g. modified electronic properties, strain gradients and different propagation behavior of defects, charge carriers and phonons. Further on, quantum confinement effects and coherent interactions between structures are occurring [44]. In contrast to carbon nanotubes [4], there is no need for a distinction between metallic or semiconducting NWs, because their properties are always determined by the material they are consisting of. Another very important advantage of NWs is that a large variety of different semiconductor base materials, such as e.g. Si, Ge, GaAs, GaN and InAs are available for NW growth [5]. Attributing to the fact that the aforementioned materials exhibit different electrical and optical properties, NWs have not only attracted intense research interest for future microelectronic devices such as ultra-scaled gate-all-around (GAA) transistors [2, 7], but exhibit an enormous potential to be important building blocks of future photonic [8], plasmonic [9], photovoltaic [10], solar energy harvesting [11], energy storage [12] or sensor devices [13]. Over the last few years especially Ge NWs have received significant attention. The increased interest in Ge based NWs can be dedicated to the superior charge carrier mobility and large a_B^* of Ge. Investigations on Ge NWs have e.g. addressed strain-driven band structure engineering [18], transport modulation [45] or band offset efficiency [46] of core-shell NWs [47].

2.2.1 Nanowire Synthesis

The highly favorable properties of NWs combined with their enormous potential for future devices triggered intense research interest in the field of NW synthesis and led to the exploration of a large variety of different synthesis technologies like electron beam lithography [48], laser ablation [49], template [50] or VLS [51] and VSS [52] growth mechanisms [15]. Since the work at hand is concerning Al-Ge-Al heterostructures consisting of VLS grown Ge NWs, this technology will be discussed more in detail.
Today catalytic NW growth by the VLS mechanism is a well-established growth technique for the bottom-up fabrication of semiconductor NWs. Since the first demonstration in the 1960s [51], intense research archived a continuous improvement of this synthesis method allowed better insight into growth dynamics, kinetics and morphology control of VLS grown NWs [47].

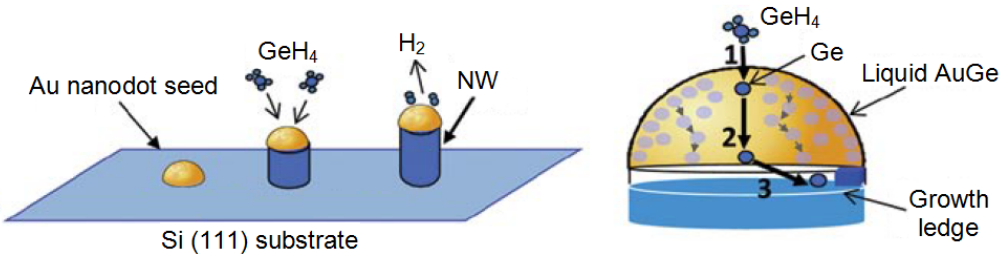

Figure 2.7: *(left) Schematic illustration of the VLS synthesis of Ge NWs, (right) detailed view of the kinetic process of Ge incorporation at the Au-Ge interface during VLS growth: (1) Adsorption and decomposition of GeH_4 on the Au nanodroplet, (2) Ge diffusion through the AuGe liquid, (3) Ge incorporation at the liquid-solid AuGe interface. Image adapted from [44]*

In order to synthesize Ge NWs by the VLS growth mechanism, schematically illustrated in fig. 2.7, a thin metal layer, mostly Au, is deposited on a Si wafer. Subsequently, the wafer introduced in a chemical vapor deposition (CVD) reactor is annealed, thus due to dewetting of the Au layer, small Au nanodroplets are formed. These nanodroplets not only serve as catalytic seeds, but also define the diameter of the NWs. To achieve VLS growth, the reactor is heated above the eutectic temperature of the Au-Ge material system, which is at 539 K [53]. As fig. 2.7 depicts, a gaseous precursor (GeH_4) is then introduced to the CVD reactor. This triggers a kinetic process, which starts with the absorption of GeH_4 on the Au nanodroplet, followed by a subsequently decomposition into volatile H_2 and Ge, which occurs at the vapor-liquid interface. After that, the remaining non-volatile Ge is diffusing through the AuGe liquid. Finally, due to supersaturation, Ge is incorporated at the liquid-solid interface forming a vertically growing solid quasi one-dimensional Ge NW [5, 44]. In order to prevent kinking along the growth direction, it is mandatory to ensure stable conditions for pressure, temperature and gas concentration in the CVD reactor [44, 54].

2.3 Solid State Diffusion

Diffusion is a fundamental process in solid-state physics. The origin of diffusion is the irregular movement of atoms, which is called the Brownian motion. This behavior is e.g. relevant for the kinetics of microstructural changes occurring during material processing, such as nucleation of new phases, diffusive phase transformations, recrystallization and thermal oxidation. Since diffusion and electrical conduction phenomena in ionic conductors are closely related, technological applications of diffusion processes include e.g. solid electrolytes for batteries and fuel cells, surface hardening of steel through carburisation or nitridation, diffusion bonding, or sintering. Moreover in microelectronics, diffusion is a fundamental process involved in semiconductor doping and silicide/germanide formation [55]. A mathematically description of diffusion processes is provided by Fick laws [55, 56]. According to these laws, the flux of diffusing quantities J in three dimensional vector notation is given by:

$$J = -D\nabla C \tag{2.1}$$

It is important to note, that the negative sign in eq. 2.1 is indicating opposite directions for the diffusing quantities J and the concentration gradient vector ∇C, which is always pointing in the direction of the most rapid increase of the concentration field. The proportionality factor between these two parameters, D [$\mathrm{cm}^2\,\mathrm{s}^{-1}$], is called diffusion coefficient, given by:

$$D = D_0 \exp\left(-E_A/k_B T\right) \tag{2.2}$$

where E_A is the activation energy and k_B denotes the Boltzmann constant and D_0 is the maximum diffusion coefficient at infinite temperature. Since diffusive processes usually exhibit a conserved number of diffusing particles, assuming that the involved species neither undergo reactions nor exchanges with internal sources or drains, the continuity equation can be denoted as:

$$\frac{\partial C}{\partial t} = \nabla \cdot J \tag{2.3}$$

By combining Fick's first law (eq. 2.1) with the continuity equation (eq. 2.3) a linear second-order partial differential equation denoted Fick's second law can be obtained:

$$\frac{\partial C}{\partial t} = \nabla \cdot (-D\nabla C) \tag{2.4}$$

One of the most important diffusion processes in crystalline solids are point defects, which are capable of moving through the crystal. In contrast to metals, where point defects appear to be uncharged, point defects in semiconductor can introduce electronic energy levels within the band-gap. According to the fact that the packaging density of covalent semiconductor crystals is considerably lower than in close-packed metals, semiconductors are offering significantly more space for self-interstitials. Beside that, high quality semiconductors exhibit orders of magnitude lower defect concentrations compared to both metals and ionic crystals, which can be attributed to the covalent bonding of semiconductors [55]. Fig. 2.8 depicts a selection of the most important diffusion mechanisms in crystalline materials. As can be seen in (a) considerably smaller solute atoms compared to the host lattice atoms may diffuse by jumping between interstitial sites before being incorporated on interstitial sites of the host lattice. Further on, in cases where the solute atoms are equally sized compared to the host atoms, diffusion mechanisms like direct exchange (b) or direct ring exchange (c) are possible. In crystal structures that additionally exhibit thermally induced atomic defects like vacancies, it is possible that diffusion is occurring by jumps of solute atoms into a neighboring vacancy (d). Beside the aforementioned diffusion mechanisms, solute atoms equally sized to the host lattice atoms, denoted as self-interstitials, which are atoms located between the lattice sites, might occur. In this case an unison move of both a self-interstitial and a lattice atom can result in a replacement of a host lattice atom, which is subsequently itself forced to replace a neighboring lattice atom (e) [55].

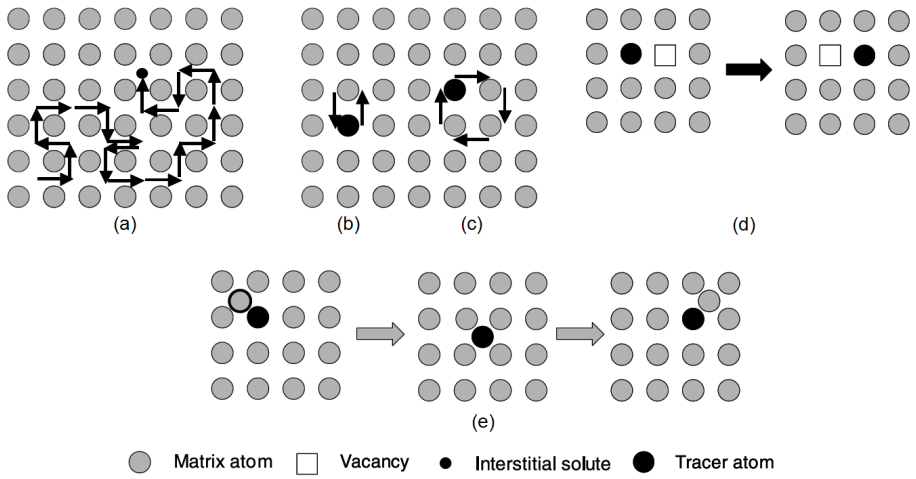

Figure 2.8: *Diffusion mechanisms in crystalline solids: (a) Direct interstitial diffusion of solute atoms smaller than the host lattice atoms. For solute atoms similar sized to the host lattice atoms direct exchange (b) or ring diffusion (c) is possible. In crystal structures with thermally induced atomic defects like vacancies, solute atoms can jump into a neighboring vacancy, which is denoted monovacancy diffusion (d). Further on, the unison movement of both a self-interstitial and a lattice atom can result in a replacement of a host lattice atom, which is subsequently itself forced to replace a neighboring lattice atom, is called interstitialcy mechanism (e).*
Image adapted from [55]

2.3.1 Diffusion and Substitution in the Al-Ge System

In order to generally discuss the process of interdiffusion in a binary A-B system, the Kirkendall effect [57] provides a suitable description of the diffusive motion of A and B atoms exhibiting different intrinsic diffusion coefficients D_A and D_B relative to lattice planes [57, 58]. Because of Fick's first law (eq. 2.1), the diffusing quantities J and the concentration gradients ∇C of both species must be equal and opposite to each other when a fixed volume axes is considered. Hence, for many applications only a single parameter, denoted as the chemical interdiffusion coefficient $\tilde{D}$ is sufficient for the description of the behavior of a two component diffusion process [55, 57, 58]. By introducing the fractional concentrations N_A and N_B, the interdiffusion coefficient $\tilde{D}$ is given by:

$$\tilde{D} = N_A D_B + N_B D_A \tag{2.5}$$

Further on, the combination of different magnitudes of diffusion rates relative to local lattice planes of the considered materials and conserved lattice site density led to a net total flux of atoms across the lattice planes [58]. This circumstance causes a shift of the diffusion zone to compensate the imbalance of the fluxes across the lattice plane, which is called the Kirkendall effect [57, 58]. Subsequently a process of vacancy creation on one side and an annihilation of vacancies on the other side is proceeding. Considering all these processes, it can be observed, that interdiffusion is occurring on a lattice locally moving relative to the axes, which were used for the calculation of $\tilde{D}$ (eq. 2.5) [58]. Experimentally, the aforementioned behavior was first observed by using a sample prepared with inert markers [57, 58]. The product of the concentration gradient ∇C at the marker position $\partial N_A/\partial x$ and the difference between the intrinsic diffusion coefficients yield the equation for marker velocity as:

$$v = (D_A - D_B)\frac{\partial N_A}{\partial x} \tag{2.6}$$

Based on these fundamentals, the diffusion and substitution behavior in heterostructures consisting of a Ge NW connected to Al electrodes was comprehensively investigated [59, 60]. It was shown that a thermal annealing process can be applied to diffuse Al from the electrodes into the attached Ge NW. According to the large difference between the diffusion coefficient of Ge in Al ($3.27 \times 10^{-12}\mathrm{cm}^2\,\mathrm{s}^{-1}$) [57, 58] and Al in Ge ($1.25 \times 10^{-25}\mathrm{cm}^2\,\mathrm{s}^{-1}$) [57, 58], Ge is diffusing into the Al electrodes. Further on, the relatively fast diffusion of Al ($1.46 \times 10^{-12}\mathrm{cm}^2\,\mathrm{s}^{-1}$) [57, 58] is contributing to a filling of the vacancies left behind by the diffusing Ge, resulting in an unreacted pure Ge segment connected by monocrystalline Al leads [59, 60]. Although during the annealing process, the formation of metastable alloys was observed at the moving Al-Ge interface, below 674 K an abrupt metal-semiconductor interface is formed.

2.4 Ballistic Transport

Over recent years, intense research facilitated rapid scaling of microelectronic devices down to structural sizes reaching the scattering mean free path of the charge carriers [61] at which electrons experience almost no collisions [4].
Hence, the scattering mean free path l_m is defined as the average distance the electrons or phonons can travel before they encounter successive impacts (collisions) with scattering sources like crystal defects, impurities or grain boundaries [4]. Fig. 2.9 depicts a sketch of different electron transport mechanisms, ranging from diffusive to ballistic electron transport. It can clearly be seen, that the probability for collisions of electrons and impurities is getting less significant as the structures are reaching sizes that are comparable to l_m [36, 62].

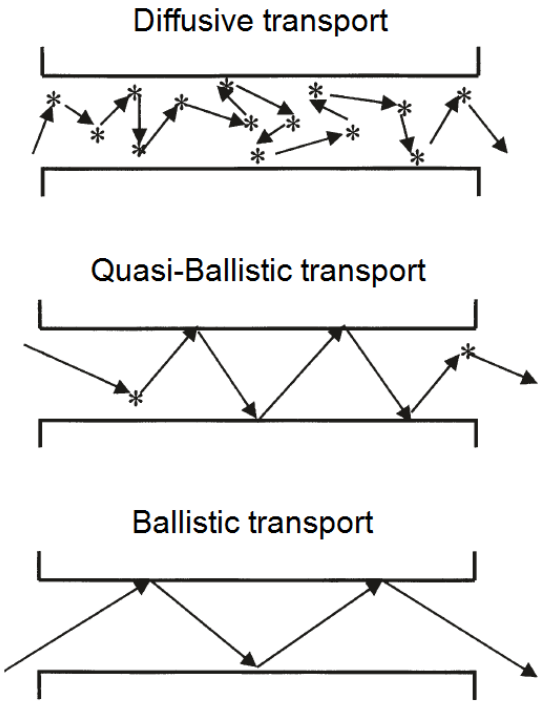

Figure 2.9: *Electron transport mechanisms:*
In bulk conductors diffusive transport is dominated by scattering of electrons or phonons with crystal defects, impurities or grain boundaries. As structural sizes are getting close to l_m, the probability for collisions is getting less significant (quasi-ballistic transport). Further on, for structural sizes below l_m scattering events are completely absent (ballistic transport).
Image adapted from [62]

The equation of the scattering mean free path l_m, shown in equ.2.7, is depending on the effective mass m^*, the electron density n and the momentum relaxation time τ_m [61].

$$l_m = \frac{\hbar}{m^*}\sqrt{2\pi n}\tau_m \tag{2.7}$$

Therefore, in order to estimate the critical length of the Ge segments of the fabricated Al-Ge-Al NW heterostructures to show a transition from diffusive to ballistic transport, l_m was calculated based on eq. 2.7.
Since the electrical characterization of the used Ge NWs, due surface doping of adsorbates on the surface of the NWs, reveled p-type behavior, the effective mass of holes $m^*_{Ge} = 0.041m_0$ [31] was applied for the calculation of l_m. If the surface doping is assumed be equivalent to $N_A = 1 \times 10^{18}\text{cm}^{-3}$ and the τ_m of Ge $\tau_{mGe} = 0.26\,\text{ps}$ [63] is inserted into eq. 2.7, l_m can be estimated to be $l_{mGe} = 34.64\,\text{nm}$.

In respect to the Fermi distribution, all aspects of electrons as matter waves are valid for ballistic motion. Hence, the electron behavior is best characterized by propagating waves. Concerning ballistic transport, it is very important to point out, that ballistically propagating waves are no longer predominately characterized by the internal material properties of the structure used for propagation. Instead, due to collisions and deflections of electrons at the boundaries of the structure, the shape of the external boundary is gaining influence. Conductors exhibiting this type of geometry are denoted quantum wires, where electrons have to be interpreted as quantum mechanical matter waves [62].
In terms of electron transport, reaching ever smaller structural sizes is equivalent to a shift from diffusive to ballistic electron transport.
Due to the absence of scattering events, the charge carriers are able to gain energy from the field without losing it to the lattice. Therefore, the charge carriers can propagate at velocities exceeding the saturation velocity. Additionally, the drift velocity is increasing proportional to qEt/m^*, facilitating values momentarily exceeding the steady state velocity. This phenomenon is called velocity overshoot [36]. Further on, ballistic transport is probably enabling electronic devices with novel characteristics like minimal resistive voltage drop in the channel, leading to transistors operating at the upper limit of ON-state conductance [64]. Moreover, temperature depending phonon scattering resulting in serious degradation of the performance does not exist in ballistic devices. The combination of these advantageous properties is one of the major motivating factors for further shrinking of transistor channel lengths and may pave the way for novel nanoelectronic devices featuring high working speeds and quick response times.[36].
One example for these novel devices are ultrashort-channel solid-state-drives (SSDs). It was simulated that by shrinking the channel lengths down to the ballistic regime, a doubling of the average drift velocity can be achieved. Moreover, this not only improves the high-frequency performance, but also decreases the overall energy loss in the device. In consequence, the working efficiency of SSDs can significantly be improved [65].

2.4.1 The Ballistic Conductor

To actually use one dimensional ballistic conductors as building blocks for future nano-electronic devices, a coupling with a three dimensional bulk electron reservoir is necessary for connection purposes. An example for such an arrangement is schematically depicted in fig. 2.10(a).

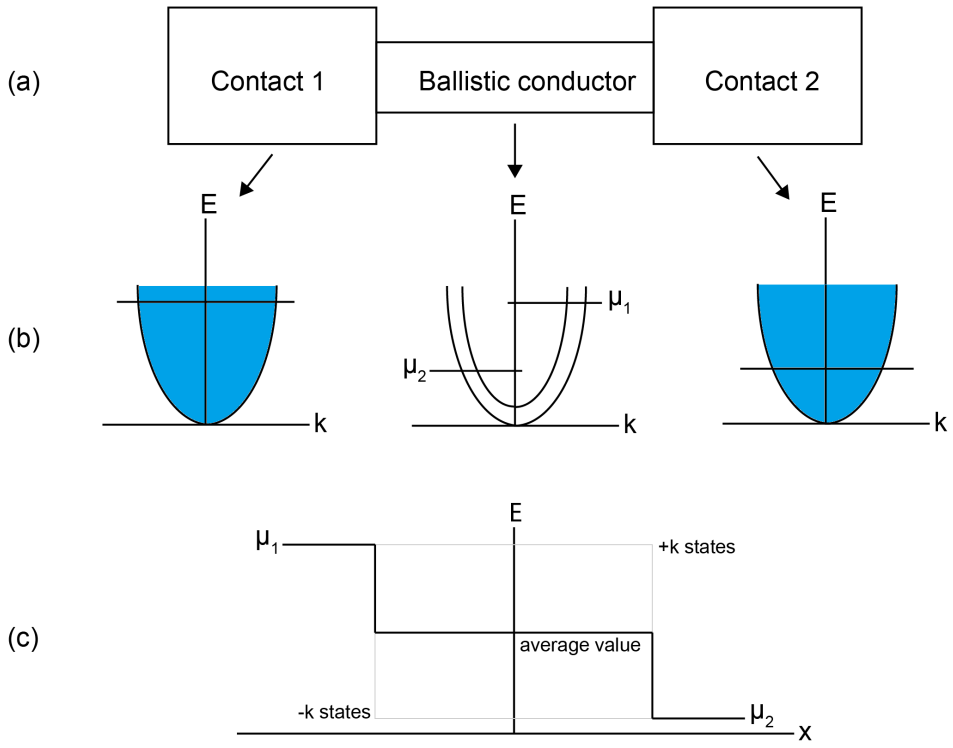

Figure 2.10: *Ballistic conductor connected to two macroscopic contacts:*
(a) Sketch of connected ballistic conductor,
(b) Band-diagrams of contacts and ballistic conductor,
(c) Variation of the electrochemical potential for applied bias.
Image based on [61]

At this point, it is important to mention the difference between bulk and ballistic conductors. For bulk conductors ($l >> l_m$), the resistance is depending on the conductivity of the material σ as well as the width to length ratio (W/L). Thus, the conductance is expected to grow indefinitely as the length is decreasing. According to the spatial confinement in a ballistic conductor, the allowed transverse modes (sub-bands) are discretized. In contrast, the modes in a bulk material are relatively dense. Although momentum conservation is assumed, most modes get reflected at the interface between the macroscopic contacts and the ballistic conductor. Hence, there is only a small intersection of modes below the Fermi energy, which can propagate into the ballistic conductor. This behavior is illustrated in

fig. 2.10(b), where the blue shading in the band-diagram indicates the high density of transverse modes in the contacts.
In contrast to that, a completely different situation can be observed in a ballistic conductor. Not only is the density of modes much lower compared to the contacts, but the +k and -k states also exhibit noticeably different quasi-Fermi levels. This can be understood by considering fig. 2.10(c), which depicts a sketch of the variation of the electrochemical potential of the entire arrangement for an applied bias. As can be seen, the +k states are following the electrochemical potential (μ_1), whereas the -k states ensue the electrochemical potential (μ_2). If now the average of the quasi-Fermi level is considered, it can be observed, that there is a drop at the interfaces between the contacts and the ballistic conductor. According to this behavior, the quasi-Fermi level is flat inside the ballistic conductor [61]. Hence, despite ballistic transport takes place, according to the reflections at the interface, a finite conductance, denoted as contact resistance, is observed at the two interfaces between the contacts and the ballistic conductor [4]. The origin of this contact resistance is resulting from the redistribution of the current among the modes at the interface. Hence, it is important to note, that the contact resistance is not related to quantum mechanical effects, but can be attributed to the short length of the conductor, which is below the scattering mean free path l_m. In this regime, the contact resistance reaches a physical limit denoted R_{Ball} [61].
In order to calculate R_{Ball}, it is first necessary to formulate the density of states of a one-dimensional channel [66]:

$$D(E) = \frac{g_S g_V}{\pi\hbar} \sum_i \sqrt{\frac{m^*}{2(E - E_i)}} \tag{2.8}$$

where, g_S and g_V denote the spin degeneracy and valley degeneracy respectively. Further on, the current carriage of a single sub-band can be expressed as [61]:

$$I = \int_{E_F - eV}^{E_f} D(E)v(E)dE = \frac{2e^2}{h}\frac{\mu_1 - \mu_2}{e} \tag{2.9}$$

where, the factor $\frac{2e^2}{h}$ denotes the current carried per mode and unit energy by an occupied state [61]. If the number of modes (M) can be assumed to be constant over $\mu_1 > E > \mu_2$, it is possible to obtain the contact conductance by a rearrangement of the equation of the current:

$$I = \frac{2e^2}{h} M \frac{\mu_1 - \mu_2}{e} \Rightarrow G_{Ball} = \frac{2e^2}{h} M \tag{2.10}$$

Further on, the contact resistance R_{Ball} can be expressed as:

$$R_{Ball} = \frac{(\mu_1 - \mu_2)/e}{I} = \frac{h}{2e^2 M} \tag{2.11}$$

As can be seen, the contact resistance of a ballistic conductor arranged between two bulk contacts is inversely proportional to M. In order to calculate M, the cut-off energies of the different modes are required. This problem can be simplified, if the magnetic field can be assumed to be zero. In this case, the exact shape of the confining potential is not important anymore. Hence, M can be estimated by applying periodic boundary conditions. Considering an energy $E_f = \hbar {k_f}^2/2m$, only modes in the range of $-k_f < ky < k_f$ are allowed [61]. Thus the obtained modes are spaced by $2\pi/W$ and can be calculated using the integer function Int(x). The number of modes is therefore given by:

$$M = Int[\frac{k_f W}{\pi}] = Int[\frac{W}{\lambda_f/2}] \tag{2.12}$$

where, λ_f is denoting the Fermi wavelength [61].

This equation can be used to qualitatively estimate the number of occurring sub-bands in Al-Ge-Al NW heterostructures fabricated based on Ge NWs. By inserting NW diameters between 30 nm and 35 nm as well as the λ_f of Ge $\lambda_{fGe} = 10.5$ nm [36] into eq. 2.12, estimates M to be between 5 and 6.

2.4.2 Ballistic Transport in 1D Nanostructures

Electron confinement in nanostructures is strongly influenced by their shape and size. NWs, due to their elongated shape, form a quasi one-dimensional channel. Whereas there are only a few sub-bands in the transverse direction, the energy levels are much more dense in the longitudinal direction ($L_x >> L_{y,z}$). A schematic illustration of a one-dimensional nanostructure showing this geometric proportions is depicted in fig. 2.11

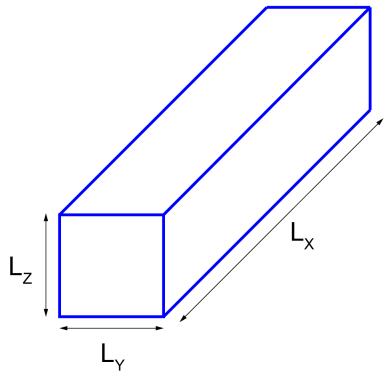

Figure 2.11: *Schematic illustration of 1D nanostructure indicating the L_X, L_Y and L_Z directions.*

Therefore, in one dimensional structures like NWs, current transport is only possible in discrete modes (sub-bands). By integrating the NW into a transistor, the occupation of the sub-bands can be controlled by applying an external gate-voltage. Hence, for certain materials at low temperatures, the conductance of their one dimensional channel reveals a regular step function, if the gate-voltage is varied [62]. By measuring the quantization of conductance, it was demonstrated that each of these spin-degenerate sub-bands contributes a conductance of $G_0 = 2e^2/h$ [67]. Since this deliberation is neglecting the magnetic field, the factor 2 in G_0 indicates that both spin polarizations are contributing equally [62]. Further on, it was proven that the formation of individual plateaus appear exactly at integer multiples of G_0 [62]. Fig. 2.12 exemplary shows the conductance in a one dimensional channel as a function of the gate-voltage revealing a regular step function. However, achieving conductance quantization in NWs is rather difficult, because a strong suppression of disorder, which is due to structural imperfections and structural states [68] between the source and drain contracts, is required [69].

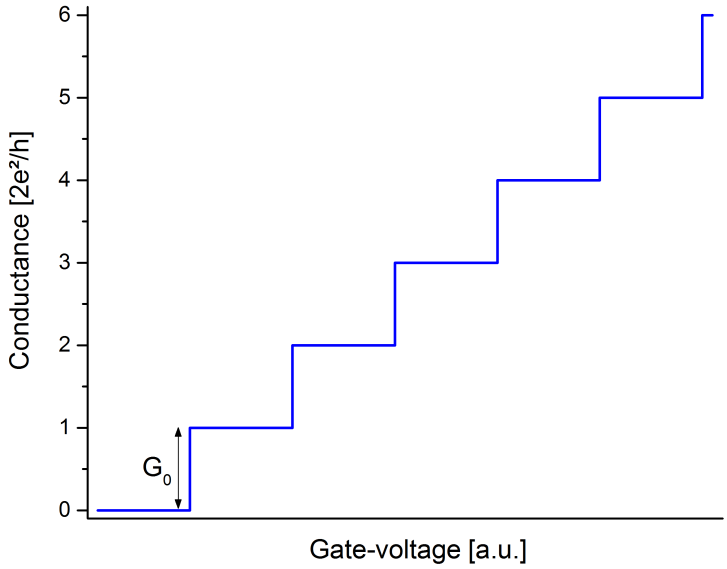

Figure 2.12: *Schematic illustration of the conductance in a one dimensional channel as a function of the gate-voltage revealing a regular step function.*

As can be seen in fig.2.13(a), these imperfections can be attributed to the radial confinement in NWs, where it is likely, that scattering at an impurity leads to a back-reflection of the electron towards the source reservoir. Moreover, close to the reservoir, this process can result in backscattering. Thus, conductance quantization is being erased [69].
In contrast to that, scattering centers outside the one dimensional constriction are not that problematic in two dimensional geometries, because only a small amount of ballistic electron trajectories are impaired. Hence, as depicted in fig.2.13(b), backscattering to the originating reservoir in 2D systems is less likely compared with 1D geometries [69].

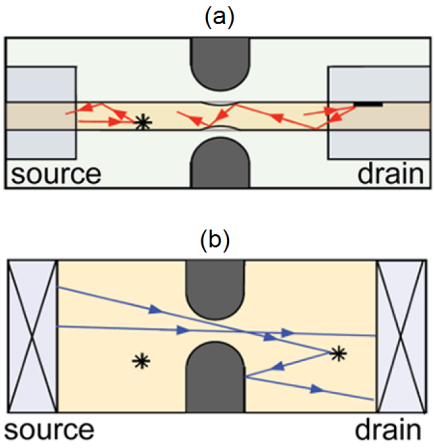

Figure 2.13: *Schematic representation of scattering in (a) 1D and (b) 2D geometries. Image adapted from [69]*

In addition to scattering related phenomena in NW based devices, degenerate sub-bands originating from the structural symmetry of cylindrical NWs have been found [70]. These degenerate sub-bands are occurring, when there are eigenenergies exhibiting equal wave-functions but different directions [71]. Since the geometry of the NW is heavily influencing the energetic spacing between the eigenenergies, it was shown that the occurrence of degenerate sub-bands, is strongly depending on the NW diameter. According to a better quantum confinement, the spacing of the eigenenergies is increasing with decreasing NW diameter [70]. As a result of degenerate sub-bands, it was demonstrated that certain conduction plateaus seam weakened or are even completely absent in conductance measurements of NW based devices [70].

Further on, there is the effect of temperature related conduction plateau broadening. This effect is assumed to be caused by a combination of thermal broadening of the electron distribution in the sub-bands and disorder broadening at the sub-band edges [71]. The combination of these effects are descried by the following thermal broadening function [70]:

$$F(E) = \frac{\partial f(E)}{\partial E} = \frac{1}{4k_BT}\ sech^2(\frac{E}{2k_BT}) \tag{2.13}$$

where, $f(E)$ denotes the Fermi function and $sech = \frac{1}{cosh(x)}$. Hence the total number of populated sub-bands taking thermal and disorder broadening into account is:

$$N_{subband}(E_F) = \int N_{subband}(E)F(E - E_F)G(E - E_F)dE \tag{2.14}$$

where, G(E) is the Gaussian distribution function:

$$G(E) = \frac{1}{c\sqrt{2\pi}} \exp(\frac{-E^2}{2c^2}) \tag{2.15}$$

with the variance c^2 [70].

Moreover, the combination of both thermal and disorder broadening should result in a shift from abrupt steps to rounded plateaus for temperatures $T > 0\,K$ [70].

2.5 Fabrication Techniques

In the last section of this chapter, theoretical aspects of the fabrication techniques required for the formation of Al-Ge-Al NW heterostructures are discussed.

2.5.1 Atomic Layer Deposition

Atomic layer deposition (ALD) is a gas phase deposition method based on sequential, self-limiting surface reactions allowing the fabrication of continuous and pinhole-free ultrathin films with high conformity [72]. Moreover, ALD features the advantage of depositing thin films with enormous aspect ratios, which are e.g. needed for highly scaled deep trench DRAM capacitors [73]. In addition, ALD allows thickness control on the monolayer level. Only limited by the size of the working chamber, it is possible to process very large substrates as well as parallel processing of multiple substrates [72]. These highly desirable characteristics meet the needs for the deposition of todays high quality high-k gate oxides such as Al_2O_3, hafnium oxide (HfO_2), titanium oxide (TiO_2) and zirconium oxide (ZrO_2) in sub 45 nm technology nodes [74]. Beyond that, ALD e.g. can be used for the fabrication of copper diffusion barriers in backend interconnects [75]. Fig. 2.14 depicts a sketch of the binary reaction sequence occurring during the ALD process. First, precursor A is introduced to the working chamber of the system and chemisorption on the surface of the sample takes place. As a result, the surface of the substrate is entirely covered with a monolayer composed of material A. Subsequently, the working chamber is flushed with inert gas to remove the residuals of precursor A. In the next step, precursor B is introduced to the working chamber. Hence, a chemical reaction with the first layer results in a formation of a monolayer of the desired material. In order to remove the residuals of the used process gases, the working chamber is flushed again with inert gas. The whole process is repeated until the required layer thickness is achieved [72].

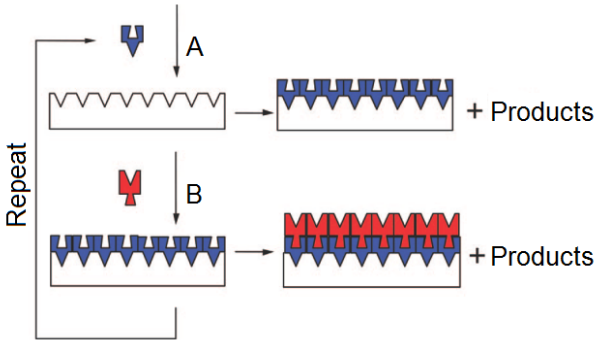

Figure 2.14: *Schematic representation of the binary reaction sequence of an ALD process: As a result of introducing precursor A to the working chamber of the ALD system, a monolayer composed of material A is formed on the surface of the sample. Subsequently, the working chamber is flushed with inert gas to remove the residuals of precursor A. Next, introducing precursor B to the working chamber triggers a chemical reaction with the first layer results in a formation of a monolayer of the desired material. In order to remove the residuals of the used process gases, the working chamber is flushed with inert gas. The whole process is repeated until the required layer thickness is achieved. Image adapted from [72]*

2.5.2 Photolithography and Lift-off Processing

One of the most important processes enabling the success use of microelectronics and particularly ICs, is photolithography. The continuous improvement of lenses combined with rapid advancements of light sources providing ever shorter wavelengths contributed to the ability to dramatically increase the number the transistors per chip [76]. Photolithography is used to transfer patterns from a mask to a substrate. This process begins with spin coating a light sensitive resist on the substrate. According to the pattern on the mask, certain areas of the resist get exposed to light, which results in soluble or insoluble areas. The resolution of lithography systems is determined by the wavelength of the exposure light λ, the numerical aperture of the lens systems NA and the factor k_1 depending on various process parameters. Eq. 2.16 depicts the resolution of the minimum achievable feature sizes [76].

$$Resolution = k_1 \frac{\lambda}{NA} \tag{2.16}$$

In contrast to positive resists, where the exposed areas get soluble after the development, for negative resists the exposed areas remain insoluble. Whereas inclined edges of positive resists are well suited for etching procedures and achieving smaller feature sizes, negative resists due to overhanging edges exhibit an advantageous lift-off behavior. Image reversal resists can be used to combine both the advantages of positive and negative resists. Hence,

the resulting structures exhibit both small features sizes and overhanging edges. The working principle of image reversal resists is depicted in fig. 2.15. First, a mask is being used to expose light on the areas that finally will remain insoluble (a). The result of this process is equal to the pattern using a positive resist (b). For the image reversal process, a moderate bake is used to make the soluble area inert (c). Subsequently, a maskless flood exposure is applied (d). As a result, the originally unexposed areas get soluble (d). The image reversal process is completed after the development, which removes the soluble parts of the resist (f) [77].

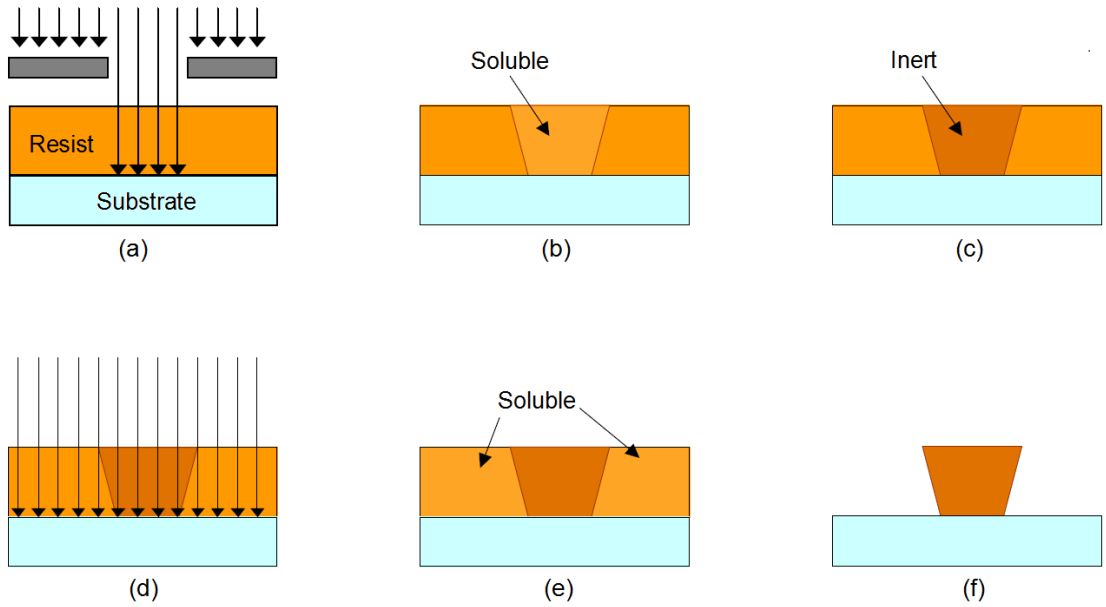

Figure 2.15: *Photolithography using an image reversal resist:*
First, a mask is being used to expose light on the areas that finally will remain insoluble (a). The result of this process is equal to the pattern using a positive resist (b). For the image reversal process, a moderate bake is used to make the soluble area inert (c). Subsequently, a maskless flood exposure is applied (d). As a result, the originally unexposed areas get soluble (d). The image reversal process is completed after the development, which removes the soluble parts of the resist (f).
Image adapted from [77]

2.5.3 Sputter Deposition

This paragraph is briefly discussing the working principle of magnetron sputtering, which is one of the most frequently applied deposition technologies for the fabrication of thin films used in microelectronics. A schematic of a magnetron sputter system is depicted in fig. 2.16. In a sputter system, the target material and the sample holder are connected to opposing terminals of a high-voltage power supply. First, to remove residual gases

the working chamber of the sputter system is pumped to base pressure, which is usually accomplished by using a turbomolecular pump. At a set working pressure, the high frequency generator is turned on and an inert plasma is ignited. This triggers a gas discharge process resulting in high energy ions bombarding the target material. As a consequence, an ejection of target atoms is subsequently followed by a condensation of the ejected atoms on the sample surface. This process is forming a thin film consisting of the target material. In order to increase the mean free path of the ejected atoms, the sputter process takes place in low pressure environments provided by vacuum chambers. By combing both a magnetic and electric field, magnetron sputtering is applied to enhance the ionization efficiency [78, 79].

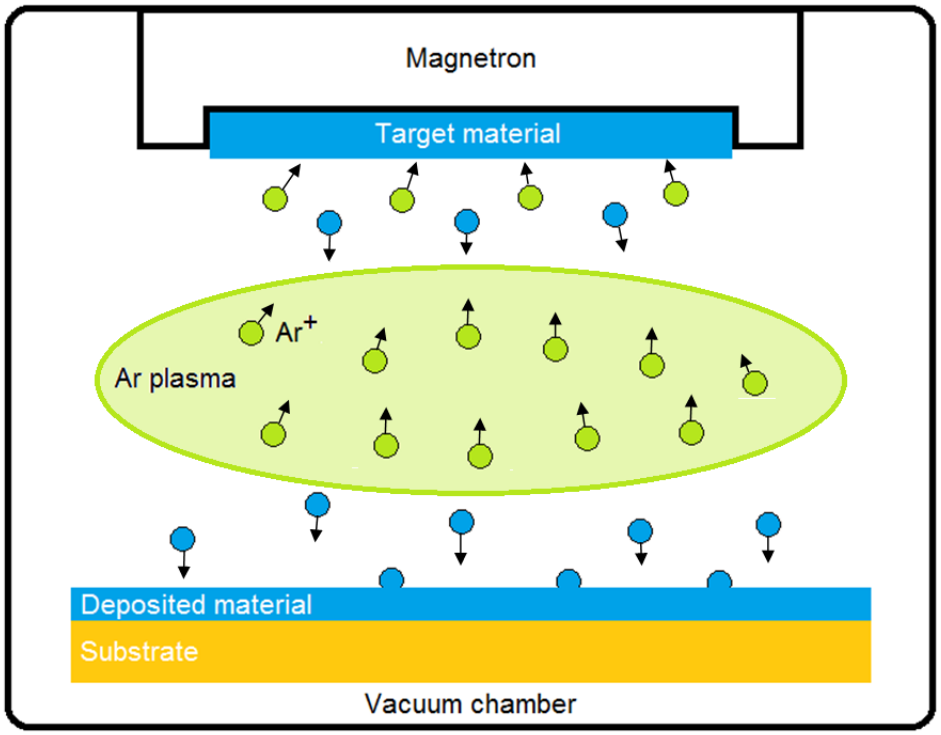

Figure 2.16: *Schematic illustration of magnetron sputtering:*
Ions ejected from an Ar plasma are accelerated towards a target consisting of the material of interest. As a result, atoms from the target are ejected and a thin film consisting of the target material is deposited on the substrate.

The "VonArdenne LS320 S" sputter system, which was used for the fabrication of the Al-Ge-Al NW heterostructures, features a 300 W RF-powered sputter source. The system is capable of holding up to 6 sputters targets, which makes it perfectly suited for multilayer deposition. In addition, the system is equipped with a substrate heater and reactive gas inlet. The max. substrate size of the system is limited to 2" samples.

2.5.4 Electron Beam Lithography

EBL is a high-resolution patterning technology capable of overcoming the resolution limits of photolithography. In contrast to photolithography, where photosensitive resists are applied, EBL patterning requires electron sensitive resists, such as Polymethylmethacrylat (PMMA). The resolution limit of EBL is not determined by electron optical system, but by spot size, electron scattering, secondary electron range, resist development and mechanical stability of the resist [80–82]. These effects limit the resolution of EBL to approximately 4 nm features and 8 nm half-pitch using conventional resists [83]. The main drawback of EBL systems are their significantly longer process times compared to photolithography. Depending on the number of structures to be exposed, the process times can range from several hours to a coupe of days. This circumstance is dedicated to the working principle of EBL, which requires the electron beam to scan over the sample with an certain amount of energy to ensure that the resist gets soluble.

2.5.5 Scanning Electron Microscopy

Scanning electron microscopy (SEM) enables the possibility to investigate structures, which are smaller than the wavelength of visible light. The basic working principle of a SEM is based on the bombardment of electrons on a specimen, as an electron beam is scanning over the surface of the sample. The detection of the resulting emission of secondary and backscattered electrons is used to obtain an image of the specimen's surface [84].

Figure 2.17: *Zeiss NEON 40EsB CrossBeam. Image taken from [85]*

Since the ultrahigh field emission SEM column of a Zeiss NEON 40EsB CrossBeam [86], seen in fig. 2.17, was used to optically verify the fabricated Al-Ge-Al NW heterostructures, the features of this system will be discussed in the following paragraph.
Beyond the usage as SEM, the Zeiss NEON 40EsB CrossBeam system also features a focused ion beam (FIB) column, enabling the possibility to investigate internal microstructures of samples. Moreover, the system allows applications such as TEM sample preparation, device modifications, failure analysis and sublayer examinations. In addition, the system also features the possibility to conduct energy-dispersive X-ray spectroscopy and particle beam induced material deposition by using a precursor gas injection system. In order to allow a full eucentric tilt of the sample, the system includes a 6-axis specimen stage. The electron beam, used for the SEM operation, is generated by a Shottky field emission gun, which allows high brightness and low energy spread as well as a small virtual source diameter. Directly below the gun area, a magnetic condenser lens is used for adjusting the optimum beam aperture of low voltage operation. Subsequent to the magnetic condenser lens, a combination of a magnetic objective lens and electrostatic immersion lens is used for forming a crossover free beam path with minimized energy spread [86].

Chapter 3

Experimental Techniques

This chapter is describing the experimental techniques and process parameters for the fabrication of Al-Ge-Al NW heterostructures with ultrashort Ge segment lengths.
In order to allow electrical characterizations of the fabricated Al-Ge-Al NW heterostructures, the device integration strategy involves using a measurement module consisting of macroscopic Au contacts patterned on a highly doped Si substrate with a dielectric layer on top. Drop-casting of Ge NWs on this measurement module enables the possibility of choosing only NWs with a suitable geometry. Further on, the combination of EBL, sputter deposition and lift-off techniques, was used to connect particular NWs with Al pads. By introducing an RTA induced controlled reaction between the VLS grown Ge NWs and the Al contact pads, Al-Ge-Al NW heterostructures with ultrashort Ge segments were formed.
In addition to the fabrication of Al-Ge-Al NW heterostructures, this chapter is also discussing the measurement setups for conducting the electrical characterization procedure of the devices at room temperature as well as cryogenic temperatures.

3.1 Fabrication of Al-Ge-Al NW Heterostructures

This paragraph discusses the fabrication of Al-Ge-Al NW heterostructures based on unpassivated as well as passivated Ge NWs. For reasons of simplicity, the process flow for the fabrication of unpassivated Al-Ge-Al NW heterostructures is addressed prior to the discussion of passivated devices.
First, a small piece of a Si growth substrate with VLS grown Ge NWs is cleaved. Further on, ultrasonication was used to transfer the Ge NWs into a liquid solution, which was then used for drop-casting the Ge NWs onto a measurement module featuring macroscopic Au contacts. Al contacts were used to fabricate individual connections between the Ge NWs and the macroscopic Au pads on the measurement module. The Al metalization also serves as source for the diffusion of Al into the Ge NWs. In order to realize these Al contacts, a combination of EBL, hydroiodic acid (HI) dip to remove the native Ge oxide at the contact between the Ge NW and the Al metalization, Al sputter deposition and lift-off process was applied. Subsequently, RTA was used to induce a diffusion process leading to Al-Ge-Al heterostructures exhibiting ultrasmall Ge segments with abrupt metal semiconductor interfaces. The success of the fabrication process was confirmed using SEM.

In order to fabricate Al-Ge-Al NW heterostructures based on Ge NWs passivated with 20 nm Al_2O_3, the aforementioned process flow of unpassivated devices was adapted. Passivating Ge NWs with a high quality high-k dielectric is motivated by preventing surface defects and adsorbates like H_2O in the unstable oxide shell of the Ge NWs, which would alter the electrical characteristic of the devices [87, 88]. In order to allow an all-around passivation of the Ge NWs, 20 nm of Al_2O_3 were deposited on the Si growth substrate with VLS grown Ge NWs. The Al_2O_3 passivation layer was fabricated by ALD in a Cambridge NanoTech Savannah 100 with the precursor gases trimethylaluminium (C_3H_9Al) and water (H_2O). The passivated Si growth substrate with grown Ge NWs was then used for depositing the Ge NWs onto the measurement module. Moreover, to allow an electrical connection between the Ge NW and the Al metalization, in addition to the HI dip, the passivation layer at the contact area had to be removed prior to the Al sputter deposition. This was done by performing a buffered hydrofluoric acid (BHF) dip. All further processes including EBL, HI dip, Al sputter deposition and lift-off process as well as the RTA induced heterostructure formation were adopted from the fabrication scheme of unpassivated Al-Ge-Al NW heterostructures.
The entire process flow for both device architectures is depicted in fig. 3.1.

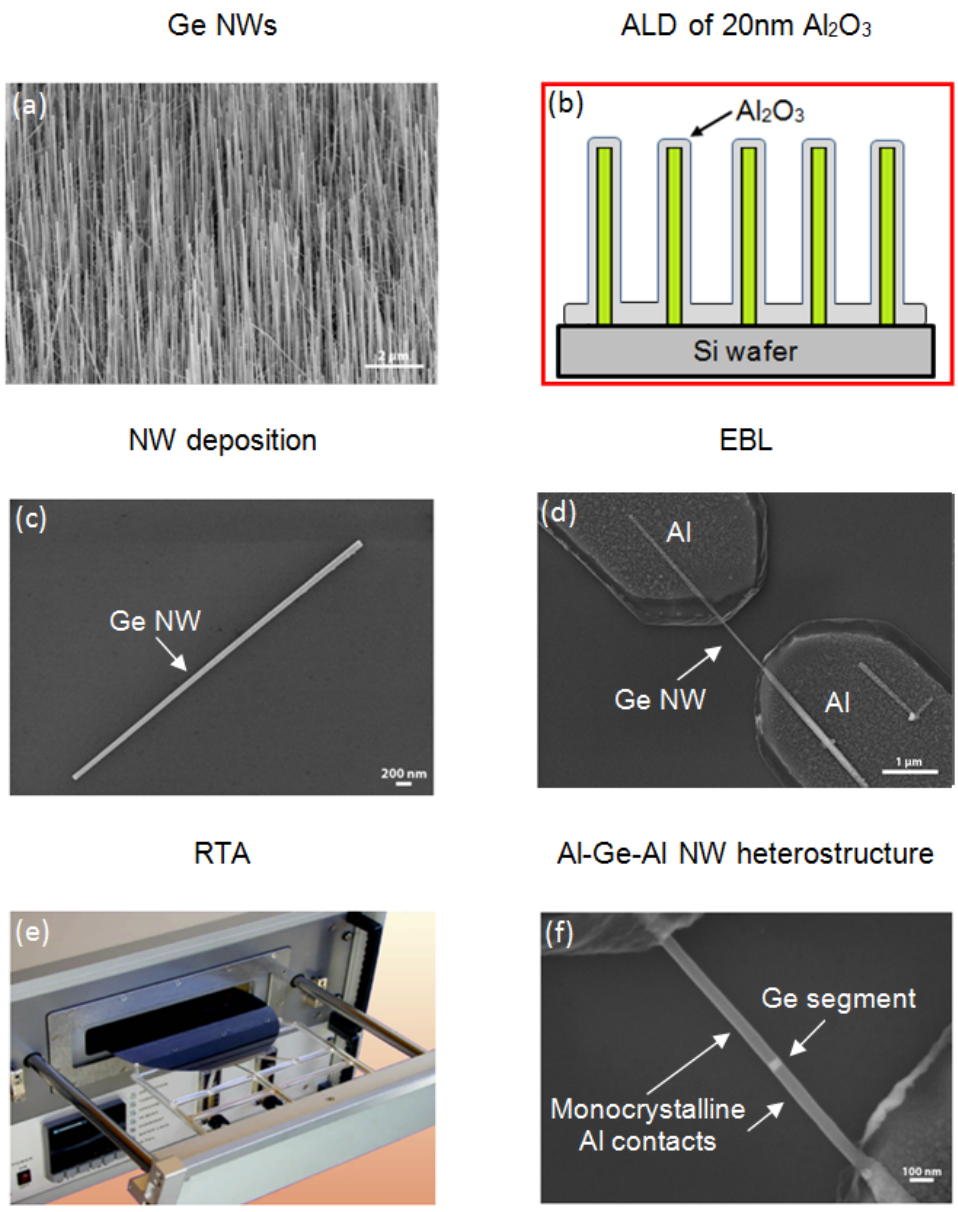

Figure 3.1: *Formation of Al-Ge-Al NW heterostructures:*
In order to use Ge NWs passivated with a high quality high-k dielectric, the Si growth substrate with grown Ge NWs (a) was passivated with 20 nm *of* Al_2O_3 *(b). The passivated Si growth substrate was then used for drop-casting the NWs on the measurement module (c). Further on, a combination of EBL, HF etching of the* Al_2O_3 *layer at the contact area, HI dip, sputter deposition and a lift-off process was applied for the fabrication of Al contracts to particular Ge NWs (d). Subsequently, RTA was used to induce a diffusion process leading to Al-Ge-Al heterostructures passivated with* 20 nm *of* Al_2O_3 *(e). A SEM image of the completed Al-Ge-Al NW heterostructure based on passivated Ge NWs is depicted in (f).*

3.2 Measurement Module

The measurement module allows electrical characterization of individual Al-Ge-Al NW heterostructures. Moreover, the measurement module was necessary for measurements at cryogenic temperatures, which required macroscopic pads for wire bonding. In order to allow the fabrication of back-gated Al-Ge-Al NW heterostructures, the measurement module consists of a highly p-doped Si substrate with a SiO_2 layer on top. As can be seen in fig. 3.2, the measurement module exhibits different macroscopic Au contact structures. There are 19 "hex-pad structures" each consisting of 6 macroscopic Au pads (blue). In addition, the measurement module features differently shaped back-gate contacts (orange), which are connected to the p-doped Si substrate below the SiO_2 layer.

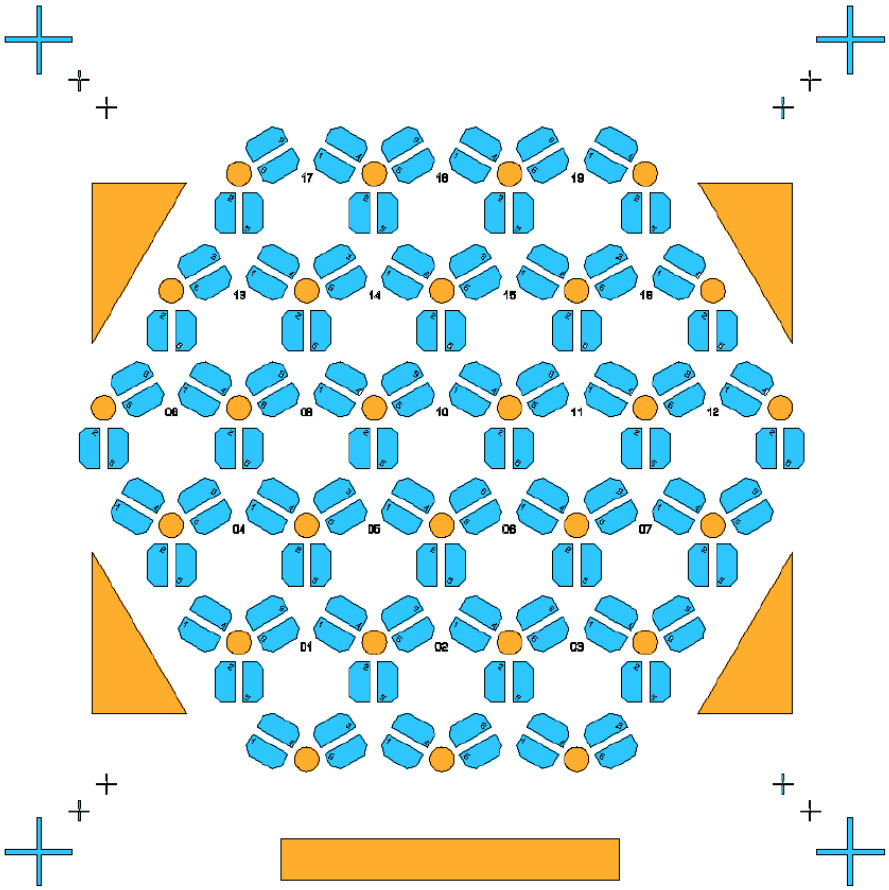

Figure 3.2: *Schematic illustration of the measurement module: There are 19 "hex-pad structures" each consisting of 6 macroscopic Au pads (blue). Further on, differently shaped back-gate contacts (orange) are connected to the highly p-doped Si substrate below the SiO_2 layer. The marker structures in the corners of the measurement module ensure accurate lithography alignments.*

Regarding the fabrication of the measurement module, a highly p-type doped 500 µm thick <100>-oriented Si wafer with 100 nm thermally grown SiO_2 on top was used as substrate material.
In oder to pattern the macroscopic Au contacts on the measurement module, a combination of photolithography using Cr hardmasks, image reversal resist (AZ5214) and developer solution (AZ726MIF) was applied. Photolithography was conducted using a MJB3 mask aligner from Karl Süss MicroTec AG. The used mask aligner system features a 275 W mercury short-arc lamp exposing light with 450 nm, allowing minimal feature sizes of 0.8 µm.
To finalize the measurement module, the macroscopic Au pads were fabricated by Ti/Au deposition via magnetron sputtering with the "VonArdenne LS320 S" sputter system.
Subsequent to the sputter deposition, a lift-off process was used to remove the excess metal.
A detailed listing of all process parameters, used for the fabrication of the measurement module, can be found in appendix A.1.
In order to motivate using the aforementioned measurement module, fig. 3.3 depicts a schematic illustration of the completed measurement module with a connected Al-Ge-Al NW heterostructure based on passivated Ge NWs. As can be seen, the macroscopic Au pads of the measurement module extend the electron beam lithography patterned Al contacts of the Al-Ge-Al NW heterostructure. In combination with the macroscopic back-gate contacts, it is possible to operate the connected devices as back-gated FETs. Further on, the macroscopic contacts are needed for measurements with a cryostat setup, which requires wire bonds from the macroscopic pads to a printed circuit board (PCB).

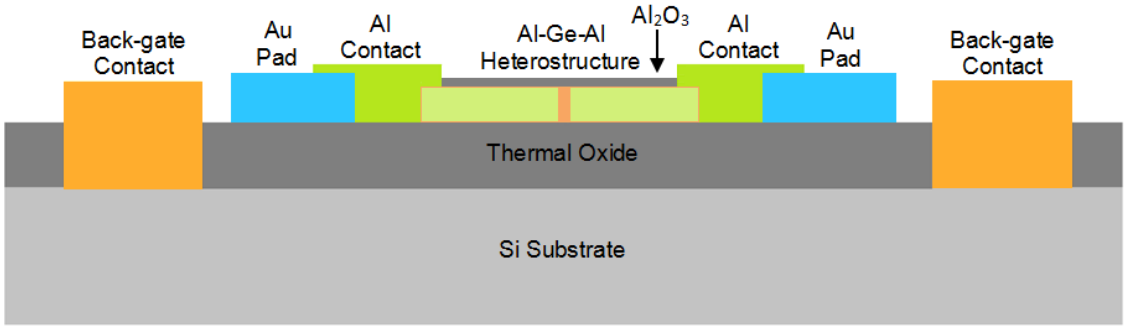

Figure 3.3: *Schematic illustration of the measurement module with connected Al-Ge-Al NW heterostructure. In this configuration the the Al-Ge-Al NW heterostructures can be operated as back-gated FETs. Further on, the macroscopic contacts of the measurement module are needed for measurements with a cryostat setup, which requires wire bonds from the macroscopic pads to a PCB.*

3.3 Nanowire Deposition

A SEM image of the used Si growth substrate with VLS grown Ge NWs at a magnification of approximately 20.000 × at a 45° tilt angle is shown in fig. 3.4.

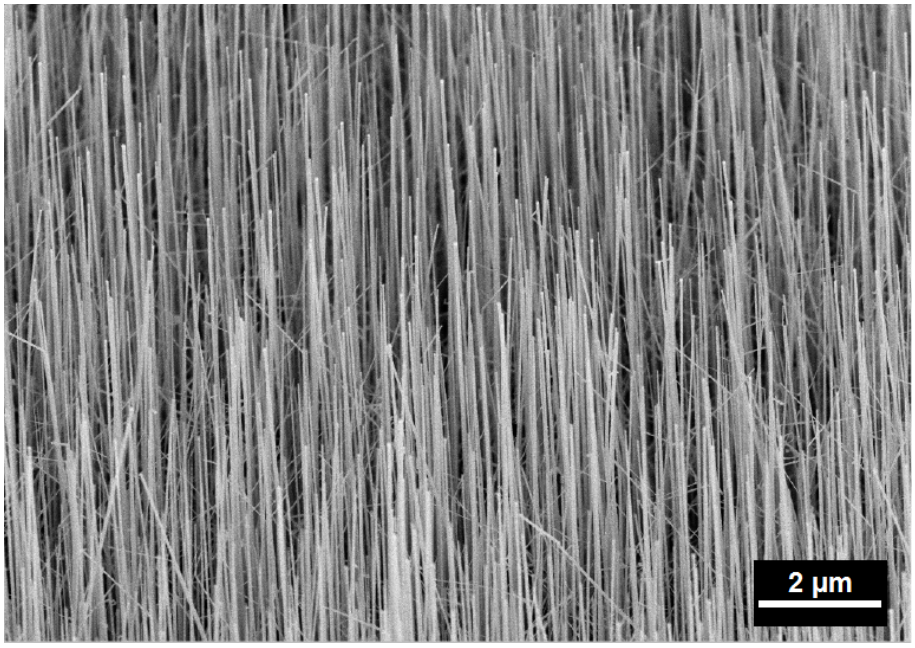

Figure 3.4: *SEM image of unpassivated VLS grown Ge NWs recorded at a* 45° *tilt angle: The majority of the NWs are approximately* 7 µm *long and exhibit diameters between* 25 nm *and* 70 nm. *The image was recorded at a magnification of approximately* 20.000 ×.

In order to integrate passivated Ge NWs into the measurement module, a piece of a passivated Si growth substrate with VLS grown Ge NWs was cleaved and dispersed in isopropanol. To harvest the NWs, the dispersed Si growth substrate was put into an ultrasonic bath for 120 s at 30 % power. After that, 4 µL of the NW containing solution were drop-casted on the measurement module using a micropipette. Subsequently, the substrate was carefully dried with nitrogen. As a result, the NWs are randomly distributed on the measurement module. Applying a directed nitrogen stream enables the opportunity to give the NWs a preferred direction during the drying process. Fig. 3.5 depicts a schematic representation of the entire NW deposition process. The success of this procedure was observed by using light microscopy. The deposition process was repeated until the NW density on the measurement module was adequate to find enough NWs suitable for further processing. After the deposition process, SEM was used to investigate the deposited NWs in terms of length and diameter.

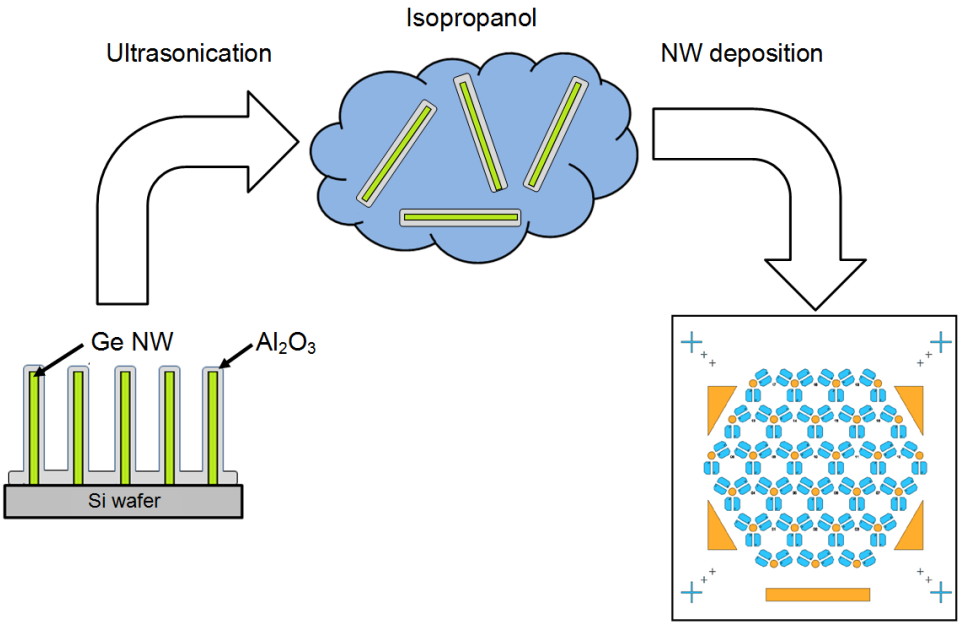

Figure 3.5: *Schematic illustration of the NW deposition process by drop-casting: The Ge NWs were harvested by ultrasonication of the in isopropanol dispersed growth substrate. Subsequently, the Ge NWs were drop-casted on the measurement module.*

3.4 Electric Contact Formation

Patterning of the Al contacts connecting the macroscopic Au pads with the deposited Ge NWs was achieved by using a combination of a "Raith eLiNE" EBL system and a positive resist (PMMA). The used EBL system features a piezo stage allowing precise movement during the alignment and exposure process in 5 nm steps.
Subsequently to the search of appropriate Ge NWs, a PMMA resist (AR-P 679.04) was spin coated on the sample, which was then baked for 900 s at 443 K. Further on, contacts with contact gaps between 1.2 µm and 1.6 µm were manually drawn. After the exposure, the EBL process was completed by dipping the sample for 35 s in the developer solution (AR 600-56). This was subsequently followed by a 10 s dip in the stopper solution (AR 600-60). Finally, the sample was dried with nitrogen.
In order to establish a conductive connection between the Ge NWs and the Al contacts deposited by a magnetron sputter process, the ALD grown Al_2O_3 had to be removed by etching BHF.
Exposed to ambient air, Ge forms a few nanometer thin native oxide layer of both germanium monoxide (GeO) and germanium dioxide (GeO_2). To enable an electrical contact between the Al metalization and the Ge NWs, both oxide layers had to be removed prior to the Al sputter deposition. In contrast to GeO_2, which is soluble in water, the GeO layer on the NWs required etching by dipping the sample in 14 % diluted HI [89].

After the HI dip, magnetron sputtering with the "VonArdenne LS320 S" sputter system was applied for the deposition of a 100 nm thick Al layer. To finalize the fabrication of the Al contacts, the excess metal was removed from the sample by a lift-off process.
A detailed listing of all process parameters of the EBL is provided in appendix A.2.
Fig. 3.6 depicts an SEM image showing an individual Ge NW connected to the macroscopic Au electrodes.

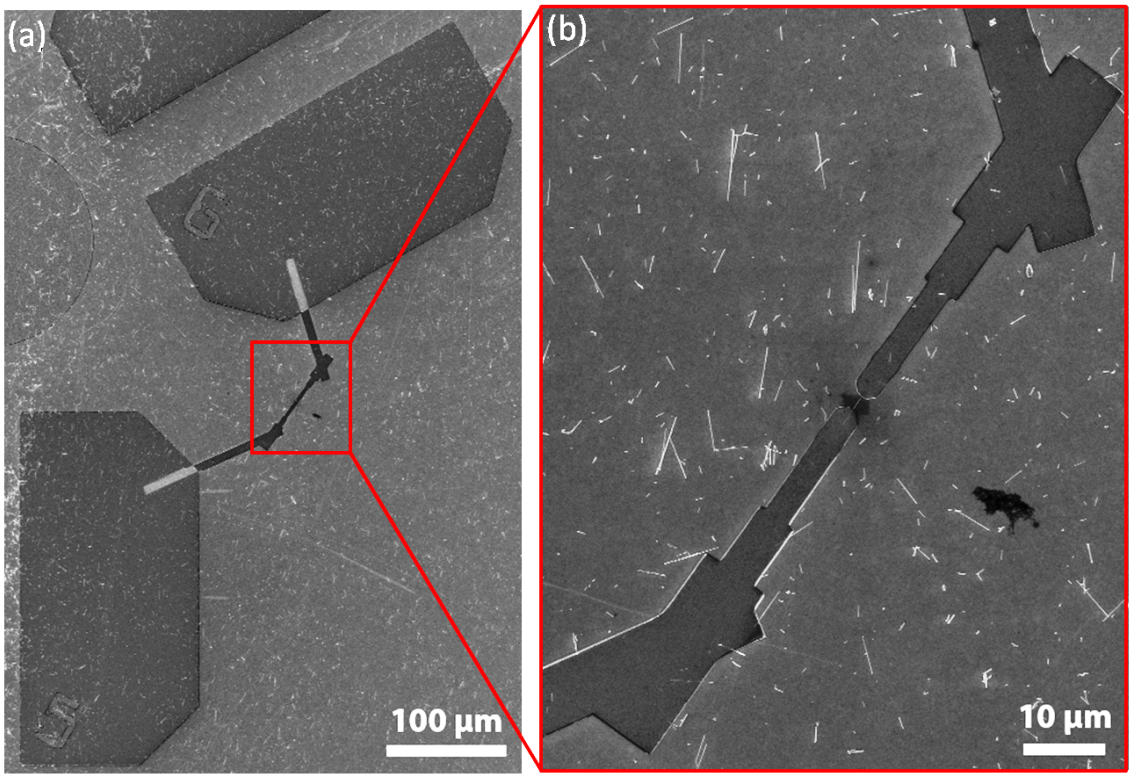

Figure 3.6: *SEM images of contacts on the measurement module: (a) SEM-image showing an Al-Ge-Al-NW heterostructures connected to the macroscopic Au contacts of the measurement module, (b) Detailed view of the Al contacts of one heterostructure device.*

3.5 Thermal Induced Substitution of Ge NWs by Al

Controlled diffusion from the Al contacts into Ge NWs was activated by an annealing process conducted in a RTA system.
As a result, Al-Ge-Al NW heterostructures with abrupt interfaces between the monocrystalline Al leads and the Ge segment were fabricated [59, 60]. The length of the remaining Ge segment can be controlled by the annealing time and temperature. Further on, the Ge segment length also appeared to be deepening on the diameter and surface roughness of the used Ge NWs [59, 60]. Moreover, by designing different contact gaps between the Al

contacts, it was possible to fabricate samples with Al-Ge-Al NW heterostructures featuring Ge segment lengths between 10 nm and 400 nm. Average diffusion rates of Al into the Ge NWs were experimentally determined between 2.5 nm s^{-1} and 4 nm s^{-1}.

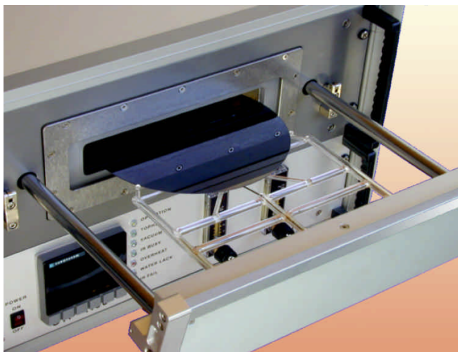

Figure 3.7: *UniTemp UTP 1100 RTA system. Image taken from [90]*

The used UniTemp UTP 1100 RTA oven, seen in fig.3.7, uses 18 kW infrared lamps capable of achieving temperatures exceeding 1200 K. The maximum ramp-up rate of the system is limited to 75 K s^{-1}. Further on, the quartz chamber of the oven is hermetically sealed and allows the processing of a 6" wafer, which can be manually loaded by a quartz tray. In addition to a vacuum system, the RTA system also allows a purging of the oven with N or forming gas to ensure a clean environment in the process chamber. To provide adequate energy to initiate the diffusion process, the working temperature was set to 624 K.
A detailed listing of all RTA parameters can be found in appendix A.3.
The final inspection of the fabricated Al-Ge-Al NW heterostructures was done by SEM using a combination of the "InLens" and "SE2" detector. Fig. 3.8 depicts a schematic of the completed Al-Ge-Al NW heterostructure device after RTA.

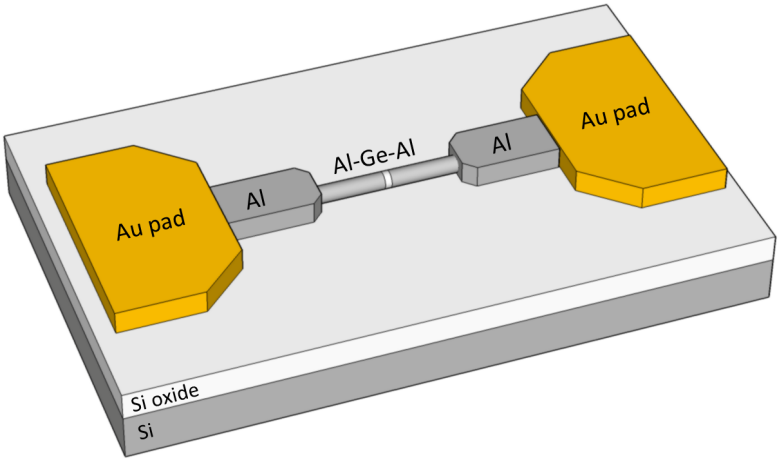

Figure 3.8: *Schematic illustration of a completed Al-Ge-Al NW heterostructure device with an ultrashort Ge segment after the RTA induced substitution of Ge by Al.*

3.6 Electrical Characterization

The electrical measurements at room-temperature and ambient atmosphere were performed using a combination of an "HP 4156B Precision Semiconductor Parameter Analyzer" featuring four independent source measure units (SMUs) and a probe station with four tungsten carbide test prods. In order to minimize the influence of the ambient light as well as electromagnetic fields on the devices under test, the needle probe station was placed in a dark box. Further on, a stereoscope was applied to precisely establish connections between the macroscopic Au pads and the test prods. In order to save the measurement data, the HP 4156B either allows to store the data on a floppy disk or features the possibility to send the data via GPIB port to a PC. Fig. 3.9 depicts a photo of the used needle probe station with the dark box and the HP 4156B measurement unit.

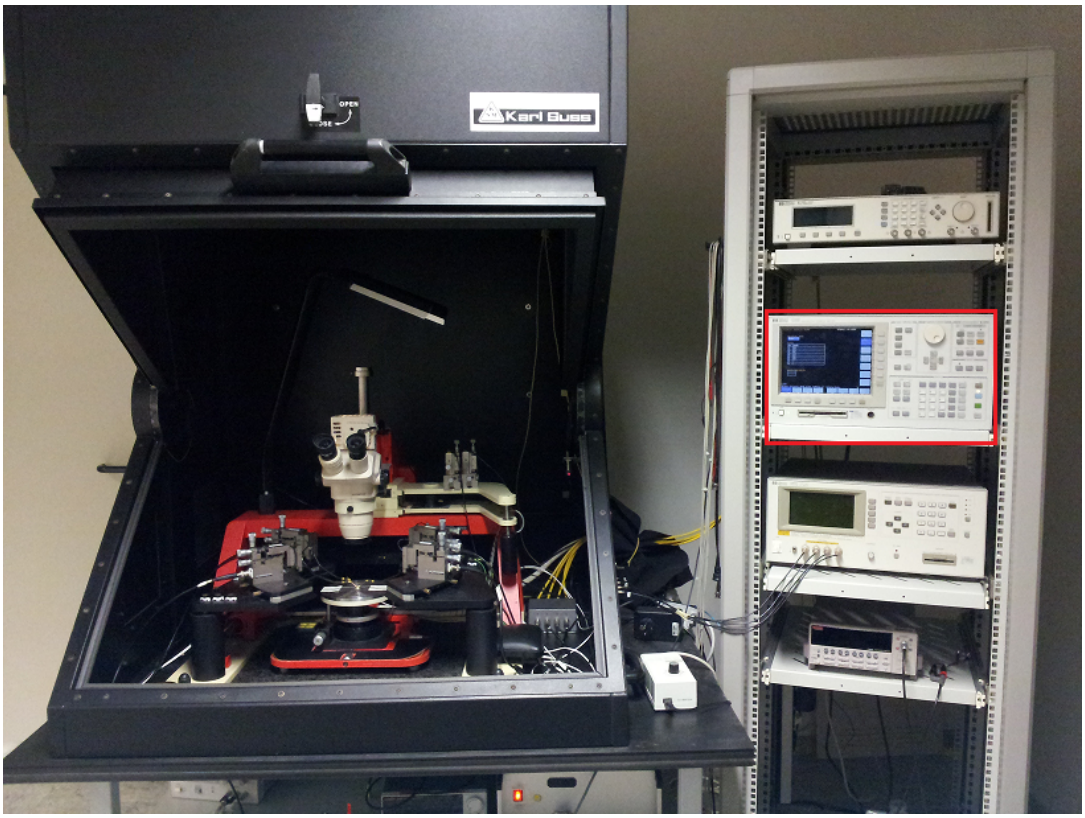

Figure 3.9: *Needle probe station with dark box and connected HP 4156B Precision Semiconductor Parameter Analyzer used for measuring the I/V characteristic as well as the transfer characteristics of the fabricated Al-Ge-Al NW heterostructure devices. The HP 4156B is highlighted in red.*

3.6.1 I/V Characteristic Measurements

In order to measure the current-voltage (I/V) characteristic of Al-Ge-Al NW heterostructures at room temperature and ambient atmosphere, the aforementioned measurement setup consisting of the HP 4156B analyzer and the needle probe station was recorded by 2T measurements.
Since only 2T measurements were conducted, the measured data contains a series resistance originating from the Al contacts between the Au pads and the Al-Ge-Al NW heterostructure as well as the monocrystalline Al leads contacting the Ge segment. Although conducting 4T measurements would eliminate the contact resistance of the devices, the resistance of the Schottky barriers, which connect the Ge segment with the monocrystalline Al leads, can not be excluded. Beside the increased process complexity, this was one of the most crucial factors for maintaining 2T measurements.
A schematic illustration of the measurement setup for measuring the I/V characteristic is depicted in fig. 3.10. Depending on the Ge segment length of the Al-Ge-Al NW heterostructures, the I/V characteristics of the devices was investigated for a V_{DS} in the measurement range between in the between 1 V and 5 V by sweeping the drain-source voltage V_{DS} in 5 mV steps and measuring the source-drain current I_{DS}. For all devices, the measurements were conducted for different back-gate voltages V_{BG} between -15 V and 15 V.

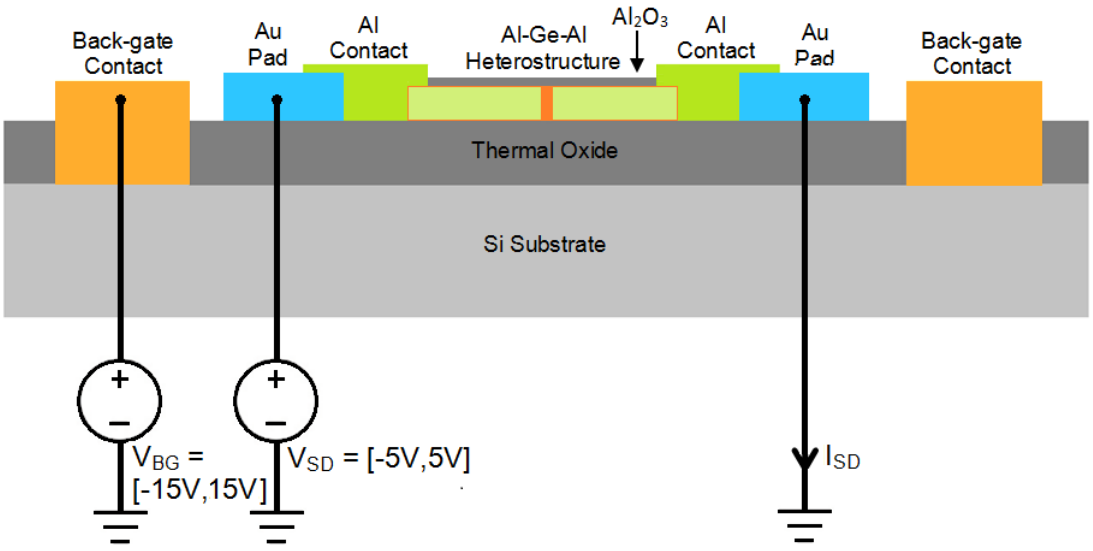

Figure 3.10: *Configuration for I/V characteristic measurements: I_{DS} was recorded in 5 mV steps in the range of $V_{SD} = [-5\,\mathrm{V}; 5\,\mathrm{V}]$ for $V_{BG} = [-15\,\mathrm{V}, 0\,\mathrm{V}, 15\,\mathrm{V}]$.*

3.6.2 Transfer Characteristic Measurements

In order to investigate the electrostatic modulation capability of Al-Ge-Al NW heterostructures at room temperature and ambient atmosphere, the transfer characteristic of the devices was recored by 3T using the aforementioned measurement setup consisting of the HP 4156B analyzer and the needle probe station.
A schematic illustration of the used measurement configuration for recording the transfer characteristic is depicted in fig. 3.11. As can be seen, for this setup, the Al-Ge-Al NW heterostructure is reassembling a back-gated FET. Hence, the charge carrier concentration in the Ge segment can be electrostatically modulated by sweeping the back-gate voltage V_{BG}. In order to record the transfer characteristics of the Al-Ge-Al NW heterostructures, the waveform of I_{SD} was recorded for a fixed V_{DS} while V_{BG} was varied in 30 mV steps between -15 V and 15 V. Depending on the Ge segment length of the Al-Ge-Al NW heterostructures, V_{DS} was fixed to 1 mV or 10 mV. In oder minimize charging effects of parasitic capacities during the measurements, an initial hold-time of 5 s as well as a 250 ms delay-time between the measurement points were set.
Further on, to investigate the time depended behavior of the devices, the same measurement setup was also used for recording transient measurements. For these investigations, V_{BG} was varied in different time intervals and I_{SD} was recorded for a fixed V_{DS}.

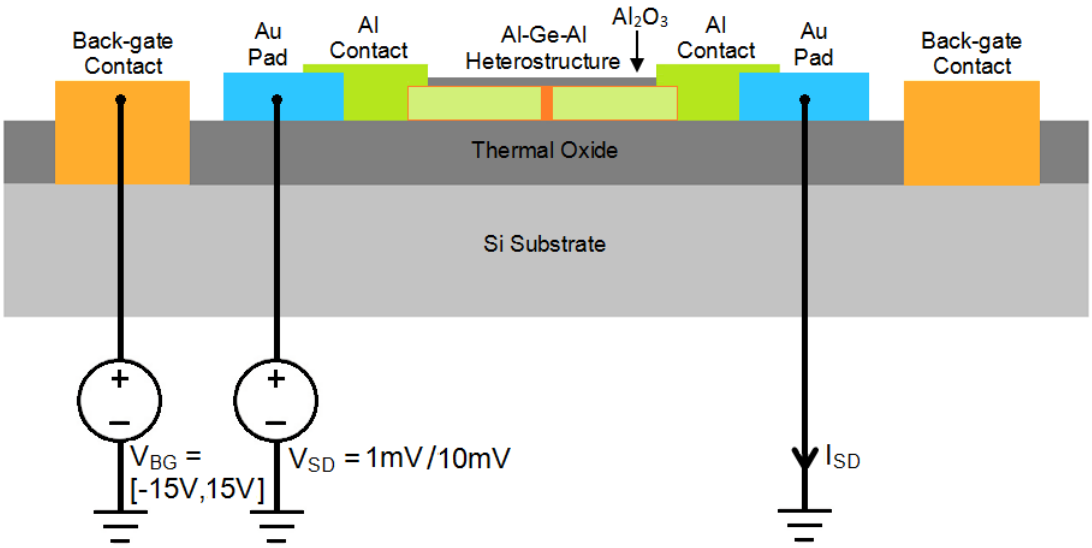

Figure 3.11: *Configuration for measuring transfer characteristic of Al-Ge-Al NW heterostructures: For this setup, the Al-Ge-Al NW heterostructure is reassembling a back-gate FET. The transfer characteristic was recorded in* 30 mV *steps in the range* $V_{BG} = [-15\,\mathrm{V}; 15\,\mathrm{V}]$ *for a constant bias of* $V_{DS} = 1\,\mathrm{mV}$ *or* 10 mV.

3.6.3 Electrical Characterizations at Cryogenic Temperatures

Investigating ballistic transport phenomena in Al-Ge-Al NW heterostructures requires low temperature and thus vacuum conditions. Therefore, fig. 3.12 depicts a schematic illustration of the setup for cooling the sample down to cryogenic temperatures using liquid helium (He) or liquid nitrogen (LN_2).

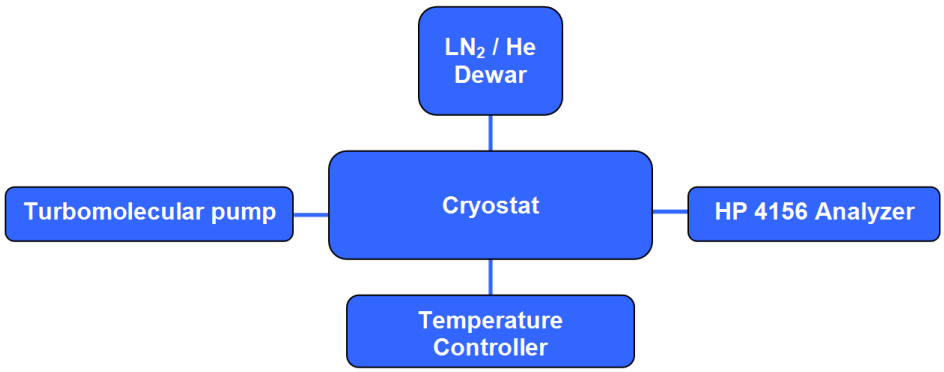

Figure 3.12: *Schematic illustration of the experimental setup for conducting measurements at cryogenic temperatures.*

Whereas for measurements down to T = 5 K liquid He was required, LN_2 embodies an uncomplicated approach to conduct measurements in the temperature range between 78 K and 300 K. Fig. 3.13(a) depicts a photo of the cryostat mounted on a vertically adjustable stage. The measurement temperatures were adjusted using a "Cryo Con 32B temperature controller". Moreover, the temperature controller was also required for temperature stabilization during the measurements. In order to monitor the set temperatures, the cold finger of the used cryostat featured a temperature sensor enabling an accurate temperature measurement in the immediate surroundings of the sample. To prevent damage by freezing of the sample at cryogenic temperatures, the measurement chamber of the cryostat was evacuated to a pressure of approximately 10^{-6} mbar using a turbomolecular pump.
Instead of using the needle prober setup, discussed in 3.6, applying the aforementioned setup for electrical measurements enables the possibility to have significantly lower noise levels during the measurements. This is dedicated to the stable conditions in vacuum environments such as e.g. the absence of humidity. Further on, the reduction of thermal fluctuations in low temperature environments is also contributing to lower noise levels.
In order to conduct both the measurements of the I/V characteristic (fig. 3.10) as well as the transfer characteristics (fig. 3.11), the "HP 4156B Precision Semiconductor Parameter Analyzer" was connected with the cryostat via its 12 vacuum feed-throughs. All temperature depending measurements were conducted beginning with T = 5 K.

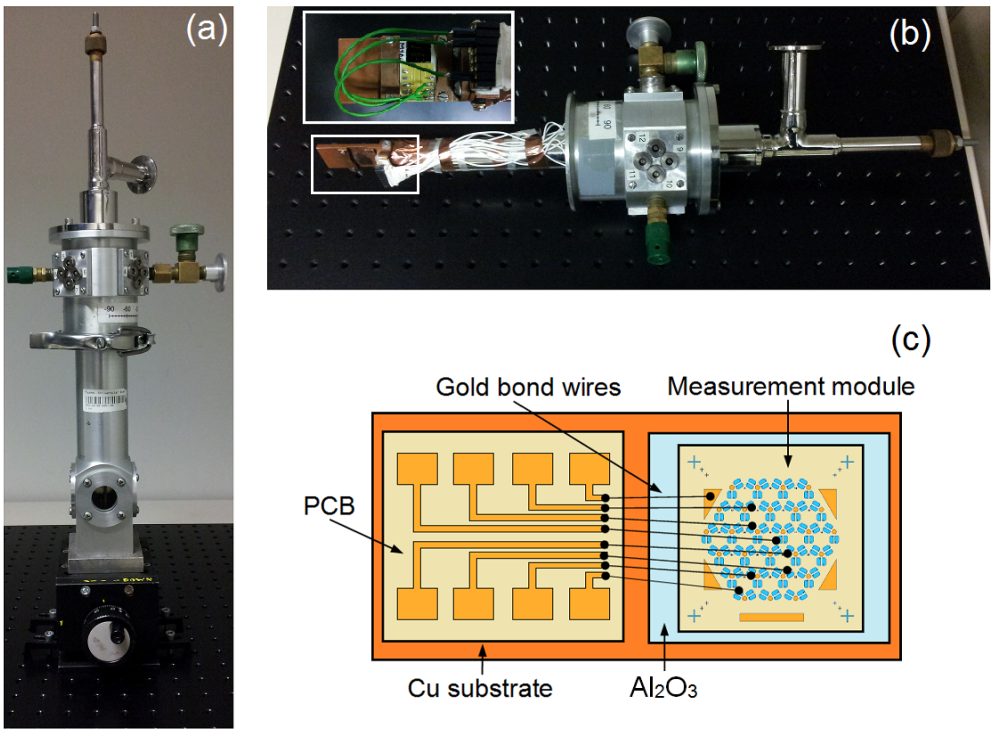

Figure 3.13: *Setup for electrical characterization at cryogenic temperatures:*
(a) Cryostat mounted on a vertically adjustable stage,
(b) Detailed view of the sample holder on the cold finger of the cryostat
(c) Schematic illustration of the measurement module mounted on the Cu substrate

The cryogenic measurements required mounting the measurement module on a (2.5 x 1.5) cm^2 Cu substrate fitting to the sample holder slot of the cryostat, which can be seen in fig. 3.13(b). Moreover, the Cu features perfect physical properties as a substrate material such as good thermal conductance and mechanical stability. In order to allow 3T back-gate measurements, it was mandatory to isolate the measurement module from the highly conductive Cu substrate. This was done by gluing a approximately 1 mm thick Al_2O_3 plate between the measurement module and the Cu substrate using silver conductive paint. Further on, a PCB with a soldered on socket strip was glued on the Cu substrate using epoxy resin. Next, the Al-Ge-Al NW heterostructures as well as the back-gate contact on the measurement module were connected with the PCB by using wire bonding between the conducting paths of the PCB and the macroscopic Au pads. A draft of the mounted measurement module is depicted in fig. 3.13(c). A detailed description for mounting the sample into the cryostat is provided in appendix A.4.

Chapter 4

Results and Discussion

In this chapter, the experimental results regarding the formation of Al-Ge-Al NW heterostructures and their corresponding electrical characterization at room temperature and cryogenic temperatures down to 5 K is addressed.
In order to allow interpretation and to gain a better insight into the measurement results of the investigated Al-Ge-Al NW heterostructures, simulations based on the 2D Schrödinger equation concerning the diameter depending quantum confinement effects of Ge NWs were conducted. A comparison between the simulations and the experimental data of conductance measurements in the temperature range between 5 K and 300 K is discussed.

4.1 Formation of Al-Ge-Al NW Heterostructures

4.1.1 Al-Ge-Al NW Heterostructures

As mentioned in chapter 3, for reasons of reduced fabrication complexity and to gain a better insight in the heterostructure formation process, the first device generation involved Al-Ge-Al NW heterostructures based on Ge NWs without passivation. By designing different contact gaps between the Al contacts, it was possible to fabricate samples with Al-Ge-Al NW heterostructures featuring Ge segment lengths between 15 nm and 300 nm. A selection of Al-Ge-Al NW heterostructures based on unpassivated Ge NWs with Ge segment lengths between 15 nm and 310 nm is depicted in fig. 4.1.

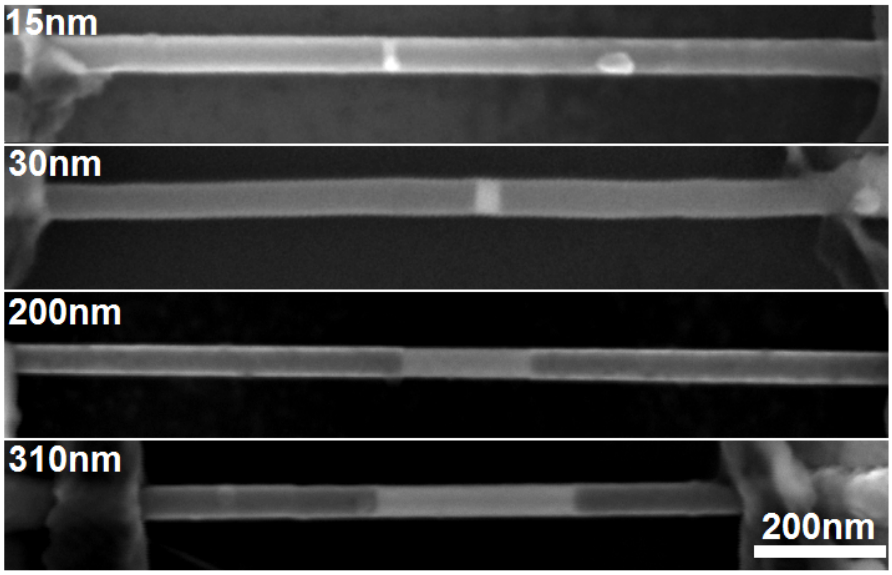

Figure 4.1: *Compilation of SEM images showing Al-Ge-Al NW heterostructures with Ge segment lengths between* 15 nm *and* 310 nm*. The images were recorded at* 150.000 × *magnification.*

In order to show a detailed view of an Al-Ge-Al NW heterostructure with an ultrasmall Ge segment integrated into the measurement module, fig. 4.2(a) depicts the SEM image of an Al-Ge-Al NW heterostructure with a 30 nm long Ge segment connected to the Al metalization that connects the heterostructure device with the top contacts of the measurement module. In addition, fig. 4.2(b) shows a detailed view of the same device clearly showing an abrupt interface between the monocrystalline Al leads and the Ge segment.

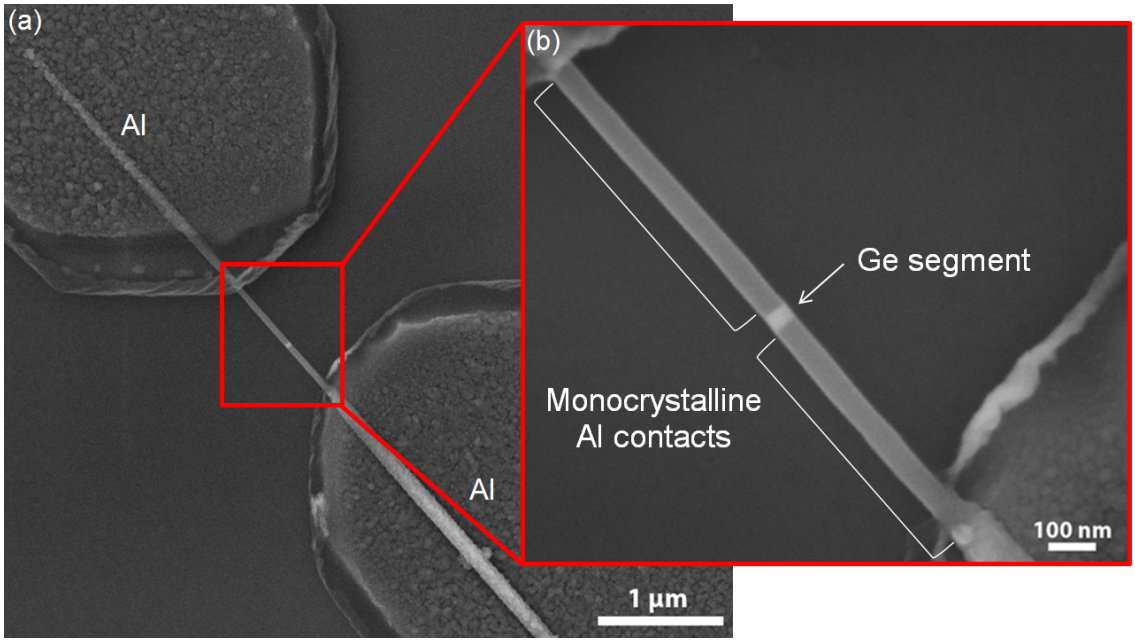

Figure 4.2: *SEM images of an Al-Ge-Al NW heterostructure with a* 30 nm *long Ge segment: (a) SEM image at* 40.000 × *magnification showing the heterostructure device integrated in the measurement module by Al contacts. (b) SEM image depicting a detailed view of the Al-Ge-Al NW heterostructure at* 200.000 × *magnification clearly showing the monocrystalline Al leads connecting the Ge segment.*

4.1.2 TEM Investigation of the Al-Ge Interface

In order to discuss the interface between the Ge segment and the monocrystalline Al leads, fig. 4.3(a) depicts a high-angle annular dark field scanning transmission electron microscopy (HAADF STEM) image of the Al-Ge interface. As can be seen, there is a strong chemical contrast between the unreacted Ge NW (dark) and the monocrystalline Al (bright). Moreover, fig. 4.3(b) depicts a high-resolution transmission electron microscopy (HRTEM) image, with the most prominent lattice planes of the Al-Ge interface indicated. Since the Ge part was oriented in the [110] direction of observation, the corresponding reciprocal lattice peaks obtained from the conducted Fourier transformation (FFT) in fig. 4.3(c) reveal a <111> growth direction with a diamond cubic structure. In contrast, the FFTs of the monocrystalline Al, depicted in fig. 4.3(d), reveal only one family of planes, corresponding to the <111> planes of the fcc structure of Al [59].
Further on, the in-situ observation of the RTA induced diffusion of Al in Ge NWs has clearly revealed, that a substitution of Ge by Al rather than the formation of new phases is the dominating the diffusion process in the investigated Al-Ge material system [59].

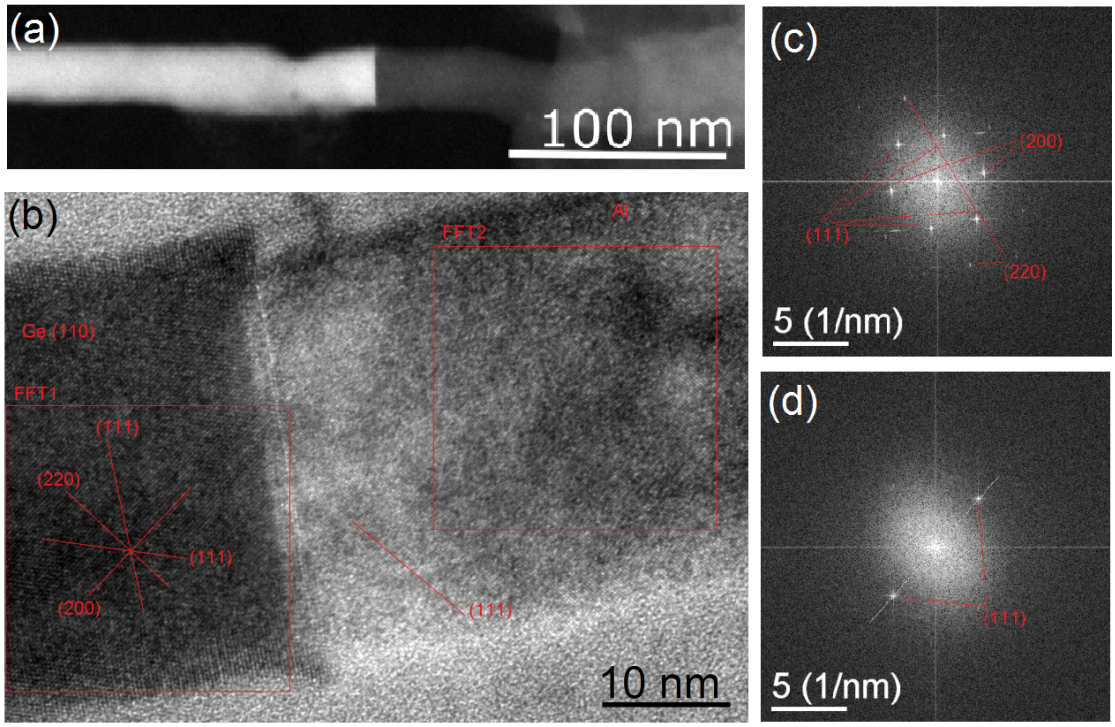

Figure 4.3: *Metal semiconductor interface within Al-Ge-Al NW heterostructures: (a) HAADF STEM image showing a strong chemical contrast between the unreacted Ge NW (dark) and the monocrystalline Al (bright), (b) HRTEM image exhibiting the atomic planes at the abrupt Al-Ge interface. (c,d) Indexed FFT patterns showing a diamond cubic structrure for the Ge segment and a fcc structure for the monocrystalline Al NW. Image adapted from [60]*

4.1.3 Al-Ge-Al NW Heterostructures Based on Passivated Ge NWs

In order to prevent surface traps and adsorbates on the surface of the used Ge NWs and thus reduce hysteresis effects in electrical transport investigations, the second device architecture of Al-Ge-Al NW heterostructures was based on Ge NWs passivated with 20 nm of Al_2O_3.
Therefore, the processes parameters for the heterostructure formation were adapted to fabricate Al-Ge-Al NW heterostructures with ultrasmall Ge segments.
A compilation of SEM images showing Al-Ge-Al NW heterostructures based on passivated Ge NWs with different Ge segments lengths between 10 nm and 94 nm is depicted in fig. 4.4.

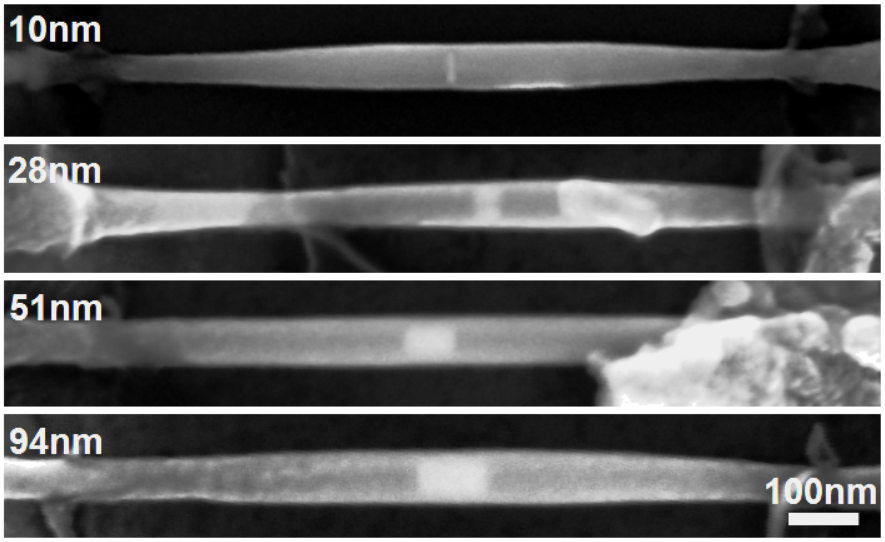

Figure 4.4: *Comparison of SEM images showing Al-Ge-Al NW heterostructures based on Ge NWs with a* 20 nm *thick* Al_2O_3 *all-around passivation. The depicted passivated heterostructure devices feature Ge segment lengths between* 10 nm *and* 94 nm. *The images were recorded at* 150.000 × *magnification.*

As previously reported in [28], the fabrication of heterostructure devices featuring ultra-small nanodots by using a RTA induced controlled reaction between a NW and the contact material weakens the common problem of short-channel back-gated devices, were the gate induced electric field is screened by the source and drain contacts. However, devices with Ge segments below 10 nm showed no more response to the applied back-gate voltages. Regarding this problematic, the process was tuned to fabricate devices with Ge segments in the range between 15 nm and 35 nm.
In order to retain a sufficiently thick passivation layer across the Ge NW, it was mandatory to rinse the sample long enough with water after the BHF etching of the passivation layer at the contact area. Otherwise the BHF was flowing in the gap between the resist and the etched aluminum oxide and an unwanted etching process of the passivation occurs.

4.2 Electrical Characterization of Al-Ge-Al NW Heterostructures

4.2.1 I/V Characteristic

In previous publications concerning Al-Ge-Al NW heterostructures, impact ionization [59] and NDR [27] were shown for devices with Ge segments longer than 500 nm.
Consequent fine tuning of the process parameters now allows the fabrication of Al-Ge-Al NW heterostructures featuring Ge segment lengths below a^*_{BGe}. Thus, it is now possible to study quantum confinement effects like ballistic transport in Al-Ge-Al NW heterostructures. Fig. 4.5 depicts the I/V-characteristics of Al-Ge-Al NW heterostructures with Ge segment lengths varying between 15 nm and 310 nm shown in fig. 4.1.

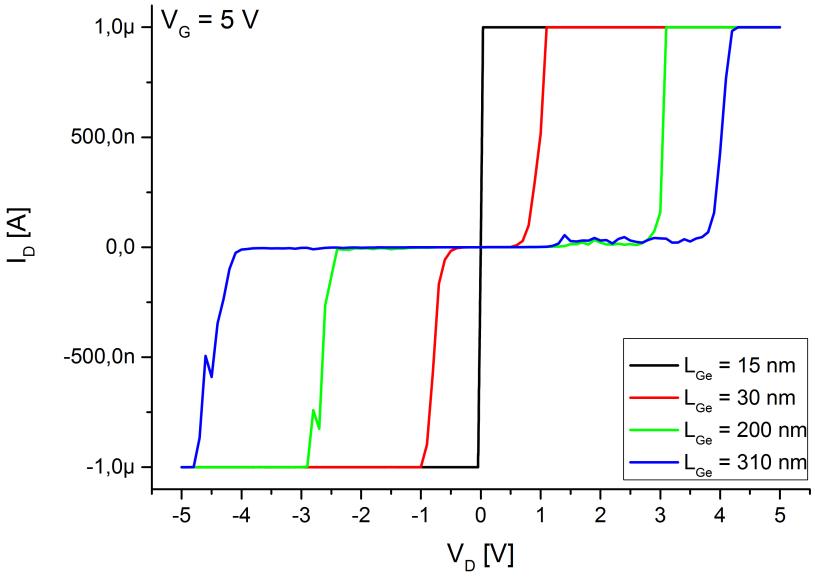

Figure 4.5: *I/Vs of Al-Ge-Al NW heterostructures: The I/Vs were recorded for a V_D sweep in the range from* -5 V *to* 5 V *for a V_G of* 5 V*. The current compliance of I_D was set to* 1 µA*. As can be seen, devices with Ge segments down to* 30 nm *show impact ionization behavior. Devices with Ge segment lengths below this value reveal an almost metal like I/V, which is indicating ballistic transport. The measurement data were recorded at ambient conditions.*

Since the Ge segment of the Al-Ge-Al NW heterostructures is connected by two Schottky barriers, the observed characteristic of devices with Ge segment lengths longer than 30 nm can be explained based on a Schottky diode biased in reverse direction. At low bias,

the space-charge region of the diode is increasing, which results in low current levels. As the bias is increasing, hot electrons release their energy gained from the electric field by creating an electron-hole pair (exciton). Further on, the exciton is split by the strength of the electric field. The continuation of this process initiates an avalanche like increase of current distinctive for impact ionization. Therefore, in order to prevent damage of the devices during the I/V measurements, the current compliance of I_D was set to 1 µA. For devices showing impact ionization, it can clearly be seen, that there is a coherence between the critical voltage, at which the current compliance of 1 µA is reached, and the Ge segment length. The critical voltage is increasing with the length of the Ge segment. Further on, to discuss the I/V characteristic of Al-Ge-Al NW heterostructures with ultrasmall Ge segments, fig. 4.6 depicts the I/Vs of a device with a Ge segment of 15 nm recorded for three different back-gate voltages. Representative for Al-Ge-Al NW heterostructures with Ge segments below 30 nm, the I/V characteristic shows that, however there is still control by the electrostatic field of the back-gate, a transition from impact ionization behavior towards a linear, almost metal-like I/V takes place. In the case of these devices, the Ge segment length is too small for the traversing electrons to gain enough energy to generate excitions by impact ionization. Instead, the electrons are passing through the Ge segment without scattering, which is a clear indication for ballistic transport.

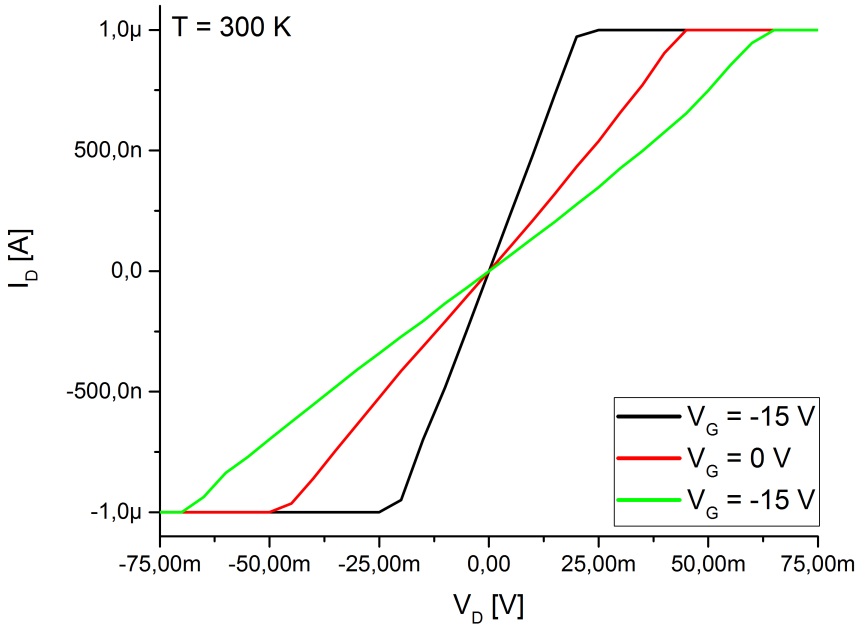

Figure 4.6: *I/Vs of an Al-Ge-Al NW heterostructure with a Ge segment length of* 15 nm *for different back-gate voltages: The I/Vs reveal a linear, almost metal like I/V indicating a shift towards ballistic transport. The measurement data were recorded at ambient conditions.*

4.2.2 Transfer Characteristic

In order to investigate the electrostatic modulation capability of Al-Ge-Al NW heterostructures, the transfer characteristics of the devices depicted in fig. 4.1 were measured. Although chemically intrinsic Ge NWs were used for the fabrication of Al-Ge-Al NW heterostructures, the measurement data depicted in fig. 4.7, reveals that all investigated devices exhibit a p-type field-effect. This behavior is dedicated to a combination of surface doping by adsorbates on the surface of the NWs and negative surface charges that accumulate on the NW surface in interband trap levels [91]. Further on, the measurement data reveals that one major problem of unpassivated Al-Ge-Al NW heterostructures is their weak response to the electrostatic field of the back-gate. Experimental investigations on numerous devices revealed that heterostructures with Ge segments larger than 200 nm exhibit almost no response to the back-gate voltage.
In contrast to Al-Ge-Al NW heterostructures with large Ge segments, devices with Ge segment lengths between 15 nm and 30 nm can be significantly better electrostatically modulated by the electrostatic field of the back-gate.

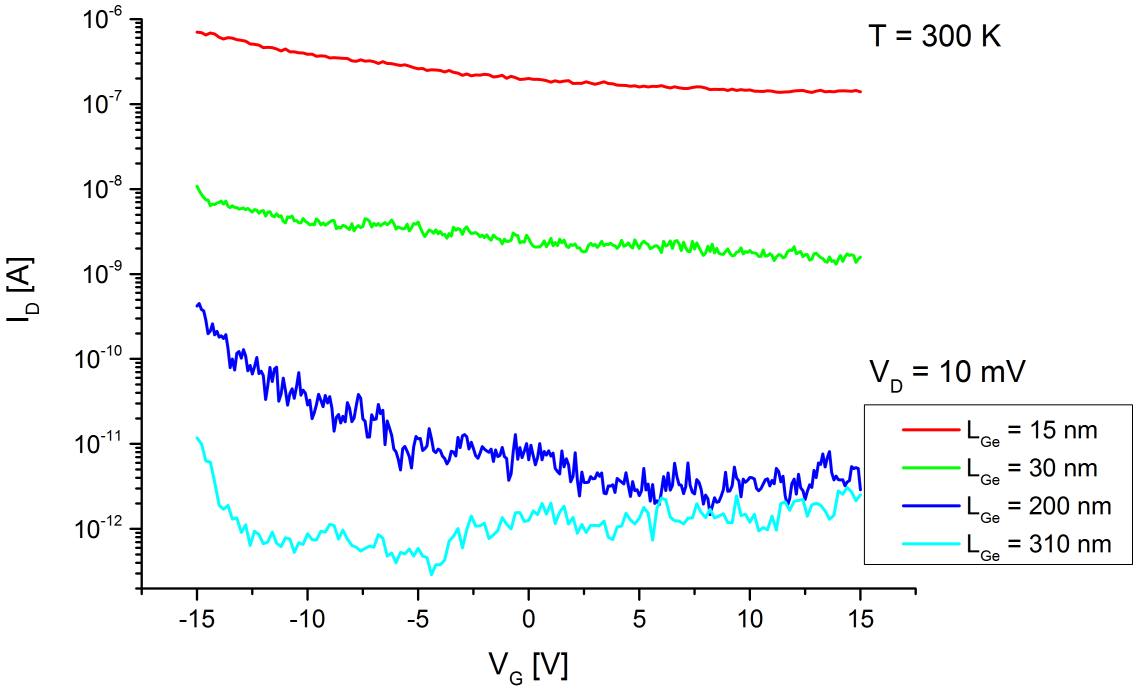

Figure 4.7: *Comparison of the transfer characteristic of Al-Ge-Al NW heterostructures with different Ge segment lengths for a bias of $V_D = 10\,\mathrm{mV}$: As can be seen, all investigated devices clearly show p-type behavior. Devices with Ge segment lengths between* 15 nm *and* 30 nm *exhibit a significantly better controllability compared to devices with larger Ge segment lengths. The measurement data were recorded at ambient conditions.*

4.2.3 I/V Characteristic at Cryogenic Temperatures

The temperature-dependent electrical behavior of back-gated Al-Ge-Al NW heterostructures with different Ge segment lengths was investigated by I/V measurements at temperatures between 80 K and 300 K.
The I/Vs were recorded starting with the lowest temperature. For discussion, a device with a Ge segment of 200 nm showing impact ionization as well as a device featuring an ultrasmall Ge segment of 15 nm exhibiting a metal-like I/V indicating ballistic transport were chosen. The investigated devices are depicted in fig. 4.1.
A comparison of the I/Vs of Al-Ge-Al NW heterostructures with different Ge segment lengths revealed that the development of the conductivity over temperature is depending on the Ge segment length.
It was demonstrated that for impact ionization devices with Ge segments between 300 nm and 650 nm, at a temperature of 270 K, the dominating effect determining the conductivity of the devices is shifting from lattice vibration induced scattering of charge carriers to a temperature related enlargement of the Ge band-gap (eq. 4.1) [60].

$$E_g = 0.742 - \frac{4.8 \times 10^{-4}\ T^2}{T + 235} \tag{4.1}$$

Therefore, in the regime were the temperature related enlargement of the band-gap is dominating, an increase of the conductivity with rising temperatures takes place. However, as the temperature exceeds 270 K, lattice vibration induced scattering of charge carriers is becoming the dominating effect. Hence, the conductivity is decreasing again. As can be seen in fig. 4.8(a), the exact same behavior was observed for an impact ionization device with an 200 nm Ge segment.
In contrast, Al-Ge-Al NW heterostructures with ultrasmall Ge segments due to ballistic transport show a completely different behavior. Exemplary for the temperature dependence of Al-Ge-Al NW heterostructures with ultrasmall Ge segments, fig. 4.8(b) depicts the I/V-characteristic of an Al-Ge-Al NW heterostructure with a 15 nm Ge segment for different temperatures between 80 K and 300 K. As can be seen, the conductivity is monotonically increasing with rising temperatures. This can be attributed to the fact that the l_m of these devices is much larger than the length of the Ge segment. Therefore, it can be assumed that phonon induced scattering of charge carriers is less pronounced compared to Al-Ge-Al NW heterostructures with larger Ge segments showing impact ionization. The absence of scattering is a clear indication of ballistic transport. Hence, the effect of temperature induced enlargement of the band-gap is dominating for ballistic devices.

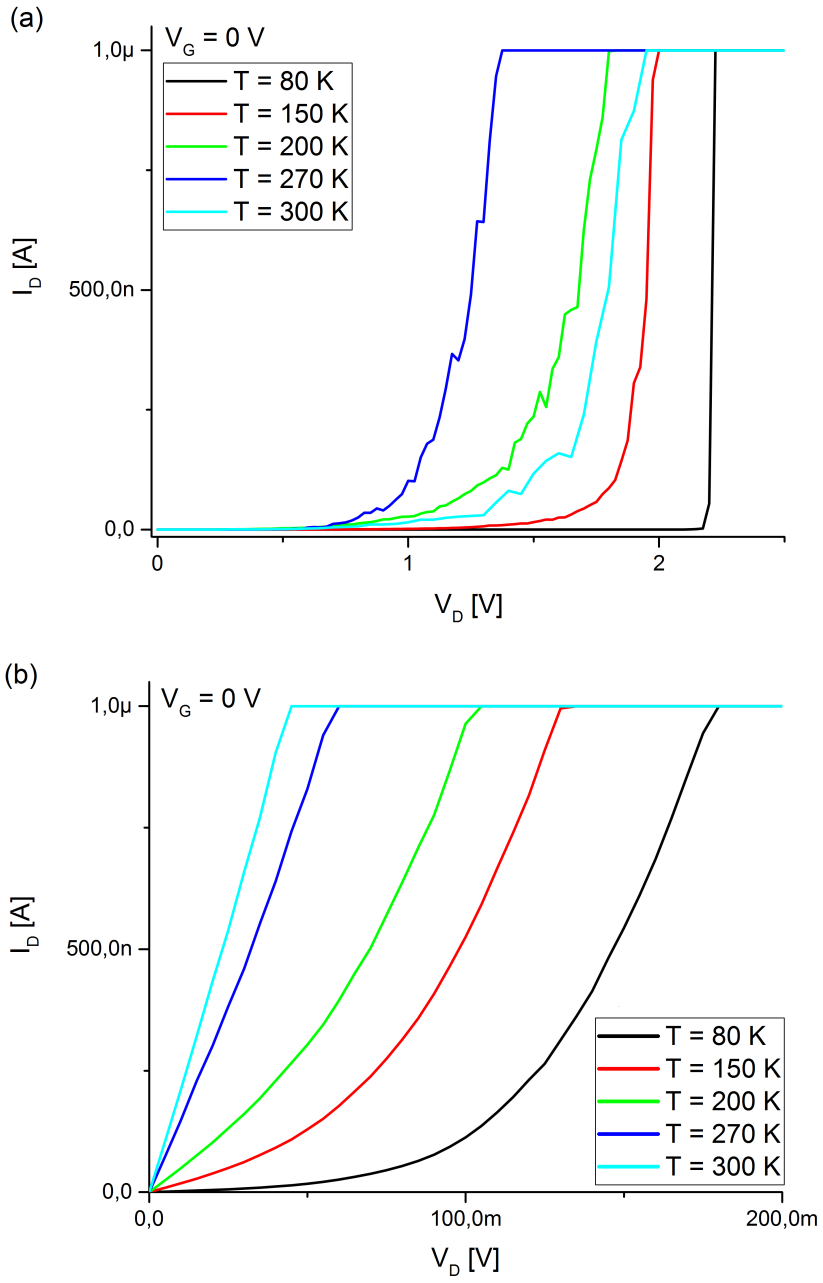

Figure 4.8: *I/Vs of Al-Ge-Al NW heterostructures with different Ge segment lengths as a function of temperature between* 80 K *and* 300 K *for* $V_G = 0$ V*: (a) I/Vs of an Al-Ge-Al NW heterostructure with a* 200 nm *long Ge segment. As can be seen, due to a combination of lattice vibration induced scattering of charge carriers and an enlargement of the band-gap at decreasing temperatures, the conductivity is reaching its maximum at* 270 K*. (b) Al-Ge-Al NW heterostructure with a* 15 nm *Ge segment, revealing a monotone increase of conductivity with rising temperatures.*

4.3 Electrical Characterization of Passivated Al-Ge-Al NW Heterostructures

4.3.1 I/V Characteristic

The electrical properties of Ge NWs appeared to be critically dependent on adsorbates and surface traps. Therefore using passivated Ge NW as basis for Al-Ge-Al NW heterostructures is motivated by the ability to replace the native oxide of the Ge NWs by a high quality high-k dielectric. The Ge NWs, which served as basis for the following I/V measurements were passivated with a 20 nm thick layer of ALD grown Al_2O_3. Fig. 4.9 provides a comparison of I/Vs of the passivated Al-Ge-Al NW heterostructures depicted in fig. 4.4.

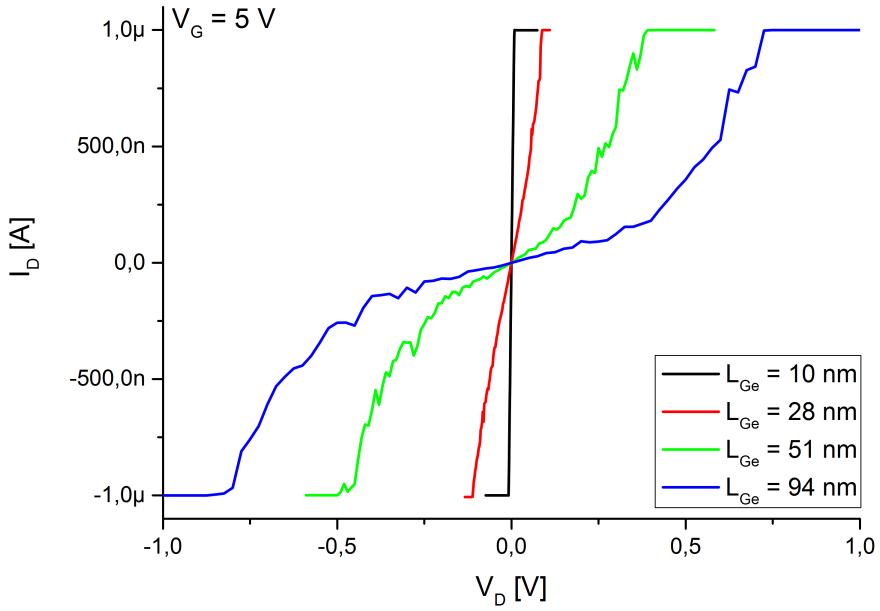

Figure 4.9: *I/Vs of passivated Al-Ge-Al NW heterostructures: The I/Vs were recorded for a V_D sweep in the range from* -1 V *to* 1 V *for a V_G of* 5 V. *A current compliance for I_D was set to* 1 µA. *The measurement data were recorded at ambient conditions.*

In analogy with unpassivated devices, the critical voltage, at which the current compliance is reached, is increasing with the Ge segment length of the devices. By comparing both device architectures, it can clearly be observed that for Al-Ge-Al NW heterostructures with similar Ge segment size, the critical voltage is significantly lower for devices based on

passivated Ge NWs. Further on, the I/Vs of devices based on passivated Ge NWs reveal no avalanche like increase of the current, which would indicate impact ionization behavior. This is dedicated to the interface between the Ge NW and the Al_2O_3 passivation. As a result, the current is increased. Therefore, passivated Al-Ge-Al NW heterostructures reach the current compliance before the electrical field is high enough to trigger impact ionization. Moreover, fig. 4.9 shows that similar to unpassivated Al-Ge-Al NW heterostructures with Ge segments below 35 nm, a shift towards ballistic transport is indicated by a transition to a linear almost metal like I/V.

4.3.2 Transfer Characteristic

To investigate the electrostatic modulation capability of passivated Al-Ge-Al NW heterostructures, the transfer characteristics of the passivated devices depicted in fig. 4.4 were measured. In addition to these devices, the transfer characteristic of a passivated Al-Ge-Al NW heterostructure with a 310 nm long Ge segment was also included.

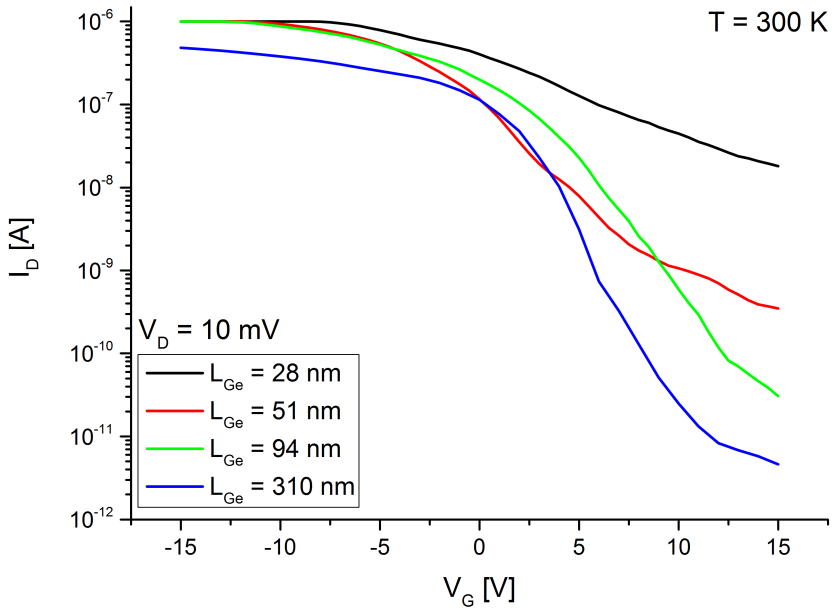

Figure 4.10: *Transfer characteristic of passivated Al-Ge-Al NW heterostructures with different Ge segment lengths: Similar to unpassivated Al-Ge-Al NW heterostructures, p-type behavior can clearly be observed. Passivated devices with Ge segment lengths between* 50 nm *and* 300 nm *biased with* $V_D = 10$ mV *show a remarkable room-temperature* I_{ON}/I_{OFF} *ratio of up to* 10^5*. The measurement data were recorded at ambient conditions.*

Although, the passivated device with the 10 nm Ge segment is also included in fig. 4.4, due to the current compliance of 1 µA, it was not possible to bias the device with $V_D = 10$ mV. In analogy to the transfer characteristic of unpassivated Al-Ge-Al NW heterostructure devices (fig. 4.7) a clear p-type behavior was observed. According to the measured data, back-gated passivated devices with Ge segment lengths ranging from 30 nm to 310 nm show a remarkable I_{ON}/I_{OFF} ratio of up to 5 orders of magnitude. Concerning that a relatively low current compliance of just 1 µA was set to prevent damage of the devices, it is likely that raising the compliance would further increase the I_{ON}/I_{OFF} ratio.
Compared with the unpassivated Al-Ge-Al NW heterostructures, depicted in fig. 4.7, this corresponds to an increase of the I_{ON}/I_{OFF} ratio of up to 3 orders of magnitude. In contrast to unpassivated Al-Ge-Al NW heterostructures, it can clearly be seen, that passivated devices even with Ge segment lengths larger than 300 nm exhibit a decent I_{ON}/I_{OFF} ratio as well. Further on, according to the large surface-to-volume ratio of NWs, it was suggested, that surface defects, which are trapping charge carriers and adsorbates like H_2O, which are causing p-type surface doping, have a huge impact on the electrical behavior of NW based devices [92, 93].

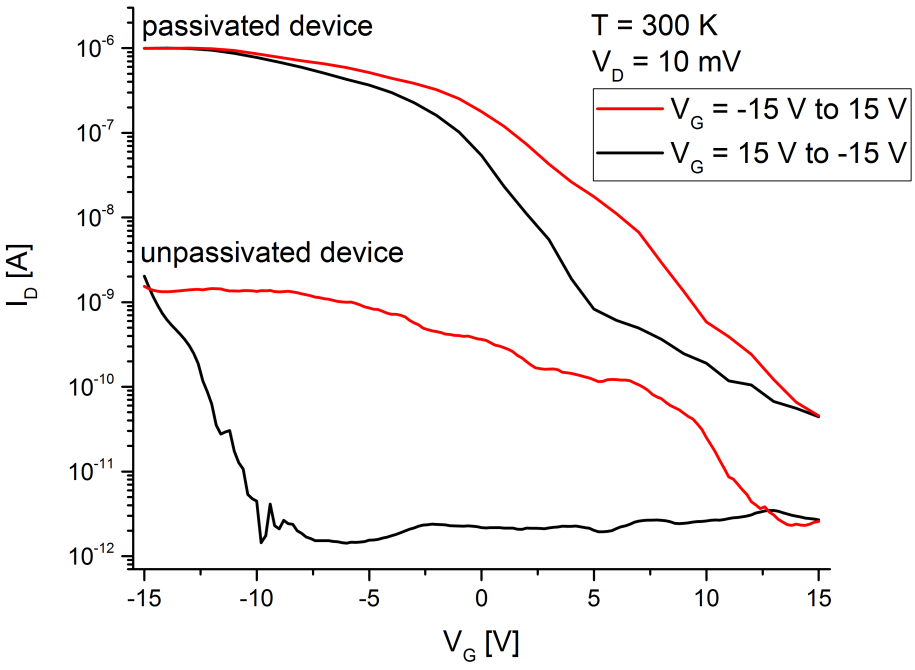

Figure 4.11: *Comparison of the transfer characteristic of passivated and unpassivated Al-Ge-Al NW heterostructures: Using passivated Ge NWs, due to a reduction of surface traps and adsorbates, diminishes hysteresis effects. Further on, the ON-current and the electrostatic modulation capability by the back-gate could be increased. The measurements were conducted at room temperature for a bias of $V_D = 10$ mV. For both devices a double sweep from V_G = -15 V to 15 V was performed.*

In order to investigate the reduction of hysteresis effects by using passivated Ge NWs for the fabrication of Al-Ge-Al NW heterostructures, a comparison of the transfer characteristics of an unpassivated and a passivated Al-Ge-Al NW heterostructure with Ge segment lengths of 150 nm is depicted in fig. 4.11.
For both devices, the transfer characteristic was first recorded from V_G = -15 V to 15 V, before a sweep in the reverse direction was started. The measurements were executed at a bias voltage of V_D = 10 mV.
Similar to numerous other publications [87, 88], it can clearly be observed that using passivated Ge NWs for the fabrication of Al-Ge-Al NW heterostructures is resulting in less hysteresis effects in the transfer characteristic.
Further on, the current levels of the ON-state (V_G = -15 V) of passivated Al-Ge-Al NW heterostructures are up to 3 orders of magnitude higher compared to unpassivated devices. The OFF-Current (V_G = 15 V) is about one order of magnitude higher. The increased electrostatic modulation capability of passivated Al-Ge-Al NW heterostructures is a consequence of replacing the unstable native oxide-shell of Ge NWs with a high quality high-k ALD deposited Al_2O_3 passivation layer.

4.3.3 I/V Characteristic at Cryogenic Temperatures

Regarding the problematic of Al-Ge-Al NW heterostructures featuring ultrashort Ge segments of having no electrostatic modulation capability by the back-gate, discussed in sec. 4.1, investigations on devices with different Ge segment lengths revealed a lower limit of 10 nm for back-gate architectures. Although, it was possible to fabricate Al-Ge-Al NW heterostructures with Ge segment lengths smaller than 10 nm, these devices showed no more response to the applied back-gate voltage.
In order to investigate the temperature dependence of passivated Al-Ge-Al NW heterostructures with Ge segment lengths below 30 nm, fig. 4.12 depicts both the experimental results of a passivated Al-Ge-Al NW heterostructure with a 28 nm long Ge segment as well as a device with a Ge segment length of 10 nm. The depicted I/V measurements were conducted for V_G = 0 V.
Whereas I_D clearly shows a weak temperature dependence, for the Al-Ge-Al NW heterostructure with a 28 nm long Ge segment, for the device featuring a Ge segment length of 10 nm, I_D reveals almost no temperature dependence. This behavior is assumed to be dedicated to an absence of lattice vibration induced scattering of charge carriers, which is an indication for ballistic transport.
Comparing this temperature dependence with unpassivated Al-Ge-Al NW heterostructures revealed some differences. Whereas for unpassivated devices the temperature dependence of the conductivity is depending on the Ge segment length (sec. 4.2.3), a different behavior was observed for passivated Al-Ge-Al NW heterostructures. In contrast to unpassivated devices, all Al-Ge-Al NW heterostructures based on passivated Ge NWs reveal a monotonous increase of the conductivity with rising temperatures.

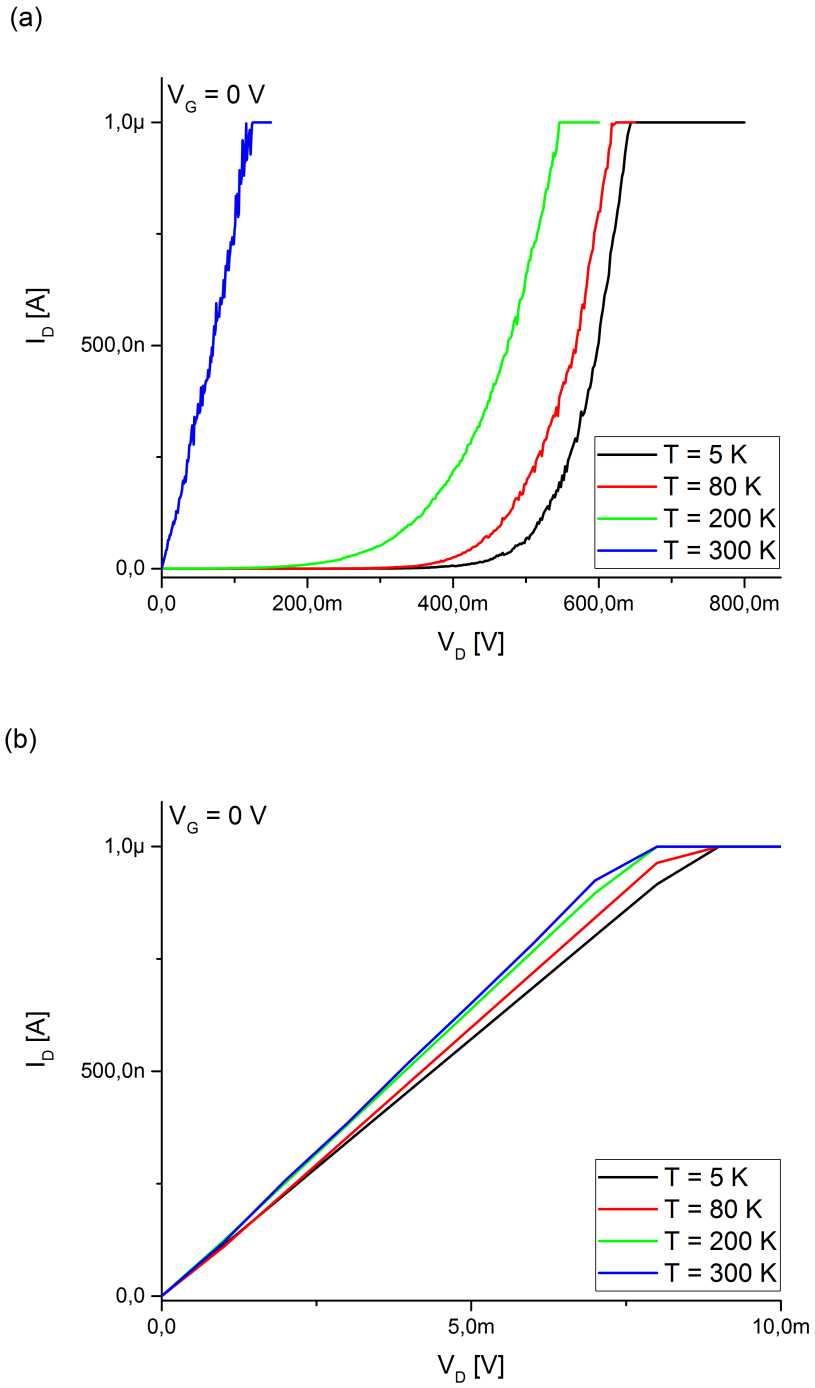

Figure 4.12: *I/Vs of passivated Al-Ge-Al NW heterostructures as a function of temperature: (a) Passivated Al-Ge-Al NW heterostructure with a Ge segment length of* 28 nm *showing a weak temperature dependence. (b) Passivated device with a Ge segment length of* 10 nm *revealing almost no temperature dependence.*

Further on, based on the experimental data from I/V measurements at $V_G = 0\,V$, the temperature dependence of the resistivity of passivated Al-Ge-Al NW heterostructures with ultrasmall Ge segment lengths was investigated in the range between 5 K and 300 K. Since only 2T measurements were conducted, the resistivity contains a series resistance originating from the Al contacts as well as the monocrystalline Al leads. As previously shown, the monocrystalline Al NWs, which are contacting the Ge segment, reveal a 18 times higher resistivity compared to bulk Al $\rho_{Al} = 2.65\,\mu\Omega\,cm$ [94, 95]. This can be attributed to impurity scattering caused by Ge atoms, which to some extend may be incorporated into the crystal structure of the Al NWs during the rapid diffusion of Ge in Al [59]. Although conducting 4T measurements would eliminate the contact resistance of the devices, the resistance of the Schottky barriers, which connect the Ge segment with the Al leads, can not be excluded. Beside the increased process complexity, this was one of the most crucial factors for maintaining 2T measurements.
According to the fact, that the recorded I/Vs show a nonlinear characteristic, the device resistance R_D was calculated based on a linear fit of the measured drain current in the voltage range between $-10\,mV$ and $10\,mV$. In order to calculate the resistivity, the geometry of the Ge segment as well as the calculated R_D was inserted in eq. 4.2.

$$\rho = \frac{R_D A_{Ge}}{L_{Ge}} = \frac{R_D \frac{d_{Ge}^2 \pi}{4}}{L_{Ge}} \tag{4.2}$$

where, the geometry of the Ge segment is considered by the length (L_{Ge}), the diameter (d_{Ge}) and the area (A_{Ge}).

The resulting plot showing the temperature dependence of the passivated Al-Ge-Al NW heterostructures is depicted in fig. 4.13.
As can be seen, for passivated devices with Ge segments between 15 nm and 28 nm the resistivity is dropping with rising temperatures. Further on, the temperature dependence of the resistivity is getting smaller with decreasing Ge segment lengths. Since it is predicted that the resistivity of intrinsic semiconductors is decreasing with increasing temperatures, the observed behavior is in good accordance with theory [32]. However, comparing the measured resistivities with bulk values, one has to keep in mind that the resistivity of semiconductors is heavily depending on the amount of present impurities and crystal defects. Thus, the bulk resistivity of Ge at 300 K is ranging from $\rho_{Ge} = 0.05$ - $50\,\Omega\,cm$ [33]. Since the measured Al-Ge-Al NW heterostructures with Ge segment lengths $\geq$ 15 nm reveal a room-temperature resistivity of 0.45 - $4.5\,\Omega\,cm$, a comparison with the aforementioned bulk resistivity reveals a moderate doping of the Ge segments. This is in good accordance with measurements of the transfer characteristic, which due to surface doping by adsorbates, clearly shows a p-type behavior of the devices.
In contrast to Al-Ge-Al NW heterostructures with Ge segments $\geq$ 15 nm, devices with Ge segments of only 10 nm reveal an almost constant resistivity over the investigated temperature range. According to the fact that the resistivity is heavily depending on the

purity of the material [94] and comprising that a 10 nm Ge segment is corresponding to structure that is only consisting of 18 atomic layers, the resistivity caused by scattering of electrons with impurities and crystal defects should be negligible. Hence, the resistivity is almost constant over the investigated temperature range, which is indicating a shift towards ballistic transport. Further on, a comparison with bulk values reveals that the room-temperature resistivity of Al-Ge-Al NW heterostructures with Ge segments of only 10 nm is comparable with highly doped bulk Ge. Moreover, as fig. 4.13 shows, the room-temperature resistivity of a monocrystalline Al NW is about a factor 1000 lower than the resistivity of the Al-Ge-Al NW heterostructure with a Ge segment length of 10 nm.

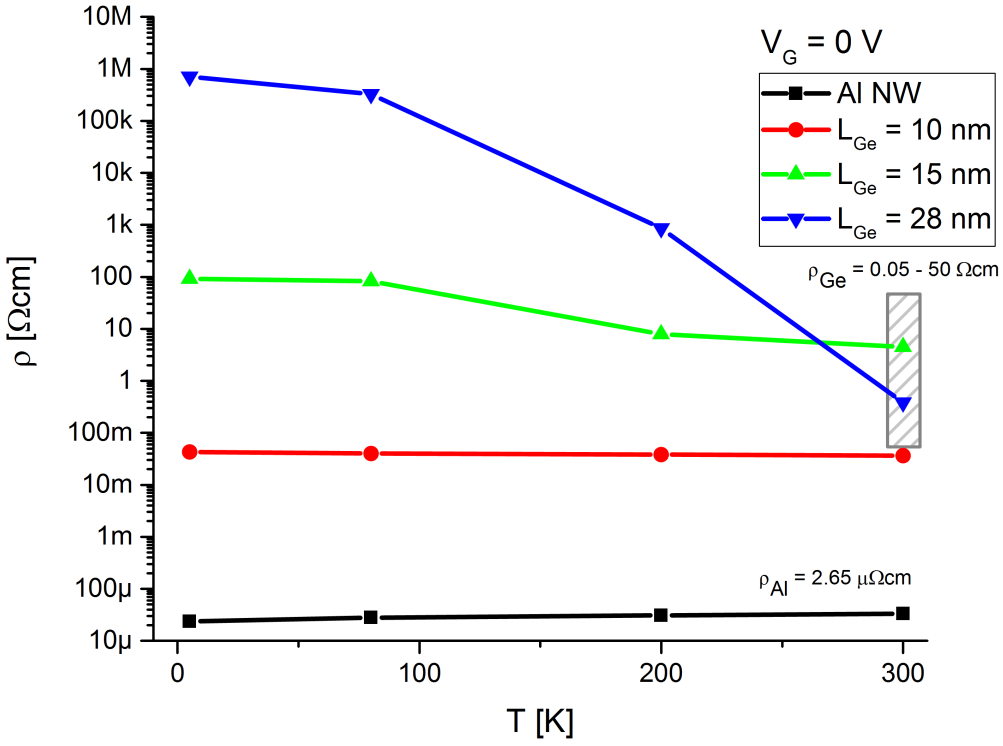

Figure 4.13: *Temperature dependence of the resistivity of passivated Al-Ge-Al NW heterostructures with different Ge segment lengths compared with a monocrystalline Al NW. The resistivity is based on 2T I/V measurements for* $V_G = 0\,\mathrm{V}$. *The gray shaded area is indicating the room-temperature resistivity of bulk Ge. All investigated devices including the monocrystalline Al NW were based on passivated Ge NWs with diameters between* 30 nm *and* 35 nm.

4.3.4 Time Dependent Behavior

In order to study the influence of surface traps [91] on the transport measurements of passivated Al-Ge-Al NW heterostructures, the time dependent behavior of the drain current was recorded for different back-gate voltages.
Based on numerous transport measurements, it seamed that the influence of surface traps is prohibiting the detection of ballistic transport phenomena. Hence, to allow reproducible measurements of the intrinsic transport properties of passivated Al-Ge-Al NW heterostructures, it was necessary to deplete all surface traps present in the system.
Representative for Al-Ge-Al NW heterostructures with ultrasmall Ge segments, the transient behavior of a passivated Al-Ge-Al NW heterostructures with a Ge segment length of 35 nm at room temperature is depicted in fig. 4.14.

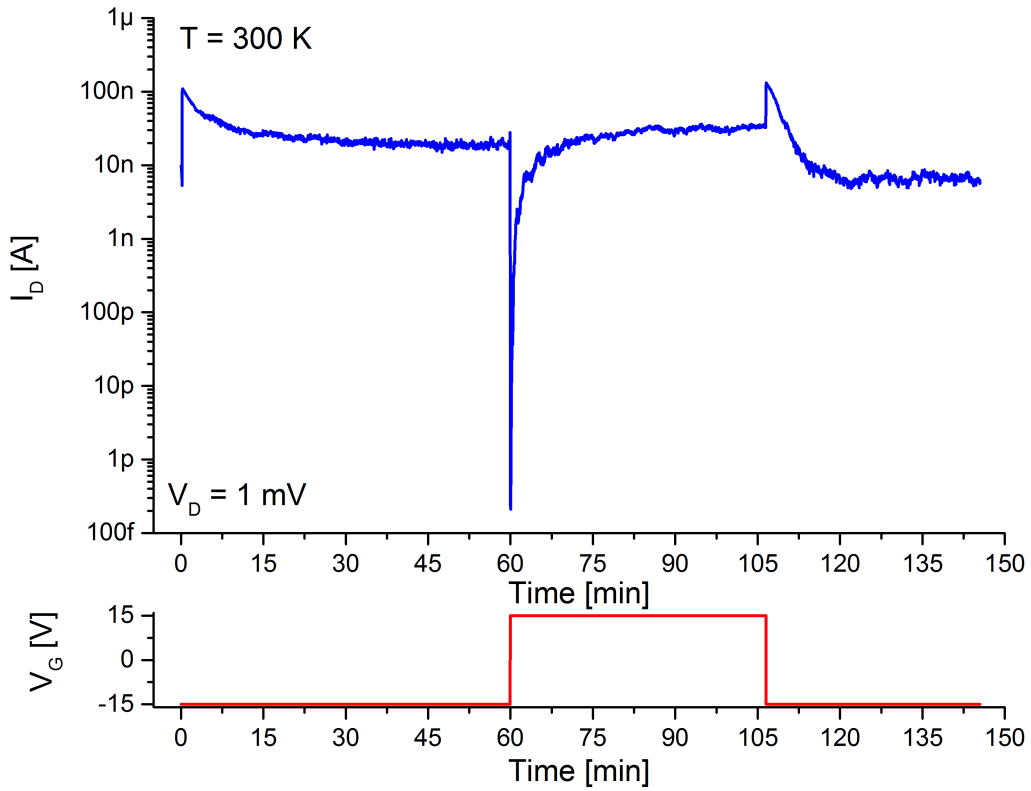

Figure 4.14: *Transient behaviour of a passivated Al-Ge-Al NW heterostructure with a Ge segment length of* 35 nm *at room temperature for* $V_D = 1\,\mathrm{mV}$*:*
In the first 60 min $V_G = -15\,\mathrm{V}$*, due to a depletion of traps, results in an exponential decay of the drain current. After that,* $V_G = 15\,\mathrm{V}$ *was applied. As a consequence, the drain current is increasing, which is indicating that the traps are being filled.*

As can be seen, applying a negative back-gate voltage, due to a depletion of traps, results in an exponential decay of the drain current. In contrast to that, applying a positive gate-voltage increases the drain current. This behavior is indicating a filling of the traps. This transient behavior was investigated for passivated Al-Ge-Al NW heterostructures with different Ge segments lengths between 15 nm and 300 nm. Whereas the density of the traps as well as contact area of all devices can be considered to be equal, the exponential decay of the drain current due to trap depletion appeared to be slower for devices with smaller Ge segment lengths. However, the trap filling process was not depending on the length of the Ge segments or the applied bias voltage.
According to this trap filling and depletion mechanism, all ballistic transport measurements were conducted after depleting the traps for about 80 min. As can be seen in fig. 4.15, the trap depletion procedure was accomplished by applying a V_G of -15 V for about 80 min before cooling down the sample to 5 K. After this depletion process was complete, the sample was cooled below the freezing point of traps at 77 K [96], before the aforementioned measurement routine was stopped and the ballistic transport measurements were started.

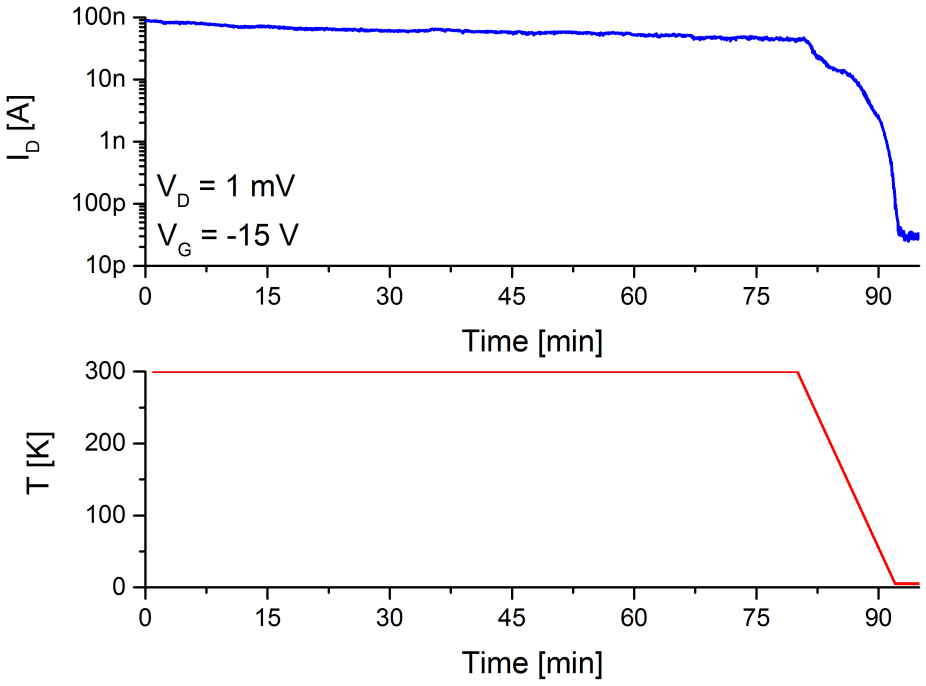

Figure 4.15: *Transient measurement of I_D for a bias voltage of V_D = 1 mV at V_G = -15 V of a passivated Al-Ge-Al NW heterostructure with a Ge segment length of* 35 nm *during cooling to* 5 K. *After the trap depletion, the cooling procedure was started.*

4.4 Simulation of the Quantum Confinement in Ge NWs

In order to discuss the quantum confinement effects in passivated Al-Ge-Al NW heterostructures, simulations of the eigenenergies concerning different NW diameters were implemented.
Due to the huge increase of complexity, the conducted simulations only concern an infinitely extended Ge NW passivated with 20 nm of Al_2O_3. Hence, the simulation is only capable of taking into account the quantum confinement by the diameter of the Ge NW. In order to concern the confinement by the Ge segment lenghts as well, a 3D simulation would be required.
Since the characteristic lengths of the device geometry are in the order of the electron wavelength, a quantum mechanical transport model based on the 2D Schrödinger equation, shown in eq. 4.3, was implemented.

$$i\hbar\frac{\partial}{\partial t}\Psi(\vec{r},t) = \hat{H}\Psi(\vec{r},t) \tag{4.3}$$

Furthermore, the general Hamilton operator $\hat{H}$ was simplified for a 2D geometry concerning a time constant potential:

$$\hat{H} = -\frac{\hbar^2}{2m^*}\left(\frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2}\right) + U(x,y) \tag{4.4}$$

Since realistic systems require to solve the Schrödinger equation numerically, the matrix representation of the Hamilton operator was obtained for discretization by using a finite difference method, which allows to convert a differential equation into a difference equation. In the same step, the grid spacings of the discrete lattice denoted by d_x and d_y were implemented to convert the wavefunction into a column vector:

$$\frac{\partial^2\Psi(x,y)}{\partial x^2} \quad \Rightarrow \quad \frac{1}{d_x^2}\left(\Psi_{x+1,y} - 2\Psi_{x,y} + \Psi_{x-1,y}\right) \tag{4.5}$$

$$\frac{\partial^2\Psi(x,y)}{\partial y^2} \quad \Rightarrow \quad \frac{1}{d_y^2}\left(\Psi_{x,y+1} - 2\Psi_{x,y} + \Psi_{x,y-1}\right) \tag{4.6}$$

$$U(x,y)\Psi(x,y) \quad \Rightarrow \quad U_{x,y}\Psi_{x,y} \tag{4.7}$$

Inserting the relations from eq. 4.7 into the Schrödinger equation (eq. 4.3), results in the following expression:

$$i\hbar\frac{\partial\Psi_{x,y}}{\partial t} = (U_{x,y} + 2t_x + 2t_y)\Psi_{x,y} - t_x\Psi_{x+1,y} - t_x\Psi_{x-1,y} - t_y\Psi_{x,y+1} - t_y\Psi_{x,y-1} \tag{4.8}$$

with the following substitutions (hopping parameters):

$$t_x = \frac{\hbar^2}{2m^* d_x^2}, \qquad t_y = \frac{\hbar^2}{2m^* d_y^2} \tag{4.9}$$

Concerning that rapid oscillations in the wavefunction are only occurring at high energies, the deviation of the applied numerical simulation approach is negligible compared to an analytical calculation of the eigenvalues. In order to solve the problem of having a 3-dimensional Hamiltonian matrix, the wavefunction vector was sorted as seen in eq. 4.10.

$$\vec{\Psi} = [\Psi_{1,1}, \Psi_{1,2}, \ldots, \Psi_{1,N_y}, \Psi_{2,1}, \ldots, \Psi_{2,N_y}, \ldots, \Psi_{N_x,1}, \ldots, \Psi_{N_x,N_y}]^\top \tag{4.10}$$

In this equation N_x and N_y denote the number of points in the x- and y-direction resulting in a $N_xN_y \times N_xN_y$ Hamiltonian matrix. This form of the Hamiltonian matrix was then implemented in a MATLAB program calculating the eigenvalues of the investigated devices by solving the following equation:

$$H\Psi = E\Psi \tag{4.11}$$

Since the fabricated devices, due to surface doping by adsorbates on the surface of the Ge NWs, clearly show p-type behavior, the simulation was conducted using the effective mass of holes of Ge $m^*_{Ge} = 0.041m_0$ [31]. Furthermore, as a tradeoff between computing time and accuracy, the simulation grid size was defined by $N_x = N_y = 61$. The gird spacing was set to $d_x = d_y = 0.1\,\text{nm}$.

Fig. 4.16 depicts the probability density profiles for a Ge NW with a diameter of 30 nm passivated with 20 nm of Al_2O_3. Based on the calculation of the eigenenergies, a degeneracy is occurring, where $E_2 = E_3$. The simulated eigenenergies and their degeneracies (energy levels with equal wavefunctions but different directions) were used for the interpretation of the experimental results.

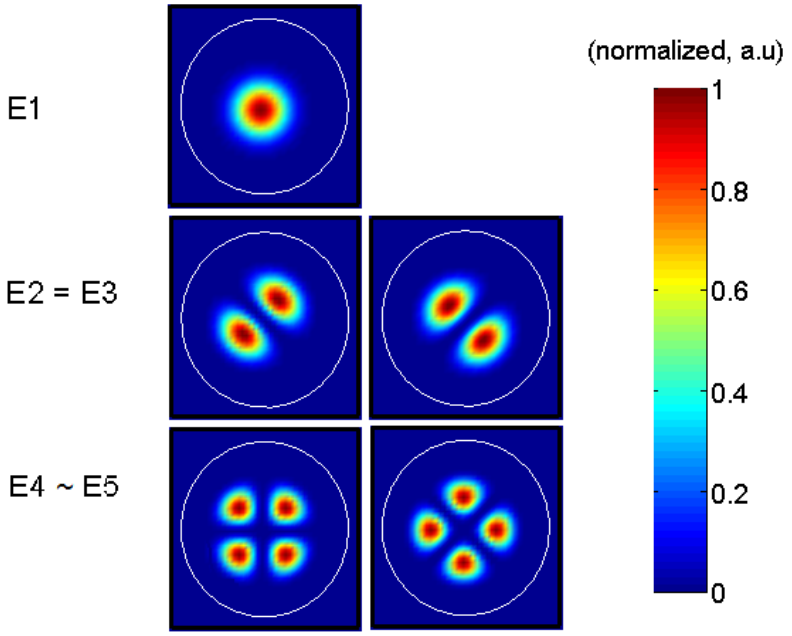

Figure 4.16: *Simulated probability density profiles of a Ge NW with a diameter of* 30 nm *showing the first five eigenenergies and their degeneracies: The calculations revealed a degeneracy, where* $E_2 = E_3$. E_4 *and* E_5 *are not degenerated, but very close in value.*

Moreover as fig. 4.17(a) depicts, the eigenenergies E_4, E_5 and E_6 are very close together, which should manifest itself either in weak individual plateaus at $4G_0$, $5G_0$ and $6G_0$ or a pronounced $3G_0$ conduction step from $3G_0$ to $6G_0$.
Since, eigenenergies with small energetic spacing are often populated at similar gate-voltages [97], the case where a pronounced plateau at $6G_0$ is occurring is much more likely compared to the occurrence of three individual plateaus at $4G_0$, $5G_0$ and $6G_0$. Hence, this case is schematically illustrated in (b).

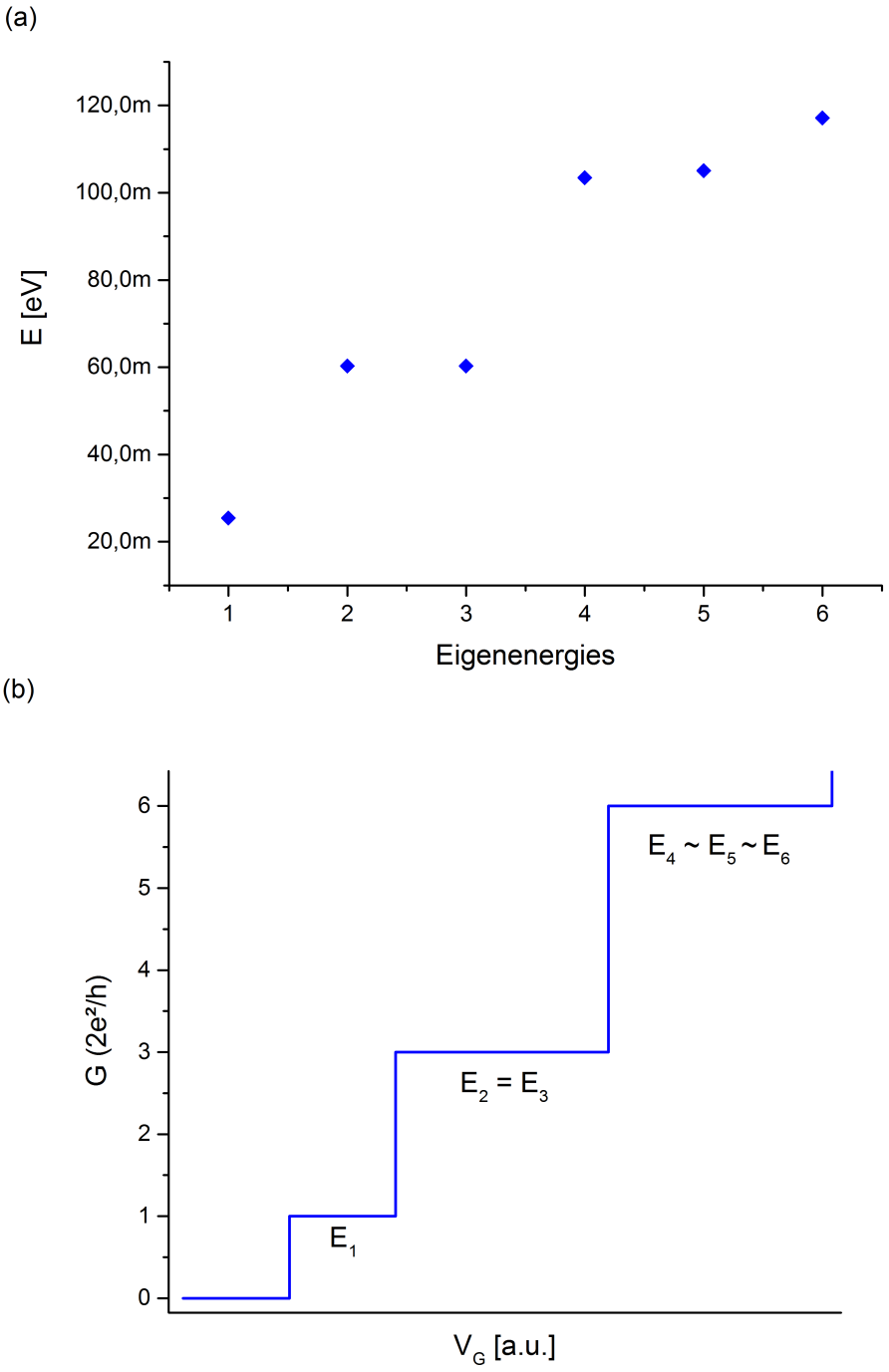

Figure 4.17: *Simulation of the eigenenergies of a Ge NW with a diameter of* 30 nm*:*
(a) The eigenenergies E_2 and E_3 are degenerated. Further on, E_4, E_5 and E_6 are very close in value. This should manifest itself ether in weak individual plateaus or a 3 G_0 conductance step from 3 G_0 to 6 G_0. (b) Schematic illustration of the predicted conductance plateaus at G_0, 3 G_0 and at 6 G_0.

Further on, fig. 4.18 depicts the results of a simulation concerning the impact of the NW diameter on the eigenenergies and their degeneracies.
The data from the simulation clearly reveals that with increasing NW diameter, the eigenenergies are much closer together, which deteriorates the ability to detect individual conductance plateaus [70]. In addition, the plot also exhibits the evolution of degenerate eigenenergies. Whereas the eigenenergies E_2 and E_3 are degenerated for all investigated diameters, the spacing between E_4, E_5 and E_6 is increasing with decreasing NW diameter. A Comparison of the data retrieved from the conducted simulation showed good accordance with the findings of other groups [70].

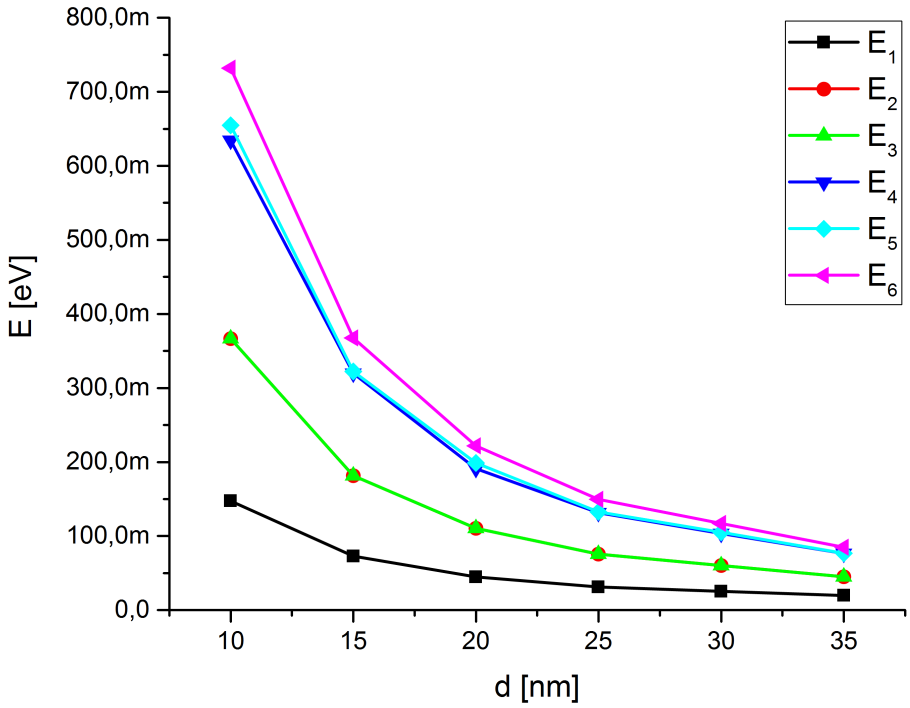

Figure 4.18: *Simulated dependence of the eigenenergies and their degeneracies on the Ge NW diameter: The spacing of the eigenenergies is increasing for decreasing NW diameters. Hence, devices based on Ge NWs with smaller diameters exhibit a better quantum confinement. The degeneracy of E_2 and E_3 is persisting for all simulated NW diameters.*

Although the diameters of the used Ge NWs are quite large and therefore not facilitating a superb quantum confinement, according to the estimation in eq. 4.12 [98], the sub-band energy spacing ($\Delta E_{sub-band}$) is large enough to allow room-temperature observation of conductance quantization:

$$\Delta E_{sub-band} \approx \frac{h^2}{m^*_{Ge} d^2_{NW}} = 75.97\,\text{meV} > k_B T \approx 25\,\text{meV}\ (300\,\text{K}) \tag{4.12}$$

where h is Planck's constant and d_{NW} denotes the diameter of the Ge NW.

An schematic illustration of band-splitting for Ge segment lengths below a^*_B is depicted in fig. 4.19. The estimated energetic spacing between the sub-bands $\Delta E_{sub-band}$ is indicated.

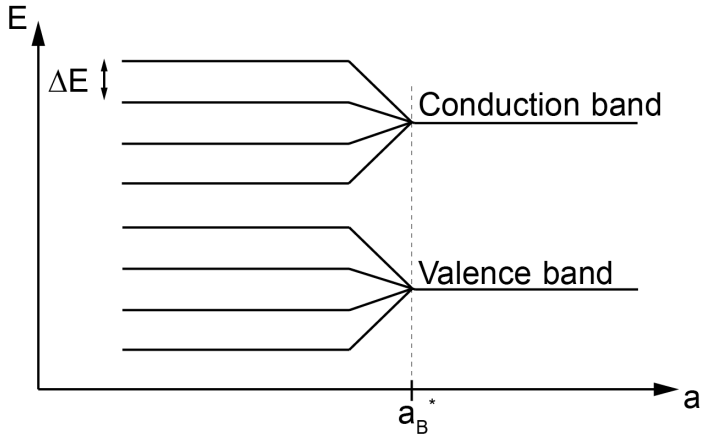

Figure 4.19: *Schematic illustration of band-splitting below a^*_B:*
The conduction band as well as the valence band are split into sub-bands. The estimated spacing between the sub-bands $\Delta E_{sub-band}$ is indicated.

4.5 Ballistic Transport in Passivated Al-Ge-Al NW Heterostructures

The following section discusses the observation of conductance quantization in passivated Al-Ge-Al NW heterostructures with ultrasmall Ge segments. Although, conductance quantization was observed in more than 10 Al-Ge-Al NW heterostructures with Ge segment lengths between 15 nm and 35 nm, two devices were chosen for detailed discussion. Using passivated Al-Ge-Al NW heterostructures for conductance measurements is motivated by their significantly better electrostatic modulation capability compared to Al-Ge-Al NW heterostructures based on unpassivated Ge NWs. Further on, trap induced surface disorder, which is blurring out the sub-band profile [70], is reduced by using a passivation layer. Additionally, the bias voltage for the recording of the conductance could be lowered from 10 mV to 1 mV. This increased the possibility for the observation of ballistic transport, because the influence of temperature and energy relaxation of injected hot electrons could be significantly reduced [71].
To show that conductance quantization can even be observed for devices featuring Ge segment lengths up to 30 nm a passivated Al-Ge-Al NW heterostructure featuring a 28 nm long Ge segment was chosen for discussion. Further on, to investigate the occurrence of conductance quantization in devices with Ge segment lengths significantly smaller than their diameter, a passivated Al-Ge-Al NW heterostructure with a 15 nm long Ge segment was selected. SEM images of the passivated Al-Ge-Al NW heterostructures chosen discussion are depicted in fig. 4.20.
In order to get evidence of conductance quantization, the simulated quantum confinement effects depending on the NW diameter from sec. 4.4 and the experimental data are compared. According to the fact that many other groups favor back-gated devices because of more pronounced conduction plateaus, it was not necessary to fabricate a more complicated top-gate architecture [28, 64, 70].

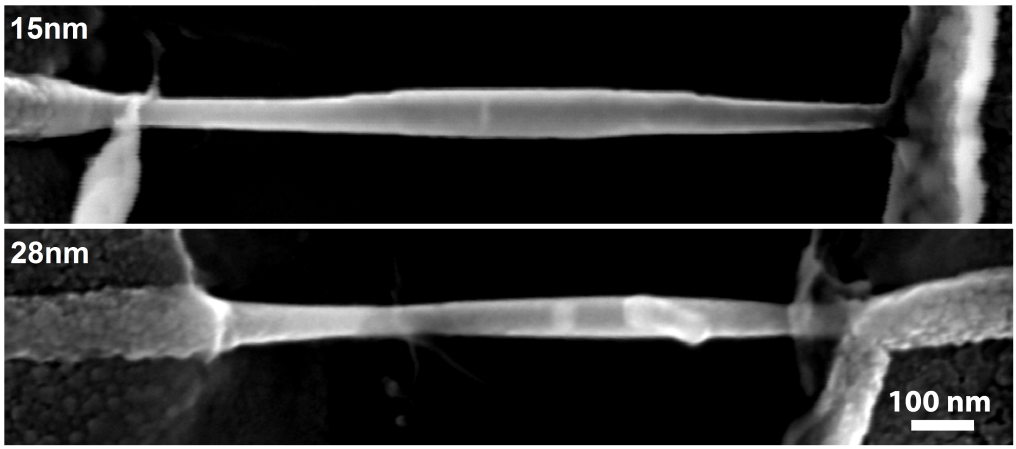

Figure 4.20: *SEM images of passivated Al-Ge-Al NW heterostructures with Ge segment lengths of* 15 nm *and* 28 nm *chosen for discussion of conductance quantization.*

4.5.1 Conductance Measurements at T = 5 K

Conductance quantization at T = 5 K was detected for a passivated Al-Ge-Al NW heterostructure featuring a 28 nm long Ge segment (fig. 4.21).
As can be seen, the first sub-band as well as the double step at $3G_0$ are matching the simulations. However the plateaus at $4G_0$ and $5G_0$ are missing, the single step at $6G_0$ is clearly visible. One possible explanation for the absence of the conduction steps of the fourth and fifth plateau is likely dedicated to the fact that the eigenenergies E_4, E_5 as well as E_6 are very close in value. Hence, the occurrence of the pronounced $6G_0$ plateau seams to be a clear confirmation for a $3G_0$ step. Concerning ballistic transport, the absence of plateaus is a commonly observed phenomenon, which is often dedicated to the fact that degenerate sub-bands as well as sub-bands close in energy, are likely populated at similar gate-voltages [97].

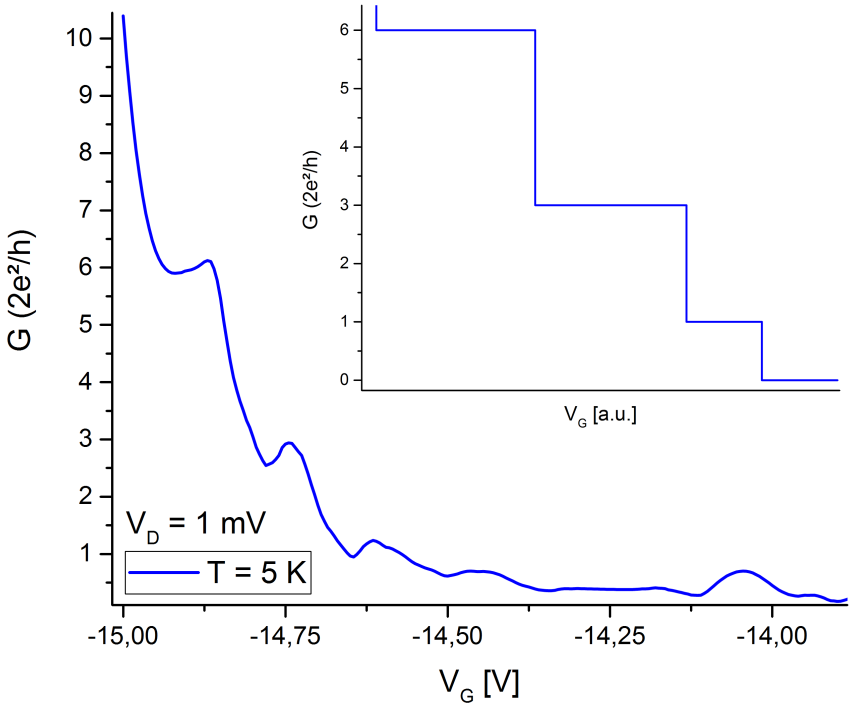

Figure 4.21: *Conducatance of a passivated Al-Ge-Al NW heterostructure featuring a Ge segment length of* 28 nm *at a temperature of* 5 K *and a bias of* V_D = 1 mV*:*
The experimental data clearly shows the simulated conductance steps at 1 G_0*, 3* G_0 *and 6* G_0*. In addition, a feature at 0.5* G_0 *is also shown. The data was recorded by sweeping* V_G *in* 5 mV *steps. The insert is showing a qualitative representation of the simulated eigenenergies.*

In addition to the aforementioned conductance plateaus, the device clearly shows a feature at $0.5G_0$. Further on, the experimental data clearly reveals that the conductance plateaus are not sharp but rounded. This is not only a temperature depending effect, but can also be dedicated to the confining potential [71].

4.5.2 Conductance Measurements at Different Bias Voltages

In order to investigate the impact of higher bias voltages V_D on conductance quantization, additional measurements with 10 mV bias were conducted at T = 5 K. The results concerning the aforementioned passivated Al-Ge-Al NW heterostructure with a 28 nm long Ge segment are depicted in fig. 4.22.
As can clearly be seen, the conductance plateaus occurring at $3G_0$ and $6G_0$ as well as the half-integer plateau at $0.5G_0$ are persisting for higher bias. However, the plateau at G_0 is slightly shifted. One possible explanation for this effect might be increased energy relaxation of hot electrons at higher bias voltages [71].

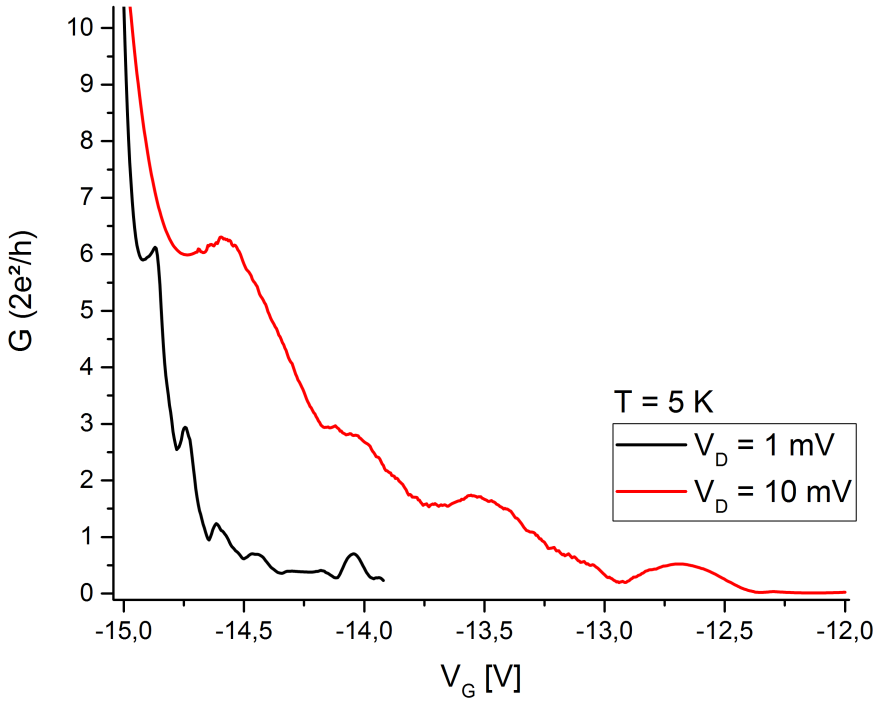

Figure 4.22: *Comparison of conductance quantization for different bias voltages at $T = 5$ K. The data was recorded by sweeping V_G in 5 mV steps.*

4.5.3 Conductance Measurements for Temperatures up to T = 300 K

Based on the conducted simulation as well as the experimental data at T = 5 K, the evolution of conductance quantization for temperatures up to 300 K will be discussed based on Al-Ge-Al NW heterostructures with a 15 nm and a 28 nm segment length.
As mentioned before, the observation of ballistic transport is limited to the temperature regime where the thermal broadening k_BT exceeds the sub-band spacing (eq. 4.12). Moreover, as the temperature increases the conductance plateaus are being blurred out, which manifests itself by rounding effects of the plateaus. If finally the temperature is getting sufficiently high, the plateaus disappear [71]. Representative for passivated Al-Ge-Al NW heterostructures with Ge segment lengths comparable to their diameter, the evolution of conduction plateaus from T = 5 K to 300 K is discussed based on a device featuring a Ge segment length of 28 nm.

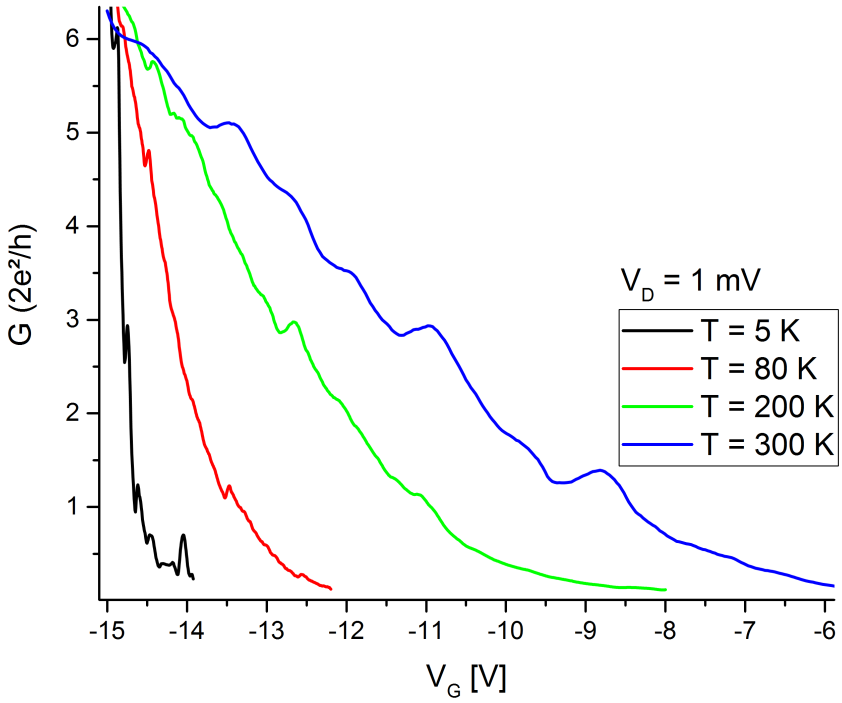

Figure 4.23: *Conductance quantization of a passivated Al-Ge-Al NW heterostructure with a Ge segment length of* 28 nm *for* V_D = 1 mV *as a function of temperature.*

As can be seen in fig. 4.23, the $0.5G_0$ feature occurring at T = 5 K is missing for all other temperatures. Moreover, comparing the conductance plateaus of the T = 5 K and the T = 300 K plot, the effect of thermal broadening can clearly be observed. Whereas at

T = 5 K the degenerate plateaus at $4G_0$, $5G_0$ and $6G_0$, due to their small energy spacing are falling together at $6G_0$, the experimental data at T = 300 K clearly reveals three independent plateaus. One explanation for this effect could be dedicated to the fact that at T = 5 K, the conductance steps are only distributed over a gate-voltage range of 1.5 V. In contrast to that, at T = 300 K, the conductance steps are extending over about 10 V. Hence, at T = 5 K there is a high probability that the plateaus at $4G_0$, $5G_0$ and $6G_0$ are populated at similar gate-voltages [97]. Therefore, instead of three independent plateaus, there is only one large step occurring at $6G_0$. According to the simulation, which predicts that the energetic spacing between E_4 and E_5 is smaller compared to the spacing of E_5 and E_6, the plateau at $5G_0$ is more pronounced compared to the plateau at $6G_0$. Overall, the comparison between the experimental data at T = 300 K and the simulated positions of the conduction steps is in good agreement.
Further on, in order to investigate the evolution of conductance quantization of passivated Al-Ge-Al NW heterostructures with Ge segment lengths significantly smaller than their diameter, fig. 4.24 depicts conductance plots of a passivated device with a Ge segment length of 15 nm for different temperatures between T = 5 K and 300 K.

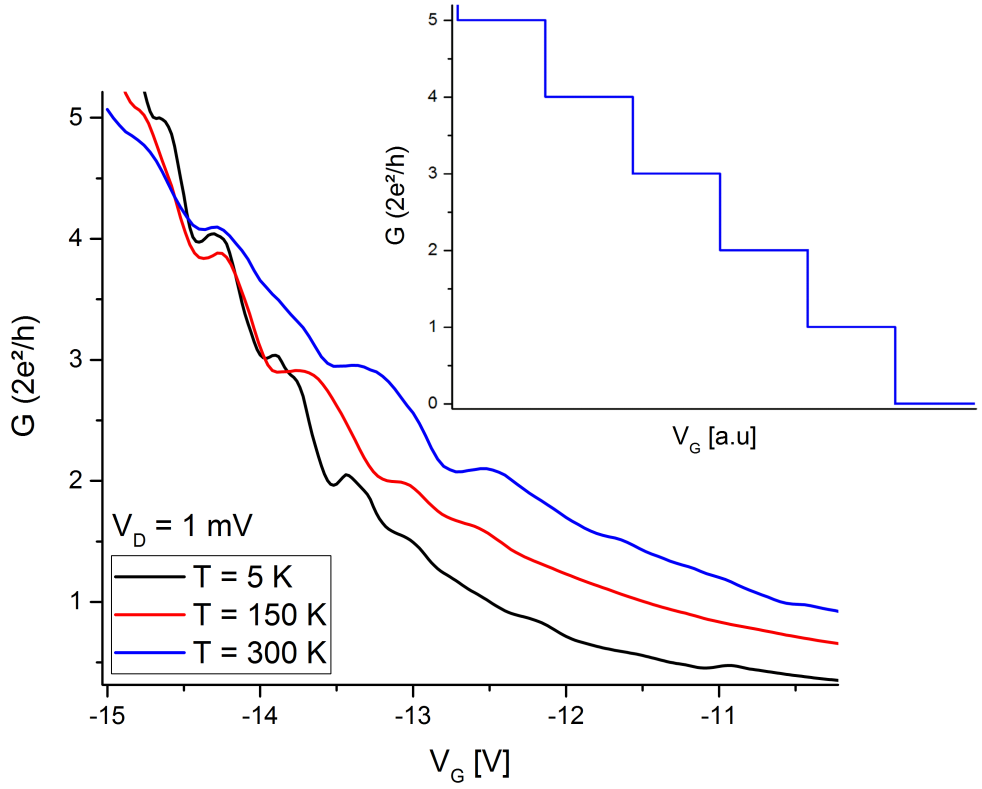

Figure 4.24: *Conductance quantization of a passivated Al-Ge-Al NW heterostructure with a Ge segment length of* 15 nm *for* V_D = 1 mV *as a function of temperature. The insert is showing an schematic illustration of the ideal conductance plot.*

It was observed that for Al-Ge-Al NW heterostructures with Ge segments smaller than their diameter, the simulated quantum confinement taking only the diameter of the Ge NW into account seams to be not valid anymore. This can most probably be dedicated to the increased confinement by the Ge segment. Hence, in contrast to the device with a Ge segment length of 28 nm, only G_0 conductance steps were observed. This is a clear indication, that all degeneracies arising from the structural symmetry of the NW have been lifted. Further on, the conductance plot reveals that at T = 5 K the $0.5G_0$ anomaly appearing in the passivated device with 28 nm long Ge segment is also occurring for the passivated Al-Ge-Al NW heterostructure with a 15 nm long Ge segment. However, the plateaus at $2G_0$, $3G_0$, $4G_0$ can clearly be identified, the G_0 plateau is very weak at T = 5 K. In the conductance plot measured at T = 150 K, the first plateau is even completely missing. Finally, at T = 300 K, a weak plateau at G_0, possibly due to thermal broadening, is visible again. Although until now the origins of absent conduction plateaus at certain temperatures is not fully understood, it is believed that a variety of different effects like e.g. impurity induced anomalies like tunneling resonances [99], single electron charging effects [100] or geometric transmission resonances arising from potential discontinuities [101, 102] are the most probable origins. However, thermal broadening should result in more pronounced conductance plateaus, in case of the $5G_0$ step, it can clearly be observed that the plateau is getting weaker with increasing temperatures. Moreover, fig. 4.24 clearly reveals, that the temperature dependence of the conductance is further reduced compared to the device with the 28 nm segment length.

4.5.4 Deviations Between Theory and Experimental Data

However conductance quantization of Al-Ge-Al NW heterostructures can clearly be observed up to T = 300 K, there are some deviations from the ideal case simulated in sec. 4.4. According the huge variety of different interfering effects, the origins of these deviations are hard to distinguish.
Although, ultrashort Ge segments have been observed by SEM investigations, some Al-Ge-Al NW heterostructures showed no signs of conductance quantization. As discussed in sec. 2.4.2, the observation of ballistic transport in NW based transistors is limited by scattering events originating from impurities and imperfections in the crystal lattice as well as surface states [103, 104]. Further on, the rotational symmetry of NWs favors additional orbital degeneracies, resulting in the absence of conductance plateaus [70].
In contrast to diffusive transport, which is only depending on the density of impurities, the total scattering matrix of the system is depending on the exact location of impurities and boundary fluctuations [71]. Hence slightly different impurity configurations can have a huge impact on the conductance [71]. The influence of different impurity configurations is assumed to be the most probable reason for degradations of the conductance below G_0 [71]. Therefore, however the fundamental conductance is defined as described in eq. 2.10, according to [105], taking the barrier shape of the quantum point contact (QPC) into account, conductance plateaus below G_0 are possible [71].

Hence, the definition of the conduction is expanded by the barrier shape parameter α:

$$G = \frac{2e^2}{\alpha h} \quad \alpha > 1 \tag{4.13}$$

Beside more exotic conduction anomalies like the so-called 0.7 feature [106], $\alpha = 2$ enables the possibility to observe the appearance of half plateaus. In this specific case, the voltage must drop symmetrically across the QPC [71, 107].
In addition, there is the problem with surface traps, discussed in sec. 4.3.4, which have a huge impact on the electrical behavior of the devices. According to the fact that above T = 77 K [96], the traps are not frozen out anymore, trap induced surface disorder is blurring out the sub-band profile [96].
Further on, one intrinsic problem of measuring ballistic transport in Al-Ge-Al NW heterostructures with Ge segments defined by Schottky barriers is backscattering, which is occurring directly at the abrupt interface between of the monocrystalline Al leads and the Ge segment. Hence, the conductance plateaus appear rounded [71].

Chapter 5

Summary and Outlook

In this diploma thesis, the synthesis of axial Al-Ge-Al NW heterostructures with abrupt metal-semiconductor interfaces is demonstrated. Ultrasmall Ge segments connected by monocrystalline Al leads were formed by a RTA induced exchange reaction between VLS grown single-crystalline Ge NWs and Al contact pads. Applying this exchange reaction is one of the key advantages of the fabrication strategy, because it enables the possibility to intrinsically connect a Ge nanodot without requiring a precise lithographic alignment of the contacts. Thus, it was possible to fabricate Al-Ge-Al NW heterostructures featuring ultrashort Ge segments down to 10 nm, which can be operated as back-gated FETs. Furthermore, the common problem of back-gated devices, which often suffer from the gate induced electric field being screened by the source and drain contacts is weakened. Although, it was possible to fabricate Al-Ge-Al NW heterostructures with Ge segment length smaller than 10 nm, these devices showed no response to the applied back-gate voltage. Regarding this problematic, the process was tuned to fabricate devices with Ge segments in the range between 10 nm and 30 nm.
According to the unstable native oxide of Ge and the large surface-to-volume ratio of NWs, adsorbates and surface traps are having a significant impact on the electrical characteristic of unpassivated Ge NW based devices. Therefore, efforts were shifted towards the development of Al-Ge-Al heterostructures based on Ge NWs passivated with a high quality high-k dielectric. An all-around passivation of the Ge NWs was achieved by depositing 20 nm of Al_2O_3.
The transfer characteristic of passivated Al-Ge-Al NW heterostructures clearly revealed p-type behavior. Further on, the ON-state current levels of passivated Al-Ge-Al NW heterostructures were up to 3 orders of magnitude higher compared to unpassivated devices. This behavior was a consequence of the altered interface between the NW and the oxide, which results from replacing the native Ge oxide with an high quality high-k dielectric. Whereas devices based on unpassivated Ge NWs showed almost no electrostatic modulation by the electric field of the back-gate, passivated devices depending on the Ge

segment length revealed an I_{ON}/I_{OFF} ratio of up to 5 orders of magnitude. Moreover, due to a reduction of adsorbates on the surface of the Ge NWs, the hysteresis effects in the transfer characteristic were significantly diminished.
The temperature dependence of the resistivity of passivated Al-Ge-Al NW heterostructures with different Ge segment lengths revealed that for devices with Ge segments between 15 nm and 28 nm the resistivity was only showing a weak temperature dependence compared to bulk Ge. Further on, the temperature dependence of the resistivity was getting dramatically smaller with decreasing Ge segment lengths. This behavior was assumed to be dedicated to a decrease of scattering of charge carriers with impurities and crystal defects with decreasing Ge segment lengths and is a clear indication for a shift towards ballistic transport.
Moreover, trap induced surface disorder, which is blurring out the sub-band profiles in the conductance measurements, was reduced by using passivated NWs. According to the increased current in passivated devices, the bias during the recording of the conductance measurements could be lowered. This increased the possibility for the observation of ballistic transport, because the influence of temperature and energy relaxation of injected hot electrons was significantly reduced.
In order to discuss the quantum confinement effects in Al-Ge-Al NW heterostructures, simulations of the eigenenergies concerning different NW diameters were implemented based on the 2D Schrödinger equation. A comparison between the simulations and the experimental data revealed evidence of conductance quantization in passivated Al-Ge-Al NW heterostructures with Ge segment lengths up to 30 nm at room-temperature.
Based on the gained insight into the fabrication of Al-Ge-Al NW heterostructures with ultrasmall Ge segments, further investigations could involve the adaption of the fabrication process towards a top-gate architecture, facilitating devices with even higher I_{ON}/I_{OFF} ratio. Concerning ballistic transport, using Ge NWs with smaller diameter as basis for the heterostructure formation process would result in a better quantum confinement. Hence, the number of populated sub-bands would be reduced and the remaining conduction plateaus would be distributed over a larger gate-voltage range. Therefore, it would be easier to observe conductance quantization.

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List of Abbreviations

Al	Aluminum
Al_2O_3	Aluminum Oxide
ALD	Atomic Layer Deposition
Ar	Argon
Au	Gold
BHF	Buffered Hydrofluoric Acid
C_3H_9Al	Trimethylaluminium
CMOS	Complementary Metal-Oxide-Semiconductor
CVD	Chemical Vapor Deposition
Co	Cobalt
Cr	Chrome
Cu	Copper
DI	Deionized Water
DRAM	Dynamic Random Access Memory
EBL	Electron Beam Lithography
ESD	Electrostatic Discharge
Fcc	Face Centered Cubic
FET	Field-Effect Transistor
FFT	Fast Fourier Transformation
FIB	Focused Ion Beam
GAA	Gate-All-Around
GaAs	Gallium Arsenide
GaN	Gallium Nitride
Ge	Germanium
GeO	Germanium Monoxide
GeO_2	Germanium Dioxide
GH_4	Germane
HAADF	High-Angle Annular Dark Field

H_2O	Water
HF	Hydrofluoric Acid
HfO_2	Hafnium Oxide
HI	Hydroiodic Acid
HRTEM	High-Resolution Transmission Electron Microscopy
II	Impact Ionization
IC	Integrated Circuit
I/V	Current-Voltage
LN_2	Liquid Nitrogen
InAs	Indium Arsenide
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
Mn	Manganese
N	Nitrogen
Ni	Nickel
NDR	Negative Differential Resistance
NW	Nanowire
PCB	Printed Circuit Board
PMMA	Polymethylmethacrylat
Pt	Platinum
QPC	Quantum Point Contact
RTA	Rapid Thermal Annealing
SSD	Solid-State-Drive
SEM	Scanning Electron Microscopy
Si	Silicon
SMUs	Source Measure Units
Sn	Tin
STEM	Scanning Transmission Electron Microscopy
Ti	Titanium
TiO_2	Titanium Oxide
VLS	Vapor-Liquid-Solid
VSS	Vapor-Solid-Solid
VSU	Voltage Source Unit
ZrO_2	Zirconium oxide

List of Symbols

a_B^*	Exciton Bohr Radius
D	Diffusion Coefficient
$\tilde{D}$	Interdiffusion Coefficient
∇C	Concentration Gradient Vector
e	Electronic Charge
E_A	Activation Energy
E_C	Charging Energy
E_F	Fermi Energy
G	Conductance
g_S	Spin Degeneracy
g_V	Valley Degeneracy
h, $\hbar$	Planck Constant, Reduced Planck Constant
I	Current
J	Flux of Diffusing Quantities
k	Wavenumber
k_B	Boltzmann Constant
L	Gate Length
l	Length
l_m	Scattering Mean Free Path
λ_F	Fermi Wavelength
M	Number of Modes
m^*	Effective Mass
μ	Electrochemical Potential
n	Electron Density
N_A, N_B	Fractional Concentrations
σ	Conductivity
T	Temperature
τ_m	Momentum Relaxation Time
W	Gate Width

Appendix A

Process Parameters

A.1 Measurement Module

Substrate Preparation

The substrate, used for the fabrication of the measurement module, was a highly p-doped 500 µm thick <100>-oriented Si wafer with 100 nm thermally grown SiO_2 on top. By using a diamond scribe, a 15x15 mm sample was manually cleaved from the wafer.

Substrate Cleaning

Prior to the patterning of the measurement module, the following cleaning procedures were performed:

- Ultrasonic cleaning for 120 s at 100 % power in acetone
- Ultrasonic cleaning for 120 s at 100 % power in isopropanol
- Drying with nitrogen

Photolithography

Process procedures needed for the patterning the structures on the measurement module:

- Spin coating of image reversal resist (AZ5214) at 9000 RPM (ramp-up constant 2)
- Softbake at 373 K for 60 s
- Alignment of mask for back-gate contacts on the substrate
- Exposure for 5.5 s (Karl Süss MicroTec MJB3)
- Immerse sample 30 s in developer solution (AZ726MIF)
- Immerse sample 35 s in deionized water (DI)
- Drying with nitrogen
- BHF dip (7:1) for 130 s
- Immerse sample 10 s in DI
- Drying with nitrogen
- Resist stripping with acetone
- Dip sample in isopropanol
- Drying with nitrogen
- Spin coating of image reversal resist (AZ5214) at 9000 RPM (ramp-up constant 2)
- Softbake at 373 K for 60 s
- Alignment of metalization mask and back-gate structures on the substrate
- Exposure for 4 s (Karl Süss MicroTec MJB3)
- Reversal bake at 394 K for 60 s
- Flood exposure for 20 s (Karl Süss MicroTec MJB3)

- Immerse sample 30 s in developer solution (AZ726MIF)
- Immerse sample 35 s in DI
- Drying with nitrogen
- BHF dip (7:1) for 5 s
- Immerse sample 10 s in DI
- Drying with nitrogen

Ti/Au Sputtering

The empirically determined sputter rates are $0.17\,\mathrm{nm\,s^{-1}}$ at 50 W for Ti and $1.6\,\mathrm{nm\,s^{-1}}$ at 50 W for Au. The following procedures were executed to deposit a 10 nm Ti and a 100 nm Au layer:

- Base pressure: 2×10^{-5} mbar
- Working pressure: 8×10^{-3} mbar
- Ti cleaning procedure: 60 s, 100 W
- 10 nm Ti deposition: 1x60 s, 50 W
- 200 nm Au deposition: 2x60 s, 50 W

Lift-Off

Subsequent to the sputter deposition, the excess metal was removed by the lift-off procedure listed below:

- Ultrasonic cleaning with 80 % power in acetone
- After 5 min, rinse the sample carefully with acetone
- Isopropanol dip
- Drying with nitrogen

A.2 Electrical Contact Formation

Electron Beam Lithography

The EBL pattering of individual contacts between the macroscopic Au pads and the deposited NWs was done by the following procedures:

- To provide a sufficient connection between the sample and the EBL system, the thermally grown SiO_2 layer was carefully removed from one macroscopic back-gate contact by using a diamond scribe
- Place sample on sample holder
- Insert sample holder via loadlock into the working chamber of the EBL-system
- Execute coordinate system alignment procedure
- Execute writefield alignment procedure
- Search NWs with a diameter between 25 nm and 35 nm in the immediate surroundings of the macroscopic Au contacts
- Remove sample via loadlock
- Spin coating of PMMA (AR-P 679.04) for 35 s at 4000 RPM (ramp-up constant 2)
- Bake sample for 900 s at 444 K
- Drawing of contacts with a spacing between 1.2 µm and 1.6 µm
- Place sample on sample holder
- Insert sample holder via loadlock into the working chamber
- Measure electron beam current with Faraday cup
- Calculate dwell times
- Execute coordinate system alignment procedure
- Execute writefield alignment procedure

- Start exposure process with 200 pA and a dose of 0.110 pA s
- Remove sample via loadlock
- Immerse sample for 35 s in developed solution (AR 600-56)
- Immerse sample for 35 s in stopper solution (AR 600-60)
- Drying with nitrogen

BHF dip

At the contact area between the Al contacts and the Ge NWs, the ALD grown Al_2O_3 was removed by applying the following BHF etching procedure:

- Dipping sample for 20 s in BHF (7:1) (etch rate approximately 1 nm s^{-1})
- Dipping sample for 10 s in DI
- Dipping sample for 10 s in another beaker filled with DI
- Drying with nitrogen

HI dip

Prior to the Al sputter deposition, the native GeO_2 layer on the NWs was removed by dipping the sample in diluted HI:

- Dilution: one part 57 % HI was diluted with three parts DI
- Dipping sample for 5 s in 14 % diluted HI (etch rate approximately 1 nm s^{-1})
- Dipping sample for 20 s in DI
- Drying with nitrogen

Al Sputtering

The sputter rate for the deposition of Al was empirically determined as $0.42\,\mathrm{nm\,s^{-1}}$ at 50 W. The following sputter parameter were used to deposit 100 nm of Al:

- Base pressure: 2×10^{-5}mbar
- Working pressure: 8×10^{-3}mbar
- Al cleaning procedure: 2x60 s, 100 W
- 100 nm Al deposition: 4x60 s, 50 W

Lift-Off

To finalize the fabrication of the Al contacts, the excess metal was removed from the sample by a lift-off procedure:

- Immerse sample in acetone and heat to a temperature of 326 K
- After 30 min, rinse the sample carefully with acetone
- Isopropanol dip
- Drying with nitrogen

A.3 Rapid Thermal Annealing

The used RTA procedure for the formation of Al-Ge-Al NW heterostructures is listed below:

- Open working chamber and place sample on quartz tray
- Pumping 120 s to 2 mbar
- Flushing 120 s with nitrogen
- Pumping 120 s to 2 mbar
- Flushing 120 s with nitrogen
- Pumping 120 s to 2 mbar
- Flushing 120 s with forming gas
- Heating to 574 K with a $75\,\mathrm{K\,s^{-1}}$ temperature ramp in forming gas atmosphere (no top-heat)
- To prevent an temperature overshoot, execute a $50\,\mathrm{K\,s^{-1}}$ temperature ramp to 624 K in forming gas atmosphere (no top-heat)
- Hold temperature for 180 s in forming gas atmosphere (no top-heat)
- Cooling to ambient temperature
- Open working chamber and remove sample from quartz tray

A.4 Preparations for Cryostat Measurements

In detail, the following steps were executed for adapting the measurement module to the sample holder of the cryostat:

- Cleaning the Cu substrate with isopropanol
- Solder a socket strip onto the PCB
- Glue the PCB on the Cu substrate using a epoxy resin
- Cleave the Al_2O_3 plate to fit onto the Cu substrate
- Glue the cleaved Al_2O_3 plate on the Cu substrate using a epoxy resin
- Glue the measurement module on the Al_2O_3 plate using silver conductive paint
- Use wire bonding (K&S iBond5000-Wedge) to connect the devices on the measurement module with the PCB
- Short-circuit the used conducting paths on the PCB using ultrasonic wire bonding to prevent damaging the devices by electrostatic discharge (ESD)
- Insert and connect sample with the holder on the cryostat finger
- Connect the cryostat with the HP 4156B analyzer and the temperature controller
- Remove the short-circuiting wire bonds carefully using a tweezer
- Test the functionality of the arrangement before inserting the finger into the cryostat
- Insert the finger into the cryostat
- Connect the vacuum pump with the cryostat
- After the vacuum reaches 10^{-6} mbar, start the cooling process by connecting the He/LN_2 dewar with the cryostat
- Use the temperature controller and the He/LN_2 flow valve of the dewar to adjust the desired temperature

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