Vienna University of Technology

DISSERTATION

ION TRANSPORT AT HETERO- AND HOMOPHASE BOUNDARIES OF YTTRIA STABILIZED ZIRCONIA (YSZ) THIN FILMS

ausgeführt am

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ABSTRACT

Numerous recent research activities in solid state ionics dealt with the ionic conductivity in nanomaterials, including thin films. Strong deviations from bulk properties are often found but only partly understood. Many studies were performed on yttria stabilized zirconia (YSZ), but only on YSZ bulk materials grain and grain boundary conductivity can easily be separated. For a better understanding of the conductivity mechanisms in thin films, separation of grain and grain boundary conductivities is needed, which becomes highly sophisticated and limited by the stray capacitance of the substrate. In this thesis a method is introduced which allows grain and grain boundary conductivity separation in nanocrystalline YSZ thin films by an optimized electrode geometry.

The other important property discussed in the thesis is the anisotropy of the conductivity of YSZ thin films. The conductivity of thin layers can be measured perpendicular and lateral to the thin film plane. Both types of measurements are important and reveal any potential anisotropy of the conductivity. Usually YSZ in- and across-plane conductivities are measured separately, because for in-plane measurements substrates with a higher resistivity than YSZ are needed while for across-plane measurements it is vice versa. Moreover, across-plane measurements are very difficult to be done on very thin layers, since this usually leads to short-circuits due to pin holes in the layer. Here a novel method is presented to overcome these problems by deposition of YSZ thin films on silicon. Silicon substrates usually have a native silica layer, which can be made use of in conductivity measurements. For across-plane conductivity measurements impedance spectra were obtained with circular microelectrodes on top of the YSZ layer and a counter electrode at the bottom side of the sample. The silica layer acts as a blocking capacitance for low frequencies, which helps to avoid short circuit, while for the high frequencies it is transmittable. The contribution of YSZ is identified by varying diameter of the electrodes and layer thickness. Silica and YSZ conductivities and capacitances can be successfully separated in the temperature range from 200 °C – 400 °C for YSZ films as thin as 20 nm. The across-plane conductivity of the YSZ films does not significantly depend on the layer thickness and is only slightly lower than the bulk conductivity of a YSZ polycrystalline sample. Experimental results of across-plane conductivity measurements are supported by finite element simulations (COMSOL).

The in-plane measurements on silicon substrates are done with parallel stripe electrodes on YSZ. The high dc resistance of the silica interlayer causes strongly frequency dependent current lines and allows determination of the in- and across-plane conductivity of the YSZ film from a single impedance spectrum. The high frequency part of the impedance spectrum corresponds to an across-plane measurement geometry while the low frequency part is governed by in-plane current flow. Validity of this analysis is proven by varying electrode width and distance between the electrodes. It is shown that the measured in-plane conductivity is about one order of magnitude lower than the across-plane bulk conductivity. This anisotropy is attributed to the blocking effect of grain boundaries in the columnar structured YSZ films. Again the experimental results are well supported by finite element simulations (COMSOL). This insulating oxide on silicon was varied (ZrO_2, Al_2O_3 and Y_2O_3 instead of SiO_2) and its effect on in- and across-plane conductivity was analysed.

KURZFASSUNG

Zahlreiche Forschungsaktivitäten auf dem Gebiet der Festkörperionik (solid state ionics) befassten sich mit der ionischen Leitfähigkeit in Nanomaterialien, einschließlich Dünnschichten. Starke Abweichungen von makroskopischen Eigenschaften im Volumen der Materialen wurden gefunden sind aber oft nur teilweise verstanden. Viele Studien wurden an Yttrium stabilisiertem Zirconiumdioxid (YSZ) durchgeführt, aber nur in Volumenproben von YSZ können Korn- und Korngrenzleitfähigkeiten leicht separiert werden. Auch für ein besseres Verständnis der Leitfähigkeitsmechanismen in dünnen Filmen wird die Trennung von Korn- und Korngrenzleitfähigkeiten benötigt, die jedoch bisher durch die Streukapazität des Substrats verhindert wurde. In dieser Arbeit wird ein Verfahren vorgeschlagen, welches die Korn- und Korngrenzleitfähigkeit in nanokristallinen YSZ Dünnschichten durch eine optimierte Elektrodengeometrie trennt.

Als weitere Eigenschaft wird in dieser Arbeit die Anisotropie der Leitfähigkeit von YSZ Dünnschichten diskutiert. Dabei wird die Leitfähigkeit von dünnen Schichten senkrecht und entlang der Dünnschichtebene (in-plane) gemessen. Beide Arten von Messungen sind wichtig, zeigen mögliche Anisotropien der Leitfähigkeit und können gewöhnlich nur separat gemessen werden. Für die senkrechten Messungen werden Substrate mit einem geringen spezifischen Widerstand als YSZ benötigt, während für die in-plane Messungen Substrate mit höherem Widerstand verwendet werden. Darüber hinaus können senkrechte Messungen schwierig auf sehr dünnen Schichten durchgeführt werden, da dies oft zu Kurzschlüssen aufgrund kleiner Löcher in der Schicht führt. Hier wird ein neues Verfahren vorgestellt, um diese Probleme durch Leitfähigkeitsmessungen von dünnen YSZ Schichten auf Silizium zu überwinden. Siliziumsubstrate haben in der Regel eine native Siliziumdioxidschicht, die für Leitfähigkeitsmessungen ausgenutzt werden kann. Für senkrechte Leitfähigkeitsmessungen wurden Impedanz-Spektren mit kreisförmigen Mikroelektroden auf der YSZ-Schicht und einer Gegenelektrode an der Unterseite einer Probe bestimmt. Die Siliziumoxidschicht wirkt dabei als Sperrkapazität für niedrige Frequenzen und vermeidet Kurzschlüsse, während sie für die hohen Frequenzen stromdurchlässig bleibt. Es wird belegt, dass unterschiedliche Elektrodendurchmesser und Schichtdicken die YSZ Impedanzspektren beeinflussen. Leitfähigkeiten und Kapazitäten von Siliziumoxid und YSZ Dünnschichten (bis 20 nm Schichtdicke) konnten im Temperaturbereich von 200 °C – 400 °C erfolgreich untersucht werden. Die Schichtdicke zeigt einen geringen Einfluß auf die senkrechte Leitfähigkeit der YSZ Schichten, welche nur geringfügig niedriger ist als die Leitfähigkeit einer polykristallinen YSZ-Probe. Experimentelle Ergebnisse von senkrechten Leitfähigkeitsmessungen werden durch Finite-Elemente-Simulationen (COMSOL) unterstützt.

Die in-plane Messungen wurden mit parallelen Streifenelektroden auf YSZ durchgeführt. Der hohe Gleichstromwiderstand der Siliziumoxid-Zwischenschicht bewirkt stark frequenzabhängige Stromverteilungen und erlaubt deswegen die Bestimmung der in-plane und senkrechten YSZ Leitfähigkeiten aus einen einzigen Impedanzspektrum. Der hochfrequente Teil eines Impedanzspektrum entspricht Experimenten mit senkrechtem Stromfluss, während der niederfrequente Teil die Leitfähigkeitsergebnisse einer in-plane Probengeometrie zeigt. Die Gültigkeit dieser Analyse wurde durch Variieren der Elektrodengeometrie bezüglich Breite und Abstand der Elektroden bewiesen. Es wird auch gezeigt, dass die gemessene Leitfähigkeit in der Ebene (in-plane Geometrie) etwa eine Größenordnung niedriger ist als die senkrecht gemessene Leitfähigkeit. Diese Anisotropie wird auf die Sperrwirkung der Korngrenzen in den säulenförmig strukturierten dünnen YSZ Schichten zurückgeführt. Die experimentellen Ergebnisse werden durch zusätzliche Finite-Elemente-Simulationen (COMSOL) unterstützt. Schließlich wurde das isolierende Oxid auf Si variiert (ZrO_2, Al_2O_3 und Y_2O_3 statt SiO_2) und der Einfluss auf die Leitfähigkeiten (senkrecht un in-plane) analysiert.

1 INTRODUCTION AND STATUS OF RESEARCH

1.1 Scope and goals of the thesis

Ion conduction in dimensionally reduced systems such as thin films has become a highly active research area with applications, for example, in sensors [1] or micro solid oxide fuel cells (SOFC) [2]. Numerous studies have been performed on yttria stabilized zirconia (YSZ) [3-10], gadolinium doped ceria (GDC) [3, 12-15] and other oxides. One reason for modified properties in thin films is the fact that they often consist of nanocrystalline grains and thus exhibit a high density of grain boundaries; grain boundary properties may also differ from those in micro-crystalline solids. Thus studies dealing with grain and grain boundary conductivities are important. The first goal of the thesis is to experimentally and theoretically (by means of finite element calculations) prove that inter-digit electrode geometry allows separation of grain and grain boundary contributions in impedance spectra.

Partly even more important is the conductivity along the interface to the substrate: For example, structural effects such as a lattice mismatch between the substrate and thin film may lead to increased ionic conductivity. In a recent theoretical study, an enhancement of ionic conductivity at YSZ/$SrTiO_3$ interfaces of up to three orders of magnitude was reported for 400 K [16]. Modified interfacial conductivities should be reflected in thickness dependent averaged film conductivities. In some papers it was indeed demonstrated that the conductivity of YSZ increases when the layer thickness decreases [17], while others did not notice any effect of the layer thickness [18]. More details on the ionic conductivity of thin YSZ films are discussed in section 1.3, but all together, it can certainly be concluded that ion conduction in films of nanometer-size thickness is still not well understood.

Most studies on the ionic conductivity of thin films dealt with the in-plane ion transport [17-19]. However, textured layers can be expected to exhibit a conductivity anisotropy: the effective in-plane conductivity is most probably affected by grain boundary resistances and the film–substrate interface may contribute as a parallel conductive path. The across-plane conductivity measurements of columnar structured thin films, on the other hand, can be expected to mainly represent the conductivity of the grain bulk (in case of blocking grain boundaries) and should be hardly affected by interfacial conduction.

Even though thus anisotropic transport properties are expected, these are hardly investigated. The main reason is the fact that for in-plane measurements ion conducting layers are usually prepared on highly resistive substrates (e.g. sapphire), while for investigating the across-plane conductivity, the layers have to be deposited onto substrates with higher conductivity (e.g. platinum). In the latter case, layers often have to be prepared with substantial thickness, because pores or pinholes [20] can easily lead to short-circuit of the film. The second goal of the thesis was therefore to significantly improve knowledge and methodology of thin films studies for conducting substrates. Measurements and theoretical studies (FEM) of the in- and across-plane conductivity were performed for YSZ layers on a silicon substrates.

1.2 Yttria stabilized zirconia: Applications and ionic conductivity

Pure zirconia has a high melting temperature (2860 °C [21]) and low thermal conductivity, however its applications are limited due to the polymorphism. Zirconia has two phase transition points and may exist in three phases – cubic, monoclinic and tetragonal. The monoclinic polymorph is stable at low temperatures and it transforms to the tetragonal phase at about 1000 °C [22]. Due to this transition the lattice volume changes strongly and this causes coating failure [22]. The phase transformation from tetragonal to cubic starts at 2300 °C. The cubic polymorph, which has the highest ionic conductivity, may be stabilized at room temperature by doping zirconia with dopants like CaO, MgO, Y_2O_3, CeO_2, Mg_3N_2, Si_3N_4, AlN [22-25]. Doped zirconia with yttria up to 3 mol% still exhibits monoclinic structure (a = 5.159 Å, b = 5.211 Å, c = 5.321 Å and $\beta = 99.16°$). A higher doping level partially stabilizes zirconia and leads to a tetragonal phase (3 – 5 mol% of dopants) or a mixture of tetragonal and cubic phases. Full stabilization of zirconia (about 8 mol%) leads to the cubic phase (*Figure 1.1*).

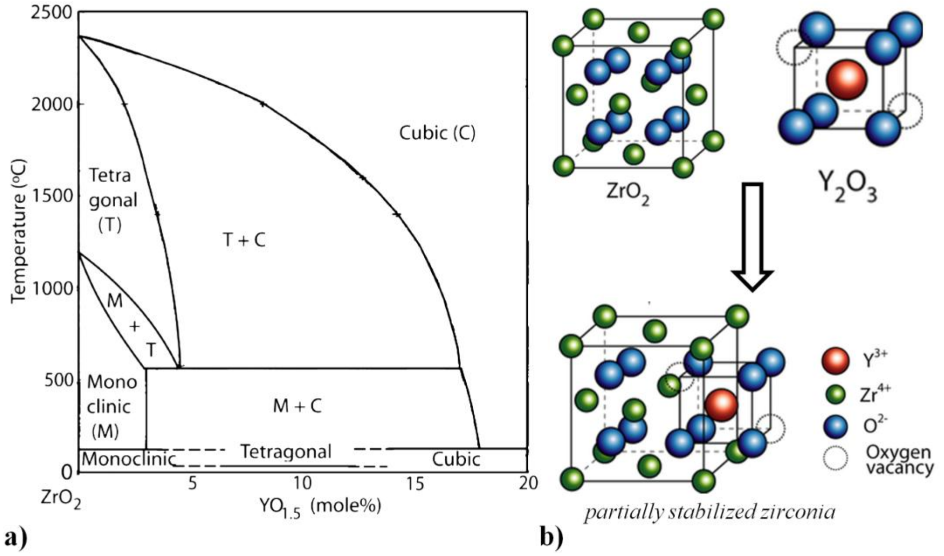

Figure 1.1. *Phase diagram of zirconia doped with yttrium [26] and structure of partially stabilized zirconia [27]*

Partially stabilized zirconia, due to its excellent thermal and mechanical properties is applied as a thermal barrier coating (TBC) [22]. The main requirement for TBCs is low thermal conductivity, high-temperature phase stability, high thermal expansion coefficient (CTE) and low Young's modulus [28]. Zirconia-based layers are also widely used as high refractive index material [29, 30]. Due to the high dielectric permittivity of YSZ, which varies in the range from 16 to 30 [31, 32], it is also investigated as a gate dielectric [33]. The relatively high ionic conductivity and mechanical strength of YSZ allows to apply it in oxygen sensors, oxygen separation membranes and fuel cells. One of the examples of YSZ applications is the lambda probe [34, 35] which is used for determining the amount of oxygen needed to optimize the air-fuel ratio of combustion engine. The working principle of a lambda probe is based on a Nernst cell consisting of an electrolyte (YSZ) and electrodes (usually platinum). The Nernst cell separates ambient air from exhaust gas. The voltage generated in this cell depends logarithmically on the oxygen partial pressure in the exhaust gases.

Another application of YSZ is the solid oxide fuel cells (SOFC) for power generation. Due to its high ionic conductivity, thermal and chemical stability YSZ is the most frequently applied electrolyte in SOFCs. In a SOFC electrochemical energy is being transformed into electrical energy and heat. The conversion is done using various fuels like hydrogen or natural gas. The hydrogen is supplied to the anode of the SOFC, where it oxidizes and water is formed. At the cathode the oxygen containing gas is supplied and oxygen is reduced to oxygen ions and incorporated into the electrolyte. The oxygen ions may pass through the electrolyte. Summarizing the working principle – the electrons are generated on the anode side and flow through the external circuit while oxygen ions flow through the electrolyte (*Figure 1.2*).

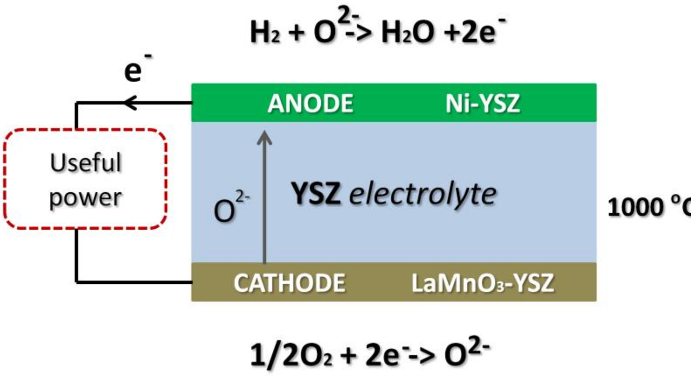

Figure 1.2. *The operation principle of SOFC's. The oxygen is reduced at the cathode site to oxygen ions. The oxygen ions diffuse through the electrolyte and on the anode side they are oxidized. As a result of the oxidation electrons are created*

The oxygen partial pressure difference between the anode and cathode forces oxygen ions to permeate through the electrolyte. Gas tightness of the electrolyte is very important for the efficiency of SOFCs, while both of the electrodes are generally porous. This concept is also applied in the µ-SOFC, which may replace the batteries in portable electronic devices. This technology is based on silicon [36-38].

The main requirement for ionic conductivity is a sufficiently high concentration of point defects in the material. The large number of point defects can be introduced into a material by doping. In zirconia oxygen vacancies are the mobile defects and they are formed upon doping with lower valent cations such as Y^{3+} or Ca^{2+}. It was found that first ionic conductivity increases with the doping level since higher doping concentration leads to a higher concentration of oxygen vacancies. However, very high concentrations of dopants may cause ordered vacancies which have a limited mobility. The dopant concentration has an optimal value where the product of oxygen vacancy concentration and mobility leads to the highest conductivity; for Y-doping this is at about 8 mol% Y_2O_3.

1.3 The conductivity of YSZ thin films

Since properties of thin films may differ from bulk materials, recently a lot of studies have been made on the ionic conductivity of thin layers and heterostructures, particularly on thin YSZ layers [17, 39-44]. For all of these studies thin YSZ layers were synthesized on highly resistive substrates and were measured with two parallel electrodes formed on the layer.

In ref. [17] YSZ layers were prepared by pulsed laser deposition on magnesium oxide substrates with the thickness in the range of 15-58 nm. It was found the enhancement of in-plane conductivity (*Figure 1.3*) which was attributed to the interface controlled diffusivity. In other study [43] YSZ layers were prepared on silicon substrate by sol-gel method with the thickness of ~600 nm and crystallite size of 50 nm. It was found 10 times higher conductivity than that of the YSZ pellets. The study on conductivity in thick YSZ layers (thickness 600-1500 nm) [44] which were deposited on sapphire substrate by a PLD method demonstrated close conductivity values to that of bulk specimens (*Figure 1.3*). Other study on thick YSZ layers (thickness 11 µm) deposited by e-beam method on quartz substrate also demonstrated conductivity values similar to that of bulk.

For reasons of comparison the conductivities of YSZ layers obtained in those studies are plotted in *Figure 1.3*. The conductivity of YSZ pellet [41] is also included in the graph. Obviously the conductivity data are widely spread and more details of the conductivity of YSZ are discussed in the following.

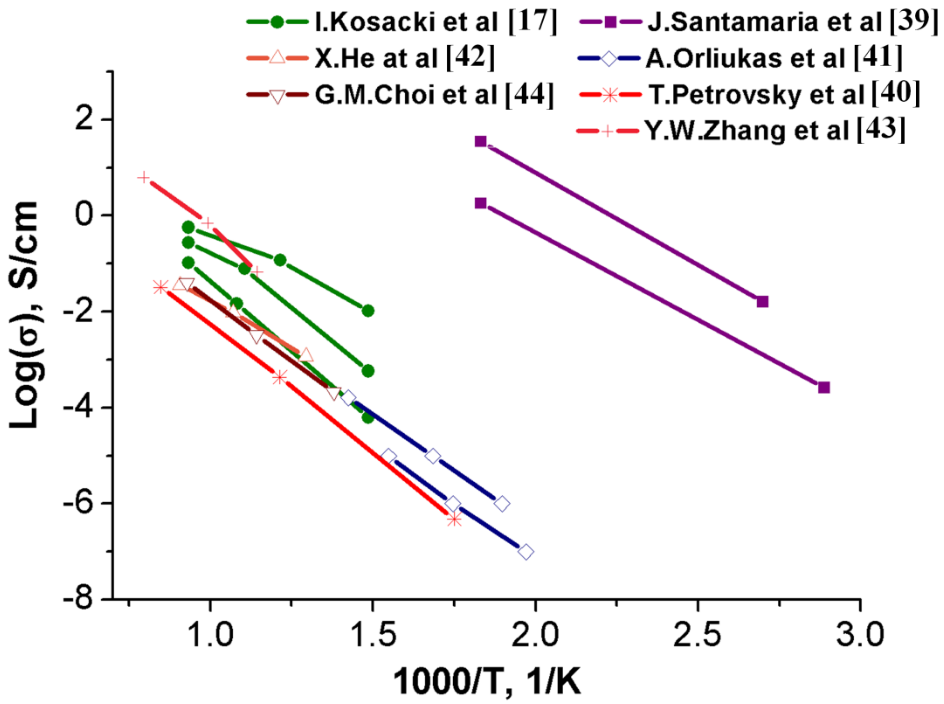

Figure 1.3. *Temperature dependence of electrical conductivity of YSZ layers obtained in various studies*

The conductivity of polycrystalline materials consists of two components - bulk conductivity and conductivity of grain boundaries. The grain boundaries in the material might have significantly different properties than the grain bulk. Between two adjacent crystalline regions there is always a disordered region, where higher defect concentration is usually found. Grain boundaries may exhibit a completely different structure, which plays an important role for ionic conductivity. The ionic conductivity depends on defect concentration and mobility of charge carriers. Grain boundaries may lower the mobility of the ions. There are a lot of studies on different materials such as $BaZrO_3$ doped with yttria, $SrTiO_3$, GDC or YSZ where particularly the conductivity of grain boundaries was investigated.

In YSZ grain boundaries exhibit a two or three orders of magnitude lower conductivity than the bulk, and have higher activation energies. Space charges and impurity segregation are discussed as the main reasons of the low ionic conductivity at grain boundaries. Grain boundaries in YSZ are characterized by yttria segregation to the grain boundary region, which may lead to a depletion of oxygen vacancies in the space charge zone (*Figure 1.4*) [18, 45].

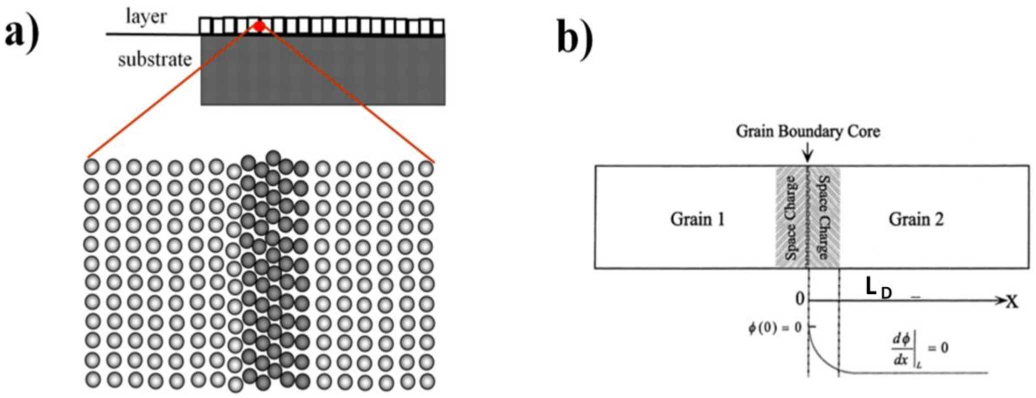

Figure 1.4. *Grain boundaries exhibit a completely different structure of the material (a). Schematic representation of a grain boundary with varied electrostatic field (b) [45]*

The oxygen vacancy concentration (c_v) in this zone is described by [*45*]:

$$\frac{c_V(x)}{c_V(\infty)} = e^{\left(-\frac{1}{2}\left(\frac{x-\lambda'}{L_D}\right)^2\right)} \qquad \textbf{(Eq. 1.1)}$$

where L_D – Debye length and λ’ – thickness of one space charge layer. It was found that the thickness of both space charge layers in YSZ is approximately 2.5 nm.

Grain boundary conductivity studies are usually done on bulk materials (mechanically pressed and sintered pellets). In this case the measurement of grain and grain boundary conductivity is performed by electrochemical impedance spectroscopy. Two or three semicircles are found in the Nyquist plot (*Figure 1.5*) and data evaluation is straightforward.

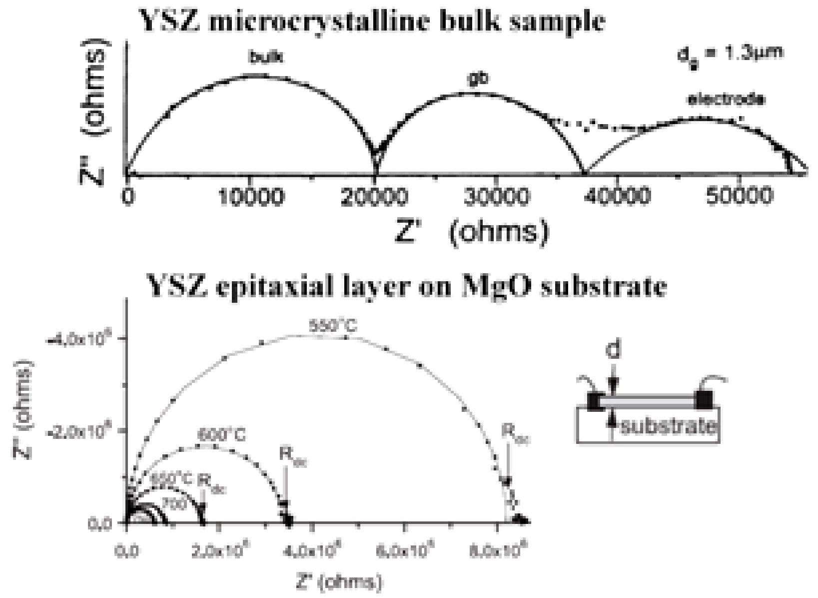

Figure 1.5. *Nyquist plots of YSZ microcrystalline bulk sample and of a YSZ epitaxial thin layer on MgO substrate [46]*

There are many studies on the ionic conductivity in YSZ, where the effect of the crystal size was probed. Micrometer range crystallites lead to activation energies for bulk conductivity of approximately 0.85 eV above 700 °C [47] and 1.14 eV below 700 °C [47]. For grain boundaries it is 1.0 - 1.2 eV [48]. In YSZ grain boundaries may exhibit different chemical composition. This strongly depends on the purity of YSZ which very often includes silica, hafnium and other impurities. There are a number of publications which have demonstrated the effect of silica on the conductivity [52, 53]. Silica tends to segregate into a grain boundary region. The resulting grain boundary silicate phase has a low oxygen ion conductivity and high activation energies.

The interfaces in nanomaterials are very close spaced and the effect of interfaces may therefore increase, while decreasing the crystallite size. A number of studies have been made to measure the ionic conductivity of nanocrystalline YSZ [49-63]. Some papers have claimed an increase of the specific grain boundary conductivity due to the low silicon content in grain boundaries of nanomaterials [50]. It was found that ionic conductivity activation energies in nanomaterials may decrease to ~1 eV for grain boundaries and ~0.8 eV for grain bulk [50]. Another study [51] on nanocrystalline YSZ also observed a conductivity increase, which was reported to be one order of magnitude higher than the YSZ bulk conductivity.

The understanding of conductivity mechanisms in thin YSZ layers is another relevant topic of solid state ionics. In most of the studies YSZ layers are synthesized on non-conductive substrates (quartz, sapphire or magnesia) [5, 9, 11, 15, 17-20] and impedance is measured with two parallel electrodes formed on the layer. In this case parasitic capacitances hinder the separation of grain and grain boundaries in impedance spectrum and measurements lead to two semicircles in impedance spectrum (*Figure 1.5*). The high frequency semicircle is attributed to superposition of the grain and grain boundary contributions and low frequency semicircle is attributed to electrodes effect. However, the separation of grain and grain boundary contributions with a special geometry of electrodes is possible and is discussed in details in Sec. 3.3 and Sec. 4.1.

The other important research field is the hetero-interface effect of the ionic conductivity. The interfaces between two ionic conductors or ionic conductor and a substrate are highly interesting due to the different chemical and physical properties at the boundary [60-64]. Mass transport along such interfaces might be significantly different, since it may have a different structure and chemical composition. Moreover, the interfaces may cause an ion redistribution in the space charge regions. In the study of CaF_2 and BaF_2 heterostructures, it was demonstrated that the ionic conductivity increases proportionally to the number of interfaces. The ionic conductivity of the CaF_2/BaF_2 heterolayer increases by two orders of magnitude then the layer thickness is decreased from 500 to 16 nm and neighbouring space-charge layers overlap. Moreover, at the interface of two phases strain may develop which may strongly increase or decrease the conductivity. In the previous studies on bulk materials it has been demonstrated that compressive strains may lower the ionic conductivity in yttrium doped barium cerate [54]. An increase of the proton conductivity activation energy was found and the proton conductivity depends on the space available in the lattice, which decreases with the applied compressive strains [55].

Many theoretical and experimental studies were also performed on strains effect on the conductivity of YSZ [56-59]. From these results including MD calculations of strained YSZ, we can thus affirm that the presence of a biaxial tensile strain could effectively lead to an increased conductivity in zirconia.

Usually, to separate the interface contribution from the bulk conductivity the thickness of the layer is varied systematically. In thin film cases three independent conduction paths may exist (*Figure 1.6*): through the volume regions including transport perpendicular to grain boundary, along the interfacial regions at the conductor/insulator boundary and along the grain boundaries. In case interfacial conductivity is much higher than that of the volume, the interfacial conductivity could be evaluated from the slope of a σ (*t*) graph with t thickness (*Figure 1.6*). The effect of blocking grain boundaries, however, is generally not visible in impedance spectra, see *Figure 1.5*.

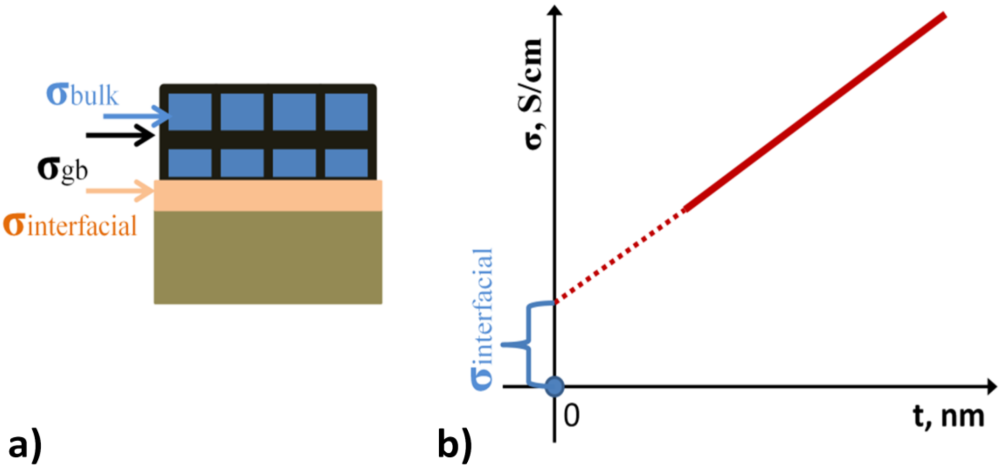

Figure 1.6. *a) The ionic conductivity of a thin film consists of bulk, grain boundary and interfacial conductivities. b) The contribution of the interfacial conductivity can be estimated from σ(t) graph*

The ionic conductivity in thin films is usually measured with two different geometries of the electrodes: in- and across-plane (*Figure 1.7*). Most of the studies presented in this thesis are dealing with these two measurement geometries. The in-plane conductivity measurements are done on two parallel electrodes which are prepared on top of the layer. The resistivity of the substrate has to be much higher than that of the layer in order to ensure, that the current would pass only through the layer. Usually in this case thin layers are deposited on highly resistive ceramic substrates like sapphire or magnesia.

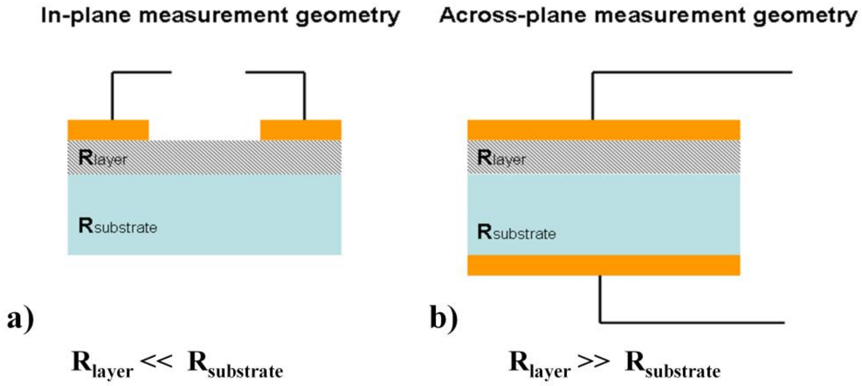

Figure 1.7. *In- and across-plane measurement geometries applied for conductivity measurements of thin films.*

There are only a couple of studies on the across-plane conductivity of YSZ layers [42, 44, 64]. For the across-plane measurement one conductive electrode is formed on top of the layer, while the other on the bottom side of a substrate (*Figure 1.7 b*). The main requirement for a sample in across-plane measurement is a highly conductive substrate. In this case the current flow direction is parallel to the normal vector of the thin film surface. For across-plane conductivity measurements a metallic interlayer may be used. The metallic interlayer is being deposited on top of the substrate. In- and across-plane measurements, due to the mentioned requirements for the substrates, are done separately on different samples. Combining both conductivity measurements may reveal an anisotropy of the conductivity in thin films as it was demonstrated in ref. [42, 44] on YSZ layers (*Figure 1.8*). However, the evaluation of the anisotropy in these measurements is not very precise, since it requires different layers formed on different substrates. The substrate may affect the crystallinity of the layer or even the chemical composition (silicon diffusion in a layer from the silicon / quartz substrate) and hence such a comparison of the measurement is not straightforward. Moreover it is worth of mentioning that across-plane measurements are usually done on relatively thick layers (>500 nm), since pin holes in the layer easily lead to a short-circuit of the measurement [44].

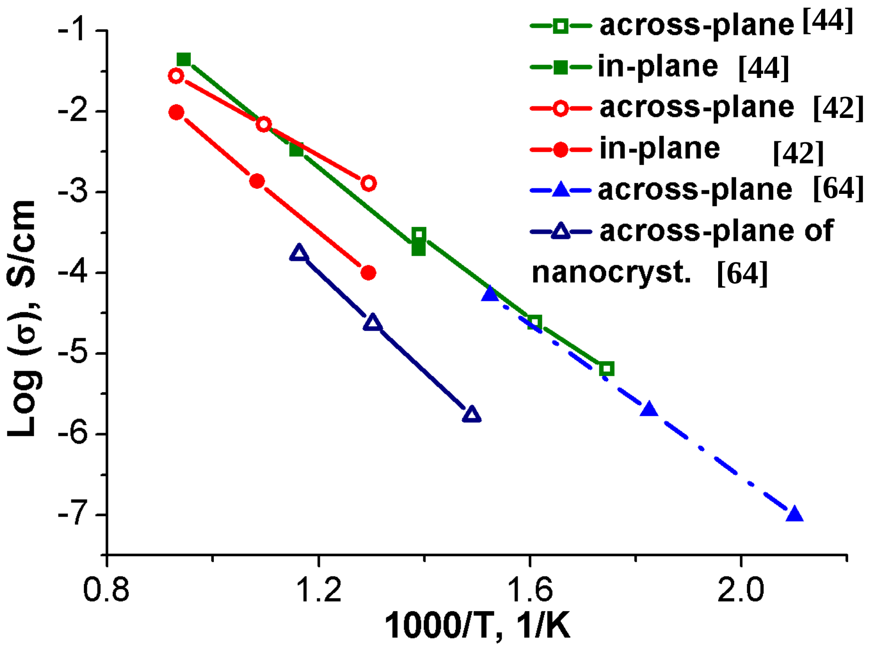

Figure 1.8. *Arrhenius plots from previous studies on in- and across-plane conductivity of YSZ thin films (in ref.[42] YSZ layer thickness – 11 µm, in ref.[44] YSZ thickness ~ 1 µm and in ref.[64] layer thickness - 220-600 nm)*

Ref. [43] dealt with the in-plane impedance measurements of YSZ and 8ScZr thin films on a silicon substrate. In this case spectra consisted of one high frequency semicircle and it was attributed to the superposition of bulk and grain boundary effects (*Figure 1.9*). The measurements were done using platinum electrodes which were deposited on the sample sides as shown in *Figure 1.9*. It is not very well understood why the current flow through the layer, which contains a higher resistance than the silicon substrate.

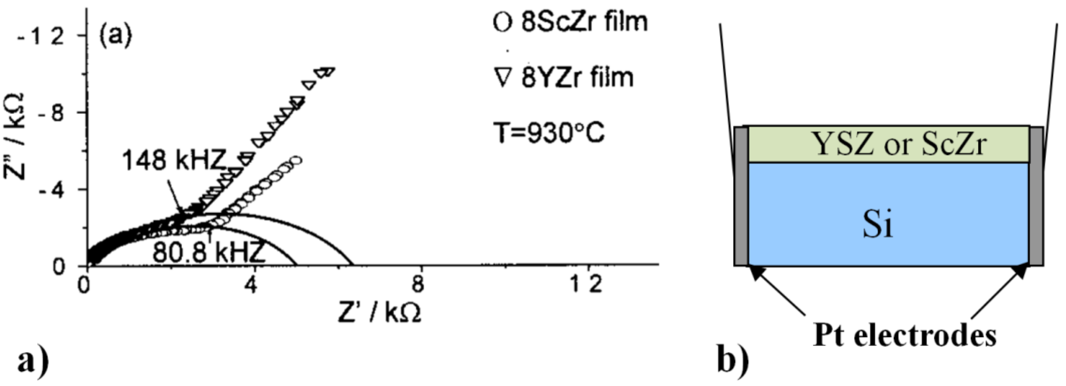

Figure 1.9. *a) Nyquist plot of an in –plane measurement on ScZr and YSZ thin layers (t = 580 nm)[43] and b) measurement sketch*

1.4 YSZ thin film synthesis

YSZ layers can be prepared by various physical (PVD) and chemical (CVD) vapour deposition methods such as: electron beam evaporation [65-70], pulsed laser deposition [5, 71], magnetron sputtering [72], plasma spraying [73], sol-gel method [74], etc. All mentioned techniques are different by nature and have their own advantages. The properties of the layers, crystallinity, growth mode, etc. strongly depend on the deposition temperature, pressure, substrate material, surface cleanness and crystal orientation [75]. The structure of thin layers can be controlled during the deposition by varying deposition parameters. Firstly it was demonstrated that the microstructure of the layer is affected by substrate temperature and it strongly depends on the ratio of substrate temperature to the absolute melting point of deposited material ($T_{substrate}/T_{melting}$)[75]. Thornton developed the model of thin film microstructure development in dependence of deposition parameters where the pressure effect was also considered. Mochan, Demchishin and Thornton structure model depending on the background pressure and film growth temperature suggests three structure zones. The first zone ($T_{substrate}/T_{melting} < 0.3$): low substrate temperature leads to a limited adatom mobility on the surface and porous columnar layers are formed. The second zone ($0.3<T_{substrate}/T_{melting} < 0.5$): at higher substrate temperatures the surface diffusion becomes prevailing and dense polycrystalline columnar structure layers are formed. The third zone ($T_{substrate}/T_{melting} >0.5$): at high temperature bulk diffusion is dominating which enhances crystallization and grain growth. This model was explicitly discussed for pulsed laser deposition of the YSZ thin film case by Infortuna [3]. It was found that the higher background pressure strongly affects layer density – layers prepared at higher pressure (> 30 Pa O_2) were porous. According to these experiments, the effects of pressure and temperature for the YSZ layer structure were suggested (*Figure 1.10*). Since the PLD method is the main deposition technique applied for YSZ layer synthesis in this thesis, the governing parameters of PLD will be discussed more explicitly.

In the case of PLD the layer is formed from molten droplets on the substrate, which are expelled from the target. The microstructure strongly depends on the cooling rate on the substrate. Due to the low substrate temperature and rapid cooling of arriving droplets on the substrate surface metastable phases might be formed. The laser fluence is the major parameter on the particulate size and density.

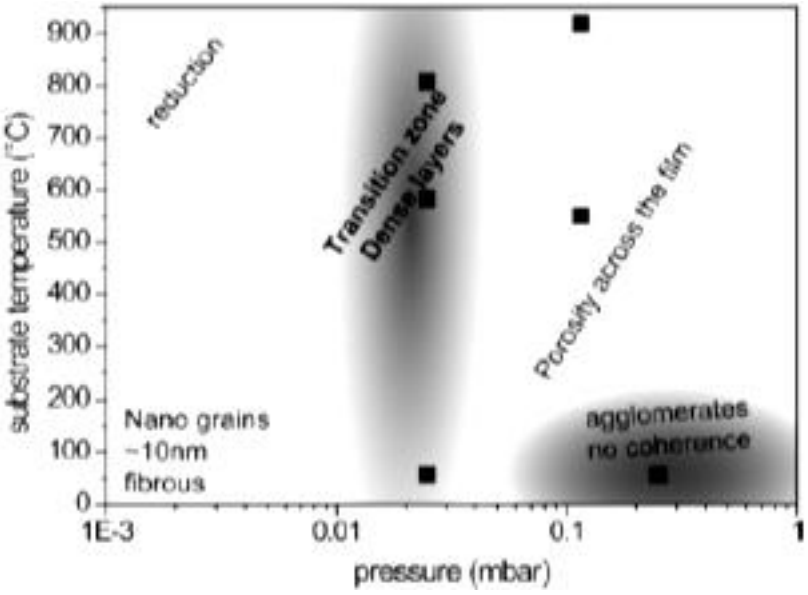

Figure 1.10. *The structure map for YSZ thin layers prepared by the PLD method with varied substrate temperature and oxygen pressure [3]*

The effect of the substrate is also very important for the microstructure (porosity, roughness) and structure (crystalline orientation) of the layer [76, 77]. The selection of substrate is also determined for the conductivity measurements, see above. There are many studies of YSZ thin film deposition on silicon substrates, since YSZ thin films are often used as a buffer layer for superconductive layers [78], as a gate insulators [75, 77-79], oxygen sensors [80] and in micro fuel cells [38]. Since a lot of studies in this thesis were performed on YSZ layer on a silicon substrate, particular attention has to be paid to the growth of YSZ thin films on silicon.

It was reported in all previously mentioned studies, that during the deposition of YSZ a native silica layer is always present on silicon. This interlayer worsens the mechanical properties of the YSZ layer and is unfavourable. It was demonstrated in previous studies that the silica interlayer might be changed from amorphous to crystalline or even it may disappear. It was also shown that the structure of the silica interlayer strongly depends on the oxygen background pressure during the deposition and at low pressure (<7 Pa, 730 °C [78]) it is reduced from SiO_2 to SiO. For the thicker YSZ layers it might completely disappear. The free energy for ZrO_2 (ΔG = -941.6 kJ/kmol at 800 K [78]) formation is lower than for SiO_2 (ΔG = -734.2 kJ/kmol at 800 K [78]), which leads to a reduction of silica at low pressures. Another study also reported the effect of oxygen pressure during e-beam deposition of YSZ layers [65]. It was found that the variation of the deposition pressure (from 0.1 to 0.001 Pa) firstly affects the thickness of the silicon interlayer. In a further study it was shown that the crystal orientation of the YSZ layers strongly depends on the substrate temperature during the deposition and crystalline orientation of a substrate. It was found that for Si (111) at higher temperatures (>700 °C) YSZ layers are highly oriented (111). The possible arrangement of the YSZ unit cell on silicon (111) is shown in *Figure 1.11*. YSZ on Si (111) has a preferential orientation, however other orientations may also appear at lower deposition temperatures [78].

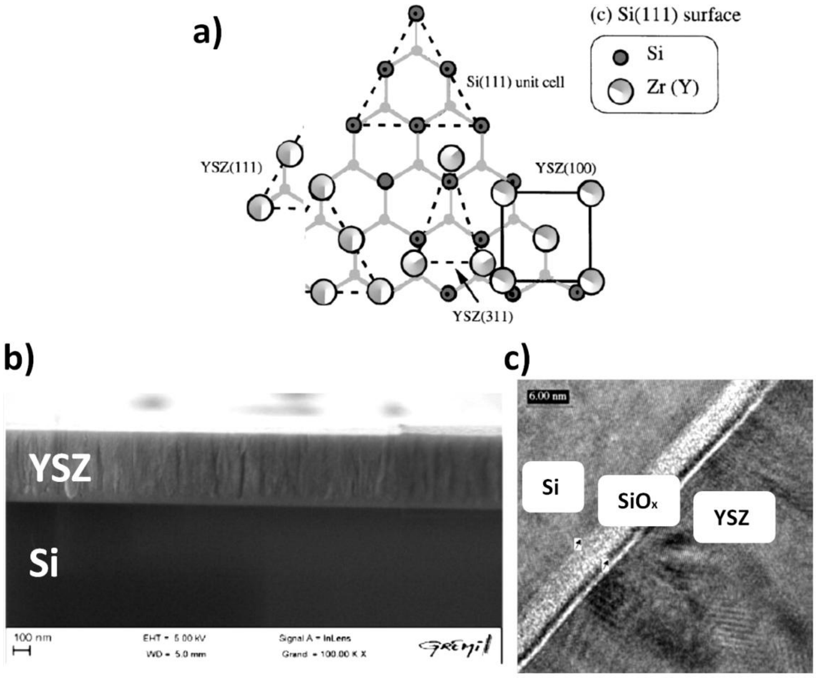

Figure 1.11. *a) The rearrangement of Zr on the silicon substrate [81];b) and c) cross-section image of PLD layer deposited on silicon substrate [79]*

There are some comparative studies between magnetron sputtering and PLD method [*71*]. It was found that the PLD method, when employed with a substrate heater, leads to a fine structured layer with columnar microstructure, which was observed from SEM cross-section image (*Figure 1.11 b*). Since the same PLD deposition parameters were used in the thesis we also expect a columnar microstructure YSZ layers here.

2.1 Thin film deposition methods

2.1.1 Pulsed laser deposition (PLD)

YSZ thin layers were deposited on alumina (0001) and crystalline silicon (111) substrates (CrysTec GmbH, Germany). The deposition targets were prepared from 8 mol % Y_2O_3 doped ZrO_2 powder (Tosoh, Japan). YSZ targets were formed by unaxial pressing of YSZ powder. Pressed pellets were annealed at 1200 °C for 10 hours. In order to form a smooth surface annealed pellets were grinded and polished with a diamond disk. During the PLD process (the principal sketch of the PLD system is shown in Figure 2.1), the substrates were heated to a maximum set temperature of 900 °C. Set temperature was measured by a K-type thermocouple, which is placed very close to the substrate. Additionally, temperature was also measured by IR pyrometer and measurements resulted in ~600 °C. The emissivity value for the pyrometer was set to 0.9. The huge difference between the set temperature and the temperature measured by the pyrometer may result from the bad thermal contact between the heater and the substrate. The vacuum chamber was initially evacuated up to 0.02 Pa with the rotary and turbo pumps. The YSZ films were deposited in oxygen ambience, the oxygen pressure was 4 Pa. The deposition was performed with an eximer KrF laser (248 nm) (“Lambda Physik”). The repetition rate and energy of the laser were 5 Hz and 400 mJ. The beam spot size was 7 mm^2 and the fluence of the beam was approximately 2 J/cm^2 on the rotating YSZ target. The laser beam entered the chamber at an angle of 45° and hit the rotating YSZ target. The distance between the target and the substrate is a very important parameter for deposition rate and homogeneity of the layer thickness. From the previous experiments it was found that homogeneous layers were formed with a distance of 6.3 cm between the target and the substrate. This distance was used for deposition and it led to a deposition rate of about 3 nm/min. In order to sustain the uniform deposition rate during the whole process, the YSZ targets were changed after each 30 min of deposition. In a rotating target holder three YSZ targets were placed, which is needed for longer deposition processes. Further details on PLD preparation are given in the chapter – Measurement Results and Discussion.

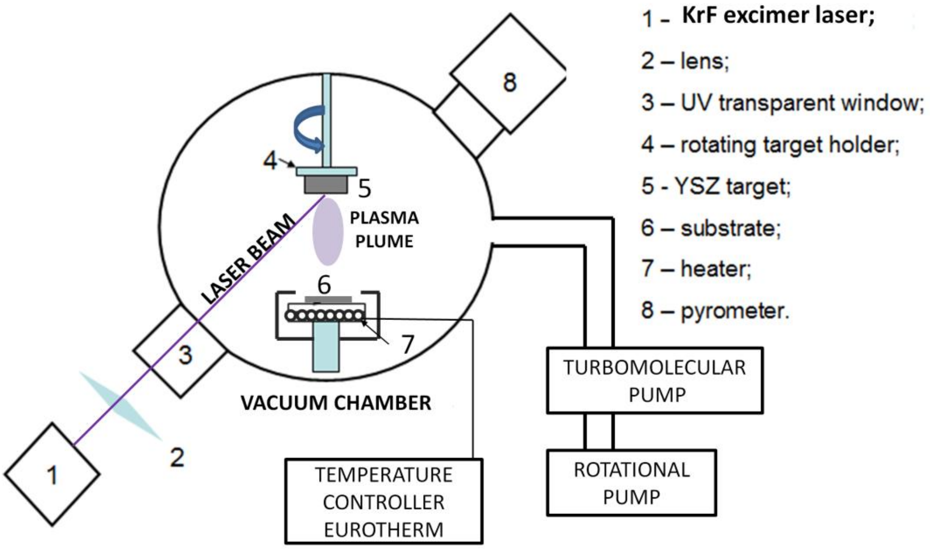

Figure 2.1. *The sketch of the pulsed laser deposition (PLD) system*

2.1.2 Sol-gel method

In some studies YSZ layers were prepared by sol-gel technique. The sol-gel layers were made by two different procedures:

A. For across-plane measurements layers were prepared by aqueous sol–gel citrate-precursor method in the Chemistry Department of Vilnius University [82]. For the preparation of Y-Zr-O nitrate-citrate sols analytical grade $ZrO(NO_3)_2{\cdot}2H_2O$ and $Y(NO_3)_3{\cdot}6H_2O$ were used as starting materials. The stoichiometric amounts of zirconium oxonitrate and yttrium nitrate were dissolved in 80 ml of aqueous solution of citric acid at 80 °C and afterwards evaporated in order to form gels. The prepared gel was diluted with ethanol (1:4) and used for layers preparation by spin-coating technique. Gel was pipetted onto a rotating silicon (111) substrate with a rotation speed of 2000 rpm for 40 s. The silicon substrates were cleaned in hydrogen peroxide and afterwards in sulfuric acid. In order to get thicker layers the spin coating procedure was repeated a couple of times. After preparation of each YSZ layer on a substrate, the layer was heated to 400 °C for 10 min. After the third coating procedure the formed layer was annealed for 5 h at 800 °C. The thickness of the YSZ layer was measured from SEM cross-section and by laser ellipsometry and resulted to 160 nm.

B. The structure effect on the ionic conductivity was studied on YSZ layers, which were prepared by two different methods - sol-gel and PLD. The YSZ sol-gel layers were formed by alkoxide route. The layers were prepared at the Institute of Chemical Technologies and Analytics at Vienna University of Technology. The preparation procedure of the sol was the same as in ref. [74]. Zr (IV) butoxide solution (80 wt. % in 1-butanol) (Aldrich, USA) was used as a starting material, which was then diluted with isopropanol. YSZ sol was formed by adding yttrium salt solution to the zirconia sol. Acetic acid (100 % p.a.), Y (III) nitrate 3-hexahydrate (99 %) and 2-propanol (99.5 %) were obtained from Merck, Germany. The composition of the sol corresponded to 7.8 % YSZ. The sol was diluted 1:1 with a mixture of 10 % vol. HNO_3 conc. in 2-propanol. 80 μl of the YSZ sol was dripped onto the spinning silicon substrate with the rotational speed to 12,000 rpm. The rotational speed was maintained for 30 seconds. Afterwards layers were dried at room temperature and thereafter at 100 °C for 2 minutes each. The calcination was done at 500 °C for 10 minutes. Finally, the layer was sintered for 12 hours at 1200 °C with heating and cooling rate of 10 °C/min.

2.1.3 Atomic layer deposition (ALD)

For studying of the dielectric interlayer effect on the conductivity, dielectric layers were prepared by ALD method. The different dielectric interlayers (Al_2O_3 Y_2O_3 and ZrO_2) were deposited on silicon substrate. The deposition temperatures for Al_2O_3 and ZrO_2 were 200 °C and 250 °C for Y_2O_3. Al_2O_3 interlayers were grown from trimethylaluminum and H_2O, Y_2O_3 interlayers were formed from tris(methylcyclopentadienyl)yttrium and H_2O and ZrO_2 interlayers prepared from Tetrakis(dimethylamino)-zirconium and H_2O. The growth rate for Al_2O_3 was 1.1 Å per ALD cycle, 1.0 Å for ZrO_2 and 1.5 Å for Y_2O_3. Pulse duration was varied in the range of 0.015 s up to 1 s and the purge times were varied between 1 s and 30 s. The thickness of all dielectric layers was evaluated from the deposition rates and led to a thickness of approximately 4 nm. All the layers were prepared at the Institute of Solid State Electronics of Vienna University of Technology. The ALD system used for the deposition was TFS 200 from Beneq.

2.2 Electrochemical impedance spectroscopy (EIS)

2.2.1 Concept of EIS

The concept of impedances was introduced by Oliver Heaviside in the 1880 and up to now it is a highly developed and widely used tool for materials characterization. A sample electrical resistance may be measured by the direct current method and is defined by Ohm's law:

$$R = \frac{U}{I} \qquad \textbf{(Eq. 2.1)}$$

where R – resistance, U – voltage and I – current.

However, in ceramic materials with predominant ionic conductivity (and in many other materials) alternating current (impedance) measurements are more useful and reveal more information. Impedance spectroscopy is also widely used in electrochemistry for fuel cells, batteries or corrosion studies, since impedance measurements may reveal physical characteristics of electrochemical system such as electrode reaction rates. Impedance measurements are done by applying an alternating signal on the investigated system:

$$U = U_m \sin (\omega t) \qquad \textbf{(Eq. 2.2)}$$

where U_m – amplitude of the voltage, ω – angular frequency ($\omega = 2\nu\pi$), t – time.

For a resistor the phase in between the alternating current and voltage matches while for a capacitor and inductor the phase between the voltage and current is shifted. The measured current is given by:

$$I = I_m \sin (\omega t + \varphi) \qquad \textbf{(Eq. 2.3)}$$

where I_m– amplitude of the current, φ – phase shift.

According to Ohm's law, the impedance (Z) is given by:

$$Z = \frac{U_m \cdot sin\,(\omega t)}{I'_m \cdot sin\,(\omega t + \varphi)}$$ **(Eq. 2.4)**

In order to simplify the situation this is transfer to complex numbers:

$$\hat{Z} = Z' + j\omega Z''$$ **(Eq. 2.5)**

with $|\hat{Z}| = U_m/I_m$ and $tan\varphi = Z''/Z'$.

The system's response is usually analysed by the equivalent circuit method. Each process of an electrochemical system is represented by a passive electrical circuit element. The impedance of a resistance, capacitance and an inductor is given by:

$$\hat{Z}_{resistor} = R$$ **(Eq. 2.6)**

$$\hat{Z}_{capacitor} = \frac{1}{j\omega C}$$ **(Eq. 2.7)**

$$\hat{Z}_{inductor} = j\omega L$$ **(Eq. 2.8)**

Figure 2.2. *Equivalent circuit elements*

In the most simple cases system can behave as a capacitor or resistor, but in reality it is more complex and a couple of circuit elements are required.

Impedance spectroscopy allows to determine conductivity and permittivity of a system. Conductivity describes the charge transport in a system, while the permittivity is related to the current flow due to the polarization. Depending on applied frequency the polarization might be electronic, orientational or ionic. The displacement current corresponds to the polarization related current flow through the material at higher frequencies, while at the low frequencies Faradaic (free) current due to the free charge carriers flows. The displacement current is related to the imaginary admittance part, while the free current can be attributed to the real part of the admittance. Both currents contribute to impedance spectra.

Impedance results are often presented in Nyquist plots, where the imaginary part of the impedance is plotted on the y axis and the real part on the x axis. In order to illustrate some impedance spectra simulations with equivalent circuits were done (*Figure 2.3*).

For dielectric materials investigations often modulus plots are used (*Figure 2.3 c*). The modulus (M^*) is a derivative of the complex impedance and can be expressed as:

$$\widehat{M} = M' + j \cdot M'' = j \cdot \omega \cdot \hat{Z} = -\omega \cdot Z'' + j \cdot \omega \cdot Z' \qquad \textbf{(Eq. 2.9)}$$

$$M' = -\omega \cdot Z'' \qquad \textbf{(Eq. 2.10)}$$

$$M'' = j \cdot \omega \cdot Z' \qquad \textbf{(Eq. 2.11)}$$

The relaxation frequency is also very often used for characterization of dielectric materials and it describes the time, which is needed to polarize a sample in the applied external field. The relaxation frequency is usually found from the maximum point of the arc in the Nyquist plot. In many cases each relaxation time (frequency) represents a certain process in a system.

For representation of the resistance Nyquist plot are best suited, while the modulus plots better represent the capacitive behaviour of a system. The frequency in a modulus or Nyquist plots are not visible, due to this Bode plots are used to represent relaxation frequencies. For the analysis of impedance spectrum all of the mentioned spectra have to be used.

In *Figure 2.3* some simple cases of impedance representations are shown, which are more detailed discussed in the theoretical consideration or experimental results part. The first case (*Figure 2.3*) shows the spectrum of a blocking capacitance, where the resistance and capacitance are connected in series. This case was observed in YSZ across-plane measurements on silicon substrate, where the silica interlayer blocked the current flow. The impedance in this case is given by:

$$\hat{Z} = R - j\frac{1}{\omega C} \qquad \textbf{(Eq. 2.12)}$$

The other case represented in *Figure 2.3* b is very common for ionic conductivity measurements in solids. Two RC elements represent two different processes, like ionic conductivity of grains and grain boundaries. The complex impedance of one RC element is given by [83]:

$$\hat{Z} = \frac{R}{1+(\omega RC)^2} - j\frac{\omega R^2 C}{1+(\omega RC)^2} \qquad \textbf{(Eq. 2.13)}$$

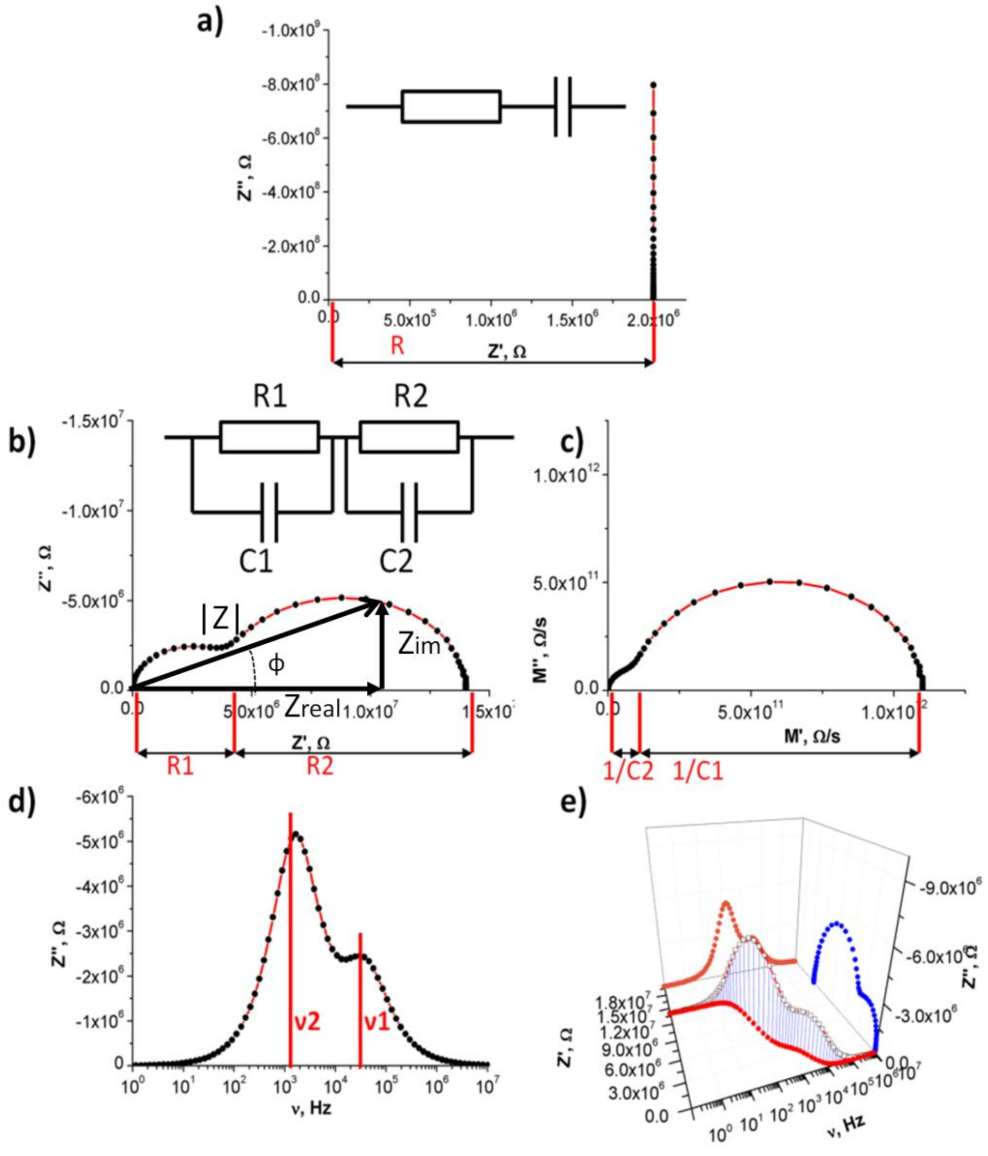

Figure 2.3. *a) Nyquist graph of a resistance and capacitance connected in series; Impedance spectra graphs: b) Nyquist graph of two RC elements connected in series (R1 = 4 MΩ, R2 = 10 MΩ); c) Modulus plot (C1 = 1 pF and C2 = 10 pF); d) Bode plot of imaginary impedance part (ν1 = 37 kHz and ν2 = 1.6 kHz); e) Impedance spectrum presentation in 3 D plot*

In most real electrochemical systems spectra cannot be fitted with such ideal capacitance elements [84]. This effect comes from the distribution of physical properties like structure resistivity or dielectric constant [85]. For a fitting such electrochemical systems in equivalent circuit usually a constant phase element (CPE) instead of a capacitance is used. The impedance of CPE is given by:

$$\hat{Z}_{CPE} = \frac{1}{Q(j\omega)^n} \qquad \textbf{(Eq.2.14)}$$

where Q and α are fitting parameters. If $n = 1$, then Q has capacitance units, in general it is $F \cdot s^{-(1-n)}$. In all equivalent circuits which were used for the analysis of experimental impedance spectra, CPE instead of an ideal capacitor was used.

2.2.2 Experimental EIS setup

The electrical properties of the samples were measured by impedance spectroscopy (Novocontrol Alpha High Performance Frequency Analyzer). The measurement temperature and frequency range depends on the study and are described in more detailed in the experimental part. All impedance measurements were performed on a micro-measurement stage (*Figure 2.4*). The measurement stage is equipped with a microscope (Mitotoyo, Japan) and a heating unit. The heating unit consists of temperature control (Eurotherm), platinum heater and K–type thermocouple, which is in contact with the sample. For contacting the microelectrodes, tungsten needles (tip diameter 1 μm) were used. For the positioning of the needles micromanipulators (Karl Suss, Germany) were employed. In order to avoid electromagnetic noise an additional Faraday cape was used. The grounded shielding grid was placed on top of the heating stage.

Fitting and simulations of the impedance spectra were accomplished with ZView software (Scribner), which is based on the equivalent circuit method.

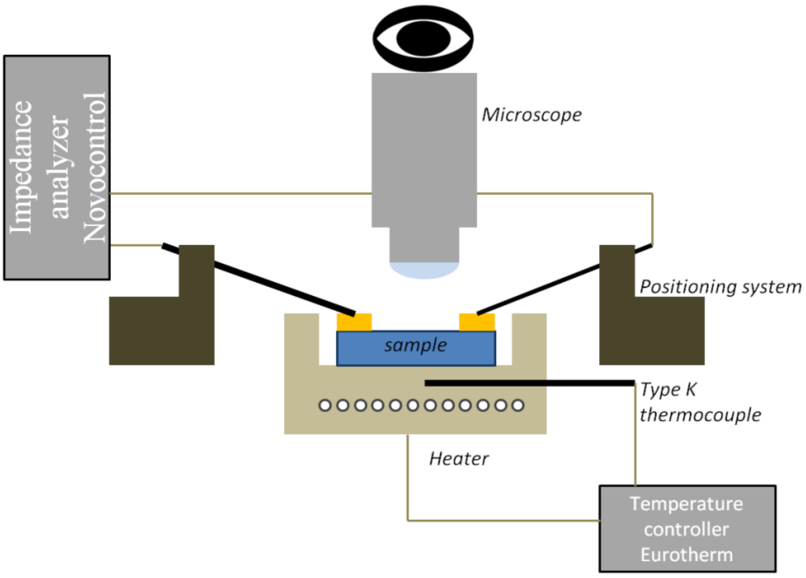

Figure 2.4. *Sketch of the micro measurement stage*

2.3 Thin film characterization methods

2.3.1 X-ray diffraction

The X-ray diffraction (XRD) is widely used for characterization of crystalline materials and it allows structure and phase identification. In crystalline materials atoms form a periodical structure within the distance of the X-ray wavelength. The waves scattered by each of the atom planes have to be in phase, so diffraction may occur only at special irradiation angles θ. The diffraction pattern allows determination of the interplanar distance, which is the core of crystallography. The distance between crystallographic planes can be determined by Bragg's law:

$$2d \sin\theta = n\lambda \qquad \textbf{(Eq. 2.15)}$$

where θ is the Bragg angle between the incident beam and the scattering planes, λ is the wavelength of the X-ray, d is the interplanar distance in a crystal, n is an integer number and describes the diffraction order.

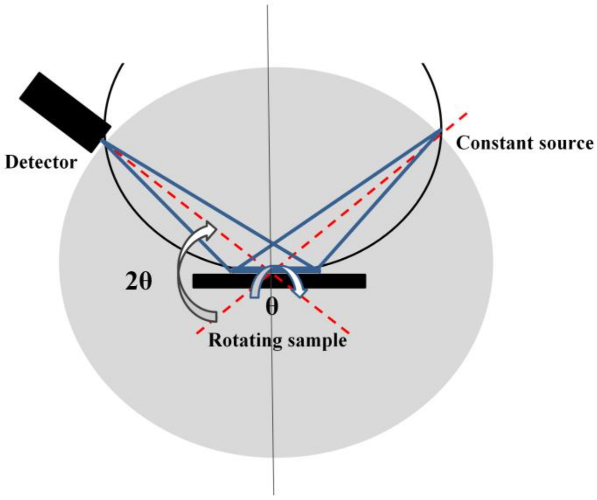

Figure 2.5. *Θ-2Θ Bragg-Brentano diffractometer [86]*

The measurements presented in the thesis were done with Θ-2Θ Bregg-Brentano diffractometers with copper K_{α} irradiation. In Θ-2Θ configuration (*Figure 2.5*) the X-ray source does not move, while the sample is rotated around its axis with the angle Θ. The detector is moving along the focusing circle with an angle 2Θ (*Figure 2.5*), this allows recording diffraction from crystallographic planes. For the XRD measurements two different laboratory diffractometers PANalytical X'Pert PRO and DRON 3.0, were used. PANalytical X'Pert PRO was employed with Soller slits of 0.04 rad, a fixed divergence slit of 0.5°, a fixed antiscatter-slit of 1°. Measuring time for all samples was 30 min. The PANalytical X'Pert PRO system was employed with X'Celerator detector with Ni K_{β} filter (scan length ca. 2.55°). Both diffractometers were equipped with a 4 axis sample holder. Most of the XRD measurements were done at X-ray Center of Vienna University of Technology.

Synchrotron measurements on selected samples were performed at Stanford Synchrotron Radiation Light Source beamline 7.2 [87]. This beamline is equipped with a 6 axis goniometer, which allows to orient the sample in a position where the scattering vector of a given crystallographic plane would be parallel to the surface normal (*Figure 2.6*). As it was mentioned above, all laboratory difractometers were equipped with a copper target, to which emitted electrons from a filament are accelerated. Electron interaction with the target leads to the emission of a discontinuous X-ray emission spectrum. Only characteristic irradiation is being used for XRD studies. In the copper case K_{α} is used with a wavelength of 1.54 Å. The way of X-ray generation in the synchrotron is different. In this case accelerated charged particles emit the electromagnetic radiation. The main advantage of a synchrotron is irradiation intensity and possibility to choose a desired wavelength. In the synchrotron XRD measurements the 14 keV ($\lambda = 0.8856$ Å) beam was used.

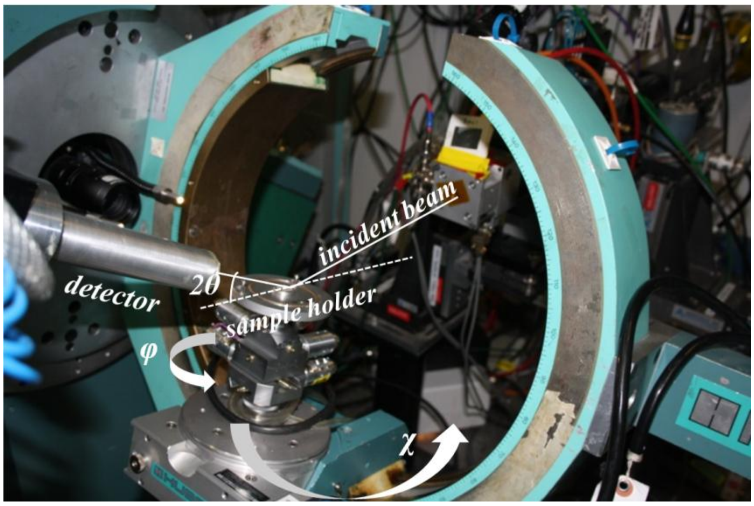

Figure 2.6. *XRD measurements with six-axis goniometer at SSRL*

All measured samples were quantitatively and qualitatively analysed. The XRD measurements were done on thin films in order to identify phase and texture of thin YSZ layers. All samples were analysed by a Rietveld method. The Rietveld refinement technique was developed for use in the characterization of crystalline materials. The X-ray diffraction of powder samples results in a pattern characterized by peaks in intensity at certain positions. The height, width and position of these peaks can be used to determine many aspects of the material's structure. Rietveld analysis is a Fundamental Parameters program for XRD, which refines lattice parameters, peak width and shape, and preferred orientation. The Rietveld method uses a least square method to refine a theoretical line profile until it matches the measured profile.

For the surface investigation X-ray Reflectometry (XRR) were used which allows to assess structural details of thin layers. XRR technique is usually used for analysing the layer thickness, surface and interface roughness and the electronic density [88]. In XRR mode the diffractometer is operated in the previously discussed $\theta/2\theta$ mode, but with lower angles, basically it is operated in parallel beam configuration. From the reflectivity curve we can find out parameters of thin layer like density, roughness and thickness. The modelled X-ray data [89, 90] of YSZ thin layers with the thicknesses of

10 and 30 nm (the beam energy is 8 keV) is plotted in *Figure 2.7*. The thickness of the material is determined from the XRR data according to Kiessig formula:

$$\theta^2 - \theta_C^2 = m^2\left(\frac{\lambda}{2\cdot t}\right)^2 \qquad \textbf{(Eq. 2.16)}$$

where θ_C – critical angle (*Figure 2.7*), t – layer thickness, m – an integer number and λ – X-ray wavelength. As one can see the frequency of fringes depends on the layer thickness. From the critical angle one can estimate the density of the layer. The slope of the curve represents the roughness of the layer. In order to define the mentioned values of YSZ layers, the X-ray reflectivity data were fitted with the software [89].

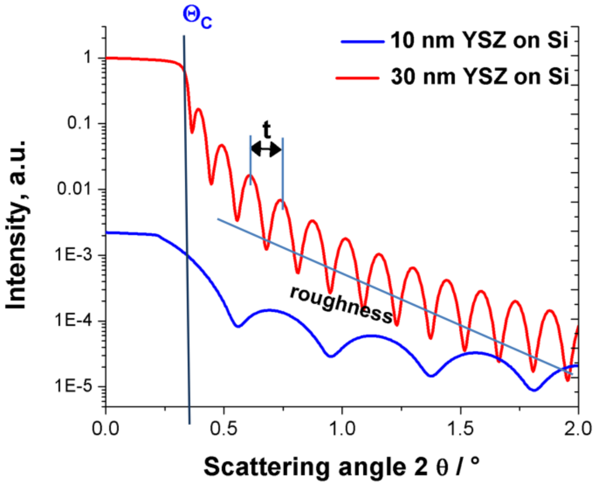

Figure 2.7. *Modeled X-ray reflectivity data of YSZ thin films (10 nm and 30 nm) on a silicon substrate (beam energy - 8keV)*

2.3.2 Atomic force microscopy

Atomic force microscopy (AFM) measures the force between the sample and a tip and allows determining the surface topography. AFM can operate in three different modes: contact, non-contact and tapping modes. The tip of the AFM cantilever is placed on the investigated surface. If the tip is placed in contact with the surface AFM measures a repulsive force, however such a mode is very sensitive to noise. Another AFM measuring mode is based on measuring van der Waals forces and a tip is in the non-contact regime with the surface. In the tapping mode the cantilever oscillates up and down near the resonant frequency. In this case the cantilever oscillation frequency is being changed due to the van der Waals or dipole-dipole interaction or electrostatic force. The AFM in a tapping mode can achieve a resolution of ~1 nm. All measurements presented in the results part were measured in tapping mode.

The AFM method is used for detection of the quantitative surface morphology. In this work atomic force microscope NanoScope V (Bruker Nano) with silicon cantilever and integrated silicon tips (Arrow NC cantilevers, Nano World, Switzerland, resonant frequency 285 kHz) was used to determine the width of grains. All the measurements were done with a scanning rate of 2 Hz. The maximum scanned area of the samples was 1x1 µm.

2.3.3 Scanning electron microscopy

Scanning electron microscope (SEM) was used to detect surface features of thin films (structure, agglomerates etc.) and thickness of layers. SEM method is widely used for thin film characterization. The SEM uses a focused electron beam which hits the investigated surface. A signal which comes from electron-sample interaction reveals information about the sample, like surface topography or chemical composition. The electrons interact elastically or inelastically with atoms of a sample. Inelastic electron collisions with the atoms produce backscattered electrons (BSE), secondary electrons (SE) or photons. During interaction with atoms the electrons lose some energy and certain type of electrons might be generated from a special depth.

In this thesis SEM was mostly used for the layer thickness determination. For cross-section measurement the samples were cut into two pieces by a diamond cutter. YSZ layers formed on silicon and alumina substrates, due to the poor electronic conductivity, tend to charge. The charging effect was partially overcome by covering the sample with a platinum thin layer, but microstructure determination from cross-section was indeed not possible. The SEM images presented in the results part were obtained by SEM microscope - FEI FEMTA 200F.

2.3.4 Rutherford back scattering spectroscopy

Rutherford backscattering spectroscopy (RBS) is used for surface analysis of solids. RBS technique allows determining the elemental composition or depth profile of individual elements. The physics of this analytical technique is based on elastic ion scattering. The energy of the incident ion beam varies from 500 eV to 4 MeV. The energy of backscattered ions is recorded by a solid state detector. The analysed depth of RBS is usually up to 2 µm and it strongly depends on the sample elemental composition, incident ion beam energy and ion mass.

The Rutherford cross-section for backscattering ions is given by [91]:

$$\sigma_R = 5.1837436 \cdot 10^6 (\frac{Z_1 Z_2}{E})^2 \frac{\{(M_2^2 - M_1^2 \cdot \sin^2 \Theta)^{1/2} + M_2 \cos\theta\}^2}{M_2 \sin^4\theta (M_2^2 - M_1^2 \sin^2\theta)^{1/2}} \qquad \textbf{(Eq. 2.17)}$$

where Z and M are nuclear charge and mass of atoms or incident ions, E – incident ion energy. The RBS method is very sensitive for heavy elements. As incident ions usually ^{4}He or protons are used. The RBS analysis was performed with the PSI/ETH Tandem accelerator. The thickness and chemical layer composition was measured at an energy of 5 MeV ^{4}He. The analysis was performed under standard conditions [92]. The measured spectra were fitted by the RBS spectra simulator RUMP.

2.3.5 Ellipsometry

Ellipsometry is an optical non-destructive method, which allows determination of refractive index and layer thickness. The layer thickness was determined by subsequent ellipsometry measurements on transparent YSZ layers, which were formed on silicon substrates. The ellipsometry measurements are based on incoming light polarization at a dielectric interface or the shift of the incoming light phase. The shift of the phase depends on the materials refractive index. The ellipsometry is used to measure layers as thin as 1 nm [93]. Here the ellipsometry measurements on thin films were done with an ellipsometer Santech SE 850 ADV, which is equipped with a red laser.

2.3.6 Raman spectroscopy

Raman spectroscopy is one of the vibrational spectroscopy methods and it relies on inelastic scattering of monochromatic light. Raman scattering can occur due to the change in vibrational, rotational or electronic energy of a molecule. Crystal lattice vibrations of solids are also Raman-active and very useful for solid material phase determination. Raman spectroscopy is also used for strain estimation in thin films. The Raman spectroscopy measurements were done with a Raman spectroscope (Renishaw 2000), which was employed with a green laser (514 nm).

2.3.7 UV lithography

The conductivity measurements in most experimental studies of this thesis were done using microelectrodes. Micro-patterned electrodes are widely used in electronics, but only recently they were applied in the field of solid state ionics [94-96]. It is discussed below that microelectrodes allow investigating properties which are not detectable with common electrodes.

Microelectrodes were prepared by the UV lithography method. Before micro-patterning the samples were cleaned in an ultrasonic bath with acetone and alcohol, which helps to avoid any residues on the surface and improves the quality of the electrodes. Afterwards samples were dried in nitrogen flux. The prepared samples were covered with a positive photoresist (N-1430, Micro Resist technology) by spin-coating (spin coater SCC-200, KLM, Germany). The rotational speed was 2700 r/min and the duration of a spinning procedure was 60 seconds. The photoresist was dried on a heating stage for 120 seconds at 100 °C. The sample with prepared photoresist was positioned beneath a photo mask and exposed to UV light for 40 seconds. After exposition, the pattern was developed in a photographic developer (MircoResist Technology), where the positive photoresist is soluble.

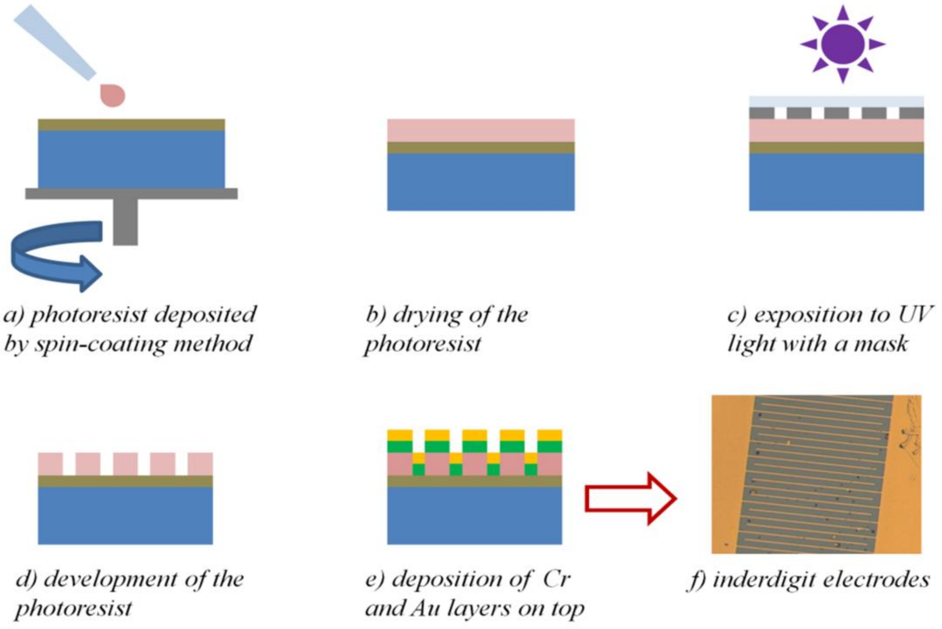

Figure 2.8. *The preparation procedure of microelectrodes*

After the development of the photoresist a gold layer was prepared by magnetron sputtering. Magnetron sputtering was done with a MED 020 sputtering system (BalTec, Germany). Firstly an adhesive layer of chromium (20 nm) was deposited. The chromium cathode was cleaned in an argon plasma for 30 s (I = 100 mA, p_{Ar} = 0.9 mPa) to remove the oxide layer. Thin adhesive layers were deposited with the following parameters – I = 100 mA, p_{Ar} = 0.9 mPa, t = 40 s. Afterwards a gold layer of 200 nm was deposited on top (I = 100 mA, p_{Ar} = 0.27 mPa, t = 400 s). The gold electrodes were developed in acetone with ultrasonic bath (lift-off procedure). The whole UV lithography procedure is shown in *Figure 2.8*. For the conductivity measurements different geometries of the electrodes were used. Across-plane conductivity was measured with circular electrodes (*Figure 2.9 a*), while for the in-plane conductivity interdigit (*Figure 2.9 b*) and stripe (*Figure 2.9 c*) electrodes were used. The dimensions of the electrodes were different and are described in the results part.

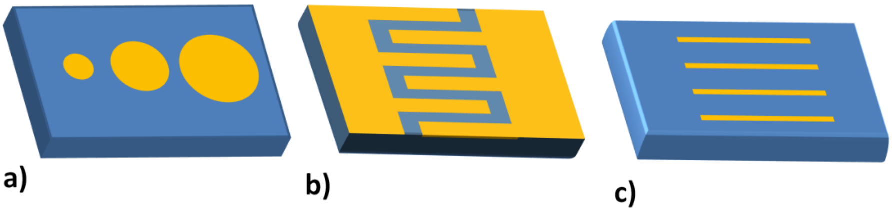

Figure 2.9. *The geometries of the electrodes: a) circular, b) interdigital ("comb shape") and c) stripe electrodes*

3 THEORETICAL CONSIDERATIONS AND SIMULATIONS

This chapter consists of four parts – first an introduction to the physics of a model for impedance simulation, than three parts dealing with special problems like grain and grain boundary separation in impedance spectra in thin thin film case, across-plane impedance measurements of YSZ thin films on silicon and in- and across-plane analysis in a single measurement. The modelled impedance spectra were analysed by fitting with an equivalent circuit.

3.1 Modeling of impedance spectra using finite element theory

Modelling of impedance spectra by the finite element method allows prediction of the current path in a sample, shape of impedance spectra or the definition of capacitances and resistances of ideal systems. The simulations of impedance spectra were done using the finite element modelling (FEM) software “Comsol Multiphysics” (Inc. COMSOL, Sweden) with the frequency domain (time harmonic) solver. Simulations of impedance spectra are based on classical electrodynamics. We begin with the numerical solution of Poisson’s equation (*Eq. 3.1*), which allows determining potential distribution and impedance of a system:

$$div(grad\varphi) = -\frac{1}{\varepsilon} \cdot \rho(r) \qquad \textbf{(Eq. 3.1)}$$

where φ represents the scalar electric potential, ε – dielectric permittivity of the sample and ρ is the total charge density. In the two-dimensional case without a space charge, equation (*Eq. 3.1*) can be simplified to:

$$\frac{\partial^2\varphi}{\partial x^2} + \frac{\partial^2\varphi}{\partial y^2} = 0 \qquad \textbf{(Eq.3.2)}$$

From Ohm’s law the Faradaic (free) current density is determined by:

$$\mathbf{j} = \sigma\mathbf{E} \qquad \textbf{(Eq. 3.3)}$$

where $\boldsymbol{E}$ is an electric field, which is given by:

$$\mathbf{E} = \text{-}grad\varphi \qquad \textbf{(Eq.3.4)}$$

Symbol σ denotes the conductivity. The current flowing through a cross-section of area A is given by:

$$J = \int_A \mathbf{j}\, d\mathbf{s} \qquad \textbf{(Eq.3.5)}$$

When also including time dependent displacement current, the complex total current $\hat{\mathrm{J}}$ can be expressed as an integral of the complex current density through the equipotential surface A:

$$\hat{J} = \text{-}\int_A \hat{k} \cdot grad\hat{\varphi}\, d\mathbf{s} \qquad \textbf{(Eq. 3.6)}$$

where $\hat{\varphi}$ is the complex potential distribution in a sample and $\hat{k}$ is the complex conductivity. The latter includes free and displacement current and is given by:

$$\hat{k} = \sigma + i\varepsilon\omega \qquad \textbf{(Eq. 3.7)}$$

In order to find out the impedance of a system the problems were solved by a frequency domain study in Comsol. The frequency domain study generates a solver sequence that is used to solve a stationary parametric problem and the equations are time dependent. The dynamic formulations of conduction currents and displacement currents are used:

$$\nabla\mathbf{J} = \nabla(\sigma \cdot \boldsymbol{E} + \boldsymbol{J}^e) = -\mathrm{j}\omega\rho \qquad \textbf{(Eq. 3.8)}$$

where J^e – displacement current. Considering that:

$$\boldsymbol{D} = \varepsilon_0\boldsymbol{E} + \boldsymbol{P} \qquad \textbf{(Eq. 3.9)}$$

$$\nabla\boldsymbol{D} = \rho \qquad \textbf{(Eq. 3.10)}$$

$$\boldsymbol{E} = -\nabla\varphi \qquad \textbf{(Eq. 3.11)}$$

The dynamic formulation of conduction currents is

$$\nabla\boldsymbol{J} = \nabla(\sigma \cdot \boldsymbol{E} + \boldsymbol{J}^e) = -\frac{\partial\rho}{\partial t} \qquad \textbf{(Eq. 3.12)}$$

In generalized form, considering (*Eq. 3.9*), (*Eq. 3.10*) and (*Eq. 3.11*) the equation becomes:

$$-\nabla \frac{\partial}{\partial t}(\varepsilon_0 \nabla\varphi + \boldsymbol{P}) - \nabla(\sigma\nabla\varphi - \boldsymbol{J}^e) = 0 \qquad \textbf{(Eq. 3.13)}$$

where $\boldsymbol{P}$ – electric polarization.

The last equation (*Eq. 3.13)* is used in the time harmonic equation. Once the potential distribution in a sample is known the admittance/impedance of a system can be calculated. The total admittance of a system is equal to the ratio of current density and voltage:

$$\hat{Y} = \frac{-\int_A \hat{k}\cdot grad\hat{\varphi}\, d\mathbf{s}}{U} \qquad \textbf{(Eq.3.14)}$$

The whole impedance/admittance spectrum was calculated by varying frequency *ω*, as the potential distribution in a system is known. The current density was determined from the integral through an equipotential surface. All models were 2 D and integration was done along the electrode/electrolyte boundary. The total current density consists of free current and displacement current, so the simulated admittance consists of a real part and imaginary part, which is a consequence of the polarization of the dielectric:

$$\hat{Y} = Y' + iY'' \qquad \textbf{(Eq.3.15)}$$

The impedance is vice versa proportional to the admittance and is given by:

$$\hat{Z} = \frac{1}{Y'+iY''} = \frac{Y'}{Y'^2+Y''^2} + \frac{iY''}{Y'^2+Y''^2} \qquad \textbf{(Eq.3.16)}$$

The real and imaginary impedance values were calculated from (*Eq.3.16*) for the given frequencies.

3.2 The effect of micron-sized electrode geometry

The FEM method was applied to simulate the effect of a changing current distribution in thin films in the microcontacting case. All the experimental and simulation studies discussed in the thesis are dealing with microelectrodes application to thin films. It has been shown in previous studies [97, 98] that microcontacting leads to a non-uniform distribution of the current in a sample, which may cause errors in the analysis of data. In a simple case with two parallel electrodes the conductivity of a system can be defined by:

$$\sigma = \frac{l}{A \cdot R} \qquad \textbf{(Eq.3.17)}$$

where l – denotes the distance between the electrodes and A is the area of the electrodes. (*Eq.3.17*) can be applied for parallel and congruent electrodes. If the electrodes are not parallel, or differ from each other geometrically, this leads to a nonuniform electrical potential distribution in a sample and requires geometrical correction factors in (*Eq.3.17*). The half infinite circular microelectrode case was investigated in ref. [97-100] and a formula for the conductivity was derived by Newman [97]:

$$\sigma = \frac{1}{4 \cdot R \cdot r} \qquad \textbf{(Eq.3.18)}$$

where r – electrode radius.

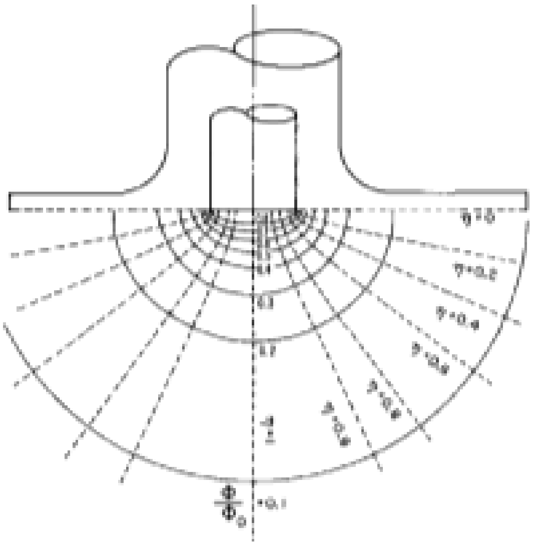

Figure 3.1. *Equipotential surfaces in the medium near the disk [97]*

With the help of the finite element method the effect of the electrode geometry will be analyzed for the across-plane thin film case. The finite element calculations considered a homogeneous electrolyte with two parallel electrodes (*Figure 3.2*). The resistance of the electrolyte is relatively high in comparison with the electrode and electrodes were considered in terms of a first type boundary condition. Resistances of electrochemical reactions were also not considered in the model. One of the electrodes was set as high potential electrode (1 V) and the other as ground (0 V). The width and thickness of the electrolyte were 50 μm and 1 μm respectively. Conductivity and relative dielectric permittivity were set to $2\cdot10^{-4}$ S/cm and 27 (experimental values for YSZ), respectively. The width of the counter electrode (*w1*) was the same as the width of the electrolyte and was kept constant. The width of the working electrode (*w*) was varied from 100 nm to 50 μm. Although the numerical simulations are 2D, for conductivity calculations it was considered that the length of the electrodes was 1 cm. The meshing parameters of a system: maximum meshing element - 10^{-6} m, minimum element - 10^{-8} m. In order to minimize computational errors, the boundary of the electrode was meshed additionally (*Figure 3.2*) with a meshing increment parameter of 1.1 and with 30 elements as it is shown in *Figure 3.2*.

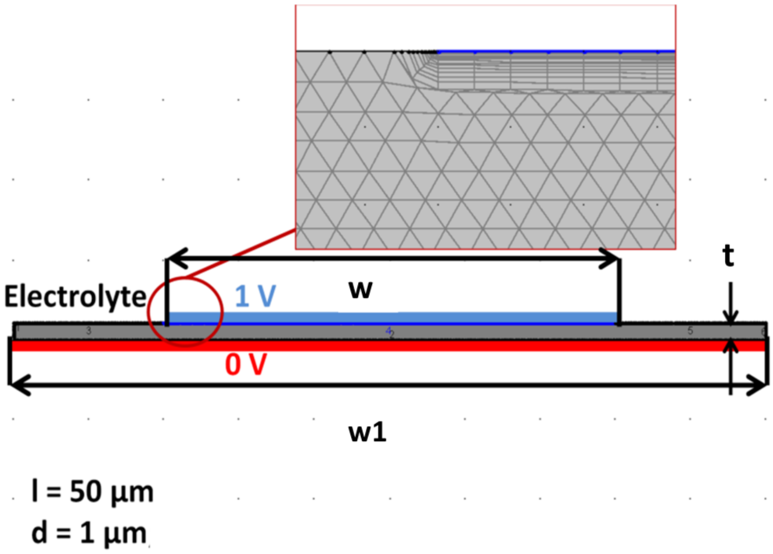

Figure 3.2. *Homogeneous solid electrolyte (thickness t) with parallel and incongruent electrode geometry*

Numerical simulation results are compared with the results obtained from (*Eq.3.17*) and plotted in *Figure 3.3*. The variable width of the working electrode was normalized to a thickness of electrolyte – t/w, which reveals much better the effect of the microelectrode geometry.

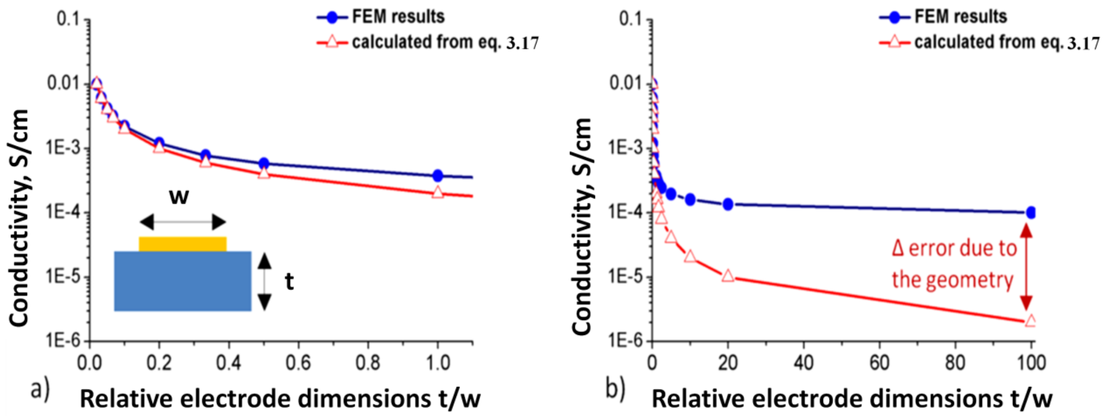

Figure 3.3. *Electrode geometry effect for conductivity values*

It is obviously seen from *Figure 3.3* that with electrode length, t/w < 1, conductivity results match very well, i.e. a geometrical correction factor is not needed. If the width of the electrode is comparable with the layer thickness (t) or smaller ($w \leq t$), then an additional geometry factor has to be included in (*Eq.3.17)* due to the non-uniform potential distribution. We may conclude that in nanolayer studies, where the electrode geometry is usually in the µm range, the geometry effect can be neglected and (*Eq.3.17)* can be applied.

3.3 Separation of grain and grain boundaries in impedance spectra

In the first section, the grain and grain boundary separation problem in impedance spectroscopy has been discussed. There is plenty of literature dealing with the ionic conductivity of grain and grain boundaries in YSZ pellets. In impedance spectra measured on pellets grain and grain boundary contributions are well separable. This type of measurement usually leads to two or three semicircles in a Nyquist plots (the third one, the low frequency semicircle, comes from the electrode effect, which will not be considered in our model). The high frequency semicircle is attributed to the bulk contribution, which is followed by a second arc – the grain boundary contribution. According to a brick model such type of impedance spectrum is fitted with an equivalent circuit consisting of two RC elements connected in series. The separation of grain and grain boundary contributions in this case is trivial. However, in the thin film case due to the substrate capacitance usually only one semicircle is detectable [101-103]. The resistance of this arc is a combination of grain and grain boundary contributions. In the following part the main difference between these two measurements and sample geometries will be demonstrated and it is shown how the separation of grain and grain boundaries can be improved in impedance measurements on thin films. The impedance spectra will be simulated using two methods: equivalent circuit model (ZView software) and numerical simulations (COMSOL). In order to further analyze the numerical simulation results, the simulated spectra were fitted by an equivalent circuit model.

The difference between the measurements of pellets and thin films is firstly demonstrated by an equivalent circuit model. According to a brick model the equivalent circuit for a polycrystalline sample consists of two RC elements which are connected in series (*Figure 3.4* c). The values of equivalent circuit elements, i.e. C_{gb}, C_{bulk}, R_{gb}, R_{bulk} were estimated from the following considerations. One of these RC elements represents resistance and capacitance of the YSZ bulk and is given by:

$$C_{bulk} = \frac{\varepsilon_{bulk} \cdot A}{D} \qquad \textbf{(Eq. 3.19)}$$

And

$$R_{bulk} = \frac{D}{A \cdot \sigma_{bulk}} \qquad \textbf{(Eq. 3.20)}$$

where D – distance between the electrodes, A – area of the electrodes, σ_{bulk} - the conductivity of grain bulk and ε_{bulk} – bulk permittivity. The conductivity of YSZ bulk was taken from [104] -σ_{bulk} = $1 \cdot 10^{-4}$ S/cm at 300 °C. The bulk permittivity of YSZ (value $27 \cdot \varepsilon_0$) was used. The sample geometry used for calculations on pellets was as follows: D = 1 cm, A = 1 cm^2.

The other RC element in the equivalent circuit represents resistance and capacitance of grain boundaries. The conductivity value of grain boundaries of YSZ was as well taken from ref. [104] (σ_{gb} = $1 \cdot 10^{-7}$ S/cm at 300 °C). The resistance and capacitance of grain boundaries were evaluated from the following equations:

$$C_{gb} = \frac{\varepsilon_{gb} \cdot A}{D} \cdot \frac{d_g}{d_{gb}} \qquad \textbf{(Eq. 3.21)}$$

$$R_{gb} = \frac{D}{A \cdot \sigma_{bulk}} \cdot \frac{d_{gb}}{d_g} \qquad \textbf{(Eq. 3.22)}$$

where d_{gb} – grain boundary thickness, which is about 1 nm for YSZ [104] and d_g – grain size - 100 nm was used in the model. The model sketch, equivalent circuit and simulated spectra for a YSZ pellet (bulk) sample and $\varepsilon_{bulk} = \varepsilon_{gb}$ are shown in *Figure 3.4*. As it was mentioned before, impedance spectra contain two semicircles (*Figure 3.4 f*).

Impedance simulations with an equivalent circuit model were also done for the thin films case. Simulations were performed assuming two parallel electrodes on a YSZ layer (*Figure 3.4 b*). In this case the area A in (*Eq. 3.19*) to (*Eq. 3.22*) is given by electrode length l and thin films thickness t. The width and length of the electrodes were 100 μm and 1 cm respectively. The distance between the electrodes used in the model was 1 cm. The layer thickness was 100 nm. For such in-plane measurements YSZ thin layers are formed on a highly resistive substrate, therefore the DC current flows only in the layer. In this case the substrate capacitance comes into play and has a crucial role for the impedance spectra. Usually the substrate (stray) capacitance is much larger than the capacitance of the YSZ bulk or grain boundaries and this hinders the possibility to separate grain and grain boundary contributions in the impedance spectrum.

This is illustrated by impedance spectra simulated with two RC elements representing YSZ bulk and grain boundary contributions and with an additional stray capacitance which was added in parallel (*Figure 3.4 d*). The stray capacitance represents displacement current flow through the substrate and has to be always included in the equivalent circuit in the thin films case. Other possible stray capacitances, like capacitance between contact needles might be very small and will not be considered in the model. The stray capacitance was estimated from the equation:

$$C_{stray} = \frac{\varepsilon_{substrate} \cdot \omega \cdot l}{D} \cdot \beta \qquad \textbf{(Eq. 3.23)}$$

where β – geometrical factor, which takes the in-plane electrode arrangement into consideration and depends only on electrodes length and width (w/l) and $\varepsilon_{substrate}$ – dielectric permittivity of the substrate. An alumina substrate was used in the model ($\varepsilon_{Al2O3} = 10 \cdot \varepsilon_0$). Since the capacitance of YSZ bulk is much smaller than the stray capacitance this allows simplifying the equivalent circuit and neglecting the capacitance of the YSZ bulk. The equivalent circuit shown in *Figure 3.4 e* will be used for impedance spectra simulation and in further impedance spectrum analysis.

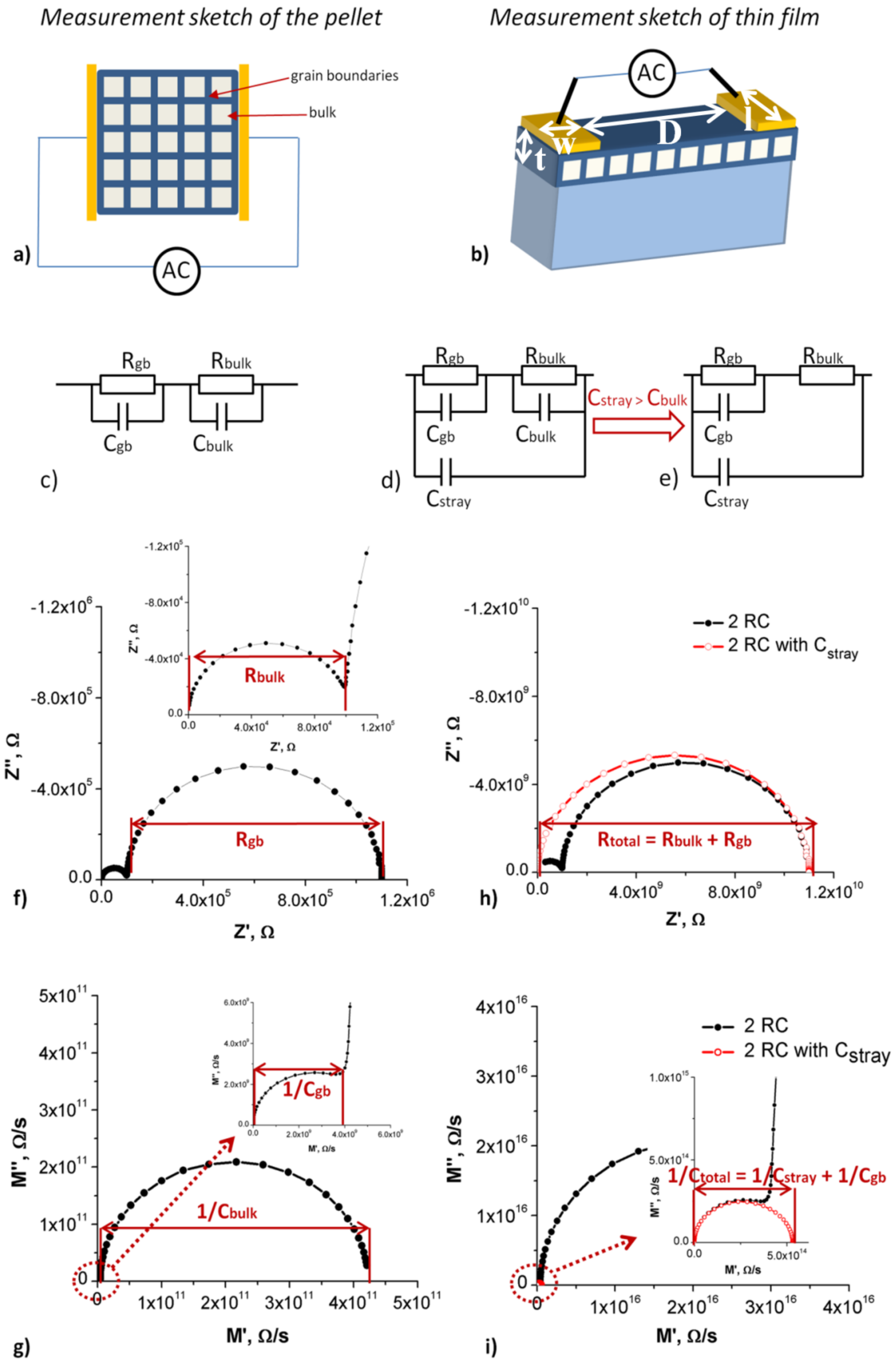

Figure 3.4. *Impedance measurement sketch on pellet and thin film (electrode width - 100* μm *and distance between the electrodes -1 cm) (a and b); Equivalent circuits used for simulation (c and e); Nyquist and modulus plots of pellet measurement (f and g); Nyquist and modulus plots of thin film measurement (h and i)*

Simulated impedance plots of thin layers with the above mentioned parameters are shown in *Figure 3.4 h)* and *i)*. As one can see the stray capacitance of the substrate makes a separation of grain and grain boundaries impossible. Improvements of the measurement geometry could lead to a lower stray capacitance and better grain and grain boundaries separability. In order to demonstrate the effect of the measurement geometry, simple calculations were done with varied distance between the electrodes and different electrode width. The values of bulk and grain boundaries capacitance were calculated according to (*Eq. 3.19)*, (*Eq. 3.21)* and (*Eq. 3.23)* and are listed in *Table 3.1*. The stray capacitance was calculated by numerical simulations, considering two parallel electrodes on a thick (500 μm) alumina substrate. The determined values of the stray capacitance are also listed in *Table 3.1*. The capacitance results demonstrate that lowering the electrode width could minimize the stray capacitance.

Table 3.1. *The values of YSZ bulk, grain boundaries and stray capacitance with varied electrode width (D = 100 μm, layer thickness t = 100 nm). Stray capacitance values were numerically simulated on an alumina substrate ($\varepsilon_{substrate} = 10 \cdot \varepsilon_0$)*

Electrode width w, μm	C_{bulk}, pF	C_{gb}, pF	C_{stray}, pF
500	$2.39 \cdot 10^{-15}$	$2.39 \cdot 10^{-13}$	$9.67 \cdot 10^{-11}$
100			$8.96 \cdot 10^{-11}$
10			$3.86 \cdot 10^{-11}$
1			$2.39 \cdot 10^{-11}$

Impedance spectra simulations with the equivalent circuit model demonstrate the system behavior in the ideal case. For further electrode geometry effect analysis numerical simulations were used. For the modelling of impedance spectra the electrode arrangement is shown in *Figure 3.5*, as a side view of a modeled structure, which consists of three subdomains: alumina substrate, a YSZ layer with the thickness *t* and a single grain boundary in the layer. The system consists of three subdomains: thin YSZ layer, grain boundaries in the layer and alumina substrate. The grain boundaries contribution was thus evaluated by involving an effective single grain boundary in the layer. The width of this effective single grain boundary was calculated from the distance between the electrodes, grain size (d_g = 30 nm) and grain boundary thickness. The dielectric permittivity of YSZ was taken from ref. [104-106]. The permittivity of grain boundaries is assumed to be the same as in the YSZ bulk, since it was demonstrated that irrespective of different yttrium concentrations at grain boundaries, the dielectric constant is the same [105]. The permittivity values are listed in *Table 3.2*. The conductivities of YSZ bulk and grain boundary subdomains were taken from ref. [6] at 250 °C.

Table 3.2. *Physical characteristics of materials used in the model*

Material	***Relative dielectric permittivity***	***Conductivity, S/cm***
YSZ bulk	27 [104-106]	$2 \cdot 10^{-6}$ [6]
YSZ gb	27 [104, 105]	$8 \cdot 10^{-8}$ [6]
Al_2O_3	10 [107, 108]	$2 \cdot 10^{-12}$ [108]

The meshing parameters of the system: maximum meshing element - 10^{-6} m, minimum element - 10^{-8} m. The boundary of the electrode on top of the sample was meshed additionally to minimize calculation errors. The effect of the surrounding atmosphere was neglected. Any resistive effect of the electrodes was not taken into account due to the high electrode conductivity and neglecting the resistance of the electrochemical reactions. One electrode was placed on the YSZ layer and the potential was set to 1 V, while the ground electrode (0 V) was placed on the cross-section of the sample (symmetry considerations). The simulations were carried out with the following geometrical parameters: the width of a sample - 50 μm, thickness of YSZ layer – 200 nm and thickness of alumina substrate - 30 μm. The frequency domain solver was used for simulation of impedance spectra.

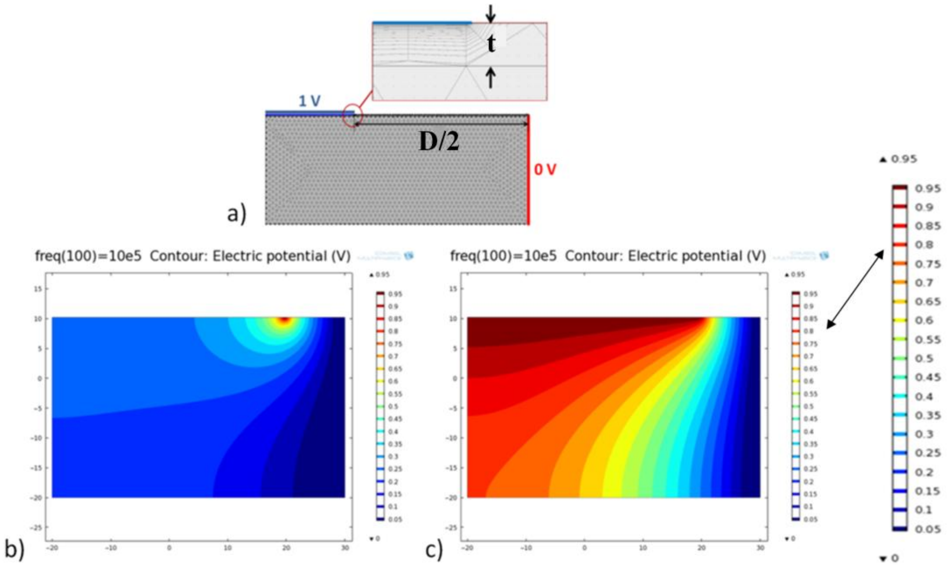

Figure 3.5. *a) Side view of a modeled structure, which consists of three subdomains: alumina substrate, a YSZ thin layer with the thickness t and a single grain boundary in the layer. For symmetry reasons only one half of the sample has to be considered; b) and c) simulated electrical potential distribution in a sample with different electrode width: b) w – 1µm and c) w – 20 µm (ν = 1 MHz)*

The role of the electrode geometry on the shape of impedance spectra was assessed by varying the width of the working electrode from 0.5 µm to 20 µm, while the distance in between the electrodes was constant (*D/2* = 20 µm). In *Figure 3.5 b)* and *c)* the effect of the width of the electrode for the potential distribution in a sample is demonstrated at 1 MHz, where colors present the absolute values of electric potential. The numerically simulated impedance spectra (Nyquist and modulus) with varied width of the electrode are shown in *Figure 3.6*. From the Nyquist graph it becomes obvious that the total resistance of the sample is constant and independent of the electrode geometry. The capacitance of the system varies in accordance with the electrode width, which clearly demonstrates the effect of the stray capacitance. One should note, that with the thinner electrodes (5 µm and 0.5 µm) Nyquist and modulus graphs look asymmetric. In this case the contributions of grain and grain boundaries are separable. This is even more pronounced in the modulus plot (*Figure 3.6 b*). When increasing the electrode width to 40 µm the second arc becomes much less pronounced in the spectrum.

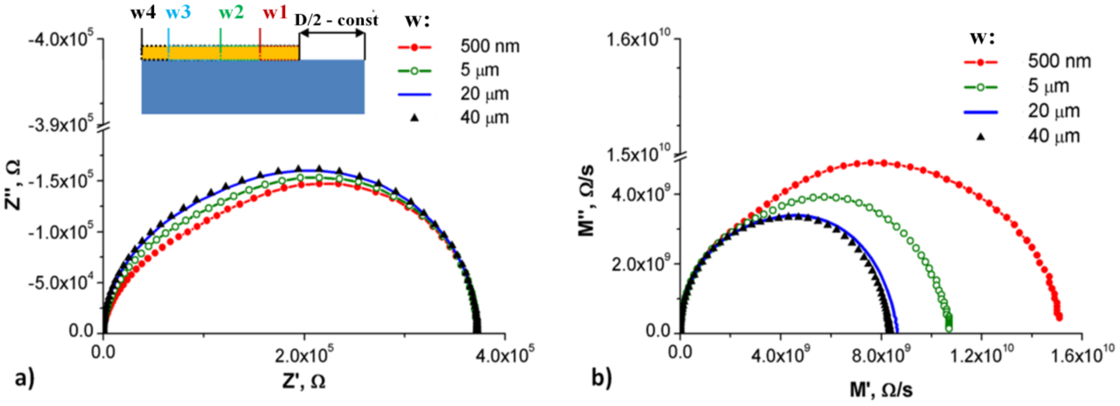

Figure 3.6. *Nyquist (a) and modulus (b) plots of simulated impedance with varied electrode width*

Numerically simulated spectra were fitted with the equivalent circuit shown in *Figure 3.4 e*. Fitting results are listed in *Table 3.3*. In order to verify fitting results all parameters of the equivalent circuit were calculated according to (*Eq. 3.19*), (*Eq. 3.20)* and (*Eq. 3.23*). All theoretical results are also listed in *Table 3.3* (green cells). One should note, that variation of the electrode width, while the distance in between the electrode is constant, should affect only the stray capacitance. The R_{gb} and R_{bulk} values listed in *Table 3.3* also vary with the variation of the electrode width. The best accordance between the theoretical values and fitted values are found with the narrowest electrodes. The increasing of the width leads to a considerable deviation of the fitting value from the theoretical one, since the grain and grain boundary contributions become less separable in the impedance spectra.

Table 3.3. *Fitting results of numerically simulated impedance spectra with an equivalent circuit (Figure 3.4 e). The parameters are compared with theoretically estimated C_{gb}, R_{gb}, C_{stray} and R_{bulk} values*

Width of the electrode	C_{gb}, pF	R_{gb}, Ω	R_{bulk}, Ω	C_{stray}, pF
500 nm	$2.17\cdot10^{-10}$	$1.41\cdot10^{5}$	$2.34\cdot10^{5}$	$7.50\cdot10^{-11}$
5 µm	$2.93\cdot10^{-10}$	$1.89\cdot10^{5}$	$1.84\cdot10^{5}$	$9.85\cdot10^{-11}$
20 µm	$3.79\cdot10^{-10}$	$2.31\cdot10^{5}$	$1.42\cdot10^{5}$	$1.19\cdot10^{-10}$
40 µm	$4.20\cdot10^{-10}$	$2.41\cdot10^{5}$	$1.31\cdot10^{5}$	$1.23\cdot10^{-10}$
Analytically calculated parameters	$2.39\cdot10^{-10}$	$1.56\cdot10^{5}$	$2.44\cdot10^{5}$	

A similar effect was also observed for varied distance in between the electrodes. The numerically simulated impedance plots are shown in *Figure 3.7*. The increase of the distance not only increases the total resistance but also affects the shape of the impedance spectrum. Measurements with the smallest distance in between the electrodes lead to two semicircles in a Nyquist plot, while with the 5 and 30 µm distance only one semicircle is observed.

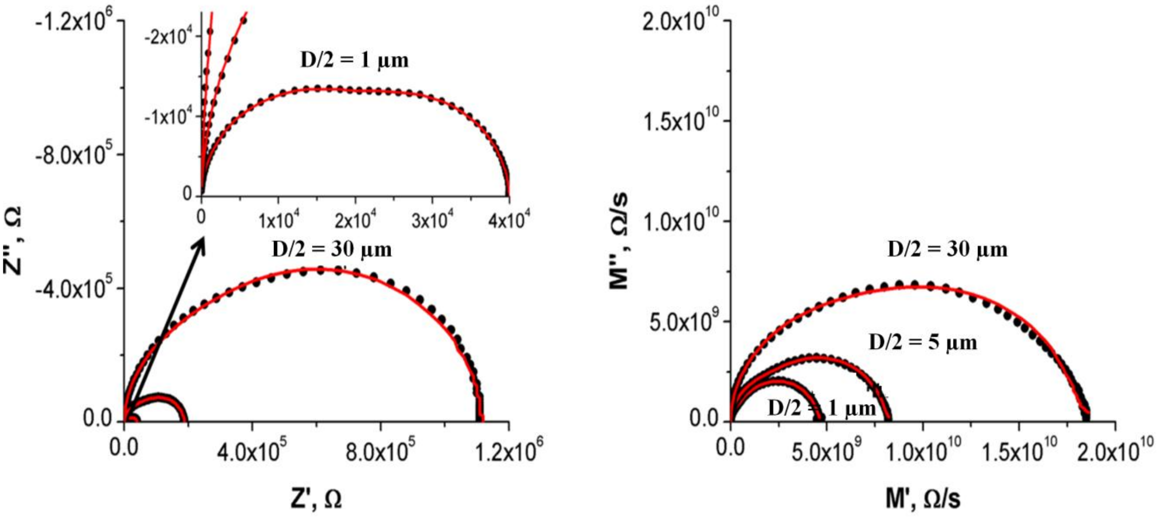

Figure 3.7. *The numerically simulated (black circle) Nyquist and modulus plots with varied distances in between the electrodes. Simulated spectra were fitted with the above suggested equivalent circuit (e). The width of the electrodes was constant (at 1 µm), while the distance (D/2) was varied from 1 µm to 30 µm*

All numerical and equivalent circuit impedance spectra simulations discussed in this chapter let us conclude that grain and grain boundary contributions in impedance spectra are separable with an improved geometry of the electrodes. Narrow and closed spaced electrodes would allow to probe grain and grain boundary conductivities in impedance spectra.

3.4 Across-plane measurements of YSZ thin films on silicon substrates

The FEM studies were applied to find out the effect of a highly resistive interlayer for impedance measurements of YSZ thin films on silicon substrate. There are a number of papers which are dealing with YSZ as high-k material in transistors or in other silicon based technologies like microelectromechanical systems (MEMS). In this model it will be demonstrated that a highly resistive dieletric interlayer might be very useful for fundamental investigation of ionic conductivity in YSZ layers. Firstly it is important to understand the effect of a dielectric interlayer for the shape of impedance spectra.

Interpretation of the impedance measurements on YSZ/SiO_x/Si structure is sophisticated and requires a priori understanding of the processes. The impedance spectra were simulated with a 2D model, which consists of a YSZ thin layer formed on a silicon substrate. Previous TEM studies on YSZ/Si had demonstrated that for typical thin layer synthesis parameters usually a silica native layer is formed. Also the subdomain of silicon with an appropriate physical characteristic was included in the model. Polarization effects of the electrodes were neglected and electrochemical reactions are not considered in the model. The potential of the electrodes was the same as of the adjacent electrolyte (first boundary condition). Likewise the effect of the sample surrounding was not considered and displacement current passing through the free surface was neglected in the model (second boundary condition). For the simulation two parallel and geometrically equal electrodes were used. The potential of 1 V was applied to the upper electrode, while the bottom electrode was set as a ground electrode. The impedance was calculated for frequencies ranging from 1 Hz to 1 MHz. The sketch of the sample, which consists of three subdomains (YSZ layer, SiOx interlayer and Si substrate) is shown in *Figure 3.8 a*. Physical characteristics of the subdomains, which are needed for calculations (dielectric permittivity and conductivity) are listed in *Table 3.4*. The subdomains were meshed with a triangular mesh. The maximum meshing element was 10^{-6} m and minimum element - 10^{-8} m. The smallest subdomain (5 nm SiOx layer) of the model included at least two mesh elements per length. The electrode/electrolyte boundary was additionally meshed to minimize calculation errors.

Table 3.4. *Physical parameters of materials used in the model*

Material	*Relative dielectric permittivity*	*Conductivity, S/cm*
YSZ	*27*	$2\cdot10^{-6}$
SiOx	*4*	$2\cdot10^{-12}$
Si	*11.5*	*30*

The width and thickness of the silicon substrate were 10 μm and 2 μm respectively. Silica is highly resistive and may strongly block the DC current flow, so in order to check the effect of the silica interlayer for impedance spectra, the thickness of YSZ and silica layers were varied from 5 to 20 nm and from 5 to 500 nm, respectively.

YSZ layers are usually polycrystalline, but to make the simulations less complex the grain boundary contribution was not included in the model.

Numerical simulation results were further analyzed by fitting with an equivalent circuit model. The model consists of two RC elements. One of them represents the YSZ resistance and capacitance. In series to the YSZ RC element a silica RC element is connected. Although silica is highly resistive, it is not completely blocking and a finite resistivity part also has to be included. Since the silicon substrate has only moderate conductivity, the subdomain of it was included and it may affect impedance measurements at high frequencies. A resistive element corresponding to silicon was therefore included in series in the equivalent circuit model. Numerical simulation results were interpreted by fitting with the suggested equivalent circuit (*Figure 3.8 b*).

The potential distribution in the sample at 1 MHz is shown in *Figure 3.8* c. The colors in the potential distribution figure represent the absolute values of the potential. One should note that at high frequencies the main potential drops in the YSZ layer and this allows to probe the across-plane conductivity.

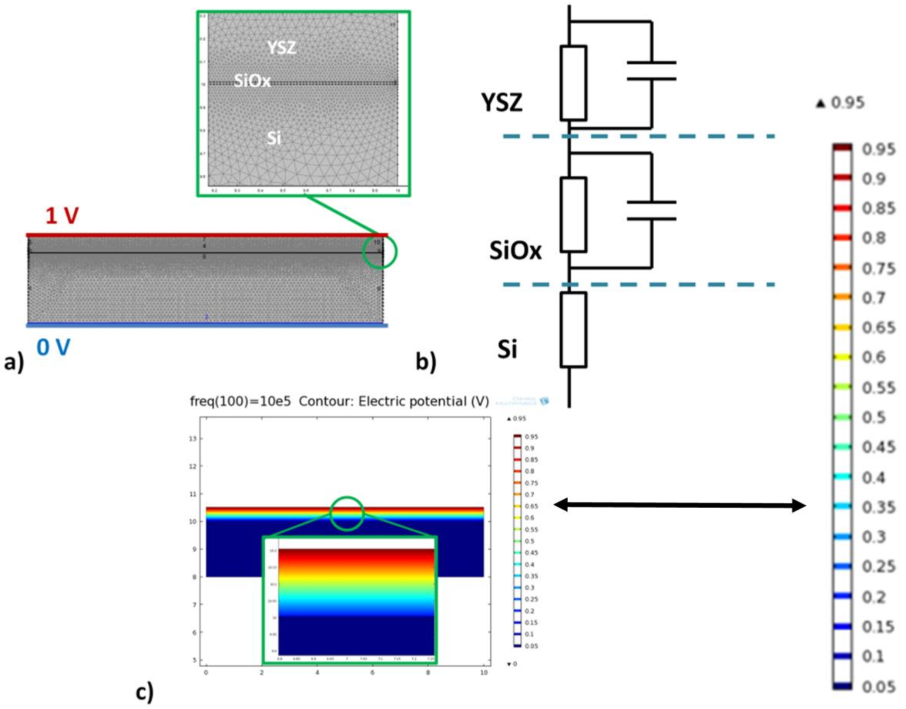

Figure 3.8. *2D system used in the simulations consisting of YSZ and a native silica layer on a silicon wafer (a). Modelling was done with two parallel electrodes. b) The equivalent circuit of across-plane measurement used for fitting; c) Electrical potential distribution in a sample (*$v = 1\cdot10^6$ *Hz), the colors present the absolute values of potential*

Numerically simulated impedance spectra with varied silica thickness are shown in *Figure 3.9*. In a Nyquist graph (*Figure 3.9 a*) only a part of the highly resistive semicircle can be observed. This semicircle can be attributed to the contribution of the silica interlayer, since the increase of the silica layer thickness leads to an increase of the resistance. One should note that in the high frequency range (*Figure 3.9 b*) a part of a semicircle can be found. The resistance of this semicircle does not change with silica thickness variation, which is more obvious in Bode plot of imaginary modulus (*Figure 3.9 d*). Finally the change of the silica layer thickness can be obviously seen in the modulus plot (*Figure 3.9 c*), where the inverse capacitances of the elements become visible. The low frequency semicircle varies respectively with the silica layer thickness – the increase of the silica layer thickness leads to lower capacitance values.

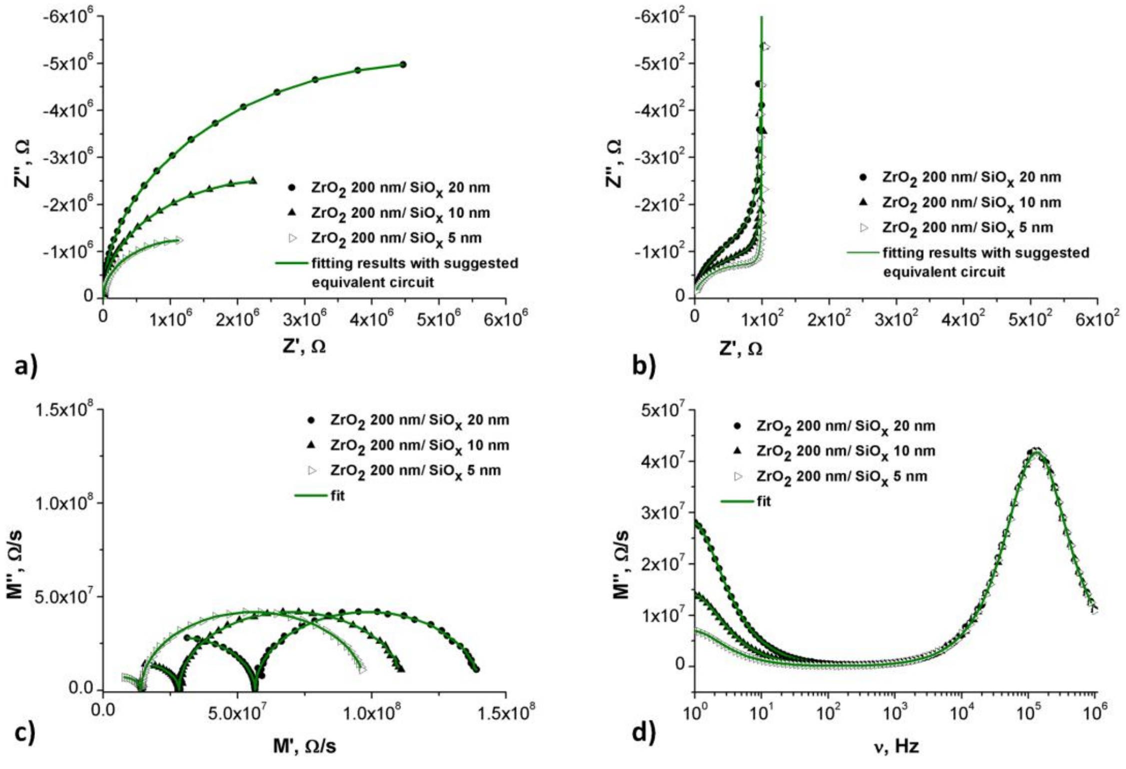

Figure 3.9. *Simulated and fitted impedance spectra with varied silica interlayer thickness, while the YSZ layer thickness was kept constant (t_{YSZ} = 200 nm). a) Nyquist graph; b) Magnified high frequency part of Nyquist plot; c) Modulus plot; d) Bode plot*

The silicon substrate contribution was not found in the impedance spectra, therefore the simulated spectra were finally fitted with a two RC elements equivalent circuit. Fitting curves are also shown in *Figure 3.9*. Numerically simulated spectra and fits are completely identical, which indicates the correctness of the equivalent circuit.

All resulting parameters of the fitting are listed in *Table 3.5*. The fitting errors with the suggested equivalent circuit do not exceed a 3 % limit. The theoretical values were calculated from (*Eq. 3.19)* and (*Eq. 3.20)* in order to verify parameters of the equivalent circuit and are as well listed in *Table 3.5*. Theoretical results and fitting results match very well with almost no deviation. Higher thickness of silica makes the shoulder in Nyquist plots less pronounced, but still allows to probe the YSZ conductivity and it does not make the results less reliable.

Table 3.5. *Results of fitting numerically simulated impedance spectra with varied silica layer thickness. The theoretical values of capacitive and resistive elements of equivalent circuit are evaluated according (Eq. 3.19) and (Eq. 3.20).*

Silica layer thickness:	***5 nm***	***10 nm***	***20 nm***
Theoretical: $R_{YSZ\perp}$, Ω	100		
$C_{YSZ\perp}$, F	$1.19 \cdot 10^{-8}$		
Simulated: $R_{YSZ\perp}$, Ω	99.7	99.9	100.0
$C_{YSZ\perp}$, F	$1.20 \cdot 10^{-8}$	$1.18 \cdot 10^{-8}$	$1.19 \cdot 10^{-8}$
Theoretical: $R_{SiOx\,\|\|}$, Ω	$2.5 \cdot 10^{6}$	$5.0 \cdot 10^{6}$	$1.0 \cdot 10^{7}$
$C_{SiOx\,\|\|}$, F	$7.08 \cdot 10^{-8}$	$3.54 \cdot 10^{-8}$	$1.77 \cdot 10^{-8}$
Simulated: $R_{SiOx\,\|\|}$, Ω	$2.5 \cdot 10^{6}$	$5.0 \cdot 10^{6}$	$1.0 \cdot 10^{7}$
$C_{SiOx\,\|\|}$, F	$7.09 \cdot 10^{-8}$	$3.54 \cdot 10^{-8}$	$1.77 \cdot 10^{-8}$

The numerical simulations were also performed on samples with varying YSZ layer thickness. A variation of the YSZ thickness was also done experimentally and the impedance features will be explicitly discussed in the results part of the thesis. Nevertheless, the fitting results of simulated impedance spectra and theoretical values of equivalent circuit elements are listed in the *Table 3.6*. The capacitance and resistance values of silica from fitting match very well with the theoretical values, independent of the YSZ thickness. Fitting values of the YSZ layer resistance are also in good agreement with theoretical values, although it is worth mentioning that measurements of thinner layers lead to a higher errors. The separability and fitting of the contribution of very thin YSZ layers in the impedance spectrum becomes more complex. The corresponding measurements are shown in Sec. 4.2.

Table 3.6. *Results of fitting numerically simulated impedance spectra with varied YSZ layer thickness. The theoretical values of capacitive and resistive elements of the equivalent circuit are evaluated according (Eq. 3.19) and (Eq. 3.20).*

YSZ layer thickness:	**5 nm**	**10 nm**	**50 nm**	**200 nm**	**500 nm**
Theoretical: $R_{YSZ\perp}$, Ω	2.50	5.00	25.00	100.00	250.00
$C_{YSZ\perp}$, F	$4.78\cdot10^{-7}$	$2.39\cdot10^{-7}$	$4.78\cdot10^{-8}$	$1.19\cdot10^{-8}$	$4.78\cdot10^{-9}$
Simulated: $R_{YSZ\perp}$, Ω	2.65	5.11	25.23	99.73	248.80
Relative error of $R_{YSZ\perp}$, %	6	2.2	0.9	0.3	0.5
$C_{YSZ\perp}$, F	$4.78\cdot10^{-7}$	$2.38\cdot10^{-7}$	$4.79\cdot10^{-8}$	$1.20\cdot10^{-8}$	$4.77\cdot10^{-7}$
Theoretical: $R_{SiOx\,\|\|}$, Ω	$5\cdot10^{6}$				
$C_{SiOx\,\|\|}$, F	$3.54\cdot10^{-8}$				
Simulated: $R_{SiOx\,\|\|}$, Ω	$5\cdot10^{6}$				
$C_{SiOx\,\|\|}$, F	$3.54\cdot10^{-8}$				

3.5 In- and across-plane conductivity using two stripe electrodes

According to the previously demonstrated numerical simulation results, across-plane conductivity measurements on YSZ thin films on silicon substrates are possible. The displacement current may pass through the dielectric interlayer and the across-plane conductivity of YSZ might be extracted from the high frequency shoulder in the impedance spectrum. There are some papers which dealt with the in-plane impedance measurements of YSZ and 8ScZr thin films on silicon substrate [43]. In order to better understand current flow in an in-plane electrode geometry on YSZ layers formed on a silicon substrate, again finite element calculations were used. The modelling was done on the structure shown in Figure 3.10, which is very similar to the previously discussed model. In this case both electrodes are on top of YSZ. This geometry can be simplified for symmetry reasons by placing the ground electrode at the left corner of YSZ, SiOx and Si subdomains. As in the previously discussed model, electrochemical electrode effects were not considered. The sample consisted of three subdomains: YSZ layer (t = 200 nm), SiO_x interlayer (t = 20 nm) and silicon substrate (t = 2 µm), sample length - 10 µm (Figure 3.9). The physical characteristics of the materials used in the model are defined in the Table 3.4. The meshing parameters were the same as in previous models.

It was proven for the previous model that, the displacement current may flow through the silica layer and thus we are able to probe the YSZ conductivity. With the in-plane geometry it is also expected that high frequency current will flow across-plane through the layer, since the resistivity for in-plane flow is much higher. On the other hand, it was also shown in a previous chapter that for lower frequencies current is blocked by the silica layer.

Moreover, it is expected that in an in-plane measurement geometry the low frequency current should flow along the film to the second electrode, which may give us the in-plane conductivity. To prove these statements and to determine how current flows for intermediate frequencies, the numerical simulations were performed. The current flow in a sample and impedance spectra were simulated for frequencies ranging from 100 mHz to 1 MHz.

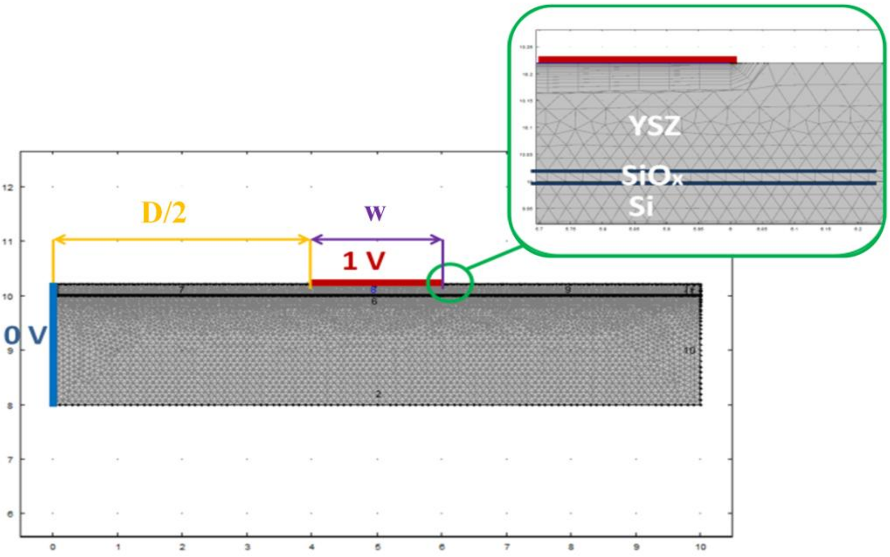

Figure 3.10. *Meshing of the system and model sketch where the electrodes geometry and sample structure (YSZ, SiOx and Si) are presented*

For the simulation of the current distribution in a sample two parallel electrodes were used instead of the measurement geometry shown in Figure 3.10. A model sketch and the simulated distributions of the current lines in a sample are shown in Figure 3.11 for the given frequencies (1 MHz, 50 kHz, 5 kHz and 100 mHz). As it was expected, at high frequencies current flows parallel to the surface normal vector and passes the YSZ and silica layers twice. At lower frequencies there is a transition regime, where the current starts to flip from across-plane to in-plane flow. At very low frequencies only faradaic current exists, which is blocked by silica and therefore flows only in-plane the layer.

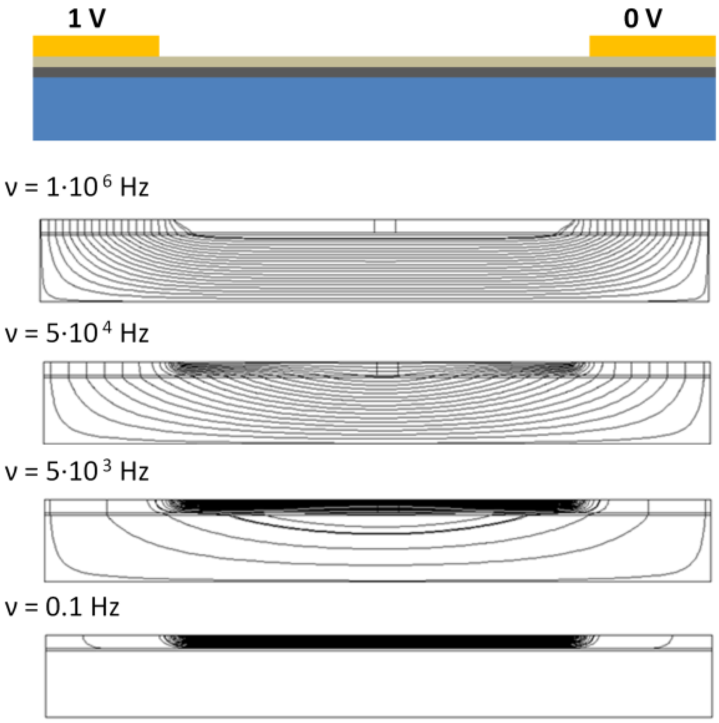

Figure 3.11. *Simulated current line distribution in a sample with in-plane measurement geometry with the given frequencies: 1 MHz, 50 kHz, 5 kHz and 100 mHz*

This demonstrates that the current flips from across- to in-plane flow while the frequency is decreasing. The equivalent circuit in this case has to consider two limiting cases – in and across-plane (*Figure 3.12*). The equivalent circuit for frequencies with prevailing across-plane current flow, i.e. for high frequencies is the same as for the across-plane measurement. The low frequency impedances are fitted with one RC element, where $R_{YSZ\,||}$ presents the in-plane YSZ resistance. The equivalent circuit is more explicitly explained in the experimental results part.

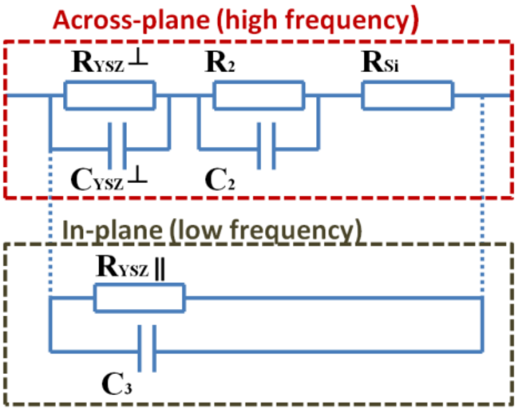

Figure 3.12. *Equivalent circuit used for the in-plane measurement geometry*

The electrode geometry was changed in order to demonstrate the contributions of in- and across-plane conductivities in the impedance plots. The distance between the two electrodes was changed from 1 μm to 6 μm. The variation of the distance between the electrodes should affect only the in-plane part. The width of the electrode was kept constant and thus the across-plane resistance must be constant as well. The numerical simulation results of impedance spectra are shown in *Figure 3.13*. As one can see in the Nyquist plot (*Figure 3.13 a*) the low frequency part of the spectrum consists of one semicircle, which scales with the distance between the electrodes. Lowering the distance between the electrodes leads to a lower resistance and this is one of the strong arguments that the low frequency impedance part corresponds to an in–plane measurement.

The high frequency part, as in the across-plane impedance spectrum, contains a high frequency shoulder, which has a constant resistance, despite variation of electrode distance. Thus the high frequency part can be attributed to the across-plane conductivity of the YSZ layer. Modulus plots give another argumentation for in- and across-plane contributions. One can observe, that the high frequency arc is constant (*Figure 3.13 c*) and variation of the distance does not affect the capacitance which may be attributed to the across-plane YSZ capacitance. In the magnified part of the modulus plot (*Figure 3.13 d*) there are obvious changes of capacitances, which can be related to the in-plane geometry. The fitting results of numerically simulated impedance spectra and theoretical results calculated according to (*Eq. 3.19)* and (*Eq. 3.19)* are listed in *Table 3.7*.

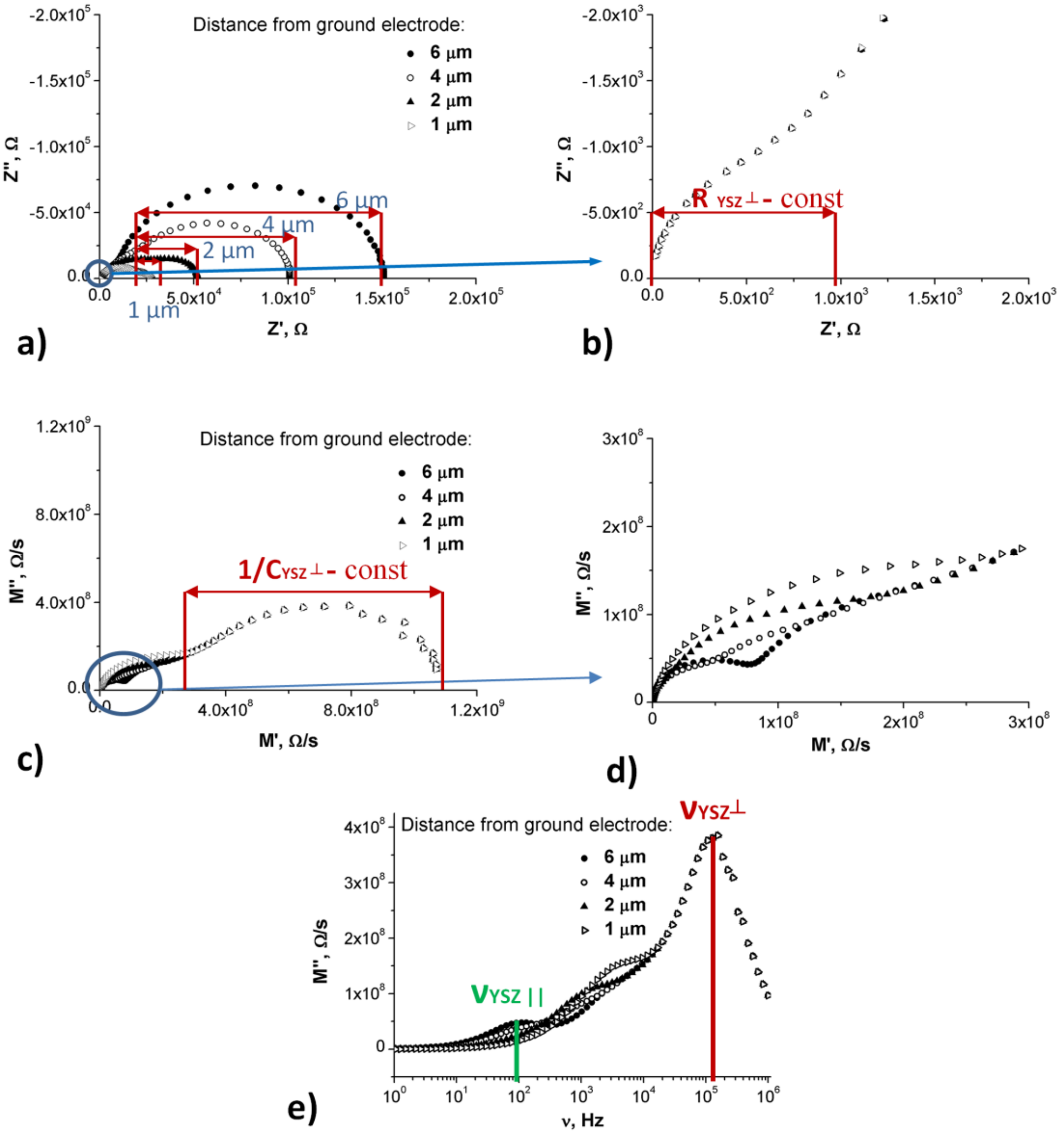

***Figure 3.13.** The effect of distance between ground and electrode with potential 1 V. D/2 in the model was changed to 1, 2, 4 and 6 µm, while the width was kept constant (1 µm): a) Nyquist diagram; b) High frequency part of Nyquist plot; c) Modulus diagram; d) Magnified low frequency part of modulus; e) Bode plot of imaginary part of modulus*

Since only a small part of the across-plane semicircle is visible in the impedance spectrum, this makes the fitting complicated and leads to errors. The simulated impedance spectrum gives us a hint, that the separation of across- part and in-plane in the impedance spectrum can be improved by increasing the distance between the electrodes. The separability of these parts strongly depends on the ratio between $R_{YSZ\perp}$ and $R_{YSZ\,||}$.

Table 3.7. *Fitting results of numerically simulated impedance spectra with varied distances in between the electrodes, while the width was constant (w = 1 μm). The theoretical values were estimated according to (Eq. 3.19) and (Eq. 3.20) with above mentioned geometrical parameter*

Distance from ground electrode:	**1 µm**	**2 µm**	**4 µm**	**6 µm**
Theoretical: $R_{YSZ\perp}$, Ω	10^3			
$C_{YSZ\perp}$, F	$1.19\cdot10^{-9}$			
Simulated: $R_{YSZ\perp}$, Ω	816.7±89.5	813.5±93.5	813.5±93.1	813.0±92.9
$C_{YSZ\perp}$, F	$1.18\cdot10^{-9}$	$1.16\cdot10^{-9}$	$1.16\cdot10^{-9}$	$1.17\cdot10^{-9}$
Theoretical: $R_{YSZ\,\|\|}$, Ω	$2.50\cdot10^{4}$	$5.00\cdot10^{4}$	$1.00\cdot10^{5}$	$1.50\cdot10^{5}$
C^*_{stray}, F	$13.4\cdot10^{-11}$	$8.55\cdot10^{-11}$	$5.02\cdot10^{-11}$	$3.56\cdot10^{-11}$
Simulated: $R_{YSZ\,\|\|}$, Ω	$2.72\cdot10^{4}$	$5.20\cdot10^{4}$	$1.02\cdot10^{5}$	$1.51\cdot10^{5}$
C_3, F	$1.04\cdot10^{-8}$	$1.19\cdot10^{-8}$	$1.25\cdot10^{-8}$	$1.14\cdot10^{-8}$

** in-plane capacitance was calculated by FEM*

The fitting results of the in-plane part are also listed in *Table 3.7.* As one can see, the resistance of the in-plane part is in a good agreement with the theoretical values. Nevertheless interpretation of the in-plane capacitance values is more complex. The theoretical values of in-plane capacitance cannot be calculated according to *Eq. 3.19* since both electrodes are arranged in the same plane. The theoretical values of the capacitance were calculated by the finite element method with electrostatic model. One can see that simulated in-plane capacitance values (C_3) are higher than the theoretical values. The in-plane capacitance is also independent of the electrode geometry and its physical meaning is unclear.

Table 3.8. *Fitting results of numerically simulated impedance spectra with varied width of the electrodes, while the distance in between the electrodes was constant (D/2 = 4 μm). The theoretical values were estimated according to (Eq. 3.19) and (Eq. 3.20), with the above mentioned geometrical parameter*

Electrode width:	**1 µm**	**2 µm**	**4 µm**	**6 µm**
Theoretical: $R_{YSZ\perp}$, Ω	1000	500	250	167
$C_{YSZ\perp}$, F	$1.19\cdot10^{-9}$	$2.39\cdot10^{-9}$	$4.78\cdot10^{-9}$	$7.19\cdot10^{-9}$
Simulated: $R_{YSZ\perp}$, Ω	766.0	420.0	199.2	144.0
$C_{YSZ\perp}$, F	$1.02\cdot10^{-9}$	$2.00\cdot10^{-9}$	$3.00\cdot10^{-9}$	$5.65\cdot10^{-9}$
Theoretical: $R_{YSZ\,\|\|}$, Ω	10^5			
C^*_{stray}, F	$50.2\cdot10^{-12}$	$50.5\cdot10^{-12}$	$51.1\cdot10^{-12}$	$51.2\cdot10^{-12}$
Simulated: $R_{YSZ\,\|\|}$, Ω	$1.02\cdot10^{5}$	$1.02\cdot10^{5}$	$1.02\cdot10^{5}$	$1.02\cdot10^{5}$
C_3, F	$12.1\cdot10^{-9}$	$12.4\cdot10^{-9}$	$12.8\cdot10^{-9}$	$12.9\cdot10^{-9}$

** in-plane capacitance was calculated by FEM*

For the final argumentation in terms of in- and across-plane measurement, additional numerical simulations of impedance spectra were done with varied electrode width. Fitting results of the simulated spectra and theoretical values are listed in *Table 3.8* and results deviate due to the sophisticated fitting of the spectra. Simulated impedance spectra are shown in *Figure 3.14*. A highly resistive arc in the Nyquist graph (*Figure 3.14 a*) with a constant resistance is observed. Variation of electrode width changes only the across-plane part in impedance spectra (*Figure 3.14 b*). The capacitance of the across-plane part also changes in accordance with the electrode geometry, while the in-plane capacitance is constant (*Figure 3.14 d)*. Finally, Bode plot of the imaginary modulus (*Figure 3.14 e*) demonstrates that in- and across-plane parts are constant and that the relaxation frequency is independent of geometry. All these observations let us conclude that in- and across-plane information can be obtained in one impedance measurement. The corresponding experiments are shown in Sec. 4.3.

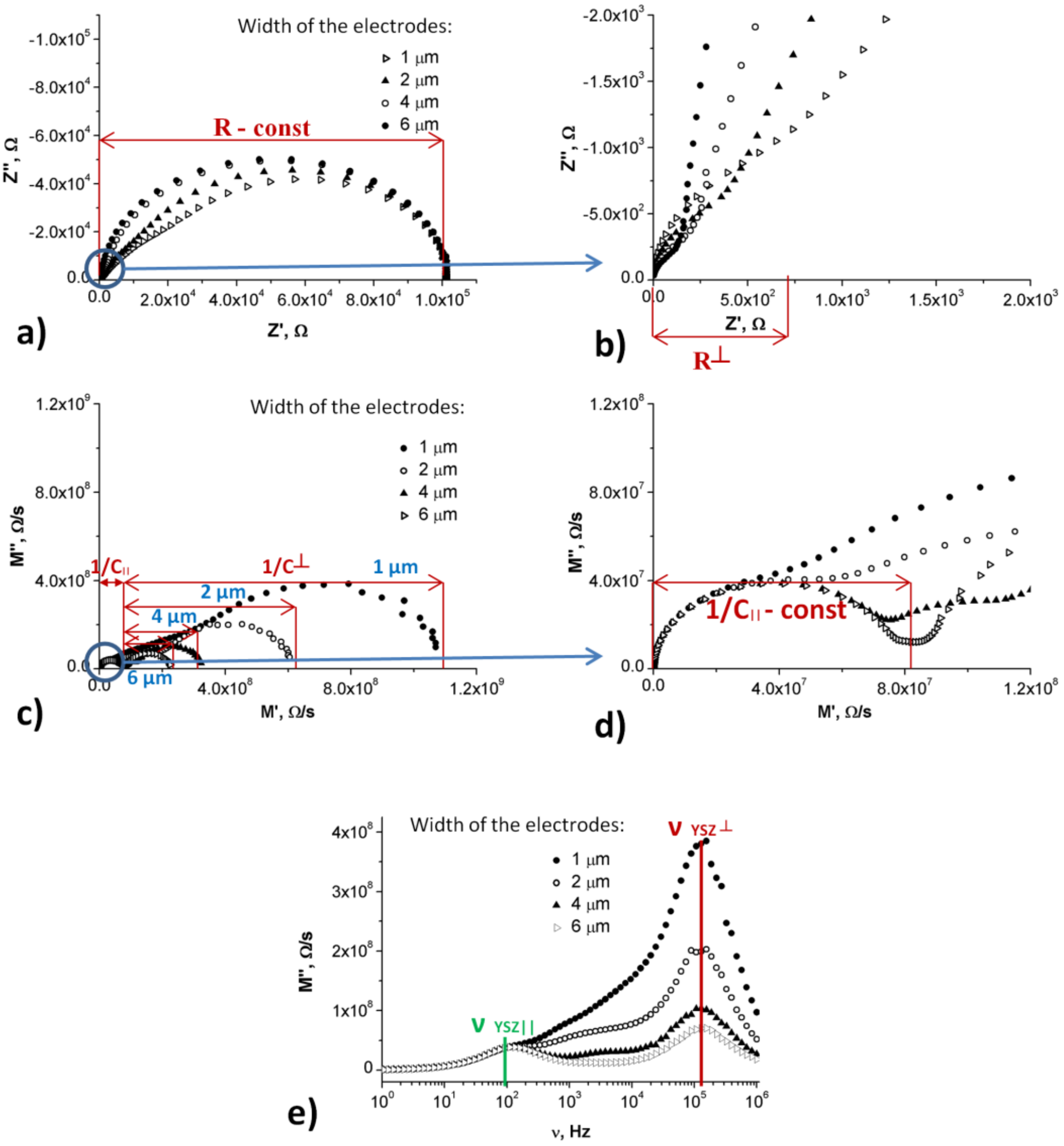

Figure 3.14. *The effect of the electrode width (w = 1, 2, 4 and 6 μm), while D/2 in the model was kept constant (4 μm): a) Nyquist diagram; b) High frequency part of Nyquist plot; c) Modulus diagram; d) Magnified low frequency part of modulus; e) Bode plot of the imaginary part of the modulus*

The experimental chapter consists of five parts. In the first part the experimental results on the grain and grain boundary separation problem in the thin film case are presented [111]. The second part deals with the across-plane conductivity measurements of YSZ thin films on silicon substrates, where the role of a dielectric interlayer for impedance studies is shown [112]. In the third part a study is presented which deals with the effect of the thin film microstructure on the across-plane conductivity [82]. The fourth part demonstrates the conductivity anisotropy of the YSZ thin films on silicon substrates [113]. In the last part the effect of a dielectric interlayer is demonstrated for in- and across-plane measurements of YSZ thin films.

4.1 Separation of grain boundary contribution to impedance spectra in case of YSZ thin films

As it was discussed in the finite elements calculations part - grain and grain boundary separation in thin films is not trivial and requires a special geometry of the electrodes. In this part of the thesis the corresponding experimental ionic conductivity measurements on YSZ thin films with interdigit electrodes will be shown. YSZ thin layers were synthesized by the PLD method with deposition parameters listed in *Table 4.1*. The distance in between the PLD target and alumina substrate was kept constant (6.3 cm). All depositions were made with the same laser repetition rate (5 Hz) and laser power (400 mJ). The substrate set temperature was 900 °C, while temperatures measured with a pyrometer (the emission coefficient was set to 0.9) are listed in *Table 4.1*. YSZ thin films were deposited on (0001)-oriented single crystalline sapphire substrates at 4 Pa oxygen background pressure. All the layers were synthesized with the same procedure, except deposition time, which was varied in order to change the layer thickness. The deposition of thicker layers was performed with two/three targets, since longer deposition causes significant changes of a target surface.

Table 4.1. *The PLD synthesis parameters of YSZ thin films (laser power - 400 mJ, oxygen pressure – 4 Pa, distance target-substrate - 6.3 cm)*

Sample	Substrate temperature, °C	Deposition time, min	Layer thickness, nm
A	630	30	18±3
B	628	2x30	32±1
C	685	3x30	105±1

The crystallography of all synthesized layers was checked by X-ray diffraction and diffractograms are shown in *Figure 4.1* and *Figure 4.3*. The thin YSZ layers are highly textured and demonstrate only (111) orientation. In order to investigate the microstructure of a YSZ layer SEM measurements were done on a cross-section of a sample. For the cross-section SEM measurement an additional platinum layer was deposited on the YSZ layer. The determination of the microstructure was indeed sophisticated, since layer and substrate were charging and even the thin platinum layer did not help to overcome charging effects (*Figure 4.2*). According to the XRD results, which demonstrate YSZ cubic phase with a predominant orientation and from previous studies [5] - YSZ thin films prepared with such deposition parameters should have a columnar microstructure.

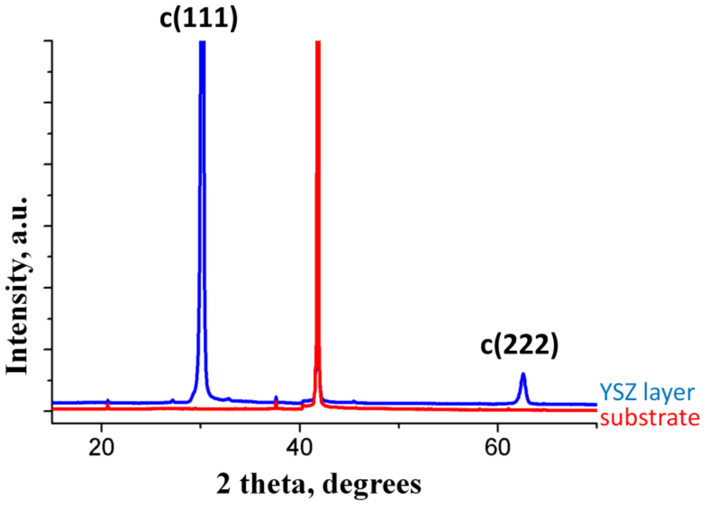

Figure 4.1. *XRD patterns of YSZ thin film (105 nm, sample C) and sapphire substrate*

From the cross-section photo (*Figure 4.2*) the determination of the layer thickness was impossible. The sample thickness was determined from a combination of two methods – secondary ion mass spectrometry (SIMS) with digital holographic microscopy (DHM). The samples were firstly etched with the SIMS to the layer-substrate interface and the sputter crater was measured by DHM. The resulting thickness values for all the layers are listed in *Table 4.1*.

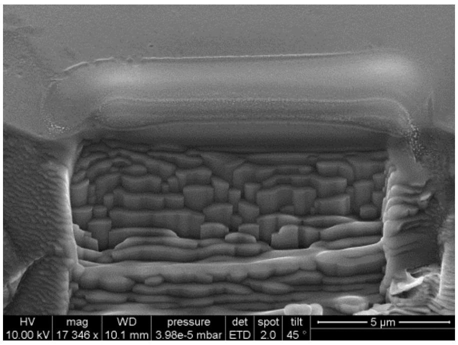

Figure 4.2. *The cross-section image of the sample B prepared by ion beam milling*

For the further study samples A and B were divided into four pieces and each of them was annealed. The annealing of YSZ thin films can lead to the following two possible effects: a) the growth of grains and b) the formation and growth of an additional ordered phase (phase decomposition) [114]. In order to vary the crystallite size and grain boundary density, the samples were annealed at 1000 °C with varied duration of the annealing process (1 h, 3 h and 5 h). One of the pieces of sample A and sample B was annealed at 1200 °C for 5 h. The annealing parameters are listed in *Table 4.2*.

Table 4.2. *The annealing parameters of samples A and B*

Sample	Temperature, °C	Annealing duration, h
A1 and **B1**	Not annealed	
A2 and **B2**	1000	1
A3 and **B3**		3
A4 and **B4**		5
A5, B5	1200	5

The XRD diffractograms of as prepared samples A and B and after annealing are shown in *Figure 4.3*. Both layers before and after annealing demonstrate cubic fluorite structure with a predominant (111) orientation. One should note, that the peak (111) shifts towards a higher diffraction angle in both samples after annealing (the magnified part in *Figure 4.3*), due to the change of lattice parameters. The lattice parameters shifted from 0.517 nm to 0.512 nm in the sample A and from 0.516 nm to 0.512 nm in the sample B. The shift of lattice parameter might be attributed to a crystallization of the layers.

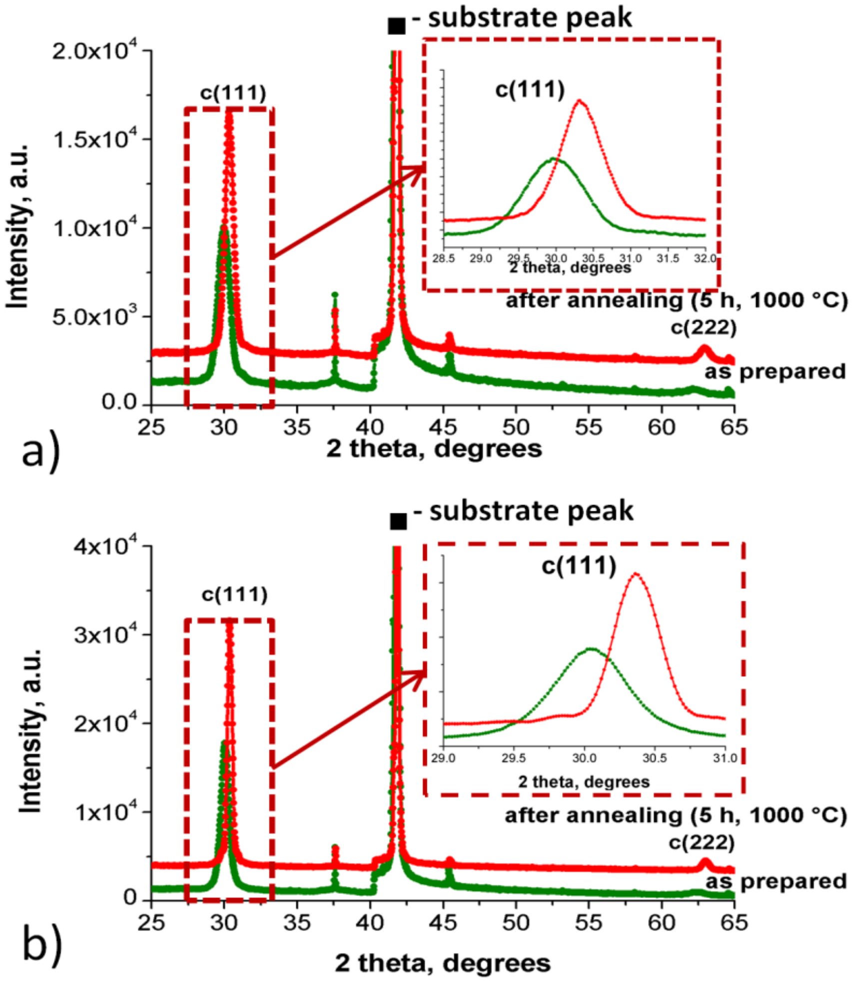

Figure 4.3. *XRD patterns of YSZ thin layers before and after annealing (1000 °C, 5 h): a) t = 18 nm (sample A) and b) t = 32 nm (sample B)*

The XRD measurements were done with Bragg-Brentano θ-2θ measurement geometry, which allows to probe perpendicular dimensions of the crystallite. The crystallite size was determined from a (111) peak broadening by TOPAS software and resulted in 15 nm for layer A, 22 nm for layer B and 72 nm for layer C. The XRD patterns after annealing (5 h at 1000 °C) reveal decreased peak width of YSZ peaks due to the increasing crystallite size after annealing. The calculated nominal crystallite size for layers A and B resulted in 21 nm and 43 nm respectively after annealing. The layer C was not annealed.

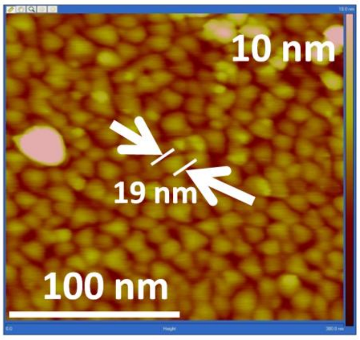

Figure 4.4. *The surface topography of sample C measured by AFM*

In order to determine the column width of the sintered layers, surface topography was checked by AFM (*Figure 4.4*). The surface topography of layer C demonstrated a homogenous distribution of grains with similar width (*Figure 4.4*). The average column width was determined from AFM measurements for layer C and resulted in 19 ± 3 nm. Unfortunately determination of column widths for very thin layers (A and B) was impossible due to insufficient contrast.

The AFM measurements on layer A5, annealed at 1200 °C revealed defects (*Figure 4.5 b* noted with the white arrows) and cracks which were developed during the annealing process. The defects observed in the layer may be caused by the recrystallization, which is also visible from the XRD pattern (*Figure 4.5 a*). After deposition this sample contained only one orientation (111) (*Figure 4.5 a 1*), while after annealing other crystallographic orientations appear (*Figure 4.5 a 2*) and according XRD analysis the sample becomes polycrystalline. Such recrystallization of a layer may lead to a formation of cracks. The analysis of impedance spectra of such a layer would not be straightforward, since additional features appear in the spectrum (*Figure 4.5 c*).

The impedance measurements were performed on the samples A and B before and after annealing. The measurements were done in a frequency range from 1 Hz to 1 MHz with the amplitude of 1 V and the temperature range was from 200 °C to 550 °C (more detailed description of a micro-measurement can be found in the methods part).

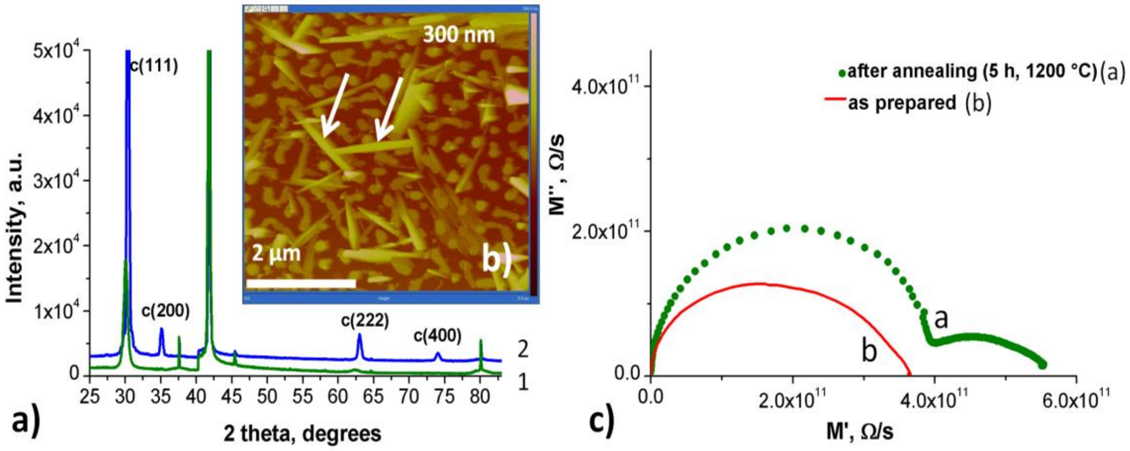

Figure 4.5. *a) XRD patterns of YSZ layer before (1) and after (2) annealing; b) Surface topography of a sample **A** after annealing at 1200 °C for 5 h; c) Modulus plot of as deposited layer and after annealing at 1200 °C for 5 h*

As it was discussed in the theoretical considerations part the grain and grain boundary contributions might be separated in impedance spectra applying a special geometry of the electrodes. The impedance measurements on layer C were done with two different electrode geometries: interdigit electrodes (*Figure 4.6 a*) and with the wide electrodes (D = 500 µm and w = 5000 µm) (*Figure 4.6 b*), similar to those usually used for ionic conductivity measurements in thin films.

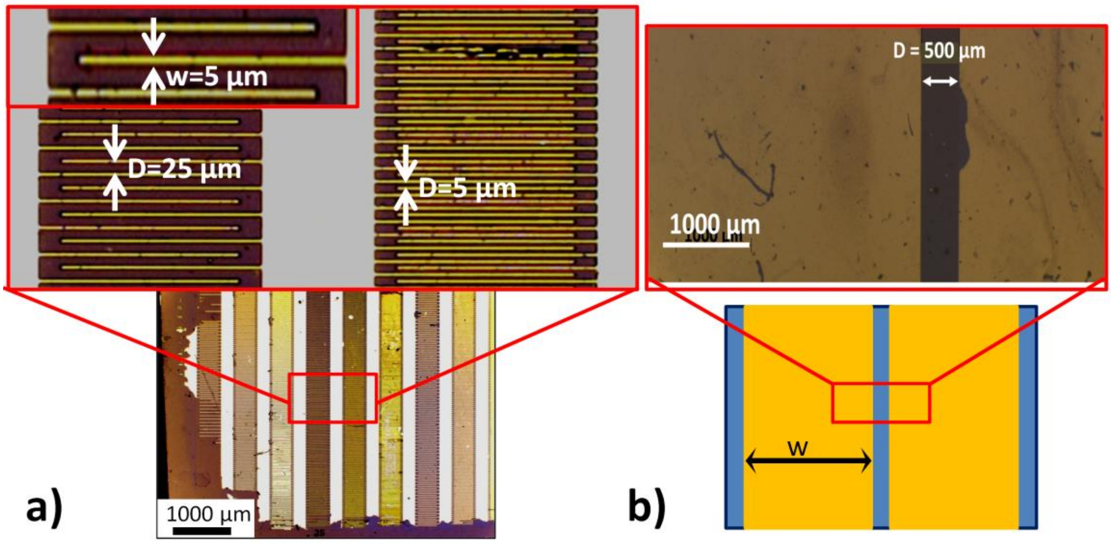

Figure 4.6. *The geometry of the electrodes applied in the impedance measurements: a) interdigit electrodes; b) wide electrodes (usually used for impedance measurements)*

In order to demonstrate the effect of a stray capacitance for impedance spectra, the impedance measurements were done with different geometries of close spaced interdigital electrodes. The main differences between electrode geometries were different distances between the interdigit electrodes (D = 25, 10 and 5 µm) and different widths of the interdigit electrodes (w = 10 and 5 µm). The geometries of the electrodes are shown in *Figure 4.6 a*.

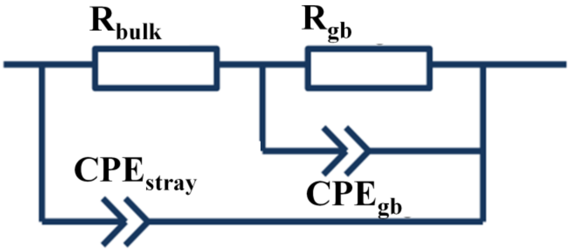

Figure 4.7. *The equivalent circuit for a fitting of the in-plane impedance measurement on an insulating substrate (also denoted 2 R-CPE simplified)*

The measured Nyquist and modulus plots with both geometries are shown in *Figure 4.8*. The fitting of the impedance spectra was done with the equivalent circuit shown in *Figure 4.7*. The meaningfulness of it was more explicitly discussed in the theoretical considerations part. The equivalent circuit consists of a R-CPE element (grain boundaries contribution), a resistive element in series (bulk contribution) and a capacitive element in parallel (stray capacitance of the substrate).

Figure 4.8 a and b also shows that impedance spectrum of interdigital electrodes cannot be fitted with one R-CPE element. This is particularly obvious from the modulus graph (*Figure 3.8 b* red line). The semicircle in the Nyquist plot, which was measured with the interdigital electrodes, is slightly depressed (*Figure 4.8 a* and *b*), which is an indication that it consist of two overlapping arcs. Indeed, the impedance spectrum was successfully fitted with the suggested equivalent circuit in *Figure 4.7*.

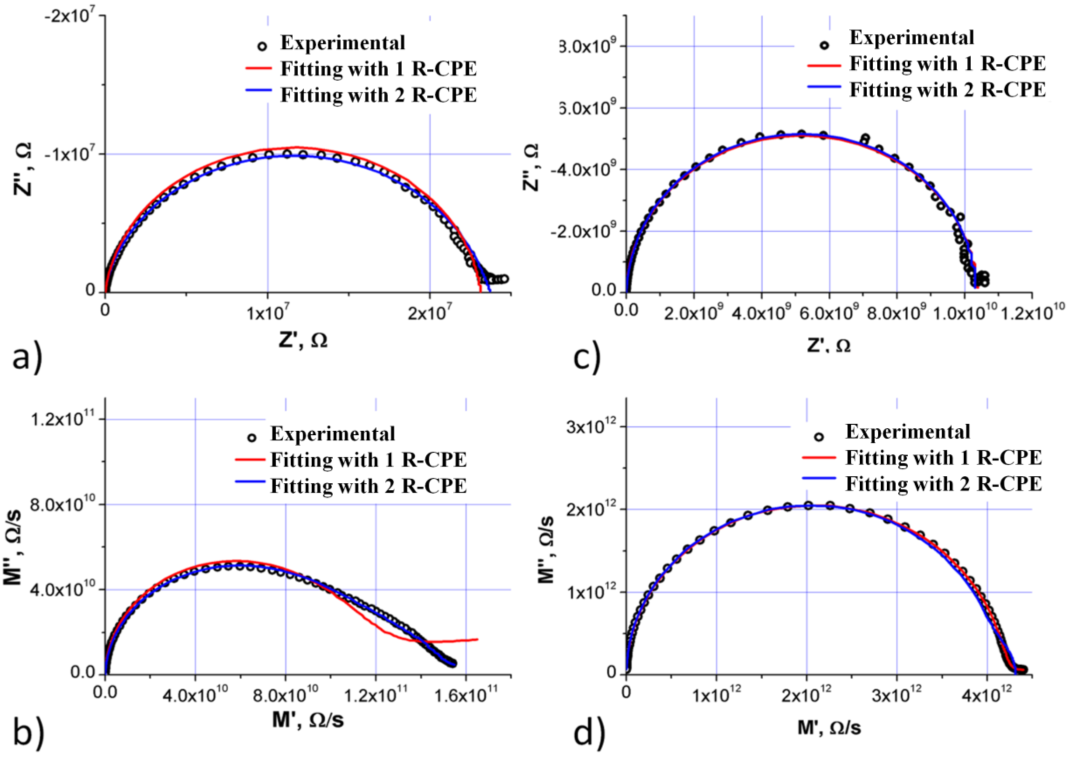

Figure 4.8. *a) and b) Nyquist and modulus plots in interdigit electrodes case (D = 25 µm and w = 10 µm). The red line in the graphs presents fitting results with one R-CPE element, blue line – fitting results with the equivalent circuit shown in Figure 4.7; c) and d) Nyquist and modulus plots with the wide electrodes (D = 500 µm and w = 5000 µm). Red and blue lines are the fitting results. In both cases impedance was measured at 300 °C*

The impedance spectra measured on the wide electrodes exhibit a different shape and consist only of one arc. The impedance spectra of wide electrodes were also fitted with both equivalent circuits. In this case fitting of the spectra with one R-CPE element resulted in an acceptable fit (*Figure 3.8 c* and *d*). As explicitly discussed in the theoretical part, the wide electrodes lead to a high stray capacitance, thus making contributions of grain and grain boundaries in impedance spectra inseparable. In the equivalent circuit (*Figure 4.7*) constant phase elements instead of capacitive elements were used and the capacitance was calculated by [114]:

$$C_{CPE} = (R^{(1-n)} \cdot Q)^{\frac{1}{n}} \qquad \textbf{(Eq. 4.1)}$$

where n and Q are fitting parameters. For an ideal capacitor $n = 1$. The fitting parameter n in the fitting usually resulted in 0.7-0.8 for CPE of grain boundaries and approximately 1 for CPE of the stray capacitance.

The meaningfulness of the analysis by the circuit (*Figure 4.7*) was first checked by considering the geometry dependence of the capacitances. Measured values are given in *Table 4.3*. For comparison with model considerations, the capacitance of grain boundaries was calculated according to:

$$C_{gb} = \frac{\varepsilon_{YSZ} \cdot t \cdot l}{D} \cdot \frac{d_g}{d_{gb}} \qquad \textbf{(Eq. 4.2)}$$

where D – distance between the interdigital electrodes, l – length of the electrode and t – layer thickness. The d_g and d_{gb} are crystallite size and grain boundary width. The grain size was estimated from AFM and resulted is 19 nm and the grain boundary width according ref. [45] was taken as 1 nm. The fit results of grain boundary and stray capacitances for the different electrode geometries were normalized to the length of the electrodes and are listed in *Table 4.3*. The stray capacitance of such an electrode geometry depends on the β coefficient (*Eq. 4.3)*, which varies non-linearly with the geometry of the electrodes as this has been demonstrated in the theoretical part.

$$C_{stray} = \frac{\varepsilon_{substrate} \cdot w \cdot l}{D} \cdot \beta \qquad \textbf{(Eq. 4.3)}$$

where w – electrode width.

The numerical simulations were done for a 2 D model (*Figure 3.5*) to obtain theoretical values of the stray capacitance for a varied electrode geometry. The calculated values are also included in *Table 4.3*.

Table 4.3. *The effect of interdigital electrode geometry for measured stray and grain boundary capacitances*

Electrode geometry: width/distance	C_{gb}, pF/m	C_{stray}, pF/m	C_{gb}/C_{stray}	C_{stray}*, pF/m (from numerical simulations)
10/25	45.1	95.1	0.44	41.71
5/25	48.6	66.5	0.73	38.91
10/10	73.7	70.4	1.05	62.64
10/10	83.8	73.9	1.13	
5/10	95.9	53.3	1.79	55.41

One should note from the numerical simulation results that the lowest stray capacitance was observed on the narrowest electrodes with the largest distance in between the electrodes (*w* = 5 µm, *D* = 25 µm). The effect of the stray capacitance was checked experimentally by varying the width of the electrodes, while the distance was kept constant. In this case only the stray capacitance should change. One should note, that with the same distance between the electrodes, but with the different widths (5/25 and 10/25, 10/10 and 5/10) the grain boundary capacitances are similar, while the stray capacitance varies in accordance with the geometry. The stray capacitance for the geometry 10/25 is unexpectedly high in comparison with the theoretical value. When decreasing the distance between the electrodes from 25 µm to 10 µm the capacitance of grain boundaries increases by a factor of 1.86 for w = 10 µm and 1.97 for w = 5 µm. This is somewhat less than expected theoretically. Lowering the distance and the width of the electrodes (*Table 4.3,* 10/10, 5/10) lead to meaningful stray capacitance values, which are in accordance with the theoretical one. All together it can be concluded that the experimentally determined capacitances vary in the expected manner when changing the electrode geometry.

The ratio of grain boundary capacitance and stray capacitance is an important parameter for grain and grain boundaries separation in impedance spectrum. A higher ratio leads to a less complex separability. The highest ratio was found for closed spaced and narrow electrodes (*D* – 10 µm and *w* – 5 µm) – 1.79.

The other argument of successful separation of grain boundaries and bulk contributions are the conductivity values and activation energies. As it was discussed in the introduction, due to the yttrium segregation YSZ may have highly resistive grain boundaries [45]. Yttrium tends to segregate to grain boundaries, which causes oxygen depletion in adjacent space charges. The grain boundaries usually exhibit two orders of magnitude lower conductivity and 0.2 eV higher activation energy than YSZ bulk. The conductivity in our experiment was evaluated by three different electrode geometries. The Arrhenius plot for bulk and grain boundary conductivities is shown in *Figure 4.9*. For reasons of comparison the conductivity measurements were also done on YSZ pellets with two parallel silver electrodes. The conductivity values are also plotted in on Arrhenius graph. The conductivity of grain boundaries was calculated according to:

$$\sigma_{gb} = \frac{D}{l \cdot t \cdot R_{gb}} \cdot \frac{d_{gb}}{d_g} \qquad \textbf{(Eq. 4.4)}$$

In *Figure 4.9* Arrhenius graphs are plotted, obtained from impedance measurements with three different geometries: interdigit electrodes (25/10 and 10/10) and wide electrodes (500/5000). For reasons of comparison the YSZ bulk conductivity of a pellet is also shown in *Figure 4.9*.

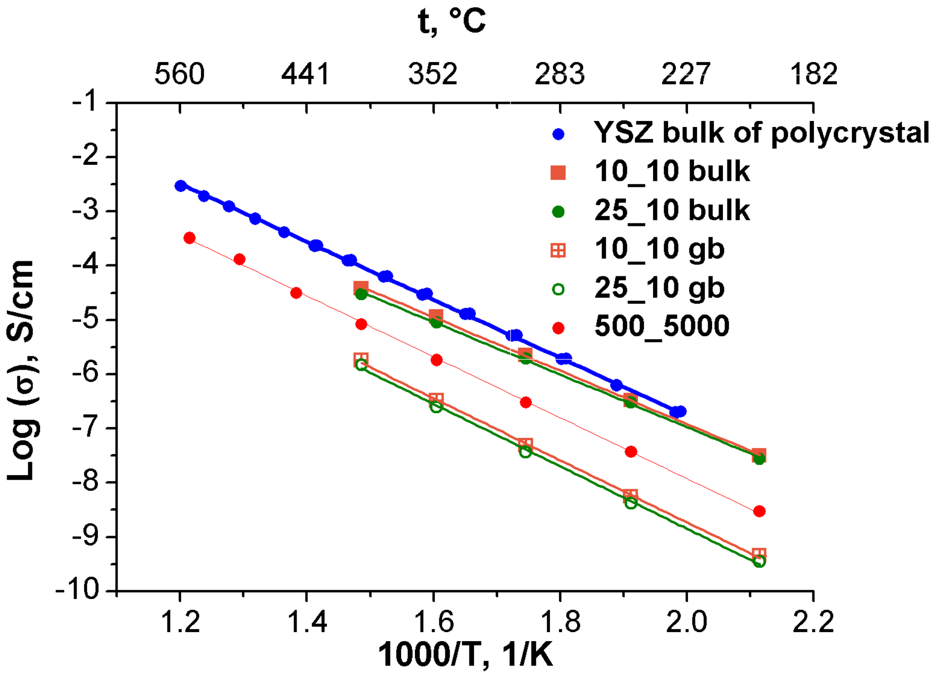

Figure 4.9. *Arrhenius plot of conductivities with varied geometry of the electrodes. The blue line presents the bulk conductivity of a YSZ pellet. The conductivity of the YSZ thin film was measured with three different electrode geometries*

One should note that the bulk conductivities obtained with the interdigit electrodes are in line with each other, independent of the geometry. The bulk conductivity of YSZ thin films is slightly lower than the YSZ polycrystal bulk conductivity. This could be caused by the temperature measurement errors of thin film experiments. The conductivity of grain boundaries (*Figure 4.9* open symbols) with both geometries match with each other and as expected is two orders of magnitude lower than the bulk conductivity. The impedance measurements with the wide electrodes (500/5000) lead to one arc in a Nyquist plot, hence the contribution of grains and grain boundaries were inseparable. Impedance measurements with such an electrode geometry only reveal the total conductivity, which is a combination of grain and grain boundary conductivities.

This can be seen in the Arrhenius plot (*Figure 4.9*), where the total conductivity obtained with 500/5000 electrodes is plotted (red line) and is lower than the bulk but higher than the conductivity of grain boundaries.

The activation energies for all measured conductivities are determined from Arrhenius plots and listed in *Table 4.4*. The activation energies for bulk conductivity are approximately 0.17 eV lower in comparison with the activation energies for grain boundary conductivity.

Table 4.4. *Activation energies of bulk (E_{bulk}) and grain boundary (E_{gb}) conductivities of YSZ measured with different electrode geometries*

Geometry of the electrodes: width/distance	E_{gb}, eV	E_{bulk}, eV
10/25	1.14	0.96
10/10	1.13	0.98
5000/500	1.11	

The same measurements were done on A and B samples, which have significantly lower thickness. As it was mentioned previously A and B samples were divided into 4 pieces and each of them was annealed at 1000 °C with different annealing time. The annealing of thin layers should lead to a crystallization of YSZ layers, which changes the crystallite size. The growth of the crystallites changes the density of grain boundaries in thin films, which should be visible in the impedance spectrum.

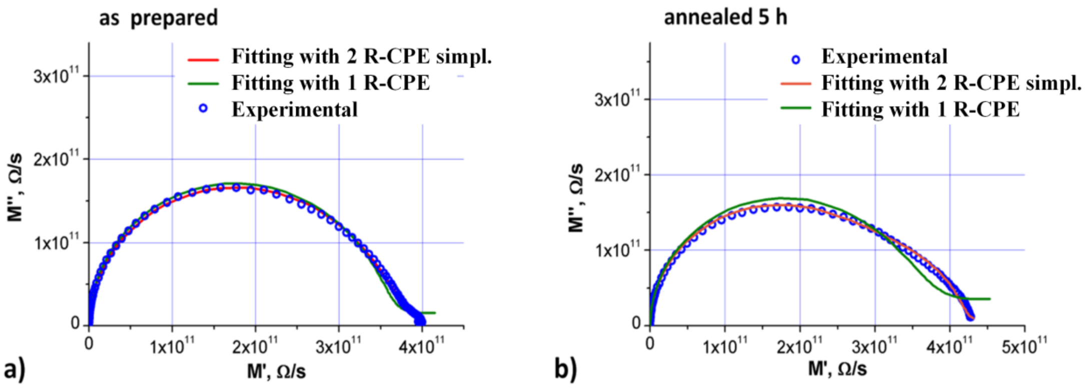

Figure 4.10. *Modulus plots of as prepared layer and an annealed one (after 5h). The modulus plots were fitted with two equivalent circuits: the equivalent circuit shown in Figure 4.7 and one R-CPE element*

The impedance measurements were done with interdigital electrodes with the following geometrical parameters: D = 25 µm, w = 10 µm. Measured modulus plot of sintered and annealed layers are shown in *Figure 4.10.* It is not possible to compare these two plots quantitatively, since the number of interdigital electrodes was different. However, qualitatively one can observe that the shapes of the spectra are different. The contribution of grain boundaries after annealing becomes more pronounced in the modulus part, since the capacitance of grain boundaries increases. The impedance measurements were done in a temperature range from 200 to 550 °C and for each temperature the capacitance values were determined. The average stray and grain boundary capacitance was determined for each sample and listed in *Table 4.5.*

Table 4.5. *The annealing effect on stray and grain boundary capacitance*

	Annealing time	**C_{gb}, pF/m**	**C_{stray}, pF/m**
Sample A (YSZ layer (18 nm))	**Not annealed**	38.70±16.6	51.4±5.2
	1 h	16.5±3.4	54.8±3.0
	3 h	17.4±2.4	51.6±3.2
	5 h	23.7±2.5	63.2±3.4
Sample B (YSZ layer (32 nm))	**Not annealed**	19.6±3.0	74±5.1
	1 h	20.1±3.0	54.4±2.0
	3 h	23.7±1.6	50.3±3.7
	5 h	33.3±2.3	62.8±3.7

The measurements of impedances on very thin as sintered layers lead to unexpectedly high capacitances and deviation of the results (*Table 4.5*), which is accompanied by a wide error range. The grain boundary capacitances of annealed layers of sample A are increasing with sintering time. In this case the stray capacitance should not change since it is normalized to the electrode length and all other geometrical parameters were the same. The stray capacitance values slightly deviate from one sample to another.

The grain boundary capacitance of sample B demonstrates a clear tendency to increase with the annealing time due to the decreasing total grain boundary thickness. The other evidence of the microstructure change can be observed in the Bode plot of imaginary modulus (*Figure 4.11 a*). The frequency of a peak in the Bode plot of the imaginary modulus presents the relaxation frequency of an RC element and is equal to:

$$\omega_r = \frac{1}{RC} \qquad \textbf{(Eq. 4.5)}$$

The relaxation frequency is independent of the geometry of the electrodes and it depends only on material properties. The slight shift of the relaxation frequency indicates that not only number but also the grain boundary structure or chemistry changes during annealing.

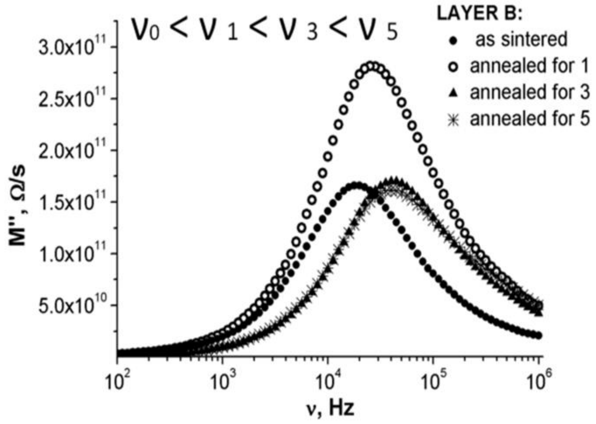

Figure 4.11. *a) Bode plot of imaginary modulus part (measured at 300 °C) of the samples with varied annealing time*

The conductivities of YSZ layer bulk were determined for all A and B samples before and after annealing. The conductivities of two samples (with the shortest and longest annealing times) are shown in Arrhenius plot (*Figure 4.12*). From the impedance measurements only the YSZ bulk conductivities were determined. For these samples the determination of grain boundary conductivity was not possible despite separation of R_{gb} and R_{bulk}, since the column width is not known.

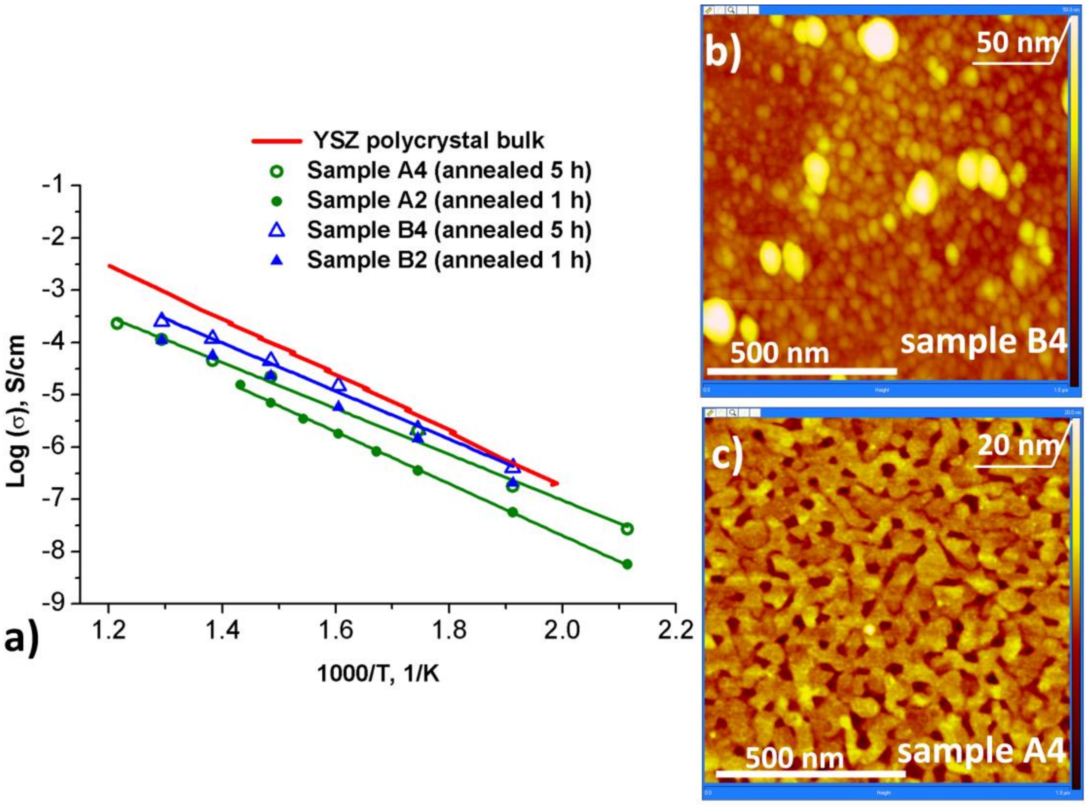

Figure 4.12. *Arrhenius plot of bulk conductivities of the samples A and B as prepared and after annealing (T = 1000 °C, 5h)*

As one can see from Arrhenius plot the conductivities of shorter annealed (A2, B2) samples are slightly lower than those of the longer annealed ones (A4, B4). This could be explained by crystallization of the samples. The conductivities of the thinner sample (A) are lower than the conductivities of the thicker one (B), which could be attributed to higher porosity of sample A. It was observed from AFM image that the thinner sample A exhibits a porous microstructure (*Figure 4.12 c*).

The activation energies of conductivities are listed in *Table 4.6*. Independent of the layer thickness and annealing time the activation energies are ~0.9 eV, which is in accordance with YSZ bulk activation energy.

Table 4.6. *The activation energies of bulk conductivity of YSZ thin films*

Annealing time, h	**0**	**1**	**3**	**5**
E_{bulk} (eV) of sample A (YSZ 18 nm)	0.81	0.98	0.87	0.87
E_{bulk} (eV) of sample B (YSZ 32 nm)	0.89	0.88	0.93	0.91

Summarizing this part of the thesis, one can conclude, that the application of a special electrode geometry leads to separation of grain and grain boundaries in the impedance spectrum also for thin films. It was proven experimentally that the optimization of the electrode geometry (distance and width) results in a lower stray capacitance and improved the ratio between stray and grain boundary capacitance. The effect of an optimized capacitance ratio was also demonstrated by annealing the samples and varying the density of grain boundaries. It was proven that the conductivity measurements of grain and grain boundaries can be done on layers as thin as 18 nm. The experimental results of impedance measurements such as conductivity, capacitance and activation energies were in a meaningful range, which is a strong indication of the correctness of the analysis in terms of bulk and grain boundary contributions.

4.2 Impedance measurements of YSZ layers deposited on silicon substrates

4.2.1 Silica interlayer effect on the across-plane conductivity measurement of YSZ thin films

Across-plane conductivity measurements on ion conducting thin films of a few ten nanometers thickness are challenging due to frequently occurring short-circuits through pinholes in the layer. In Sec. 3.4, a method was proposed which should allow across-plane conductivity measurements on very thin yttria stabilized zirconia (YSZ) layers. In this chapter it is experimentally shown that such measurements are indeed possible on YSZ layers with thicknesses as low as 20 nm. YSZ layers were prepared onto silicon substrates with a thin native silica interlayer and the across-plane conductivity was measured on circular microelectrodes by impedance spectroscopy. The silica interlayer exhibits strongly blocking behavior, which helps to avoid short-circuits through the pinholes. Different relaxation frequencies of YSZ and silica make separation of these layers possible. The suggested equivalent circuit, which allows extraction of YSZ properties and its validity is proven by varying microelectrodes size and layer thickness.

YSZ layers of 20 – 90 nm thickness were prepared by varying the PLD deposition time. The thickness of the layers was determined from scanning electron microscopy cross section images. Structure and phase of the layers were determined by X-ray diffraction measurements. The width of the grain columns in the layers was estimated by atomic force microscopy (AFM).

For the conductivity measurements, circular microelectrodes of different diameters (200, 100 and 80 µm) were prepared on the YSZ thin films. A gold layer (400 nm thickness) was deposited on a chromium adhesion layer (20 nm thickness) by magnetron sputtering and was micro-patterned by UV lithography as described in the experimental methods part (chapter 2.3.7). Painted silver paste on the bottom of the silicon substrate served as counter electrode. Electrical properties of the resulting samples were measured by impedance spectroscopy in a frequency range from 1 Hz to 1 MHz with an amplitude of 1 V at temperatures between 200 °C and 450 °C. The impedance measurements were performed on a micro-measurement stage, which is described in the experimental methods part. Fitting and simulation of the impedance spectra by equivalent circuits was accomplished with ZView software.

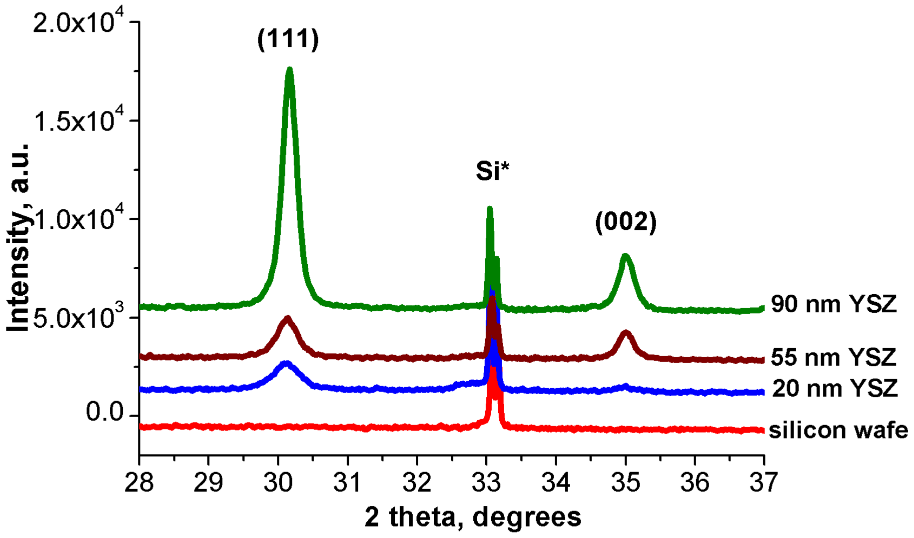

Figure 4.13. *XRD diffraction patterns of YSZ thin films with different thicknesses (*- indicates the peak which is an artifact of the silicon substrate)*

The XRD patterns (*Figure 4.13*) demonstrate the crystallinity and major orientation of the YSZ films synthesized onto the silicon substrate. Dominating (111) crystallite orientation of YSZ can be observed for the thinnest layer (20 nm) with an additional (002) orientation. According to the literature, the deposition parameters used in our case can be expected to lead to a columnar microstructure [3, 20 116]. The column size was estimated from AFM micrographs and values of approximately 30 nm resulted for all layers (*Figure 4.14a, c, e*). According to SEM cross section images

(*Figure 4.14 b, d, f*), the YSZ thin films exhibited thicknesses of 20 nm, 55 nm and 90 nm.

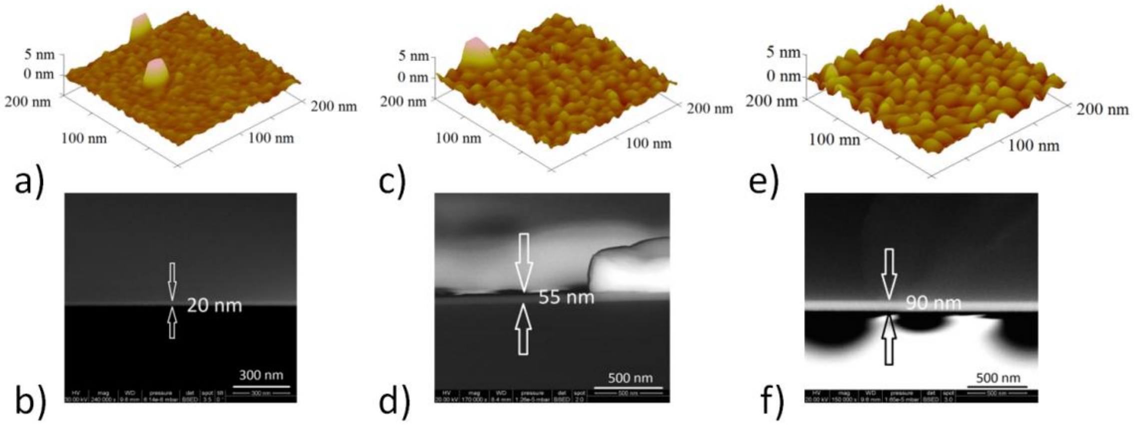

Figure 4.14. *AFM micrographs of PLD YSZ films with different thicknesses (a: 20 nm, c: 55 nm, e: 90 nm) and SEM backscattering images of the cross sections of these thin films (b, d and f)*

A sketch of the sample setup is shown in *Figure 4.15*. Typical impedance spectra in the complex impedance plane are given in *Figure 4.16 a*. A pronounced blocking effect is found in such across-plane conductivity measurements, particularly at lower temperatures. At higher temperatures, the spectra become more semicircle-like. It will be discussed in more detail below that this part of the impedance spectra can be ascribed to the silica interlayer. However, in addition to the silica impedance, a pronounced high frequency shoulder is also visible (*Figure 4.16 b*). This contribution can be attributed to the YSZ layer as will be proven below. These two features are even better visible and separable in the modulus (M) plot (*Figure 4.16 c*). Low temperature impedance measurements exhibit the beginning of a vertical line in the high frequency part of the modulus plot. This part of the spectrum, also visible as a high frequency intercept in the complex plane, could be observed for measurements up to 300 °C and reflects the serial resistance of the silicon substrate. The related features are also observed in the Bode plot of the phase angle (*Figure 4.16 d*).

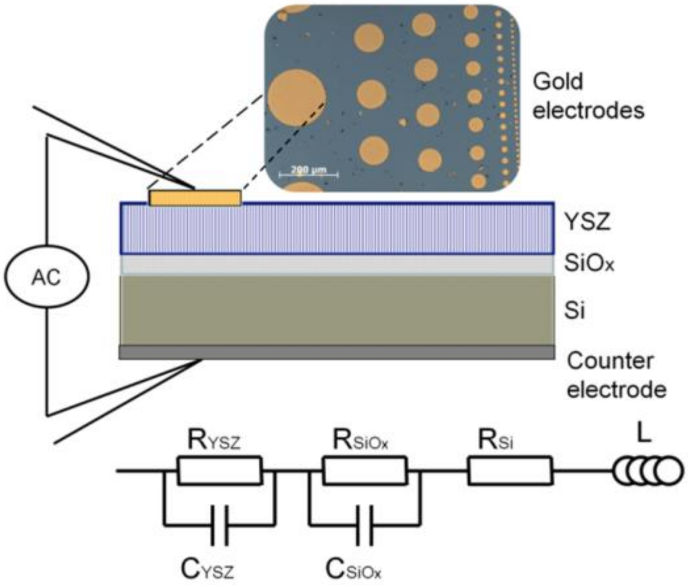

Figure 4.15. *Sketch indicating the sample set-up and the equivalent circuit used to quantify the impedance spectra*

In accordance with the theoretical considerations in Sec. 4.3, the equivalent circuit given in *Figure 4.15* is used to quantify impedance spectra of such across-plane measurements. One RC element (R_{YSZ}, C_{YSZ}) is attributed to the YSZ layer resistance and capacitance. A second serial RC element (R_{SiOx}, C_{SiOx}) describes the silica interlayer and a final serial resistor (R_{Si}) represents the electron conduction in the silicon substrate.

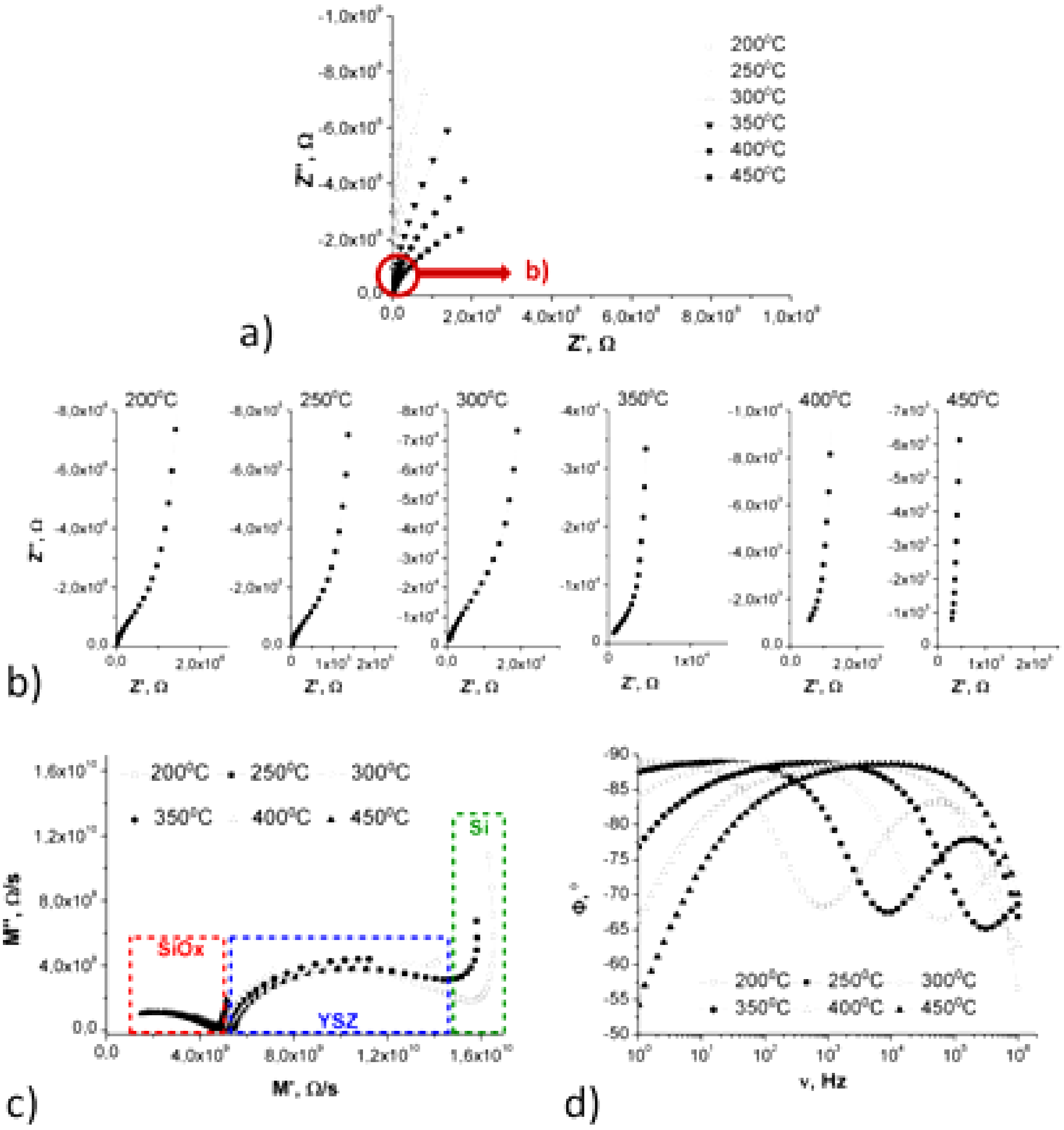

Figure 4.16. *Impedance spectra measured in the temperature range from 200 °C to 450 °C (frequency range: 1MHz – 1 Hz, electrode diameter: 200 µm, 90 nm YSZ films thickness). b) High frequency part of each impedance spectrum. c) Modulus plots. d) Bode plots of the phase angles*

The high frequency part of the low temperature spectrum is further affected by an inductance of the order of 10^{-5} H *Figure 4.16 c*, silicon part). This was described by a serial inductive element (*L*) and can be attributed to the electrical wiring. Additional contributions due to electrode effects are not required, most probably because electrodes only affect the results at frequencies lower than those used here. Non-idealities were taken into account by using constant phase elements (CPE) instead of capacitances in the equivalent circuit. The suggested model fits to all experimental data of this study and in the following we discuss the appropriateness of the interpretation of all the circuit elements.

The conductivity values of the silicon substrate σ_{Si} were evaluated from R_{Si} according to the spreading resistance formula [97, 114]

$$R_{Si} = \frac{1}{2d_{me}\sigma_{Si}} \qquad \textbf{(Eq. 4.6)}$$

where d_{me} is the diameter of the gold microelectrodes. The temperature (T) dependent conductivity values are represented in an Arrhenius plot (*Figure 4.17*). Despite some variations between the different samples, the resulting conductivity is in reasonable agreement with the conductivity of intrinsic silicon, which was calculated from $\sigma = 1/(A\cdot exp(E_a/2\cdot k\cdot T))$ [117], where A is a constant ($1.1\cdot10^{-4}$ Ω·cm) and E_a the activation energy (1.12 eV), see *Figure 4.17*. Deviations may partly originate from the fact that at most a few experimental points in the impedance spectra represent the serial silicon resistor. Extrapolation is required, particularly at high temperatures and fitting errors become so large that above 300 °C the serial resistor was not further used in the equivalent circuit when fitting the measured data.

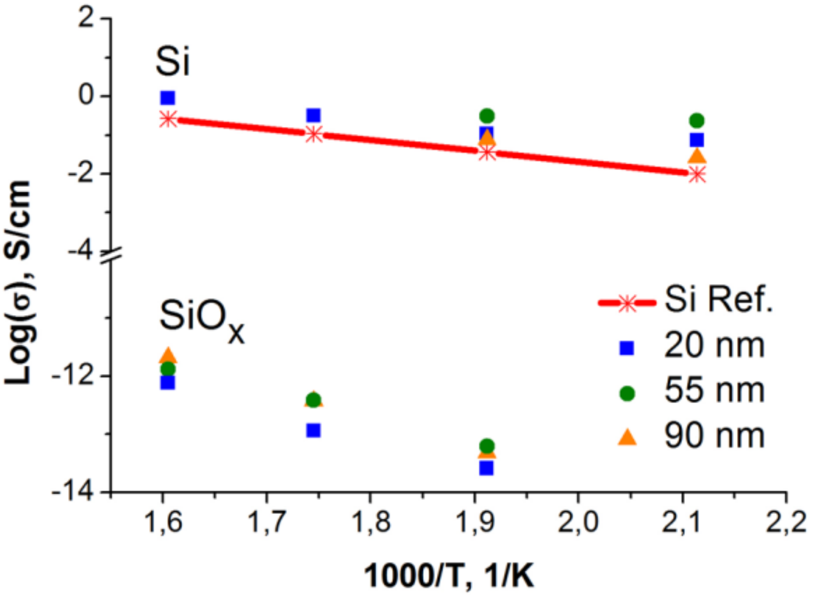

Figure 4.17. *Arrhenius plot of conductivities of silicon and silica determined from the across-plane measurements with varying YSZ film thickness (20, 55, 90 nm) (electrode diameter of 200 µm)*

The low frequency RC element is attributed to the silica interlayer. Silica is well known as an insulating material with a very large band gap and some residual ionic conductivity at higher temperatures, which often can be attributed to sodium impurities [118]. At temperatures below 300 °C the resistance becomes so high that its determination was not possible from the available impedance data and in the equivalent circuit the silica layer was represented by a capacitor only. The resulting conductivity of silica is shown in *Figure 4.17*. From the constant phase elements with impedance $(i\cdot\omega)^n\cdot Q^{-1}$ replacing the capacitors in *Figure 4.15*, the capacitance was evaluated by the equation (*Eq. 4.1*). The parameter *n* was very close to 1, which indicates an almost ideal capacitance. The thickness t_{SiOx} of the silica layer was estimated from the capacitance and the relative permittivity ε_r (dielectric constant for thermally grown silica – 3.8 [118]) according to:

$$t_{SiOx} = \frac{\varepsilon_r \varepsilon_0 A}{C_{SiOx}} \qquad \textbf{(Eq. 4.7)}$$

where ε_0 denotes the vacuum permittivity and A is the area of the electrode. Thickness values between 4 nm and 7 nm resulted (*Table 4.7*), which is very reasonable for thermally grown silica. The constant capacitance values of C_{SiOx} over the whole measured temperature range and its little dependence on the YSZ layer thickness (*Table 4.7*) are further arguments for the correctness of the proposed equivalent circuit.

Table 4.7. *Capacitance values of YSZ and silica layers measured with different electrode diameters and for several YSZ film thicknesses, and thickness values of silica calculated from C_{SiOx} and (Eq. 4.7)*

Electrode diameter, µm *(YSZ thickness: 90 nm)*	***C_{YSZ}, pF***	***C_{SiOx}, pF***	***t_{SiOx}, nm***	**YSZ layer thickness, nm** *(electrode diameter: 200 µm)*	***C_{YSZ}, pF***	***C_{SiOx}, pF***	***t_{SiOx}, nm***
80	25	43	4	**20**	530	157	7
100	39	64	4	**55**	290	190	6
200	160	260	4	**90**	160	260	4

Accordingly, the high frequency shoulder visible up to 400 °C can indeed be attributed to the YSZ layer and the corresponding conductivity will be analyzed in the following. The conductivity values σ_{YSZ} were evaluated from R_{YSZ} according to

$$\sigma_{YSZ} = \frac{4t_{YSZ}}{\pi d_{me}^{2} R_{YSZ}} \qquad \textbf{(Eq. 4.8)}$$

Conductivity values of layers with different thickness t_{YSZ} are plotted in an Arrhenius diagram (*Figure 4.18*). For comparison, conductivity data of a polycrystalline YSZ sample were measured in a conventional macroscopic measurement set-up and the bulk conductivity is also plotted in *Figure 4.18*. One can see that across-plane conductivities of all three films are very similar. The nominal activation energies of the conductivity slightly increase with the thickness of the layer (20 nm – 0.90 eV, 55 nm – 0.95 eV, 90 nm – 0.98 eV) but this might also be an artifact due to the limited number of data points representing the shoulder.

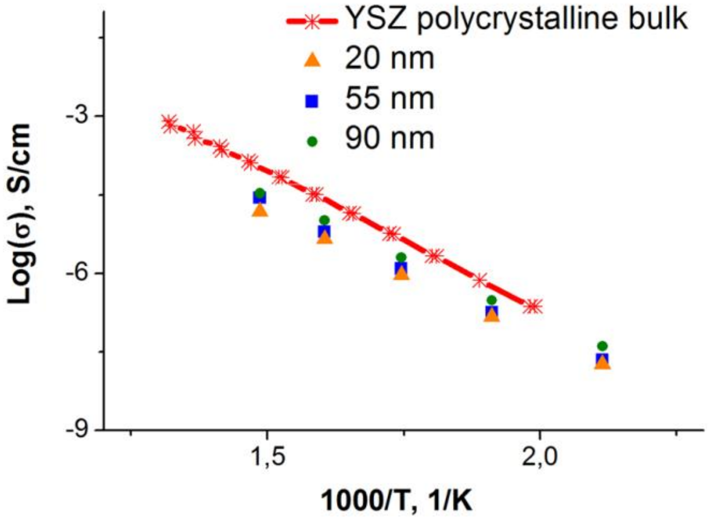

Figure 4.18. *Arrhenius plots of the conductivities of YSZ determined from across-plane measurements on films with varying YSZ thickness (electrode diameter of 200 µm)*

Conductivity values of thin YSZ layers are slightly lower than those of the polycrystalline samples. However, it may easily be that this deviation is mainly caused by some differences between the true film temperature and the set temperature of the heating table used in this study [119]. Hence, we conclude that the across-plane bulk conductivity of the YSZ layers on Si/SiO$_x$ does at least not significantly deviate from the bulk conductivity of macroscopic samples even for films as thin as 20 nm. A statement on grain boundary contributions is not possible. Those are not expected in across-plane measurements on columnar films anyway, but if present, they were mimicked by the RC element of silica dominating the entire low frequency range. This is illustrated in *Figure 4.19*: Exemplarily, we consider the existence of a hypothetical single grain boundary plane in parallel to the YSZ / substrate interface, i.e. an effective across-plane grain size of 27.5 nm for a 55 nm thin YSZ film. This grain boundary plane is assumed to exhibit the conductivity and thickness of the grain boundaries analyzed in the in-plane study on similar YSZ films on sapphire substrates [111]. Hence, they are about two orders of magnitude less conductive than the YSZ bulk. *Figure 4.19* displays impedance data measured in our across-plane study. In addition, it shows impedance data calculated from the fit results including a grain boundary impedance plane with the properties mentioned above (area specific resistance and capacitance values of 1.7 $\Omega\cdot\text{cm}^2$ and 27 $\mu\text{F/cm}^2$, respectively). Obviously, this does not change the impedance spectrum, neither in the Nyquist plot nor in the modulus and Bode (phase) plot. However, this is only because the corresponding grain boundary response is mimicked by the silica impedance. Grain boundary effects become clearly visible when plotting the impedance data of YSZ only (grain and hypothetical grain boundary plane), that is without silica. Equivalent circuits of the two simulated data sets with and without silica are given in *Figure 4.19*.

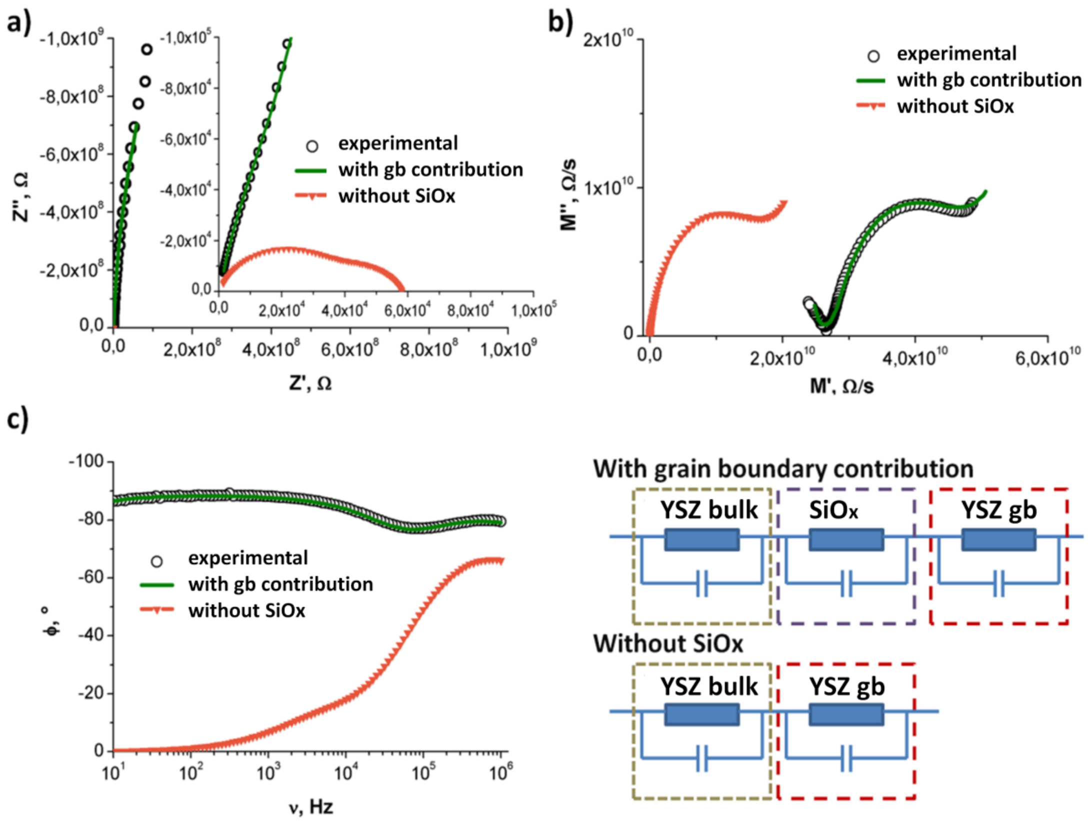

Figure 4.19. *Impedance data measured on a 55 nm YSZ layer at 300 °C by means of a 100 µm microelectrode in a) Nyquist, b) modulus and c) Bode (phase) plots and simulated data sets described by the equivalent circuits on the r.h.s. In addition to the experimental results (circles), the case including a hypothetical grain boundary plane (green line) and a calculated spectrum with the grain boundary plane but without the silica layer is shown (orange triangles). Constant phase elements rather than capacitances are used for YSZ bulk and grain boundary with exponents of n=0.8 and* $Q=1.55\cdot10^{-8}\ s^{n}/(\Omega\cdot cm^{2})$ *respectively*

The capacitance of the YSZ layers was estimated from the fit data of the constant phase element according to (*Eq. 4.1*), *n*-values were about 0.8. The calculated capacitance values for different circular electrode diameter (80 µm, 100 µm and 200 µm) are given in *Table 4.7*. The capacitances correlate well with the area of the electrodes. Moreover, the capacitances are inversely proportional to the YSZ layer thickness. The averaged relative dielectric constant ε_{YSZ} for 20 nm layers is 30 and for thicker layers 50 is found. This is in acceptable agreement with the value of 40 determined from our measurements on the polycrystalline sample. The literature dielectric constant values vary for YSZ thin films from one publication to another and are in the range of 15 to 27 [120, 121]. Hence, all data support that across-plane measurements of very thin YSZ layers are indeed possible using microelectrodes and thin insulating interlayers between conducting substrate and thin films.

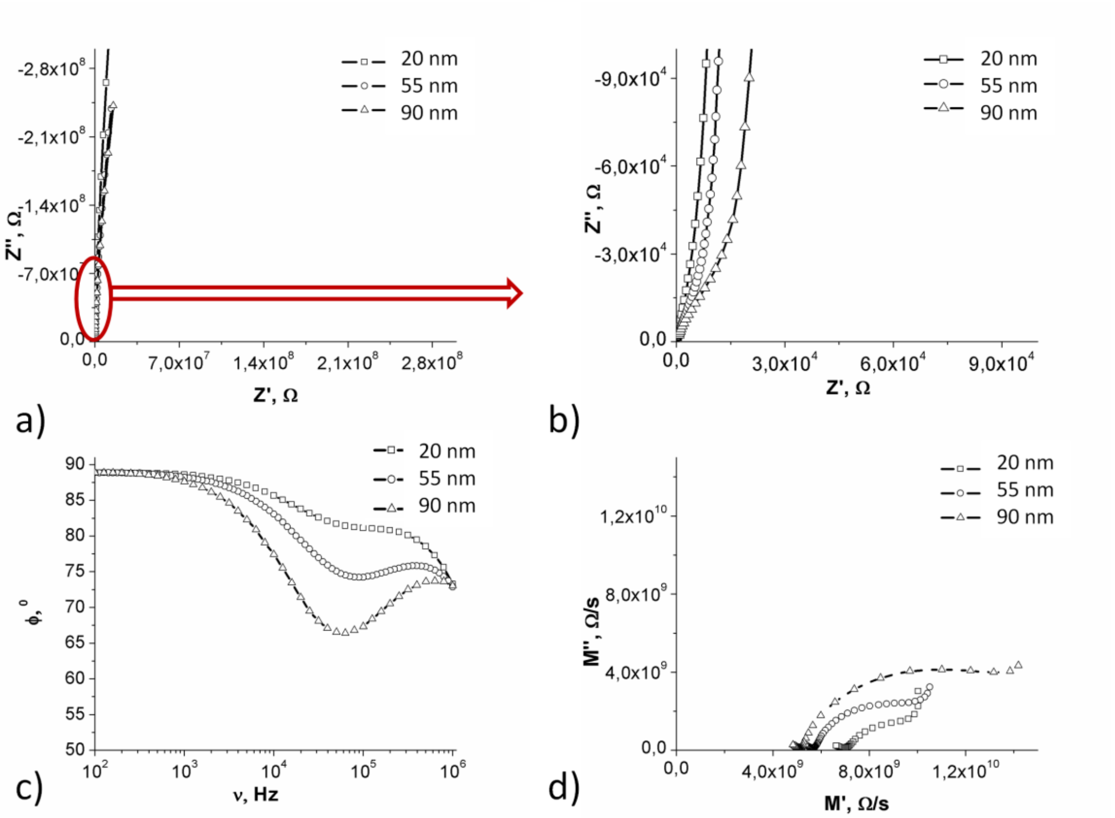

Figure 4.20. *Impedance spectra measured on YSZ films of different thickness (frequency range: 1MHz – 1 Hz, electrode diameter: 200 µm, measurement temperature: 300 °C). b) High frequency part of each impedance spectrum. c) Bode plots of the phase angles. d) Modulus plots*

It is finally worth discussing the requirements for successful measurements in terms of YSZ and silica thickness, or more general, in terms of the capacitance ratios of the insulating layers and the ion conducting layer. Some simulations using ideal RC elements were already presented in Sec. 3.5. Measured impedance spectra of YSZ layers with different thicknesses are shown in *Figure 4.20* as Nyquist (Z), Bode (phase angle) and modulus plots. Obviously, visibility of the shoulder in the Nyquist plot and separability of the YSZ arc in the modulus plot becomes worse, the thinner the YSZ layer. In order to estimate the range for which a separation and thus determination of across-plane conductivities becomes possible, some further impedance simulations were performed. In these simulations the equivalent circuit in *Figure 4.15* was used and only the values of the silica RC element were changed. The values of the other equivalent circuit elements were taken from an experimental data fit (t_{YSZ}=55nm, T=300 °C, 200 µm electrode) and kept constant. For an estimation of the separability the following thickness ratios were considered

$$\frac{t_{SiOx}}{t_{YSZ}} = \frac{2}{55}; \frac{6}{55}; \frac{12}{55}; \frac{36}{55}. \qquad \textbf{(Eq. 4.9)}$$

For the ratio of 6/55, experimental data are shown. The impedance spectra for the other ratios were obtained by varying the silica resistance and capacitance in accordance with the thickness (*Figure 4.21*). A clear separability is given for ratios of 2/55 and 6/55. YSZ is seen as a pronounced shoulder in the Nyquist plot and as a peak in the phase angle Bode plot. High experimental data quality may still allow a separation for a ratio of 12/55. However, samples with very thick silica interlayer ($t_{SiOx}/t_{YSZ} \rightarrow 1$) cannot be investigated in this manner.

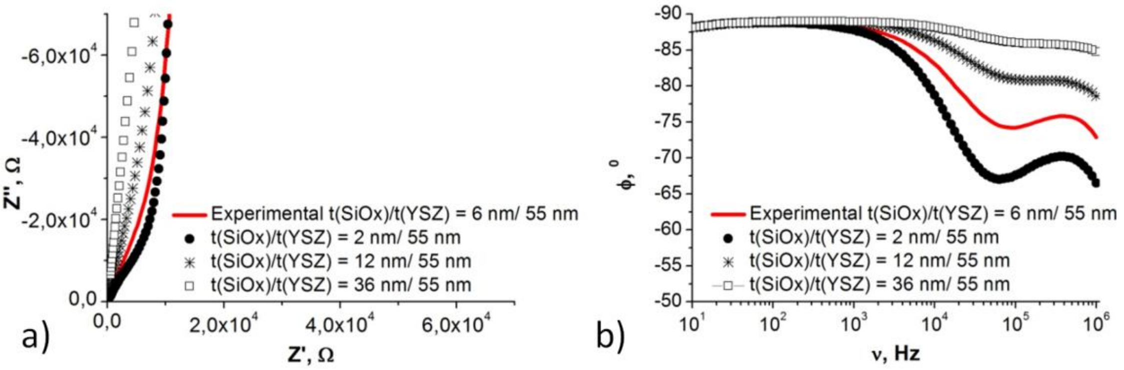

Figure 4.21. *Experimental and simulated high frequency part of Nyquist plots (a) and Bode (b) plots for varying silica layer thickness and constant parameters of the YSZ layer (t_{YSZ}=55 nm, T=300 °C, d_{me} = 200 µm)*

An increased range of YSZ thickness might become accessible if the insulating layer had a higher dielectric constant, e.g. for alumina ε_{Al2O3} ~14 [122], yttrium oxide ε_{Y2O3} ~16 [123], or zirconia ε_{ZrO2} ~22 [122]. This is exemplified in *Figure 4.22* by simulated impedance spectra. An experimental proof is discussed in more detail in the thesis part 4.3.2 (“The interlayer effect for conductivity measurements”).

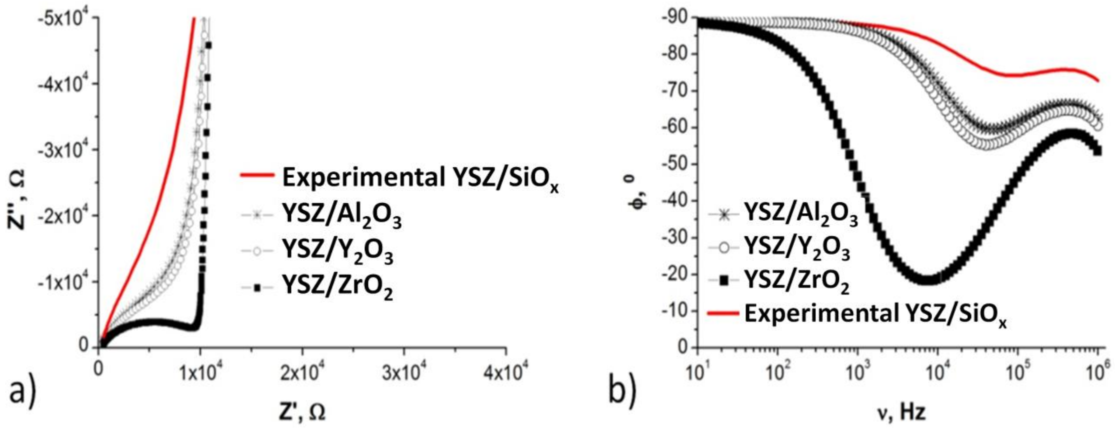

Figure 4.22. *Experimental and simulated high frequency part of Nyquist plots (a) and Bode plots (b) for varying dielectric interlayer material (SiO$_x$: experimental data for t_{YSZ}/t_{SiOx} = 55nm/6nm, T = 300 °C, Al$_2$O$_3$, Y$_2$O$_3$ and ZrO$_2$)*

4.2.2 The effect of the thin film microstructure on the across-plane conductivity

In this thesis part, the effect of the microstructure on the YSZ across-plane conductivity was checked on samples, prepared by three different procedures. The different preparation methods should lead to a different microstructure of the layers. The PLD layers, as it was discussed in the previous chapters, should exhibit a columnar structure, hence the measurements of across-plane conductivity should represent only the bulk conductivity. As it was discussed in the literature overview part the grain boundaries in YSZ case are highly resistive, thus leading to most of the current flowing through the grain bulk (*Figure 4.23*).

The sol-gel layers may have a polycrystalline structure, which changes the flow of the current. In this case the current has to flow across the grain boundaries (*Figure 4.23*). Hence, the measured conductivity consists of bulk and grain boundary components. As it was demonstrated theoretically in the previous section, the contribution of grain boundaries is not detectable in impedance spectra, due to the large capacitance of silica. All YSZ layers were prepared on silicon substrates, as in the cases already presented. It was expected that the silica interlayer thickness also may change due to the different preparation route - annealing the sol-gel layers at high temperature should lead to a thicker silica interlayer.

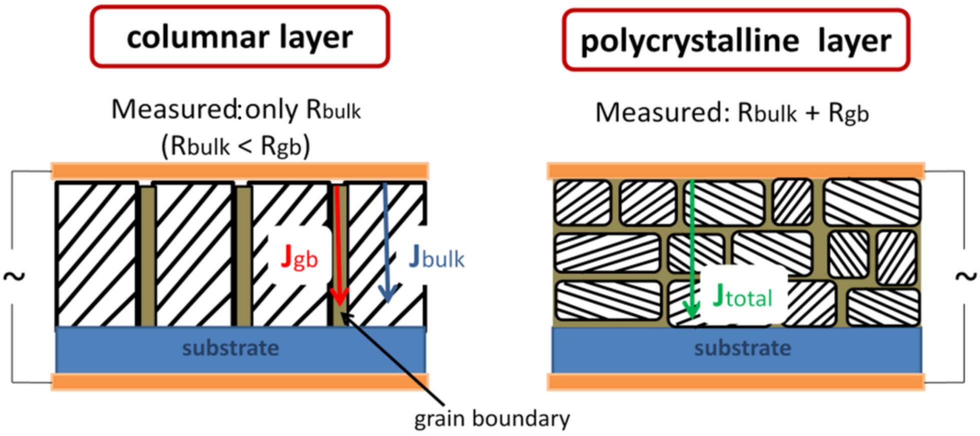

Figure 4.23. *Measurement sketch of the across-plane conductivity of YSZ thin films with different microstructure*

One of the YSZ layers (S3) was deposited by the PLD method onto silicon (100) substrate, which was heated to a temperature of 600 °C (measured by an IR pyrometer). The other deposition parameters are defined in the methods part.

Another YSZ layer (S2) was prepared by a sol-gel method, which is described in the methods part as sol gel synthesis route B. After the synthesis layer was dried at room temperature, and afterwards annealed at 100 °C for 2 minutes each. The calcination was done at 500 °C for 10 minutes. Finally, the layer was sintered for 12 hours at 1200 °C with 10 °C/min heating and cooling rate. The thickness of the layer was determined by ellipsometry and by Rutherford backscattering (RBS) measurement. The RBS analysis was performed with the PSI/ETH Tandem accelerator. The thickness and chemical layer composition of YSZ and silica layers was measured by 5 MeV ^{4}He RBS. The crystallography of the synthesized layers was determined by X-ray diffraction (XRD) performed on a Philips X'Pert (Cu anode, λ = 1.54Å) diffractometer. The surface topography was checked by atomic force microscopy (AFM).

A third layer (S1) was prepared by the sol-gel technique described in the methods part as sol-gel method A. The synthesis of the YSZ layer was done in the Chemistry Department of Vilnius University. X-ray diffraction analysis was carried out with CuKα radiation on a Bruker AXS GmbH diffractometer with standard Bragg-Brentano focusing geometry. The surface morphology of YSZ samples was characterized by scanning electron microscopy. The thickness of the layers was defined from a cross-section image made by SEM. The preparation routes of all samples are listed in *Table 4.8.*

Table 4.8. *List of the samples*

Sample	**Preparation route**
S1	Sol-gel preparation route A (described in methods part)
S2	Sol-gel preparation route B (described in methods part)
S3	Pulsed laser deposition

The electrical characterization of the samples was done with rectangular shaped electrodes (400 µm x 1000 µm and 50 µm x 1500 µm) prepared by UV lithography as described in the experimental methods part. The counter electrode was prepared by painting silver paste to the bottom side of the silicon substrate. The ionic conductivity of synthesized layers was measured by two probe impedance spectroscopy in a temperature range from 200 to 450 °C in ambient air. The impedance spectra were obtained in the frequency range 1 Hz - 1 MHz using an impedance analyzer. The sample was measured with a micro measurement stage which is described in the experimental methods part. The fitting of impedance spectra was done with the equivalent circuit model described in the previous chapter (*Figure 4.15*).

The XRD patterns of all three samples are shown in *Figure 4.24*. The diffraction patterns of all three layers demonstrate YSZ cubic structure. An average crystallite size was determined from the broadening of the peaks. The average crystallite size for PLD sample S3 and sol-gel sample S2 amounts to 38 nm and 44 nm respectively. The average crystallite size of sol-gel sample S1 was found to be 34 nm.

From the diffraction patterns also a slight shift of the peak of crystallographic orientation (111) was observed. The peak in both diffractograms of sol-gel layers was slightly shifted towards lower diffraction angle (*Figure 4.24* magnified part), which corresponds to an increased lattice parameter. The lattice parameters were calculated to 5.092 Å for PLD layer (S3), 5.125 Å for sol-gel layer (S2) and 5.134 Å for sol-gel layer (S1). The difference in the lattice parameter may be due to the crystallization, since both sol-gel layers (S2 and S1) were annealed (S1 at 800 °C and S2 at 1200 °C), in contrast to the PLD layer. This effect was also observed in other studies.

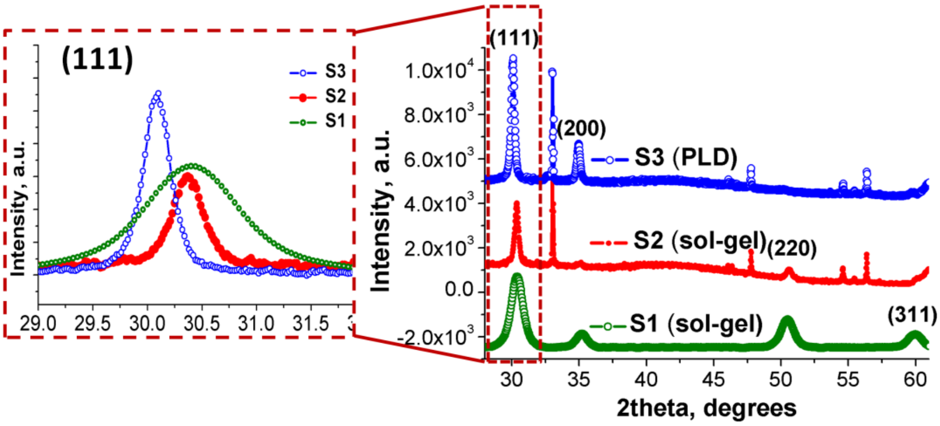

Figure 4.24. *The diffractograms of YSZ layers prepared by different methods: S1- sol-gel layer (preparation route A), S2 - sol-gel layer (preparation route B) and S3 - PLD layer*

The XRD diffractograms of sample S2 and S3 (*Figure 4.24*) demonstrate that both layers have highly pronounced (111) orientation. However both of the layers also exhibit other orientations ((200), (311), (220)) but the intensity of the peaks is very low. The XRD pattern of sample S1 demonstrates a polycrystalline like structure, since all possible orientations of the cubic structure are present. The texture coefficient of the layers was estimated from:

$$TC_{(hkl)} = \frac{\frac{I_{(hkl)}}{I^0_{(hkl)}}}{\frac{1}{N}\sum_N \frac{I_{(hkl)}}{I^0_{(hkl)}}} \qquad \textbf{(Eq. 4.10)}$$

where $I_{(hkl)}$ – measured intensities, $I^0_{(hkl)}$ – intensities from reference (PDF file No. 82-1246). The ratios of measured and reference intensities and the estimated texture coefficients for the corresponding crystallographic planes are listed in *Table 4.9*.

Table 4.9. *The texture coefficients (TC) for all samples*

(hkl)	**S1**		**S2**		**S3**	
	I/I_0	**TC**	**I/I_0**	**TC**	**I/I_0**	**TC**
(111)	3.08	0.94	3.63	1.78	4.92	1.29
(200)	4.83	1.48	1.10	0.54	9.54	2.50
(220)	2.88	0.88	2.24	1.10	0.18	0.05
(311)	2.29	0.69	1.18	0.58	0.65	0.17

Form texture coefficients one can conclude that the YSZ layer prepared by the PLD method (S3) has a preferential orientation (200). Sol-gel layer S2 has dominating (111) orientation and layer S1 has (200) more pronounced.

The surface topography of samples S2 and S3 was checked by AFM, which is shown in *Figure 4.25*. One can see from the AFM images that sol-gel layers exhibit higher roughness. This could be a result of annealing, which leads to a coarsening of the grains.

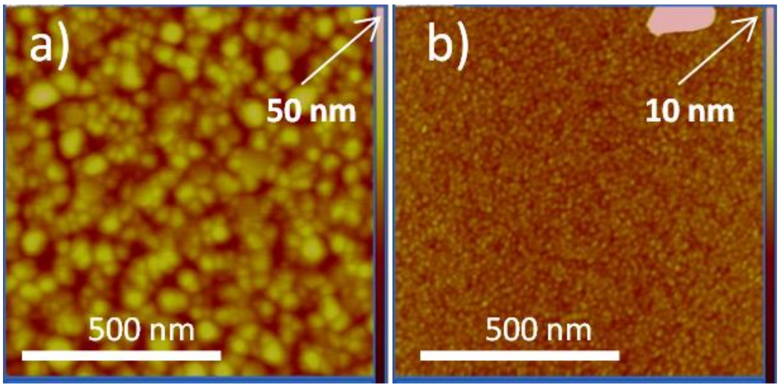

Figure 4.25. *AFM images of YSZ layers prepared by a) sol-gel (S2) and b) PLD methods*

The thickness of S2 and S3 layers was determined from RBS measurements (*Figure 4.26*). The determined thickness for samples S3 and S2 were 66 nm and 85 nm, respectively. The chemical composition was also determined from RBS measurements. Nominal values suggest increase of the oxygen content in sol-gel layer (S2) while the PLD layer has the expected stoichiometric amount of oxygen for YSZ 8mol% (*Figure 4.26*). The nominally increased oxygen content of the sol-gel layer could be due to fitting errors of RBS spectra. There is an apparent difference between RBS spectra of S2 and S3 layers – the contribution of silica. For the PLD layer the silica layer was not detected in RBS spectra, although it exists as it was confirmed from the previous impedance measurements. For the sol-gel layer a silica interlayer was detected in the RBS spectrum and from fitting a thickness of 164 nm was found. During annealing of the layers oxygen tends to diffuse through the YSZ layer, which leads to a thermal growth of the silica interlayer. The roughness of the sol-gel layer was also determined from the peak tails of RBS spectra. The roughness for S3 was not detectable.

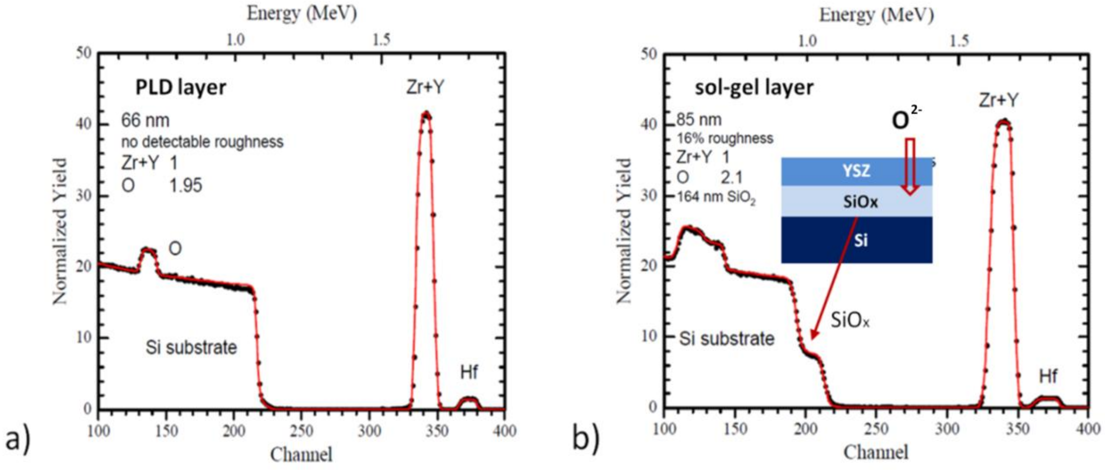

Figure 4.26. *RBS measurement results of YSZ layers prepared on silicon wafers by a) pulsed laser deposition (S3) and b) sol-gel method (S2)*

The thickness of layer S1 was defined from SEM cross-section image (*Figure 4.27*) and resulted in 120 ±5 nm.

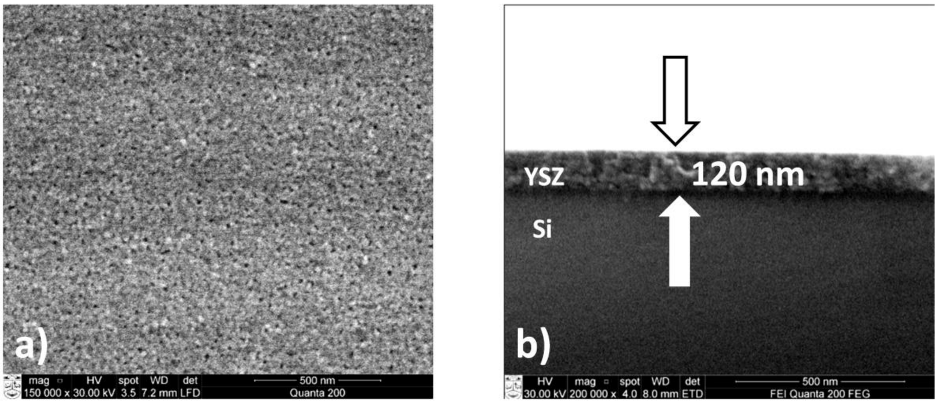

Figure 4.27. *a) SEM image of YSZ layer (S1) surface topography; b) the cross-sectional image of YSZ layer demonstrates isotropic microstructure [82]*

The ionic conductivity of the layers was measured by two probe impedance spectroscopy with across-plane geometry in a temperature range from 200 to 450 °C. Some impedance spectra measured on layer S1 are presented in *Figure 4.28*. Low temperature measurements demonstrate blocking capacitance behaviour in the Nyquist plot (*Figure 4.28*) which is caused by the silica layer. This contribution appears in the low frequency part of impedance spectra, while a pronounced shoulder is visible in the high frequency range. This part of the spectrum can be attributed to the YSZ layer in accordance with the proof given in the previous chapter. The impedance spectra were fitted with the equivalent circuit *Figure 4.15* which was discussed in theoretical consideration part and also applied in Sec. 4.2.1.

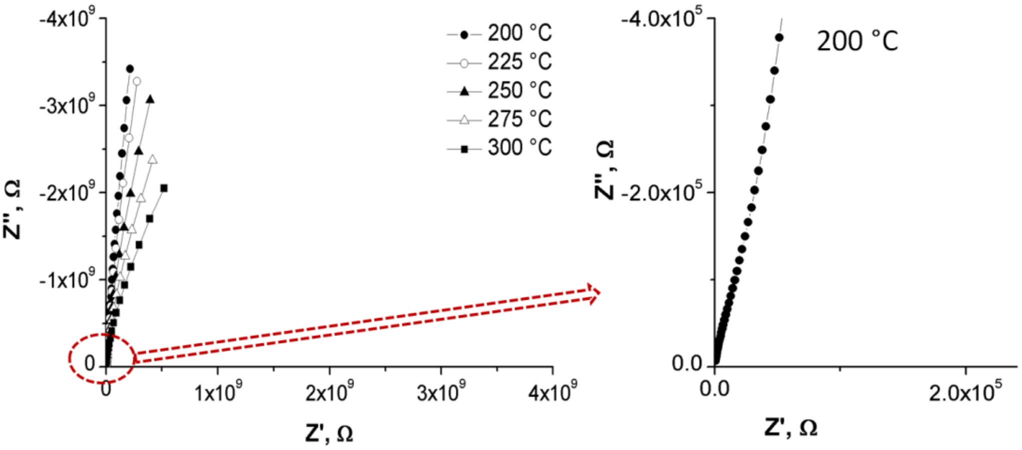

Figure 4.28. *Nyquist graphs of across-plane measurements with a magnified high frequency part of sol-gel layer (S1)*

The same impedance measurement procedure was applied for S2 and S3 samples. Impedance measurements of YSZ layer prepared by PLD (S3) also resulted in a high frequency shoulder in a Nyquist graph. Impedance measurements of sol-gel layer (S2), which was annealed at high temperatures was more problematic in terms of YSZ layer analysis. Annealing of the layer at high temperatures leads to growth of the silica layer, as it was demonstrated from RBS measurement. The large thickness of the silica interlayer hinders probing of the across-plane conductivity of the YSZ layer. The Nyquist plot for S2 sample is shown in *Figure 4.29 a*. The high frequency part does not exhibit any shoulder and it is obvious that it does not change with the temperature. The resistivity of silica is much higher than that of the YSZ layer and this makes the YSZ part in the impedance spectrum inseparable. However, in the modulus plot it is still possible to detect two capacitances (*Figure 4.29 b*). One of them is referred to YSZ and the other to silica. The modulus plot was fitted with the standard equivalent circuit for the across-plane measurement.

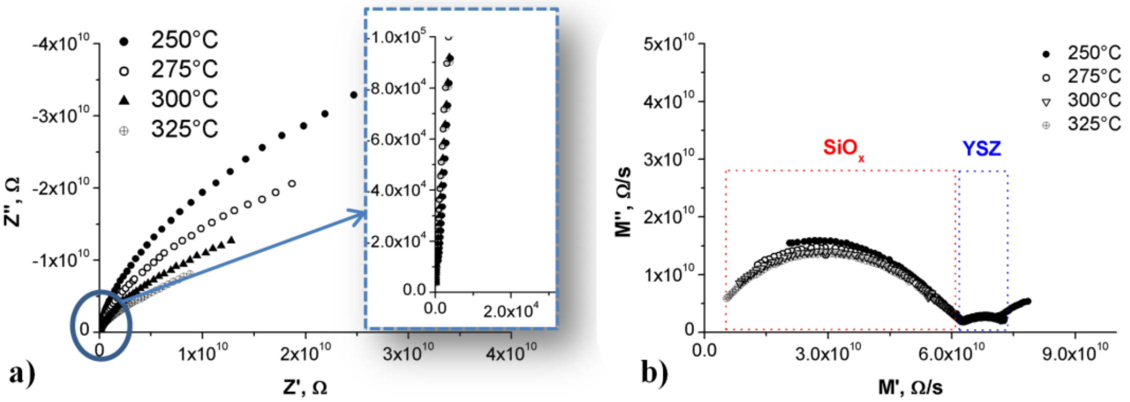

Figure 4.29. *Nyquist (a) and modulus (b) plots of YSZ sol-gel layer (S2)*

The conductivity of the layers was determined from (*Eq. 4.8*). The conductivity dependence versus temperature for sample S1 is presented in the Arrhenius plot (*Figure 4.30*). For reasons of comparison, the bulk conductivity of a YSZ pellet is also included in the Arrhenius plot (*Figure 4.30*). Conductivity values of all three thin YSZ layers are similar and slightly lower than those of the polycrystalline sample. The activation energies were estimated from linear fits of Arrhenius graphs. The activation energy for the across-plane conductivity of sample S1 was 0.9 eV, for S2 and S3 it was 0.87 and 1eV respectively.

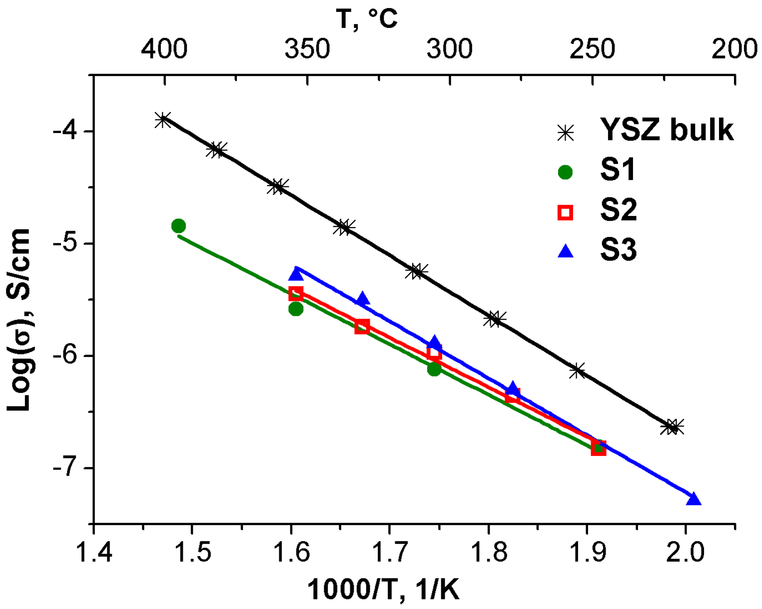

Figure 4.30. *Arrhenius plot of sol-gel (S1 and S2) and PLD (S3) layers*

In conclusion, the ionic conductivity and conductivity activation energies for all the layers independent on the preparation route differ only slightly and were also similar to that of YSZ bulk. That latter difference may be partly due to the inaccurate temperature measurement in the micro probe station. For across-plane measurements grain boundaries do not contribute significantly to the obtained conductivity. However, even if grain boundaries were present, they would not contribute to the high frequency arc. This was shown in the theoretical considerations. The corresponding grain boundary response is mimicked by the silica impedance.

The effect of the silica interlayer thickness for across-plane impedance measurements is another important outcome of this study. It was proven that across-plane conductivity measurements are indeed possible, even though the silica interlayer is thicker than the YSZ layer. Due to the huge silica resistance the YSZ layer contribution is no longer detectable in Nyquist graph but the modulus graphs can still separate the contributions.

4.3 In- and across plane conductivity of YSZ layers obtained from a single impedance spectrum

4.3.1 In-plane impedance measurements of YSZ thin films deposited on silicon substrates

For this study YSZ thin films were prepared by pulsed laser deposition (PLD) on silicon (100) substrates. The PLD parameters are described in the methods part of the thesis. The thickness of the YSZ layers on the silicon substrates was determined from cross-section images obtained by scanning electron microscopy. The crystal structure of the synthesized YSZ films was analyzed by X-ray diffraction (XRD). Electrical properties of the samples were investigated by impedance spectroscopy in a frequency range from 100 mHz to 1 MHz (1 V amplitude) and for temperatures from 200 °C to 500 °C set temperature. Impedance spectra were measured between two stripe–shaped gold electrodes with a distance of 25 µm, 50 µm or 75 µm (10 µm width, 450 µm or 900 µm lengths). The electrodes were formed by UV lithography described in the methods part. For electrical characterization, samples were positioned on a micro-probe station. An additional shielding (*Figure 4.31*) was used to avoid “inductive loops” at low frequencies, which often appear in such measurements [124, 125]. The additional shielding lead to a temperature difference of about 30 °C between set temperature and film temperature; this was estimated from the across-plane measurement with and without shielding. In the following, all temperature values refer to the (estimated) true film temperatures. For contacting the stripe electrodes, tungsten needles (tip diameter 1 µm) were used. Fitting of the impedance spectra was accomplished by ZView software.

The following novel measurement approach allows analysis of the in-plane and across-plane conductivity of an ion conducting thin film from a single impedance spectrum. A sketch of the measurement set-up is shown in *Figure 4.31 a*: A thin film is deposited on a conducting Si substrate covered by a very thin insulating silica (SiO_x) interlayer. Two close-distant stripe electrodes on the thin film are used to measure the impedance spectrum of the sample. The impedance of the silica layer is extremely frequency dependent with very low impedance values at high frequencies and almost insulating behavior at low frequencies. Hence, a strongly frequency dependent current flow has to result as this was demonstrated in the theoretical part. It is indicated in *Figure 4.31 a* that for high frequencies the current can flow across-plane through the YSZ and the silica layer in the conducting silicon substrate. For low frequencies, however, the impedance of the silica layer becomes so high that current has to flow along the YSZ layer (in-plane) from one stripe electrode to the other. As a prerequisite, the in-plane resistance of the YSZ film has to be much smaller than the residual across-plane resistance of silica due to some ion conduction [112, 118]. Hence, preferably narrow stripe electrodes with a small distance should be used to enforce these frequency dependence of the current lines.

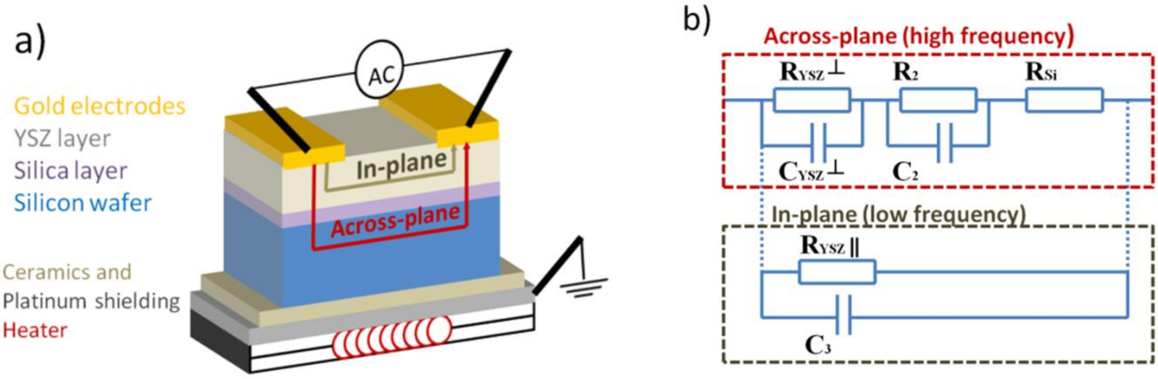

Figure 4.31. *Sketch of the sample with expected current paths (a) and suggested equivalent circuit (b) reflecting the frequency dependent current lines of in- and across-plane measurement on YSZ thin films deposited on a silicon wafer with a native silica layer. In a real fit constant phase elements instead of the capacitances were used in the equivalent circuit*

In accordance with the theoretical considerations, the current flow can thus be approximated by the frequency dependent equivalent circuit model in *Figure 4.31 b*: For high frequencies, the across-plane current flow is described by an RC element for YSZ ($R_{YSZ}\perp$, $C_{YSZ}\perp$), the serial capacitance of the silica layer (C_{SiOx}) and a small resistor R_{Si} reflecting the Si substrate. The elements of YSZ and silica have to consider that these layers are passed twice by the current (see *Figure 4.31 a*). With decreasing frequency, the current lines tend to flip, as this has been demonstrated in the theoretical part (*Figure 3.11*). However, to a first approximation (and within a certain frequency range) we may represent the on-set of "flipping" current lines by an additional RC element (R_{fr}, C_{fr}) [125] in parallel to the silica capacitor. Accordingly, a serial RC element (R_2=R_{fr}, C_2=C_{fr}+C_{SiOx}) instead of only C_{SiOx} is assumed to complete the high frequency equivalent circuit. The experiments on YSZ polycrystals showed that the capacitor of YSZ should be replaced by a constant phase element Q. Moreover, grain boundaries in YSZ may add an additional RC (RQ) element but PLD layers of columnar structure often do not exhibit serial grain boundaries in the across-plane current flow. Hence, this additional grain boundary contribution is not considered here.

The intermediate frequency range with "flipping" of the current lines may lead to some complexity in the spectrum and is not in our focus. In the low frequency range, however, the spectrum is expected to again correspond to an RC element with the resistor now representing the in-plane current flow in YSZ ($R_{YSZ\,||}$). The capacitor (C_3) may include effects from stray capacitances, the in-plane grain boundary capacitance of YSZ and possibly also unknown contributions from the current line flipping. Also the theoretical considerations showed that this capacitance has no simple meaning. Electrode impedances are neglected in the frequency range under investigation. Hence, in a certain (low) frequency range a single RC element (or, more general, an RQ element) should be appropriate to quantify the frequency dependence of the experimental impedance data.

From these basic considerations we see that it should be possible to analyze the across-plane as well as in-plane ion conduction in a YSZ thin film by varying the frequency, thus probing the one at high frequencies and the other at low frequencies. It should be emphasized that "high" and "low" frequencies are relative statements and depend on temperature. For low temperatures and thus large resistances, the low frequency current path can easily be out of the typical measurement range. The same is true for the high frequency path at high temperatures. In the following it is shown that this simplified picture in terms of limiting equivalent circuits indeed approximates the results and that across-plane and in-plane conductivities of YSZ can be determined from the spectrum.

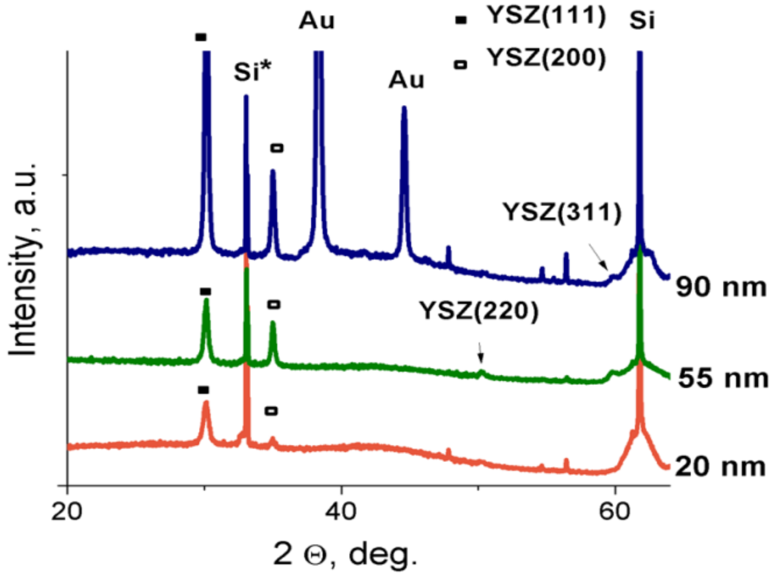

Figure 4.32. *XRD diffraction patterns of YSZ thin films of different thickness on silicon substrates (sample was measured with the gold electrodes on top of the YSZ layer) (*- the first silicon peak is a λ/2 peak).*

Thicknesses of YSZ layers on silicon substrates were determined from SEM BS cross-section images and yielded values of approximately 20 nm, 55 nm and 90 nm. The XRD patterns demonstrate that crystalline YSZ films resulted (Figure 4.32). A dominating (111) orientation of YSZ can be observed in the thinnest layer (20 nm) with an additional YSZ (100) orientation. Thicker layers (55 nm and 90 nm) exhibit both YSZ (111) and YSZ (100) crystallite orientations and in addition to that also contain other crystallite orientations like YSZ (110) or YSZ (311). The lattice parameters *a* of the layers calculated from a fitting by fundamental parameter algorithm and are 5.149 Å for all layers. According to literature [3, 127], the deposition parameters used in this study can be expected to lead to a columnar microstructure.

The impedance measurements were firstly done with the measurement set-up shown in *Figure 4.31* without the shielding of a heater. Impedance measurements with two close-distant stripe electrodes on the thin film led not to ideal arcs, but resulted in a loop in a modulus plot (*Figure 4.33 b*). The loop in the impedance spectrum is an artifact of the displacement current, which flows to metallic parts, in this case to the heater [124, 125]. An increased distance between the sample and the heater usually helped to minimize inductive loops in the impedance spectrum. The high and low frequency parts of spectra can be analyzed as discussed in the Sec. 3.5. The low-frequency intercept represents the in-plane resistance (estimated conductivity at 320 °C, σ = 1.42 S/cm while conductivity from chapter 4.1 measured with the wide electrodes was σ = 1.81 S/cm). In order to overcome the problem with inductive loops in impedance spectrum, an additional sapphire substrate with grounded platinum foil was used as a shield.

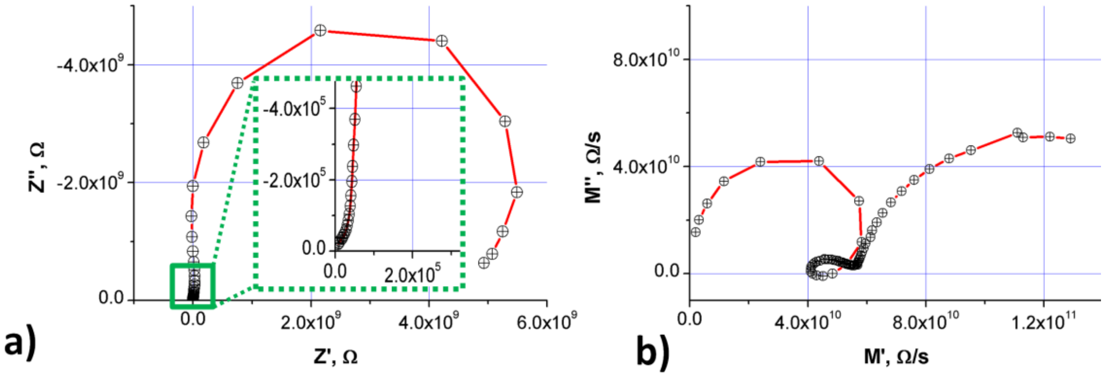

Figure 4.33. *Impedance spectrum of YSZ thin films on silicon substrate with the in-plane measurement geometry (T = 320° C). The magnified high frequency part shows the onset of an arc which is in accordance with numerical simulations. The intercept of the low frequency arc can be attributed to in-plane YSZ resistance*

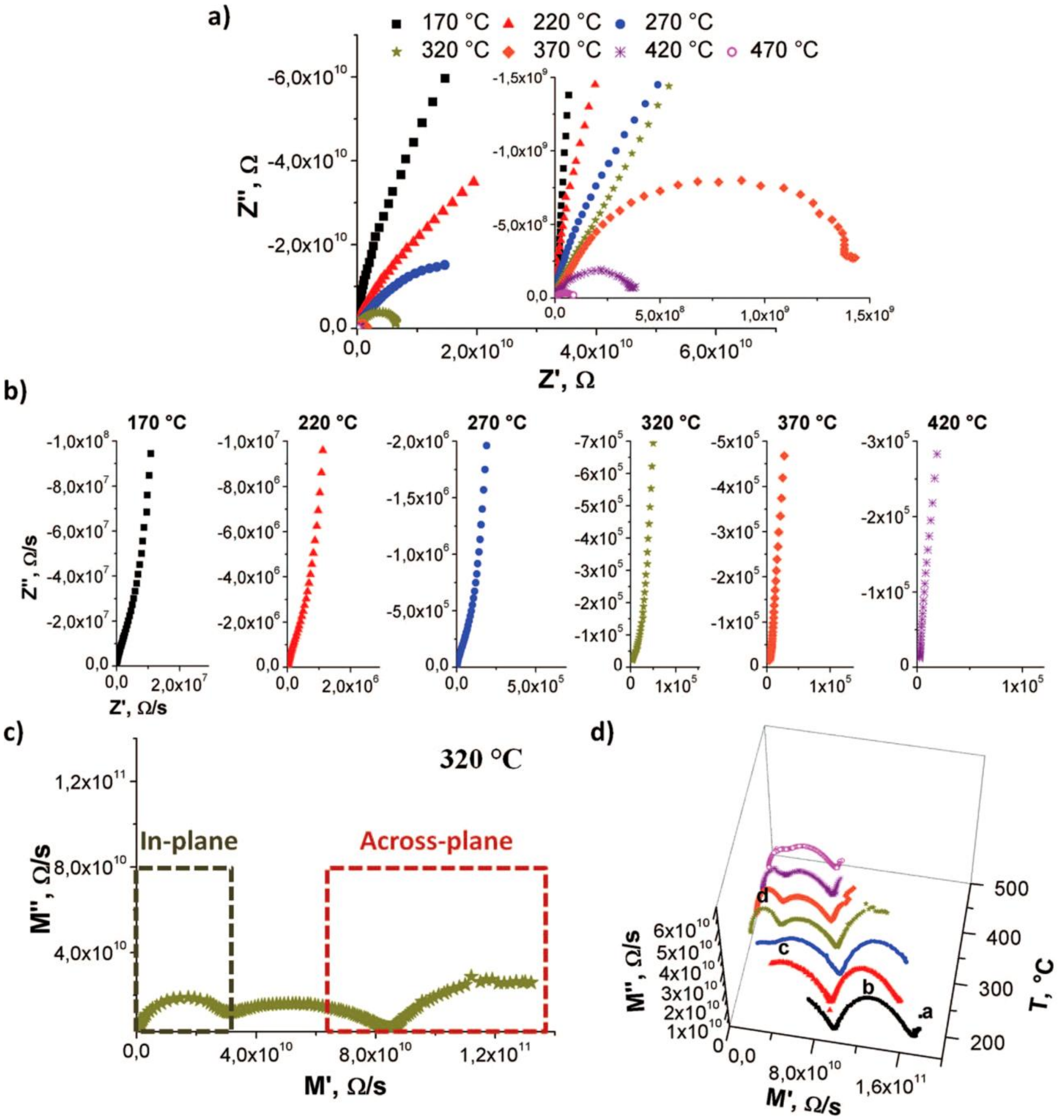

Figure 4.34. *a) Nyquist plots of YSZ layer (t_{YSZ}~55 nm) presenting the impedance behavior in the temperature range from 170 °C to 470 °C; b) High frequency part of Nyquist plots at the certain temperatures presenting the across-plane part; c) Modulus plot of this YSZ layer measured at 320 °C with boxes sketching frequency ranges of in- and across plane current flow; d) Evolution of modulus plots with the temperature*

Typical impedance spectra obtained with additional shielding are shown in *Figure 4.34*. The spectra obtained at lower temperatures exhibit strongly blocking behavior at low frequencies, while a shoulder is observed in the complex impedance plane (Nyquist plot) at high frequencies (*Figure 4.34 b*). The spectra measured at higher temperatures reveal a temperature dependent low frequency arc in the Nyquist plot (*Figure 4.34 a*).

This behavior is already in accordance with the suggested equivalent circuits for high and low frequencies (*Figure 4.31 b*). More details of the impedance spectra become visible in the modulus plots (*Figure 4.34 c* and *d*). One can see that measurements at low temperatures clearly show three features (*Figure 4.34 d*), namely the arcs or peaks **a**, **b** and **c**. Geometry dependent measurements (see below) reveal that the high frequency peak **a** and arc **b** can indeed be associated with the across-plane current flow and thus with silicon (R_{Si}) and the YSZ layer ($R_{YSZ\perp}$, $C_{YSZ\perp}$). The third semicircle in the modulus spectrum (arc **c**) is more complex and neither its resistance nor its capacitance fits to properties of the silica interlayer [112].

Peak **a** diminishes while arc **c** fully develops in the modulus plot (*Figure 4.34 d*) when increasing the temperature. At even higher temperatures, a fourth arc **d** (*Figure 4.34 c, d*) becomes visible at low frequencies while arc **b** shifts out of the measurable frequency range. The overlapping low frequency arcs **c** and **d** in the modulus plot have their counter-part in the large low frequency arc visible in the Nyquist plot. However, in the latter plot a separation into two features is hardly visible (*cf. Figure 4.34 a*). Further increase of the temperature leads to an increasing overlap of arcs **c** and **d** and they become inseparable at the highest temperature. In accordance with the low frequency equivalent circuit model (*Figure 4.31 b*) and the geometry dependent measurements (see below), the low frequency limit of arc **d** represents the in-plane YSZ resistance ($R_{YSZ\,||}$). However, a more detailed mechanistic interpretation of the arcs **c** and **d** is hardly possible since they most probably primarily reflect the current path flipping from across-plane to in-plane current flow. In particular, none of the capacitance values fit to that of typical grain boundary capacitances expected for in-plane conduction (see below).

Essential in this context is the fact that the across-plane resistance of the silica interlayer was much larger than the low frequency resistance (end of arc d) measured here. This was proven by measuring the impedance between a stripe electrode and the silicon substrate as counter electrode: much higher resistance values were found in the low frequency limit since then the impedance is dominated by the very high (ionic) resistance of silica. This is also in accordance with the across-plane measurements reported in Sec. 4.2.1. There, the finite (ionic) resistivity of silica was quantified and the corresponding values again indicate that all low frequency resistance data reported for two stripe electrodes are not affected by the silica resistance. Moreover, it is worth mentioning that the onset of electrode polarization (i.e. an additional arc) was visible for high temperatures and very low frequencies. However, due to the insufficient number of data points, this part of the impedance spectrum was not further analyzed.

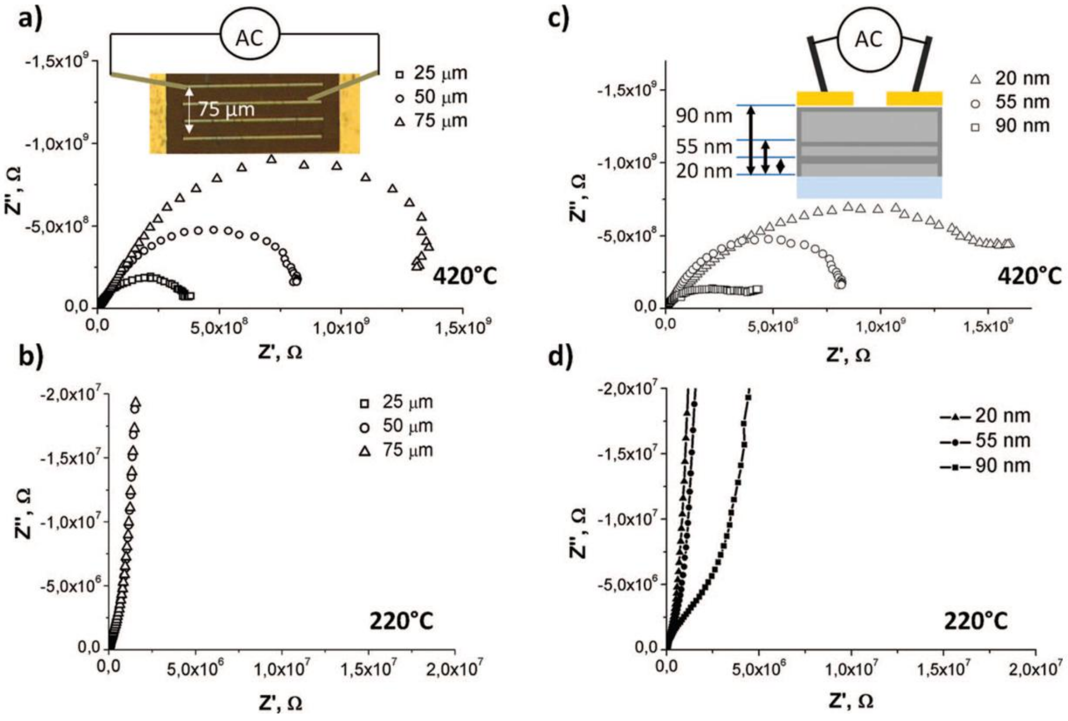

Figure 4.35. *a) Nyquist plots of the low frequency parts of impedance spectra measured with different electrode distances (25 µm, 50 µm and 70 µm); b) High frequency part of impedance spectra measured at 220 °C; c) Low frequency part of impedance spectra measured at 420 °C on layers of different thickness; d) High frequency part of spectra measured at 220 °C*

The interpretation of the high frequency and low frequency limits of the spectra in terms of across-plane and in-plane conduction is further confirmed by measurements with different electrode distances: it is shown in *Figure 4.35 a* and *b* that the high frequency part of the spectrum remains almost identical (across-plane case) when increasing the distance between electrode stripes from 25 to 75 µm, while the size of the low frequency arc in the Nyquist plot increases with increasing electrode distance (in-plane current flow). On the other hand, when changing the thickness of the YSZ layer, the high frequency part as well as the low frequency part of the spectrum varies: Thicker layers decrease the low frequency resistance in accordance with its interpretation as in-plane resistance of YSZ and the high frequency shoulder becomes larger as expected for the across-plane resistance of YSZ.

Even though all features of the temperature dependent spectra are in accordance with our model, it remains to be shown that a quantitative analysis indeed leads to reasonable values. In order to quantify $R_{YSZ\perp}$ and $C_{YSZ\perp}$, the high frequency part of the spectrum was fitted to the across-plane part of the equivalent circuit shown in *Figure 4.31 b*. The across-plane conductivities of films with thickness t_{YSZ} were then calculated according to

$$\sigma_{across-plane} = \frac{2 \cdot t_{YSZ}}{R_{YSZ\perp} \cdot l \cdot w} \quad \textbf{(Eq. 4.11)}$$

where l and w are the length and width of the electrodes, respectively. The factor of 2 takes into account that the current has to pass the YSZ layer twice. The resulting YSZ conductivities are shown in an Arrhenius plot (*Figure 4.36*).

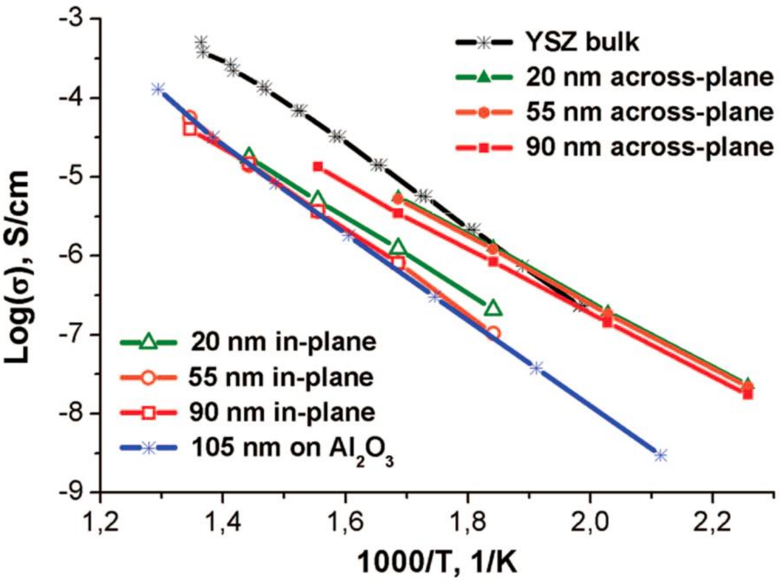

Figure 4.36. *Comparison of YSZ bulk conductivity (from polycrystal) and in-plane conductivity of YSZ thin film on sapphire with the in- and across-plane conductivities obtained for YSZ thin films on silicon*

For the highest temperatures used, arc **c** is out of the measured frequency range and thus across-plane conductivities could only be determined up to about 370 °C. $R_{YSZ\perp}$ scales linearly with the YSZ layer thickness and hence the resulting conductivities are almost identical for all three YSZ films under investigation. Also the values of capacitance $C_{YSZ\perp}$ show a consistent behavior: There is no change for electrodes distance variation but substantial change for YSZ film thickness variation (*Table 4.10*).

$C_{YSZ\perp}$ was calculated from the corresponding constant phase element according to *(Eq. 4.1*). Relative permittivities deduced from these capacitances (~30) are reasonable for YSZ [128].

Table 4.10. *Capacitance values of YSZ determined from in- and across plane measurements.*

Geometry of the electrodes: length = 850µm, width = 10µm, 55 nm YSZ layer		Geometry of the electrodes: length = 850µm (400µm)*, width = 10µm, distance = 50 µm	
Distance between the electrodes:	**$C_{YSZ\perp}$, pF**	**Layer thickness:**	**$C_{YSZ\perp}$, pF**
25 µm	26	**20 nm**	54
50 µm	26	**55 nm**	26
75 µm	26	**90 nm***	6

The low frequency resistance $R_{YSZ\,||}$ was obtained from a fit of the low frequency part of arc **d** to one RQ element (cf. *Figure 4.31 b* bottom), i.e. extrapolation of the impedance to the real axis in the Nyquist plot. The in-plane conductivity was then estimated from

$$\sigma_{in-plane} = \frac{D}{R_{YSZ\,||} \cdot t_{YSZ} \cdot l} \qquad \textbf{(Eq. 4.12)}$$

where D is the distance between the electrodes. The resulting values are again shown in *Figure 4.36*. The in-plane conductivity could not be determined for the lowest temperatures since arc **d** was out of the measurement range.

These conductivity data are compared to those of a YSZ layer on insulating sapphire. Obviously, the in-plane conductivity of YSZ on silicon is similar to that on sapphire and is approximately one order of magnitude smaller than the across-plane conductivity (on Si). In case of films on insulating substrates, the lower effective conductivity was proven to be caused by blocking contributions of grain boundaries [46, 129] and we regard it as reasonable to conclude the same for the films on Si substrates. The across-plane conductivity values are similar to the bulk values of a macroscopic polycrystalline sample (analyzed by conventional impedance spectroscopy), see *Figure 4.36*. The calculated activation energies determined from these data (*Table 4.11*) also suggest a strong contribution of grain boundaries to in-plane current flow: The activation energies of in-plane conductivities are larger by about 0.2 eV which is in accordance with many studies on the grain boundary properties of polycrystalline YSZ samples [131]. Hence, also quantitative analysis of resistance and capacitance values confirms our interpretation and the validity of the model and proofs the applicability of the novel method.

Table 4.11. *Activation energies for in- and across-plane conductivities in YSZ layers of different thickness*

Layer thickness, Nm	E_a across-plane, eV	E_a in-plane, eV
20	0.82	0.96
55	0.86	1.06
90	0.80	1.00

These experiments demonstrate that simultaneous in- and across-plane conductivity measurements on YSZ layers are possible in a limited temperature range. Hence, the blocking effect of a native silica interlayer on a Si substrate allows anisotropy studies of ion conduction in thin films. However, owing to the flipping current lines with decreasing frequency, two different equivalent circuits have to be used to fit high and low frequency data in order to extract the in- and across-plane conductivity values. It was found that the across-plane conductivity of YSZ thin films is approximately one order of magnitude higher than the in-plane values. This is most probably due to the effect of grain boundaries partially blocking the in-plane ion transport.

4.3.2 Interlayer effect on conductivity measurements

The YSZ thin films prepared on silicon substrates always have a native interlayer of silica, as was demonstrated in the previous studies. The interlayer might be useful, because on one hand we can avoid short-circuits in the across-plane measurements and it allows to probe conductivity anisotropy [113]. On the other hand this interlayer might also affect the structure of the thin YSZ layer [132]. Moreover, the role of the dielectric interlayer in impedance spectra has been demonstrated by an equivalent circuit modelling, which was discussed in the across-plane measurement part (Sec. 4.2). It was shown that an interlayer with higher permittivity should make the high frequency shoulder even more pronounced in the Nyquist plot, thus making separability of the across-plane resistivity less complex (*Figure 4.22*). In this last part of the thesis the effect of the dielectric buffer layer is investigated. Different dielectric buffer layers with dielectric permittivities higher than silica were prepared on silicon substrate.

Table 4.12. *YSZ thin layers with varied dielectric buffer layer. The deposition time of YSZ layers and thicknesses of the buffer layers are given in brackets*

Dielectric interlayer	**Sample No.**	**Sample structure**
Y_2O_3	EN14	YSZ (**30 min**)/Y_2O_3 (4nm)/ Si wafer
	EN15	YSZ (**15 min**)/Y_2O_3 (4nm)/ Si wafer
	EN16	YSZ (**10 min**)/Y_2O_3 (4nm)/ Si wafer
	EN17	YSZ (**5 min**)/Y_2O_3 (4nm)/ Si wafer
ZrO_2	EN18	YSZ (**30 min**) /ZrO_2 (4nm)/ Si wafer
	EN19	YSZ (**15 min**) /ZrO_2 (4nm)/ Si wafer
	EN20	YSZ (**10 min**) /ZrO_2 (4nm)/ Si wafer
	EN21	YSZ (**5 min**) /ZrO_2 (4nm)/ Si wafer
Al_2O_3	EN22	YSZ (**30 min**) /Al_2O_3 (4nm)/ Si wafer
	EN23	YSZ (**15 min**) /Al_2O_3 (4nm)/ Si wafer
	EN24	YSZ (**10 min**) /Al_2O_3 (4nm)/ Si wafer
	EN25	YSZ (**5 min**) /Al_2O_3 (4nm)/ Si wafer
	EN26	YSZ (**3 min**) /Al_2O_3 (4nm)/ Si wafer
	EN27	YSZ (**1 min**) /Al_2O_3 (4nm)/ Si wafer

The YSZ layers were prepared by PLD method according to the procedure described in the methods part. All deposition parameters were kept constant except the deposition time, which was varied in order to change the layer thickness. The deposition time for a series of samples was as follows: 30 min, 15 min, 10 min and 5 min. Thinner layers with the deposition time of 3 min and 1 min were also prepared, but after XRD measurement were not further analyzed. Three types of dielectric buffer layer were prepared on silicon substrates by atomic layer deposition (ALD): alumina (ε_r ~ 10 [107, 108]), yttria (ε_r - 9 - 18 [133, 134]) and zirconia (ε_r ~ 27 [104, 106]). The deposition temperatures for Al_2O_3 and ZrO_2 were 200 °C and 250 °C for Y_2O_3. The thickness of all dielectric interlayers was estimated from layer growth rate and the thickness of all the layers was 4 nm. The deposited dielectric buffer layers should be amorphous, since all of them were deposited at low temperatures. The structure of the samples and YSZ thin film deposition time is defined in *Table 4.12*.

The structure of all samples was determined by XRD method and the patterns are shown in *Figure 4.37*. Deposited layers are very thin, hence the estimation of layer structure from laboratory XRD measurements is sophisticated. As one can see from XRD graphs, YSZ layers deposited on alumina and zirconia buffer layers are highly (111) oriented. Weak intensity of other orientations (e.g. 220) can also be observed in thicker layers. As this has been found from TOPAZ analysis, the YSZ layers on yttria buffer layer have a polycrystalline structure. A peak shift of the (111) orientation was also observed for YSZ layers deposited on an alumina buffer layer (*Figure 4.37 a*). The peak shift might be attributed to the effect of strain and a more detailed study on this is discussed below.

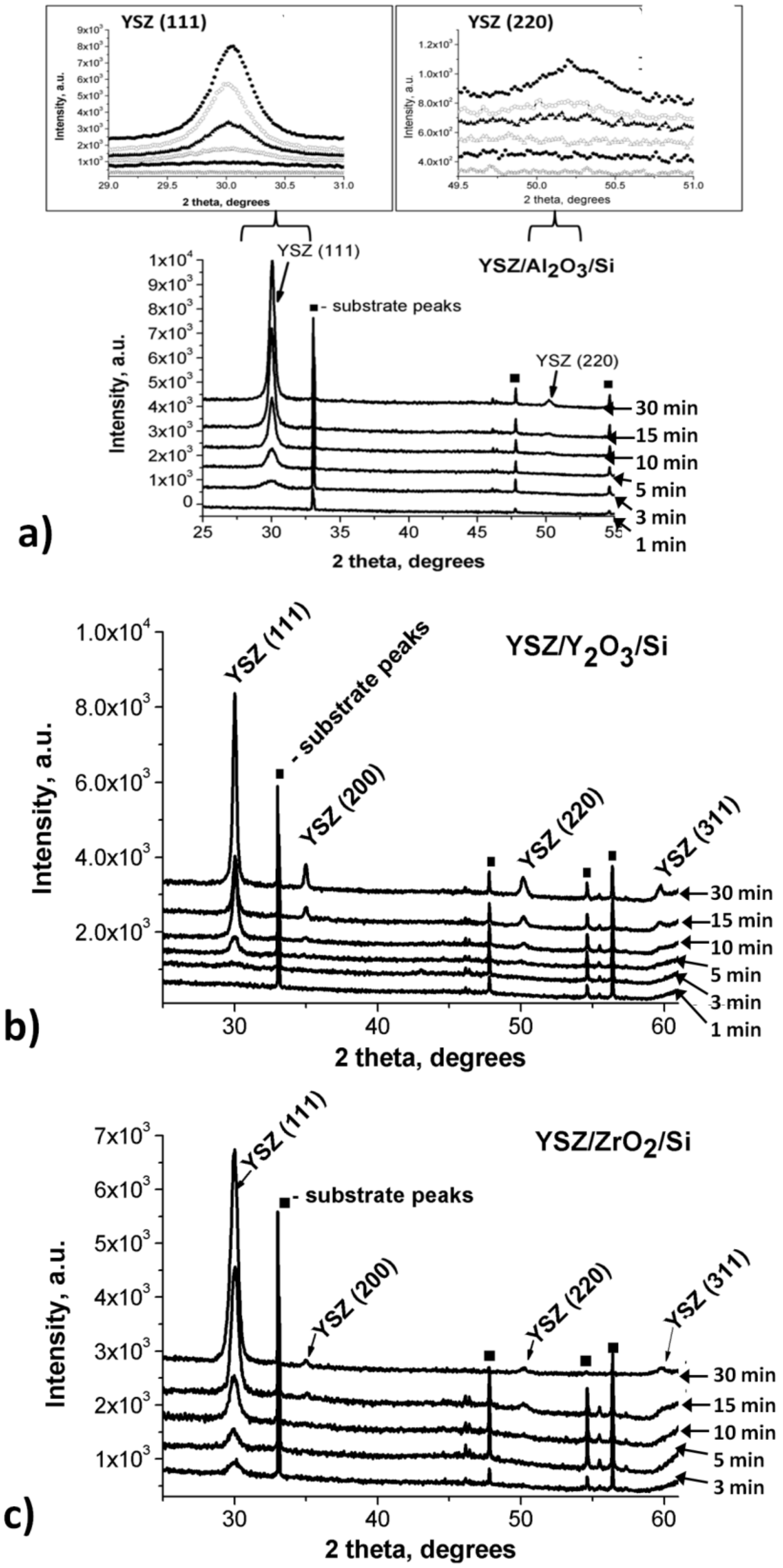

Figure 4.37. *XRD patterns of YSZ thin films deposited with varied deposition time on silicon substrates with alumina (a), yttria (b) and zirconia (c) buffer layers*

The XRD measurements on EN22 sample were done in the usual XRD measurement geometry (χ = 90°) and tilted by 70° (χ = 160°) (*Figure 4.38*). The tilting of the sample reveals more information on the YSZ microstructure. The tilting of a polycrystalline sample leads to a lower intensity of the XRD pattern, although the ratio between the intensities from different crystallographic planes is constant. After tilting the diffractograms of sample EN22 demonstrate significantly decreased intensity of the (111) peak, which is an indication of highly oriented columnar layers.

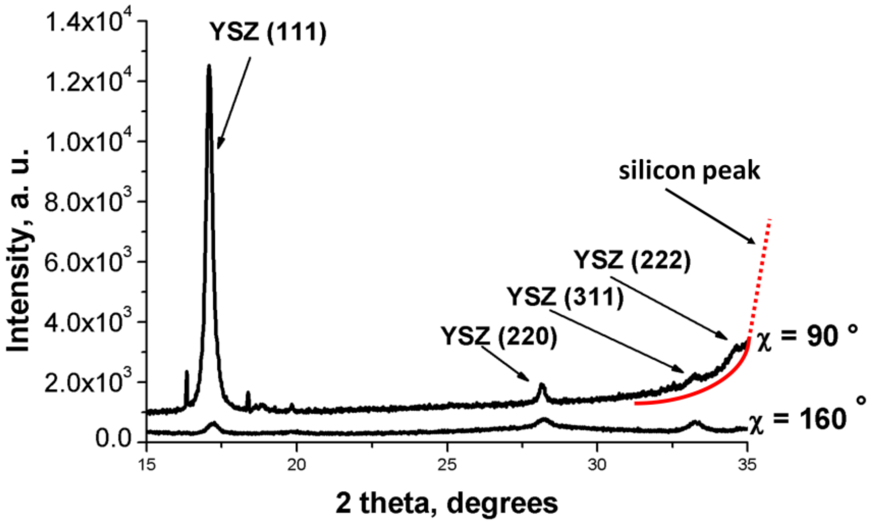

Figure 4.38. *The X-ray diffraction patterns of sample EN22 obtained with usual XRD measurement geometry ($\chi = 90°$) and tilted by 70° ($\chi = 160°$)*

In order to prove the existence of the strain in YSZ layers additional XRD measurements were made on selected samples with 6 circle goniometer at SSRL. This type of goniometer allows to orient the sample in a position where the scattering vector of a given crystallographic plane is parallel to the surface normal. In this case the measurements were done on (111) and (11-1) orientations. For the (11-1) orientation measurement samples were tilted by 70°. The measured diffractograms of (111) (black curve) and (11-1) (open circles) orientations are shown in *Figure 4.39*. This measurement was done in order to check the presence of strain. Layers with a cubic structure without strain should have the same spacing between crystallographic planes ($d_{(111)} = d_{(11\text{-}1)}$). As one can see from *Figure 4.39* the peak position of (111) is shifting towards lower values of *d*, which could be an indication of tensile strain. On the other hand the θ (d, τ) is a function of spacing between the planes (*d*) and penetration depth (τ). The measurement geometry was changed and the shift of *d* values can be due to two reasons - penetration (absorption) and strain. Since it was not possible to evaluate the penetration effect from two measurements at different tilting angles, the presented diffractograms are used for quantitative evaluation.

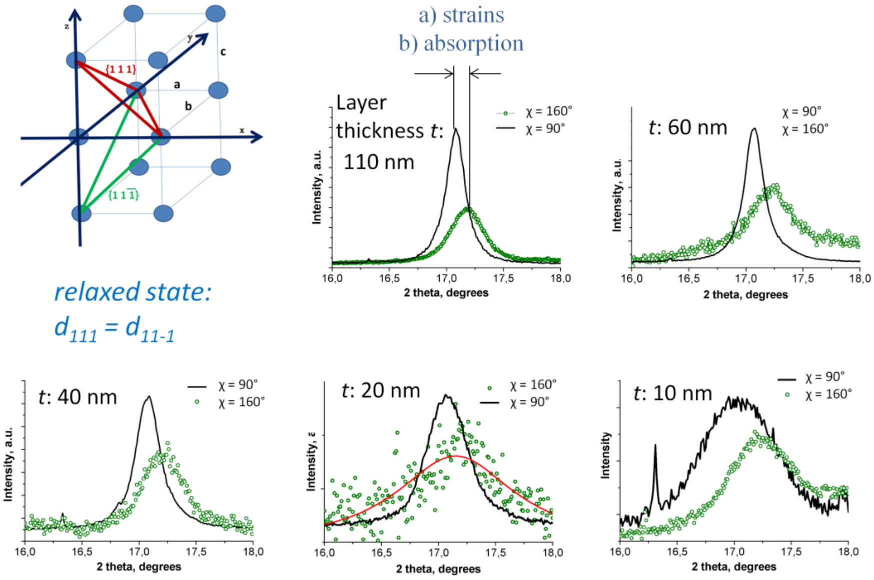

Figure 4.39. *X-ray diffraction measurement of (111) and (11-1) crystallographic planes*

Lattice parameters of XRD demonstrate tendencies correlated with deposition time (layer thickness). The YSZ layer on alumina buffer layer with deposition time of 30 min has a lattice parameter of a = 5.168 Å. Lattice parameters of thinner films are slightly shifted – a film with 10 min deposition time has a of 5.173 Å and a YSZ film, which was deposited for 5 min, has a of 5.180 Å. In all layers it was found that the peaks have a tendency to shift towards higher diffraction angles i.e. to lower d. The estimated lattice parameter a for all YSZ layers is plotted in *Figure 4.40* and it demonstrates a clear tendency to decrease for thicker layers.

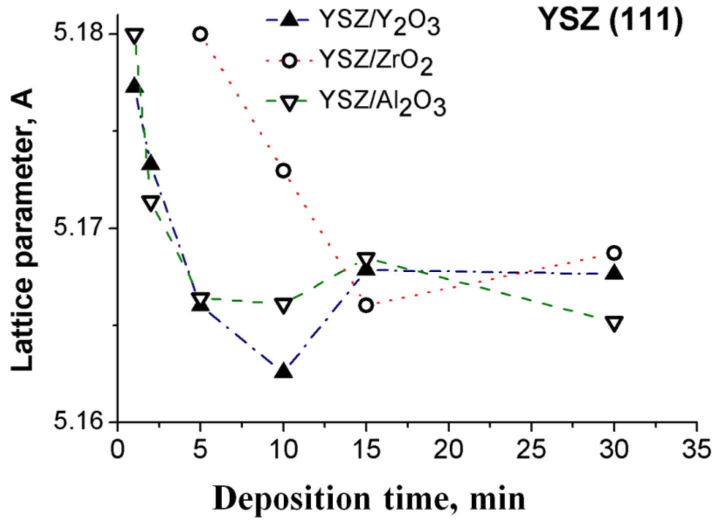

Figure 4.40. *The lattice parameter a of deposited YSZ thin films is decreasing with deposition time (thickness)*

In some publications [10, 136, 137] Raman spectroscopy was used on thin YSZ layers for phase identification and it was reported, that strain effects might be estimated from such Raman measurements. Raman spectroscopy was used for detection of strain in the thin layers, since strain should change the distance between Zr and O ions in the lattice. Measurements were done on YSZ layers deposited on an alumina buffer layer (EN23, EN24 and EN25). For reasons of comparison Raman spectra of YSZ pellet and Si substrate are also included in *Figure 4.41*. One can see that only the peaks of the silicon substrate can be observed in Raman spectra of YSZ layers. Any possible contribution of YSZ layers was not observed due to the insufficient optical thickness of the YSZ layer.

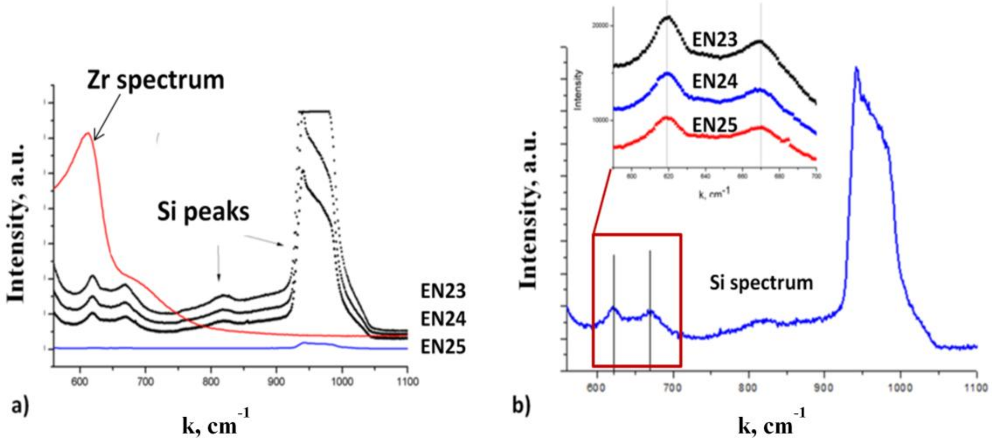

Figure 4.41. *a) Measured Raman spectra of YSZ thin layers and of a YSZ pellet; b) peaks found for the YSZ layers at 619 cm^{-1} and 670 cm^{-1} correspond with the silicon peaks*

The surface roughness of YSZ layers was checked by AFM. It was found that the roughness decreases with the film thickness from R_{rms} - 1.5 nm for EN23 sample to R_{rms} - 0.2 nm for EN25 sample. The AFM measurements were as well done on the YSZ layer deposited on Y_2O_3 and Al_2O_3 buffer layers. The AFM measurements of the thinnest samples EN17 (YSZ/Y_2O_3) and EN25 (YSZ/Al_2O_3) resulted in R_{rms} roughness of 0.37 nm and 0.43 nm, respectively. For the thickest layer EN14 (YSZ/Y_2O_3) and EN22 (YSZ/Al_2O_3) the R_{rms} increases (0.79 nm and 0.78 nm, respectively). Similar tendencies of R_{rms} of thin films with varied deposition time were also observed in other studies [138] and it was attributed to the surface coverage.

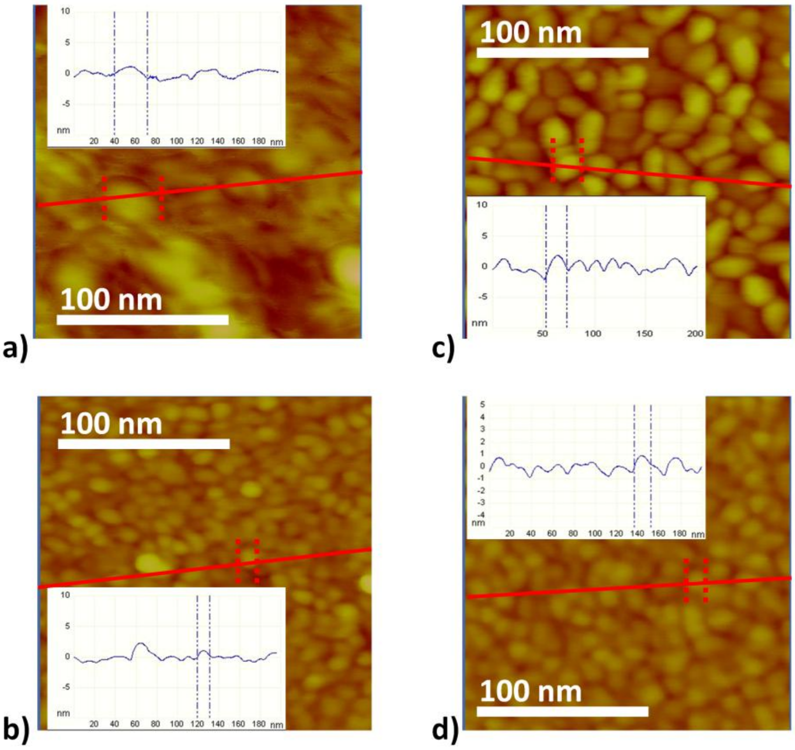

Figure 4.42. *The AFM micrographs of YSZ layers: a) EN17; b) EN14; c)EN 25 and d) EN22*

XRR measurements on selected samples were done in order to define the thickness of the YSZ layers. The measurements were performed on EN14, EN15 and EN16 samples. The resulting XRR profiles are shown in *Figure 4.43* a. The thicknesses of YSZ layers were estimated from the difference between neighboring maxima of interference fringes, which are obtained at XRR reflectivity profiles (*Figure 4.43 b*):

$$t = \frac{m \cdot \lambda}{2 \cdot \sqrt{\sin^2\theta_m - \sin^2\theta_c}} \qquad \textbf{(Eq. 4.13)}$$

where m - integer, λ – X-ray wavelength (0.154 nm), θ_m – angle position of maxima, θ_m – critical angle of incidence. According to (*Eq. 4.13)* the thickness was estimated from the slope of the graph plotted in *Figure 4.43 c*. The resulting thicknesses for the samples were as follows: EN14 (deposition time: 30 min) – 72 nm, EN15 (deposition time: 15 min) – 36 nm and EN14 (deposition time: 10 min) – 23 nm. For reasons of comparison the simulations of XRR patterns were made with the software in ref. [135]. The simulations were done for a YSZ layer on a silicon substrate (X-ray energy - 8040 eV). The theoretical XRR patterns (*Figure 4.43 d*) are in accordance with the experimental ones (*Figure 4.43 b*).

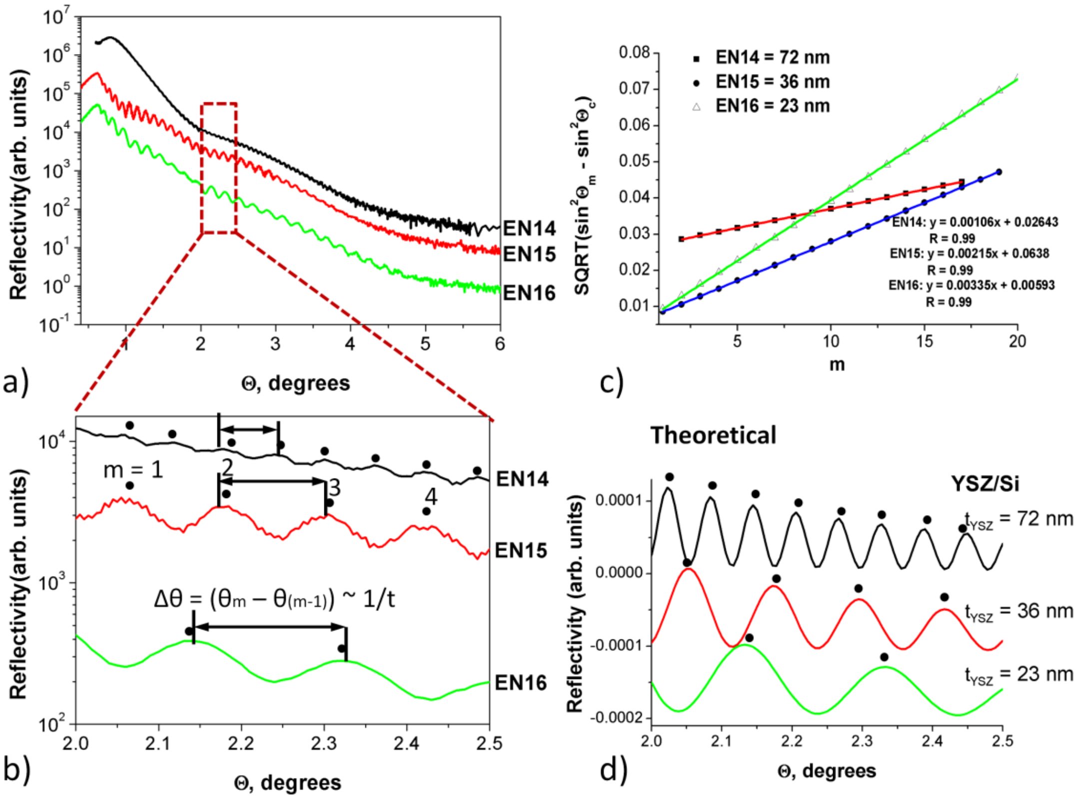

Figure 4.43. *Measured (a and b) and simulated (d) X-ray reflectivity profiles of YSZ thin films. The thicknesses of YSZ layers were determined from the slope in graph c*

The electrical characterization of the samples was performed by impedance measurements. For the measurements gold stripe electrodes were prepared by UV lithography (*Figure 4.44*). The length and the width of the electrodes was 450 µm and

10 µm, respectively. The distance (D) between the electrodes was 25 µm. In order to check the effect of the buffer layer in- and across-plane measurements were performed on the same sample. For the in-plane measurements stripe electrodes were used. For the across-plane measurement the bottom side of the samples was covered with a silver paste. In the across-plane measurement one needle was placed on a stripe electrode and while the other one on the counter electrode (*Figure 4.44*). Standard parameters (amplitude 1 V, f = 10 mHz to 1MHz) were used for impedance measurements.

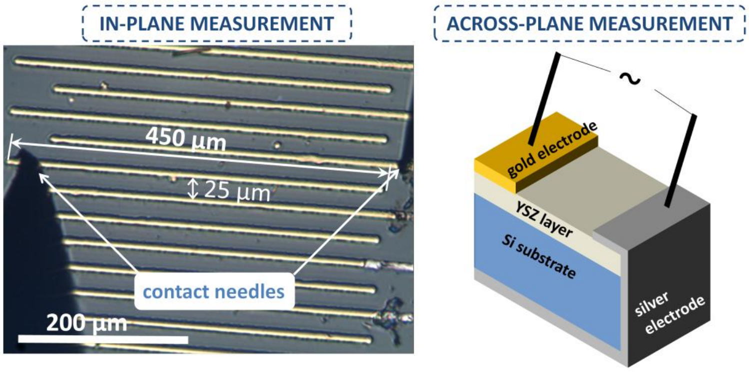

Figure 4.44. *In- and across-plane measurement sketch*

The across-plane impedance measurements took place at low temperatures (250 °C) since there the relevant part is more pronounced in the impedance spectrum. The impedance spectra of YSZ layers on a Y_2O_3 buffer layer are shown in *Figure 4.45*. As one can see from the Nyquist graph (*Figure 4.45 a*) the impedance spectra are very similar to those in chapter 4.3. The low frequencies contain a part of the highly resistive arc, while for high frequencies a shoulder can be observed. There are no additional features in the Bode plot, which could originate from the dielectric buffer layer.

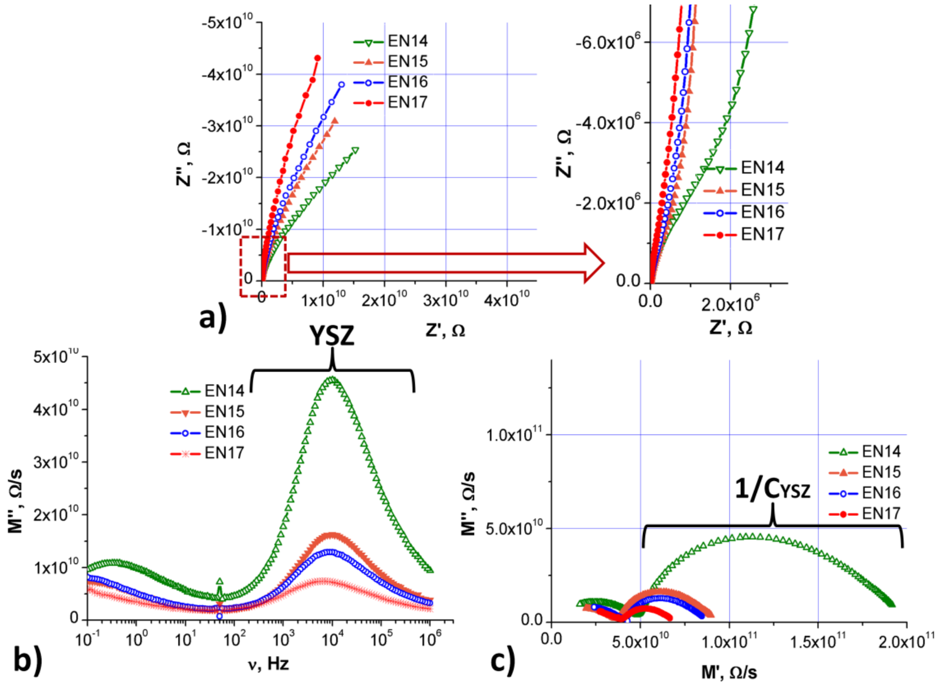

Figure 4.45. *Nyquist (a), Bode (b) and Modulus graphs (c) of across-plane measurement of YSZ layers with varied thickness*

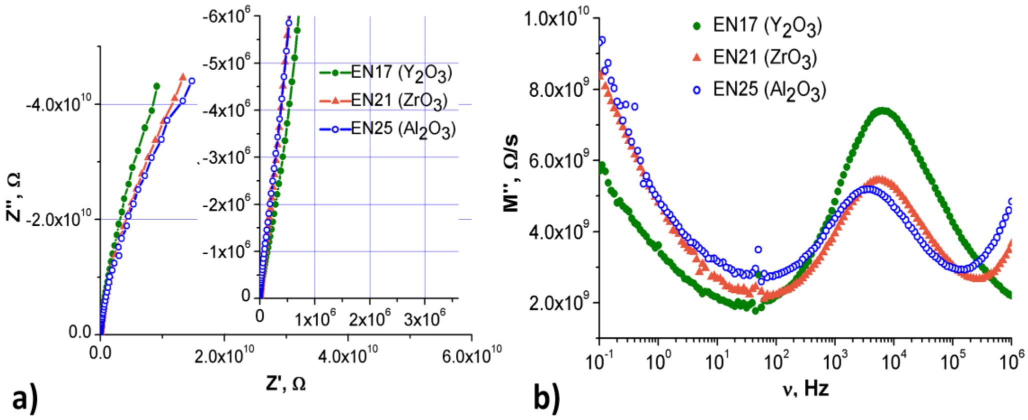

Figure 4.46. *The Nyquist (a) and Bode (b) plots of YSZ layers deposited on dielectric Y_2O_3, ZrO_2 and Al_2O_3 interlayers*

The across-plane measurements were done for YSZ layers on Y_2O_3, ZrO_2 and Al_2O_3 interlayers. It was demonstrated in chapter 4.2.1 (*Figure 4.22*) that an increased range of YSZ thickness might become accessible if the insulating layer had a higher dielectric constant. The Nyquist and Bode plots of the thinnest YSZ layers are shown in *Figure 4.46*. Unfortunately an impact of increased dielectric permittivity of dielectric interlayers was not observed. This might be explained by an insufficient thickness of the buffer layer or some compositional changes of this interlayer, which is observed at the layer/silica interface [140].

Table 4.13. *The capacitance values of buffer and YSZ layers (electrode geometry 450x10 µm), estimated from across-plane measurement*

Dielectric interlayer	**Sample No.**	**$C_{YSZ\perp}$, pF**	**t_{YSZ}, nm**	**C_d, pF**	**ε_d***
Y_2O_3	EN14	11.7	72.0	27.0	2.7
	EN15	33.6	36.0	33.5	3.4
	EN16	44.1	23.0	32.4	3.3
	EN17	89.4	12.0	31.4	3.2
Zr_2O_3	EN18	16.1	66.7	41.1	4.1
	EN19	33.0	32.6	40.7	4.1
	EN20	70.1	15.2	33.9	3.4
	EN21	153.9	7.0	27.1	2.7
Al_2O_3	EN22	18.0	59.7	24.7	2.5
	EN23	52.7	20.4	37.4	3.8
	EN24	88.2	12.2	34.8	3.5
	EN25	192.2	5.6	27.9	2.8

The impedance spectra of across-plane measurements were fitted with the equivalent circuit shown in *Figure 4.15* with CPE instead of capacitors. The equivalent circuit consists of two RC elements – one for the YSZ resistance and capacitance, the other for the dielectric interlayer resistance and capacitance. $C_{YSZ\perp}$ was calculated from the corresponding constant phase element according to (*Eq. 4.1*). The obtained capacitance values of YSZ layers are listed in *Table 4.13*.

The YSZ layer thickness of EN14, EN15 and EN16 was estimated from XRR measurements. As the geometry of the electrodes and the capacitance is known, the average relative permittivity resulted in 27, which is in accordance with ref. [105]. The thickness values of other YSZ layers were estimated according to (Eq. 4.7) and are listed in *Table 4.13*.

The capacitance values of dielectric buffer layers (C_d) were estimated from the impedance spectra. C_d were calculated from the corresponding constant phase element according to (*Eq. 4.7*) and are listed in *Table 4.13*. As it was mentioned above the thicknesses of all dielectric buffer layers are approximately 4 nm. With this assumption we can evaluate the relative dielectric permittivity of the buffer layer according to:

$$\varepsilon_d = \frac{C_d \cdot 4 \cdot 10^{-9}[m]}{\varepsilon_0 \cdot A}$$ **(Eq. 4.14)**

The resulting permittivity values are listed in *Table 4.13*. One should note that the permittivity does not vary significantly from one dielectric buffer layer to another and the values close to 4 are a good agreement with permittivity of silica (~4) but far from from those of the oxides used. This suggests that during PLD deposition a silica layer of a few nm thickness is formed between silicon and the dielectric interlayer.

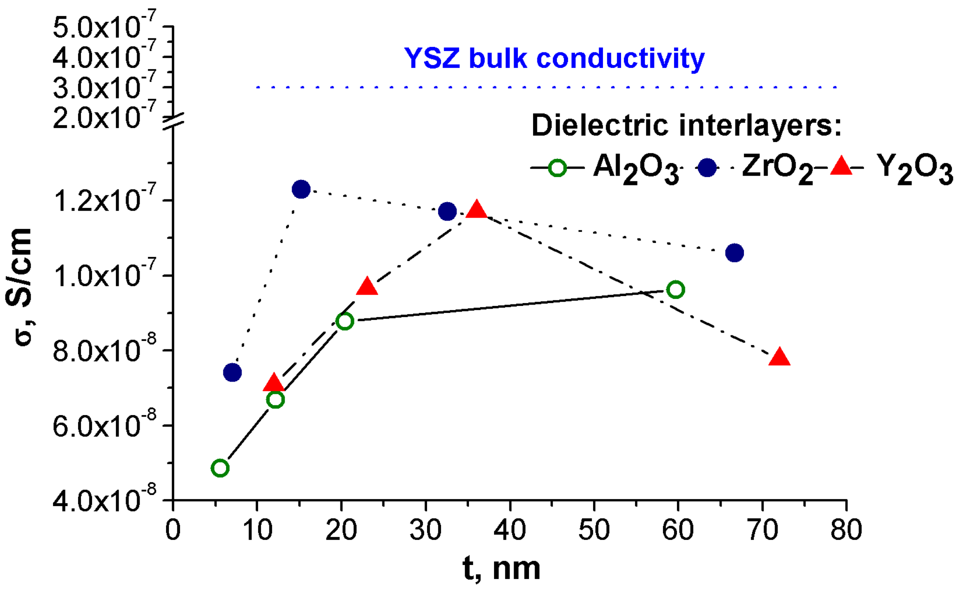

Figure 4.47. *The across-plane conductivities (measured at 450 °C) as a function of YSZ layer thickness for different dielectric interlayers (Al_2O_3, ZrO_2, Y_2O_3)*

From the thickness values of the YSZ layers the conductivity can be calculated according to:

$$\sigma_{YSZ\perp} = \frac{t_{YSZ}}{R_{YSZ} \cdot S}$$ **(Eq. 4.15)**

The across-plane conductivities ($\sigma_{YSZ\perp}$) of YSZ layers with varied dieletric interlayers are plotted in *Figure 4.47*. For reasons of comparison the bulk conductivity of a YSZ pellet is also marked on the graph. One can see that the across-plane conductivity values for all the layers are very similar and are somewhat lower than the YSZ bulk conductivity. The across-plane conductivity has a tendency to decrease with the layer thickness, this could be addressed to a high porosity of thinner films, since it also was observed in chapter 4.1.

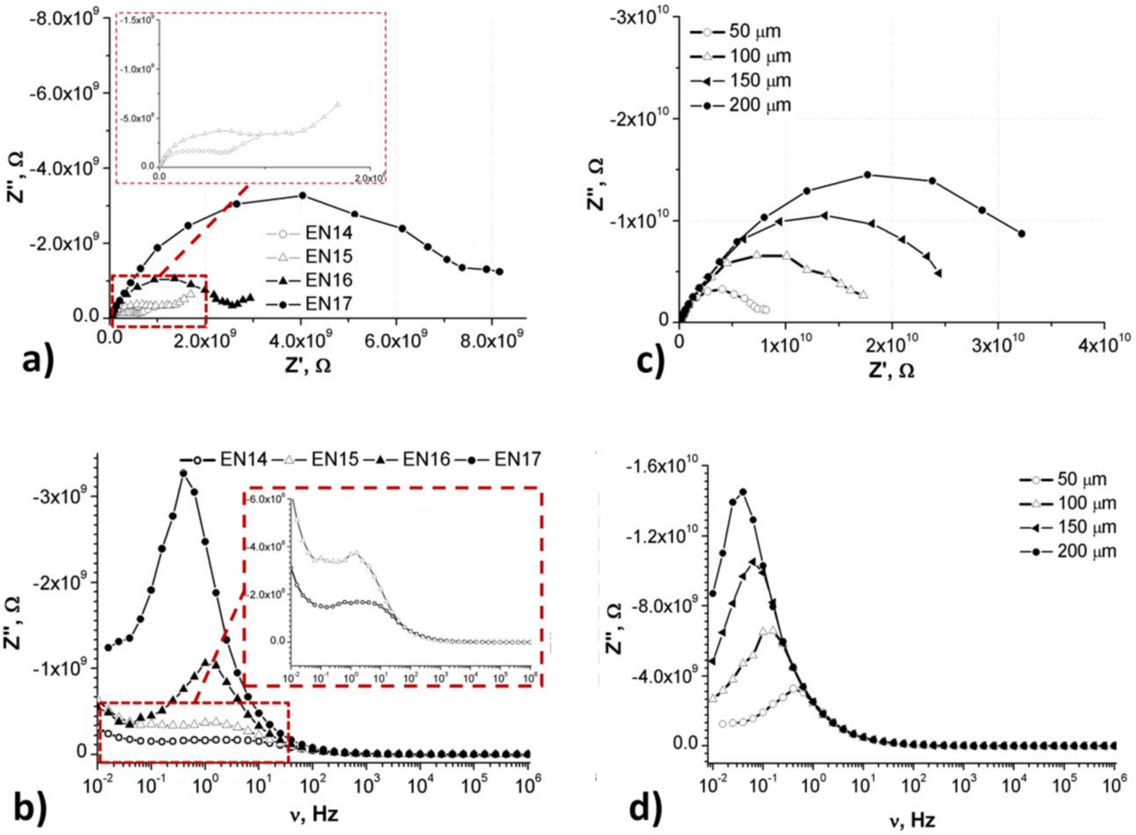

Figure 4.48. *The Nyquist and Bode plots of the in-plane measurement of YSZ/Y_2O_3 layers with varied thickness (a and b) and varied distance between the stripe electrodes (c and d)*

The in-plane measurements were performed at 450 °C, since the in-plane part of a spectrum is detectable only at high temperatures. Impedance spectra were measured between two stripe–shaped gold electrodes with a distance of 50 µm, 100 µm or 150 µm and 200 µm. As it was demonstrated the variation of dielectric interlayer does not lead to a significant change in the impedance spectrum of across-plane measurements. The in-plane impedance spectra are shown in *Figure 4.48*. The in-plane conductivity part on all the layers was measured four times with varied distance between the electrodes and estimated from the low frequency arc. The resulting Nyquist and Bode plots of spectra with varied distance between the electrodes are shown in *Figure 4.48 c* and *d*. The resistance changes in accordance with the distance *D* between the electrodes. The values obtained from the fitting the main arc with one RC element are listed in *Table 4.14*. For a given material the relaxation frequency should not depend on the geometry of the electrodes but from Bode plots one can observe a shift of relaxation frequency towards the lower frequency range when increasing *D*. However it was discussed in a previous part and in the theoretical consideration part that the interpretation of the in-plane capacitance is not straightforward. It is not a property of YSZ and therefore a geometry independence of the relaxation frequency cannot be expected anymore.

Table 4.14. *The in-plane resistance values of the YSZ layer with varied distance between the electrodes (layer thickness is constant – 12 nm) and with a varied layer thickness (D is constant – 50 µm)*

Distance between the electrodes – 50 µm		**Layer thickness – 12 nm**	
YSZ layer thickness, nm	**$R_{YSZ\|\|}$, GΩ**	**The distance between the electrodes, µm**	**$R_{YSZ\|\|}$, GΩ**
72	0.7	50	8.0
36	1.4	100	17.0
23	2.5	150	26.9
12	8.0	200	36.0

The conductivity values as a function of layer thickness on different buffer layers are shown in *Figure 4.49*. The decreasing conductivity at a lower layer thickness is not well understood and might be caused by a higher porosity of thinner layers, as this has been demonstrated in the previous study (Sec. 4.1). However, most obvious is the much larger conductivity found on a ZrO_2 interlayer. On Al_2O_3 and Y_2O_3 buffer layers the conductivity is about one order of magnitude smaller than for bulk YSZ, similar to studies on a sapphire substrate and also similar to YSZ films on a native silica substrate. On the ZrO_2 buffer layer the YSZ conductivity comes much closer to that of a YSZ bulk. Since the decreased in-plane conductivity is attributed to grain boundaries, this suggests less grain boundaries for YSZ on ZrO_2 buffer layer, possibly due to the better lattice match during growth. Comparing in- and across-plane conductivity on ZrO_2 buffer layers even suggests almost identical conductivity values, i.e. absence of any anisotropy Deviation from the YSZ bulk value might therefore partly be caused by some inaccuracy of the temperature measurements.

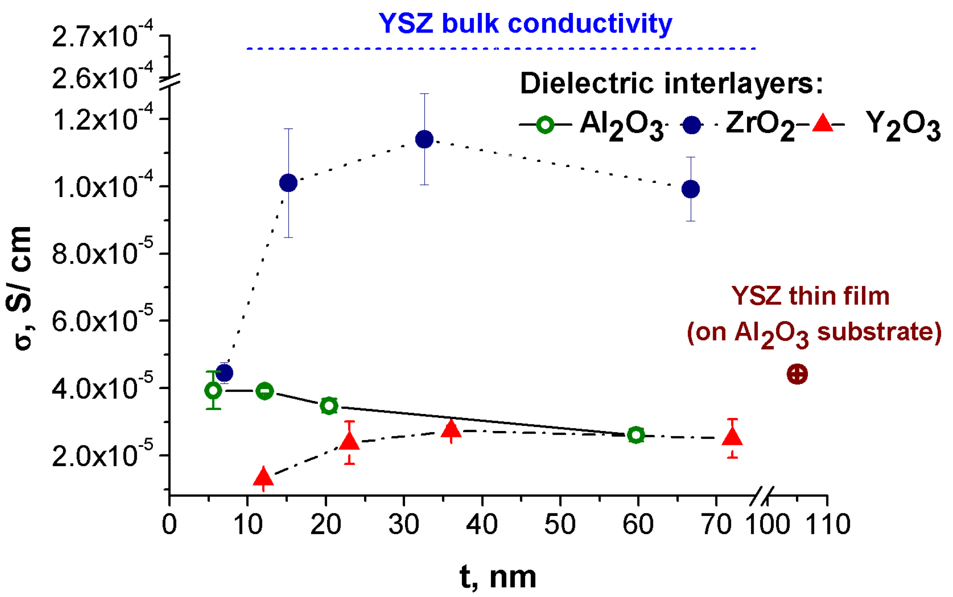

Figure 4.49. *The in-plane (measured at 450 °C) conductivities as a function of layer thickness for varied dielectric buffer layer (Al_2O_3, ZrO_2, Y_2O_3)*

Concluding this part, it was demonstrated that the buffer layer on one hand may affect the structure of the YSZ thin film and on the other hand it is useful for impedance measurements. From impedance measurements it was found that all dielectric buffer layers exhibit nominal dielectric permittivity values which are lower than expected. It was demonstrated that across-plane measurements can be done on YSZ layers as thin as 12 nm but that the expected effect of the dielectric buffer layer in across-plane impedance spectra was not observed due to the low permittivity. The across-plane conductivity is not affected by the buffer layer but tends to decrease with layer thickness. From the in-plane conductivity measurements it was finally observed that the in-plane conductivity of YSZ layers deposited on a zirconia buffer layer is 5 times higher than that on the other substrates. This might be caused by much less grain boundaries in the layer.

]

5 CONCLUSIONS

1. It could be proven by finite element calculations that narrow and closely spaced interdigital electrodes minimize the stray capacitance and allow the access to grain and grain boundary contributions in impedance spectra for thin films on an insulating substrate.
2. It was experimentally shown that the separation of grain and grain boundaries in impedance spectra is possible with interdigit electrodes on YSZ thin films.
3. It was found that the conductivity of grain boundaries is two orders of magnitude lower and the activation energy is 0.15 eV higher than the bulk values.
4. It was demonstrated experimentally and by FEM calculations that an additional dielectric interlayer on a conducting substrate is highly useful in across-plane conductivity measurements, since it minimizes problems due to short-circuiting pinholes. It dominates the low frequency part of impedance spectra, while the conductivity of a YSZ layer can still be determined from the high frequency part.
5. Silica and YSZ across-plane conductivities and capacitances of YSZ/Si samples were successfully separated with the proposed equivalent circuit in the temperature range from 200 °C – 400 °C. It was observed that the across-plane conductivity of the YSZ films does not significantly depend on the layer thickness and is only slightly lower than the bulk conductivity of a YSZ polycrystalline sample.
6. From the across-plane measurements it was found that the thickness of the dielectric layer limits the accessibility of YSZ thin film conductivities in such a sample configuration.
7. FEM calculations and experiments demonstrated that due to frequency dependent current lines simultaneous in- and across-plane conductivity measurements on YSZ layers are possible in a limited temperature range (200 °C – 550 °C), thus allowing anisotropy studies of ion conductivity in thin films.
8. It was found that between 200 °C and 500 °C the across-plane conductivity of YSZ thin films on silicon with a silica buffer layer is approximately one order of

magnitude higher than the in-plane value, which can be attributed to blocking grain boundaries.

9. A variation of the buffer layers (ZrO_2, Al_2O_3, Y_2O_3 instead of SiO_2) could successfully be employed. The expected improvement of the separability of the YSZ across-plane conductivity was not achieved. However, a strong effect of the substrate on the in-plane conductivity was observed: For ZrO_2 buffer layers in- and across-plane conductivities were almost the same, i.e. the anisotropy of the effective conductivity found in all other layers was no longer present.

LIST OF PUBLICATIONS BY THE AUTHOR

M1. Gerstl, M.; Navickas, E.; Friedbacher, G.; Kubel, F.; Ahrens, M.; Fleig, J., The separation of grain and grain boundary impedance in thin yttria stabilized zirconia (YSZ) layers. Solid State Ionics 2011, 185, 32-41.

M2. Navickas, E.; Gerstl, M.; Friedbacher, G.; Kubel, F.; Fleig, J., Measurement of the across-plane conductivity of YSZ thin films on silicon. Solid State Ionics 2012, 211, 58-64.

M3. Navickas, E.; Gerstl, M.; Friedbacher, G.; Kubel, F.; Fleig, J., Simultaneous measurements of the in- and across-plane ionic conductivity off YSZ thin films. Journal of the Electrochemistry Society 2012, 159, B411-B416.

M4. Abakevičienė, B.; Žalga, A.; Tautkus, S.; Pilipavičius, J., Navickas, E.; Kareiva, A.; Tamulevičius, S., Synthesis of YSZ thin films by the novel aqueous sol–gel citrate-precursor method. Solid State Ionics 2012, 225, 73-76.

PARTICIPATION AT CONFERENCES

Poster presentations

1. Navickas, E.; Gerstl, M.; Fleig, J., Simultaneous Measurement of the In and Across Plane Conductivities of YSZ Thin Films on Silicon Substrate // E-MRS 2010, Spring Meeting, Strasbourg, France – June 7-11.

2. Navickas, E.; Gerstl, M.; Friedbacher, G.; Kubel, F.; Doebeli, M.; Braun, A., Tamulevičius, S.; Fleig, J., In-and across-plane conductivity of YSZ thin films on silicon // Advanced Materials and Technologies, book of abstracts of the 13-th International Conference-School, 27-31 August 2011, Palanga, Lithuania. Kaunas : Technologija. ISSN 1822-7759. 2011, p. 66.

3. Žalga, A.; Abakevičienė, B.; Navickas, E.; Beganskienė, A.; Kareiva, A.;Tamulevičius, S.; Fleig, J., Synthesis of YSZ thin films by the novel aqueous sol-gel citrate-precursor method // 18th International Conference on Solid State Ionics, 3-8

July, 2011, Warsaw, Poland : book of poster abstracts / Warsaw University of Technology, ISSI - International Society for Solid States Ionics. Warsaw, 2011. p. 96.

Oral presentations

1. <u>Navickas, E.</u>; Gerstl, M.; Fleig, J., YSZ plonų dangų joninio laidumo tyrimai // Neorganinių junginių chemija ir technologija = Chemistry and technology of inorganic compounds: konferencijos pranešimų medžiaga / Kauno technologijos universitetas. Kaunas: Technologija, 2010. ISBN 9789955258025. p. 8-11.

2. <u>Navickas, E.</u>; Gerstl, M.; Fleig, J., In- and across-plane conductivity measurements on YSZ thin films // CYSENI 2010: 7th Annual Conference of Young Scientists on Energy Issues, May 27-28, 2010, Kaunas, Lithuania: Conference proceedings/Lithuanian Energy Institute, Young Scientists Association of LEI. Kaunas: LEI. ISSN 1822-7554. 2010, p. VII-374-VII-381.

3. <u>Navickas, E.</u>; Gerstl, M.; Fleig, J., Grain and grain boundary conductivity separation and anisotropy of the conductivity of YSZ thin films, 9th International Symposium "Systems with Fast Ionic Transport", June 1-5, 2010, Riga, Latvia.

4. <u>Navickas, E.</u>; Gerstl, M., Fleig, J., Anisotropy of ionic conductivity in YSZ thin films, 18th International Conference on Solid State Ionics, 3-8 July, 2011, Warsaw, Poland: book of poster abstracts / Warsaw University of Technology, ISSI - International Society for Solid State Ionics. Warsaw, 2011. p. 478.

5. <u>Navickas, E.</u>; Gerstl, M.; Chen, Q.; Tamulevičius, S.; Kubel, F.; Doebeli, M.; Braun, A.; Fleig, J., Interface contribution to ionic conductivity in thin films // Materials engineering 2011: 20th International Conference, October 27-28, Kaunas, Lithuania : book of abstracts / Kaunas University of Technology, Association of Baltic Materials Societies, Lithuanian Materials Research Society, Lithuanian Foundries Association. Kaunas: Technologija. ISSN 2029-8307. 2011, p. 9.

6. <u>Navickas, E.</u>; Gerstl, M.; Friedbacher, G.; Kubel, F.; Döbeli, M.; Toney, M.; Tamulevičius, S.; Fleig, J., In- and across plane conductivity measurements on YSZ thin films in dependent on a substrate, // E-MRS 2012, Spring Meeting, Strasbourg, France – May 14-18.

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LIST OF ABBREVIATIONS

YSZ	Yttria stabilized zirconia
GDC	Gadolinium doped ceria
STO	Strontium titanate
XRD	X-ray diffraction
PLD	Pulsed laser deposition
AFM	Atomic force microscopy
RBS	Rutherford backscattering spectrometry
DHM	Digital holographic microscopy
SEM	Scanning electron microscopy
XRR	X-ray reflection
SOFC	Solid oxide fuel cell
FEM	Finite element method
AC	Alternating current
CPE	Constant phase element
DC	Direct current
GB	Grain boundaries
TC	Texture coefficient

LIST OF SYMBOLS

D	The distance between the electrodes
l	Electrode length
t	Layer thickness
d_g	Grain size
d_{gb}	Grain boundary width
W	The width of the electrode
C_{gb}	Grain boundary capacitance
C_b	Bulk capacitance
Z', Z''	Real and imaginary part of impedance
M', M''	Real and imaginary part of modulus
E	Permittivity
$R_{YSZ\,\|\|}, C_{YSZ\,\|\|}$	In-plane resistance and capacitance
$R_{YSZ\perp}, C_{YSZ\perp}$	Across-plane resistance and capacitance
R_{gb}	Grain boundary resistance
R_b	Bulk resistance
E_{bulk}, E_{gb}	Activation energy of bulk and grain boundaries
ω_r, f_r	Relaxation frequency
C_{stray}	Stray capacitance
C_{gb}	Grain boundary capacitance
D_v	Diffusion coefficient
Q, n	CPE fitting parameters
V_O^{**}	Oxygen vacancy
C_{stray}	Stray capacitance

LIST OF FIGURES

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