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Control Circuits for an Electronic-Photonically Integrated Optical Switch Matrix

ausgeführt zum Zwecke der Erlangung des akademischen Grades

eines Doktors der technischen Wissenschaften unter der Leitung von

Univ.-Prof. Dr.-Ing. Horst Zimmermann
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Fakultät für Elektrotechnik und Informationstechnik

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Erklärung zur Verfassung der Arbeit

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Abstract

There are several research goals which drove the writing of this thesis. The main goal of this research was to develop control circuits for driving photonic components with high power efficiency. In this work, a highly integrated photonic chip, with over 1000 optical functions, is 3D-integrated via micro copper pillars on an electronic IC (EIC). One of the research goals is also to achieve high density of optical functions per mm^2, the target being 1000 optical functions on 21 mm^2. This integration level is very high, including the waveguides crossings, the number of optical functions per mm^2 amounts to 200, in the area of the switch matrix. The function of EIC is to control all photonic switches in the photonic chip. Both integrated and additional discrete electronics are designed properly to satisfy the constraints in terms of power consumption, power efficiency and package size of the proposed device. All steps in the design process of this device are discussed in this work.

Photonic switches are brought into resonance by heating resistors, integrated in the photonic chip. One of the central topics of this research is the development of different approaches for heater control: analog, digital or analog-digital are investigated in terms of power efficiency, resolution and scalability. Two chips designed in different technologies, photonic and electronic, are 3D integrated via micro copper pillars. The BCD 180 nm technology was chosen for the design of EIC. Core circuit blocks such as OTAs, sample&hold circuits, current-to-voltage converters (TIAs), analog-to-PWM converters, Gray counter, registers, SPI interface, multiplexers and an 8-bit DAC are designed and optimized in this technology to meet the requirements driven by photonics specifications. These blocks are contained in a complete multimode ring resonator heater control EIC with more than 800 heater control cells. The switching matrix has 768 elements; therefore efforts have been made to optimize the design of a single driving heater control cell which is further replicated. Also, the design of transimpedance amplifier has been optimized since it is replicated 84 times for the corresponding monitoring photodiodes placed at the key points in the photonic chip. Technological limitations such as maximum speed of the counter clock necessary for the generation of PWM signal and minimum size of the matrix cell area were investigated. The possibilities of scalability of presented solutions by using more advanced technologies for the design of EIC were also one of the foci of this research.

Characterization of different types of microring resonators designed in a photonic platform is also investigated with different control approaches implemented in electronic circuits. Special minimatrix test structures were used for this purpose.

Another major challenge was the design of a compact package of a device capable of conducting heating power of 4 W. The main dissipation comes from PIC, so the cold side of a Peltier cooler is attached to the substrate of PIC while the hot side is connected via metal sheets to the heatsink of the package. Power dissipation of a complete EIC chip, placed above PIC, has to be minimized in order to reduce the influence of heat transfer from EIC to PIC, as well to the air inside the package. Efforts have been made to design proper package heatsink, rather than using an additional fan for cooling.

Two control loops are implemented in the ATMEL ATXmega microcontroller. One loop is for controlling and monitoring of the state of ring resonators. The second loop is for the temperature regulation of EPIC device by driving a thermo-electric cooler since the photonics circuits are very temperature sensitive.

The comparison of control approaches in terms of power consumption, electronic characteristics, scalability and further improvements are also discussed at the end of this work.

Kurzfassung

Es gibt mehrere Forschungsziele, die das Schreiben dieser These angetrieben haben. Das Hauptziel dieser Forschung war die Entwicklung von Steuerkreisen für die Ansteuerung photonischer Komponenten mit hoher Energieeffizienz. In dieser Arbeit wird ein hochintegrierter photonischer Chip mit über 1000 optischen Funktionen über Mikrokupfersäulen auf einem elektronischen IC (EIC) 3D-integriert. Eines der Forschungsziele ist auch, eine hohe Dichte optischer Funktionen pro mm^2 zu erreichen, wobei 1000 optische Funktionen auf 21 mm^2 angestrebt werden. Dieses Integrationsniveau ist sehr hoch, einschließlich Wellenleiterüberkreuzungen, die Anzahl der optischen Funktionen pro mm^2 beträgt 200, im Bereich der Schaltmatrix. Die Funktion der EIC ist, alle photonischen Schalter im photonischen Chip zu steuern. Beide integrierte und zusätzliche diskrete Elektronik sind so ausgelegt, richtig die Einschränkungen in Bezug auf den Stromverbrauch, Energieeffizienz und die Paketgröße der vorgeschlagenen Vorrichtung zu erfüllen. Alle Schritte im Designprozess dieses Geräts werden in dieser Arbeit diskutiert.

Photonische Schalter werden durch im photonischen Chip integrierte Heizwiderstände in Resonanz gebracht. Eines der zentralen Themen dieser Forschung ist die Entwicklung unterschiedlicher Ansätze für die Heizungssteuerung: Analog, Digital oder Analog-Digital werden hinsichtlich Energieeffizienz, Auflösung und Skalierbarkeit untersucht. Zwei Chips, die in verschiedenen Technologien, photonischen und elektronischen, entworfen sind, werden 3D über Mikrokupfersäulen integriert. Die BCD-180-nm-Technologie wurde für das Design des EIC ausgewählt. Kernschaltungsblöcke wie OTAs, Sample & Hold-Schaltungen, Strom-Spannungs-Wandler, Analog-zu-PWM-Wandler, Gray-Zähler, Register, SPI-Schnittstelle, Multiplexer und ein 8-Bit-DAC sind in dieser Technologie ausgelegt und optimiert, um die Anforderungen zu erfüllen angetrieben durch photonische Spezifikationen. Diese Blöcke sind in einer kompletten Multimode-Ring-Resonator-Heizungssteuerung EIC mit mehr als 800 Heizungssteuerzellen enthalten. Die Schaltmatrix hat 768 Elemente, daher wurden Anstrengungen unternommen, um den Entwurf einer einzelnen Heizungssteuerzelle, die weiter repliziert wird, zu optimieren. Außerdem wurde das Design des Transimpedanzverstärkers optimiert, da es 84 Mal für entsprechende Überwachungsphotodioden repliziert wird, die an den Schlüsselpunkten des photonischen Chips angeordnet sind. Technologische Einschränkungen wie maximale Geschwindigkeit des Zählertaktes notwendig zur Erzeugung der PWM-Signals und Mindestgröße der Matrixzellenfläche wurden untersucht. Die Möglichkeiten der Skalierbarkeit der Lösungen durch den Einsatz fortschrittlicher Technologien für das Design von EIC waren ebenfalls ein Schwerpunkt dieser Forschung.

Die Charakterisierung verschiedener Arten von Mikroring-Resonatoren, die in photonischen Plattformen entworfen sind, wird ebenfalls mit verschiedenen Steuerungsansätzen untersucht, die in elektronischen Schaltungen implementiert sind. Spezielle minimatrix Teststrukturen wurden für diesen Zweck verwendet.

Eine weitere große Herausforderung war die Konstruktion eines kompakten Gehäuses, das eine Heizleistung von 4 W ermöglicht. Die Hauptdissipation kommt von PIC, daher ist der Peltier-Kühler mit der kalten Seite an dem Substrat von PIC angebracht, während die heiße

Seite über Metallbleche mit dem Kühlkörper des Gehäuses verbunden ist. Die Verlustleistung eines vollständigen EIC-Chips, der oberhalb von PIC angeordnetet ist, muss minimiert werden, um den Einfluss der Wärmeübertragung von EIC auf den PIC sowie auf die Luft im Gehäuse zu reduzieren. Es wurden Anstrengungen unternommen, einen geeigneten Gehäusekühlkörper zu entwerfen, anstatt einen zusätzlichen Lüfter zum Kühlen zu verwenden.

Im ATMEL ATXmega-Mikrocontroller sind zwei Regelkreise implementiert. Eine Schleife dient zum Steuern und Überwachen des Zustands von Ringresonatoren. Die zweite Schleife dient zur Temperaturregelung der EPIC-Vorrichtung durch Ansteuern eines thermoelektrischen Kühlers, da die Photonikschaltungen sehr temperaturempfindlich sind.

Der Vergleich der Steueransätze in Bezug auf Stromverbrauch, elektronische Eigenschaften, Skalierbarkeit und weitere Verbesserungen werden auch am Ende dieser Arbeit diskutiert.

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To my girlfriend Ana Jovanović, for all the time that I did not spend with her.

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Acronyms

ADC Analog-Digital Converter.

AWG Arrayed-Waveguide Grating.

CMOS Complementary Metal-Oxide-Semiconductor.

cRIO Compact Reconfigurable Input Output.

DAC Digital-Analog Converter.

DC Direct Current.

DMOS Double Diffusion Metal-Oxide-Semiconductor.

EIC Electronic Integrated Circuit.

EPIC Electronic-Photonic Integrated Circuit.

EMI Electromagnetic Interference.

GUI Graphical User Interface.

HF High Frequency.

I/O Input/Output.

MOSFET Metal-Oxide-Semiconductor Field-Effect Transistor.

MSB Most Significant Bit.

MPW Multi-Project Wafer.

MR Microring.

LSB Least Significant Bit.

NI National Instruments.

NMOS n Channel Metal-Oxide-Semiconductor.

PCB Printed Circuit Board.

PIC Photonic Integrated Circuit.

PMOS p Channel Metal-Oxide-Semiconductor.

PXI PCI Extensions for Instrumentation.

PWM Pulse Width Modulation.

SPI Serial Parallel Interface.

RF Radio Frequency.

SNR Signal to Noise Ratio.

SOI Silicon on Insulator.

STI Shallow Trench Isolation.

TEC Thermoelectric Cooler.

TIA Trans-Impedance Amplifier.

USB Universal Serial Bus.

1 Introduction

1.1 Motivation

The amount of data nowadays is rapidly increasing. Companies are collecting trillions of bytes of information about customers' habits and suppliers. In the same time, millions of networked sensors are embedded in devices such as smart phones and automobiles, capturing and processing data. The phenomenon of social networks and multimedia services will support this exponential trend of data generation even more.

The need for high-powered simulations is common in many scientific disciplines, from nanoscale particle physics up to cosmology. For example, simulations of fusion takes in account millions of variables and particle interactions requiring an "exascale" computer system that can perform one quintillion calculations per second. This is equivalent to the combined processing power of the 500 fastest supercomputers present today. This "exascale" computer could lead to significant advances in precision medicine, quantum physics, prediction of earthquakes, weather and the cosmos. These disciplines are all based on complex equations [2].

One of bottlenecks of this computer is the transfer of data from memory to processor and from processor to processor fast enough. Better ways have to be identified to transmit data over novel optical interconnections, shortening data travel paths and to route data more efficiently. Moving data inside supercomputers consumes a lot of power and generates very much heat. It is necessary to develop new optical interconnects since copper and traditional memory protocols cannot provide demanded (needed) transfer rate [3].

Electrical networks continue to scale with new topologies, advances in routing, but there is constant need for lower-power and higher-bandwidth networks. Silicon-photonic technology is well-positioned to offer a solution for these two fundamental weaknesses of electrical links. Proper integration strategies need to be implemented in order to preserve the advantages of optical switches [4]. However, rapidly reconfigurable optical switches with a high number of ports and low insertion loss are still not developed [5]. Switching times of few nanoseconds have been demonstrated with chip-scale optical switches, but their number of ports has been limited to 16 x 16 ports at best [6], [7], [8] and [9]. On the other hand, optical switches based on MEMS mirrors technology with hundreds of ports are used within datacenters and supercomputers [10] but they suffer from microsecond-scale reconfiguration times which makes them an inappropriate choice for big-data application. The main challenge is still in the development of technologies and architectures of optical-networks which can deliver aggressive bandwidth and latency goals.

The photonic switch technology offers unique capabilities that overcome pin-count and power dissipation limitations of electrical networks to deliver the required bandwidth of multiple terabytes per second.

Silicon photonics integration technologies exploit highly developed silicon manufacturing infrastructure, based on the adaptation of fabrication infrastructure for

electronic integrated circuits. This ensures low cost and mass production. High refractive index contrast of silicon enables implementation small footprint optical circuits. Of course, there are some limitations of silicon photonics technology, e.g. light sources are based on InP technology which requires heterogeneous integrated blocks.

Optical switch matrices for data center should allow the connection of an input port to an arbitrary output port. Port count should be as large as possible, however loss and crosstalk increase with the number of ports and matrix complexity limiting scalability.

One of the mechanisms used for optical switching is related to an index change in the refraction of optical waveguides in switching cells. This index variation causes a change of signal direction from one input port to a selected output port.

There are two common physical effects used in silicon photonics optical switching devices: plasma dispersion effect and thermo-optic effect. Response times are quite different, i.e. with the plasma dispersion effect, reconfiguration time is in nanoseconds scale, while with the thermo-optic effect it is in the order of microseconds. Plasma dispersion effect, also called free carrier dispersion effect, used in optical switches, utilize the variation of the refractive index in an optical waveguide influenced by the variation in the free carriers concentration.

By changing waveguide refractive index, optical loss is also affected by generated free carrier absorption. These two effects are coupled by the Kramers-Kronig equation. Plasma dispersion-based switches are implemented as p-i-n junctions operating in forward mode, where waveguide is formed in intrinsic region, in between highly doped p- and n-regions. Free carriers are injected in the intrinsic waveguide area, by forward-biasing the p-i-n junction varying refractive index of the waveguide. Time response of this effect is limited by the carrier diffusion time in the injection area, typically in the nanoseconds range.

The optical switch used in presented matrix is based on thermo-optic effect, which is the topic of this research; therefore it will be analyzed in detail in Chapter 2. The thermo-optic effect is low loss and it is used in optical waveguide switching cells for tuning and switching with very low insertion loss. However, the response time of thermally controlled switches is limited by the heat diffusion process.

Micro-electromechanical system (MEMS) switching cell represents a completely different mechanism for switching in silicon monolithic integrated technology based on physical movement of optical waveguides driven by electrostatic actuators. This technology is widely utilized in consumer electronics gyroscopes and accelerometers in cell phones. The reconfiguration times of this kind of optical switches is typically in the range from 1 to 100 μs. MEMS-based optical switches have large scalability but low reliability, they usually require complex driving circuits, increasing manufacturing costs [11].

In order to achieve small footprint of entire optical switch network, very high density of photonic integration coupled with 3D integrated electronic IC packaging technology is necessary. Each optical path must allow parallel transmission on multiple wavelengths from source to destination in an optical switch plane.

Researcher applied silicon photonics technology to demonstrate 4 x 4 and 8 x 8 port switches with monolithically integrated driver circuits. The switch operates over a large spectral bandwidth with reconfiguration times in nanosecond scale and power dissipation in milliwatt-scale [6]. The challenge of this approach is to scale the number of switch ports, while

difficulties are mainly induced by insertion losses in switch elements, wavelength crossings, I/O coupling, and routing.

Semiconductor optical amplifiers (SOAs) can provide amplification gain over a broad spectrum and multiwavelengths such as Indium Phosphide (InP) optical gain elements. Integration into switch planes is feasible since they can operate with low power dissipation and small footprint. Since SOAs have an active function, a switch driver and control IC should be dedicated to provide electrical power and control for the SOAs.

The design and realization of optical switch matrix with high bandwidth and a high number of ports have numerous packaging challenges. Integration of multiple and different photonic and electronic functions as well as optical coupling. 3D integration of flipped EIC and PIC chips is the packaging approach wherein both photonic and electronic chips are independently optimized for performance, reliability and yield.

Oracle's [12] and ST Microelectronics [13] integrate photonics and electronics chips through face-to-face micro-bump or copper pillar bonding. This approach enables optimized electronics and photonics but with the price of high interconnection parasitics which limit the link performance. One way of reducing this interconnection parasitics is to establish connection through tight-pitch shallow through-oxide vias(TOVs). First the photonic SOI wafer is oxide bonded with the CMOS wafer, then the substrate of the photonic wafer is removed and the connections between the CMOS wafer and the photonic wafer, TOVs are inserted [14]. Estimated parasitic capacitance of the TOV is around 3 fF, while the capacitance of the micro-bump/copper pillar interconnection is 10-15 times larger. The UC Berkeley team developed a through silicon via (TSV) approach for 3D integration electronic and photonic chips. TSVs have more than an order of magnitude larger parasitic capacitance than TOVs because via must traverse the thick silicon substrate rather than thin oxide layers. Very high density of 3D integration, with the pitch of 2-3 μm is achievable with TSV technology [15], and with the pitch of 4 μm with TOVs [16].

There are basically two approaches for integrating photonics with electronics. One approach is hybrid assembly and the other approach is monolithic integration. IHP is developing new monolithic ePIC technology, photonic BiCMOS, integrating high-speed heterojunction bipolar transistors (HBTs) together with photonic integrated circuits based on CMOS process. The integration of BiCMOS transistors with photonics is favorable since complex real-time mixed signals systems require huge digital cores, typically implemented in scaled CMOS technologies. Various bipolar transistor families with maximum transit frequencies up to 190 GHz are offered for the design of high-speed analog circuits. This monolithic technology platform is offering broadband silicon photonics devices such as Ge detectors – lateral PIN diode, depletion type Mach-Zehnder modulators and waveguides. The baseline BiCMOS technology for the integration of photonics is a 0.25μm technology. Backend-of-line (BEOL) interconnect metals are used for connection photonic devices and electronic circuits, eliminating parasitics of pad capacitance and bond-wire inductance. On the other hand, BEOL interconnection between photonic and electronic circuits is economical in comparison to the approaches where electronics and photonics chips are fabricated independently and then packaged [17], [18], [19] and [20].

Researchers from IBM have developed 90 nm CMOS-integrated Nano-Photonics technology where analog and mixed signal circuits are integrated with optical components such

as modulators, photodetectors and wavelength division multiplexing (WDM) filters. A set of passive nanophotonics components integrated into the shallow trench isolation include optical waveguides, directional couplers, WDM filters and vertical grating couplers while a set of analog nanophotonics features includes modulators which require shallow silicon etch and waveguide-integrated Ge PD. Silicon transistors share the same silicon layer with silicon nanophotonics devices. The single-die 25 Gb/s multi-channel WDM optical transceiver built in this technology is demonstrated in [21]. The technology is aimed for building single-chip transceivers with the size of 4x4 mm^2 which can transmit and receive over Terabits per second. The technology is also developed for building a supercomputer that can perform one million trillion calculations or Exaflop per second as a part of Exascale computing program [3].

The motivation for the exploitation of silicon photonics was driven by three main reasons. First, silicon substrates for the fabrication of active photonic devices are two orders of magnitude cheaper in comparison to traditional III-V substrates. Second, silicon photonics manufacturing infrastructure is based on CMOS electronics technology. Third reason is that photonic devices made in silicon allow integration with high-performance electronics [22].

Most important demonstrations system developed in EPIC device fabrication techniques will be described in the following section. The EPIC team from MIT developed a wideband RF channelizer in monolithic technology. Silicon photonics and CMOS electronics were employed in a 150 nm CMOS process. Luxtera team constructed a 4 x 10 Gb/s transceiver for chip-to-chip communication. Hundreds of thousands of transistors were monolithically integrated with tens of optical components. A team composed of Berkley, MIT and the University of Colorado demonstrated a link between a dual core processor and memory. The chip consisted of 850 photonic components and 70 million transistors. Memory bandwidth of 5 Gb/s was achieved at 1.3 pJ/bit [23]. Researchers at Ghent University developed a first-ever electrically driven, completely optical flip-flop. This is a big step to the creation of optical memory on a silicon platform. The technology used includes heterogeneous integrated InP membranes on an SOI platform. A single microdisk laser is coupled to a SOI wire waveguide, demonstrating electrical power consumption of a few milliwatts, switching time of 60 ps with 1.8 fJ optical energy [24]. Large-scale nanophotonic phased array with over 4,000 photonic components was the most complex integrated photonic chip. A static optical phased array of 64 x 64 emitters combined to produce the MIT logo in the far field [25]. The MIT team is working to deliver a fully integrated, LIDAR system in the chip size of 10 mm^2 [22]. US Berkeley fabricated a demonstration system for LIDAR, but focused on electronic-photonic sub-systems, not on non-mechanical beam-steering. The two chips, electronic and photonic chips, were fabricated in different processes and later integrated via TSVs. The electronic chip was fabricated in 180 nm process, while the silicon photonics chip was fabricated in 250 nm technology. The photonic chip contained a Mach-Zehnder interferometer and photodiodes realized on a chip area of 9 mm^2. The result is an 8 μm root-mean-square error at a target distances of ±50 mm [26]. All these project results are illustrating rapidly growing maturity of silicon photonic technology.

Silicon comes up short with optical power handling and optical nonlinearities. On-chip gain for optical amplification and lasing is the main missing component of silicon photonics. This limitation of silicon could be broken through heterogeneous integration of III-V light sources and amplifiers with silicon photonics, silicon nitride passives, and high-performance

CMOS and GaAs driver circuits. A variety of optical components has been enabled by co-integration III-V active media with low-loss silicon photonics. These devices often exceed the capability of a single material. An example would be hybrid Si/III-V semiconductor lasers. By integrating the InP gain medium with silicon photonics technology, a world-record semiconductor laser linewidth of less than 1 kHz has been achieved [27]. The heterogeneous integration approach was also expanded to integrate high-performance electronics chips built from materials such as GaAs and InP.

Vertical-cavity surface-emitting lasers, VCSELs, are used to generate the light signal which is used in most optical transmissions today. In typical optical networks each optical transmission cable needs its own VCSEL and the complete network system consists of a large number of cables needed for the interconnection of all components. From economic reasons it is clear that this approach is not justified. Using optical modulators deeply integrated with the other silicon components in different types of optical interconnect is an example of a better approach, i. e. the cost of expensive lasers is amortized for several optical channels. Researches are building integrated silicon photonic components which can modulate a laser's signal and transmit data down each optical fiber. This direction of integrating several functions into a single photonic component is more efficient than having several different components connected with cables or wires [2].

The MIT team developed an entire library of silicon photonic components, which consists of silicon and silicon nitride waveguides, germanium photodetectors with 1 A/W responsivity, lasers and amplifiers, as well as Mach-Zehnder modulators and tunable filters. The components are developed as parameterized cells (p-cells) at various levels of abstraction. Together with electronic devices these photonics components are combined in photonics-CMOS process design kit (PDK). Verilog timing models of both photonic and electronic devices are included in this PDK [22]. ST Microelectronics also developed highly-sophisticated photonic technology starting with the 300 mm SOI wafer, featuring 310 nm thickness of silicon with a wafer to wafer SOI tolerance of ± 1.85 nm. The thickness of BOX is 720nm. Models and p-cells of devices designed in this technology are integrated into a PDK fully compatible with standard EDA tools. Also, simulation of 3D integrated electrical and optical devices are included [13]. STM demonstrated a 3D E/O transceiver at 56Gbps designed in this PIC25G photonic technology platform [28]. Development of these PDKs give us the capability to design mobile, compact, robust, chip-scale EPIC systems contrary to the large, bulky and expensive systems developed in the laboratory environment.

With described photonic passive and active devices, power amplifiers and memory elements developed in silicon photonics we should have all the elements necessary to build a complete processor in silicon photonics. Their computation power will significantly exceed the performance of standard CMOS processors. The new era of silicon photonics processors is about to come soon.

1.2 Research Goal

There are several research goals which drove the writing of this thesis. The main goal of this research is to develop control circuits for driving photonic components with high power efficiency. In this work, a highly integrated photonic chip, with over 1000 optical functions, is 3D-integrated on an electronic IC (EIC). One of the research goals is also to reach high density of optical functions per mm^2, i.e. the target was 1000 optical functions on 21 mm^2. This integration level is very high, including the waveguides crossings number of optical functions per mm^2 which is 200 in the area of switch matrix. The function of EIC is to control all the photonic switches in the photonic chip. Both integrated and additional discrete electronics had to be designed properly to satisfy the constraints in terms of power consumption, power efficiency and packaging size of the proposed device. All the steps in the design process of this device are discussed in this work.

The photonic switches are brought into resonance by heating resistors, integrated in the photonic chip. One of the central topics of this research is the developing of different approaches to heater control: analog, digital or analog-digital ones had to be investigated in terms of power efficiency, resolution and scalability. Two chips designed in different technologies, photonic and electronic, are 3D integrated via micro copper pillars. The BCD 180 nm technology was available for the design of EIC. Core circuit blocks such as OTAs, sample&hold circuits, current-to-voltage converters (TIAs), analog-to-PWM converters, Gray counter, registers, SPI interface, multiplexers and an 8-bit DAC were properly designed and optimized in this technology to meet the requirements driven by photonics specifications. These blocks are contained in a complete multimode ring resonator heater control EIC with more than 800 heater control cells. The switching matrix has 768 elements; therefore efforts have been made to optimize the design of a single driving heater control cell which is further replicated. Also, design of transimpedance amplifier is optimized since it is replicated 84 times for the corresponding monitoring photodiodes placed at key points in photonic chip. Technology limitations such as maximum speed of counter clock necessary for the generation of PWM signal and minimum size of matrix cell area were investigated. The possibilities of scalability of presented solutions by using smaller technologies for the design of EIC were also a focus of this research.

The characterization of different types of microring resonators designed in a photonic platform is also investigated with different control approaches implemented in electronic circuits. Special minimatrix test structures were used for this purpose.

Table 1-I First estimation of power consumption of EPIC device *[1]*

Circuit	Max power [mW]	Number of circuits
MR resonator in OFF state	2	752
MR resonator in ON state	15	16
Interleaver	70	12
AWG	150	8
EIC	1000	1
Total	**5000**	

Another major challenge is the design of a compact package of a device capable of conducting heating power of 5 W according to Table 1-I. The main dissipation is coming from PIC, so the cold side Peltier cooler is attached to the substrate of PIC while hot side is connected via metal sheets to the heatsink of the package. Power dissipation of a complete EIC chip, placed above PIC, has to be minimized in order to reduce the influence of heat transfer from EIC to PIC, as well to the air inside the package. Efforts have been made to design proper package heatsink, rather than use an additional fan for cooling. The challenge of packaging is to simultaneously satisfy electrical, optical, and thermal design requirements on a small-footprint device, while paving the route to scalable commercial implementation.

Two control loops are implemented in the ATMEL ATXmega microcontroller. One loop is for controlling and monitoring the state of ring resonators. The second loop is for the regulation of the temperature of the EPIC device by driving a thermo-electric cooler since the photonic circuits are very temperature sensitive.

The comparison of control approaches in terms of power consumption, electronic characteristics and scalability and further improvements are also discussed at the end of this work.

1.3 Related Work (State of the Art)

Optical transport networks are evolving to sustain the increase in the traffic demand and the technological bottlenecks and operational rigidities that are still present in current optical switching nodes of the metro and core transport networks. These limitations will be removed to allow a reduction of operational costs, permit the optimization of transport resource utilization and support re-routing functions in the event of faults in a cost effective manner. Next generation reconfigurable add and drop multiplexer (ROADM) will be provided with flexibility at the end points where the transponders are interconnected to the switching node and there, the rigid wavelength multiplexers and demultiplexes will be replaced by transponder aggregator switches (TPA). Although commercial TPAs have been implemented using the PLC (Planar Lightwave Circuits) technology [29], [30] and recently, a new TPA architecture integrating a number of wavelength selective switches using a combination of spatial and planar optical circuits (SPOC) has been presented in [31], author thinks that VLSI technologies, and in particular silicon photonics, are more attractive for cost, size, energy efficiency and performance reasons. A silicon photonics based TPA has been already demonstrated in [32] but it is based on a multicast switch architecture and needs additional external tunable optical filters or coherent receivers to select the proper wavelengths at the transponder input.

IRIS switch is a wavelength selective TPA implemented with silicon nano-photonics, working without the need of additional external components (like tunable filters). The TPA presented here allows colorless (add/drop switching structure is not color specific), directionless (a wavelength can be added/dropped to/from any direction), and contentionless operation (adding/dropping in one direction does not produce contentions for other directions). [33] It has the highest level of scalability and miniaturization, being based on very small SI micro-ring (MRR) switch elements, but its circuits also present the drawback of being polarization sensitive and its final design should adopt polarization diversity architectures to

achieve a low polarization dependent loss (PDL), as required by most of system applications. The presented device can be used either as add TPA or drop TPA and it has four line ports for reception or transmission toward the network and eight local ports for adding or dropping local wavelengths.

In drop configuration, a comb of wavelengths received from the network is demultiplexed in two stages, first by interleavers, and second by array waveguide gratings (AWGs), prior to entering the optical crossbar matrix (48x16) of MR switch elements where individual wavelengths are switched to the drop ports. In ADD configuration, the wavelengths to be added to the network, connected to the add ports, are individually switched by the optical crossbar matrix toward the proper output multiplexer before being sent to the output line port.

A comparison with commercial and new types of TPA is presented in Table 1-II.

Table 1-II. Performance summary and TPA comparison with recent publications *[33]*

	This work: 4x8 Silicon Integrated TPA	**8x8 Enablance TPA** [29]	**8x8 Splitter-Switch TPA** [30]	**8x24 SPOC TPA** [31]	**8x8 Silicon Integrated TPA** [32]
Architecture	**Matrix of Microring Resonators (MR)**	**Multicast Switch**	**Multicast Switch**	**WSS-type**	**Multicast Switch**
Technology	**Silicon Nano-Photonics**	**Planar Lightwave Circuits**	**Planar Lightwave Circuits**	**Spatial and Plana Optical Circuits**	**Silicon Photonics with thicker rib waveguides**
Size (mm)	**8.4x7.8**	**180x140x16 (packaged)**	**110x15**	**72x28 (front end only)**	**12x14**
Loss (dB)	**15**	**13.4**	**11.7 (average)**	**16.2 (average)**	**10.7-20.5**
Response Time (µs)	**4**	**6000**	**Tens ms range (not reported)**	**Tens ms range (not reported)**	**20**
Crosstalk (dB)	**-35**	**-40 (Switch only)**	**-40 (Switch only)**	**-20.5**	**-35 (Switch only)**
PDL (dB)	**High**	**0.4**	**Low (not reported)**	**Low (not reported)**	**0.6**
Notes		**Needs tunable filters**	**Needs tunable filters**	**Integrated front end assembled with free space optics components**	**Needs tunable filters**

Different types of the high radix silicon photonic switch matrices demonstrated so far are MEMS based, ring resonator based and Mach-Zehnder based. There is no reported 3D integration like the one on IRIS project in the literature so far. IBM used the approach based on monolithic integration of CMOS electronic with all photonics in the same chip for switch matrices [34]. They demonstrated only a 4x4 switch but with intention to use this technique with larger matrices.

In [35], a 32x32 switch matrix based on Mach-Zehnder switching cells is presented. For the integration, they have used a ceramic LGA (Land Grid Array) interposer that converts the pad arrangement on the chip with 180 µm pitch into 500 µm pitch LGA array of pads which are further connected to a mother board where electronic circuits are placed.

An 8x7 switch matrix based on micro-ring resonators controller by heaters is presented in [36]. The heaters are wire bonded to the pads placed at the periphery of the PIC and it is clearly not a scalable solution.

Scalable silicon photonic MEMS switch uses the technique of routing electrical contacts to the edge of the chip for access to wire bonding [37] it looks simpler than [35] and [36] approaches, but it does not allow for high density interconnection and does not look like a promising candidate for mass production.

This is first time that a complete EIC ASIC for control of the switches is developed so far for a big matrix since the demos were focused on the PIC not on electronic circuits. In these demo PICs switches have been controlled with external voltage/current sources with the only purpose to verify optical performances (loss, crosstalk, time response etc.). In [34], there are the details of the monolithically integrated CMOS logic and switch drivers used by IBM to drive the 4x4 MZI switch matrix with nanosecond response time. Their matrix is very fast since it is targeted for optical packet switching, not circuit switching using electro-optic effect instead of a thermo-optic effect like in IRIS. A single tunable silicon photonic ring modulator with integrated ultra-efficient active wavelength control is presented in [38]. The fine tuning of the ring resonance to a desired wavelength is controlled with high precision by driving the current through an integrated metal resistor. A 15-bit DAC with a current output, realized on area of 650 μm^2, is used to drive the resistor with maximum output power of 8 mW.

In conclusion, IRIS switch matrix is the first real demonstration of 3D integration of a PIC optical matrix with an EIC control ASIC. The IRIS project is a real technological advancement for the high integration scale, for 3D integration and high energy efficient EIC. However, the device is not yet mature for a system application due to polarization sensitivity and losses, but it represents a big step forward.

In Data Centers, hundreds of processors are interconnected with data storage servers to process the data with high bandwidth. IRIS optical switching device finds purpose as switch in data exchange between the nodes. Besides data centers, IRIS optical switching device is aimed to find application also in 5G networks, optical transport networks, and high performance computing [1].

1.4 Thesis Organization

Chapter 2 begins with the architecture of optical switch matrix and the description of the photonic components used in optical switch matrix and then progresses towards deriving specifications for control electronic circuits. The chapter ends with a description of characteristics of Ge monitoring photodiodes used for monitoring states of ring resonator switches and temperature measurement.

Chapter 3 is dedicated to the technologies used for the design of electronic and photonic chips. Also, the process of 3D integration of these two chips is described.

Chapter 4 deals with the packaging challenges and setup for the measurement of EPIC device. Three techniques for driving a thermoelectric cooler are investigated. Implementation of the control loop for setting heater power, monitoring photodiodes and regulating temperature in the microcontroller is also described. Electrical and photonic measurement results of the packaged EPIC device are also presented in this chapter.

In Chapter 5 a set of techniques for the control of ring resonator heaters in photonic by electronic circuits is developed. Circuits, simulations, measurement setup and characterization results of three approaches, analog, digital and hybrid with and without an 8bit DAC converter,

are described. Deep analysis of the advantages and disadvantages of each approach as well as technology limitations are discussed.

In Chapter 6, conclusions are drawn and the comparison of power consumption of all control approaches is presented. Potential topics for future improvements and research are suggested.

2 Photonic Components

2.1 Architecture of the System

Architecture of the integrated TPA is presented in Figure 2.1. while the block diagram of the electronic-photonic system is shown in Figure 2.2. The same device can work in two configuration: drop and add. Common architecture enables simply inverting the direction of optical flows so we have the function of dropping WDM channels from input ports to local drop ports and the function of adding WDM channels from local add ports to output ports [39], [40], [41], [42], [43].

In the drop configuration, four sets of up to 12 WDM channels with 200 GHz spaced, arrive at each of the four input line ports. They are coupled by single polarization grating couplers (SPGC). Further, with Interleaver blocks, input channels are separated into odd and even channels increasing wavelength spacing inside the switch matrix. At the same time, channel isolation requirements are relaxed. Then, with two types of demux blocks, odd and even channels are separated. From the output of demultiplexer the signals are sent to the switching matrix with the optical crossbar of microring resonator switch elements. The matrix is constituted of 4 x 12 rows and 8 x 2 columns, which are drop ports connected to optical receivers [44]. So, the demultiplexed signal travels on a row through the switching matrix until the cross point where it switched to the column connected to drop output port. At the cross point the signal is coupled to the resonator, built from one or two microrings, which are thermally tuned to the resonance with the signal wavelength. Two waveguides are combined by Interleaver again at the drop port, one working with odd wavelengths while the other one with the even wavelengths. Then, the drop port is coupled with SPGC to an optical fiber.

In the Add configuration, the WDM signal is added through eight tunable transmitters to the chip coupled by the SPGC. Function of the Interleavers at each Add input port is to direct the odd and even wavelengths to the proper columns in the switch matrix. Only the ring resonators at the cross point with proper direction to which the signal has to be added are activated. All the other ring resonators in the matrix are turned off. In this way, the signal is deviated horizontally toward the output multiplexer reaching Interleaver. Again, odd and even wavelengths are combined to the same output fiber [44].

Monitor photodiodes are placed at key points, input and outputs to enable monitoring the function of different blocks.

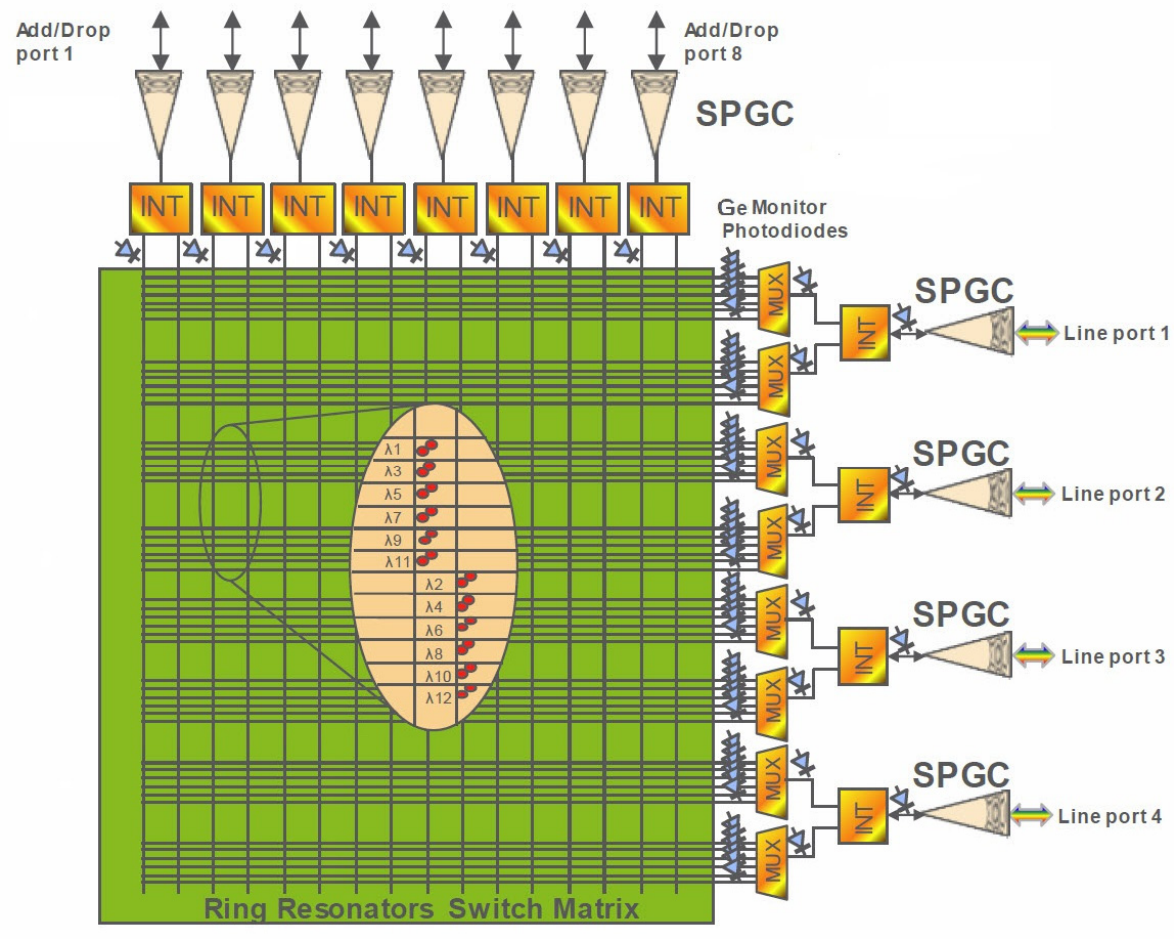

Figure 2.1: Architecture of IRIS TPA *[44]*

The function of channel interleavers is to relax the requirements of the demultiplexer. The design is based on infinite impulse response filters composed by a ring resonator in one branch and a Mach-Zehnder interferometer [45]. They include two independent heaters which allow the adjustment of tuning and phase balancing. Both heaters are controlled by the EIC through copper pillars. There are two version of Interleaver block, one with equal heater resistances of 46 Ω and another one with the resistance of 40 Ω and 80 Ω. Power dissipation of one Interleaver block is expected to be 70 mW.

After the channels are interleaved, the signals are further demultiplexed by Arrayed Waveguide Gratings (AWGs) to enable switching of each channel independently [46], [47] and [48]. The AWG is designed with the channel space of 400 GHz. Insertion loss is < 3 dB, and channel isolation is > 25 dB. These devices include the so-called “whiskers”, i.e. waveguide extensions at the unused boundaries of the star couplers to reduce back-reflections [44]. The temperature-dependent wavelength shift of the waveguides is experienced by the AWG. Special design techniques based on negative thermo-optic coefficient were used in order to reduce thermal shift [49] and [50].

Fine-tuning of the AWG channel-output is provided by four metal heaters placed over the structure of AWG to allow equal heating. The current through each of the heaters should not exceed the maximum value of 47 mA. Resistance value of the implemented heaters is 38.2 Ω, and the expected power consumption of one AWG block is around 42 mW. Each of the four heaters is independently controlled by the EIC through copper pillars. FSR (Free Spectral Range) of the AWGs is around 24 nm whereas one of the ring switches is 19 nm. Both ring switches and the AWGs are periodic. Micrograph of the PIC full matrix chip with the main blocks marked is presented in Figure 2.3.

Passive photonic components, such as waveguides, waveguide crossings, and grating coupler structures are also a part of the presented photonic device. They are marked on the micrograph of PIC, shown in Figure 2.4.

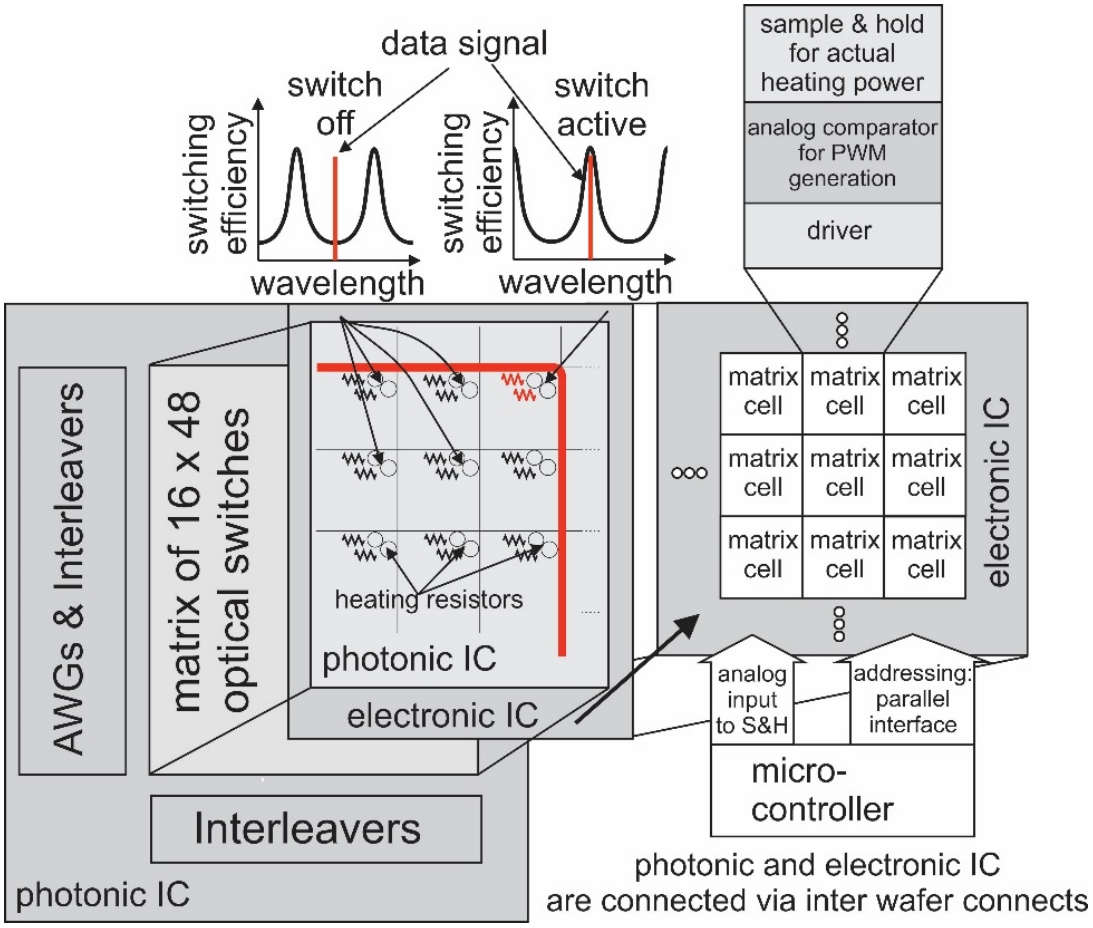

Figure 2.2: Block diagram of the complete EPIC device, with implementation of improved hybrid approach for control of heaters in PIC *[51]*

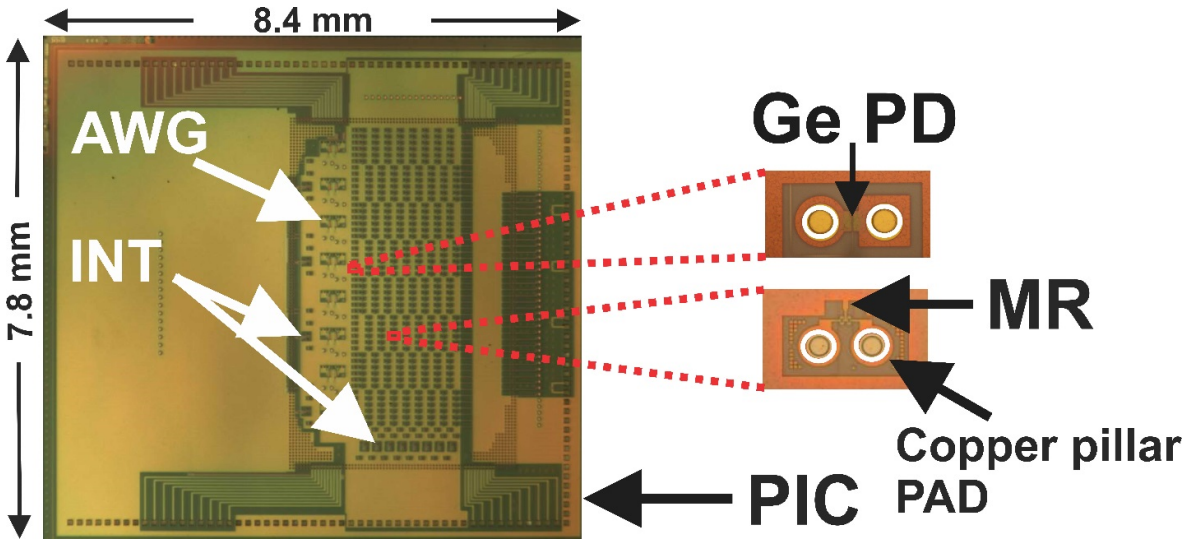

Figure 2.3: Micrograph of PIC full matrix chip with marked main blocks *[33]*

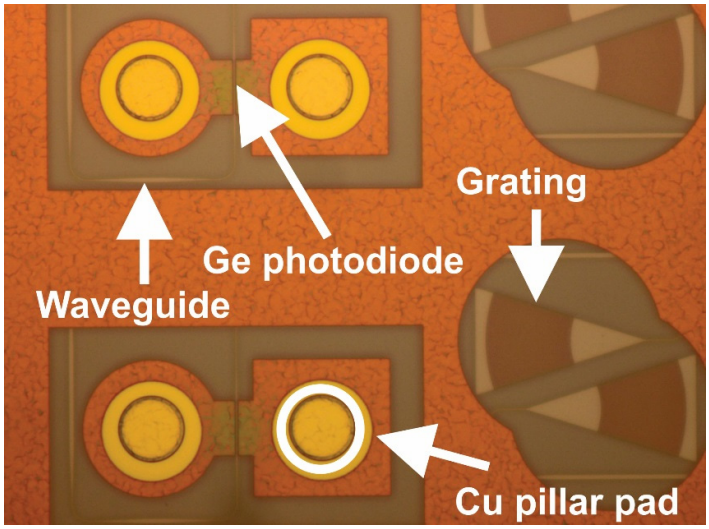

Figure 2.4: Zoomed in micrograph of PIC with Germanium photodiodes, fiber grating couplers, waveguide and copper pillar pad

2.2 Principle of Thermal Switch, i.e. Ring Resonator Switch

The principle of a single ring resonator optical switch shown in Figure 2.6 is based on the thermal change of refraction index.

To find out the tunability of the switch we have to start from the ratio between the applied dissipated power P_D and the corresponding resonance wavelength shift $\Delta\lambda$ [52]. If we introduce the average temperature variation in the ring as ΔT in the ration, we can write the following equation:

$$\frac{P_D}{\Delta\lambda} = \frac{P_D}{\Delta T}\frac{\Delta T}{\Delta\lambda}, \quad (1)$$

In the following equation $\frac{P_D}{\Delta T}$ stands for the transfer of heat from the heater to the ring-resonator per unit time and it is efficiency dependent. Ration $\frac{\Delta T}{\Delta\lambda}$ is dependent of the optical properties of the ring with temperature variation. Ration $\frac{P_D}{\Delta T}$ increases with the increase of the cross-sectional area (the area which is perpendicular with the path of the heat flow) and it is reversely proportional to the distance between the heater and the ring. Of course, thermal conductivity of the material between the ring and the heater is directly proportional to the heat transfer.

The following equation give us the relation between the resonance wavelength shift $\Delta\lambda$ and the temperature variation ΔT:

$$\frac{\Delta\lambda}{\lambda} = \frac{1}{n_g}\left(\frac{\delta n_{eff}}{\delta n_{core}}\frac{\delta n_{core}}{\delta T} + \frac{\delta n_{eff}}{\delta n_{clad}}\frac{\delta n_{clad}}{\delta T}\right)\Delta T, \quad (2)$$

In this equation λ is the resonant wavelength of the ring resonator, n_{eff} is the effective and n_g is the group index of the mode. Variations of the effective index with respect to the core and cladding refractive indices are marked with $\frac{\delta n_{eff}}{\delta n_{core}}$ and $\frac{\delta n_{eff}}{\delta n_{clad}}$, respectively. Quotients $\frac{\delta n_{core}}{\delta T}$ and $\frac{\delta n_{clad}}{\delta T}$ are refractive index changes respect to the temperature. Quotients $\frac{\delta n_{eff}}{\delta n_{core}}$ and $\frac{\delta n_{eff}}{\delta n_{clad}}$ are dependent on the core-cladding refractive index contrast, while $\frac{\delta n_{core}}{\delta T}$ and $\frac{\delta n_{clad}}{\delta T}$ depend on the characteristic of materials. In SOI technology, the values of $\frac{\delta n_{core}}{\delta T}$ and $\frac{\delta n_{clad}}{\delta T}$ are $2\cdot10^{-4}\frac{1}{℃}$ and $1\cdot10^{-5}\frac{1}{℃}$.

For TE (transverse electrical wave) fundamental mode at λ=1550 nm, on applying cylindrical mode solver, the computed values of n_{eff}, n_g, $\frac{\delta n_{eff}}{\delta n_{core}}$ and $\frac{\delta n_{eff}}{\delta n_{clad}}$ are:

$$n_{eff} = 2.37,\ n_g = 3.8,\ \frac{\delta n_{eff}}{\delta n_{core}} = 0.25 \text{ and } \frac{\delta n_{eff}}{\delta n_{clad}} = 1. \quad (3)$$

Calculated free spectral range of proposed ring resonator is then: $FSR = \frac{\lambda^2}{2\pi R n_g} = 20.12\ nm$. Where R is ring radius with the value of R=5 µm.

When we replaced the calculated values from Eq. (3) to Eq. (2) we got a wavelength shift of 0.0833 nm (which corresponds to a frequency shift of 10 GHz) for a temperature

resolution of 1 ℃ (or K). Dependence of resonance wavelength shift versus temperature variations is shown in Figure 2.5.

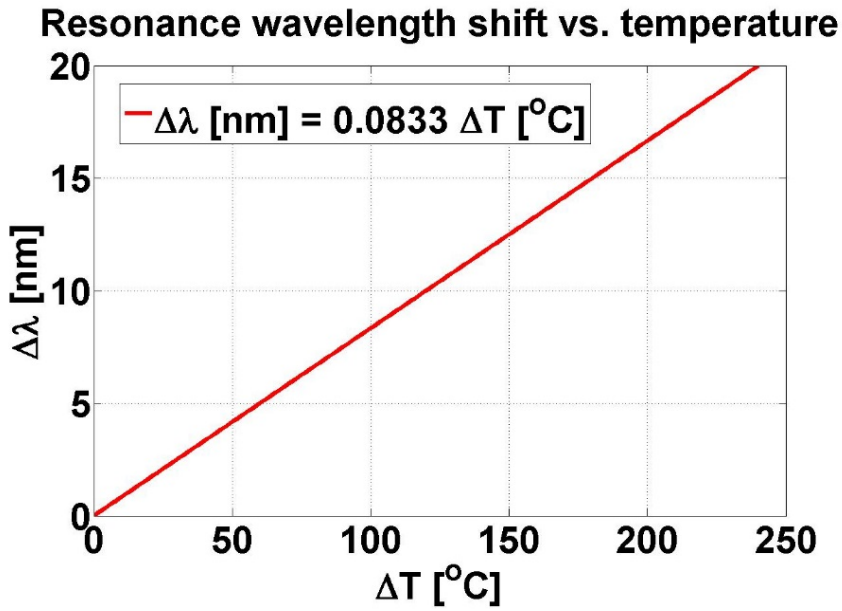

Figure 2.5: Function of resonance wavelength shift of the thermal tuning *[52]*

2.3 Single vs. Double Rings

The micro-ring-resonator switch is the most important element of the matrix [53], [54], [55], [56]. It requires very high channel isolation (>35 dB), low insertion loss, and energy efficiency [57]. Single micro-rings or higher-order filter built from cascading several micro-rings could be used. The examples of geometries are shown in Figure 2.6. The main advantage of the single micro-ring is lower power consumption, since only one micro-ring has to be tuned by heating. However, specified minimum channel isolation (35 dB) is not achievable with a single micro-ring. A filter made with two micro-rings can fulfill the required channel isolation with the very narrow channel width of 14 GHz at 1 dB. The price is paid with double power consumption, due to the fact that two elements need to be tuned. In addition, a filter of the second order requires identical optical paths in both rings, which is difficult to be fulfilled since fabrication deviations introduce asymmetries either in heater geometry or in the waveguide. This requires independent heating of both micro-rings.

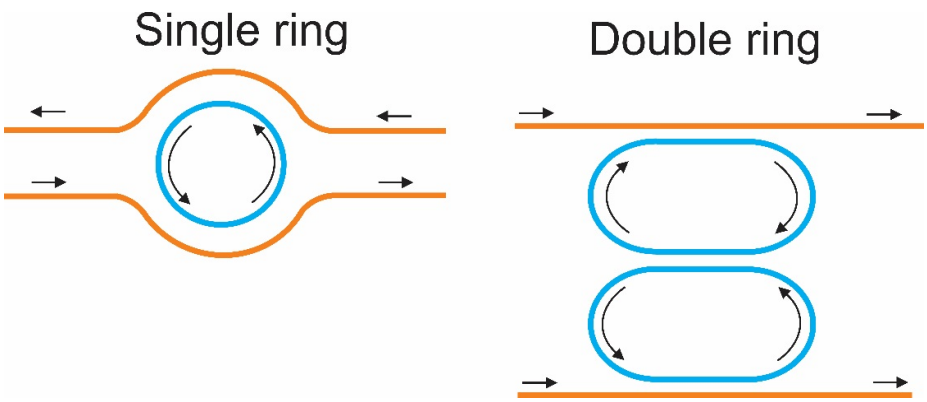

Figure 2.6: Single and double micro-ring geometries *[44]*

The fabricated single-micro-ring, is fully-etched circular ring with the radius of 5 μm and the width of 480 nm. Curved couplers are used, as with straight couplers it is not possible to achieve such a high coupling coefficient [58]. On the other hand, the double micro-ring consists of two fully-etched racetrack resonators with straight couplers and the coupling length of 2.2 μm.

2.4 Ring Heaters used in Photonics IC

The best fabricated integrated double ring heaters had the power consumption of ~35mW/FSR/ring, while the best metallic double ring heaters consumed ~22mW/FSR/ring [59]. So, the metallic heaters are more efficient [60].

The results from the ring characterization showed a good filter response and good tuning range and efficiency. In particular, tuning range was about 15nm (aimed 11nm), and consumption was about 22mW/FSR/ring for the double-ring filter, while tuning range of 11nm and 28mW/FSR was met for the single ring heater, all above the specified minimum of 8nm [59].

The characteristics of the different heater types are listed in Table 2-I, for applied voltages of 1.8V and 5V.

Table 2-I Integrated heater performance for applied voltages 1.8V and 5V. *[52]*

Structure	V (V)	I_{max}(mA)	P= $V*I_{max}$ (mW)	R (Ω)	ΔT (°C)	P/ ΔT (μW/°C)	P/Δλ (mW/nm)	P/FSR (mW/FSR)
Basic (MMR-NoC)	1.8	0.603	1.08	2985	10	107.0	1.28	25.8
Basic Optimized	1.8	1.599	2.879	1125.4	23.96	120.15	1.4418	28.8360
Internal heater	1.8	4.738	8.529	379.9	73.14	116.61	1.3993	27.9864
Interdigital contact	1.8	24.159	43.487	74.5	368.63	117.97	1.4156	28.3128
Metallic heater	1.8	16.66	30	108	240	125	1.42-1.66	30
Integrated silicide heaters	1.8	9.66	17.34	186	108	160	1.92	37.5
Basic	5	4.443	22.214	1125.4	184.88	120.15	1.4418	28.8360
Internal heater	5	13.161	65.807	379.9	564.35	116.61	1.3993	27.9864
Interdigital contact	5	67.114	335.57	74.5	2844.34*	117.97	1.4156	28.3128

*too high temperature, since the melting point of silicon is at 1414 °C

The corresponding values for Table 2-I for the applied voltages of 1.8V and 5V are calculated applying the following equation [52]:

$$\boldsymbol{P_d = \frac{(\Delta V)^2}{R} = \frac{\Delta T}{R_{th}}}, \tag{4}$$

in which R represents electrical resistance, while R_{th} represents thermal resistance.

From Eq. (4) we can derive an expression which describes the resolution of voltage in dependence of temperature spacing:

$$\boldsymbol{\Delta V_{min} = \Delta V_{max} \cdot \sqrt{\frac{\Delta T}{\Delta T_{max}}}}. \tag{5}$$

2.5 Ring Resonators with Metallic Heater

The TiTiN metal layer used for the metallic exhibits a very uniform sheet resistance of 6.3±0.3 ohms/square. The total resistance of the heater is about 100Ω , but the value increases with respect to the voltage or current supply (see Figure 2.7). Up to a voltage supply of 2.5V, the heating power reaches 40mW which allows for tuning the ring over more than 1 FSR (19nm). This means that the thermal shifting efficiency is in the range of 0.6-0.7nm/mW.

The resistance of the metallic heater varies with the different applied currents as it is shown in Figure 2.7 (left). This is also reflected to the characteristic of heating power in function of voltage supply, shown in Figure 2.7 (right). If heater resistance is constant, PWM approach of driving it would give us linear dependence of heating power with duty cycle (D) by equation $P = D \cdot \frac{Vdd^2}{R}$.

However, heater resistance is the function of power $\bar{P} = D \cdot \frac{V_{dd}^2}{R(\bar{P})}$, and the control variable, duty cycle, can then be calculated with the following formulae: $D = \bar{P} \cdot \frac{R(\bar{P})}{V_{dd}^2}$.

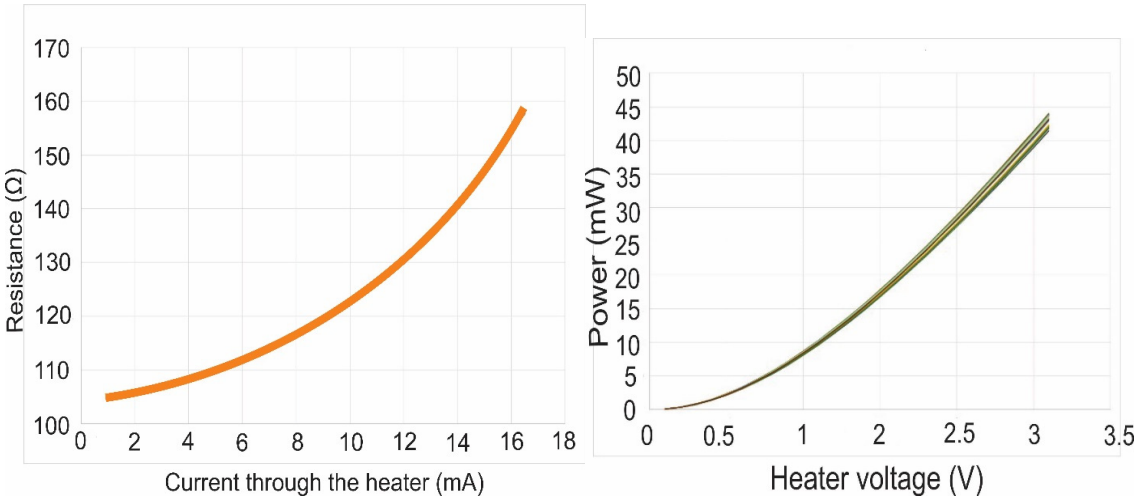

Figure 2.7: Heater resistance as a function of current supply (left) Heating power with respect to the voltage supply (right) *[59]*

2.6 Minimum Resolution and Maximum Range for Tunability for Resonance Wavelength Shift

Since ΔT is proportional to the ΔV^2 we can derive the minimum and maximum voltages necessary for minimum resolution and maximum tunability of the ring resonator.

Frequency spacing (resolution) is connected with wavelength spacing (resolution) with the following relation $\Delta\nu=c*\Delta\lambda/\lambda^2$. Replacing the values for wavelength of 1550 nm, we have $\Delta\nu=1.25e20\cdot\Delta\lambda$. Putting relation between wavelength spacing and temperature spacing, $\Delta T[℃] \approx 12 \cdot \Delta\lambda[nm]$ we can fulfill Table 2-II:

Table 2-II: Resonance wavelength shift, resonance frequency shift and temperature variation *[52]*

	ΔT [℃]	Δλ [nm]	Δν [GHz]
Resolution	0.12	0.01	1.25
Resolution	0.24	0.02	2.50
ITU grid x1	9.6	0.80	100
ITU grid x2	19.20	1.60	200
ITU grid x4	38.40	3.20	400
1 FSR (20 nm)	240	20.00	2500

Combining the resonance wavelength shift from Table 2-II with Eq. (5) we can calculate the voltage necessary to be applied for the corresponding wavelength shift. The results are shown in Table 2-III.

Table 2-III: Resonance wavelength shift with respect to the temperature and applied voltage of 1.8V *[52]*

	Voltage resolution, ΔV [V]			Frequency shift Δν [GHz]	Temperature space ΔT [℃]
	Basic	Full	Interdigital		
Resolution	0.1274	0.0729	0.0325	1.25	0.12
Resolution	0.1802	0.1031	0.0459	2.50	0.24
ITU grid x1 [63]	1.1394	0.6521	0.2905	100	9.6
ITU grid x2	1.6113	0.9222	0.4108	200	19.20
ITU grid x4	NA	1.3042	0.5810	400	38.40
1 FSR (20 nm)	NA	NA	1.4524	2500	240

*NA – not applicable, since the maximum applied voltage is 1.8V

According to Eq. (5) and the values from Table 2-III we can make a conclusion that for fixed wavelength shift $\Delta\lambda$, minimum wavelength shift (resolution) increases proportionally with the applied voltage and also has larger values for larger values of heater resistance. However, higher resistance limits the tuning range ΔT_{max}, and resolution of the applied voltage is inversely proportional to it: $\frac{1}{\sqrt{\Delta T_{max}}}$. Ideally, for this purpose, the resistance of 230 Ω would give us the tuning range of 240 ℃ (20 nm) for the applied voltage of 1.8 V. So, for resistances of the heater lower than this value we have a larger tuning range that is necessary, and for the same resolution the voltage step, LSB, will be smaller.

Of course, maximum applied voltage depends on the chosen technology for the design of electronics. BCD8sp technology has the fastest transistors with the minimum voltage of 1.8 V, and also, slower 5V transistors are available (see Chapter 3). For PWM control of heaters, the resolution of the applied voltage is calculated using the following formulae:

$$\Delta V_{min} = \frac{\Delta V_{max}}{2^n},$$

in which n represents the number of bits. So, for 8 bit resolution we have the voltage step to apply of:

$$\Delta V_{min,1.8V} = \frac{1.8V}{2^8} = 7\ mV,$$

$$\Delta V_{min,5V} = \frac{5V}{2^8} = 19.5\ mV,$$

for 1.8 V and 5 V, respectively.

2.7 Transient Analysis of Ring Resonators

For computation of requirements for minimal PWM frequency for the control of microrings and resolution some assumptions should be taken. The first assumption taken is that the temperature has the first order response which is described by the following equation [62]:

$$\boldsymbol{\Delta T(t) = \Delta T_{max} \cdot \left[1 - e^{-\frac{t-t_{off}}{\tau}}\right]} \quad (6)$$

The electrical switch is considered to be ideal. The worst case time constant τ for all heater structures is 3.30 μs [52]. Zero value of PWM signal (duty ration of 0) corresponds to off state, i.e. no current through the heater of the microring, and the duty ratio of 1 means that the current is applied to the heater for the entire period.

Figure 2.8 shows the results of simulation for peak-to-peak temperature ripple vs. duty ration of PWM signal, for different frequencies of PWM signal (f_{PWM}) for the PWM approach of thermal regulation of ring resonators. For this purpose, tuning range was set to be from 0 to 96 ℃, which corresponds to 8 nm. This means that when duty cycle of PWM signal is 1, we have ΔT=96 ℃. As we expected, temperature ripple is the largest in PWM duty cycle of 0.5, i.e. the case when PWM signal is symmetrical rectangular signal, shown in Figure 2.9.

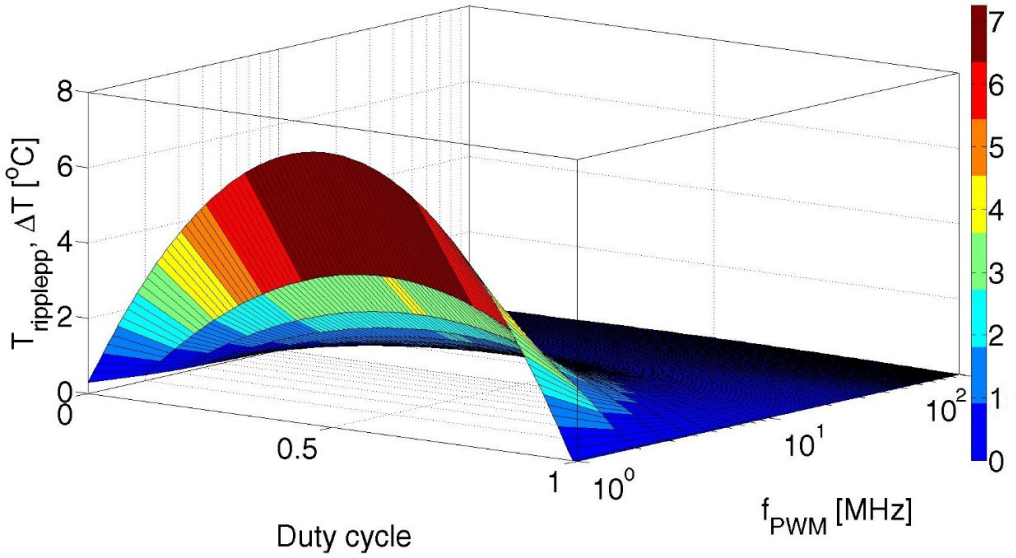

Figure 2.8: Temperature ripple induced by PWM control, dependence of duty cycle and PWM frequency for tuning range of 8 nm *[62]*

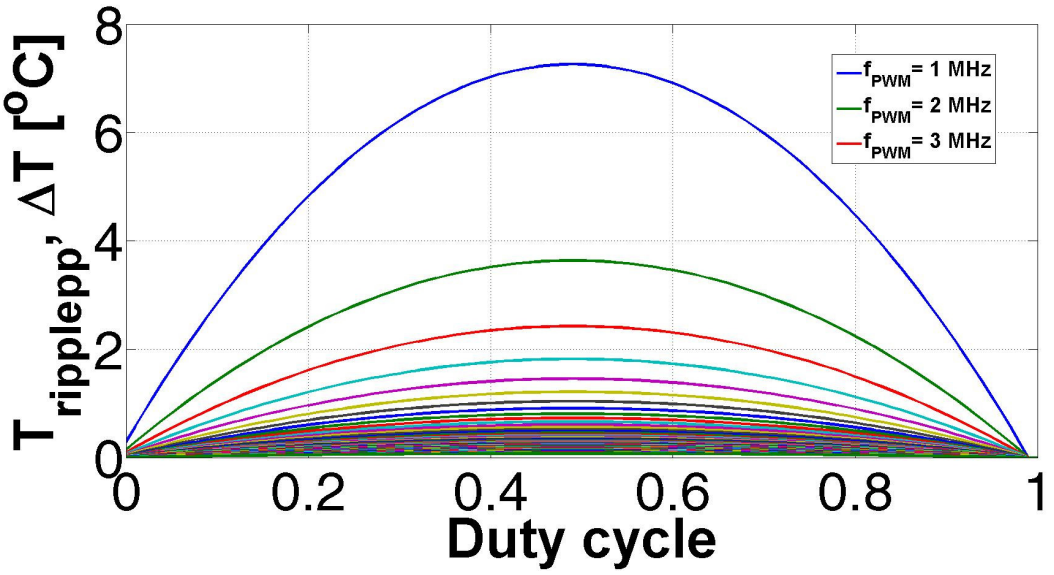

Figure 2.9: Temperature ripple vs. duty cycle for different PWM frequencies *[62]*

Simple analytical relation between f_{PWM} and $T_{ripple,pp}$ can be derived for this worst case [62]:

$$T_{ripple,pp} = \Delta T_{max} \frac{1-e^{-\frac{1}{2f_{PWM}\tau}}}{1+e^{-\frac{1}{2f_{PWM}\tau}}} \qquad (7)$$

With Eq. (7) we can plot Figure 2.10. Temperature ripples for the tuning range of 8nm are shown. In the same figure, Figure 2.10, minimum temperature steps for three different tuning resolutions ($\Delta\nu_1$=1 GHz, $\Delta\nu_1$=4 GHz, $\Delta\nu_1$=10 GHz,) are shown.

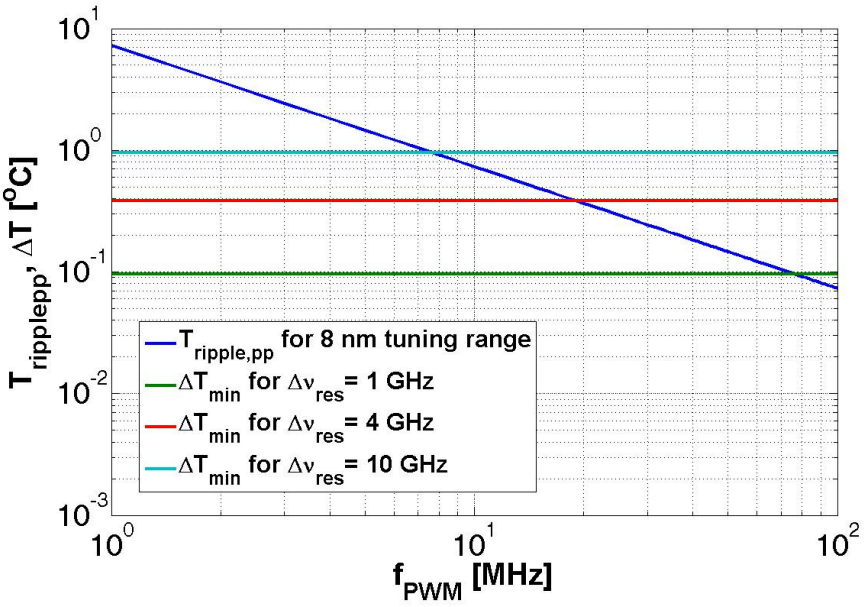

Figure 2.10: Temperature ripple depending on the PWM frequency for PWM duty = 0.5 for different tuning resolution *[62]*

From Figure 2.10 we can calculate cross sections which define the area in which we have temperature ripple lower than the maximum given temperature ripple (that corresponds to wavelength ripple) for the tuning range of 8nm. In Table 2-IV the necessary PWM frequency, f_{PWM}, the necessary number of bits for PWM and the resulting counter frequency are presented. The number of bits for the PWM is chosen in a way that wavelength resolution is smaller or equal to wavelength ripple.

Table 2-IV: Wavelength ripple, required minimum PWM frequency, number of bits and resulting counter frequency for 8 nm tuning range *[62]*

Δλ – wavelength ripple [GHz]	Required f_{PWM} [MHz]	# of bits for PWM	f_{MAX} [GHz]
1	75.76	10	77.6
4	18.94	8	4.9
10	7.58	7	0.969

The values of counter frequencies 77.6 GHz and 4.9 GHz are too high for the technology used for the design of electronics. Finally, the minimum resolution of wavelength of 10 GHz and the tuning range of 8 nm are selected. The corresponding minimum PWM frequency of 7.58 MHz, with 7 bits of resolution and minimum clock frequency of 970 MHz are chosen for the design of electronic control circuits. All photonic components are designed to have tuning ranges which could be achieved with the supply voltage of 1.8 V. This means that the heaters of Interleavers and AWGs are split in order to achieve the necessary tuning range with this supply.

2.8 Transient Simulations

Figure 2.11 shows the step response of temperature after the applied PWM signal change from the duty cycle of 0 to 0.5 for three different PWM frequencies. The zoomed in temperature ripple for three different PWM frequencies is shown in Figure 2.12.

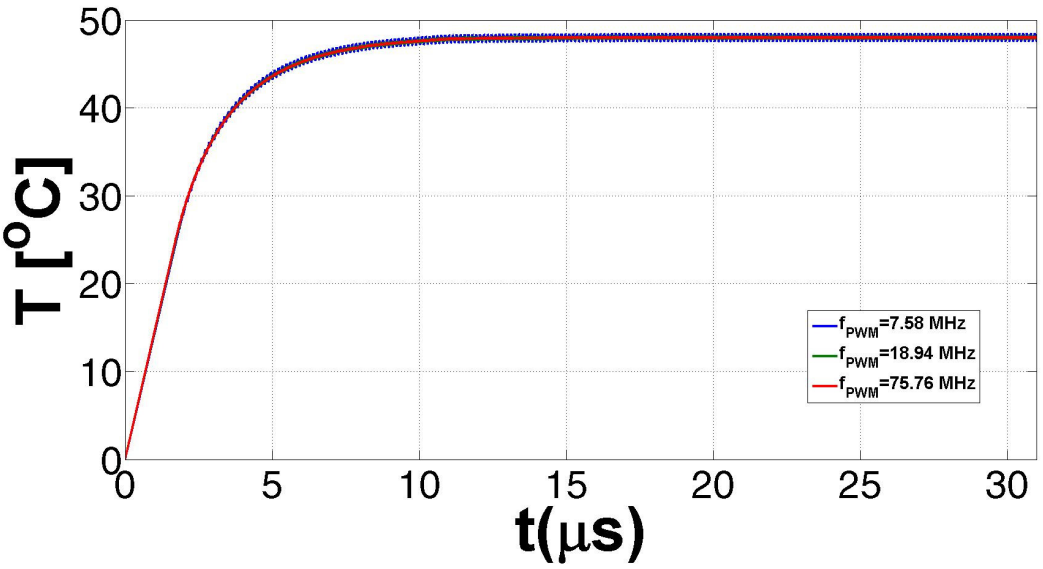

Figure 2.11: Temperature transient after a step change of PWM signal from 0 to 50 for a tuning range of 8 nm *[62]*

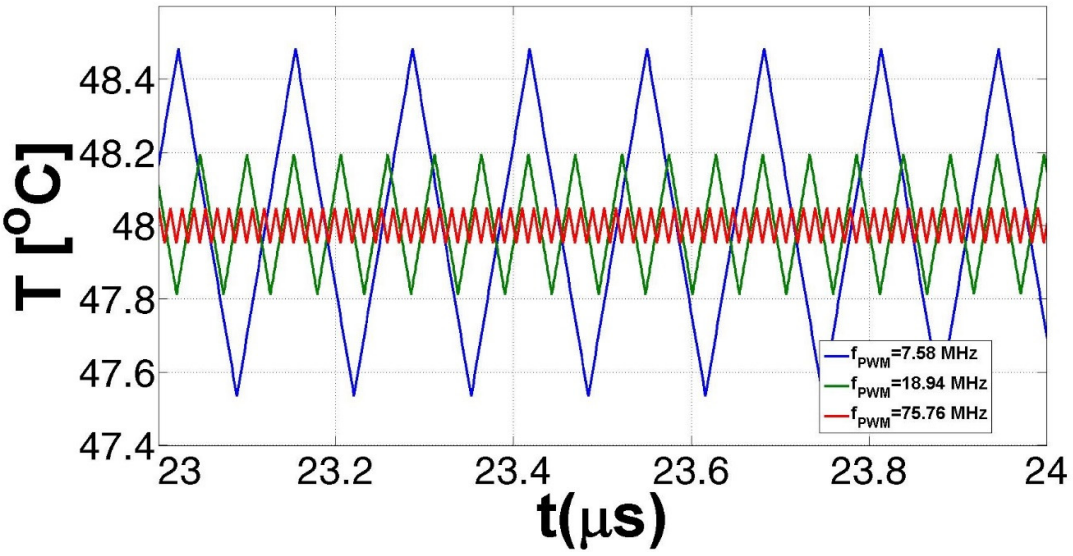

Figure 2.12: Zoomed in temperature ripple after settling time *[62]*

2.9 Design of Driver Stage

Figure 2.13 shows a test circuit for the design of driving transistors. The origin of parasitic capacitance is from copper pillar pads in EIC and PIC and its value is estimated at 50fF.

There are two criteria used for the design of the driving transistor M1 shown in Figure 2.13.

The first criterion is to limit power dissipation on the driving transistor below 5 %. The second criterion is to have the falling time less than 1 ns, which is a consequence of calculations from subchapter 2.7. Regarding the first criterion, the worst power dissipation on the transistor M1 is when heater resistance is minimum, which is the case of the heater of AWG with the value of 38.2 Ω. The same specifications of the driver are used for the design of drivers for the heaters of the remaining photonics components, such as the heaters in Interleavers and ring resonators.

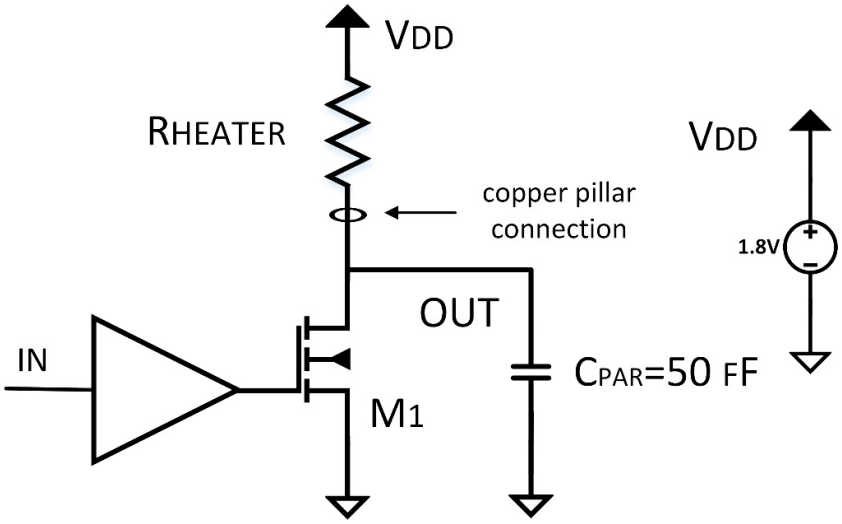

Figure 2.13: Test circuit for design of driving transistor

Voltage drop on the turned on M1 transistor is 60 mV in case of heater value of 38.2 Ω. This gives us power dissipation of $P_{DM1} = \mathrm{V}_{DS} \cdot \mathrm{I}_{DS} = 60\mathrm{mV} \cdot \frac{1.8V - 0.06V}{38.2\ \Omega} = 2.73mW$ while total power consumption is:

$$P_{Total} = \mathrm{V}_{DD} \cdot \mathrm{I}_{DD} = 1.8\mathrm{V} \cdot \frac{1.8V - 0.06V}{38.2\ \Omega} = 81.9mW$$

$$EFF = \frac{P_{DM1}}{P_{Total}} = 3.3\ \% < 5\ \%$$

So, the criterion of power efficiency is satisfied.

In the following the rising and falling times and transient simulations of PWM signals for the different values of heaters are presented and analyzed. Figure 2.14 shows the rising and falling times in a function of heater resistance. The value of heater resistance is varied from 60 to 510 Ω in steps of 50 Ω. The yellow line shows the intersection of ideal heater resistance with the value of 230 Ω (as it is described in Chapter 2.6, for this value of heater and supply voltage

of 1.8V, maximum heating power corresponds to the full tuning range). The green line shows the intersection of experimental heater value of 110 Ω, as it can be seen in Figure 2.14. In both cases, the rising and falling times are lower than 1 ns.

Figure 2.15 shows transient simulations for the PWM output from Figure 2.13, while the value of the heater is varied in the same range as for Figure 2.14.

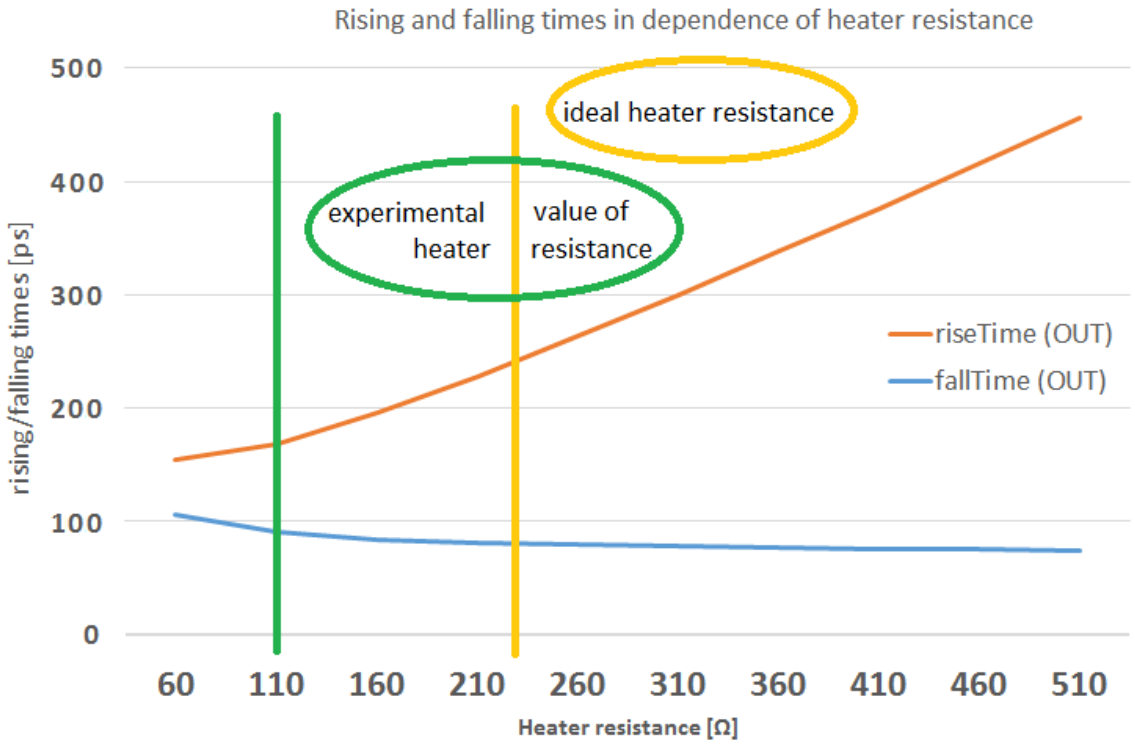

Figure 2.14: Rising and falling times in dependence of heater resistance in the range of heater value from 60 to 510 Ω (W_{M1}=441 µm, L_{M1}=180 nm)

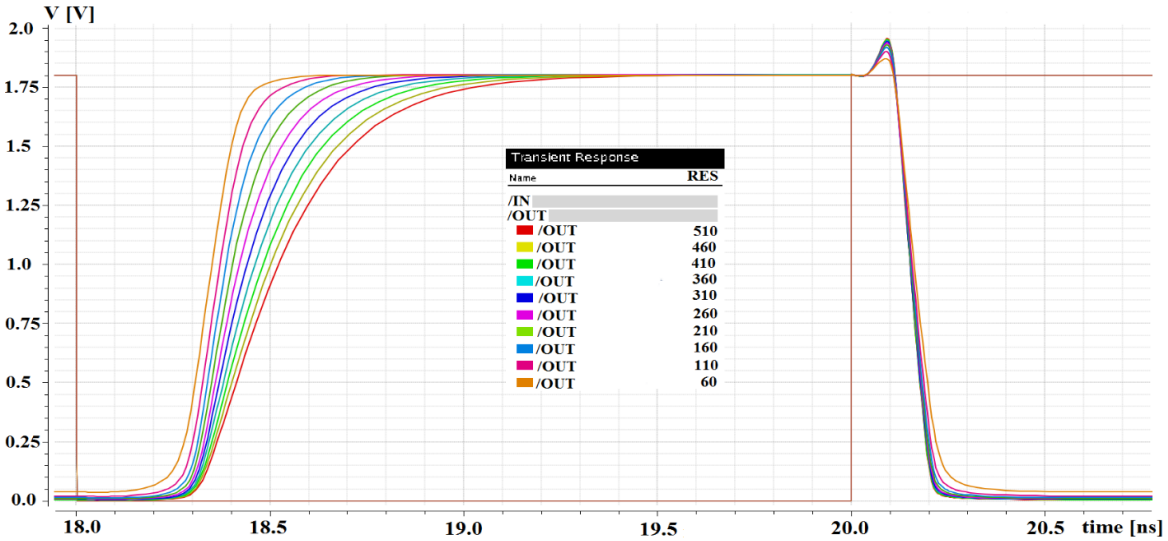

Figure 2.15: Transient simulations of PWM output signal at the drain of M1 transistor for the range of heater value from 60 to 510 Ω (W_{M1}=441 µm, L_{M1}=180 nm)

An investigation of drivers with 5V transistors has also been done. However, for the same specifications, the falling time of less than 1 ns and power dissipation on driver MOSFET of less than 5% lead to the transistor width of 1.1 mm. The minimal length of transistors up to 5V is 600 nm. These dimensions would require much more area in layout than the driver with a MOSFET transistor with maximal drain-source voltage of 1.8V. However, in this design, the area is limited to the cell dimensions of 100 x 100 μm^2. For this reason, further design has been done with transistors, resistors and capacitors with the voltage range of up to 1.8V.

2.10 Monitor Photodiodes

Since the system requires the adjustments of heating power for proper operation, feedback signal from monitoring diodes is necessary in the key points of the switching matrix. The monitors are bidirectional due to the fact that the device operates in drop and add modes, depicted in Figure 2.16.

Monitoring circuits are implemented by the use of an integrated power splitter and Ge monitoring photodiodes. Specified monitoring optical power splitting radio was 10%, while maximum operating optical power range at the monitoring photodiode input was from -15 dBm to -30 dBm.

The logarithmic I-V characteristic of Germanium PIN photodiode is shown in Figure 2.17. The dark current of the photodiode at 1V of reverse bias voltage is lower than 100 nA. Figure 2.18 shows optical responsivity (A/W) at the wavelength of 1550 nm, the lowest value in the range is 0.6 A/W.

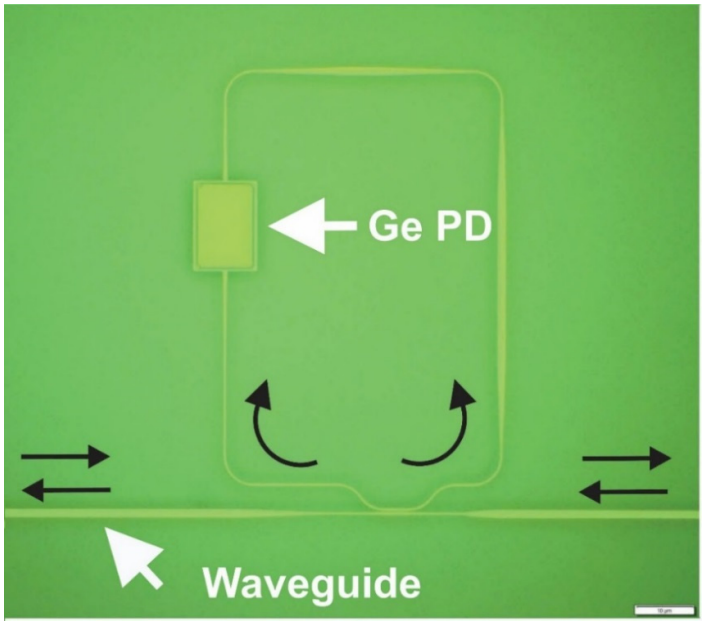

Figure 2.16: Bidirectional monitor *[63]*

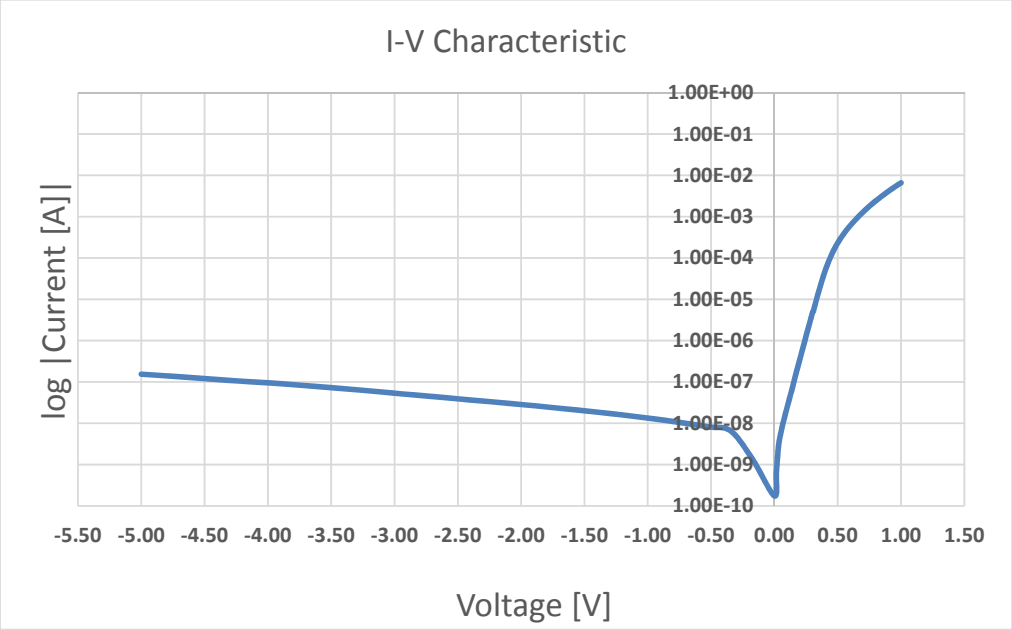

Figure 2.17: Logarithmic characteristic current vs. voltage of the Germanium photodiode *[59]*

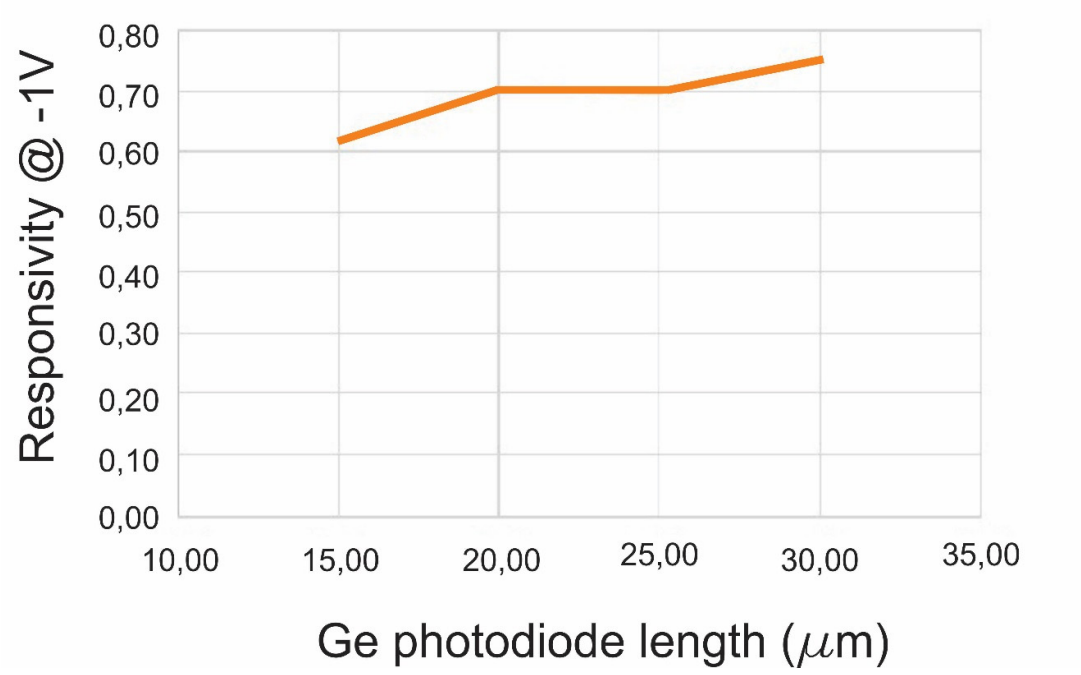

Figure 2.18: Responsivity of Ge PIN diode (A/W) at 1550 nm *[59]*

3 Technologies Used for the Design of PICs, EICs and EPICs

3.1 Used Technology for the Design of PICs

Wafers are fabricated in a fully CMOS compatible 8 inches fab at CEA-LETI. Starting materials are Silicon-On-Insulator (SOI) substrates featuring a 220nm thick silicon film on top of a 2µm thick Buried Oxide (BOX) [33]. The main waveguides of photonic circuits are 480 nm width strip waveguides. A modular approach is used to build the process flow that supports various sets of devices. The simplest process flow allows fabrication of passive devices only, meanwhile the full process includes the fabrication of active devices such as photodiodes and modulators, as well as tuning capability using a thermal heater option (Figure 3.1).

The silicon patterning module is the foundation for most of the photonic platform's supported devices. A multi-level etch is used to define the various silicon thicknesses. 193 nm Deep Ultra Violet (DUV) lithography is used to allow the design of line and space minimum sizes down to 120nm with an alignment tolerance as low as 20nm, which is critical for certain devices e.g. waveguide transitions.

Photodiode fabrication is based on the selective epitaxial growth of pure germanium in cavities at the end of waveguides. The excess material of the facetted overflowing Ge layer is removed by Chemical Mechanical Planarization (CMP) prior to the ion implantation of the n-type and p-type zones forming the lateral pin structure. Metal 1 connection plugs are then defined. They land directly on doped Germanium regions.

The proposed Back End of the Line (BEOL) consists of one Al-Cu interconnection level with W plugs and vias. An additional Under Bump Metallization (UBM) process is also done for 3D integration of electronics on the photonics.

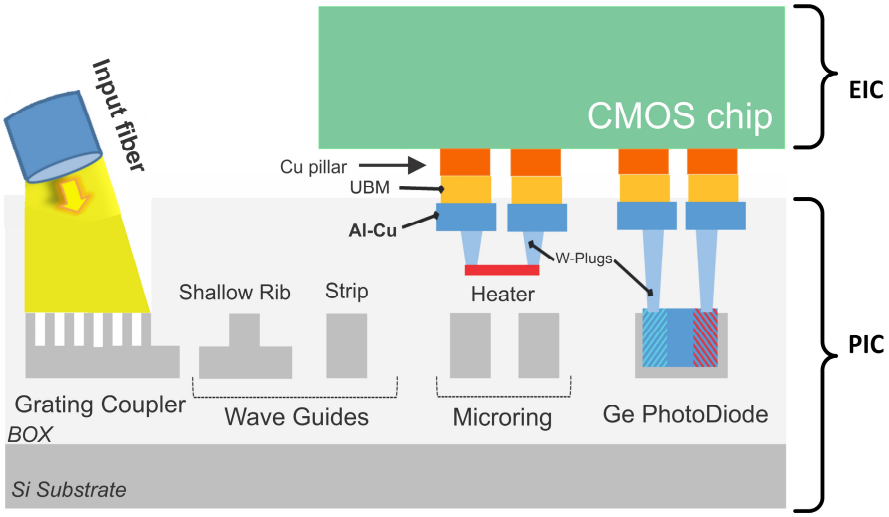

Figure 3.1: Cross section illustration of the Silicon Photonics technology and 3D-integration *[33]*

3.2 BCD8sp Technology

BCD (Bipolar-CMOS-DMOS) is world-class technology developed by ST Microelectronics Company for power ICs. STMicroelectronics made this BCDsP technology platform for smart-power ICs available for prototyping to universities, research labs and design companies. This platform is available through services provided by CMP (Circuits Multi Projects) [64].

These released BCD design capabilities for prototyping shows a growing importance of state-of-the-art power integration for future application in high-performance fields in computing, consumer and industrial electronics.

Figure 3.2 shows a roadmap and available ST's BCDs technologies. ST has a unique offer of BCD process technologies, each referring to specific application, with an optimal trade-off between performance and cost. There are two classes: high-voltage BCD and high-density BCD. High-voltage BCD enables reliable coexistence on the same chip of low-voltage control circuits and very high-voltage DMOS transistors with voltage capability up to 800 V. High-density BCD option is developed by the need to integrate more and more complex and diversified functions on the same chip. As it can be concluded from Figure 3.2, the BCD8sp technology used for EIC designs is mature, but not the latest.

BCD8sP process enables the integration of analog and logic circuits with high voltage power components for the production single-chip devices for complex power-conversion, power actuators and control applications. BCD belongs to a family of silicon processes and in itself combines the strengths of three different process technologies onto a single chip. Bipolar transistors used for precise analog designs, CMOS transistors used for digital design and DMOS (Double Diffused Metal Oxide Semiconductor) for high-voltage and power devices. Many advantages are obtained by the integration of these three technologies: smaller chip area, reduces EMI and improved reliability.

It was decided in the project to use this technology for the design of all EICs, since in the early phase of the project we did not know what voltage rates would be necessary for the heaters in PIC, i.e. which types of transistors would be necessary for driving the heaters in photonic devices. However, CMOS part of BCD8sP technology platform was sufficient for the design of all electronic chips for control and drive photonics. This is also advantageous since cheaper CMOS technology could be used for this purpose in future. Power transistors could be used for the integration of DCDC converters with control electronics. Cadence framework was used as a design kit for this technology.

During the project TU Wien participated in 3 commercial MPW runs. Altogether, 12 different types of EICs were designed and fabricated.

BCD technology platform with 0.16 μm node offers dense logic transistors (1.8V and 5V CMOS) and high performance analog features. The development of this technology is driven by an increasing demand in power needs, larger current delivery, better efficiency and a larger number of regulators in a single die. Also, BCD8sP offers very high performing power class in the 8V to 42V range integrated in an advanced CMOS platform. For large logic cores integration, high performance analog sections and I/Os ports, 1.8 V and 5 V CMOS transistors are available. The process is based on a dedicated P-epitaxial growth on P-/P+ substrates with the introduction of an N-type buried layer. The main technology modules are shared with the

standard CMOS platform as a columnar poly-silicon, Shallow Trench Isolation (STI), cobalt silicide and borderless contacts, as it is shown in Figure 3.3. Characteristics of the main devices are summarized in Table 3-I for the purpose of both logic and analog application. A typical set of capacitors, poly resistors and diodes is also a part of this process. In addition to the typical set of standard devices, high density SRAM (3.9 μm^2 bit size), NVM EEPROM, OTP and 5V Zener diode are also provided. The multiple thin metal layers (3 or 4 Al/Cu) with 0.16 µm lithography pitch enables the integration of an interdigitated MOM capacitor with high voltage and high linearity. Power devices and their characteristics are listed in Table 3-II. A wide range of N- and P- MOS high voltage signal transistors are also developed in this process in order to provide a complete set of devices for application such as drivers and power stages. The availability of PMOS gives benefits in some realizations such as power bridge blocks, where usage of PMOS as high side power stage simplifies the driving circuit reducing the need for the charge pump and external bootstrap capacitor circuit [65], [66].

Table 3-I Characteristics of main devices *[65]*

Bipolar	**$H_{FE,\ max}$**	**BV_{CEO} [V]**	
5V NPN	40	7.5	
5V IVPNP*	80	-12	
18V IVPNP*	35	-34.5	
CMOS	**V_{TH} [mV]**	**$I_{D,SAT}$ [µA/µm]**	**I_{OFF} [pA/µm]**
NMOS 1.8V	600	650	< 20
PMOS 1.8V	550	260	< 15
NMOS 5V	770	510	< 1
PMOS 5V	830	250	< 0.05
RESISTORS	**R [kΩxmm²]**	**Mismatch [%x µm]**	
HIPO	5	3.1	
CAPACITOR	**C/A [nF/mm²]**	**Linearity [ppm/V]**	
12V POLYPOLYCAP	1.2	< 150	
30V MOM	0.645	50	
LLDiode 45V	Sub loss < 1e-5		

*IV: isolated vertical

Table 3-II Characteristics of power devices *[65]*

Power device	**R_{ON} x area @ E=4MV/cm [mΩ x mm²]**	**BV_{DSS} [V]**
NDRIFT 8V ID*	2.8	14.3
NDRIFT 18V ID*	8.5	29
NDRIFT 27V ID*	14.2	36
NDRIFT 42V DR*	28.4	57
PDRIFT 8V	8.7	-12.7
PMOS 48V	103	-61

*ID: Isolated drain, *DR: Double resurf

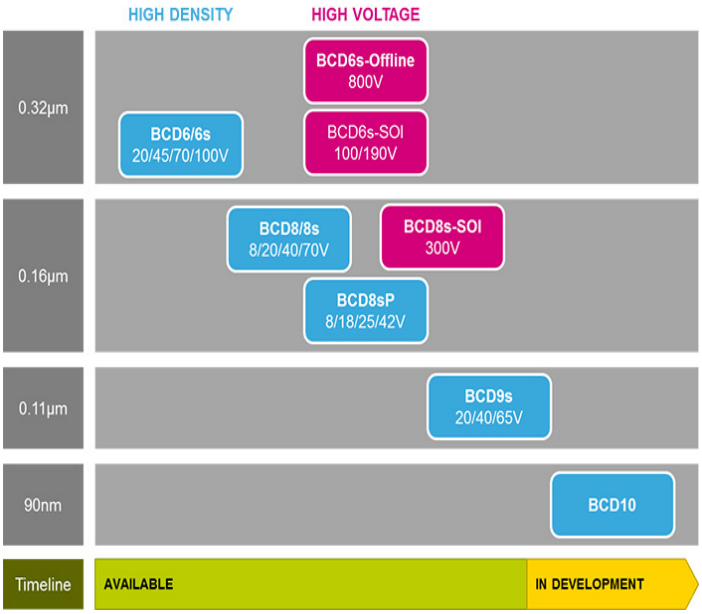

Figure 3.2: Roadmap of ST BCD technologies *[64]*

Several back-end process options are available to reduce product costs depending on the purpose. Different routing thin Al/Cu levels and last thick metal options (Al/Cu or Cu) are offered. Thick last metal AlCu or damascene Cu layer can be used as a power metal interconnect. For the designs of EICs, process option with 4 metal levels is used with the last thick metal Al/Cu.

STMicroelectronics Company is a global semiconductor leader offering customers a wide spectrum of solutions. Power, sense, smarter driving products, and embedded systems solutions are some of them. ST's products are found everywhere microelectronics makes an innovative contribution to make people's life easier and more comfortable: from energy management to data security, across healthcare to smart consumer devices, at work, in the home, as well as in the car and leisure [67].

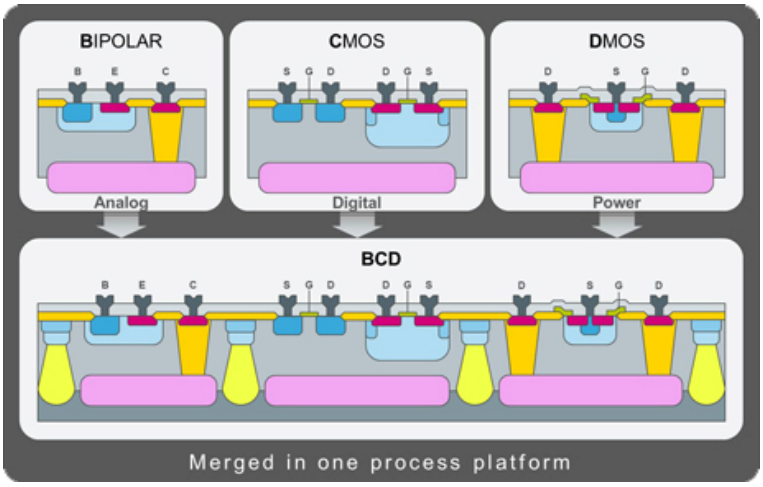

Figure 3.3: Cross-section of devices available in ST BCD technology *[64]*

3.3 3D EIC-PIC Integration Technology

The EIC-to-PIC interconnection is made using micro copper pillars. Electronic wafers are post-processed with growing micro copper pillars, as it is depicted in Figure 3.4 and Figure 3.5. Electroplating semi-additive process of a Ti/Ni/Cu metallic stack through a thick resist mask is used for post-processing EICs. Also, on the top of the micro copper pillar an additional layer of eutectic solder (SnAg) is deposited. The photonic wafers are processed with under bump metallization (UBM) pads composed of an Cu/Ni/Au stack.

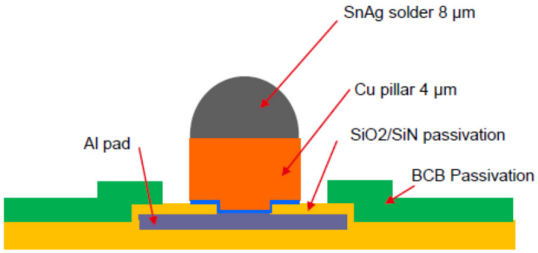

Figure 3.4: Structure of microbump implemented on the EIC wafer *[68]*

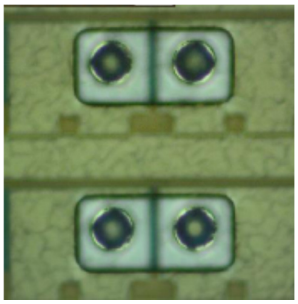

Figure 3.5: Detailed view of microbump *[68]*

The fabricated copper pillars have a Cu growth thickness = 5.07 ±0.1 µm and a SnAg growth thickness = 7.3 ±0.25 µm [68]. The inspection after solder reflow shows a perfect formation of the µbumps and no residue and no degradation of Alu pads on the EICs as shown in Figure 3.5 and Figure 3.7. The process was evaluated as “high quality”: no residue, uniform formation of the µbumps, conform post-reflow shape and no alupad degradation were reported.

This 3-D integration of EIC and PIC chips fulfills the target of integration level with the pitch of 50 µm and less than 1 Ω of contact serial resistance. The estimated capacitance of pads and copper pillar structure is around 50 fF. This integration technology is also scalable to the current minimal pitch of 30 µm which would allow for higher density. However, in case of this work, the limitations come for two reasons; first, thermal crosstalk between microrings and, second, the size of electronic circuits for the control of microring heater power.

3.3.1 Design of Copper Pillar Pads in EIC

A detailed view of copper pillars grown on a full matrix EIC chip is shown in Figure 3.7. There are more than 2000 bumps in total used for 3D integration of EIC and PIC chips.

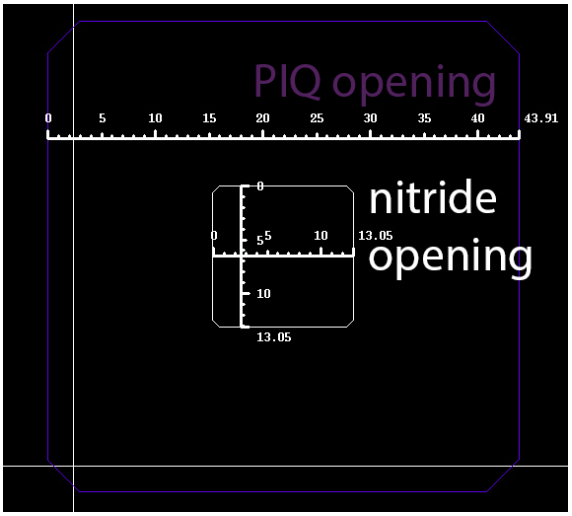

Figure 3.6: Copper pillar PAD on EIC

Figure 3.6 shows the layout of the PAD on which a copper pillar for the connection of EIC and PIC will be grown. The dimensions of PIQ opening are 43.91 x 43.91 μm^2, while the dimensions of nitride opening are 13.05 x 13.05 μm^2. Below the opening there is a metal stack with all 4 metals and all vias. These layout dimensions are shrunk by a factor of 8% in order to obtain the physical dimensions.

The copper pillars are placed inside the control cells and there is also a ring formed of two copper pillars in the row. Some parts of these copper pillars rings are connected to the GND and some to the VCC potential in the PIC chip. The same copper pillar pads was used for each of the electronic chips designs for 3D integration with PIC.

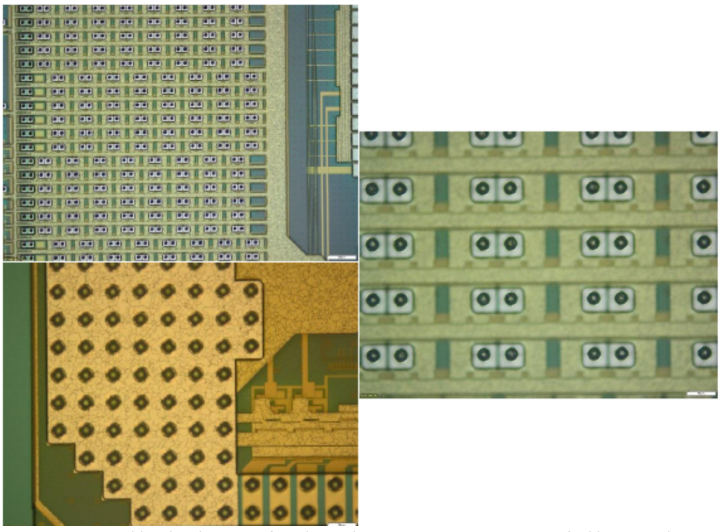

Figure 3.7: Detailed view of microbumps grown on full matrix EIC *[68]*

Copper pillars for connecting the EIC chip with the PIC chip are located in the middle of the chips (see Figure 3.7) as well as in the form of a ring all around the chip.

3.3.2 Chip to Chip Bonding

In Chapter Introduction, the possibilities of 3D hybrid integration of a chip with TSV, TOV and copper pillars were already discussed.

In general, there are three possibilities for 3D hybrid integration depending on the stage of bonding, as described in Figure 3.8 [69]. The third approach, chip-to-chip bonding, is used in IRIS project.

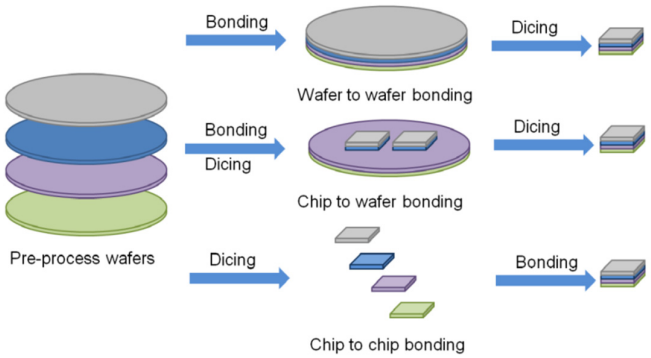

Figure 3.8: Different approaches of 3D integration of chips

4 Packaging and Measurement of EPIC Device

4.1 Packaging (Host and Module Boards)

Two PCBs are designed for testing EPIC device. A modular approach was chosen, the packaged device is mounted onto a host board as it is shown in Figure 4.1. The purpose of the host board is to provide the necessary supply voltages as it is shown in the block diagram in Figure 4.2. Peltier drivers and USB, serial and PDI (programming and debugging interface) interfaces for monitoring, control and programming of the microcontroller inside the module board are also placed on the host board. The locations of these components are marked in Figure 4.1.

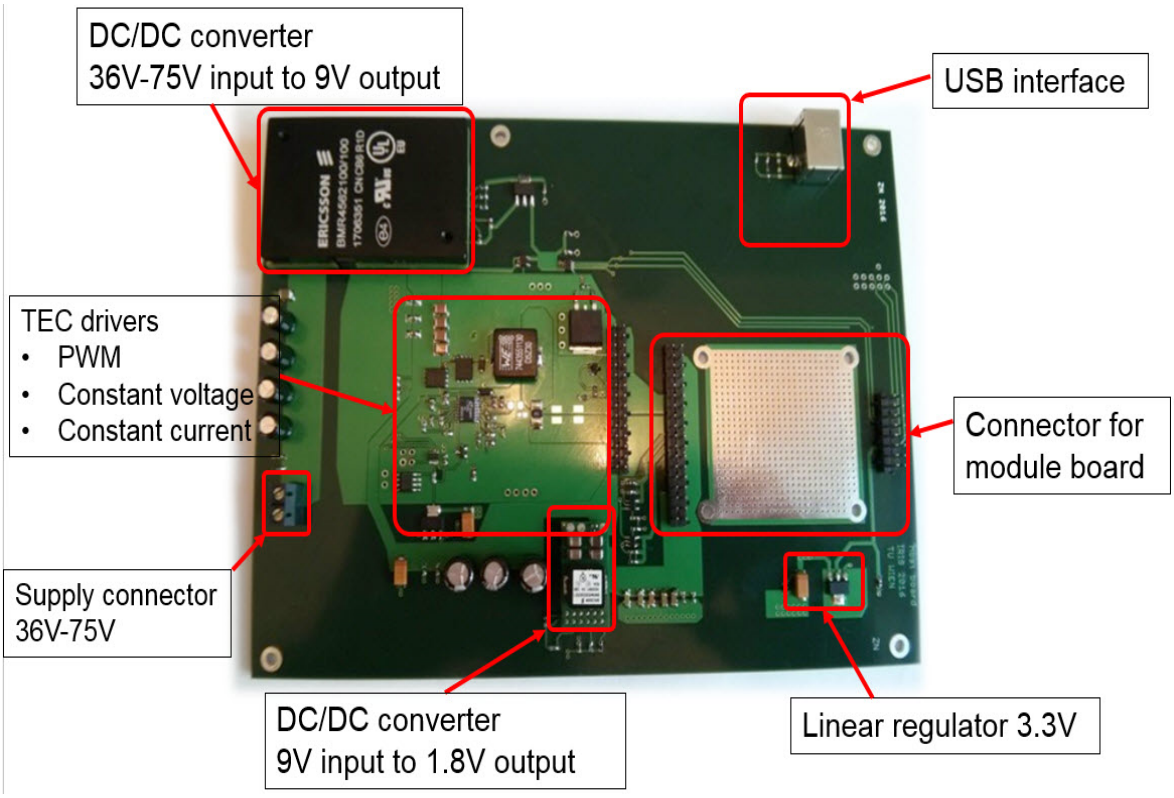

Figure 4.1: Top view of host board PCB

The dimensions of the host board are 145 mm x 196.2 mm. The PCB is a design with 4 layers with the thickness of 1.6 mm. The bottom layer was used as the ground plane, while the middle layers were used for supply planes, 9V and 3.3V.

Surface finishing is HASL and minimum spacing is 6 mils. Metal planes, on top and bottom layers, connected with vias, are placed below the package improving heat conduction

from the bottom side of the case frame further to the optional heatsink, as will be discussed further.

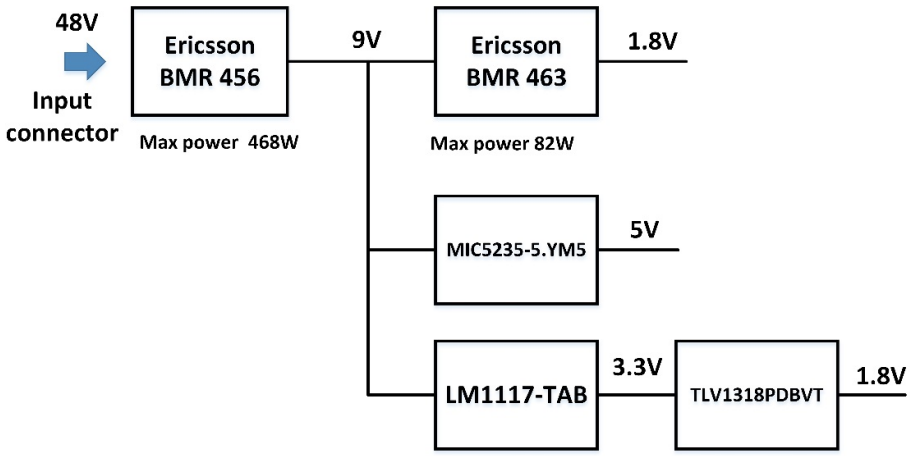

Figure 4.2: Block diagram of supply voltages used on the host board

A block diagram of supply voltages used on the host board is shown in Figure 4.2.

Module board PCB is designed to be placed inside the package. The microcontroller for controlling the EPIC chip and readouting the monitor photodiodes is placed inside the package in order to reduce the length of analog lines, as well as to protect it from the possible EMI from the power supply modules. Additional decoupling capacitors, level shifters, an oscillator for the microcontroller, as well as current sources for monitoring diodes, are also placed on this module board, as it is marked in Figure 4.3. The module board, placed inside the package is later connected to the host board via pin header connectors. This modular approach simplifies the testing of packaged devices, since the same host board is used for the measurement of several modules. In this way, different packaged devices can easily be plugged in and out.

The dimensions of the module board are 72.11 mm x 48.25 mm. The PCB was designed with 4 layers and a total substrate thickness of 1.2 mm. The surface finishing is made of gold to allow the direct bonding of the EPIC with the minimum spacing of 5 mils.

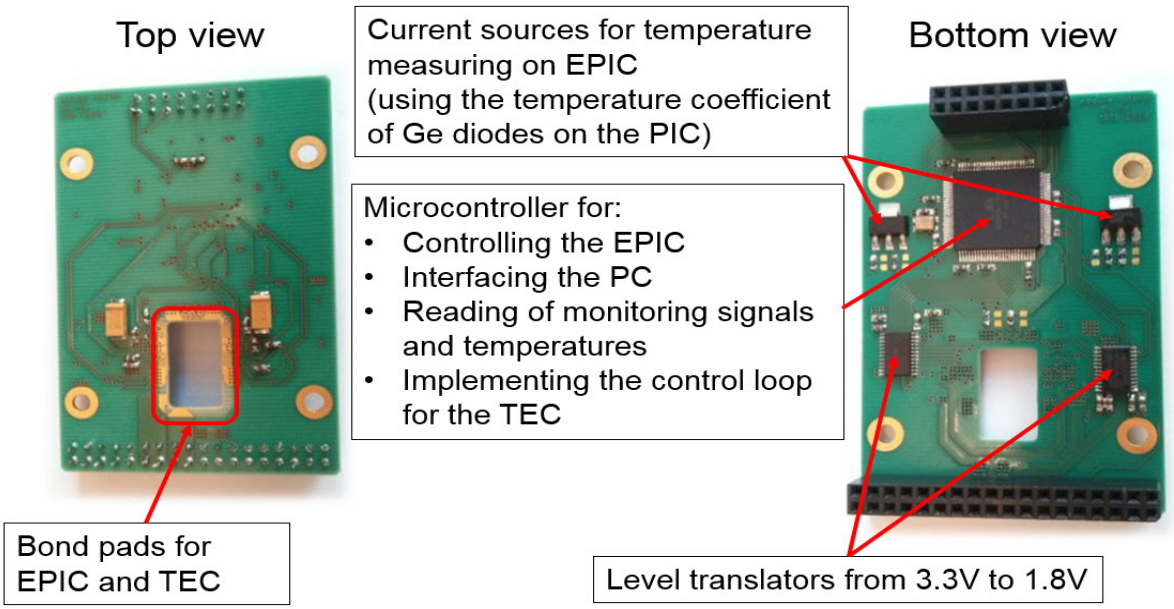

Figure 4.3: Module board PCB with marked components

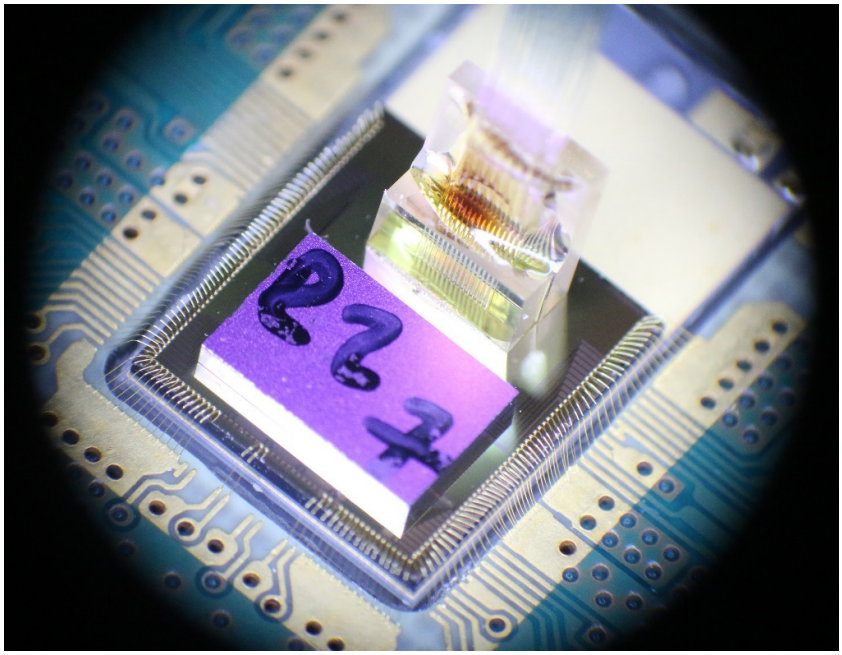

Figure 4.4: Zoomed in wire-bonding of the EPIC device into module board PCB

Wire bonding of EPIC chip pads and the TEC to the module board PCB is shown in Figure 4.4 and Figure 4.5. Ball-wedge technique of bonding is used in this case. Applying heat, pressure and ultrasonic energy, a “ball” connection is made on the pad of the EPIC chip, and the wedge bonding is realized on the other side of the bond wire connection, i.e. PCB. Wire bonder TPT equipment, by the project partner at University of Valencia, is used for bonding purpose with a 20 µm thick bond wire.

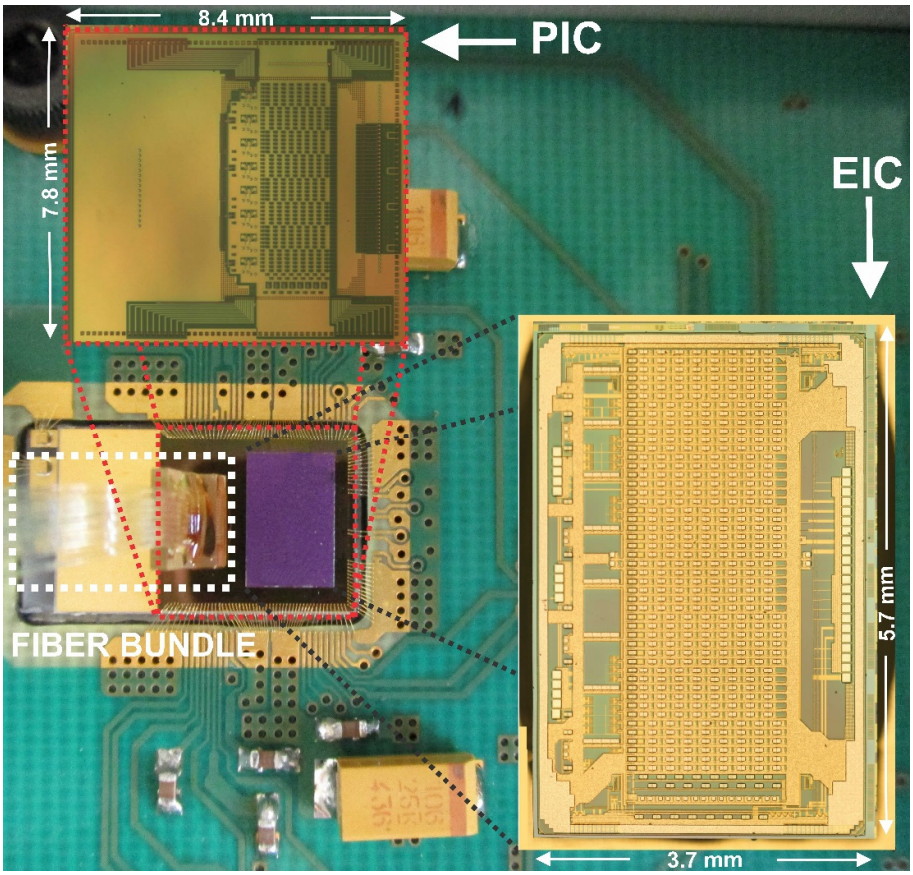

Figure 4.5: Wire-bonded electronic-photonic integrated chip (EPIC) to the PCB inside the Al frame with zoomed photos of PIC and EIC. The EIC chip is flipped upside down *[33]*.

Furthermore, vertical coupling and pigtailing of a fiber array (comprised of 16 channel V-groove assembly) over the chip gratings was realized (Figure 4.5). Finally, demountable cases and a lid were placed so that the entire assembly stays protected, as depicted in Figure 4.6 and Figure 4.7.

The packaging process is divided into several steps. The first step after 3D integration of EPIC device involves the soldering of all components on the module board which is placed inside the package. The construction of the package should guarantee good thermal conductivity and heat flow between the parts, enabling dissipation of the chip heat power.

Assembly parts of the package are shown in Figure 4.8. A thermoelectric cooler is soldered below the chip to dissipate heat power generated by the PIC chip. TEC's top and bottom AlN ceramic surfaces are gold plated which guarantees good thermal dissipation. The chosen TEC, rated to allow dissipation of up to 30W, is soldered inside the package with SnPb solder bumps melted at 200 ℃. Afterwards, the EPIC chip is glued to a thermosetting resin on the TEC. Finetech machine is used for pick-and-place of both the TEC and the EPIC chip.

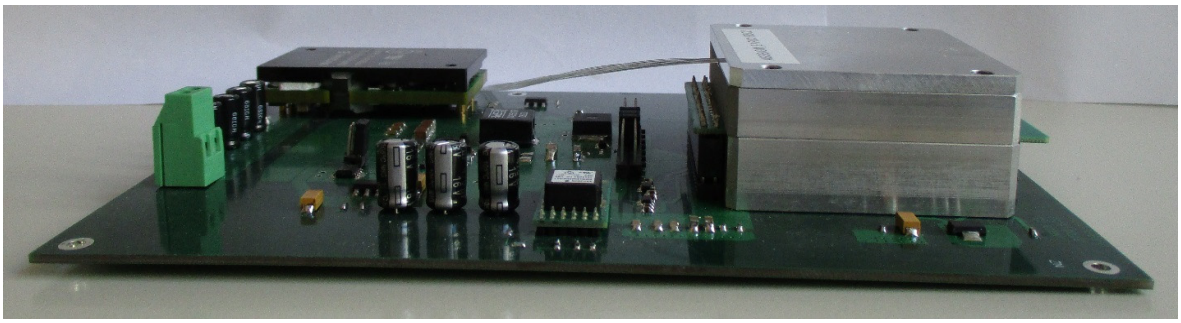

Figure 4.6: Side view of mounted packaged device on the host board

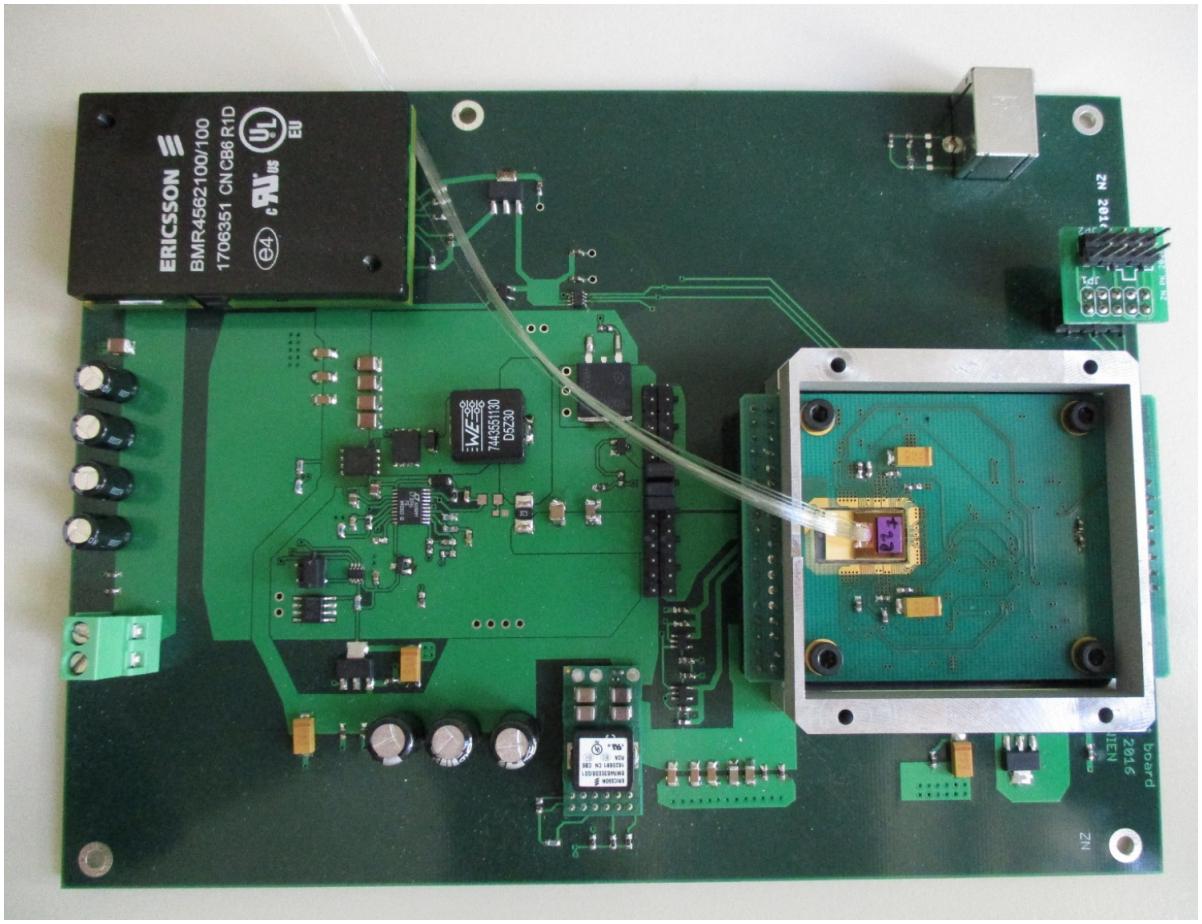

Figure 4.7: Mounted package on the host board

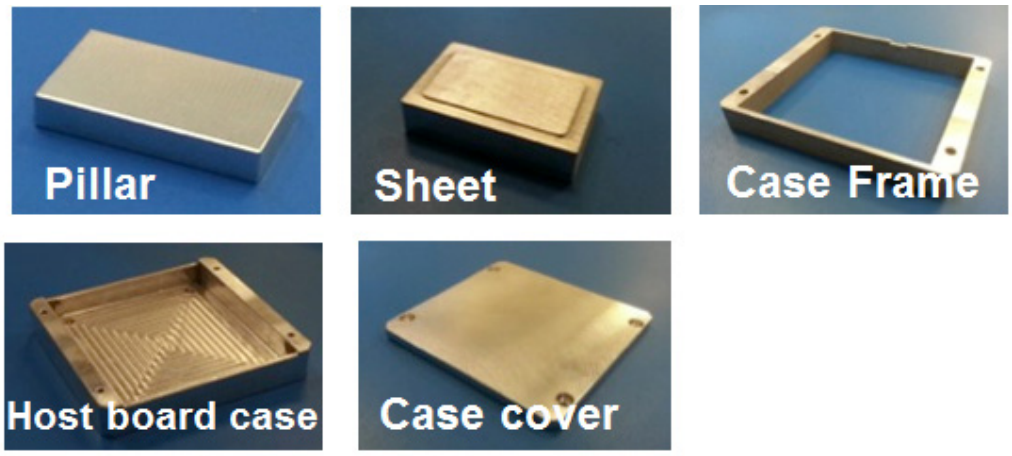

Figure 4.8: Assembly parts of the package *[1]*

Different test were applied for temperature regulation of the packaged device. The first version of the package, shown in Figure 4.6, showed low heat conductivity. The case heatsink itself was not capable of sinking the heat, so it was not possible to stabilize temperature of the packaged device below 43 ℃ with applied typical load, i.e. typical power consumption of the EPIC device of 3.3W. Mean heat power dissipated by the module depends strongly on process variation for the fabricated PIC, since total heat power is mainly determined by heater power necessary to compensate for process variations. The expected typical mean total heater power should be considerably less than the tested 3.3W.

By applying thermally conductive paste between the metal layers of the package, minimum temperature of the PIC can be decreased to ~37 ℃. If even lower temperatures are necessary, this can easily be achieved by attaching an additional heatsink on top of the lid of the package. With this option, it was possible to decrease the lowest regulated temperature to ~32 ℃.

However, by attaching a heatsink with fan to the lid of the case we get much more freedom for the temperature regulation. In such a case, the package temperature of 20 ℃ and below is easily achievable.

Finally, Figure 4.9 shows the improved version of the package. The main improvement is based on the integration of heat sink to the lid and to the bottom side of the package. All the parts are combined by screws so it gives us flexibility on mounting package on the host board. In the host board, below the module board case, there is a large metal area with a huge number of vias in the host board PCB. It allows us to attach a heat sink at the bottom side of the host board. In order to reduce thermal resistance, it is necessary to apply the thermally conductive paste between all the metal surfaces: top heat sink and case lid, case top frame and bottom case, as well as on the both sides of the host board, between the bottom case and the bottom heat sink. With this additional heatsinks, heat dissipation of the package is improved.

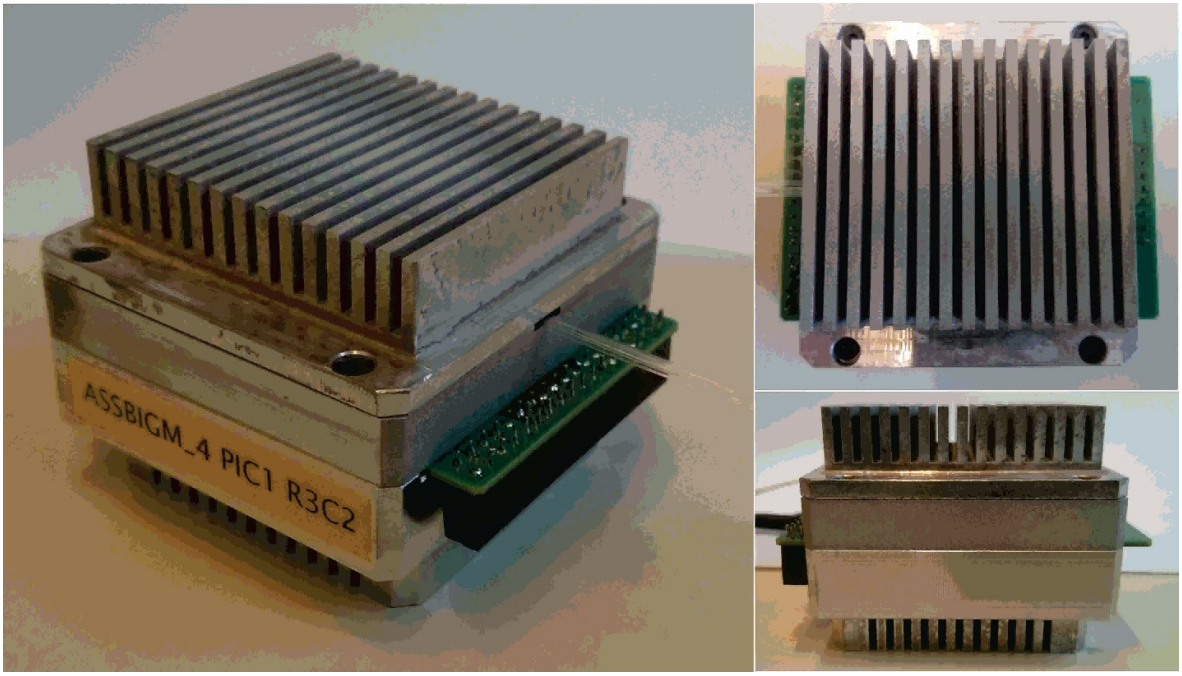

Figure 4.9: Improved package design – integrated heatsink on the lid and bottom side of frame

4.2 Measuring and Control of the Temperature of EPIC

For a Ge diode, temperature coefficient (NTC) is around -2.5 mV/°C. The effect is almost perfectly linear, so it is suitable for making the diode a temperature sensor by supplying it with a constant current.

The I-V characteristic of Ge temperature diode is shown in Figure 4.10.

In fact, the same Ge PIN diode, described in Chapter 2, is used for monitoring states of the micro-ring resonators. Several of these diodes are placed on the peripherals of the PIC chips. Connection to each of the diodes, cathode and anode, is provided via standard pads.

The constant current of 1 mA is supplied to the Ge diode and the voltage is read out with the ADC from the microcontroller. Each device has to be calibrated individually since the characteristics of the diodes are different due to process tolerances.

Figure 4.11 shows the linear function of voltage on the diode as a function of the temperature. The cause of difference between the voltages on the diode shown in Figure 4.10 and Figure 4.11 is in serial resistance of Ge diode and the resistance of the routed signal on the PCB which was not present during characterization of the Ge diode. Simple calculation give us the value of 141 Ω. (0.7975V-0.656V/ 1 mA).

Calibration of the temperature of the EPIC device is made by a FLUKE thermometer device.

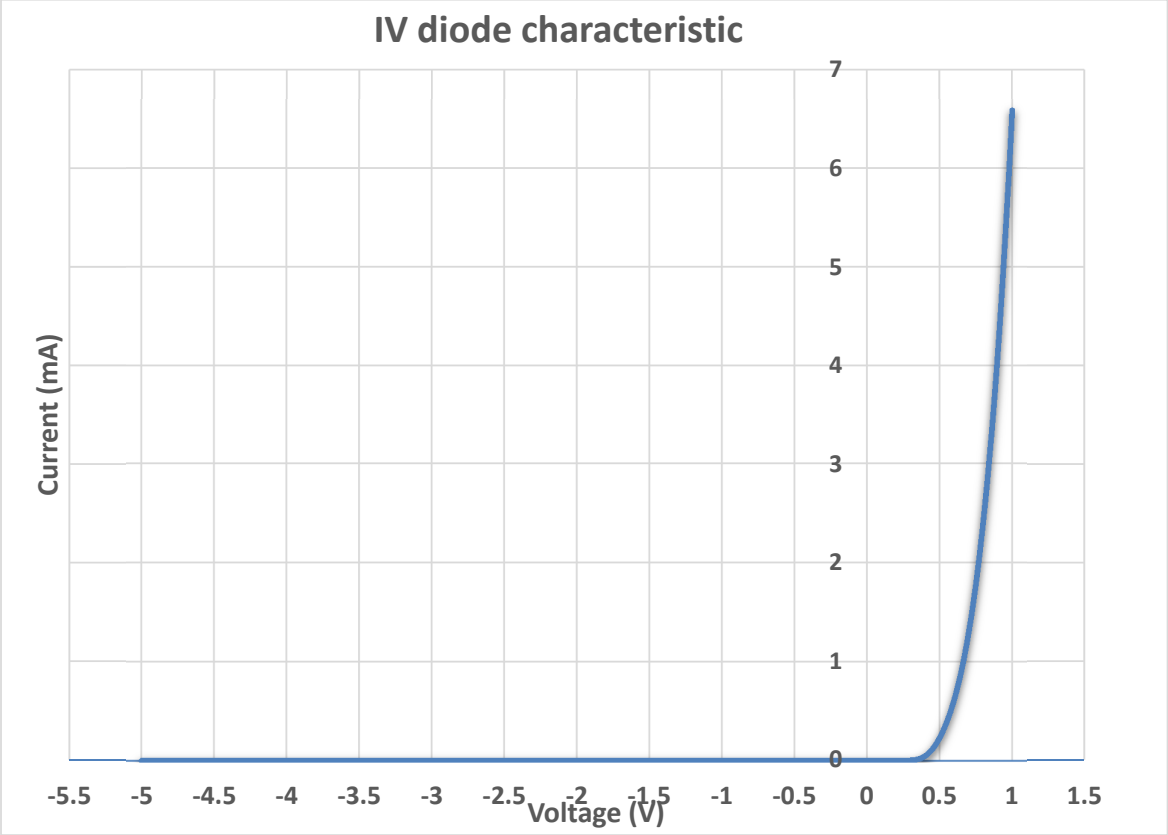

Figure 4.10: Current vs. voltage characteristic of Ge temperature diodes

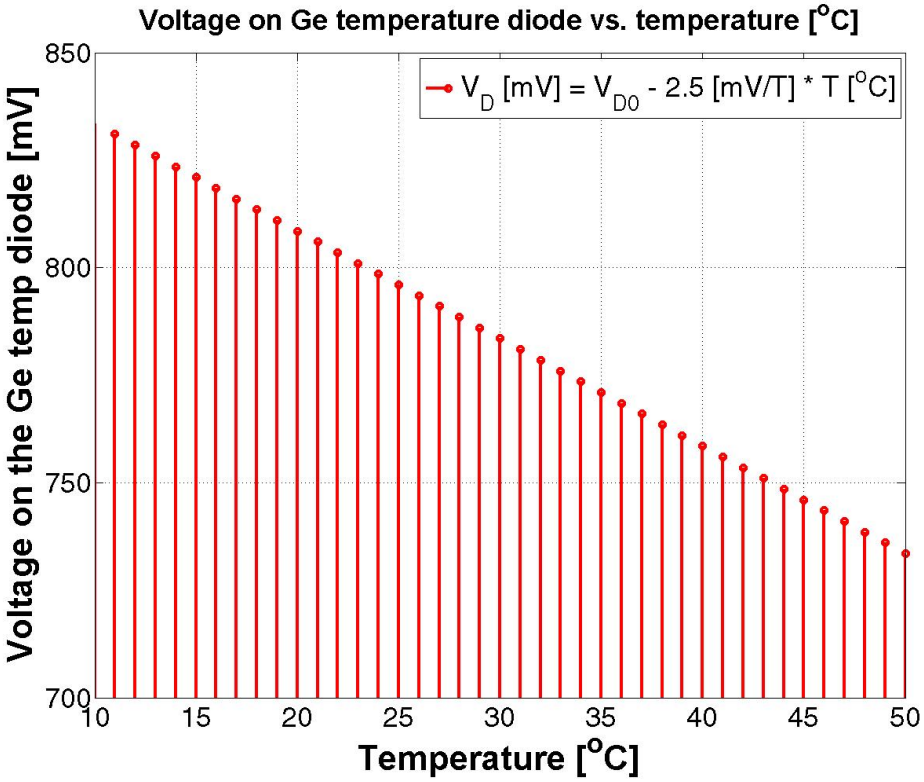

Figure 4.11: Voltage on the Ge temperature diode as a function of the temperature

4.3 Peltier Drivers

The cold side of the thermoelectric cooler is soldered to the bottom side of the PIC. The hot side of the Peltier is attached to a metal sheet positioned inside the board applying a high-thermal conductivity epoxy resin. Then, the metal sheet and the copper pillar are glued together, while the other side of the copper pillar is glued to the bottom side of the aluminum package designed to improve thermal dissipation of the assembly. The dimension of the Peltier are 15 cm x 8.4 cm. It is bonded with wire-bonding to the module board PCB connections.

The used Peltier drive (TEC) is 1MD06-080-03 and is made by RTM company. The characteristics are shown in Table 4-I and Figure 4.12.

Table 4-I Performance Data of 1MD06-080-03 thermoelectric cooler.

@ 27°C, Vacuum	ΔT_{MAX} [K]	Q_{MAX} [W]	I_{MAX} [A]	U_{MAX} [V]
1MD06-080-03	68	30.32	5.2	10.0

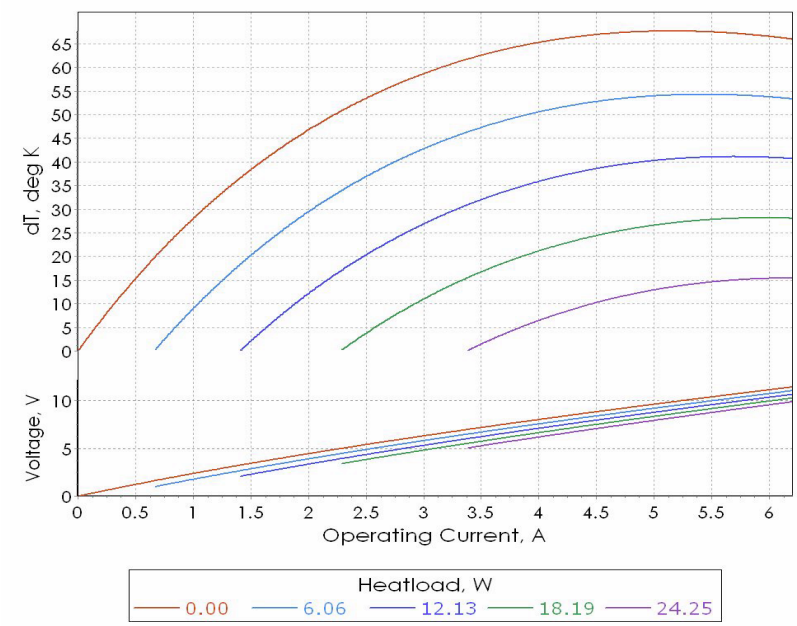

Figure 4.12: Performance data of TEC for different heat loads *[70]*

There are, in principle, two approaches to driving a Peltier cooler. The first one is by supplying it with a constant current, and the second one by driving it with a PWM signal. The second approach is not recommended, since it reduces TE module efficiency. In any case, the signal frequency should be larger than approximately tenfold value of the reciprocal time constant of the TEC. For the TEC 1MD06-080-03 (no object on the cold side) the time constant equals 0.35 sec. So, minimal PWM frequency is approximately 30 Hz.

Three approaches to the regulation of TEC were implemented on the PCB host board: constant current, PWM and constant voltage approach, marked in Figure 4.13.

The most efficient approach is the approach with a constant current described in Figure 4.14 and Figure 4.15. The idea was to rework the standard buck converter by cutting the feedback loop from the output voltage and closing it with fixed voltage, i.e. bandgap voltage reference. In this way, only the current regulation is working and the value of the current is set by the DAC output connected to the pin CTRL1 of the LT3741 chip. The circuit is designed with a maximum output current of 20 A, which is much more than we need for driving the Peltier. Typical efficiency of this approach is around 94%. In the program of microcontroller, the maximum current is set to the value of 2.5 A.

The used DAC is TI 7513 DAC with an SPI serial interface and 12bit resolution. Access to the DAC is provided by the ATMEL microcontroller places on the module board. The SPI peripheral from port F was used for this purpose. In the program of the microcontroller, the digital value of the current is set to be in the range from 0 to 256. The relation between the output current of the circuit and the CRTL1 voltage is given by the following equation:

$$I_O = \frac{V_{CTRL1}}{30 \cdot R_S} \tag{4.1}$$

The resistance of the sense resistor is 2 mΩ. The proportion between reference voltage of the DAC and the digital value is given by following equation:

$$\frac{V_{CTRL1}}{2.5\,V} = \frac{\mathrm{x}}{4095} \tag{4.2}$$

Finally, combining equations (4.1) and (4.2) we get the relation between the output current and the digital value: $I_O = 0.01 \cdot \mathrm{x}$.

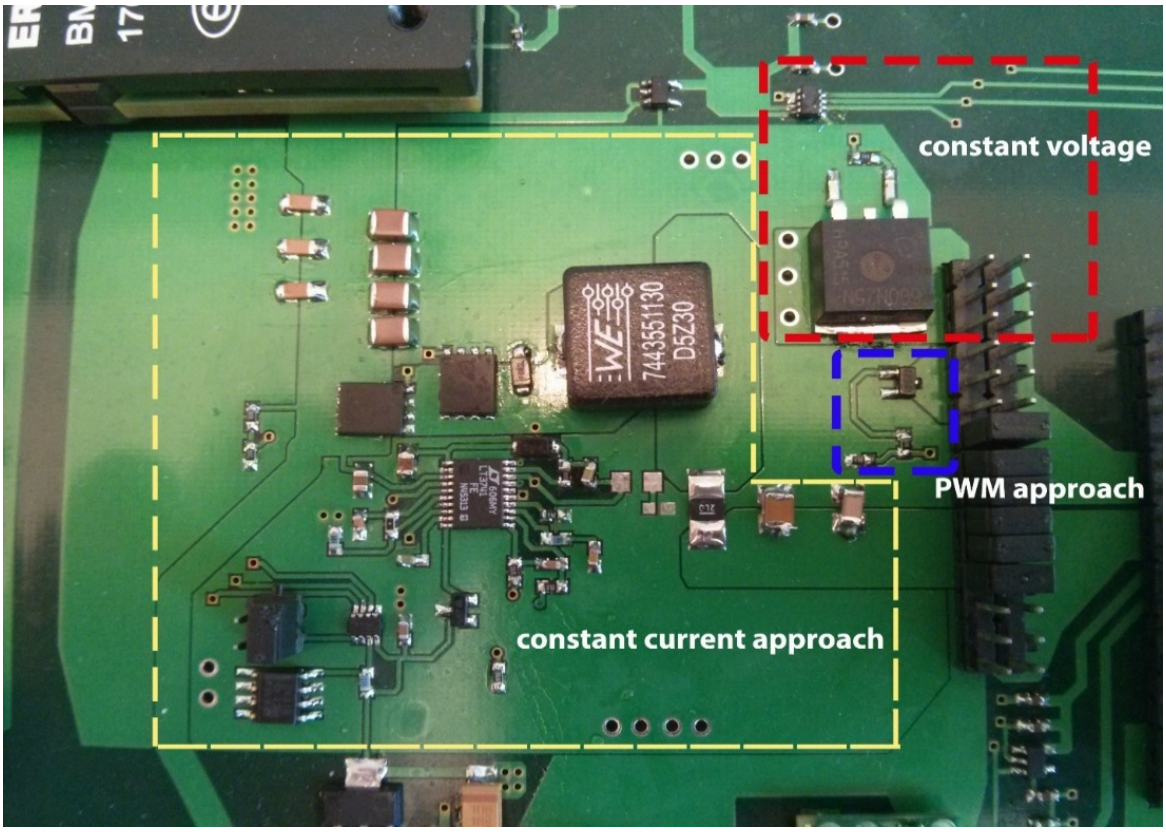

Figure 4.13: Marked blocks of components on host board PCB for different approaches of driving Peltier

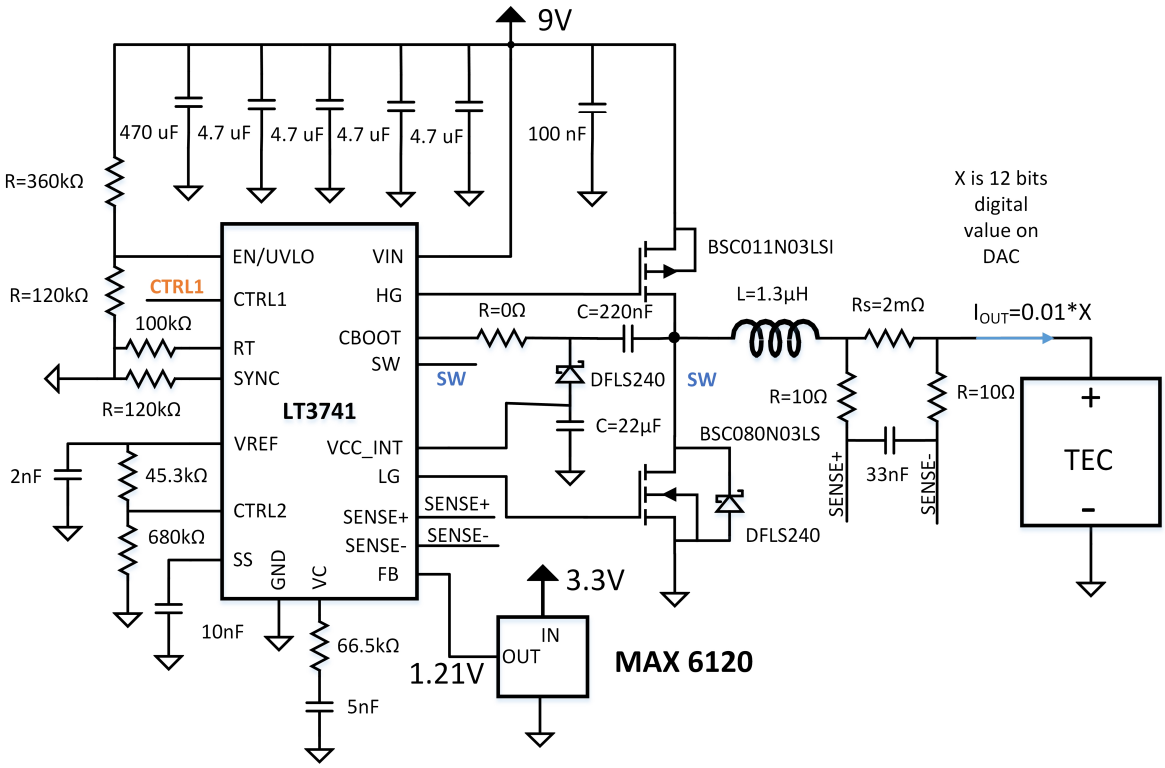

Figure 4.14: Schematic diagram of constant current approach of driving TEC

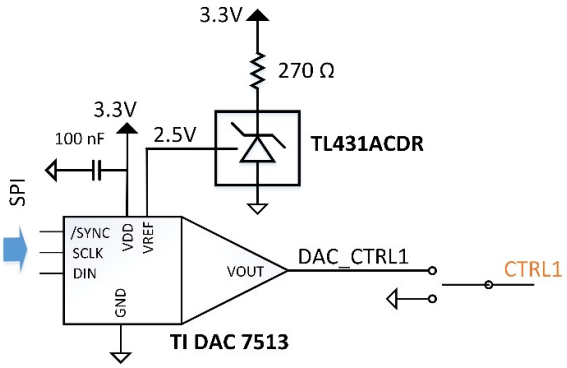

Figure 4.15: Schematic diagram of DAC used for const. current approach of driving TEC

The feedback loop for temperature control is closed by reading out voltages of the temperature diodes. The average value of 100 samples of temperature diode voltage is used as a feedback signal, since it give us more accurate data, due to sampling noise. The control loop for the regulation of the overall temperature of the PIC is directly closed within the microcontrollers firmware by means of a proportional-integral (PI) controller.

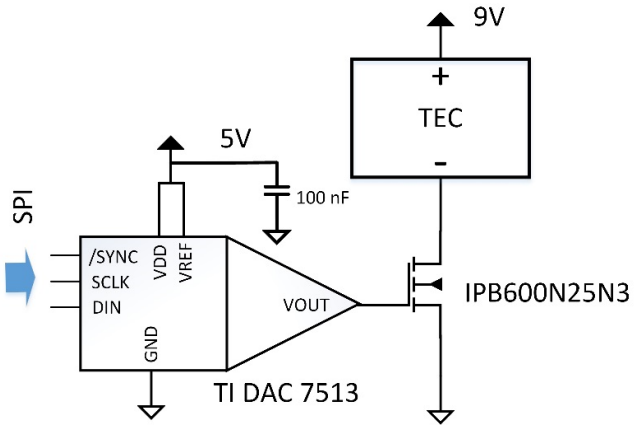

Figure 4.16: Schematic diagram of circuit used for driving Peltier (TEC) with constant voltage approach

A schematic plan of the constant voltage approach for driving the Peltier is shown in Figure 4.16. The idea is to provide constant voltage across the TEC with the regulation of a power transistor IPB600N25N3 driver. This approach is power inefficient, due to the dissipation of the driver MOSFET. Efficiency could be improved by using lower supply voltage. Unfortunately, the value of 9V is fixed by Ericson supply modules which were primary chosen to match the requirement for the design of the circuits for the constant current driving approach. Also, in this case, the DAC is accessed via the SPI interface from port F, while the configuration of the driving approach is selected by the proper position of jumpers on the host board.

The third, PWM, approach for driving the TEC is shown in Figure 4.17. Control is done by setting the duty cycle of the PWM signal, generated by the digital port of microcontroller: capture and compare channels. With the supply voltage of 9V, the values of duty cycle are very low, so the range is not efficiently used. Smaller supply voltage would allow for better

utilization of this approach, but the primary criterion for the selection of supply voltage comes from requirement for the design of circuits for the constant current driving approach.

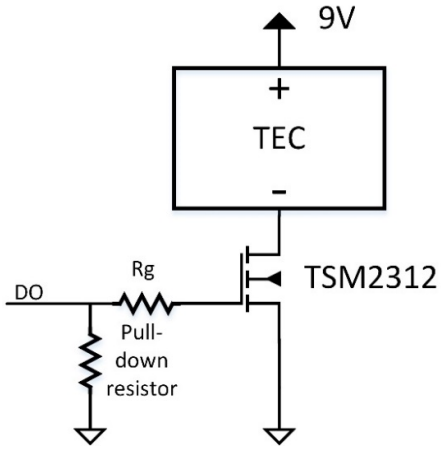

Figure 4.17: Schematic diagram of PWM approach for driving TEC

4.4 Program of the Microcontroller

Figure 4.18 shows that the EIC is connected to a microcontroller to close the control loop for controlling and optimizing the performance of optical switches in the PIC below the EIC.

The control loop circuits for monitoring the EIC-PIC switches in the full matrix and keeping its temperature constant are implemented in the microcontroller ATxmega128A1U with integrated ADCs and DACs. The block diagram of the program for this microcontroller for controlling and monitoring of the EIC-PIC is shown in Figure 4.19. Two different types of control loops were implemented: one for controlling the overall PIC temperature and the other one for a set of heater powers closed with the feedback loop from the monitoring diodes. Due to the leakage currents of the S&H circuits, the refresh rate of minimum 1.5 ms is required. A look-up table (LUT) with proper values for the calibration of heaters (determined by project partner University of Trento) to compensate for process tolerances in the photonics IC is also implemented in the program.

Microring resonators, Interleavers and AWGs require calibration, which is performed by the stochastic optimization algorithm to align the pass-band of the photonic components to the selected wavelength. If there is no heater power applied into the switching elements, the optical signal is expected to be at its maximum at the through port. When the micro-ring heater is driven, feedback control, on the basis of the monitor diode-feedback, finds the best set of heating power values for minimum optical power at the through port of the switching element. That means that the optical signal is directed to the drop port, and the switch is enabled. The algorithm is implemented in software LabVIEW and converges over multiple instances [71]. Thanks to this technique, after the automatic initialization of the switch matrix system, the device is operative (ready for operation) with microsecond fast reconfiguration of the routing function.

The first part of the program is related to the initialization of the peripherals used for this purpose – DMA, Timer counters, DAC, ADC, SPI, digital ports and USB. Since the full

matrix was divided into 4 blocks, we used DACA and DACB, both with 2 channels (in total 4 channels) to provide analog value to the S & H circuit into each cell. Timers have been used to address each cell, and also to trigger conversion of each DAC channel. In order not to overload the main program, the DMA has been used to transfer data to the DAC.

Four channels of the DAC feeding DACs are working in parallel as it is shown in the block diagram of the program for the microcontroller. The data for each of 824 cells are initialized from the look-up table and later adjusted by the feedback loop which is closed by the monitoring TIAs.

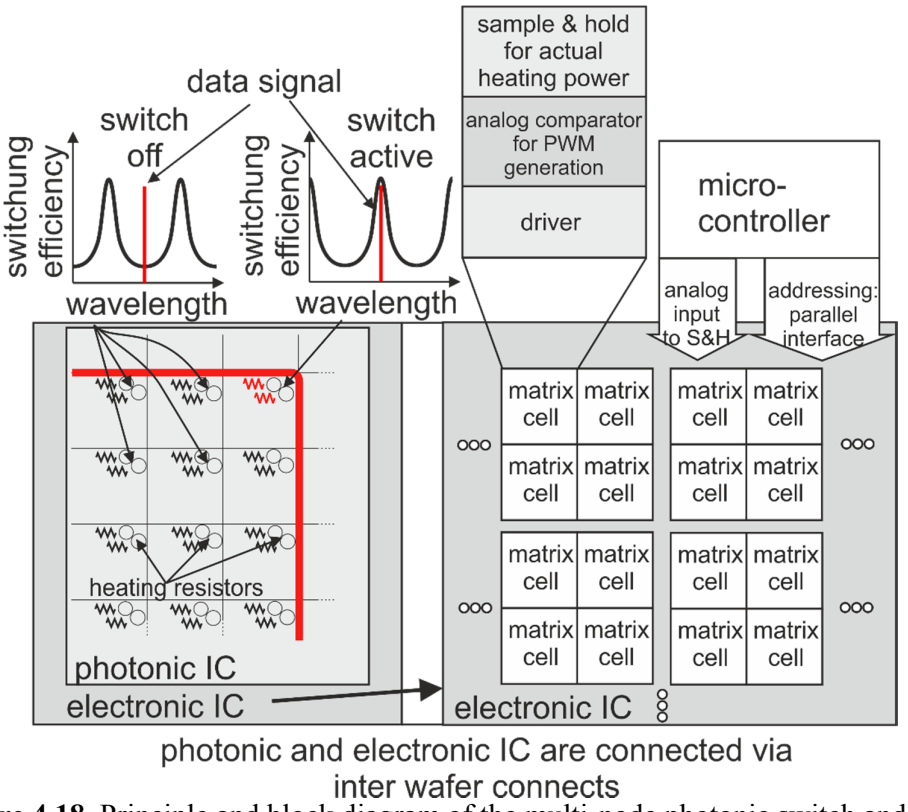

Figure 4.18. Principle and block diagram of the multi-node photonic switch and EIC containing the hybrid heater control circuit in each matrix cell

Both ADCs have been used, and each has 4 channels. In total, 8 channels are used for sampling the values of 6 monitoring TIAs and the voltages from two temperature diodes, simultaneously. The select signals for selecting one TIA out of a group, by means of an analog multiplexer, are provided from digital output port of the microcontroller. Two analog voltages from Ge temperature diodes are read in by two ADC channels to monitor the temperature of the EPIC. The values of these two monitoring photodiodes are later processed to control the TEC. For constant voltage and the constant current driving approach, the SPI peripheral from port F was used to store the value into the external DAC. Timer/counter module of the microcontroller is used to generate the PWM signal for driving the TEC with the PWM approach. In the main loop, operations of storing data into each cell (refreshing the values because of the leakage currents) and monitoring the TIAs and temperature diodes are constantly repeated.

The SCPI based protocol is implemented via serial interface for communication between the microcontroller and the computer. This simple protocol is used for setting heaters and reading out monitoring diodes and temperatures.

An example of heater command is: HEAT Address_Nr Heating_Value\n (e.g. H 23 187, M? 28, T? 0)

The advantages of this SCPI protocol are that it is simple, easy to use and compatible with most measurement control software (C, Java, Matlab, and Labview).

USB and PDI (programming and debugging interface) interfaces are provided from the host board for monitoring, controlling and programming the microcontroller inside the module board.

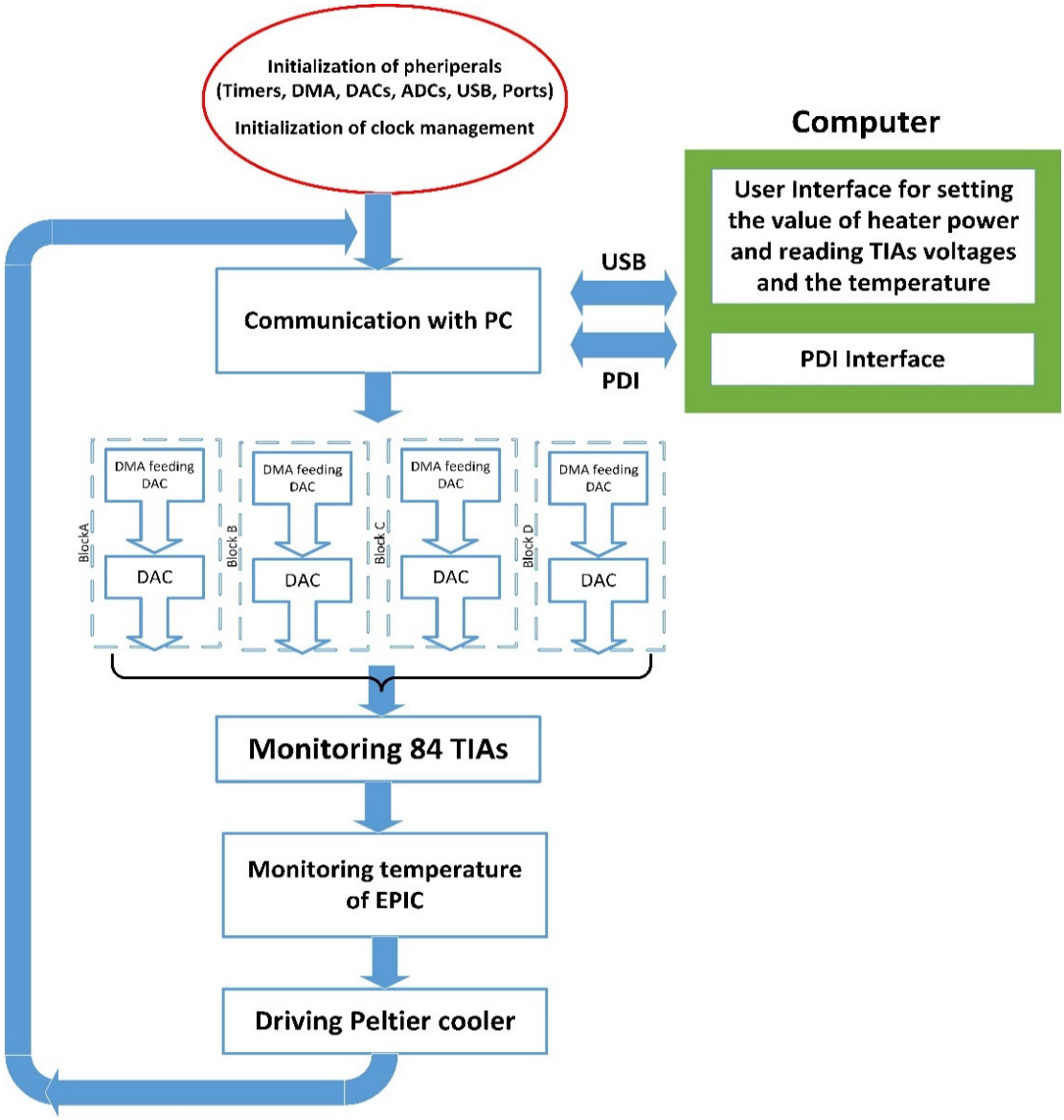

Figure 4.19: Block diagram of program in microcontroller

The command set for communication with the microcontroller that is used for characterizing the full matrix EPIC, allowing to control all heater cells and read out the monitoring TIAs, as well to set and regulate the temperature of the EPIC, is shown in Table 4-II. It allows controlling all heater cells, reading out the monitoring TIAs, and setting the temperature of the EPIC.

Table 4-II Command set

Command	Explanation	Example
*IDN?\n	Reads the Chip ID (Example: PIC1_R3C1)	
*HEAT address_nr heater_val\n	Sets the heater power.	heater_val: 0…145 (0: Minimum heater power, 145: Maximum heater power) After power up all heaters are initialized to 0.
*TEMP? diode_nr\n	Reads the temperature in m°C of the Ge diodes.	The temperature is sent in m°C (e.g. 35,23°C → reading would be 35230). The absolute accuracy should be in the range of a few °C.
*MON? address_nr\n	Reads the monitoring power in a.u. of element at address_nr.	For no light, the returned value is in the range between 3600 and 3700. For increasing amount of light this value decreases.
*TEC temp_val\n	Sets the TEC control loop to the given temperature in temp_val.	The value in temp_val must be in m°C (for 35°C → temp_val needs to be 35000). After power up, the set temperature is 45°C. Attention: for lower temperatures, an additional passive or even an active cooler is necessary!
*TEC?\n	Reads the actual set value of the TEC current.	Positive values are proportional to the TEC current in the range from 0 … 246 (~0… ~2.5A). For higher values, the TEC current is limited to 2.5A.

4.5 Measurement Results of Testing EPIC Device

Figure 4.20, containing measured results obtained by University of Trento, shows the matrix switch working when one channel is added to a direction for two different scenarios (switch A active or switch B active). Transmission spectra at different stages within the device are reported in Figure 4.20. The test was performed by injecting a signal (6dBm) from a tunable laser into the input fiber while the transmission at the output was monitored with an InGaAs detector. The signal paths within the chip are shown in the left part of Figure 4.20. The right part of Figure 4.20 shows the spectra (measured in dB) in different parts of the device. Fiber to fiber insertion loss is presented in the top panel, i.e. the measured transmitted signal at the output fiber, with respect to the input signal, i.e. at the input fiber. Due to the selection of an odd or even channel by one of the switches A or B of the switch matrix we note two high transmission lines. Total insertion loss of about -22dB, a channel bandwidth of 60GHz at -1dB and of 100GHz at -3dB, a side channel rejection of -60dB, which means a crosstalk lower than -35dB, are measured. The other panels show the in-the-chip spectra measured by the monitor Ge photodiodes, normalized by the signal from the first photodiode after the input grating. Note that the Ge diodes are fed by a long microring with a large coupling factor, which explains the undulation observed in the grating transmission.

The interleaver transmission proving the splitting of the input signal into even and odd wavelengths (almost 0dB device losses on the channels and more than -25dB out of the channels) is shown on the bottom panel. The other three panels show the spectra on the way through the device: before and after the AWG and after the interleaver. The second panel shows the signal measured at the output interleaver and the third panel shows the signal after the AWGs (device losses -5 dB). The forth panel reports the wavelengths dropped by the temperature tuned optical switch nodes. The free spectral range of 19 nm and the device losses of -10 dB which account for the whole channel path losses (rings, crosses and waveguides) is noted here. Therefore, the overall loss of -15dB is measured on the chip device (-5dB from the AWGs and -10dB in total from the rings, the waveguide crossings and waveguides), which summing up the input/output gratings losses of -7 dB accounts for the total insertion losses of -22dB [33]. The temperature of the device was kept at 38.8 ℃. AWGs and Interleavers were aligned by driving the corresponding heaters.

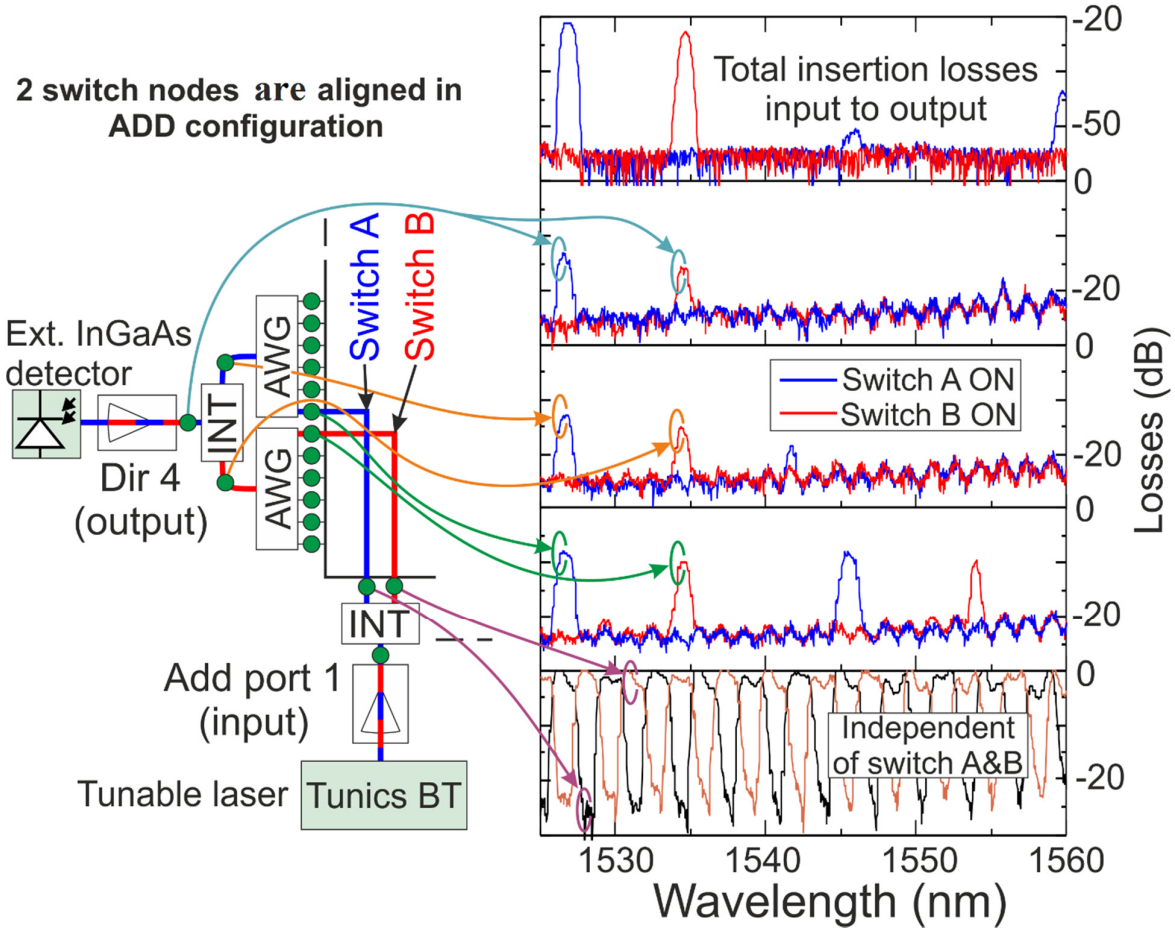

Figure 4.20: Measured performance of the EPIC chip in ADD working mode *[33]*

5 Different Approaches to the Control of Photonics

5.1 Analog Approach to Control PIC

A block diagram of the EIC control chip with the analog approach is shown in Figure 5.1. The main blocks on the EIC are: analog multiplexers, TIAs, address decoders, S & H circuits and drivers. With this EIC 800 heaters need to be driven.

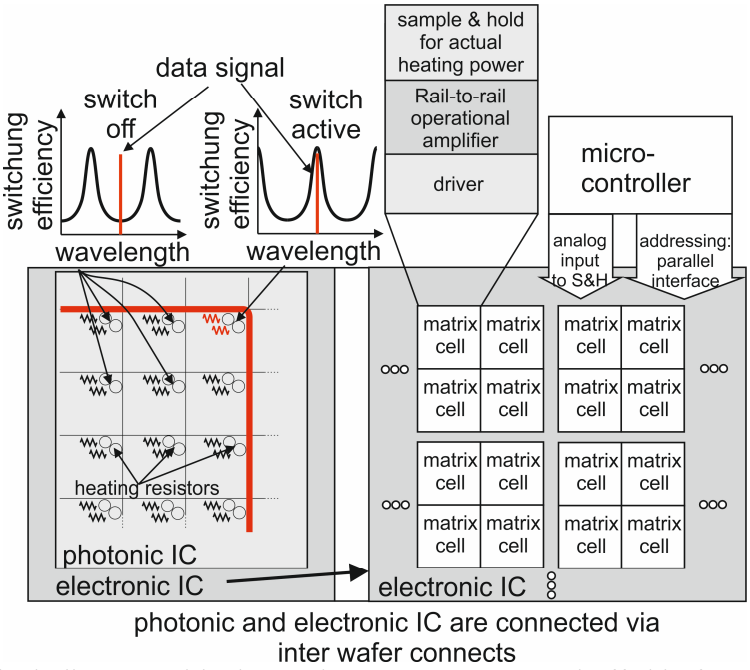

Figure 5.1: Block diagram with electronic components on and off chip for analog approach to control heaters

The principle circuit diagram of one heater control cell is shown in Figure 5.2. It consists of a sample and hold (S & H) circuit, a rail-to rail operation amplifier, a driving MOSFET transistor and a voltage divider. Voltage on the gate of the M_1 driving transistor is regulated by the feedback loop. The loop consists of an operational amplifier and a voltage divider. In this configuration, the drain-source voltage of the transistor M_1 is set to 111.11 % of the value stored in the S & H circuit. With setting the value V_{IN} in the S&H circuit, the value across the heater is inherently set, which means that we are able to control heating power P_{HEATER}. The S&H circuit consists of two transmission gate switches (W_{S1}=500 nm, L_{S1}=300 nm) and one NMOS switch (W_{S2}=500 nm, L_{S2}=180 nm) and sampling capacitor (C=550 fF). The purpose of a voltage divider is to ensure fully turn off of the heater power in case when operational amplifier input offset voltage.

A circuit diagram of the used operation amplifier is shown in Figure 5.3. The input range is rail to rail built up by two complementary differential pairs, NMOS M_8 and M_{11} and PMOS M_9 and M_{10}. They are coupled via current mirrors M_6 and M_7, i.e. M_4 and M_5. Load current mirror forms a couple made of $M_{1\text{-}2}$ while the output stage is formed by the transistor

M_3 and Miller's capacitance. If the input common-mode voltage is close to the GND, operation of the amplifier is done by a differential pair M_9-M_{10} while the pair M_8-M_{11} is almost inactive. For input voltages in the middle range of voltage supply both stages are active. In this way, proper function of the amplifier is maintained for common-mode voltages in a full supply range [72]. Power consumption of this operational amplifier at the switching frequency of 60 MHz is 77 µW.

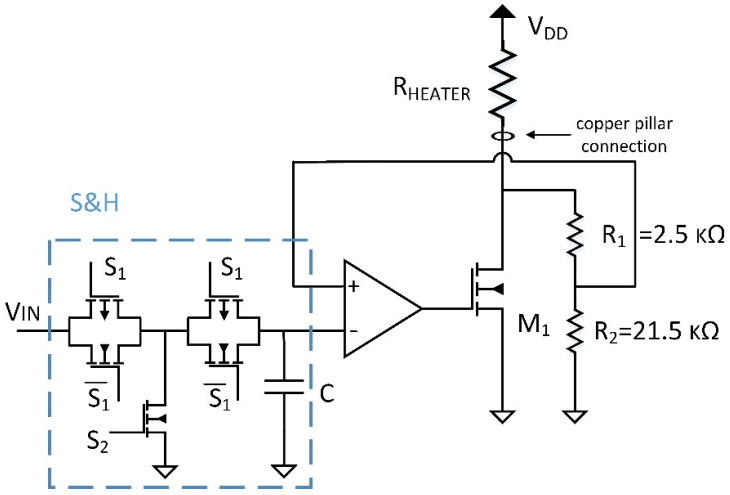

Figure 5.2: Circuit of cell used in analog approach *[44]*

Proof of the analog approach concept of driving heaters in the PIC is tested with the minimatrix chip shown in Figure 5.6. The chip was designed and fabricated in a 160 nm BCD8sP process. Only CMOS part of this technology was used.

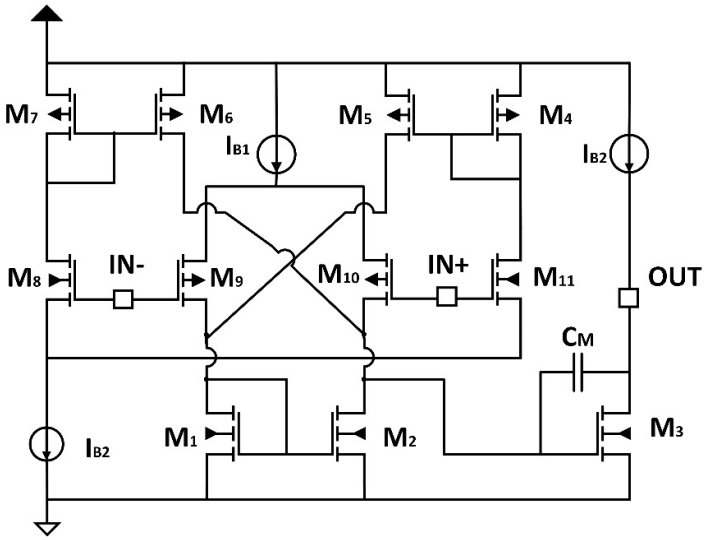

Figure 5.3: Rail-to rail operational amplifier *[51]*

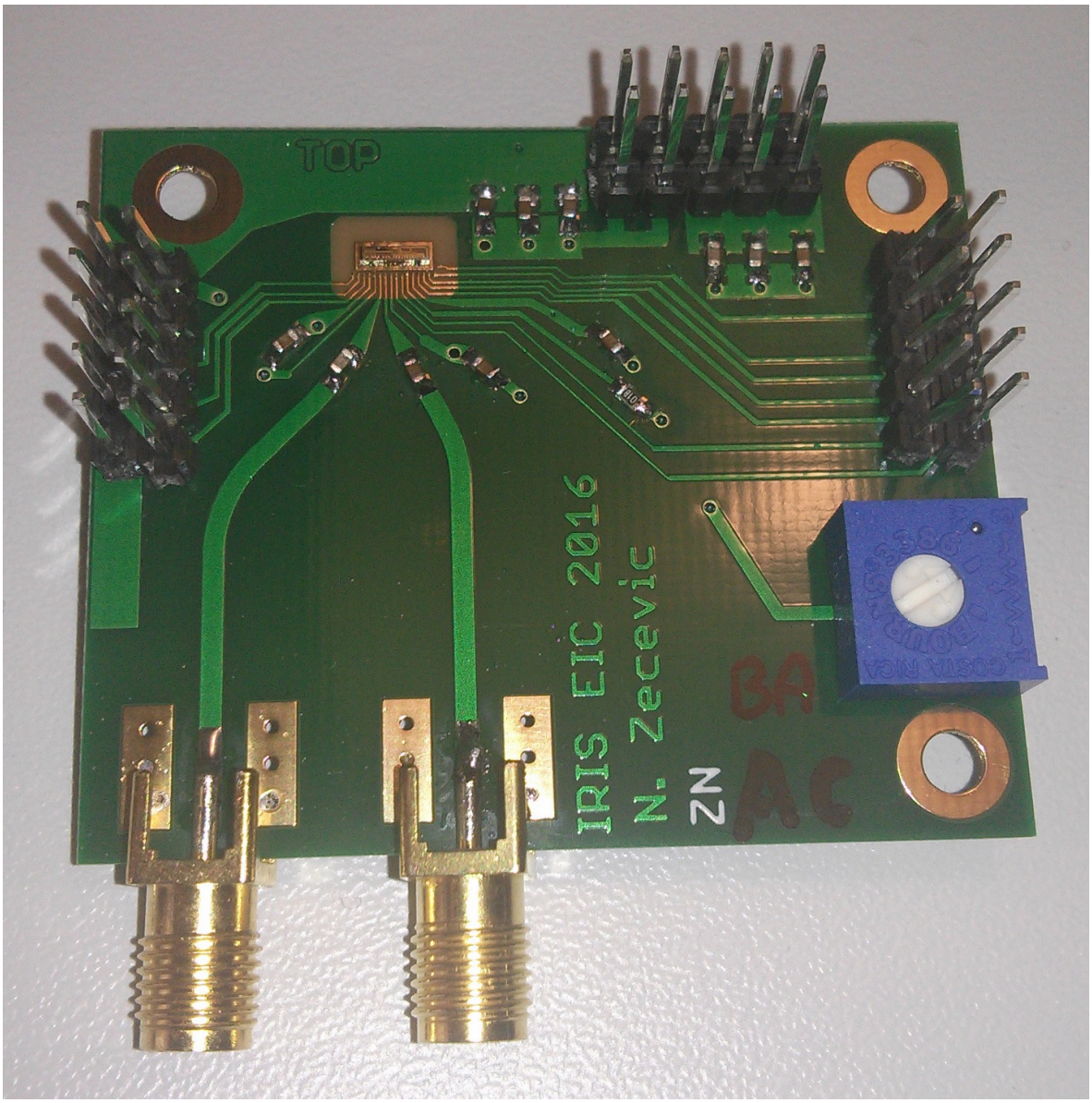

Figure 5.4: PCB with bonded chip with analog approach, electronic components and connectors

Figure 5.4 shows a photo of the PCB used for testing a bonded chip with analog heater control circuits and additional necessary electronics. A micrograph of the minimatrix test EIC with the analog approach is shown in Figure 5.6, while the wire bonded core circuit of the EIC chip for characterization of the analog heater control approach is shown in Figure 5.5. Total dimensions of the mini-matrix EIC chip are 0.8 mm times 3.7 mm. Measurement results of test circuits with 16 nodes and an integrated heater resistance of 230 Ω are shown in Figure 5.7, Figure 5.8 and Figure 5.9.

Figure 5.7a shows a very linear relationship between V_{IN} and voltage on the heater V_{HEATER}. There is a quadratic relationship between V_{IN}, voltage on the S & H circuit, and heater power P_{HEATER} shown in Figure 5.7b. The necessary resolution of the digital-to-analog converter (DAC) is defined by the steepest section of this graph. An 8 bit DAC is necessary to

guarantee wavelength resolution better than 10 GHz, i.e. resolution of heating power of 100 μW (according to Table 2-II). This can be easily calculated from the table described in Chapter 2.

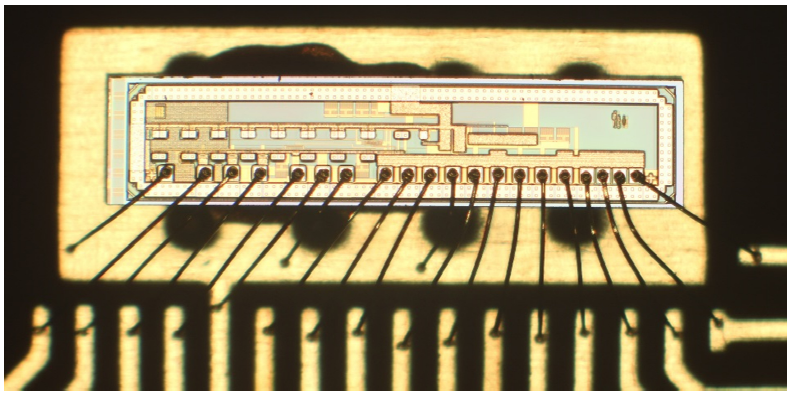

Figure 5.5: Bonded minimatrix EIC chip with analog approach on PCB for measurement

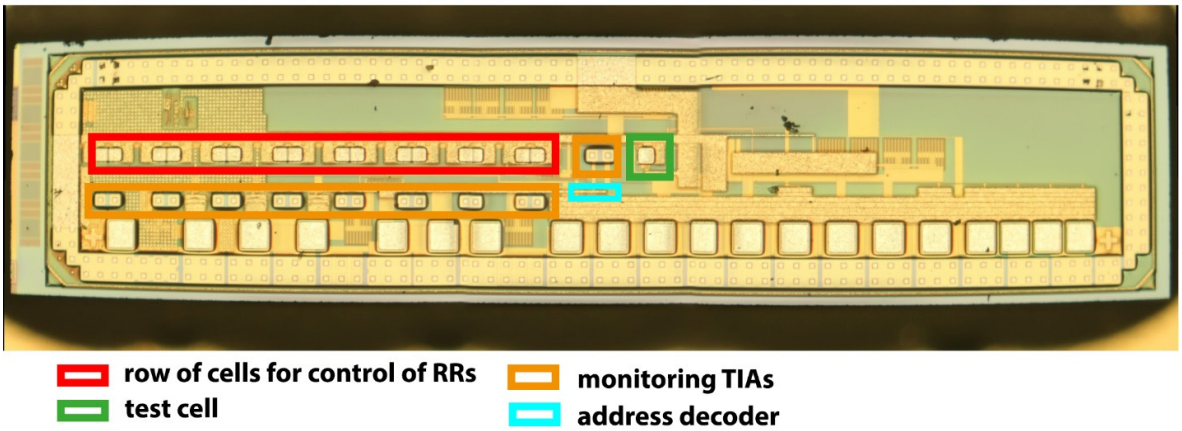

Figure 5.6: Micrograph of minimatrix test EIC chip with analog approach

Output voltage decreases with time due to leakage currents in the S & H circuit (see Figure 5.8). Due to this discharging of the sample and hold capacitance the heating power will increase with time. In case the microcontroller refresh loop does not work properly, this effect can lead to a situation where all heaters are on with a maximum current and the chip can be overheated and burned. For this reason, the inverted function between input voltage and heating power is necessary to protect the chip and to exclude this danger.

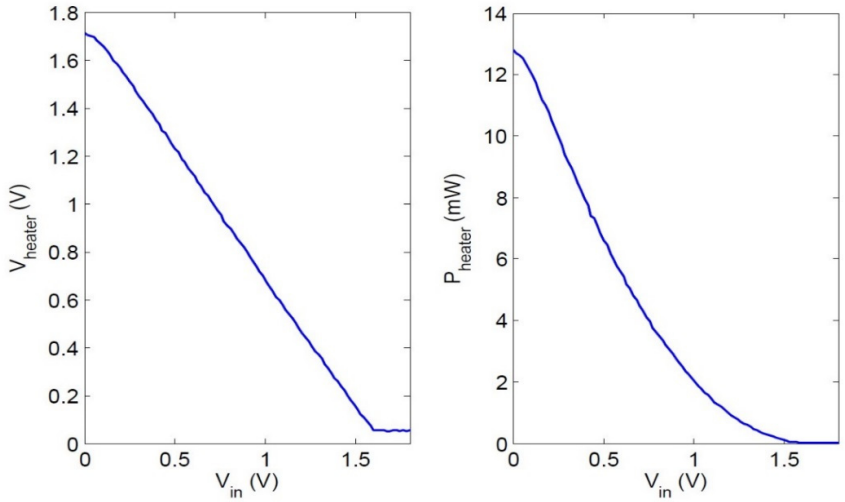

Figure 5.7: Heater voltage (a) and heater power dependence of input voltage stored in S&H circuit (b)

This leakage of voltage stored inside the S & H circuit also changes the actual heating power, which leads to a detuning of microrings. The S & H capacitances have to be refreshed frequently in order to keep this effect below critical limits.

Figure 5.8 shows a relatively linear drop of voltage on the S & H circuits over time. The measured drop rate on the chips is in the range of 20 to 35 mV/ms. This drop rate results in a minimum refresh period of 250 µs. This is still feasible for the control of all heaters with selected ATMEL microcontroller. With this rate and an increased sampling capacitance by a factor of 10, the thermal ripple can be improved by an order of magnitude in comparison to the digital PWM heater control approach. The thermal ripple is present in both approaches, analog and digital PWM, but the causes are very different. The thermal ripple caused by the refresh rate in the analog approach is much smaller than the thermal ripple cause by the PWM driving approach.

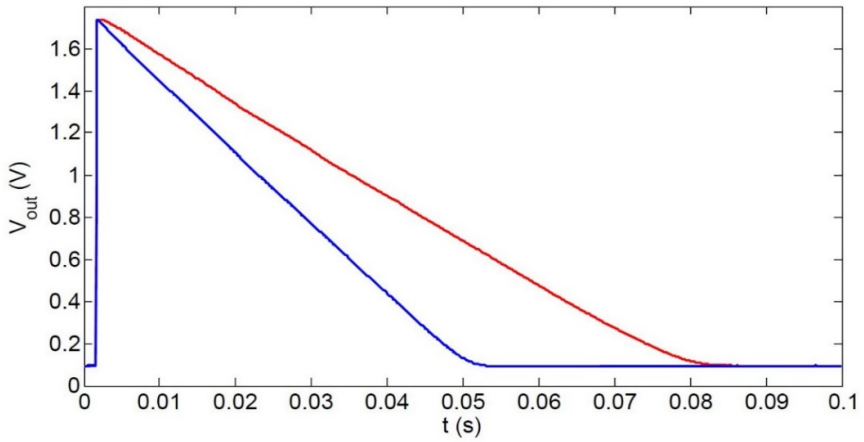

Figure 5.8: Output voltage drop of the analog heater control circuit over time cause by leakage for two different samples

Sampling noise is another issue of the analog approach (see Figure 5.9). If we take in consideration standard deviations of ±4 σ, the maximum uncertainty of voltage on the sampling capacitor will be in the range of ±10 to 12 mV. This corresponds to ±80-100 μW in heating power, which can lead to a partial detuning of the ring resonators.

An increase of sampling capacitance improves sampling noise, which will be further discussed in the analog-digital approach.

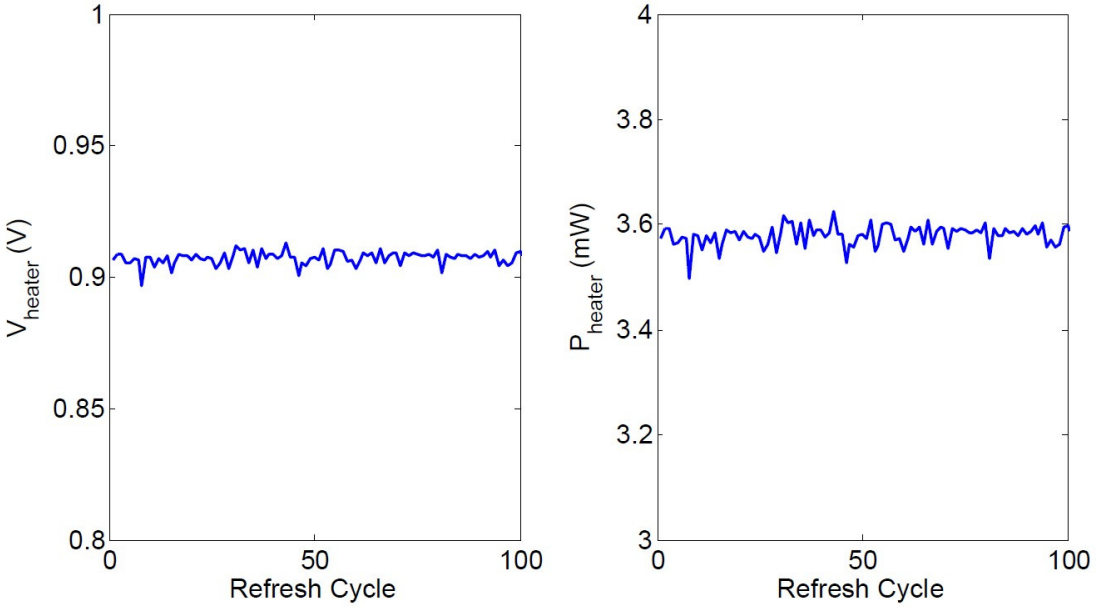

Figure 5.9: Sampling noise (left: heater voltage; right: heater power) of the analog heater control circuit

Figure 5.6 depicts the microphotograph of the mini matrix driver with the analog approach. Unfortunately, due to the metal-fill design patterns, not many details can be seen. The microscope camera optics distorts the parallel edges of the chip. Major circuit blocks, placed in a row of 16 cells for driving the heaters of the ring resonators are marked with a red rectangle in Figure 5.6. The physical area size of one single cell is 100 x 100 μm^2. Each cell contains control circuit logic as well as a microbump pad on which a copper pillar can be grown. The other blocks, nine monitoring TIAs, an address decoder, and test cells, are also marked in Figure 5.6. Each output of the monitoring TIAs is provided to the analog multiplexer. A heater resistor is included inside a dedicated test cell contrary to the 16 cells from the row that do not have a heater integrated inside since their heating resistor is placed in the corresponding PIC cell. All standard pads, used for wire bonding, such as supply pads and pads for control signals are located on the bottom side of the chip. On the left side there are pads for supply and selection of TIAs, while on the right side, there are pads for supply and selection of control cells. These are the pads used for testing the EIC, while supply lines and signals are routed to the pads on the PIC via copper pillar pads, as it is shown in Figure 5.10 and Figure 5.11. The Ge diode for measuring of the temperature of the EPIC chips is placed in the left bottom corner.

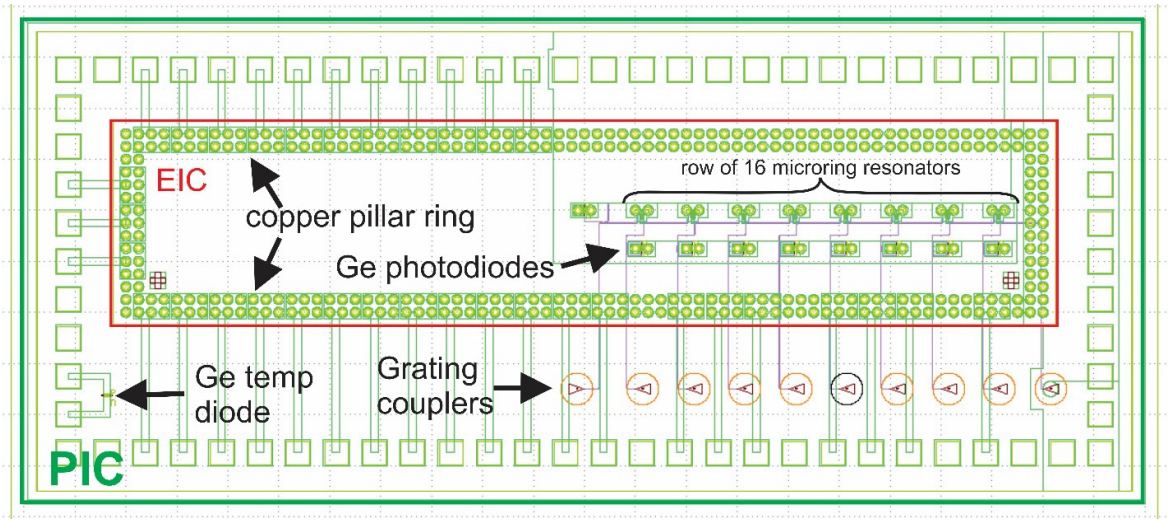

Figure 5.10: Layout of EPIC minimatrix test chip

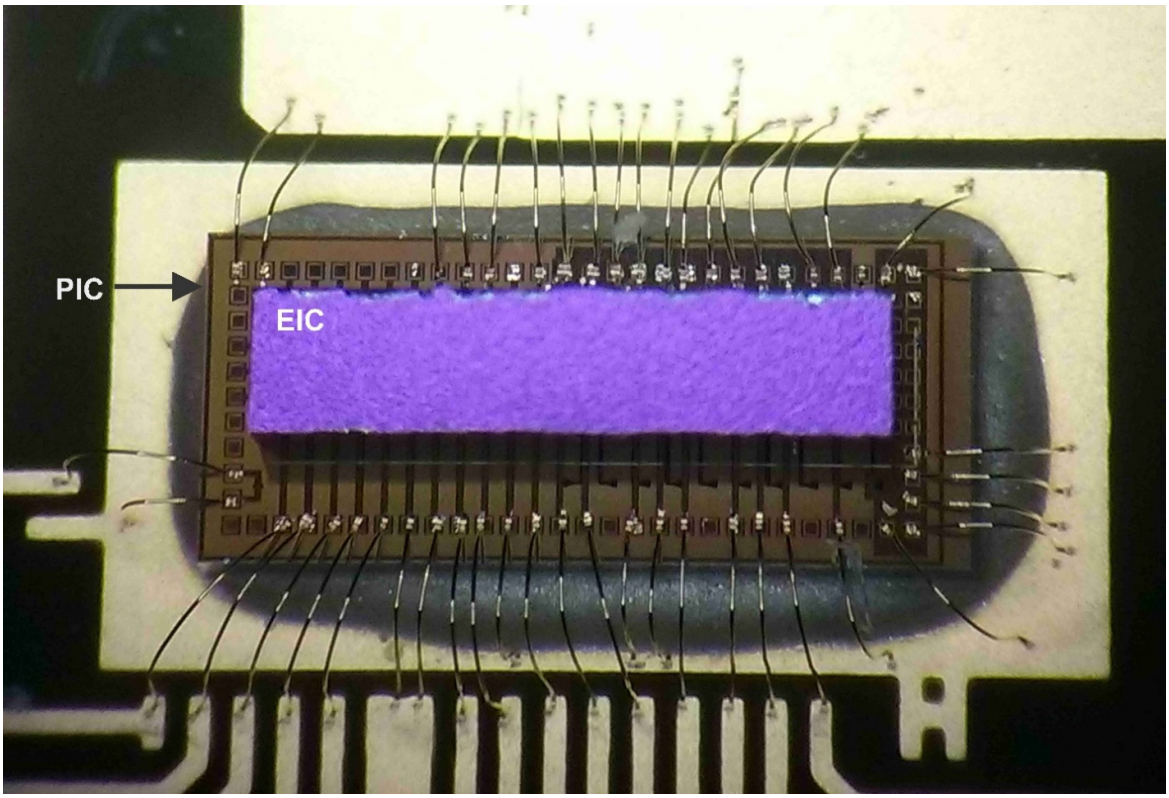

Figure 5.11: Bonded EPIC minimatrix with analog approach for driving heaters

Unfortunately, due to the lack of time this EPIC chip was not photonically characterized during the duration of the project, i.e. during the writing of thesis.

There are two reasons why we have to tune each of the 824 heaters in the full matrix; first, to control the state of the switching elements, and second, to tune the optical elements to compensate for production tolerances.

When it comes to power dissipation of the circuit for analog approach, maximum dissipation on the side of the electronics circuit occurs when resistance of the main MOSFET is equal to the resistance of the heater. Resistance of the heater is 108 Ω, and the power needed

for the tuning range of 20 nm is 28 mW with a voltage supply of 1.8V. For this application, a tuning range of 8 nm is sufficient. This means that the corresponding power of 11.2 mW for the heater is needed. Ideally, we would use the full range if we have a resistance value of the heater of 1.8*1.8V²/11.2mW=290 Ω. The tuning range of heating power would be used more efficiently if the resistance of the heater is close to this ideal value. Power dissipation on the transistor M for the analog approach if we drive the heater to the maximum tuning range of 8 nm is 7.1 mW, calculated by:

$$P_M = \frac{Vdd^2}{(R_H + R_M)^2} \cdot R_M$$

The resistance of the M transistor in on state is marked with R_M.

If we add quiescent current consumption of the circuit times the voltage supply (20 µA x 1.8 V = 36 µW) we obtain total power consumption of the circuit with the analog approach of 7.2 mW. In fact, the efficiency of heating the ring resonator with the analog approach is 61 % (11.2 mW/(11.2 mW+ 7.2 mW)).

The other ring resonators, which are in the off state, should be tuned by 1-2 nm to compensate for production tolerances. The corresponding power consumption of the control circuits of one cell is, in that case, 5.2 mW for 1 nm. Figure 5.12 shows the comparison of power consumption in the PIC and EIC chips for the complete matrix of 768 nodes with the analog approach. The assumption that all the ring resonators are in off state is taken into consideration, since only 16 nodes will be in on state and, for the complete matrix, the power consumption for driving them would be negligible.

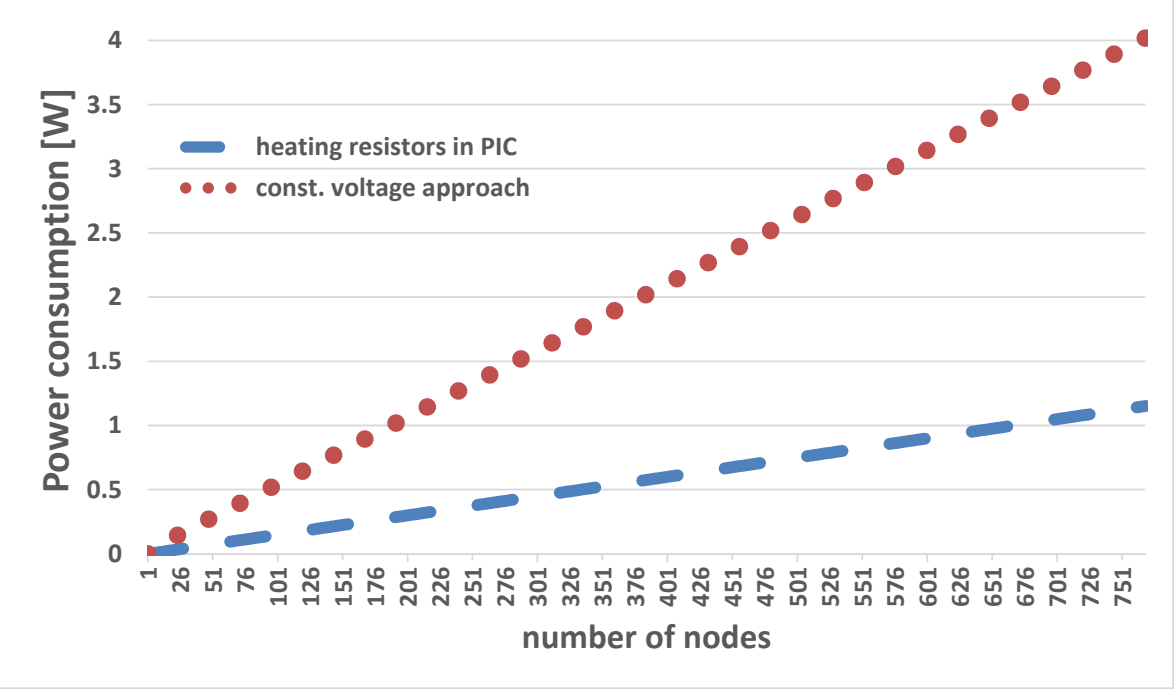

Figure 5.12: Comparison of power consumption of PIC and EIC with analog approach for the matrix of 768 cells

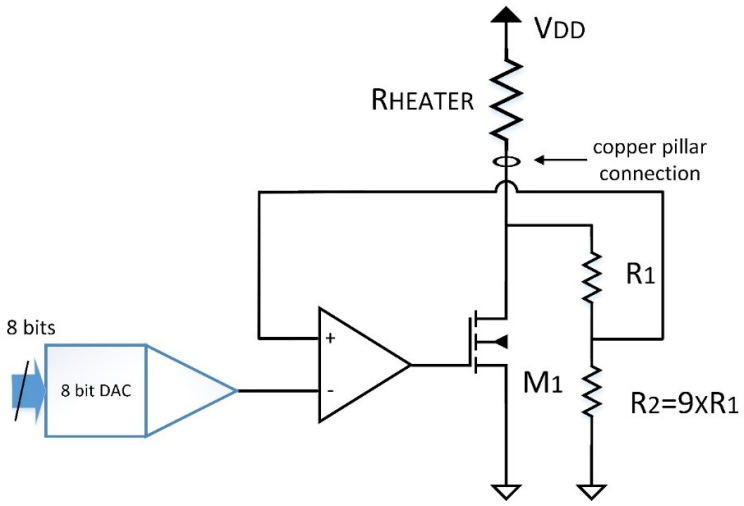

Figure 5.13: Circuit of cell for analog approach with DAC instead of S&H circuit

In Figure 5.13 the implementation of an 8bit DAC instead of the S&H circuit is suggested as an option for the improvement of the analog approach, especially when it comes to avoiding problems with the S&H circuit.

5.2 Digital Approach to Control PIC

One way of thermal tuning of the microring is to control the dissipated power of a heating resistor by pulse width modulation. This heating power could be used for setting the status of the microring, as well as for compensating production tolerance by fine tuning the microrings. Figure 5.14 shows a block diagram for the digitally controlled switch matrix [73].

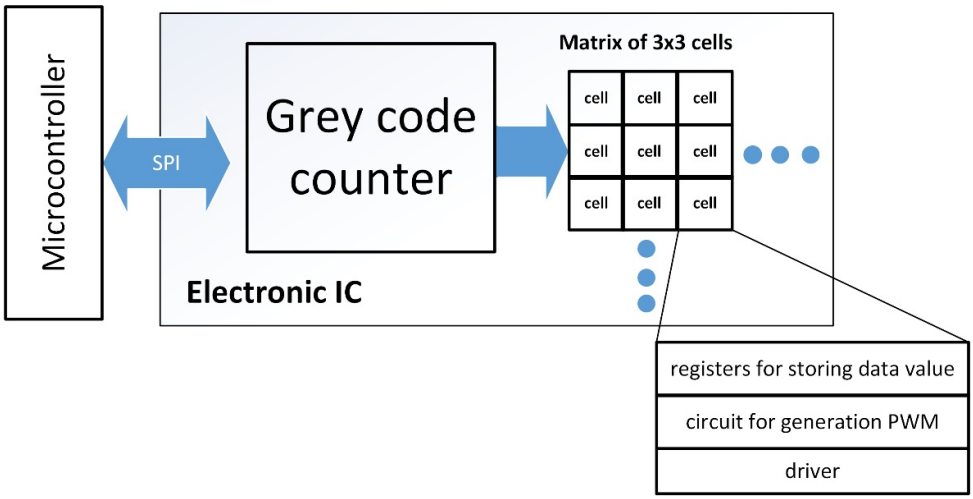

Figure 5.14: Block diagram of electronic IC with digital approach

The chip from Figure 5.20 presents energy efficient scalable implementation of the pulse width modulation (PWM) approach capable of controlling heater power for MRs. In this demonstration chip a 3x3 cells matrix is presented for controlling 9 MRs. The developed approach is scalable to control many more switching elements.

Typical functionality of the optical switching matrix requires only a low number of switches to be in on state and many are in off state. When it comes to controlling the switches in off state, only a small amount of heating power is sufficient for the compensation of production tolerances. They should be tuned in such a way to reach the optimum off position, increasing isolation of the off signal path. In comparison to the constant voltage approach where for these switches most voltage would be across the driver, which means much larger power dissipation on the driver itself than heating power dissipated in the corresponding heater of the microring.

In this PWM approach, contrary to the constant voltage approach, heating power for the MRs is controlled with a change of the duty cycle of the output driver signal presented in Figure 5.17. If the driver is off, there is no power consumption, dissipation on the heater. Leakage currents are neglected. When the driver is on, small saturation voltage of the transistor multiplied with the current through the heater gives a small amount of dissipated power on the electronic chip. A driver transistor (w=420 um, L=180 nm) is designed to have saturation voltage lower than 5 % of the total supply voltage range of 1.8 V. This means that, in on state, power consumption of the driver transistor can be neglected, which is also an advantage of the digital approach, since dissipated power in the EIC could not lead to a detuning of the MRs. The main power consumption of the digital approach lies in the Gray's counter, while a smaller portion is distributed to the digital circuits for the generation of the PWM signal.

The PWM approach has the advantage that it keeps power dissipation of the control circuits low compared to driving the heating resistor with constant voltage.

5.2.1 Implementation with Digital Circuit and Measurement Results

A micrograph of the chip is presented in Figure 5.20. The chip was fabricated in the CMOS part of 160 nm BCD8sP technology. Gray's counter and control matrix are the main parts of this chip (see Figure 5.14). In order to simplify communication between microcontroller and the chip, a serial peripheral interface (SPI) is implemented inside the chip. This interface enables the process of setting heater power for all heating resistors in a serial manner, which requires fewer pads on the chip.

The architecture of the Gray's counter is depicted in Figure 5.15. This architecture guarantees that the counter operates with clock frequencies of 1 GHz and even a little bit above, which was a requirement from the calculations in Chapter 2, in order to provide thermal ripple less than 0.96 ℃, which corresponds to wavelength ripple less than 10 GHz. As it is shown in Figure 5.15, it consists of 7 parallel 128 bit shift registers. As a measure of prevention of

metastability of the flip-flop outputs, since the clock frequency is very high, synchronous reset signal is used for the initialization of registers (see Figure 5.16). The disadvantages of this implementation are a large area and large power consumption; however it is very fast. In Gray's counter, only one bit is different in two successive instants and this is crucial for this purpose. With this counter, we can generate the PWM signal in each matrix cell in a very compact way and it saves us power since the logic is now glitch free. Outputs of the counters are connected further to the drivers, which drive long lines to all matrix cells. Only one counter is necessary for a complete matrix of 16 cells. Power consumption of this counter at 1 GHz is ~80 mW. If the number of elements in the matrix is increased, it could require more than one counter for proper operation.

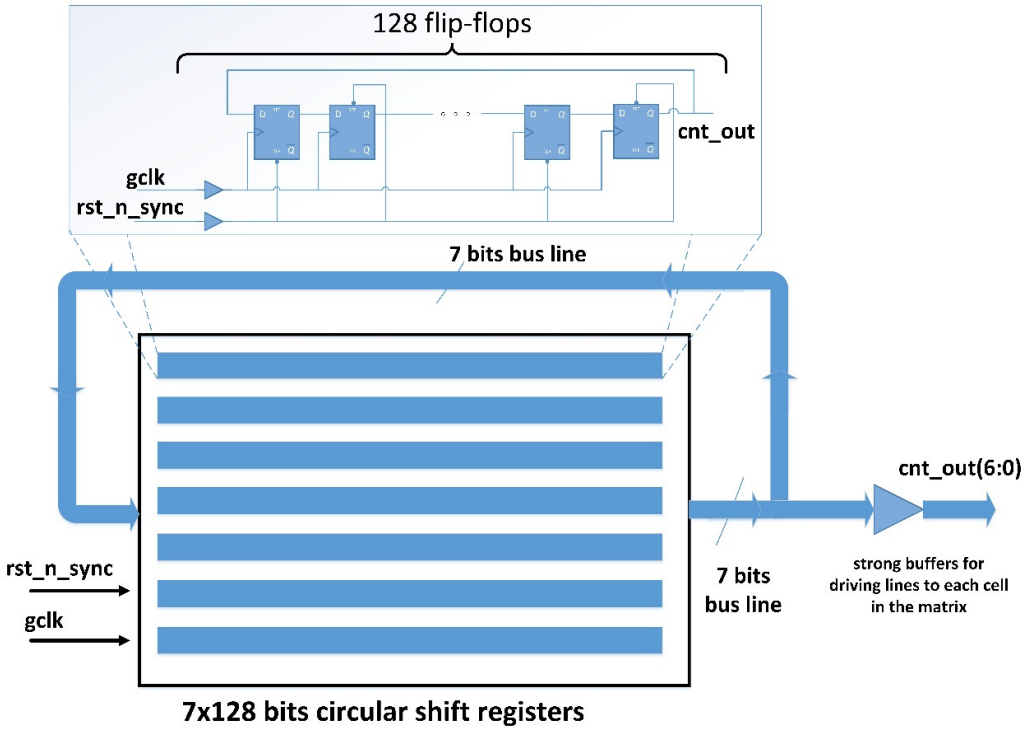

Figure 5.15: Circuit diagram of Gray counter *[73]*

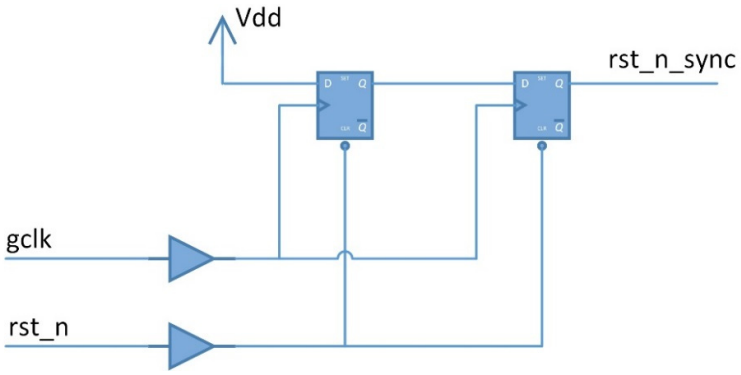

Figure 5.16: Synchronization of reset signal

In each cell of the control matrix the registers for storing the actual heating power in digital form (PWM code) are placed, including a driver circuit for the heating resistor and a logic block for the generation of the PWM signal as it is depicted in Figure 5.17. The generation of the PWM signal is done by flip-flop. Counter values are compared with the stored digital value by an asynchronous digital comparator. When the counter value and stored values are equal, the output of flip-flop is set. The output of flip-flop is connected to the gate of the switching transistor that drives the heating resistor. Overflow signal of the counter resets the flip-flop again.

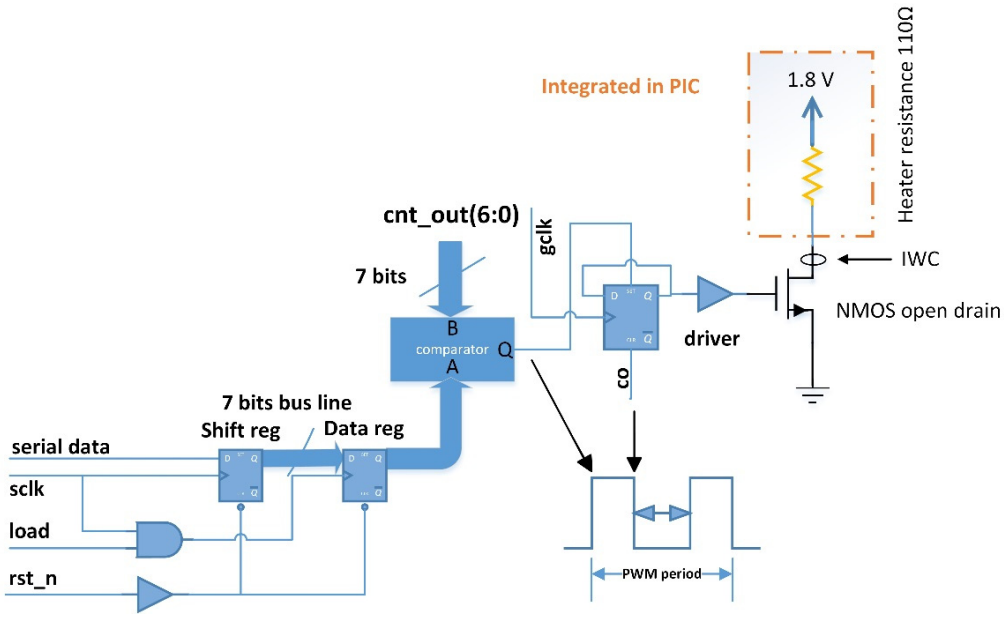

Figure 5.17: Circuit diagram of one cell for digital approach *[73]*

Drain of the transistor is connected to the pad structure which is used for inter wafer connection (IWC) [16]. The connection between the EIC and PIC will add 40 fF of parasitic capacitance. Heater resistances are placed in the photonic IC, they are connected between pad in PIC and supply voltage in PIC. The value of heater resistance is between 110 Ω and 160 Ω depending on the applied voltage. The corresponding maximum heating power is ~28 mW. This heating power is enough for the control temperature range of ~240 ℃ in the microrings (see Chapter 2).

Minimum frequency of 7.58 MHz is required to keep the thermal ripple induced by the PWM control inside the limits as it is already calculated in Chapter 2. In addition, 7 bit pulse width resolution is necessary to tune the resonance of the microring fine enough to activate it and compensate for production tolerances. This give us a minimum clock frequency of the counter for the PWM generation of 970 MHz. This is a simple product of the PWM frequency and resolution (7.58 MHz*128). Digital control circuit and counter are designed to operate with a clock frequency larger than 1 GHz. With 1ns period, the counter is almost on the limit for this technology, because a typical gate has the latency of 200 ps, and the setup time of a flip-flop is in the range of 200-300 ps. So, it is quite tight to design a 7bit counter in synchronous logic in this ST BCD 180 nm technology.

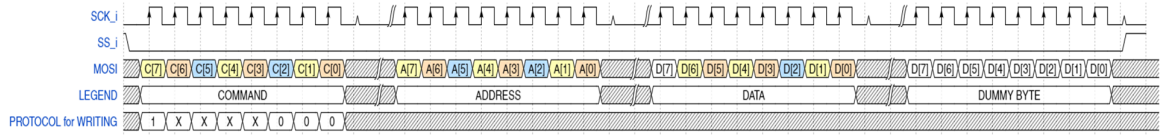

Figure 5.18: SPI transfer protocol for writing data into cell

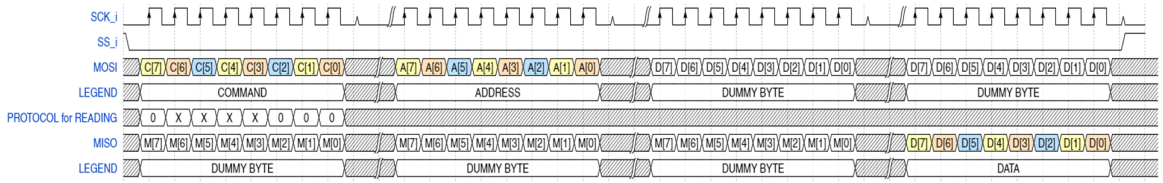

Figure 5.19: SPI transfer protocol for reading data from cell

A protocol for writing data into one cell is shown in the Figure 5.18. The first byte is a command, with an MSB logical one and three least significant bits three zeros. The second byte is an address, followed by data. The last byte is a dummy byte, necessary for storing the data into the cell, since the serial interface and the serial register are used for storing the 8bit data.

A protocol for reading data from a single cell is shown in Figure 5.19. The first byte is a command, with an MSB logical zero and three least significant bits three zeros. The second byte is an address, followed by two dummy bytes. These two dummy bytes are necessary for reading out the data from the cell, since the serial interface and the serial registers are used for storing the 8bit data. The first bit of DATA BYTE is not used, as it is shown in Figure 5.17.

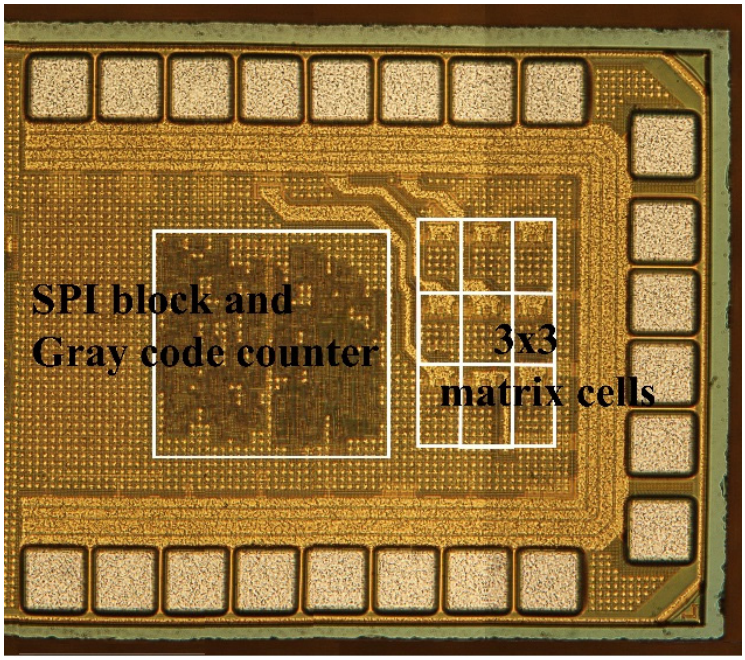

Figure 5.20: Marked micrograph of minimatrix EIC with digital approach

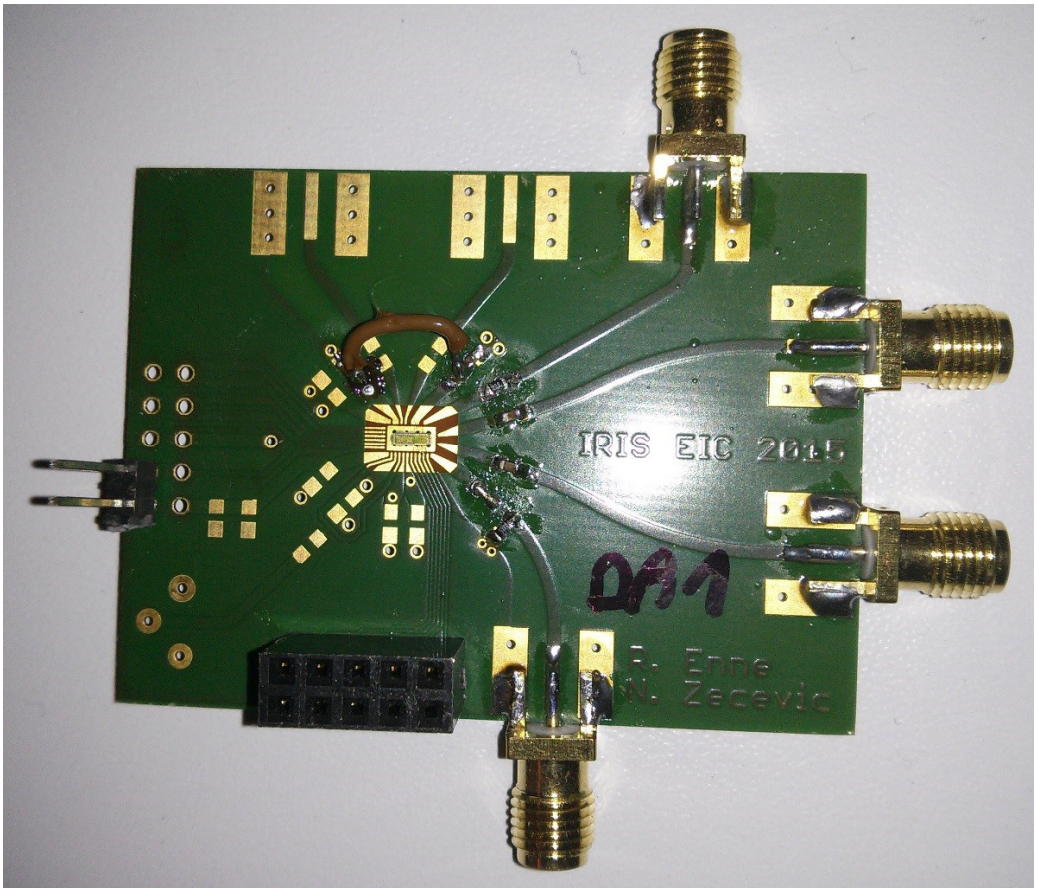

Figure 5.21: PCB with bonded chip with digital approach, electronic components and connectors

The PCB used for measurement and characterization of the digital approach is shown in Figure 5.21. The PWM approach is successfully characterized as it is shown in the results in Figure 5.22. The frequency of the Gray counter clock was varied from 800MHz to 1300MHz. A very linear relation between the PWM code stored in the register and the corresponding mean heating power is proven for clock frequencies of up to 1.2 GHz without missing codes. The linearity is still good at 1250MHz, however, heater power is somewhat smaller. At 1300MHz, a glitch can be observed.

For wavelength resolution of 10GHz, a PWM (pulse width modulation) frequency of at least 7.58MHz with a 7bit pulse width range is necessary, requiring a clock frequency of at least 969.7MHz as it is derived in Chapter 2, Table 2-IV. So, this gives us a margin of 200 MHz and a guarantee that thermal ripple is within the limits for this microring resonator application.

The PWM output signal of the digital heater control test circuit for a clock frequency of 1000 MHz in dependence of the 7bit PWM code in time, is shown in 3D graph, in Figure 5.23. Proper function of the PWM generator circuit is still achieved at 1.2 GH clock frequency as it is shown in Figure 5.24a.

Maximum operating frequency of the Gray's counter is measured to be at 1.2 GHz. At this value, the digital logic block which generated PWM signal reaches its limit. The limit of

the used technology and, in fact, this approach is shown in Figure 5.24b. Output signal of the PWM generator is presented for all possible values of PWM codes at clock frequency of 1.3 GHz. The brighter red lines on the top of triangles of the 3D graph show codes and time periods for which the operation of the PWM generator does not work properly. The explanation is that the maximum operating speed of the counter is reached. The values of the counter are not correct anymore and the digital comparator compares the data stored in the data register with the incorrect counter values. This happens at a clock frequency of approximately 1.2 GHz. Furthermore, the comparator gives false impulses and does not set the flip-flop properly. So, the function of the PWM generator is corrupted, and the output signal stays off or does not behave as we expected. If, of course, at some point, the clock frequency of the counter is further increased, the counter will stop working.

This improper behavior is also visible in Figure 5.22. The mean heating power decreases since the output driver is not set in each PWM period for clock frequencies higher than 1.2 GHz. With an increasing clock frequency, this effect gets stronger.

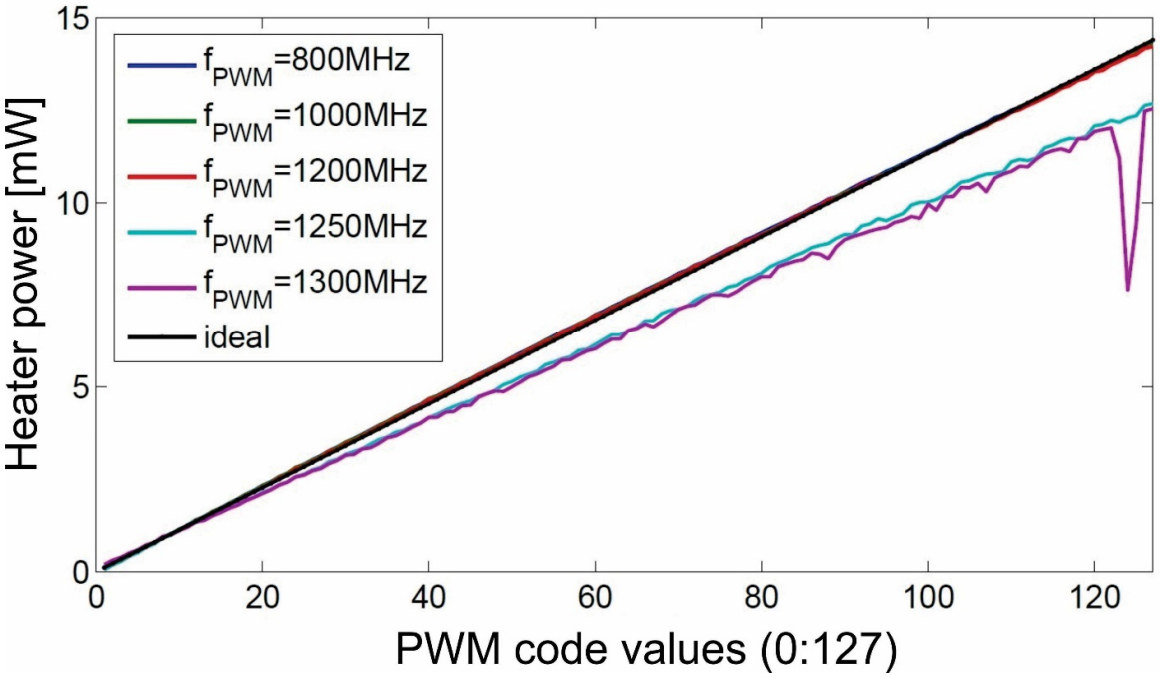

Figure 5.22: Heater power for all possible PWM codes (7 bit) of the digital heater control circuit calculated from measured PWM output signals *[73]*

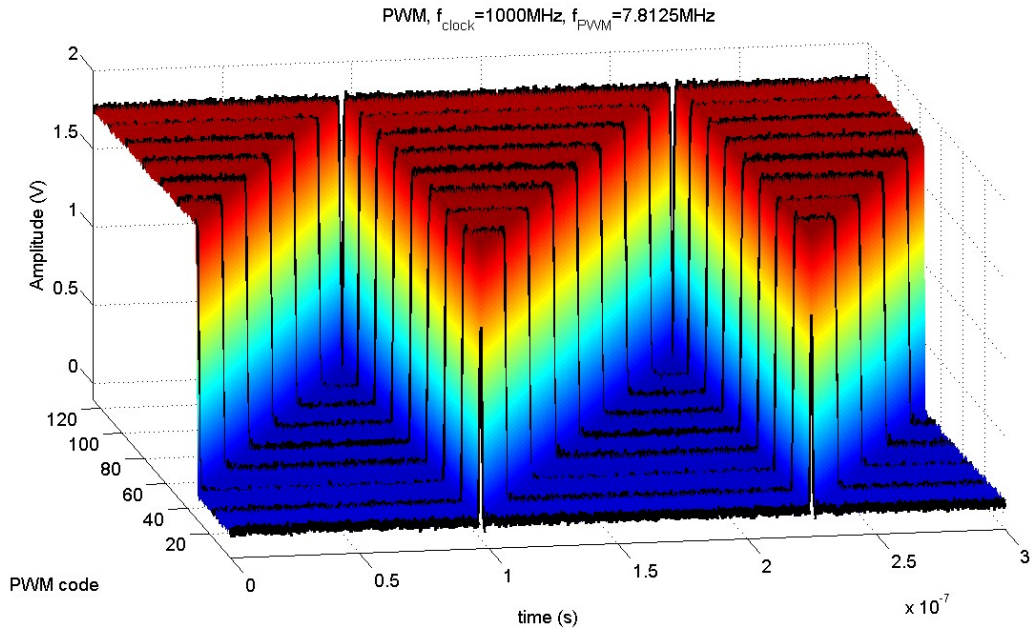

Figure 5.23: PWM output signals of the digital heater control test circuit for a clock frequency of 1000MHz

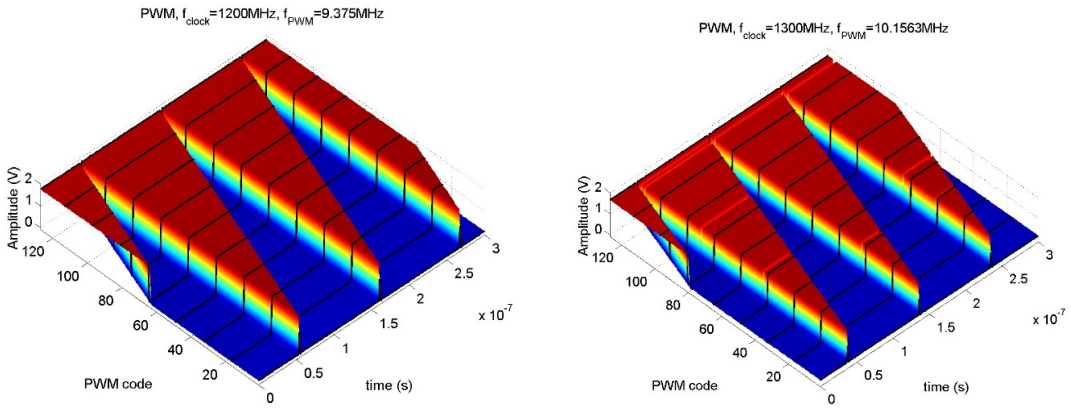

Figure 5.24: PWM output signals of the digital heater control test circuit for a clock frequency of 1200MHz and all possible PWM code values (a) Measured PWM output signals of the heater control circuit for a clock frequency of 1.3 GHz for all possible PWM codes (b)

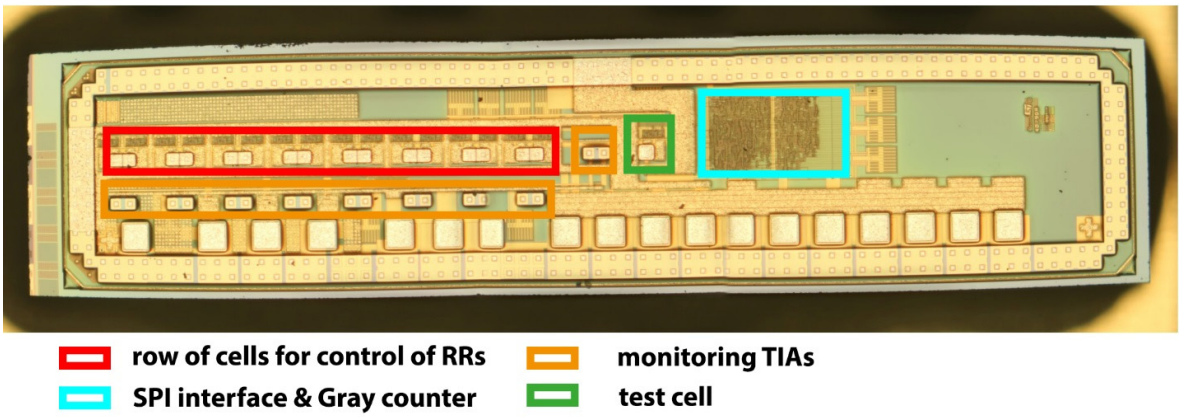

Figure 5.25: Micrograph of the chip with digital approach

Figure 5.25 depicts at zoomed microphotograph of the digital heater control minimatrix EIC chip designed for controlling a row of 16 MRs in the PIC. The chip size is 3.7 x 0.8 mm^2. Due to the metal-fill design rules, not many details can, unfortunately, be seen. The floorplan of the EIC corresponds to the floorplan of the minimatrix PIC shown in Figure 5.10.

Major circuit blocks such as the SPI interface, a Gray counter and a matrix row of 16 cells are visible in Figure 5.25. All 16 cells are identical and contain registers, a digital comparator, a latch, a driver, and fast a 1.8V switching MOSFET. There is an additional 17^{th} cell with an integrated heater resistor for testing. The output of each cell is connected to micro pads on which copper pillars for connecting to the minimatrix PIC structure can be grown. The layout of a cell with the digital approach is shown in Figure 5.26, while the layout of the SPI interface and Gray counter circuits is shown in Figure 5.27.

Nine monitoring TIAs and an analog multiplexer are a part of the feedback monitoring circuit. On the left bottom side, 8 TIAs and an analog demultiplexer are located. For this purpose, there are 8 input signals of 16 input signals of the analog demultiplexer used. On the left bottom side, there are also PADs which are used for connecting the supply, controlling the TIAs and selecting signals of the demultiplexer. Supply PADs and PADs for controlling and testing the 16 cells are located on the bottom right side of the chip.

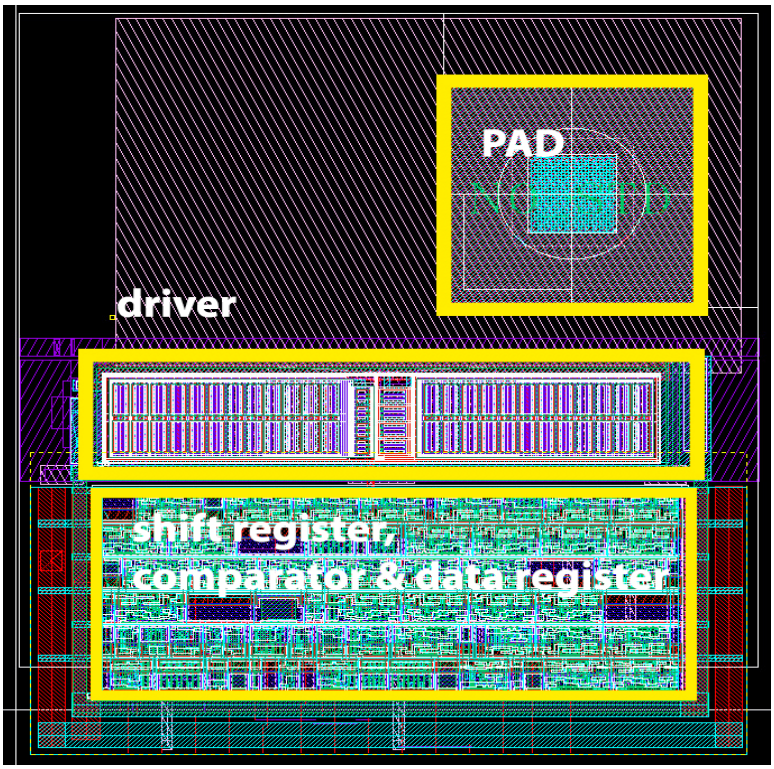

Figure 5.26: Layout of a cell of the digital heater control approach with dimensions of 108.69×108.69 μm^2 (the dimension has to be scaled by a factor of 0.92 to obtain the physical dimension after chip fabrication in BCD8sp; i.e. the physical dimension is 100 x 100 μm^2)

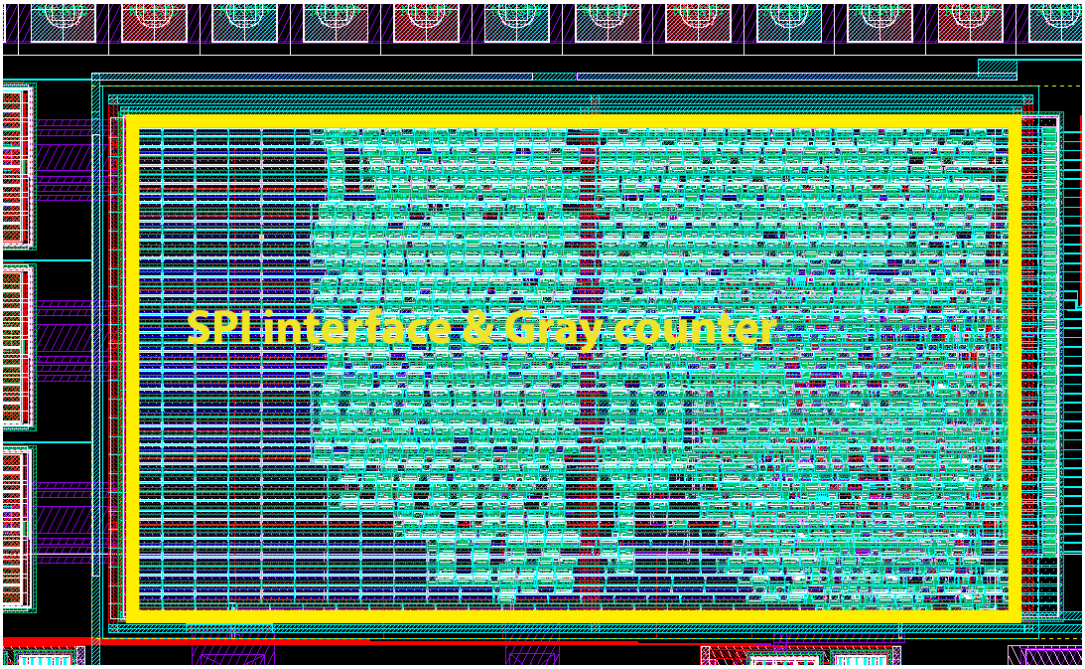

Figure 5.27: Layout of digital approach, SPI block and Gray's counter

5.2.2 Analysis of Power Consumption of the Digital Approach

Only a few microrings are active in a typical optical switch matrix. This means that the power needed for heating them can be neglected in the estimation of the total power consumption of a large matrix. All other microrings have to be tuned by 1-2 nm to compensate for the variations of the process.

Figure 5.28 shows a comparison of power consumption depending on the number of microrings of the matrix cells with the digital PWM approach and power consumption of the heaters in the PIC. For this presentation, only the microrings in off states are considered. The reason behind this lies in the functionality of the optical switch matrix, where only a few microrings are in the on-state.

Power consumption per matrix cell is ~210 µW at a counter clock frequency of 1 GHz. This power consumption is independent of the set of heating power. To this power consumption, the power consumption of the driving transistor in saturation mode should be added. This, results in total power consumption of 0.3 mW per cell in the EIC. Power consumption of Gray's counter at 1 GHz is approximately 83 mW, but only one counter is necessary for supplying (driving) the complete matrix.

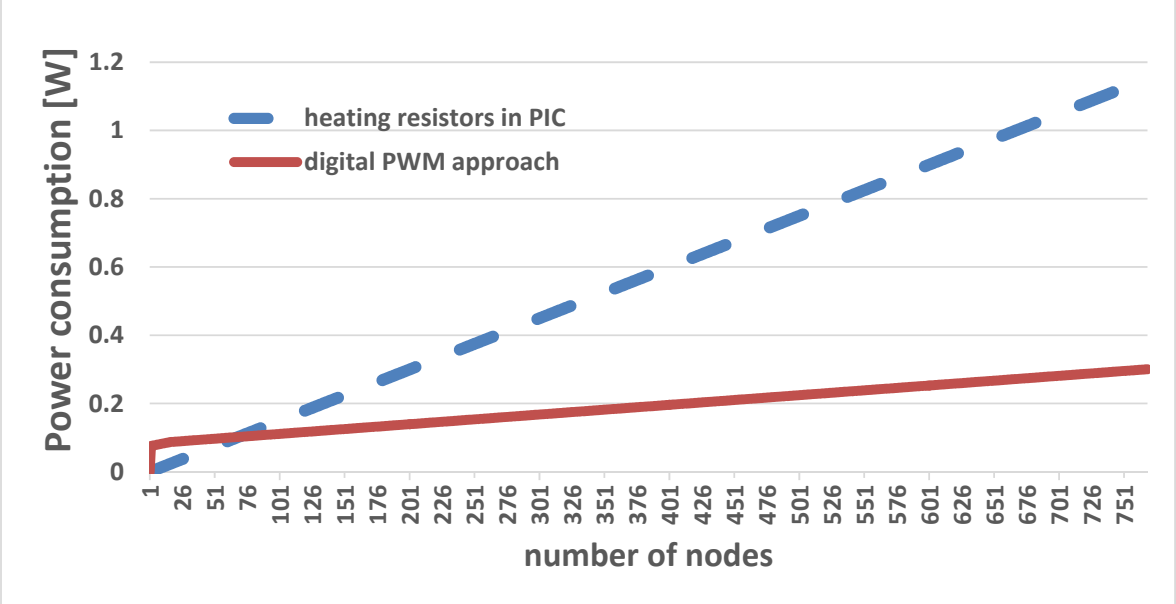

Figure 5.28: Power consumption as a function of the number of photonics switch nodes for the digital PWM approach in comparison to the heater power dissipated by the heating resistors in PIC. Note: only non-active microrings tuned for compensating process variations are considered.

5.3 Analog-Digital Approach for Control PIC

In Figure 4.18, a block diagram of the electronic IC for driving and controlling a large MR switch matrix is presented. The control circuit of one cell of this analog-digital (hybrid) approach is shown in Figure 5.29. The idea of this approach is to use an analog input voltage and to control heating power on the heating resistor by driving it with the digital PWM signal. This PWM approach help us to reduce power dissipation of the control circuits in the EIC. The analog input voltage is stored on a sample-and-hold (S & H) capacitor which serves further as reference voltage. The same S&H circuit is used as shown in Figure 5.2. An operational amplifier is used as a comparator to generate the PWM signal. The structure of the used operational amplifier is described in subchapter 5.1. Two inverter buffers are connected in a serial way to ensure fast switching of the N-channel MOSFET driver (M1). This MOSFET is a high-frequency transistor with a total gate width of 184 µm in configuration of 20 fingers with minimum gate length.

The resistors voltage divider R1-R2 is made with two resistors with values of 2.5 kΩ and 21.5 kΩ, respectively. A certain margin of 0.2 V of the reference signal is necessary to define the off-state of the MOSFET M1 well, as a form of protection from the input offset voltage of the comparator. This voltage divider reduces the active control range of the reference input voltage V_{IN} to 0-1.6V. Supply voltage of the circuit VDD is 1.8V. For a switching behavior which satisfies the specifications derived in Chapter 2, the feedback filter consisting of R_F (200 kΩ), C_F (210 fF) and a hysteresis capacitor (C_{HYST}) are set. Thus, the switching frequency is regulated by hysteresis from the voltage across the capacitor C_{HYST}. Without the pad structure for growing a copper pillar for connection to the heater in the photonic IC, the layout area of the circuits for the hybrid approach of one cell is about 56 µm times 50 µm. Current consumption of the operational amplifier at the switching frequency of 60 MHz is about 43 µA, while the driver stage for the driving transistor M1 takes 73 µA.

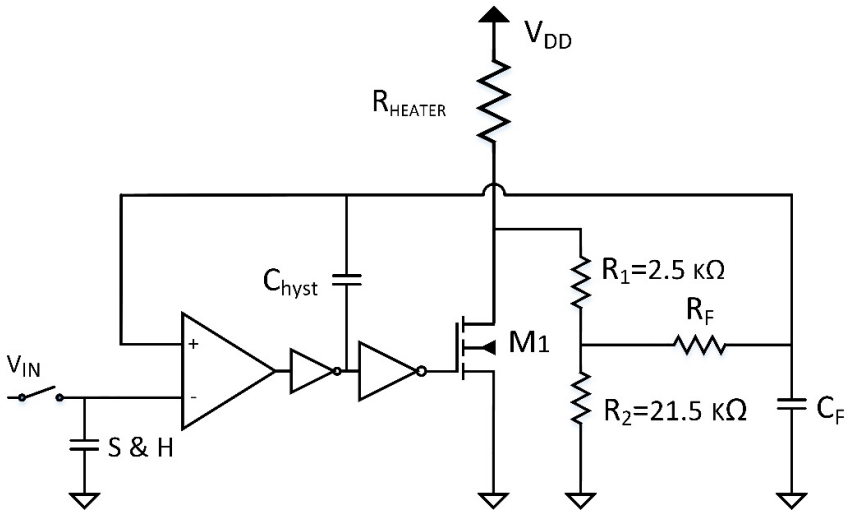

Figure 5.29: Circuit diagram of analog-digital PWM control of one cell with ring resonator *[51]*

A test chip with 16 cells of the hybrid heater control core circuit was fabricated in the first tapeout run. The later improved version of this approach will be presented and compared with original version. The results of characterization of the original version of the hybrid control approach with integrated heater resistors with 230 Ω will be presented in the following paragraphs.

Figure 5.30 shows the wire-bonded EIC chip for testing the hybrid heater control approach. The photo of the PCB used for testing with a bonded hybrid heater control core circuit, discrete electronic components and connectors to the measurement devices is shown in Figure 5.32. A zoomed micrograph of the chip is presented in Figure 5.31. One output pad is presented for each of the 16 cells to enable direct measurement of the PWM waveform. A LeCroy Waverunner WR204Xi oscilloscope and a 3 GHz picoprobe with an input capacitance of 100 fF and an input resistance of 10 MHz were used to record voltage across the integrated heater resistor. Heating power was then calculated by integrating $\frac{V_{Rheater}^2}{R_{heater}}$ over time and further dividing it by total integration time.

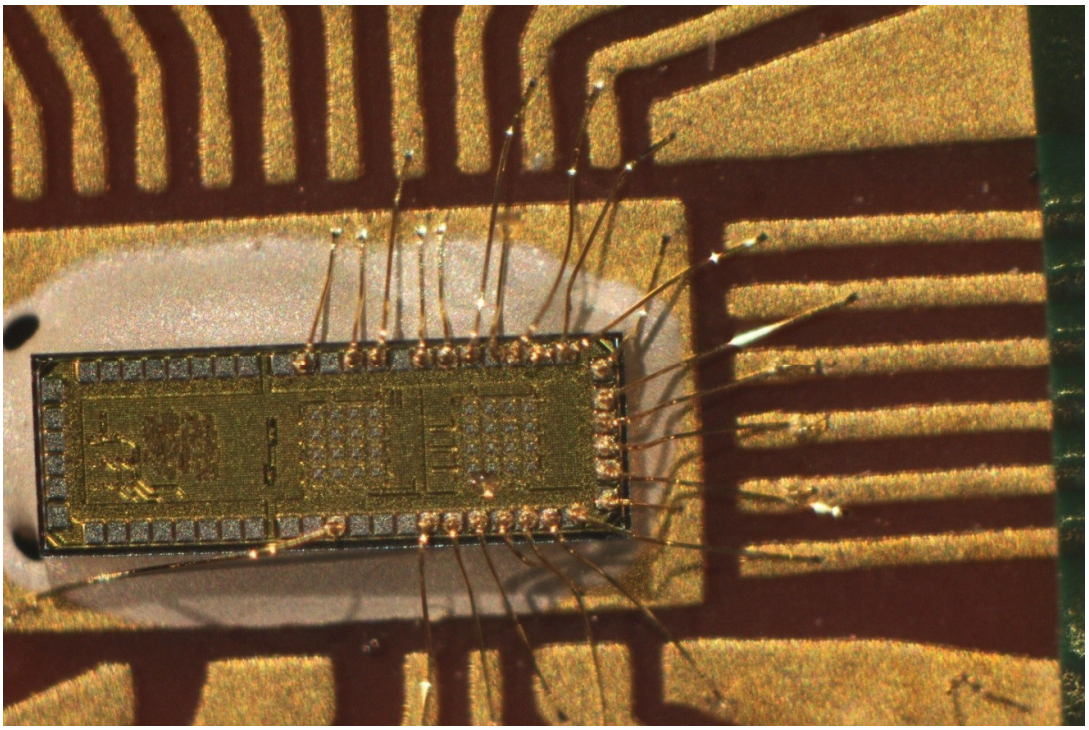

Figure 5.30: Bonded EIC chip for testing circuits of hybrid approach

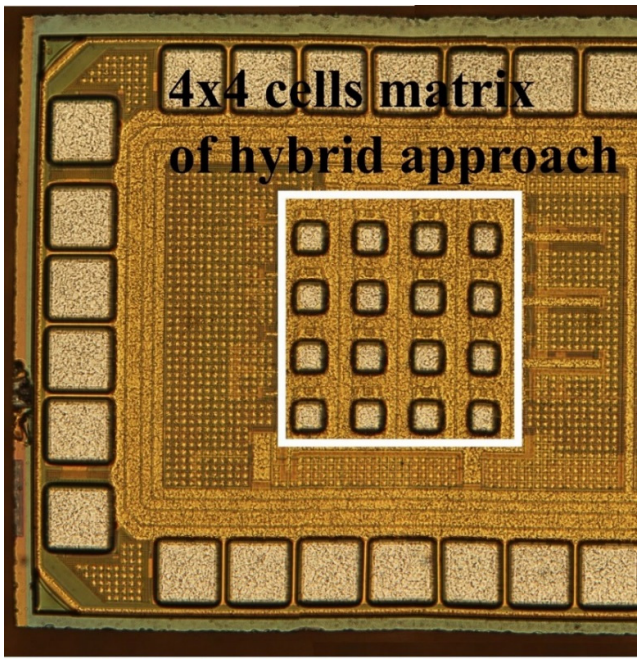

Figure 5.31: Zoomed microphotograph of EIC hybrid heater control core circuit

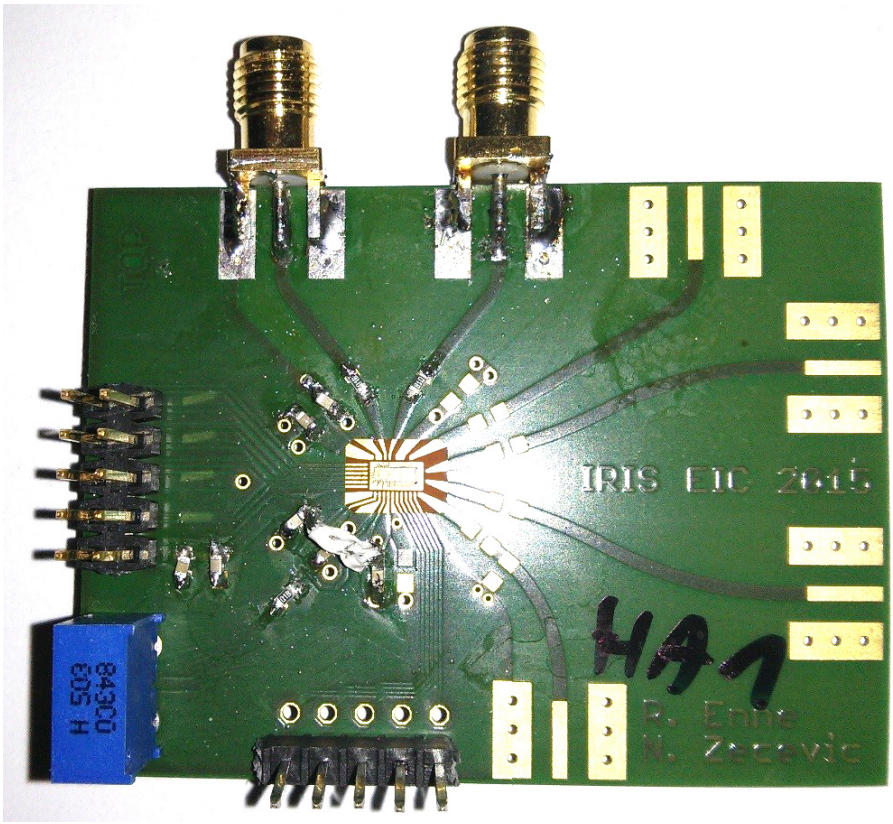

Figure 5.32: PCB for testing EIC chip with hybrid approach with chip, connectors and additional components

In Figure 5.33 presents the measured results of heater power as a function of the input voltage stored in the S & H circuit. As it can be seen, heater power decreases linearly with the input voltage. The PWM frequency as a function of input voltage is presented in Figure 5.34.

The peak PWM frequency is more than a factor of 7 larger in the middle of the input voltage range, where the temperature ripple is the largest. This characteristic is very beneficial since it means that the temperature ripple at the ring resonators will be much smaller for medium heater powers than with the digital heater approach.

Leakage currents in the S & H circuit were investigated very carefully, because they cause an increase in duty cycle in time. This is effect shown in Figure 5.35. It leads to an increase in heater power with time, about 0.7 % per ms. This means that a refresh within 750 µs of each S & H circuit of the matrix is necessary. So, both the analog approach and the hybrid approaches have the same disadvantage caused by the S & H circuit. The effective solution could be an integrated 7-bit DAC inside of each cell.

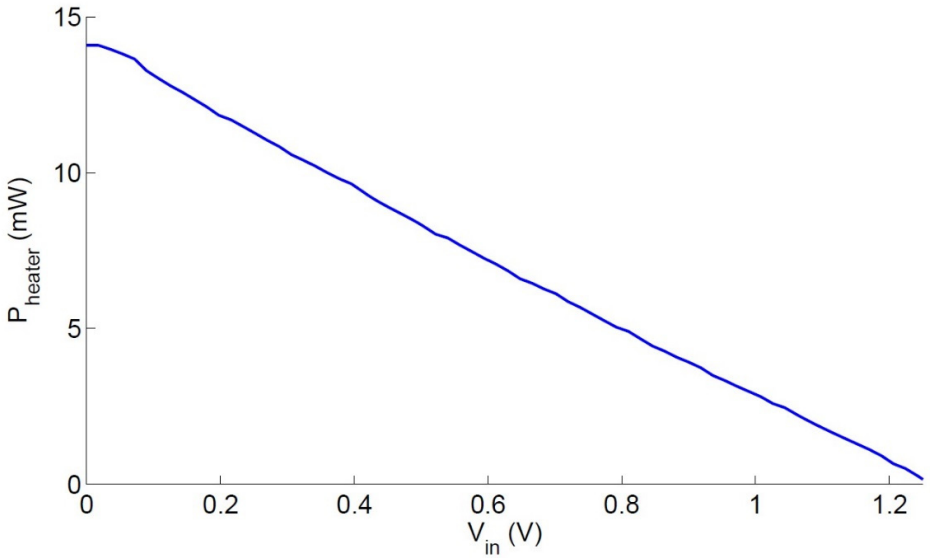

Figure 5.33: Heater power vs. input voltage on S & H circuit of the hybrid approach

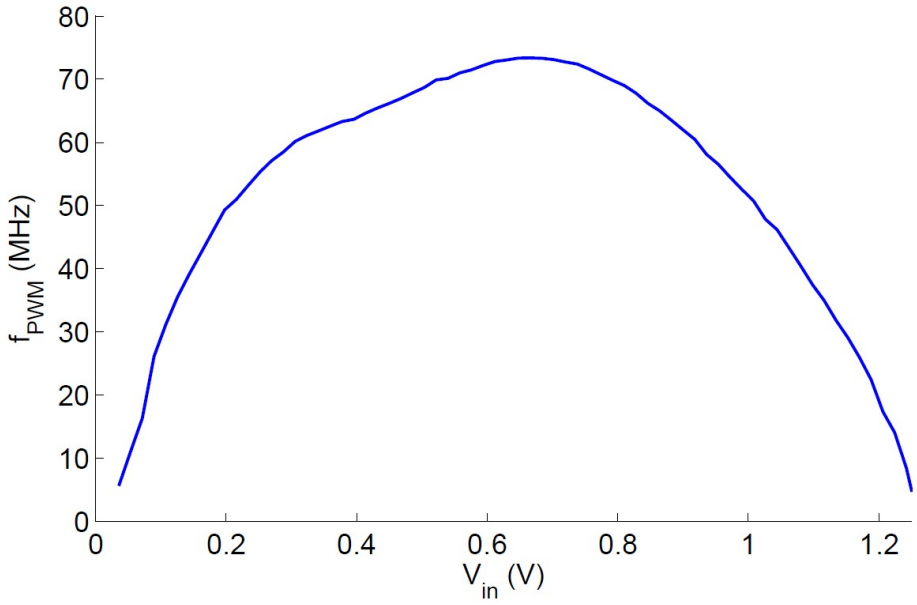

Figure 5.34: PWM frequency as a function of the input voltage on S&H circuit

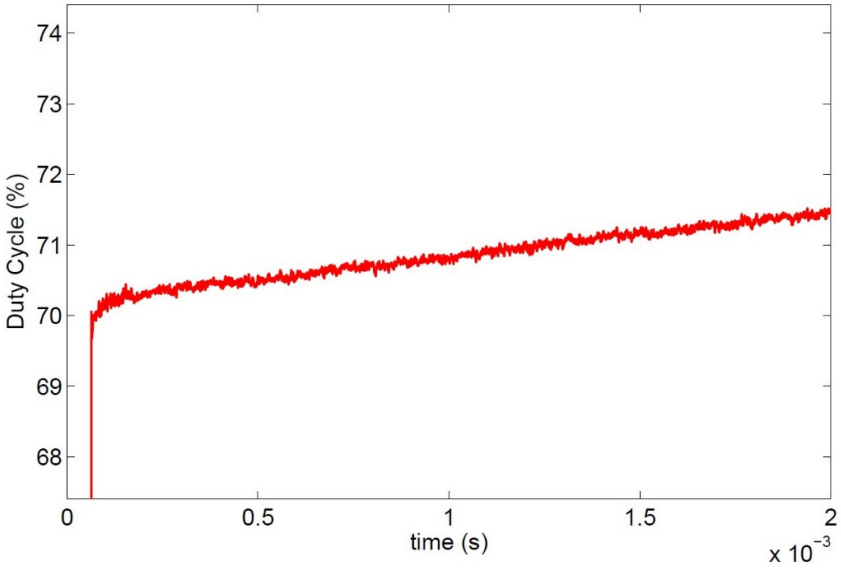

Figure 5.35: Dependence of duty cycle of hybrid heater control circuit on time due to leakage currents in the S&H circuit

Sampling noise, shown in Figure 5.36, causes a standard duty cycle deviation of 0.2 %. This corresponds to a standard deviation of 28 μW of the heater. This standard deviation can cause errors of up to about ±0.1 mW (±3-4 σ), which corresponds to a little bit larger than an LSB in a 7bit resolution. Therefore, it may lead to a partial detuning of the ring resonators.

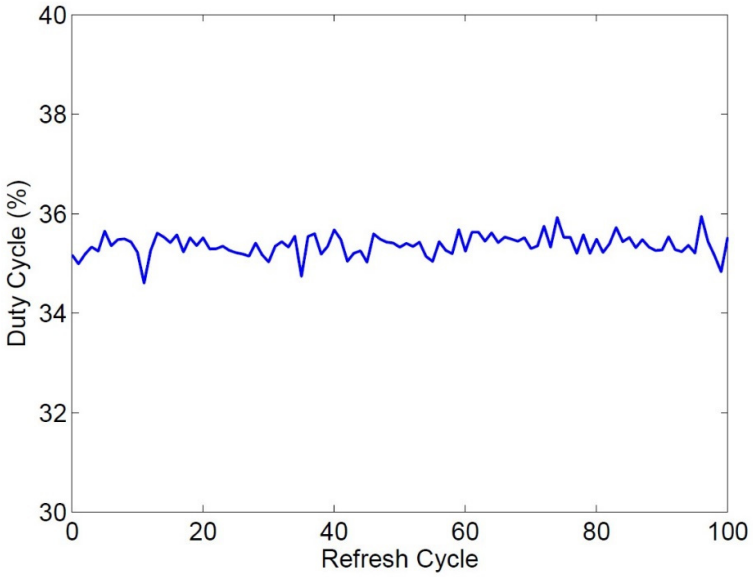

Figure 5.36: Sampling noise on S & H capacitor of the hybrid heater control circuit

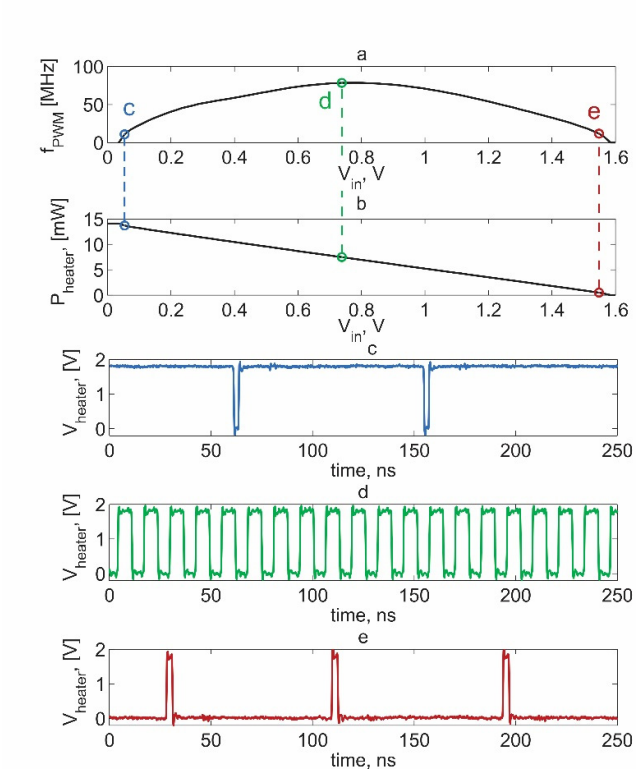

Figure 5.37: Measurement results *[51]*

a mean heating power as function of input voltage on the S & H circuit
b frequency of PWM signal as function of voltage on the S & H circuit
c, d, e Measured PWM voltage waveform of the signal applied on the heater

Figure 5.37 depicts the PWM output voltage waveforms for low, medium and high heater power.

To summarize, a 7 bit DAC is sufficient for loading value into the S & H circuit and a refresh cycle with a frequency of 1.33 kHz for each switch matrix cell is necessary. This means that all nodes have to be refreshed within 750 µs. Compared to the analog approach, this is relaxed by a factor of three. The cause of difference lies in different relationship between V_{IN} and voltage on the heater V_{HEATER}, i. e. heater power P_{HEATER}, in these two approaches. There is a quadratic relationship in analog approach and linear in hybrid control approach.

5.3.1 Improved Analog-Digital Approach

In this subchapter, the results of characterization of the improved hybrid approach are presented and analyzed.

The main improvements of hybrid approach presented in previous subchapter are related to the following four points:

- Input-output characteristic is inverted, i. e. for 0V at the input of the S&H circuit power dissipation on the heater is minimal (this protects the circuit when the leakage current discharges the S & H capacitor – the danger of overheating is eliminated if the refresh is not done on time)
- Increased value of the S & H capacitor by a factor of 10 (the previous value was 550fF, now it is 5.5 pF)
- Added offset of 0.2V, characteristic starts from 0.2V up to 1.8V
- Width of the driver transistor is increased from 184 µm up to 420 µm in order to enable the driving heaters from the AWGs and Interleavers

Measurement results will show that, the critical parameters of the hybrid approach are considerably improved.

Figure 5.38 depicts a circuit diagram of the improved hybrid approach. Dimensions of transistors in S&H circuit are the same as in Figure 5.2, while the value of sampling capacitor is increase by factor of 10.

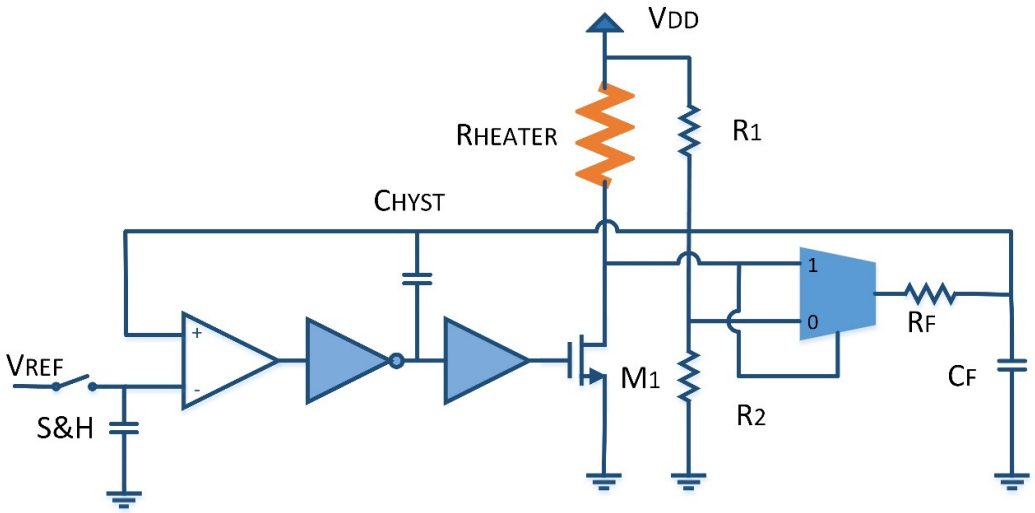

Figure 5.38: Circuit diagram of improved analog-digital PWM control of one cell with ring resonator

Figure 5.39 shows a photo of the PCB with a wire-bonded EIC containing the new hybrid control approach used for testing. Zoomed wire-bonded EIC with the improved hybrid heater approach is shown in Figure 5.40.

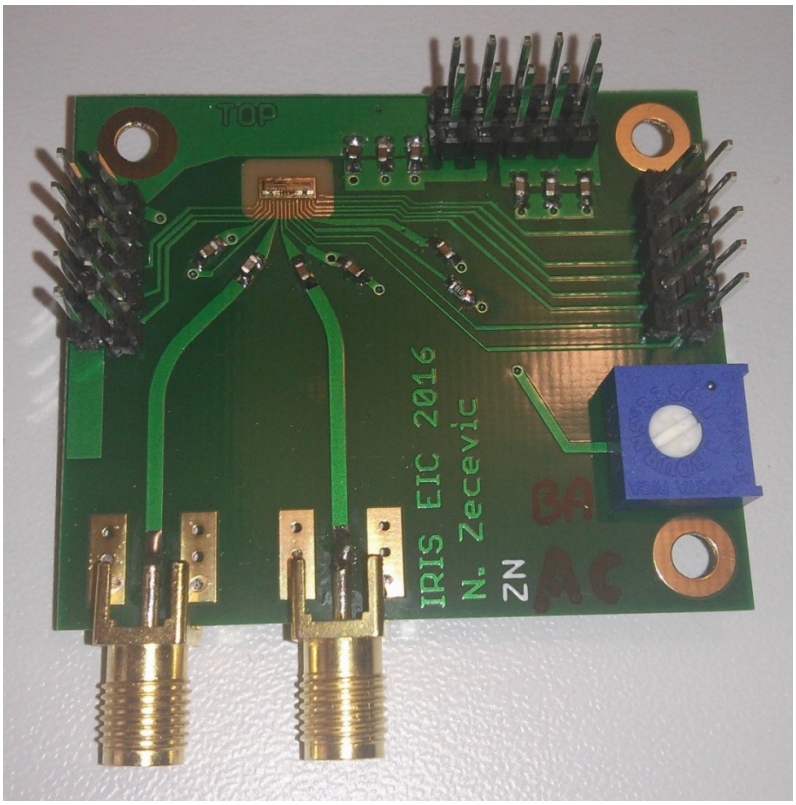

Figure 5.39: Figure PCB for testing EIC chip with hybrid approach

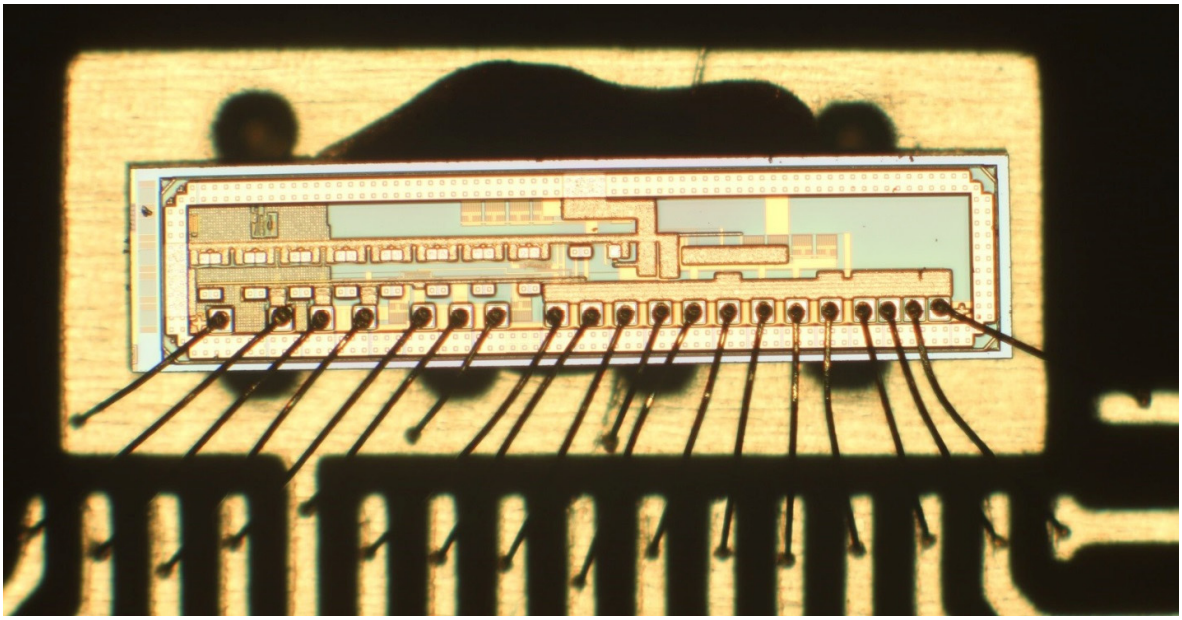

Figure 5.40: Microphotograph of bonded minimatrix EIC chip with new hybrid approach

Figure 5.41 depicts the microphotograph of the mini matrix driver with the new improved hybrid approach design for 3D integration with the PIC minimatrices with different types of ring resonators. Due to the metal-fill design rules, unfortunately, not many details can be seen. The microscope camera optics distorts the parallel edges of the chip. Major circuit blocks in a row with 16 cells for driving heaters of the ring resonators are marked with a red rectangle in Figure 5.41. A layout of a single cell with layout dimensions of 108 x 108 μm^2 (which corresponds to physical dimensions of 100 x 100 μm^2, after applying scaling factor of 0.92), designed to fit into matrix pattern, is shown in Figure 5.53. Each cell contains control circuit logic as well as a micro pad on which a copper pillar can be grown. Other blocks, monitoring TIAs, an address decoder, and test cells, are also marked in Figure 5.41. There are in total 9 monitoring TIAs. Each output of the monitoring TIAs is provided to the input of the analog multiplexer. A heater resistor is included inside the test cell contrary to the 16 cells from the row which do not have a heater integrated inside them. Total dimensions of the mini-matrix EIC chip are 0.8 mm times 3.7 mm.

The floorplan of the EIC is defined by a PIC layout, Figure 5.10, i.e. to match the copper pillar positions for 3D integration.

Unfortunately, due to the lack of time this EPIC chip was not photonically characterized during the duration of the project, i.e. during the writing of thesis.

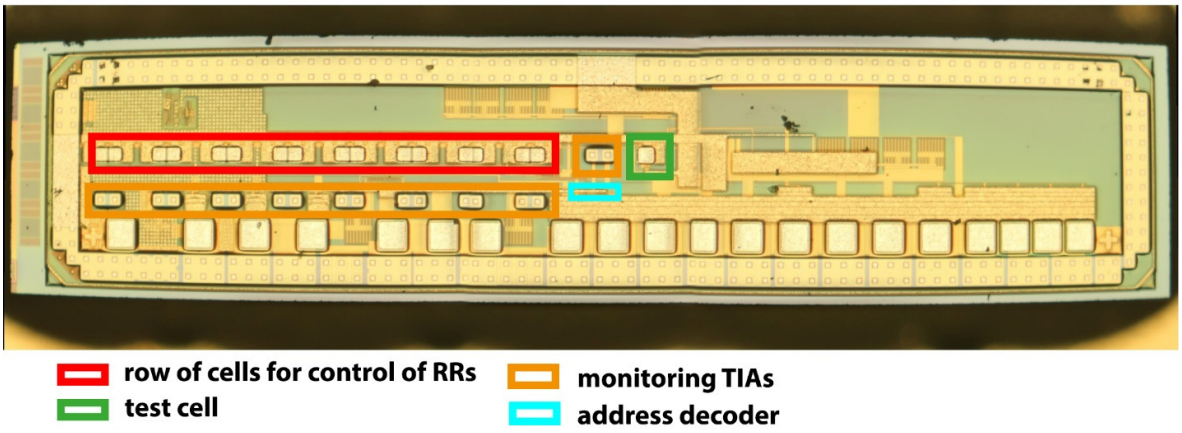

Figure 5.41: Micrograph of EIC chip minimatrix with hybrid approach

5.3.2 Minimatrix Test Chips with Bondpads

Figure 5.43 shows a microphotograph of the mini-matrix driver chip with the new improved hybrid approach and pads for wire bonding. Due to the metal-fill design rules, not many details can be seen. On the right side of the chip, there is the major circuit block, a row with 16 cells for driving heaters of the ring resonators, which is marked with a blue rectangle. A layout of a single cell is shown in Figure 5.53. All cells are identical and contain control circuit logic. Other blocks are also marked in Figure 5.43, along with monitoring TIAs and an analog multiplexer. There are 5 monitoring TIAs in total. Each output of a monitoring TIA is provided

to the input of an analog multiplexer. Total dimensions of the mini-matrix EIC chip with bond pads are 0.8 mm x 3.7 mm.

Measurement and characterization of the improved hybrid approach circuits are done with this chip and the PCB shown in Figure 5.42.

A PXI system from the National Instruments, as well as a fast real-time oscilloscope, were used for the characterization of the improved hybrid approach. The NI PXI system was used to generate analog and digital control signals for the EIC, as well as to provide and monitor the supply voltages.

A heater resistor of 100 Ω was used for the purpose of characterization.

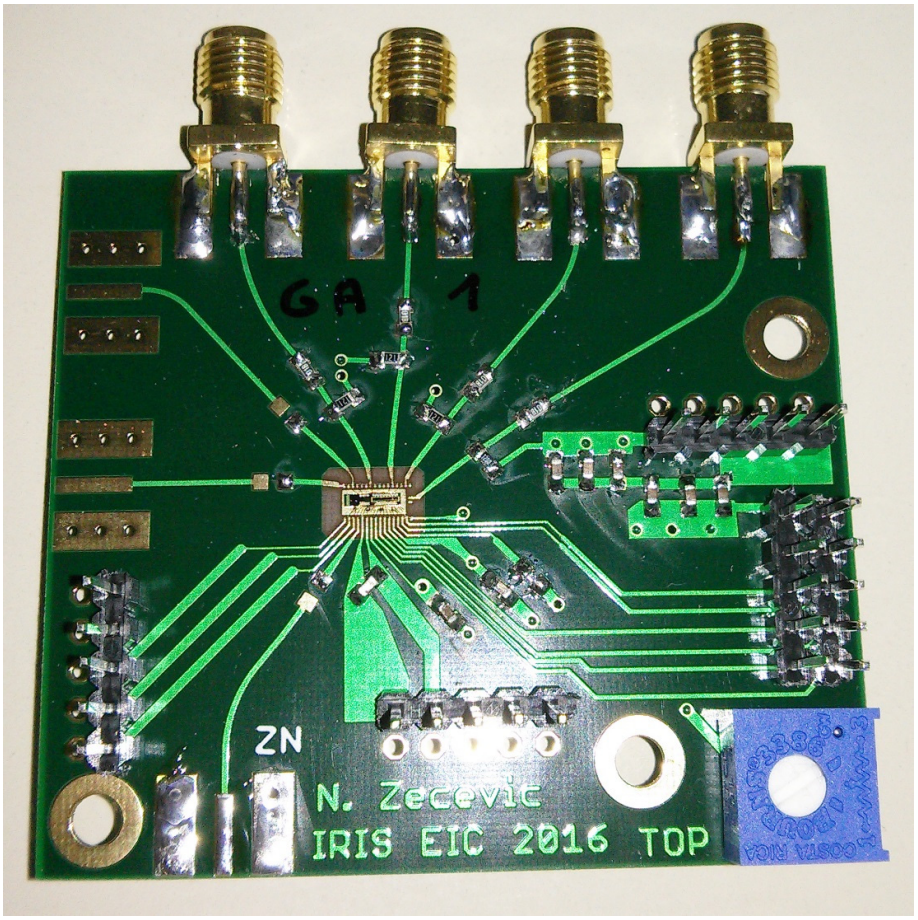

Figure 5.42: PCB with bonded minimatrix EIC chip with improved hybrid approach and with bond-wire pads, electronic components and connectors

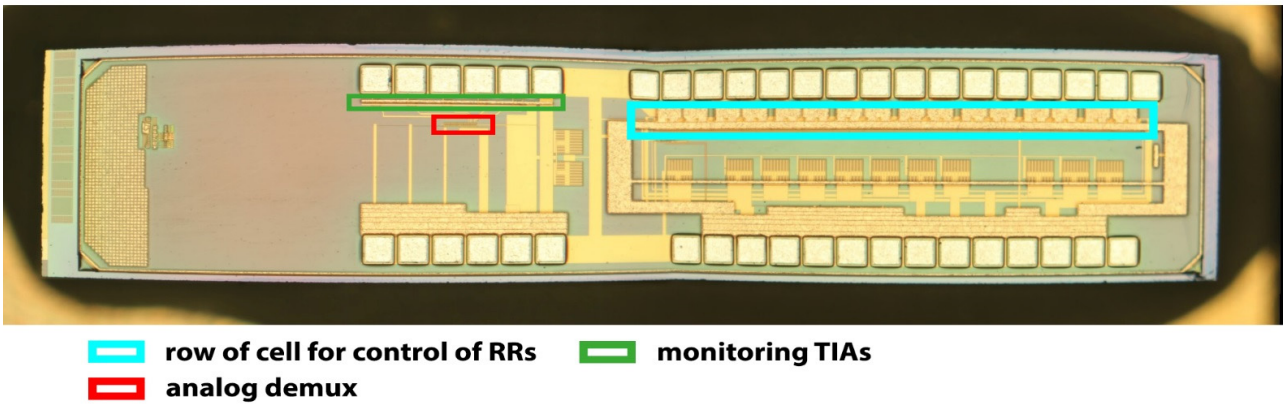

Figure 5.43: Marked microphotograph of minimatrix EIC containing the new hybrid approach with bondpads

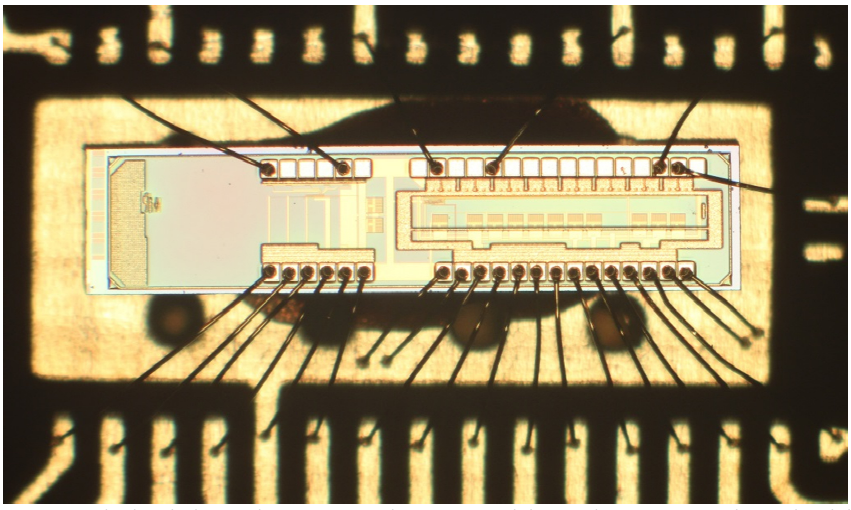

Figure 5.44: Bonded minimatrix EIC on the PCB with analog approach and with standard bond-wires

Figure 5.45 shows the dependence of mean heater power with the input voltage V_{IN}, stored in the S & H circuits. On the figure, there are the plotted characteristics of the 4 selected matrix cells with the new hybrid approach. One major improvement of the new hybrid approach compared to the old one is that now maximum heater power is reached for maximum input voltage (1.8 V) instead of 0V. This is a very important improvement since the S & H elements have a certain leakage current that discharges the S & H capacitor over time. The stored voltage will tend to zero if the value into the S & H circuit is not loaded frequently. As a consequence, with the old hybrid approach, heater power values of all matrix elements would reach their maximum values if the refresh cycle is interrupted. This would lead to the thermal destruction of the EIC. The risk is omitted in the new hybrid approach. In order to guarantee that all matrix cells can be turned off completely the offset of the characteristic is embedded. This means that heater power starts to increase only for input voltages larger than approx. 0.2 V, this is set during the design phase. This offset is larger than process dependent offset variations could be, thereby guaranteeing that all matrix cells can be completely turned off. Small variations of the

characteristics of the different analyzed matrix cell are not critical, because the necessary heater power needs to be calibrated for all photonic elements anyhow.

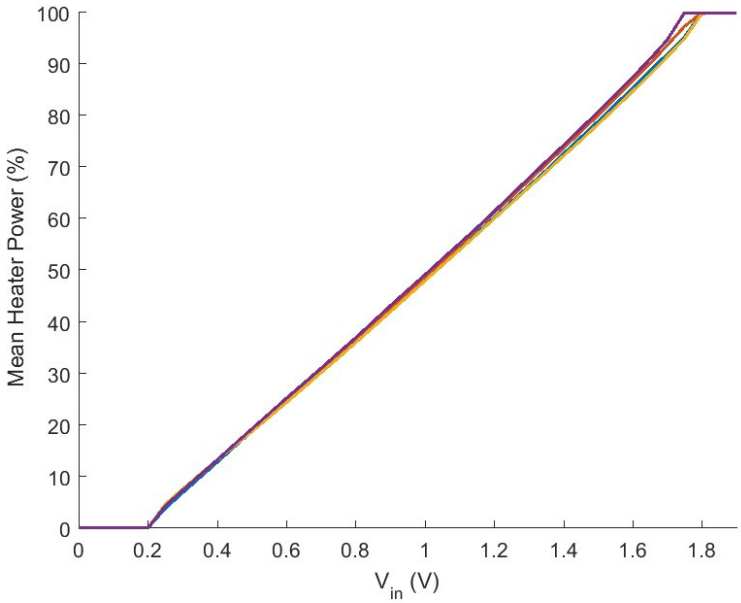

Figure 5.45: Mean heater power as function of input voltage for 4 selected matrix cells *[74]*

In Figure 5.46, pulse width modulation frequency in a function of input voltage is shown for the 4 selected matrix cells. This behavior is similar to the old hybrid approach, the PWM frequency depends on the set heater power, and reaches its maximum value of approximately 70 MHz at 50% heater power. Maximum frequency of the new hybrid approach is the same as for the old hybrid approach set to keep the PWM induced temperature ripples below critical limits, described in Chapter 2.

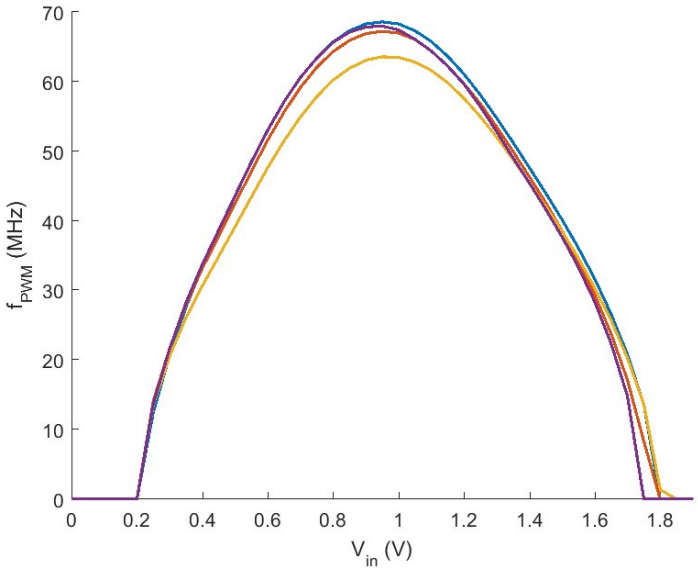

Figure 5.46: PWM frequency as function of input voltage V_{in} for 4 different matrix cells *[74]*

In Figure 5.47, the influence of sampling noise of the S & H capacitor is presented for the 4 selected matrix cells. The figure is generated in the following way: for each input voltage shown, an S & H element was refreshed 1000 times, and heater power after each refresh cycle was extracted. Heater power varies slightly after each refresh cycle. The reason behind is sampling noise and cross talk, although the same input voltage was applied. In order to guarantee that microring resonance is not detuned significantly, these variations must be small enough.

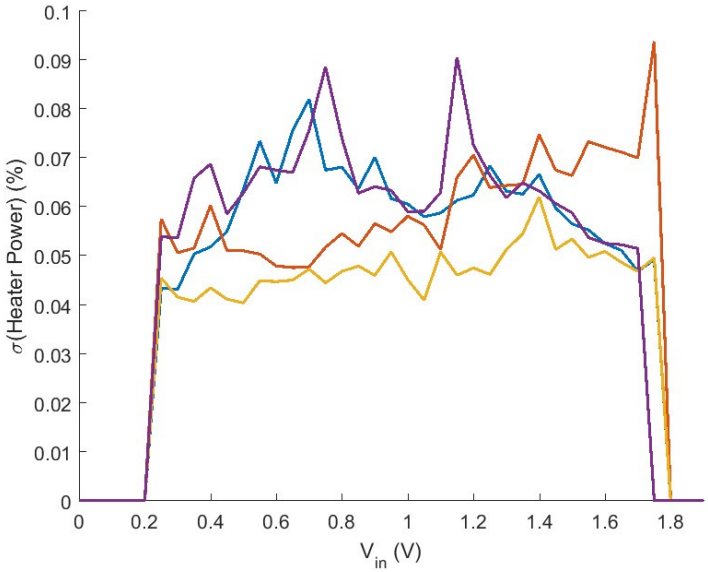

Figure 5.47: Standard deviation of the heater power after loading the sample & hold capacitance 1000 times with a constant voltage value, for the whole input range and 4 selected matrix cells

Standard deviation of the output power in the old hybrid approach was in the range of 0.2%, which is acceptable especially for the double ring switches. Characterization of the new approach showed a standard deviation of the set heater power in the range of 0.04% to 0.09%, in the entire possible heater power range. This improvement is considerable, mainly caused by an increased sampling capacitance. The risk that sampling noise could considerably affect the performance of the final device is reduced.

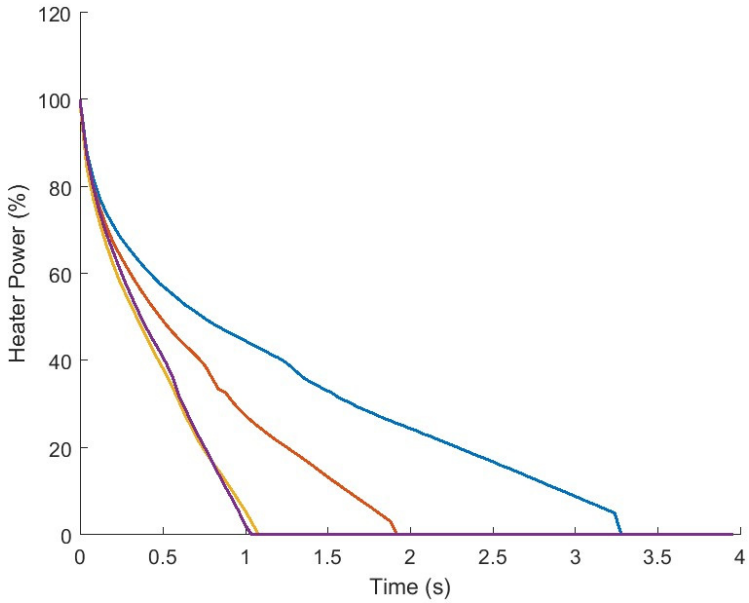

Figure 5.48: Drop of the heater power due to leakage in the S & H circuit after stopping the refreshing cycles for 4 selected matrix cells *[74]*

This increased capacitance of the S & H circuit has another major advantage. Due to the leakage currents in the S&H circuit, voltage has to be refreshed after a certain time. The refresh time period of ~750μs was necessary in the old hybrid approach and this was already achievable with the microcontroller ATMEL XMEGA used to control the combined full matrix EIC/PIC chip described in Chapter 4. However, this refresh time was quite at the limit of this microcontroller. The increased sampling capacitance considerably reduces the voltage drop rate, shown in Figure 5.48. This leads to relaxed refresh requirements. In the old version of the hybrid approach the change of heater power over time was in the range of 0.7%/ms, without the refresh. As shown in Figure 5.48, the leakage varies significantly for different matrix cells. Additionally, the drop rate changes for different settings of the address decoder during the time when the refresh is stopped. The maximum measured drop rate shown in Figure 5.49 is in the range of 0.35%/ms, which is approximately one half of the drop rate of the old hybrid approach. The corresponding refresh time would be approximately 1.5ms. In the new hybrid approach, the drop rate is the largest for the highest heater power. As it can be seen from Figure 5.49, for heater power below 80% it decreases rapidly below 0.2%/ms, reaching the values close to 0.1%/ms for heater power below 65%.

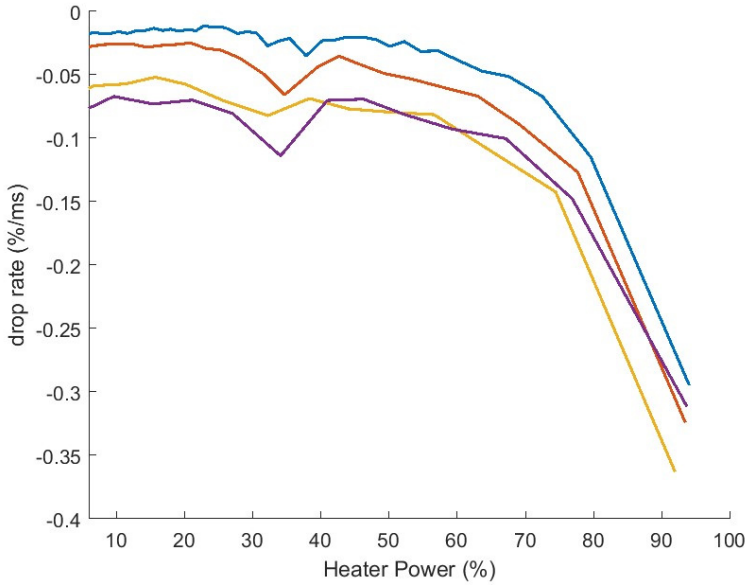

Figure 5.49: Drop rate of the heater power caused by the leakage currents in the S & H circuit dependent on the actual heater power for 4 selected matrix cells

There are few reasons behind this effect of a larger leakage current for larger voltages on the S&H circuit. One reason could be the dependence of leakage currents in the MOSFET transistor with the voltage across drain and source. The typical behavior is shown in Figure 5.50 and Figure 5.51 ([75] and [76]). Values for my technology, BCD8sp, are not available so I tried to explain behavior with literature results. It can be seen from the figures that for larger drain-source voltages, the leakage current is also larger. Gate-Induced Drain Leakage (GIDL) effect is also shown in Figure 5.50. The second cause lies in the supply voltage drop on the supply lines for digital logic which controls the switches of the S&H circuit. So, these transistors are not 100% turned off, i.e. V_{GS} of the PMOS transistors is not 0V. Therefore a slightly larger V_{GS} voltage according to Figure 5.50 results in a larger leakage current contrary to the situation when the PMOS transistor is completely turned off. The drain leakage current has exponential dependence with V_{GS} in a weak inversion regime. Subthreshold swing is ~70..100mV/decade.

These are two assumptions explaining nonlinear dependence of the leakage current and drain-source voltage. However, more precise investigation of this effect would require a design of several different S&H circuits and deeper characterization, which, due to the defined project schedule, was not possible. Also, there is the question of accuracy of transistor models when they work in weak inversion mode.

However, there are some techniques for the reduction of this influence on the overall functionality of the circuit. The first one would be the separation of the supply lines for the S&H circuit, the second one could be the shrinking of the input voltage range, e.g. from 0.2-1.8V to 0.2-1.6V. However, the best solution for all the weaknesses of the S&H circuits, would be a replacement with an 8bit DAC with a voltage output. The design and characterization of the circuits with this approach are described in the Subchapter 5.4.

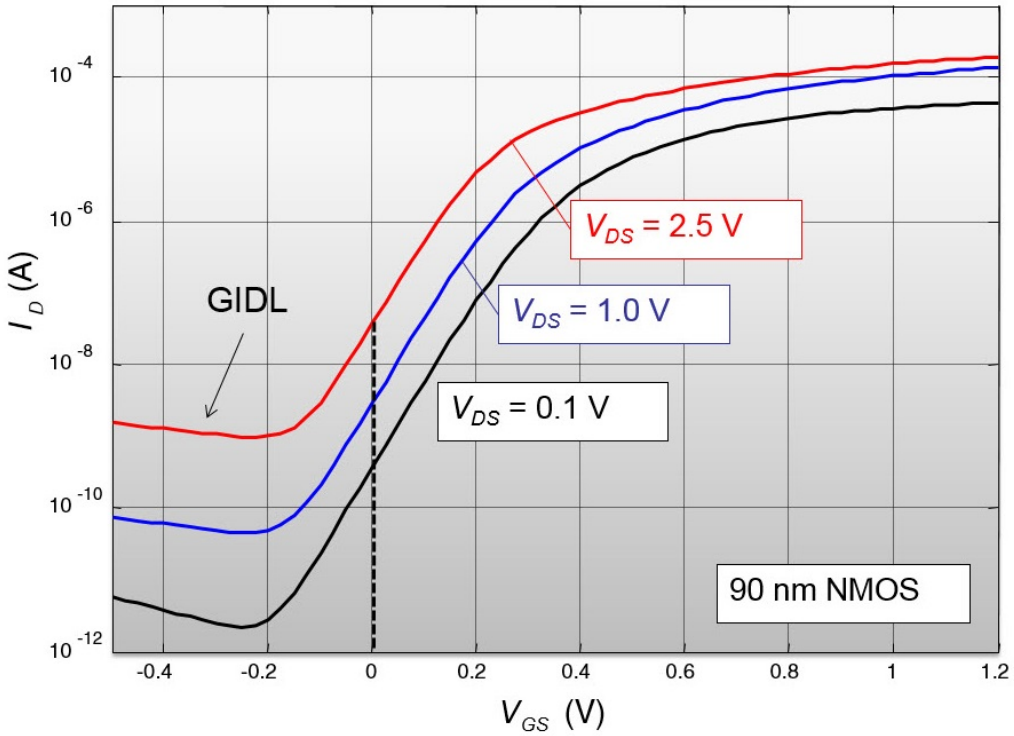

Figure 5.50: Drain leakage current in dependence of V_{DS} and V_{GS} voltages *[75]*

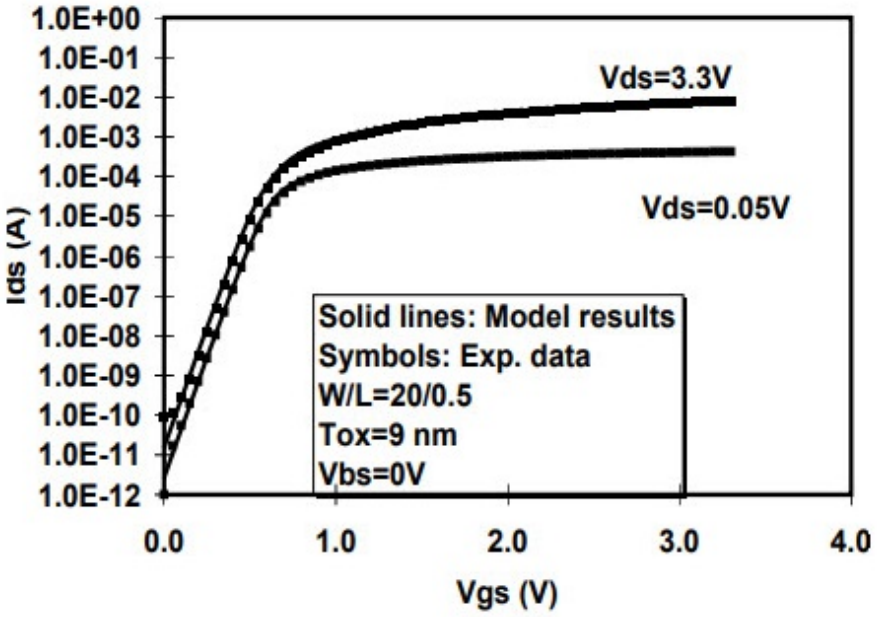

Figure 5.51: Leakage currents as function of drain-source voltage for short channel MOS transistors *[76]*

The PCBs and minimatrices with bond pads chips, shown in Figure 5.42 and Figure 5.43, are used for the investigation of cross talk. Three different scenarios are compared. In each of these scenarios, the input voltage of one matrix cell was swept from 0V to 1.9V, while the input values of all other matrix cells were set to the same constant value. For each of scenario, this constant value was set to 0V, 0.9V, and 1.8V. This allows for the comparison of

the input/output characteristic of the swept matrix cell, when all other cells are set to minimum heater power (V_{IN} = 0V), to maximum heater power (V_{IN} = 1.8V) and to an intermediate heater power (V_{IN} = 0.9V). Considering cross talk, the scenario with intermediate heater power, where the PWM frequency is quite high, should be the worst of the three scenarios. In Figure 5.52, standard deviation of mean heater power depending on the input voltage of one swept matrix cell is shown for all three scenarios with the statistics of 1000 refresh cycles. To conclude, there is no visible dependence of standard deviation on the heater setting of the remaining matrix cells.

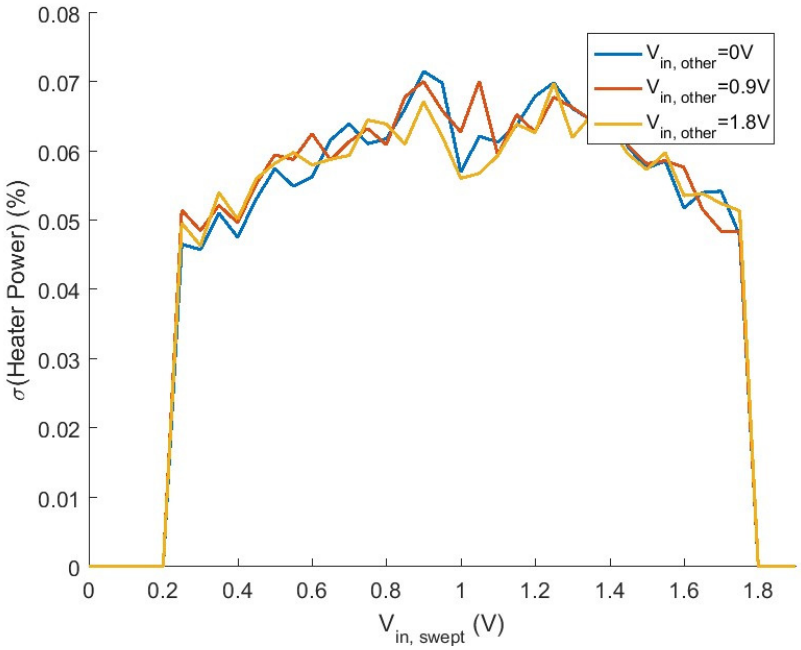

Figure 5.52: Standard deviation of the heater power of a selected matrix cell under conditions when the inputs of all the other cells are set to 0V (blue), 0.9 V(red), and 1.8V(orange), for N=1000 refresh cycles *[74]*

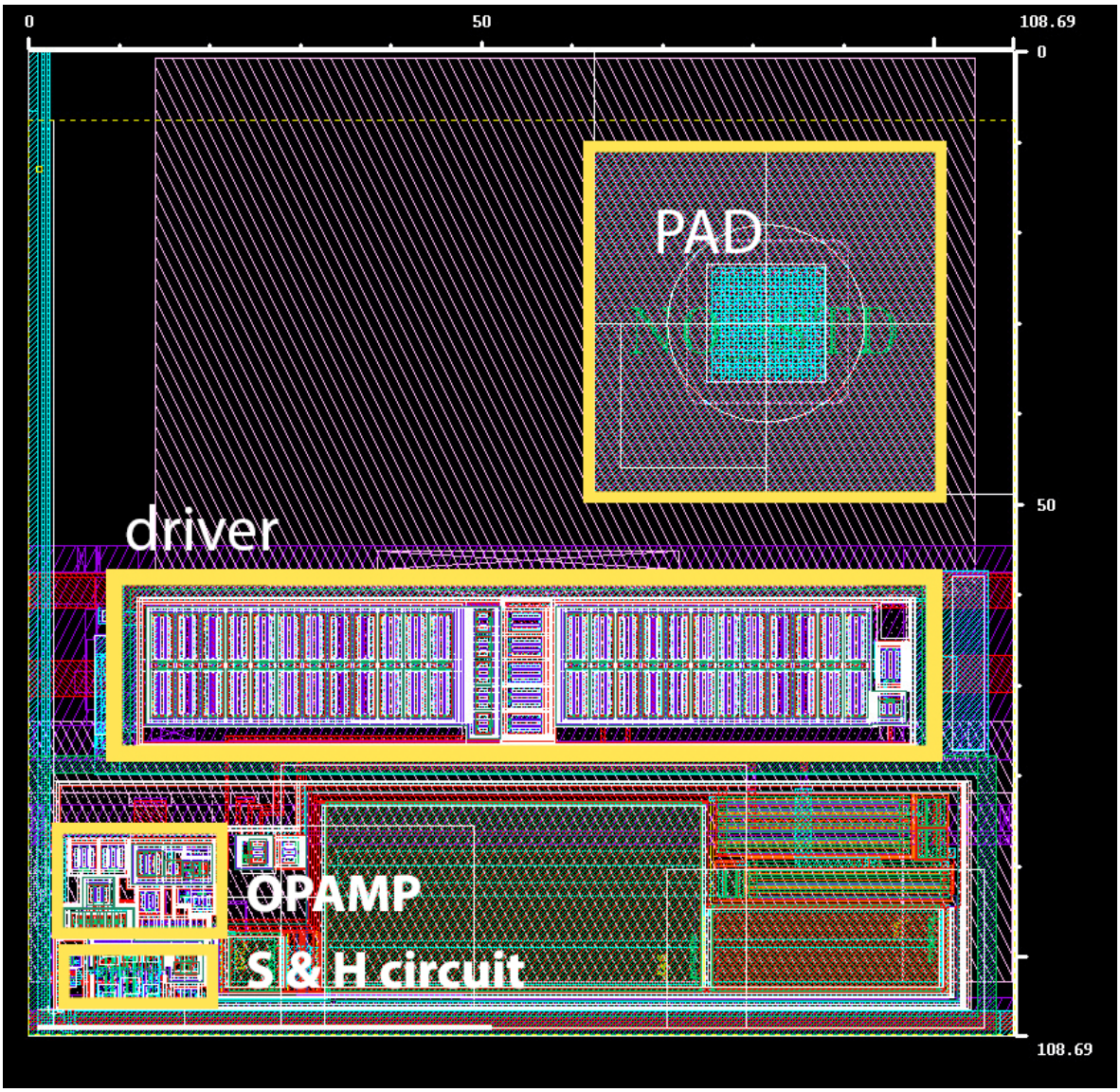

Figure 5.53: Layout of one cell for the new, improved, hybrid heater control approach with dimensions of 108.69 × 108.69 µm². The dimension has to be scaled by a factor of 0.92 to obtain the physical dimension after chip fabrication in BCD8sp; i. e. the physical dimension is 100×100 µm², which is equal to the 2-dimensional pitch of the PIC matrix.

The new hybrid approach has considerably improved in comparison to the old hybrid approach in all important parameters, such as the shape of the IO characteristics, sampling noise and leakage of the sample&hold. However, refreshing the S&H voltage is still necessary, which is the main weakness of this approach.

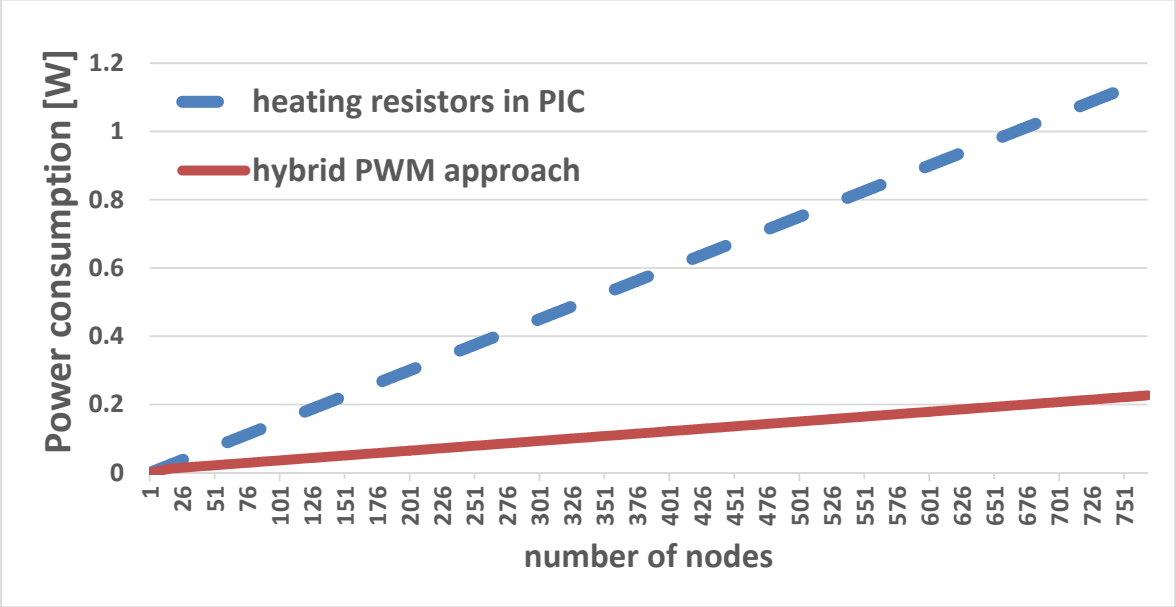

Figure 5.54: Power consumption of EIC and PIC in dependence on the number of photonic switches

Figure 5.54 shows the comparison of power consumptions of the EIC with the hybrid approach and the power consumption of heaters in the PIC. For this analysis, the typical scenario is used: only a few MRs are active and therefore in estimation of the total power consumption of a matrix with a large number of nodes, they can be neglected. All other MRs have to be tuned only slightly to compensate for process tolerances. The needed heating power is around 1.5 mW for each cell. For a matrix with 768 switch nodes, power dissipation in the electronics chip with the hybrid heater control approach is around 220 mW. Total heating power for all heating resistors in the PIC is 1.25W.

5.4 Analog-Digital Approach with Integrated 8bit DAC for Control PIC

The approach with the minimatrices is an area and a cost saving approach to testing additional heater control approaches together with the different photonically integrated ring modulator switches.

The improved hybrid heater control approach still requires a refresh due to the leakage current of the sample & hold circuit, although not as often as the first hybrid heater control approach. In order to avoid any need for refresh cycles of the data stored in the improved hybrid heater control cell, we further improved this approach by replacing the sample & hold circuit with a digital to analog converter (DAC). Figure 5.55 shows a circuit diagram of one cell with the improved hybrid heater control approach using the DAC.

The circuit of the DAC [77] is shown in Figure 5.56. An output buffer in the DAC is not necessary since the OPAMP used in the cell has a MOS input. The resistors in the MSB network have the value of 500 Ohm and the resistors in the LSB network have the value of

7.5 kΩ. The switches S_M and S_L are identical, consisted of transmission gate with PMOS transistor (W_{PMOS}=3.5 µm, L_{PMOS}=180 nm) and NMOS transistor (W_{NMOS}=1 µm, L_{NMOS}=300 nm).

A micrograph of the minimatrix EIC chip with an improved version of the analog-digital control with an integrated DAC is shown in Figure 5.63. For this minimatrix chip, the physical dimensions of this chip are increased from 0.8 × 3.7 mm^2 to 1.32 × 3.7 mm^2. This improvement allows us to change the pinout and to add more pads for the functional mode. In this way, redundant supply pads are added, and the positions of pads are changed to simplify bonding of the EPIC. Additionally, more area allowed us to improve the supply lines and the routing overall.

In the middle of the chip, 16 control cells are located and on the right side of the chip two test cells are located, as it is marked in Figure 5.63. One test cell includes an integrated heater resistor and the other one is just a DAC with the output connected to an output bond pad. A layout of a single cell of the new hybrid control cell with integrated 8bit DAC is shown in Figure 5.57. Since the physical dimensions of the horizontal pitch are fixed to 100 µm, the only way to fit the DAC into a cell was to extend the vertical dimensions of the cell. Total dimensions of the cell are 205.96 × 108.69 µm^2. On the bottom side there are 8 TIAs and an analog multiplexer. For this purpose, 8 input signals of 16 input signals of the analog multiplexer are used. On the bottom side, there are also PADs which are used for connecting the supply for the TIAs and selecting signals of the multiplexer, as well as the output signal from analog multiplexer. Supply pads and pads for controlling and testing the 16 cells are located on the top, left and right side of the chip.

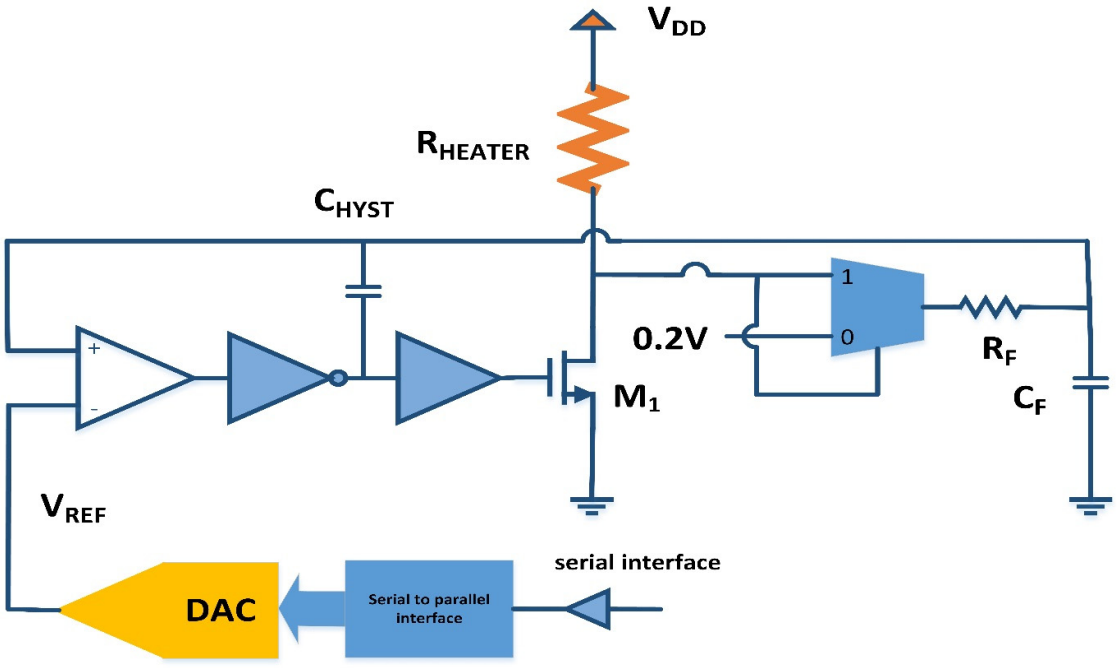

Figure 5.55: Circuit diagram of improved hybrid approach with DAC

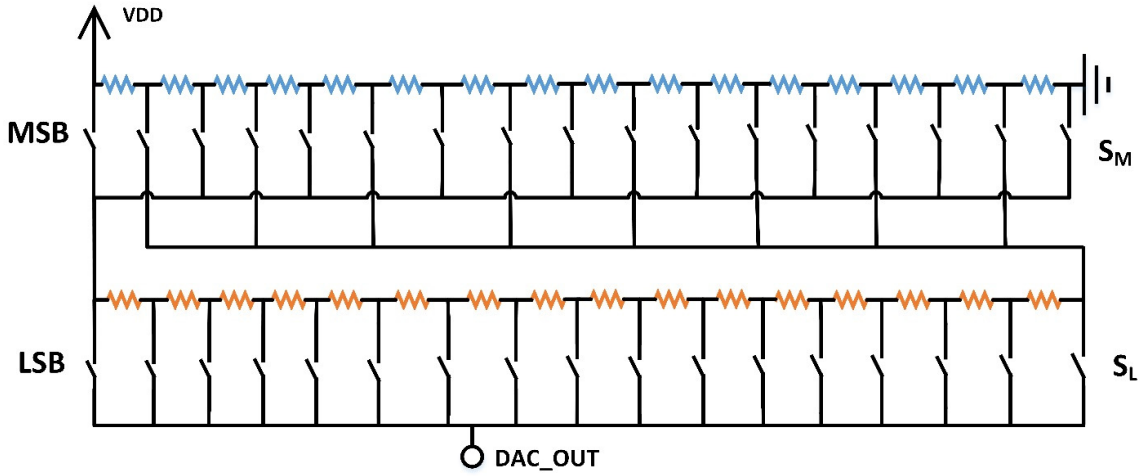

Figure 5.56: Circuit diagram of the DAC

Figure 5.58 shows the layout of an 8bit DAC which is a part of each control cell. The digital-analog converter is switch-based with a serial interface for writing the data for control of the switches. As it can be seen from Figure 5.55 and Figure 5.58, the DAC consists of a digital part and networks of switches and resistors. The digital part consists of a serial interface for storing the 8bit data in registers. This data is further used for controlling the state of each switch in the network of switches and resistors. The network of switches and resistors consists of two parts one - for selecting the upper 4 bits and the other one for selecting the lower 4 bits, as it is shown in Figure 5.58.

Using a parallel interface in the heater control cells instead of a serial interface would require only a register instead of serial interface and a register. Thereby the chip area of the DAC could be reduced by about 10%.

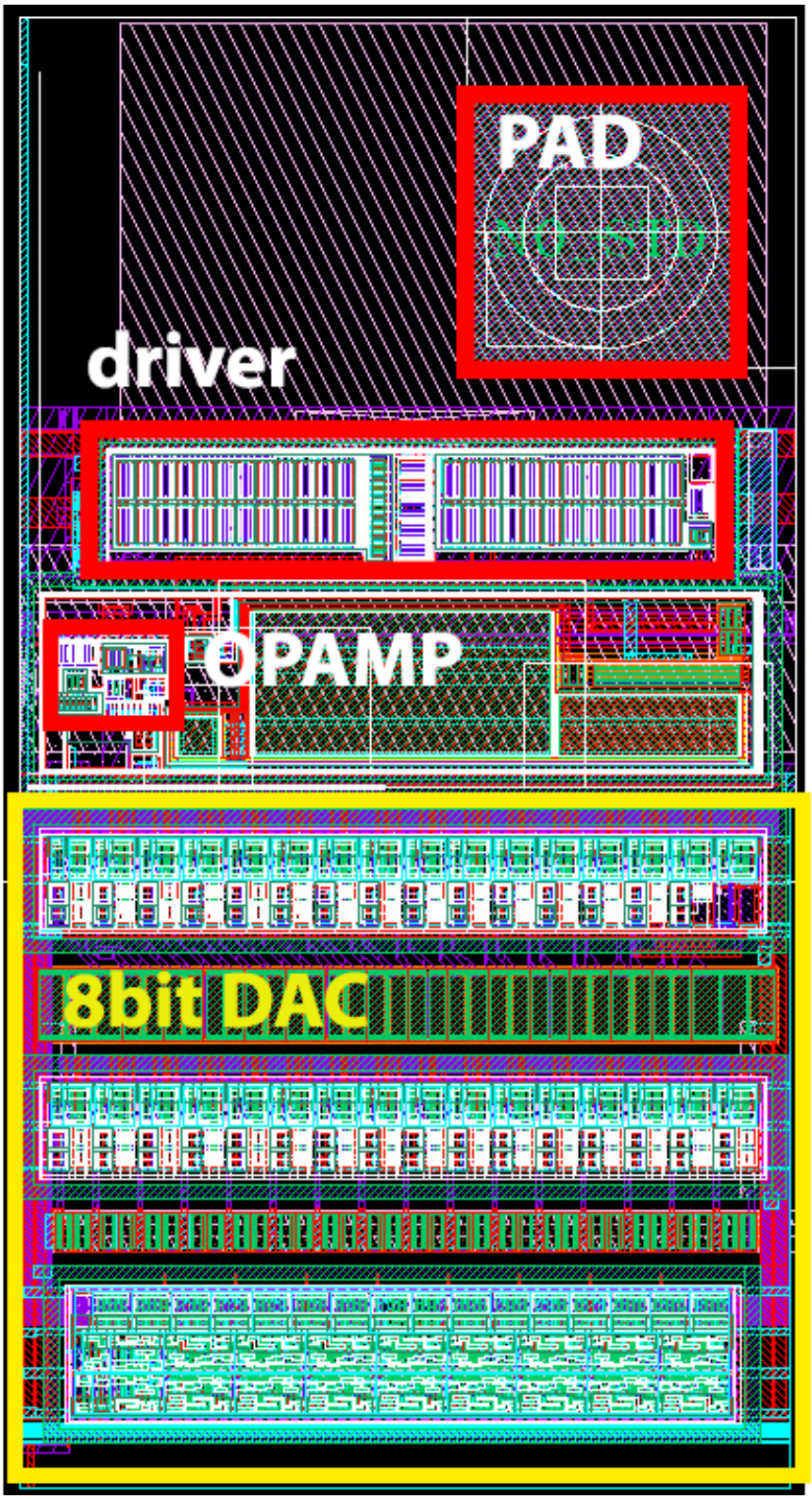

Figure 5.57: Layout of one cell for the new, improved, hybrid heater control approach with integrated DAC with dimensions of 205.96 × 108.69 μm^2. The dimension has to be scaled by a factor of 0.92 to obtain the physical dimension after chip fabrication in BCD8sp; i. e. the physical dimension is 189.48 × 100 μm^2.

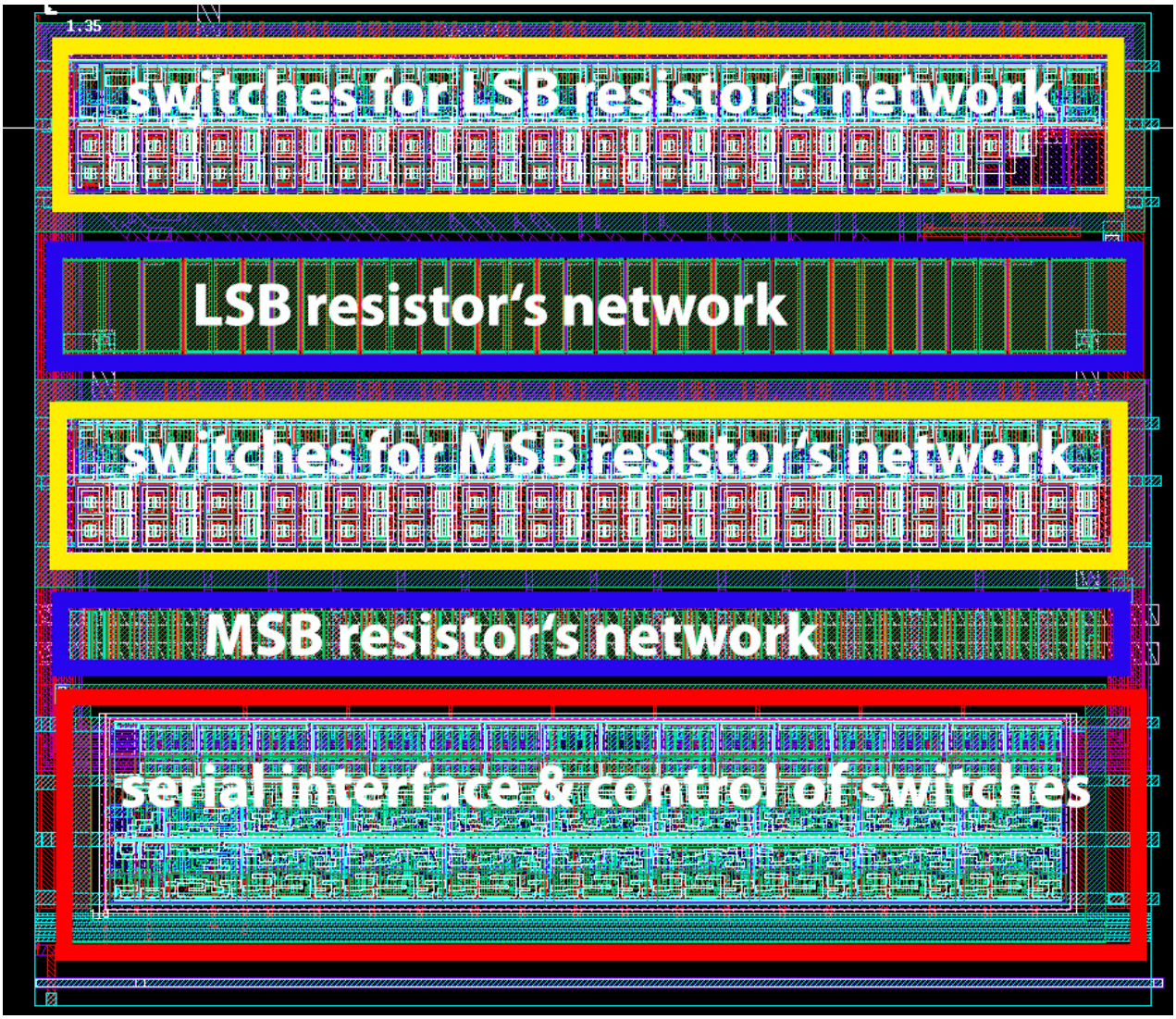

Figure 5.58: Layout of 8bit DAC used as integrated part of the improved hybrid approach cell with DAC

A DAC was designed for the test minimatrix since it was not possible to fit it in the predefined cell area of 108.69 × 108.69 μm^2 of the large-matrix EIC. However, using smaller structure-size technology than 0.16μm CMOS should make it possible to integrate the DAC with the circuits for the analog-digital approach.

5.4.1 Simulation Results

An 8bit DAC has a serial interface similar to SPI. A timing diagram for programming test cells is shown in Figure 5.59. The test cells are selected with the active addr_test_i input signal and the values of addr_sel_i<0:3> bus can be chosen arbitrarily. Both test cells are selected at the same time and the same 8bit digital value is stored in both registers of the test cell DACs.

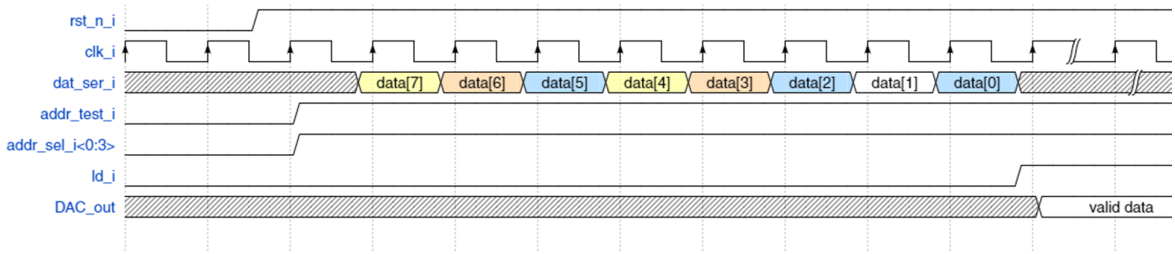

Figure 5.59: Timing diagram for programming minimatrix EIC with hybrid approach with integrated 8bit DAC

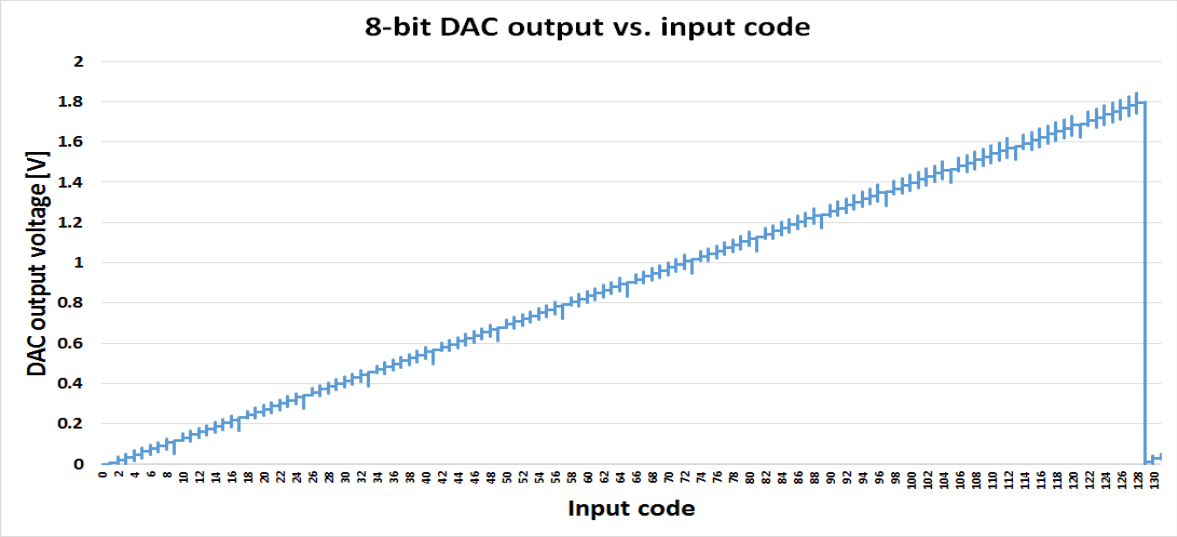

Figure 5.60: Simulation results of DAC output voltage vs. input code

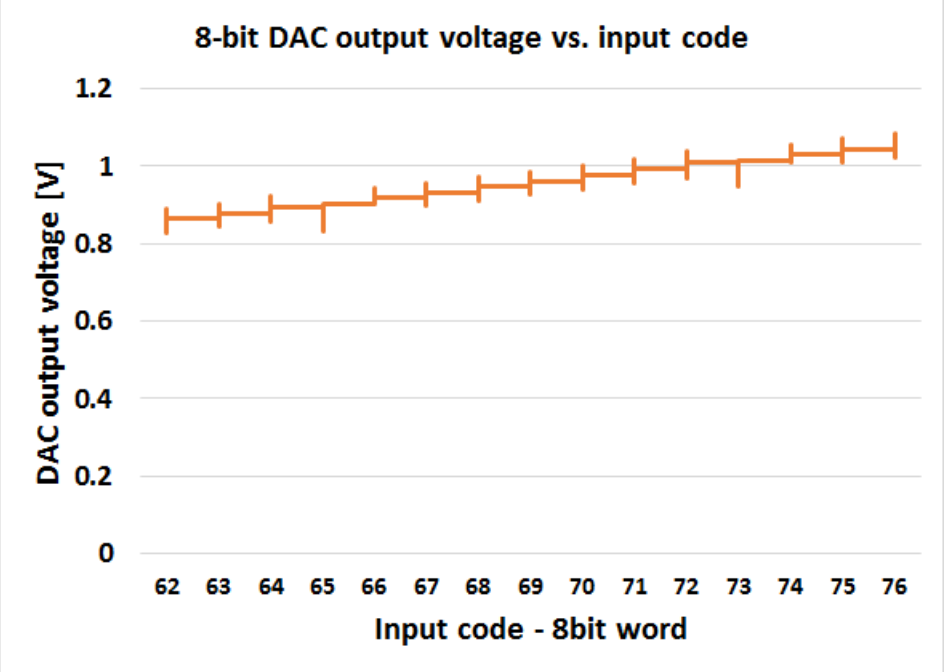

Figure 5.61: Zoomed in output characteristic of DAC output voltage

The result of post-layout simulation of the output voltage characteristic as a function of the 8bit digital input value is shown in Figure 5.60. The characteristic is monotonic. Zoomed in part of the output characteristic of the DAC is presented in Figure 5.61.

5.4.2 Characterization Results

In this section, characterization results of the improved hybrid approach with an integrated 8bit DAC are presented.

Figure 5.62 shows a photo of the test PCB with a wire-bonded EIC containing the new hybrid heater control approach with an integrated 8bit DAC. Figure 5.64 shows a zoomed version of this wire-bonded EIC with the new hybrid heater control approach with an integrated 8bit DAC.

3D integrated minimatrix EIC with the hybrid approach with integrated DACs with the minimatrix PIC is shown in Figure 5.65. Unfortunately, these combined chips were not photonically tested during the writing of this thesis, but they are planned to be tested anyway.

For the characterization of the new hybrid approach with integrated 8bit DAC, a PXI system from the National Instruments, as well as a fast real-time oscilloscope, were used. The PXI system was used to generate the digital control signals, acquire analog output signals of the EIC, and to provide and monitor the necessary supply voltages.

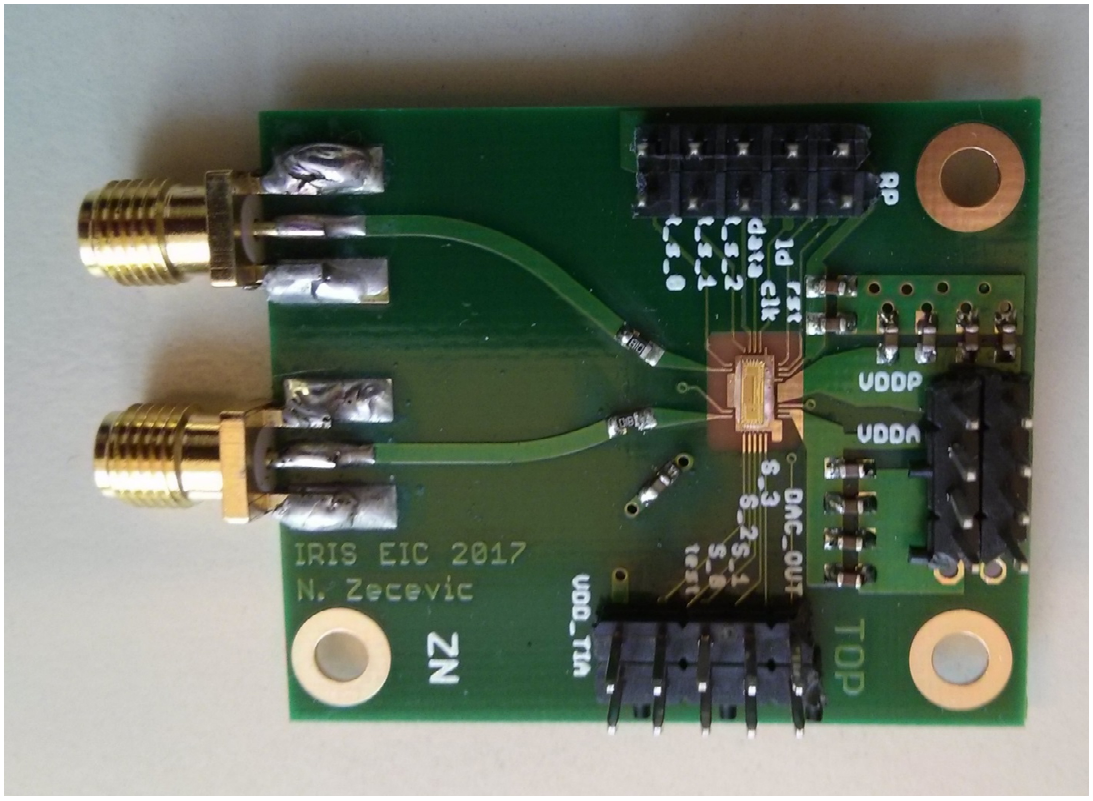

Figure 5.62: PCB with bonded minimatrix EIC with new hybrid approach with integrated 8bit DAC, additional components and connectors

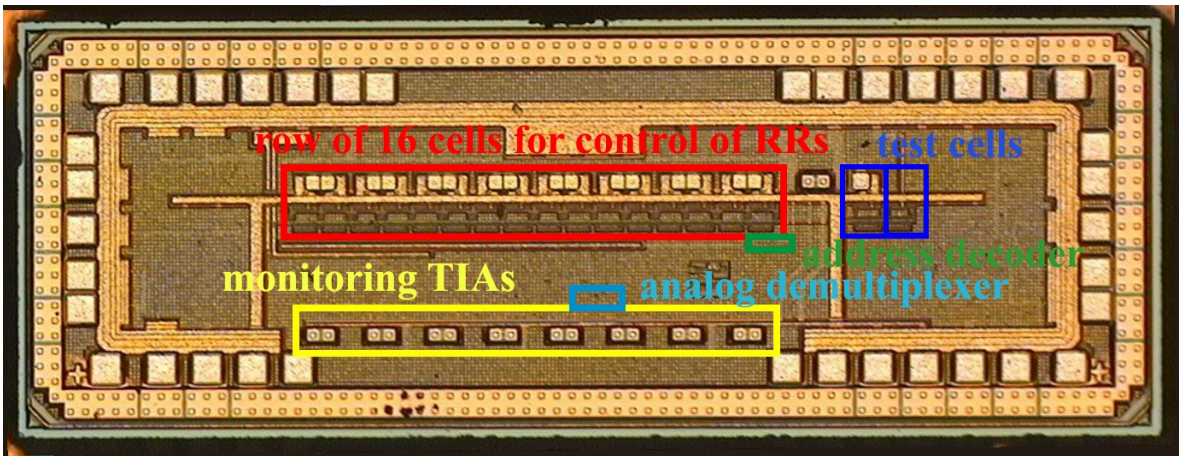

Figure 5.63: Marked micrograph of minimatrix EIC with improved hybrid approach with integrated DAC

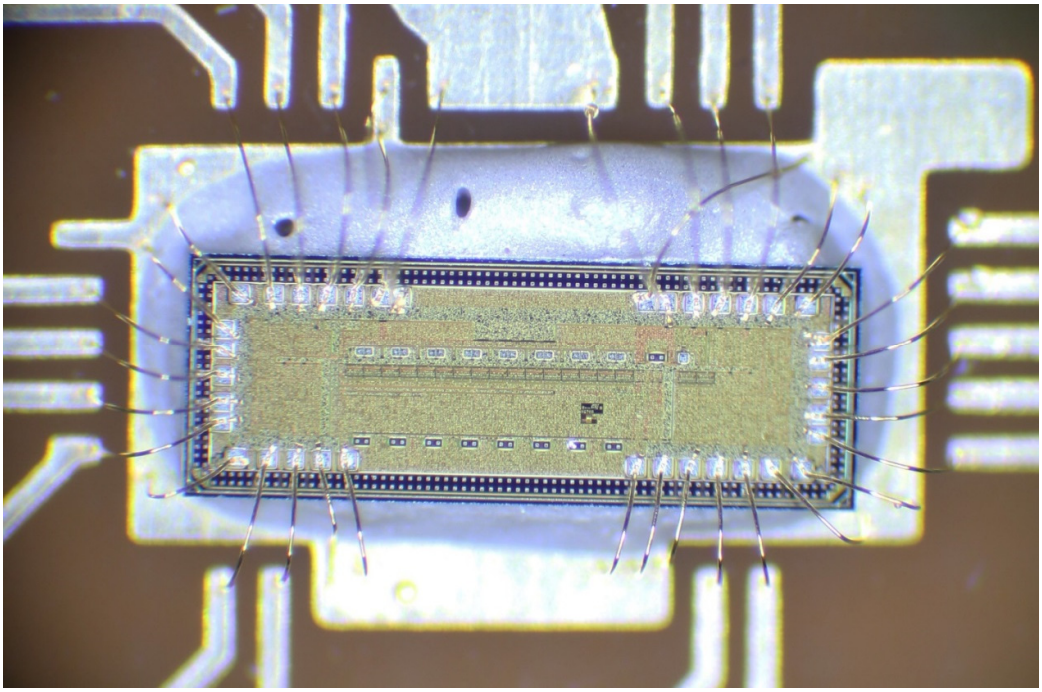

Figure 5.64: Bonded minimatrix EIC with hybrid approach with integrated 8bit DAC

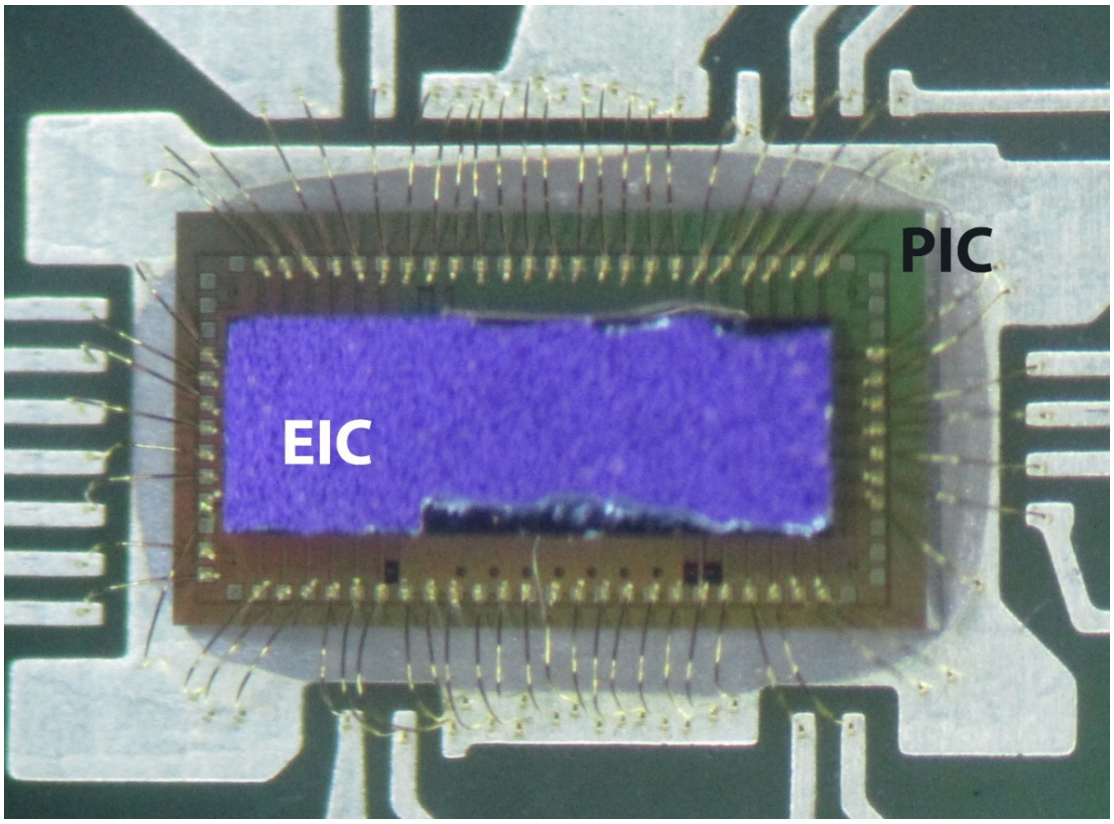

Figure 5.65: 3D integrated minimatrix EPIC chip with hybrid control approach with 8bit DAC

Three different samples were characterized. For the measurement results shown in Figure 5.66 and Figure 5.67, the value stored in the DAC's data register was swept from 0 to 255. For each data value 100 measurements of the output were taken. The left side of Figure 5.66 shows the mean value of the output voltage of the DAC versus the DAC byte stored in the DAC's register. The characteristic of all three samples is quite similar. There is a clearly visible offset of ~23mV. This offset does not cause any problems, since the PWM generator also has an offset with a different sign. The right side of Figure 5.66 shows standard deviation of the measured output voltage. It is influenced by noise in the EIC as well as by noise of the measurement setup. The measured standard deviation of the output voltage is far below 1/10 of the LSB (1 LSB ≈ 6.9mV) and therefore far below any critical limits.

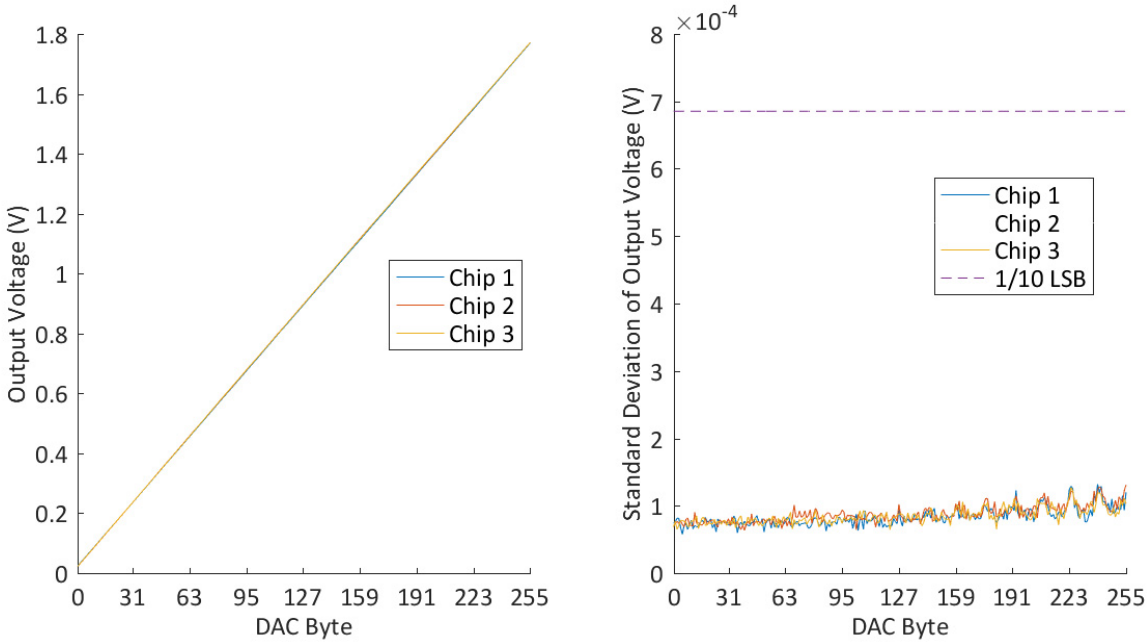

Figure 5.66: Mean output voltage (left) and standard deviation of the output voltage (right) depending on the DAC data byte (100 samples per voltage step)

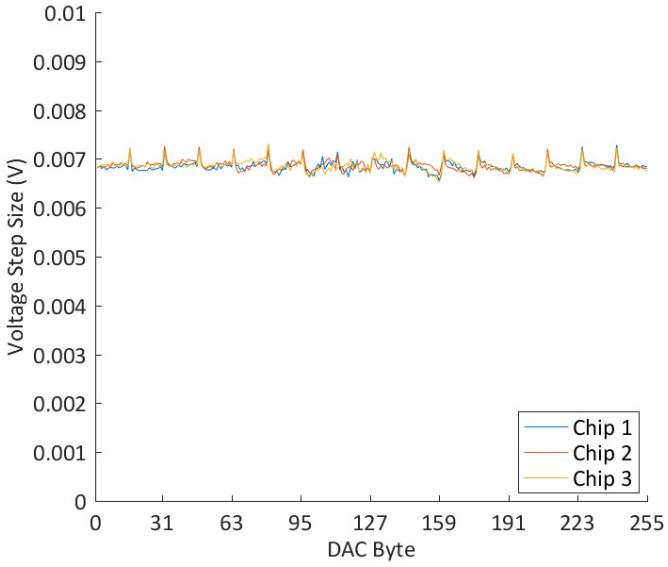

Figure 5.67: Mean output voltage step size depending on the DAC data byte (100 samples per voltage step)

Figure 5.67 shows the mean step size of the DAC versus the DAC byte. It is measured by subtracting the actual output voltage by the voltage measured for the DAC value before. This Figure proves that for the characterized chips there are no missing codes and no non-monotony errors. The differential non-linearity (DNL) is around 0.45mV, which is considerably below 1/10LSB. The integral non-linearity (INL) is between 1.7mV and 4mV, corresponding to the range of 0.25 LSB to 0.58 LSB. These characteristics are sufficiently accurate for heater control.

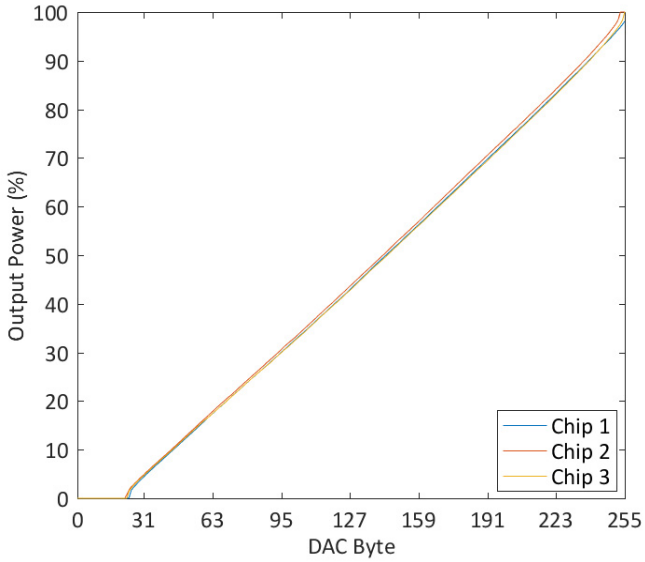

Figure 5.68: Output power of the PWM heater driver depending on the DAC data byte

Figure 5.68 shows mean heater power at the output of the PWM driver. The linearity is still good. The characteristics of the three tested chips are slightly different. This does not cause any problems, since heater power of different heaters needs to be calibrated anyway.

Figure 5.69 shows the PWM frequency for different ADC bytes. High PWM frequencies of around 70MHz are especially reached for medium heater powers. As mentioned in the previous Chapter 2 this is important to keep thermal ripples introduced by the PWM approach below critical limits. The reached PWM frequencies are more than high enough.

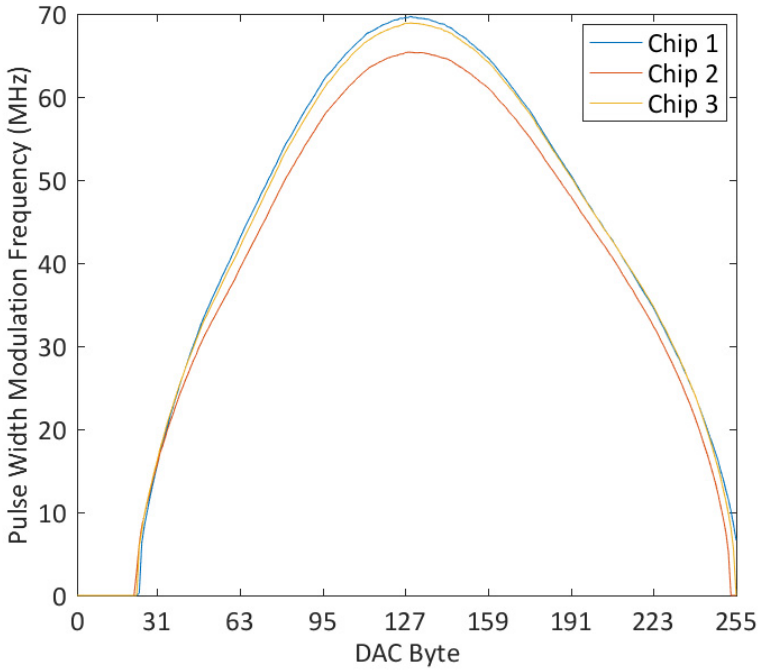

Figure 5.69: PWM frequency of the PWM heater driver depending on the DAC data byte

The most important improvement was the integration of a DAC replacing the sample&hold circuit in the mini-matrix hybrid approach. The version including the DAC reaches the same PWM performance as the previous version with the sample&hold circuit. But, contrary to the old approach, this new approach does not require any refresh cycles. These refresh cycles would have been a limiting factor for further scaling of the number of integrated heaters. The test of the new approach with the integrated DAC was successful. This new approach paves the way for even higher integration in future.

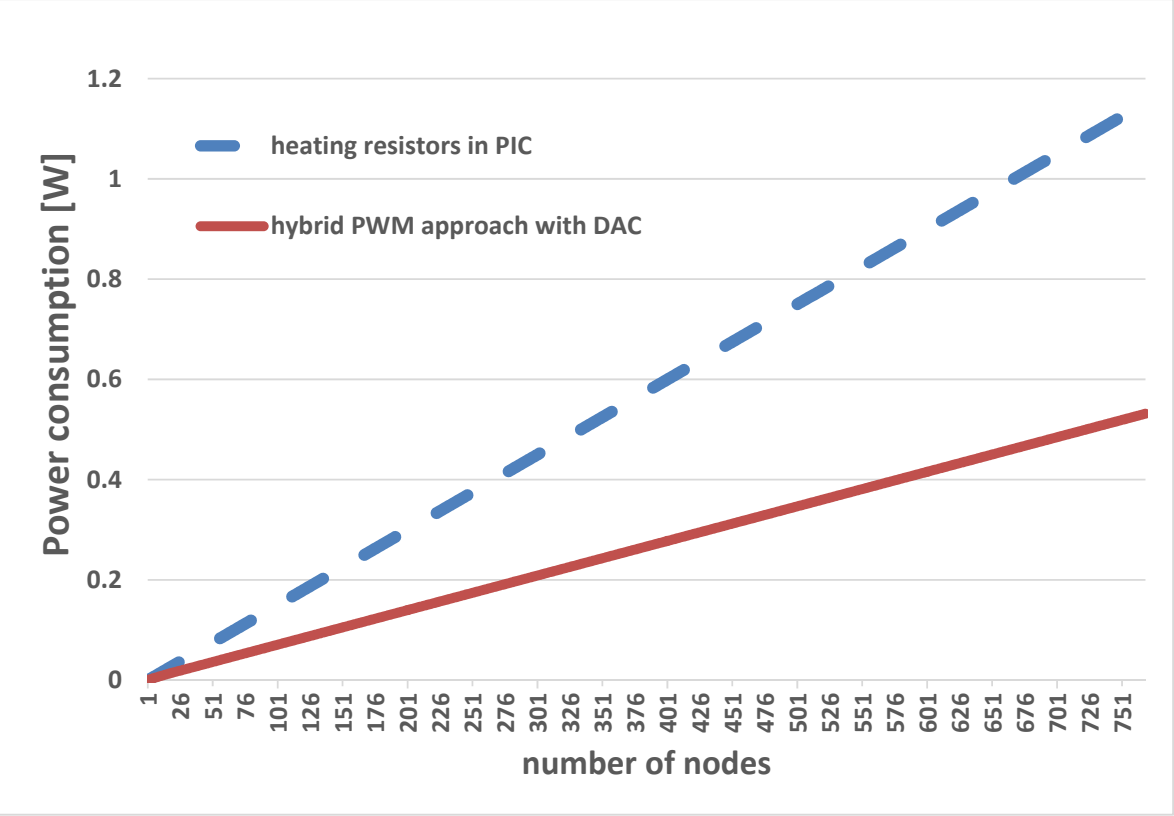

Figure 5.70: Comparison of power consumption of hybrid approach with 8bit DAC and power consumption in PIC as function of number of photonic switches

Power consumption of an 8-bit DAC is approximately 400 µW. Adding this value to the power consumption of the circuits of the improved hybrid approach, we get 685 µW in total for the power consumption of one cell for a tuning range of 1nm. As for the matrix of 768 cells, the comparison of power consumption of the heaters in the PIC with the power consumption of the EIC is shown in Figure 5.70.

5.5 Full Matrix Architecture and Measurement Results

A complete large-matrix multi-node electronics chip, fabricated in the second tapeout run is shown in Figure 5.71. It includes 824 nodes of independent heater control circuits with improved hybrid approach. The dimensions of EIC chips are 5.7 × 3.7 mm^2.

In Figure 5.72**,** the regions with the pads used in functional mode and testing mode are marked in red and blue, respectively. In the middle of the chip area, the matrix of 16 x 48 cells for the control of the ring resonator heaters is located. A block with a heater control cell for driving AWG heaters and Inteleaver heaters are also marked in Figure 5.72. The complete large-matrix EIC uses the new improved hybrid heater control approach with reduced refresh frequency described in Subchapter 5.3.1. Characterization results of the new hybrid approach (with sample & hold circuits) have already been reported in Chapter 5.3. Furthermore, leakage currents of the sample & hold circuit now lead to discharging the hold capacitor and zero heater power in case the refresh algorithm or the overall control algorithm should fail intermediately. A layout of a single cell of the new hybrid control cell with marked circuits is shown in Figure 5.53. To enable the testing of the new hybrid cell circuit before connecting the EIC and the PIC, test cells with a heater resistor integrated in the circuit cell were included (see green rectangles in Figure 5.72). The counters for addressing the cells are marked with yellow-colored rectangles (Figure 5.72). The matrix is divided into four independent blocks, each having a dedicated interface for addressing and storing analog values into the S&H circuit of the heater control cell.

On the right side, prior to the Interleavers and the signal enters the matrix, and on the bottom side of the matrix, at the outputs of the matrix, transimpedance amplifiers are placed. There are 6 analog multiplexers used to multiplex the outputs of 84 photodiodes to 6 output PADs. A circuit diagram of a single analog multiplexer with 16 analog input signals and one output signal is shown in Chapter 5.6.

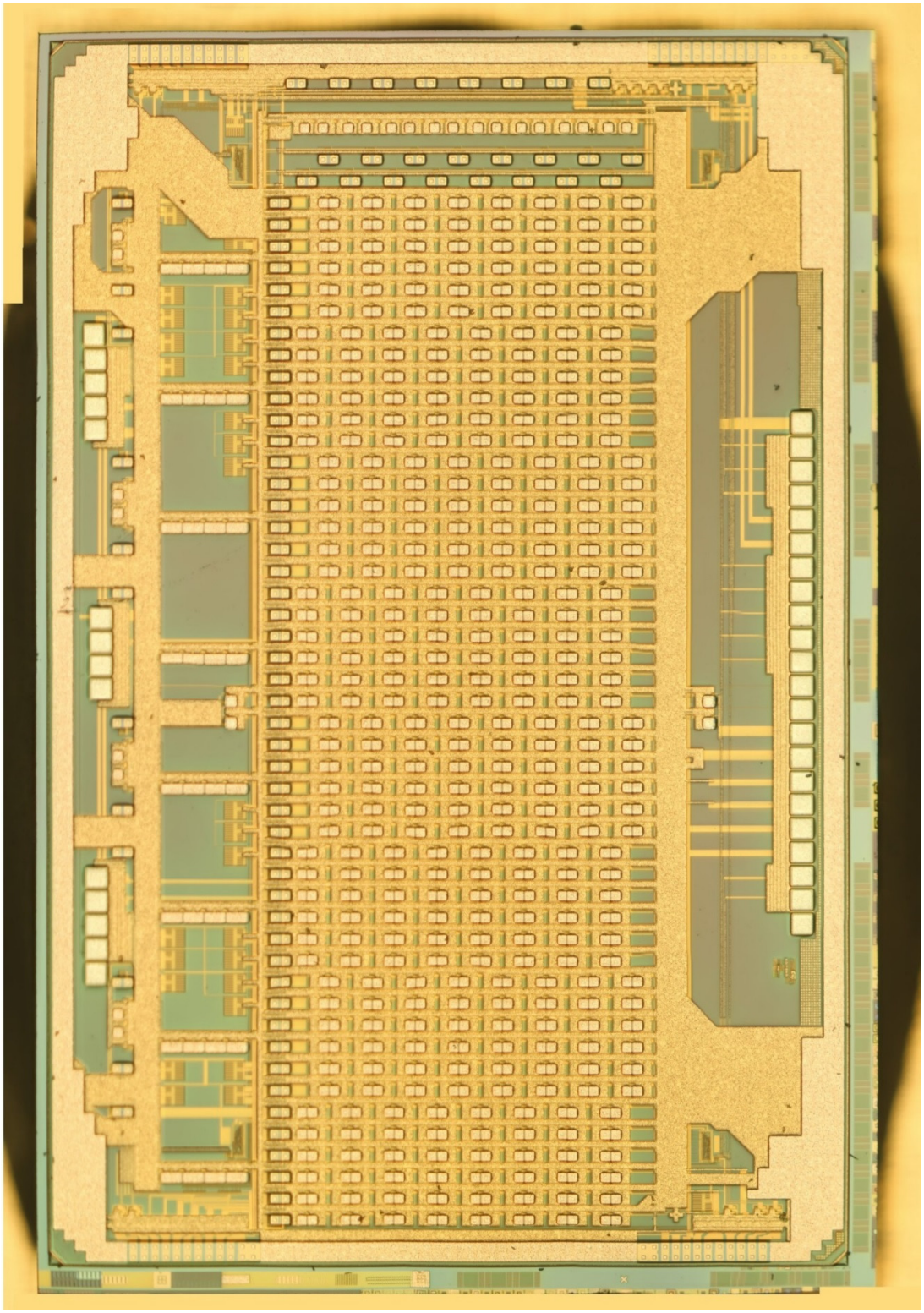

Figure 5.71: Micrograph of full matrix EIC chip with hybrid control approach

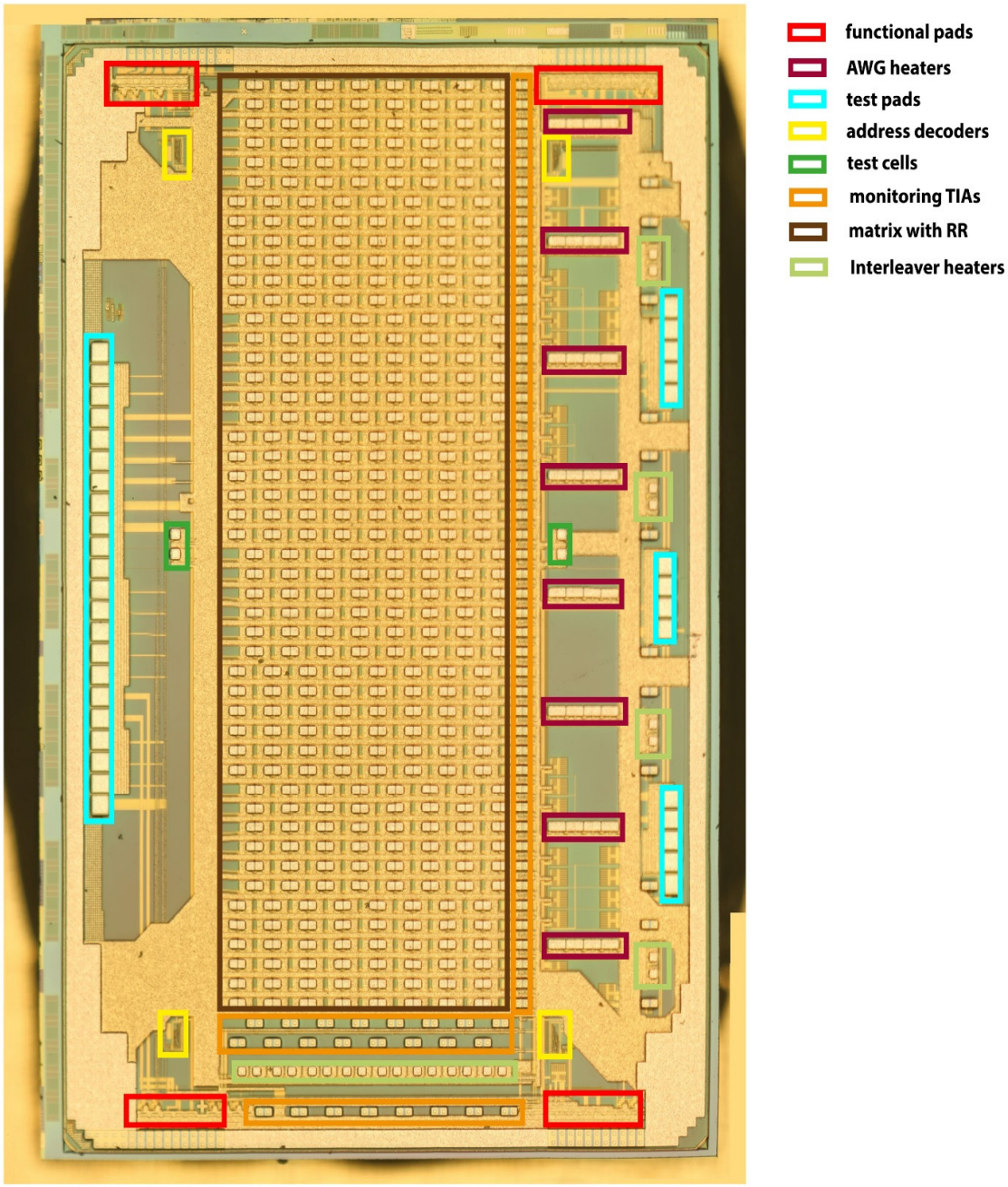

Figure 5.72: Micrograph of full matrix EIC chip with marked blocks

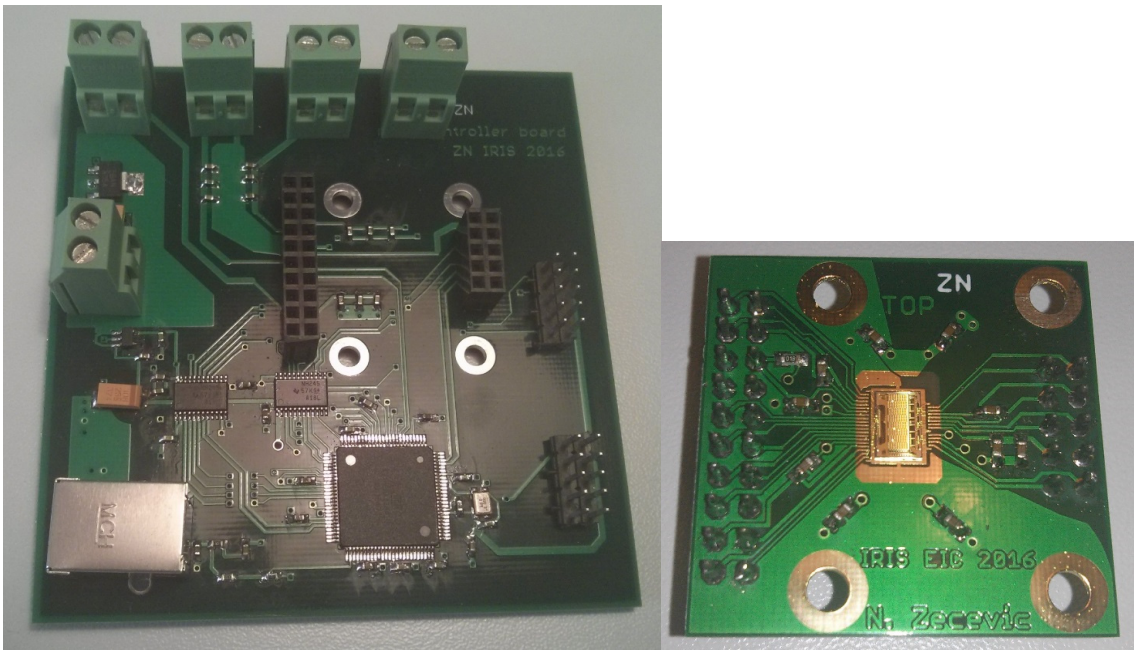

Figure 5.73: a) PCB with microcontroller, USB and serial interfaces and supply connectors b) PCB with bonded full matrix EIC with hybrid approach and decoupling capacitors and pinheader connectors

Two PCBs were designed for testing full matrix EICs. For testing and characterization of these chips with a microcontroller the modular approach was chosen. On the PCB shown in Figure 5.73a, a microcontroller with additional components such as USB, PDI and serial interfaces and supply connectors is mounted. On the other one, a smaller, top PCB full matrix EIC is bonded and decoupling capacitors are mounted (Figure 5.73b). These two PCBs are later combined with pin header connectors, as shown in Figure 5.74. In this way, we avoid the soldering of a microcontroller and additional components on each PCB with a full matrix EIC (which saves us time and reduces the costs).

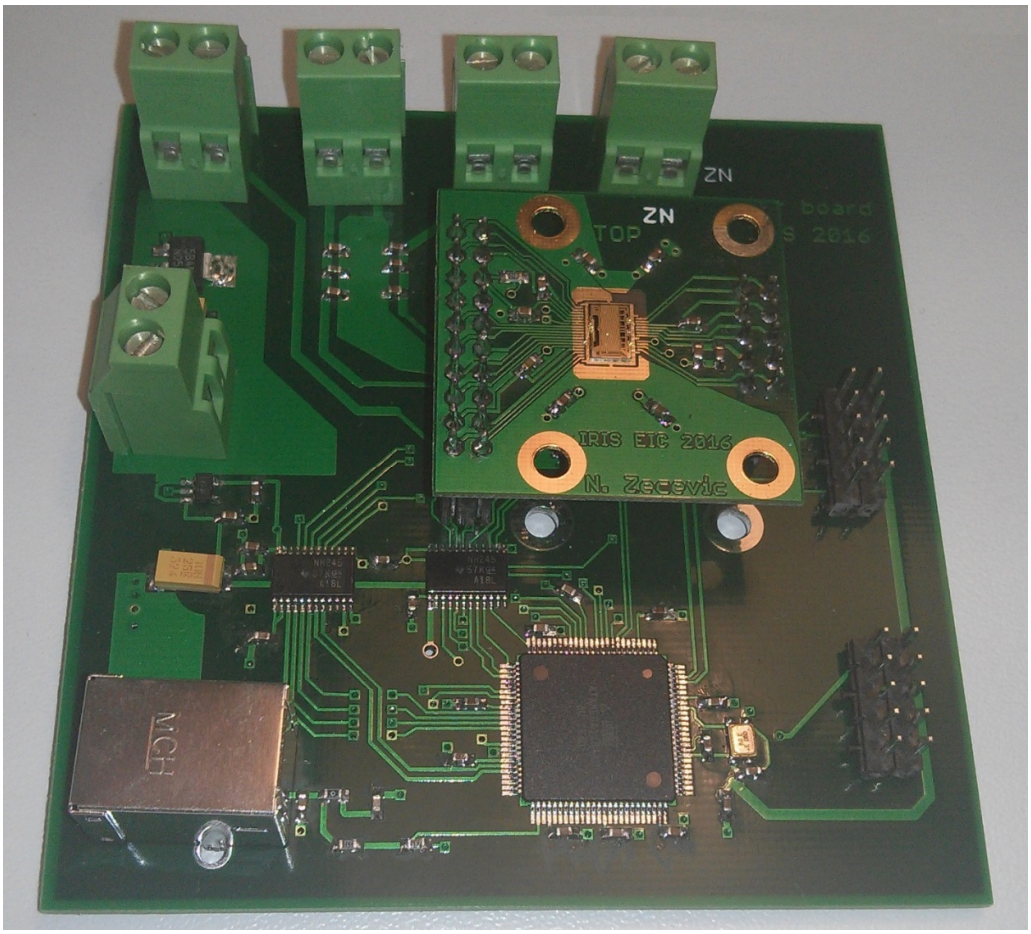

Figure 5.74: System of PCBs for easier testing of full matrix EIC with hybrid approach

5.6 Monitoring TIAs and Analog Multiplexers

A circuit of a transimpedance amplifier for processing photocurrents of the Ge monitor photodiodes is presented in Figure 5.75. The required resolution of the input power of a TIA is less than 0.1dB, which corresponds to the resolution of 11 bits for an ADC connected to the output of a TIA. Since the number of monitoring TIAs in the EIC chip is large (84), analog multiplexers are used to multiplex the outputs of TIAs, i.e. to reduce the number of output pads. Output voltages of the TIAs are then further processed within a closed loop in the microcontroller. Offset can be compensated for by using a look-up table in the microcontroller.

The bandwidth of the TIA is 25 MHz, as shown in Figure 5.76.

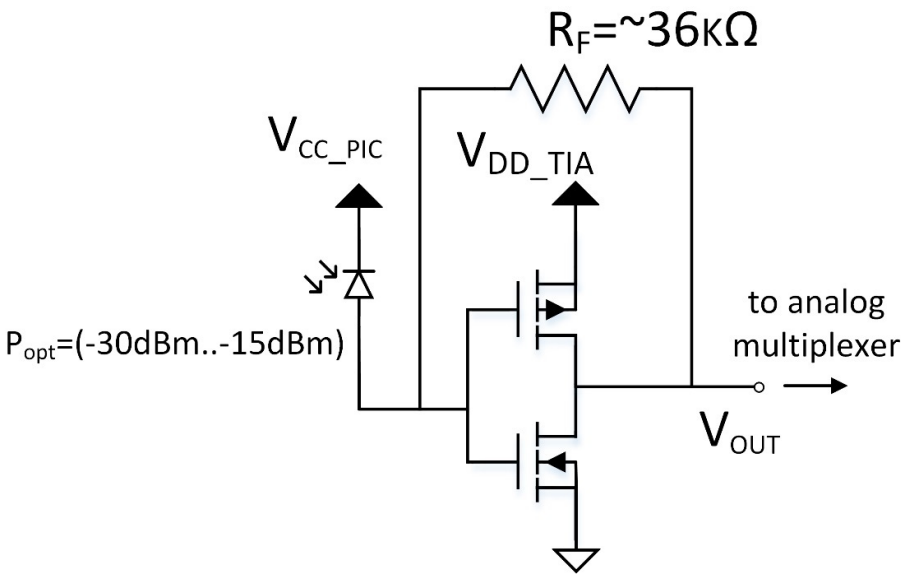

Figure 5.75: Schematic of TIA for monitor photodiodes

Since the measurement results of the photodiodes in the PIC showed that the response of the photodiodes is 0.6 A/W instead of the expected 1 A/W, a redesign of the monitoring TIAs inside the EIC was necessary. The value of the feedback resistor is increased by a factor of 1/0.6 (1.66), so the new value is 36.75 kΩ. According to this increase of the feedback resistor value, the bandwidth of the monitor TIA is slightly reduced. However, its bandwidth will still be orders of magnitude larger than the specified value of 1 kHz.

The measured DC transfer characteristics of the monitor TIAs designed for the photodiodes with the responsivities of 1 A/W and 0.6 A/W are depicted in Figure 5.77 and Figure 5.78. The specified dynamic range from -30dBm to -15dBm is marked in red. In this power range, the characteristic is quite linear. For the specified 0.1dB resolution at -30dBm, an 11bit ADC with a 0.9V full scale range is necessary. If an ADC with higher resolution is used, an even lower limit than -30dBm for the dynamic range of the monitor TIA will be possible (e.g. -35dBm). The current consumption of the TIA is 10 µA at 1.8V.

The simulated DC transfer characteristics of the monitor TIAs designed for two different photodiodes with the responsivities of 0.6 A/W and 1 A/W are depicted in Figure 5.79.

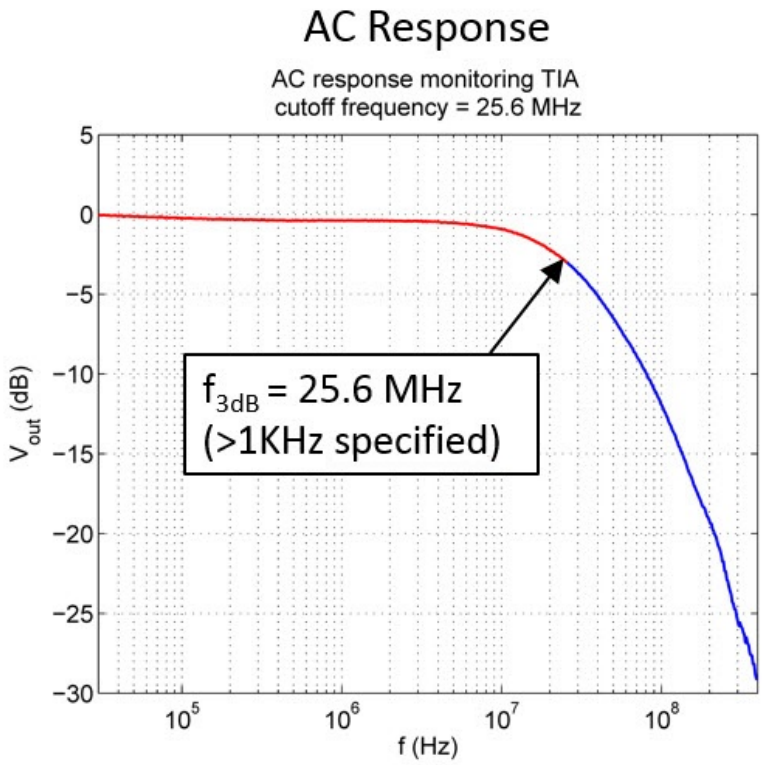

Figure 5.76: Frequency response of the monitor transimpedance amplifier

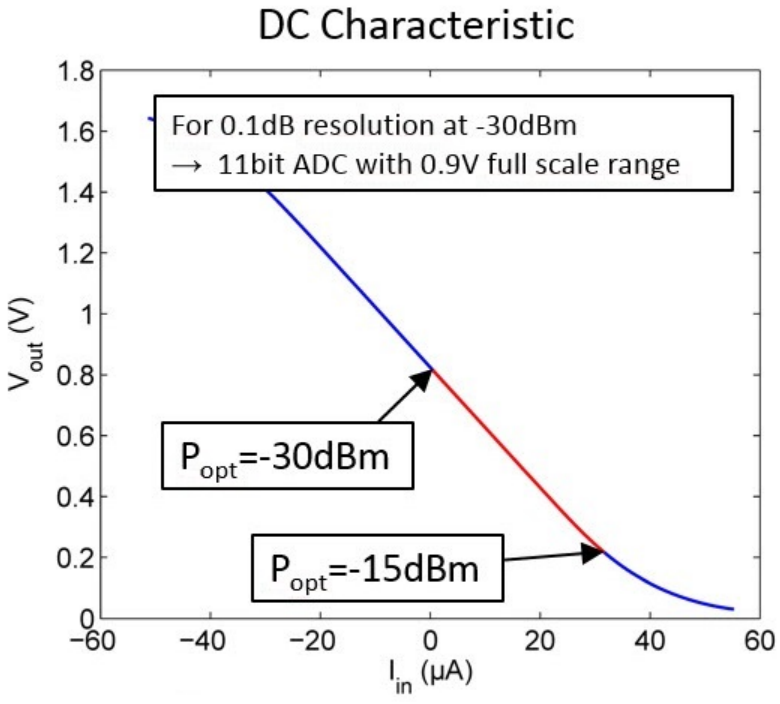

Figure 5.77: DC transfer characteristics of the monitor transimpedance amplifier designed for the photodiode with responsivity of 0.6 A/W

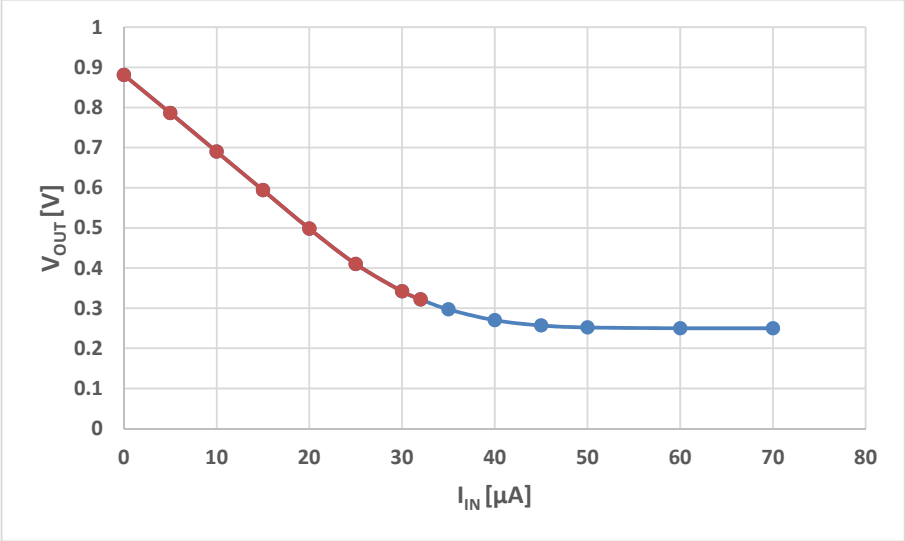

Figure 5.78: Measure DC transfer characteristics of the monitor transimpedance amplifier designed for the photodiode with responsivity of 0.6 A/W

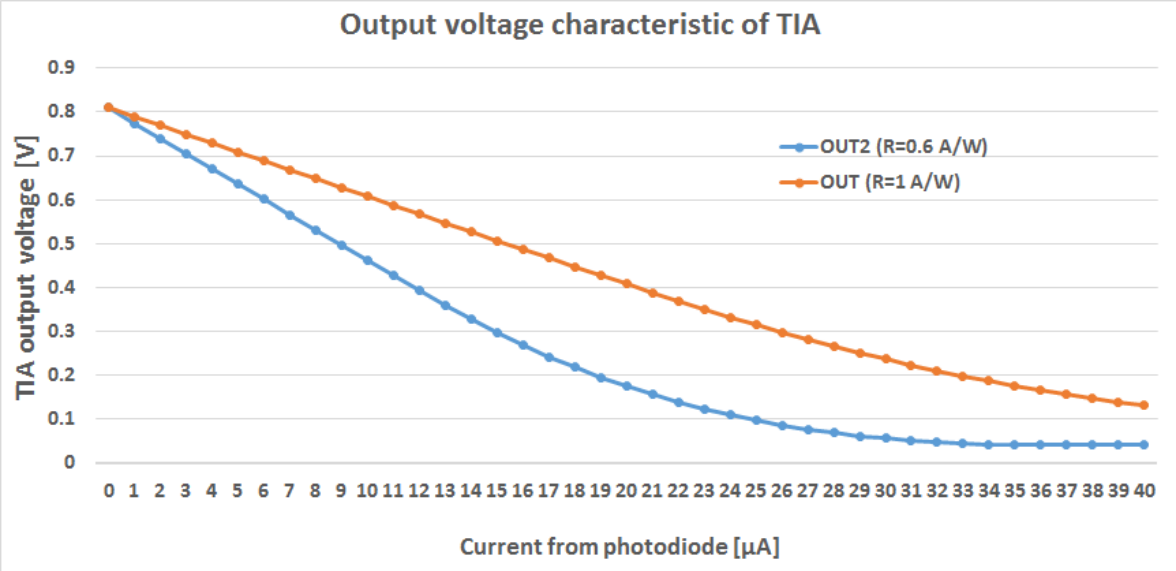

Figure 5.79: Output voltage characteristic of TIAs designed for photodiodes with two responsivities, R=0.6 A/W and R=1 A/W

In the big matrix chip, all TIAs are grouped in groups of 16 TIAs. The outputs of the TIAs are connected to the 16 inputs of the analog multiplexers. With 4 digital control signals, one of these 16 input signals is selected to be present at the output of the analog multiplexer for a certain time period.

A circuit of the analog multiplexer with 16 analog input signals, 4 select signals and one output is shown in Figure 5.80. The switches are designed from transmission gates. It was not necessary to insert the output buffer.

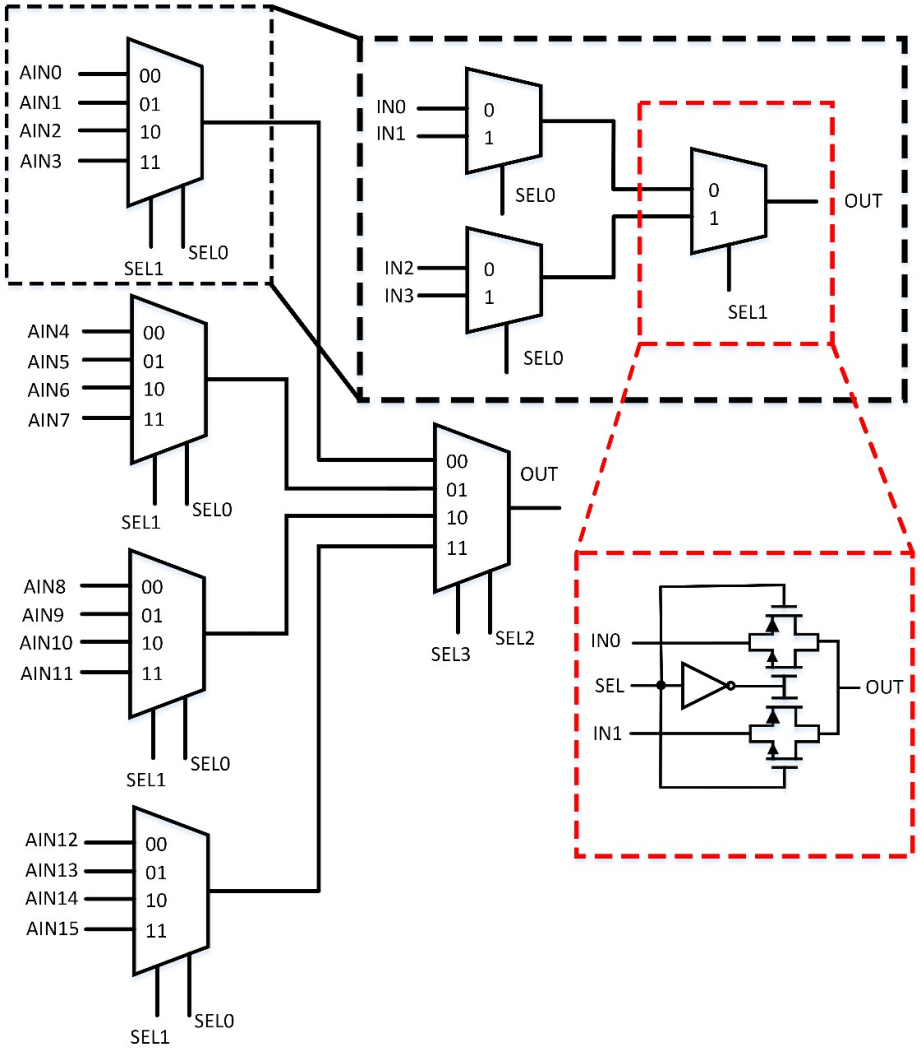

Figure 5.80: Schematic diagram of analog multiplexer with 16 input analog signals, 4 selection signals and one output signal

6 Conclusion and Future Work

6.1 Conclusion

This dissertation explored the possibilities of designing energy-efficient control circuits for driving photonic devices. Heat dissipation from the electronic control IC should be minimized. The first and most important reason is to reduce the overall power consumption of the device, and second to reduce the risk of heat transfer from EIC to PIC, which could lead to a detuning of photonic devices inside the PIC. These are the main points for designing power efficient approaches to control the heaters in the photonic IC.

Temperature of the PIC needs to be kept constant since the micro-ring resonator switches are tuned by temperature varying. The PIC requires operating temperature independent of the environment. Temperature of the PIC is regulated by cooling with an external thermo-electric cooler (TEC). Additional temperature diodes on the PIC are used to measure the actual temperature of the PIC and close the control loop by driving the TEC. However, designing a proper package solution with a heatsink was a challenging task. These were the main challenges of this research which are successfully fulfilled.

6.2 Comparison of Approaches

Two basic approaches for driving the heaters in photonic components were investigated: the constant voltage approach and the pulse width modulation approach. The constant voltage approach caused large power dissipation in the EIC which had an impact on heating of the PIC, with the risk of detuning photonic elements. Another challenge was the removal of dissipated heat from the package.

In the digital and hybrid approaches, the PWM frequency must be high enough to keep temperature ripple below critical limits. For the chosen technology, it is still possible to reach the necessary clock frequency, but it is close to the technology limit.

In Table 6-I, there is a list of pros and cons of each of the approaches to control heaters of photonic components in the PIC. The best characteristics were noted in the hybrid approach with an integrated 8bit DAC inside of each control cell. However, using more advanced technology advantages of the digital approach are gaining importance.

Table 6-I Comparison of control approaches

	Advantages	Disadvantages

Analog	No thermal ripple	• Power consumption/heating of EIC is much larger contrary to the digital approach (PWM):
		  ○ Increased total power dissipation
		  ○ Thermal crosstalk may detune microrings
		• External DAC required
		• Periodic refresh of S&H circuits necessary (<250 µs)
		• Sampling noise & EMI

Digital – PWM	Reduced power consumption, i.e. low heating of the EPIC	• **Thermal ripple** caused by the PWM in heating resistors can lead to a periodic partial **detuning** of the micro-rings • Requirements for counter clock freq. are at **technology limit**
Hybrid	• Reduced power consumption -> lowest heating of the EPIC • **Increased f_{PWM}** for medium heating power	• Thermal ripple caused by the PWM in heating resistors can lead to a periodic partial detuning of the micro-rings • External DAC required • Periodic refresh of S&H circuits necessary (<1.5 ms) • Sampling noise & EMI
Hybrid with an integrated 8bit DAC	• Reduced power consumption -> low heating of the EPIC, increased f_{PWM} for medium heating power • Integrated DAC -> digital interface between the EIC and µC, no sampling noise & EMI issues	• Thermal ripple caused by the PWM in heating resistors can lead to a periodic partial detuning of the micro-rings • Smaller technology is necessary to fit circuits into cell dimensions

Table 6-II Power consumption of circuit blocks used in EIC with improved hybrid approach and PIC

	EIC					
	Nr. of cells	I(A)	V(V)		P/cell (W)	P(W)
TIA	84	1.00E-5	1.8		1.80E-05	1.51E-03
Heater cell	824	1.26E-4			2.27E-04	1.87E-01
Address decoder	4	7.78E-6			1.40E-05	5.60E-05
					Total EIC	**1.88E-01**
	PIC (worst case)					
	Nr. of heaters	R(Ω)	V(V)	P(%)	P/cell (W)	P(W)
RR*OFF but tuned	48	108	1.8	20	6.00E-03	2.88E-01
RR* totally OFF	704	108		0	0	0
RR* ON	16	108		75	2.25E-02	3.60E-01
Interleavers	24	46		100	7.04E-02	1.69E+00
AWGs	32	38.2		50	4.24E-02	1.36E+00
*RR – Ring resonator					**Total PIC**	**3.70E+00**
R – heater resistance						

The power consumption of each circuit block in the EIC with improved hybrid approach and PIC is listed in Table 6-II. Estimated total power consumption in the worst case is ~4W, which is less than the first estimated value of total power consumption, as it is mentioned in Table 1-I.

In the constant voltage approach, power consumption per matrix cell circuit controlling the switched on ring-resonator is approximately 7.2 mW, assuming a heating resistor of 110 Ω and a supply voltage of 1.8 V. Heating power for compensating production tolerances of one cell is approximately 1.5 mW. For a supply voltage of 1.8 V and a voltage of 0.6 V across the heating resistor this would lead to a voltage of 1.2 V across the driving transistor. In this case, power dissipation of the driving transistor would be two times the power dissipation of the heating resistor itself. This power dissipation gets even worse if the voltage across the heating resistor is further decreased, which is the case when less heat for the compensation of production tolerances of the ring resonators is needed.

The PWM approaches have considerably lower power consumption than the constant voltage approach, as it can be seen from the Figure 6.1. In the data centers involved, the switch matrices will have several hundreds of nodes or even several thousand nodes. The presented PWM approaches could be easily extended to control matrices with that many elements. For the matrix with 768 nodes, power consumption of the digital PWM approach (including the counter and the necessary bus drivers) is reduced to 7.5% of that of the constant voltage approach. For the matrix of the same size, power consumption of the hybrid approach without an integrated 8bit DAC and with it is reduced to 5.6% and 13.3% of power of the constant voltage approach, respectively. At VDD=1.8V, room temperature and maximum PWM switching frequency, power consumption of the comparator used in the hybrid approach without the DAC is ~77μW, while the driver for the MOSFET M1, shown in Figure 5.38, consumes ~131μW. Power dissipation on driver MOSFET M1 is ~75μW. This results in total

power consumption of ~284µW per heater driver. In comparison to the heater driver circuit used in [38] and [12], based on a DAC with a current output, the heater driver presented within this work has almost 90% less power consumption. Maximum heater power of 12.25 mW used in [38] is smaller compared to the ~29mW of the heater resistor presented in this work. Reducing the power consumption of the control circuit by the PWM approaches is therefore a crucial step towards large integrated optical switch matrices.

It is obvious that the analog approach (const. voltage approach) shows quite large power consumption, which could be very difficult to handle from the package.

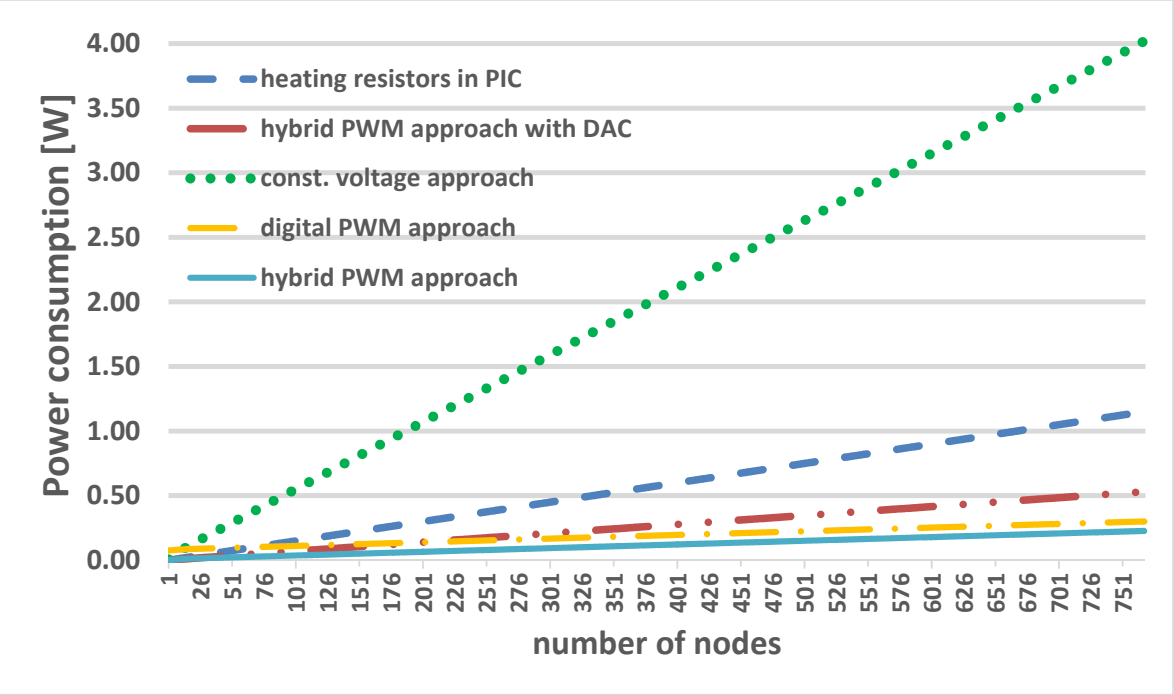

Figure 6.1: Comparison of power consumption of analog, digital, hybrid approaches with and without DAC and PIC in dependence of number of heater cells

6.3 Future Work

6.3.1 Improvements in Photonics

Advancements in the realization of scalable, highly integrated optical switching matrices in silicon photonics technology are encouraging for commercial production and usage of optical switching in data centers. High port count, low power consumption, high speed, low footprint size, low cost, wide bandwidth are all characteristics of these optical switch matrices which should be met.

However, there are still some technical challenges which have to be met in order to envisage commercial realization of such devices (optical matrices) in the near future.

The losses in the switch matrix can be significantly reduced with a better waveguide crossing fabrication and an improved grating coupler design. The best possible insertion loss of a single polarization grating coupler today is <1dB, shown by Luxtera at ECOC 2017. The use of an InP based semiconductor optical amplifier block heterogeneously integrated with the PIC is also one of the possible techniques for the reduction of total losses (for compensation of losses) [44].

Future efforts to make commercially mature device with polarization insensitive operation, as an absolute characteristic, are also needed.

Imperfections of integrated optical circuits due to fabrication require some fine tuning to be compensated - consuming significant power and demanding the development of complex calibration algorithms. With advances in manufacturing processes (development of silicon wafer with better thickness tolerances), the tuning power consumption and the complexity of algorithms for the compensation of imperfections are expected to be reduced. This should also relax the requirements for the device package design.

6.3.2 Scalability

A very important consideration in the design of a complete system was future scalability. 3D EPIC has been proposed and discussed by many organizations, but the commitment to product usage is very doubtful, considering the costs and moderate performance, e.g. on a high data rate transceiver. However, there are some advantages of 3D integration in comparison to the wire-bonding approach in our case. As it is mentioned in Chapter 3, the presented electronic-photonic IC (EPIC) has more than 2000 micropillars for connecting the EIC and the PIC. This large number comes from a need to control more than 800 heaters, read out 84 monitoring diodes and have a sufficient number of pads to carry the necessary current for heater supply. Using standard bond pads instead of these 2000 micropillars would have several major consequences. First of all, regular bond pads are much bigger than micro pillar pads, resulting in a much bigger chip area necessary for both, the electronic IC (EIC) and the photonic IC (PIC), if wire bonding is used, increasing production cost. Additionally, the distance between the heater driver output and the heater that is placed close to the micro-ring resonator would be in the range of 1cm and above, resulting in parasitic inductances in the range of 10nH which is a problem for the used PWM approach. Considering the high frequency components of the PWM control the performance of heater control would degrade.

While it might be possible to use wire bonding for those 2000 pads by considerably increasing chip sizes, it would definitely not be feasible anymore if we want to scale EPIC for larger matrix sizes. For example, an increase by a factor of 10 would result in 20.000 pads, which is still feasible for 3D integration, but not commercially possible for wire bonding. So, this 3D integration technology with micro copper pillars gives us possibilities for scalability. However, there are some other difficulties which limit size of the optical switch matrix.

Thermal crosstalk: Temperature distribution between multiple switches inside the matrix is simulated to predict cross-talk among individual switch elements [78]. Three micro-rings are turned on with the same voltage of 1.25 V. Details of the applied scenario are

presented in [44]. The results show that thermal cross talk between the neighboring micro-rings is less than 1.6 ℃, while thermal cross talk between the heated micro-rings is lower than 1.2 ℃. The measured resonance shift is ~10 GHz per degree, which means that turning on the adjusted rings could detune a turned off ring by up to 16 GHz, i.e. a turned on ring can be detuned by up to 12 GHz. As regards the turned off ring, this shift has no influence, since the filter is located much further from the resonance wavelength. However, the impact of a 12 GHz shift, when the ring is in the on state, depends on the filter characteristic. On a double ring, with a very broad channel, around 80 GHz, this cross talk should have no impact. However, on a single ring filter, this effect may have impact [44].

Smaller technology for the design of the control EIC is available, allowing a smaller layout area for the control circuits. In IRIS project, the smallest pitch size is 50 μm, while smaller pitch sizes are technologically available. However, a limitation in pitch sizes comes from the photonic side, thermal crosstalk and footprint size of the photonic components. Efforts in this direction are needed to make scalable electronic-photonic systems in the near future.

6.3.3 Improvements in EIC

There are several directions for further research and improvement of this work suggested in this final chapter. As already concluded, the best electronic performances are salient in the hybrid approach with an integrated 8bit DAC inside of each control cell. So, using a more advanced integrated electronics technology implementation of this approach into full matrix could be an interesting direction. Also, using more advanced technology for the design of EIC would make it possible to implement digital control approach into the full matrix, since digital circuits are scalable.

Of all designs of an electronic circuits, only a CMOS part of the BCD8sP technology was used. This would reduce the cost of mass production since CMOS technologies are cheaper than BCD technologies. However, having available BCD technology for the design gives us the possibility to integrate a highly efficient DCDC converter into the same chip with control electronics, having a more compact packaged device. Integration of IPs such as a processor, DACs or ADCs used for closing the feedback loop would also be an interesting direction, enabling smaller packaging.

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PERSONAL DATA

Date of birth: 22nd June 1987
Nationality: Serbian

PROFESSIONAL EXPERIENCE

Jan 2014 – Dec 2017 **Mixed signal IC designer,**
Project assistant at Vienna University of Technology

- working on FP7 EU project IRIS in which highly integrated photonic chip is 3D-integrated on an electronic IC (EIC), which has to control all the photonic switches in the photonic chip
- designing analog-digital control electronic chips from scratch to gds
- Analog designs: OPAMPs, comparators, oscillators, SC circuits, voltage & current references, TIAs, DAC, DCDC converter
- Digital designs: SPI, FSMs, power-area-timing trade off driven efficient implementation of registers, address decoders, PWM generators, counters…
- the most complex chip had more than 52300 CMOS transistors
- deep knowledge of CADENCE flow for analog and digital designs
- technology BiCMOS 180 nm
- programming ATMEL microcontroller ATxmega128A1U in AVR studio
- design of PCBs in EAGLE, multilayer, high frequency
- testing, measurement and characterization of chips

Sep 2012 – Dec 2013 **Digital Design Engineer,**
ELSYS Eastern Europe, Belgrade (Serbia) – subcontractor for Texas Instruments, Germany

- Digital IP development
- RTL coding in VHDL, RTL checks with Spyglass
- NCsim simulations, pre and post-layout simulations
- Tools : Cadence – RC compiler, Encounter, STA, LEC, EPS, DFT and ATPG
- Low power design techniques, technology 130 nm
- TCL, DesignSync, ClearCase

Nov 2011 – Aug 2012 **Power Electronics Engineer**
Informatika, A.D. Belgrade (Serbia)

- Design of Power Supply for Industrial Computers, 100 W
- AC-DC converter, current fed push pull, multiple outputs topology
- Developing algorithms for analog and digital control (CPLD)
- simulations and calculations are done in MATLAB, Pspice, Epcos,
- design with discrete technology, high efficiency

INTERNSHIP

Sep – Nov 2010 IAESTE Praxis at the Bremen Institute for Metrology, Automation and Quality Science, Bremen, Germany

EDUCATION

2014 – 2018 Faculty of Electrical Engineering, Vienna University of Technology

- **Doctoral studies**
- Title of thesis: "Control circuits for an electronic-photonically integrated optical switch matrix"
- Courses: Optoelectronic integrated circuits, Analog integrated circuits, Nanoelectronic circuits, RF techniques, Lab RF techniques, Fast signal processing in high-energy physics, Device modeling

2010 – 2011 Faculty of Electrical Engineering, University of Belgrade

- **Master of Science in Electronics**
- GPA: 10.00/10, full scholarship
- Master's thesis: "Quasiresonant buck convertor type A with thyristor"
- Master courses: RF electronics, Power electronics 2, Digital signal processors, ARM Microcontrollers, Digital Control of Electrical drives

2006 – 2010 Faculty of Electrical Engineering, University of Belgrade

- **Bachelor of Science in Electronics**
- GPA: 9.6/10, full scholarship all the time
- Bachelor's thesis: "FPGA Implementation of PID regulator"

SEMINARS AND BUSINESS TRIPS

- European Commission, Brussels, March 2017
- CEA-LETI, Grenoble, March 2017
- Universitat Politècnica de València, March 2016
- CNIT, Pisa, Italy, January 2014
- Petnica Science center, Serbia – seminar in Physics (2005)
- Excursion to CERN, Genève –invited by Serbian Physical Society (2005)

MEMBERSHIP

- member of IEEE society from 2009
- Goethe Institute, Belgrade

COMPUTER SKILLS

Computer skills: Windows, Linux
Programming skills: Assembler, C, C++, VHDL, Verilog
CAD tools: CADENCE (RC, Encounter), Virtuoso, ADE L/XL, Spectre, MATLAB

LANGUAGE SKILLS

- Serbian - native
- English - professional working proficiency
- German – intermediate

COMPETITIONS AND AWARDS

- I took part at the state and republic competitions in mathematics and physics of high Schools of Serbia
- ”Elektrijada” - competition for students studying Electrical Engineering in Balkan, 2007:

  3rd award in Physics
- 1st place and prize of 30 000 RSD (300 €) in the quiz organized in honor of 150 years of birthday the famous Serbian scientist Nikola Tesla in Zrenjanin

INTERESTS

- sport, fitness, basketball, tennis, swimming, playing guitar, music, cooking, skiing

LICENSE

- Driving license, B category

Vienna, March 2018