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Dissertation

Optoelectronic Circuits in 40nm CMOS Technology

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Declaration of Authorship

I, Mohammed Hassan, declare that this thesis titled, 'Optoelectronic Circuits in 40nm CMOS Technology' and the work presented in it is my own and the work done by other authors is appropriately cited.

Signed:

Date: Wien, im March 18, 2015

"He who performs not practical work nor makes experiments will never attain to the least degree of mastery."

Jabir-Ibn-Hayyan

Abstract

The rapidly increasing interest in high speed access networks and large capacity communication encouraged the advancement of low-cost optical transmission systems. The tendency to design highly integrable and low cost broadband optical systems, makes it desirable to realize optoelectronic circuits such as transimpedance amplifiers (TIAs) and laser diode drivers (LDDs) in CMOS technology. Since advanced CMOS technology introduces challenges regarding the design of such circuits, the need of lower power dissipation and higher integrability motivates further research on new circuit topologies.

This dissertation shows that nanometer CMOS technology can be used to design two of the most vital blocks in a typical optical transmission system, namely, the TIA in the optical receiver and LDD in the optical transmitter. Main focus of this thesis is to propose new topologies to overcome the technology limitations and allow the implementation of low power compact TIAs and a high voltage LDD. The circuits are all designed in standard 40nm CMOS technology.

On the receiver side, three novel different inductorless TIAs are presented. For measurement purposes, the TIAs are integrated with a chain of voltage amplifiers and a 50Ω output buffer. The first TIA is implemented using a push pull current mirror (PPCM) with a feedback resistor. Experimental results show that this TIA achieves a power efficiency of 0.324 mW/Gb/s from a 1.2V supply at a maximum data rate of 10Gb/s. The whole design occupies an active area of 51×96 μm^2. The second TIA is implemented using a common drain active feedback (CDAF). Measurement results show that this TIA acquires a power efficiency of 0.3 mW/Gb/s from a 1.2V supply at a maximum data rate of 8Gb/s. The full design occupies an active area of 33×101 μm^2. The third TIA introduces a regulated cascode TIA with an active feedback (RGCAF). Experimental results show that the TIA achieves a power efficiency of 0.24mW/Gb/s from a 1.2V supply at a maximum data rate of 10Gb/s. The whole design occupies an active area of 44×89 μm^2. In comparison with the state-of-the-art the proposed TIAs show a competitive power efficiency while occupying minimum chip area.

On the transmitter side, a high voltage LDD is implemented. An open drain double cascode fully differential structure is used to provide a high modulation current of up to 80mA and to guarantee a reliable operation of the devices under high voltage condition. To reduce power consumption, the LDD is supplied by 1.1V for the pre-driver and 5V for the output stage. Measurement results show a step response with rise and fall times (10%- 90%) of 209ps and 153ps, respectively. Therefore the LDD can operate at a data rate of 3Gb/s.

Kurzfassung

Das ansteigende Interesse an Hochgeschwindigkeitsnetzwerken und Kommunikation mit hohen Kapazitätsanforderungen animiert die Weiterentwicklung von preiswerten, optischen Übertragungssystemen. Die Tendenz solche hochintegrierbaren Übertragungssysteme anzuwenden, macht es wünschenswert optoelektronische Schaltungen wie Transimpedanzverstärker (TIAs) und Laserdiodentreiber (LDDs) in CMOS-Technologie zu entwerfen. Da diese Nanometer-CMOS-Technologie neue Herausforderungen bezüglich Design solcher Schaltungen mit sich bringt, wird weiterführende Forschung an neuen Schaltungstopologien wegen kleiner werdender Leistungsaufnahme und höherer Integrierbarkeit vorangetrieben.

Diese Dissertation zeigt auf, dass in einer Nanometer-CMOS-Technologie mit einem TIA in der optischen Empfängereinheit und einem LDD in der optischen Sendeeinheit zwei essentielle Blöcke in einem typischen optischen Übertragungssystem entwickelt werden können. Ferner konzentriert sich diese Arbeit auf Vorschläge neuer Schaltungstopologien um Technologielimits zu überwinden und die Implementierung von kompakten und sparsamen TIAs und Hochvolt-LDDs zu ermöglichen. Die Schaltungen sind in einer standard 40nm CMOS-Technologie realisiert.

Auf der Empfängerseite werden drei verschiedene, spulenlose TIAs präsentiert. Zu Messzwecken sind die TIAs in einer Kette von Spannungsverstärker mitsamt einem 50Ω Ausgangstreiber integriert. Der erste TIA ist als push-pull Stromspiegel (PPCM) mit einem Rückkopplungswiderstand ausgeführt. Messergebnisse zeigen einen Wirkungsgrad von 0.324 mW/Gb/s bei einer Versorgungsspannung von 1.2V und einer maximale Datenrate von 10Gb/s. Das gesamte Design benötigt eine aktive Fläche von $51\times96\mu m^2$. Der zweite TIA wurde als 'common drain' aktives Feedback (CDAF) verwirklicht. Der Wirkungsgrad liegt laut Messungen bei 0.3 mW/Gb/s. Die Versorgungsspannung beträgt 1.2V und ergibt eine maximale Datenrate von 8Gb/s. Die TIA-Schaltung benötigt eine aktive Fläche von $33\times101\mu m^2$. Im Vergleich mit dem heutigen Stand der Technik zeigen alle TIAs einen konkurrenzfähigen Wirkungsgrad bei minimaler Chipfläche.

Seitens des Senders wurde ein Hochvolt-LDD implementiert. Um sowohl eine hohe Aussteuerung von bis zu 80mA, als auch einen verlässlichen Betrieb unter Hochvoltbedingungen gewährleisten zu können, wurde eine komplett differenzielle, 'open drain' - Doppelkaskodenstruktur verwendet. Zur Stromeinsparung wird der LDD mit 1.1V für die Vorstufe und mit 5V für die Endstufe versorgt. Die Messergebnisse zeigen eine Sprungantwort mit Anstiegs- bzw. Abfallzeiten (10% - 90%) von 209ps bzw. 153ps. Dadurch kann der LDD mit einer Datenrate von 3Gb/s betrieben werden.

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To my

Mother and Father

Chapter 1

Introduction

1.1 Motivation

In the past years, the speed of data processing and computation have been increasing rapidly and will continue to do so in future. The processing and computing power are not determined only by the microprocessor's speed but equally important is the speed at which data is transferred to and from the core processor. That means that the required bandwidth of the input and output (IO) channels must cope with the microprocessor's speed [20]. It is strongly believed in future that these channels will be the speed bottle-neck for the whole system.

Until recently, for short and medium distance the data communication links are implemented by electrical connections such as printed-circuit transmission lines, twisted pairs or coaxial cables. Electrical transmission medium has severe problems at high speeds such as signal losses due to skin effect resulting in bandwidth limitation, poor matching which leads to distorted signals and significant Electro-Magnetic noise generation which deteriorates the performance of the whole system [19]. In order to overcome these problems, equalization techniques may be used or parallel Gb/s links are added to achieve the desired data rates. Both solutions, increase the complexity of the system and hence the cost, without a significant improvement in the capacity of communication links. Instead of increasing the complexity of the transmission links, a more efficient way is to use optical transmission medium [44].

Better Signal-to-Noise-Ratio (SNR), higher bandwidth, decreased number of amplifiers in the signal path and effectively low cost, have made optical fibre communication the technology of choice to potentially close the gap between the interconnect speed and the data processing speed. Additionally, parallel optical signalling at short distance is

simpler than electrical IOs. It's either implemented by using optical fibre bundles or free space to send parallel light beams from one chip to another. The cross talk between beams in both cases are considerably lower than in electrical IOs [9].

Optical fibres can support very large data rates for short distances due to their negligible frequency dependent loss and dispersion, therefore it is not the data rate limiter. The maximum data rate of an optical link is limited by the operation speed of the optical transmitter (TX) and receiver (RX) [30].

In this thesis we aim to study and investigate the challenges in the design of vital blocks in both the TX and RX ends and introduce a number of solutions to ease the implementation of low cost and high performance optical IOs. In order to achieve this goal a new simple, low power and highly integrable circuit topologies are presented.

1.2 Optical Link Architecture

A simplified optical transmission system is shown in figure 1.1. It consists of a TX, transmission medium (optical fibre) and a RX. The TX converts electrical signal into optical and transmits it through a low cost optical fibre then the electrical signal is attained again at the RX end [39].

The TX consists of three main modules: a serializer, a driver and a light emitter. The serializer consists of a multiplexer (MUX), a phased-locked loop (PLL) and a retimer. The MUX combines the synchronous parallel digital input signal into a single high speed bit stream. Nonidealities such as jitter and intersymbol interference (ISI) introduced by the MUX are absorbed by the retimer. Both the MUX and the retimer need clock signals, which are generated by the PLL. The retimer is followed by a driver which delivers a high modulation current to the light emitter. The light emitter converts the electrical data into optical pulses. Laser diode (LD) is usually used as light emitter because it produces high light intensity to compensate the attenuation that will experienced by light as it travel through the optical fibre.

On the RX side, the same process happens in a reverse manner. The RX is divided into three modules: photodetector, front-end and a deserializer. The front-end consists of a transimpedance amplifier (TIA), limiting amplifier (LA) and an automatic gain control (AGC). The deserializer consists of two blocks: clock and data recovery block (CDR) and a demultiplexer (DMUX).

The transmitted light signal is received by the photodetector which is a photodiode (PD) in most cases. The PD converts the optical signal into a proportional output

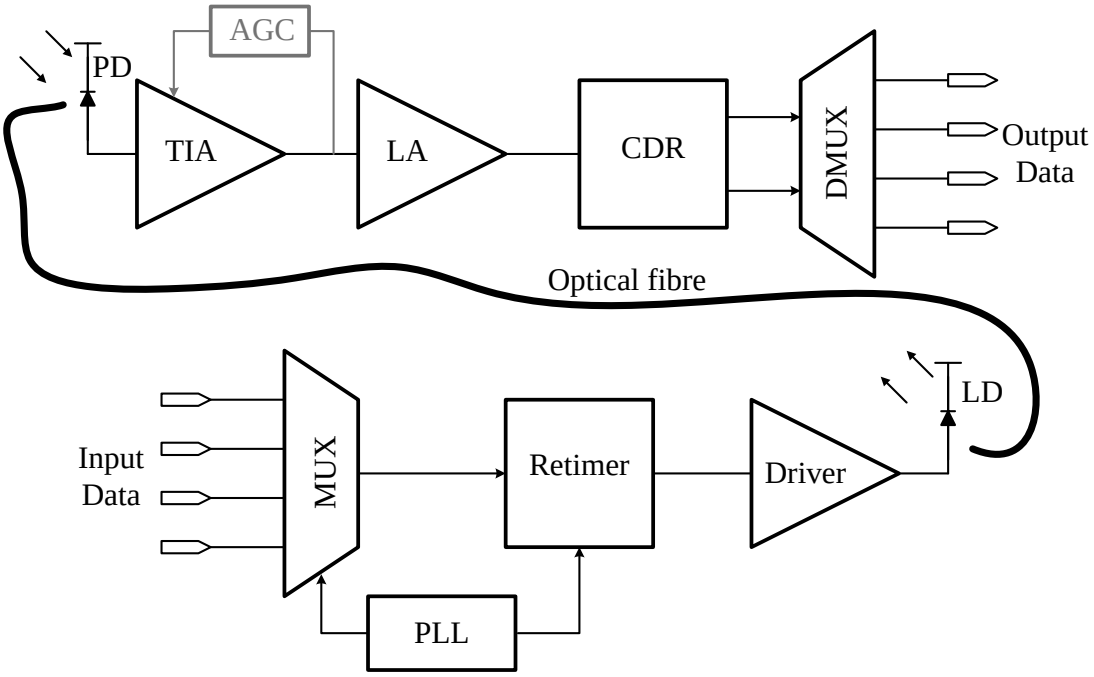

FIGURE 1.1: Optical link architecture

photocurrent. Because the transmitted light is attenuated by the optical fibre, the PD should be highly sensitive to light. The weak photocurrent is converted into an amplified voltage by the TIA. The TIA's output voltage is further amplified to provide logical levels by a high gain LA. An AGC is employed to a TIA to decrease its gain for high input signal amplitudes to allow a linear operation for a wide range of input signal amplitudes. At that point, the output voltage is strong enough. Finally, this voltage is fed into the deserializer, where the CDR extracts the clock signal and retimes the data signal. The CDR is followed by a DMUX where the fast serial bit stream is demultiplexed to a parallel digital output signal.

1.3 Thesis Objectives

Although Hot Electron Mobility Transistors (HEMT), Heterojunction Bipolar Transistors (HBT) and Silicon (Si) bipolar transistors were favourable technologies for high speed optical transceivers due to their noise and speed advantages, they result in a high cost product [26]. Therefore, Complementary Metal Oxide Semiconductor (CMOS) technology is possibly the best choice for low cost, low power and high integration density optical transceivers. On the other hand, the low intrinsic voltage gain and low power supply of nanometer CMOS devices lead to design difficulties which must be overcome to compete with other technologies [38].

The main objective of this thesis is to introduce new circuit ideas to implement low power high speed inductorless TIAs and high voltage laser diode driver (LDD) in standard 40nm CMOS technology.

Usually CMOS TIAs use inductors to achieve data rates of 10 Gb/s or higher. However, using inductors have a number of disadvantages [31]:

1. The chip area increases significantly, leading to a higher cost.
2. High substrate coupling, results in higher cross talk.
3. Poor group delay linearity.

Therefore, to achieve low cost compact TIA designs the use of inductors are avoided leading to more design challenges to achieve the desired data rate.

With the shrinking of the CMOS transistor feature size, the supply voltage is reduced to ensure reliability of the device. This reduction in supply voltage results in some difficulties in LDD design, because there is a large change in the voltage drop over the LD between logical 0 and 1, which makes it difficult to reduce the supply voltage of the LDD below 3.3V. Red lasers have voltage drops larger than 2V. Therefore, it is desirable to introduce new circuit topologies of CMOS LDDs to sustain high supply voltages and provide large modulation current [15].

1.4 Thesis Outline

The thesis consists of three main parts: theoretical background, the circuits implementation and the results discussion and conclusion. The thesis is organized as following:

Chapter 2 provides the theoretical background of LDD and TIA. The chapter reviews the traditional circuit techniques for both blocks. The analysis, advantages and limitations of each technique will be stated and discussed.

Chapter 3 presents the state of the art of high voltage CMOS LDDs and high speed CMOS TIAs. The chapter begins with explaining the latest high performance CMOS TIAs, then the most recent high voltage CMOS LDDs will discussed.

Chapter 4 states briefly in the beginning the physical effects and drawbacks of nanometer CMOS technology. Then the chapter will show the characteristics of both the p-channel metal oxide semiconductor (PMOS) and the n-channel metal oxide semiconductor (NMOS) transistors in 40nm CMOS technology.

Chapter 5 introduces three solutions for high speed inductorless CMOS TIAs and a high voltage CMOS LDD. The chapter will include a theoretical analysis and discussion of each design. Then the simulation and measurement results will be presented and compared with one another and with the state of the art.

Chapter 6 concludes and highlights the main achievements of the proposed solutions.

Chapter 2

Fundamentals of Optoelectronic circuits

In this chapter, two of the most critical blocks in an optical link will be discussed. The main focus will be on the TIA on the RX side and the LDD on the TX side. The basic idea, performance requirements and technology independent circuit concepts of both circuits will be explained in details. Finally, the most important points will be summarized in the chapter's conclusion.

2.1 Transimpedance Amplifiers

2.1.1 General Concept

Since the PD converts the transmitted light to a weak output photo-current and since the successive processing occurs in the voltage mode. Therefore, the photo-current must be transformed to voltage. This function is performed by the transimpedance amplifier (TIA), it transforms the input current into amplified output voltage. The TIA's amplification factor is called the transimpedance gain and it is defined as the derivative of the output voltage as a function of the input current (Z_T=$dV_o(I_{PD})/dI_{PD}$). TIA is the most vital block in an optical front-end as it defines the receiver's data rate, linearity and most importantly the sensitivity [49].

The simplest TIA uses a resistor (R_T) as shown in figure 2.1. The transimpedance gain is equal to the resistance value of (R_T). The bandwidth (BW) is defined by the resistor (R_T) and the parasitic capacitance of the PD (C_{PD}), BW=1/ $2\pi C_{PD}R_T$, showing a clear trade-off between the transimpedance gain and bandwidth.

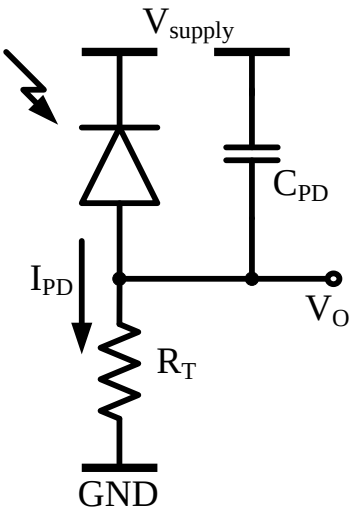

FIGURE 2.1: TIA using a simple resistor.

Another important aspect is noise which is directly related to the sensitivity of the RX. The thermal noise in the resistor R_T [39] is :

$$\overline{I_{noise}^2} = \frac{4kT}{R_T}, \tag{2.1}$$

where k is the Boltzmann constant and T is the absolute temperature.

The total output integrated noise is:

$$\overline{V_{o,noise}^2} = \frac{4kT}{R_T} \int_0^\infty \left[R_T \parallel \frac{1}{2\pi j C_{PD} f} \right]^2 df \tag{2.2}$$

$$= \frac{4kT}{R_T} \int_0^\infty \frac{R_T^2 df}{4\pi^2 R_T^2 C_{PD}^2 f^2 + 1} \approx \frac{kT}{C_{PD}} \tag{2.3}$$

Equation 2.3 shows that the total integrated output voltage noise is independent of the resistance value R_T. Decreasing R_T increases $\overline{I_{noise}^2}$ but the transimpedance gain $R_T^2/(4\pi^2 R_T^2 C_{PD}^2 f^2 + 1)$ decreases with the same amount keeping $\overline{V_{o,noise}^2}$ constant.

For understanding of the dependence of noise on the transimpedance gain, the noise must be referred to the input. The input referred noise is

$$\overline{I_{in,noise}^2} = \frac{\overline{V_{o,noise}^2}}{R_T^2} \tag{2.4}$$

$$= \frac{kT}{R_T^2 C_{PD}}. \tag{2.5}$$

Equation 2.5 shows that maximizing the R_T is essential to decrease the input referred noise current.

The fundamental trade-offs between transimpedance gain, bandwidth and input referred noise current suggest that the resistive/diode combination is not suitable for high performance applications.

The analysis of the simple resistive TIA shown in figure 2.1 proved that resistance R_T directly couples the bandwidth and noise equations. Therefore, more complex configurations are needed to provide large bandwidth (low input resistance), high gain and minimum noise for a given photodiode parasitic capacitance. Two main categories of TIAs are known to achieve high performance noise-bandwidth-gain requirement: open-loop TIAs and feedback TIAs.

2.1.2 Open Loop TIA

2.1.2.1 Transfer Function

Common gate (CG) amplifier is a well known low input resistance amplifying stage. Figure 2.2 shows CG amplifying stage including the input capacitance C_{in} and the output capacitance C_{out}. C_{in} is the summation of photodiode capacitance (C_{PD}), gate-source capacitance of M_1 (C_{gs_1}), gate-drain capacitance of M_2 (C_{gd_2}) and drain-bulk capacitance of M_2 (C_{db_2}). C_{out} includes the input capacitance of the subsequent stage, gate-drain capacitance of M_1 (C_{gd_1}) and drain-bulk capacitance of M_1 (C_{db_1}).

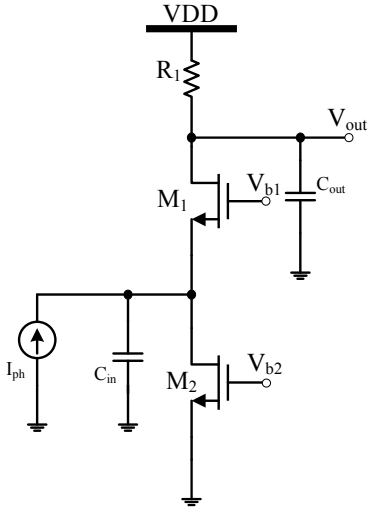

FIGURE 2.2: Common gate TIA.

From the small signal model shown in figure 2.3, the parameters of the CG TIA could be derived. In the following analysis body effect and channel-length modulation are included [39].

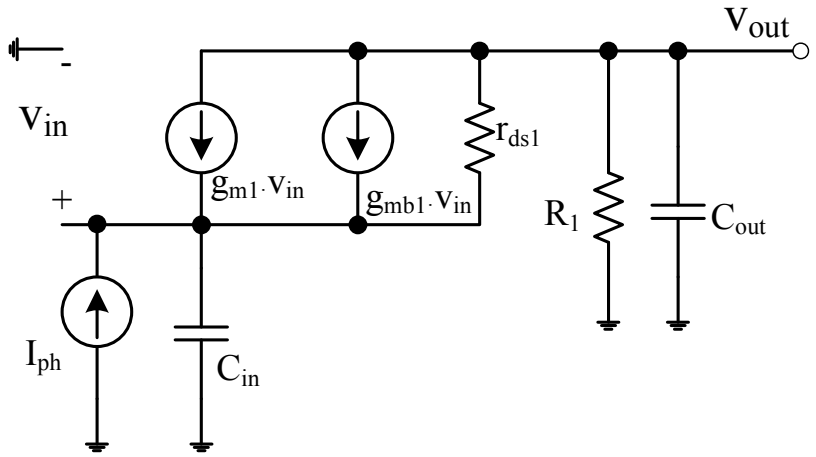

FIGURE 2.3: Common gate TIA small signal model.

The input resistance can be derived from the equations extracted from figure 2.3,

$$-V_{in} = I_{ph}R_1 + (r_{ds_1}I_{ph} + (g_{m_1} + g_{mb_1})V_{in}), \tag{2.6}$$

$$R_{in_{CG}} = \left|\frac{V_{in}}{I_{ph}}\right| = \frac{r_{ds_1} + R_1}{1 + r_{ds_1}(g_{m_1} + g_{mb_1})}. \tag{2.7}$$

Since $r_{ds_1}(g_{m_1} + g_{mb_1}) \gg 1$,

$$R_{in_{CG}} = \frac{r_{ds_1} + R_1}{r_{ds_1}(g_{m_1} + g_{mb_1})}. \tag{2.8}$$

If r_{ds_1} approaches ∞, $R_{in_{CG}} \approx 1 \ / \ (g_{m_1}+g_{mb_1})$. In short-channel devices, the output resistance r_{ds_1} is comparable to R_1, leading to a higher input resistance.

The input impedance of CG TIA is the parallel connection of $R_{in_{CG}}$ and C_{in},

$$R_{in_{CG}}(s) = \frac{r_{ds_1} + R_1}{r_{ds_1}(g_{m_1} + g_{mb_1}) + sC_{in}(r_{ds_1} + R_1)}. \tag{2.9}$$

The first step to derive the CG TIA's transimpedance gain is to state the voltage gain of the CG stage,

$$A_{CG}(s) = \frac{V_{out}}{V_{in}} = (g_{m_1} + g_{mb_1})\left(\frac{R_1}{1 + sC_{out}R_1}\right). \tag{2.10}$$

The transimpedance gain is the multiplication of 2.9 and 2.10,

$$Z_{T_{CG}}(s) = \frac{V_{out}}{V_{in}} \cdot \frac{V_{in}}{I_{ph}} = \frac{V_{out}}{I_{ph}}. \tag{2.11}$$

$$Z_{T_{CG}}(s) = \frac{(r_{ds_1} + R_1)(g_{m_1} + g_{mb_1})R_1}{(r_{ds_1}(g_{m_1} + g_{mb_1}) + sC_{in}(r_{ds_1} + R_1))(1 + sC_{out}R_1)}. \tag{2.12}$$

The DC transimpedance gain of the CG stage is

$$Z_{T_{CG}}(0) = R_1 \left[1 + \frac{R_1}{r_{ds_1}}\right]. \tag{2.13}$$

From equation 2.12, CG TIA has two poles: the input pole $(g_{m_1} + g_{mb_1})/C_{in}$ and the output pole $(C_{out}R_1)^{-1}$. The input pole is the dominate pole, since the photodiode parasitic capacitance is quite large.

To maximize the bandwidth, the quantity $(g_{m_1} + g_{mb_1})$ must be maximized, either by increasing the width of M_1 or the biasing current of the CG TIA. However, increasing the width of M_1 with increase the gate-source capacitance and hence lead to bandwidth limitation. Increasing the biasing current of the CG stage will increase the voltage drop over R_1, resulting in the decrease of the overhead voltage of M_1 and M_2, requiring a higher supply voltage. If R_1 is decreased to have the same voltage drop, the transimpedance gain will decrease and the TIA's noise current will increase. If the width of M_2 is increased to accommodate the decrease of the overhead voltage, then both the noise and drain capacitance will increase.

The previous analysis shows achieving a wideband performance will lead to a low transimpedance gain, resulting in significant noise contribution for this stage and subsequent stages.

2.1.2.2 Noise Analysis

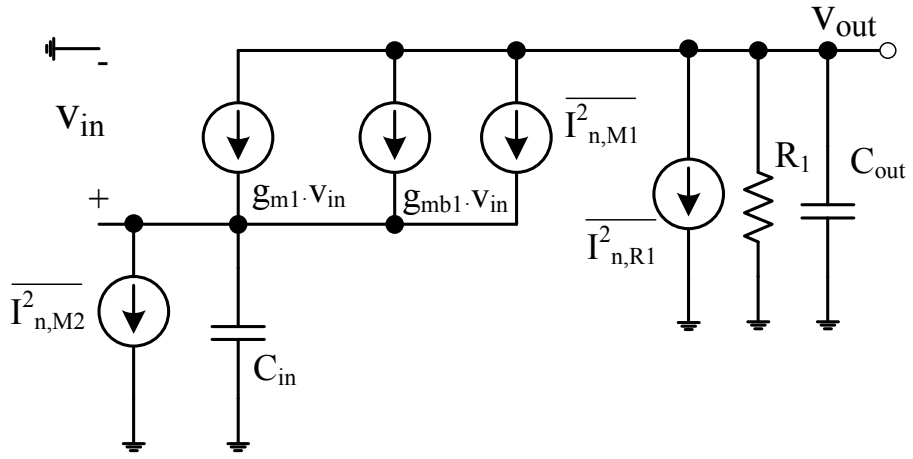

FIGURE 2.4: Noise model of CG TIA.

Figure 2.4 shows the small signal noise model of the CG TIA. It includes the thermal noise of R_1 and the noise current of M_1 and M_2.

The spectral output noise voltage of CG TIA [39] is

$$\overline{V_{out,noise}^2} = \frac{R_1^2}{(R_1 C_{out} s)^2 + 1} \left[\frac{\overline{I_{n,M1}^2}(sC_{in})^2 + \overline{I_{n,M2}^2}(g_{m_1} + g_{mb_1})^2}{(sC_{in})^2 + (g_{m_1} + g_{mb_1})^2} + \overline{I_{n,R1}^2} \right]. \tag{2.14}$$

The total integrated output noise voltage from s=0 to s=∞ [39] is

$$\overline{V_{out,int,noise}^2} = \frac{kT}{C_{out}} \left[\frac{g_{m_1} R_1 C_{in} \gamma}{C_{in} + (g_{m_1} + g_{mb_1}) R_1 C_{out}} + 1 \right] + \frac{2kT(g_{m_1} + g_{mb_1}) g_{m_2} R_1^2 \gamma}{C_{in} + (g_{m_1} + g_{mb_1}) R_1 C_{out}}. \tag{2.15}$$

Since the dominate pole is located at the input $C_{in}/(g_{m_1} + g_{mb_1}) >> R_1 C_{out}$

$$\overline{V_{out,int,noise}^2} \approx \frac{kT}{C_{out}} \left[g_{m_1} R_1 C_{in} \gamma + 1 \right] + \frac{2kT(g_{m_1} + g_{mb_1}) g_{m_2} R_1^2 \gamma}{C_{in}}. \tag{2.16}$$

Dividing equation 2.16 by the R_1^2 results in the integrated input referred noise current:

$$\overline{I_{in,int,noise}^2} \approx \frac{kT}{C_{out} R_1^2} \left[g_{m_1} R_1 C_{in} \gamma + 1 \right] + \frac{2kT(g_{m_1} + g_{mb_1}) g_{m_2} \gamma}{C_{in}}. \tag{2.17}$$

For short channel MOS transistors, γ >1, which shows that input referred noise current increases as the CMOS technology is scaled down.

Equation 2.17 shows that g_{m_1} can be lowered to decrease noise at the cost of bandwidth. Decreasing g_{m_2} is the only parameter that can decrease noise without affecting the bandwidth. However, it will decrease the voltage headroom for a given biasing current, showing that CG TIA has limited flexibility from noise perspective. Therefore, it is ill suited for low noise applications.

2.1.3 Shunt Shunt Feedback TIA

2.1.3.1 Transfer Function

The basic topology of a shunt shunt feedback TIA is shown in figure 2.5, where the feedback resistor R_F is connected between the input and the output of an inverting voltage amplifier. R_F converts the input photodiode current to output voltage. The inverting voltage amplifier guarantees low noise at high frequencies [49].

C_{in} is the total capacitance at the input node of the TIA. It includes the photodiode capacitance, input capacitance of the amplifier, pad capacitance and parasitic capacitance associated with R_F. Since C_{in} introduces loss at high frequencies, it is important to keep C_{in} as small as possible to achieve high noise performance.

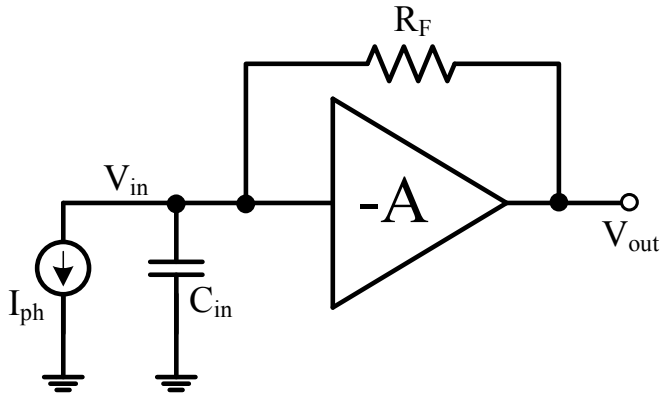

FIGURE 2.5: Shunt shunt feedback TIA.

The inverting voltage amplifier is assumed to have a single pole lowpass behaviour $A(s)$ with a DC gain A_{DC} and a single pole at f_o,

$$A(s) = \frac{A_{DC}}{1 + \frac{s}{2\pi f_o}}. \tag{2.18}$$

Applying Kirchhoffs laws to the TIA in figure 2.5 results in:

$$I_{ph} = -sV_{in}C_{in} - \frac{V_{in} + V_{out}}{R_F}. \tag{2.19}$$

Knowing that $V_{out} = A(s)V_{in}$, the transimpedance gain is

$$Z_T(s) = \frac{V_{out}}{I_{ph}} = -\frac{A(s)R_F}{A(s) + 1 + sR_FC_{in}}. \tag{2.20}$$

Substituting 2.19 in equation 2.20, the transimpedance gain can be expressed as

$$Z_T(s) = -\frac{2\pi f_o A_{DC} C_{in}^{-1}}{s^2 + s\left(\frac{2\pi f_o R_F C_{in} + 1}{R_F C_{in}}\right) + \frac{2\pi f_o (A_{DC}+1)}{R_F C_{in}}}. \tag{2.21}$$

The low frequency (s=0) transimpedance gain is

$$Z_T(0) = -\frac{A_{DC}}{A_{DC} + 1} R_F. \tag{2.22}$$

From control theory, for a second order transfer function with a denominator equal to $s^2 + s2\zeta\omega_n + \omega_n^2$, the damping factor ζ has to be equal to $\sqrt{2}/2$, to avoid ringing in the TIA's step response.

The TIA's natural frequency ω_n and damping factor ζ are

$$\omega_n = \sqrt{\frac{2\pi f_o (A_{DC} + 1)}{R_F C_{in}}}, \tag{2.23}$$

$$\zeta = \frac{1}{2}\frac{2\pi f_o R_F C_{in} + 1}{\sqrt{2\pi f_o R_F C_{in}(A_{DC}+1)}}. \tag{2.24}$$

For critical damping $\zeta = \sqrt{2}/2$, the -3dB bandwidth of the voltage amplifier is

$$f_o \approx \frac{1}{\pi}\frac{A_{DC}}{R_F C_{in}}. \tag{2.25}$$

To derive the -3dB bandwidth of the feedback TIA, we equate the magnitude of equation 2.21 to $\sqrt{2}/2$ resulting in

$$f_{-3dB} \approx \frac{1}{2\pi}\frac{\sqrt{2}A_{DC}}{R_F C_{in}}. \tag{2.26}$$

Equations 2.25 and 2.26 show that the -3dB bandwidth of the voltage amplifier should be approximately 1.5 times the -3dB bandwidth of the TIA to achieve a critically-damped response. If $f_o > 1.5 \times f_{-3dB}$, the feedback exhibits over-damping response. If $f_o < 1.5 \times f_{-3dB}$, the step response exhibits under-damping, creating inter symbol interference (ISI).

2.1.3.2 Noise Analysis

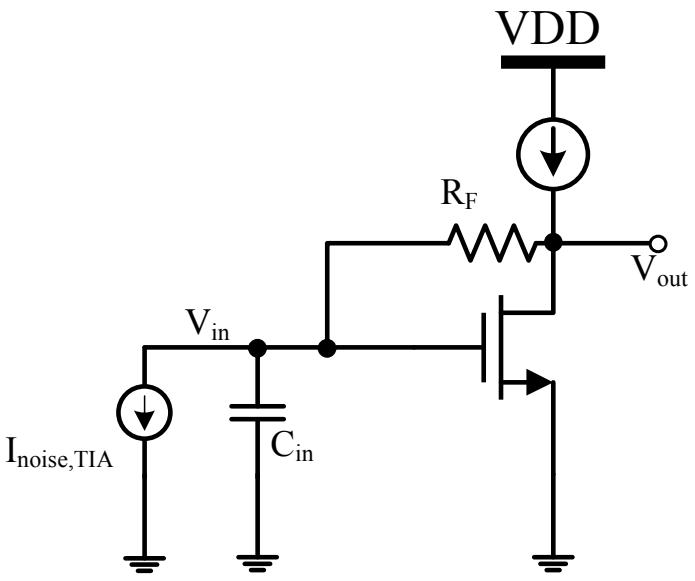

FIGURE 2.6: CMOS Shunt shunt feedback TIA.

In this subsection we analysis the noise performance of a shunt shunt feedback TIA. The analysis will be limited to MOSFET input device, since bipolar technology is beyond the scope of this work. Figure 2.6 shows a simple CMOS shunt shunt feedback TIA.

The input referred noise current is mainly dominated by two noise sources: the noise from the feedback resistor $\overline{I^2_{R_F,noise}}$ and the noise from the NMOS input device $\overline{I^2_{M_N,noise}}$.

These noise sources are usually uncorrelated. Therefore, they can be summed as follows

$$\overline{I^2_{in,noise}}(f) = \overline{I^2_{R_F,noise}}(f) + \overline{I^2_{M_N,noise}}(f). \tag{2.27}$$

The noise generated from the feedback resistor is thermal-noise. For a certain frequency band (f),it is formulated as follows

$$\overline{I^2_{R_F,noise}}(f) = \frac{4kT}{R_F}. \tag{2.28}$$

Equation 2.28 shows that the feedback resistor should be as high as possible to optimize the noise of the TIA.

The noise sources in the NMOS input device are the noise generated by gate leakage current and channel noise. The noise generated by the gate leakage current [41] is

$$\overline{I^2_{M_N,G,noise}}(f) = 2qI_G, \tag{2.29}$$

where I_G is the gate leakage current and q is the charge of an electron. This noise source contributes directly to the input referred noise current of the TIA. This noise component increases as the minimum channel length of the MOSFET decreases.

The most important noise source in a MOS transistor is the channel noise,

$$\overline{I^2_{M_N,C,noise}}(f) = 4kT\Gamma g_m, \tag{2.30}$$

where g_m is the transconductance of the transistor and Γ is the channel noise factor. In a MOS transistor, Γ varies from 0.7 to 3.0, where the high numbers correspond to the short channel transistors [39]. Unlike the previously mentioned noise sources, this noise source is not directly contributing to the input referred noise current. To refer the channel noise to the input, $\overline{I^2_{M_N,C,noise}}$ should be divided by the transfer function from $\overline{I^2_{in,noise}}$ to $\overline{I^2_{M_N,C,noise}}$. This transfer function can be shown to be [41]:

$$T(f) = \frac{g_m R_F}{1 + 2\pi f R_F C_{in}}. \tag{2.31}$$

Using the transfer function in 2.31, the input referred channel noise is

$$\overline{I^2_{M_N,C,in,noise}}(f) = \frac{4kT\Gamma}{g_m R_F^2} + \frac{4kT\Gamma(2\pi f C_{in})^2}{g_m}. \tag{2.32}$$

Equation 2.32 explains the phenomena of the f^2 noise component. This noise component rises from the white noise, which increases due to the lowpass characteristic of the transfer function of 2.31 with a cutoff frequency of $1/2\pi R_F C_{in}$.

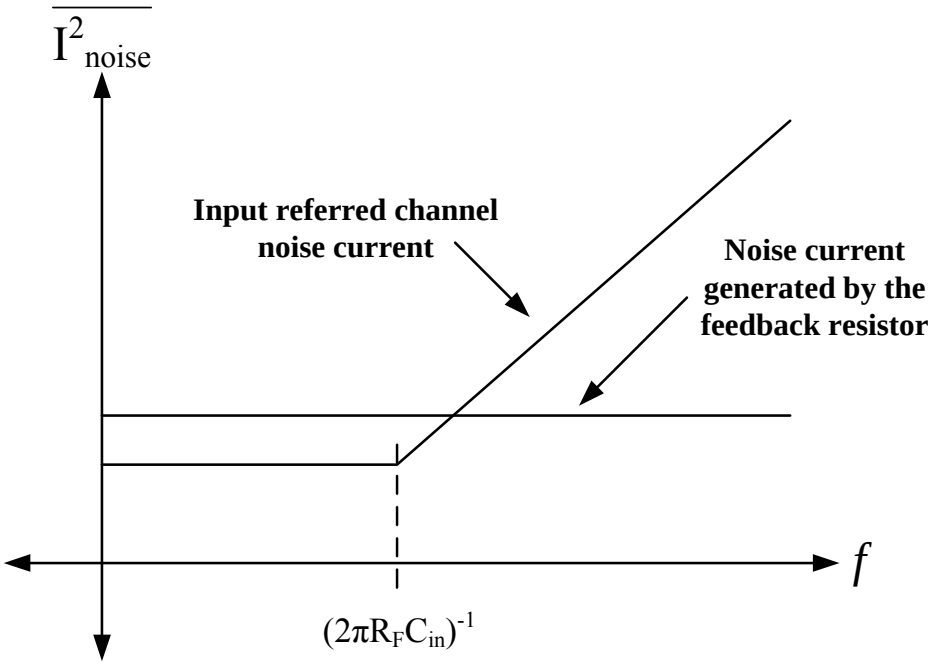

FIGURE 2.7: NMOS channel noise and feedback resistor noise spectrums.

The total input referred noise current spectrum is the summation of all the previously mentioned noise sources:

$$\overline{I^2_{in,noise}}(f) = \frac{4kT}{R_F} + 2qI_G + \frac{4kT\Gamma}{g_m R_F^2} + \frac{4kT\Gamma(2\pi f C_{in})^2}{g_m}. \tag{2.33}$$

Integrating equation 2.33 results in the total integrated input referred noise current in bandwidth B, resulting in the following equation

$$\overline{I^2_{tot,in,noise}} = \int_0^B \overline{I^2_{in,noise}}(f)df = \frac{4kT}{R_F}B + 2qI_G B + \frac{4kT\Gamma B}{g_m R_F^2} + \frac{4kT\Gamma(2\pi C_{in})^2 B^3}{3g_m}. \tag{2.34}$$

Equation 2.34 shows that for high speed front ends the value of the feedback resistor decreases resulting in a significant contribution of noise from both the amplifier and the resistor, worsening the noise performance of the amplifier.

2.2 Laser Diode Drivers

2.2.1 General Concept

Laser diode drivers (LDD) can be modelled as a switching current source that turns the laser diode on and off depending on the modulating input data, as shown in figure 2.8. If the temperature of the laser diode varies during operation, large fluctuation in

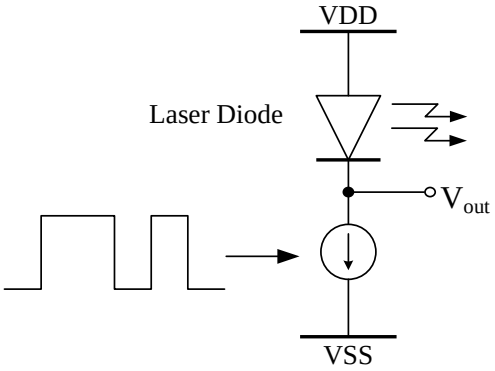

FIGURE 2.8: Ideal model of laser diode driver as a switching current source.

the output power can occur. To reduce this effect, the output power is defined as a function of current (figure 2.9) instead of voltage. For this reason, and because of current switching speed advantages, laser diodes are driven by current [41].

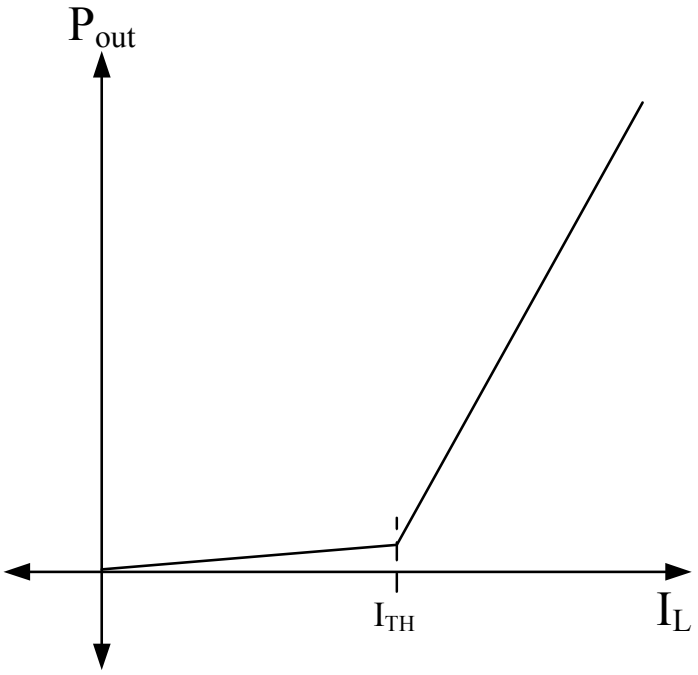

FIGURE 2.9: The power/current characteristic curve of the laser diode.

In general, the electro-optical interface in most optical systems defines the maximum bandwidth of the system. The laser driver is a very vital block in determining the performance of the optical transmitter. Therefore, the driver must fulfil the following criteria:

1: Sufficient switching speed to modulate the output optical power with minimal inter-symbol interference.

2: Provide high output current to generate the adequate output optical power.

3: Tolerant to the voltage swing across the laser diode.

The above criteria makes the design of laser drivers very difficult. As the transistor's minimum feature size scale down to acquire high speeds, the unavoidably lower breakdown voltage makes it increasingly difficult to tolerate the high voltage swing across the laser diode. The large output current required to be delivered by the laser driver obligates the use of wide transistors, thus leading to large input and output capacitances for the laser driver.

2.2.2 LDD Circuit Concept

2.2.2.1 Output Stage

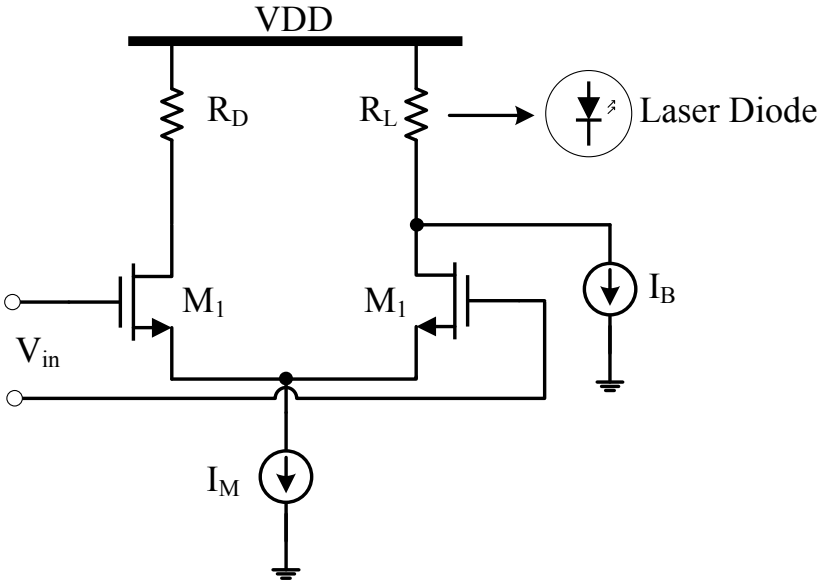

FIGURE 2.10: Simple laser diode driver circuit.

The output stage of most LDDs is based on the differential pair shown on figure 2.10. The differential pair steers the tail current I_M between the laser diode R_L and the dummy load R_D. To achieve full switching between R_L and R_D, the differential input voltage swing V_{in} must be large enough. V_{in} depends on the tail current and the transistor's size, to steer large I_M with a moderate voltage swing, wide transistors are required. This current steering approach has a number of advantages [41]:

1: The differential design has important advantages over single-ended design. First, it is less sensitive to common-mode noise and has better power supply rejection, to

achieve drivers with low jitter. Second, it averts the use of input reference voltage, thus avoids pulse-width distortion which results from the error in this reference voltage.

2: It provides constant power supply current, no matter a high or low logic value is transmitted. As a result, the power and ground bounces generated from parasitic inductance is minimized.

3: The current overshoots and variations which result from the charging of the parasitic capacitor across the tail current source is minimized, because the voltage across the tail current source is constant as it is defined by the input common mode voltage of the input devices.

2.2.2.2 Predriver

As explained previously, the input transistors of the output stage are made to be quite wide to be able to switch hundreds of milliamperes. As a result, the input capacitance of the output stage is large. An on-chip block, such as 50Ω input matching circuitry, may not be able to drive the output stage at the desired frequency. Furthermore, driving the output stage from off chip, may lead to unacceptable degradation of input mismatch parameter due to the large input capacitance of the output stage. Another concern is that the input voltage swing should be large enough to switch the output stage on and off. To solve this issue, a predriver is needed to drive the output stage. The predriver must have enough voltage gain to ensure sufficient voltage swing at the input of the output stage, to guarantee full switching operation. In addition, the prediver should be able to drive large capacitance while maintaining low input capacitance and low output resistance.

The desired voltage gain of the predriver can be achieved by multiple gain stages especially in short channel MOSFET technologies. For the predriver to be able to drive the large input capacitance of the output stage several broadband techniques are used and they are listed as follows [41]:

- Load reduction techniques
  - Intermediate stage buffers such as source followers and super source followers.
  - Negative capacitance such as negative Miller capacitance and negative impedance converter capacitor.
- Inductive techniques

  - Shunt inductive peaking.
  - Series peaking and T-coil network placed between stages of the predriver.
  - Distributed amplifiers.

- Feedback techniques
  - Series feedback such as source degeneration and f_T doubler.
  - Cascode transistor.
  - Shunt shunt feedback.

2.2.2.3 Back Termination

The laser diode is usually connected to the output stage with a transmission line. To avoid unwanted reflections from the load into the output stage, the characteristic impedance of the transmission line should match the impedance of the laser diode. To match the transmission line with a laser diode, which typically has a resistance of 5Ω, a 20Ω resistor is connected in series with the laser diode to match the diode with a 25Ω transmission line or a 45Ω resistor is connected in series with the laser diode to match the diode with a 50Ω transmission line.

For low supply voltage design, a transmission line with lower characteristic impedance is preferred since the power dissipation is lower. The best case from power perspective, is not to use transmission lines and matching resistors and connect the laser diode directly to the output stage.

Since the laser diode resistance is bias dependant, matching with a transmission line can't be guaranteed for all operating conditions, leading to undesired reflections. When these reflections propagate back to the output stage, they see a high impedance and propagate back unattenuated to the load. These reflections are called double reflections and may lead to degradation in the driver's jitter performance and extinction ratio. The problem of double reflections can be solved by using an output stage with back termination. There are two types of back termination: passive and active [41].

The concept of back termination is to create a low impedance node at the output stage, where the reflection from the laser diode is absorbed. In passive back termination this is done using a termination resistor, leading to higher power consumption due to the voltage drop over this resistor. This problem is solved in active back termination where under normal operation the voltage drop over the termination is zero and no power is dissipated in this resistor.

Chapter 3

State of the Art

3.1 Transimpedance Amplifiers

Despite the fact that there are many papers on TIAs in micron, submicron and nanometer CMOS technology. In this section only TIAs in submicron and nanometer CMOS technology are summarized.

TIAs using regulated cascode (RGC) topology as an input stage were previously reported in [35, 36, 42]. The RGC circuit, shown in figure 3.1, amplifies the input photo-current and converts it to voltage at the drain of M_1. The local feedback common source amplifier (M_2 and R_2) reduces the input impedance by the factor of its voltage gain, increasing the bandwidth.

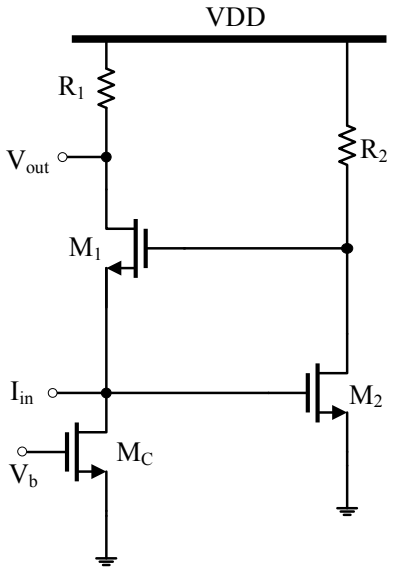

FIGURE 3.1: Regulated Cascode CMOS TIA.

The use of a local feedback also enhances the RGC's input transconductance, reducing the high frequency noise contribution related with the high input parasitic capacitance of the photodiode.

In [36], the proposed TIA with RGC input stage was implemented in 0.6μm digital CMOS technology. The TIA achieved a 58dBΩ and a -3dB bandwidth of 860MHz for 1pF photodiode parasitic capacitance. The measured average spectral noise density is 6.3 pA/$\sqrt{Hz}$ and sensitivity of -20dBm for a data rate of 1.25 Gb/s and a bit error rate of 10^{-12}. The chip consumes 17mA current and dissipates 85mW from 5V supply.

In [7], a pseudo differential TIA with a RGC input stage (M_1-M_4 and M_7-M_{10}) followed by a common source with a shunt feedback resistor (M_5, M_{11}, R_1, R_2, R_{1f}, R_{2f}, L_1 and L_2) was presented. The input common mode voltage of the shunt feedback common source amplifier is set (V_{set}) by local feedback amplifier as shown in figure 3.2. To enhance the bandwidth of the TIA, a three dimensional (3-D) transformer is used. The 3-D transformer is formed of an inductor pair (L_1-L_2) with an inductance of 2.85nH each. The quality factor of the 3-D transformer is 4.5 at 7 GHz. As a result of the use of 3-D transformer, the TIA consumes a chip area of 330μm $\times$ 550μm. The front-end is implemented in 0.18 μm CMOS technology. It provides a conversion gain of 87dBΩ and a -3dB bandwidth of 7.6 GHz. The measured sensitivity is -12dBm at a data rate of 10 Gb/s and a bit error rate of 10^{-12}. The chip dissipates 210mW from 1.8V supply.

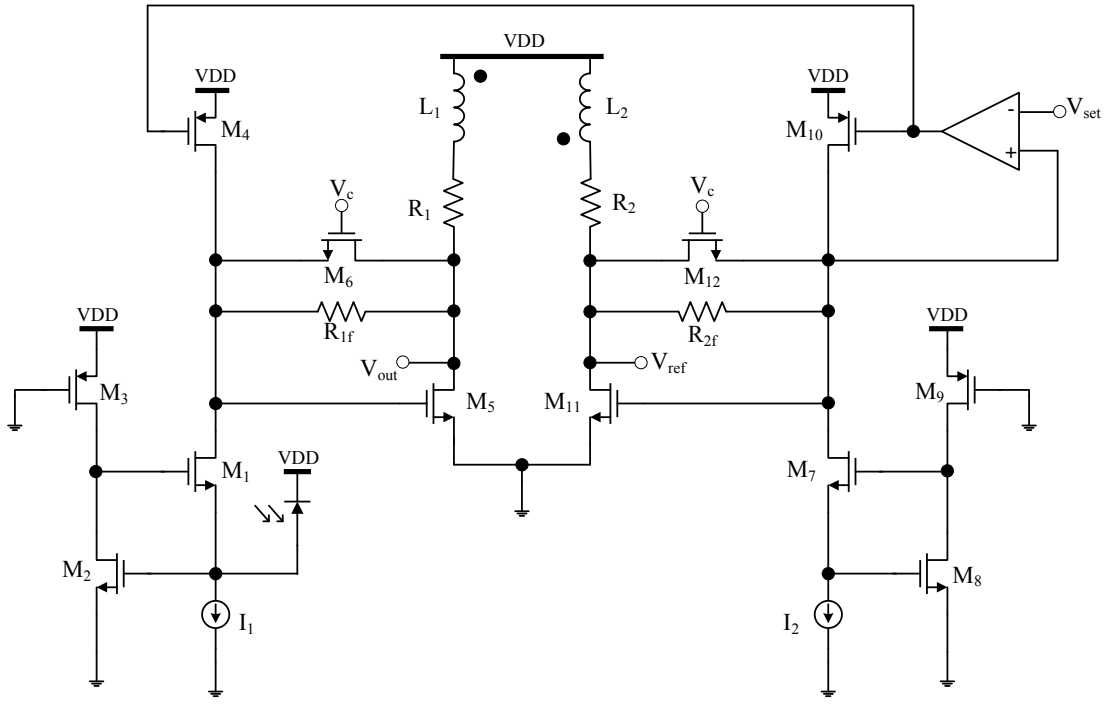

FIGURE 3.2: The pseudo differential TIA with a RGC input stage proposed in [7].

A common gate feedback TIA was introduced in [19]. The TIA shown in figure 3.3 is a modified version of the conventional RGC TIA shown in figure 3.1. The modification is the insertion of M_3. M_3 acts a level shifter. The use of this concept allows the gate voltage of M_2 to be as low as one transistor V_{GS} instead of two transistor gate-source voltages as in RGC TIA. The feedforward technique increases the input transconductance and reduces the input impedance of this topology resulting in bandwidth increase. As shown in figure 3.3, three spiral inductors are used to further enhance the bandwidth. Each inductor is 2.2nH, with eight turns and occupies a chip area of 18μm×18μm. The TIA is implemented in 80nm digital CMOS technology. The measured transimpedance gain of the TIA is 52dBΩ and -3dB bandwidth of 13.4 GHz for a photodiode capacitance of 320fF. The measured input referred noise current spectral density is 28 pA/$\sqrt{Hz}$ at 3 GHz and sensitivity of -8 dBm for a bit error rate of 10^{-12} at a data rate of 20 Gb/s. The TIA dissipates 2.2mW from 1V supply.

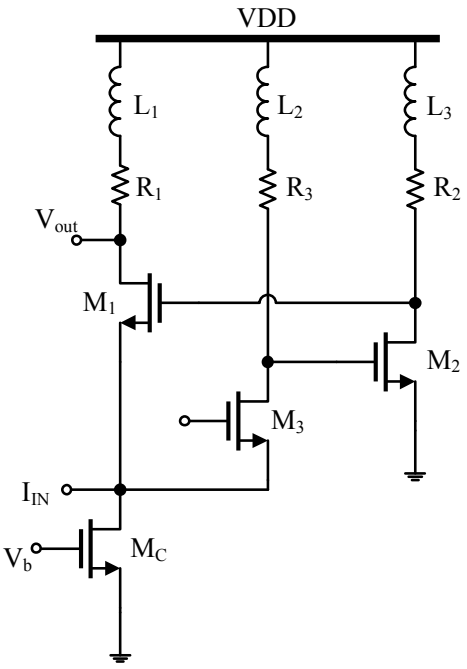

FIGURE 3.3: Common gate feedback TIA presented in [19].

In [25], a feedback common gate (CG) TIA was introduced. As shown in figure 3.4, the CG stage is followed by an amplifying stage and R_F connected between the output and the source of M_1 forming a negative feedback. Although, the feedback formed by R_F decreases the input resistance, it increases the input referred noise current. It was mathematically proven in [25] that the presented topology can achieve a lower input resistance than a conventional CG TIA without increasing the input referred noise current, if $A > 1$ and $R_F > MR_1/(M-1)$ where M is the scaling factor of the transistor width of M_1 and the biasing current I_b. The TIA was implemented in 90nm digital CMOS technology and it was designed for 40 Gb/s application.

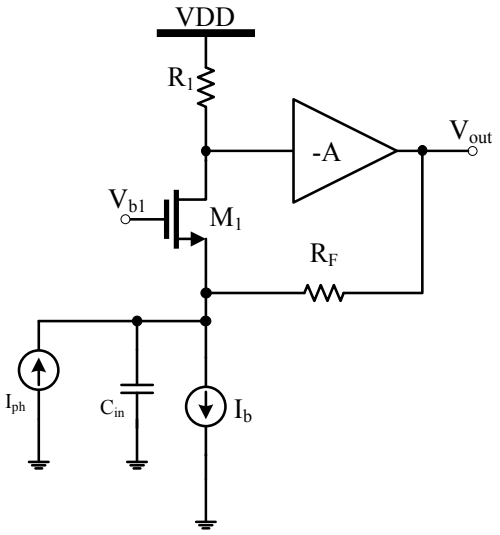

FIGURE 3.4: A feedback common gate (CG) TIA introduced in [25].

In [12], a gain reuse RGC compensation was introduced. Figure 3.5 shows the proposed topology. The main concept of this topology is to reuse the amplified voltage at the drain of M_1-M_2 and feeding it back through a source follower M_3-M_4. The cross coupled connection from the source of M_3 to M_2 and M_4 to M_1 maintain the negative feedback. This technique makes the TIA less sensitive to C_{in} and achieve a higher gain bandwidth while sacrificing a minor reduction in transimpedance gain. The TIA was fabricated in 130nm CMOS technology. This design achieved a transimpedance gain of 400Ω and a -3dB bandwidth of 2.8GHz for an input capacitance of 2pF. The TIA consumes 8mA from 1.8V supply.

The novel [26] shows the design mechanism of current mode TIA with active feedback. The TIA is shown in figure 3.6. The input transistor M_1 is in a common gate configuration and the active feedback transistor is a PMOS transistor in a common source configuration. This topology have the same input impedance as the RGC TIA. The presented TIA broadens the bandwidth on the expense of transimpedance gain. Therefore, it is desirable to use large R_1, small M_1 and small M_2 to maximize the gain. Moreover, M_2's channel thermal noise adds directly to the input referred noise current. Therefore, it is desired to keep the width of M_2 small. The TIA is followed by two capacitively degenerated common source voltage amplifiers to achieve high gain. An input series spiral inductor is used for bandwidth extension. The chip is fabricated in 180nm CMOS process. The overall measured transimpedance gain is 55dBΩ and a -3dB bandwidth of 7 GHz for a total input parasitic capacitance of 300fF. The measured average input referred noise current is 17.5pA/$\sqrt{Hz}$ up to 7 GHz. In addition, the measured group delay until 7 GHz is 65±10 ps. The chip dissipates 18.5 mW from a single 1.8V supply.

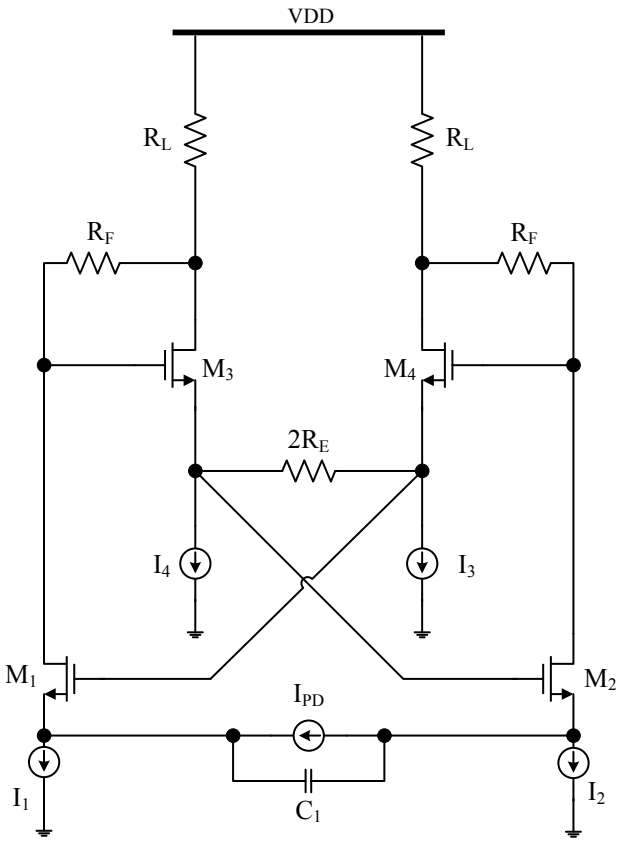

FIGURE 3.5: A RGC TIA with gain reuse introduced in [12].

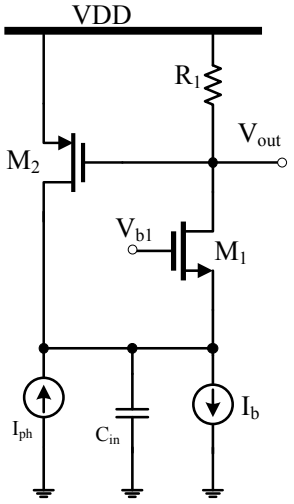

FIGURE 3.6: A current mode TIA with active feedback [26].

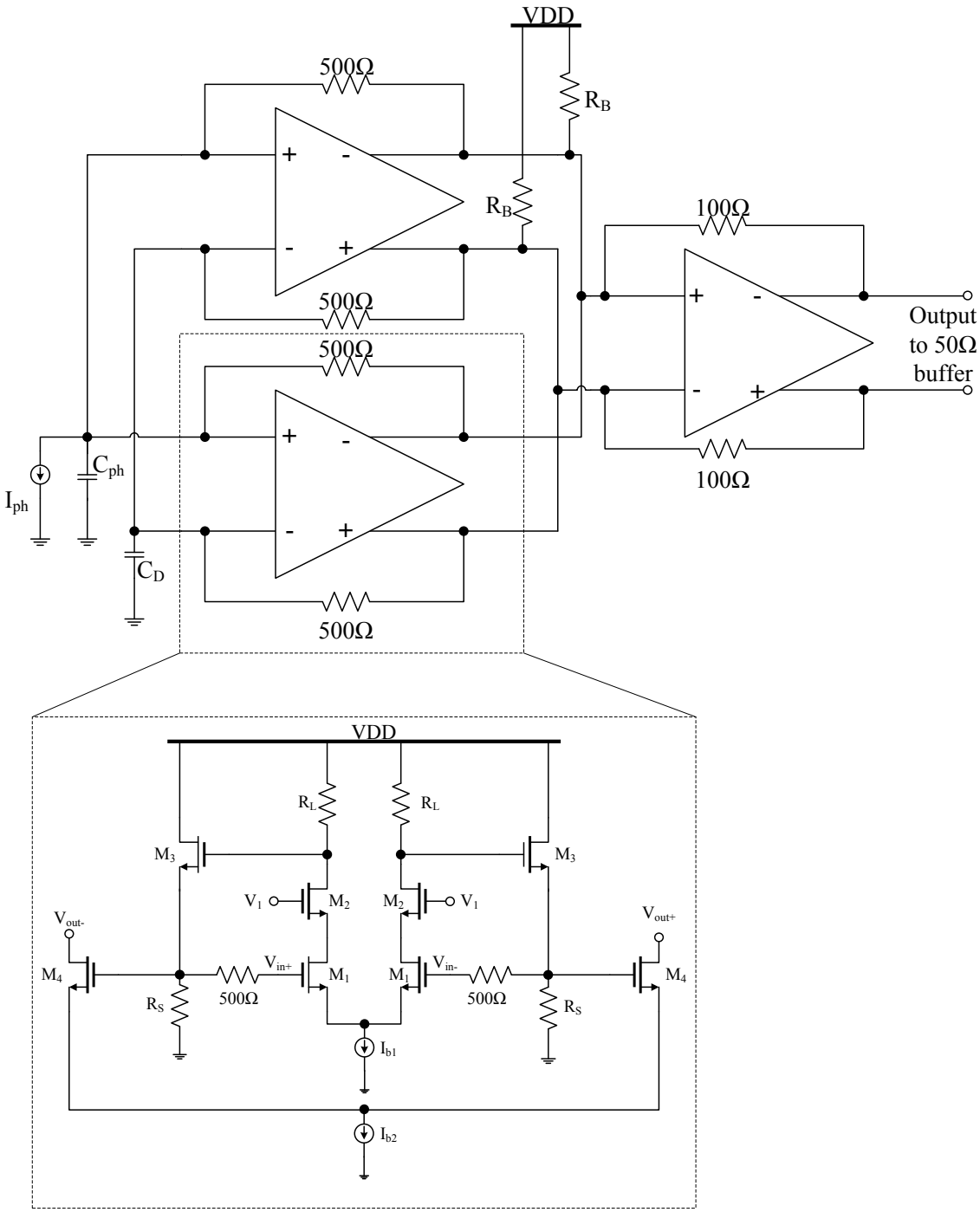

FIGURE 3.7: TIA in parallel configuration for bandwidth enhancement [31].

A different bandwidth enhancement techniques was proposed in [31]. The presented technique requires no inductors, it is based on the use of N (in this case it is 2) similar TIAs connected in parallel configuration, as shown in figure 3.7. In this technique, each single TIA experience smaller input capacitance (C_{ph}/N) resulting in bandwidth enhancement without changing the transimpedance gain of a single TIA. The circuit implementation of the feedback TIA is shown in figure 3.7, the input amplifier is a cascode differential amplifier (M_1, M_2 and R_L) followed by a source follower (M_3 and R_s) and the output of the two TIAs are summed by a common source buffer (M_4 and R_B). The parallel TIAs are followed by another TIA to convert the summed currents of the parallel TIAs. The chip is implemented in 130nm digital CMOS process. The measured transimpedance gain is 62 dBΩ and bandwidth of 6 GHz for an input parasitic capacitance of 250fF. The measured minimum detectable input current is 22.4 μA and it dissipates 98mW ($N = 2$) from a 2V supply.

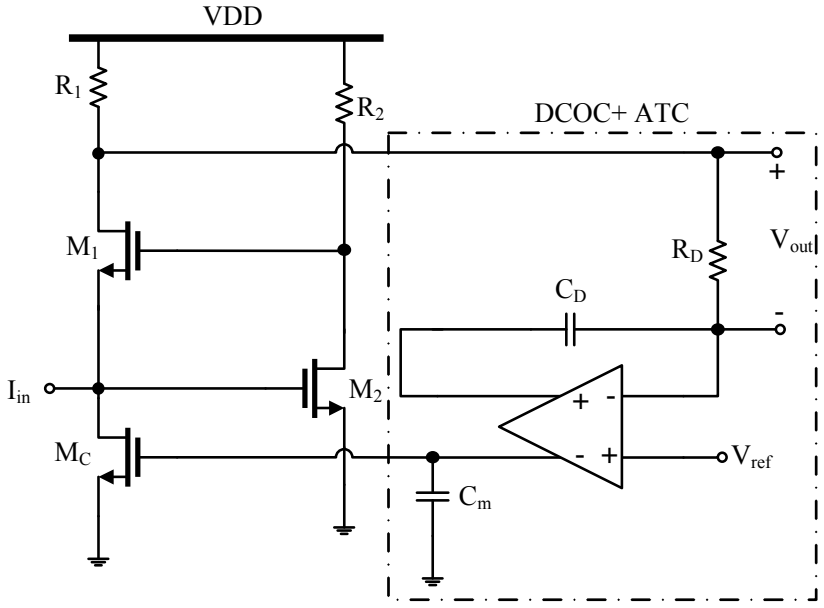

FIGURE 3.8: The low power RGC TIA present in [1].

A RGC TIA with low power and area efficient method of single to differential signal conversion is proposed in [1]. The method is based on sharing the passive components for DC offset canceller (DCOC) and autothreshold controller (ATC) at the TIA as shown in figure 3.8. The DCOC is implemented with a non-inverting integrator connected between input and output forming a negative feedback as shown in figure 3.8. C_D and R_D of the integrator also act as ATC saving area and power. The TIA was fabricated in 65nm CMOS. The measured transimpedance gain of the TIA and the limiting amplifier is 75.6 dBΩ and the data rate achieved is 6Gb/s for 300fF input capacitance. The achieved sensitivity is -3.8dBm at a BER of 10^{-11}. The chip dissipates 2.86mW from 1.1V supply.

3.2 Laser Diode Drivers

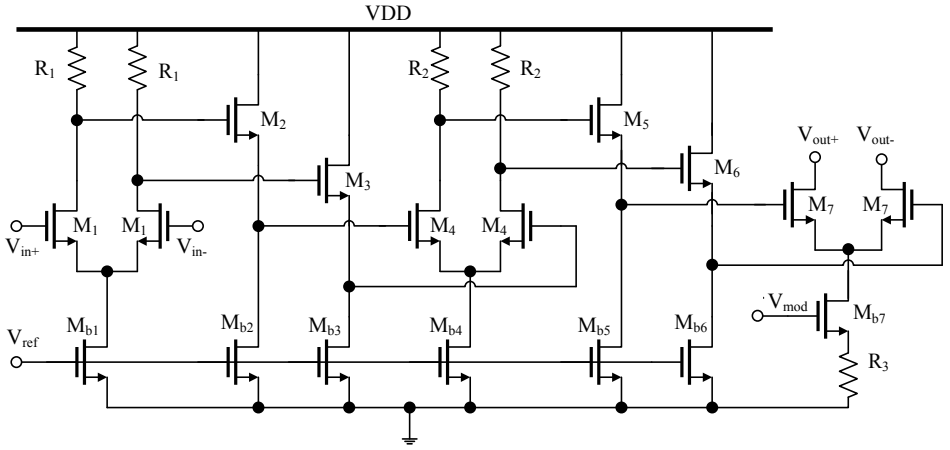

FIGURE 3.9: Laser diode driver (LDD) proposed in [47].

The laser diode driver (LDD) proposed in [47] consists of 3 stages as shown in figure 3.9. The output stage (M_7, M_{b7} and R_3) is an open drain topology where the laser diode is connected externally to the drain of M_7. R_3 and M_{b7} act as the tail current source which define the modulation current of the LDD. This stage offers the modulation current and enough voltage swing to the laser diode. The two differential pairs (M_1, M_{b1}, R_1, M_4, M_{b4} and R_2) are voltage gain stages to provide enough voltage swing to the input of the output stage. The purpose of the source followers (M_2, M_{b2}, M_3, M_{b3},M_5, M_{b5}, M_6 and M_{b6}) is to avoid the loading effect of the large gate width of the input transistor of the differential pairs. The presented LDD is realized in 0.35μm CMOS technology achieving a data rate of 2.5 Gb/s. The maximum output current provided is 60mA with a 200mV voltage swing peak to peak. The power consumption is 500mW from a 5V supply. The amplifying stages including the source followers are consuming 45mA and dissipating 225mW from a 5V supply.

Figure 3.10 shows the output stage of LDD presented in [6]. The driver is a simple differential pair (M_1) with a tail current source defining the modulation current (I_{mod}). The laser diode (LD) and resistor are connected externally. The biasing current of the LD is defined by a DAC (not shown for simplicity). This paper enhances the switching speed of the LDD by using active inductive peaking and pre-emphasis techniques. The pre-emphasis circuit (PAC) (M_5, M_6, M_7 and M_8) provides more current to the LD at every transition edge of the input data enhancing the switching speed of the LDD. The PAC needs a delay cell which is realized by a differential pair (M_2) with an active inductive load (M_3 and M_4). The proposed LDD is implemented in 0.35μm digital CMOS technology. It achieves a data rate of 2.5 Gb/s and modulation current of 20mA with power dissipation of 150mW from a 3V supply and area of 1200μm $\times$ 900 μm.

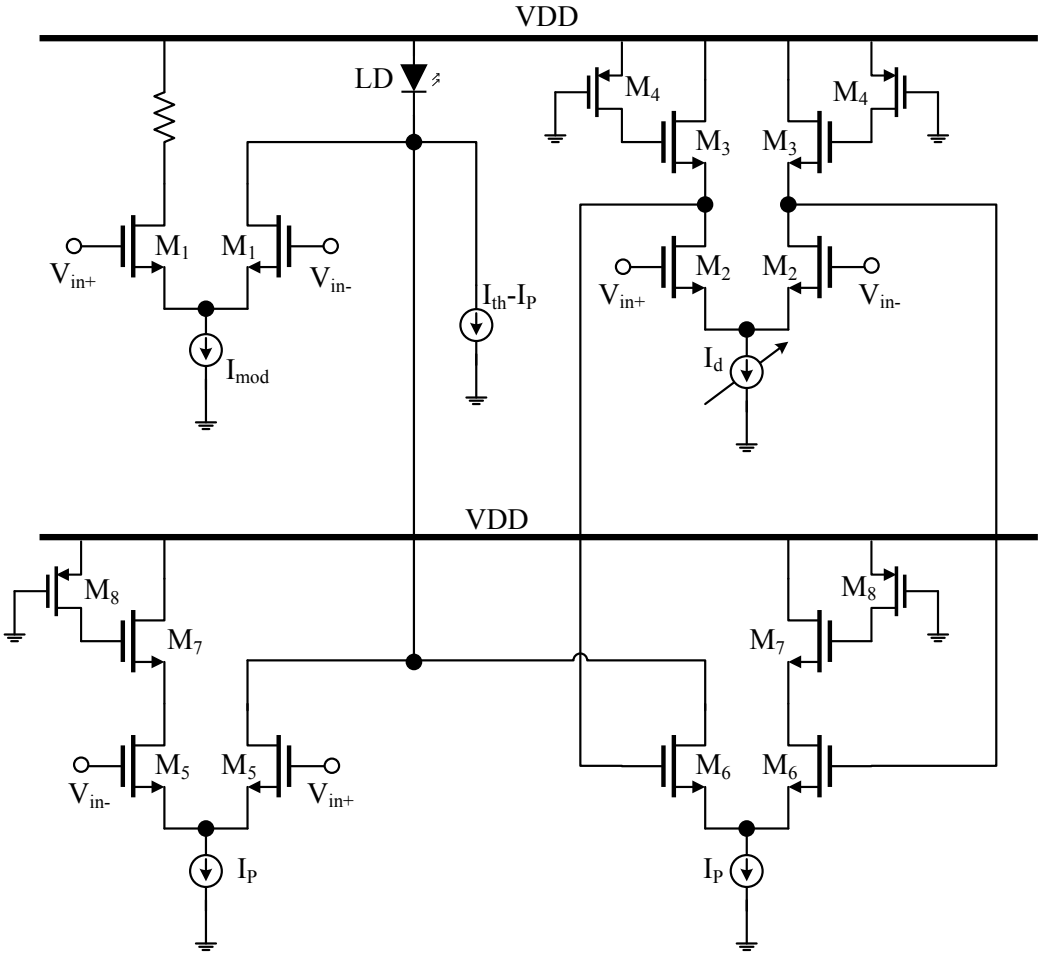

FIGURE 3.10: LDD using active inductive peaking and pre-emphasis techniques in [6].

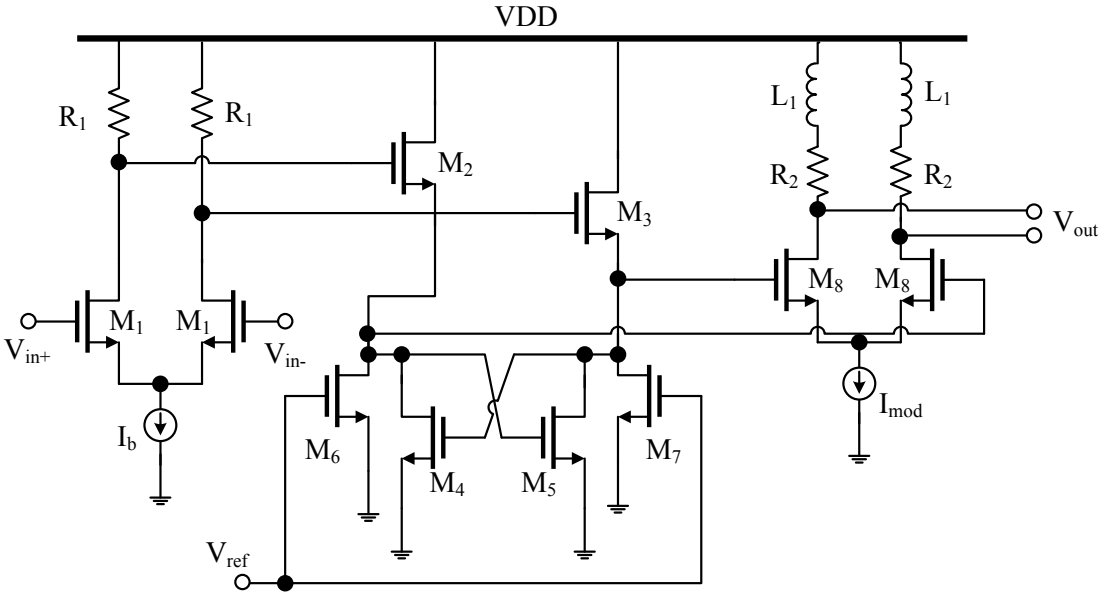

FIGURE 3.11: LDD with a push-pull source follower preamplifier proposed in [24].

The LDD introduced in [24] is shown in figure 3.11. The LDD consists of a pre-amplifier and output driver. The preamplifier is a differential pair (M_1, R_1) followed by a quasi push-pull source follower (M_2, M_3, M_4, M_5, M_6 and M_7). A quasi push-pull source follower is a classical source follower with two cross-coupled pairs This topology is used to avoid the asymmetric rise and fall edge of the signal caused by the classical source follower. The output driver is a simple differential pair (M_8) connected externally to an inductor and resistor to establish DC circuitry. The LDD was implemented in 0.35μm CMOS process. The achieved data rate is 5Gb/s with maximum peak to peak voltage(V_{p-p}) of 4.2V_{p-p} under 3.3V supply and 6.2V_{p-p} under 5V supply. The chip dissipates 310mW and 945mW from 3.3V and 5V supply voltage, respectively. The chip area is 0.57mm^2.

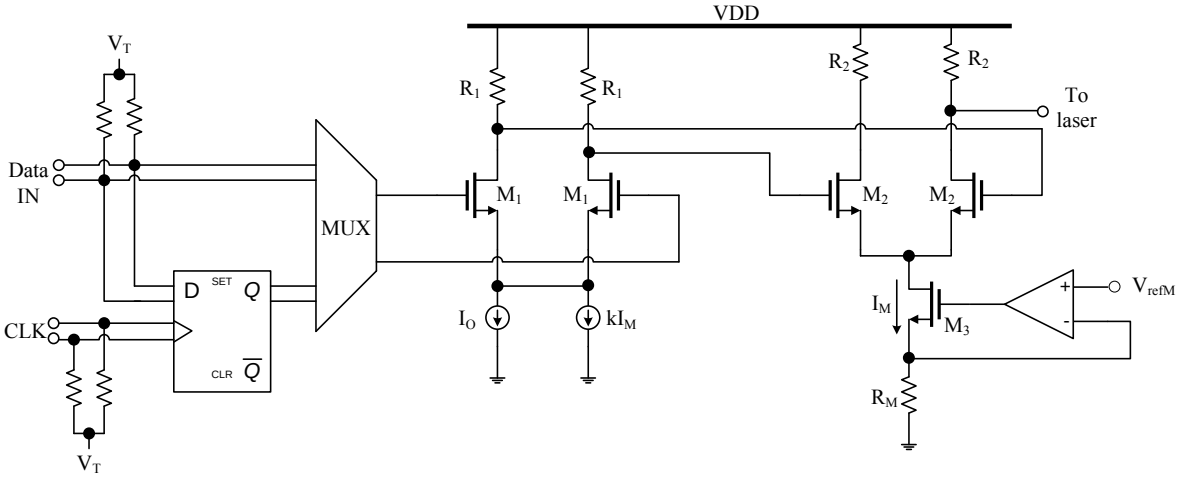

FIGURE 3.12: The proposed LDD architecture in [11].

The LDD presented in [11] is shown in figure 3.12. The proposed LDD includes data retiming control, waveform shaping control and output driver. The LDD's input stage include a 50Ω single to differential converter for both the clock (CLK) and the data inputs, a master slave flip flop for retiming control, a 2 to 1 multiplexer, a waveform shaping control with a tail current source proportional to the modulation current (I_M) at the buffer stage and the output stage is a differential pair for providing I_M to the laser diode. The purpose of the offset current I_O is to increase the linearity of the buffer. The LDD is implemented in 0.25μm CMOS technology. It operates at a 3.8 Gb/s data rate and supports a maximum modulation current of 60mA. The chip consumes 37mA excluding the modulation and biasing current of the LD from 2/3.3V supply. The chip including pads is 1.2mm × 1mm.

The LDD architecture proposed in [23] is shown in figure 3.13. The LDD as shown in the left hand side of the figure is formed of 3 identical slices connected in parallel. Each slice contains a pre-amplifier and output driver. The preamplifier (M_1, L_s, L_1, L_2 and R_1) is a differential pair with three techniques to improve the bandwidth: Negative impedance

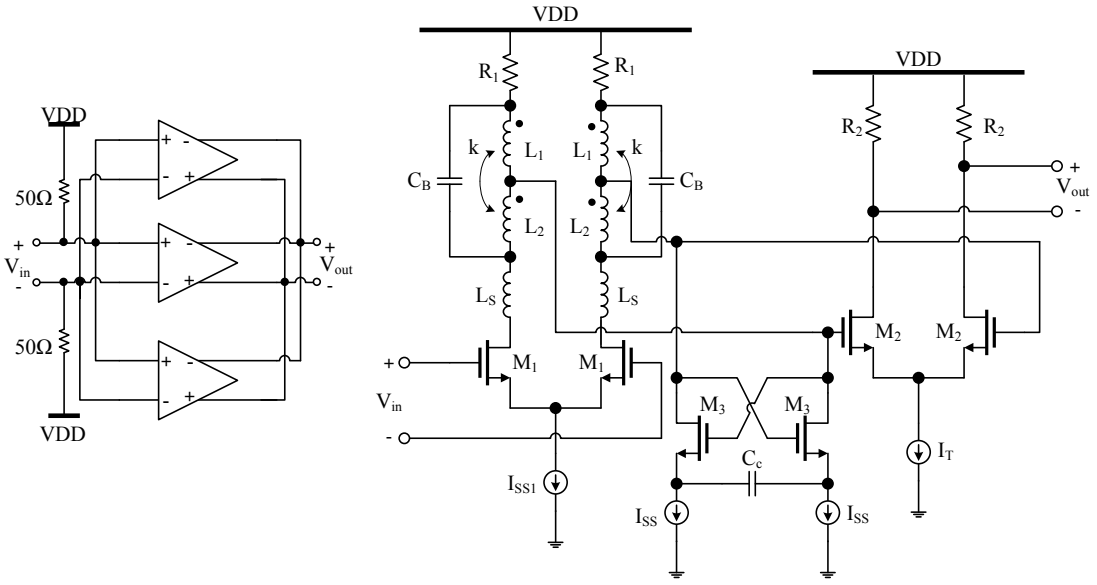

FIGURE 3.13: 10Gb/s LDD presented in [23].

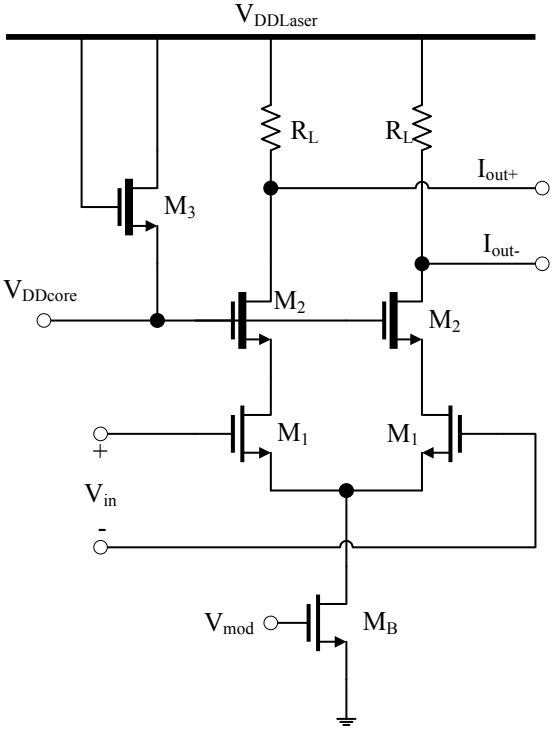

FIGURE 3.14: LDD output stage with thick oxide cascode transistors shown in [28].

converter (M_3 and C_c) transforming C_c to a negative capacitance between the input nodes of the output driver, T-coil (L_1, L_2 and C_B) and series (L_s) inductive peaking. The T-coil is designed to be 3nH and the series inductors is 1.75nH. These techniques are used to overcome the bandwidth reduction caused by the large input capacitance of the output driver. The output driver is a simple differential pair with a resistive load of 25 Ω. The whole LDD is fabricated in 180nm CMOS technology. The LDD is operating at 10Gb/s with a modulation current of 100mA. The whole chip dissipates a 675mW from a single supply of 1.8V. The LDD occupies a 0.9mm × 1.8mm.

In [28], a LDD for high energy physics was introduced. The system design of the LDD is a classical system including 50Ω input stage, buffer stage, pre-driver, emphasis circuit and output stage. The output stage shown in figure 3.14 is a cascoded differential pair with a resistive load. The load resistance in this case is 50 Ω for correct termination. As shown in figure 3.14 the cascode transistor (M_2) are thick oxide, 2.5V compatible NMOS transistors have been used to protect the input core transistors (M_1) from the high voltage supply of the laser diode. All the transistors are NMOS to maximize the speed. Triple-well transistors are used to reduce the threshold voltage and hence decrease the size of the transistor. This approach allows better shielding between the different blocks. The proposed LDD is implemented 130nm CMOS technology. The circuit achieves a 5Gb/s data rate and provides a modulation current up to 24mA and bias current of 43mA. The whole chip is supplied by a 2.5V supply voltage.

Chapter 4

CMOS Technology

System on Chip (SoC) is a concept to integrate all relevant components of a system on a single chip, to achieve a small-sized, energy saving and competitive system in order to improve sales volume. Although SoC is a highly integrated system, it isn't a simple combination of digital, analog and mixed signal blocks. The integration into a SoC associates innovative techniques to achieve a system trade off between cost efficiency, area and power consumption [40].

The process technology used in a SoC design has the main cost impact. Therefore, the use of a cheap process technology is essential to have a cost efficient design. The cheapest available technology is deep submicron CMOS technology [8]. Although SoC is mainly dominated by the digital part, the small analog part has a crucial performance determining role. Input/output ports, analog-to-digital converters (ADC), digital-to-analog converters (DAC), sensor readouts and radio frequency (RF) front-end are all analog circuits. To enhance analog circuit design in CMOS technology additional processing steps are available, but these steps are expensive. Therefore, standard CMOS technology is widely used.

4.1 Scaling in CMOS Technology

4.1.1 Constant Electric Field Theory

The CMOS technology undergoes a consistent progress reducing structure sizes, which is called scaling. The strategy in scaling is decreasing the physical dimensions of the device while keeping the electrical field in the channel of the MOSFET constant [10]. The channel length (L), channel width (W) and the gate oxide thickness (t_{ox}) are scaled by a shrinking factor SF. This results in the scaling of the device area by a factor of

SF^2 and the parasitic capacitance by a factor SF. To keep the electrical field constant, the supply voltage, the threshold voltage and the channel doping are scaled down by SF. This scaling technique results in the improvement of the speed of the technology and reduction in chip area. Despite the improvement associated with scaling, it brings difficulties.

Supply and threshold voltage In digital circuits, the dynamic power consumption is the outcome of the current consumption during the switching activity and charging the load capacitance. Therefore, scaling down the supply voltage saves dynamic power consumption of the circuitry [4]. To keep the electric field in the channel constant, the threshold voltage is scaled down with the same factor. Lowering the threshold voltage leads to an increase in the leakage current during the off-mode of the transistor resulting in the increase of the static power consumption.

Gate oxide thickness The gate thickness is also scaled down with the same factor of the supply and threshold voltage to keep the electric field constant [13]. The gate leakage current increases exponentially with the decreasing gate thickness and the tunnelling current may damage the gate oxide.

Short channel effects Short channel transistors are fast transistors because the time taken for charge to move from the source to drain is shorter. However, there are many disadvantages associated with this type of transistors:

- In the case of gate source voltage is lower than the threshold voltage, current flows from the drain to source. This current is a result of punch-through and drain induced barrier lowering (DIBL). This current is called the sub-threshold current[13].
- In the pinch off regions, the electric field is high leading to electron-hole pair generation due to impact ionization. The electrons drift to the drain and the holes drift to the substrate resulting in substrate current, raising the potential of the substrate and hence decreasing the threshold voltage, which leads to a rise in the channel current [48].
- Electron mobility is reduced because of surface scattering [16].
- The mobility of the carriers of the transistor in saturation is lowered by the velocity saturation [34].
- Electrons in high electric fields are called hot electrons. These electrons drift to the gate oxide and charge it, resulting in the degradation of the performance and lifetime of the transistor [33].

Channel doping However, increasing the channel doping of the transistor reduces the short channel effects. It results in lower carrier mobility and increases the probability of band-to-band tunnelling [13].

4.1.2 Nanometer CMOS Scaling

In nanometer CMOS technology, the scaling strategy is different from constant field strategy because of many parasitic effects and drawbacks. The scaling of gate length, gate oxide thickness and source-drain junction are the main parameters that effect the transistor's performance [5]. The scaling of these parameters has a direct effect on the reliability, power consumption and performance of the device.

Reliability Scaling of the gate dielectric has a major effort on the reliability of the device and leads to some stress effects [22], such as

- Electromigration.
- Hot carrier injection.
- Time-dependent gate insulator breakdown.
- Negative bias temperature instability in PMOS device.

Power Consumption Scaling down the power supply voltage is a direct method to minimize the power consumption, since the sub-threshold current and gate leakage current are power supply voltage dependent [5]. Reducing the power supply voltage is limited by the threshold voltage of the transistor. Low threshold voltage transistors lead to increase in the subthreshold current resulting in the increase of the static power consumption. Therefore the threshold voltage is not scaled down by SF. To maintain the speed advantages of nanometer CMOS technology the supply voltage is also not scaled by the SF. Technology with multi threshold voltages are used for power and performance optimization. Thin, regular and thick gate oxide transistors are available to meet different design specification. The disadvantage of multi threshold technology is the need of additional masks for chip fabrication [18].

Performance Enhancement The enhancement of the speed of the transistor has been degraded during the down scaling of CMOS technology. The main reasons behind this degradation are the short channel effects, which don't scale down. In digital circuits the performance depends mainly on the capacitance and saturation current of the device. Previously, the saturation current was maximized by scaling the threshold voltage and the oxide thickness. Since this scaling scheme results in

the increase of the leakage current, this method is not possible any more [18]. Nowadays, the saturation current is increased by silicon on insulator, strained silicon techniques, channel oriented design and High-K dielectric gates. These techniques improve the device performance without scaling the gate oxide thickness. Another performance factor is the capacitance. The gate and overlap capacitance decrease with scaling. On the other hand, the gate-to-contact and the fringing capacitances, don't scale down, having a significant impact on the total parasitic capacitance [5].

4.2 Challenges of Nanometer CMOS Technology in Analog Circuits

Transistor's Gain and Speed The main benefit from scaling in digital circuits is to enhance the speed and increase the integration level. Analog circuits also benefit from the increase in speed. Scaling reduces the parasitic capacitance resulting in the increase in the transit frequency of the transistor and the maximum oscillation frequency. The intrinsic gain and transistor's speed are in direct contradiction. CMOS transistors with nanometer gate channel length suffer from low output resistance leading to low intrinsic gain. Intrinsic gain can be improved by operating in moderate inversion. However, operation in moderate inversion leads to significant drop in the transit frequency and maximum oscillation frequency of the transistor [29].

Supply Voltage and Headroom Supply voltage is scaled down in digital circuits to reduce power consumption and increase logic speed. In analog circuits, scaling down supply voltage results in a limited signal swing and headroom. At constant power consumption, the performance of analog circuits deteriorates significantly [2, 29]. By scaling down the supply voltage power consumption has to be increased to maintain constant circuit performance. As the supply voltage approaches the threshold voltage, the power consumption increase becomes more relevant to achieve constant circuit performance. However, the use of low threshold devices reduces the power consumption in analog circuitry, it increases the power consumption of digital circuitry due to the subthreshold current. The limited signal swing and headroom demand new analog circuits to achieve low noise performance to maintain suitable signal-to-noise ratio (SNR) and dynamic range.

1/f Noise The source of 1/f noise is the fluctuation of the mobility of the carriers in the channel and the variation of the total number of the carriers [21]. 1/f noise obtains increasing observance in nanometer CMOS technology because it is inversely

proportional to the gate area, as shown in the following expression [43],

$$\overline{dv^2} = \frac{K_F}{WLC_{OX}^2}\frac{df}{f}, \tag{4.1}$$

where K_F is a technology independent parameter. W and L are the gate width and length, respectively. C_{OX} is the gate oxide capacitance.

Matching Analog circuits depend mainly on differential topologies. Therefore, matching is an important criterion. The precision of the manufacturing process effects the matching of the threshold voltage, transconductance and saturation current. In nanometer CMOS technology, additional factors become important. Voltage matching, which is the difference of threshold voltage between two similar transistors, becomes less sensitive to the transistor dimensions, when the transistor scales down. Matching is usually improved by using larger devices [22].

Linearity Due to the down scaling of the supply voltage the voltage swing and headroom result in degradation of the linearity. In addition, the distortion increases in nanometer CMOS transistors due to the increased influence of the series resistance and velocity saturation, further worsening the linearity [46].

Gate Leakage Current In nanometer CMOS technology, gate leakage current has a significant effect in analog circuit design. Gate leakage current depends on the gate oxide thickness, the gate-source voltage, the gate-drain voltage and the gate area [22]. The gate leakage current affects the gate leakage mismatch, input biasing current and the shot noise resulting from the gate current. To reduce the gate leakage current High-K dielectrics are used as the gate dielectric material [29].

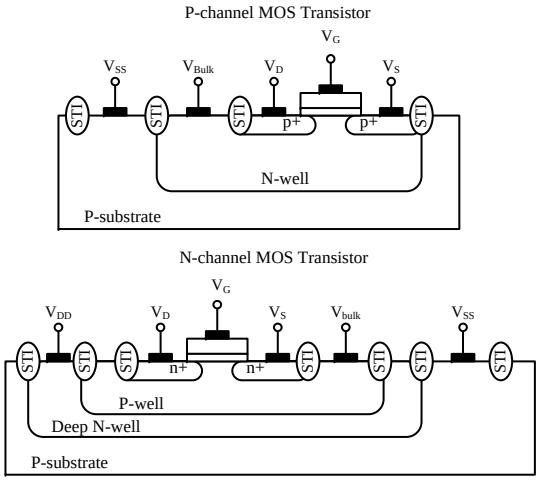

FIGURE 4.1: Cross section of NMOS and PMOS transistors in 40nm triple well technology.

4.3 40nm CMOS Technology

40nm CMOS technology is developed for SRAM, digital logic, mixed-signal, multi voltage applications and I/O applications. 40nm CMOS technology is shrunk by 90% to have a minimum feature size of 36nm. It is a low power process with multi-threshold voltage technology: low, regular and high threshold voltages. The technology has three gate oxide thicknesses to support three different supply voltages 1.1V, 1.8V and 2.5V.

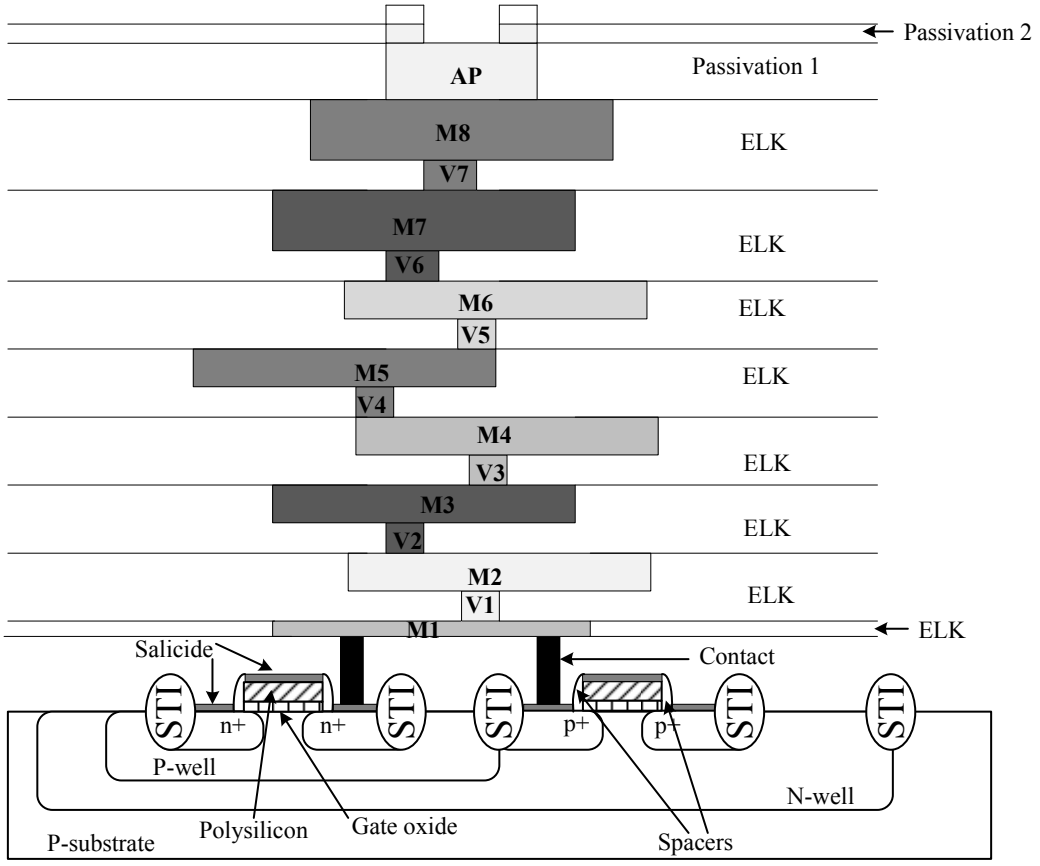

FIGURE 4.2: Cross section of low power 40nm CMOS technology.

In the circuits presented in this thesis only low power 40nm CMOS technology is used, thus only the characteristics of the devices belonging to this technology are highlighted. The 40nm CMOS technology is a triple well process on a p-substrate. The NMOS transistor is located in an isolated P-well and the PMOS is placed in an isolated N-well. Cross section of the transistors are shown in figure 4.1. PMOS and NMOS transistors are separated by a shallow trench isolation (STI).

The core supply voltage of 40nm CMOS technology is 1.1V and it can sustain up to 1.21V. The cross section of the low power 40nm CMOS technology is shown in figure 4.2. The process uses triple P-well on a N-well within the P-substrate. n+ and p+ diffusion

regions are inside the wells. Spacers ensure the isolation of the gate from the drain\source regions. Salicide (self-aligned silicide) are used to connect the semiconductor to metal layers. As shown in figure 4.2, the process has 8-metal layers. The layer AP is a thick Aluminium layer used mainly for input\output pads.

4.3.1 MOSFET Transfer Characteristics

The output transfer characteristics of an NMOS device in 40nm CMOS technology is shown in figure 4.3. The transistor's width was set to be 960nm and the applied gate source voltage is 550mV. The early voltage decreases with increasing gate length and is in the range of hundreds of milli-volts, because the short channel effects decreases with increasing gate length. The early voltage at gate length L=40nm is about 0.4V. As shown in figure 4.3, for constant transistor width, the drain current increases with decreasing gate length at high v_{ds} values. For low v_{ds}, the drain current doesn't behave as expected because of the threshold voltage roll-off which results from the short channel effects causing an increase in the threshold voltage.

Figure 4.4 presents the behaviour of the transconductance of an NMOS device for different gate lengths. The transistor's transconductance increases with decreasing gate length. The transistor's output resistance is equal to the reciprocal of the output transconductance of the transistor. The NMOS's output resistance increases with larger gate length, as depicted in figure 4.5, because the transistor's output transconductance increases with smaller gate length.

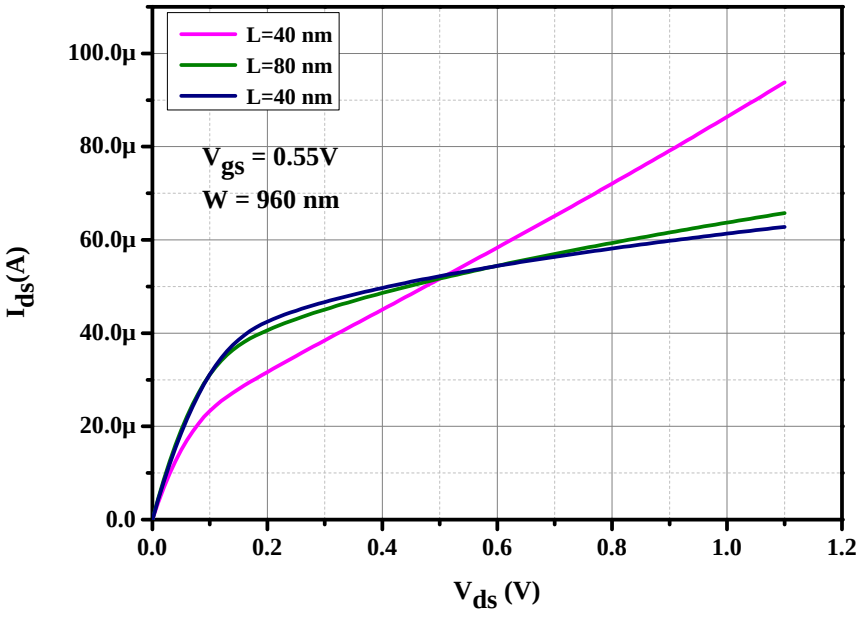

FIGURE 4.3: NMOS output transfer characteristics for various gate length L.

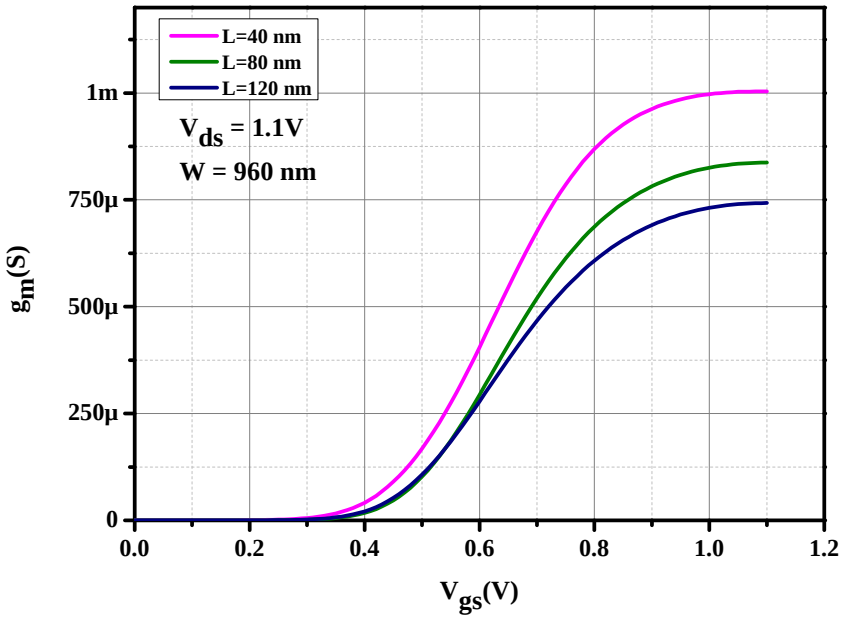

FIGURE 4.4: NMOS transconductance g_m for various gate length L.

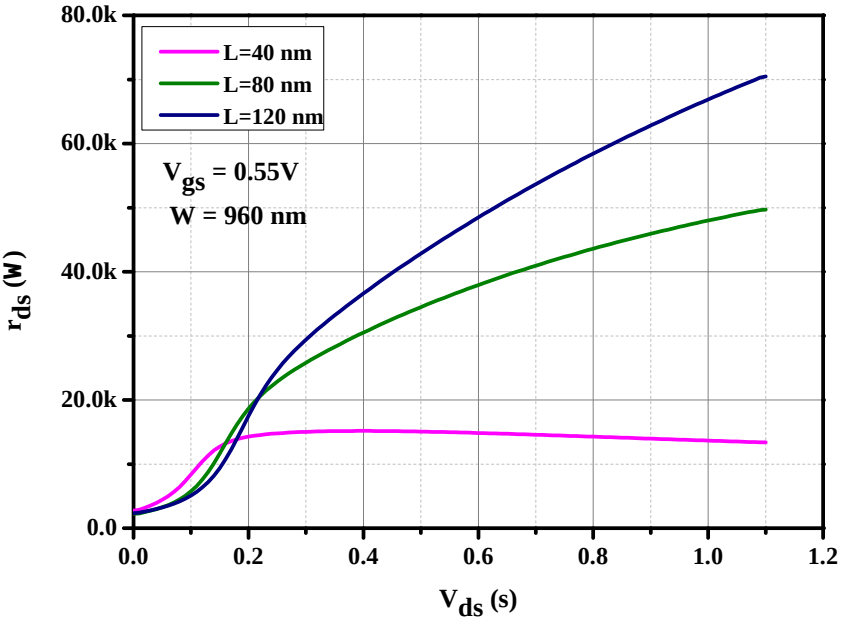

FIGURE 4.5: NMOS output resistance R_{ds} for various gate length L.

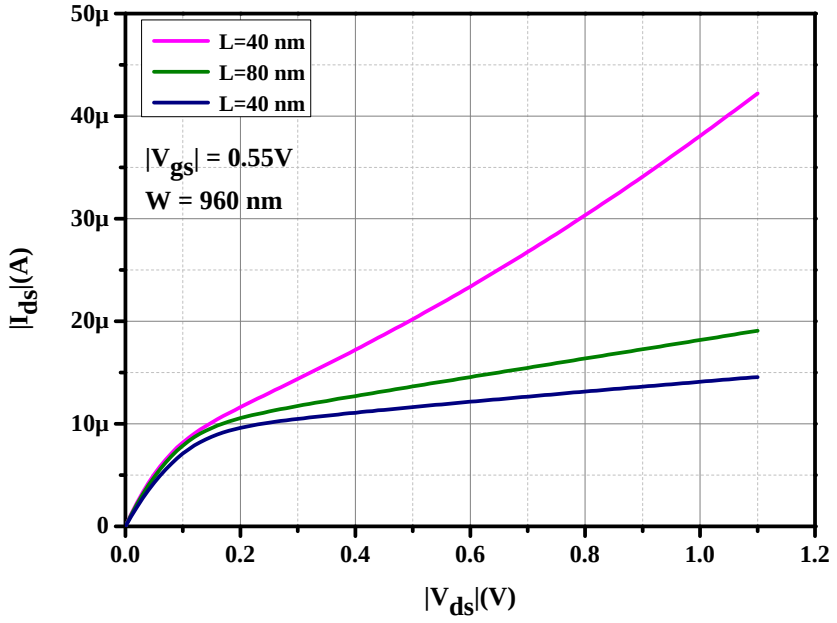

FIGURE 4.6: PMOS output transfer characteristics for various gate length L.

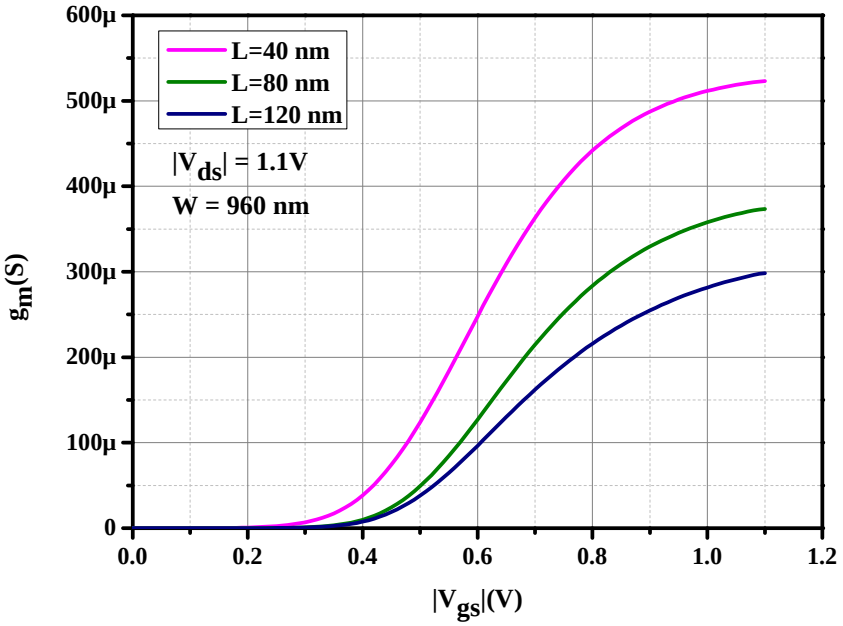

FIGURE 4.7: PMOS transconductance g_m for various gate length L.

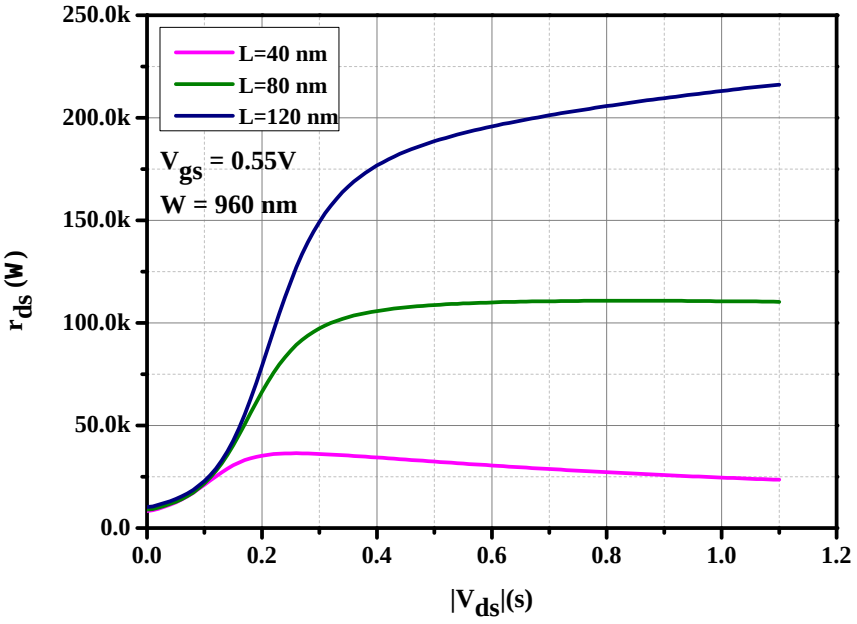

FIGURE 4.8: PMOS output resistance R_{ds} for various gate length L.

Figure 4.6 shows the transfer characteristics of a PMOS device in 40nm CMOS technology. The Early voltage of a PMOS transistor for L=40nm is about 0.2V. Figures 4.7 and 4.8 depict the behaviour of the transconductance and output resistance, receptively, for different gate lengths. They obey the same explanations as their NMOS counterpart.

Chapter 5

Realization of Optoelectronic Circuits

In this chapter, different types of integrated optoelectronic circuits will be presented. It will include implementation of three different topologies of high speed TIAs and a high voltage LDD. These implementations will be explained in details and the special feature of each implementation will be highlighted. For each implementation, the simulation and experimental results will be shown and discussed.

5.1 Transimpedance Amplifiers

5.1.1 Push Pull Current Mirror TIA

5.1.1.1 PPCM Theory

Current mode TIAs are implemented either using current buffers such as CG, RGC or feedback current amplifiers. The current amplifier senses the input current with low input resistance and amplifies it at a high impedance node at the output. For the purpose of comparison, a brief review of the current mirror TIA is necessary. A straight forward implementation of a current amplifier is a current mirror as shown in figure 5.1. Ideally, the input current at the drain of M_1 is amplified with a factor of A which is the ratio of the width of M_2 over the width of M_1 [41].

The NMOS current mirror feedback TIA provides a low input impedance. The low frequency input impedance is approximately:

$$R_{in_1} \approx \frac{1}{g_{m_1} \cdot (A+1)}, \tag{5.1}$$

where A is the current amplification gain and g_{m_1} is the transconductance of M_1. The transimpedance gain of the NMOS current mirror TIA is given by:

$$Z_T(s) \approx \frac{A}{A+1} \cdot \frac{R_{FB} - R_{in_1}}{(1 + sR_{in_1}C_{in}) \cdot (1 + s(R_{ds_4} \parallel R_{ds_2})C_{out})}, \tag{5.2}$$

where C_{in} is the summation of the photodiode capacitance C_{PD}, C_{gs1}, C_{gs2}, C_{gd3} and C_{db3}. C_{out} is the summation of the C_{db2}, C_{db4} and the load capacitance of the subsequent stages. R_{ds2} and R_{ds4} are the output resistance of M_2 and M_4, respectively.

The low frequency transimpedance gain is:

$$Z_T(0) \approx \frac{A}{A+1} \cdot (R_{FB} - R_{in_1}). \tag{5.3}$$

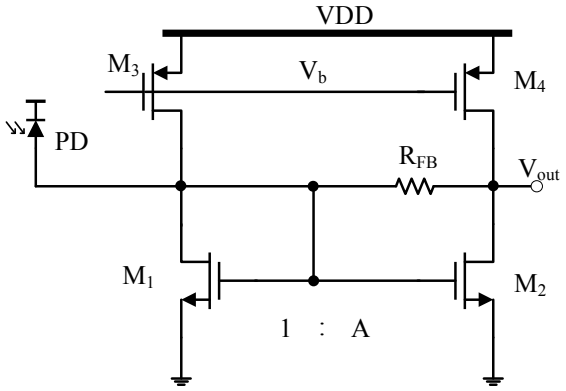

FIGURE 5.1: NMOS current mirror TIA.

As shown in equations 5.2 and 5.3, the transimpedance function is very similar to the transfer function of the shunt feedback voltage mode TIA (Chapter 2).

Like most of the current-mode TIAs, the primary disadvantage of this topology is that it generates more noise than the corresponding voltage-mode TIA. In particular, the input FETs M_1, M_2 and M_3, impact the input-referred noise current.

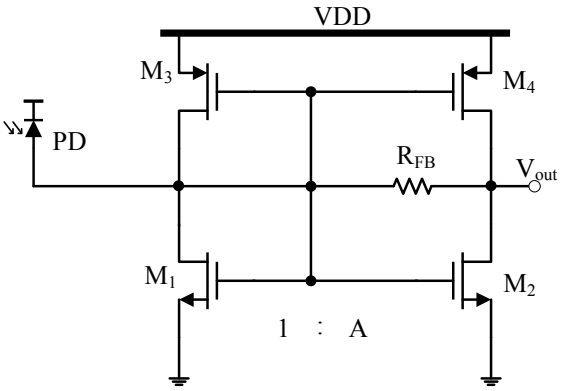

FIGURE 5.2: Push pull current mirror (PPCM) TIA.

The idea of the push pull current mirror (PPCM) TIA is to use the biasing transistors M_3 and M_4 to create a parallel AC path to the original one created by M_1 and M_2, by connecting M_3 and M_4 as a PMOS current mirror as shown in figure 5.2 [14].

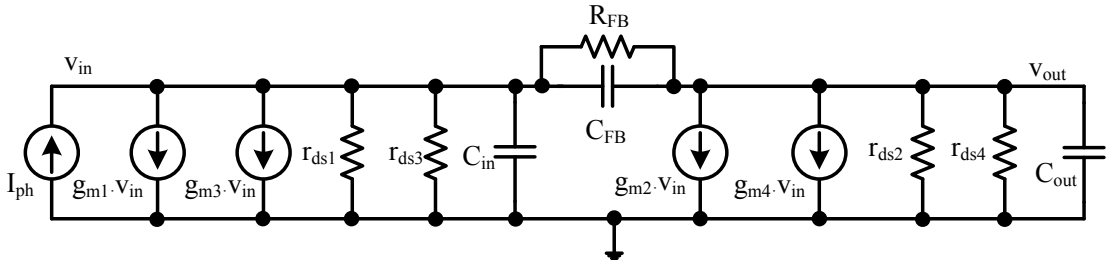

FIGURE 5.3: Small signal model of the PPCM TIA.

For small signal analysis the simplified model of the PPCM TIA in figure 5.3 could be used. The model shows parasitics and expected loads of the PPCM TIA. r_{ds1}, r_{ds2}, r_{ds3} and r_{ds4} are the output resistances of M_1, M_2, M_3 and M_4, respectively. C_{in} is the summation of the photodiode's capacitance (C_{PD}), input pads and the gate-source capacitance (C_{gs}) of transistors M_1, M_2, M_3 and M_4. C_{FB} is the feedback capacitance which is the summation of the gate-drain capacitance (C_{gd}) of transistors M_2 and M_4. C_{out} is dominated by the input capacitance of the subsequent stage.

From the small signal model in figure 5.3, the input resistance is derived and formulated as follows:

$$R_{in_2} \approx \frac{1}{(g_{m_1} + g_{m_3}) \cdot (\frac{g_{m_2}+g_{m_4}}{g_{m_1}+g_{m_3}} + 1)}, \tag{5.4}$$

where the current amplification in this case is given by:

$$A_{PPCM} = \frac{g_{m_2} + g_{m_4}}{g_{m_1} + g_{m_3}}. \tag{5.5}$$

Equations 5.4 and 5.5 show that the input resistance is approximately half the input resistance of it's NMOS counterpart.

The general transimpedance gain expression of PPCM TIA is

$$Z_{T_{PPCM}}(s) \approx \frac{A_{PPCM}}{A_{PPCM} + 1} \cdot \frac{Z_{FB} - Z_{in}}{1 + \frac{Z_{FB}}{Z_{out}}}, \tag{5.6}$$

assuming that $Z_{out} >> Z_{FB}$, the low frequency $Z_{T_{PPCM}}(0)$ is

$$Z_{T_{PPCM}}(0) \approx \frac{A_{PPCM}}{A_{PPCM} + 1} \cdot (R_{FB} - R_{in_2}). \tag{5.7}$$

For similar R_{FB}, equation 5.7 shows that the transimpedance gain of PPCM TIA is higher than the NMOS current mirror TIA, since R_{in2} is smaller than R_{in1}.

To prove the previously stated theoretical analysis by circuit simulation, a comparison between the two structures has been done, where all the transistors sizing and R_{FB} values are equal in both structures.

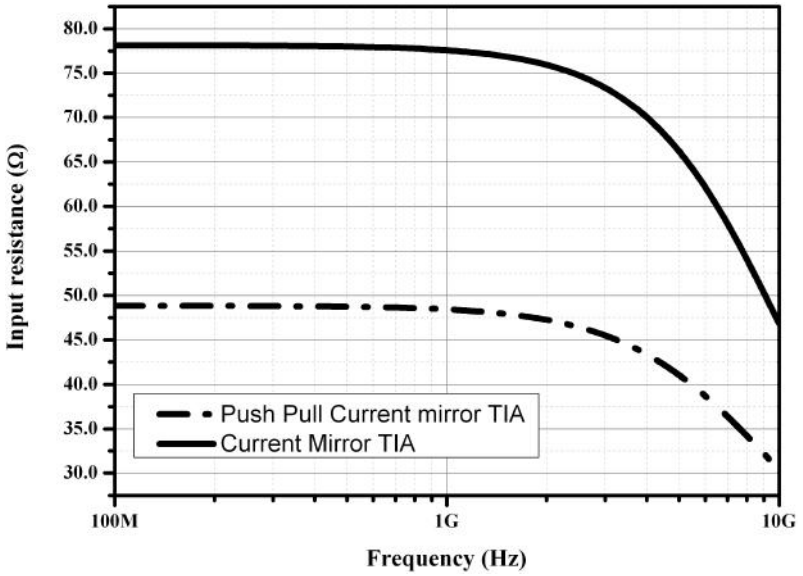

FIGURE 5.4: Comparison of the input resistance of the two current mirror TIAs.

As shown in figure 5.4, the input resistance of the PPCM TIA is approximately half the input resistance of the NMOS current mirror TIA. As a result, the transimpedance gain of PPCM TIA is 3dBΩ higher than that of the NMOS current mirror TIA, as shown in figure 5.5. A slight decrease in the PPCM TIA's bandwidth due to the increase of the input capacitance of the TIA is caused by C_{gs3} and C_{gs4}.

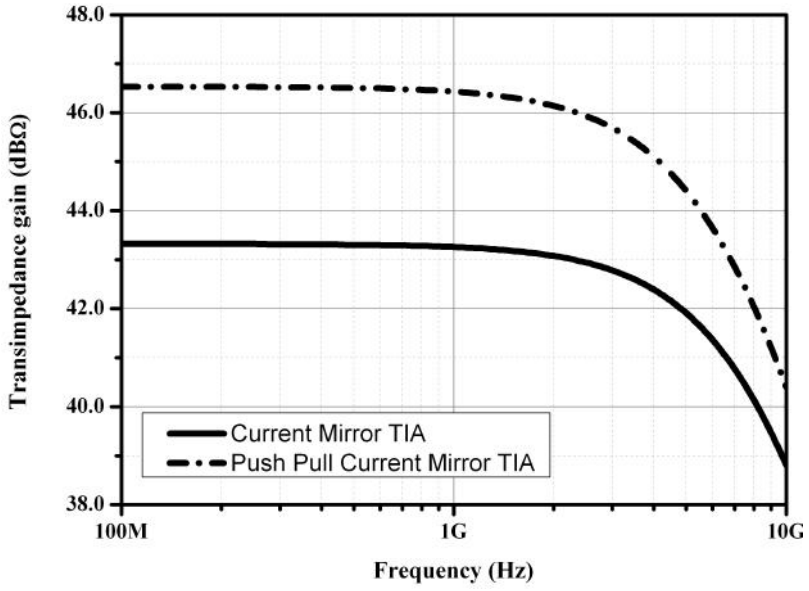

FIGURE 5.5: Comparison of the transimpedance gains of the two current mirror TIAs.

The transimpedance gain has a direct impact on the noise performance of the TIA. The higher the transimpedance gain the lower the input referred noise current of the TIA. Figure 5.6 shows the simulated equivalent input referred noise current spectral density of both topologies from 100 MHz to 10 GHz. The simulated equivalent input referred noise current spectral density of the PPCM TIA is approximately 17.5pA/$\sqrt{}$Hz at 1 GHz, which is about 6pA/$\sqrt{}$Hz lower than that of the NMOS current mirror TIA.

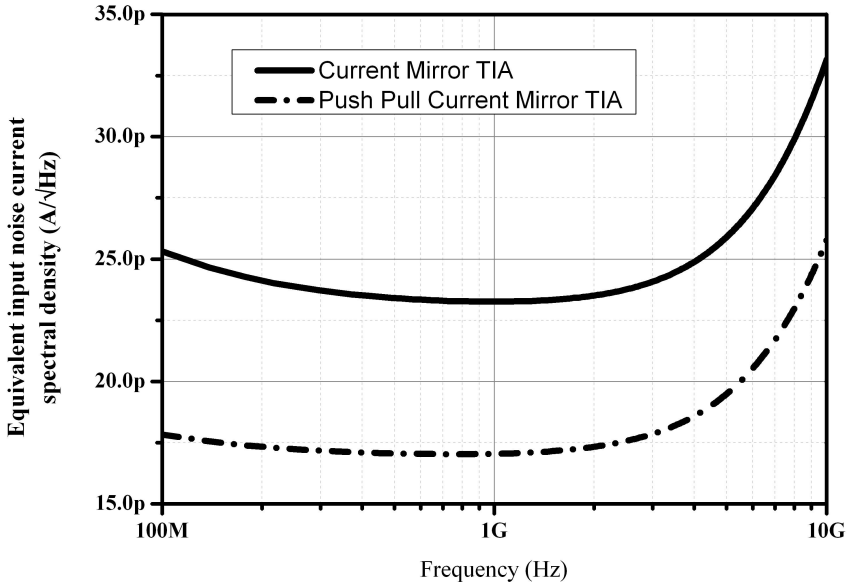

FIGURE 5.6: Comparison of the input referred noise current spectral density of the two current mirror TIAs.

5.1.1.2 PPCM Complete Optical Receiver

The architecture of the PPCM optical receiver is shown in figure 5.7. The input stage is PPCM TIA to convert the input photo-current to output voltage. The TIA's output voltage is amplified by the post amplifier. The post amplifier's output voltage is further amplified and converted to a differential signal by the single to differential ended amplifier. The final stage is a 50Ω output buffer to match the optical receiver with the measurement equipment.

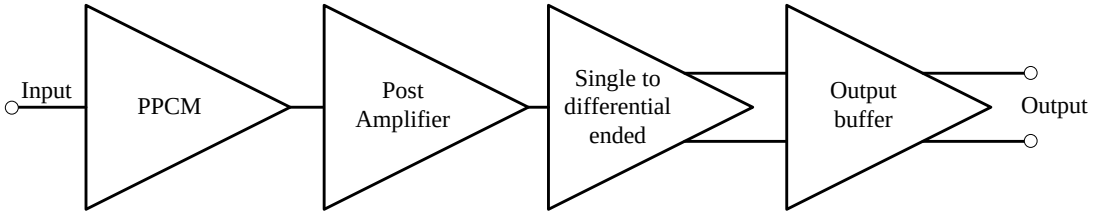

FIGURE 5.7: The architecture of the PPCM complete optical receiver.

Post Amplifier

The post amplifier is a common source amplifier (CS) with resistive-capacitive degeneration, as shown in figure 5.8. The post amplifier is a single input single output configuration because it provides higher voltage gain than it's differential counterpart.

Resistive-capacitive degeneration increases the effective transconductance of transistor M_1 which compensates the gain roll-off of the transimpedance gain, this effect happens when the zero at $(R_2C_1)^{-1}$ created by the parallel connection of R_2 and C_1 cancels the pole at the output of the amplifier [39].

An additional advantage of this topology is that the gate source capacitance of M_1 is decreased by half compared to the classical common source amplifier, resulting in a lower input capacitance seen by the previous stage and hence increases the bandwidth [39].

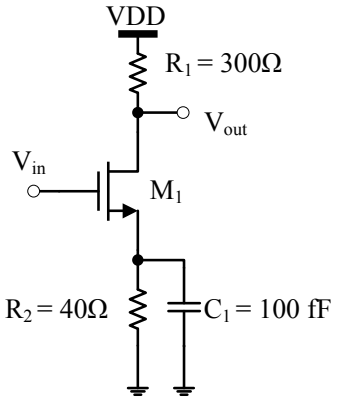

FIGURE 5.8: CS amplifier with resistive-capacitive degeneration.

The active transistor is implemented with low threshold voltage (V_{th}) deep n-well NMOS device to achieve the lowest possible V_{th} and the highest g_m possible. R_1 and R_2 are poly-resistors without silicide to achieve high sheet resistance with lowest tolerance percentage. C_1 is implemented with metal-oxide-metal (MOM) to obtain a capacitance value with high accuracy. This stage achieves a 6dB voltage gain with a bandwidth of approximately 10GHz.

Single to Differential Converter

It is important to convert the post amplifier's single output voltage to a differential signal, to have better immunity against supply and substrate noise. The core of this converter is a differential pair with resistive load (M_1, M_2 and R_1). The single to differential conversion is performed by the low-pass filter formed by R_2 and C_1. The low-pass filter extracts the DC component of the signal from the post amplifier's output and apply it to transistors M_1. The low-pass filter's time constant $(R_2C_1)^{-1}$ defines the lower corner

frequency of the optical receiver chain. Since the accuracy of C_1 is unimportant, C_1 is implemented using thick oxide NMOS transistor. This stage also provides voltage gain which is approximately equal to $g_{m1}R_1 = 2\text{dB}$.

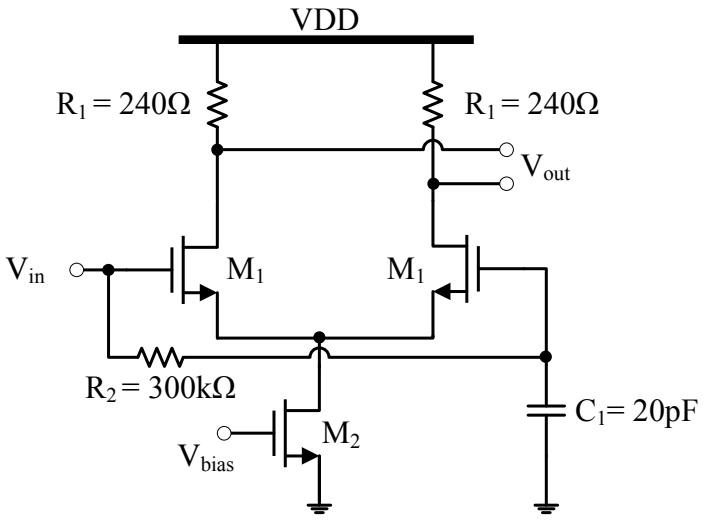

FIGURE 5.9: Single-ended to differential-ended signal converter.

Output Buffer

The 50Ω output is needed for measurements. The 50Ω output resistance provides matching to the measurement equipment. The output buffer is a simple differential pair with resistive load as shown in figure 5.10. The load resistance R_1 is larger (67Ω) than 50Ω to overcome the contribution of the output resistance of M_1 and result in an equivalent output resistance of 50Ω. This stage provides a gain of approximately 0 dB with a 10GHz bandwidth.

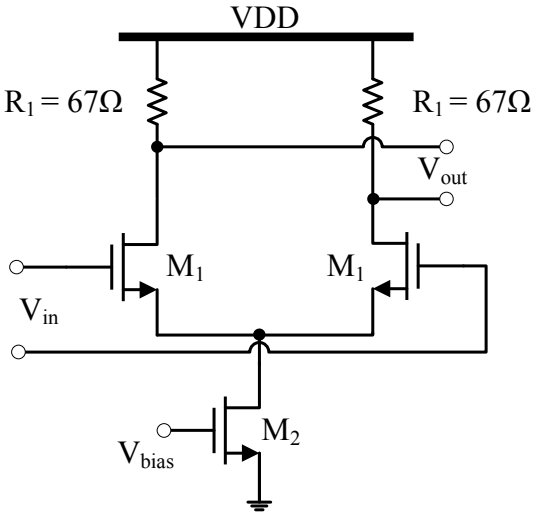

FIGURE 5.10: 50Ω output buffer.

5.1.1.3 Simulation Results

This subsection shows the post-layout simulation where the parasitic capacitances and resistances of the amplifying chain are included. The parasitic bondwire inductances are taken into account. The optical receiver is optimized for an external 10Gbps GaAs PIN photodiode with a capacitance of 0.25pF (TPD-8D12-652) and additional parasitic capacitance of the ESD protection and the pad of 0.15pF.

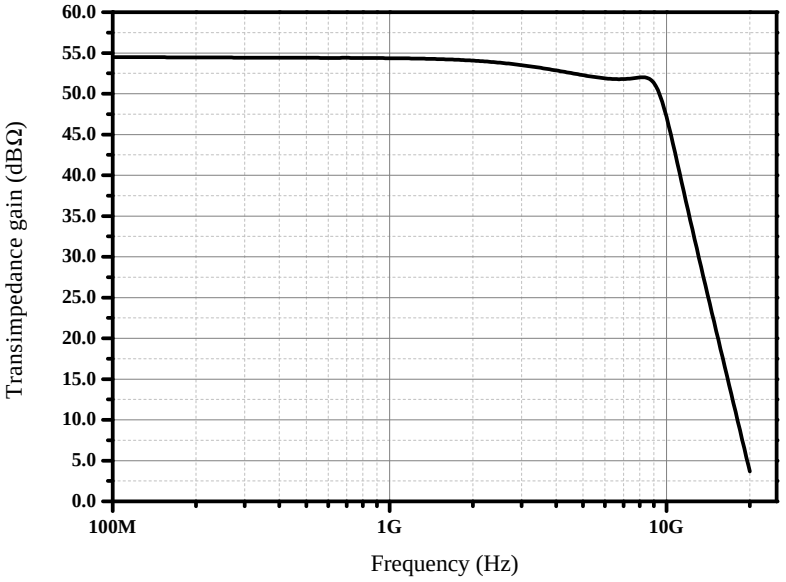

FIGURE 5.11: Simulated transimpedance frequency response of PPCM optical receiver.

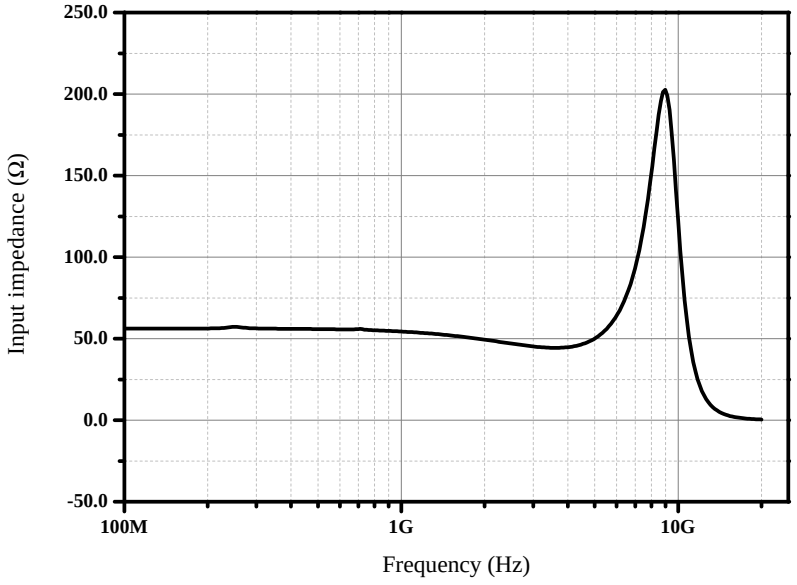

FIGURE 5.12: Simulated input impedance of PPCM TIA.

The small signal frequency response of the PPCM optical receiver is shown in figure 5.11. The overall transimpedance gain is 54.5dBΩ and the -3dB bandwidth is 8.8 GHz. Since the frequency response includes the resonance of the parasitic bondwire inductance and

the input capacitance, the -3dB bandwidth is expected to decrease due to the increase of the input capacitance in real life. The input impedance of the PPCM TIA is shown in figure 5.12, it achieves a 55Ω input impedance at DC.

The simulated input referred noise current and the output noise voltage behaviour are shown in figures 5.13 and 5.14, respectively. The average input referred noise current density is 20 pA/Hz$^{1/2}$ at 1 GHz. The integrated input referred noise current from DC to 10GHz is 1.72μA and the integrated output noise voltage for the same frequency range is 862μV.

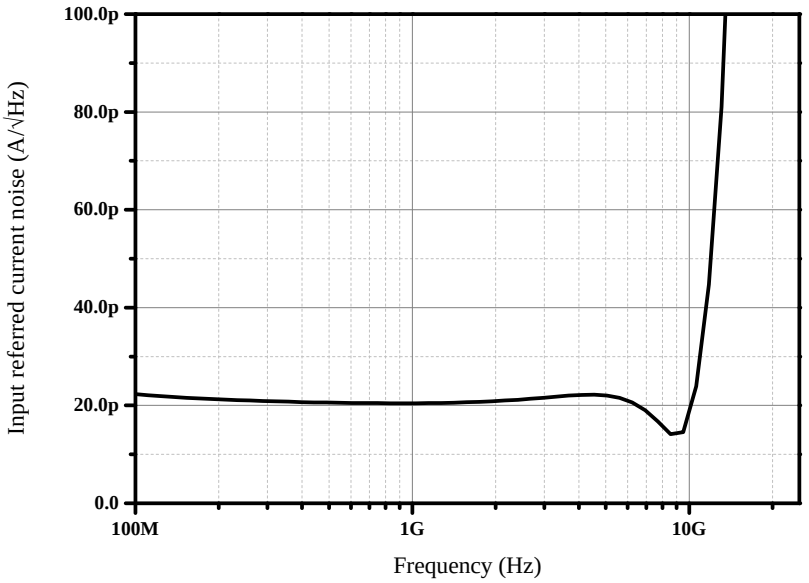

FIGURE 5.13: The input referred noise current spectral density of the PPCM optical receiver.

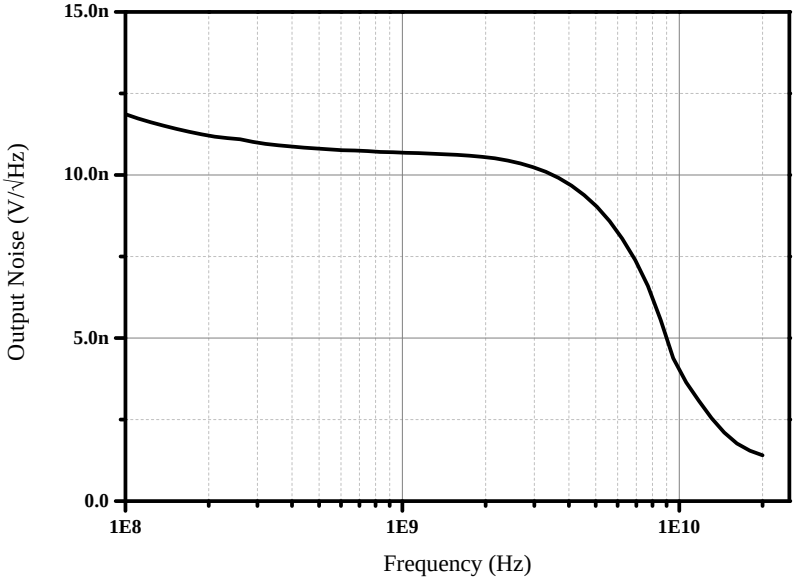

FIGURE 5.14: The output noise voltage spectral density of the PPCM optical receiver.

5.1.1.4 Chip Layout

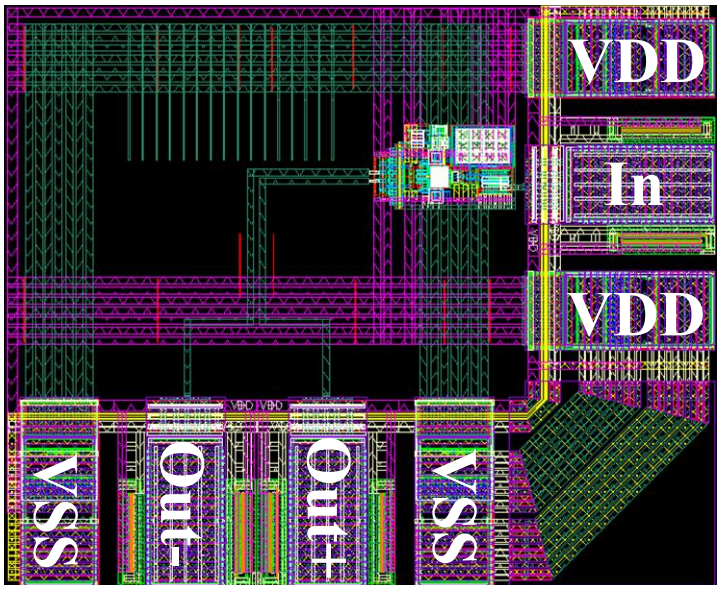

FIGURE 5.15: The layout of the PPCM optical receiver.

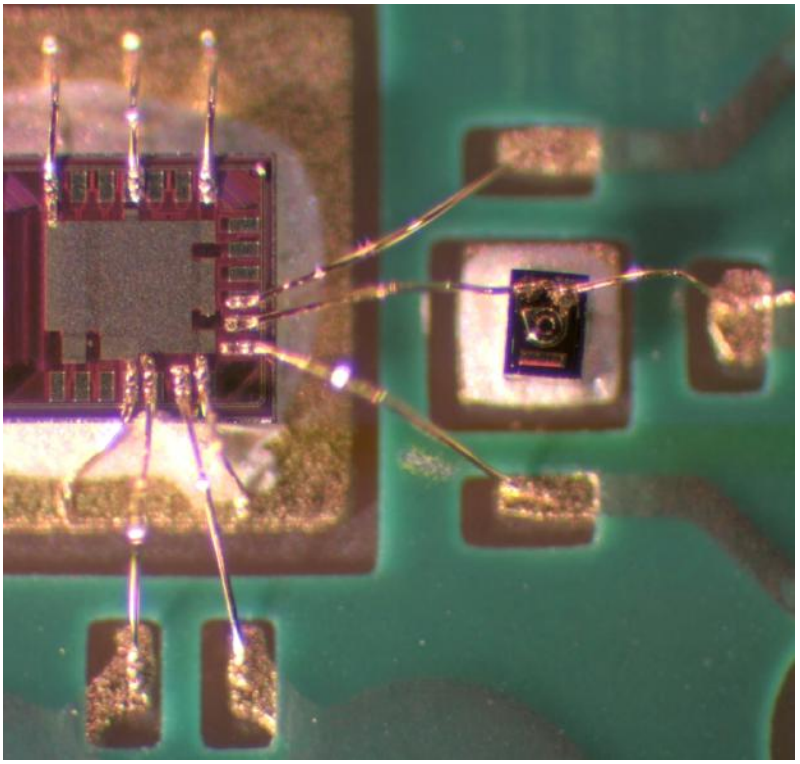

FIGURE 5.16: Chip photo of the PPCM optical receiver bonded to an external photodiode.

The chip layout shown in figure 5.15 occupies an area of 350μm $\times$ 480μm. The active area is 51μm $\times$ 96μm. The total area is mainly occupied and defined by the input/output pads. The PPCM optical receiver is placed very close to the input pad to avoid the parasitic resistance of long metal lines which increases the input impedance of the input

TIA and hence degrades the bandwidth of the receiver. Figure 5.16 is a photo of the PPCM optical receiver bonded to an external 10GHz photodiode.

5.1.1.5 Measurement Results

For measurements, a laser diode with a wavelength of 1.55μm was modulated with a 12Gb/s pattern generator. For frequency response measurement, one end of the differential output of the receiver is connected to the network analyser and the other end is terminated with a 50Ω termination. The frequency response of the PPCM optical receiver is shown in figure 5.17, the -3dB cutoff frequency is 6.11GHz. The measured -3dB cutoff frequency is lower than the value expected from simulation.

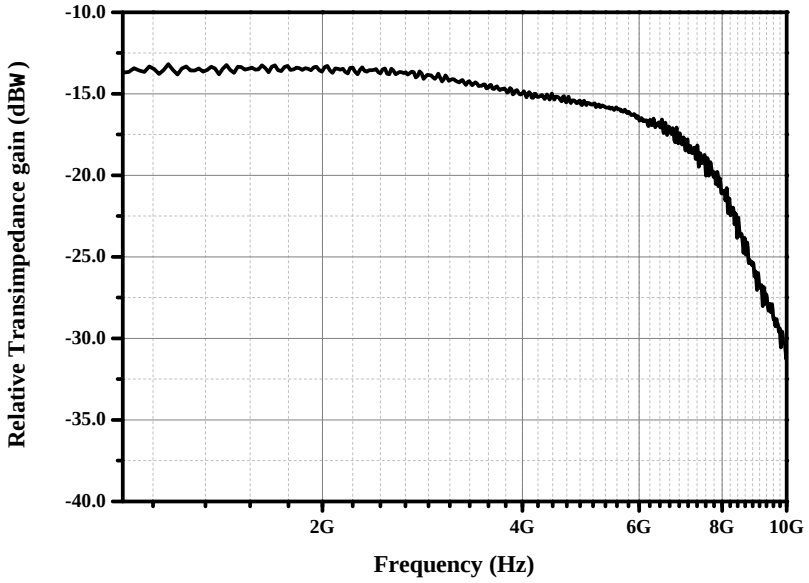

FIGURE 5.17: Measured frequency response of PPCM optical receiver.

For bit error rate measurements, a bit error analyser is used to count the failing bits. In this measurement, the laser diode was modulated from a pseudo random bit sequence (PRBS) generator. The bit error rate (BER) was measured for different power levels and a length of PRBS of 2^{23}-1. In figure 5.18, the BER vs different input power level at 9Gb/s and 10Gb/s are shown for a wavelength of 1.55μm. The sensitivity for a BER of 10^{-9} is -10dBm and -8.1dBm at 9Gb/s and 10Gb/s, respectively.

In figures 5.19 and 5.20, the eye diagrams for average optical input power of -10dBm at a data rate of 9Gb/s and -8.1dBm at a data rate 10Gb/s are shown, respectively.

The overall transimpedance gain of the PPCM optical receiver is 50dBΩ (316Ω). The chip consumes 16mA from 1.2V supply voltage, leading to a power consumption of 19.2mW. The TIA consumes 2.7mA only and the output buffer consumes 8mA.

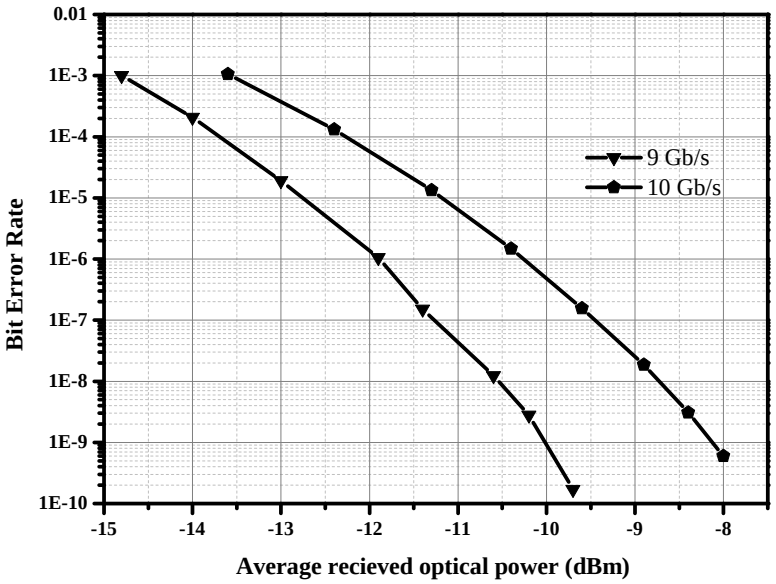

FIGURE 5.18: BER for different input power levels at 9Gb/s and 10Gb/s for a wavelength of 1.55μm.

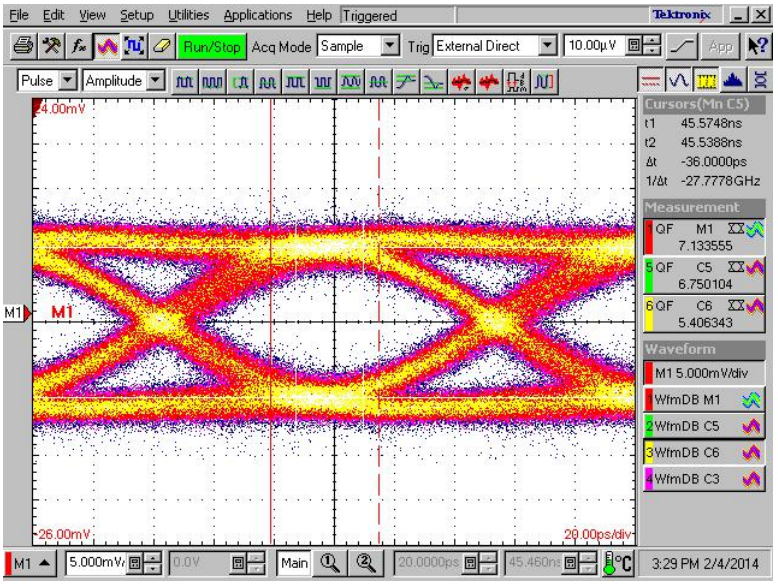

FIGURE 5.19: Eye diagram for average optical input power of -10dBm at a data rate of 9Gb/s for a BER=10^{-9}. (Horizontal scale: 20 ps/div., vertical scale: 5 mV/div.)

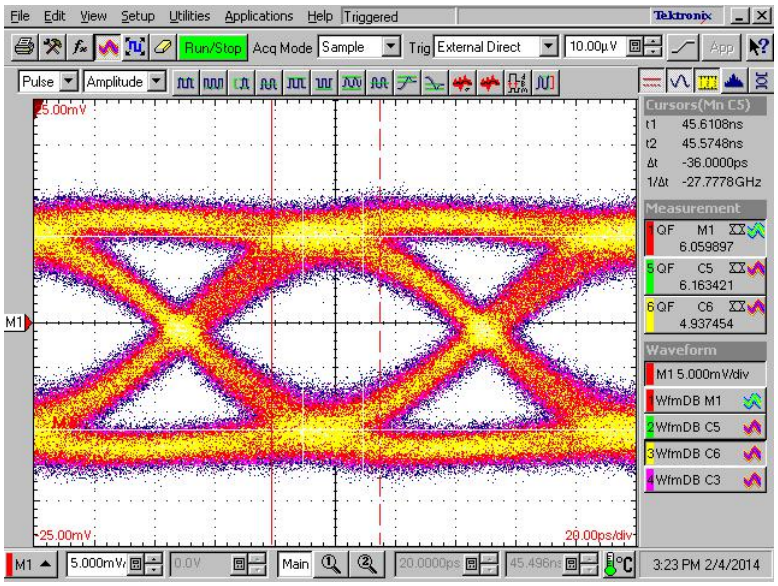

FIGURE 5.20: Eye diagram for average optical input power of -8.1dBm at a data rate of 10Gb/s for a BER=10^{-9}. (Horizontal scale: 20 ps/div., vertical scale: 5 mV/div.)

5.1.1.6 Summary

A 10Gb/s PPCM optical receiver in 40nm standard CMOS technology is introduced. The proposed design is based on a PPCM topology. The measurement results show that this optical receiver achieved a transimpedance gain of 50dBΩ (316Ω) and a bandwidth of 6.11 GHz for a total input capacitance of 0.45pF. The sensitivity for a BER of 10^{-9} is -8.1dBm at 10Gb/s. The presented receiver consumes 19.2mW from 1.2V and occupies an active area of 51μm $\times$ 96μm.

5.1.2 Common Drain Active Feedback (CDAF) TIA

5.1.2.1 CDAF TIA Theory

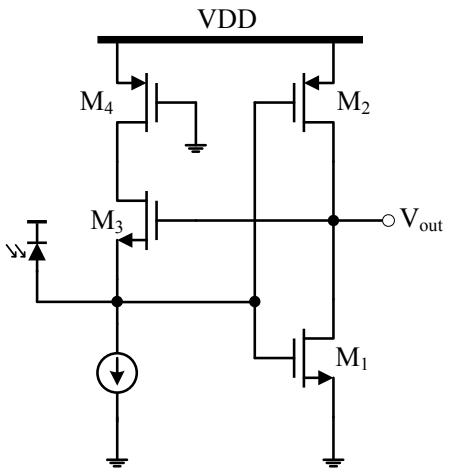

FIGURE 5.21: Common drain active feedback TIA in [3].

The first implemented CDAF TIA in [3] is shown in figure 5.21, the main amplifier is an inverter (M_1 and M_2) with a common drain configuration as an active feedback (M_3). This design has two disadvantages, the first is the number of devices connected at the input, leading to a high input capacitance reducing the bandwidth of the TIA and the second is the presence of M_4 that reduces the overhead voltage of M_3 and has no clear advantage in the design.

The proposed CDAF TIA is shown in figure 5.22, the TIA consists of a NMOS cascode amplifier (M_1, M_2 and R_1), current source (M_4) and the active feedback is implemented using a common drain configuration with transistor M_3.

The input capacitance is much lower since the cascode amplifier eliminates the miller capacitance. In addition, minimum number of devices are connected to the input terminal leading to minimal parasitic capacitance resulting in higher bandwidth.

Using common drain as the active feedback has an advantage in setting the DC operating point for the cascode amplifier. Since the common drain is a level shifter, the output is set to 800mV giving adequate headroom for transistors (M_1 and M_2) and the input is set to 400mV keeping M_1 in saturation region.

The small signal model of the proposed CDAF TIA is shown in figure 5.23. Small signal parameters of the CDAF TIA can be derived from the presented model. Using Kirchhoff's current (KCL) and voltage (KVL) laws, result in the following equations:

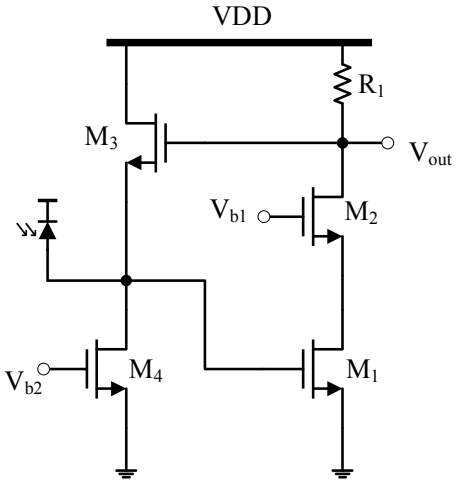

FIGURE 5.22: The proposed CDAF TIA.

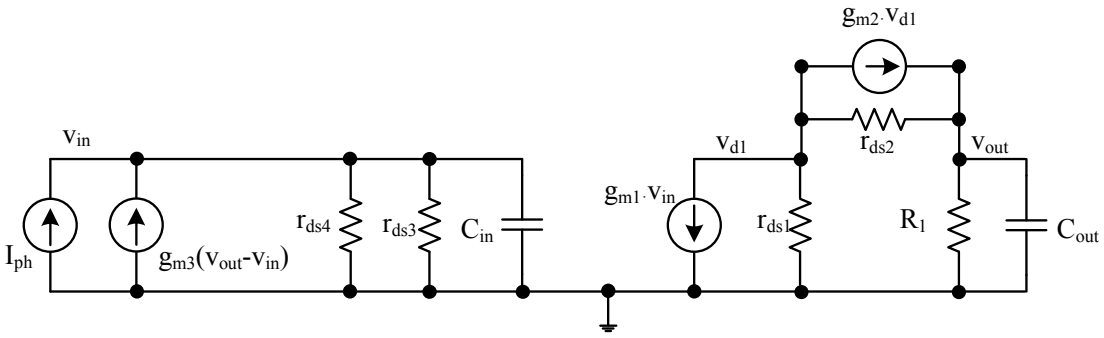

FIGURE 5.23: The small signal model of the proposed CDAF TIA.

$$V_{in} = (I_{PH} + g_{m_3}(V_{out} - V_{in}))(r_{ds_4} \parallel r_{ds_3} \parallel C_{in}). \tag{5.8}$$

$$V_{out} - V_{d_1} = -g_{m_3} r_{ds_2}. \tag{5.9}$$

$$V_{out} = (g_{m_1} V_{in} + V_{d_1}/r_{ds_1}) R_1. \tag{5.10}$$

By combining equations 5.8, 5.9 and 5.10, the DC input resistance can be derived:

$$Z_{in}(0) = \frac{1}{g_{m_3}(g_{m_1} R_1 + 1)}, \tag{5.11}$$

and the frequency dependent input impedance is:

$$Z_{in}(s) = \frac{1}{g_{m_3}(g_{m_1} R_1 + 1) + sC_{in}}, \tag{5.12}$$

where C_{in} is the summation of the photodiode's capacitance, pad's capacitance and the

gate capacitance of M_1. The term $g_{m_1}R_1$ is approximately equal to the open loop voltage gain of the cascode amplifier. The input impedance of the proposed CDAF TIA can be decreased by increasing the voltage gain of the cascode amplifier.

The CDAF TIA's transimpedance gain can also be derived from the small signal model in figure 5.23. By substituting equation 5.12 in equation 5.8 the transimpedance gain is:

$$Z_T(s) = \left[\frac{1}{g_{m_3}}\right]\left[\frac{1 - g_{m_3}(g_{m_1}R_1 + 1) + g_{m_3}}{g_{m_3}(g_{m_1}R_1 + 1) + sC_{in}}\right]. \tag{5.13}$$

From equation 5.13, the DC transimpedance gain is:

$$Z_T(0) = -\frac{1}{g_{m_3}}. \tag{5.14}$$

From equations 5.11 and 5.14, the proposed CDAF TIA behaves similarly to the shunt shunt resistive feedback TIA. If we identify $1/g_{m_3}$ as the feedback resistance, the transimpedance gain is equal to the feedback resistance and the input impedance is equal to the feedback resistance reduced by a factor which is approximately equal to the voltage gain of the cascode amplifier.

The presented CDAF TIA has two main poles which could be intuitively extracted from the small signal model in figure 5.23. The first pole is located at the input terminal:

$$\omega_{p1} = \frac{g_{m_3}(g_{m_1}R_1 + 1)}{C_{in}}. \tag{5.15}$$

The second pole is located at the output

$$\omega_{p2} = \frac{1}{R_1 C_{out}}, \tag{5.16}$$

where C_{out} is the load capacitance of the subsequent stage.

Since the input resistance $Z_{in}(0)$ and the output resistance R_1 are comparable, the dominate pole is determine mainly by the capacitance value. The input capacitance is clearly larger than the output capacitance. Therefore the dominate pole is located at the input and it defines the bandwidth of the presented TIA. The -3dB bandwidth of the TIA is:

$$BW = \frac{g_{m_3}(g_{m_1}R_1 + 1)}{2\pi C_{in}}. \tag{5.17}$$

Increasing the voltage gain of the cascode amplifier will result in the decrease of the input resistance, leading to the increase of TIA's bandwidth. Increasing the cascode's voltage gain can be achieved either by increasing R_1 or g_{m_1}. Increasing R_1 is more effective since increasing g_{m_1} will result in the increase of the input capacitance reducing the bandwidth.

5.1.2.2 CDAF Complete Optical Receiver

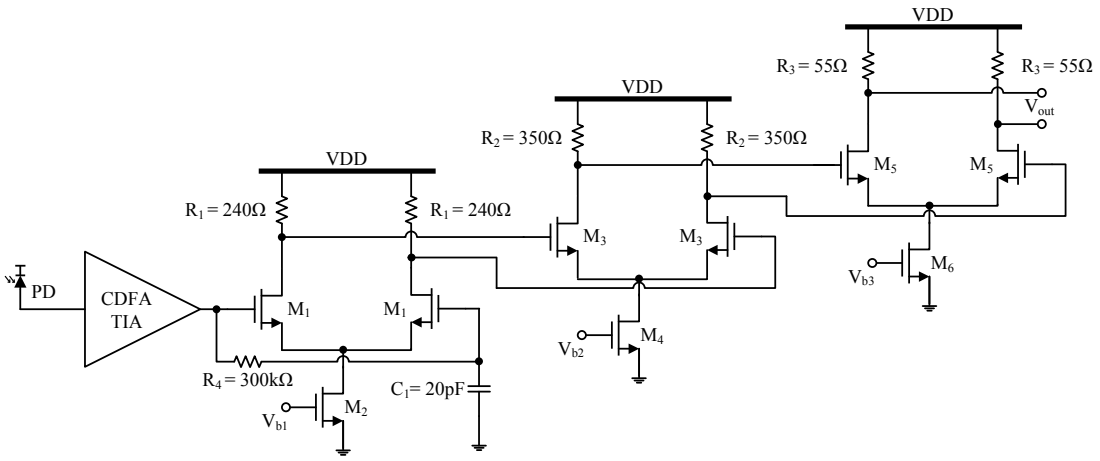

FIGURE 5.24: CDAF complete optical receiver.

The complete CDAF optical receiver is shown in figure 5.24. The receiver consists of the CDAF TIA, a single to differential converter (R_1, M_1, M_2, C_1 and R_4), post amplifier (R_2, M_3 and M_4) and 50Ω output buffer (R_3, M_5 and M_6).

The stages following the CDAF TIA are integrated with the TIA to provide enough gain and to interface with the measurement equipment. The single to differential amplifier and post amplifier are used to amplify the output voltage of the CDAF TIA. In addition, these two stages help in isolating the TIA from the large input capacitance of the 50Ω output buffer to reduce the loading effects of theses parasitic capacitors.

The single ended TIA output is converted to differential output to benefit from the better power supply and common mode rejection. The post amplifier is used to further increase the gain. The final stage is a 50Ω output buffer to create an appropriate matching to the 50Ω measurement equipment.

The tail currents of the three differential pairs are mirrored from a 100μA reference current which is generated on chip. The CDAF TIA, the single to differential converter, the post amplifier and the 50Ω output buffer consume 2mA, 2mA, 2mA and 8mA, respectively.

The CDAF TIA has a transimpedance gain of 47dBΩ. The single to differential converter and post amplifier have a total voltage gain of 8dB with a bandwidth of 10GHz. The 50Ω output buffer has approximately a unity gain. The CDAF TIA's bandwidth is limited by the loading effects at its input and the total optical receiver's bandwidth is further reduced by the parasitic capacitance associated with the output buffer.

5.1.2.3 Simulation Results

This subsection shows the post-layout simulation where the parasitic capacitances and resistances of the amplifying chain are included. The parasitic bondwire inductance are taken into account. The optical receiver is optimized for an external 10Gbps GaAs PIN photodiode with a capacitance of 0.25pF (TPD-8D12-652) and additional parasitic capacitance of the ESD protection and the pad of 0.15pF.

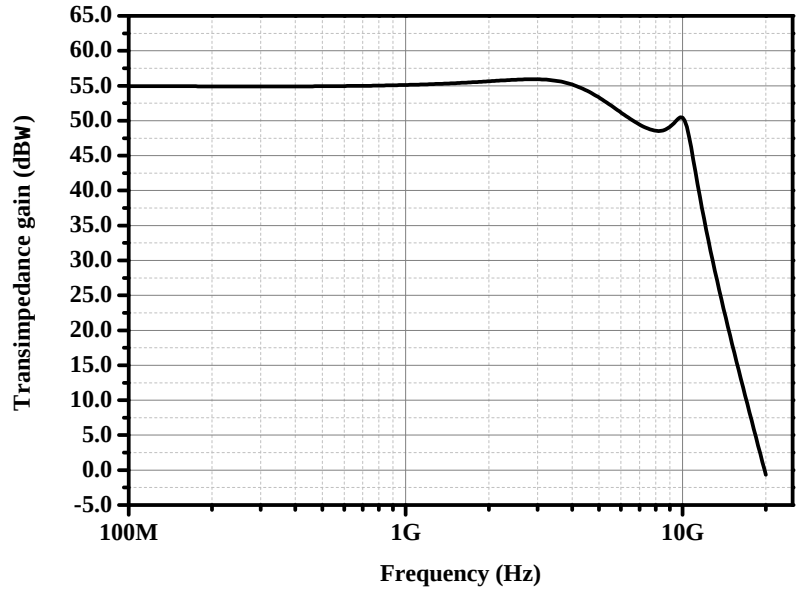

FIGURE 5.25: Simulated frequency response of the CDAF optical receiver.

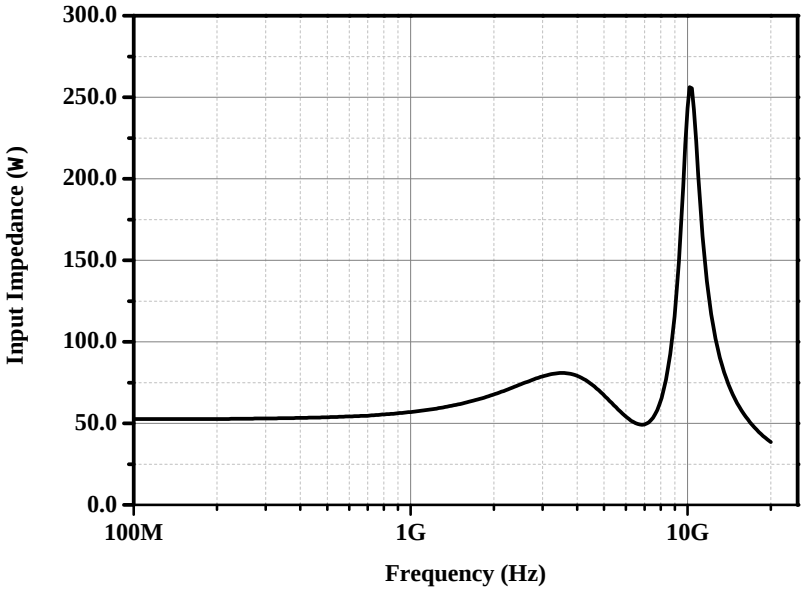

FIGURE 5.26: Simulated input impedance of the CDAF optical receiver.

The small signal frequency response of the CDAF optical receiver is shown in figure 5.25. The overall transimpedance gain is 55dBΩ and the -3dB bandwidth is 5.6 GHz. The 1 dB peaking occurring at 3 GHz is due to the complex conjugate poles created at the input and the output of the TIA. The second peaking occurring at 10GHz is due to the resonance of the bond wire inductance and the parasitic input capacitance. The input impedance of the CDAF TIA is shown in figure 5.26, it achieves a 52.6Ω input impedance at DC.

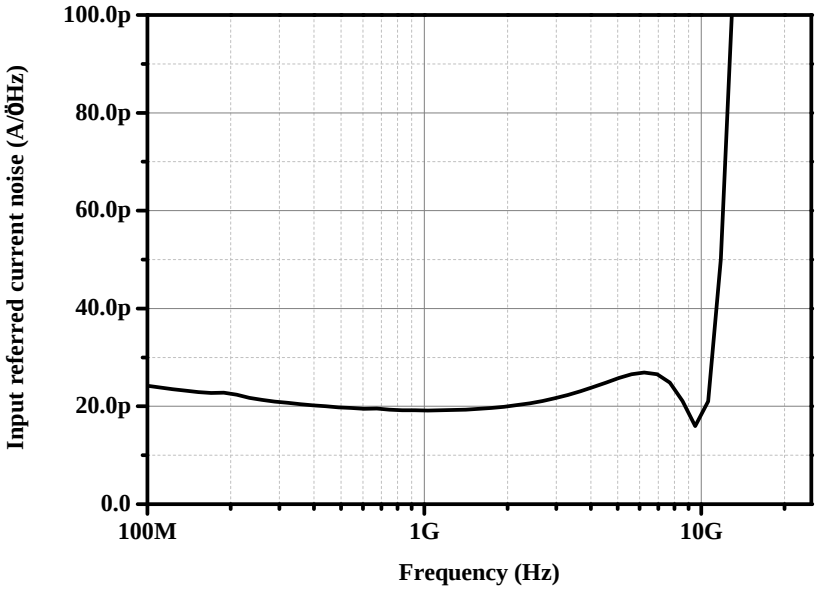

FIGURE 5.27: Simulated input referred current noise spectral density of the CDAF optical receiver.

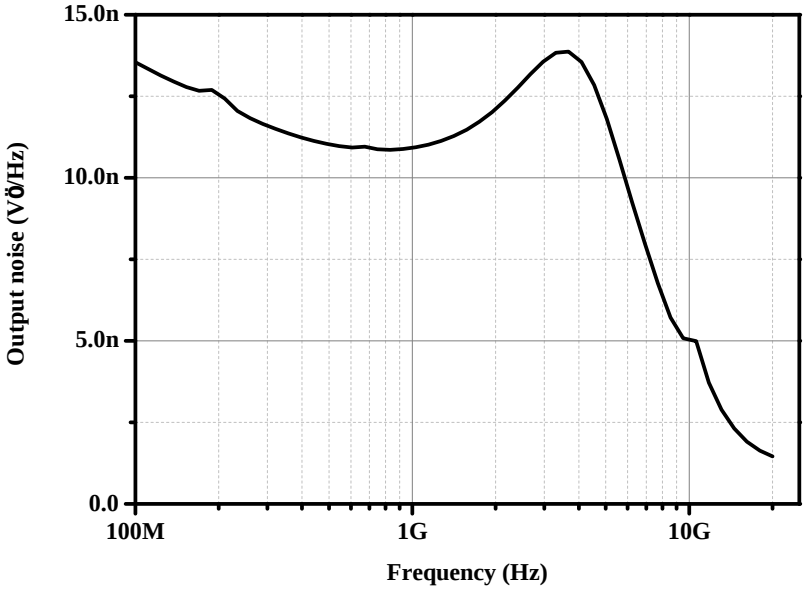

FIGURE 5.28: Simulated output noise voltage spectral density of the CDAF optical receiver.

The simulated input referred noise current and the output noise voltage behaviour are shown in figures 5.27 and 5.28, respectively. The average input referred noise current density is 20 pA/Hz$^{1/2}$ at 1 GHz. The integrated input referred noise current from DC to 8GHz is 1.9μA and the integrated output noise voltage for the same frequency range is 1068μV.

5.1.2.4 Chip Layout

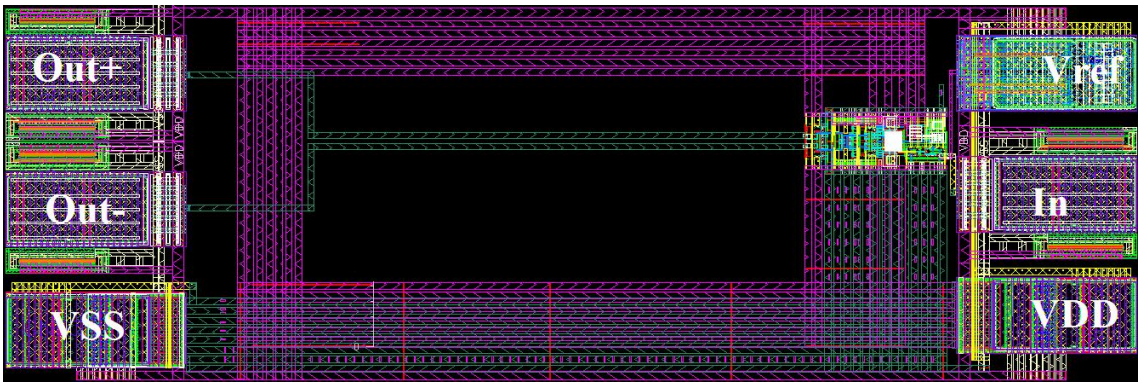

FIGURE 5.29: Layout of the CDAF complete optical receiver.

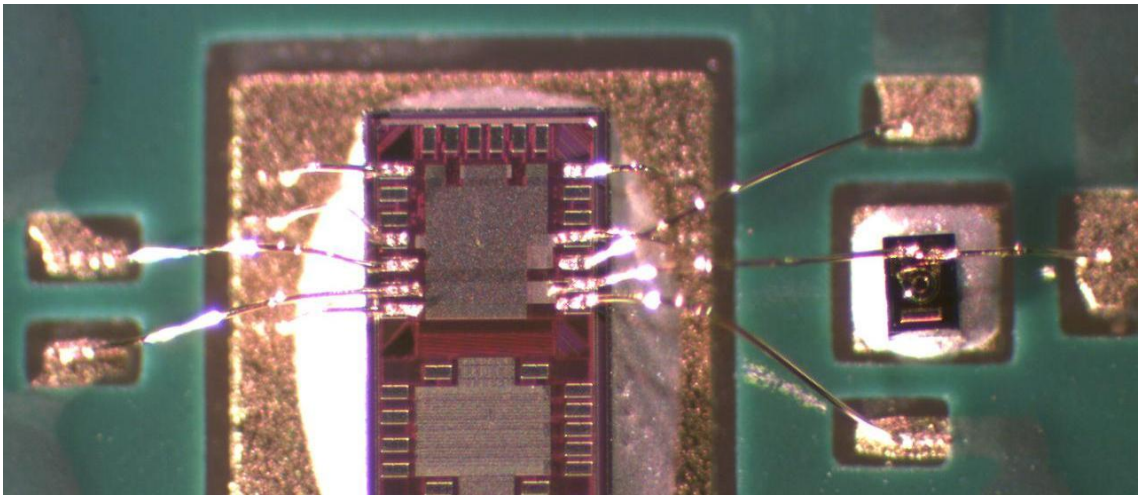

FIGURE 5.30: Chip photo of the CDAF optical receiver bonded to an external photodiode.

The chip layout shown in figure 5.29 occupies around 240μm $\times$ 750μm. The active area is 33μm $\times$ 101μm. The area is mainly occupied and defined by the input/output pads. The CDAF optical receiver is placed very close to the input pad to avoid the parasitic resistance of long metal lines which increases the input impedance of the TIA and hence degrades the bandwidth of the receiver. Figure 5.30 is a photo of the CDAF optical receiver connected to an external 10GHz photodiode.

5.1.2.5 Measurement Results

For measurements, a laser diode with a wavelength of 1.55μm was modulated with a 12Gb/s pattern generator. For frequency response measurement, one end of the differential output of the receiver is connected to the network analyser and the other end is terminated with a 50Ω termination. The frequency response of the CDAF optical receiver is shown in figure 5.31, the -3dB cutoff frequency is 5.2GHz. The measured -3dB cutoff frequency is lower than the value expected from simulation, due to the parasitics added by the PCB.

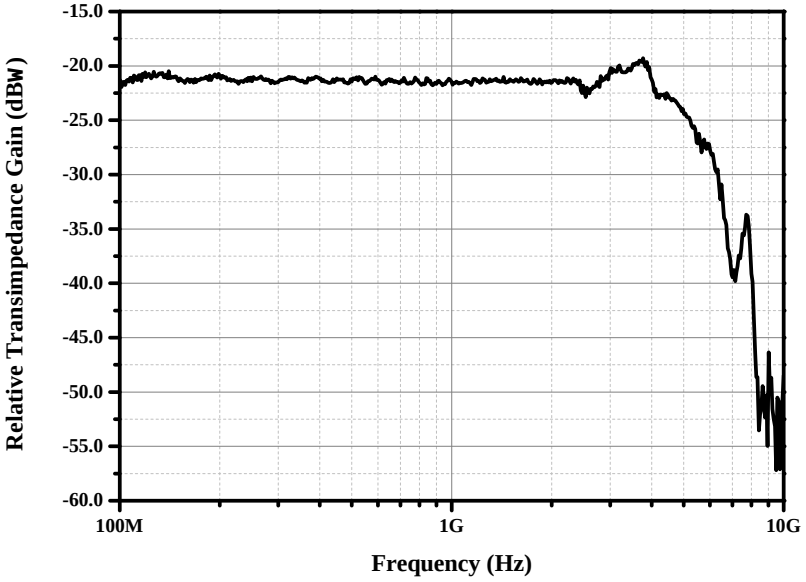

FIGURE 5.31: Measured frequency response of the CDAF optical receiver.

For bit error rate measurements, a bit error analyser is used to count the failing bits. In this measurement, the laser diode was modulated from a pseudo random bit sequence (PRBS) generator. The bit error rate (BER) was measured for different power levels and a length of PRBS of 2^{15}-1. In figure 5.32, the BER vs different input power levels at 6Gb/s, 7Gb/s and 8Gb/s are shown for a wavelength of 1.55μm. The sensitivity for a BER of 10^{-9} is -13.9dBm, -12dBm and -11.4dBm at 6Gb/s, 7Gb/s and 8Gb/s, respectively.

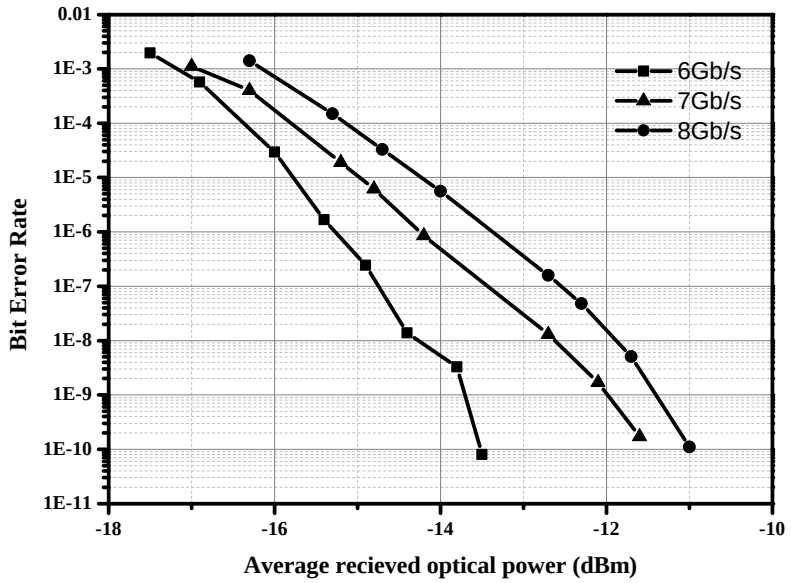

FIGURE 5.32: Measured BER vs different input average optical power levels for data rates at 6Gb/s, 7Gb/s and 8Gb/s for $\lambda = 1.55\mu$m.

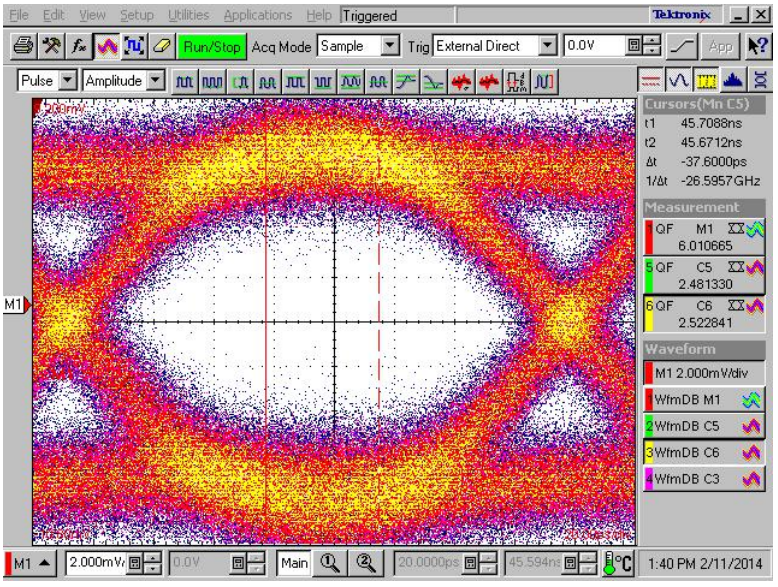

FIGURE 5.33: Measured eye diagram for 6Gb/s at input optical power of -10.1dBm with BER=10^{-9}.(Horizontal scale: 20 ps/div., vertical scale: 2 mV/div.)

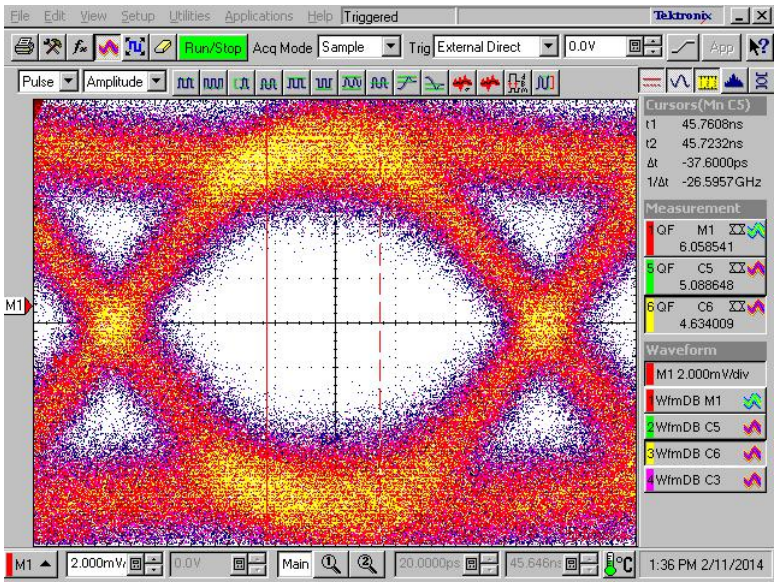

FIGURE 5.34: Measured eye diagram for 7Gb/s at input optical power of -9.9dBm with BER=10^{-9}.(Horizontal scale: 20 ps/div., vertical scale: 2 mV/div.)

In figures 5.33, 5.34 and 5.35, the eye diagrams for average optical input power of -10.1dBm at a data rate of 6Gb/s, -9.9dBm at a data rate of 7Gb/s and -9.9dBm at a data rate 8Gb/s are shown, respectively.

The overall transimpedance gain of the CDAF optical receiver is 51dBΩ (355Ω). The chip consumes 14mA from 1.2V supply voltage, leading to a power consumption of 16.8mW. The TIA consumes 2mA only and the output buffer is 8mA.

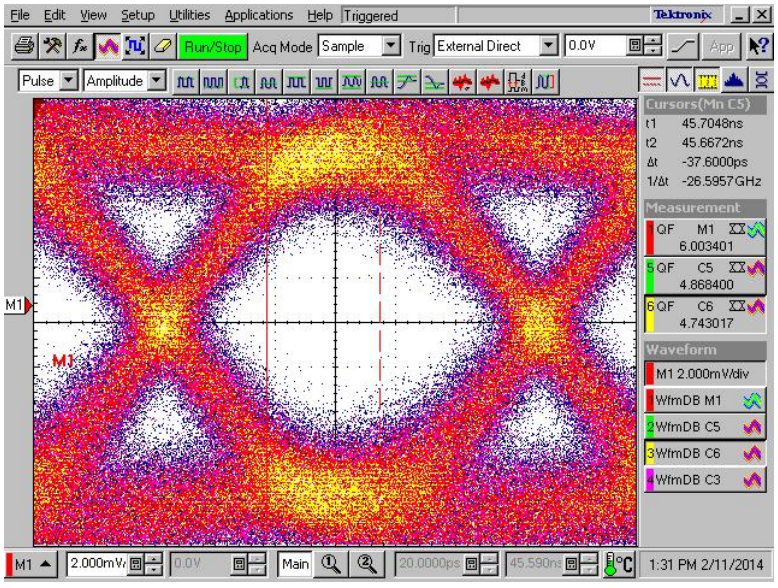

FIGURE 5.35: Measured eye diagram for 8Gb/s at input optical power of -9.9dBm with BER=10^{-9}.(Horizontal scale: 20 ps/div., vertical scale: 2 mV/div.)

5.1.2.6 Summary

A CDAF optical receiver in 40nm standard CMOS technology is introduced. The proposed design is based on a CDAF topology. The measurement results show that this optical receiver achieved a transimpedance gain 51dBΩ (355Ω) and a bandwidth of 5.2 GHz for a total input capacitance of 0.45pF. The sensitivity for a BER of 10^{-9} is -11.7dBm at 8Gb/s. The presented receiver consumes 14mA from 1.2V and occupies an active area of 33μm $\times$ 101μm.

5.1.3 Regulated Cascode with Active Feedback (RGCAF) TIA

5.1.3.1 RGCAF Theory

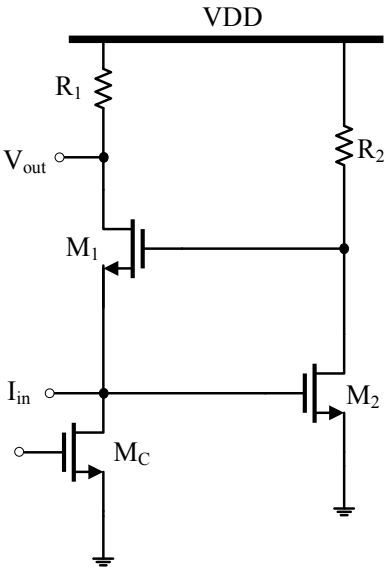

FIGURE 5.36: Classical RGC TIA.

A classical regulated cascode (RGC) TIA is shown in figure 5.36. In this TIA topology, the gate potential of M_1 should be at least equal to the headroom of two gate source voltages and V_{out} node voltage should be equal to one gate source voltage and one drain source saturation voltage. If the transistors are biased at least at half the supply voltage, the two gate source voltage requirement will lead to a difficult biasing scheme with supply voltage less than 1.2V, resulting in a significant performance change over process and temperature variation. The biasing of the transistor could be reduced to fit the supply voltage. However, this will result in a significant decrease in the speed of the RGC TIA [19].

The regulated cascode with active feedback is shown in figure 5.37. The modification shown in figure 5.37 is the addition of a common source active feedback PMOS transistor M_3. This feedback is a shunt shunt feedback, decreasing the input resistance and hence helps in the increase of the bandwidth of the TIA to overcome the limitation of the lower biasing voltages to fit the low supply voltage.

The implemented TIA consists of a common gate (CG) stage as a main amplifier [M_1, R_1], a boosting feedback amplifier [M_2 and R_2] and a PMOS active feedback (M_3). Resistor R_3 operates as a current source.

The small signal model of the proposed RGCAF TIA is shown in figure 5.38. Small signal parameters of the RGCAF TIA can be derived from the presented model. Using

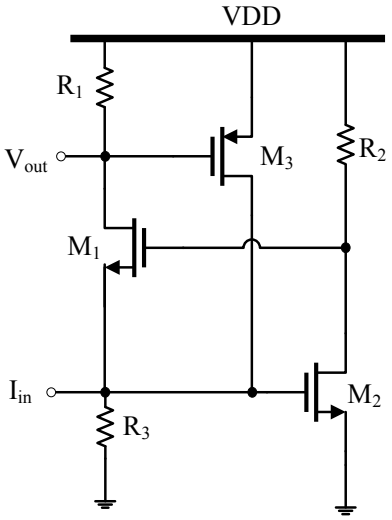

FIGURE 5.37: The proposed RGCAF TIA.

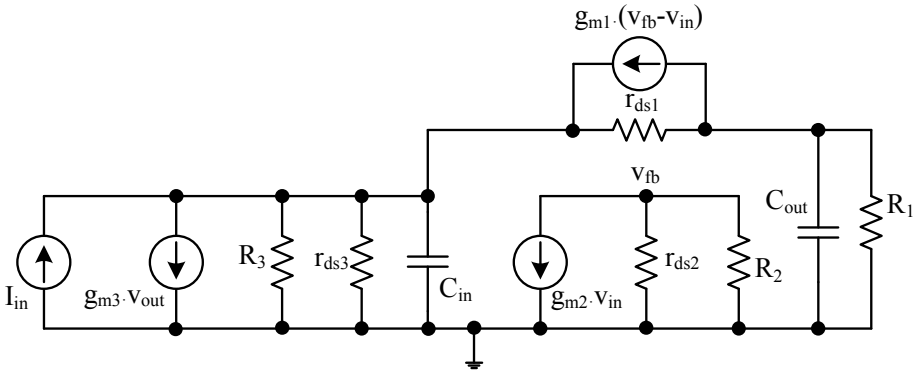

FIGURE 5.38: Small signal model of the RGCAF TIA.

Kirchhoff's current (KCL) and voltage (KVL) laws, the following equations are extracted:

$$I_{in} = g_{m_3} V_{out} - g_{m_1}(V_{fb} - V_{in}), \tag{5.18}$$

$$V_{fb} = -g_{m_2}(R_2 \parallel r_{ds_2}) V_{in}, \tag{5.19}$$

$$V_{out} = -g_{m_1} R_1 (V_{fb} - V_{in}). \tag{5.20}$$

By combining equations 5.18, 5.19 and 5.20, the DC input resistance can be derived:

$$Z_{in}(0) = \frac{1}{g_{m_1}(g_{m_2}(R_2 \parallel r_{ds_2}) + 1)(g_{m_3} R_1 + 1)}, \tag{5.21}$$

and the frequency dependent input impedance is:

$$Z_{in}(s) = \frac{1}{g_{m_1}(g_{m_2}(R_2 \parallel r_{ds_2}) + 1)(g_{m_3} R_1 + 1) + sC_{in}}, \tag{5.22}$$

where g_{m_y} is the gate source transconductance of M_y, r_{ds_y} is the output resistance of M_y and C_{in} is the summation of the photodiode's capacitance, pad's capacitance, the source capacitance M_1, the gate capacitance of M_2 and the source capacitance M_3.

The low frequency input impedance expressed in 5.21 shows that the transconductance of the CG transistor (M_1) g_{m_1} is multiplied by two voltage gain factors $g_{m_2}(R_2 \parallel r_{ds_2})$ and $g_{m_3}R_1$, which allows the achievement of lower input impedance than the CG, RGC and active feedback TIAs, allowing the achievement of higher bandwidth.

In addition, it can achieve the same input impedance as the CG and RGC TIAs, with smaller devices and lower current consumption, since g_{m_1} is increased by two voltage gain factors compared to the CG stage and one voltage gain factor compared to the RGC stage.

The transimpedance gain $Z_T(s)$ can also be derived from equations 5.18, 5.19, 5.20 and 5.22 as follows:

$$Z_T(s) = \frac{R_1}{(g_{m_3}R_1 + 1)(1/Z_{in}(0) + sC_{in})(1/R_1 + sC_{out})}, \tag{5.23}$$

where C_{out} is the summation of the drain capacitance of M_1, the gate capacitance of M_3 and the input capacitance of the subsequent stage.

The low frequency transimpedance gain $Z_T(0)$ is reduced to be as follows:

$$Z_T(0) = \frac{R_1}{(g_{m_3}R_1 + 1)} = \frac{1}{g_{m_3}} \parallel R_1. \tag{5.24}$$

The presented RGCAF TIA has more than one path from the input to the output. The presence of these paths usually creates more than one zero in the transimpedance transfer function. These zeros are created by source-drain capacitance of M_1 and gate-drain capacitances of M_1, M_2 and M_3. Since these capacitances are orders of magnitude smaller than the dominate parasitic capacitance at the input and output capacitance of the TIA, the zeros are located at frequency higher than the TIA's bandwidth of interest. Therefore, they are omitted from $Z_T(s)$ transfer function.

This topology has two main poles. The dominate pole is located at the input terminal and is expressed as follows:

$$\omega_{p_1} \approx \frac{g_{m_1}(g_{m_2}(R_2 \parallel r_{ds_2}) + 1)(g_{m_3}R_1 + 1)}{C_{in}}, \tag{5.25}$$

The second pole is located at the output and is expressed as follows:

$$\omega_{p_2} \approx \frac{R_1}{C_{out}}. \tag{5.26}$$

Since C_{in} is larger than C_{out}, the bandwidth is defined approximately by the dominate pole. The -3dB bandwidth is:

$$BW \approx \frac{g_{m_1}(g_{m_2}(R_2 \parallel r_{ds_2}) + 1)(g_{m_3}R_1 + 1)}{2\pi C_{in}}. \tag{5.27}$$

Equations 5.24 and 5.27 show an advantage of the this topology, that the bandwidth of the TIA can be increased independently from the transimpedance gain by increasing the voltage gain of common source amplifier (M_2 and R_2). Increasing the value of R_2 is more effective than increasing the transconductance of M_2, which will result in a wider transistor and hence higher input capacitance and lower bandwidth.

5.1.3.2 RGCAF Complete Optical Receiver

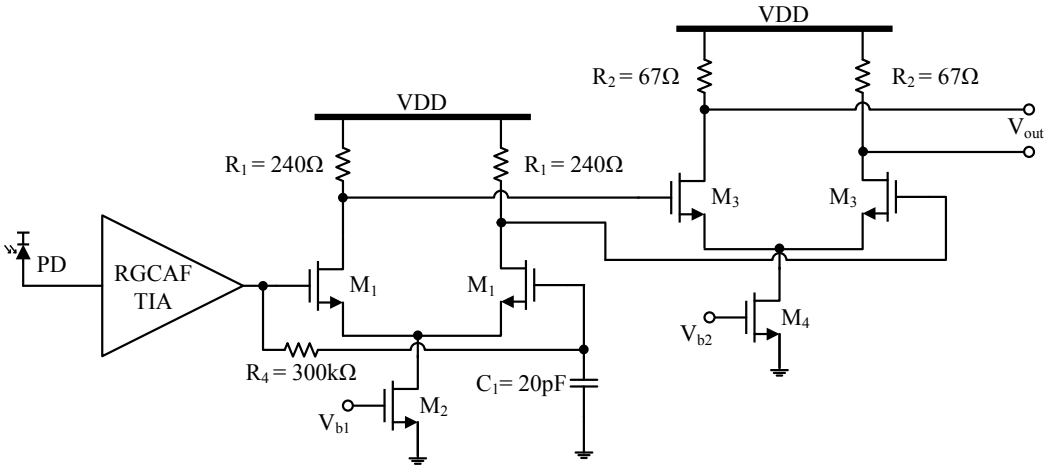

FIGURE 5.39: RGCAF complete optical receiver.

The complete RGCAF optical receiver is shown in figure 5.39. The receiver consists of the RGCAF TIA, a single to differential converter (R_1, M_1, M_2, C_1 and R_4) and 50Ω output buffer (R_2, M_3 and M_4). The stages following the RGCAF TIA are integrated with the TIA to provide enough gain and to interface with the measurement equipment.

The single to differential amplifier is used to amplify the output voltage of the RGCAF TIA, isolate the TIA from the large load capacitance of the 50Ω output buffer and convert the single output voltage to fully differential output to benefit from the better power supply and common mode rejection. The final stage is a 50Ω output buffer to create an appropriate matching to the 50Ω measurement equipment.

The tail currents of the two stages are mirrored from a 100μA reference current which is generated on chip. The RGCAF TIA, the single to differential converter and the 50Ω output buffer consumes 2mA, 3mA and 10mA, respectively.

The RGCAF TIA has a transimpedance gain of 48dBΩ. The signal to differential converter has a voltage gain of 3dB with a bandwidth of 10GHz. The 50Ω output buffer provides a 1 dB voltage gain. The RGCAF TIA's bandwidth is limited by the loading effect of the large input capacitance and the total optical receiver bandwidth is further reduced by the parasitic capacitance associated with the output buffer.

5.1.3.3 Simulation Results

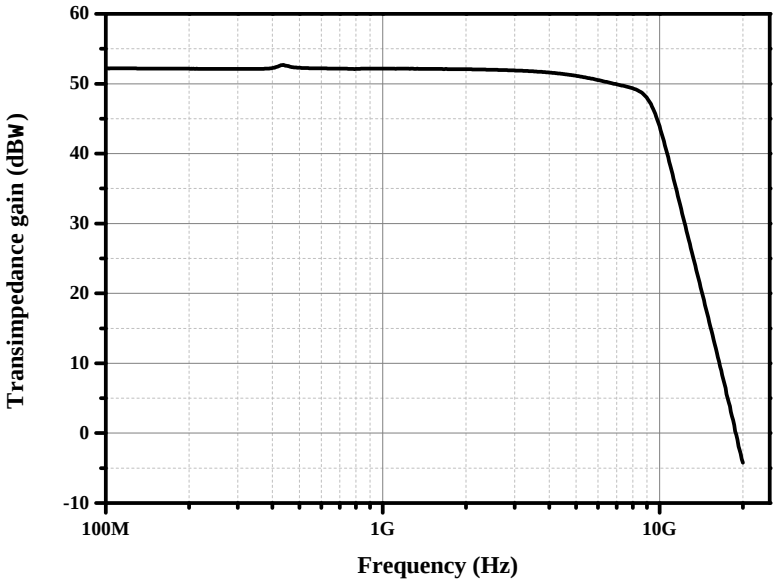

FIGURE 5.40: Simulated frequency response of the RGCAF optical receiver.

The post-layout simulations are presented in this section. In these simulations the parasitic capacitances and resistances of the amplifying chain are included. The parasitic bondwire inductance are included. The optical receiver is optimized for an external 10Gbps GaAs PIN photodiode with a capacitance of 0.25pF (TPD-8D12-652) and additional parasitic capacitance of the ESD protection and the pad of 0.15pF.

The small signal frequency response of the RGCAF optical receiver is shown in figure 5.40. The overall transimpedance gain is 52.2dBΩ and the -3dB bandwidth is 8.2 GHz. Since the parasitic bonding inductance and input capacitance are included in the simulation, the bandwidth is extended due to the resonance effect of these parasitics. Therefore, the simulated -3dB bandwidth is expected to decrease due to the increase of the input capacitance in real life. The input impedance of the RGCAF TIA is shown in figure 5.41, it achieves a 22Ω input impedance at DC.

The simulated group delay frequency response of the RGCAF TIA is shown in figure 5.42. According to figure 5.42, the group delay is about 110ps ± 20ps, which shows about ±20% variation over the specified range for a data rate of 10Gb/s.

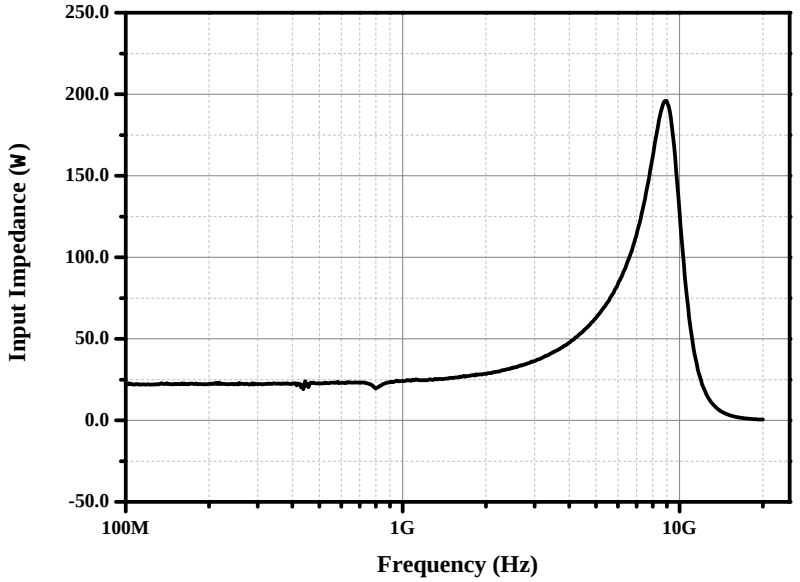

FIGURE 5.41: Simulated input impedance of the RGCAF optical receiver.

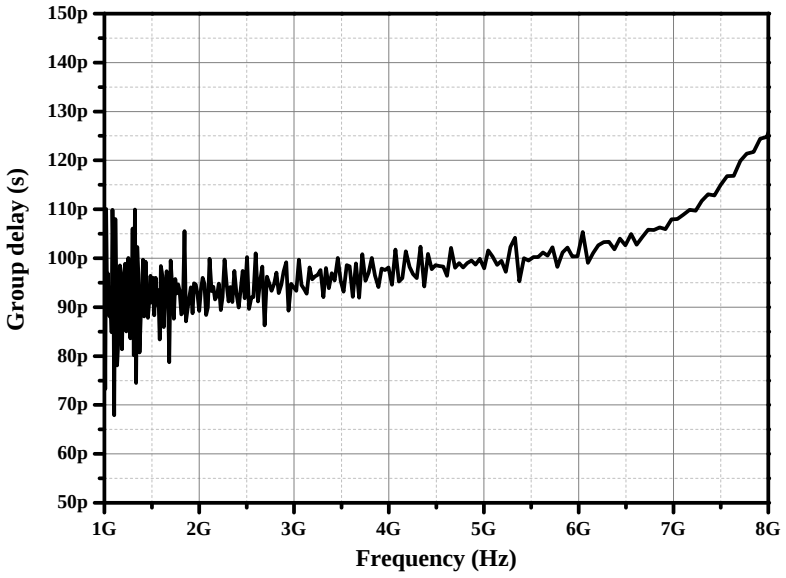

FIGURE 5.42: Simulated group delay of the RGCAF optical receiver.

The simulated input referred noise current and the output noise voltage behaviour are shown in figures 5.43 and 5.44, respectively. The average input referred noise current density is 25 pA/Hz$^{1/2}$ at 1 GHz. The integrated input referred noise current from DC to 10GHz is 1.61μA and the integrated output noise voltage for the same frequency range is 641μV.

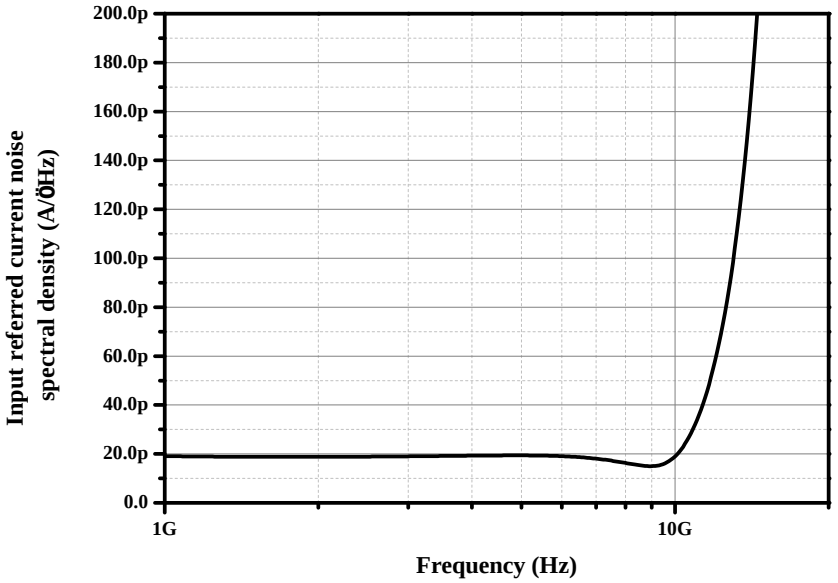

FIGURE 5.43: Simulated input referred current noise spectral density of the RGCAF optical receiver.

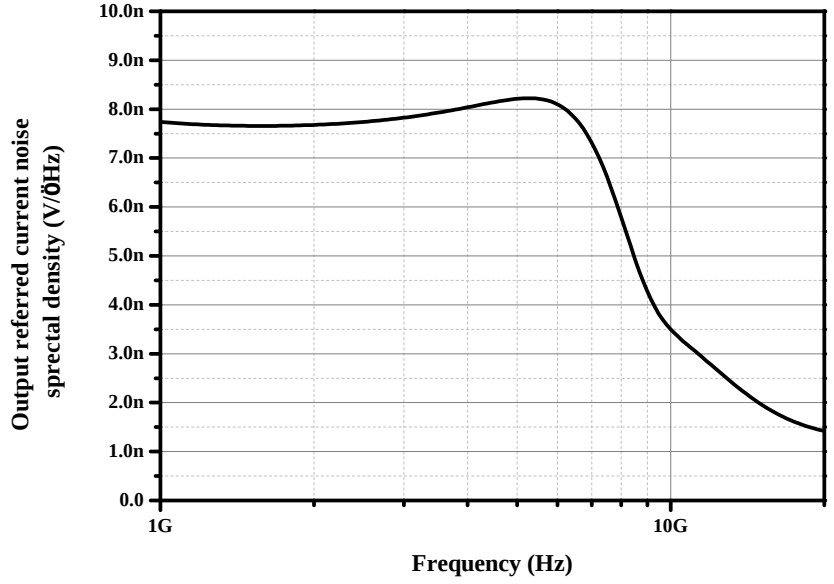

FIGURE 5.44: Simulated output noise voltage spectral density of the RGCAF optical receiver.

5.1.3.4 Chip Layout

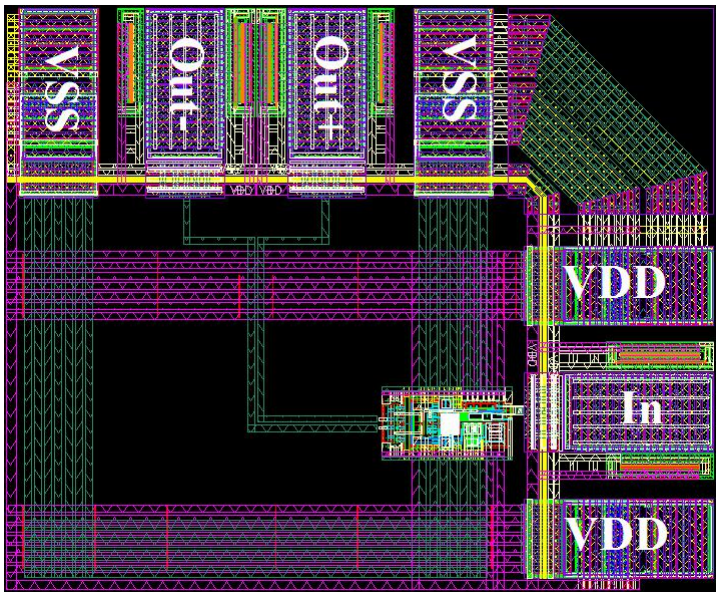

FIGURE 5.45: The layout of the RGCAF optical receiver.

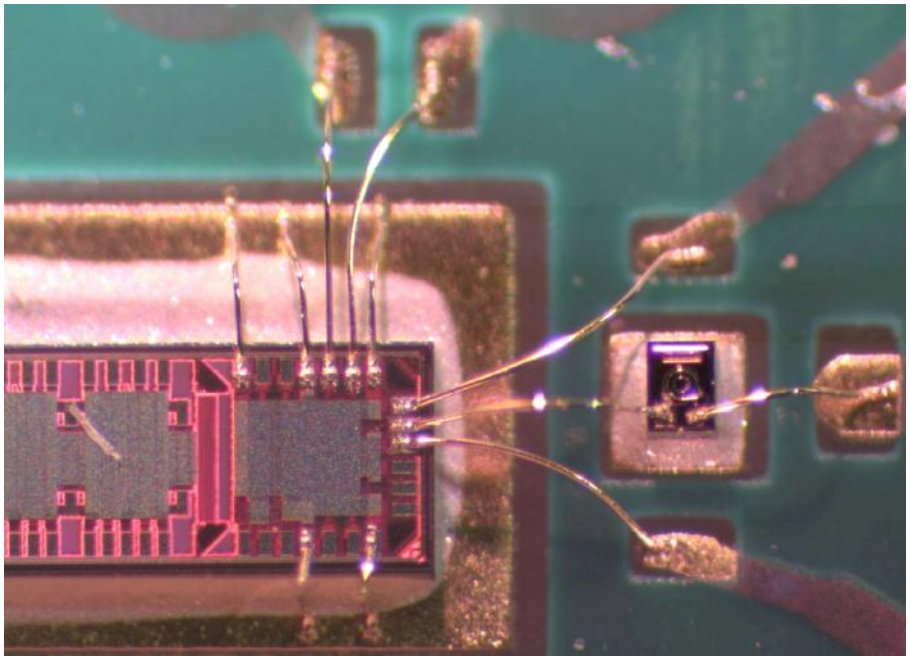

FIGURE 5.46: Chip photo of the RGCAF optical receiver bonded to an external photodiode.

The chip layout shown in figure 5.45, it occupies around $350\mu m \times 480\mu m$. The active area is $44\mu m \times 89\mu m$. The area is mainly occupied and defined by the input/output pads. The RGCAF optical receiver is placed very close to the input pad to avoid the parasitic resistance of long metal lines which increases the input impedance of the TIA and hence degrades the bandwidth of the receiver. Figure 5.46 is a photo of the RGCAF optical receiver connected to an external 10GHz photodiode.

5.1.3.5 Measurement Results

For measurements, a laser diode with a wavelength of 1.55μm was modulated with a 12Gb/s pattern generator. For frequency response measurement, one end of the differential output of the receiver is connected to the network analyser and the other end is terminated with a 50Ω termination. The frequency response of the RGCAF optical receiver is shown in figure 5.47, the -3dB cutoff frequency is 5.9GHz. The measured -3dB cutoff frequency is lower than the value expected from simulation, due to the parasitics added by the PCB.

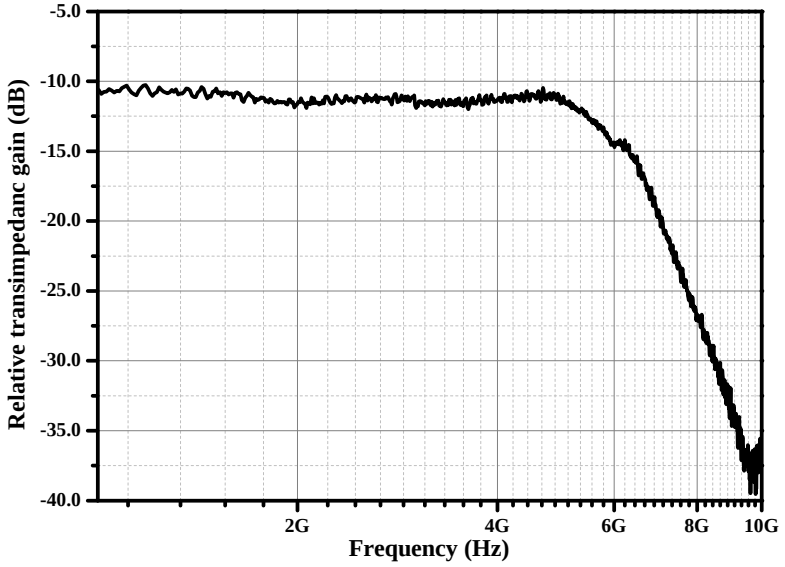

FIGURE 5.47: Measured frequency response of RGCAF optical receiver.

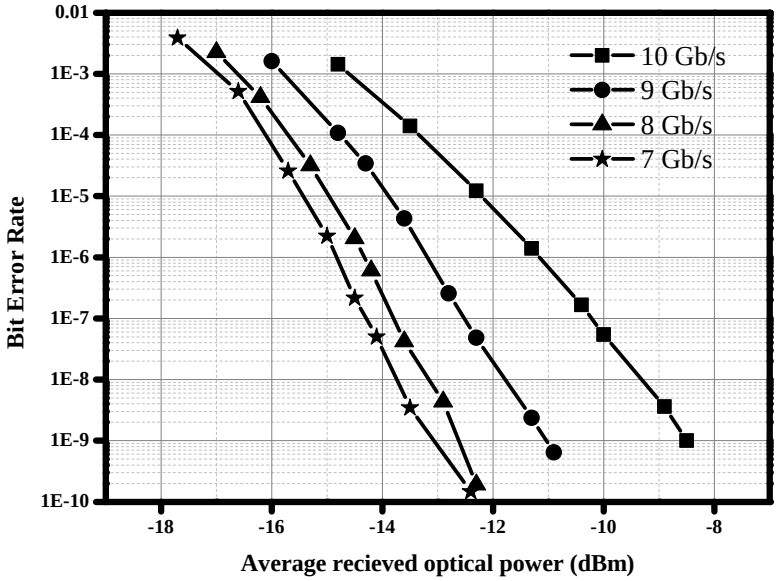

FIGURE 5.48: Measured BER vs average optical power for data rates of 7Gb/s, 8Gb/s, 9Gb/s and 10Gb/s for $\lambda = 1.55\mu$m.

For bit error rate measurements, a bit error analyser is used to count the failing bits. In this measurement, the laser diode was modulated from a pseudo random bit sequence (PRBS) generator. The bit error rate (BER) was measured for different power levels and a length of PRBS of 2^{23}-1. In figure 5.48, the BER vs different input power levels at 7Gb/s, 8Gb/s, 9Gb/s and 10Gb/s are shown for a wavelength of 1.55μm. The sensitivity for a BER of 10^{-9} is -13.2dBm, -12.6dBm, -11dBm and -8.5dBm at 7Gb/s, 8Gb/s, 9Gb/s and 10Gb/s, respectively.

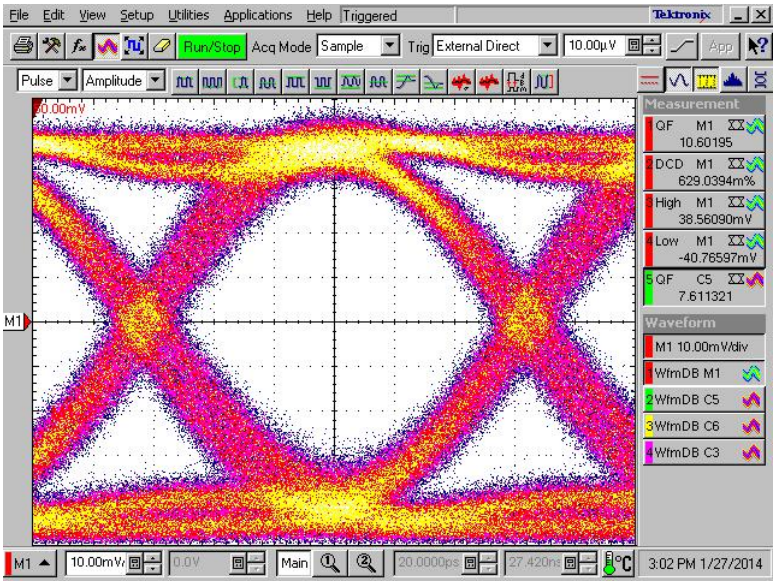

FIGURE 5.49: Measured eye diagram for 8Gb/s at input optical power of -5dBm with BER=10^{-9}.(Horizontal scale: 20 ps/div., vertical scale: 10 mV/div.)

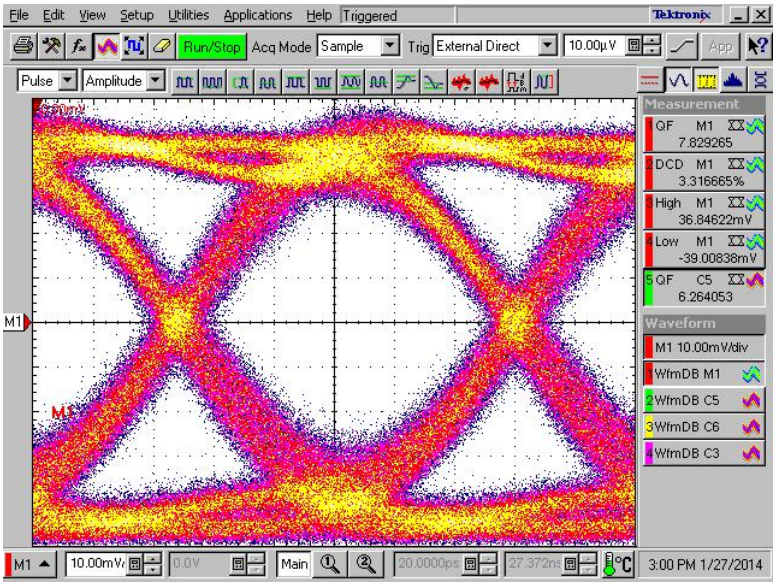

FIGURE 5.50: Measured eye diagram for 9Gb/s at input optical power of -6dBm with BER=10^{-9}.(Horizontal scale: 20 ps/div., vertical scale: 10 mV/div.)

In figures 5.49, 5.50 and 5.51, the eye diagrams for average optical input power of -5dBm at a data rate of 8Gb/s, -6dBm at a data rate of 9Gb/s and -8dBm at a data rate 10Gb/s are shown, respectively.

The overall transimpedance gain of the RGCAF optical receiver is 48dBΩ (251Ω). The chip consumes 15mA from 1.2V supply voltage, leading to a power consumption of 18mW.

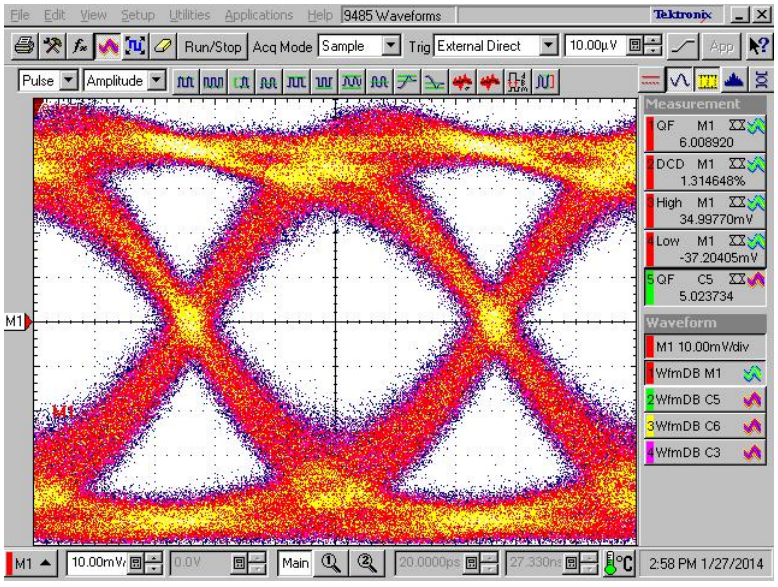

FIGURE 5.51: Measured eye diagram for 10Gb/s at input optical power of -8dBm with BER=10^{-9}.(Horizontal scale: 20 ps/div., vertical scale: 10 mV/div.)

5.1.3.6 Summary

A RGCAF optical receiver in 40nm standard CMOS technology is introduced. The proposed design is based on a RGCAF topology. The measurement results show that this optical receiver achieved a transimpedance gain of 48dBΩ (251Ω) and a bandwidth of 5.9GHz for a total input capacitance of 0.45pF. The sensitivity for a BER of 10^{-9} is -8.5dBm at 10Gb/s. The presented receiver consumes 15mA from 1.2V and occupies an active area of 44μm × 89μm chip area.

TABLE 5.1: TIAs performance summary and comparison with the state-of-the-art.

	Data Rate (Gb/s)	**TIA Power Consumption (mW)**	**Total Power Consumption (mW)**	**Supply Voltage (V)**	**Sensitivity**	**CMOS Process (nm)**	**Active Area (μm^2)**	**TIA Power Efficiency (mW/Gbps)**	**Input Capacitance (pF)**
[19]	20	2.2	-	1	-8dBm (BER of 10^{-12})	80	140 × 70	0.11	0.32
[7]	10	53	210	1.8	-12dBm (BER of 10^{-12})	180	1028 × 1796	5.3	0.15
[12]	5	14	-	1.8	-	130	210 × 90	2.8	1
[26]	10	18.6	-	1.8	-13.8dBm (BER of 10^{-12})	130	400 × 250	1.86	0.3
[31]	10	49	98	2	22.4μA (BER of 10^{-12})	130	230 × 260	4.9	0.25
[37]: T-coil RX	25	6	44.4	1.2	-3.8dBm (BER of 10^{-11})	90	250 × 390	0.24	0.08
[45]	28	43.5	137.2	2	-8.2dBm (BER of 10^{-12})	65	400 × 800	1.55	-
[32]	10	9.6	-	1.6	13.3μA_{pp} (BER of 10^{-12})	65	170 × 25	0.96	0.27
[27]	10	10	-	1	-	28	-	1	-
[17]	28	9	46.8	1	-8dBm (BER of 10^{-12})	28	600 × 530	0.321	0.1
PPCM TIA	**10**	**3.24**	**19.2**	**1.2**	**-8.1dBm (BER of 10^{-9})**	**40**	51 × 96	0.324	0.45
CDAF TIA	**8**	**2.4**	**16.8**	**1.2**	**-11.4dBm (BER of 10^{-9})**	**40**	33 × 101	0.3	0.45
RGCAF TIA	**10**	**2.4**	**18**	**1.2**	**-8.5dBm (BER of 10^{-9})**	**40**	44 × 89	0.24	0.45

5.1.4 Comparison

Table 5.1 shows comparison of the three designs to the state-of-the-art. All the values listed in the table are extracted from measurement results. The inductorless TIA designs proposed in this thesis achieve a competitive power efficiency while keeping the area as small as possible. This is at the cost of sensitivity and noise.

In comparison to the TIAs operating at a data rate less than or equal to 10Gb/s, the proposed designs show a significant improvement in power efficiency, while occupying the least active area.

For the TIAs operating at data rates greater than 10Gb/s, the RGCAF TIA shows very comparable power efficiency performance. However, the TIA design in [19] shows a better power efficiency performance than the RGCAF TIA, it occupies 2.5 times the area occupied by RGCAF TIA. The difference in area between the two designs is due to the four spiral inductors used in [19] to achieve a data rate of 20Gb/s.

Although the designs in [27] and [17] are implemented in 28nm CMOS technology, the CDAF and RGCAF TIAs achieve better power efficiency performance proving that the improvement in power efficiency is not linked to faster CMOS technologies, it is related more to the design.

5.2 Laser Diode Driver

5.2.1 High Voltage Laser Diode Driver

5.2.1.1 Proposed Laser Driver Design

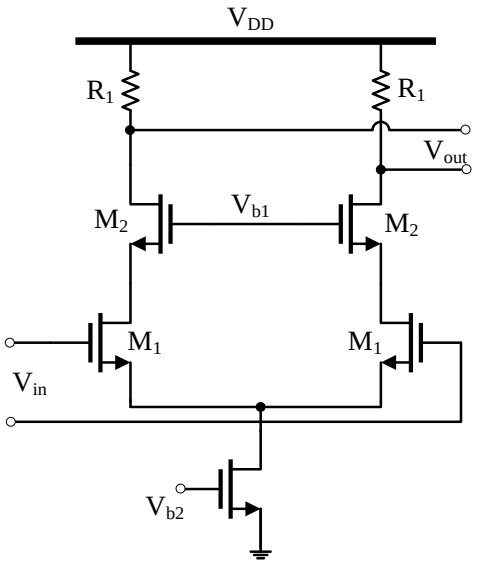

FIGURE 5.52: Output stage of a LDD using the single cascode transistor concept.

A classical way to implement a high voltage LDD in submicron CMOS technology is a differential pair with a single cascode transistor as shown in figure 5.52.

A single cascode topology allows the usage of a supply voltage up to 2.5V in 40nm CMOS technology. Higher supply voltages may introduce a breakdown through the gate-drain junction, oxide breakdown and hot-carrier degradation. To overcome this problem and ensure reliable operation, the cascode transistors are implemented using thick gate oxide devices [28] to isolate the core devices from the power supply. The low transit frequency of the thick gate oxide devices poses a disadvantage to this approach at high frequency, leading to the use of bandwidth broadening techniques such as inductive peaking, which increases the complexity of the design.

The LDD design described here uses the double cascode approach to be able to sustain supply voltages up to 5V and achieve the targeted speed without the use of inductors [15].

The high voltage LDD for GPON communications at 3Gb/s is designed in 40nm CMOS technology. The LDD is fully differential and consists of three main blocks: the input stage, the pre-driver and the output stage, as shown in 5.53.

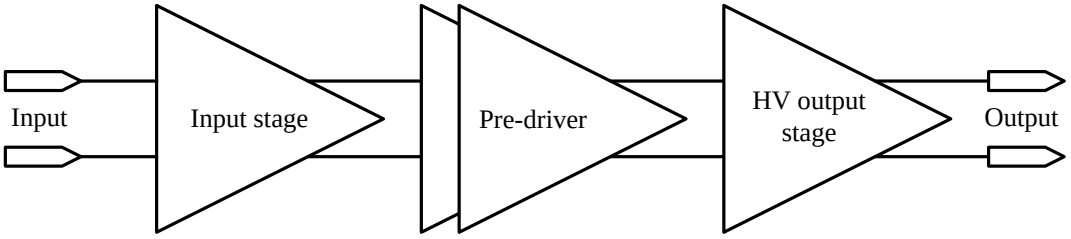

FIGURE 5.53: Simple block diagram of the LDD.

5.2.1.2 Input Stage and Predriver

The 50Ω input stage (figure 5.54) is needed for measurements [M_1, R_1 and R_2]. The 50Ω input resistance provides matching to the pattern generator. The input stage is a common-gate circuit with a 50Ω source resistance at a supply voltage of 1.1V. The output of the 50Ω stage is connected to an inverter stage in the 1.1V domain. The inverters [M_2 and M_3] act as pre-pre-drivers, which are implemented with wider transistors to drive a larger output load capacitance. The target is to boost the input signal for the output load of the pre-driver. The pre-driver is a differential NMOS pair with resistive loads [M_4, R_3, M_5 and M_6] at a supply voltage of 1.1V as well. It is used for further signal amplification and to drive the high gate capacitances of the output stage's input transistors [M_7]. The voltage gain of the pre-driver and the input stage $A_v(s)$ is

$$A_v(s) = \overbrace{\frac{g_{m1}R_2}{1+sR_2C_{o1}}}^{\text{Input Stage}} \cdot \overbrace{\frac{(g_{m2}+g_{m3})(r_{ds2} \parallel r_{ds3})}{1+s(r_{ds2} \parallel r_{ds3})C_{o2}}}^{\text{Inverter Stage}} \cdot \underbrace{\frac{g_{m4}(R_3 \parallel r_{ds4})}{1+s(R_3 \parallel r_{ds4})C_{o3}}}_{\text{NMOS Differential Pair}}, \tag{5.28}$$

where C_{o1} is approximately equal to the summation of C_{gs2}, C_{gs3} and the Miller capacitance of C_{gd2} and C_{gd3}, C_{o2} is approximately the sum of C_{gs4} and the Miller capacitance of C_{gd4} and C_{o3} is approximately the input capacitance of the LDD's output stage.

To ensure the stability of this stage, special focus was laid on the output resistance of the pre-driver in order to keep the parasitic pole far away from the desired frequencies.

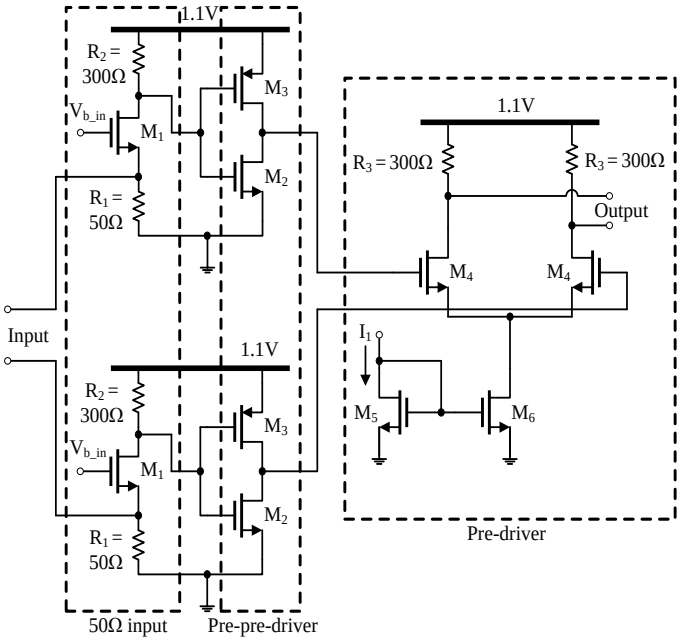

FIGURE 5.54: The 50 Ω input stage, inverter and pre-driver operating at 1.1V supply voltage.

5.2.1.3 LDD's Output Stage

The LDD's output stage [M_7, M_8, M_9, M_{10}, M_{11}, M_{12} and R_4] shown in figure 5.55 is capable of a 5V power supply. For speed purposes only thin gate oxide transistors layouted as RF transistors are used. It has an open-drain output at which the laser diode (for instance the laser diode EBS63432-141 having an equivalent resistance of 10Ω) can be connected.

For measurement instead of the laser diode a 10Ω resistor is placed and a matching network [11] to the 50Ω measurement equipment is connected. The current through the laser diode is switched between the two branches of the differential LDD (assuming that there is an additional DC current path to bias the laser diode always above its threshold current). This current-switching has benefits in speed of the LDD's output stage, because M_7-M_9 do not have to carry this DC current in addition and their widths are smaller. The laser diode current swing can be set by the cascode current source [M_{10} and M_{11}] of the LDD. Because of the strongly temperature dependent optical output power of the laser diode a large laser diode current range is needed. Laser diode currents up to 100mA can be processed by the LDD. The laser diode current of the LDD can be set by an external reference current. The high supply voltage operation of the LDD is dangerous for the thin gate oxide transistors. All biasing voltages and currents of the LDD have been set to guarantee safe operating points for all transistors. Therefore a doubled cascode structure [M_8 and M_9] and a cascode tail current source [M_{10} and M_{11}]

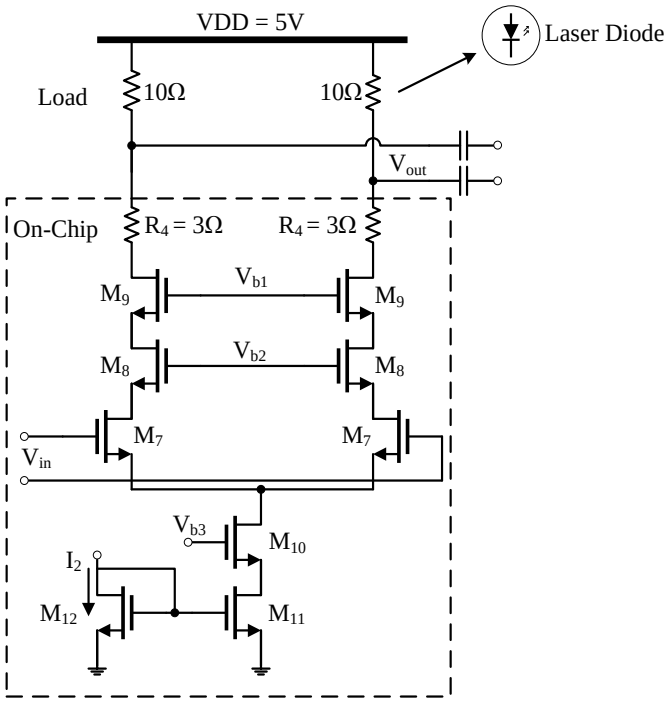

FIGURE 5.55: Output stage of the LDD operating at 5V supply voltage.

are implemented. This has two main advantages: the high supply voltage is distributed between the cascodes and the Miller effect of the input transistors [M_7] is reduced making the circuit faster. Correct bias voltages of the cascodes guarantee the safe operation of the laser driver.

For improvement of the ESD protection, M_9 are implemented with a serial resistance. Each finger of the transistor M_9 has a resistance of 650 Ω, which is in sum approximately 3 Ω. Additionally silicon-controlled rectifiers (SCR) were added at all input, bias, and output pins to protect the laser driver and ensure the reliability of the design.

5.2.1.4 Measurement Results

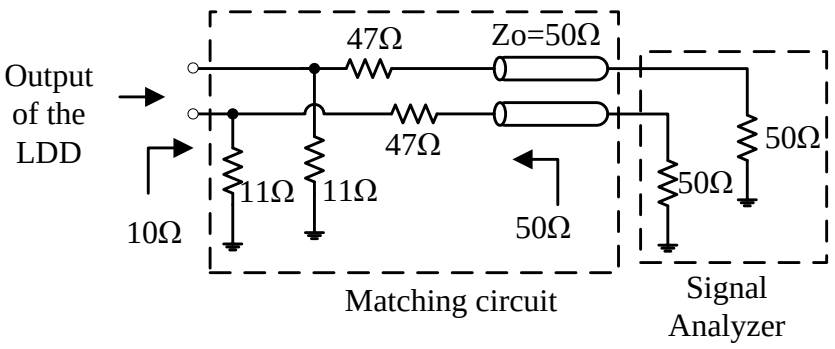

FIGURE 5.56: Off-chip 50 Ω matching output circuitry.

The pre-driver (figure 5.54) and the output driver (figure 5.55) are fabricated in 40nm standard CMOS technology. The chip photo is shown in figure 5.57. The area of the complete LDD chip is 1mm × 0.56mm. The active area of input stage, predriver and output stage together is 296μm × 85μm. The rest of the chip area is filled with bondpads, ESD protection circuits and block capacitors. The chip consumes 10mA from 1.1V and 80mA from 5V for a modulation current of 80mA. The LDD has an operating data rate of 3 Gb/s.

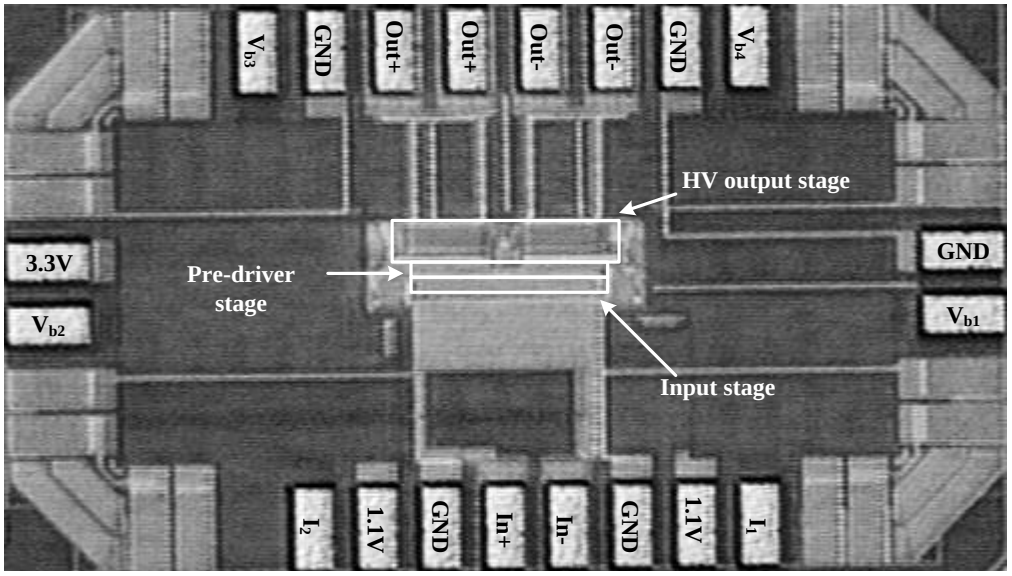

FIGURE 5.57: Micrograph of the high voltage LDD.

The LDD must drive a 10Ω load resistance (equivalent resistance of the communication laser diode), making the measurement of the circuit very difficult with 50Ω measurement equipments. Therefore the matching circuit shown in figure 5.56 was used off chip to provide 50Ω matching to the signal analyser and 10Ω matching to the LDD output. The matching circuit is in parallel configuration with the 11Ω load resistance, resulting in the same equivalent load resistance as realised by the LDD. Due to this matching circuit (voltage divider by 1/2), the output voltage measured with the oscilloscope is attenuated by 50%.

Table 5.2 compares the measurement results of the introduced LDD to the state of the art. Unfortunately, only a small number of publications of high voltage LDD in nanometer CMOS technology are available. Therefore, older submicron CMOS technologies are involved in the comparison. The comparison shows that this design sustains a high modulation current of 80mA, which is higher than that of the designs described in [47], [6], [11] and [28] with comparable bandwidth. The LDDs introduced in [23] and [28] achieve a higher data rate due to the use of an inductive peaking technique requiring large chip area. Although the introduced LDD is designed in 40nm standard CMOS technology, it sustains a much higher supply voltage than [23] and [28].

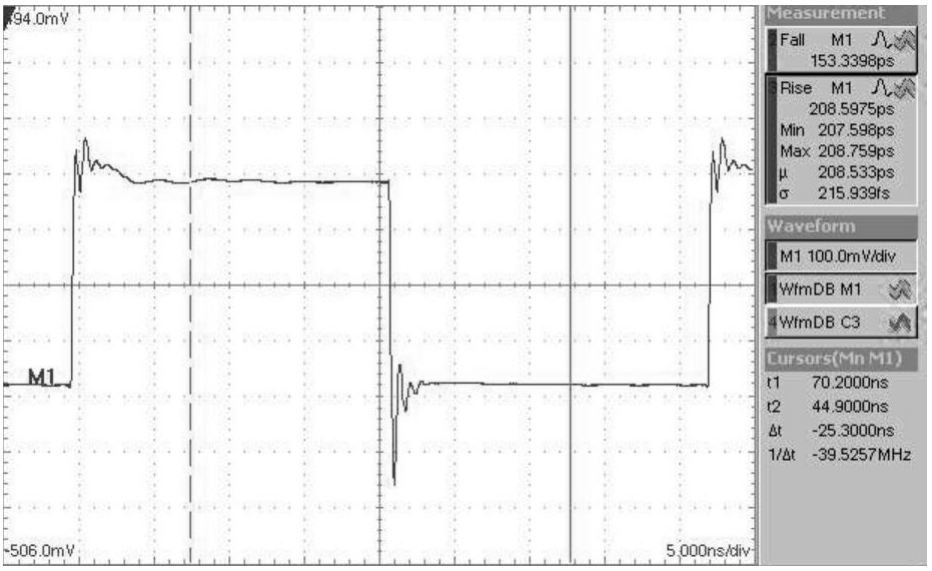

FIGURE 5.58: Electrical step response of the laser diode driver.(Horizontal scale: 5 ns/div., vertical scale: 100 mV/div.)

The electrical step response of the LDD was measured at 10Ω load using a Tektronix DSA8200 digital signal analyser (see figure 5.58). The rise/fall time is measured at 10% - 90% of the output voltage swing. The measured rise/fall times are 209ps and 153ps, respectively. This leads to a conservative bandwidth estimate of 1.67 GHz which fits to the proposed data rate of 3Gb/s. The peak to peak output voltage is 400mV implying that the actual peak to peak voltage of the LDD is 800mV.

5.2.1.5 Summary

A high-voltage LDD in 40nm CMOS technology was introduced. Using the double cascode open drain circuit topology, the LDD sustains 4.5 times the nominal supply voltage of the technology. The LDD achieves a data rate of 3Gb/s with rise and fall times (10%-90%) of 209ps and 153ps, respectively, for a modulation current of 80mA. The presented LDD is appropriate for infra-red, near infra-red and red laser diodes.

TABLE 5.2: LDDs performance summary and comparison with the state-of-the-art.

	Data Rate (Gb/s)	**Modulation current (mA)**	**Supply Voltage (V)**	**Rise Time (ps)**	**Fall Time (ps)**	**CMOS Process (nm)**
[47]	2.5	60	5	-	-	350
[6]	2.5	20	3	190 (10%-90%)	240 (10%-90%)	350
[11]	3.8	60	2/3.3	104 (20%-80%)	109 (20%-80%)	250
[23]	10	100	1.8	-	-	180
[28]	5	24	2.5	-	-	130
Proposed Design	**3**	**80**	**5**	**209 (10%-90%)**	**153 (10%-90%)**	**40**

Chapter 6

Conclusion

This thesis studies and examines the challenges in the design of optoelectronic circuits in standard nanometer CMOS technology. It presents a number of solutions to simplify the implementation of cost efficient, low power and high performance optical links. This work introduced new circuit solutions for critical blocks of both optical receivers and transmitters.

On the receiver side, three new circuit topologies were introduced to achieve high speed and low power inductorless TIAs. The use of inductors is mainly avoided to lead to a cost efficient design. The first topology is based on a push pull current mirror (PPCM) TIA. The PPCM TIA is a current mode TIA which showed a better response compared to the classic NMOS current mirror TIA. The second topology is a TIA with an active feedback. The active feedback was designed in a common drain configuration. The third topology is a regulated cascode TIA with a boosting feedback amplifier. It is an improved topology based on RGC TIA which achieves a significantly lower input impedance leading to high speed performance at low power consumption. The proposed designs are implemented in 40nm CMOS technology with a supply voltage of 1.2V. In comparison to the state-of-the-art, the three TIAs achieve a competitive performance in terms of power and area efficiency to exiting TIAs in literature.

On the transmitter side, a high-voltage LDD in 40nm CMOS technology was designed using only thin oxide transistors to achieve maximum speed. Using the double cascode open drain circuit topology, the LDD sustains 4.5 times the nominal supply voltage of the technology and delivers a high modulation current of 80mA. The presented LDD is appropriate for infra-red, near infra-red and red laser diodes.

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