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Multiphase Switch-Mode BCM Controllers – Design Challenges in CMOS Implementation

supervised by

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Abstract

As population and demand for energy grow, global fossil fuel reserves decline at an alarming rate. The industry has responded with increasingly aggressive and environmentally destructive extraction techniques to supply the global energy demand. For example, oil extraction from the open tar sands pits in Canada is creating a massive environmental dead-zone which will be large enough to be seen from the moon. But declining reserves and environmental damage are only part of the problem; energy-related trade deficits burden entire countries with loans to central banks that can never be repaid, and interest payments that compound the debt.

Fortunately engineering is responding to the problem, and significant progress is being made. Local distributed energy production from renewable resources is reducing some of the burden in meeting the growing demand for energy, and large untapped reserves exist. But the silent revolution occurring is improved device and system efficiency. For instance, LED lights produce the same luminous flux at 8W that a 60W incandescent bulb once produced. Distributed among millions of homes, such energy-saving devices are having a far larger impact than could be seen from new energy production.

Advances in power systems are equally impressive. Today, a state-of-the-art commercial 50kW power converter operating at hundreds of amps will have a conversion efficiency exceeding 99%. But improvements in consumer goods have a potentially larger energy-saving impact. New consumer products should have high operational efficiencies *and* large converter dynamic range to reduce the vampire load in standby mode. Switch-mode efficiency is optimized by minimizing the combined switching, ohmic, and core losses. Multiphase systems help distribute the load, reducing losses and filter requirements, and improving the power factor. In this thesis some of the improvements that have been developed and new trends in published research are reviewed. The discussion is organized as follows:

- Chapter 1: The relative advantages and disadvantages of switch-mode operating modes are discussed. A comparison of the ohmic, switching, and magnetic core losses is made between continuous conduction (CCM) and boundary conduction (BCM) operating modes.
- Chapter 2: A survey of multiphase (master-slave) BCM controllers is made. Open-loop controllers in both current- and voltage-mode are compared for stability and relative advantages/disadvantages. A promising alternative to open-loop control is the closed-loop controller. It has a wider range of stable voltage-mode operation, provided technical issues are resolved in the design. A developing trend in multiphase converters is the coupled-inductor design; the windings of two or more phases are wound on the same magnetic core. Energy is coupled directly from the magnetizing phase to the demagnetizing phase via the mutual coupling, thus reducing the energy stored in the core. Such coupling can improve efficiency by reducing the core and ohmic losses.
- Chapter 3: The industry trend is toward cheaper, compact integrated designs; an investigation is made into the practical issues of integrating a switch-mode controller in silicon. While the nominal design is straightforward, many problems are encountered when temperature effects, CMOS process variations, and component mismatches are included. Central to timing generation is a current reference, and various feedback techniques to help stabilize the current source against process and temperature are examined. A typical current source will have a 50% process-related current spread, and current mirroring into the nano-amp range adds a 30% mirroring error. A dual-slope ramp with correlated double sampling is used to cancel these errors, and only a 2% tracking error is seen in the final timing. Comparators are another component of the timing circuit with process-related problems. A rail-to-rail comparator with input hysteresis can latch at the rails on certain process corners; the comparator is also plagued with low gain on some process corners and input voltages. These problems could leave the controller in an uncontrolled (latched) or unknown (meta-stable) state, with disastrous consequences for the converter. To guarantee a robust design, these errors cannot be allowed to occur under any combination of process variation, operating condition, and system noise. Reset injection charge was used to prevent comparator latching errors. Additionally, a digital pulse-width conditioning circuit and the comparator output slew rate form a bandpass filter for system noise; when a minimum output slew rate is guaranteed, the bandwidth of this filter goes to zero and the design guarantees a meta-stable condition can never occur. The most challenging aspect of CMOS integration was the dynamic range that could be guaranteed by the design; a nominal-model dynamic range of 200 dropped to only 50 when the process corners were considered, and some corners saw high chip failure rates. The strategic use of injection charge, and delayed injection charge cancellation, was explored to address these problems. But to be truly competitive with discrete controllers, a nonlinear adaptive current reference is proposed that guarantees a dynamic range of more than 200. Such adaptations provide the needed performance to compete with discrete voltage-mode controllers, and to classify it as a “universal” BCM controller design.

- Chapter 4: In this chapter an investigation is made of a class of hybrid converters capable of supplying two power outputs. These converters are useful in systems where a high-voltage output interfaces to a power train or utility grid, and a low-voltage output drives control systems. The boost-flyback converter is capable of adaptively directing power to two outputs, with charging priority given to the output with the heaviest load. This adaptive nature of the converter simplifies the controller requirements and hardware. However, a problem encountered with high-voltage flybacks is the inter-winding capacitance. In a high-voltage, low-current secondary circuit the energy needed to charge and discharge this capacitance can exceed the energy in the inductor windings. When this happens the converter will not start up, and the minimum power the converter can operate at is increased. The problem is addressed in the transformer design by reducing the parasitic capacitance of the windings. Depending on the design, the number of winding layers, wire density per layer, dielectric thickness between layers, direction the secondary is wound with reference to the primary, selecting which secondary layer is closest to the primary, selecting how the layers are wound, and the circuit configuration can be designed to reduce the winding capacitances. Design examples are discussed, and test results for a 330V design capable of operating down to a watt is shown.

BCM converters are an important emerging class of energy-saving power systems; in this thesis the question is raised as to whether a BCM controller implemented in silicon can achieve the same performance seen in controllers implemented with discrete components. Two requirements were imposed on the conceptual model. First, no failures should occur as the result of any combination of CMOS process variations, component mismatch errors, and converter operating conditions; preventing these failures means that some expensive production testing can be avoided. The second requirement was that the dynamic range should be large enough that a “universal controller” is developed. The dynamic range must be the guaranteed range when all process corners are considered. This would create portability, allowing the same controller to be used in different product designs.

6-sigma simulations are not sufficient to guarantee design robustness. A better approach is to look for mismatch errors using Monte Carlo simulation run from the weak process corners. The conclusions are drawn from these simulations and testing.

Although many problems were encountered, and every solution seemingly created new problems, in the end these problems were resolved through design. The conclusion then is that power systems controllers can be implemented in CMOS with no loss of controller performance. For large-scale production, replacing a PC board full of components with a single chip offers an attractive option in reducing product size, weight, and manufacturing costs. It is an option that should be considered seriously.

Kurzfassung

Aufgrund des Wachstums der Weltbevölkerung und des daraus resultierenden immer höher werdenden Energiebedarfs, steigt der globale fossile Brennstoffverbrauch bei endlichen Reserven alarmierend an. Daher versucht die Industrie, diesem mit immer aggressiveren und immer umweltbelastender werdenden Fördermethoden entgegenzuwirken. Als Beispiel kann hier die Ölgewinnung aus Ölsand im Tagbau in Kanada genannt werden, welche eine massive ökologische Todeszone zur Folge hat, die sogar bald vom Mond aus zu sehen sein wird. Die immer geringer werdenden fossilen Brennstoffreserven, als auch die Umweltverschmutzung sind nur ein Teil des Problems. Aufgrund eines energiebedingten Handelsbilanzdefizits sind ganze Staaten dazu gezwungen, Kredite bei den jeweiligen Zentralnotenbanken aufzunehmen, welche aber nie zurückgezahlt werden können und darüber hinaus zusätzliche Belastungen aufgrund von Zinszahlungen bewirken.

Glücklicherweise nehmen sich die Ingenieurwissenschaften dieses Problems an, wobei signifikante Fortschritte gemacht werden. Lokale Energiegewinnung aus erneuerbaren Ressourcen vermindert einige Probleme, die durch den steigenden Energiebedarf versursacht werden, und in diesem Bereich sind noch einige Reserven vorhanden, die noch nicht genutzt werden. Die stille Revolution erfolgt auch aufgrund von optimierten Geräten und verbesserter Systemeffizienz. Als Beispiel können hier LED-Lampen angeführt werden, die bei einem Leistungsverbrauch von 8W die gleiche Beleuchtungsstärke wie eine alte 60W Glühbirne liefern. Bei einer flächendeckenden Verwendung durch Millionen von Verbrauchern haben solche energiesparenden Mittel eine viel größere Wirkung als die Erzeugung neuer Energien.

Der Fortschritt im Bereich der Stromversorgung ist beindruckend. Nach dem heutigen Stand der Technik hat ein industrieller 50kW Stromrichter, welcher bei Stromstärken von mehreren Hundert Ampere arbeitet, einen Wirkungsgrad, der sogar 99% überschreiten kann. Aber Verbesserungen und Optimierungen in elektrischen Konsumgütern haben einen potentiell noch größeren Energiespareffekt. Neuere Konsumgüter sollten dabei eine hohe Effizienz aufweisen und eingebaute Konverter sollten einen hohen Dynamikbereich besitzen, um den parasitären Verbrauch im Stand-by Modus zu verringern. Der Wirkungsgrad von Schaltnetzteilen kann mittels einer kombinierten Minimierung von Schaltverlusten, ohmschen Verlusten und Transformatorverlusten optimiert werden. Multiphasensysteme helfen die Last zu verteilen, die Verluste und Filteranforderungen zu reduzieren und den Leistungsfaktor zu verbessern. In dieser Masterarbeit werden einige Verbesserungen, die entwickelt wurden und die neue Trends in der Forschung darstellen, behandelt. Die Arbeit ist, wie folgt, aufgebaut:

- Kapitel 1: Die jeweiligen Vor- und Nachteile von verschiedenen Ansätzen in der Arbeitsweise von Schaltnetzteilen werden behandelt. Es wird ein Vergleich der ohmschen Verluste, der Schaltverluste und der Transformatorkernverluste bei einem Continuous-Conduction-Mode Wandler (CCM, Betrieb mit kontinuierlichem Strom) und einem Boundary-Conduction-Mode Wandler (BCM) angestellt.
- Kapitel 2: Ein Überblick über Multiphasen (Master-Slave) BCM Regelungen wird gegeben. Dabei werden verschiedene Steuerschaltungen ohne Regelkreis (sowohl Strom-, als auch als Spannungsregler) betrachtet und deren Stabilität, Vor- und Nachteile verglichen. Eine vielversprechende Alternative zur offenen Regelung sind Steuerschaltungen in einer geschlossenen Regelschleife. Diese haben einen weiten stabilen Bereich im Spannungsbetrieb, unter der Voraussetzung, dass einige technische Probleme gelöst werden. Ein Entwicklungstrend im Bereich der Multiphasenkonverter ist ein Design mit gekoppelten Spulen; die Windungen von zwei oder mehr Phasen sind auf demselben magnetischen Kern aufgewickelt. Die Energie wird direkt von der Magnetisierungsphase zur Entmagnetisierungsphase über gegenseitige Kopplung übertragen, wobei die Energie, welche im Kern gespeichert ist, vermindert wird. Solch eine Kopplung kann die Effizienz durch Reduzierung der Kernverluste und der ohmschen Verluste verbessern.
- Kapitel 3: Der Trend in der Industrie geht in Richtung billiger und kompakt integrierter Lösungen; eine Untersuchung der praktischen Aspekte von integrierten Schaltwandlersteuerungen in Silizium wurde gemacht. Obwohl das zugrundeliegende Schaltungskonzept unkompliziert wirkt, treten viele Probleme auf, da man Details wie Temperatureffekte, CMOS Prozessvariationen und Bauteildiskrepanzen mitberücksichtigen muss. Die Erzeugung einer Zeitbasis für die Schaltvorgänge basiert auf einem Referenzstrom. Daher werden unterschiedliche Rückkoppeltechniken, die die Stromquelle gegen Temperatur- und Prozessvariationen stabilisieren sollen, untersucht. Eine typische Stromquelle hat eine prozessverursachte Stromvariation, ausgehend vom nominalen Wert, von 50%, wobei einfache Stromspiegel für den Nano-Amperebereich noch 30% Fehler hinzufügen. Die Fehler werden mit Hilfe von einem Zweirampenansatz (positive und negative Steigung) mit korrelierter Doppelabtastung behoben, wobei als Resultat nur mehr 2% Fehler in der resultierenden Zeitgebung auftreten. Weitere Komponenten der Zeitgeberschaltung, wo prozessbezogene Probleme entstehen können, sind Komparatoren. Ein Komparator mit Eingangshysterese und mit einem Ausgangsspannungshub, der den kompletten Versorgungsspannungsbereich abdeckt (rail-to-rail), kann aufgrund des Auftretens von extremen Prozessungleichheiten falsch schalten, wobei kleine Verstärkungen und niedrige

Eingangsspannungen das Problem vergrößern. Diese Probleme könnten die Steuerschaltung in einem unkontrollierten oder undefinierten (keine Entscheidung des Komparators) Zustand belassen, was schlimme Konsequenzen für den Konverter hätte. Um ein robustes Design zu garantieren, darf nicht zugelassen werden, dass solche Fehler in jeder möglichen Kombination von Prozessvariationen, Arbeitszuständen und Systemrauschen, auftreten. Injizierte Schaltladungen wurden während des Zurücksetzens (Reset) verwendet, um Schaltfehler des Komparators zu vermeiden. Zusätzlich bilden eine Schaltung zur digitalen Pulsbreitenkonditionierung und die Flankensteilheit des Komparators am Ausgang einen Bandpassfilter für das Systemrauschen; wenn eine minimale Ausgangsflankensteilheit sichergestellt ist, geht die Bandbreite dieses Filters gegen Null und ein metastabiler Zustand kann nie auftreten. Die größte Herausforderung in der CMOS-Schaltungsentwicklung war der Aussteuerbereich, welcher vom Design garantiert werden konnte; ein nominaler dynamischer Bereich von 200 sank unter Berücksichtigung von extremen Prozessvariationspunkten auf 50, wobei hohe Fehlerraten in einigen Prozessvariationsecken auftraten. Um eine Lösung dafür zu finden, wurde der gezielte Gebrauch von Schaltinjektionsladungen und verzögerte Injektionsladungsauslöschung untersucht. Aber um wirklich mit diskreten Steuerschaltungen wettbewerbsfähig zu sein, wird eine nichtlineare, adaptive Stromreferenz vorgeschlagen, um einen dynamischen Aussteuerbereich von mehr als 200 zu garantieren. Solche Anpassungen liefern das benötigte Verhalten, um mit diskreten Spannungsreglern konkurrieren zu können und um das Design als „universelle“ BCM Schaltung zu klassifizieren.

- Kapitel 4: In diesem Kapitel wird eine Klasse von Hybridwandlern untersucht, die zwei Ausgänge zur Versorgung besitzen. Diese Wandler werden in Systemen gebraucht, wo ein Hochspannungsausgang an ein Aggregat oder ein Servicenetz angekoppelt wird und wo gleichzeitig ein Niederspannungsausgang Kontrollsysteme versorgt. Der Aufwärtssperrwandler kann die Leistungen, die an zwei verschiedene Ausgänge geliefert werden, anpassen, wobei die höchste Priorität dem Laden jenes Ausgangs mit der größeren Last gilt. Diese Adaptionsmöglichkeit des Wandlers vereinfacht die Anforderungen an den Regler und an die Hardware. Ein Problem, das man bei Hochspannungssperrwandlern antrifft, ist die Kapazität zwischen den Windungen der Spulen. In einer anschließenden Schaltung, die im Hochspannungs- und Niederstrombereich arbeitet, kann die Energie, die zum Laden oder Entladen dieser Kapazitäten gebraucht wird, die Energie in den Spulen übertreffen. In einem solchen Fall kann der Wandler nicht starten und die minimale Leistung, mit der der Wandler arbeitet, ist erhöht. Hier kann beim Design des Transformators Abhilfe geschaffen werden, wobei die parasitären Kapazitäten der Windungen reduziert werden müssen. In Abhängigkeit vom Design können die Anzahl der Windungsebenen, die Drahtdichte per Ebene, die dielektrische Dicke zwischen den Ebenen, die Wicklungsorientierung der sekundären Spule im Vergleich zur primären Spule, die Lage der sekundären Wicklungsebene im Verhältnis zur primären Ebene, die Art der Windung der Ebenen und die Schaltungsstruktur ausgesucht werden, um die Wicklungskapazitäten zu reduzieren. Es werden Beispiele von Designs erörtert und Testergebnisse einer 330V-Lösung, die bis zu einem Watt herab arbeitet, präsentiert.

BCM Wandler sind eine wichtige, aufkommende Klasse von energiesparenden Stromversorgungsystemen. In dieser Arbeit wird die Frage aufgeworfen, ob eine in Silizium integrierte BCM Steuerschaltung die gleiche Arbeitsleistung erreicht wie eine Schaltung, die aus diskreten Bauteilen aufgebaut wurde. Es werden zwei Anforderungen an das konzeptuelle Modell gestellt. Erstens sollten keine Fehler auftreten, die durch mögliche Prozessvariation, durch Bauteilungleichheiten und durch Arbeitsbedingungen des Wandlers entstehen können. Die Vermeidung solcher Fehler bedeutet, dass einige teure Produktionstests unterlassen werden können. Die zweite Anforderung ist, dass der dynamische Bereich groß genug sein soll, sodass eine universelle Steuerschaltung entwickelt werden kann. Der dynamische Bereich muss jener garantierte Bereich sein, wo alle extremen Technologietoleranzecken berücksichtigt sind. Dies würde Übertragbarkeit bringen, wobei dann der gleiche Regler in unterschiedlichen Produkten verwendet werden kann.

6-Sigma Simulationen sind nicht ausreichend, um ein robustes Design zu garantieren. Stattdessen wurden aufgrund von Ungleichheiten wegen der auftretenden Toleranzen der Technologie, Monte-Carlo Simulationen durchgeführt, um schlechte Konstellationen in der Toleranzvariation bei einer gegebenen Bauteilanordnung zu finden. Aus diesen Simulations- und Testergebnissen wurden dann Schlussfolgerungen gezogen.

Obwohl viele Probleme auftraten und jede Lösung scheinbar ein neues Problem hervorgerufen hat, wurde am Ende erkannt, dass diese Probleme durch ein gutes Design gelöst werden können. Schlussfolgernd kann man sagen, dass Stromversorgungssystemsteuerungen in CMOS Technologien ohne Verminderung der Arbeitsleistungsfähigkeit implementiert werden können. Für Großproduktionen wäre das Ersetzen einer Printplatte voller elektronischer Bauteile mit einer einzelnen integrierten Schaltung eine attraktive Option, um Produktgrößen, Gewicht und Produktionskosten zu reduzieren. Diese Möglichkeit sollte ernsthaft in Betracht gezogen werden.

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Contents

Abbreviations & Symbols

A	area
AC	alternating current
A_{center}	cross-sectional area of center
A_{core}	cross-sectional area of core
A_{gap}	effective gap area
AMS	Austria Microsystems
ASIC	application-specific integrated circuit
A_V	differential voltage gain
B	magnetization
B	current mirror gain
BCM	boundary conduction mode
CCM	continuous conduction mode
C	capacitance
C1…	capacitor reference identifier
C_{drain}	drain capacitance
CDS	correlated double sample
C_{DS}	drain-to-source capacitance
C_{gate}	gate capacitance
C_{GD}	gate-to-drain capacitance
C_{GS}	gate-to-source capacitance
CK	clock
CMOS	complementary metal-oxide-semiconductor
CMP	comparator
C_{ox}	gate oxide capacitance
$C'_{primary}$	transformer secondary inter-winding capacitance reflected into the primary
CRT	cathode ray tube
CS	current source
$C_{secondary}$	transformer secondary inter-winding capacitance
CTAT	complimentary-to-absolute temperature
CW	clockwise
D	duty cycle
D1…	diode reference identifier
dB	decibel
DC	direct current
DCM	discontinuous conduction mode
DL	delay line
DP	differential pair
DSL	dynamic switching loss
$\mathcal{E}_{mf}$	electromotive force
EMI	electromagnetic interference
ESD	electrostatic discharge
ESR	equivalent series resistance
f_c	converter frequency
FET	field-effect transistor

FF_M / FF-M	master flip-flop
FF_S / FF-S	slave flip-flop
g_m	transconductance
g_{mb}	transconductance due to body effect
H	magnetic field intensity
H_{core}	magnetic filed in the core material
H_{gap}	magnetic field in the air gap
H_{UGC}	ideal magnetic field intensity if the core was ungapped
I_0	initial current
I_D	drain current
I_{gate}	transient gate current
I_{in}	input current
I_{Invtr}	inverter current during switching
I_L	inductor current
I_{Leq}	the equivalent current in an uncoupled inductor with inductance L_{eq}
I_{LM}	inductor current of the master phase
$I_{Lpk,ref}$	reference control voltage for the desired peak current
$I_{Lpk,ref-M}$	reference control voltage for the desired peak current of master phase
$I_{Lpk,ref-S}$	reference control voltage for the desired peak current of slave phase
$I_{LM,peak}$	peak master phase inductor current in steady-state operation
I_{LS}	inductor current of the slave phase
I_{LU}	equivalent inductor current in an uncoupled inductor with inductance L_{eq}
$I_{LU,peak}$	peak current of the equivalent uncoupled inductor
I_{mirror}	output current from the current mirror
I_{peak}	peak current
$I_{peak\ dischrg}$	peak current during discharge
I_{out}	output current
$I_{primary}$	current in the transformer primary winding
I_{rampM}	ramp current of master
I_{rampS}	ramp current of slave
I_{RN}	return-side current contribution under nominal bias of a simple current source
I_{RP}	supply-side current contribution under nominal bias of a simple current source
I_{slope}	current slope
I_σ	standard deviation of simulated current
I_μ	mean simulated current
k	coupling coefficient
k_N	transconductance parameter for NMOS
k_P	transconductance parameter for PMOS
kT/C	mean-square thermal voltage noise across a capacitor
L	inductor reference designator
L	MOSFET channel length
LCD	liquid crystal display
l_{core}	field path length through magnetic core
LED	light-emitting diode
l_{gap}	magnetic core air gap length
L’	MOSFET channel length

L_{eq}	equivalent inductance of an uncoupled inductor
L_M	inductance of master phase
L_S	inductance of slave phase
M	mutual inductance
M1…	MOS transistor reference designator
MC	master clock
MOSFET	metal-oxide-semiconductor field-effect transistor
MPPT	maximum power point tracking
N	number of turns in the inductor winding
N	current mirror gain
N	transformer turns ratio
N1…	schematic node
NED	negative edge detector
NMOS	n-channel MOSFET
OUT1…	outputs from the ramp generator circuit, resets the slave clock
P_{DPD}	dynamic power dissipation switching loss
P_{DSL}	dynamic switching loss
PH1…	control signals
$P_{inverter}$	power dissipated in the inverter during switching
P_{LM}	power in the master phase inductor
P_{LU}	power in an equivalent uncoupled inductor
PMOS	p-channel MOSFET
POR	power-on reset
PTAT	proportional-to-absolute temperature
$P(t)_{CH}$	power dissipated in the MOSFET channel
Q	Flip-flop output clock
QN	Flip-flop output clock_not
Q_{drain}	drain charge
Q_{gate}	gate charge
r_o	impedance looking into MOSFET drain
r_{out}	impedance looking into the output node
R	resistor reference designator
R	S-R latch input: reset
$\mathscr{R}_{core}$	magnetic reluctance in the core material
$\mathscr{R}_{gap}$	magnetic reluctance of the air gap
R_{CH}	MOSFET (drain-to-source) channel resistance when the switch is on
R_{DR}	output impedance of gate driver
R_{DS}	MOSFET drain-to-source small-signal resistance when used as a current source
R_L	load resistance
R_N	equivalent impedance of the load-side in a summing node
R_P	equivalent impedance of the supply-side in a summing node
RS1…	ramp circuit reset interval
RS	S-R latch control signal: reset
R_S	added source resistance to induce the MOSFET body effect
S	S-R latch input: set

S_1	PSPICE primitive voltage-controlled resistor (switch)
SC	slave clock
S-R latch	set-reset digital latch
ST	S-R latch control signal: set
t	time
t_{cycle}/T_C	cycle period
t_d	delay time
T-FF	toggle flip-flop
t_{in}	input period
t_{off}	off period
t_{out}	output period
TM	transient model
T_{SW}	period of the master clock
U1…	component reference identifier
u_B	energy density
U_C	energy stored in capacitive reactance
U_L	energy stored in inductive reactance
V_{bias}	bias voltage for analog circuits
V_{BG}	body to gate voltage
V_{core}	core volume
$V_{control}$	control signal for the ramp generator
$V_{D1…}$	diode voltage
$V_{DD\,/\,CC}$	digital supply voltage
V_{drain}	drain-node voltage
V_{DS}	MOSFET drain-to-source voltage
V_{gate}	MOSFET gate voltage
V_{GB}	MOSFET gate-to-body voltage
V_{GS}	MOSFET gate-to-source voltage
V_{HV}	voltage of high-voltage battery stack
$V_{hysteresis}$	hysteresis voltage
V_{in}	input voltage
V_{Invtr}	inverter voltage (input and output)
V_L	applied voltage across inductor
V_{offset}	offset voltage / input offset
V_{ON}	on-voltage
V_{out}	output voltage
V_{pp}	peak-to-peak voltage
V_R	voltage drop across resistor
V_{Ramp}	ramp voltage
V_{RampM}	ramp voltage of master
V_{rms}	root-mean-squared voltage
V_S	MOSFET source voltage
V_{th}	MOSFET threshold voltage
V_{TN}	NMOS threshold voltage
V_{TP}	PMOS threshold voltage
W	width

W’	MOSFET channel width
WO	worst-case one process corner
WP	worst-case power process corner
WS	worst-case speed process corner
WZ	worst-case zero process corner
XOR	exclusive OR
ZCD-M	zero-current detect signal of master
ZCD-S	zero-current detect signal of slave
ZCS	zero-current switching
ZTC	zero temperature coefficient
ZVS	zero-voltage switching
δk_N…	transconductance process variation…
ΔB	peak-to-peak magnetization
ΔI_L	peak-to-peak inductor current
ΔL	inductance variation
Δt	time interval
Δt_{in}	control signal timing error
$\Delta \Psi$	peak-to-peak flux
λ	MOSFET channel-length modulation factor
μ	carrier mobility
μ_0	permeability of free space
μ_{eff}	effective permeability
μ_m	material permeability
μ_N	carrier mobility in NMOS
μ_r	reversible permeability
σ	standard deviation
τ	exponential time constant
Ψ	magnetic flux
Ψ_{12}	magnetic flux coupled from leg1 to leg2

1. Basic principles of power converters

All switched-mode power converters have the same basic operation. The converter has an input period where energy is taken from the source and stored in an inductive core. An output period follows where the magnetized inductance is demagnetized and the energy is delivered to the load. Increasing the input period increases the converter power, provided the magnetizing core does not saturate.

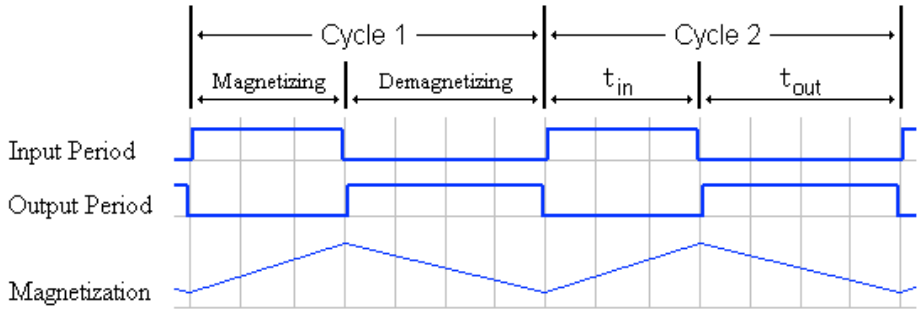

Figure 1.1. Magnetizing and demagnetizing a core is the basic energy transfer mechanism in switched-mode power supplies.

Within this basic scheme, there are three principle modes of operation. In continuous conduction mode (CCM) the core is not fully demagnetized at the end of the cycle. With boundary conduction mode (BCM), the core is demagnetized right at the end of the cycle, and with discontinuous conduction mode (DCM) the core fully demagnetizes some time before the cycle ends. Each mode has advantages and disadvantages as will be discussed. The power converter hardware is the same for all three operating modes, but the controllers are very different.

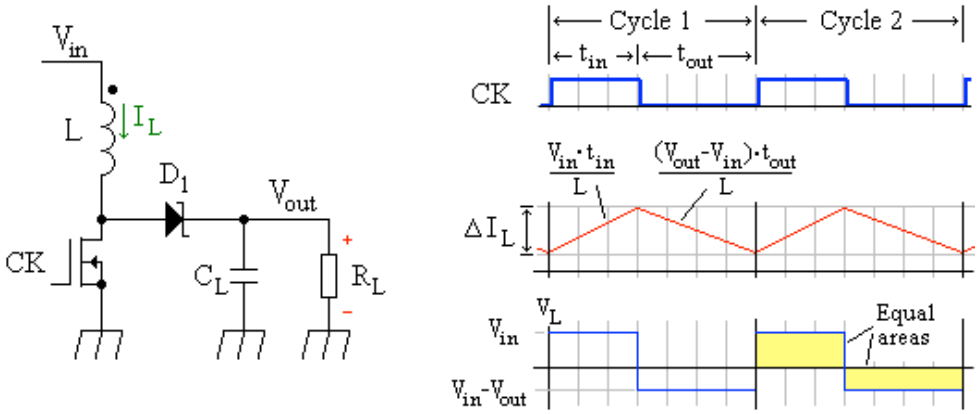

Figure 1.2. The inductor volt-second balance is used to find the CCM transfer function.

To better understand the operating modes, consider the boost converter shown in Figure 1.2. During the input period t_{in}, the inductor current must increase by $t_{in} \cdot V_{in}/L$. During the output period t_{out} the inductor current must decrease by $t_{out} \cdot (V_{out} - V_{in})/L$. In steady-state operation the net current change over the cycle period is zero. The inductor voltage-time product, shown as the yellow boxes in the figure, also averages to zero over the cycle; from this volt-second product the converter transfer function is obtained.

$$\frac{V_{in} \cdot t_{in}}{L} = \frac{(V_{out} - V_{in}) \cdot t_{out}}{L} \qquad (1\alpha)$$

$$\frac{V_{out}}{V_{in}} = \frac{1}{1-D} \qquad (1)$$

D is the duty cycle, defined as t_{in} / t_{cycle}. This transfer function is valid for CCM and BCM operation. For a constant output voltage, the duty cycle can be changed to regulate against variations in the input voltage. However for changes in load power while the output voltage remains constant, the cycle time must be changed and the duty cycle held constant. This is because more power requires a longer input period to store the needed energy, and a constant output voltage requires a constant duty cycle. [1]

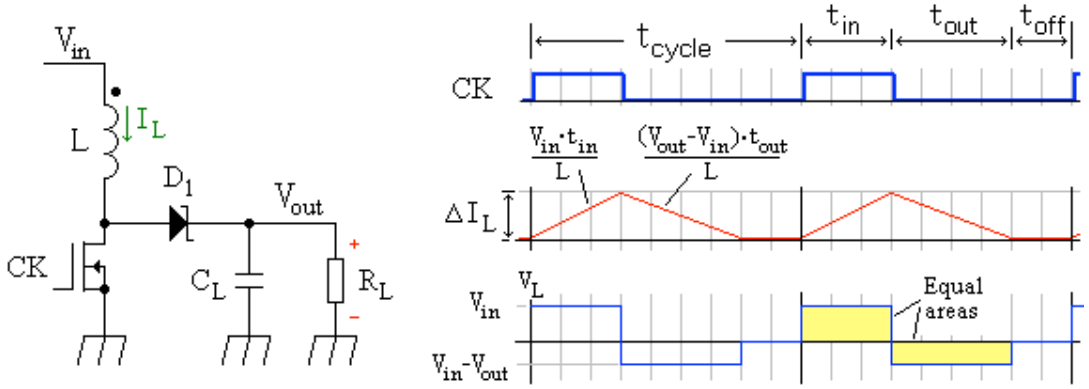

Figure 1.3. The inductor volt-second balance is used to find the DCM transfer function.

Figure 1.3 shows the timing for DCM operation. During the input period, the inductor current must increase by $t_{in} \cdot V_{in}/L$. During the output period the inductor current must decrease by $t_{out} \cdot (V_{out} - V_{in})/L$. In steady-state operation the net current change and inductor voltage-time product (area of colored boxes) average to zero over the cycle; from this volt-second product the converter transfer function in DCM is derived.

$$\frac{V_{in} \cdot t_{in}}{L} = \frac{(V_{out} - V_{in}) \cdot t_{out}}{L} \qquad (2\alpha)$$

$$\frac{V_{out}}{V_{in}} = \frac{t_{out}}{t_{out} - D \cdot t_{cycle}} \qquad (2)$$

From the transfer function the advantage of DCM is seen. The off period t_{off} allows either voltage or power regulation by simply adjusting the duty cycle while keeping the cycle time constant. The relative simplicity of the controller makes DCM operation ideal for digital controllers where a constant clock frequency is used. [2]

1.1 Ripple currents

Depending on the system requirements, the power system designer has many options for controlling the ripple currents seen by the source and load. Depending on which mode and which converter is used, some converters will provide a near constant load to the source with very little ripple, while others will provide large ripple and even reversed current for part of the switching cycle. For renewable energy applications reverse-input currents can be a serious problem and require additional input filtering.

For many consumer applications output ripple may be the concern. Pulsed output from the converter means less voltage regulation and higher power supply noise. In these applications switch-mode converters like the Cúk and Zeta converters offer continuous output current at the cost of higher circuit complexity. [3]

There are no absolute rules, but generally CCM offers the lowest ripple, and DCM has the worst ripple performance. This can be seen in the waveforms shown in Figures 1.2 and 1.3. The peak-to-peak input current ΔI_L can be made quite small in CCM, but in BCM this current always returns to zero, and in DCM the current returns to zero and parasitic elements cause oscillations that pulse current into and out of the source. Table 1.1 summarizes the comparative advantages and disadvantages of the three modes for the boost converter. [4]

Operating mode	Voltage regulation	Power regulation	Input current ripple	Output current ripple
CCM	Duty cycle	T_C and/or D	Lowest	High
BCM	Duty cycle	Cycle period (T_C)	Higher	Higher
DCM	Duty cycle	Duty cycle (D)	Highest	Highest

Table 1.1. Comparison of the control and ripple currents for the three operating modes.

Which converter and operating mode will provide the highest efficiency? That largely depends on the application. Maximizing efficiency is a tradeoff between ohmic and switching losses. Understanding these losses is essential to good system design.

1.2 Ohmic losses

Ohmic losses occur primarily in the inductor winding resistance and the channel resistance of the power switches. It is tempting to use larger diameter wires to reduce the winding resistance, but even moderately sized wires suffer eddy current losses within the wires. A better solution is to use many small diameter wires in parallel. Litz wires are specifically designed to reduce eddy current losses in the windings. [5] Design optimization is the tradeoff between ohmic and other losses; the resistance is decreased at the cost of increased switching and magnetic losses.

High frequency switching reduces the effective wire diameter (skin effect), so the AC resistance must be used in calculations. Parallel wires with high fill-factor can have high inter-winding capacitance, which can cause problems. In particular with high-voltage low-current low-power applications, the energy stored in the inter-winding capacitance may actually exceed the energy stored in the inductance. In this case a reduced fill-factor with winding layer separation may be necessary. [6]

Figure 1.4 shows the comparative channel currents seen when the average CCM and BCM currents are equal. Current flows in the channel for only part of the cycle, but continuously in the inductor making inductor ohmic losses a concern.

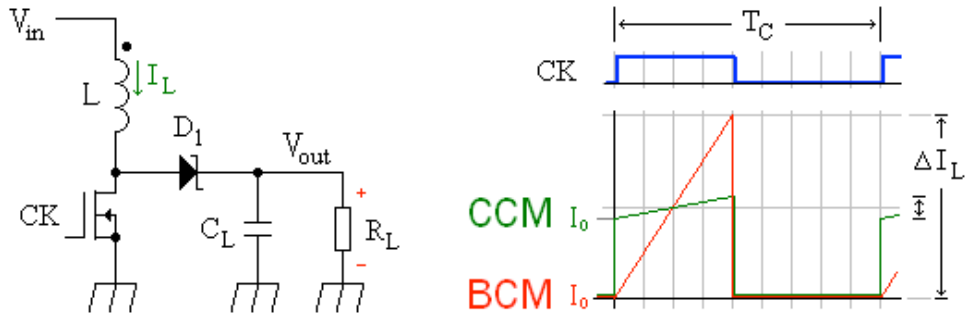

Figure 1.4. MOSFET channel current in CCM and BCM operation. The average currents are equal.

BCM has twice the peak current and CCM current approaches a square wave in the extreme limit of infinite inductance. The current can be decomposed into the initial current I_0 and the incremental current ΔI_L. In BCM the initial current is zero, and in CCM the incremental current approaches zero. The total channel current and power are then:

$$I(t) = I_0 + \Delta I_L \cdot \frac{t}{t_{in}} \tag{3\alpha}$$

$$I(t)^2 = I_0^{\,2} + 2 \cdot I_0 \cdot \Delta I_L \cdot \frac{t}{t_{in}} + \Delta I_L^{\,2} \cdot \frac{t^2}{(t_{in})^2} \tag{3\beta}$$

$$P(t)_{ch} = \int_0^{t_{cycle}} I(t)^2 \cdot R_{ch}\, dt \tag{4}$$

where R_{ch} is the channel resistance, and the inductor winding losses are considered separately. Carrying out the integration gives the average power dissipated in the channel resistance.

$$P_{ch} = I_0^{\,2} \cdot R_{ch} \cdot t \Big|_0^{t_{in}} + R_{ch} \cdot I_0 \cdot \Delta I_L \cdot \frac{t^2}{t_{in}} \Big|_0^{t_{in}} + \tfrac{1}{3} \cdot R_{ch} \cdot \Delta I_L^{\,2} \cdot \frac{t^3}{(t_{in})^2} \Big|_0^{t_{in}} \tag{5}$$

In BCM the first two terms become zero and the power lost is equal to the third term. In CCM as the inductance approaches infinity, the current approaches a rectangular pulse and ΔI_L approaches zero. The lost power in CCM is then approximated by the first term. Comparing BCM against CCM in the limit of infinite inductance, the power losses due to resistance can be up to 1.33 times higher for BCM.

CCM reduces the ohmic losses in the MOSFET channel, but at the cost of a larger inductance (and higher inductor winding losses) or higher converter frequency. Inductor winding losses can be decreased by reducing the number of winding turns, which implies decreased inductance. To obtain a lower dI_L/dt, a much higher converter switching frequency is then needed, and this increases the switching losses.

1.3 Switching losses: dynamic power dissipation

To reduce the channel resistance a wider MOSFET is used, which increases the gate capacitance. The channel resistance and gate capacitance are intrinsically linked and they are inversely proportional. From device physics the relationship between gate capacitance C_{GS} and channel resistance R_{ch} is:

$$R_{ch} = \int_0^{L'} \frac{dl}{\mu \cdot Q(l) \cdot W'} \cong \frac{L'}{\mu \cdot W' \cdot C_{GS}(V_{GS} - V_{th})} \tag{6}$$

The variables describe a MOSFET with channel length L', channel width W', carrier mobility μ, and gate charge Q which varies across the channel length at effective gate voltage V_{GS}-V_{th}. [7][8] The power lost charging and discharging the gate capacitance is called the *dynamic power dissipation*. [9] It is dependent on the gate-to-source voltage V_{GS} and frequency of the converter cycle f_c. The dynamic power dissipation is:

$$P_{dpd} = C_{GS} \cdot V_{GS}^{\ 2} \cdot f_c \tag{7}$$

If complementary switches are used in the design, resonant gate drivers can be used to reduce this loss. The idea is to connect the gates of the two switches through a small inductor creating a resonant circuit. The gate charge of the 'on' switch assists the 'off' switch in turning on, and vice versa. The gate charge is then recycled, driver requirements (and losses) are reduced, and switching times can be improved. Considering that higher gate voltages are needed to get the lowest channel resistance, this circuit is an attractive gate drive solution. [10]

The dynamic power dissipation can easily exceed the ohmic losses. By combining equations 5 -7, the optimum channel resistance can be found – gate capacitance ratio for a given design and the best power MOSFET can be selected. Generally higher channel resistance favors low current designs, and lower channel resistance favors high current designs. However, this simple analysis ignores an important power loss in the system: the dynamic switching losses.

1.4 Dynamic switching losses as the switch turns on

Dynamic switching losses occur when current is pushed into the channel as the switch turns on. In BCM the initial inductor current I_L is zero, so the dynamic switching losses are zero. However in CCM the drain voltage V_{DS} stays clamped at V_{out} until the drain current I_D exceeds I_L and D_1 turns off. At time t_1, the channel resistance equals V_{out}/I_L. This resistance is two to three orders of magnitude greater than the channel on-resistance; the entire switching transient occurs before the switch is fully turned on. After t_1 the drain current is limited by I_L as V_{DS} drops and the channel resistance decreases. Because of the overlap between the high drain voltage and the high drain current, power losses are high through the transition. The problem is exacerbated when D1 is implemented with a diode; the reverse-recovery of silicon diodes increases the overlap time and large current spikes associated with discharging the diffusion capacitance [11].

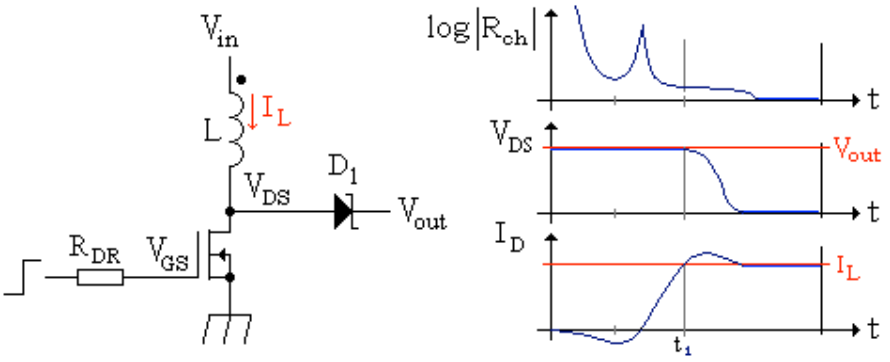

Figure 1.5. As the switch turns on in CCM, V_{DS} is clamped at V_{out} until I_D exceeds I_L and D_1 turns off. After t_1, I_D clamps at I_L and the drain voltage drops. The I_D-V_{DS} overlap causes a large power dissipation.

Before t_1 the power dissipation equals the integral of the drain-current · output-voltage product. After the diode turns off, the power dissipation is then the integral of the inductor-current · drain-voltage product. The drain voltage follows the saturation model with channel-length modulation factor λ, given in equation 8. [12] The dynamic switching loss is approximated using equation 9. This equation works for both rising and falling edges once the integration times are set correctly.

$$V_{DS} = \frac{I_D - \frac{1}{2}\mu \cdot C_{ox} \cdot \frac{W'}{L'} \cdot (V_{GS} - V_{TH})^2}{\frac{1}{2}\lambda \cdot \mu \cdot C_{ox} \cdot \frac{W'}{L'} \cdot (V_{GS} - V_{TH})^2} \tag{8}$$

$$P_{DSL} = \int_0^{t_1} \frac{1}{2}\mu \cdot C_{ox} \cdot \frac{W'}{L'} \cdot (V_{GS} - V_{TH})^2 \cdot (V_{DS} + \lambda V_{DS}{}^2)\, dt + \int_{t_1}^{T/2} I_L \cdot V_{DS}\, dt \tag{9}$$

Assuming a simple gate driver model, the gate voltage V_{GS} increases to the gate driver supply voltage V_{DD} with exponential time constant $\tau = R_{DR} \cdot C_{GS}$. At five time constants the switch is fully on. The initial gate current I_0 is V_{DD} divided by the driver output impedance R_{DR}. As the switch turns on, I_D will clamp at I_L.

- Consider now a hypothesis that *if* the transient gate current I_{gate} exceeds I_D until the switch is fully turned on, then the dynamic switching losses will be zero, and that *if* the drain current exceeds the gate current as the switch turns on dynamic switching losses will occur. Figure 1.6 shows the detail.

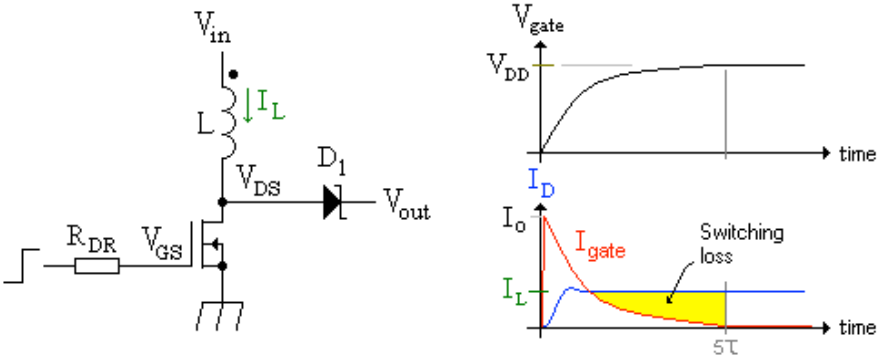

Figure 1.6. In CCM dynamic switching losses are reduced when carriers (holes) released from the gate interface supply part of the channel current as the switch turns on.

Dynamic switching losses will only be zero if I_D is zero; this occurs in BCM. In CCM the losses are minimized when I_{gate} supplies as much of the drain current as possible. The idea is to minimize the shaded area shown in Figure 1.6. Ideally, the charge on the gate ($Q_{gate} = C_{GS} \cdot V_{DD}$) should exceed the charge coming into the drain ($Q_{drain} = I_L \cdot 5\tau$). That comparison gives:

$$Q_{gate} > Q_{drain} \tag{10\alpha}$$

$$C_{GS} \cdot V_{DD} > I_L \cdot 5 \cdot R_{DR} \cdot C_{GS} \tag{10\beta}$$

$$R_{DR} < \frac{V_{DD}}{5 \cdot I_L} \tag{10}$$

This suggests that the gate driver output impedance R_{DR} should be as low as possible. This reduces τ and thus the current-time product of the shaded area. To test the validity of Equation 10 a PSPICE simulation is made and the results are given in Table 1.2. (Test conditions: $R_{ch} = 1.31m\Omega$, $C_{GS} = 12.1nF$, $C_{DS} = 200pF$, $V_{out} = 12V$.) The gate driver supplies 151.25nJ ($U = \frac{1}{2}CV^2$ for $V_{DD} = 5V$), which is independent of R_{DR} or I_D. The shaded boxes show the loss when R_{DR} is greater than the value calculated in Equation 10.

R_{DR}	I_L = 0A (BCM)	I_L = 1.0A (CCM)	I_L= 2.0A (CCM)	I_L = 3.0A (CCM)
100mΩ	0.6nJ	28nJ	42nJ	57nJ
500mΩ	0.3nJ	37nJ	60nJ	84nJ
1Ω	0nJ	43nJ	74nJ	106nJ
2Ω	-0.2nJ	54nJ	96nJ	141nJ
5Ω	-0.3nJ	78nJ	148nJ	224nJ
10Ω	-0.5nJ	111nJ	222nJ	343nJ

Table 1.2. The table shows the simulated dynamic switching loss for a rising-edge gate transition at different values of gate resistance and drain current. These results support the assumption made with Equation 10.

Equations 8 and 9 tell us the optimum MOSFET parameters needed to minimize the dynamic switching loss. Equation 10 tells us the best gate driver design needed to minimize this loss. In all cases of CCM operation a faster driver with lower output impedance will reduce this switching loss, and this loss must be compared against the driver power requirements. In contrast, BCM dynamic switching losses are always zero even for slow gate driver circuits.

1.5 Dynamic switching losses as the switch turns off

In both CCM and BCM the switch turns off at peak current. A poor design will have higher switching losses and undue component stresses. The problem with this circuit is the Miller Effect; power MOSFETs have very high gain, and the drain voltage increases rapidly. The energy coupled into the gate through the gate-to-drain capacitance C_{GD} can stall or even reverse the falling gate voltage. With a simple simulation the solution becomes clear. Based on the physical model, the circuit is shown in Figure 1.7. Instead of using the abstract small-signal voltage-controlled current source model, a more realistic model is made using a voltage-controlled resistor S_1 (PSPICE switch).

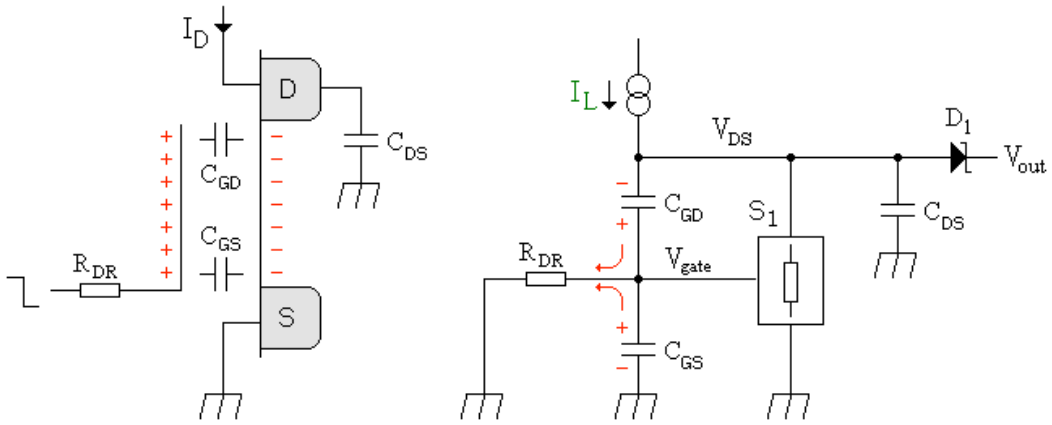

Figure 1.7. A simple model is all that is needed to analyze the switching losses and determine the best approach to minimizing these losses.

Transient analysis can be done using Laplace transforms and nodal analysis. However, with two assumptions the analysis is greatly simplified. First, assume that the gate voltage has temporarily stalled and the gate capacitance is no longer discharging. This occurs when the current needed to charge C_{GD} equals the discharge current of C_{GS}:

$$\frac{V_{gate}}{R_{DR}} = C_{GD} \cdot \frac{dV_{DS}}{dt} \tag{11}$$

Here V_{gate} is the gate voltage, which stalls just below the threshold voltage. If the drain voltage rises faster than the condition set in Equation 11, the gate voltage will actually increase and the switch will start to turn on again. This can sometimes be seen as a small rise in the gate voltage as the switch turns off, and it causes larger switching losses. The prevention is to limit the drain voltage rise time.

As the switch turns off, the channel resistance rises rapidly. The second analysis assumption is that the channel current drops so rapidly that the majority of the inductor current charges the drain node capacitance instead of going into the drain ($I_L >> V_{DS}/R_{DS}$). The transistor small-signal gain does not affect the drain voltage slope; the slope is limited at $dV_{DS}/dt = I_L/(C_{DS}+ C_{DG})$. Combining this with Equation 11 gives the new gate voltage stall condition:

$$C_{DS,stall} = C_{GD} \cdot \left(\frac{I_L \cdot R_{DR}}{V_{gate}} - 1 \right) \tag{12}$$

To avoid stalling the gate discharge, the drain capacitance must be larger than $C_{DS,stall}$. The simulation results in Figure 1.8 show the tradeoff between drain slope and the gate discharge rate. The drain circuit is an integrator, and when C_{DS} is about 10 times $C_{DS,stall}$ the Miller Effect is essentially eliminated.

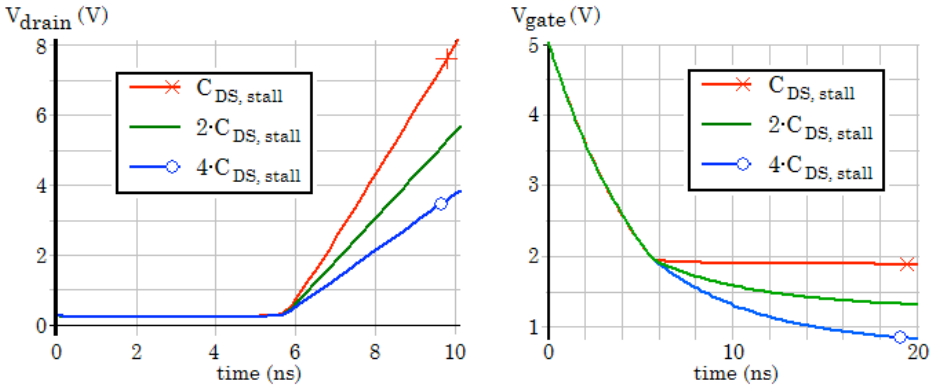

Figure 1.8. Increasing the drain node capacitance decreases the drain voltage rise time. The slower rise time decreases the Miller Effect and the switch turns off faster.

To reduce the slope, additional drain capacitance C_1 may be needed. Increasing C_1 decreases the V_{DS}-I_D overlap, which decreases the dynamic switching losses. C_1 effectively behaves as a snubber, a class of circuits that are used to reduce switching losses. [13] In BCM, the energy needed to charge the drain capacitance is returned to the source when it discharges. In CCM this charge is lost at switching, and added capacitance will cause higher dynamic power dissipation (Equation 7).

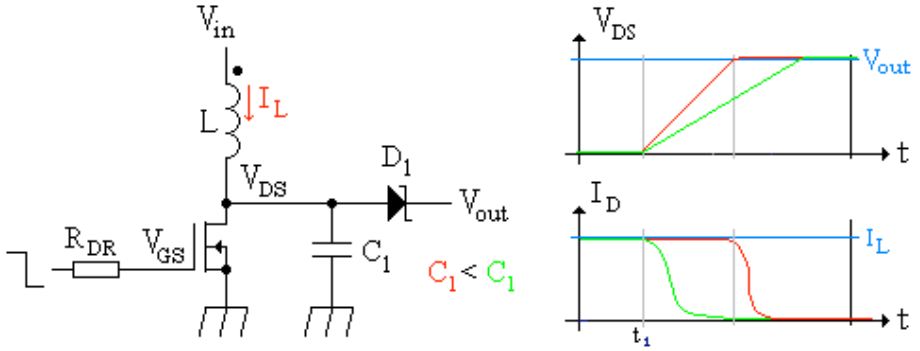

Figure 1.9. Adding drain capacitance helps the switch turn off faster, which reduces the V_{DS}-I_D overlap. This overlap causes the dynamic switching loss seen as the switch turns off.

Operating mode	C_1	I_L	MOSFET DSL/cycle	Loss @100kHz
CCM	0	5.0A	313nJ	31.3mW
BCM	0	7.4A	497nJ	49.7mW
BCM	2nF	7.4A	256nJ	25.6mW
BCM	5nF	7.4A	128nJ	12.8mW
BCM	10nF	7.4A	53nJ	5.3mW

Table 1.3. The table shows the effect of C_1 on dynamic switching loss as the MOSFET turns off.

1.6 Magnetic core losses

Switch-mode power systems convert energy by magnetizing and demagnetizing a magnetic core; changes in magnetization B generate core heating and losses [14]. Core losses increase as 1) ΔB increases, and 2) dB/dt increases [15]. However, the energy U stored is also proportional to ΔB. For a core with volume V_{core} (cross-sectional area A_{core} and closed magnetic field path length l_{core}), magnetic field intensity H, and magnetization B, the energy stored in the core material over one converter cycle is then [16]:

$$U = \int_{B1}^{B2} H(t) \cdot l_{core} \cdot A_{core} \cdot dB(t) = V_{core} \cdot \int_{B1}^{B2} H(t) \cdot dB(t) \qquad (13)$$

The stored energy is depicted graphically as the shaded area of the B·H product in Figure 1.10. CCM stores less energy per cycle because of the reduced current swing. To achieve the same power output in CCM, the inductance must be increased (H is increased by increasing the winding turns N), the converter frequency must be increased (Power = U/t), or the core volume must increase.

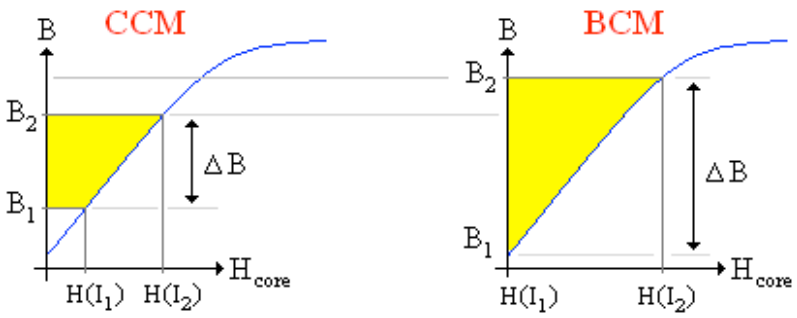

Figure 1.10. The core volume multiplied by the B·H product (shaded area) gives the converted energy per cycle. Because BCM has a larger ΔI_L, it delivers more power than CCM for the same core and cycle time.

H is derived from Ampere's Law for an un-gapped core with length l_{core} and N winding turns carrying current I_L (Equation 14). The B·H slope is modulated by the effective permeability μ_{eff} (Equation 15), which can be adjusted over a large range by adding an air gap with length l_{gap} (Equation 16) [17]. Increasing the air gap decreases μ_{eff}, which decreases B. A practical limit is reached at a few millimeters [18] (industry gap E160 is 1.2mm) where the flux leakage rapidly increases the effective gap area A_{gap} beyond the core cross-sectional area A_{core}. Additionally, μ_{eff} decreases with H_{core} due to a decrease in $\mu_m(H_{core})$ (refer to μ_r in material data sheets) [15]. This decrease in μ_{eff} (Figure 1.11) mathematically describes core saturation.

$$H_{UGC} = \frac{N \cdot I_L}{l_{core}} \tag{14}$$

$$B = \mu_0 \cdot \mu_{eff} \cdot H_{UGC} = \mu_0 \cdot H_{gap} = \mu_0 \cdot \mu_m \cdot H_{core} \tag{15}$$

$$\mu_{eff}(H_{core}) = \frac{l_{core}}{\frac{l_{core}}{\mu_m(H_{core})} + l_{gap} \cdot \frac{A_{core}}{A_{gap}}} \cong \left. \frac{l_{core}}{l_{gap}} \right|_{H_{core} \to 0} \tag{16}$$

The energy density u_B (J/m^3) is approximated in Equation 17. Ideally B·H (energy stored) should be maximized while ΔB (core loss) is minimized; this occurs as H_{UGC} increases (via $N \cdot I_L$) *and* μ_{eff} decreases (via l_{gap}). Since B influences the core losses and H influences the ohmic losses (via the N·I product), the gap length is chosen to minimize the total loss.

$$u_B = u_{core} + u_{gap} = \tfrac{1}{2} \cdot \mu_0 \cdot \mu_m \cdot H_{core}^{\ 2} + \tfrac{1}{2} \cdot \mu_0 \cdot \mu_m^{\ 2} \cdot H_{core}^{\ 2} = \tfrac{1}{2} \cdot \mu_0 \cdot \mu_{eff} \cdot H_{UGC}^{\ 2} \tag{17}$$

Figure 1.11 shows the result. The μ_{eff} no-gap line (left image) is the material permeability μ_m. The gap provides feedback that stabilizes μ_{eff}; without it the inductance would decrease rapidly above the specified H=40A/m in the 3C90 material data sheet. Since μ_{eff} is a function of H, an optimum H_{core} at which the energy density is maximized is expected. This occurs around H=60A/m (E32/6 core, L=5μH). The energy density in the gap is μ_m times larger than the energy density stored in the core material. The gap storage capability is best utilized when H=60A/m or less. That the gap decreases ΔB is not immediately obvious since B peaks around 60mT in both cases. However H_{core}=60A/m occurs around I_L=2A for the un-gapped inductor, and around I_L=14A for the gapped inductor.

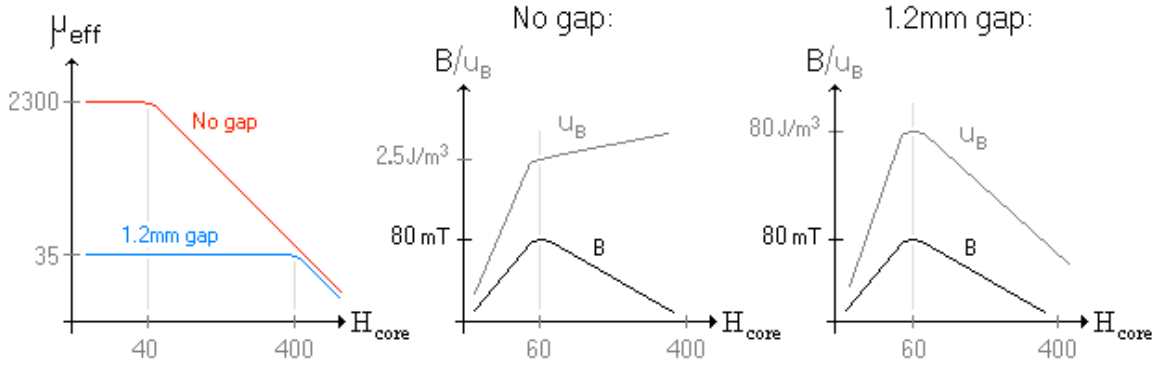

Figure 1.11. The core air gap stabilizes μ_{eff}, increases the range of H and BH product, and reduces ΔB.

The distinction between H_{core} and H_{UGC} is clarified with Equation 18. H_{UGC} is set by the applied magnetomotive force ($N \cdot I_L$). Part of this force magnetizes the core, and the rest is stored in the field across the gap. The core and gap reluctances determine the magnitude of H_{core}. In the un-gapped inductor, $H_{core} = H_{UGC}$ and the entire applied force magnetizes the core, resulting in a very low input current at saturation. The gap increases the current at which saturation occurs.

$$H_{core} = H_{UGC} \cdot \frac{\Re_{core}(H_{core})}{\Re_{core}(H_{core}) + \Re_{gap}} \tag{18}$$

Material hysteresis causes the decrease in μ_m as H_{core} increases; this is seen as a decreased B-H slope on a section of the B-H curve shown in Figure 1.12(a). If an AC signal is applied to the inductor, there is no net magnetization of the material and the permeability will be large (Amplitude permeability in the material data sheets). However, when current flow is restricted to only one direction as it is in switch mode systems, the core material becomes magnetized and μ_m will decrease (reversible permeability μ_r or μ_{eff}). This problem is exacerbated in CCM where there is a large DC current and small ΔI_L. In this respect the current reversal seen in BCM (discussed in section 2.1) helps to keep the core from saturating.

The gapped μ_{eff} shown in Figure 1.11 is idealized and may not accurately reflect true operation. The core reluctance $\mathscr{R}_{core}$ is a function of H_{core} and as μ_m decreases $\mathscr{R}_{core}$ begins to increase. This causes the core flux to drop as H_{core} increases above 40A/m. A strange H_{UGC}-H_{core} relationship results, as shown in Figure 1.12(b); the effect is similar to the negative resistance seen in some semiconductor devices. This effect is the result of a positive feedback ($\uparrow H_{core} \rightarrow \mu_m\downarrow \rightarrow \mathscr{R}_{core}\uparrow \rightarrow H_{core}\uparrow$) that pushes the gapped inductor into saturation sooner than would be expected from the material data sheets. The best solution is to keep operation around the μ_m knee or at least ensure some I_L reversal. This is one advantage of the coupled-inductor that will be discussed in section 2.6.

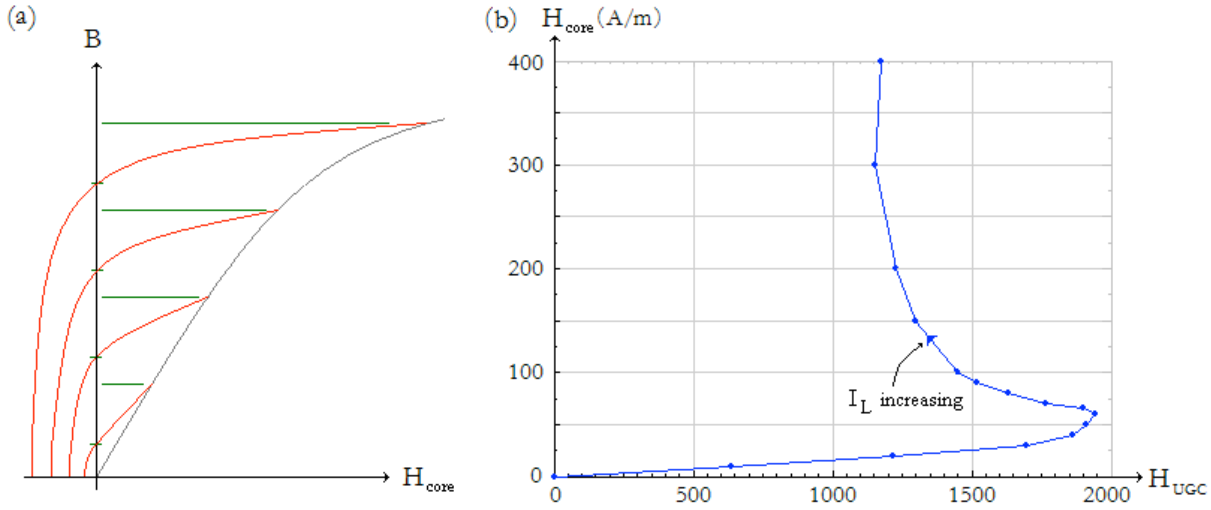

Figure 1.12. As H_{core} increases the B·H slope decreases (the material μ_m decreases as the material becomes magnetized) (a). The μ_m decrease causes the material reluctance to increase and when the inductor has an air gap the core flux may no longer increase monotonically with applied current. As the total reluctance increases and core flux decreases, the material begins to rapidly magnetize (b). The effect is similar to the negative resistance seen in some semiconductor devices.

Equation 19 compares the input power for CCM and BCM. The initial current I_0 in CCM means that H can be large, while the lower ΔI_L gives a lower ΔB. To achieve the lower ΔI_L in CCM, either the inductor must be larger (increased winding resistance) or the cycle time T_C must be shorter (increased dB/dt). The result is that CCM has lower total inductor losses in most, but not all cases.

$$\tfrac{1}{2} \cdot V_{in} \cdot \Delta I_{L,BCM} = I_0 \cdot V_{in} + \tfrac{1}{2} \cdot V_{in} \cdot \Delta I_{L,CCM} \tag{19}$$

The final design tradeoff is between core size and converter switching frequency. Increasing the core volume increases the stored energy; increasing the switching frequency increases the delivered power. Using a higher switching frequency allows a smaller core to be used; there are two good reasons to do this:

- Low frequency conversion needs higher inductance, which increases N. If the number of turns is doubled and the same fill factor is used, the resistance increases by 4x because the number of parallel windings must be cut in half. Higher frequency conversion decreases ohmic losses.
- Typically the inductor is one of the largest, heaviest, most expensive parts in the system, so design practice seeks to find the minimum core volume that meets the system requirements.

1.7 CCM/BCM loss comparison

The long analysis leads to an unsatisfying conclusion: neither mode has a clear advantage in converter efficiency. The design process is a compromise between switching, ohmic, and core losses. Generally, the lower switching losses will make BCM a better choice with high frequency switching, and the lower ripple current will give CCM lower ohmic and core losses. But when the design guidelines are followed, both modes will have similar efficiencies over most operating ranges. Table 1.4 gives a relative comparison of losses when the same core and cycle time are used:

Operating mode	MOSFET R_{CH}	MOSFET P_{DPD}	MOSFET P_{DSL} (rising edge)	MOSFET P_{DSL} (falling edge)	Inductor core loss	Inductor ohmic loss
BCM	Higher	Same	Zero	Lower *	Higher	Higher
CCM	Lower	Same	Higher	Higher	Lower	Lower

* with sufficient drain capacitance.

Table 1.4. The table shows a comparison of the power losses for the two operating modes.

1.8 Why use BCM?

Historically BCM converters were limited to low power systems (300W maximum), with limited applications in power factor correction and flyback converters [19]. The reflected impedance from the flyback secondary makes switching losses much higher for CCM converters. To deliver the same power, with the same converter efficiency, Dixon used a core with twice the volume for his CCM flyback converter compared against his BCM design example (he reduced switching losses by decreasing the converter frequency, and thus needed a larger core) [20].

The performance limitations on BCM converters were soon solved and today they are seen in many state-of-the-art systems with efficiencies exceeding 99%, power up to 50kW, and hundreds of amps of current [21]. The breakthrough originated with Jamieson, who proposed “negative coupled inductors” [22]. Multiphase systems reduce current peaks by distributing the current in time; if two phases are 180° out-of-phase, the combined ripple current is reduced. Coupled inductors combine these two phases on the same core. When two inductors are mutually-coupled on the same core, the core flux and losses can be reduced [23].

The concept is simple: part of the energy from the magnetizing phase is coupled through the mutual inductance to the demagnetizing phase. This makes the inductance of the magnetizing phase appear larger, and so fewer winding turns may be used. The result is decreased core and ohmic losses. A secondary benefit is that the reduced magnetic flux means a smaller core can be used [24].

The analysis has ignored the DCM operating mode. It is easy to see that DCM will not give higher efficiency compared to the other operating modes. Figure 1.3 shows DCM timing; for the same cycle time and power, the peak current will always be *more* than twice the average current. However DCM has some distinct advantages; DCM is inherently stable because the input current will always start from zero. Additionally the constant cycle time makes DCM ideal for systems where asynchronous power supply noise is problematic. For instance a DCM controller can be synchronized to the pixel or line rate in imaging systems, thus reducing system noise.

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2. Multiphase Interleaved BCM controllers

Which power converter operating mode is best (CCM/BCM/DCM)? The answer appears to be more a matter of preference than science as each mode has its own loyal following and creative engineering techniques to enhance performance. CCM suffers from comparatively higher switching losses, and many "soft-switching" solutions have been implemented [1]. BCM suffers from higher ohmic and core losses, and multiphase converters became a popular way to reduce these losses [2].

Soft switching in CCM is accomplished using an auxiliary resonant circuit or snubber. The basic idea is that current is diverted from the main power switch into the auxiliary circuit before switching occurs. This reduces switching losses of the main switch and reverse recovery losses in the diode. But this comes with the cost of additional circuit complexity –an additional inductor, capacitor, switch or switches, and control circuitry [3].

Multiphase BCM converters require additional inductors, switches, and control circuitry as well, and it may seem that there is no advantage to the multiphase BCM solution. However, multiphase converters have many advantages, and typically converters today will be multiphase regardless of the operating mode used. They increase power output while achieving higher efficiency and reducing the input current ripple. Current ripple reduction means that less input filtering is needed, reducing the size, cost, and weight [4].

Recently designers have favored converters with 180º phase-shifted interleaved pairs (2-phase, 4-phase…). The 180º phase shift minimizes the ripple seen by the source. It is called "ripple cancellation" because the source essentially sees a DC load and the ripple is due primarily to component mismatches [5]. For renewable energy sources such as solar panels, the reduced ripple means less decoupling capacitance is needed, and lower equivalent series resistance losses are seen. For grid connections, the lower ripple means lower harmonic distortion, and this interleaved design is seen widely in power factor correction [6]. Interleaving also reduces the output ripple, which improves the efficiency for charging batteries or improves voltage regulation for active loads. To achieve the highest performance, power systems today are likely to have the following features [7]:

- Soft switching to reduce switching losses. The best performance is achieved with the combination of zero-current switching (ZCS) and zero-voltage switching (ZVS).
- Interleaved multiphase design to reduce conduction and core losses.
- Coupled-induction between interleaved phases to reduce core losses and inductor size.

While it is clear that both CCM and BCM systems have realized high performance, the wider current swing with BCM better utilizes the magnetic core, and the return-to-zero causes fewer stability problems. Its growing popularity and technical challenges made a multi-phase BCM controller an interesting topic for this thesis.

2.1 Basic BCM operation

CCM is defined as switching before inductor demagnetization is complete (time t_0 in Figure 2.1). At instant t_0, the inductor current is zero and the inductor is demagnetized. Technically, switching precisely at t_0 is BCM; since the current is zero, BCM operates with ZCS. Diode D1 is current-starved so its reverse-recovery switching losses will be zero [8]. However, the drain node capacitance is still charged at V_{out}, and discharging it will result in dynamic power dissipation as defined in Equation 7.

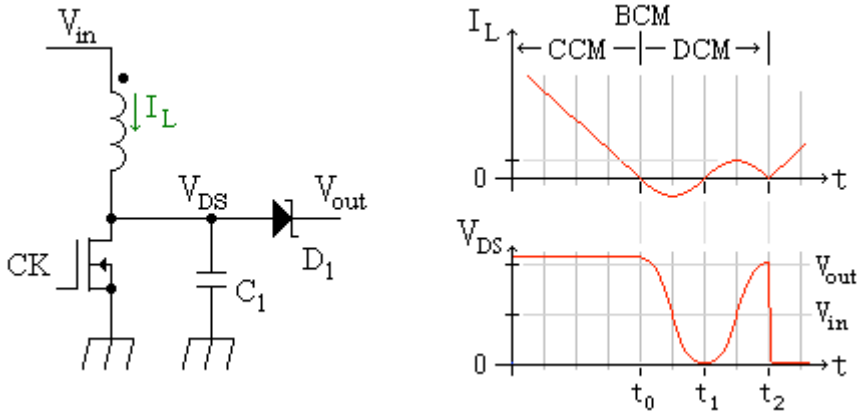

Figure 2.1. The timing diagram helps clarify the definition of the three operating modes. At time t_0 the inductor is demagnetized; switching at this instant would be BCM. BCM operates with ZCS, however a better switching time would be t_1 when both ZCS (inductor current is zero) and ZVS (drain voltage is zero) occur. Technically, switching at t_1 is DCM, but it is loosely defined as BCM as well. Switching randomly at any time after t_1 is always regarded as DCM.

If switching does not occur at t_0, the drain node capacitance begins to discharge through the inductor; the charge is recycled to source V_{in} and is not lost in switching. The inductor and drain capacitance form a resonant circuit, which causes the drain voltage to oscillate around voltage V_{in}. Ideally, switching should occur on the first oscillation minima at time t_1, but the exact operation depends on the input and output voltages. The three cases are:

- $V_{out} < 2 \cdot V_{in}$: In this case the voltage minimum will not drop to zero. Switching at the minimum is called valley switching, and the charge remaining on the node capacitance is lost to switching.
- $V_{out} = 2 \cdot V_{in}$: The drain voltage drops to zero at a delay of half of an oscillation cycle. Switching occurs at the voltage minimum when both the current and voltage are zero (ZCS and ZVS occur) [8]. In this case switching losses are minimized and the charge on the node capacitance is recycled.
- $V_{out} > 2 \cdot V_{in}$: In this case the voltage attempts to drop below zero volts. If the switch is not turned on at the zero-crossing, the MOSFET body diode will forward-bias. Most power MOSFETs are designed to handle large body diode currents, but the device rating should be checked. Some designs use a current sensor to find t_0, and the half-cycle delay to t_1 is calculated by the controller. In this case the delay should be reduced to minimize MOSFET power dissipation.

During the oscillation cycle, the source must accept current from the drain capacitance discharge, which is:

$$I_{peak\ dischrg} = (V_{out} - V_{in}) \cdot \sqrt{\frac{C_{drain}}{L}} \tag{20}$$

In DCM switching occurs asynchronously on this oscillation period causing a random inductor current component between $\pm I_{peak\ dischrg}$. This is undesired because it creates uneven phase currents, which increase the input ripple [9]. ZCS or ZVS operation solves the problem and it reduces switching losses. To distinguish between a random switching time in DCM and precise switching at time t_1, switching at t_1 will be referred to as BCM. The confusion regarding this distinction is not lost with many researchers, as the t_0-t_1 time interval has been given many names: synchronous conduction mode [2], critical mode [8], transition mode [6], DCM/CCM boundary [10], to name just a few.

2.2 System diagram

The full system actually has two controllers: a top-level system controller specific to the application, and a sub-controller that manages the converter timing. Different applications have different hardware requirements. A voltage-regulated converter adjusts the control signal according to the error between the output and reference voltages. However a renewable energy system with a battery output will have little or no output voltage control. Instead, a maximum power point tracking (MPPT) circuit may be used which prevents overdriving the source, and charges the battery according to the available power. It would be impossible to design a generic controller for every conceivable application. However, in both cases the same sub-controller may be used.

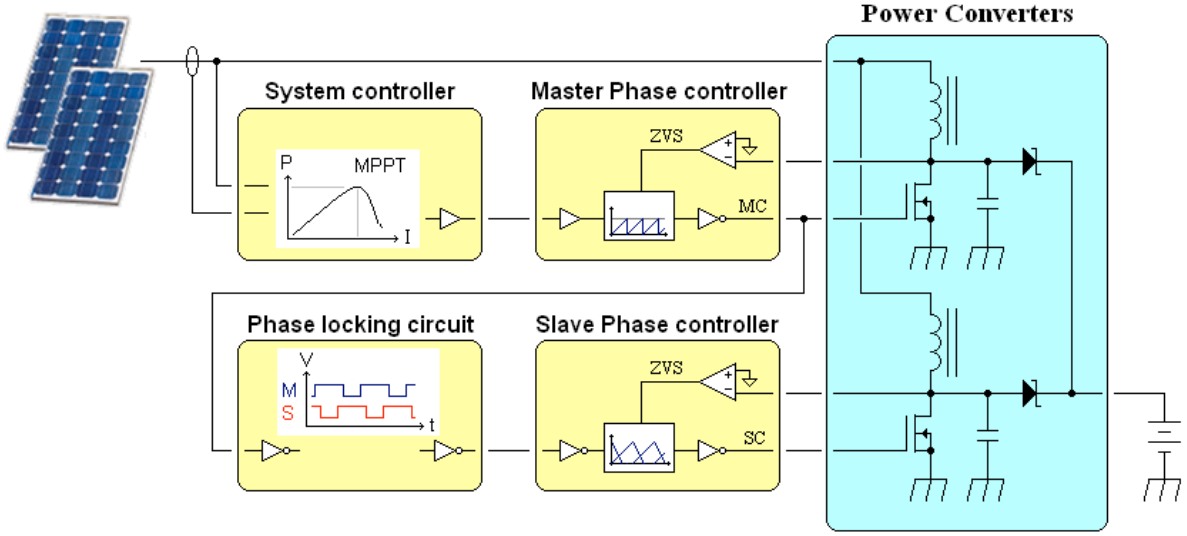

Figure 2.2. The complete design includes two controllers: an application-specific system controller, and a sub controller that manages the multiphase timing of the power converters.

2.3 Interleaving converter phases

With single-phase BCM the current peak will be twice the average current, or a 200% current ripple. The high spectral content will cause higher ESR losses and may require an EMI filter. Multiphase converters reduce the input current ripple significantly as shown in Figure 2.3. However, the ripple reduction is only seen if the phases have the proper phase shift. A 2-phase converter with 50% duty cycle can either have complete ripple cancellation (the two phases have a relative 180º phase shift), or the ripple current can be twice the average current when the converters are in phase.

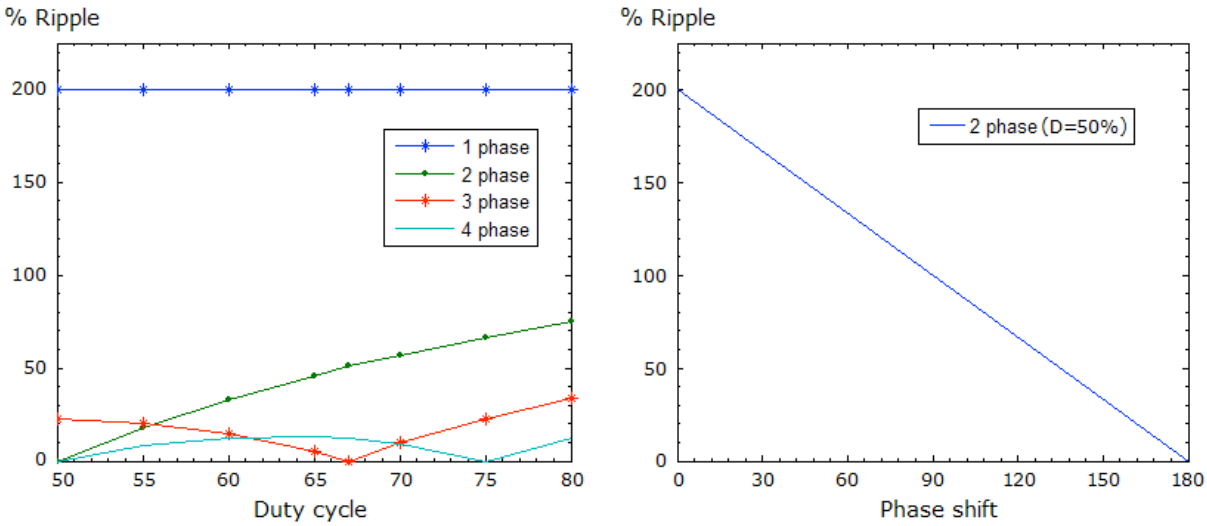

Figure 2.3. Multiphase converters reduce the input ripple current significantly, but the ripple reduction requires a proper phase shift between the converter phases.

To prevent the large current peaks that would randomly occur with asynchronous phases, the interleaved phases need to be phase-locked together. Two general interleaving strategies have been proposed: master-slave and democratic interleaving. In master-slave configurations, one converter phase operates as a stand-alone converter, and the other phases adjust their timing to track the master's clocking frequency and provide the proper phase shift. The democratic configuration is a little more complicated as each phase adjusts its timing to the other phases. Sadly for democracy, it appears that slavery is a more efficient use of resources, as the few published papers for democratic controllers are limited to two phases, and the performance does not appear to justify the additional hardware [11]. For this reason the discussion will be limited to master-slave configurations.

BCM converters are variable-frequency, which complicates phase locking. The clock frequency varies over several decades, and ideally phase locking should occur within one cycle, on a cycle-by-cycle basis. Several methods are published that attempt to achieve this. Open-loop controllers derive one edge of the slave's clock from the master clock, and this way the slaves follow the master. Closed-loop controllers are similar except they use a phase detector to modify the timing of this edge. The phase detector compares the phase shift between the master and slave, and uses the phase difference to help adjust the timing [11]. Both methods must work within the constraint that the system controller may use voltage-mode or current-mode control.

2.4 Open-loop controllers

Converter stability is a major problem with interleaved controllers. Since the slave converters are partially controlled by the master, there is the possibility of an incomplete slave cycle. If the slave enters CCM, it may never recover and the slave current is no longer controlled. The conditions for stability depend on whether a voltage-mode or current-mode controller is used. Consider the equation for the converter input power:

$$P_{in} = \tfrac{1}{2} \cdot V_{in} \cdot I_{peak} = \frac{V_{in}^{\,2}}{2 \cdot L} \cdot t_{in} \tag{21}$$

A current-mode controller turns off the power switch when a certain peak current is reached. A voltage-mode controller adjusts the time the switch is on (t_{in}) based on generating a voltage ramp and then comparing it with a control voltage. Timing errors (Δt_{in}) and component variations (ΔL) cause current variations that the voltage-mode controller does not sense. By reading the actual phase currents, the current-mode converter has an inherent feedback that the voltage controller does not have, giving it an apparent advantage in stability.

Controller stability is determined by whether the input current returns to zero at the end of the conversion cycle [8][12]. It is tested with two conditions: component mismatches (ΔL) in an unperturbed system, and a master delay-time perturbation. Stability depends on which circuit configuration is used. For proper interleaving, the slave phases must reference to the master clock. Two reference points exist: the rising and falling clock edges. This gives four basic open-loop configurations. Huber analyzed these configurations and tabulated the stability results shown in Table 2.1 [10].

Slave referenced to Master clock rising edge				Slave referenced to Master clock falling edge			
Current -mode		Voltage-mode		Current-mode		Voltage-mode	
D < 0.5	D > 0.5	D < 0.5	D > 0.5	D < 0.5	D > 0.5	D < 0.5	D > 0.5
Stable	Stable	Unstable	Unstable	Unstable	Stable	Unstable	Stable

Table 2.1. Two-phase controller stability for duty cycle (D) range and circuit configuration.

The first configuration (current-mode, rising edge) is said to be unconditionally stable; it is the only open-loop circuit configuration that is stable when the duty cycle is less than 50%. However what "stable" actually means needs further clarification.

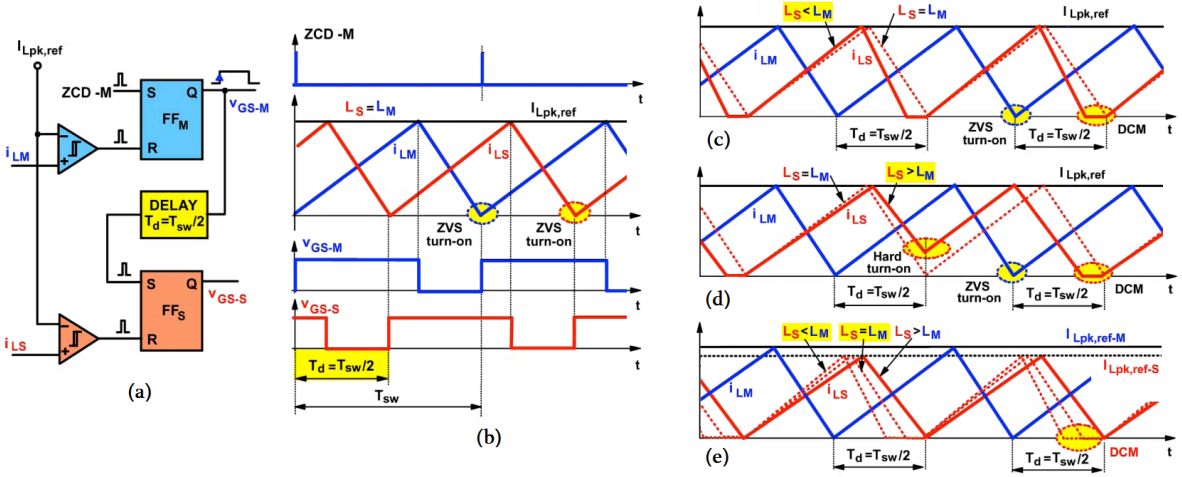

Figure 2.4. The figure shows the block diagram (a), timing (b), and stability analysis (c-e) for the current-mode controller synchronized to the rising edge of the master clock; T_{SW} is the period of the master clock. Details are given in the text. This image was compiled from [10].

Figure 2.4 shows a simplified block diagram of a two-phase current-mode controller. The system controller provides a control voltage proportional to the desired peak current $I_{Lpk,ref}$, and two signals proportional to the current in each phase (I_{LM} and I_{LS}). The system controller also supplies a zero-current detect signal (ZCD-M –or a ZVS signal could also be used) from the master phase. For two-phase converters the slave has a 180º phase shift, so the slave clock is set after a half-cycle delay from the rising edge of master clock V_{GS-M}. In order to synchronize to the master clock rising edge, the slave controller does not have its own ZCS / ZVS signal. If the slave phase achieves soft switching conditions, it is merely by timing coincidence.

Stability is determined by calculation (Equation 22), or through use of slope timing diagrams (Figure 2.4c-e). In these estimations, the converter off-time (t_0-t_1 interval in Figure 2.1) associated with ZVS is ignored.

$$I_{in}(T_{sw}) = \frac{V_{in}}{L}\cdot t_{in} - \frac{V_{out}-V_{in}}{L}\cdot t_{out} = I_{Lpk,ref} - \frac{V_{out}-V_{in}}{L}\cdot[T_{sw}-t_{in}] \le 0 \qquad (22)$$

Inductor mismatches cause three possible converter responses:

- If the slave and master inductances are equal ($L_S = L_M$), the slave current should have the same slope as the master current, and ZVS conditions should be seen (Figure 2.4b).
- If $L_S < L_M$, the slave current will have a larger slope and the slave cycle will finish before the master cycle. In this event the slave will operate in DCM (Figure 2.4c).
- If $L_S > L_M$, the slave cycle will be longer than the master cycle. In this case the slave will enter CCM; however, this will result in a shorter on-time in the next cycle and the slave will operate in DCM. The slave will then operate with this CCM-DCM subharmonic oscillation cycle (Figure 2.4d).

This CCM-DCM oscillation cycle will cause a larger ripple current and higher switching losses. To avoid this some systems include a calibration cycle in which the phase with the largest inductance becomes the master phase [13]. This approach guarantees the slave phases will operate in DCM. To achieve true BCM operation for all phases, the further step of adjusting the reference current control level for each phase is still needed (Figure 2.4e) [14]. Alternatively, BCM operation can be achieved by adaptively selecting the master phase based on actively-measured cycle times [15]. To achieve good switching conditions, the controllers can be quite complex.

The delay circuit can be perturbed by noise, so a second stability test checks for recovery from a delay-time perturbation. Because the BCM converter is variable frequency, the delay time must be determined on each cycle, which causes the slave to be a cycle behind the master. Any frequency change will thus cause a perturbation condition. Figure 2.5 shows the result. If the perturbation causes a shorter delay time ($T_D < ½\ T_{sw}$), a slave DCM cycle will occur. If it causes a longer delay ($T_D > ½\ T_{sw}$), a two-cycle CCM/DCM sequence follows.

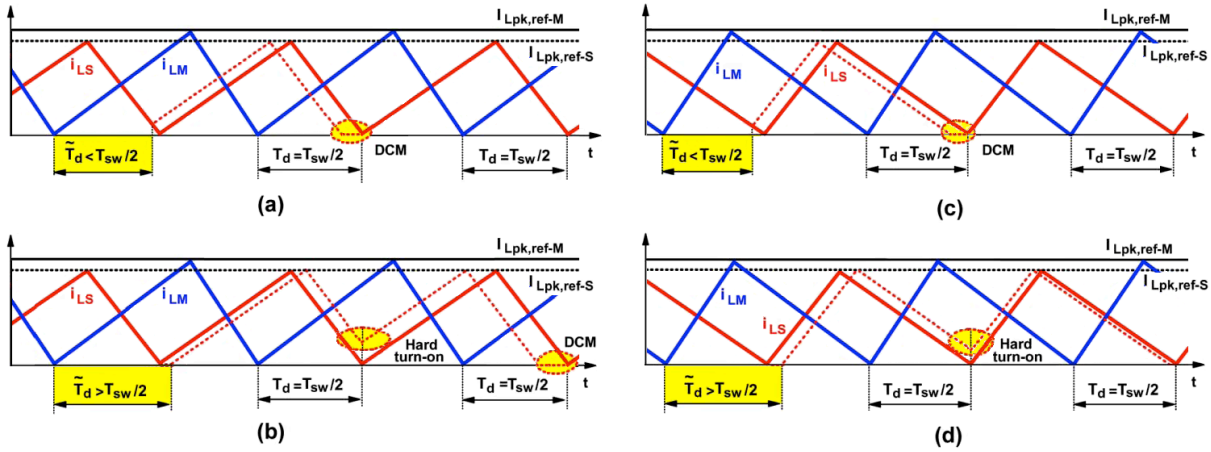

Figure 2.5. The figure shows the effect of a delay-time perturbation on the master and slave inductor currents. (a) D>50%, delay < ½ T_{sw}, (b) D>50%, delay > ½ T_{sw}, (c) D<50%, delay < ½ T_{sw}, (d) D<50%, delay > ½ T_{sw}. This image was compiled from [10].

Figures 2.4 and 2.5 show the inherent disadvantages with this interleaving scheme. It needs extra hardware and control to get it to behave well, but even then it has problems with delay-time perturbations. Any system noise or dithering of the control signal can leave the slave phases in a perpetual state of minor perturbations causing hard switching that reduces efficiency. If the duty cycle limitation (DC > 50%) can be tolerated, the open-loop controllers that synchronize to the master clock falling edge have some strong advantages.

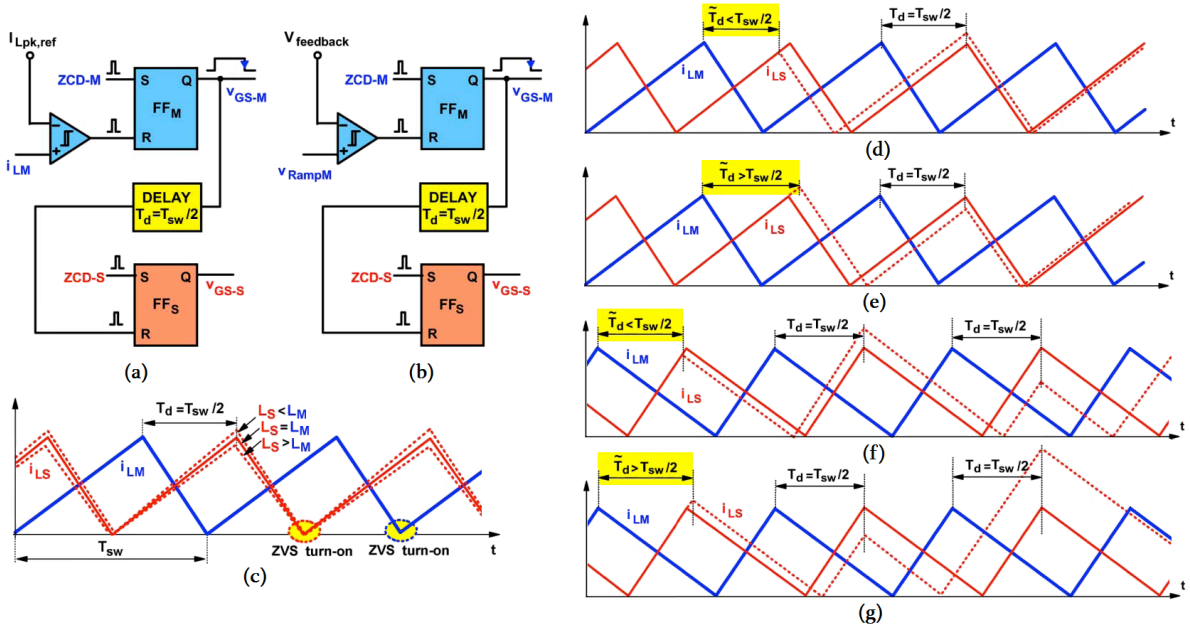

Figure 2.6. The figure shows block diagrams for a (a) current-mode, and (b) voltage-mode controller referenced to the falling edge of the master clock. Provided D >50%, the controllers are stable against inductor mismatches (c) and delay-time perturbations (d) D>50%, delay<½T_{sw}, (e) D>50%, delay>½T_{sw}. However, these controllers are unstable when (f) D<50%, delay<½T_{sw} and (g) D<50%, delay>½ T_{sw}. Image compiled from [10].

Figure 2.6 shows the block diagrams for the current-mode and voltage-mode controllers. By referencing to the falling edge of the master clock, the slave phases have their own ZCS (or ZVS) signal and will always have soft switching. The controller is stable against inductance variations (Figure 2.6c), so identifying the phase with the largest inductance is unnecessary. The controller is unstable when D < 50% (Figure 2.6f and g). In this case unstable means that phase-lock is lost and asynchronous slave current peaks as large as twice the master current peak can be seen. Such peaks could disrupt the system level control, potentially making the entire converter unstable.

The controller is stable and BCM operation is guaranteed when D > 50% (Figure 2.6d and e). Using Equation 22 and the timing diagrams in Figure 2.6d-e, the sequence of current peaks following a single delay-time perturbation can be calculated as shown in Equation 23. The 50% duty cycle restriction is an indirect way of stating that the output voltage must be more than twice the input voltage for controller stability. For $V_{out} > 2 \cdot V_{in}$, the summation converges and the perturbation will decay. When $V_{out} = 2 \cdot V_{in}$ (D=50%) the perturbation response becomes an infinite series, and when $V_{out} < 2 \cdot V_{in}$ the summation diverges.

$$I_{LS,peak}(n) = \frac{V_{in}}{L} \cdot t_{in} + \frac{V_{out} \cdot T_D}{L} \cdot \sum_{n=1} \left(\frac{-V_{in}}{V_{out} - V_{in}} \right)^n \tag{23}$$

The question remains if the controller is stable under dynamic conditions. Calculations show that if the control signal slews faster than the inductor current slope, the slave controller will miss a cycle, but return to normal operation in the next cycle. Figure 2.7 shows the simulation results when the control signal slews at one-tenth of the inductor current slope. At this extremely high control signal slew rate, a few instances of slave current overshoot and small steps (non-monotonic peaks) in the ripple of the input current are seen, but the slave controller remains stable and tracks the master over a two-decade frequency sweep. BCM operation is maintained even when the system is perturbed.

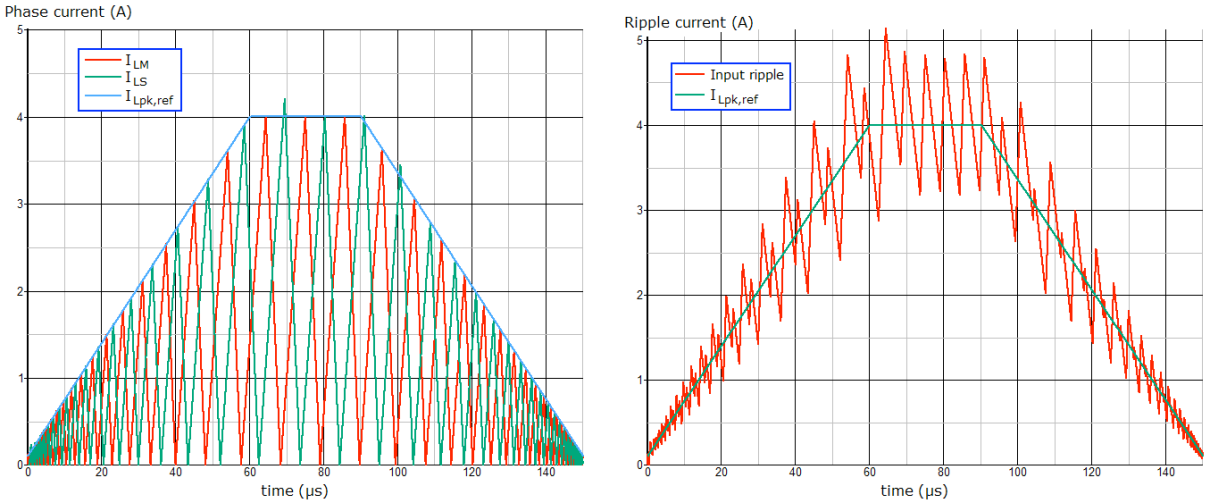

Figure 2.7. The figure shows the PSPICE simulated phase currents and input current for a current-mode controller referenced to the falling edge of the master clock. For extremely high control signal slew rates the slave current overshoots the control signal, and steps in the input current-ripple are seen. However, the controller remains stable even with high control signal slew rates.

The only instability this controller suffers is with a ZVS failure –in which case the controller simply turns off. In some cases this is actually desired, as in the phase shedding schemes that reduce the active phase count during startup or standby operation [14]. A detailed discussion of the controller design is given in the next chapter including the half-cycle delay circuit, the startup sequence, and recovery from a ZVS signal failure. Compared with the other design options, the current- and voltage-mode controllers of Figure 2.6a and b are robust controllers requiring comparatively simple controller hardware. The single ramp-generator design makes this controller ideal for integration in CMOS.

2.5 Closed-loop controllers

Open-loop controllers that reference to the falling edge of the master clock have simple hardware and work really well –provided the duty cycle is greater than 50%. In an effort to improve controller performance when D<50%, closed-loop controllers were developed. These controllers have their own features and problems.

Closed-loop controllers work on the phase-locked-loop principle; they measure the phase difference between phases and delay the slave clock to produce the 180º phase shift relative to the master. The basic assumption here is that both controllers operate with the same frequency. However, the XOR-style phase discriminator requires heavy filtering [6][11]. The long filter time-constant causes a slow tracking response and the controller responds poorly to disturbances, taking tens of cycles to recover from a perturbation [15].

A possible solution is an integrator with sampled output to replace the filter. A variation on that concept is shown in Figure 2.8a [12] where the phase detector and filter functions are combined using a ramp generator and two sample-and-holds. The interleaving circuit ramp is synchronized to the master clock, and the ramp is sampled at half-ramp by the slave ZVS signal and at peak-ramp by the master ZVS signal. A DC error voltage is generated by subtracting the half-peak sample from half of the peak sample. Unfortunately the samples are not correlated to the same ramp, which would reduce sample noise. (Alternatively, the ramp could be synchronized to the slave and the sample signals reversed, which would give a correlated sample.) A g_m circuit converts the error voltage to an error current that steers the slave controller timing ramp. This circuit must sink and source current depending on the error, and a simple version is shown in Figure 2.8b [11]. The timing diagram shows how the controller corrects for slave timing perturbations (Figure 2.8c). In both cases, movement of the slave ZVS signal creates an error voltage that adjusts the slope of the slave ramp generator.

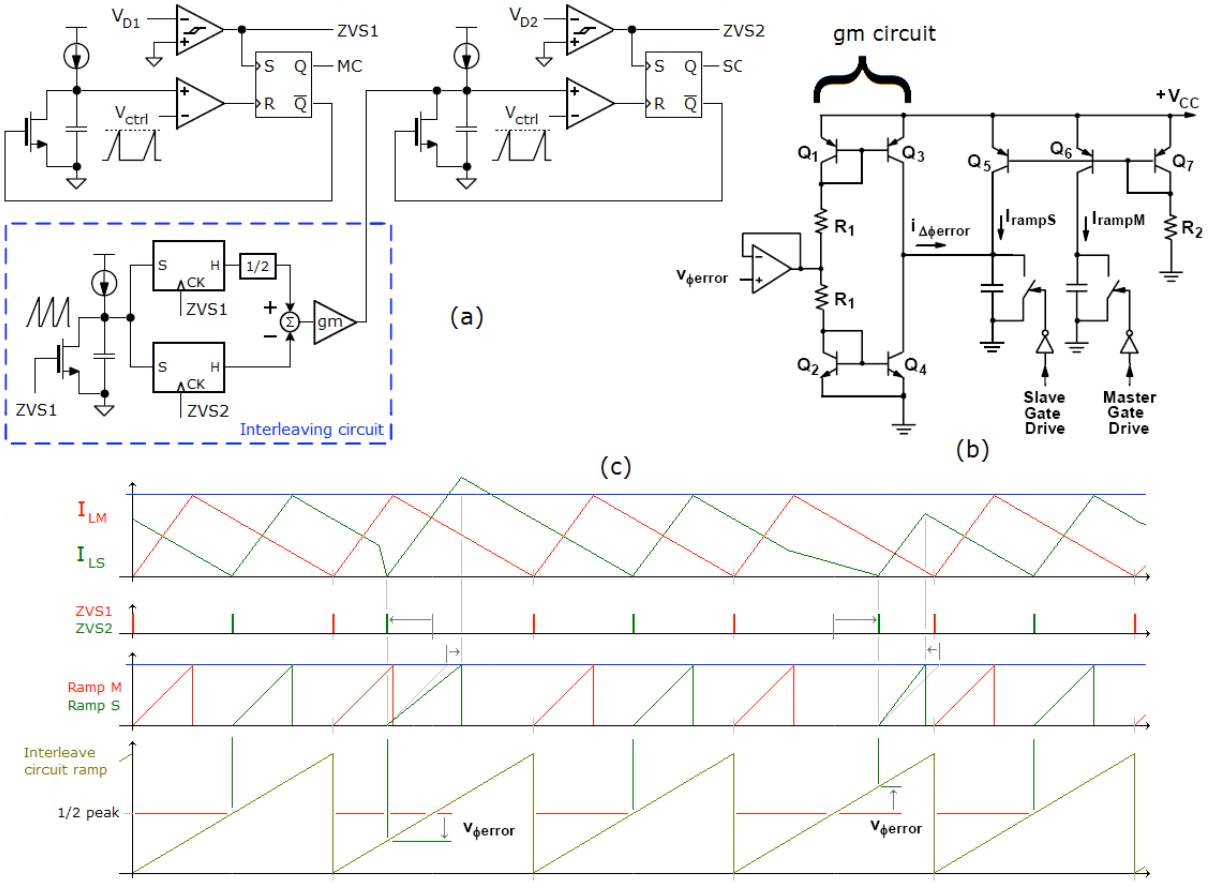

Figure 2.8. The figure shows an implementation for a voltage-mode closed-loop controller. The controller is stable for any duty cycle provided the gain is set correctly. The circuit in (b) [11] is a simple implementation of the g_m circuit, which must source and sink current. Stabilizing the gain of this circuit is essential for controller stability and good tracking. The timing diagram in (c) shows the recovery from perturbations.

The strength of this controller is that it is stable at any duty cycle and soft switching is guaranteed. When implemented using discrete components, component mismatches can be controlled and performance should be good. The g_m gain determines how quickly the circuit tracks and responds to perturbations; however, if g_m exceeds the slave ramp current divided by V_{cc} ($g_m > I_{rampS} / V_{cc}$) the circuit becomes unstable. In order to guarantee stability against component and other variations, the slave settling time must be set greater than one clock cycle.

The weakness of this controller is its complexity. For good performance the three ramp generators should have good matching, and the comparators, sample-and-holds, and subtraction-circuit should have low voltage-offsets. The accuracy of the ½ gain stage directly affects the slave phase angle, and the g_m circuit must have good matching between the N and P current mirrors. All this may be easily achieved with discrete components, but implementing such accuracies in CMOS may be a challenge.

In particular, for the controller to operate at the typical frequencies used in switch-mode converters, the ramp currents must be low. For instance, a converter with a 50kHz minimum switching frequency and 1pF integration capacitors will need a ramp current of 250nA (assuming a 5V range). Current mirror matching in this weak-inversion regime will be poor, and large errors will be seen. Not only is good matching required, but good component accuracy is required as well. The g_m gain must be carefully set, which may be a real challenge in CMOS because process variations limit the accuracy. The circuit requires an accurate current reference, which may not be as easy to achieve as the authors of the circuit suggest [12].

Of the controller options available, the open-loop controllers that synchronize to the master clock falling edge are simple and provide good performance provided the duty cycle restriction can be tolerated. A voltage-mode open-loop controller was implemented in CMOS and is discussed in the next chapter. The closed-loop controller discussed in this section is one of the best published examples. It has some distinct advantages and with perhaps a little additional work may be the best available option as a general multiphase controller.

2.6 Coupled-inductors

Interleaved controllers maintain a 180º phase shift between converter phases so that one phase is magnetized while the other phase demagnetizes. Ideally, it would be nice if some of the magnetizing energy could be diverted directly to the demagnetizing phase and thus bypass storage in the magnetic core altogether. This could potentially reduce the core size and losses associated with magnetizing and demagnetizing [7]. A byproduct of such a scheme would be that the magnetizing inductance appears larger than it actually is, meaning that the actual inductance could be reduced [4]. This could reduce the ohmic losses because there would be fewer winding turns in the inductor. This was the motivation behind the coupled-inductor concept. Mutual coupling can be achieved by winding the two inductors on the same core, providing a third benefit that the number of cores is reduced.

Figure 2.9 shows the coupled-inductor circuit configuration. Using Faraday's Law ($\mathcal{E}mf_{12} = -M \cdot dI_2/dt$) and the definition for mutual inductance ($M = k \cdot (\mathrm{sqrt}(L_1 \cdot L_2))$) [16], the inductor currents for the boost configuration are derived; the coupled equations are given as Equations 24 and 25, where k is the coupling coefficient between the inductors.

$$\Delta I_1 = \frac{V_{L1} \cdot \Delta t}{L_1 \cdot (1-k^2)} + \frac{k \cdot \sqrt{L_1 \cdot L_2} \cdot V_{L2} \cdot \Delta t}{L_1 \cdot L_2 \cdot (1-k^2)} \tag{24}$$

$$\Delta I_2 = \frac{k \cdot \sqrt{L_1 \cdot L_2} \cdot V_{L1} \cdot \Delta t}{L_1 \cdot L_1 \cdot (1-k^2)} + \frac{V_{L2} \cdot \Delta t}{L_2 \cdot (1-k^2)} \tag{25}$$

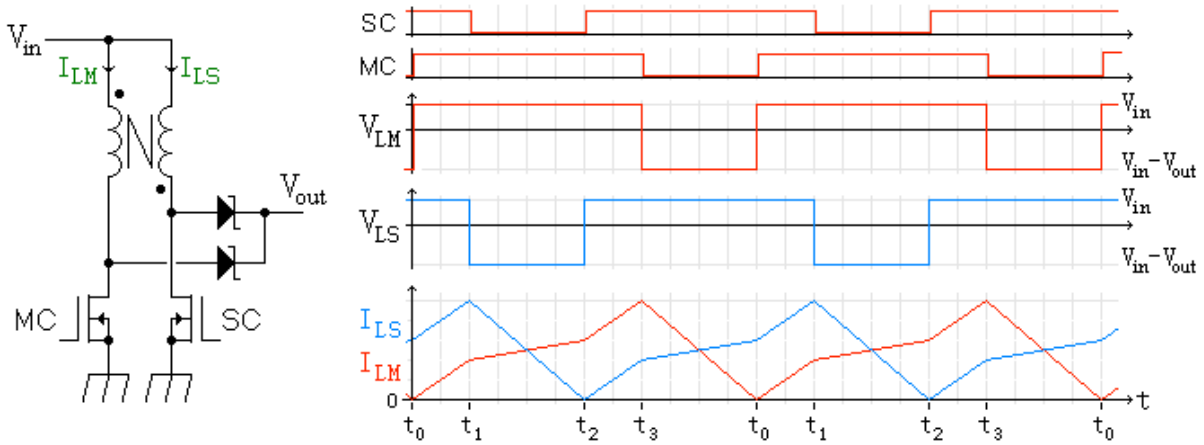

Figure 2.9. A modification of the 2-phase interleaved converter is to couple the inductors, which can be done when they are wound on the same core. The favorable cases are the t_1-t_2 and t_3-t_0 intervals where the demagnetizing inductor causes a significant reduction in the I_L slope of the magnetizing inductor.

Consider the case where Vin=5V, Vout=15V (so D =0.667, as shown in Figure 2.9), and LS=LM=5µH, and wound so that k = 0.33. The coupled-inductor current slopes are then computed using Equations 24 and 25 and compared against an uncoupled 5µH inductor for each timing interval of Figure 2.9. This result is shown in Table 2.2 below.

Time interval	V_{LM}	V_{LS}	I_{LM} (coupled)	I_{LM} (uncoupled)	I_{LS} (coupled)	I_{LS} (uncoupled)
t_0-t_1, t_2-t_3	+5V	+5V	+1.49A/µs	+1A/µs	+1.49A/µs	+1A/µs
t_1-t_2	+5V	-10V	+0.38A/µs	+1A/µs	-1.87A/µs	-2A/µs
t_3-t_0	-10V	+5V	-1.87A/µs	-2A/µs	+0.38A/µs	+1A/µs
-	-10V	-10V	-2.98A/µs	-2A/µs	-2.98A/µs	-2A/µs

Table 2.2. The coupled-inductor current slopes are compared against the uncoupled 5µH inductor for the different timing intervals of Figure 2.9. The calculations apply for inductor coupling coefficient k=0.33.

From Table 2.2, the time intervals where both phases are magnetizing (t_0-t_1 and t_2-t_3) or demagnetizing (-) have current slopes that are larger than is seen in the uncoupled inductor. In this case the inductor appears smaller than it actually is, which is undesired. However, when one phase magnetizes while the other demagnetizes (t_1-t_2 and t_3-t_0), the inductance appears larger than it is. That the input energy is bypassing storage in the magnetic core and going directly to the output can be seen in the reduced I_{LM} slope (from -2 to -1.87A/µs during interval t_3-t_0). Favorable conditions for a coupled-inductor design then are conditions where the t_0-t_1 and t_2-t_3 intervals are minimized, and the t_1-t_2 and t_3-t_0 intervals are maximized. This occurs as the duty cycle drops toward 50%.

The degree to which this coupling benefits or harms the converter performance is better understood by comparing the coupled-inductor against an equivalent uncoupled inductance with the same power output given the same cycle time. A pair of 5µH coupled-inductors with k=0.5 deliver the same power as two single 7.5µH inductors operating at the same switching frequency and 50% duty cycle (Figure 2.10).

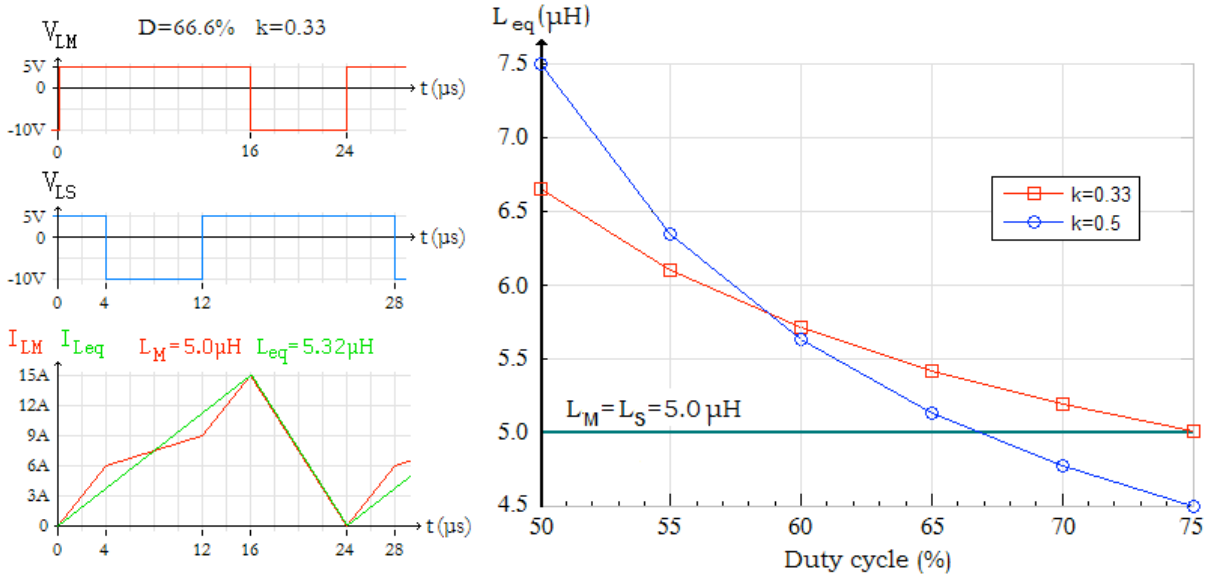

Figure 2.10. When the inductor is wound as a coupled-inductor, its inductance appears larger or smaller depending on the inductor coupling and operating duty cycle. With k=0.33 and a 66.6% duty cycle, a 5µH coupled-inductor has behavior equivalent to a 5.32µH uncoupled inductor.

The coupled-inductor stores less energy in the core –about a factor of two times less energy while delivering the same output power. The inductor power is simply the $V_L \cdot I_L$ product; power is negative when the inductor delivers energy. The uncoupled inductor power has a negative peak equal to $I_{LU,peak} \cdot (V_{in} - V_{out})$ while the coupled-inductor negative peak is reduced to $(I_{LM,peak} - k \cdot I_{LS}) \cdot (V_{in} - V_{out})$, as shown in Figure 2.11. The energy delivered by the uncoupled inductor equals the sum of the shaded areas (A+B), while the energy delivered by the coupled-inductor is just shaded area A. It might seem that coupling means less energy is converted, but the average power supplied by the source is the same as in a circuit with uncoupled inductance L_{eq}. The balance of the delivered energy (shaded area B) is coupled from the slave phase, resulting in the reduced I_{LS} slope during the t_3-t_0 interval.

The inductor power is zero when $k \cdot I_{LS} = I_{LM}$; however power is still delivered to the load until $I_{LM} = 0$ at t_0. Coupling thus has a significant secondary benefit: during this interval the net inductor flux becomes negative. This has the same effect in core demagnetization as would occur if I_{LM} became negative. With any luck the field strength due to coupling may be large enough to eliminate any remnant core magnetization. This increases μ_r and helps increase the current at which saturation will occur.

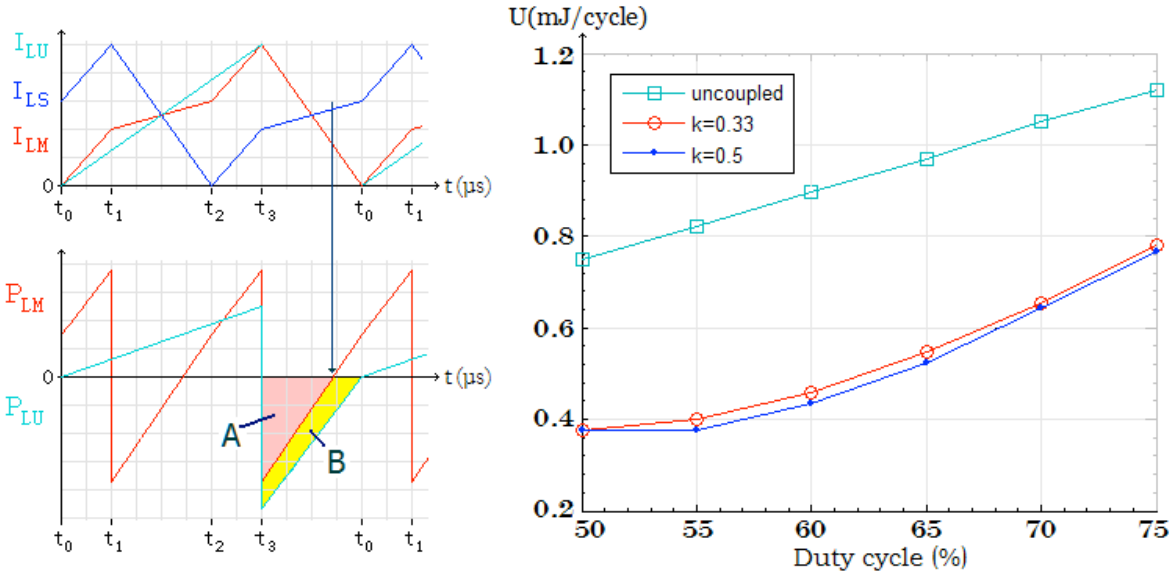

Figure 2.11. The uncoupled inductor stores energy U proportional to shaded areas A+B on each cycle. When two inductors are coupled, energy storage is reduced by the factor proportional to shaded area B (about half). For the simulation data the input power is constant (50W/phase) and the cycle time is 15µs. The inductance was changed to provide the constant power output versus duty cycle. V_{in} was 5V, and the peak current was 20A.

There are several ways to achieve inductor coupling. One way is to wind the coils on different legs of the core, and give each leg its own gap [7]. The reluctance of each leg is determined primarily by the air gap and the core material can be ignored. Equation 26 can be used to calculate the reluctance of each leg, and Equation 27 gives the flux coupled from L_1 to L_2 from which the coupling factor k is derived. The flux coupling is analogous to the current division in resistor networks. Caution must be used when this coupling approach is taken. If the outer legs have a smaller cross-sectional area than the center leg, B will increase compared to the uncoupled inductor wound on the center leg ($B = \Psi/A$, $\Psi = N \cdot I_L/\mathcal{R}$). Even though the flux decreased, the standard industry E and ETD cores do not provide a favorable geometry needed to achieve a lower ΔB.

$$\Re_{center} = \frac{\ell_{gap,center}}{\mu_0 \cdot A_{center}} \tag{26}$$

$$\psi_{12} = \psi_1 \cdot \frac{\Re_{center}}{\Re_{center} + \Re_2} = \psi_1 \cdot k \tag{27}$$

Inductor coupling can also be achieved with crossed windings between separate cores [17]. The number of cores is no longer reduced, and care must be used to control the additional winding resistance and field emissions, but it does allow standard industry cores to be used.

Figure 2.12 illustrates how the flux and coupling are calculated. For the E32/6 core, the area of the center leg is $129 \cdot 10^{-6}$ m^2 and the area of the outer legs is $69.6 \cdot 10^{-6}$ m^2. If the effective gap lengths are all 1mm, then the reluctance of the center leg is 6169kΩ and that of the outer legs is 11434kΩ. The coupling factor is calculated as k=0.35. When the gap lengths are equal no gap grinding is necessary, and spacing can be achieved with a dielectric spacer. If higher coupling is needed, the center leg gap length can be increased [7].

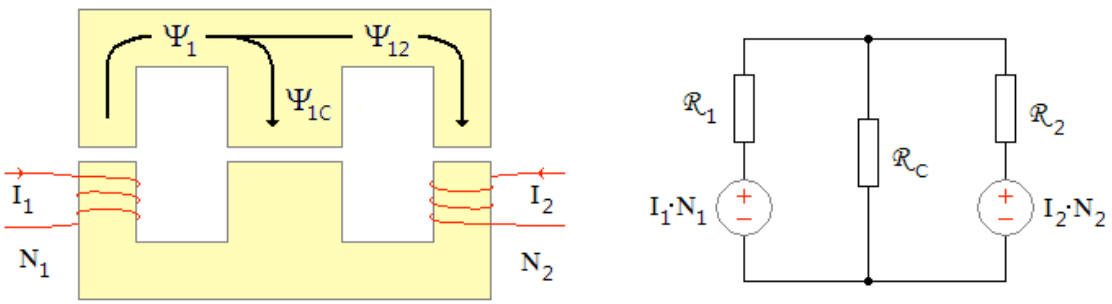

Figure 2.12. The coupled inductors are wound on separate core legs and the gap length and area of each leg determines the coupling factor. The flux in a magnetic circuit is analogous to the current in a resistor network.

Using Equations 24-27 and the timing diagram, the minimum and maximum flux through a converter cycle can be calculated for different duty cycles and coupling. The flux coupled from leg 1 to leg 2 is $\Psi_{12} = k \cdot \Psi_1$; the flux from leg 1 to the center leg is then $\Psi_{1C} = (1-k) \cdot \Psi_1$. For a coupled inductor wound as seen in Figure 2.12, the calculated fluxes are shown in Figure 2.13. The flux was normalized to the flux seen in the leg and center post in an equivalent uncoupled inductor.

A significant flux reduction is seen in the center leg, with a corresponding flux increase in the outer legs. This makes sense because energy is coupled directly between L_M and L_S. The increased $\Delta\Psi$ requires an increased cross-sectional area of the legs to reduce ΔB and limit core losses. Although $\Delta\Psi$ increased, the peak flux is reduced. Coupling shifts the entire B·H curve downward with a desired negative flux in the outer legs that helps demagnetize the core and reduce saturation. The reduced $\Delta\Psi$ in the center leg will reduce the core losses seen in that leg, but it will also cause a net magnetization with a corresponding reduction in μ_r for the center leg. To the extent that this occurs, the increased material reluctance of the center leg will only increase the coupling factor slightly since the mutual coupling stabilizes the flux.

It is worth noting that the outer leg results are a mirror image of the results in Figure 2.10. The increase in apparent inductance at lower duty cycles is offset by an increase in the peak-to-peak flux, which could increase core losses. This is yet another example of the tradeoff between ohmic and core losses in switch mode circuits.

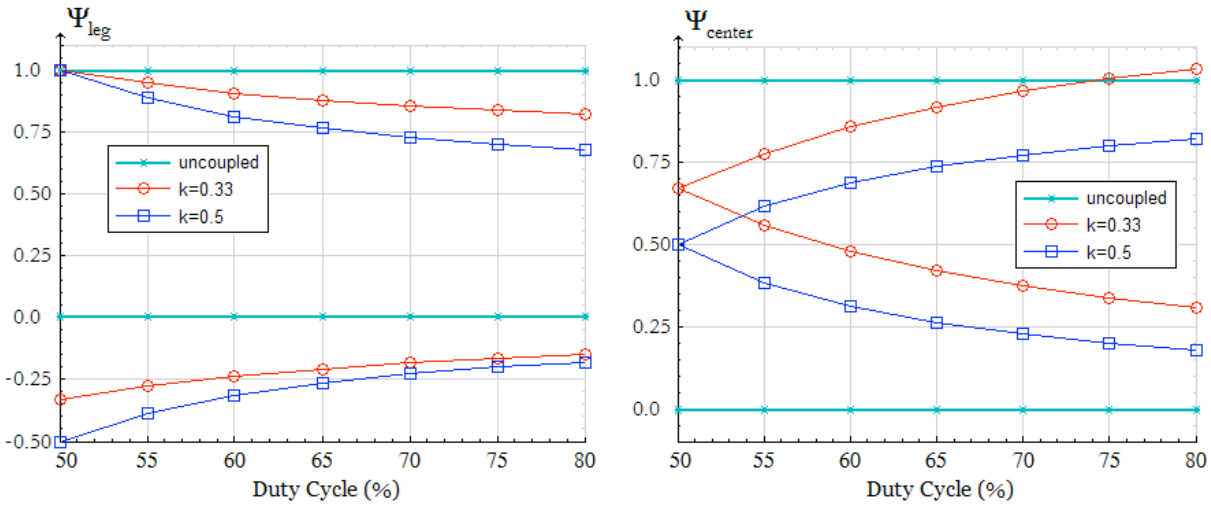

Figure 2.13. The graphs show the minimum and maximum flux seen over the converter cycle. The flux was normalized to the flux seen in an uncoupled inductor for both the center and outer legs, when the inductor is wound as shown in Figure 2.12.

The mutual coupling creates a feedback between L_S and L_M, which causes the slave current to influence the master current and timing. This feedback complicates stability and can create chaotic operation or bi-stable conditions as seen in Figure 2.13a. Fortunately, methods exist to deal with the instability (b).

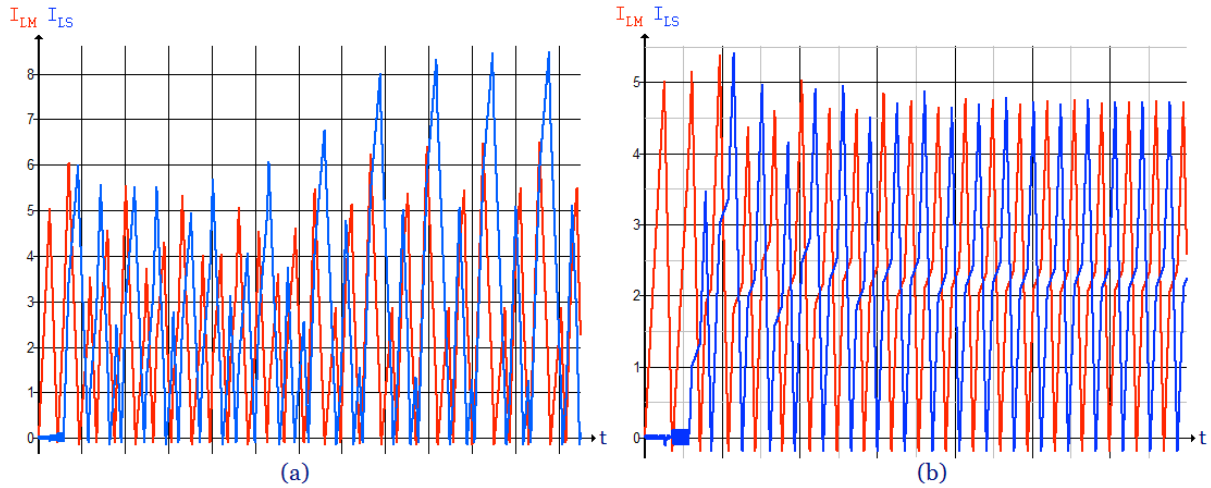

Figure 2.14. Mutual inductor coupling creates a feedback between master and slave that can cause system instability (a). However, conditions exist under which stable operation can be achieved (b).

It is not surprising that the stability problems with coupled inductors occur with voltage-mode control. As the coupling increases the minimum duty cycle at which the circuit is stable also increases. If voltage-mode control is needed, the solution would be to operate in DCM and use valley switching to reduce the switching losses. In all cases current-mode control will be stable.

Control mode	Conduction mode	Coupling k	Duty cycle
Voltage-mode	BCM	0.2	> 58%
Voltage-mode	BCM	0.33	> 66%
Voltage-mode	BCM	0.5	> 73%
Voltage-mode	DCM	All	> 50%
Current-mode	BCM	All	All

Table 2.3. The table shows the conditions under which the coupled-inductor converter is stable.

Coupling the inductors in switch mode power converters is a relatively new development that will likely become more common in future designs. By reducing the energy stored in the core and gap, shifting the B·H curve away from saturation, and coupling a negative flux into the core material, the saturation current is increased. This causes a better utilization of the core, which reduces the number and size of the core needed. It should be expected that the industry will respond with cores specifically designed for coupled inductors.

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3. Controller integration in silicon

Discrete circuits have the advantage that component accuracy is high and the tolerance is tightly controlled. Metal film resistors with 1% and 0.1% tolerance and 50ppm temperature coefficients are readily available. Active components are LASER-trimmed for low voltage offsets and high precision. However this accuracy is expensive and manufacturing circuits with many components is complex. For high-volume production the industry is moving toward low-cost, compact, easily manufactured designs. CMOS ASICs offer an attractive option in reducing size, cost, and manufacturing complexity provided that the design issues can be resolved. Discussing the technical challenges of controller integration in CMOS is the topic of this chapter.

3.1 Current sources

A current source, capacitor, and comparator form a ramp generator that is the heart of most timing controllers used in switch mode power systems. The power converter dynamic range is directly proportional to the dynamic range and accuracy of this timing circuit. The comparator input offset voltage and input common-mode range and ramp generator kT/C noise can limit the dynamic range to a factor of 100 or less. However the current source has the potential to reduce this range much further, as seen in the component current variations in Figure 3.1. Stabilizing the current source against changes in temperature, process, and controller supply voltage is therefore an important part of the controller design and discussion.

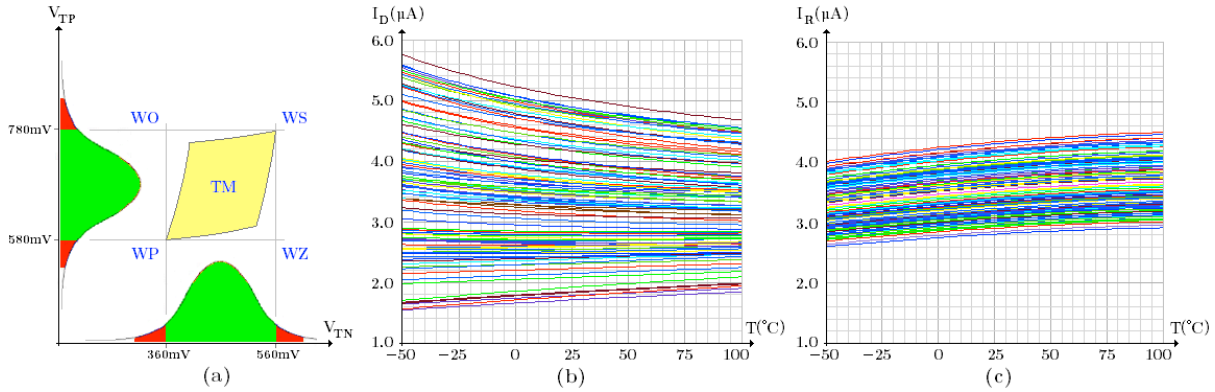

Figure 3.1. The N and P MOSFET threshold voltages have a Gaussian distribution. The transient model (TM) is the most probable voltage, and the four corners (WO, WS, WP, and WZ) [1] give the upper and lower threshold limits allowed by the technology (a). For a single NMOS with fixed drain and gate voltages, the drain current shows large variations against wafer-run process and die temperature (b). For a fixed voltage the poly resistor also shows large process and temperature variations (c).

The large current spread typical in CMOS is due to dopant variations, which affects carrier mobility and threshold voltage. A typical current source will have resistors, NMOS, and PMOS transistors that are manufactured during different process steps and so have large uncorrelated process variations. Since CMOS process is unlikely to improve significantly, designers are challenged to solve the process-variation problem at the circuit level [2]. Many papers have been published about current source design, but achieving good results is still a serious challenge.

Unlike bandgap voltage references for which cookbook design recipes exist and textbook discussions abound, there is no comprehensive design guide available for current sources. Textbook discussions [3][4] tend to concentrate on reducing the sensitivity to power supply variations, often quoting the change in current per volt of change in the supply voltage. Temperature sensitivity is given secondary priority and wafer-to-wafer process variations are often ignored. The supply-independent current source (Figure 3.6a) can be temperature stabilized by adding a diode, but overall this circuit has high sensitivity to process variations [5]. A simulation of this circuit gave a standard deviation over mean (σ/μ) of 15.48% for 100 Monte Carlo simulation runs looking at process and temperature variations. For a nominal 10µA current source the current varied from 6.9µA to 13.3µA in 100 process runs. This large variation makes this current source useless for timing generation, and another approach is needed.

Alternatively the controller power could be supplied by a bandgap-referenced voltage source. Such a regulated supply can easily achieve a +/-3% accuracy against process and temperature variations. This allows the circuit to be optimized toward reducing process and temperature sensitivities, and supply variations can be given a secondary priority in the design. Additionally, instead of viewing the MOSFET body effect as an error to be ignored, I hope to demonstrate that the body effect can be used as an effective tool for adjusting the temperature coefficient and reducing process sensitivity.

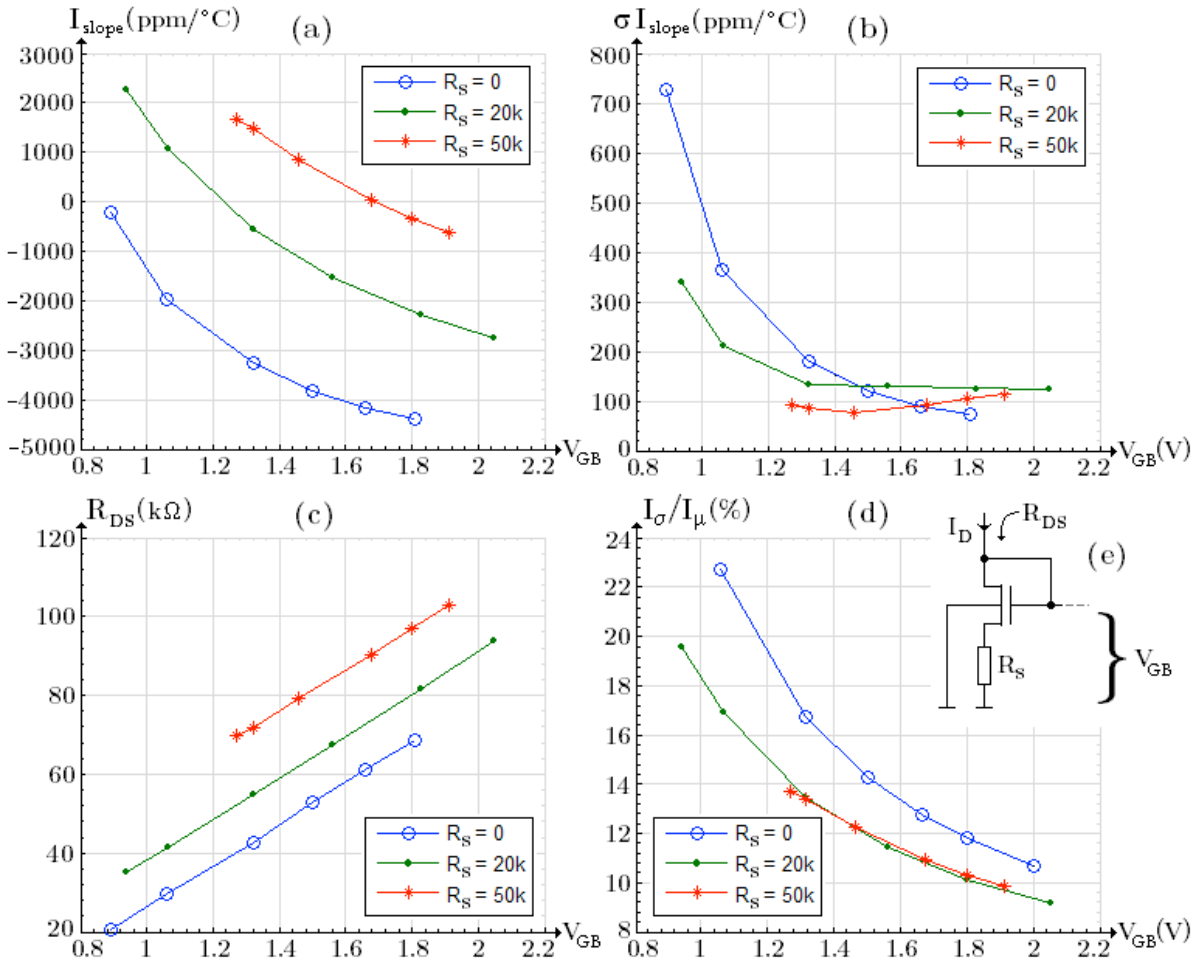

Figure 3.2. A diode-connected NMOS with optional degenerative source resistor R_S is characterized using the AMS 0.35µm 50V process technology (e). The average temperature-dependent current slope (a) and current-slope spread (b) are determined for different gate-to-body voltages V_{GB} over the temperature span from -50°C to 100°C. The small-signal impedance looking into the drain for the specific drain current I_D = 10µA (25°C) is shown in (c). Graph (d) shows the standard deviation over mean (σ/µ) of the drain current against run-to-run process variations at different gate-to-body voltages (25°C). Both (b) and (d) are measures of the process noise associated with wafer-to-wafer variations (they are not measures of circuit noise or component mismatch).

As shown in Figure 3.2a the transistor current can be proportional-to-absolute-temperature (PTAT –the current increases as temperature increases) or complimentary-to-absolute-temperature (CTAT –current decreases as temperature increases) depending on V_{GB}. This characterization is independent of I_D and W/L since this slope is influenced only by carrier mobility and threshold voltage, both of which decrease with temperature [6]. However, the designer has a powerful tool in modulating this slope using the transistor body effect via poly resistor R_S (with current slope +732 ppm/°C) as shown in the figure. This plotted slopes are normalized using the formula $I_{slope} = (I_{D,100°C} - I_{D,-50°C}) / (I_{D,25°C} \cdot 150°C)$ and are independent of I_D.

The standard deviation (spread) of this slope is shown in Figure 3.2b. This spread is associated with the wafer-to-wafer process variations, and it gives an indication of how repeatable the temperature slope is. As was seen in Figure 3.1b, selecting a gate voltage below 1V may result in an average temperature slope near zero, but a large dispersion of slopes between wafer runs will occur. Some texts suggest that the zero temperature coefficient (ZTC) bias point (880mV in Figure 3.2a) can achieve constant drain current against temperature variations, however this will have poor repeatability between wafer runs. However the AMS models suggest that a favorable feedback is introduced when the body effect is implemented with R_S and this significantly reduces slope variations associated with process.

The transistor current variation from one wafer to the next can be considered as process noise. For an average current I_μ based on the transient model (TM), there will be an associated standard deviation I_σ over many process runs. The effect of process variations is reduced as V_{GB} increases, and source degeneration can further reduce the process noise through feedback ($\uparrow I_D \rightarrow V_{RS}\uparrow \rightarrow V_{GB}\downarrow \rightarrow I_D\downarrow$). As shown in Figure 3.2(d) there is a limit to how large R_S can be. As the source resistance increases its own process noise begins to dominate; σ/µ for the poly resistor is 11.3% and this accounts for a larger σ/µ when R_S is increased above 50kΩ. The information in Figure 3.2 is a starting point for a process- and temperature-stable design.

3.1.1 Temperature and power supply variations

A current source can be thought of as a summing node between two impedances that is supplied by a stable voltage source as shown in Figure 3.3a. The simplest implementation is a current mirror and resistor (Figure 3.3b), which is used to demonstrate the design concept.

Using the simplified model, the power supply sensitivity is easily estimated (Equation 28). R_N and R_P are the closed-loop small-signal impedances whose combined impedance determines the current sensitivity to bias supply variations. The excellent power supply rejection of the classic current source is achieved using a high-impedance node. To limit sensitivity to bias variations a larger MOSFET R_{DS} is desirable. Fortunately, source degeneration increases MOSFET output impedance, and operating with increased gate voltage decreases process noise.

$$\Delta I_D = \frac{\Delta V_{bias}}{R_N + R_P} \tag{28}$$

There is a great deal of flexibility in achieving a temperature-stable circuit. Source degeneration can be used to custom design the MOSFET current slope, and the P-side and N-side slopes are weighted by their impedances (Equation 29). If one side is PTAT and the other side is CTAT a temperature-stable design is achieved when the condition in Equation 30 is met.

$$I_{slope,circuit} = \frac{R_P \cdot I_{slope,P} + R_N \cdot I_{slope,N}}{R_N + R_P} \tag{29}$$

$$R_P \cdot I_{slope,P} = R_N \cdot I_{slope,N} \tag{30}$$

This slope-impedance relationship can be used to achieve a temperature-stable design even when there are large differences between the P-side and N-side current slopes. This is illustrated in Figure 3.3c where the MOSFET has a large negative temperature slope and smaller output resistance R_N, and the resistor has a smaller positive temperature slope and larger resistance R_P. The combined circuit achieves nearly temperature-stable operation as seen in Figure 3.3d.

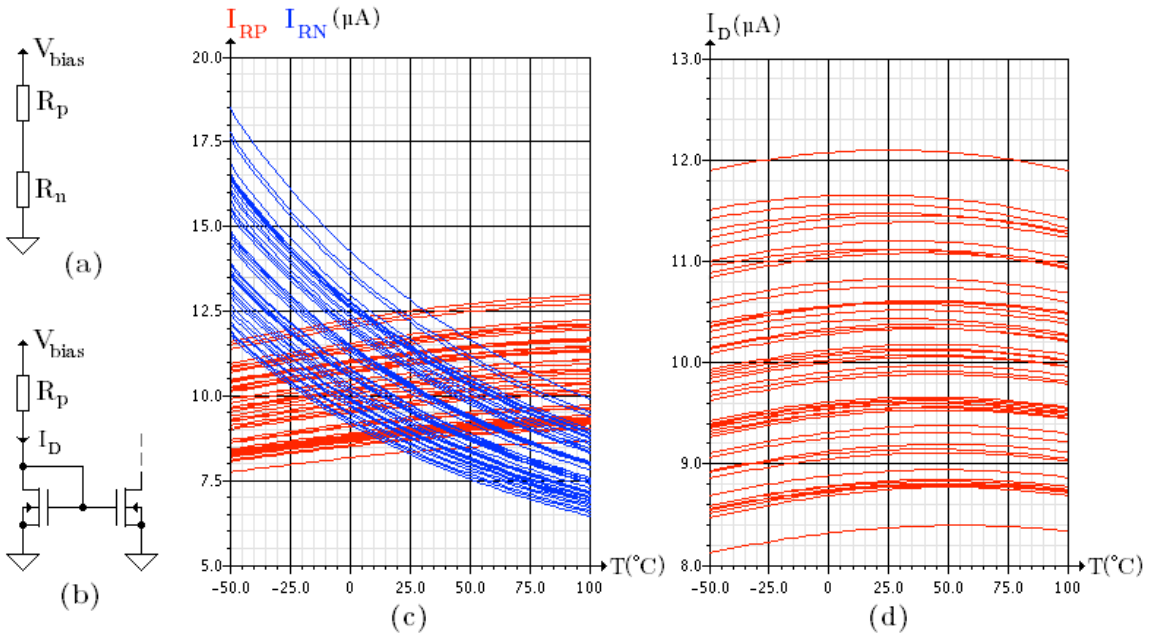

Figure 3.3. A current source can be simplified as two closed-loop impedances for which the current temperature slope, small-signal resistance, and process noise are known. From these parameters the circuit performance can be calculated (a). A simple current source is used to explain the analysis (b). Individually R_p and the NMOS current mirror have +731ppm/°C and -4370ppm/°C temperature slopes respectively with nominal bias (c). The NMOS has a drain impedance of 68.3kΩ; R_p is selected to satisfy the condition in Equation 30 (R_p = 408.3kΩ) and a temperature-stable current results for the circuit (d).

Many operating points can achieve temperature-stable operation, but selecting an operating point where σI_{slope} and the transistor I_σ/I_μ are high will result in a larger current spread for the circuit. A few examples shown in Table 3.1 illustrate the point.

MOSFET				Resistor			Circuit		
R_{DS}	R_S	$I_{slope} \pm \sigma I_{slope}$	I_σ / I_μ	R_P	I_{slope}	I_σ / I_μ	V_{bias}	$I_{slope} \pm \sigma I_{slope}$	I_σ / I_μ
23.0kΩ	0Ω	-738 ± 696ppm/°C	28.2%	23.3kΩ	+731ppm/°C	11.3%	1.17V	-13 ± 166ppm/°C	15.4%
68.3kΩ	0Ω	-4370 ± 73ppm/°C	12.1%	408kΩ	+731ppm/°C	11.3%	5.90V	24 ± 54ppm/°C	10.4%
54.9kΩ	20kΩ	-560 ± 134ppm/°C	13.4%	42.1kΩ	+731ppm/°C	11.3%	1.74V	7 ± 94ppm/°C	8.73%
102.7kΩ	50kΩ	-634 ± 115ppm/°C	9.86%	89.1kΩ	+731ppm/°C	11.3%	2.80V	13 ± 74ppm/°C	8.44%

Table 3.1. The table shows four possible temperature-stable operating points. Selecting an operating point where the MOSFET has a larger σI_{slope} and I_σ/I_μ will increase the current spread for the circuit.

The zero temperature coefficient (ZTC) operating point is subject to high process noise; the problem is that the drain current is much more susceptible to threshold voltage variations at lower gate voltages. Some researchers have argued in favor of the ZTC operating point, saying that the gate voltage could be adjusted in response to process variations. The nominal 880mV gate-to-source voltage could be adjusted up to 1.0V in the event of a WP process corner for instance (Figure 3.4a). The problem is that without a reference current for comparison, any adjustment circuit has no way of really knowing what the adjustment should be. Attempts to implement this scheme have met with some success in novel applications (1V supply [7], 9nA output current [8]), however the published results are not better than can be achieved with a simple current source under nominal conditions. The high process sensitivity at ZTC makes it difficult to achieve a stable output current.

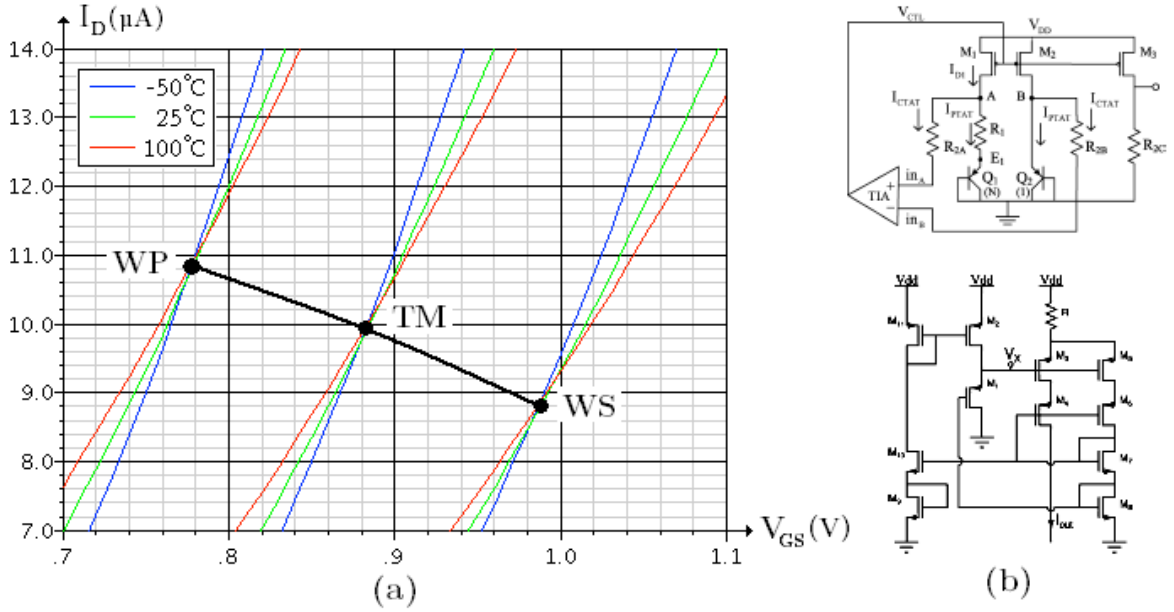

Figure 3.4. To address the temperature-stability problem, some designs attempt to bias the MOSFET at a ZTC operating point –the V_{BS} at which $I_{slope} = 0$ (Figure 3.2a). However this gate-body voltage is also associated with a high σI_{slope} (Figure 3.2b) and large I_σ/I_μ (Figure 3.2d). The problem is that the bias point for ZTC operation is highly sensitive to process variations (a). Circuits attempting to reduce process sensitivity by adjusting V_{GS} up or down (b) have not achieved better results [7][8] than could be achieved with a simple current source.

3.1.2 CMOS process variations

Process errors are categorized as component mismatches for components on the same wafer, and wafer-to-wafer variations. Common centroid layout, interdigitated components, and closely spaced components with common layout orientation are effective in reducing component mismatch errors [9]. Wafer-to-wafer variations must be addressed in the circuit design. As seen in the last three examples of Table 3.1, it is possible for the circuit to have less sensitivity to process variations than is seen in the individual components. Further analysis of the simple current source can help reduce the circuit's response to process variations and show the limits of what can be done.

$$I_D \cdot R_p + \sqrt{\frac{2 \cdot L}{k_n \cdot W}} \cdot \sqrt{I_D} + (V_{TN} - V_{bias}) = 0 \tag{31}$$

$$\sqrt{I_D} = \sqrt{\frac{L}{2 \cdot k_N \cdot W \cdot R_P^{\,2}} + \frac{V_{bias} - V_{TN}}{R_P}} - \sqrt{\frac{L}{2 \cdot k_N \cdot W \cdot R_P^{\,2}}} \tag{32}$$

The current has a quadratic relationship (Equation 31) whose solution is given in Equation 32, whereV_{TN} is the threshold voltage and k_N is the transconductance parameter ($k_N=\mu_N \cdot C_{gate}$). k_N, V_{TN}, and R_P are all process-dependent variables. Attempts to stabilize circuit operation must deal with a convolution of the process variations (δk_N, δV_{TN}, δk_P, δV_{TP}, and δR_P) whose correction circuitry is also confounded by these same process variations. The circuit has an inherent feedback: if k_N increases due to process variations from TM to WP, the increased drain current is opposed by a larger voltage drop across R_P, which decreases the gate voltage. However, if the resistance also has a WP process variation, then the whole feedback benefit is lost and a large current increase is seen. Every correction circuit is confounded by this problem, but as demonstrated in the following experiment, some improvements can still be made.

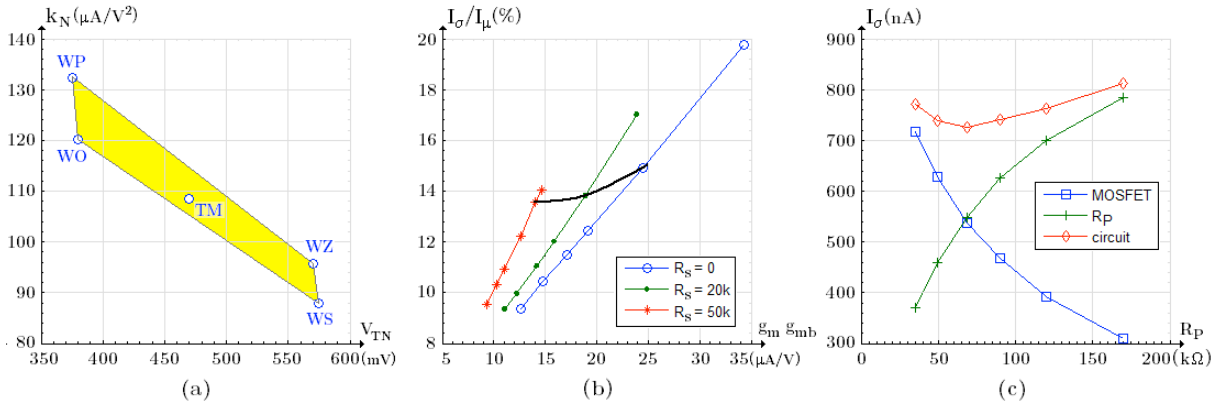

Figure 3.5. The process spread at a given operating point is characterized as variations of k_N and V_{TN} (a). A linear relationship between the transistor process noise (I_σ/I_μ) and gain (g_m or g_{mb}) is seen. By selecting a low-gain operating point the MOSFET process noise is reduced (b). For a fixed operating point, R_P and V_{bias} can be varied to determine the relative process noise contributions of both components (c). (These characterizations were for long-channel devices operated at I_D = 10µA.)

In addition to process variations, k_N is also sensitive to the operating point: carrier mobility, and thus k_N, decrease with increasing gate voltage [10]. Thus some operating points have much lower sensitivity to process variations. A minor reduction in process sensitivity is also seen with source degeneration where V_{TN} variations are reduced due to the body effect. Starting from a fixed operating point with low process sensitivity, R_P and V_{bias} are varied to obtain process noise curves for the two components and the circuit (Figure 3.5c). Using the data from Figure 3.5 the following generalizations are drawn:

- Selecting a low-gain operating point reduces the MOSFET's sensitivity to its own process variations (Figure 3.5b). Lower gains are typical for long-channel devices, and the effects of V_{TN} variations (Figure 3.5a) are reduced at higher gate-to-source voltages.
- Current sources are typically low-gain circuits and therefore heavily influenced by component variations; increasing the "circuit gain" would decrease sensitivity to these variations. The circuit gain ($g_m \cdot R_P$) in this simulation increased from -0.72(V/V) to -2.5(V/V) as R_P varied from 49kΩ to 170kΩ. As the circuit gain increases the MOSFET's process noise contribution decreases because feedback decreases sensitivity to variations in k_N and V_{TN} (I_σ for the MOSFET decreases in Figure 3.5c).
- From the resistor's perspective the transistor appears as a load with impedance $1/g_m$. As R_P increases the "resistor divider gain" increases to a limit of one (gain = $R_P/(R_P + 1/g_m)$). So the circuit's sensitivity to resistor process variations increases as R_P increases because the divider gain increases from the perspective of R_P (I_σ for the resistor increases toward the limit 10µA · 11.3% in Figure 3.5c).
- When constrained with a constant gate-to-body voltage (the black line in Figure 3.5a), adding source degeneration (R_S) reduces MOSFET gain and process sensitivity.

These results show the conflicting objectives: component gain should be low (low g_m and low R_P) to reduce the component's process noise contribution; circuit gain should be high to reduce the circuit's response to component process variations.

Many circuits such as voltage references and op amps reduce sensitivity to component variations by amplifying the error between a feedback and reference voltage. Unfortunately node voltages in the basic current source summing nodes do not increase monotonically with process-related changes in current. Table 3.2 clarifies this point.

Since it is unlikely that the process errors can be de-convolved, the table results imply that voltage-mode control cannot stabilize the current source against process variations because there is no node voltage, or linear combination of node voltages, that can produce a suitable control signal. However, current mirroring shows high immunity against these process variations and so current-mode control [11] might be a feedback option that helps stabilize the circuit.

R model	MOS model	I_D (μA)	I_{mirror}(μA)	V_S(mV)	V_G(V)
WS	WS	7.862	7.861	196	2.078
WS	TM	8.355	8.356	208	1.894
WS	WP	8.824	8.828	219	1.723
TM	WS	9.394	9.392	189	2.186
TM	TM	10.0	10.0	201	2.0
TM	WP	10.580	10.583	213	1.821
WP	WS	11.526	11.522	180	2.321
WP	TM	12.284	12.283	193	2.128
WP	WP	12.963	13.021	204	1.948

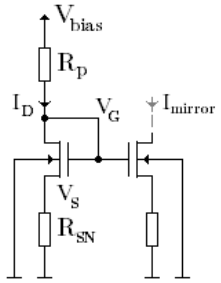

Table 3.2. For a simple current source with 50kΩ source degeneration the current and node voltages are characterized against process variations. No node voltage, or linear combination of node voltages, change monotonically with current. This means that voltage-mode control cannot stabilize the current source against process variations. However, mirrored currents have some immunity against process variations, and so current-mode control [11] could possibly reduce current source sensitivity to process variations.

The concepts just described can be used to improve the current source against variations as follows:

- The supply-independent current source has excellent power supply rejection in the TM case. However, in the non-ideal case of component process variations the circuit is sensitive to power supply variations and it is not temperature stable. To achieve temperature stability, it is necessary to add a diode as shown in Figure 3.6a. The summing node comprises the two PMOS transistors, source resistor, and the diode. Since the transistors must have different sizes, the circuit is subject to four different process variations. The resulting circuit has high sensitivity to process variations as shown in the Figure 3.6 graph. The graph shows the locus curve for several R_S-$(W/L)_{M0}$ combinations.
- If a reference-based bias voltage is used to supply the current source, the simple current source (Figure 3.6b) can be quite competitive in terms of process-sensitivity reduction. However, to achieve low process sensitivity a large gate voltage is needed, and to achieve temperature stability a large resistance and bias voltage are needed. The graph shows the locus curve for several R_P-V_{bias} combinations. All CMOS-based current sources show this characteristic trade-off between process noise and temperature coefficient.
- The source-degenerate current source (Figure 3.6c) achieves temperature stability at a much lower bias voltage. Adding R_S increases I_{slope} (Figure 3.2a), which allows a much lower R_P and V_{bias} to be used. This reduces process sensitivity in several ways: decreasing R_P reduces its contribution to the process noise (Figure 3.5c), and R_S decreases the MOSFET's process noise contribution (Figure 3.2d). R_S adds an additional feedback mechanism with the body effect that helps stabilize the current. The graph shows the locus curve for several R_P-V_{bias} combinations.
- R_S has a process noise contribution of 11.3%, which cannot be changed; however, a MOSFET can operate with lower process noise depending on its operating point (Figure 3.2d). If the bias voltage is large enough to favorably bias two MOSFETs, R_P can be moved to the source of a PMOS transistor as shown in Figure 3.6d. The primary difference between this current source and the supply-independent current source is the NMOS-PMOS combination. Although this adds two additional process variables (k_P and V_{TP}) reduced process sensitivity is seen. This is because on two of the four process corners the transistors oppose each other (WO and WZ) and this reduces the current change. However, in the supply-independent current source all four process corners adversely affect the current because the summing node is between two PMOS transistors. The graph shows the locus curve for several R_P-$(W/L)_{M0}$ combinations. A small ~1kΩ resistor R connects the two diode-connected FETs; its purpose is to reduce sensitivity to small power supply variations.

- The circuit in Figure 3.5e is used to validate the current-mode feedback concept. A PSPICE primitive ideal current source is used to provide a constant reference signal, which is subtracted from the feedback current supplied by mirror M0-M1. The current mirror has a current gain of N, and the PMOS transistor carries a nominal current of $2 \cdot I_D$. With a mirror gain of N=5, the process noise I_σ/I_μ drops to 3.24%, and when N=10 it drops to 2.05%. Ironically, if a perfect current source was available as a reference, it could be used to make a pretty good current source in CMOS.
- An ideal process-independent reference cannot be produced, but the circuit in Figure 3.5f with a current mirror gain of one makes a rough approximation. The results suggest that this is a good approach and the feedback (shunt-current) [12] makes it very easy to achieve a temperature-stable design. The graph shows the locus curve for several R_{SN}-$(W/L)_{M0}$ combinations. The only drawback of this circuit compared to the supply-independent current source is the need for a reference-based bias supply.

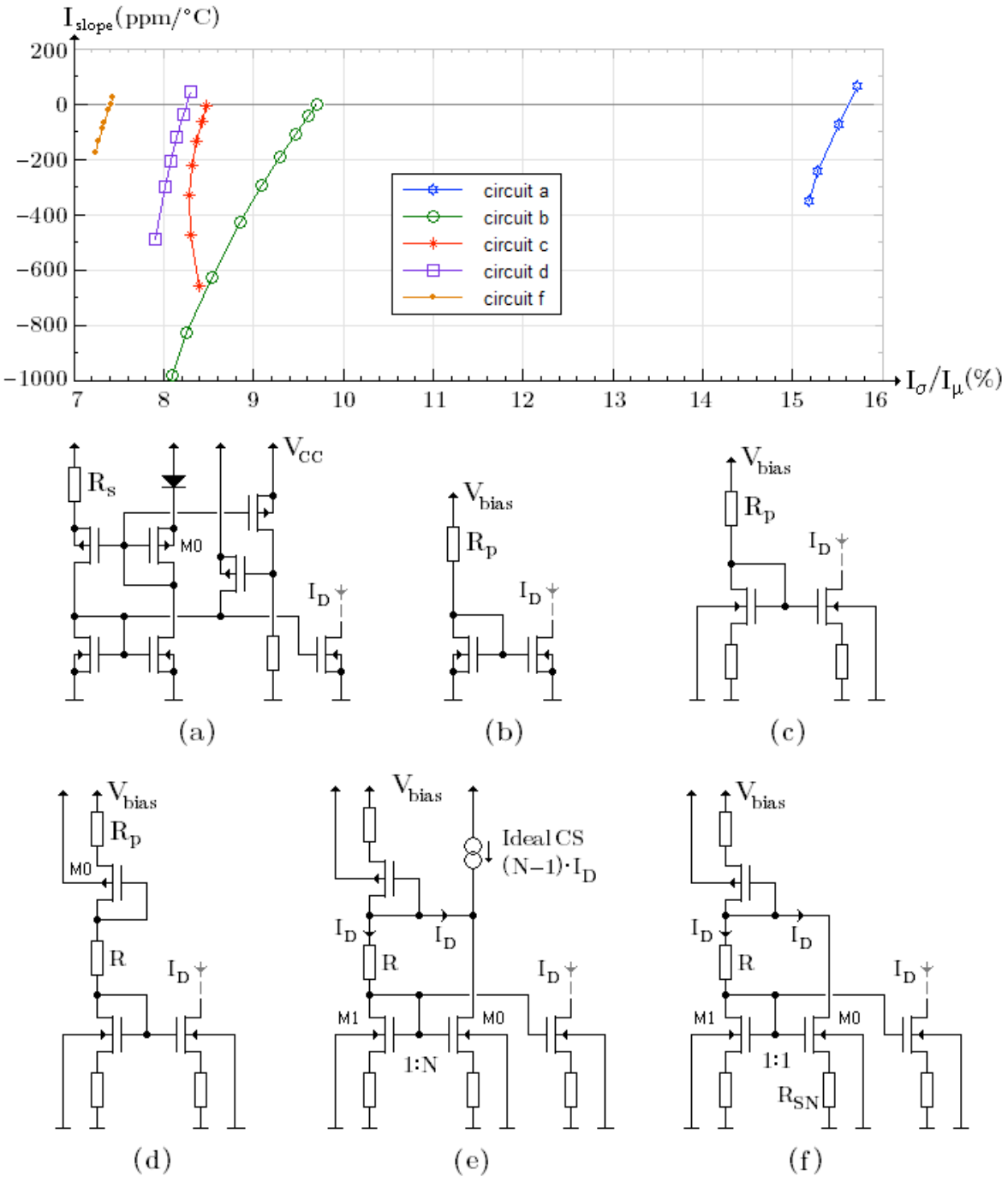

Figure 3.6. The graph shows the trade-off between temperature slope and process noise of the output current I_D. The graph is then used as a metric for comparing the sensitivities of difference current sources. The supply-independent current source (a) has high process sensitivity. If a reference-based bias voltage V_{bias} can be supplied, other circuits show much lower process sensitivity. Descriptions and justification are given in the preceding text.

The quest in state-of-the-art integrated current sources is finding suitable feedback architectures that compensate for process variations, and this work is ongoing. The consequence to controller design is that timing circuits need to be tolerant of unstable current supplies. In the next two sections, ways to minimize these errors are examined to see what can practically be achieved in terms of integrated controller performance.

It is tempting to place a precision resistor off chip and use an on-chip amplifier and reference to create a current source. This scheme is plagued with stability problems [13]. The I/O pad and external wiring add a large capacitance on the amplifier inverting node and the amplifier would need heavy compensation to ensure stability. While the possibility should not be dismissed, it is not an ideal solution and should be considered only as a last option.

3.2 Master controller

The voltage-mode master controller is basically a voltage-controlled oscillator. A simplified circuit diagram and description follows. This circuit has many potential problems as described in the following sections. Fortunately, most of the problems are resolved in the detailed design.

A current source and capacitor form a ramp generator; when the ramp voltage exceeds the Control Input voltage (Ctrl In) the comparator (CMP1) changes state and the capacitor is reset. The Ctrl In signal is supplied by the system controller and controls the length of the input period, which determines the amount of power drawn by the converter.

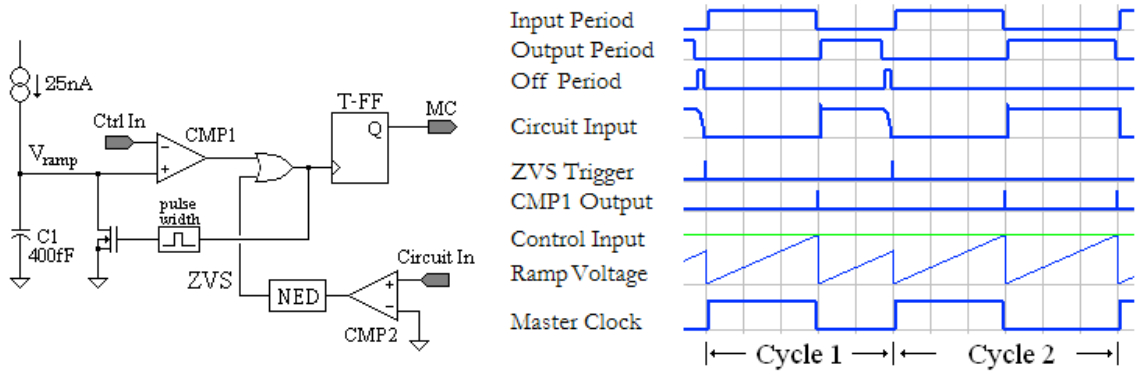

Figure 3.7. The figure shows a simplified circuit diagram for generating the master clock. The power converter generates the zero-voltage condition correctly in Cycle 1, but ZVS failed in Cycle 2.

In BCM operation the output period ends when the power inductor is demagnetized. The drain voltage of the power switch then begins to resonantly oscillate during the Off Period. The input (Circuit In) to a second comparator (CMP2) ties to the drain node of the power switch. Ideally CMP2 is triggered on either the valley or the zero-voltage crossing of the drain node oscillation cycle. A negative-edge detector (NED) circuit sees the CMP2 state-change and generates a ZVS trigger. This trigger initiates the start of the next power cycle as shown in Cycle 1 timing of Figure 3.7.

If the drain voltage minimum does not trigger CMP2 for some reason, the zero-voltage switching condition fails. In this case the ramp generator will force the start of the next power converter cycle as shown in cycle 2 of Figure 1.3. This precaution is necessary because otherwise a small system perturbation that causes a missed trigger would cause the controller to stop. However, if the ZVS-fail condition occurred because the output cycle was not finished, the forced-trigger pushes the converter into CCM. Further supervision from the system-level controller would then be needed to restore stable converter operation. The biggest challenge in BCM controller design is reducing the risk of a ZVS failure ever occurring, and creating a clean reset response in the unfortunate event that it does occur.

3.2.1 Ramp generator circuit

To increase converter dynamic range the ramp generator operates rail-to-rail. A 3.3V bias supply is used for compatibility with the digital circuit and a current reference is mirrored down to 25nA for a maximum nominal 56µs converter input period. MOSFET output impedance is very high at these low mirror currents and so a mirror cascode stage could be omitted; omitting it aids rail-to-rail operation. Large transistors were used to minimize component process mismatch errors, and the widths were selected for optimum common-centroid layout: the input transistor is split into two 10µm/4µm transistors, which straddle the 10µm/12µm output transistor. Small mirroring errors were removed by adjusting the W/L ratios. Figure 3.8 gives further details.

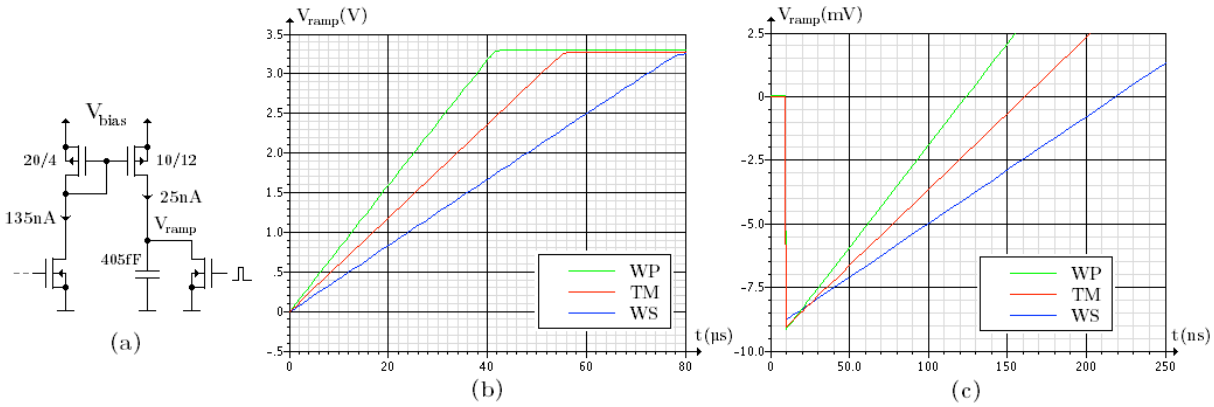

Figure 3.8. The ramp generator circuit (a). The ramp voltage is linear to the rail (b). Injection charge as the switch turns off causes a negative bias at reset (c). These timing details determine the controller dynamic range as described in the following text.

The WP process corner (CMOS, resistance, capacitance, bipolar) reduces the nominal 56µs input period to 42µs, which is primarily due to the increased current from the master current reference at WP. This process corner sets the lower limit of the *guaranteed* converter frequency range; the maximum input period of this controller can only be guaranteed to about 40µs as shown in Figure 3.8b. The voltage ramp is linear to the rail for every process variation. The low current, wide input transistor, and high PMOS threshold voltage (580-780mV) keep the output transistor in saturation to within about 50mV of the positive rail.

The upper limit of the converter frequency range is determined by the reset timing. As shown in Figure 3.8c, the reset switch dumps an injection charge on the capacitor, pushing the ramp voltage negative and taking up to 220ns to clear the injected charge. The injection charge could be reduced or eliminated with an injection-charge cancelling circuit, but this would create a potentially fatal error. At maximum frequency the circuit operates on or near the negative rail; comparators with input hysteresis can latch if operated too close to the rails and the injection charge helps prevent the latch condition from happening. The details are described in Figure 3.9.

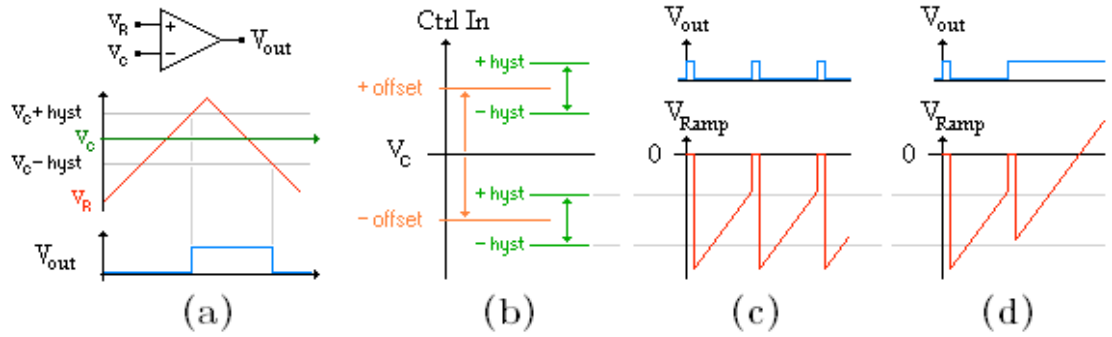

Figure 3.9. The comparator output goes high when the non-inverting input (V_R) crosses the V_C + hysteresis threshold; the comparator output will remain latched high until the V_C – hysteresis threshold is crossed (a). The input hysteresis is superimposed on an input offset error that is caused by component mismatches. The input offset can vary anywhere between some negative and positive limits depending on process variations (b). Assuming a control input of zero *and* a worst-case process variation with the input offset at the negative limit, the entire voltage ramp is below ground. The injection charge on the capacitor needs to push the ramp voltage below the comparator negative hysteresis threshold in order to reset the comparator output (c). If the ramp voltage fails to cross the hysteresis threshold, the comparator stays latched high creating a fatal error (d).

The seriousness of the comparator latching at the ground rail cannot be overstated. If the latch-state fails to reset the master clock flip-flop, the converter will remain on, drawing increasingly more power. The latch-state error could be resolved by *increasing* the control voltage; however, the system-level controller seeing the increasing input current will attempt to correct the error by adjusting the control voltage *down*. If the system controller includes an over-current protection circuit, a reset would be triggered. Otherwise, the current would increase until the inductor saturates and the coil windings fry.

The design must insure that capacitor voltage crosses the comparator negative hysteresis threshold on every reset. However, in calculating the absolute maximum controller frequency that can be guaranteed, the worst-case timing would be the WS ramp rate making a transition through the combined hysteresis and input offset windows plus a safety-margin on the capacitor voltage to assure the threshold is crossed. The input offset and hysteresis of the comparator play a critical role in determining the maximum controller frequency.

3.2.2 Rail-to-rail comparator

The most important comparator requirement is that it operates rail-to-rail. Low input offset is also critical so that the upper-frequency target is reached, and a fast output transition is needed for compatibility with the digital circuit. The comparator shown in Figure 3.10a is able to operate at input voltages up to the positive rail; however, for common-mode input voltages below about 580mV the NMOS current source cuts off, the comparator current drops to zero and the comparator stops working. The comparator shown in Figure 3.10b operates down to the negative rail; but for common-mode voltages above about 2.4V the PMOS current source cuts off and the comparator stops working. However, if the two circuits were combined, then at least one of the input differential pairs would be operational at any common-mode input voltage. The resulting circuit shown in Figure 3.10c achieves rail-to-rail operation.

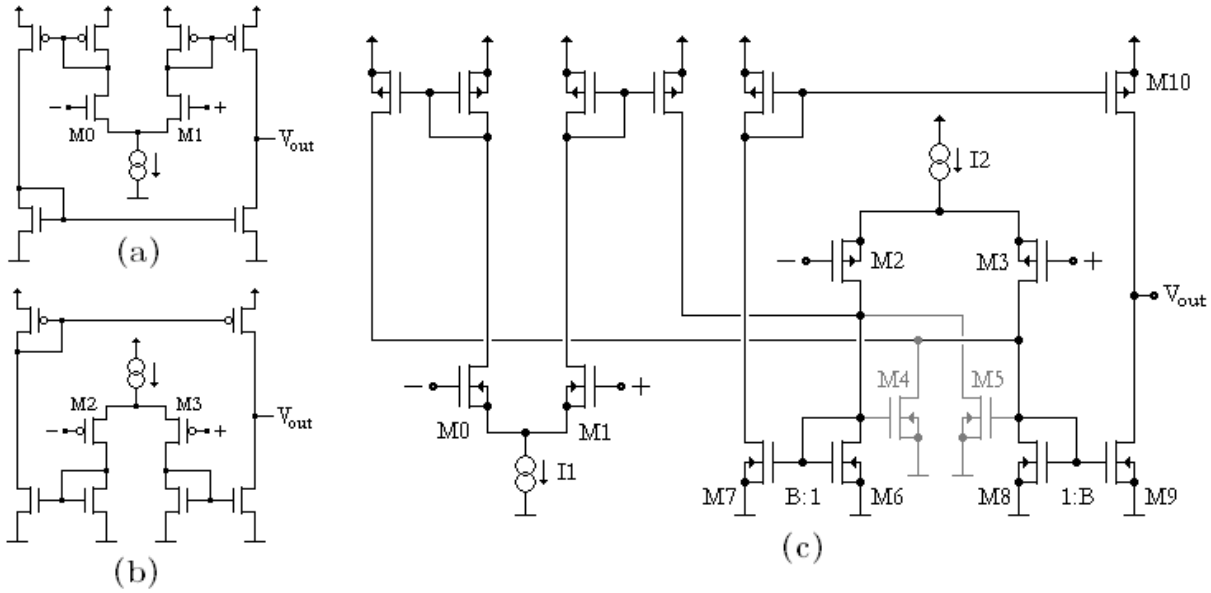

Figure 3.10. A comparator with an NMOS input differential pair will operate at common-mode voltages up to the positive rail; but the circuit fails to operate at low input voltages because the current source cuts off (a). Similarly a comparator with a PMOS input differential pair will operate to the negative rail, but fails to operate at input voltages near the positive rail (b). When the two circuits are combined, rail-to-rail comparator operation is achieved (c). Transistors M4 and M5 add positive feedback, which gives the input hysteresis.

The ramp generator current source (Figure 3.8a) operates to the positive rail because of the very low ramp current. However, to achieve fast output switching the comparator uses a much larger current (about 10μA) and so the current sources cannot be driven to their respective rails. Different comparator architectures are available other than the one in Figure 3.10; but whatever architecture is used, it will likely require both NMOS and PMOS differential pairs in order to achieve rail-to-rail operation [14].

Various comparator designs have been used to reduce or eliminate the input offset. A successful approach stores the amplifier input offset on a capacitor, and then subtracts the offset from the input signal [15]; the slave controller design in the next section uses this approach. However offset mitigation can interfere with a hysteresis circuit, and as will be discussed the master controller needs the hysteresis circuit. Other methods are available to deal with the comparator offsets, and as shown in the last section of this chapter, another approach can be used to increase the controller dynamic range.

The offset error is caused by differential pair and current mirror process variations and mismatches. Both differential pairs (NMOS and PMOS) contribute to the input offset; but only the PMOS pair affects the high frequency timing. The error is reduced through layout and component size; the standard deviation of input offset (σV_{offset}) decreases with the square root of the differential pair transistor area, as shown in Table 3.3.

PMOS DP Area	C_{SG}	σV_{offset}	Ramp risetime
15μm^2 (15x1μm)	60fF	3.73mV	54.8μs
30μm^2 (30x1μm)	120fF	2.63mV	56.7μs
60μm^2 (80x0.75μm)	240fF	1.86mV	60.8μs
90μm^2 (120x0.75μm)	360fF	1.51mV	64.8μs

Table 3.3. To reduce the input offset-voltage error, the area of the differential pair transistors is increased. The source-to-gate capacitance increases with area, but this has only a small effect on the ramp slope.

Increasing the PMOS differential pair gate capacitance has almost no effect on the ramp risetime because the M2/M3 source voltage tracks the non-inverting input; the source-to-gate voltage is approximately constant up to the positive rail. From the table, an 89% increase in gate capacitance increases the ramp rate by only 18%. The following comparator design observations are made:

- Two factors determine the output switching speed. The non-dominant factor is the slew rate. When the comparator drives a single minimum-size inverter the total load capacitance is less than 10fF including the line capacitance. With a 10µA output current and 3V output swing, the total rise time is less than 3ns (slew rate = current / capacitance). This would be the output risetime if the input was overdriven, however the slow input ramp rate means only the falling edge will be slew-rate limited.
- The dominant factor in switching speed is the slow input ramp rate and low amplifier gain. With an input ramp rate of 40mV/µs, if the comparator gain is 2000 the output risetime would be 38ns. The slow comparator output holds the digital inverter in the linear region long enough to decrease the bias voltage and affect the ramp timing and other circuits. The comparator gain is an important factor in reducing the supply current in this inverter as the comparator switches.
- The comparator can be thought of as a transconductance amplifier with a "gain" of $g_{m2/3}$, followed by a transimpedance amplifier with gain of $B \cdot r_{out}$, where r_{out} is the impedance looking into the output node ($r_{out} = r_{o8} || r_{o9}$) and B is the mirror gain. The comparator has differential voltage gain $A_v = g_{m2/3} \cdot B \cdot r_{out}$.
- $g_{m2/3}$ is increased by increasing W/L or by increasing I_2: $g_m = \text{sqrt}(2 \cdot I_D \cdot k_p \cdot W/L)$. Increasing the current improves the output slew rate, but it also decreases the comparator gain because r_{out} decreases with current ($r_{out} = 1 / \lambda \cdot I_D$). Increasing $(W/L)_{M2/M3}$ is the only practical way to increase the gain of the transconductance stage.
- The gain of the transimpedance stage is set entirely by M6 and M8. Adjusting the NMOS mirror gain B with the W/L ratio of M7/M9 will change the output current but not the voltage gain. This is clarified in Equation 33; increasing $(W/L)_{M9}$ increases $I_{D,o9}$ by the same factor, resulting in no gain change.
- r_{out} is increased by decreasing W/L for M6 and M8. This decreases $g_{m6/8}$ causing a larger gate voltage swing ($\Delta V_{GS8} = \Delta I_{D8} / g_{m8}$) and therefore higher gain. The limit in reducing $(W/L)_{M6/M8}$ is that the PMOS differential pair should remain in saturation down to the negative rail at the WZ process corner.

$$A_V = \frac{\Delta V_{out}}{\Delta V_{GS9}} = k_n \cdot r_{o9} \cdot \left(\frac{W}{L}\right)_9 \cdot \left(V_{GS8} - V_{TN}\right) = k_n \cdot \frac{1}{\lambda \cdot I_D} \cdot \left(\frac{W}{L}\right)_9 \cdot \left(V_{GS8} - V_{TN}\right) \tag{33}$$

B	$(W/L)_{M8}$	$(W/L)_{M9}$	A_V (V/V)	$I_{D,M9\ peak}$ (µA)	r_{o9} (MΩ)
0.5	4/2 µm	2/2 µm	435	2.5	34.9
1	4/2 µm	4/2 µm	435	5.0	17.9
2	4/2 µm	8/2 µm	435	10.0	8.9
1	4/2 µm	4/2 µm	435	5.0	17.9
2	2/2 µm	4/2 µm	519	10.0	10.8
4	2/4 µm	4/2 µm	652	20.0	7.1

Table 3.4. The current mirror gain (B) increases the output current. However, the voltage gain is only affected by the input-side of the current mirror $(W/L)_{M8}$. Note: only the PMOS current mirror was active, $I_2 = 10\mu A$.

Simply increasing $g_{m2/3}$ and decreasing $g_{m6/8}$ does not provide sufficient comparator gain for a truly digital-compatible output. Increased gain and a way to deal with the switching currents and noise are needed. The hysteresis circuit (M4/M5) provides feedback that can significantly increase comparator gain, so additional gain stages may not be necessary. The final design must guarantee that the master clock is not double-triggered under any input, power supply, or switching noise condition for all process and temperature variations.

Hysteresis increases the comparator gain but it also increases the delay overhead at reset. How much hysteresis is actually needed? The kT/C noise on the 405fF ramp capacitor is $100\mu V_{rms}$ with a simulated peak-to-peak variation of 380µV over a 5µs period.[1] The comparator itself has an input noise of $270\mu V_{pp}$[2] over 5µs. Switching noise occurs after the threshold crossing, so a hysteresis of +/-1.5mV should be sufficient.

[1]Transient noise analysis is used because the capacitive load gives zero current in AC analysis. The ramp slope is removed from the simulation result, and a standard deviation is made on the flattened slope.

[2] Transient noise analysis was used with an input ramp rate of 40mV/µs. A standard deviation of the switching time was made and the input noise is interpolated from that result.

For a hysteresis of +/-1.5mV at the WP process corner, the TM hysteresis was set at +/-2.2mV, which increased the nominal gain by a factor of four to 1756(V/V). This gain is satisfactory; however at input voltages near the negative rail the NMOS current mirror (M8) can push the PMOS differential pair (M3) into triode. At the WZ process corner the minimum PMOS threshold voltage (580mV) and the maximum NMOS threshold voltage (560mV) are seen. To keep M3 in saturation at the negative rail and WZ process corner would require limiting the M8 on-voltage V_{ON8} to 20mV as shown in Figure 3.11a.

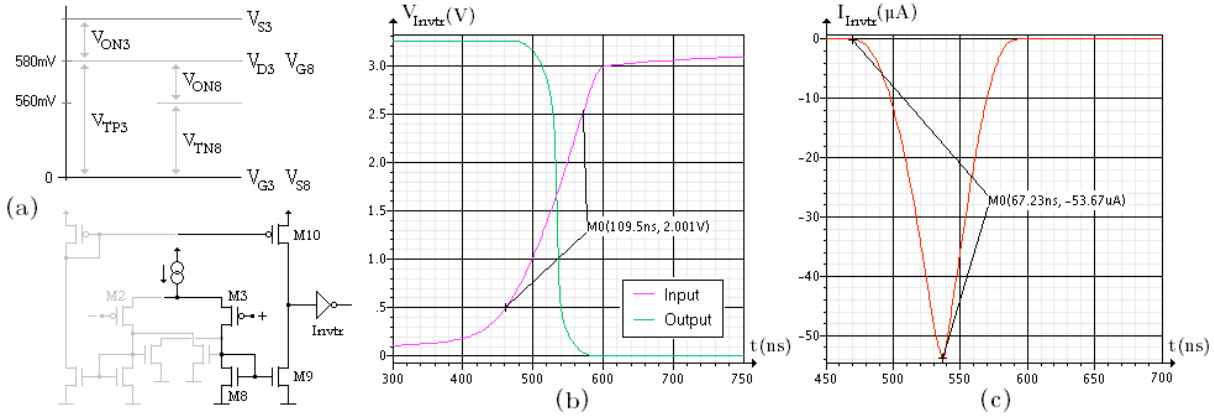

Figure 3.11. A problem is encountered at the negative rail on the WZ process corner. If the "on voltage" of M8 is greater than 20mV, the current mirror will force differential pair transistor M3 into triode (a). This causes a large comparator output risetime seen at the inverter input (b), which causes a wide current pulse on the supply as the inverter switches (c).

Limiting V_{ON8} to 20mV would mean increasing $(W/L)_{M8}$ resulting in a large g_{m8} and reduced amplifier gain. The gain is optimized by increasing g_{m8} slightly, allowing some incursion into the weak triode region, and using the hysteresis gain as the workhorse for switching. Figure 3.11b shows a comparator output risetime of 110ns (2V) for the worst-case input ramp rate of 40mV/µs when the input voltage is zero for a chip produced at WZ. In worst-case operation the comparator gain decreases to 454(V/V) causing a wide power supply current pulse drawn by the inverter (Figure 3.11c).

The current drawn by the inverter would cause serious interference if the inverter and ramp circuit were supplied from the same bias source. But when the digital gates are placed on a separate supply the switching currents are not a problem. The peak current density and average power dissipation in the inverter are well below the limits set by the technology, and AC current peaks from switching are 30 times below the threshold where electro-migration occurs. At 2MHz the inverter dissipates 36µW; if the entire chip was covered with identical inverters the power dissipation would be an unacceptable 92W/cm^2. But the high thermal conductivity of the doped silicon easily dissipates the 36µW of a single inverter. Although not ideal, the worst-case results at the negative rail are acceptable.

The problem is far worse at the positive rail where the NMOS differential pair is always in triode. The larger PMOS threshold voltage and smaller NMOS threshold voltage means that the NMOS differential pair (M0/M1) will always be in triode for all conditions at the positive rail. The worst-case is the WO process corner where the common-mode input must be below 2.88V – $V_{ON,P\text{-}mirror}$ in order for M0/M1 to be in saturation. For an input of 3.2V the gain drops to 155(V/V) at the CMOS-WO/resistance-WS process corner. However a design trick can be used to increase the gain to acceptable levels for operation at the positive rail.

For an input ramp rate of 40mV/µs hysteresis adds a delay of 25ns/mV. At the negative rail the hysteresis was limited to +/-2.2mV to minimize the delay (of 110ns) at reset. However, operation near the positive rail controls the low frequency range of the converter where large hysteresis delays are easily tolerated. Increasing hysteresis in the low frequency range would increase the gain and compensate for the lower gain caused by the NMOS differential pair operating in triode.

This is easily done by setting $I_1 << I_2$ (Figure 3.10c). At mid-range input voltages, the current through M4/5-M6/8 is $I_1 + I_2$. As the input voltage increases and the PMOS differential pair cuts off, this current drops to just I_1, which shifts the PMOS/NMOS load lines lower and increases the gain (Figure 3.12a). Thus the common-mode input voltage (and therefore operating frequency) creates a gain change in the hysteresis circuit.

In design, I_2 was set to 10µA and the hysteresis for a negative rail input is set to +/-2.2mV using $(W/L)_{M4/M5}$. Decreasing I_1 (to1µA) also decreases $g_{m0/1}$, but this does not matter because M0/M1 are in triode anyway and thus have lower gain. As the input common-mode voltage increases and M2/M3 begin to cut off, a rapid increase in the hysteresis voltage is seen. As M0/M1 move deeper into triode operation and their gain drops the hysteresis circuit gain increases and compensates for the loss allowing rail-to-rail operation. Decreasing the current by 10x increases the gain of the hysteresis circuit by 3.2 (√10x). Table 3.5 gives more details.

V_{in}	M0/M1	M2/M3	Corner	$V_{hysteresis}$	Risetime	Gain	Frequency	$P_{inverter}$
0V	Cut off	Weak triode	WZ/WP	±2.4mV	110ns	454V/V	2MHz	35.6µW
0V	Cut off	Saturation	TM/TM	±2.2mV	30ns	1667V/V	2MHz	10.7µW
1.6V	Saturation	Saturation	TM/TM	±2.2mV	28ns	1756V/V	36kHz	0.19µW
3.2V	Deep triode	Cut off	WO/WS	±35mV	83ns	600V/V	24kHz	0.28µW

Table 3.5. At different input voltages the differential pair transistors may be cut off, saturated, or in the triode region. As the PMOS transistors M2/M3 cut off, the hysteresis circuit is designed so that its gain increases, providing additional assistance with switching. At the negative rail M2/M3 operate in weak triode (WZ/WP) and the gain could be increased by decreasing I_2. But by sacrificing some gain at the negative rail, the gain at the positive rail is significantly boosted despite M0/M1 operating deep in the triode region.[3] The listed frequency is the rate at which the comparator switches, which is twice the converter frequency at 50% duty cycle. The risetime, current peak (not shown), and switching frequency determine the power dissipation in the inverter driven by the comparator.

Typically comparator gain is increased using a cascode output stage [16]. The problem is the cascode stage has the same triode problems at the rails for certain process corners that the differential pairs have. The two cascode transistors require additional bias circuits which are affected by process, making it difficult to keep M9/M10 in saturation for all process corners. In all cases the cascode stage does improve the gain (for instance at WO/WP the gain increased by 2.0), but it also lengthens the switching tails during which supply current is drawn. The net result is that the cascode output causes a small decrease in inverter current at the cost of a larger increase in bias and switching currents in the comparator output stage. A better way to deal with the slow comparator output risetime is to let the digital circuit handle it; this is discussed in detail in the next section.

The most critical detail of this design is preventing the comparator from latching at the input rails. The voltage on the ramp capacitor after reset must always be less than the maximum negative offset voltage at the input of the comparator. The input offset error is affected by both process variations and component mismatches and so the lowest possible input offset voltage that might be seen cannot therefore be determined exactly. A large reset injection charge could create the needed design safety margin, but a larger than necessary margin reduces the maximum converter frequency and guaranteed dynamic range.

To estimate the worst-case input offset error a negative-slope test ramp is applied in simulation and the output switching times are observed. Figure 3.12b illustrates a very bad way to determine the maximum offset. In theory, a Monte Carlo simulation of 100 runs should find the 6σ standard deviation limits. From this the apparent maximum offset of -6.14mV is found. After adding a 25% safety margin, the nominal ramp reset voltage is set at -8mV and a Monte Carlo simulation of the full controller shows no latching errors in 100 runs (Figure 3.12c). However this result misleading; further Monte Carlo simulations show that a wafer produced near the WZ process corner will see a 28% chip failure rate when the controller is operated at the negative rail. Chips from that wafer should essentially be scrapped.

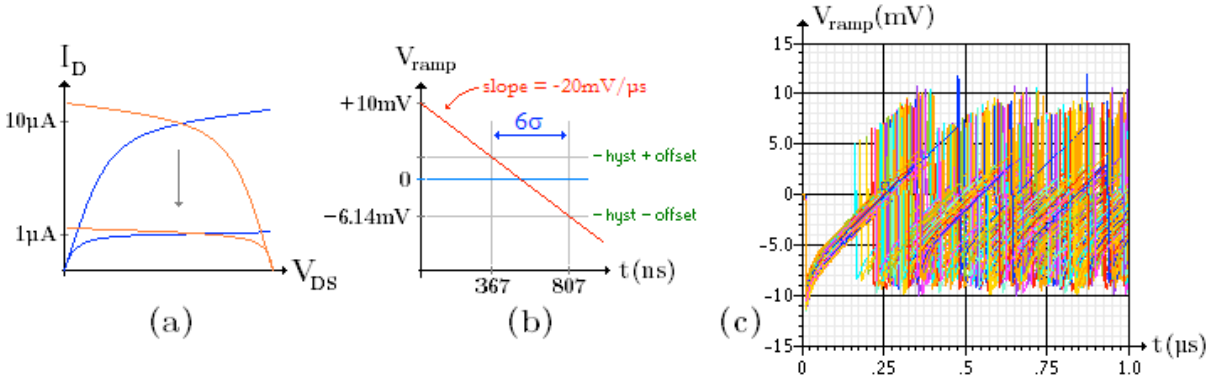

Figure 3.12. As the input voltage increases and the PMOS differential pair cuts off, the current in the hysteresis circuit decreases, shifting the MOSFET load lines down, which increases the hysteresis circuit gain (a). With the comparator reference input grounded, a test ramp is applied to the non-inverting input and the output switching times are recorded for a Monte Carlo simulation of 100 runs (~6σ). From this an apparent worst-case hysteresis minus input-offset of -6.14mV is found (b). The ramp circuit reset voltage is set to -8mV (25% margin on the worst-case input offset) and a Monte Carlo simulation of the full controller is then made. The results show no latching errors on 100 runs (c). However, these results should not be trusted; the problem is discussed in the text.

[3] Setting I_1 to only 1µA does affect the falling-edge slew rate at high input voltages, but the overdrive voltage fully compensates and a faster output slew rate is seen at the positive rail than is seen at the negative rail.

The problem with this approach is that process variations and component mismatches contribute about equally to the input offset error. In this case there is no way that a Monte Carlo simulation of only 100 runs can give a good estimation of this offset error. Both WS and WZ process corners produce larger worst-case input offsets compared with TM. The Monte Carlo simulation should then be run from the WZ and WS process corners to capture mismatch errors at the maximum input offset. (In other words, the 6σ limit for mismatch errors needs to be found from the 6σ limit for process errors.) These simulations show that the reset voltage should be set below -15.5mV to guarantee a latch-free design at the negative rail.

Setting the reset voltage to -15.5mV is easily done; however doing so limits the guaranteed dynamic range to only about 50 when all process corners and mismatch errors are included. Although the nominal controller dynamic range is an acceptable 200, the guaranteed range of only 50 is not, so another design trick is needed. The large reset voltage is used to prevent the comparator from latching at the negative rail. Once the comparator hysteresis threshold is crossed, and the comparator resets, the large reset voltage is no longer needed. If a *delayed* charge cancellation was implemented the comparator would properly reset and *then* the unwanted voltage could be removed. Figure 3.13 shows the circuit and timing.

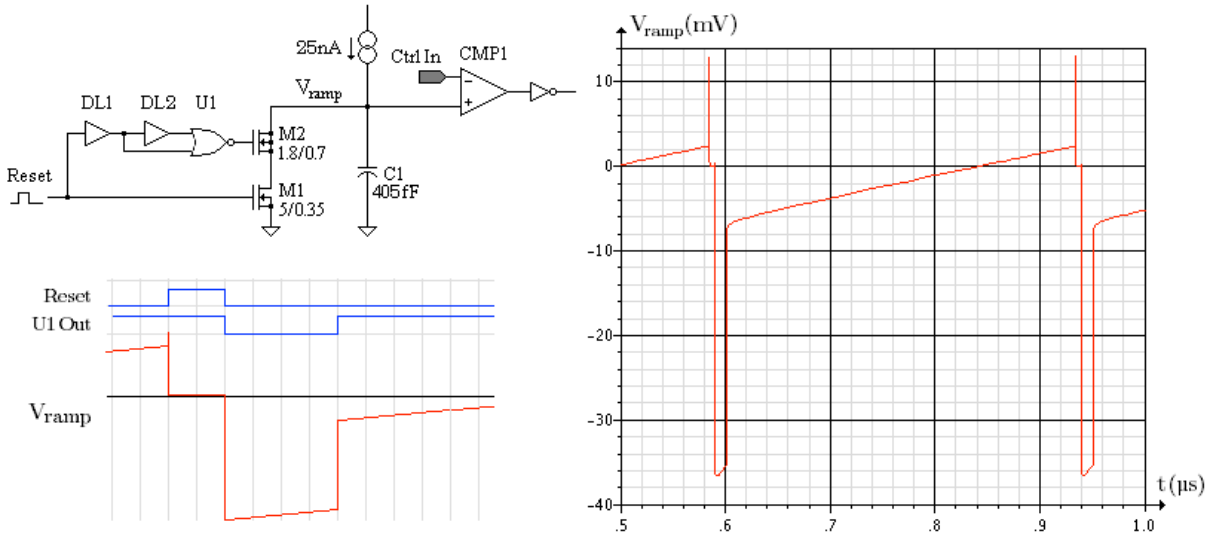

Figure 3.13. A 4ns wide pulse is supplied to the reset switch M1; the gate capacitance of M2 is used for injection charge cancellation. Delay line DL1 delays the reset pulse by 4ns, and DL2 and U1 increase its width to 8ns. The reset pulse and U1 switch low at the same time, dumping a large injection charge on the capacitor. The large negative voltage helps the comparator reset, and after 8ns most of the charge is removed.

Without charge cancellation a 28% failure rate was seen on the WZ process corner when a -8mV reset voltage is used; the reset voltage needed to be increased to -15.5mV to fix the problem, reducing the guaranteed dynamic range to only 50. With change cancellation, the reset voltage can be reduced to less than -4mV before the first latching failure is seen. At -8mV no failures are seen at WZ, and the guaranteed dynamic range is 90.

High controller dynamic range is important for two reasons: it reduces the power loss in standby operation (reduces the vampire load), and it increases controller portability to different designs (universal controller). Ideally a controller would have a guaranteed dynamic range of 300 or more. While this may be beyond what most magnetic cores can support (coercivity to saturation), it allows the same controller to be used in converters with widely different system requirements.

To address the first issue, designers developed phase shedding: as the power increases, more phases are added by the controller. N phases can increase the dynamic range by up to a factor of N. The idea works well provided that crossover issues are resolved [17]. In power converters, the high-frequency switching range controls the low-power output range. Dropping all but the master phase reduces the switching losses in standby mode, which dominate the low-power losses. Phase shedding could be controlled from this level (sub-controller) by disabling the slave phases when the input control voltage drops below a threshold. However for better portability phase shedding should be controlled from the system level where the converter requirements are known.

In large-scale production the nominal values are not important; if the guaranteed range does not meet the system requirements, or if process corner failures are allowed to occur, then expensive testing will be needed, or worse “consumer testing” will occur. To make this controller more universal further improvements are needed. In the last section of this chapter another trick is discussed that more than doubles the guaranteed range of 90 seen so far.

3.2.3 Ramp reset timing

The master controller has several potential timing-related problems: the slow comparator output risetime can cause multiple-triggers or metastability [18] of the master clock; if the reset pulse is too short the ramp voltage will not be fully reset; a ZVS failure forces a trigger, which then causes a new ZVS signal that retriggers the master clock. The design must guarantee that these errors never occur.

The digital gates switch in about 250ps, while the comparator output risetime can be 100ns or more. As the comparator output rises to the digital trigger level, noise could toggle the logic gates and leave the master clock in a random state (metastable). For the power converter this would be catastrophic; fortunately there are some good tools available to prevent this error from ever occurring:

- The comparator has input hysteresis to prevent interference from noise in the ramp circuit. Hysteresis can also be added to the inverter driven by the comparator (U1). A Schmitt-trigger input can tolerate the slow comparator output risetime and give the inverter hundreds of millivolts of input hysteresis.
- If system noise did trigger Schmitt-trigger inverter U1, a delay line following the inverter (DL1) will block narrow digital pulses. The AMS 4ns delay line is a series of eight weak inverters that act like high-gain low pass filters. The delay line has over 100dB of noise rejection to AC signals (the DC-coupled amplifiers quickly saturate at any frequency), and the delay line cannot respond to digital input pulses with a width below about 1.8ns.
- The delay line cannot pipeline more than one pulse at a time. If the narrowest (1.8ns) noise-generated pulse did occur, DL1 would have to return to its ground state (in this case a logic 1), and a 4ns recovery period would be enforced before it could be retriggered (5.8ns total time).
- If DL1 was triggered, a narrow output pulse would be produced. This narrow pulse would trigger the master clock, but the ramp reset would be incomplete. To ensure a full reset cycle, DL1 and DL2 form a pulse-width conditioning pipeline that guarantees a reset pulse width of 4ns. Pulses from DL1 less than 4ns wide are disabled by U2. Together U1-U3 form a rising edge-triggered circuit that generates a conditioned reset pulse, and has a robust rejection response to system noise.

For a single digital pulse, DL1 looks like a low-pass brick wall filter with a cutoff frequency around 170MHz (1/5.8ns); U2 and U3 decrease the cutoff frequency to around 125MHz (1/8ns delay from DL1 and DL2). Only noise occurring during the CMP1's output fall time has the potential to generate a double-trigger. To noise, the reset period looks like a high-pass filter where only noise with frequency components above the reciprocal of CMP1's output fall time can trigger U1. If the output fall time through U1's hysteresis window is less than 8ns, the cutoff frequency of the highpass filter is greater than 125MHz and a bandstop filter is formed.

In this case, a noise pulse generated within the fall-time window could not cause a double trigger because the pulse width would be less than 4ns, and such narrow pulses are blocked by U2-U3. Since the comparator output falling edge is slew rate limited, the falltime is less than 8ns and the design guarantees that double triggers are prevented. Figure 3.14 shows the blocking of a noise pulse that occurred on the comparator rising edge.

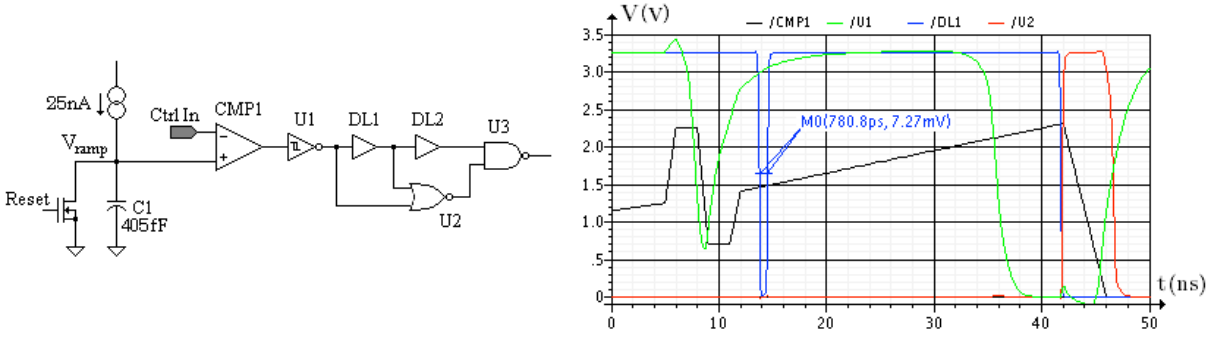

Figure 3.14. This theoretical example demonstrates the robustness of the design. As the comparator output rises toward the U1 trigger level, large switching currents occurred somewhere in the system. This causes a large transient spike that triggers U1. Supply ringing crosses both U1 hysteresis thresholds, creating a narrow (780ps) output pulse on DL1. If allowed, the narrow pulse would create an incomplete reset cycle and the ramp voltage would not start from zero. U2 creates an enable signal that only allows pulses wider than 4ns (DL1 delay time) to pass. The delay lines, U2 and U3 form a pulse-width conditioning circuit that guarantees a reset pulse width of 4ns, and blocks noise-generated pulses that are less than 4ns wide.

Metastability occurs in flip-flops when the data input is unstable during the clock edge. In the case of a toggle flip-flop (T-FF, Figure 3.15) data line routing is internal and only a clock is supplied. If a clock edge like the U1 output at 8ns (Figure 3.14) is seen, it could cause metastability and the master clock state would be unknown.

However, incomplete comparator output signals are blocked by the logic gates and U3 always has a clean digital output. The pulse width conditioning circuit guarantees that metastability on the master clock cannot occur.

The low ramp circuit noise and comparator input hysteresis virtually guarantee that a noise pulse from the ramp circuit will never be seen. However, large switching current peaks and an extremely poor comparator power supply rejection ratio (a gain peak of 2.3x is seen at 43MHz) makes noise pulses from the power supply a serious concern. As just discussed, the digital circuit can handle pretty much anything given to it; but placing the comparator on the analog bias supply and the digital gates on a separate supply makes it unlikely that power supply noise will ever trigger U1.

U1 can then be thought of as the second comparator gain stage, giving it high gain and decent power supply rejection (provided separate bias supplies are used). This comparator architecture has three output options (cascode output, MOS amplifier with current source load, or Schmitt-trigger inverter gain stage). The weak cascode output stage gain on some process corners makes it difficult to compensate against power supply noise (compensation decreases gain), and long switching current tails are seen. A better choice for this application is the MOS amplifier gain stage; the high gain makes compensation possible, giving it high power supply rejection. However the comparator should be on the same bias as the ramp circuit to prevent supply noise from coupling into the ramp circuit through the gate capacitance of comparator transistors M1/M3. Consequently the MOS amplifier option has two output stages drawing switching current from the analog bias supply. The advantage of the Schmitt-trigger inverter output option is that the switching current for one of the output stages is moved to the digital supply. The Schmitt-trigger hysteresis increases inverter gain, significantly reducing the switching-current profile, which allows some comparator compensation. The sensitive comparator operates with a protected bias, while the Schmitt-trigger inverter (with high noise immunity) operates with the supply where switching currents are seen. In either case (MOS or inverter output stage) a noise-triggered switching error will *probably* never occur; but the digital pulse width conditioning circuit *guarantees* that these errors cannot occur.

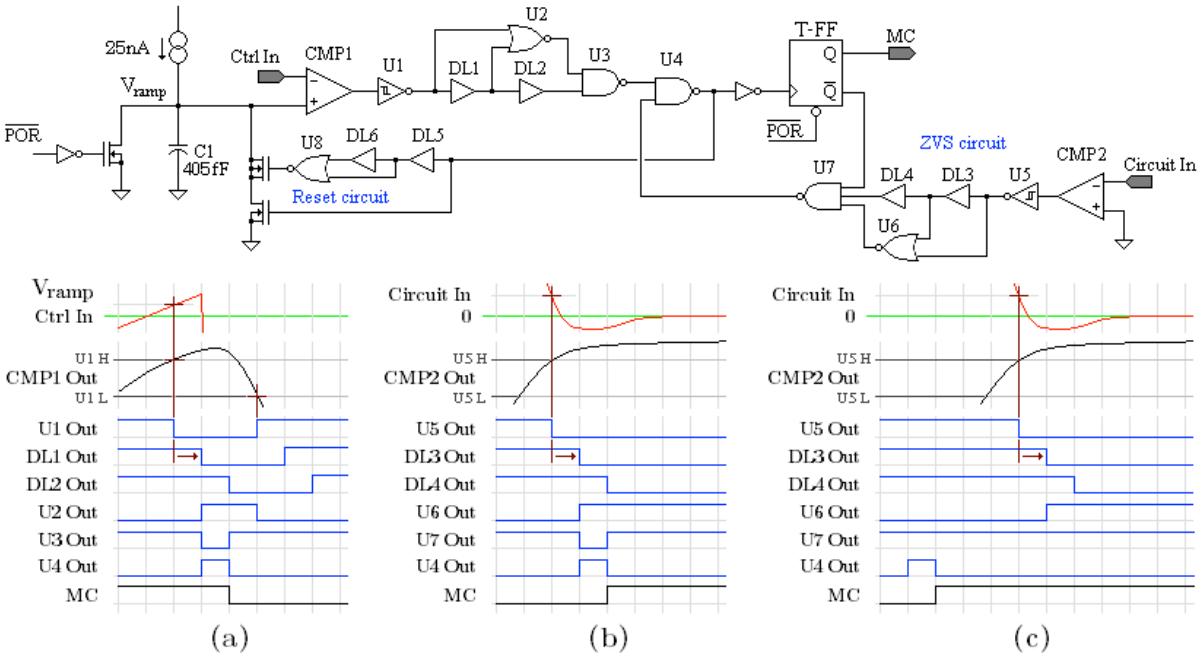

Figure 3.15. The detailed master controller circuit is shown schematically. The timing diagrams show the clock signals for the end of the converter input period (a), the end of the converter output period (b), and the forced trigger if a ZVS failure occurs (c). In the event that a ZVS failure occurs, the ramp generator forces a trigger on the master clock with the timing cycle similar to what is shown in (a). However in the ZVS failure case, the master clock goes high, which causes a zero-voltage condition in the converter. The feedback of Q_not to U7 then prevents a second trigger from occurring as shown in (c).

The ZVS comparator CMP2 is given a small positive reference bias to ensure the comparator always recognizes the zero-volt input condition. While CMP1 operates rail-to-rail, CMP2 must tolerate “over-the-rail” inputs. The ZVS input signal ties to the drain node of the converter power switch. The drain node can reach 30V or more in most power converters. To protect the comparator input transistor, a 20V gate was used for ESD protection and the input is clamped using Schottky diodes in the IO pad. The diodes clamp to ground and a heavily decoupled input supply voltage. A series resistor is then needed to limit input current and to prevent the drain node voltage from being clamped to the input supply.

3.3 Slave controller

Multiphase switch-mode converters were developed to improve efficiency and reduce ripple. The idea is to extend the input and output periods so that current flow is more evenly distributed. This reduces the requirements on expensive and bulky filtering and decoupling components, and it reduces the power peaks seen at the supplies. Reducing power peaks reduces the ESR losses and thus efficiency improves.

To be effective the phases must be phase-locked; otherwise asynchronously clocked phases in a two-phase system would randomly double the peak current drawn from the source (in a three-phase system the current would triple, etc.), creating large input and output ripples. In the sub-controller (this controller), loss of phase lock is considered instability, and it can cause controller instability at the system-level. In this case the system-level controller would see power increasing and decreasing randomly and independent of the conditions seen at the source and load. As described in Section 2.4, a slave controller referenced to the master clock falling edge is theoretically stable in voltage-mode control for duty-cycles greater than 50%. However, the level to which stability can be guaranteed depends on the accuracy and tracking speed of the phase-lock delay circuit.

3.3.1 Phase-lock ½ cycle delay tracking circuit

The controller sets the power in the converter by adjusting the clock frequency. The ratio of the converter maximum output power to standby power is the converter dynamic range; for a maximum range of 100, the master clock varies by the same factor: 100. Not only must the slave controller track the master clock with the same frequency over the dynamic range, it must also maintain the proper phase delay so that large current peaks are not seen. Because the period of the master clock is not known in advance, each cycle must be timed and a synchronization pulse generated on the next cycle.

For a two-phase controller, the slave clock (SC) tracks the master clock as shown in Figure 3.16. Referenced to the falling edges of the master clock, the slave clock resets one-half cycle later at the center of the master clock cycle. Calculating the time when the slave reset should occur could be done by charging a capacitor during the master clock cycle #1 (ramp increasing), then discharging it at twice the rate during cycle #2 (ramp decreasing). This scheme gives a phase-lock with a one-half cycle delay. Since each cycle must be measured, the phase-lock delay circuit needs two timing ramps as shown in the figure.

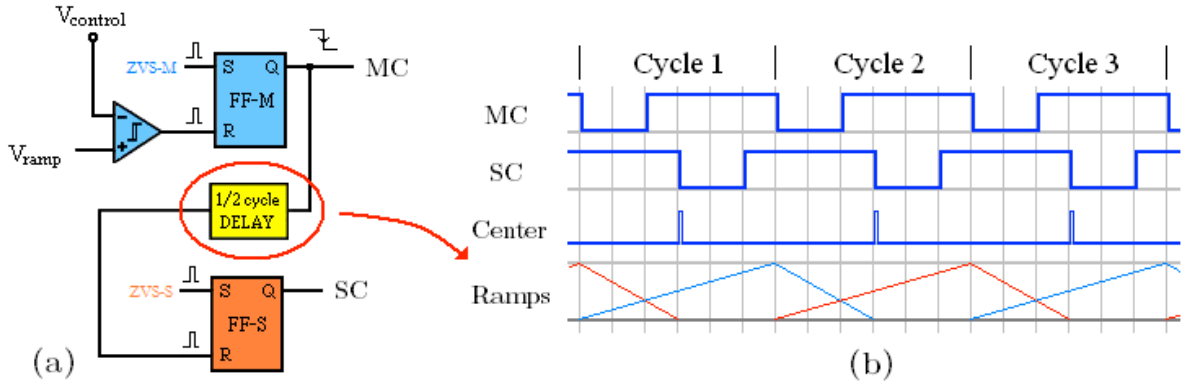

Figure 3.16. From Figure 2.6b (derived from [19]), for a two-phase system the slave clock is delayed by a half-cycle from the master clock (a). Since the master clock frequency varies by a factor of 100 or more, the half-cycle delay must be derived from the master clock on a cycle-by-cycle basis. One possible scheme to derive the delay is to charge a ramp capacitor on one master clock cycle, and then discharge the capacitor at twice the rate on the next cycle –giving a half-cycle delay. Two such ramps are needed for continuous operation (b). The slave clock is reset when the ramp crosses zero, phase-locking the slave to the master clock center.

In ZVS operation the controller resets the clocks and the external circuit sets them again after the respective output periods are complete and the zero-voltage condition (ZVS signal) is seen. The input period of the master is controlled by an input control voltage, but the input period of the slave controller is tracked from the master clock. Tracking occurs by virtue of the fact that the output period is proportional to the input period.

As the frequency of the master clock changes, the slave clock tracks and converges to the proper phase within a couple of clock cycles provided the duty cycle remains greater than 50% as the frequency sweeps. Here is where the potential stability problems lie; if the nominal duty cycle is close to 50% and the input control voltage decreases too rapidly, the slave phase can temporarily enter CCM causing the power to increase (a decreasing control voltage should decrease the power). As a broad general rule the control voltage slew rate should be limited so that large power changes occur over 10 cycles or more to give good tracking and prevent instability.

The phase-lock delay circuit ramps are insensitive to process-related current changes; the WP, TM, and WS process corners will all produce the same half-cycle delay. However, because the ramp must be charged and discharged from separate current sources, current mirror mismatches compound to produce large tracking delay errors as shown in Figure 3.17.

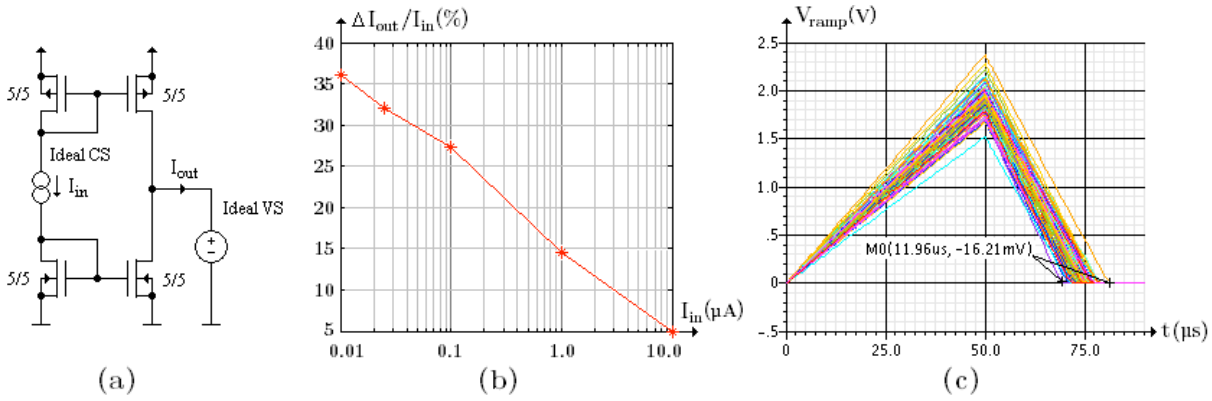

Figure 3.17. An ideal current source I_{in} supplies two current mirrors, and the mirror outputs are summed together. Any mismatch between the mirrors generates an output current I_{out} to an ideal voltage source, which is set at voltage ½ V_{bias} (a). The mirror mismatch increases as the input current decreases; at an input of 25nA, a 32% spread is seen in the output current for 100 Monte Carlo simulation runs (b). The ideal voltage source is then replaced with a capacitor; if the NMOS mirror gain is doubled, and the mirrors are sequentially switched on, a dual-slope ramp is produced (c). For 100 Monte Carlo runs, the nominal 25µs half-cycle delay sees a spread of nearly 50% at the ramp zero-crossing, resulting from the current mirror mismatches.

The results of Figure 3.17c show the problem with the g_m filter of Figure 2.8b and dual slope ramp circuits in general. If the circuit had been implemented with discrete components, where the currents are better controlled, the dual-slope ramp circuit accuracy would be acceptable. However in CMOS the current mirror mismatches make this scheme unusable. A common technique that solves this type of problem is the correlated double sample (CDS) [20]. The dual-slope ramp just discussed uses a double sample (the output timing pulse results from two slopes), but because two current sources are used the slopes have an uncorrelated error (mismatch of the two mirrors). If the same current source could be used to produce both slopes, the slopes would be fully correlated and process errors would cancel. Charging and discharging the capacitor using the same current source can be done by placing the capacitor in a bridge circuit. The results are shown in Figure 3.18.

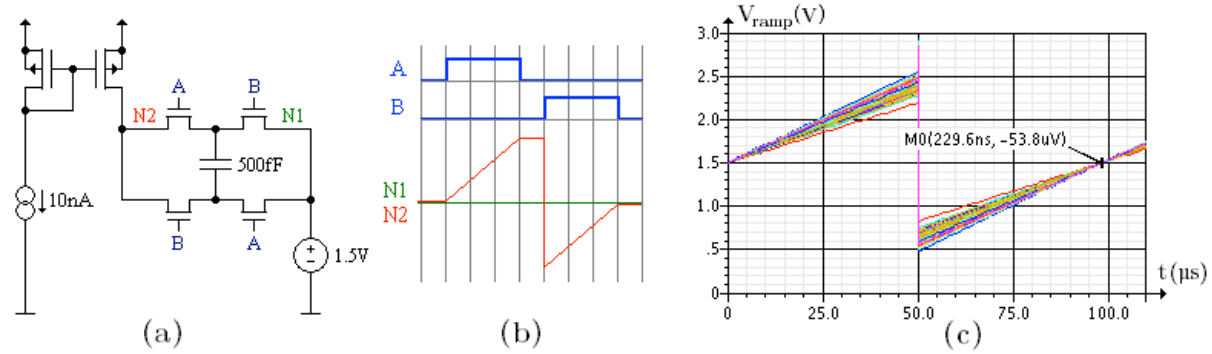

Figure 3.18. When the capacitor is placed in a bridge circuit, the same current source could be used to charge and discharge the capacitor (a). The clocks should be non-overlapping to prevent shorting the capacitor during switching (b). Because all the current source errors are now correlated, both ramps always have the same slope and errors are cancelled. As a result, the zero crossing has a 0.5% spread (230ns for a 50µs period), and a 4% systemic error (nominal zero crossing occurs at 98.2µs) is seen in 100 Monte Carlo simulation runs (c). The systemic error is easily resolved as discussed shortly, but comparing these results with those of Figure 3.17c shows the benefit of the CDS technique. Because the supply voltages are all positive, a 1.5V (½ V_{bias}) reference node allows ramp node N2 to swing negative.

With CDS, the 36% current spread at 10nA (Figure 3.17b) is reduced to a 0.5% timing spread at the zero-crossing (Figure 3.18c). However to be useful for timing, the second ramp must have a different slope than the first ramp. In contrast to large current mirror mismatches, parameter matching between neighboring capacitors is good with component mismatches below 1%. A slight modification of the bridge circuit allows two capacitors to be charged, and then one discharged. The capacitor ratio sets the charge-discharge ratio, which can be adjusted for any delay from zero to 100% of the cycle time (the percent delay equals C2/(C1+C2)), and this ratio can also remove systemic errors like the 4% error seen in Figure 3.18c.

Figure 3.19 shows the basic circuit. MOS-diodes M6 and M7 create a reference voltage of about ½ V_{bias} on node N1. The high current makes this a low-impedance node, and its voltage is not affected by charge injected from the switches. Node N2 is the high-impedance integrating node, which decouples to N1 through the capacitors. Decoupling causes N2 to track noise seen on N1, which then becomes common mode noise that is rejected by comparator U1. Because U1 references to N1 on both ramp slopes the ramp timing is insensitive to ramp noise.

Additionally, process-related variations of the reference voltage and the comparator input offset errors are also removed from the measurement. The comparator input offset is stored on the capacitors during the ramp reset period (RS), so that the initial ramp voltage is the reference voltage on N1 plus the comparator offset voltage. The two errors are thus correlated to both ramps, and so do not affect the time delay result.

Non-overlapping signals PH1 and PH2 are generated from the master clock and control current flow through the bridge. During cycle 1 both capacitors are charged, and C1 is discharged in cycle 2. The falling edge of the comparator output marks the center of the master clock (assuming C1 and C2 are equal). Both capacitors are discharged during RS. During reset U1's output is ½ V_{bias}, and the NAND gate U2 is used to prevent a short on the digital supply as described in Figure 3.19b.

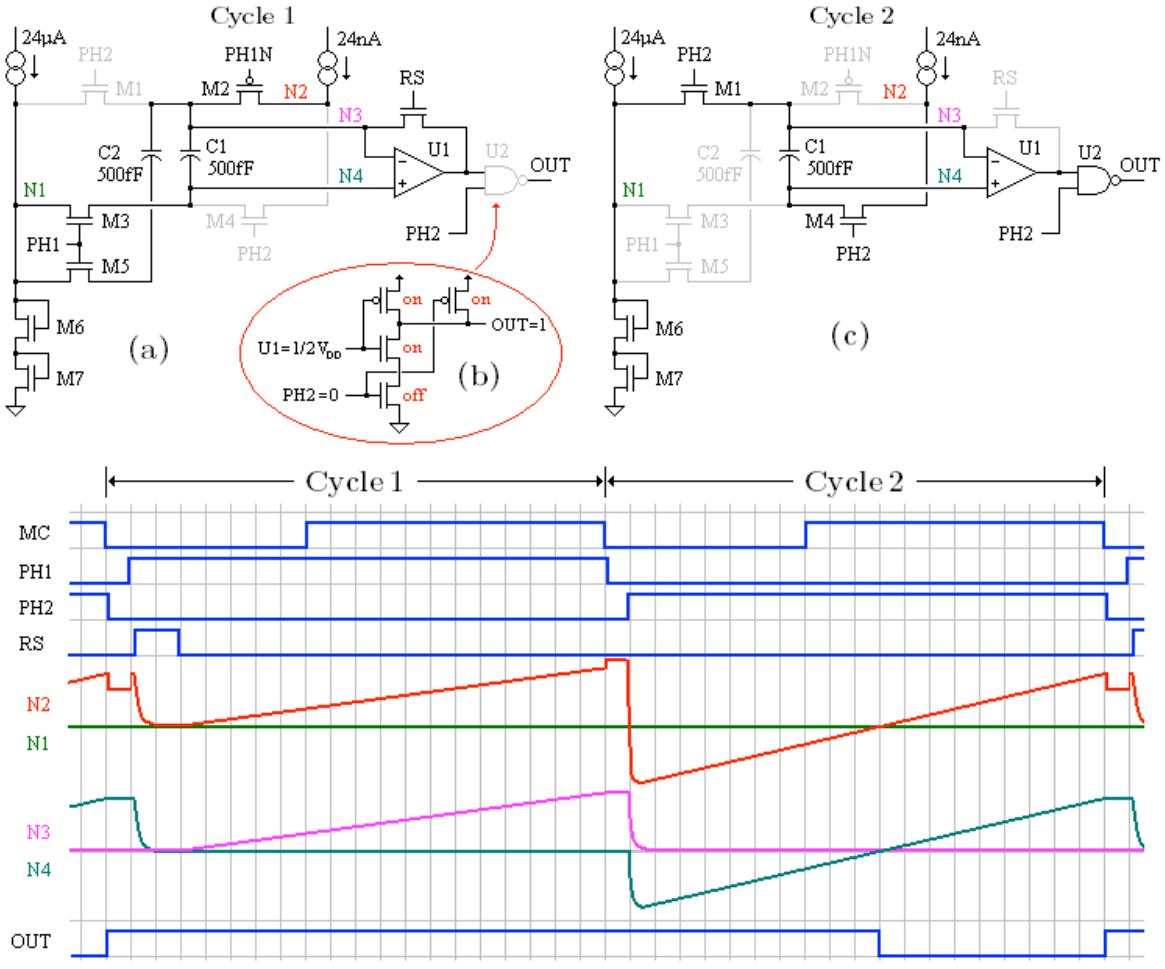

Figure 3.19. During cycle 1 two capacitors are charged, creating a rising-slope ramp on node N2. A reset pulse RS (about 150ns) sets the initial ramp voltage to the reference voltage on N1 (a). During reset the output of comparator U1 is approximately ½ V_{bias}, which is not compatible with digital inputs. A logic-low on control signal PH2 prevents a supply-to-ground short in NAND gate U2 (b). During cycle 2, C1 is effectively discharged by charging the capacitor's bottom plate. The ramp charges at twice the rate during cycle 2, giving the half-cycle delay signal seen at U2's output (c). The timing diagram shows the relative signal sequence and is not drawn to scale.

Because the comparator reference is always near ½ V_{bias} U1 does not need to operate from rail-to-rail, and so a single PMOS differential pair was used. Input hysteresis creates a problem for the linear operation; it gives the amplifier a negative phase margin causing oscillation during reset period RS. The oscillation can be dampened by placing a ~15kΩ resistor between U1 and the capacitors, but this adds a 15ns RC time constant on the reset settling time. Since the comparator inputs decouple through the capacitor and the kT/C noise is low, the comparator hysteresis circuit was omitted.

There are other good reasons for omitting the hysteresis. It adds an unwanted offset, and interferes with storing the input offset during reset. Noise-triggered outputs are more likely to come from switching noise on the bias supply anyway, and as discussed in section 3.2.3, good solutions are available for dealing with this. Any chatter on U1's output during cycle 1 is blocked by U2, so only noise occurring during cycle 2 is of concern. Switching noise generates narrow pulses and a pulse-width conditioning circuit (Figure 3.14) could reject any switching noise-generated outputs. Furthermore, double-triggers are not a concern in the slave controller because an S-R latch will be used to generate the slave clock. In the master controller a toggle flip-flop was needed in case a ZVS failure occurred; however a forced trigger on the slave clock can be derived from the master clock and so an S-R latch can be used. Once the latch is set, additional pulses are ignored, and so double-triggers are not a problem. Simply stated, the comparator hysteresis is not needed and only creates problems.

The comparator has another problem during the ramp reset. Any device that sinks *and* sources current will have an input voltage at which the output current is zero. Unfortunately, this occurs when the input differential voltage equals the input offset. As the capacitors discharge during reset and the differential input voltage decreases, the output current needed to discharge the capacitors also decreases. For the circuit shown in Figure 3.19, resetting C1 and C2 can take 250ns. The comparator is not well suited to discharge the capacitors. Fortunately this problem is easily fixed, as the bridge switches can do most of the work in discharging C1 and C2.

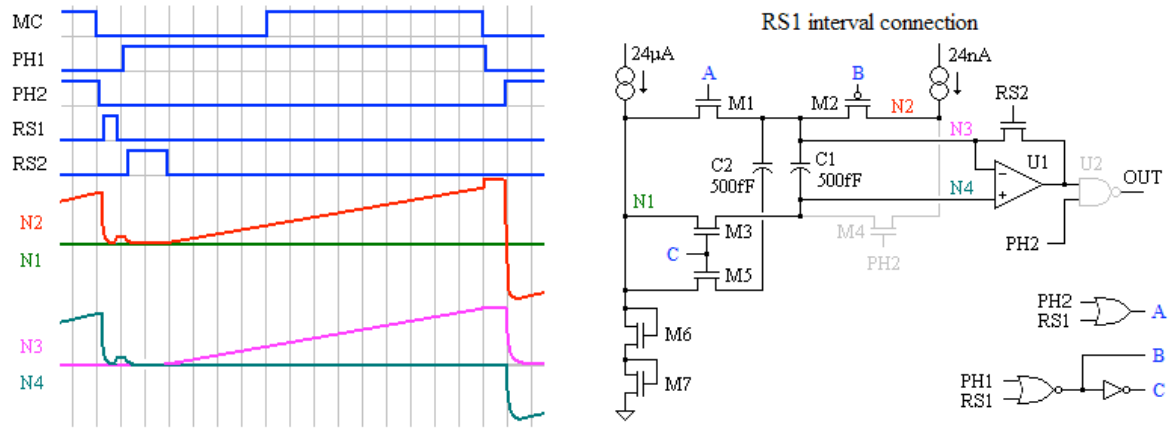

Figure 3.20. As N3 and N4 approach the same voltage during reset, the comparator's output current decreases toward zero, increasing the capacitor discharge time. However with a simple modification, the bridge switches can do most of the work resetting the capacitors. A short (4ns) pulse RS1 is placed between non-overlapping signals PH1 and PH2. M1, M2, M3, and M5 are all switched on during this pulse, shorting both capacitor plates to N1. After PH1 goes high, a second reset pulse RS2 is applied to store the comparator offset on the capacitors. Because of the low output current RS2 takes almost 100ns to settle, but this is still faster than the 250ns reset time needed when RS1 is not used. Generating RS1 allows PH1 and PH2 to remain non-overlapping at both edges and thus they can also be used to control the second ramp circuit.

Reset interval RS2 creates two problems. First, the initial ramp has a hold period that the second ramp does not have; this introduces a frequency-dependent nonlinear error in the time measurement. If the second ramp had a corresponding hold period this problem would be solved. The second problem is that during RS2 as the comparator tries to settle to zero, it is forced to accept 24nA (through M2) into its output. Both problems could be solved if the 24nA current source could be disabled during RS2 (and the RS4 reset during cycle 2).

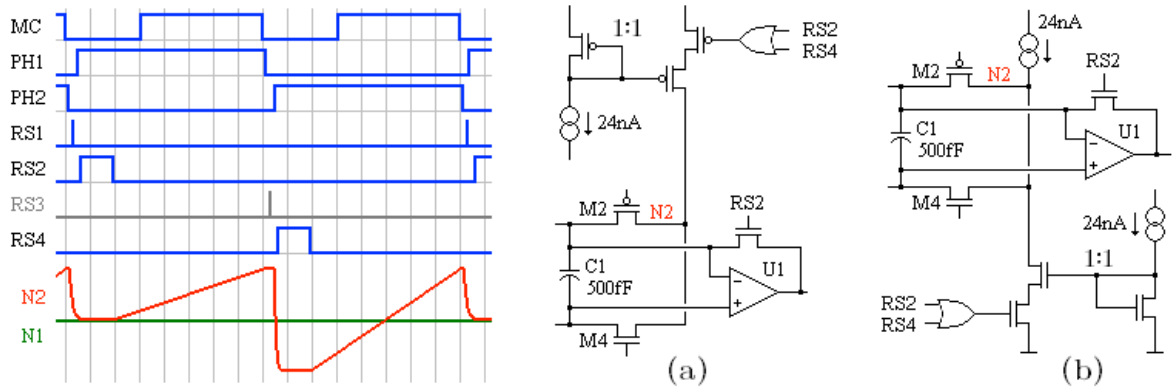

Figure 3.21. The 24nA current source could be directly disabled by switching *off* the current path of the output transistor. Unfortunately, the switch injection charge allows continuous current flow through the narrow RS2/4 pulses (a). Switching *on* a second current source (b) works much better; the second source current-starves the ramp, and mismatches and injection charge correlate out of the dual-slope measurement.

The problem with the circuit in Figure 3.21a is that the current mirror simply does not turn off. Even the smallest switch available in the AMS 0.35µm technology (0.4µm · 0.35µm) has almost 1fF of gate capacitance, which injects about 3fC ($Q=C_{gate} \cdot V_{gate}$) of charge into the channel. 3fC can supply 30nA of continuous current for 100ns, and so the current from the 24nA source does not even decrease. The current source is much easier to switch on than to switch off. The injection charge assists the mirror in turning on, and any delay in turning off can be adjusted by decreasing the pulse width of RS2/RS4. By switching in a second source (Figure 3.21b) the ramp circuit is current-starved, and the 24nA source appears to turn off. Current mismatches and injection errors are common to both ramps and so these effects cancel out of the final measurement.

One nonlinearity error still remains in the circuit. As the second cycle begins, there is a large voltage change on integrating node N2 as shown in Figure 3.22. The charge on C1 must discharge the parasitic capacitance on this node (C_{N2}), causing a voltage loss after switching (V2 < V1). By adding one transistor (M8) to the design, the charge on C2 can assist in changing the voltage on N2. Using C2 doubles the charge available to discharge C_{N2}, so the voltage loss after switching is cut in half. After the transition M8 is turned off so that only C1 is active during the second ramp; the signal RS4 (comparator reset for ramp circuit 2) is also used to control M8.

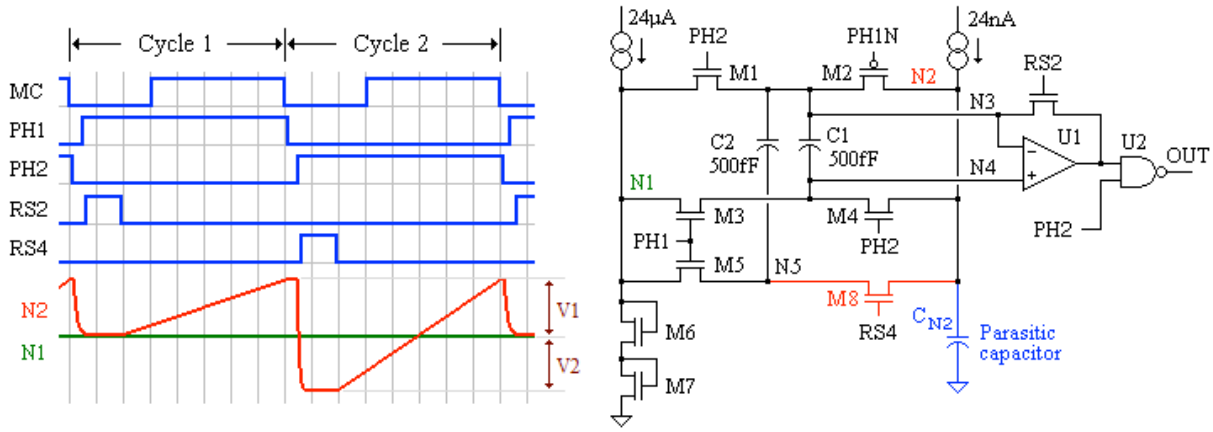

Figure 3.22. The capacitance on integrating node N2 (C_{N2}) forms a parasitic capacitor that C1 must discharge as the bridge switches. This causes a voltage loss (V2 < V1) on N2 at the cycle1-cycle2 transition. Adding M8 allows C2 to assist in discharging the parasitic capacitance during this transition. This addition significantly reduces the tracking error over the controller frequency range.

C1 and C2 also have large parasitic capacitances between their bottom plates and the substrate (C_{sub}). Which plate (top or bottom) wires to N3 has a significant impact on the tracking error. Three cases are interesting as shown in Table 3.6: the top plates wire to N3, the bottom plates wire to N3, or both capacitors are split in two parts and one of the two bottom plates is wired to N3. At the ideal limit where C_{N2} is zero, the following occurs:

- In the case where the bottom plates of C1 and C2 wire to N3, and $C_{N2} = 0$, there is no loss when the bridge switches and V2 = V1. However, there is a large deviation from the ideal ramp slopes because the first ramp charges C1, C2, and both substrate capacitances. This error is not common to both slopes and so a large tracking error is seen.
- If the capacitors are both split into two equal parts (C1a, C1b, C2a, and C2b), and one of the two bottom plates is wired to N3 (C1a and C2a have the bottom plates wired to N3), the two ramp slopes have a common error that perfectly cancels (when $C_{N2} = 0$). However the C1b substrate connection on N4 causes a voltage loss during switching and so a (smaller) tracking error is seen.
- In the case where both top plates wire to N3, both voltage loss and slope error are seen. However, the voltage loss has the same factor as the reduced ramp slope, and so the errors perfectly cancel and no tracking error occurs when $C_{N2} = 0$. From this result it appears that C_{N2} is responsible for tracking errors, and adjusting the C1-C2 ratio is the only way to reduce the error.

N3 connection	V2 / V1 switching loss	Slope 1 / Slope 2 gain	$t_{half\text{-}cycle} / T_{MC}$
C1/C2 top plates	$C1 / (C1 + C_{sub} + C_{N2})$	$(C1 + C_{sub} + C_{N2}) / (C1 + C2 + C_{N2})$	$C1 / (C1 + C2 + C_{N2})$
50/50 split	$C1 / (C1 + ½\ C_{sub} + C_{N2})$	$(C1 + ½\ C_{sub} + C_{N2}) / (C1 + C2 + C_{sub} + C_{N2})$	$C1 / (C1 + C2 + C_{sub} + C_{N2})$
C1/C2 bottom plates	$C1 / (C1 + C_{N2})$	$(C1 + C_{N2}) / (C1 + C2 + 2 \cdot C_{sub} + C_{N2})$	$C1 / (C1 + C2 + 2 \cdot C_{sub} + C_{N2})$

Table 3.6. As described in the text, the capacitor connections have a large impact on ramp tracking errors.

C1 and C2 were placed over protected wells to isolate them from substrate noise, and the wells were connected to N1. The well voltage is correlated to both ramps and has no effect on ramp timing.

Figure 3.23 shows the tracking results over a controller frequency span of 140. The slope of the tracking error can be zeroed by playing with the C1-C2 ratio, but the results show that the tracking error can be limited to a few percent for a dynamic range of more than 100. Because the errors are so well correlated in the final circuit, the guaranteed dynamic range when all process corners are considered only drops by a small amount; at a tracking error of 3% or less the guaranteed range is about 100, making the slave controller more accurate than the master. Because the slave controller measures each master clock, tracking occurs with about a one-cycle delay over the controller frequency span.

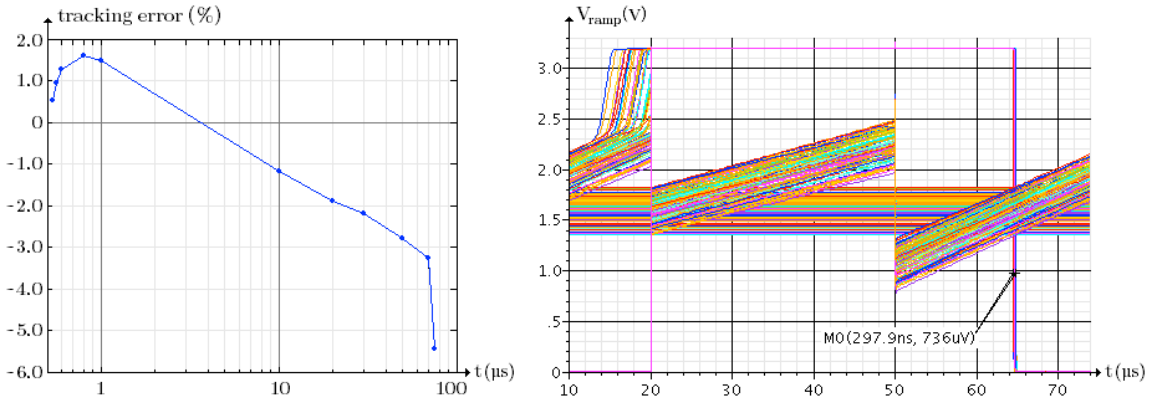

Figure 3.23. A nominal tracking error of a few percent is seen for a controller frequency span of more than 100; the slope of this error can be zeroed by adjusting the C1-C2 ratio. For a 30µs controller clock, a Monte Carlo simulation was made and nodes N1, N2, and signal OUT are shown superimposed. Large process-related variations on N1 become a common-mode error on integrating node N2, resulting in only a 2% spread (298ns) in the output signal timing.

The ½ cycle delay tracking circuit has two ramp generators. Figure 3.24 shows how they are combined using common control signals for both ramps.

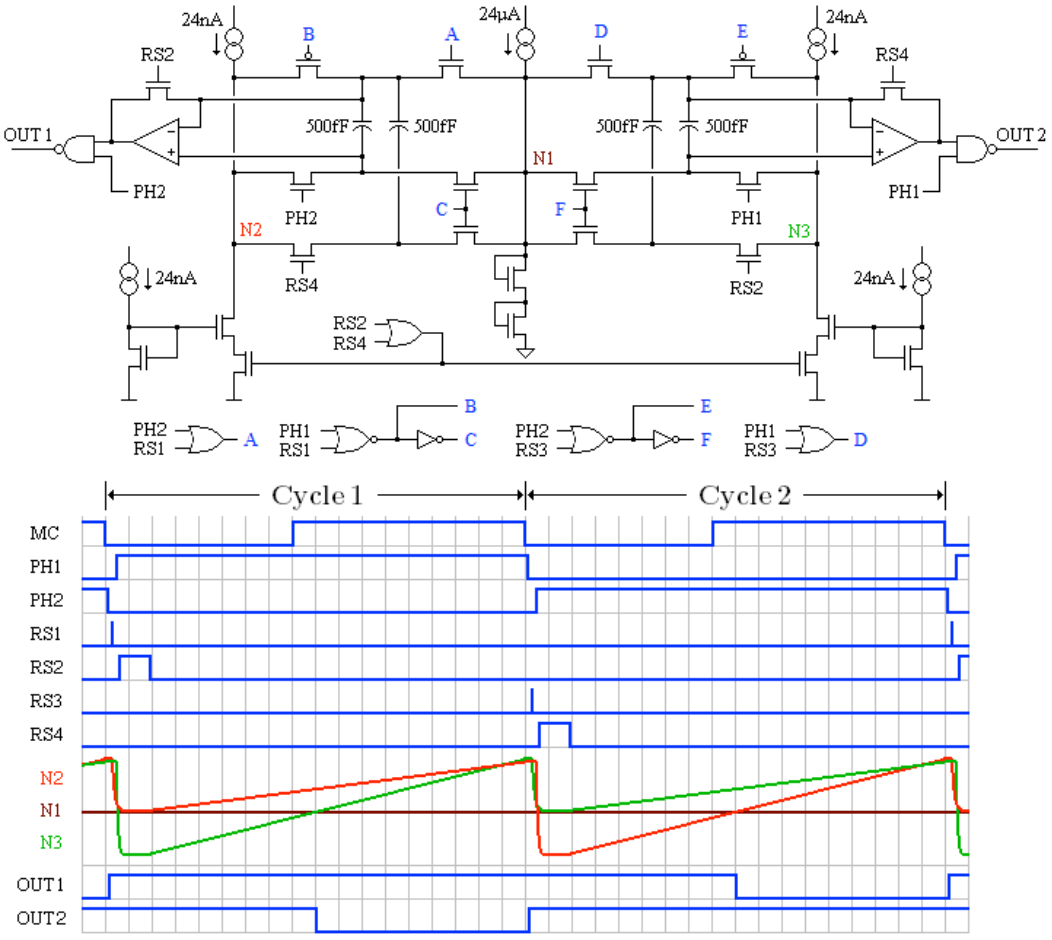

Figure 3.24. Shown are the schematic and timing diagram of the combined ramp circuits.

3.3.2 Slave controller circuit

The master controller used a toggle flip-flop so the master ramp generator could start the next cycle in case the master ZVS failed. But the T-FF caused potential problems such as double-triggers and controller metastability. The slave controller does not have this problem; in the event of a slave ZVS failure, starting the next cycle could be triggered from the master clock. This simplifies the design, allowing an SR-latch to be used for the slave clock output (SC) as shown in Figure 3.25.

The latch is set (ST) by a ZVS signal from the slave converter (ZVSS). The pulse width conditioning circuit looks for falling edges and rejects narrow pulses that could be caused by system noise; it is based on the circuit from Figure 3.14. In the event of a ZVS failure, the falling edge of the master clock sets the slave clock. The latch is set by whichever event occurs first; however, a ZVS failure in either controller requires adjustment from the system-level controller.

The latch is reset (RS) by the outputs of the tracking circuit (OUT1 and OUT2) as shown in the figure. A complete design includes a power-on reset (not shown) and a priority lock-out that resets the latch in the event that simultaneous ST and RS signals occur.

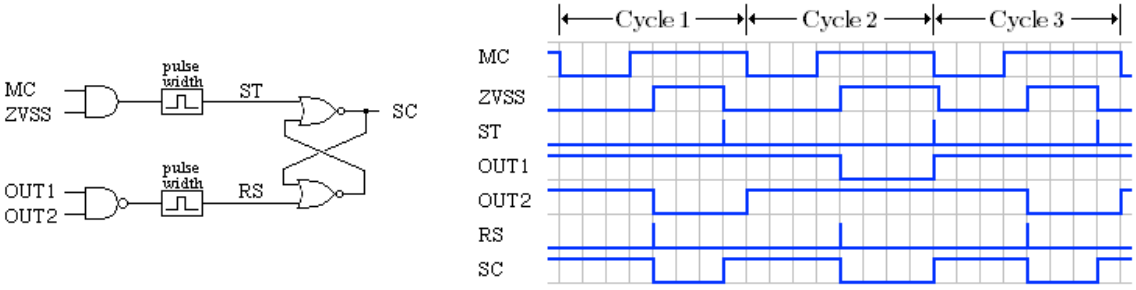

Figure 3.25. The figure shows the block diagram and timing for the slave clock generation circuit. A slave converter ZVS (ZVSS) failure occurs in cycle 2, and the slave clock latch is set (ST) by the falling edge of the master clock (MC). Signals OUT1 and OUT2 come from the ½ cycle delay-tracking circuit. Not shown are a power-on reset and priority lock-out. The lock-out circuit resets the latch and prevents metastability in the event that simultaneous ST and RS pulses occur.

The slave clock tracks the master over more than a two orders-of-magnitude frequency sweep with a tracking error of only a few percent. The design owes its success to the error cancelling ability of the correlated double sample. CDS is widely used in switched capacitor circuits [20], imaging systems [21], and high-end analog-to-digital converter designs [22]; this design shows that it can also be used in power systems, and could become more common as state-of-the-art controller designs evolve.

3.4 Current sources II

In section 3.1, process-stable current sources were investigated. Despite a large amount of effort, a 50% current spread is typically seen at the process corners (Table 3.2) even for well-designed current sources. As the current is mirrored-down to useable levels for timing circuits, component mismatch errors can add a large additional spread to the current (Figure 3.17). With some tricks to keep the comparator from latching at the negative rail, the guaranteed dynamic range of 50 was increased to 90, but it appeared that additional effort would not increase this range much beyond about 90 (section 3.2.1).

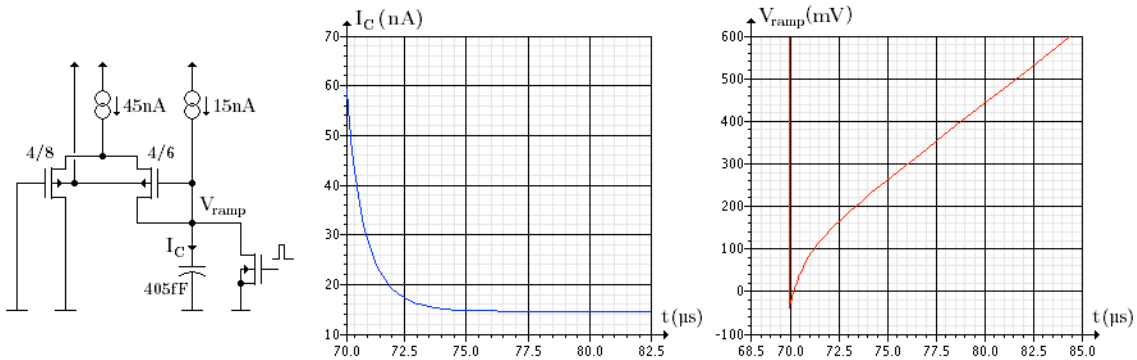

Figure 3.26. The schematic shows a modification to the ramp generator of Figure 3.7. The constant current source is replaced with a voltage-dependent nonlinear source, with a resulting nonlinear ramp. This can increase the dynamic range by a factor of two or more as discussed further in the text.

Extending the high-frequency end of the spectrum would require more current from the current source; extending the low-frequency end would require less current (Figure 3.8). The problem is solved by modifying the *constant* current source into a nonlinear source that decreases its current as the ramp voltage increases. A simply way to do this is shown in the schematic of Figure 3.26.

As the ramp begins, the current is boosted to 60nA or more; this reduces the overhead associated with resetting the comparator, and it increases the maximum guaranteed controller frequency. The supplementary current is supplied by one leg of an unbalanced differential pair that slowly turns off as the ramp voltage approaches 200mV. The increased current at low ramp voltages allows the nominal ramp current to be decreased from 25nA to 15nA or less, which extends the low frequency range. This factor-of-four change in ramp current increases the guaranteed dynamic range from 90 to more than 220 against all process corners. Further extension is possible as the 60nA/15nA values were chosen casually and are not hard limits.

For the system-level controller the nonlinear transfer function is not a problem; it will supply whatever control voltage is needed to satisfy its own feedback conditions. A nonlinear current source would correspondingly extend the dynamic range of the tracking circuit in the slave controller as well; in this case a different control scheme would be needed, but fortunately this is also easily solved.

3.5 Integrated CMOS controllers

At the beginning of the chapter the question was raised as to whether a BCM controller implemented in silicon could achieve the same performance seen in controllers implemented with discrete components. Two requirements were imposed in the conceptual model. First, no failures should occur as the result of CMOS process variations combined with component mismatch errors; preventing these failures means that some expensive production testing can be avoided. The second requirement was that the dynamic range should be large enough that a "universal controller" is developed. The dynamic range must be the guaranteed range when all process corners are considered. This would create portability, allowing the same controller to be used in different product designs.

Although many problems relating to process variations and component mismatches were encountered, it was possible to resolve these problems in the design. The conclusion then is that power systems controllers can be implemented in CMOS with no loss of controller performance. For large-scale production, replacing a PC board full of components with a single chip offers an attractive option in reducing product size, weight, and manufacturing costs. It is an option that should be considered seriously.

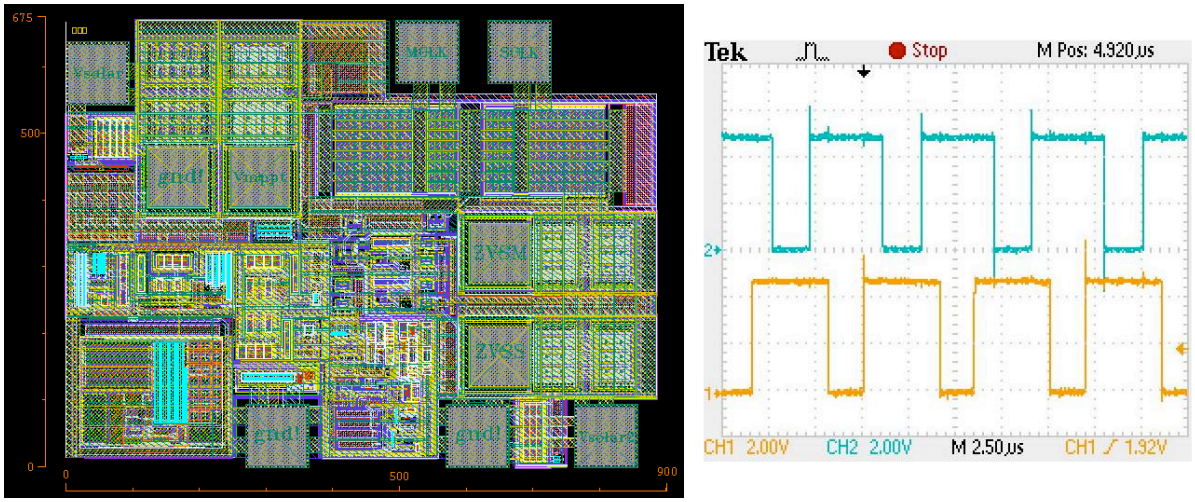

Figure 3.27. The entire two-phase controller fit into a 0.6mm^2 chip; the oscilloscope plot shows the slave clock tracking 180° behind the master clock.

3.6 References

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4. Application and results

As population and demand for energy grow, global fossil fuel reserves decline at an alarming rate. The industry has responded with increasingly aggressive and environmentally destructive extraction techniques to supply the global demand for energy. Hydraulic fracturing of the bedrock is used to extract natural gas reserves; complaints of minor earthquakes and contaminated water supplies often follow this technique. The open tar sands pits in Canada will be large enough to be seen from the moon. But declining reserves and environmental damage are only part of the problem; energy-related trade deficits burden entire countries with loans to central banks that can never be repaid, and interest payments that compound the debt.

Fortunately engineering is responding to the problem, and significant progress is being made. Two main areas of focus are local distributed generation of energy using renewable resources, and improved efficiency of consumer products. Solar, wind, tidal, and geothermal energy production is helping relieve some of the burden on the fossil fuel industry, and large untapped reserves exist. While clean renewable energy production helps, the silent revolution has been the energy-star improvements in device efficiency. A 19-inch CRT computer monitor from a few years ago consumed 110W; today a 22-inch LCD monitor consumes only 18W, which drops to less than 2W in dark screensaver mode [1]. A 30 year investment developing the quantum cascade laser led to an unexpected byproduct: LED lighting is 40% more efficient than compact fluorescent lighting, producing the same luminous flux at 10W that a 60W incandescent light produces [2]. Distributed among millions of homes, these energy-saving devices are reducing the global demand for energy.

To address global oil consumption, the automobile industry is also responding. The two lines of development have been hydrogen fuel cell and battery-powered electric vehicles. Fundamentally both approaches are electric, as the internal combustion engine is replaced with light-weight high-torque electric motors mounted on the wheels, and state-of-the-art power system design plays a critical role in developing these motor vehicles. Fuel cells work well in colder climates where battery efficiency is low; but handling hydrogen is problematic and may limit the market for these vehicles. Battery systems are more consumer-friendly, but high temperatures in warmer climates reduce battery lifetime [3].

The two main sources of battery heating are internal heating during charging and discharging, and ambient heating. At peak power, a battery stack producing 100kW can require 1-2kW of cooling [4]; this is typically done through some combination of active cooling and forced airflow [5].

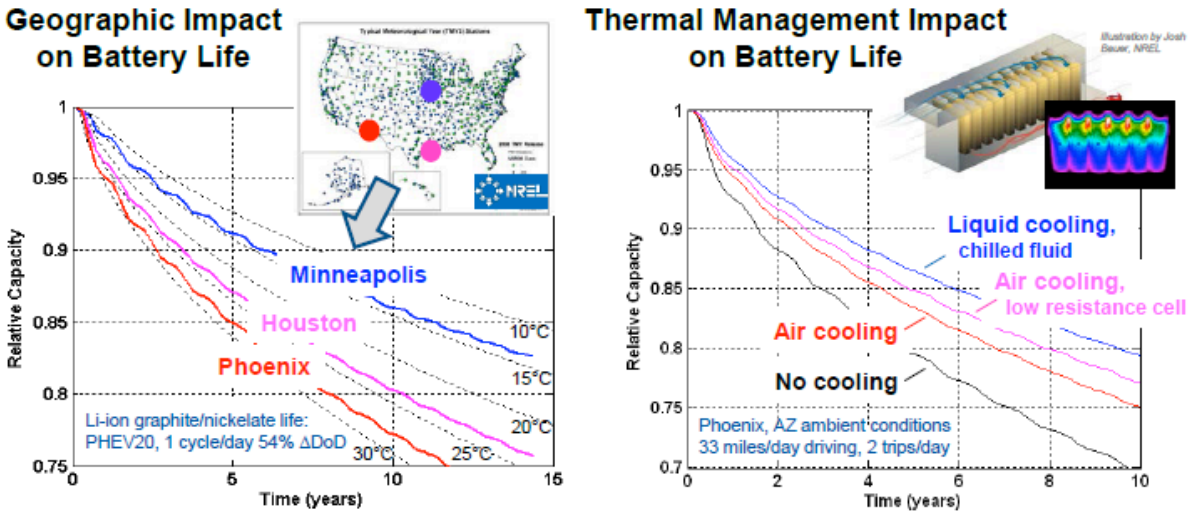

Figure 4.1 The ambient temperature has a significant impact on battery lifetime; operating at 30ºC can decrease the lifetime to less than 10 years. Under these conditions active cooling and forced airflow will be needed. Image from [4].

Ambient heating is also dangerous to the battery's life expectancy. For cars parked in sunlight all day, the temperature can easily exceed 50ºC. Cooling fans and systems can reduce the battery temperature, but the power to run these systems discharges the battery. Since sunshine is a major source of the heating problem, an integrated solar panel in the roof of the car could supply the needed power. A 0.5 m^2 solar panel can deliver about 50W in direct sunlight, which should easily cool the passive battery. But on a cool sunny day battery cooling is not needed, so the power could charge the batteries instead. Hybrid and electric cars usually come with two batteries: a high-voltage stack for the drive train, and a low-voltage battery for normal electronic systems. Here an interesting hybrid converter is proposed to do the job. The boost-flyback (or buck-flyback) converter has the ability to adaptively charge two battery stacks without the need for controller supervision.

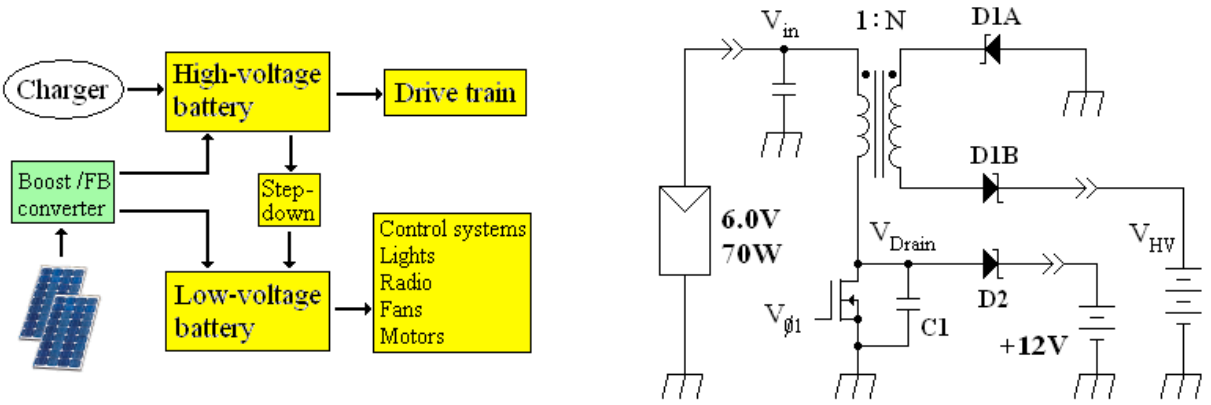

Figure 4.2. Electric cars typically have a high-voltage battery for the drive train, and a low-voltage battery for electrical devices and systems. A car parked in the sunlight all day must run cooling fans for battery thermal management; an integrated solar panel could supply the power needed for this. A hybrid converter such as the boost-flyback is ideal for adaptively charging multiple battery systems. Charging priority is given to the battery with the lower charge.

The boost-flyback architecture is achieved when the primary of a flyback transformer is used as the inductor in a boost converter; this circuit is shown in Figure 4.2. For simplicity only one phase is shown, but to reduce the input and output current ripple a two- or three-phase converter is assumed. For extended battery life low ripple charging is preferred, so it is also assumed that appropriate filtering (not shown) and connection to battery management systems will be made [6].

4.1 Boost-flyback converter

The solar panel output voltage (V_{in}) was configured to be less than the low-voltage (12V) battery; so a boost-flyback converter is used. When the switch opens, and the secondary circuit begins conduction, the drain voltage becomes:

$$V_{Drain} = V_{in} + \frac{V_{HV}}{N} \tag{34}$$

where N is the transformer turns ratio, and V_{HV} is the voltage of the high-voltage battery stack [7]. If the voltage on V_{Drain} is high enough to forward-bias D2, the 12V battery will charge. As the 12V battery charges, its voltage increases and more power is adaptively output to the high-voltage battery. When the 12V battery is fully charged, the drain node voltage will not be high enough to turn D2 on. The voltage at which the 12V battery stops charging is set in the design with turns ratio N.

Figure 4.3 shows the timing diagram for the converter. In the case where the 12V battery is discharged enough that D2 is strongly forward-biased, the converter operates like a boost converter (Figure 4.3a). After the switch turns off (at t_1), large voltage changes are seen on the drain node and in the secondary during interval t_1-t_2. The drain node capacitance, inter-winding capacitances, and capacitances on the secondary nodes must charge; this causes the current in the primary, $I_{primary}$, to decrease, and a small current I_{D1} must flow in the secondary circuit. This decrease of $I_{primary}$ causes a power loss and creates start-up problems at low current. Steps must be taken to limit the inter-winding capacitance in the high-voltage secondary. This is discussed further in the transformer design section.

How much current flows in D1 during this transition is determined by the transformer coupling, node capacitances, and the relative timing at which D1 and D2 turn on. A weakness of this circuit is that a small percentage of current will always flow in the battery with the larger charge.

In the case where the 12V battery is fully charged and D2 does not forward-bias, the converter operates like a flyback converter, and the high-voltage battery is charged (Figure 4.3b). In this mode the primary current is not continuous, but decreases to zero at time t_2. D2 does turn on during the t_1-t_2 interval while the secondary capacitances are charging. The delay turning D1 on determines how long D2 stays on. The current in the secondary is low ($I_{primary,\ peak}$ /N) and the secondary voltage is high, which exacerbates turning D1 on. To minimize the reverse-recovery delay time, D1 needs to be a Schottky diode. In addition to reducing the parasitic winding capacitances in the transformer design, a snubber in the secondary circuit can also assist in turning D1 on and minimizing the time that D2 stays on [8].

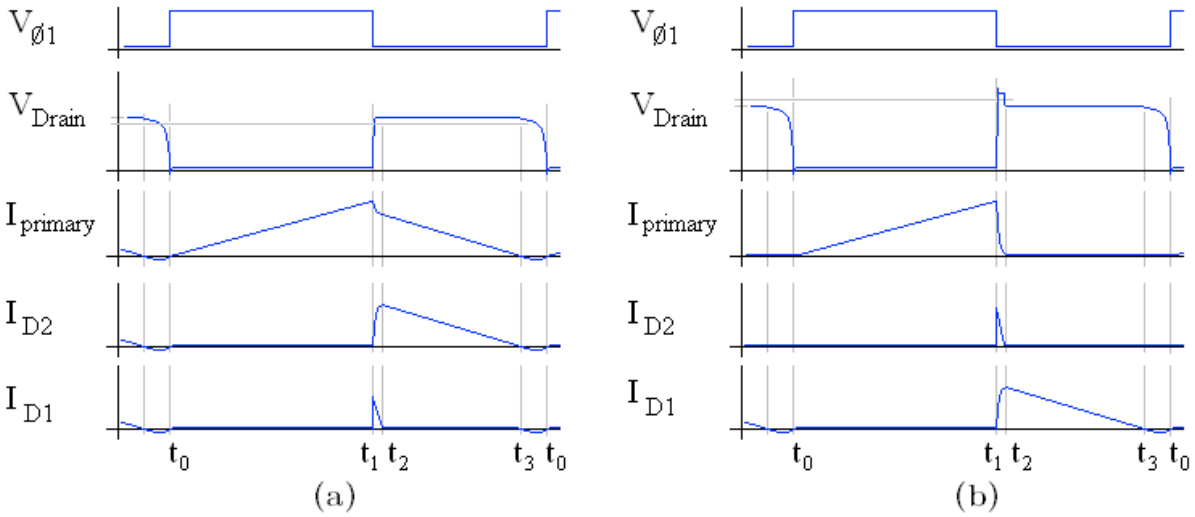

Figure 4.3. The figure shows the timing diagram for the boost-flyback converter. In the case where 12V battery is charging, the circuit operates like a boost converter (a). As the voltage of the 12V battery increases and D2 no longer becomes forward-biased, the converter then operates like a flyback (b). The battery voltages and transformer turns ratio N adaptively determine which battery is charged without supervision from a controller.

4.2 Transformer design

Ideally the drain voltage of the power switch should have fast rising and falling edges during switching, and a small oscillatory peak on the rising edge as shown in Figure 4.4a. To reduce this peak, the transformer coupling must be high. However, tight coupling means high inter-winding capacitance. The capacitance in the secondary reflects into the primary circuit as $C`_{primary} = N^2 \cdot C_{secondary}$, which causes a slow oscillatory rising edge on the drain node as shown in Figure 4.4b. This slow edge confounds the control system and significantly cuts the converter dynamic range by limiting the minimum operating power.

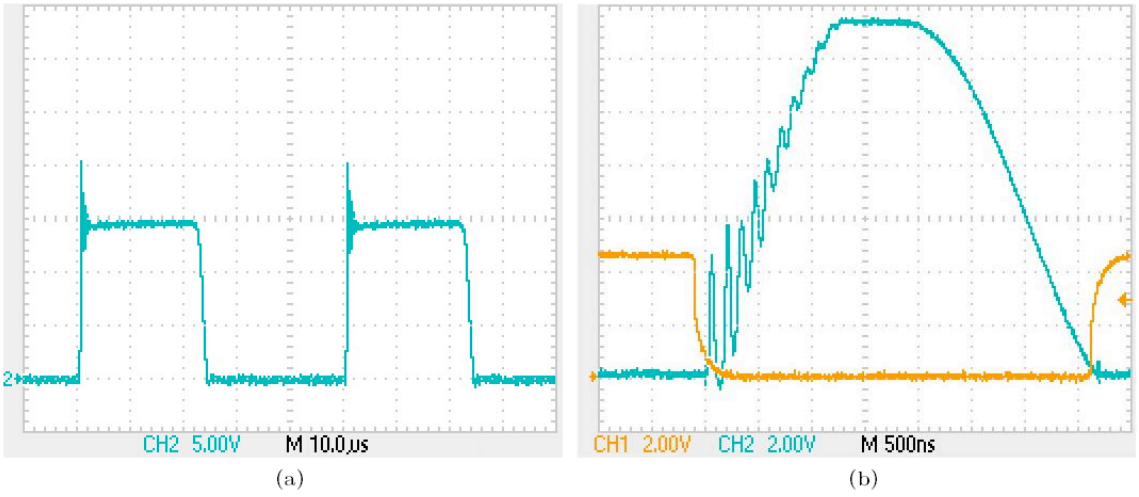

Figure 4.4. Ideally the drain node voltage should have a fast rising edge with a small oscillatory peak (a). However when the transformer turns ratio N is large, the secondary capacitance reflected into the primary circuit causes a slow oscillatory rising edge (b). The oscillations can falsely trigger the ZVS circuit, and the long risetime cuts the dynamic range and minimum converter power. In comparing the graphs, please note the scale changes.

A tightly wound secondary-over-primary, separated with a 10µm thick poly sheet, can have hundreds of picofarads of capacitance between the primary and secondary windings. Additionally, for a high turns-ratio transformer, the secondary will likely be multilayer, giving additional secondary-to-secondary capacitance. In a high-voltage, low-current secondary circuit the energy needed to charge and discharge these capacitances can exceed the energy in the inductor windings. When this happens the converter will not start up, the minimum power the converter can operate at is increased, and the conversion efficiency decreases.

- The energy stored in the inter-winding capacitances increases in the high-voltage section; this energy is independent of the converter power: $U_C = ½ C \cdot V^2$.

- The energy stored in the winding inductance is proportional to the converter current. As the power decreases, the energy stored in the inductance decreases: $U_L = ½ L \cdot I^2$.
- As the power decreases, a larger fraction of the converter energy is needed to charge and discharge the winding capacitances. The charge-discharge cycle simply moves current around, creating higher ohmic and core losses, without making any useful contribution to the converter output power.
- For high-voltage systems the energy held in the winding capacitance sets the practical high-frequency limit of the converter. To achieve a reasonable dynamic range, the low-frequency end of the converter cycle must be extended. This is done by increasing the inductance, which increases ohmic and core losses. The inter-winding capacitance then becomes a limiting factor in the achievable converter power efficiency. The most important aspect of the high-voltage transformer design is dealing with this capacitance.

To minimize these losses, the capacitance must be reduced. Increasing the spacing between layers, and decreasing the wiring density on each layer, effectively increases the distance and decreases the area of the capacitor plates. Porous low-k dielectric sheeting is used for spacers between layers [9]. To reduce the inter-winding capacitances, the fill-factor must be reduced.

Another way to reduce the energy stored in the inter-winding capacitance is to reduce the voltage difference between adjacent winding layers in the transformer. Consider the two cases shown in Figure 4.5. In the first case the layer is wound clockwise (CW) around the spool, going from left to right; the wire is then run back to the left side and the next CW layer is wound. Assuming a 200V span across two layers, the inter-layer capacitance sees a constant 100V differential across the winding layer. In the second case the layer is wound CW from left to right, and then the next layer is wound CW from right to left. In this case there is no voltage difference on the right and 200V difference on the left. Because the energy stored in a capacitor is proportional to $(\Delta V)^2$, the second case has 33% more energy stored in the parasitic winding capacitance. While the first case may be more difficult to manufacture, it is the better design for high-voltage transformers.

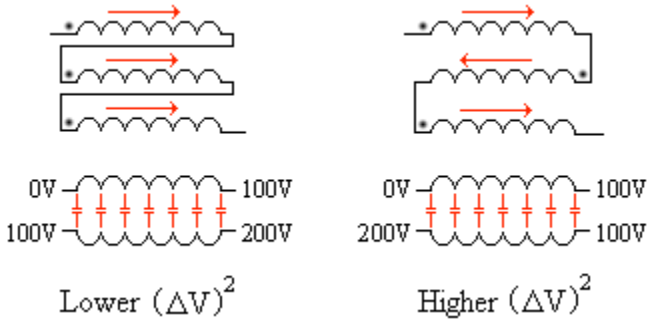

Figure 4.5. When the layers are wound in the same direction, the voltage stress on the dielectric is cut in half, and the energy stored in the inter-winding parasitic capacitance is reduced by 33%.

After a core type, size, gap length, and turns ratio have been selected, the design variables are: wire size, the number of parallel wires per winding, number of layers and wire density per layer, dielectric thickness between layers, direction the secondary is wound with reference to the primary, selecting which secondary layer is closest to the primary, selecting how the layers are wound (as shown in Figure 4.5), and selecting which secondary leg will have the rectifying diode. There is no best answer for any of these variables because the selections depend on the design requirements. To illustrate this point, three design examples are considered. In the three cases a three-layer secondary is assumed for the design:

- In the first example, most of the energy should go to the high-voltage output, and the low voltage battery gets only enough power for some control electronics; if the low voltage battery is discharged, it adaptively receives more power. In this case the secondary is wound the opposite direction as the primary, the rectifying diodes are placed on the secondary return side, the primary-secondary windings are separated with minimum dielectric thickness to increase the coupling capacitance, and the secondary layers are separated by a thicker dielectric thickness to reduce the inter-winding capacitance in the secondary. This is shown in Figure 4.6a. This configuration maximizes the voltage stress between the secondary and primary windings and the reverse winding direction and diode placement maximizes the energy coupled from the primary into the secondary during switching. This opposes the rising edge of the drain voltage, reducing the energy delivered to the low-voltage output. To help speed up the secondary diode during switching, a lossless snubber can be added to assist the diode in turning on. The increased voltage stress and capacitance limit the low power performance and dynamic range, but the configuration reduces the amount of energy coupled to the low-voltage battery.

- In the second example, approximately the same energy goes to both outputs. Adaptive charging priority is given to the output with the heaviest load or most discharged battery. In this case the secondary diodes are placed on both legs and the dielectric thickness is increased between primary and secondary windings to reduce the coupling capacitance. The secondary can be wound in the same direction or opposite of the primary depending on which output should nominally receive more power. The diode placement and reduced capacitance reduce the energy coupled from primary to secondary during switching, delivering more energy to the low-voltage output. This configuration (Figure 4.6b) also reduces the energy stored in winding capacitances, improving the low-power performance and increasing the dynamic range.
- In the last example, most of the energy should go to the low-voltage output. In the event that the low-voltage battery becomes fully charged, power is adaptively directed to the high-voltage output as the low-voltage battery charges. In this case the diode is placed on the high-voltage leg and the secondary is wound in the same direction as the primary (Figure 4.6c). In this configuration, energy is coupled from secondary to primary during switching, and assists the drain voltage rising edge –directing more energy to the low-voltage output. The fast rising edge causes a high-current spike to the low-voltage output, and if a battery is charged additional filtering will be needed. A thicker dielectric can be used between the primary and secondary windings, and the reduced voltage stress in this configuration minimizes the energy stored in the winding capacitances. This improves the low-power performance and dynamic range.

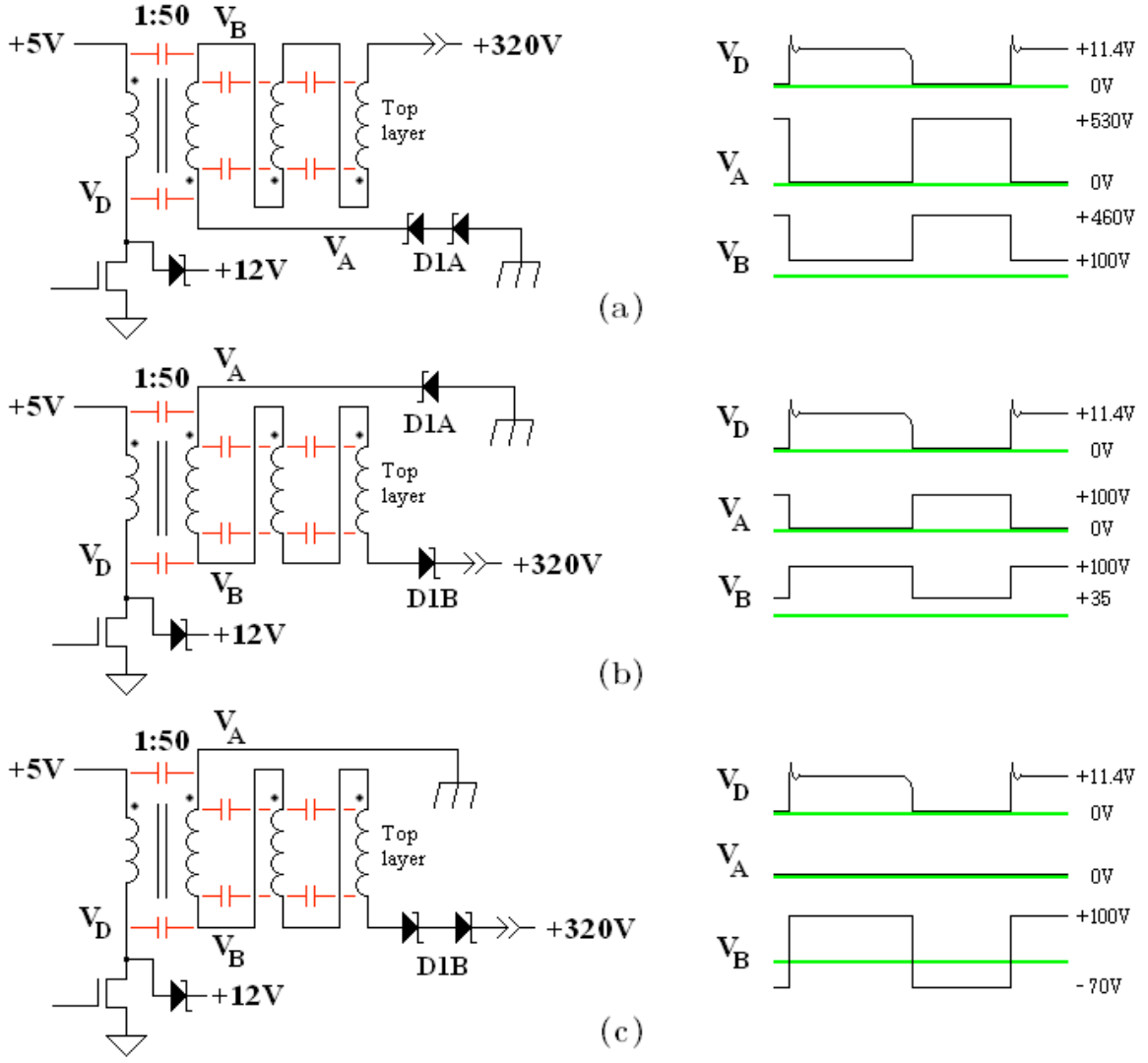

Figure 4.6. The diagram shows how the primary-secondary coupling can be used to direct the power flow. In the first case the secondary is wound in the opposite direction as the primary and the secondary diodes are placed on the return leg in the high-voltage section (a). The large voltage swings on secondary nodes V_A and V_B oppose the rising drain voltage edge during switching; this decreases the nominal power going to the low-voltage output (12V battery). Conversely, the third example shows the secondary wound in the same direction as the primary and the diodes are placed on the high-voltage leg. In this case coupling from node V_B assists the drain voltage rising edge, coupling more power to the 12V output.

Although it might seem like a minor detail, coupling through the winding capacitances influences the current peaks during switching. The third case from Figure 4.6c will have a higher current peak going to the 12V battery (Figure 4.7), requiring more filtering. Increasing the primary-secondary capacitance slows the drain voltage edge and reduces this peak; decreasing the secondary-secondary winding capacitance speeds up the diode turn-on time, which also reduces this peak. Strategically placed capacitances reduce the filter requirements, but the trade-off is more converter energy trapped in these capacitances.

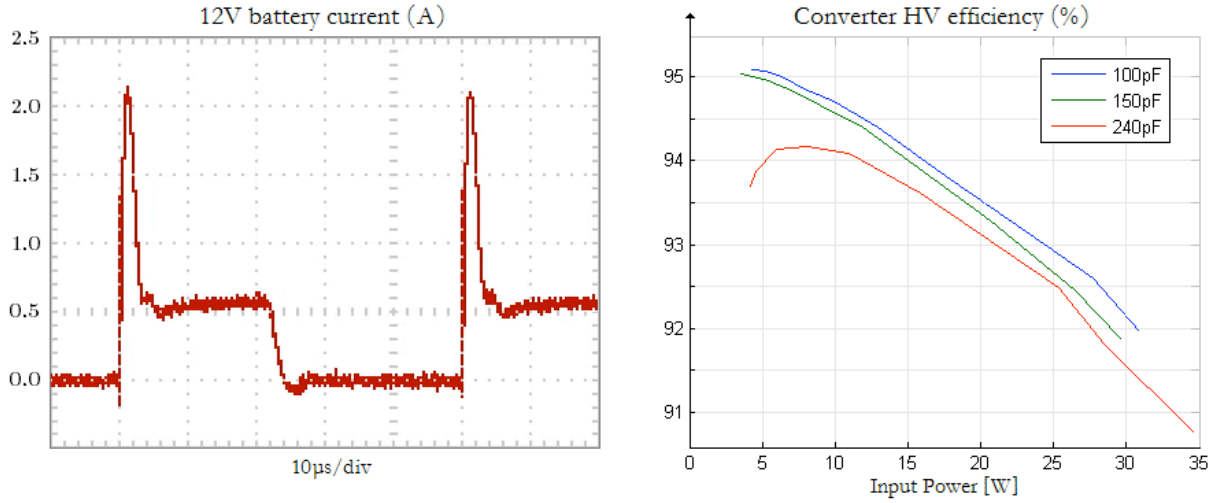

Figure 4.7. Depending on how quickly the secondary circuit turns on relative to the drain voltage rising edge, a large current peak (single phase shown) can decouple into the 12V output. High peak surges require filtering to protect the battery lifetime. This peak decreases as the inter-winding capacitance increases, but charging and discharging this capacitance decreases the converter efficiency, and if the capacitance is large enough, it affects the low-power performance.

The converter efficiency curves shown in Figure 4.7 were for the high-voltage section with a 5V input and a 330V output. They indicate that reducing the inter-winding capacitances increases flyback efficiency. For this test the same transformer was used for all three curves; the only difference was the thickness of the plastic sheets between winding layers (1, 5, and 10 wraps of poly sheeting). Adding space between the winding layers increased efficiency despite an increased leakage inductance. This is because less current is non-productively moved around charging and discharging the winding capacitances, which reduces the core and ohmic losses.

Converter losses are proportional to the current, not the power. Ferrite cores can achieve higher efficiencies than seen in Figure 4.7, but the limiting factor here was the high primary current. The solar panel was configured for a low-voltage, high-current output. This decision was made to reduce the shadowing problem: when the cells are wired in series the current is limited by the cell with the lowest current. A shadow on a single cell can limit the power of the whole stack. For a high-end system, weak cells could be bypassed. But this requires sophisticated sensing and control, which would increase the cost of the design. The compromise was wiring some cells in parallel to reduce the risk of shadowing, and accepting a slightly lower conversion efficiency.

4.3 Test results

A test was made to determine the feasibility of using a hybrid converter to supply two power outputs. Testing was done using a 12V lead-acid battery and a programmable load for the high voltage stack. Secondary voltages ranging from 200V to 375V were tested. An ETD-39 coil form with 3F3 ferrite material was used for the transformer; center-leg air gaps from 100-300µm were used. The primary was wound with 5 turns using 32 parallel 0.2mm wires; the secondary was wound over the primary using a single 0.2mm wire with 200 turns wound on 5 layers, with 80µm poly sheets between each layer. Two IDD03SG60 silicon-carbide Schottky diodes from Infinion were used for the high voltage secondary; these diodes have very low capacitance compared with other high voltage diodes.

Figure 4.8 shows the test results for a 330V load with 35W per phase input power at 6.0V input voltage. At full charge, only 3% of the output power is going to the 12V battery. At 10W input power, the efficiency peaks at more than 96%, however at 35W the high ohmic losses decrease it to around 93%. In the proof-of-concept circuit, D2 was implemented with a Schottky diode; however, the large current to the 12V supply generates an excessive amount of heat in the diode. In a practical circuit, this diode would have to be implemented with an active switch.

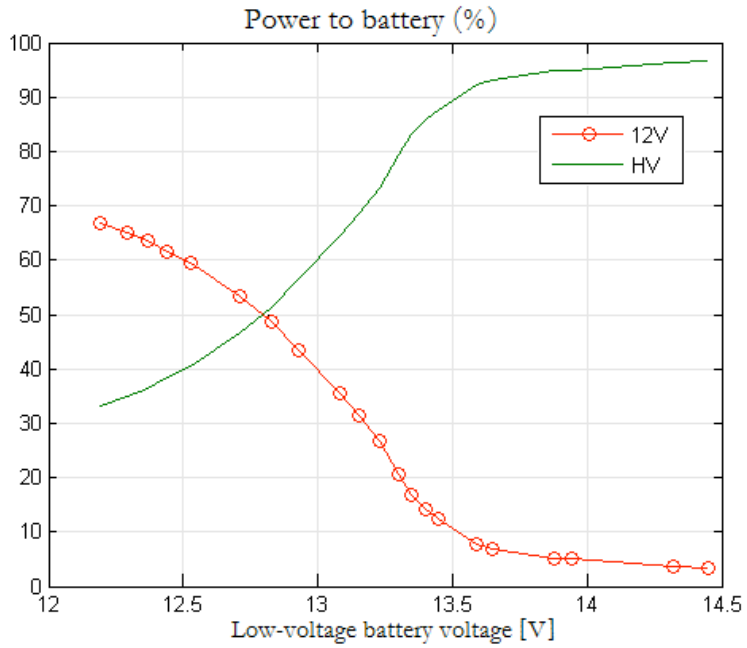

Figure 4.8. Test results show that as the 12V battery charges, more of the output power is diverted to the high voltage stack. At full charge, about 3% of the output power went to the 12V battery.

Hybrid converters such as the boost-flyback or buck-flyback offer a simple single-converter solution for systems with two power outputs. Sensitivity to changes in the relative output voltages allows the converter to adaptively direct power to the output with the heaviest load, and direct power away from an output as it approaches full charge. This adaptive nature of the converter simplifies the controller requirements and hardware.

The converter has several weaknesses. While sensitivity to output voltage changes is favorable for adaptive charging, it is also sensitive to the input voltage. If the design allows some flexibility in the output voltage of the low-voltage section, then the low-voltage output will simply track input voltage changes. But if a battery is charged, the design would need to account for input voltage variations. If a secondary step-down converter is already part of the system design (Figure 4.2), the hybrid converter can be designed to prevent overcharging of the low-voltage battery, and still use the adaptive charging abilities of the converter.

As previously discussed, the inter-winding capacitance of the high-voltage section can limit the minimum converter operating power and dynamic range. But while the inter-winding capacitance is an annoyance, there are many design options available for dealing with this problem. By reducing the capacitive coupling between adjacent transformer winding layers, the high-voltage section can operate even at extremely low input powers, where tightly wound transformers fail to work.

The boost-flyback converter is capable of delivering hundreds of watts, and by controlling the capacitance in the high-voltage section it can also operate down to a few watts. The ability to adaptively direct power between loads, and operate over a wide power range, makes this an ideal converter for working with energy-harvesting and regenerative sources where the input power can be unpredictable.

4.4 References

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5. Conclusion

Modern power system design is a rapidly evolving art in which new materials, form factors, components, circuit design, and operating modes are improving the energy efficiency of power converters. To supplement these developments, a new class of multiphase controllers is also needed. This provides an opportunity for power system engineers and circuit designers to collaborate in developing the next generation of high performance products.

The circuit design trend has been toward integrated designs in silicon. A CMOS integrated circuit can replace a printed circuit board full of components with a single chip –reducing product size, weight, and manufacturing costs. The reduced chip-count and a phase-shedding controller design can significantly reduce the vampire load a converter draws when in standby mode. When implemented in consumer products, such improvements in energy efficiency are greatly reducing the global energy demand. However, CMOS process variations and component mismatches can make controller designs quite challenging.

This thesis examined whether a BCM controller implemented in silicon can achieve the same performance seen in controllers implemented with discrete components. Two requirements were imposed on the conceptual model. First, no failures should occur as the result of any combination of CMOS process variations, component mismatch errors, and converter operating conditions; preventing these failures means that some expensive production testing can be avoided. The second requirement was that the dynamic range should be large enough that a “universal controller” is developed. The dynamic range must be the guaranteed range when all process corners are considered. This would create portability, allowing the same controller to be used in different product designs.

To guarantee design robustness it was seen that 6-sigma simulations are not sufficient. Instead, Monte Carlo simulations of mismatch errors were run from the weak process corners. This simulation gave the hard limits of circuit performance and potential controller failures and metastability. The approach exposed many problems with the nominal design, and every solution seemingly created new problems. However, it was found in the end that all problems could be resolved through design. The conclusion then is that power system controllers can be implemented in CMOS with no loss of controller performance, giving designers greater flexibility in controller design.