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DISSERTATION

Schottky Barrier MOSFETs with Atomic Layer Grown High-k Oxides and Ultrathin Metal-Interlayers on Silicon (111)

ausgeführt zum Zwecke der Erlangung des akademischen Grades eines Doktors der technischen Wissenschaften von

Dipl.-Ing. Bernhard Lutzer, BSc

Matrikelnummer: 0725386
Emil-Kralik-Gasse 5/35
1050 Wien

An der Technischen Universität Wien
Fakultät für Elektrotechnik und Informationstechnik
Institut für Festkörperelektronik, E 362

unter Leitung von

O. Univ. Prof. Dr. phil. Emmerich Bertagnolli
und
Univ. Ass. Dipl.-Phys. Dr. techn. Ole Bethge

Wien, im Oktober 2016

Unterschrift

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Kurzfassung

Substrate mit einer hohen Ladungsträgermobilität sind ein Schlüssel im Fortschritt der Halbleitertechnologie und ihrer weiteren Skalierung. Mehrere Kandidaten für neue Substrate werden derzeit untersucht, u.a. Materialien wie Germanium oder III-V-Halbleiter sowie 2D-Schicht-Materialien wie Graphen. Silizium, welches noch immer das am meisten genutzte Halbleitermaterial darstellt, weist bloß eine Elektronenmobilität von 1600 $cm^2\ V^{-1}\ s^{-1}$ sowie eine Löchermobilität von 430 $cm^2\ V^{-1}\ s^{-1}$ auf. Germanium zeichnet sich durch seine hohe Elektronenmobilität von 3900 $cm^2\ V^{-1}\ s^{-1}$ und herausragende Löchermobilität von 1900 $cm^2\ V^{-1}\ s^{-1}$ aus. Das innovative Material Graphen besitzt eine Elektronenmobilität von bis zu 200.000 $cm^2\ V^{-1}\ s^{-1}$, allerdings stellt die Prozessintegration von Graphen in übliche Siliziumproduktionslinien ein kritisches Problem dar, da hochqualitative Graphenschichten bis heute ausschließlich durch Exfoliation von Graphenflocken aus Graphit herstellbar sind.

Es wäre wünschenswert, die Mobilität in Silizium (oder in einem Siliziumkanal) zu steigern, um etablierte Prozessschemata der Silziumhalbleiterfertigung bewahren zu können. In ihrem Artikel [*Physical Review Letters* 104.24 (2010)] behaupten Kim u. a. die Existenz von fast masselosen Elektronen an der Grenzfläche zwischen Silizium und Metallfilmen. Sie zeigten mittels winkelaufgelöster Photoelektronenspektroskopie, dass ein Band mit fast masselosen Elektronen (fast 20 mal leichtere effektive Masse m_e als in Bulk-Silizium) und linearer Dispersionkurve erscheint, sobald eine Monolage Metall auf eine Si(111)-Oberfläche abgeschieden wird. Das Auftreten von fast masselosen Elektronen in solchen Strukturen kann durch ein Überlappen von Oberflächenzuständen an der Silizium-Metall-Grenzfläche erklärt werden. Kim u. a. führten auch Simulationen dieses Systems durch, welche in guter Übereinstimmung mit den experimentellen Resultaten

waren. Sie nannten ihr System daher „Graphen-ähnliches Silizum“.

Es wurde bereits von Dragoman u. a. in deren Artikel [*Nanotechnology* 23.30 (2012)]. versucht, einen Hochmobilitäts-MOSFET auf Silizium zu fertigen. Das Resultat ihrer Arbeit, nämlich die Herstellung eines funktionierenden Transistors, erwies sich als wertvolle Grundlage für diese Dissertation.

In der vorliegenden Arbeit werden Schottky-Barrieren (SB) MOSFETs mit mittels Atomablagenabscheidung (Atomic Layer Deposition, ALD) gewachsenen high-k Oxiden entwickelt. Das zugrunde liegende Halbleitermaterial ist Silizium mit (111)-Oberflächenorientierung. Zuerst werden Schottky-Barrieren-Kontakte untersucht und passende Parameter für die Herstellung von FET-Elementen ausgewählt. Das Layout für diese Feldeffekttransistor-Bauelemente wird dahingehend ausgelegt, dass es die Integration von ultra-dünnen (< 5 nm) Metalllagen ermöglicht, die Anzahl der benötigten Lithographieschritte minimiert, die Produktion vereinfacht und eine Testumgebung für weitere Arbeit im Bereich der SB-MOSFETs mit ALD-gewachsenen Oxiden ermöglicht.

Die verwendeten ALD-Prozesse sind das Wachstum von Al_2O_3 (TMA+H_2O als Präkursoren) und Y_2O_3 ($(Cp)_3Y$+H_2O) in einem *Beneq* TFS 200 Reaktor. Der Grund für die Verwendung von high-k ALD-Oxiden liegt in deren exzellenten dielektrischen Eigenschaften, welche eine hohe Oxidkapazität ermöglichen.

Als eine Vorbedingung für die Herstellung von ultra-dünnen Metallschichten werden mehrere Experimente im Zuge dieser Arbeit durchgeführt. *In-situ*-Studien des elektrischen Widerstandes von Dünnschichten während der Bedampfung auf makellose Si(111)-Oberflächen werden durchgeführt und ein passendes Model entworfen, welche die Effekte während dieses Abscheideprozesses erklärt. Ein Anstieg des Widerstands während der Abscheidung der ersten Atomlagenschichten wird gezeigt, der bis jetzt nicht in der Literatur beschrieben wurde.

Weiters werden mit ALD-Oxiden überdeckte dünne Metallschichten mittels Röntgenphotoelektronenspektroskopie (X-ray photoelectron spectroscopy, XPS) charakterisiert, um die Qualität des Materialstapels und eine mögliche Oxidation des Metallfilms während des Prozesses zu untersuchen. Kapazitive Rasterkraftmikroskopie (Scanning Capacitance Microscopy, SCM) wird durchgeführt, wo-

durch neue Eigenschaften an die Oberfläche treten, die einer geänderten Bandstruktur im Siliziummaterial zugerechnet werden. Zusätzlich werden noch elektrische Messungen von MOS-Kondensatoren und MOSFETs gezeigt, welche eine ultra-dünne Metallschicht zwischen Bulk und Gate-Oxid aufweisen. Ein Halbleiterparameteranalysegerät wird verwendet, um die relevanten elektrischen Parameter wie Ladungsträgermobilität zu extrahieren.

Abstract

Substrates with a high charge carrier mobility are a key issue in the progress of semiconductor technology and its further scaling. Several candidates for new substrates are currently investigated, e.g. bulk materials like Ge or III-V semiconductors as well as 2D-layer materials like graphene. Silicon, which is still the predominantly used semiconductor material, has a bulk electron mobility of only 1600 $cm^2\ V^{-1}\ s^{-1}$ and a hole mobility of 430 $cm^2\ V^{-1}\ s^{-1}$. Another well-known semiconductor, germanium, is particularly interesting for its high electron mobility of 3900 $cm^2\ V^{-1}\ s^{-1}$ and its outstanding hole mobility of 1900 $cm^2\ V^{-1}\ s^{-1}$. Graphene with its many innovative applications has a electron mobility of up to 200,000 $cm^2\ V^{-1}\ s^{-1}$, however, process integration of graphene into conventional Si production lines seems to be still a critical issue due to the fact that the graphene layer in devices is produced by exfoliation of graphene flakes from graphite.

It would be convenient if one would be able to increase the carrier mobility in silicon (or in a silicon channel) in order to keep the well-established processing schemes of silicon semiconductor manufacturing. In their paper, Kim *et al.* [*Physical Review Letters* 104.24 (2010)] claimed the existence of nearly massless electrons at the interface between Si and a metal film. They showed by means of Angle-Resolved Photoelectron Spectroscopy (ARPES) that a band with nearly massless electrons (nearly 20 times lighter effective mass m_e than in bulk Si) and a linear dispersion curve emerges if a monolayer of metal is deposited on a Si(111) surface. The appearance of nearly massless electrons in such structures can be accounted to the overlapping of surface states at the silicon-metal interface. Kim *et al.* also made simulations of this system which were in good agreement with the experimentally obtained results. They called their system therefore "graphene-like silicon".

A concept to establish a high-mobility Metal Oxide Semiconductor Field Effect Transistor (MOSFET) on silicon has been already described once in a paper by Dragoman *et al.* [*Nanotechnology* 23.30 (2012)]. The result of their work, namely the manufacturing of a working transistor, proved to be a valuable foundation for this thesis.

In this work, Schottky-Barrier (SB) MOSFETs with Atomic Layer Deposition (ALD) grown high-k oxides are developed, using Si(111) substrates. First, Schottky-barrier contacts are examined, resulting in the selection of suitable parameters for the manufacturing of FET devices. The layouts of these FET devices are designed to enable the integration of ultra-thin (< 5 nm) metal layers, to minimize the number of needed lithography steps, to simplify production and to provide a test-bed for further work in the field of SB-MOSFETs with ALD-grown oxides. The employed ALD processes are the growth of Al_2O_3 (TMA+H_2O precursors) and Y_2O_3 ($(Cp)_3Y$+H_2O) in a *Beneq* TFS 200 reactor. The reasons for using high-k ALD oxides are their excellent dielectric properties which allow a high oxide capacitance.

As a prerequisite for the establishment of ultra-thin metal layers, several experiments are performed within this work. *In-situ* resistance studies of the electrical behaviour of thin films during deposition onto pristine Si(111)-surface are made. A suitable model to explain the effects during this deposition process is developed. A resistance increase effect during the first layers of deposition is described which was not yet shown in literature.

Furthermore, thin metal films coated by ALD oxides are characterized with X-ray photoelectron spectroscopy (XPS) to assess the quality of the material stack and the possible oxidation of the metal film during processing. Scanning Capacitance Microscopy (SCM) measurements are performed which resulted in novel properties attributed to the altered band structure of the silicon material. Additionally, electrical characterizations of MOS capacitors and MOSFETs with an ultra-thin metal between bulk and the gate oxide are shown. Using a semiconductor parameter analyser, all relevant electrical parameters like the charge-carrier mobility are extracted.

Für Bianca

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Contents

1. Introduction

1.1. Motivation

The technology of microelectronics evolved rapidly in the last six decades since the invention of the first integrated circuit by Jack Kilby in 1958 [1] which yielded him the Nobel prize in the year 2000. The primary goal until today in microelectronics is to make the basic elements of integrated circuits like transistors smaller and smaller to be able to put more logical elements on each wafer and on each dice, therefore either allowing higher computing power or a reduction of the price. Modern smartphones in the year 2016 have roughly computing powers like high-end desktop processors in 2008 but use much less power while being also much cheaper.

Moore's law, first formulated in 1965 [2], says that the number of transistors per area doubles every year. 10 years later it has been reformulated to predict a doubling every two years. Gordon Moore, an engineer at Intel, therefore forecast the development of a whole industry for the next 40 years. Only in the last years, this law doesn't hold up any more, now in 2016 we are at a rate of every two and a half year as the shrinking of logical elements of an integrated circuit is slowly approaching fundamental physical limits.

The International Technology Roadmap for Semiconductors (ITRS) [3] is a prognosis about the foreseen development of the semiconductor industry. It forecasts and anticipates the technology of future semiconductor devices, e.g. by stating values for certain parameters, and is regularly updated to account to technological changes or two readjust the goals if it becomes clear that they were too optimistic. One of the parameters which are discussed in the ITRS is the logic

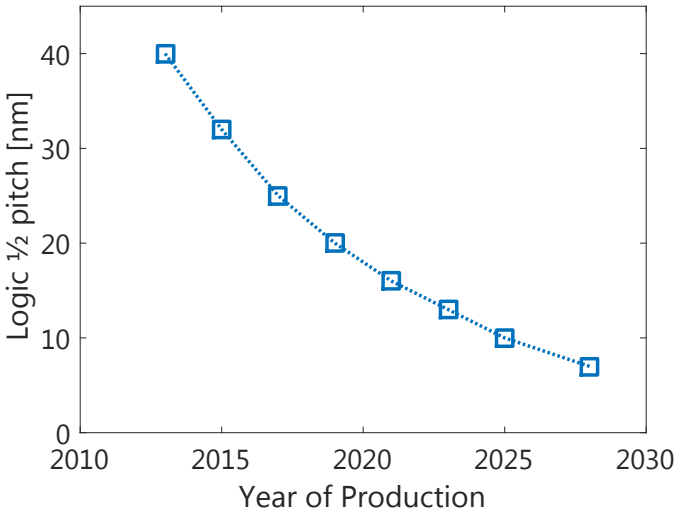


Figure 1.1.: The prediction of the ITRS 2013 for the logic half pitch of CMOS structures in the years to come [3]

half pitch width, see figure 1.1.

The physical limit of the feature size is reached when only one atom works as a switching element, a concept which has been already shown [4].

The reduction of the feature size of CMOS technology until they approach this physical limit is discussed by scaling theories, see e.g. D. Frank *et al.* in [5]. There, α is defined as a dimensional scaling parameter. Scaling the device size by α leads e.g. to a voltage reduction by $1/\alpha$ or a doping density change by α. It is clear that if the dimensional factor gets too large, the dependent parameters of the FET approach physically impossible limits.

Another issue is the trade-off between leakage current and Equivalent Oxide Thickness (EOT) [6]. Silicon dioxide (SiO_2) was used for decades in semiconductor industry. While this was a very reasonable choice for bigger feature sizes, now the low relative dielectric constant (known as k, κ or ϵ_r) of silicon dioxide has become a problem as the gate oxides have become so thin (in order to achieve high capacitance densities even with the low k-value of silicon dioxide) that the leakage current is too large. This was first discussed in 1997 by Lo *et al.* [7]. The solution which has been proposed and which is already in use are high-k oxides which are defined by a k-value > 3.9, which is the one of silicon dioxide.

Furthermore, the channel (and bulk) material of future devices may also change.

Here, silicon was also a choice which lasted for decades (even though it was not the first used semiconductor). As the main advantage of silicon (from a physically point of view, not an economical one) was its high-quality oxide and its electrical mobility, with the need for other, non-native oxides it became an opportunity to switch also to other semiconductor materials like Ge or III-V materials.

1.2. Aim of this work

Although other semiconducting materials with higher intrinsic mobilities exist (e.g. Ge), it would be be of interest if one would be able to increase the mobility of silicon (or produce a high-mobility Si channel) in order to keep the well-established processing schemes of silicon semiconductor manufacturing. In their paper, Kim *et al.* [8] claimed the existence of nearly massless electrons[1] at the interface between Si and a metal film. By means of Angle Resolved Photoemission Spectroscopy (ARPES), they showed that a band with nearly massless (nearly 20 times lighter than in bulk Si) and linear dispersion emerges if a monolayer of metal is deposited on a Si(111) surface. Kim *et al.* also made simulations of this system which where in good agreement with the experimentally obtained results. They called their system therefore "graphene-like silicon".

This concept to establish a high-mobility MOSFET on silicon has been already tried once in a paper by Dragoman *et al.* [9]. Even though they realised the manufacturing of a working transistor, the results could be optimisable.

1.3. Background

1.3.1. Silicon and Germanium

Silicon has been the favourite material for the semiconductor industry in the last 50 years, although the first bipolar transistor was manufactured by using germanium in 1947 [10] (the FET is even older). Silicon has the huge advantage of

[1] The effective mass of charge carriers is inversely proportional to the mobility

its abundance in the Earth's crust. The raw material is typically silicon oxide, which commonly is called sand. The huge market share of silicon in comparison to other semiconducting materials makes it also widely available by various suppliers and cheap. Unfortunately, some intrinsic physical properties of silicon are only mediocre, e.g. the charge carrier mobility. The mobility μ of charge carriers in the semiconductor is related to the conductivity σ by

$$\sigma = q(\mu_n n + \mu_p p) \tag{1.1}$$

whereat μ_n and μ_p represent the mobility of electrons and holes, while n and p represent the densities of these charge carriers.

If we compare the electron and hole mobilities of silicon with other commonly available semiconducting materials which are listed in table 1.1 it is clear that if the channel mobility becomes an issue the substituion of silicon by other materials like Ge or III-V semiconductors is a viable option. The substitution does not necessarely effect the whole wafers; growing other channel materials on silicon wafers is now a well-established technique [11].

Table 1.1.: Properties of various semiconductors at T = 300 K [12, 13]

	Si	**Ge**	**InP**	**GaAs**	**InAs**	**InSb**
Eff. mass: m_e [m^*/m_0]	0.19	0.082	0.077	0.067	0.023	0.0145
Lattice constant [Å]	5.431	5.658	5.8687	5.65325	6.0583	6.479
Electron Affinity [eV]	4.05	4.0	4.38	4.07	4.9	4.59
E_g [eV]	1.12	0.66	1.35	1.42	0.36	0.17
n_i [cm^{-3}]	1×10^{10}	2×10^{13}	1.3×10^{7}	2.1×10^{6}	1×10^{15}	2×10^{16}
Mobility: e [cm^2/Vs]	1500	3900	4600	8500	33000	80000
h (cm^2/Vs)	450	1900	150	400	300	1250
Melting point: T_m [°C]	1412	937	1060	1240	942	527

The main advantage of germanium are its higher carrier mobilities compared to silicon, with twice the electron mobility compared to silicon (3900 cm^2/Vs compared to 1500 cm^2/Vs) and a fourfold higher hole mobility of 1900 cm^2/Vs, which is higher than any other commonly used material. The problem with this

semiconductor is that ultra-pure germanium which is needed to produce wafers is scarce and therefore expensive. The low melting point of Ge at 937 °C is also a problem for producing contacts by diffusion [14, 15] while the lower bandgap of 0.66 eV increases leakage currents for bulk-Ge devices.

Another class of semiconducting materials (either as a bulk or as a channel material) are 2D materials like graphene [16], silicene [17] or MoS_2 [18]. All these are currently (2016) very hot topics in material science as they have mobilities which are order of magnitudes (e.g. up to 200 000 $cm^2\ V^{-1}\ s^{-1}$ for graphene on SiO_2 [19]) larger than of traditional semiconducting materials like Si.

1.3.2. Schottky contacts

If a semiconductor comes into contact with a metal, a so-called Schottky[2] barrier is formed. This barrier exhibits certain properties, e.g. a defined barrier height which controls its rectifying behaviour. A short introduction how the formation of the Schottky barrier happens is given below, it follows [20].

Formation of the Schottky barrier

This description of the Schottky barrier formation considers only ideal interfaces without any surface states (e.g. by adsorbed species on the surface of either the metal or the semiconductor). In figure 1.2, the formation process for both n- and p-type materials is shown. The formation of the barrier is guided by the principle that the Fermi levels E_{Fm} and E_{Fn} or E_{Fp} in both materials must line up, which bends the valence and conduction bands in the semiconductor as the Fermi level in a metal is fixed. This is because as they connect, a flow of electric charge from the semiconductor into the metal will happen to achieve thermal equilibrium.

The change in the Fermi level in the semiconductor is described by the difference between the the work function[3] of the metal Φ_m on the semiconductor material and the electron affinity χ of this metal, so for n-type semiconductor Schottky contacts the barrier height Φ_{Bn0} is described by:

[2] Named after the german scientist Walter Schottky.
[3] The work function depends also e.g. on the crystal orientation, not only on the type of element.

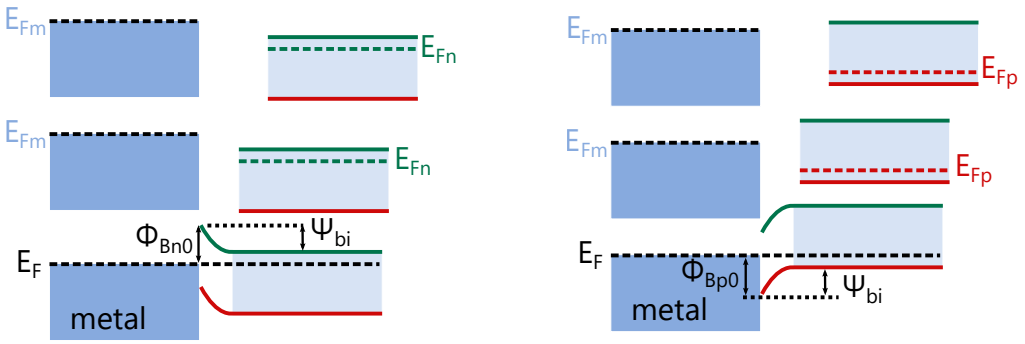


Figure 1.2.: Schematics of the formation of a Schottky barrier contact between a metal and a) n-type semiconductor or) p-type semiconductor

$$q\Phi_{Bn0} = q(\Phi_m - \chi) \tag{1.2}$$

while for the p-type semiconductor Φ_{Bp0} is the band gap E_g minus this difference:

$$q\Phi_{Bp0} = E_g - q(\Phi_m - \chi). \tag{1.3}$$

If we combine these two formulas, we see that the sum of the barrier heights Φ_{Bn0} and Φ_{Bp0} is equal to the band gap E_g of the semiconductor:

$$q(\Phi_{Bn0} + \Phi_{Bp0}) = E_g \tag{1.4}$$

This means that if a metal has a high barrier height with a n-type semiconductor, the barrier height between the same metal and a p-type semiconductor is low, and vice versa. If one needs a contact with a specific barrier height (e.g. for a Schottky rectifier), different metals have to be used to be able to achieve the same Φ_{B0} for both n- and p-type semiconductors.

The work function is defined by the energy difference between the vacuum level and the Fermi level. For a metal it is $q\Phi_m$, while for a semiconductor it is $q(\chi + \Phi_s)$ with $q\chi$ being the electron affinity and Φ_s the Fermi potential from the conduction- (for n-type) or valence-band (for p-type) edge. Table 1.2 lists the work functions in eV for common metals in semiconductor processing. The

so-called built-in potential Ψ_{bi} is furthermore defined as $\Psi_{bi} = \Phi_{B0} - \Phi_s$.

If one applies a voltage on such a metal-semiconductor junction, the band diagrams of the barrier change significantly, as shown in figure 1.3.

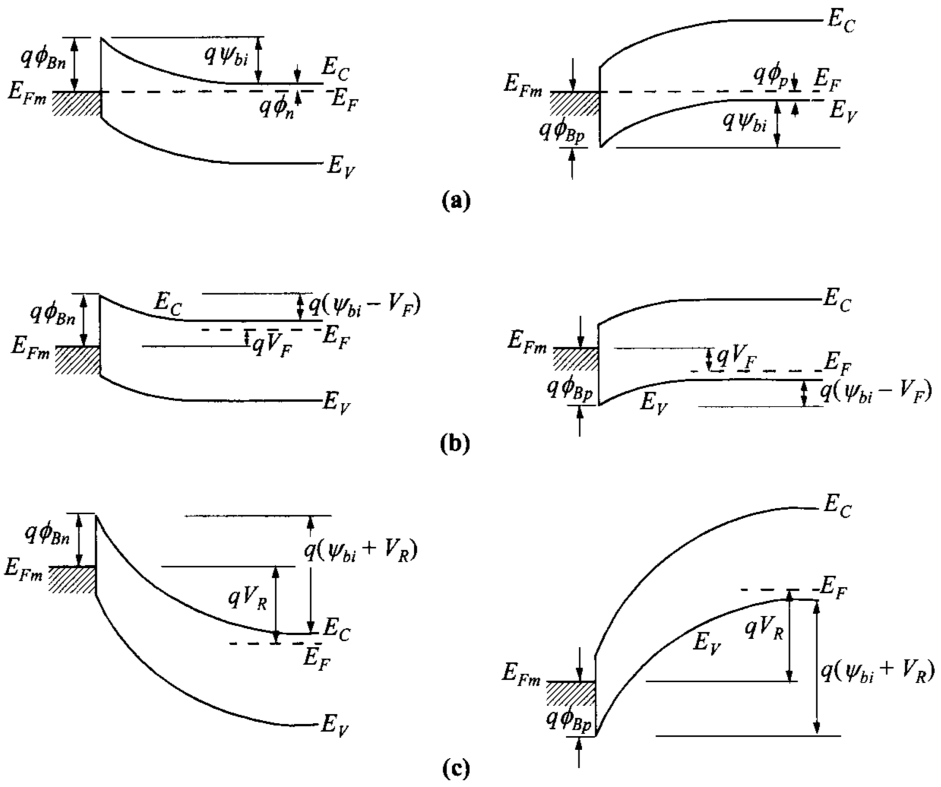


Figure 1.3.: Schematics of the energy-band diagrams of metal on n-type (left) and on p-type (right) semiconductors under different biasing conditions. (a) Thermal equilibrium (b) Forward bias (c) Reverse bias. from [20].

Applying the external voltage leads to the formation of a so-called depletion layer, where the concentration of charge carriers is strongly reduced. The width of this layer W_D is given by

$$W_D = \sqrt{\frac{2\epsilon_r\epsilon_0}{qN_D}(\psi_{bi} - V)} \tag{1.5}$$

with V being the bias voltage, ϵ_r the relative permittivity of the semiconductor (e.g. for Si 11.9), ϵ_0 the permittivity of the vacuum, N_D the doping density, k the Boltzmann constant and T the temperature.

This description ignores, as already stated, all non-ideal effects. If we follow

Table 1.2.: Work function of various metals used for contacts to semiconductors (data from [21])

Metal	χ [eV]	Metal	χ [eV]	Metal	χ [eV]
Ag	4.52–4.74	Nb	3.95–4.87	Ta	4–4.8
Al	4.06–4.26	Ni	5.04–5.35	Ti	4.33
Cr	4.5	Pt	5.12–5.93	V	4.3
Mo	4.36–4.95	Rh	4.98	Y	3.1

this theory, one would be able to compute the schottky barrier height directly by use of extensive tables of materials properties. Unfortunately this holds not true, due to various effects (e.g. Fermi-level pinning) the real Schottky barrier height depends heavily on material pureness, technique of metal deposition (sputtering, evaporation, etc.), residues on the surface, temperature, chemical interaction of the two materials and more. In the excellent article by Tung [22], he explains why the formation of a Schottky barrier is much more complicated than this simple theory here tells us, but in fact there are possibilities to simulate real Schottky junctions.

Current transport through a Schottky junction – Thermionic emission theory

The transport of current through a metal-semiconductor junction is mainly governed by majority carriers, in contrast to pn-junctions where the main role is played by minority carriers. There are five basic current transport processes:

- Thermionic emission
- Tunneling
- Recombination
- Diffusion of electrons
- Diffusion on holes

For the the most common semiconductor silicon as well as for germanium the so-called thermionic emission theory describes the current-voltage of a Schottky

junction adequately. In order to derive it, one has consider three assumptions:

- The barrier height should be much higher than the thermal energy $q\Phi_{Bn} \gg kT$
- Thermal equilibrium
- Existence of two superimposed current flows, one into and one out of the semiconductor, which do not influence each other

First we derive the current density from the semiconductor to the metal $J_{s\to m}$ which is given by

$$J_{s\to m} = \int_{E_{Fn}+q\phi_{Bn}}^{\infty} q v_x dn \tag{1.6}$$

which describes the electrons which have sufficiently high enough energy to overcome the barrier and move into the x-direction. $E_{Fn} + q\phi_{Bn}$ is the minimum energy to achieve this, so it acts as the lower integration limit while v_x is the velocity in x-direction. In the incremental energy range dn the electron density is

$$dn = N(E)F(E)dE \tag{1.7}$$

$$\approx \frac{4\pi(2m^*)^{3/2}}{h^3}\sqrt{E-E_C}\ \exp\left(-\frac{E-E_C+q\phi_n}{kT}\right)dE \tag{1.8}$$

with $N(E)$ being the density of states and $F(E)$ the distribution function.

Under the assumption that the whole electron energy in the conduction band is of kinetic nature we get

$$E - E_C = \frac{1}{2}m^* v^2 \tag{1.9}$$

$$dE = m^* v dv \tag{1.10}$$

$$\sqrt{E-E_C} = v\sqrt{\frac{m^*}{2}}. \tag{1.11}$$

After substitution of eq. 1.9–1.11 into eq. 1.7 we get

$$dn \approx 2\left(\frac{m^*}{h}\right)^3 \exp\left(-\frac{q\phi_n}{kT}\right) \exp\left(-\frac{m^* v^2}{2kT}\right)(4\pi v^2 dv) \tag{1.12}$$

which denotes the number of electrons per unit volume that have a velocity between v and $v + dv$ in all directions. The quadratic velocity of those electrons is determined by the sum of the quadratic velocities in each dimension

$$v^2 = v_x^2 + v_y^2 + v_z^2 \tag{1.13}$$

thus this results in

$$\begin{aligned} J_{s\to m} &= 2q\left(\frac{m^*}{h}\right)^3 \exp\left(-\frac{q\phi_n}{kT}\right) \int_{v_{0x}}^{\infty} v_x \exp\left(-\frac{m^* v_x^2}{2kT}\right) dv_x \cdot \\ &\quad \cdot \int_{-\infty}^{\infty} \exp\left(-\frac{m^* v_y^2}{2kT}\right) dv_y \int_{-\infty}^{\infty} \exp\left(-\frac{m^* v_z^2}{2kT}\right) dv_z \\ &= \left(\frac{4\pi q m^* k^2}{h^3}\right) T^2 \exp\left(-\frac{q\phi_n}{kT}\right) \exp\left(-\frac{m^* v_{0x}^2}{2kT}\right) \end{aligned} \tag{1.14}$$

by using $4\pi v dv = dv_x dv_y dv_z$. To enable an electron to overcome the barrier, it needs a minimum velocity of v_{0x} in x-direction. This kinetic energy is equal to $q(\psi_{bi} - V)$:

$$\frac{1}{2} m^* v_{0x}^2 = q(\psi_{bi} - V) \tag{1.15}$$

If we substitute this into the former term for $J_{s\to m}$, we result in

$$J_{s\to m} = \frac{4\pi q m^* k^2}{h^3} T^2 \exp\left(-\frac{q\phi_{Bn}}{kT}\right) \exp\left(\frac{qV}{kT}\right) \tag{1.16}$$

which is equal to

$$J_{s\to m} = A^* T^2 \exp\left(-\frac{q\phi_{Bn}}{kT}\right) \exp\left(\frac{qV}{kT}\right) \qquad with\ A^* = \frac{4\pi q m^* k^2}{h^3} \tag{1.17}$$

The parameter A^* is the so-called effective Richardson constant, measured in $Am^{-2}K^{-2}$. It can be found in literature for various semiconductor surfaces, as it depends on the material, on the crystallographic direction (e.g. 100 or 111) as well as on other properties. It can be calculated, but unfortunately, the Richardson constant cannot always be taken from literature for a given Schottky barrier as it may be different for a real junction [23–25]. Measured and calculated values for many common semiconductors as well as further theory about the Richardson constant are found in [26].

Since the barrier height for electrons moving from the metal into the semiconductor remains the same under bias, the current flowing into the semiconductor is thus unaffected by the applied voltage. It must therefore be equal to the current flowing from the semiconductor into the metal when thermal equilibrium prevails (i.e., when V = 0). This corresponding current density is obtained from Eq. 1.17 by setting V = 0,

$$J_{m\to s} = -A^* T^2 \exp\left(-\frac{q\phi_{Bn}}{kT}\right) \tag{1.18}$$

thus the total current density yields

$$J_n = \left[A^* T^2 \exp\left(-\frac{q\phi_{Bn}}{kT}\right)\right]\left[\exp\left(\frac{qV}{kT}\right) - 1\right] \tag{1.19}$$

$$J_n = J_{TE}\left[\exp\left(\frac{qV}{kT}\right) - 1\right] \tag{1.20}$$

1.3.3. Metal Oxide Semiconductor capacitors (MOS)

The Metal Oxide Semiconductor (MOS) capacitor, a special case of the Metal Insulator Metal (MIM) capacitor, is the most versatile and useful device for studying semiconductor surfaces [20]. It consists of a semiconductor substrate, a thin oxide layer (down to only a handful of monolayers in recent technology) and a top metal contact. This structure is also the main ingredient in the fabrication of a MOSFET.

To measure such an structure, an additional backside ohmic contact to the bulk is needed, which is used together with the top electrode to characterize the capacitor by CV measurements with an applied bias voltage. Figure 1.4 shows such a structure and figure 1.6 a prototypic CV-curve of a MOSCAP.

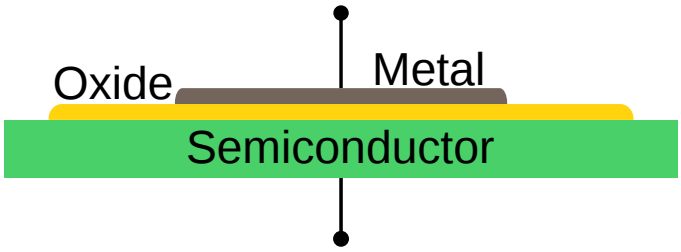


Figure 1.4.: The schematic of a MOSCAP

Depending on the bias applied to this device, one can identify in a C(V)-curve three distinctive regions: Accumulation, Depletion and Inversion [27]. These can be seen in figure 1.8.

- **Accumulation:** Beneath the gate an accumulation of free electrons occurs. This means that the measured capacitance is only determined by the oxide capacitance, which is used to extract the thickness of the oxide or the dielectric constant.
- **Depletion:** The region beneath the gate, formerly in accumulation filled with free electrons, begins to be depleted of free electrons. This widens the space charge region (scr) following in a decrease of the capacitance. At some point the silicon bulk will be completely free of electrons, which should be (theoretically and with a proper band alignment of the top electrode) at about 0 V. The voltage where this occurs is the flat band voltage

and can be related to the position of the capacitance drop in figure 1.6. Its shift from the nominal value is an indicator for charges in the oxide.

- **Inversion:** In the inversion region holes beneath the gate begin to accumulate. Actually, it takes some time after applying the voltage for the capacitor to go into inversion. First it is driven into deep depletion where it slowly relaxes into inversion.

The band diagram of a MOSCAP in flatband condition can be seen in Figure 1.5.

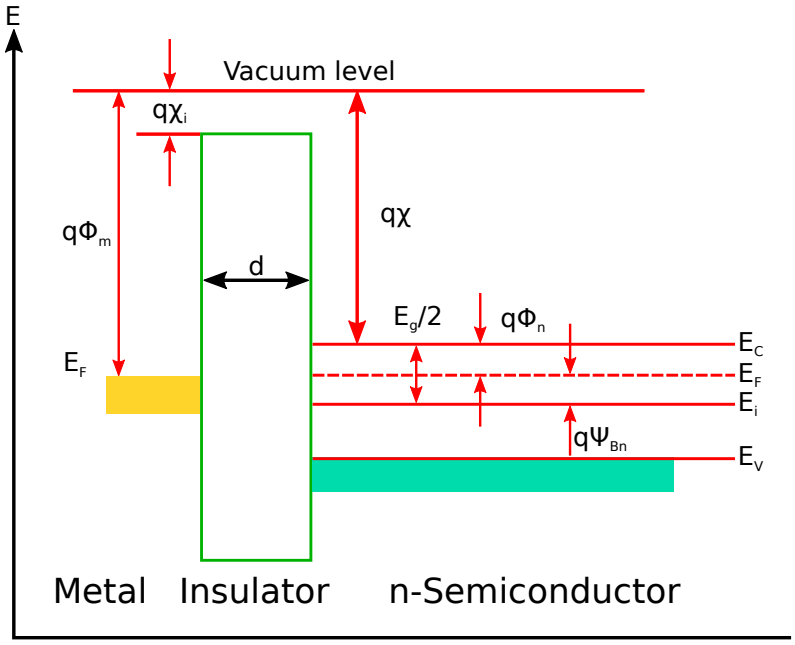


Figure 1.5.: Schematic of the band diagram of an MOS structure on a *n*-type semiconductor in flatband ($V_{bias} = 0$) condition

The flat band voltage can be theoretically calculated by

$$V_{FB} = \phi_m - \phi_s = \phi_m - \left(\chi + \frac{E_g}{2q} - \psi_{Bn}\right) \quad \text{for } n\text{-type} \tag{1.21}$$

and

$$V_{FB} = \phi_m - \phi_s = \phi_m - \left(\chi + \frac{E_g}{2q} + \psi_{Bn}\right) \quad \text{for } p\text{-type} \tag{1.22}$$

whereat ϕ_m and ϕ_s are the work functions of the gate metal and the semiconductor. ϕ_s is defined by the electron affinity χ and half the bandgap divided by the unity charge $E_g/2q$ while ψ_{Bn} (the position of the Fermi level in the semiconductor) depends on the doping level by

$$\psi_{Bn} = \frac{kT}{q} ln\left(\frac{N_A}{n_i}\right) \tag{1.23}$$

with N_A being the doping concentration and n_i the intrinsic charge carrier concentration. The CV curves of capacitors can be simulated by programmes which also include defect influences [28].

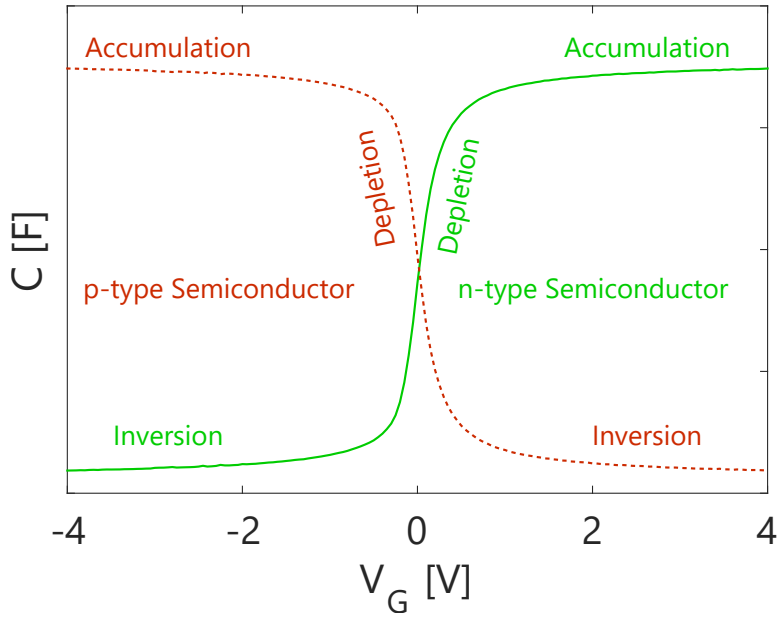


Figure 1.6.: Typical C(V)-curves of a MOS capacitor for both doping types, showing the accumulation, depletion and inversion for both

The shape of the CV-curve in Figure 1.6 only applies for high-frequency measurements. If one measures at a lower frequency or by a quasistatic capacitance measurement method, the resulting CV curves look different, see Figure 1.7 for a comparision.. Measuring the differetial capacitance at a low frequency, the thermal equilibrium of the charge carriers is always maintained, that means that the measurement is slow enough to allow recombination of charge carriers resulting in a symmetrical CV curve. Measuring at a high frequency with a small signal capacitance measurement, the measurement is too fast for the charge carriers

to follow so that an inversion layer is able to form [27], thus reflecting only the small movement of the inversion layer and the charge variation in the depletion layer. In this context, "low" and "high" frequency depend on the semiconductor and its intrinsic mobility of the charge carriers. While silicon may show a high frequency behaviour down to lower frequencies (in the order of a couple of kHz), germanium on the other hand would already behave like being measured quasistatically at the same frequencies.

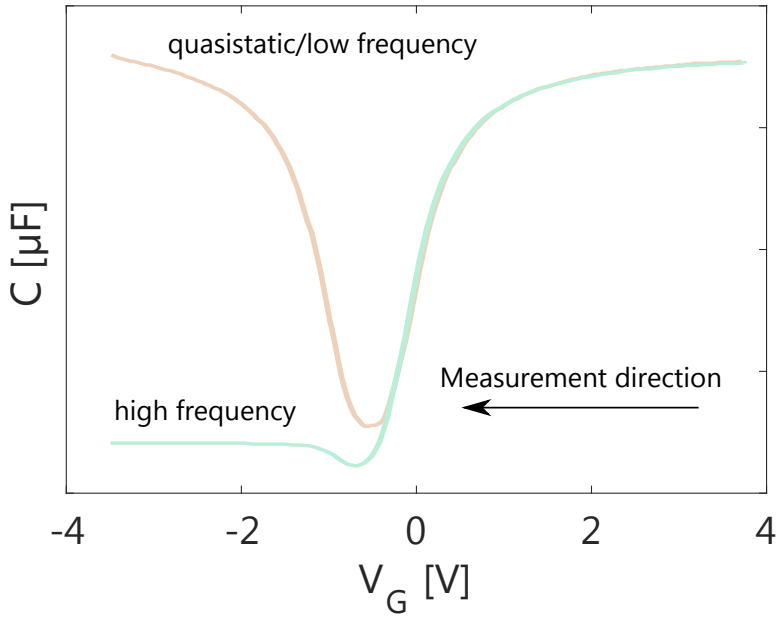


Figure 1.7.: CV response curves of a MOSCAP either measured in the quasistatic/low frequency regime (red) or in the high frequency response regime (green)

As one would prefer normally a $V_{FB} = 0$, the work function of the gate metal ϕ_m should be aligned with the work function of the semiconductor ϕ_s.

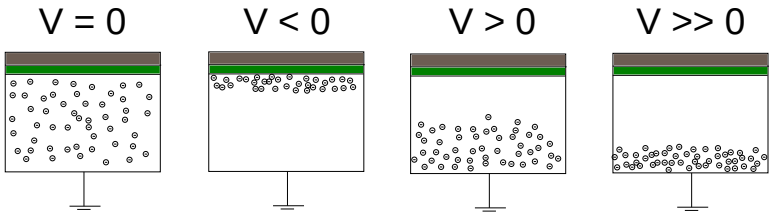


Figure 1.8.: Schematic of the MOSCAP accumulation, depletion and inversion

There may be defects at the semiconductor/oxide interface which affect the behaviour of the MOSCAP. There are three main defects which can occur [29]:

- Fixed charges in the oxide

- Mobile charges in the oxide
- Surface states at the oxide/semiconductor interface

Fixed charge which occur in the oxide shift the flat band voltage. It is caused by introduced ions in the oxide during growth/deposition or by further processing.

Mobile charges also reside in the oxide, but are mobile inside the oxide if subjected to electric force, which leads to a hysteresis of the CV-curve, depending if one measures from positive to negative bias voltage or vice versa. Some ions like sodium tend to act as mobile charges in oxides.

Surface states distort the CV curve because as the Fermi level in the interfaces changes the occupancy of those states (also called traps) changes as well, leading to a less abrupt transition or a distortion of the CV curve.

All these defects are tried to be minimized during production as those affect the properties of MOSFETs produced with gate stacks. The location of these traps in a schematic of a MOSCAP can be seen in figure 1.9, the corresponding effect on the CV-curve in figure 1.10.

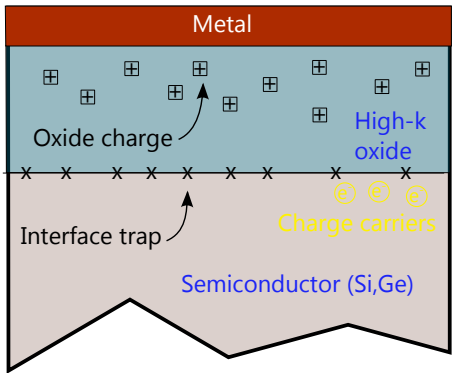


Figure 1.9.: Schematic of the traps in an oxide-semiconductor stack

The observed flat band voltage V_{FB} differs from the ideal voltage V'_{FB} without charge or trap effects by

$$V_{FB} = V'_{FB} - \frac{Q_i}{C_{ox}} - \frac{1}{\epsilon_{ox}} \int_0^{t_{ox}} \rho_{ox}(x) x dx \tag{1.24}$$

whereat the effects of charges at the oxide-semiconductor interface are represented by $\frac{Q_i}{C_{ox}}$ and effects of the the charge density in the oxide by $\frac{1}{\epsilon_{ox}} \int_0^{t_{ox}} \rho_{ox}(x) x dx$.

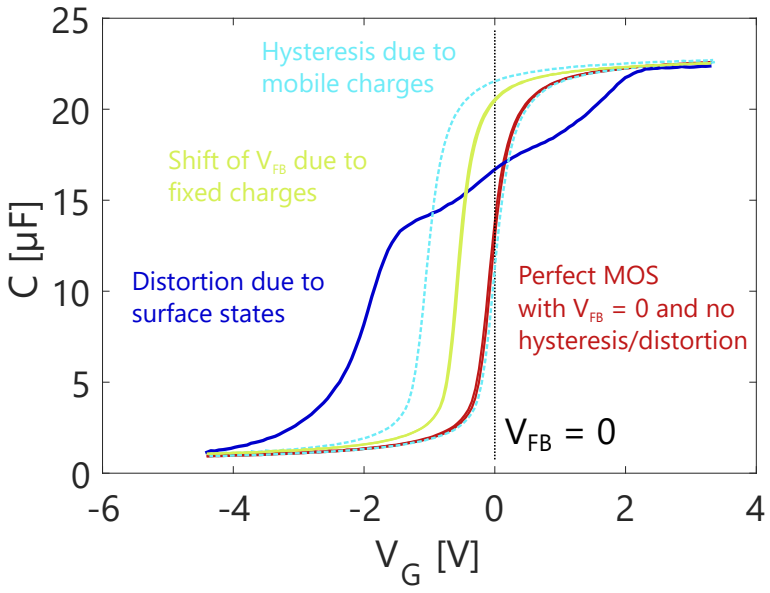


Figure 1.10.: Impact of different defects on the shape of the CV curve of a MOSCAP

1.3.4. Metal Insulator Metal Capacitor (MIM)

MIM (Metal Insulator Metal) capacitors are used typically for the integration of capacitive structures into integrated circuits. They differ to MOS capacitors by the second metallic electrode which is between the oxide and the bottom semiconductor material, see figure 1.11.

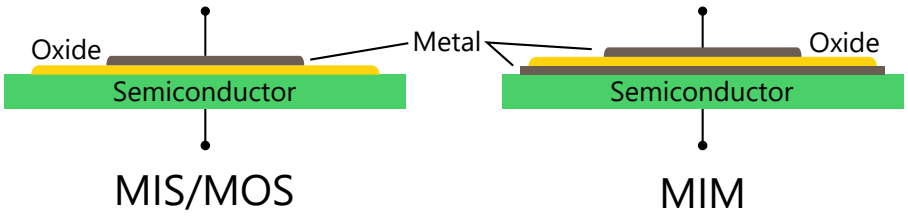


Figure 1.11.: Comparision of a MOS/MIS with a MIM capacitor structure

They can be described as a parallel-plate capacitor where effects of a possible underlying semiconductor substrate are negligible. The capacitance of a MIM capacitor can be ideally described by

$$C = \epsilon_0 k \frac{A}{d} \tag{1.25}$$

As one can see, high-k materials are also advantagageous here [30]. In reality, non-linear effects in the dielectric material cause a deviation of the capacitance

based on the applied bias voltage, described by

$$C = C_0(\alpha V^2 + \beta V) \tag{1.26}$$

Further material about MIM capacitors can be found in [31].

1.3.5. Field Effect Transistor (FET)

The Field Effect Transistor (Field Effect Transistor (FET)) and its most widely produced variety, the MOSFET, is of utmost importance for modern integrated circuits as it is the main active device in processors or (as with a different design, the double floating-gate MOSFET) as memory in computer devices. As modern processor and memory chips are produced in orders of billions per year and each of them contains billions of single FET devices, humanity produces (by a rough estimation) about $1 \cdot 10^{18}$ units per year which makes the FET by far the most produced active electronic device in history.[4]

The FET is part of the bigger family of transistors, in which the other big group are potential-effect transistors (PET) like a pnp/npn-junction transistor. The channel where current flows through is controlled capacitively, while for PETs the potential of the channel is controlled directly. This results in the advantage that FETs are controlled virtually powerless (the gate current is very small compared to the source-drain-current) while for PETs some power is needed to switch them. Furthermore, FETs have a negative temperature coefficient, which means that with rising temperature the current through the channel decreases which is a crucial feature for integrated circuits.

The invention of the MOSFET is attributed to Lilienfeld [32] and Heil [33] in the 1930s. These were actually invented before the first PET was manufactured in the Bell Labs in the 1940s, but become only commercially relevant in the 60ies.

The term Complementary Metal Oxide Semiconductor (CMOS) describes a family of semiconductor devices, where MOSFETs, both n and p-channel, are used to construct logical circuits like inverters or NOR/NAND gates [34].

[4] The resistor is probably the most produced passive electronic device.

Depending on the channel material and the voltage which has to be applied on the gate we distinguish 4 types of field-effect devices. First, the bulk material can be either n- or p-doped, which means the channel (where the bulk minorities are the main charge carriers) is p or n dominated. This leads to the designation "NFET" and "PFET", where N and P denote the charge carriers in the channel, not the doping type of the bulk. Additionally, FETs can be produced (at least in theory) in two ways. The first is that the FET for a gate voltage V_G of 0 V is in the "off" state, this is what we call "normally-off". On the other hand, there are also devices which for $V_G = 0$ are in the "on" state, called "normally-on". From these two properties we can list the four main types of FET devices:

1. Normally-on PFET
2. Normally-on NFET
3. Normally-off PFET
4. Normally-off NFET

Although we mostly see a FET as a three terminal device with source, drain and bulk, most commonly it is treated as a four terminal device were the back contact to the bulk is the fourth terminal.

A classical MOSFET schematic is seen in figure 1.12. Here all four terminals are highlighted as well as the channel width and channel length which are important as they play a crucial role in how much current a FET is able to conduct. The channel length L is also the main factor in miniaturisation of integrated circuits.

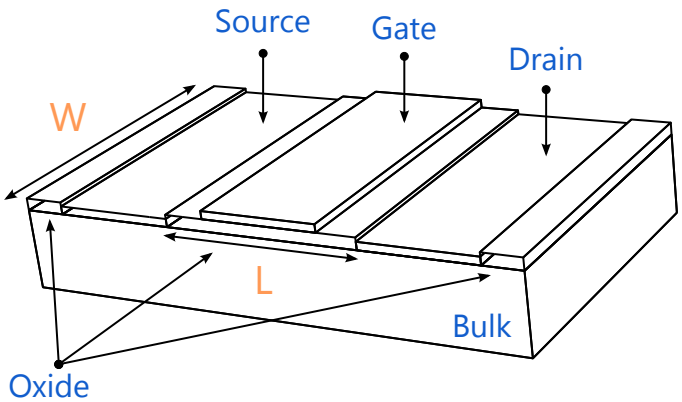


Figure 1.12.: The schematic drawing of a MOSFET with source, gate, drain and bulk shown. The width and length of the channel are also highlighted in the drawing.

The drain current I_D which flows between the source and the drain of a MOSFET in the linear region is described by (without derivation, see [20])

$$I_{DS} = \frac{W}{L}\mu C_{inv}\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right) \quad \text{for } V_D < (V_G - V_T) \tag{1.27}$$

whereat I_D denotes the drain current, W and L the channel length and width, respectively, μ the channel mobility, C_{inv} the gate inversion capacitance, V_G the gate voltage, V_T the threshold voltage and V_D the voltage across the channel (from source to drain, the source is considered in this formula to be at ground potential).

In figure 1.13, the I_{DS} versus U_{DS} and I_{DS} versus U_{GS} graphs off a normally-off NFET are shown. In figure 1.13b, the linear and saturation regions can be seen.

Important for this work is the reduction of the mobility by interface traps at the oxide/semiconductor junction. The relation between mobility and interface traps is described by (see [35, 36])

$$\mu_{inv} = \frac{\mu_0}{1 + \alpha N_{scat}} \tag{1.28}$$

whereat N_{scat} is described by the integral of the interface trap density D_{it} over the relevant energy band:

$$N_{it} = \left| \int_{E_i}^{E_f} D_{it} dE \right|. \tag{1.29}$$

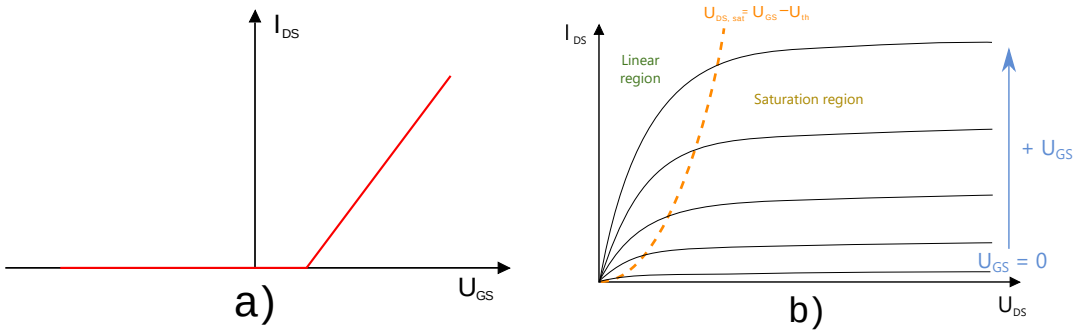


Figure 1.13.: Characteristics of a NFET

1.3.6. Mobility in Field Effect Devices

As mentioned before, the mobility of the charge carriers relates to the conductivity of a semiconductor. The most basic definition of the mobility is that it relates between the electric field $\vec{E}$ and the drift velocity $\vec{v}$ of a charge carrier

$$\vec{v} = \mu \cdot \vec{E} \tag{1.30}$$

Without scattering of the electrons and holes which leads to a loss of momentum this equation would not be valid, as the acceleration in the electric field would not stop, so $\vec{v}$ would not reach a defined (although statistical) value. A well-known theory describing the impact of scattering on the resistance is the Drude model, where the a linear relationship between the current density $\vec{J}$ and the electric field $\vec{E}$ is given by

$$\vec{J} = \left(\frac{nq^2\tau}{m}\right)\vec{E} \tag{1.31}$$

where τ is the mean free time between scattering events.

These scattering mechanisms rely on lattice vibrations (phonons), impurities, other carriers, surfaces, and other material imperfections. In figure 1.14, the three main processes are shown.

Each scattering mechanism affects the mobility on its own. Therefore the mobility defined e.g. by the scattering on the lattice μ_{lattice} and e.g. by the scattering on an impurity μ_{impurity} have to be combined to an effective, measurable mobility. This can be done by the so-called Mathiessen's rule [37], which is

$$\frac{1}{\mu} = \frac{1}{\mu_1} + \frac{1}{\mu_2} + \cdots \tag{1.32}$$

whereat μ denotes the effective mobility and μ_1, μ_2, and so forth denote the single scattering mechanism mobilities.

In equation 1.27, it has been already shown that the drain current of a FET devices depends on μ. Hereby μ denotes the mobility of the charge carriers (mi-

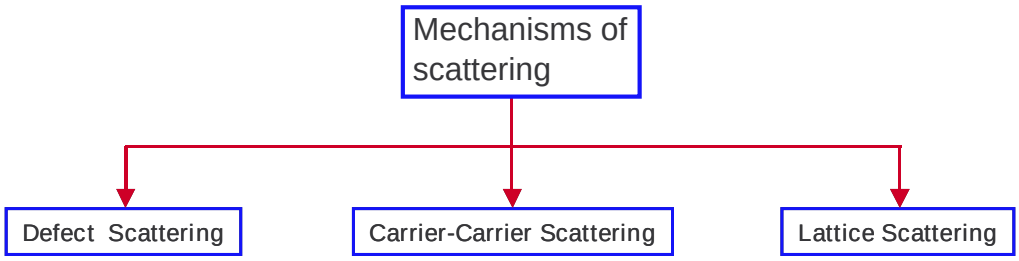


Figure 1.14.: The three main mechanisms of scattering which lead to a decrease of the charge carrier mobility μ

norities) in the FET channel. If for example the interface between semiconductor material of the channel and the oxide is not of a high quality, it leads to scattering which reduces the mobility and subsequently also the current I_{DS} through the channel.

Another important implication of the mobility of a FET is its behaviour in the interplay with high-frequency (microwave) signals. The charge has to travel very fast through the channel to ensure that high-frequency signals can be regulated by a FET. For this reason, ultra-high frequency application FETs are typically made of III-V materials like GaAs. The cut-off frequency f_T for a MOSFET is defined by [38]

$$f_T = \frac{\mu(V_{GS} - V_T)}{2\pi L^2} \tag{1.33}$$

and shows the linear relationship between the channel mobility and the high-frequency behaviour of a FET.

1.3.7. SB-MOSFET

The vast number of produced MOSFET devices are provided with doped source/drain regions. Beyond that, it is also possible to use metal-semiconductor Schottky contacts for the source and drain regions for a MOSFET, hence called Schottky Barrier MOSFET. These rectifying junctions of Schottky junction have transport properties similar to pn junctions, but the underlaying physical effect is different (see section 1.3.2). The behaviour of these SB-MOSFETs is similar to normal pn-

junction devices, but they offer a couple of advantages, e.g. in device scaling[39] or reduced parasitic resistance of the contacts compared to doped contacts.

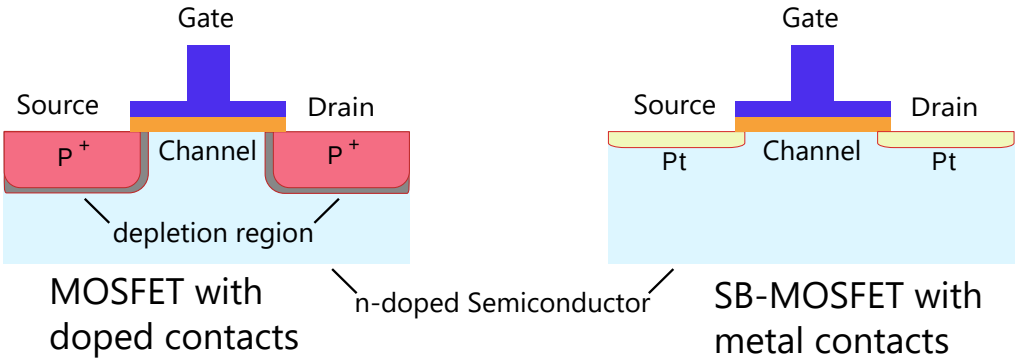


Figure 1.15.: Comparision of a MOSFET with doped S/D regions and a SB-MOSFET with metal contacts

One of the first SB-MOSFETs were produced by Nishi *et al.* [40] and Leptselter *et al.* [41].

Important for a proper operation of the SB-MOSFET is the Schottky barrier height of the contacts. For a SB-PFET (n-doped semiconductor bulk), one needs a metal contact with a high barrier height $\phi_{B,e}$ for electrons and a low barrier height for the minority carriers of the channel (holes) $\phi_{B,h}$. As already mentioned in section 1.3.2, these two conditions are fulfilled simultaneously, as the sum of both barrier heights is the band gap of the semiconductor. Examples for good metal contacts to n-doped semiconductors are noble metals like Pt while for a NFET with a p-doped bulk rare earth metals are a reasonable choice [42].

To decrease the parasitic resistance or alter the barrier properties, metal-semiconductor compounds can be formed. In the case of silicon, those are called silicides, in case of germanium, germanides. Typically, they are formed by deposition of the metal and a subsequent temperature annealing [43].

1.3.8. High-k materials

To manufacture a MOSFET, an oxide is needed. As silicon was (and still is) the most favourable semiconducting material in CMOS FET devices in the last 50 years [44], the oxide of silicon SiO_2 was a very natural and well-performing choice. The growth of high-quality silicon dioxide is easily done by either dry or

wet-oxidised silicon wafers or by other methods like PECVD or ALD. Silicon oxide is also thermally stable up to temperatures far above 1000 °C and has a large band offset to the silicon conduction and valence band, respectively. Additionally, it shows a large bandgap of 8.9 eV [45]. To reach the full bandgap of SiO_2 only about two monolayers are needed [46] while 0.7 nm thickness are sufficient for an oxide layer to reach the same properties as bulk [47]. A big disadvantage of SiO_2 is its low k value of only 3.9 [45] which prohibits further scaling of FET devices because a minimum thickness of 0.7 nm SiO_2 is needed in order to achieve reasonable low leakage currents [48].

The specific capacitance of the gate oxide is a factor in formula 1.27 which shows that a possible increase in the specific capacitance (by a higher k value) would lead to a higher drain current, improving the electrical properties of the FET. The capacitance density C' is related to the thickness d and the relative dielectric constant by this well-known formula of the parallel plate capacitor:

$$C' = \epsilon_0 \frac{k}{d} \tag{1.34}$$

with ϵ_0 being the vacuum permittivity of 8.854×10^{-12} F/m.

One idea how to replace silicon oxide as the gate insulating material was silicon nitride (Si_3N_4) with a dielectric constant of about 7 [49], however the leakage current remains an issue for this type of gate insulator [47].

Hubbard *et al.* investigated the thermodynamic stability of binary and tertiary oxides by means of using tabulated thermodynamic data in their highly cited paper [50]. Since then, a handful of possible candidates for oxides which are suitable as gate oxides have emerged, namely ZrO_2, HfO_2, Y_2O_3, La_2O_3. Other high-k dielectrics have the disadvantage of low band gap for example TiO_2, Ta_2O_5 or (Ba,Sr)TiO_3, see table 1.3 for the corresponding values of the band gap and relative dielectric constant.

The EOT is a widely used quantity in semiconductor industry [45] which denotes the thickness of a oxide used as comparison (almost exclusively SiO_2 with k = 3.9 as silicon oxide is the most widely used oxide in the industry) which is needed to achieve the same specific capacitance as a capacitor with a different

Table 1.3.: Properties of various high-k oxides (from [45])

Material	k	Bandgap [eV]	Crystal structure
SiO_2	3.9	8.8	amorphous
Si_3N_4	7	5.1	amorphous
Al_2O_3	9	8.7	cubic
Y2O3	15	5.6	cubic
ZrO_2	25	5.8	monoclinic, tetragonal, cubic
HfO_2	25	5.7	monoclinic, tetragonal, cubic
La_2O_3	30	4.3	hexagonal, cubic
Ta_2O_5	26	4.3	orthorombic
TiO_2	80	3.5	tetragonal

oxide (e.g. Y_2O_3). It is calculated as following:

$$EOT = t_{high-k}\left(\frac{k_{SiO_2}}{k_{high_k}}\right) \tag{1.35}$$

For example, if a process uses a 5 nm layer of Y_2O_3 (k ≈ 15), one would need a 1.3 nm (5 nm x 3.9/15 = 1.3 nm) thick SiO_2 layer instead if the same capacitance density had to be achieved. Literature reports EOT values down to the sub-nm range [51–53].

The reduction of the EOT is one of the problems which have to be addressed in the successful integration of high-k oxides. Murto *et al.* list in their paper [55] four main challenges in integrating high-k oxides:

1. Scaling to lower EOT
2. High defect densities
3. Gate voltage threshold shifts with a resulting need for metal gates
4. Channel carrier mobility loss with high k oxides

One issue that has to be considered in the surface passivation of the underlying semiconductor. While for silicon this passivation with SiO_2, either native or formed during the oxide deposition process, is mostly sufficient, for other bulk

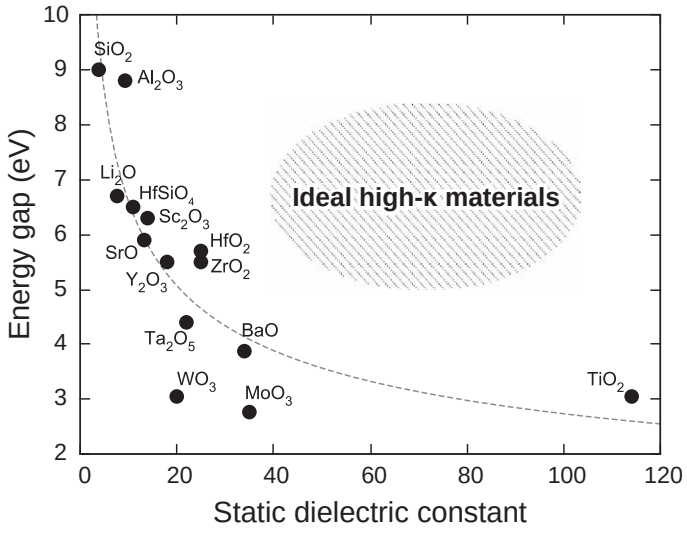


Figure 1.16.: The experimental band gap and dielectric constant for well-known oxides with the ideal property region for materials in the upper right part of the figure. Image taken from Yim *et al.* [54]

materials like Ge this still poses a problem [56]. The quality of this passivation can be measured in a interface trap density, see section 1.3.3.

1.3.9. Atomic Layer Deposition (ALD)

Working principle

To produce very thin layers as gate oxides the so-called Atomic Layer Deposition (ALD) technique handles the requirements needed very well. It offers superior properties by means of

- Uniformity
- Conformity
- Thickness controllability (monolayer by monolayer)

Atomic Layer Deposition belongs to the wide range of Chemical Vapour Deposition (CVD) methods which typically employ gaseous precursors to grow thin films in the order of micro- to nanometres. They distinguish themselves from Physical Vapour Deposition (PVD) by the formation of films by chemical reactions instead of the mere adsorption of atoms/molecules which describes PVD.

Table 1.4.: Properties of various deposition techniques [57]

Method	ALD	MBE	CVD	Sputter	Evap	PLD
Thickness uniformity	good	fair	good	fair	fair	fair
Film density	good	good	good	good	fair	good
Step coverage	good	poor	varies	poor	poor	poor
Interface quality	good	good	varies	poor	good	varies
Low temperature deposition	good	good	varies	good	good	good
Deposition rate	varies	poor	good	good	good	good
Industrial applicability	good	varies	good	good	good	poor

ALD was invented independently by two research groups in Finland and the Soviet Union in the 1970ies, in Finland by the group of T. Suntola [58] (then called "Atomic Layer Expitaxy - ALE") and in the Soviet Union by V. B. Aleskovskii [59] (called молекулярное наслаивание - МЛ, roughly in English "molecular layering - ML"). The first application was the production of electroluminescence (EL) displays which were widely used before the upspring of LCD technology. The first commercially used EL display was used at Helsinki International Airport [60]. The application of ALD as an alternative for Molecular Beam Epitaxy (MBE) was also tried by Goodman and Pessa [61] but did not found a wide impact in the semiconductor field.

The foundation of Atomic Layer Deposition lays on this four main steps which describe one so-called ALD cycle [60]:

1. Inflow of the first precursor, self-terminating reactions on the surface until complete surface coverage is reached
2. Purge with inert gas to remove unreacted precursors and/or byproducts
3. Inflow of the second precursor, reaction with the first one on the surface to form the desired thin film atom/molecules layer
4. Another purge to remove again unreacted precursors and/or byproducts
5. Return to first step for the next layer

A schematic of one ALD cycle can be seen in figure 1.17, where the growth

of hafnium oxide (HfO_2) is shown from Tetrakis(ethylmethylamido)hafnium(IV) (TEMAHf) and water (H_2O) which is also described later in this chapter.

If this these cycles are repeated, one can grow thin films which are extremely well defined in terms of thickness as in ALD the so-called growth per cycle (GPC) is constant. For various reasons (e.g. steric hindrance [60]), growth of one monolayer per cycle, thus a GPC which is equal to 1, has not been observed yet. The GPC is a very typical figure describing an ALD process at certain parameters and is typically estimated by means of ellipsometry (for transparent films), profilometry or AFM [62].

Here, only ALD processes with two precursors are shown. ALD can be made more complex by e.g. employing more precursors and pulsing them alternatively or by a certain pattern allowing the deposition of mixed-oxides films or doped layers [63–65].

The two other main features where ALD excels are, as mentioned, uniformity and conformity. This is caused by the fact that the adsorption of the precursors material is ideally self-limiting and non-directional. This distinguishes ALD from other deposition methods where uniform and conformal deposition of structured surfaces is not possible. With ALD, very high aspect ratios (AR) can be uniformly coated [66–69].

Another difference of ALD to other CVD processes is the temperature-indepedency of the growth rate (inside a certain range) [70]. Figure 1.18 shows the process temperature versus the GPC. In the centre of the figure one can see the so-called ALD process window where the GPC does not depend on the temperature [71]. If the temperature is outside the window, one of the four mentioned processes can happen which influence the ALD deposition process.

The energy for the reaction is typically drawn from the temperature of the sample surface and the chamber, called thermal ALD. Other ALD chemistries have negative heats of reaction, thus by reacting spontaneously, they allow deposition even at room temperature [71]. There are other methods like Plasma-ALD [72] where the activation energy comes from an induced plasma above the sample.

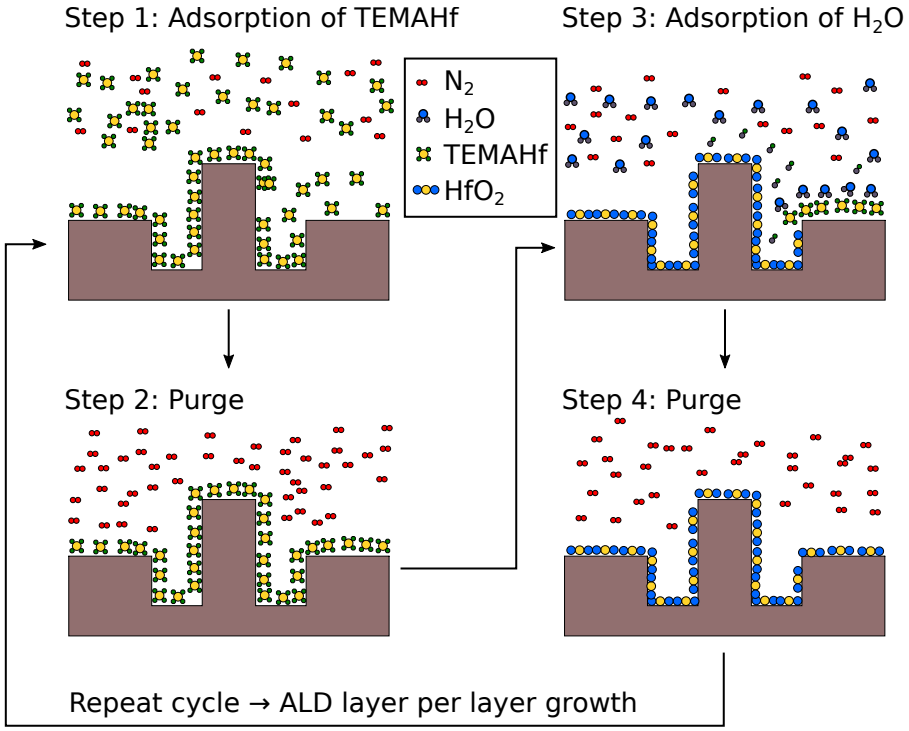


Figure 1.17.: Schematic of the ALD process cycle for the deposition of hafnium oxide, using TEMAHf and water as precursors.

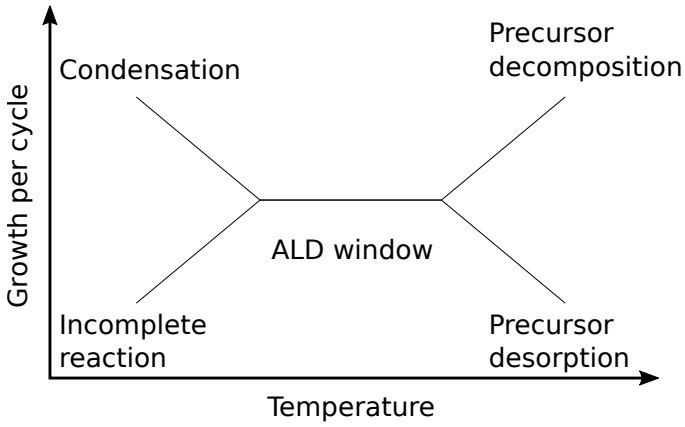


Figure 1.18.: Schematic of the ALD process window [71]

Precursor processes

In the history of ALD (at least on the Finnish side of history), the first used materials for ALD as precursors were pure elements and not compounds [73], namely zinc (Zn) and sulfur (S) to form zinc sulfide (ZnS). This has approach has a couple of drawbacks, especially the disadvantage that many elements have to be

heated to quite high temperatures to achieve suitable vapour pressures. Therefore the switching to compounds which contain the desired element has been made rather quickly in the history of ALD. A precursor should have a suitable vapour pressure at a certain pressure and should be thermally stable (so it does not decompose prematurely). Unfortunately, many precursors are not stable in air (either because of the oxygen or water content of air), some even ignite themselves in ambient atmosphere.

An overview of available precursors and processes for ALD is given in [74], table 1.5 sums this paper up.

Table 1.5.: List of precursors and possible materials with ALD, after [74]

(a)	(b)
Precursor materials	Possible materials
Elemental	Elemental (e.g. Pt, W, Ta, Ni, Cu)
Halides	Oxides (e.g. Al, Y, Zr, Cr)
Alkyls	Nitrides
Cyclopentadienyls	Sulfides
β-diketonates	Other compounds (e.g. Tellurides, Selenides)

The Atomic Layer Deposition processes used in this work are described later in section 2.2.

The mentioned precursors have only explained one half-reaction of the process. To obtain e.g. oxides, an oxidising agent is needed to complete the reaction. Two commonly used substances for this are water (H_2O) and ozone (O_3). The advantage of water is that it has a suitable vapour pressure at room temperature and does not decompose or form any hazard. Therefore it is a very common oxidiser in ALD. The other option is ozone. It is more reactive then water, but has the disadvantage that is has to be produced by UV light from O_2.

1.3.10. X-ray Photoelectron Spectroscopy (XPS)

X-ray Photoemission Spectroscopy (XPS), also known as Electron Spectroscopy for Chemical Analysis (ESCA), was invented by the Swedish physicist Kai Siegbahn in 1956 [75]. It is a powerful surface-analysis technique which allows not

only the determination of the elemental composition down to about 1‰, but also the emperical formula, chemical and electronic state of the first 0.1-10 nm of the measured specimen [76–78].

The basic principle of XPS is to induce the emission of electrons with discrete energies (which are characterized by energy and number, resulting in a energy-counts-diagram) by means of irridation of the sample by X-rays which have sufficently high energies to excite the electrons allowing them to leave the atom. The underlaying physical principle is the photoelectric effect for which Einstein received his Nobel prize [79].

The requirements for a XPS setup are [80]:

- Ultra High Vacuum (UHV) environment
- A controlled source of X-rays
- Means to manipulate the sample (e.g. spatially)
- An analyser for the emitted electrons which carry the XPS information
- A computer to process and store the data

Figure 1.19 shows a prototypic XPS setup. X-rays are produced by an X-ray canon. This source produces X-ray photons by bombarding either a water-cooled Ag or Mg block by electrons. These electrons generated in the X-ray cannon produce mainly heat (99%) while a small portion of the electron energy is converted into X-rays. The X-rays leave the cannon and hit the specimen surface. The penetration depth typically depends on the X-ray energy and has a value of 0.1 nm to 10 nm. It is possible to mechanically turn the specimen by a specified angle which reduces the effective X-ray penetration depth thus allowing destruction-free depth profiling of the first nanometres. This technique is called Angle resolved XPS (ARXPS).

The emitted electrons enter the analyser which consists of a hemispherical setup with two bent parallel plates which discriminate the electrons by their energy. At the end of the hemispherical analyser there is a detector which counts the electrons which pass through the system. The electron energy is sweeped, thus creating an XPS spectra which is a graph showing a count of electrons as a

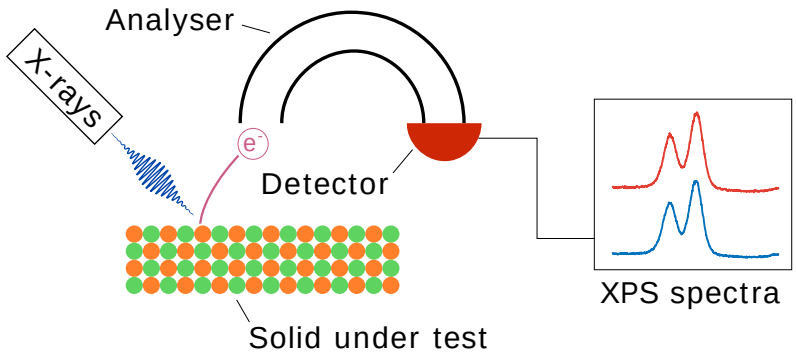


Figure 1.19.: A schematical drawing of the working principle of XPS.

function of energy.

The quantity we are interested in is the binding energy E_b. It relates to the X-ray photon energy and the measured kinetic energy of the electron by

$$E_b = E_{photon} - (E_{kinetic} + \phi) \tag{1.36}$$

whereat ϕ is the work function dependent on both the spectrometer and the material. Basically, this equation describes the conservation of energy.

The work function term ϕ is a rarely-changing constant for each detecting system. It relates to the energy which is lost due to the uptake of the electron in the detector of the instrument.

A prototypical graph with an XPS spectra is shown in figure 1.20b. To get such an XPS graph in practice, a sweep over the whole detectable spectrum[5] of the analyser is made, like in figure 1.20a. This plot contains typically a couple of peaks which emerge from the background noise. From this plot one can identify the elemental composition of the surface (as long as the concentration exceeds the XPS detection limit) by comparing the peak positions with values in a database. In most cases, each element has a bundle of peaks which appear in the graph; their respective height (or to be more precise, the integrated area under the graph) depends on the relative concentration in the specimen and on the cross section of the respective process. In XPS, the most prominent lines

[5]The measured energy ranges from 0 eV to the energy of the X-ray photons, either 1.49 or 1.25 keV for Al and Mg, respectively.

originated typically from the electrons near to the core of the substrate atoms in contrast to techniques like Ultraviolet Photoemission Spectroscopy (UPS) which rather eject valence electrons from the atomic compound.

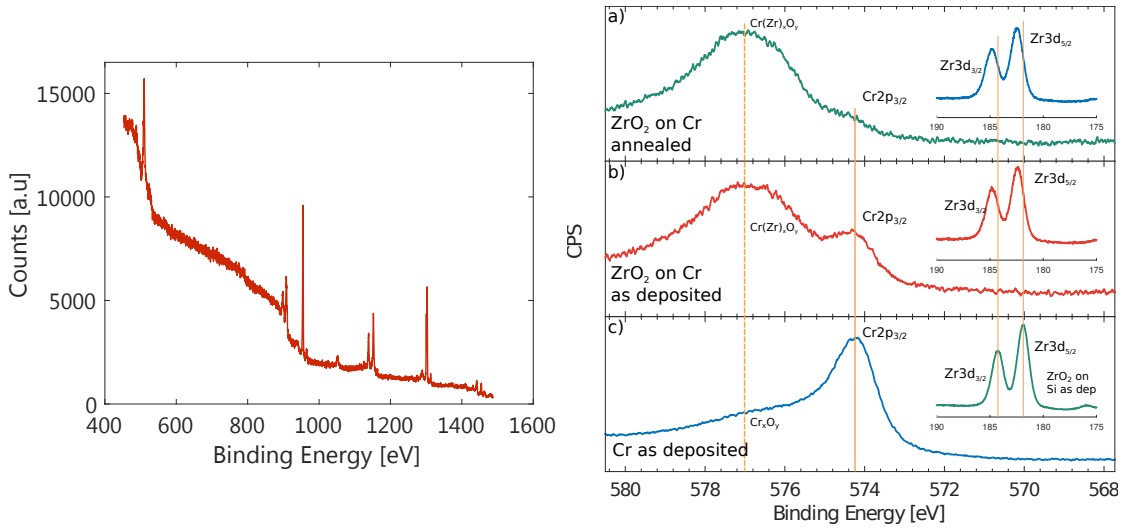


Figure 1.20.: a) XPS overall scan b) A typical graph containing XPS spectra with an overview of the whole spectrum and an inset showing only the Si2p region of the sample

The reason why an atom has more than one peak lies in the atomic orbital model and the electron configuration of each atom. Each measurable XPS peak corresponds to a specific electron in the shell of the atom. For an electron with the quantum numbers n, l and j the notion mostly used[6] is nl_j whereat l is expressed by the s(l=0)–p(l=1)–... notion.

A particular feature of XPS is the ability to get information on the chemical state of an atom. If an atom is part of a molecule, e.g. Al_2O_3, the electrostatic potential of the core electrons is shifted to either higher or lower values, depending if the electrons are attracted or repelled from the atom[7] [81]. The resulting shift can be as high as 3 to 4 eV but mostly it is lower, thus making it very difficult to detect as the Full Width at Half Maximum (FWHM) of most systems is about 1.5-2 eV.

[6]Known as spectroscopist's notion
[7]This corresponds to the oxidation number of the element.

1.3.11. Scanning Capacitance Microscopy (SCM)

Scanning Capacitance Microscopy (SCM), also known as capacative Atomic Force Microscopy (AFM), is a highly sophisticated measurement method based on commercially available AFM equipment [82]. The tip of an AFM is an ideal probe to measure the "local" capacitance of a sample in a very small (~ nm) region around the tip. The tip which scans the surface is connected electrically to an ultra-precise capacitance bridge as well as the backside of the sample.

Three main problems arise in SCM which have to be solved: First, the typical values of the capacitance change ΔC are in the aF region (up to 0.1 aF resolution can be achieved), therefore long integration times, highly shielded setups and ultra-high precision capacitance bridges are needed to allow the discrimination of such minuscule differences in the capacitance. To illustrate this, a simple estimation can be made: As $C = Q/V$ holds, one attofarad corresponds to one attocouloumb per volt. One attocoloumb is about six times the elementary charge, so a change of one attofarad means the movement of only 6 electrons for a voltage of 1 V. Thus it is justified to speak of a "atom-resolution" capacitance measurement.

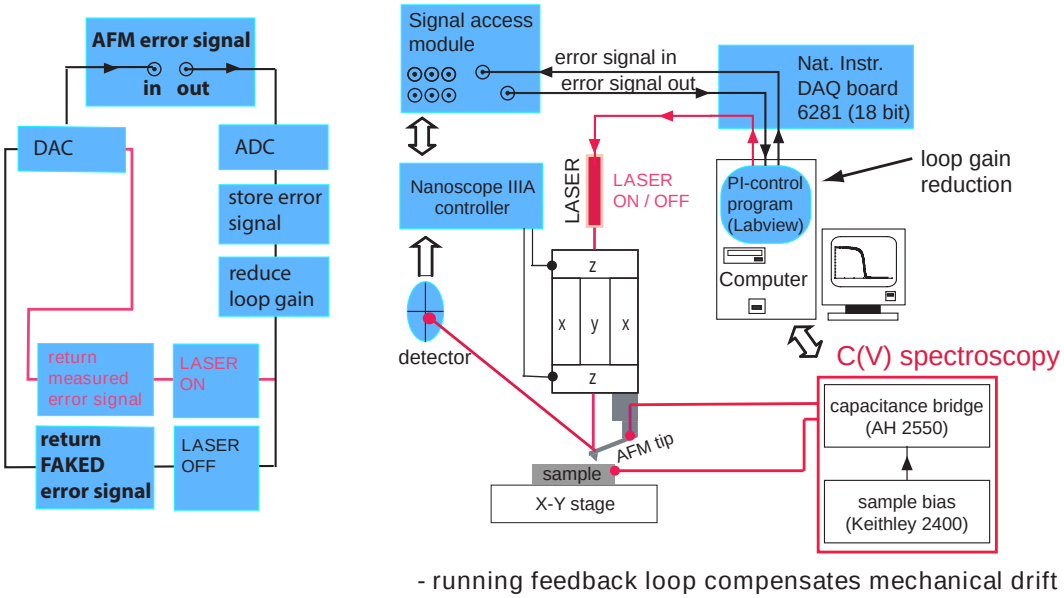


Figure 1.21.: A schematical drawing of the working principle of SCM [83]

Two other issues are the need for a temperature-stabilized enviroment (up to 0.01K/sec) and a customisation of the AFM setup to allow the deactivation of the

laser, which would induce charge carriers and influence the measurement. In [83, 84] such a setup, which was used in this work, is described. A schematic drawing can be found in figure 1.21.

1.3.12. 4-wire measurement method

Later in this work, there will be the challenge to highly accurate measure resistances inside a vacuum chamber. The only possible method of using a ultra-precise Source Measurement Unit (SMU) is to connect rather long (2 m) wires with the sample inside the vacuum, using a vacuum feed-through system. Additonally, the contact resistance of a soldered metal-semiconductor contact is not only non-linear and non-negligible, but also suspected to vary (e.g. by variations in the surface or interface quality). In order to be still being able to measure reliably, the so-called 4-wire measurement method, also known as Kelvin sensing, will be used [85].

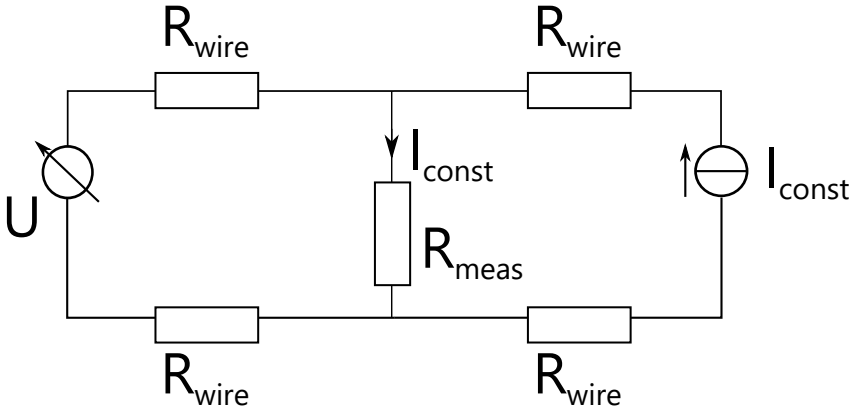


Figure 1.22.: The wiring of a 4-wire measurement of a resistance R_{Meas}, using a constant current I_{const}.

This measurement method, which is schematically depicted in figure 1.22, uses 4 wires as connection between the Device Under Test (DUT) and the SMU. During this measurement procedure, a constant current is supplied by the SMU, passing through the measured resistor with the resistance R_{meas}. The non-avoidable and non-negligible wire (and contact) resistances R_{wire} do not influence the current flow through the measured resistor as the SMU maintains a fixed current, regulating the voltage to achieve this. The other wire pair from the DUT is connected

to the voltage measurement circuit of the SMU. As this circuit has a very huge internal resistance (typically in the order of TΩ for high-precision instruments), the flowing current is very low, which means that the voltage drop caused by the wire resistance is also very low. Thus one is able to determine the true resistance of the DUT by simply applying Ohm's law $R = \frac{U}{I_{\text{const}}}$ with the knowledge that the same specified constant current is flowing through the resistor and that the measured voltage drop is not affected by the wire/contact resistance. This measurement technique is not only limited to a combination of a fixed current and a measurement of the voltage drop, the inverted method of applying a constant voltage and measuring the current is also possible but used less frequently.

2. Experimental

For the design and production of micro- and nanoelectronical devices, many different processing steps are needed which require different tools and recipes. In this chapter, the detailed parameters, recipes, etc. for each step in the processing of a MOSFET or a part of it (e.g. Schottky contacts) are given. Additionally, a description of the electrical characterization and surface analysis of structures is made.

2.1. Formation of Schottky contacts on Si and Ge

2.1.1. Lithography

In this work, the resist AZ 5214E (manufactured by *Clariant*) is exclusively used. This photoresist is intended especially for lift-off processes, where the resist is used for the pattern transfer of sputtered/evaporated films [86], but it may be used for etching purposes as well. In principle, AZ 5214E is a positive photoresist (novolak resin + naphthoquinone diazide as photoactive component), but is intended to be used as a negative resin as a special crosslinking agent is part of the resin which allows the utilisation as a negative resist [87]. This makes AZ 5214E a quite universally utilisable resist for research purposes.

As the first step of a lithography process, some drops of resist are put onto the sample with a syringe filled with undiluted resist until the sample is fully covered. The spinning process is initiated which lasts for 35 seconds at 6000 rpm. According to the data sheet [87], this results in a resist thickness of 1.14 µm. The sample with the resist is then put onto a hot plate (adjusted to 100 °C)

for one minute followed by 30 s at 120 °C to vaporise the solvent of the resist. The sample can now be put into the mask aligner and exposed to UV-light irradiation (4 seconds typically for the MJB3 mask aligner equipped with a 350 W mercury lamp).

To exploit the negative resist functionality of the AZ 5214E, a reverse bake step (60 s at 120 °C) is needed followed by a flood light exposure (without mask) for 8 seconds. After these processes the resist can be developed. For both positive and negative lithography, the sample is put for 70 seconds into an AZ 726 developer, which contains 2.38 % TMAH (tetra methyl ammonium hydroxide) in H_2O, resulting in an alkaline solution. This is followed by two times rinse in deionised water and a subsequent dry-blow with nitrogen.

2.1.2. Sputtering

A great portion of the thin films in this work have been deposited by sputtering, which has the advantage of fast turn-around times as the base pressure needed to operate and produce high-quality thin films is only $2 \cdot 10^{-5}$ mbar and the ability to deposit a wide range of materials by magnetron sputtering [88]. The employed system is a *Von Ardenne* LS320 which operates with argon as sputter gas.

The system allows for up to 6 different targets and 6 different sample holders, although in practice one is left empty as it is needed for chamber and sample cleaning, where the possibility to generate an Argon plasma is used to precondition the sample prior to sputtering. A substrate heater and a reactive gas inlet are also available, but they were not used in this work.

To deposit a metallic layer (e.g. platinum), the target is first cleaned by sputtering on an empty sample holder. This should ensure that surface contamination which may arise from opening the chamber are removed. It is sufficient to sputter only a couple of nanometres of material (also to save precious sputtering material in the case of e.g. gold).

The main disadvantage of the sputtering process in this work is the built-up of protruding side walls if one sputters on patterned samples for lift-off. In figure 2.1 the profile of a nominal 20 nm layer of platinum measured by AFM is shown. The

sputtered layer is more uniform but has the disadvantage of high side walls (also called burrs) while the evaporated layer is free from this problematic feature.

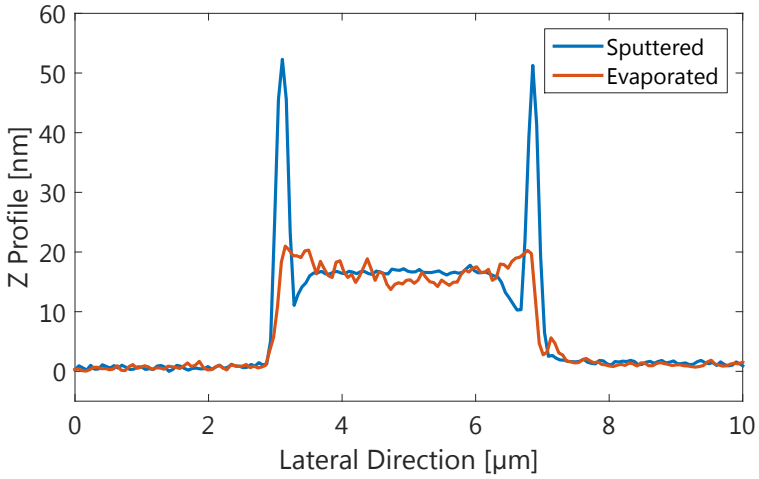


Figure 2.1.: A graph comparing the profiles measured by AFM of sputtered and evaporated platinum layers.

The suspected reason for this kind of problematic behaviour of lift-off of sputtering processes is that the inner walls of the resist are also coated and form those burrs after lift-off, see figure 2.2. Although in theory this should be prevented by the negative side wall angle of the AZ 5214E resist (used in negative resist mode), it seems that the used sputtering processes is able to coat the side walls as well. In positive mode the burrs are very similar, see figure 2.3. Furthermore, backsputtering processes may be possible which are caused by the high energy of the sputtered atoms (in contrast to the low energy atoms which condensate on the surface during e-beam evaporation) which may also support the coating of the side walls and therefore the formation of burrs. The book by Jackson and Schröter [89] also mentions that the lift-off of sputtered metal layers is difficult due to the high adhesion to all surfaces, good conformal coverage of steps and edges and the tendency that sputtered layers are harder than evaporated ones.

It has been tried to remove the burrs to allow the usage of sputtering for all processes (as it is faster because of less stringent requirements for the vacuum), but unfortunately several approaches like changing the resist parameters, the resist or the sputter parameters did not help, therefore e-beam evaporation was the first choice for all metal deposition steps where a subsequent deposition of

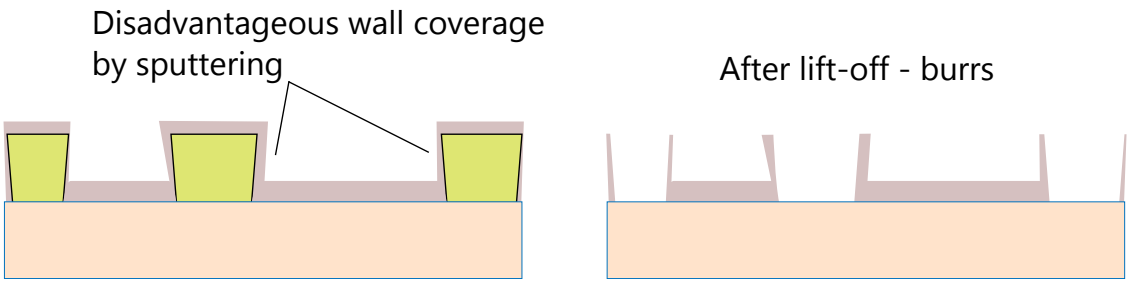


Figure 2.2.: Illustrating the problem of burrs after lift-off of sputtered metal films

an oxide on top of the metal is needed or where short-circuit problems were of concern.

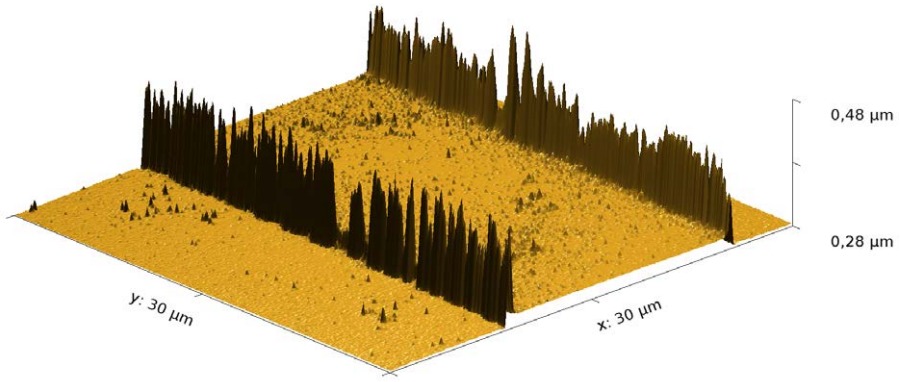


Figure 2.3.: 3D AFM Image of a sputtered nickel film, using lithography with AZ 5214E resist in positive mode

A post lift-off treatment by ultrasonic cleaning of the sample in acetone reduced the burrs slightly but was deemed unsuitable as well for MOSFET production.

2.1.3. E-beam Evaporation

Stand-alone E-beam evaporator

For metal films with higher surface uniformity or without side-walls after lift-off, an e-beam evaporator (*Leybold* L560) has been used. It consists of a vacuum chamber in which four water-cooled evaporation sources are installed. It is possible to deposit multi-layers of different materials by subsequent use of the different evaporation sources. The evaporation source itself is made out of copper to en-

sure high thermal conductivity. To prevent alloying of some materials with the copper there may be the need for liners/crucibles made out of refractive materials like tungsten, molybdenum or aluminium oxide.

The deposition process is monitored by an quartz crystal microbalance which has a resolution of 0.1 Å. This allows the production of thin films in a very controlled manner. Typical base pressures for this machine are in the range of 10^{-6} mbar, but with sufficient pumping time even pressures going down to $1 \cdot 10^{-7}$ may be achieved. To lower the pressure, titanium can be evaporated with closed shutter which acts as a getter material.

E-beam evaporator integrated in the vacuum system

The ALD-XPS system also contains an e-beam evaporator (*Specs* EBE-1) which allows the deposition of various materials from rods and crucibles, although in the course of this work only rods have been used. The deposition can be controlled by monitoring the evaporation current of the charged beam of deposition materials which typically is in the orders of nA. The main advantage of this setup is the possibility of deposition *in-situ* without breaking the vacuum to allow either subsequent ALD or XPS analysis.

2.1.4. Annealing

A Rapid Thermal Annealing (RTA) oven manufactured by *UniTemp* (model UTP 1100) has been used for all temperature annealing processes in this work. It is capable of a precise controlled fast ramp-up up to 75 K/second and a programmable temperature between room temperature and 1000 °C (for a plateau duration of max. 1 minute). The heating is done by infrared lamps. Before the annealing processes, the chamber is evacuated down to about 2 Torr, after which a arbitrarily chosen gas can be let into the chamber (O_2, N_2, forming gas = N_2+H_2, Ar). As this oven is designed to handle wafers, for smaller samples a silicon carrier wafer is used. The spotlessness of the carrier wafer was checked regularly to avoid contamination.

2.1.5. Plasma Oxidation

To remove organic contaminations, for example residual resist after a lift-off process, a plasma oxidation process can be employed to clean the sample. An activated oxygen plasma is used to oxidise the organic residues while keeping the sample unaffected. In this work, a *TePla* 100-E device was employed, see figure 2.4. The sample is put into the device and the vacuum chamber is evacuated to a base pressure of 0.7 mbar. After that, oxygen is let into the chamber and the plasma is ignited by means of RF energy. The sample lies on an isolated podium. After the process (typical processing times 1-15 min), the chamber is vented again and the sample is taken out.

Figure 2.4.: The TePla plasma oxidation device, the right image shows the sample pedestal

2.2. Formation of Al_2O_3, Y_2O_3 and HfO_2 by ALD

The oxides used to form the gate of the MOSFET are grown by the already mentioned ALD technique which allow a precise control of the obtained thin film thickness. In the course of this work two ALD processes were used in order to deposit aluminium oxide (Al_2O_3) and yttrium oxide (Y_2O_3).

The machine employed for the growth of those layers is a *Beneq* TFS 200 ALD reactor (see figure 2.5) which is equipped with three lines for precursors held at room temperature. One of the lines is dedicated to H_2O, the other two are connected to precursor storage tanks. Additionally, two hot-sources which are needed for precursors which need to be heat up to achieve a suitable vapour

pressure for ALD are installed in the machine. Our ALD is equipped with a load-lock system which is connected to the XPS system to allow the investigation of ALD-grown layers by XPS without breaking the vacuum. An option to perform plasma-assisted ALD (PEALD) exists, but was not used in the course of this work.

Figure 2.5.: A Beneq ALD.

Aluminium oxide (Al_2O_3)

Aluminium oxide is one of the best studied processes for ALD [90–92] and has been highly optimised to attain high-quality oxide layers. The deposition process employs tri-methyl-aluminium (TMA) and water as precursors employing the following reaction:

$$Al-OH + Al(CH_3)_3\,(g) \longrightarrow Al-O-Al(CH_3)_3 + CH_4\,(g)$$

$$Al-CH_3 + H_2O\,(g) \longrightarrow Al-OH + CH_4\,(g) \text{ according to [93].}$$

TMA is a highly reactive compound which reacts with water and air and has therefore to be handled in a glove-box with an inert Argon atmosphere. Its constitutional formula can be seen in figure 2.6. In this work, the reaction temperature was 250°C, the pulse and purge times for each precursor are summarised in table 2.1. This process results in a Growth per Cycle (GPC) of 0.151 nm/cycle [31].

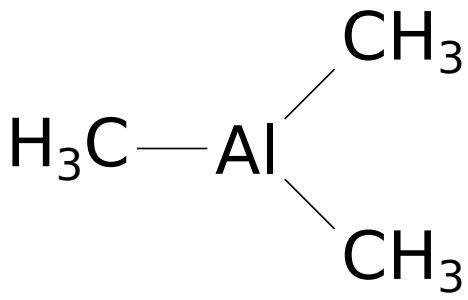


Figure 2.6.: Chemical structure of Trimethylaluminium

Yttrium oxide (Y_2O_3)

Yttrium oxide (Y_2O_3) is a highly attractive material for high-k applications as it has a high permittivity (10-15), a large bandgap (5.5 eV) and a high melting point (2439 °C) [47].

The process used in this work is a combination of Tris(cyclopentadienyl)yttrium(III) or short $(CpY)_3$, see the constitutional formula in figure 2.7, and water (H_2O) [94]. The reactions for this ALD process are too complicated to be shown in a simple chemical reaction, the detailed surface reactions is outlined in [95] where J. Ren *et al.* conducted a DFT study of the surface reaction mechanism of the ALD process forming Y_2O_3. At a temperature of 250 °C, the GPC amounts to 0.15 nm/cycle [96]. The purge/pulse times are shown in table 2.1.

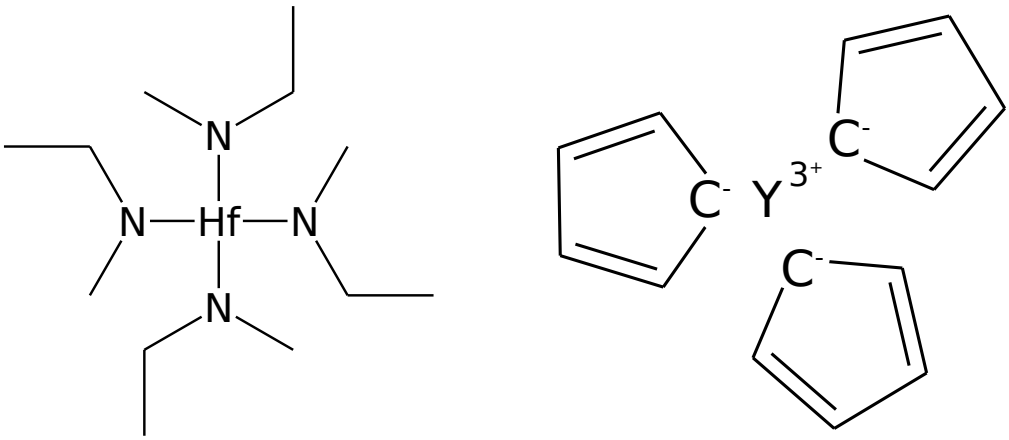


Figure 2.7.: a) Chemical structure of Tetrakis(ethylmethylamido)hafnium(IV) b) Chemical structure of Tris(cyclopentadienyl)yttrium(III)

Hafnium oxide (HfO_2) and zirconium oxide (ZrO_2)

The oxides of hafnium and zirconium [97] have also been investigated during this thesis for the use as a gate oxide due to their high k value, but deemed unfavourable due to reasons of growth rate and interface quality. The used precursors were TEMAHf (Tetrakis(ethylmethylamido)hafnium(IV), see figure 2.7) and TDMA (Tetrakis(dimethylamido)zirconium(IV).

Table 2.1.: Parameters of the various ALD processes used in this work

Oxide	Prec. A	Prec. B	Temp	Pulse A	Purge A	Pulse B	Purge B
Al_2O_3	TMA	H_2O	250°C	0.1 s	0.1 s	0.1 s	0.1 s
Y_2O_3	Cp_3Y	H_2O	250°C	0.1 s	0.1 s	0.1 s	0.1 s

2.3. Pt and Ag metal gate formation

For all SB-MOSFETs discussed in this work, metallic gates have been used as in line with the full metal gate technology which replaced the traditional gate material polysilicon by metals. Polysilicon suffers from a couple of drawbacks, namely polydepletion, boron penetration and high poly sheet resistance [3]. Platinum and silver were used as the gate metal for PFETs and NFETs, respectively. The choice of these two materials was determined by two properties of them:

First, both of them do not form native oxide surface layers in ambient atmosphere which could be insulating and therefore tamper the electrical characterization of the transistors.

Second, the choice of the metal depends also on the work function of the metal[1]. Yeo, King, and Hu formulated in their highly cited paper [98] numeric requirements for the metal gate work function: Metals for PMOS transistors should have a vacuum work function of larger than 5.17 eV while for NMOS the work function should be less than 4.05 eV. The threshold for PMOS is easily achieved

[1] Precisely, not on the vacuum work function which is usually found in tables but on the work function for a specific oxide/metal interface.

by using platinum which has a work function of 5.12–5.93 eV (see table 1.2). For NMOS, the choice for Ag with a work function of 4.52–4.74 eV does not fulfil this condition but is still a reasonable choice because other materials like Ti or Al (which also do not fulfil the condition) readily oxidise and cause the already described problems.

Both platinum and silver were deposited by means of reverse imaging lithography, sputtering (typically 30-50 nm which ensures a material thick enough to be able to be contacted with a probe needle) and lift-off. No temperature annealing step was employed for gate formation.

2.4. SB-MOSFET schematics and production parameters

While recent SB-MOSFETs have a complicated design like described in [99, 100] or with spacers as used in [101], one of the first SB-MOSFETs reported by Lepselter and Sze [41] utilised a design where the FET is realised on a pristine and flat semiconductor surface with no etching processes affecting the bulk materials. This setup is easy to manufacture and allows a quick turnaround in the evaluation of different MOSFET parameters like oxide type, thickness, barrier or similar.

In figure 2.8, the basic design of the MOSFETs investigated in this work is displayed. This layout has been chosen for a couple of reasons. First, as mentioned in the former paragraph, the layout is straightforward and allows both the production of a FET without etching into the semiconductor and a fast turnaround. Furthermore, it makes the integration of an ultra-thin metal layer possible, see section 3.7 for further details.

The dominant feature of this design is the bilayered oxide structure, which is caused by the fact that the first oxide (yttrium oxide) is better suited as a interfacial oxide to the semiconductor silicon, while the second oxide (aluminium oxide) has very good ALD growth characteristics needed to enclose the source/drain contacts to prevent shortcuts between the gate and the source/drain regions. Bi-

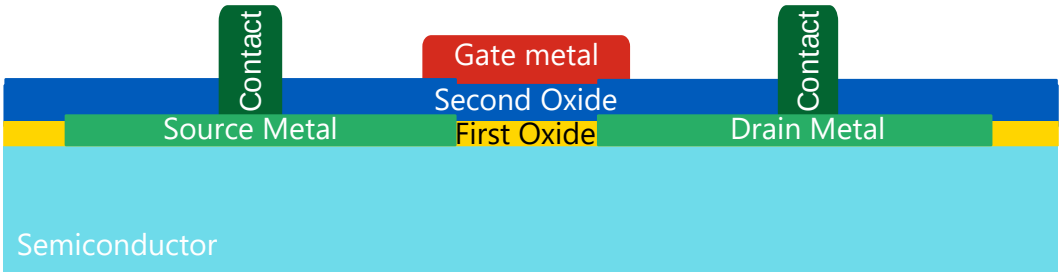


Figure 2.8.: Schematic of a SB-MOSFET with bilayer xide

layered MOSFET structures have been already mentioned in literature, see e.g. the work by Wang *et al.* [102] where a Al_2O_3/HfO_2 bilayered gate stack is shown or the paper by Chang et al. [103], who used Y_2O_3/Al_2O_3 bilayered gate stacks.

This FET structure is not achievable by conventional technology for two reasons: First, conventional processes with SiO_2 involve the bulk-consuming process of Si oxidation which is not the case for CVD methods like ALD for depositing the high-k oxide [48]. Secondly, the uniformity feature which is unique to ALD is exploited for the second oxide.

The principle process flow for the MOSFET involves 14 steps as seen in figure 2.9. It involves a cleaning process, lithographical pattering, ALD, wet etching, sputtering, e-beam evaporation and lift-off processes.

Step 1: Substrate preparation and cleaning

The wafers are taken out of the box and cut by a diamond pencil into pieces of approximately 10x10 mm^2 size. The dust of the cutting process is then blown away by dry nitrogen and the pieces are cleaned by an ultrasonic cleaning bath which employed acetone, isopropanol and water, each for 5 minutes at 100% power. After the last step, the samples were again dry-blown by nitrogen. A dip in BHF has been tried, but was dismissed as it did not improve the characteristics of the resulting MOSFET devices.

Step 2: Deposition of the first oxide by ALD

The samples are then put into the load lock of the *Beneq* ALD system. The first oxide (yttrium oxide) is deposited by a defined ALD recipe, see 2.2 for details. After the ALD deposition process, the samples are taken out and the thickness of the oxide layer is determined by ellipsometry to perform quality control of the

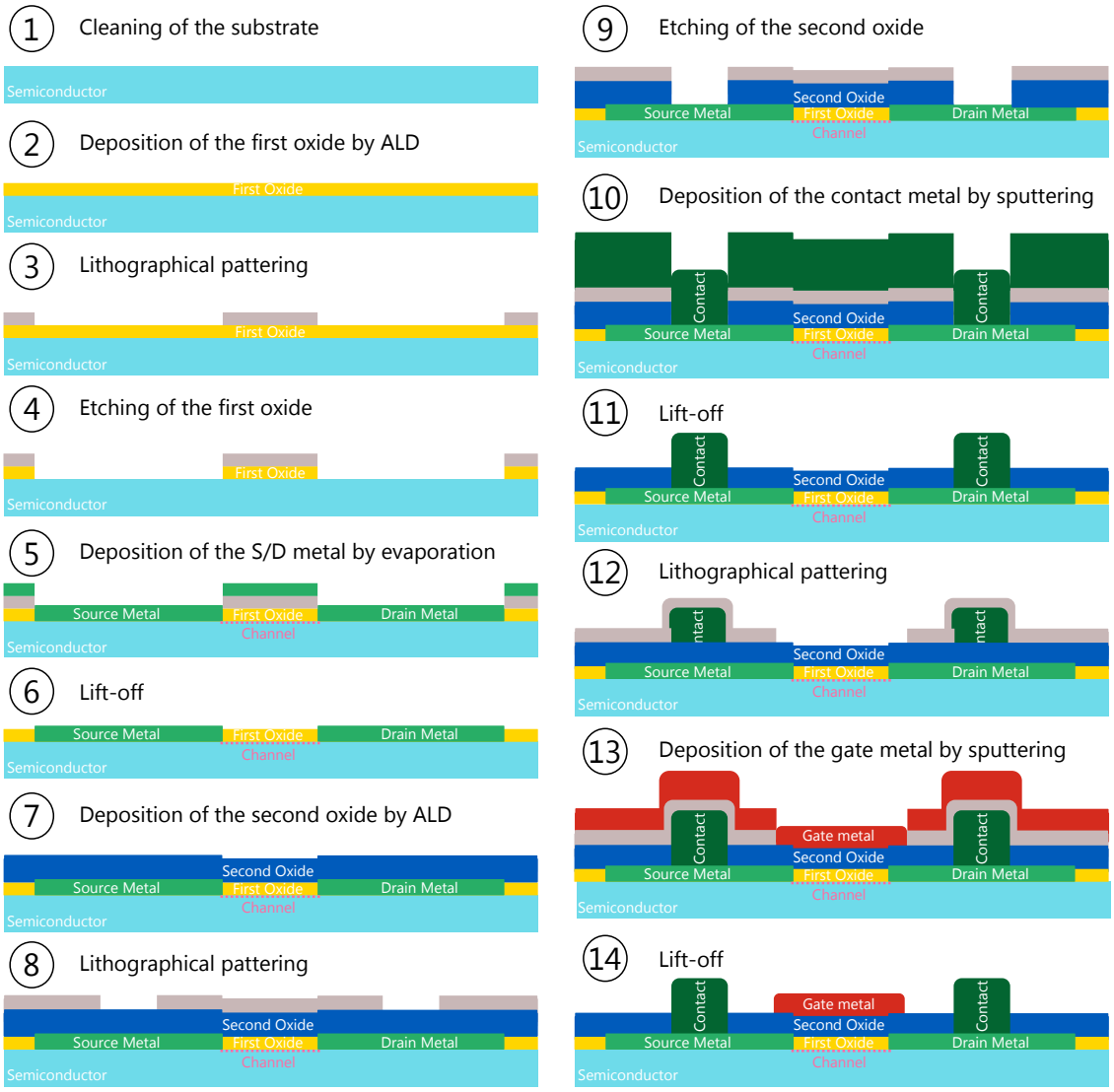


Figure 2.9.: The 14 steps needed to fabricate a SB-MOSFET

growth process.

Step 3: Lithographical pattering for the S/D regions

The semiconductor pieces are lithographically patterned with AZ 5212E photoresist by an image reversal process to allow the selective etching of the yttria to access the semiconductor for S/D formation, see section 2.1.1 for details.

Step 4: Wet etching for the S/D regions

The yttrium oxide is etched with a mixture of 1 part concentrated (36%) hydrochloric acid (HCl) with 9 parts DI water for 90 seconds (for a 5 nm thick yttria

layer, resulting in an etch rate of 3.3 nm/min) to remove the oxide selectively to prepare the sample for S/D contact formation.

Investigations showed that even after a very long HCl etching process (> 5 minutes), the surface is still not hydrophobic so a residual thin layer of SiO_2 is still present. To remove it, a short (5 s) dip into BHF is used to remove this oxide. The removal is checked by the hydrophobicity of the sample.

Step 5: S/D metal deposition by e-beam evaporation

The metal contact to form the source/drain Schottky barrier contact are deposited by means of e-beam evaporation, see 2.1.3. The use of e-beam evaporation was deemed necessary to create metal layers without burrs in the following lift-off step (see the last part of section 2.1.2). Either platinum (for PFETs) or yttrium (for NFETs) has been used.

Step 6: Lift-off of the evaporated metal

After the evaporation of the metal, a lift-off procedure in an ultrasonic bath with low power (30%) for a couple of minutes is done. Sometimes further action in the removal of the unwanted metal is needed to ensure a proper lift-off process, this is done by a special wiping tool. After the successful lift-off, the sample is cleaned by flowing acetone followed by a rinse in isopropanol and water to remove all debris from the lift-off process which may be present. The sample is then blown dry.

Step 7: Deposition of the second oxide by ALD

Before the deposition of the second oxide (aluminium oxide), a plasma-oxidation step is performed, see 2.1.5. The plasma oxidation process is performed with full power (300 W) for 5 minutes, which was deemed enough (10 and 15 minutes have been tried as well, but showed no different effect compared to 5 minutes). It is found out in the course of the work that this pre-deposition step hugely increases the yield of the produced MOSFET devices by preventing short-cuts between the S/D-contacts and the gate metal. This may be caused by two reasons: First, the process probably removes resist residue, the second that it oxidises (and/or) chemically activates the region of the oxide/metal interface, which improves ALD growth.

After this step, aluminium oxide is deposited by a certain ALD recipe, see 2.2

for details. A dummy sample is used to determine and control the thickness of the ALD oxide layer also in this step.

Step 8: Lithographical pattering for the via contacts

Lithographical holes are created which are a prerequisite to form via contacts to the S/D metal through the second oxide.

Step 9: Wet etching for the via contacts

The aluminium oxide is then etched by putting the sample into fresh AZ MIF developer. The developer is a alkaline solution, which contains tetramethylammonium hydroxide dissolved in water, which acts as etchant for Al_2O_3, like other more common alkaline compounds like KOH [104]. The etch time is 10 minutes for 15 nm of oxide, resulting in an etch rate of 1.5 nm/min. The timing with AZ MIF developer as etchant is not very critical, compared to etching by e.g. BHF which as well is possible [104], but is not deemed favourable.

Step 10: Via metal deposition by sputtering

For the via metal deposition, a sputter process (which is much faster than evaporation) was chosen as no problems with shortcuts were expected, see 2.1.2 for a description of the sputtering process. The chosen metal in both cases (PFET and NFET) is platinum because of good resistance against oxidation and low resistivity. The thickness of the platinum was around 100 nm to allow a connection with needles without difficulties.

Step 11: Lift-off of the sputtered metal

As in step 6.

Step 12: Lithographical pattering for the gate metal

Again, a lithographical pattering process is used to prepare the sample for gate metal deposition.

Step 13: Gate metal deposition by sputtering

The gate metal is sputtered, again no problem with shortcuts is expected which would deem an evaporation process necessary. Platinum or silver are the materials of choice for the gate metal.

Step 14: Lift-off

As in step 6 and 11.

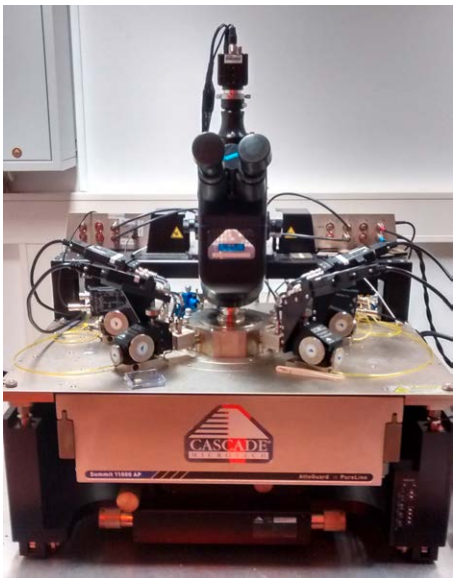
After these steps, a connection to the back contact of the sample is needed for proper electrical characterisation. This is ensured either by scratching and subsequent applying of conductive silver or a scratching and sputter deposition of a thin Ti (~10 nm) layer followed by Au for capping.

In appendix A, the drawings of the MOSFET masks can be found. The different colours represent different masks for the various processing steps performed to manufacture a MOSFET sample. Three different versions of the MOSFET mask are developed, this work mostly uses version 2 for the SB-MOSFETs without interfacial layer in section 3.2 or version 3 for the MOSFETs with interfacial layer in section 3.7. The version 3 of the MOSFET mask also contains a gate recess layer, which is not used for this work. The MESA layer in all versions is also not used as well. A comparision between a rectangular MOSFET of the different versions can be found in figure A.4, a list of gate lengths in table A.1. In all of these masks, rectangular as well as circular MOSFETs are drawn. Rectangular MOSFETs are easier to produce with a high yield, as the gate metal offers a needle contact which does not lie over the gate, thus allowing an easier needle placement procedure (see the following section) without the risk of destroying the delicate gate oxide with the needle. The circular MOSFETs have the advantage that the drain contact in the centre where the voltage is applied is protected from the outer part of the MOSFET, so no parasitic current can flow in. Furthermore, the gate length of the circular MOSFET is longer, allowing higher currents to flow. The Z in the masks and in the results chapter denotes a special gate type with a tongue-like structure, which tries to circumvent the problem of the needle contact area lying directly over the gate area by introducing a separate connecting area.

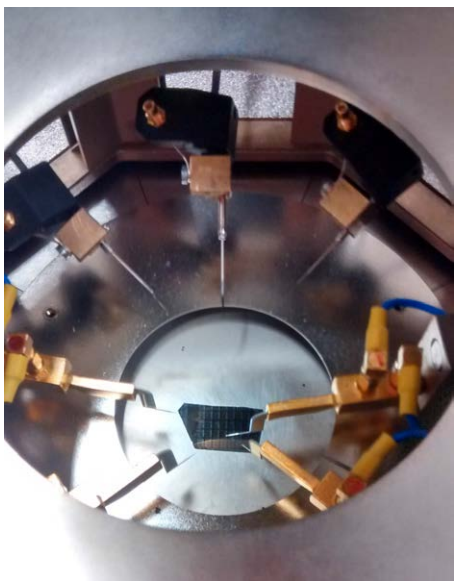
2.5. Electrical characterisation with probe station

Electrical device characterisation is carried out on a probe station (Summit 11000B-AP, *Cascade Microtech*) connected to a *Keithley* 4200 SCS parameter analyser (shown in figure 2.11 where four *Keithley* 4200 PA Remote Preamp SMUs are used for current/voltage measurements and an internal capacitance bridge for CV measurements. Figure 2.10a shows the probe station and figure 2.10b the needles which are connected to the Device Under Test (DUT).

All measurements were executed with the software environment KITE and performed at room temperature, unless otherwise noted. The probe station allows the controlled heating of the sample table which may be used e.g. for Schottky barrier analysis.



(a) Front view of the *Cascade Microtech* Summit 11000B-AP probe station



(b) View of the needles of the probe station in contact with a DUT

Figure 2.10.: Pictures of the probe station

Figure 2.11.: Front view of the Keithley Parameter Analyser 4200

2.6. Schottky barrier and MOSFET parameter extraction

2.6.1. Determination of the Schottky barrier height

Using the thermionic emission model as mentioned in section 1.3.2 the current flowing through Schottky contact is given by

$$I = AA^*T^2e^{\left(-\frac{q\phi_B}{kT}\right)}\left(e^{\frac{qV}{nkT}}-1\right) = I_S\left(e^{\frac{qV}{nKT}}-1\right) \tag{2.1}$$

with A being the area of the contact, q the elementary charge, A^* the Richardson constant (see table 2.2) and T the measurement temperature in Kelvin, q the elementary charge, V the bias voltage, n the ideality coefficient, k the Boltzmann constant and I_S the reverse current.

Table 2.2.: Values for the effective Richardson constant A^*, measured in $cm^2V^{-1}K^{-1}$ [26]

Semiconductor	*n*-type	*p*-type
Silicon	258	79
Germanium	138	43

Formula 2.1 can also be written in the following form (after [105])

$$I = I_S e^{\frac{qV}{nKT}} \left(1 - \frac{-qV}{KT}\right) \tag{2.2}$$

which allows the use of the experimental data pairs I(V). The plot V versus I/(1 − e(−qV/kT)) yields a straight line in a semi logarithmic plot. By fitting this straight line, the intercept results the saturation current I_S; from the slope m the ideality factor n can be determined as

$$m = \frac{q}{nkT} \tag{2.3}$$

The effective Schottky barrier height ϕ_B for electrons of the diode is given by

$$\phi_B = \frac{kT}{q} \ln\left(\frac{AA^*T^2}{I_S}\right) \tag{2.4}$$

In real (and thus inherently imperfect) diodes, the determination of the SBH is also prone to error by the Richardson constant A^*. The values in literature are measured for diodes which are as ideal as possible[2], therefore non-ideal Schottky diodes may have different values for A^*. Fortunately, an error in A^* does not affect ϕ_B heavily as it appears in the logarithmic term of the equation.

Another method to estimate the SBH (also after [105]) is the Richardson plot, where $1/T$ is semi logarithmically plotted against I/T^2, theoretically predicted as a linear curve. The slope allows to extract the SBH for a certain voltage without the need for the Richardson constant:

$$\phi_B = -\frac{k}{q} \frac{d\left[\ln\left(\frac{I}{T^2}\right)\right]}{d\left(\frac{1}{T}\right)} \tag{2.5}$$

As this method is not averaging the SBH over all voltages, the received values may differ from those which are extracted from the I(V)-curves in forward direction.

[2] Typically, those are produced in ultra-high vacuum by Molecular Beam Epitaxy (MBE) after thorough cleaning of the semiconductor interface [106].

2.6.2. MOSFET mobility

The mobility of a MOSFET is a surface channel mobility, in contrary to the mobilities measured by e.g. Hall measurements. The mobility is, as already described, degraded by various scattering mechanisms. For a n-channel MOSFET device with gate length L and width W, the drain current is described by [20]

$$I_D = \frac{W \mu_{eff} Q_n V_{DS}}{L} \tag{2.6}$$

with Q_n being the mobile channel charge density measured in C/cm^2 and μ_{eff} the mobility measured. From this formula one can derive a term for the mobility

$$\mu_{eff} = \frac{g_d L}{W Q_n} \tag{2.7}$$

while the output conductance g_d is defined as

$$g_d = \frac{\partial I_D}{\partial V_{DS}}|_{V_{GS}} = const. \tag{2.8}$$

with Q_n being approximated by

$$Q_n = C_{ox} (V_{GS} - V_T) \tag{2.9}$$

Another mobility parameter which can be extracted is the field-effect mobility, which is determined by using the transconductance g_m

$$g_m = \frac{\partial I_D}{\partial V_{GS}}|V_{DS} = const. \tag{2.10}$$

and results for μ_{FE}

$$\mu_{FE} = \frac{L g_m}{W C_{ox} V_{DS}} \tag{2.11}$$

which is typically lower than the effective mobility μ_{eff}.

2.6.3. Subthreshold slope

The subthreshold slope is the inverse of the subthreshold swing S

$$S = \left(\frac{\partial log I_D}{\partial V_{GS}}\right)^{-1} \tag{2.12}$$

which is equal to

$$S = \frac{1}{Slope} = \ln(10)\frac{kT}{q}\left(1 + \frac{C_D}{C_{ox}}\right) \approx \frac{60nT}{300}\text{mV}/decade \tag{2.13}$$

with C_d being the depletion layer capacitance. It describes the change of the drain current in the subthreshold region of the MOSFET with changing gate voltage. Higher absolute values for the slope mean a faster and better control of the MOSFET channel.

2.7. X-ray Photoemission Spectroscopy surface analysis setup

The XPS setup used for this thesis is a product of the company *SPECS*, consisting of an X-ray source XR 50 (which is equipped with Mg and Al targets to produce different characteristic X-ray emission lines, for Mg at 1253 eV and for Al at 1487 eV), coupled with an Phoibos 150 MCD-9 detector, all built into a UHV chamber capable of reaching routinely 10^{-11} mbar. Figure 2.12 shows the setup.

It is coupled by a vacuum line with the ALD and the EBE-1 e-beam evaporator, a LEED setup and an ion sputter gun (fur substrate cleaning). The holder on which the sample resides can be cooled or heated, the latter is used for desorption of surface layers of e.g. germanium in-situ.

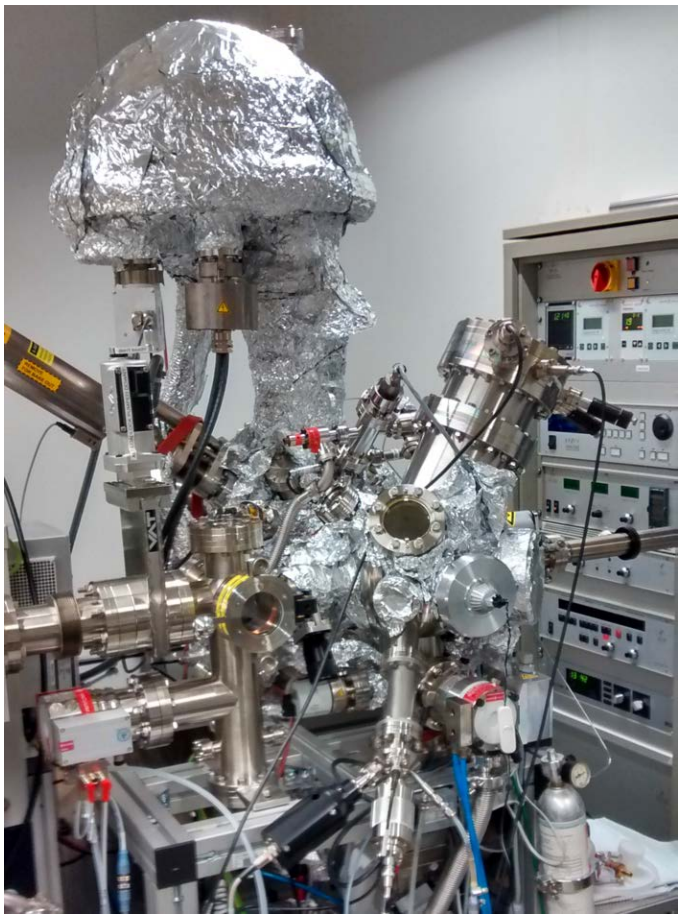


Figure 2.12.: The XPS setup used in this work

2.8. Time of Flight Secondary Ion Mass Spectroscopy (TOF-SIMS)

Time of Flight Secondary Ion Mass Spectroscopy (TOF-SIMS) (TOF-SIMS) is a well known technique which allows a mass-discriminating depth profiling. Samples undergo a sputtering process by atoms (e.g. O^+), the resulting sputtered ions from the sample (therefore called secondary) are analysed in a mass spectrometer. This technique has a very high sensitivity (high sensitivity in the ppm/ppb range) [107].

The machine used for this work is a TOF.SIMS^5 by *ION-TOF GmbH*.

2.9. Scanning Capacitance Microscopy (SCM) setup

To perform low frequency scanning capacitance microscopy, a combination of a conductive AFM tip with a high resolution, low frequency (1–20 kHz) capacitance bridge (*Andeen Hagerling* AH2700A) is used to measure the local capacitance between the tip and the sample.

The setup is also temperature-controlled. To perform a measurement, the AFM hood is closed and the temperature control started. After a settling time of several hours, a constant temperature is achieved, which is needed to eliminate all temperature effects and to allow the 0.1 aC resolution as mentioned in section 1.3.11.

The capacitance imaging is carried out by recording the capacitance by measuring with AC voltage during a DC voltage sweep to obtain a capacitance versus voltage C(V) curve for further analysis. The AC voltage was fixed at 375 mV. AFM tips coated with highly doped conductive diamond (p-type, $N_A = 1 \cdot 10^{20}$ cm^3) and a typical contact area of 30x30 nm are employed and can be regarded to behave completely metallic. More details can be found in the publications by Brezna *et al.* and Eckhardt *et al.* [108, 109].

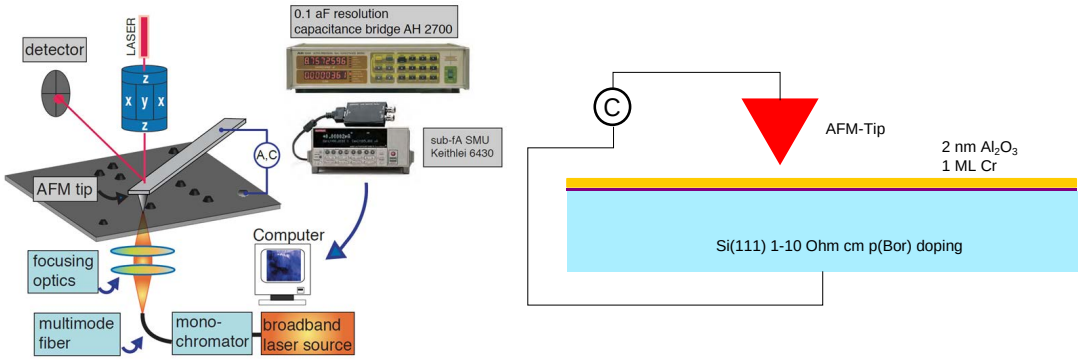


Figure 2.13.: Schematic of Scanning Capacitance Microscopy

2.10. Principle of in-situ resistance measurements while evaporating thin films

The deposition of all materials (Ag, Au, Cr, Ir, Pt, Ti) for the in-situ resistance measurements is performed in an e-beam evaporator (Leybold L560) equipped with a 4-place evaporation material holder at a base pressure of less than $1x10^{-6}$ mbar. The deposition is made from high-purity metals in pellet form either put directly into the copper-made holder or put in a crucible, depending on the material as shown in table 2.3. The materials holder is internally cooled by water during the evaporation to prevent any melting or alloying of the copper.

Table 2.3.: Deposited metals, evaporation rates and their crucibles. "-" indicates that no crucible is used.

Material	Rate [nm/sec]	Crucible
Titanium	0.0035	-
Silver	0.0033	Molybdenum
Gold	0.0044	Carbon
Platinum	0.0040	Carbon
Iridium	0.0057	-
Chromium	0.0048	Carbon

The metals to be evaporated are heated with an e-beam gun, see section 2.1.3. The measurement of the thickness by the QMB means that all given values in this experiment stating a thickness are in reality a mean thickness, where the amount of evaporated material on the surface corresponds to a thickness where the material is hypothetically homogeneously distributed and has everywhere the same density.

Various silicon wafers are used, all of them are of (111) orientation and prime quality. N-type (P doped) and p-type wafers (B doped) are used with a resistivity of 1-10 Ω·cm as well as a B doped wafer with 3000-5000 Ω·cm resistivity. The latter is used to increase the surface sensitivity of the resistance measurement by reducing the bulk conduction. All wafers are cleaved to 10x30 mm^2 pieces and are cleaned in an ultrasonic cleaner by using the following procedure: 5 min

acetone, 5 min isopropanol, 5 min water, and subsequently etching in buffered hydrofluoric acid in order to remove the native silicon oxide. The removal of the oxide is checked by the occurrence of hydrophobicity of the silicon surface.

Utilizing a shadow mask, two 520-nm thick aluminium contacts are sputtered by a physical vapour deposition system (*Von Ardenne* LS320). The rectangular contacts are each of 7x9 mm^2 size and located 15 mm apart. They are capped, after treatment in BHF, with a thin layer of silver using the same system, to allow soldering. The shadow mask was engineered to prevent edge covering of the sample during the contact sputtering, as edge covering was found to alter the measurement results. A local doping of the silicon under the contacts is tested but is dismissed because no change of the resistance behaviour has been observed.

Tin-coated copper wires (2 per contact to allow a 4-point measurement) are soldered with a standard lead-based solder to the contacts which are connected to an electrical vacuum feed-through. The resistance is measured continuously at a rate of one data point per second during evaporation by means of a high-precision source measurement unit (Keithley 238) with a constant current output of 1 mA (for the wafers with higher resistivity) or 10 mA (for the wafer with lower resistivity). These values are chosen to obtain a sufficiently large voltage across the device to allow accurate measurement, and low enough to prevent Joule heating. The resistance is determined by measuring the voltage drop between the two contacts. The short time between measurements (1 second) allows high-resolution resistance characterization during evaporation. A typical measurement consists of several thousand data points.

Prior to the installation of the sample with already attached wires into the evaporator chamber, the Si substrate is cleaned again in acetone, isopropanol, and treated in BHF resulting in an oxide-free, hydrophobic and hydrogen-terminated Si surface [110]. This treatment allows the formation of a clean and high quality surface without the need for time-consuming heating processes in UHV [111]. The evaporation rates for the metals are between 0.003 nm/s and 0.006 nm/s as shown in table 2.3.

Surface roughness imaging is conducted by means of an Atom Force Microscope (AFM, Veeco DI 3100) operated in tapping mode.

3. Results

The results of this work are separated into a couple of different sections. First, results of Schottky contacts which are essential to establish SB-MOSFETs are shown. In the second section, experimental results of SB-MOSFETs utilizing the findings of the previous sections are presented. The subsequent sections look at ultrathin metal layers; precisely their growth behaviour, capacitive AFM, the transition behaviour between MOS and MIM and in the end MOSFETs with those ultrathin metal layers.

3.1. Schottky contacts on Si and Ge

3.1.1. Experimental determination of proper S/D metals for Schottky-barrier MOSFETs on Si(111)

The method of deposition of the material influences the interface properties and therefore the electrical properties of a Schottky barrier contact. Literature suggests that phenomena like barrier height irregularities contribute to these different electrical properties [112, 113]. The model of Schottky barrier contact formation as described in section 1.3.2 assumes that the interface is homogeneous which is not true if we look at deposited structures [114]. A lot of work has been already done in the field of studying barrier height inhomogeneities [115, 116]. The conclusion of all this work is that for real applications, Schottky barrier properties have to be determined experimentally [22]. Only recently a theory of real metal-semiconductor could be constructed by means of quantum mechanics, but the theoretical understanding is still far from perfect [117].

In order to establish a MOSFET design as mentioned in section 2.4, Schottky Barrier contacts are needed which are able to work properly as a source/drain contact for a MOSFET without the need for annealing.

Several materials which are very common in SB-MOSFET technology are employed, e.g. platinum [118] or nickel [119]. Furthermore, different other available materials like Y, Nb, Ta or V are used. All those differ in their electronegativity values (see table 1.2), which should theoretically (see section 1.3.2) change the barrier properties.

All metals are sputtered (see section 2.1.2), the resulting metal thickness was for all samples about 50 nm. Two different silicon wafers are employed, both of (111) orientation and prime quality. N-type (P doped) and P-type wafers (B doped) are used with a resistivity of 1-10 Ω·cm, cleaned and BHF dipped before deposition. The samples where not annealed, so it is assumed that no significant silicidation process has happened. The measurement was performed by the Keithley probe station system (see section 2.5, the back contact was provided by scratching and subsequent application of conductive silver. Circular contacts with a diameter of 160 µm where used.

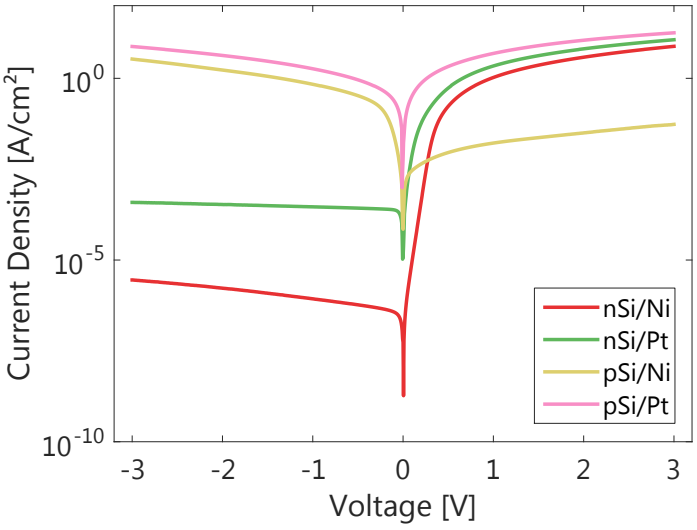


Figure 3.1.: IV-curves for sputtered Nickel and Platinum on nSi(111) and pSi(111), respectively

In figure 3.1, the behaviour of Ni and Pt on pSi(111) as well as on nSi(111) is presented. As expected, Ni and Pt perform well on nSi(111) due to their work functions while the other material combinations (on pSi) do not show a well-

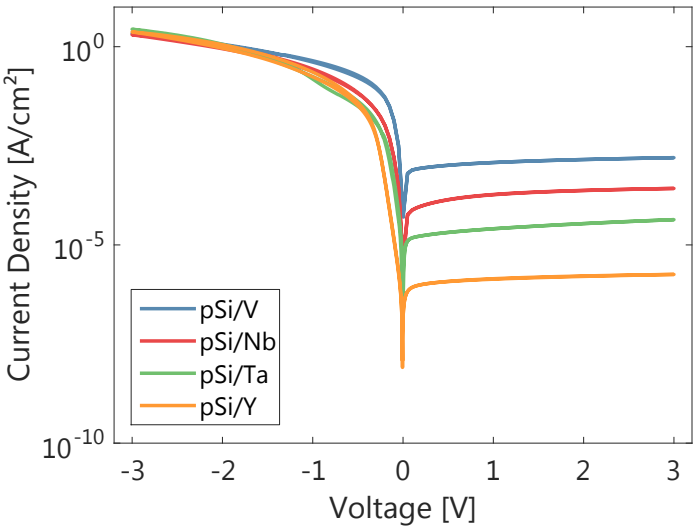


Figure 3.2.: IV-curves for sputtered Vanadium, Niob, Tantalum and Yttrium on pSi(111)

behaving rectifying behaviour. In table 3.1, the ratios of the forward and reverse currents are shown for all barriers. In figure 3.2, the combination of pSi with Y seems to perform properly, which suggests that yttrium is not only a suitable material for oxide formation by ALD, but also as a contact on pSi(111) without annealing.

Table 3.1.: Forward/Reverse Current Ratios I_f/I_r of different SB-contacts on nSi(111) and pSi(111)

Barrier	I_f/I_r **Ratio**	**Barrier**	I_f/I_r **Ratio**
nSi/Ni	$1.2{\cdot}10^{6}$	*pSi/V*	$3.7{\cdot}10^{2}$
nSi/Pt	$7.5{\cdot}10^{3}$	*pSi/Nb*	$1.3{\cdot}10^{3}$
pSi/Ni	$4.2{\cdot}10^{1}$	*pSi/Ta*	$6.0{\cdot}10^{3}$
pSi/Pt	$3.8{\cdot}10^{-1}$	*pSi/Y*	$1.6{\cdot}10^{5}$

3.1.2. Rhodium germanide schottky contacts

Platinum is already widely used material as a Schottky barrier contact for Si [42, 118, 120]and Ge [121–124] SB-MOSFETs. Apart from platinum, the platinum group contains additionally iridium, palladium and rhodium for which research work about their properties as contact to Ge exists [125–127] as well as osmium

which is not very suitable as a contact due to its high melting point [21] and toxicity of its oxide and ruthenium which we choose as a suitable topic for research. Only few reports exist on Rh_xGe_y compounds, like phase diagrams by Zhuravlev *et al.* [128], crystallographic studies by M. Wittmer *et al.* [129] and X-ray Diffraction/resistivity measurements on Ge(001) by S. Gaudet *et al.* [130]. Contrary to rhodium germanide, the Rh-Si silicide has already undergone investigation by different means [131–135]. Next to a high workfunction of 4.98 eV [21], making rhodium to an interesting candidate for pMOS devices, a main advantage of rhodium is its lower intrinsic resistivity of 4.5×10^{-8} $\Omega \cdot$ m compared to 1.0×10^{-7} $\Omega \cdot$ m of platinum [21]. Additionally, rhodium shows an even higher chemical resistance then platinum against several acids [136]. Therefore Rh-Ge contacts are considered in our view as a worthwhile subject for use in for example next generation ultrascaled Ge-based Schottky-barrier MOSFET devices.[1]

Sample preparation

As substrate, n-type (100)-Ge wafers (*MTI Corporation*) were used. Those 525 μm thick wafers were Sb-doped with a resistivity of 4.9–5.9 $\Omega \cdot$ m. The originally 2" wafers were cleaved into pieces of about 10×10 mm² size and subsequently treated to clean the wafers from cleaving debris and other contaminations. The cleaning was made in an ultrasonic bath for 5 minutes at maximum power using consecutively acetone, isopropanol and water, followed by dry blowing with N_2.

After cleaning, a standard lithography image reversal process (AZ 5124E resist) was applied for structuring the samples. The samples were put into buffered hydrofluoric acid (Sigma Aldrich AF 875-125) for one minute in order to remove the 20 nm thick GeO_2 protective layer from the Ge surface followed by a water (deionized) rinse and dry blowing by N_2. In order to minimize the oxide regrowth we ensured that the transfer into the load lock of the evaporation system was carried out in less than 5 minutes after BHF treatment. An electron beam evaporation system (EBE-1, *SPECS*, see section 2.1.3) was used equipped with a rhodium rod (*Goodfellow*, > 99.9% Rh) with 50 mm length and 2 mm diameter for Rh evaporation. Before evaporating, the vacuum chamber was evacuated to a pressure less

[1] The work in this section is published in [137].

than 1×10^{-7} mbar to ensure a clean deposition. The evaporation was carried out at a growth rate of about 0.67 nm/min which resulted in a mean Rh thickness of 20 nm. After evaporating, the samples were taken out of the vacuum chamber and a lift-off process was used for metal contact patterning. The pattern consists of one circular pad with a diameter of 350 μm and an outer ring as shown in figure 3.4a.

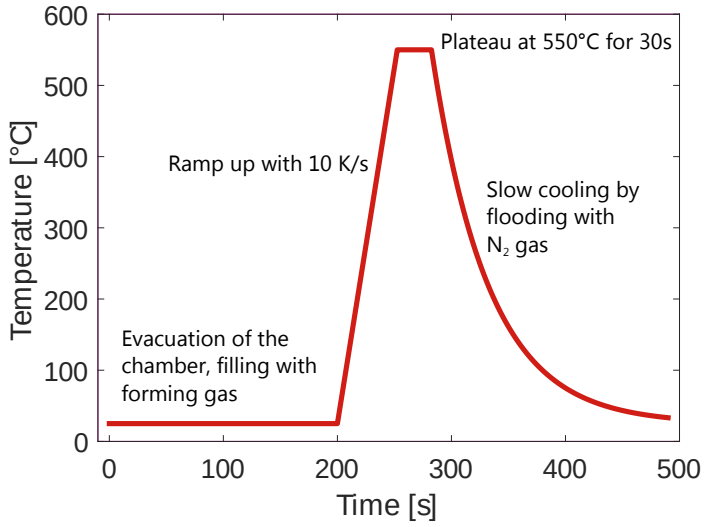


Figure 3.3.: Typical temperature evolution of an rapid thermal annealing process at 550°C for 30s

In order to induce a germanidiation of the Rh/Ge heterostructure a Rapid Thermal Annealing (RTA) infrared flash lamp furnance (UTP 1100, *UniTemp*) was used at a constant ramp rate of 10°C/s for 10 different annealing temperatures and times. The furnace chamber was evacuated to < 2 mbar and subsequently filled with forming gas (90% N_2/10% H_2). The furnace was heated up to the desired temperature within the region of 450°C < T < 800°C and was held constant for 30 s or 120 s, respectively, see figure 3.3 for the temperature profile. After the plateau time has elapsed, the chamber was rapidly flooded by dry nitrogen to ensure a rapid cooling of the sample. Extraction of the sample from the chamber was performed at temperatures less than 120°C. In table 3.2, the maximum annealing temperatures and times off all samples are noted.

Table 3.2.: Parameters (Annealing time $t_{Annealing}$ and temperature $T_{Annealing}$) of the RhGe Schottky contacts forming process

Sample #	$T_{Annealing}$ [°C]	$t_{Annealing}$ [s]
#1	450	30
#2		120
#3	500	30
#4	550	30
#5	600	30
#6	650	30
#7	700	30
#8		120
#9	750	30
#10	800	30

Electrical characterization

To perform electrical measurements of the Schottky diodes, the backside of the sample was scarified with a diamond pen and coated with conductive silver to ensure an ohmic back side contact.

The characterization was carried out by using the system described in 2.5. The measurement setup of the sample is schematically shown in figure 3.4.

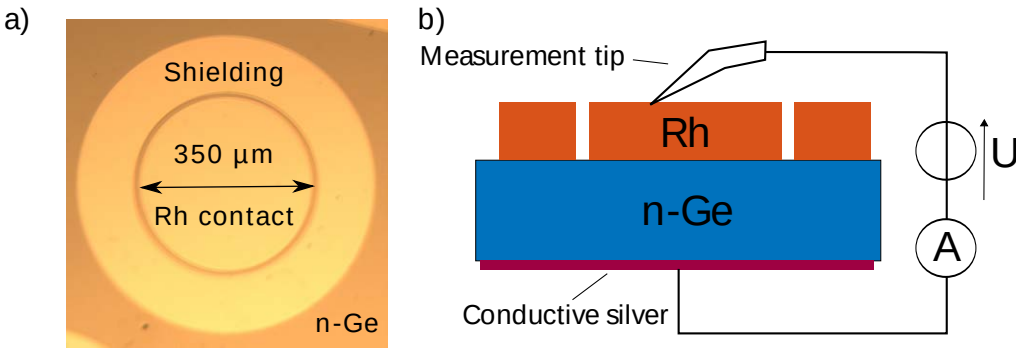


Figure 3.4.: a) Micrograph of the resulting patterned Rh on Ge structures after lift-off. b) Schematic drawing of the sample measurement setup.

IV-curves of Schottky diodes annealed at 550 °C for 30 s are shown in figure 3.5. It is visible that the reverse current depends strongly on the measurement

temperature as predicted by equation 1.20.

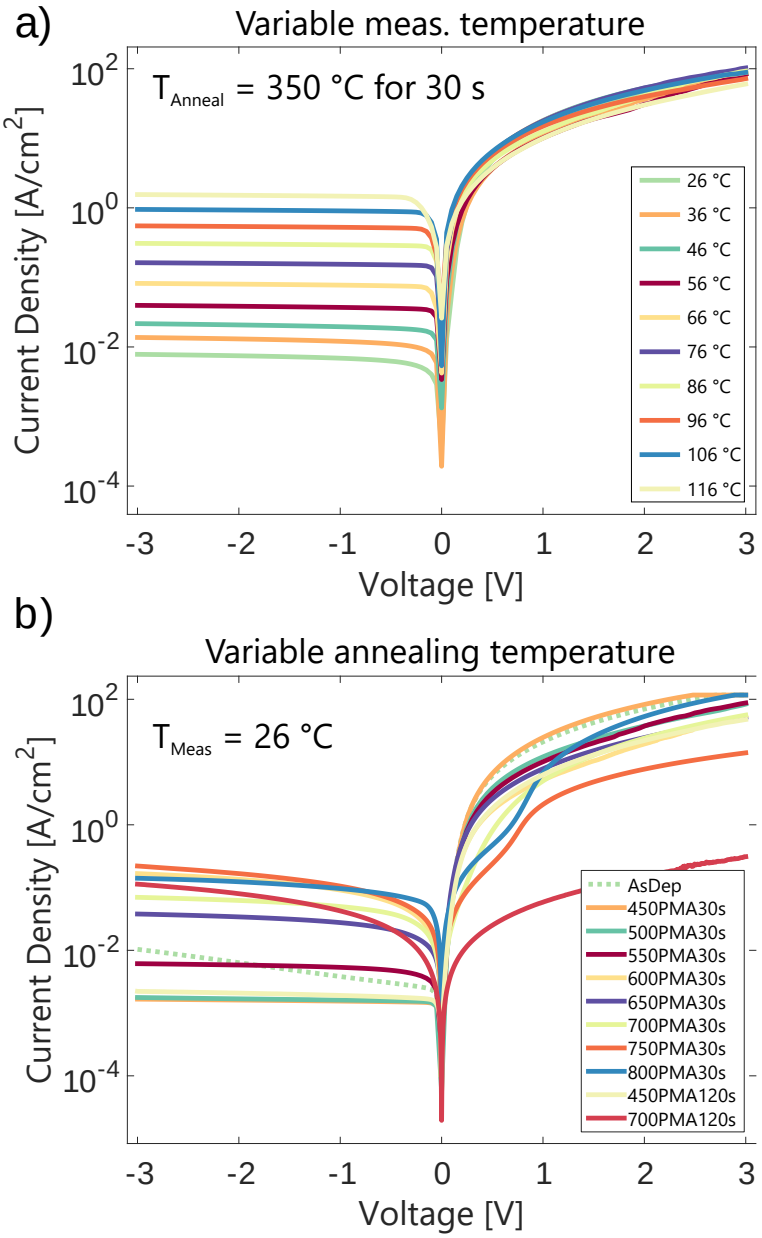


Figure 3.5.: a) IV-curves measured from -3 V to 3 V for a single spot after annealing at 550 °C for 30 s in forming gas atmosphere. Different line colours represent different measurement temperatures ranging from 26 °C to 116 °C.
b) IV-curves measured from -3 V to 3 V at 26 °C. Different line colours represent different annealing temperatures.

From the data, the effective Schottky barrier height as well as the ideality factor as a function of the measurement temperature (ranging between 26 °C and 116 °C with 10 °C steps) are calculated as shown in figure 3.6. It is obvious that

the Schottky barrier height Φ_B has a local minimum of 0.581 eV at a measurement temperature of 56 °C, whereat Φ_B increases up to 0.634 eV at higher temperatures of 116 °C for higher temperatures it increases up to 0.634 eV at 116 °C. Contrary, the ideality factor does not show a minimum and rather increases continuously with higher measurement temperature up to 2.48 at 106 °C. The observed measurement temperature dependence of the ideality factor and the SBH are in line with the findings on other materials [78, 138, 139].

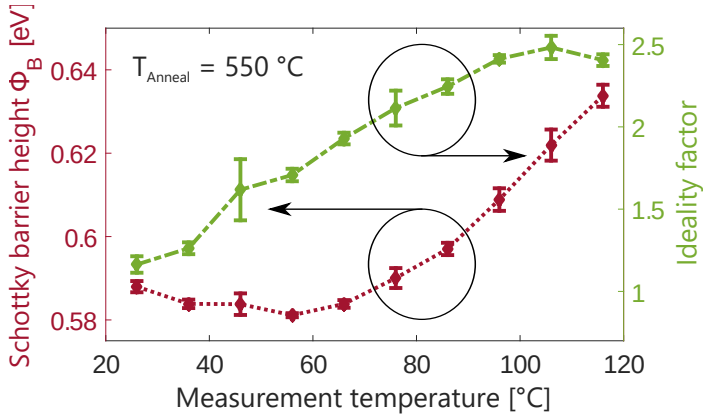


Figure 3.6.: Effective mean SBH for electrons and ideality factor (both with error bars) as a function of the measurement temperature (from 26 °C to 116 °C in 10 °C steps) for the Rh/Ge contacts which underwent an annealing at 550 °C in forming gas atmosphere.

Figure 3.5b shows similar IV curves all measured at room temperature now comparing different samples which underwent different annealing procedures. Here we can see a clear trend: although the not annealed sample shows relatively low reverse current, a constant behaviour within the negative bias region is not visible in the semi logarithmic plot. This is most likely attributed to a high series resistance of the unannealed contact. On the other hand, samples annealed at 450 and 500 °C show a constant behaviour and yield very low reverse current densities, indicating high quality rectifying Schottky contacts with low series resistance. In the case of the sample annealed for 120 s at 700 °C, we assume that the annealing process leads to a strong increase of the series resistance which is higher than for all other annealing processes and reduces the forward current resulting in this ohmic-like behaviour. The increase of the reverse current is most likely due to the formation of a defective Schottky-barrier induced by too high thermal budget. The mean ideality factor, the current ratio between forward and reverse current at ± 1V and the effective SBH for electrons have been extracted

by fitting V versus $I/(1-e^{-qV/kT})$ as described formerly from the raw data of the samples measured at 26 °C and are shown in Figure 3.7.

The SBH for electrons in this work lies between 0.53 and 0.59 eV with a tendency to decrease for higher annealing temperatures while the ideality factor as well as the current ratio change significantly. While the unannealed sample together with the samples annealed at 450 °C–550 °C show low linearity factors of < 1.2 and high current ratios of > 10^3, the quality of the samples annealed at temperatures > 550 °C deteriorates in terms of low current ratios and high values for the ideality factor n. This increase of the ideality factor n can be attributed most likely to an increasing Schottky barrier inhomogeneity at the Rh/Ge interface.

From the extracted parameters of the Schottky diodes we conclude that the optimal temperature to create rectifying contact lies between 450 °C and 550 °C while for an annealing at 500 °C highest effective SBH (0.59 eV), highest current ratio (5x10^3) and lowest ideality factor (1.07) can be achieved.

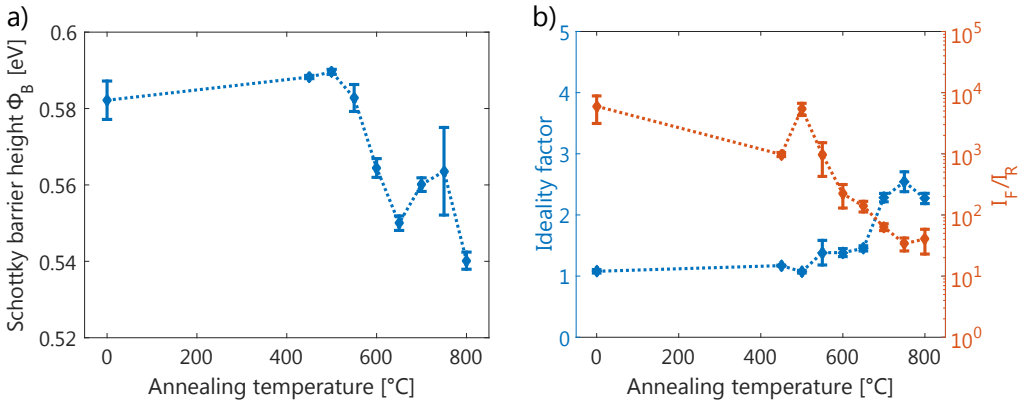


Figure 3.7.: a) Effective mean SBH for electrons with error bars vs. annealing temperature for all samples annealed for 30s at different temperatures. b) Mean ideality factor with error bars and current ratio measured at +-1V versus annealing temperature for all samples annealed for 30s.

For comparison the Richardson-plot method [105, 124] has been used for extracting the effective SBH for the diodes. For all samples, a Richardson plot has been created for each bias voltage point, resulting in a high number of Richardson plots in order to draw figure 3.8. In the inset of figure 3.8 a plot is shown where each data point is the extracted barrier height value of a corresponding Richardson plot, here extracted from a sample annealed at 500 °C. Of all 19994 Richardson plots, 40% of all fits show R^2 better than 0.95, 98% of all fits show

values for R^2 better than 0.5. The SBH at 0 V can be extracted by forward extrapolation of the linear region to 0 V where the electrons face the highest effective SBH.

The dependence of the barrier height on the bias voltage is not covered in classical thermionic emission theory of Schottky Barriers (see subsection 1.3.2), but is present in the inset of figure 3.8. This behaviour is already documented in literature [140–142]. In their paper, Mikhelashvili *et al.* discuss theoretical and experimental details of a bias-dependent Schottky barrier height [143].

Although the SBH versus temperature data of figure 3.8 evolve equivalently to the data shown in figure 3.7a, this method yields generally higher SBH values compared to the other method [22] and differs significantly for annealing temperatures higher than 700 °C.

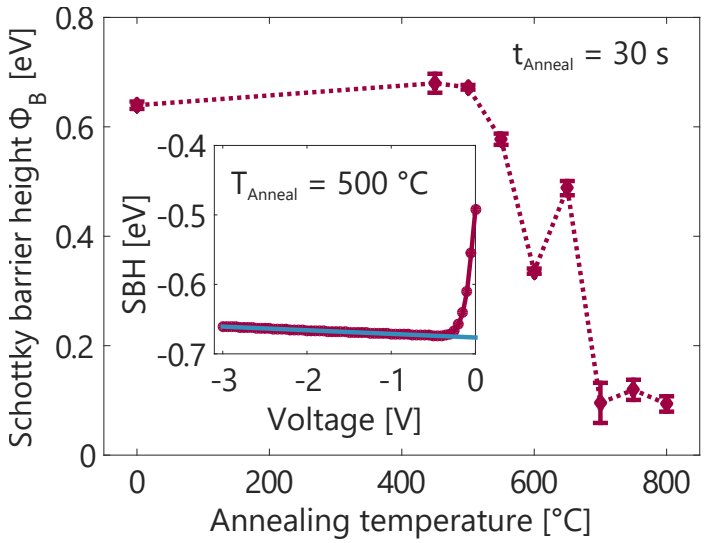


Figure 3.8.: Mean of the effective SBH at 0 V with error bars vs. annealing temperature for all samples annealed for 30 s and extracted by the *Richardson-plot* method. The inset shows the effective SBH vs. applied voltage for a RhGe diode annealed at 500 °C. The SBH values in the reverse region are used for linear fitting to interpolate the SBH at V = 0

The decrease of the Schottky barrier height, seen both in figure 3.7 as well as in figure 3.8, is most likely attributed to deteriorating microstructural changes at the interface between rhodium and germanium. We assume the formation of larger crystalline grain structures at higher temperatures which may lead to the alteration of the electrical properties of the Rh/Ge contact. These microstructural

changes resulting in a significant increased roughness are also seen in the AFM images, see figures 3.15 and 3.16.

The series resistance was found to lie in between 30 Ω and 140 Ω for all samples.

Experimental details of AFM, XRD, HR-TEM

AFM imaging is conducted using a atomic force microscope (DI 3100, *Veeco*) in tapping mode on that samples which have been used for electrical characterization.

High-resolution X-ray diffraction was used to characterize the Rh:Ge phase from a crystallographic point of view using a X'Pert PRO (*PANalytical*) machine where the Cu-K_α line is utilised as X-ray source. High Resolution Transmission Electron Microscopy (HR-TEM, *FEI TECNAI* F20) has been used to characterize the samples in terms of poly-crystallinity and thickness homogeneity.

TOF-SIMS of RhGe contacts

The TOF-SIMS is operated by using a dual-beam (Bi^+, $O_2{}^+$) in non-interlaced mode, where the sputter cycle (sputtering is carried out by $O_2{}^+$ ions) is conducted before the analysis cycle (by Bi^+ ions). The area of analysis was 75×75 μm with a resolution of 128×128 pixels while the sputter area was larger at 300×300 μm^2. The energy of the Bi^+ atoms coming from a bismuth liquid metal ion gun was 25 keV while the respective energy of the $O_2{}^+$ ions was 1 keV. For each cycle, the sputtering time with $O_2{}^+$ ions was 0.2 s, following by a pause of 0.5 s to remove slow ions for charge compensation.

Note that the sputter rate depends on the sputtered material and is not directly measurable in a TOF-SIMS system so the plots only show the sputter time on the x-axis. Nevertheless, the resulting sputter rate was estimated by means of profilometry to be ≈ 0.5–1 nm/s. The samples used for TOF-SIMS were fabricated same as for electrical measurements but without lithographical patterning.

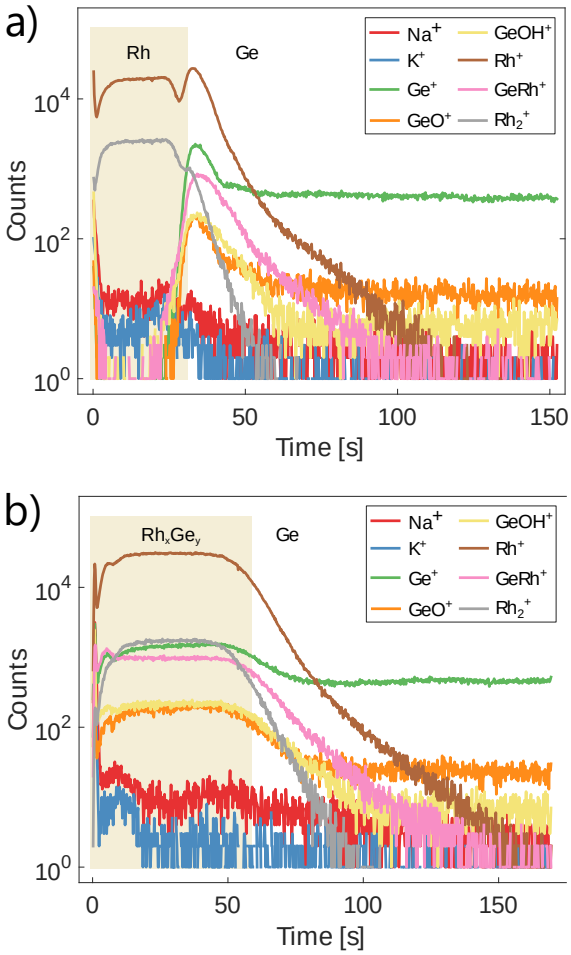


Figure 3.9.: a) TOFSIMS data for Rh/Ge before annealing. b) TOFSIMS data for RhGe after annealing at 500 °C for 30 s in forming gas atmosphere

For TOF-SIMS characterization as deposited Rh on Ge and Rh annealed at 500 °C for 30 s on Ge are compared only as the latter sample shows most superior electrical properties in contrast to all other annealed samples. The spectra before annealing in figure 3.9a show that pure deposition of rhodium on germanium leads to a rather sharp interface between the deposited metal and the semiconductor. The peaks at the Rh/Ge-interface were accounted to matrix effects of the sputter process. The measured GeO and GeOH fractions are most likely generated by the oxygen ions used for sputtering.

The data of the annealed sample in figure 3.9b show that already the short RTA process for 30 s is sufficient to ensure a complete alloying of Rh with Ge with no pure-Rh phase left. For using Rh-Ge in a Schottky-barrier MOSFET this would

be beneficial as no removal of unreacted Rh would be needed.

Additionally, the TOF-SIMS measurement reveals contaminations of the Rh phase with Na and K atoms. The specification of the used Rh-rod stated a purity of at least 99.9% with Na being the main trace (specified at <300 ppm), resulting from the separation process needed to produce pure rhodium. The potassium contamination might be originated there as well [144].

XRD of RhGe contacts annealed at 500 °C

A sample annealed at 500 °C was used for XRD measurements. The alignment was optimized for the (002) diffraction of the Ge substrate. Furthermore, the region between 20° and 35° was scanned in a dual axis geometry to identify different RhxGey phases, as shown in figure 3.10. The peaks around 20.2° and 22.9° can be attributed to the (002) diffraction of Rh_2Ge and Rh_5Ge_3 phases [145]. From the relative peak heights we estimate a Rh to Ge mass ratio of 2.1 within the contact layer. Notably, these symmetric diffraction scans did not reveal any traces of a RhGe alloy.

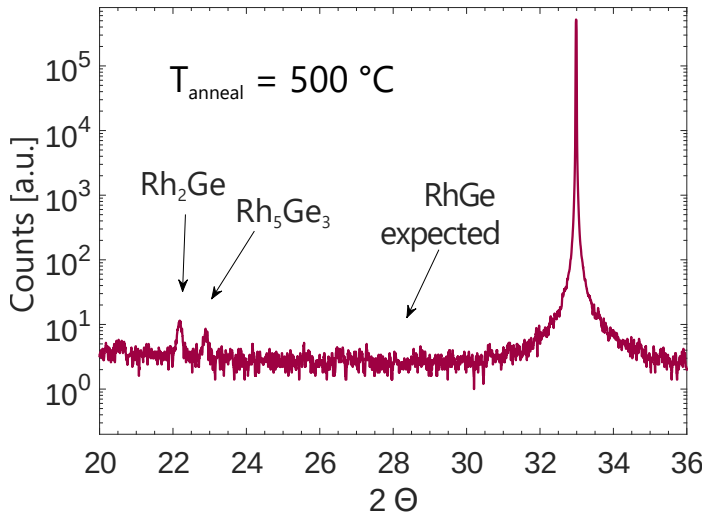
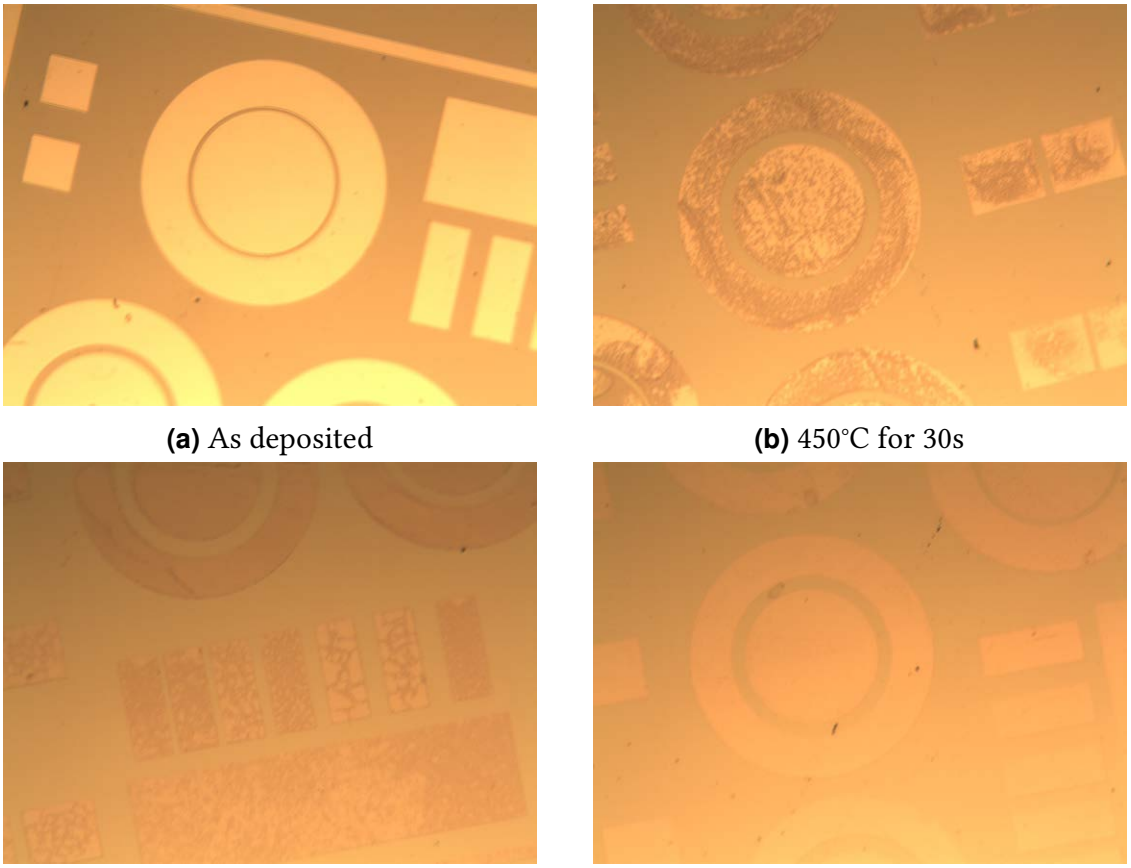


Figure 3.10.: XRD graph of a sample annealed at 500 °C for 30 s, with annotations for the two found phases

Microscopy of annealed samples with RhGe contacts

The annealing processes which were employed led not only to a change in the electronic properties but also to changes in the morphological structure of the contacts. The as deposited sample as well as the annealed ones were investigated by conventional light microscopy.



(a) As deposited **(b)** 450°C for 30s

(c) 450°C for 120s **(d)** 500°C for 30s

Figure 3.11.: Impact of the forming gas temperature annealing on the rhodium/germanium samples.
a) As grown
b) 450 °C for 30 s
c) 450 °C for 120 s
d) 500 °C for 30 s

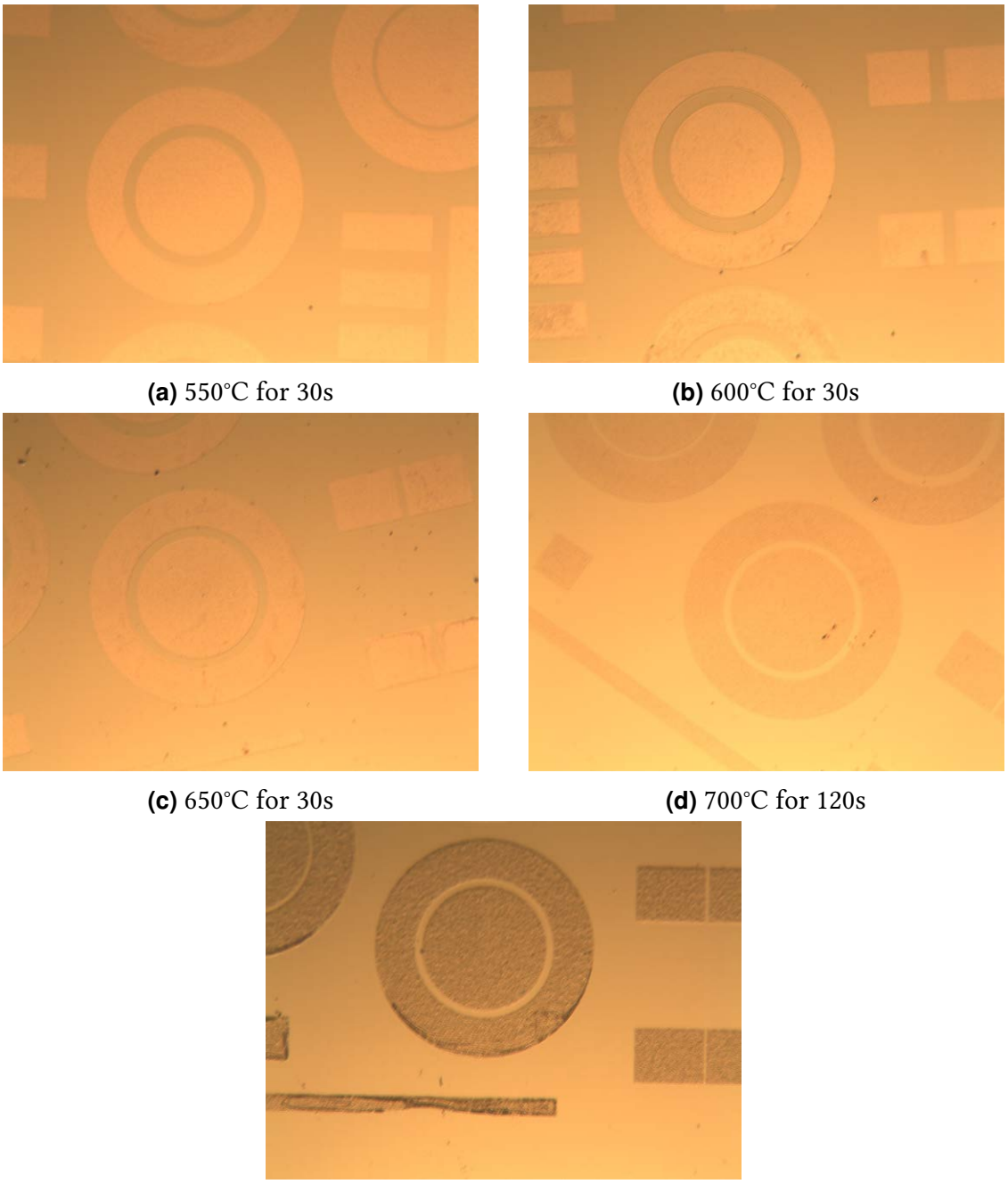
In figure 3.11 one can see the influence of the forming gas annealing for samples annealed at 450 °C and 500 °C in comparison to the as-deposited sample. The as-deposited sample shows a very smooth surface without any visible coarseness of the Rh film after lift-off. The annealing at 450 °C (Figure 3.11b) leads to a pro-

cess which alters the appearance of the metallic surface, but this does not happen homogeneously over the whole metal. If we increase the annealing time fourfold to 120 s (figure 3.11c), we see that the surface change processes which did not happen to be complete after 30s seems to be accomplished after 2 minutes.

The samples which was annealed at 500 °C (figure 3.11d exhibits, contrary to 450 °C, a uniform and shiny surface.

A further increase in the annealing temperature results in a matting/darkening of the surface. The sample annealed at 750 °C (and also at 800 °C but not shown here), for which the microscopy image is shown in figure 3.12e, shows a very coarse surface which was attributed crystallisation processes, which are further explained later in the AFM paragraph.

The microscopy images can be also correlated to the Atomic Force Microscopy images in subsection 3.1.2 were the microstructure of the Rh-Ge contacts is discussed.



(a) 550°C for 30s

(b) 600°C for 30s

(c) 650°C for 30s

(d) 700°C for 120s

(e) 750°C for 30s

Figure 3.12.: Impact of the forming gas temperature annealing on the rhodium/germanium samples. a) 550 °C for 30 s b) 600 °C for 30 s c) 650 °C for 30 s d) 700 °C for 120 s e) 750 °C for 30 s

HR-TEM of RhGe contacts

For HR-TEM, a blank sample which has been completely covered with rhodium by deposition on the Ge surface is been annealed at 500 °C for 120 seconds to ensure full consumption of the Rh layer into the Ge matrix. The layer shown in the middle of figure 3.13 consists of the RhGe and about 30 nm thick. The interface between Ge and Rh-Ge is accentuated and sharp without any interfacial layer. It is visible that the formed Rh-Ge phase is poly-crystalline which is consistent with the findings from XRD measurements.

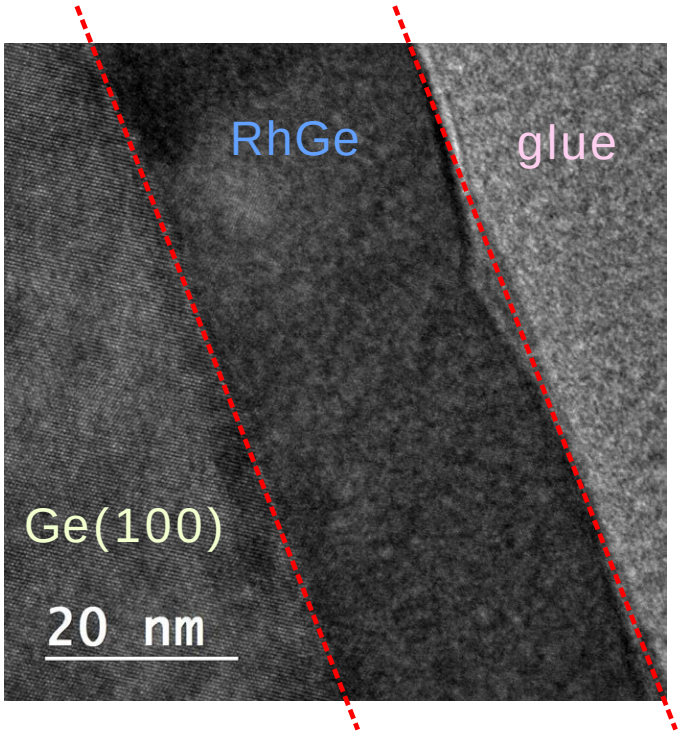


Figure 3.13.: HR-TEM image of the annealed RhGe layer. The Ge substrate is on the left side, the RhGe layer in the middle (thickness 30 nm) and the glue used for sample preparation on the right.

Atomic Force Microscopy (AFM) of RhGe contacts

AFM measurements are performed to complement the microscopy images and to investigate the changing of the surface of the Rh films which are subjected to different annealing steps. The annealing time of all AFM-characterized samples

is held constant at 30s. The images show (except 3.15b) the edge of a deposited rhodium film on the germanium surface, see figure 3.14.

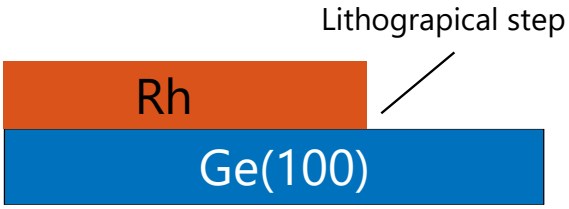


Figure 3.14.: A schematical drawing of the lithographically patterned step/edge of the Rh layer on Ge measured by AFM

Figure 3.15 depicts the AFM images of the Rh to Ge edge step which has not undergone any annealing (left) and a sample treated at 500° C for 30 s (right). One can see that the unannealed Rh film is smooth with a RMS of 0.9 nm. The visible spikes are most likely dust particles as they can also be found on the Ge surface which is situated at lower levels below the visible step. The film annealed at 500°C remains rather smooth with RMS of 2.35 nm and the step of the deposited Rh vanishes as confirmed by the microscopy images. Only a small granular structure is formed by this annealing step. On the contrary, annealing at higher temperatures completely changes the topography of the film.

Figure 3.16 includes AFM images for samples which are subject to 700° C (a) and 800° C (b) thermal annealing processes, respectively. Here, the topography is rough with a RMS of 13.5 nm at 700° C and shows a very coarse surface with small features. At 800° C the appearance changes into huge hillocks with large holes reaching deep into the germanium substrate with a RMS of 35.9 nm. The temperature dependent transformation of the thin film surface is most likely attributed to strain originated by a formation of inhomogeneous rhodium-germanium crystallites with different grain sizes. The measured coarseness by AFM can be correlated similar results of light microscopy in the previous paragraph.

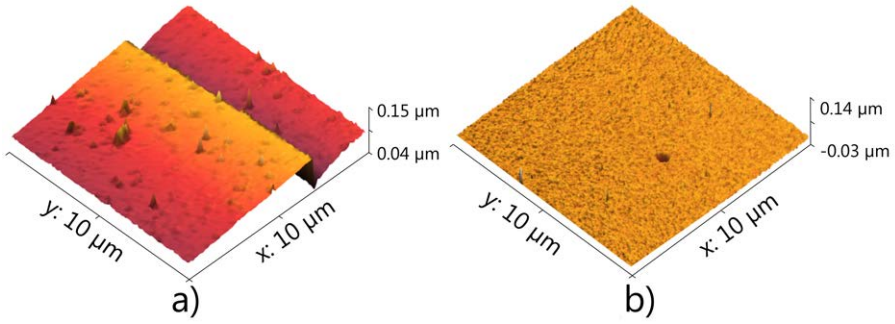


Figure 3.15.: AFM images of an unannealed sample (right) and a sample annealead at 500°C for 30s (right)

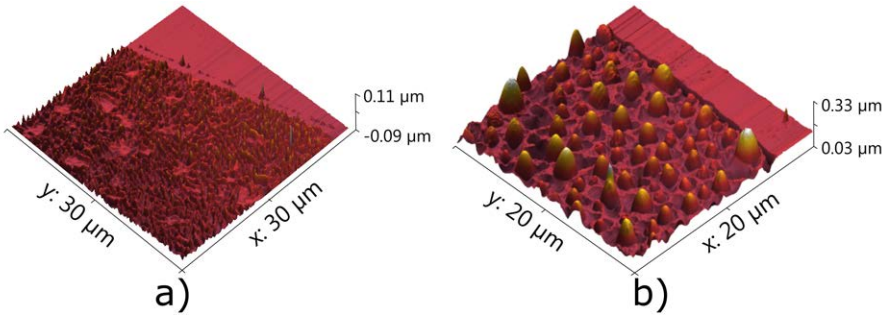


Figure 3.16.: AFM images of a sample annealead at 700°C (right) and a sample annealead at 800°C for 30s (right)

Summary

In summary, the binary phase of rhodium and germanium has been investigated, a yet not comprehensively explored metal-semiconductor compound, emphasizing its applicability in semiconductor technology. For this purpose Rh-Ge Schottky barrier diodes are fabricated by means of electron beam evaporation and forming gas annealing at different temperatures ranging from 450 °C to 800 °C in order to extract important electrical parameters from the SB contacts. The germanide has been also characterized by various analysing techniques.

It has been turned out that the optimal annealing temperature for forming rectifying high quality Schottky barriers is laying at 500 °C which is at the lower limit of the germanide phase formation temperature [18]. At these temperatures Rh_2Ge and Rh_5Ge_3 have been identified as the preferential crystalline phases formed by the germanidation process in forming gas. The effective SBH for electrons was extracted to be 0.59 eV showing a high current ratio I_f/I_r of $5x10^3$ and

a nearly perfect ideality factor of less than 1.1.

3.2. SB-MOSFETs with bilayered ALD-grown gate oxide on Si(111)

Equipped with the knowledge of the previous section addressing the question which metals are suitable for a well-behaving Schottky barrier contact to Si(111) even without annealing, the goal is now to manufacture a Schottky-Barrier MOSFET on this silicon substrate. This work will act as a prerequisite for the MOSFET with an interfacial layer in section 3.7. A layout was chosen as described in section 2.4 in the previous chapter with a bilayered oxide stack. The chosen MOSFET mask for this section was version 2, see section A.1.2.

Three different MOSFETs samples have been formed, for the two first samples several devices have been characterised on each sample. Those devices differ in the gate length and the basic MOSFET shape, either rectangular or circular. The first MOSFET sample is based on 1-10 Ω·cm n-type (phosphorus doped) Si with (111) crystal orientation as well as the second one, therefore FET devices with an P-channel, so-called PFETs are produced. The third sample is inverted, with 1-10 Ω·cm (boron doped) cm p-type Si with (111) orientation being the base material, producing NFETs.

The first sample features a gate stack consisting of 9 nm Y_2O_3, followed by 31 nm Al_2O_3, while for the second and the third sample the bilayer oxide thicknesses each are halfed, resulting in 5 nm Y_2O_3 and 15 nm Al_2O_3.

The S/D contact material for the MOSFET devices based on n-type silicon was platinum while for the p-type sample, yttrium metal was used. The gate metal was platinum for the PFET devices and silver for the NFET.

The electrical characterisation was again performed by the already described probe station at room temperature in the dark in order not to create additional photon-induced charge carriers. For the V_{GS}-I_D measurements, the source-drain voltage V_{DS} was kept at -0.5 V for all samples, the measurement frequency of the capacitance was f = 1 MHz. Figure 3.17 shows a rectangular MOSFET connected

Table 3.3.: Table listing the peak drain current I_D, the mobility μ_{eff} and the On/Off-Ratio for all measured SB-MOSFETs on Si(111) without an unintended interfacial layer. The letter Z is stating a special tongue-like structure for the gate metal for a circular MOSFET, the gate length is measured in µm, the mobility μ_{eff} in cm^2/Vs, the drain current $I_{D\,max}$ in µA/µm.

n-Type, 31 nm Al_2O_3, rectangular				**n-Type, 15 nm Al_2O_3, rectangular**			
Gate length	μ_{eff}	$I_{D\,max}$	I_{On}/I_{Off}	Gate length	μ_{eff}	$I_{D\,max}$	I_{On}/I_{Off}
2	2.5	1.34	$6.8 \cdot 10^1$	2	4	8.00	$2.2 \cdot 10^3$
5	5	0.85	$1.1 \cdot 10^2$	10	12	4.56	$2.0 \cdot 10^3$
10	10	0.93	$1.4 \cdot 10^2$	20	18	2.63	$9.4 \cdot 10^2$
20	19	0.92	$1.4 \cdot 10^2$	40	23	1.58	$1.1 \cdot 10^3$
30	24	0.85	$1.1 \cdot 10^2$				
40	24	0.21	$3.2 \cdot 10^1$				
n-Type, 31 nm Al_2O_3, circular				**p-Type, 15 nm Al_2O_3, rectangular**			
Gate length	μ_{eff}	$I_{D\,max}$	I_{On}/I_{Off}	Gate length	μ_{eff}	$I_{D\,max}$	I_{On}/I_{Off}
10	8	0.45	$3.5 \cdot 10^2$	40	-	0.1	-
10Z	6	0.57	$1.8 \cdot 10^2$				

by the needle prober, the picture was taken by using the alignment microscope of the setup. The calculation of the MOSFET parameters as the channel mobility is done as described in section 2.6.

A listing with the gate lengths, peak mobility, peak I_D and the On/Off-Ratio for all produced samples can be found in table 3.3.

SB-MOSFET with a Pt metal gate and an ALD-bilayer of 9 nm Y_2O_3 and 31 nm Al_2O_3 and Pt Schottky barrier contacts on n-Si(111)

First, MOSFETs with a "thick" bilayered oxide stack are formed and characterised. In figure 3.18, a CV curve of a corresponding MOS capacitor which is located on the same sample as the following MOSFET devies is measured, the capacitance density of this measurement is used for the subsequent mobility determination calculations. This curve shows some hysteresis and a flat band voltage V_{FB} of about +6 V.

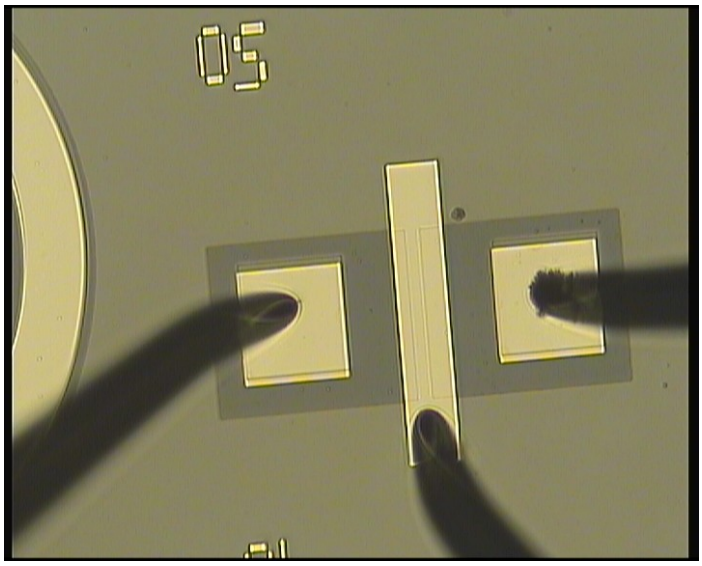


Figure 3.17.: View of a rectangular MOSFET as Device under Test in the Keithley probe station.

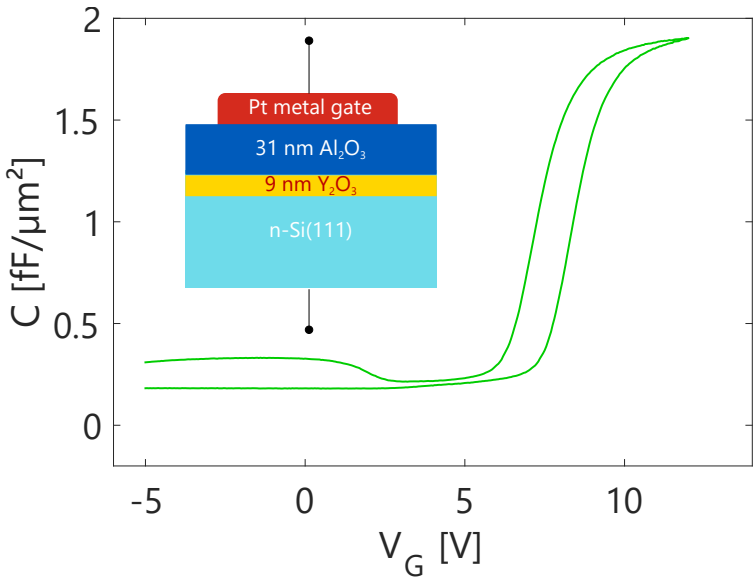


Figure 3.18.: CV curve of a MOSCAP which is located on the same sample as the following MOSFET devices.

In figure 3.19, a schematic drawing of the MOSFET structure including the ALD bilayer is shown, valid both for rectangular and circular MOSFETs.

Rectangular MOSFETs

Rectangular MOSFETs with a gate length ranging between 2 and 40 µm are measured, see figures 3.20 to 3.25. The MOSFETs measured were either rectangular with 2 to 40 µm gate length or circular, with 10 µm gate length, but with

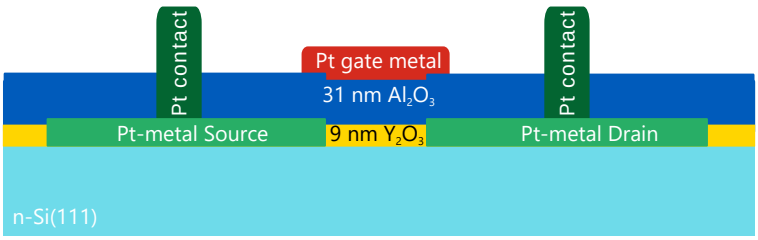
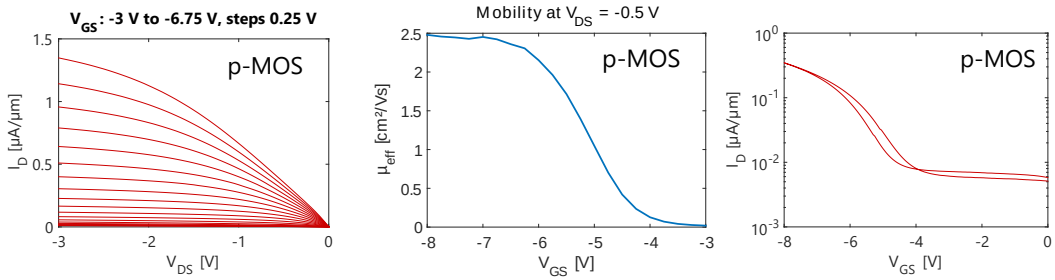


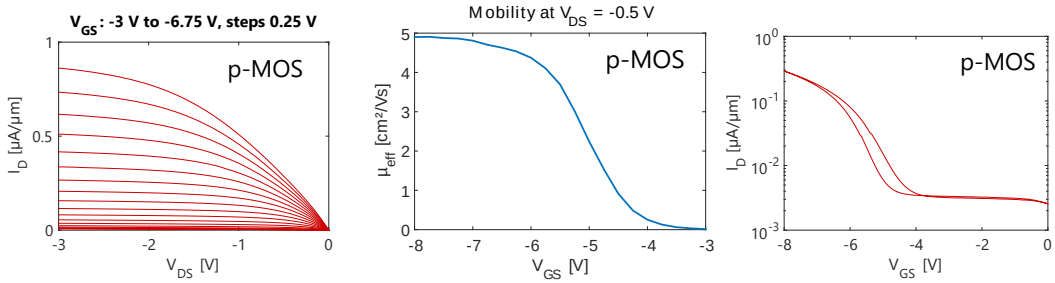
Figure 3.19.: Schematic drawing of the MOSFET type used measured in this paragraph.

different gates designs (see table A.1). All MOSFETs are characterised by their V_{DS}-I_D, V_{GS}-μ_{eff} and V_{GS}-I_D graphs.



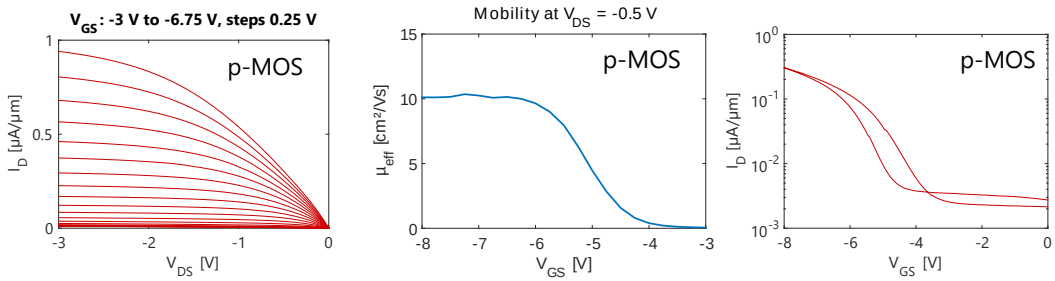
(a) Output **(b)** Mobility **(c)** Transfer

Figure 3.20.: Electrical characterisation data of a rectangular MOSFET with 2 µm gate length



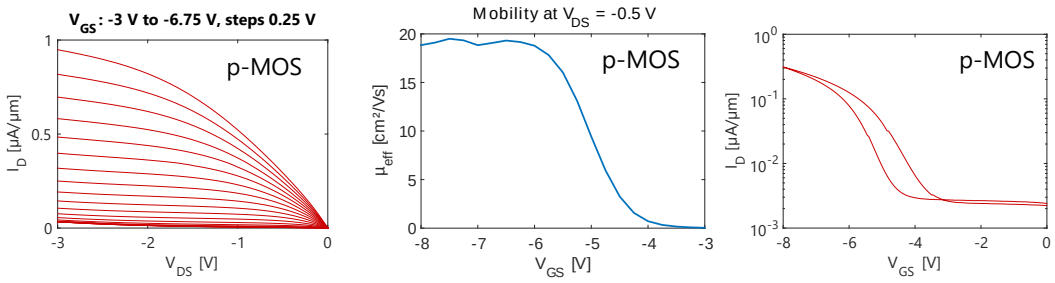
(a) Output **(b)** Mobility **(c)** Transfer

Figure 3.21.: Electrical characterisation data of a rectangular MOSFET with 5 µm gate length



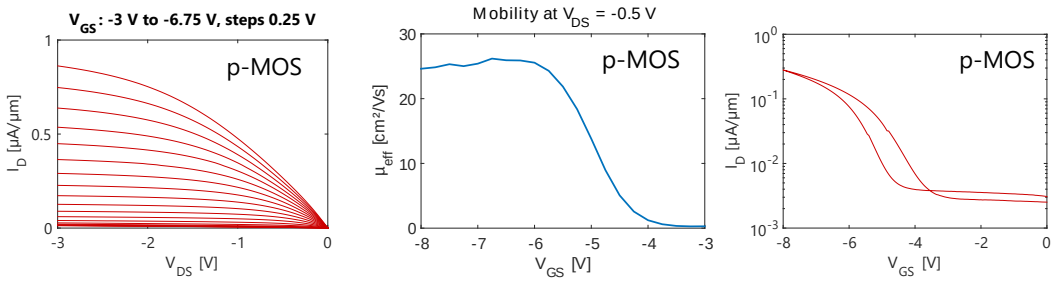
(a) Output **(b)** Mobility **(c)** Transfer

Figure 3.22.: Electrical characterisation data of a rectangular MOSFET with 10 µm gate length



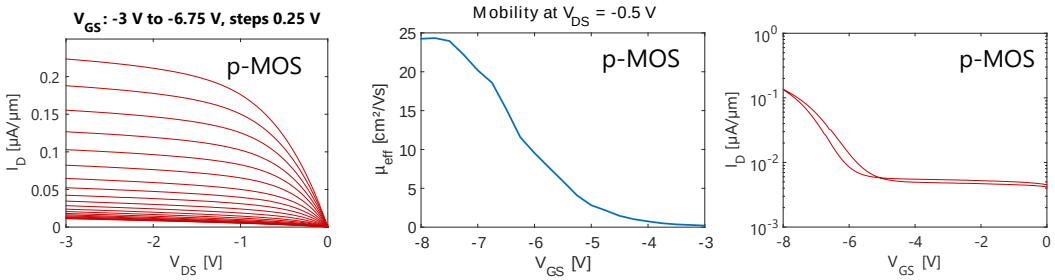
(a) Output **(b)** Mobility **(c)** Transfer

Figure 3.23.: Electrical characterisation data of a rectangular MOSFET with 20 µm gate length



(a) Output **(b)** Mobility **(c)** Transfer

Figure 3.24.: Electrical characterisation data of a rectangular MOSFET with 30 µm gate length



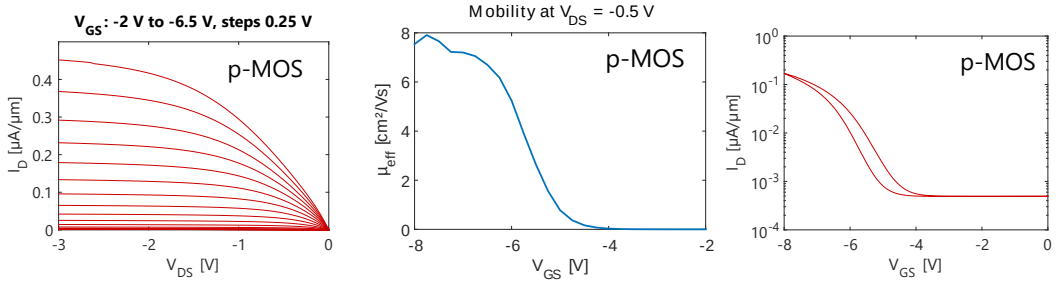
(a) Output **(b)** Mobility **(c)** Transfer

Figure 3.25.: Electrical characterisation data of a rectangular MOSFET with 40 µm gate length

As one can see, the maximum drain current depends on the gate length, as well as the mobility. While the drain current is the highest for MOSFETs with a small gate length, the mobility is the highest (around 25 cm²/Vs) for the MOSFETs with 20-40 µm gate length. The values for all devices can be found in 3.3.

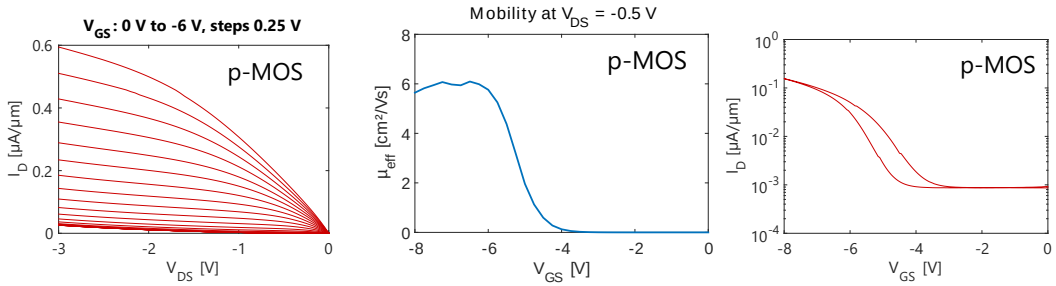
Circular MOSFETs

Circular MOSFETs have been produced as well, see appendix A for the drawings of those devices. In figures 3.26 and 3.27, the electrical characterisation curves are shown, similar to the rectangular devices before.



(a) Output **(b)** Mobility **(c)** Transfer

Figure 3.26.: Electrical characterisation data of a circular MOSFET with 10 µm gate length



(a) Output **(b)** Mobility **(c)** Transfer

Figure 3.27.: Electrical characterisation data of a circular MOSFET with 10 µm gate length and a special gate (tongue-like, designated by the letter Z) design

Here, the maximum MOSFET mobilities (8 cm²/Vs) and drain currents (0.6 µA/µm) are lower, which is accounted to the more difficult processing of circular MOSFETs compared to rectangular ones. Again, the values for all devices can be found in table 3.3.

SB-MOSFET with a Pt metal gate and an ALD-bilayer of 5 nm Y_2O_3 and 15 nm Al_2O_3 and Pt Schottky barrier contacts on n-Si(111)

Comparing the MOSFET devices produces for the following data with the previous ones, the thickness of the two oxides which form the bilayered oxide stack has been halved. As the oxide is only as half as thick as the previous one, the oxide stack capacitance should be about twice as big, which can be seen in figure

3.28, where the capacitance density is about 2.3 fF/µm² and the flat band voltage around 0 V.

For this subsection, only rectangular MOSFETs with a gate length of 2, 10, 20 or 40 µm are measured.

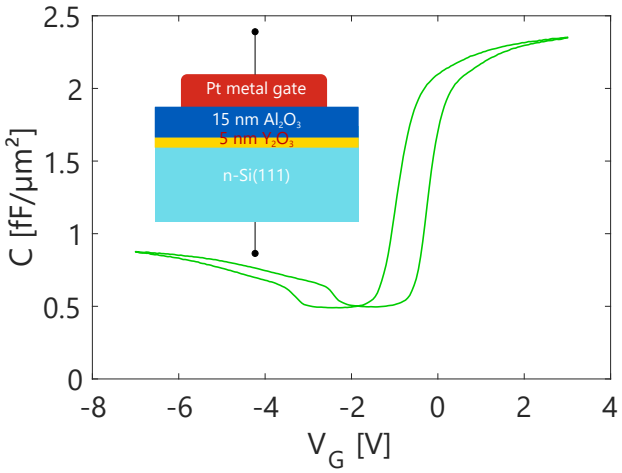


Figure 3.28.: CV-curve of the gate of a rectangular MOSFET with 10 µm gate length.

In figure 3.29, a schematic drawing of the MOSFET structure including the ALD bilayer is shown, valid both for rectangular and circular MOSFETs.

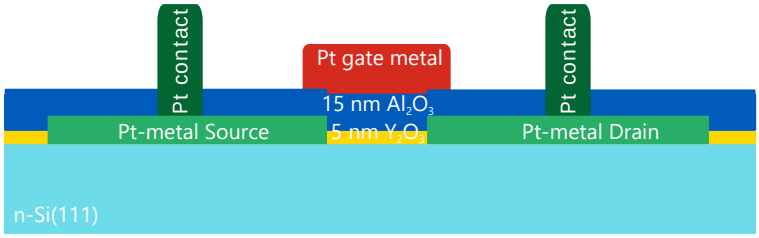
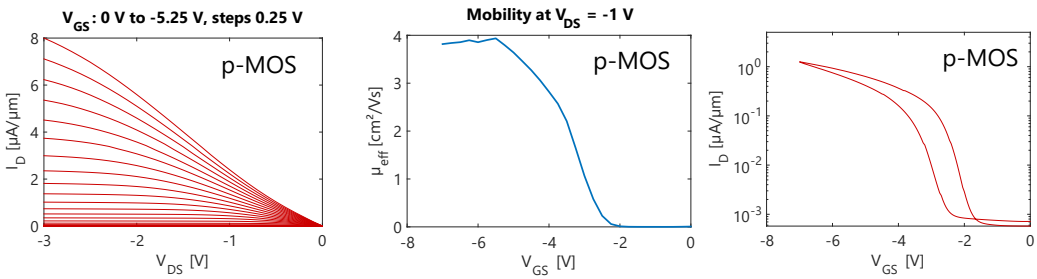


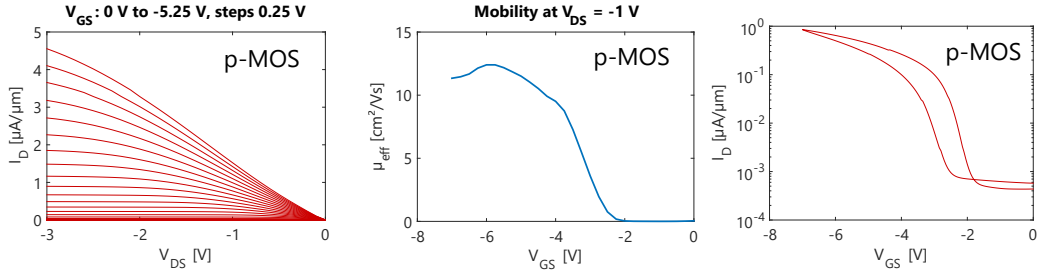
Figure 3.29.: Schematic drawing of the MOSFET type used measured in this paragraph.



(a) Output **(b)** Mobility **(c)** Transfer

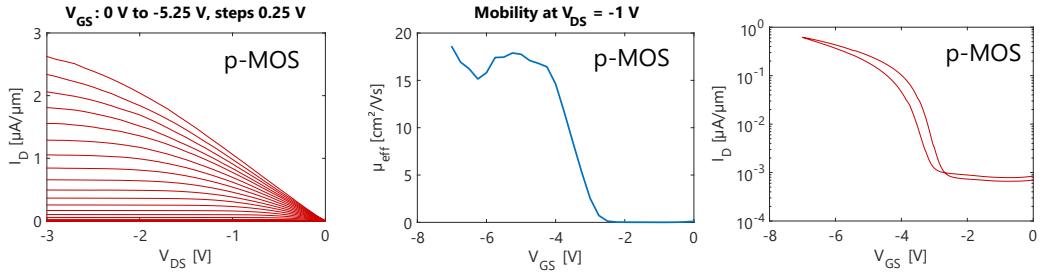
Figure 3.30.: Electrical characterisation data of a rectangular MOSFET with 2 µm gate length

As in the previous subsection, showing devices with oxide layers twice as much as in this subsection, the mobility hovers around 25 cm²/Vs for the de-



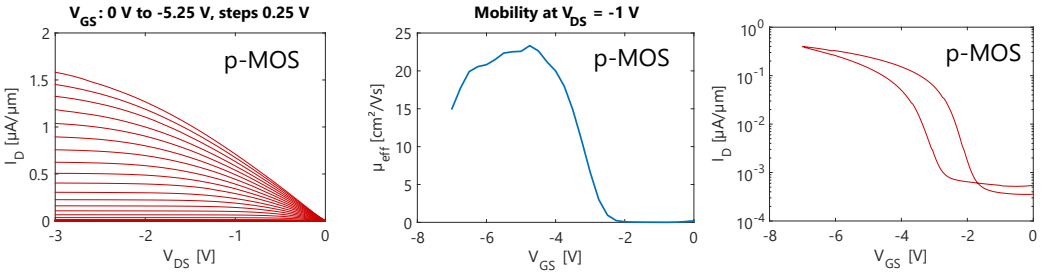
(a) Output **(b)** Mobility **(c)** Transfer

Figure 3.31.: Electrical characterisation data of a rectangular MOSFET with 10 µm gate length



(a) Output **(b)** Mobility **(c)** Transfer

Figure 3.32.: Electrical characterisation data of a rectangular MOSFET with 20 µm gate length



(a) Output **(b)** Mobility **(c)** Transfer

Figure 3.33.: Electrical characterisation data of a rectangular MOSFET with 40 µm gate length

vices with a bigger gate length (20 and 40 µm). The drain current is higher, up to 8 µA/µm. Figure 3.34 shows the relationship between the gate length and the inverse drain current $1/I_D$. As expected by MOSFET theory (see section 1.3.5), the drain current decreases with increasing gate length.

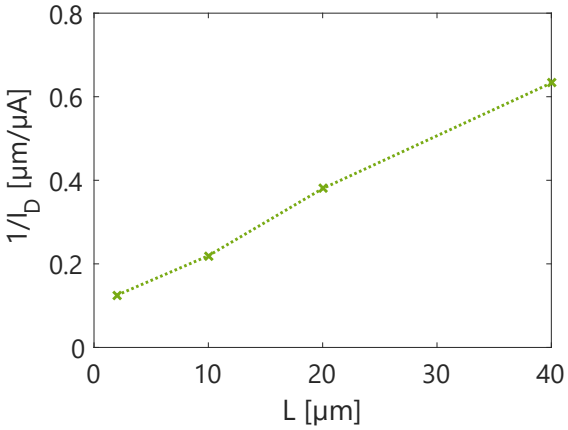


Figure 3.34.: The inverse drain current $^1/_{I_D}$ versus to the gate length L. The linear curve in the graph proves the reciprocal relationship between I_D and L

SB-MOSFET with a Ag metal gate and an ALD-bilayer of 5 nm Y_2O_3 and 15 nm Al_2O_3 and Y Schottky barrier contacts on p-Si(111)

The same MOSFET mask used for the previous devices (Mask 2, see A.1.2) has been been analysed for its suitability to produce NFET devices, which means devices where the bulk semiconductor is p-type silicon. Yttrium metal Schottky barrier contacts were used together with silver as the gate metal; the plasma oxidation process described in 2.1.5 was also employed here. The schematic drawing of n-MOS device can be seen in figure 3.35.

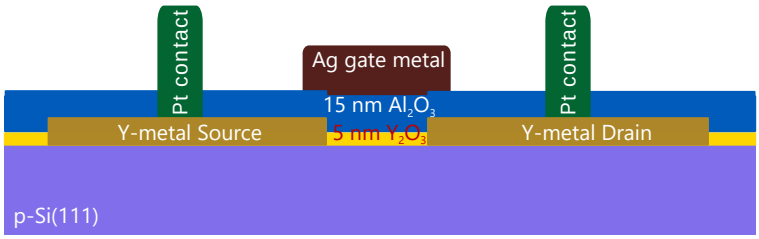


Figure 3.35.: Schematic drawing of the MOSFET type used measured in this paragraph.

Producing this device is considered a much more challenging issue, resulting in a lower yield compared to the p-MOS devices in the previous sections. In 3.36, the V_{DS}-I_D for a rectangular MOSFET with 10 µm gate length is shown. The drain current I_D is again very low, and only a slight split-up of the drain current curves depending on the gate voltage (which varies between -10 and +5 V) can be seen.

In figure 3.37, the corresponding CV-curve of the MOSFET gate can be seen. A

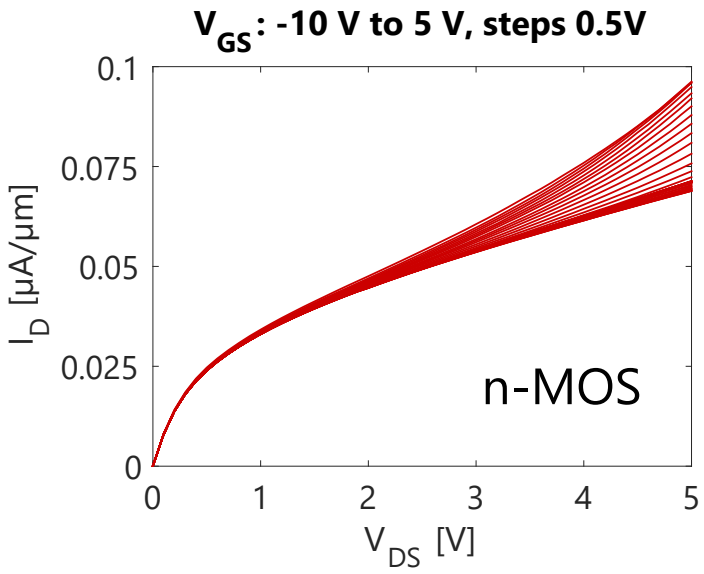


Figure 3.36.: V_{DS}-I_D-curve of a rectangular Ag metal gate SB-MOSFET with 40 µm gate length and a ALD-grown 5 nm Y_2O_3 and 15 nm Y_2O_3 bilayer oxide on p-type Si(111)

typical CV-curve on a p-type bulk can be seen, with a flat band voltage of around -1 V. This gate oxide structure has been also made without any annealing, just by depositing the bilayered oxide with ALD.

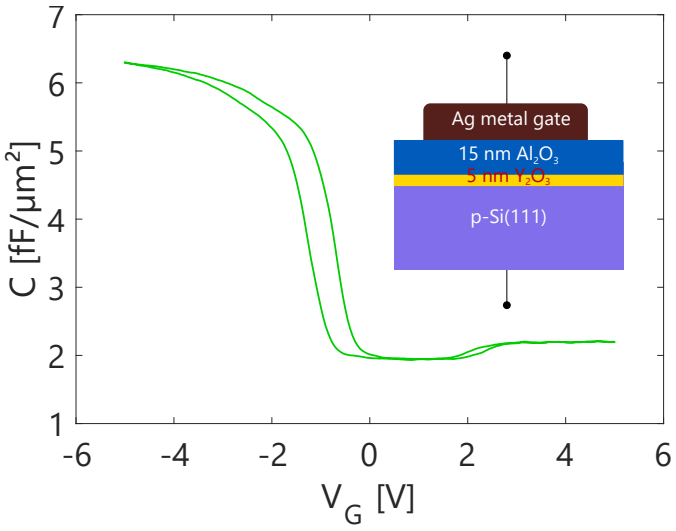


Figure 3.37.: Corresponding CV-curve of the gate of a rectangular MOSFET with a ALD-grown 5 nm Y_2O_3 and 15 nm Y_2O_3 bilayer oxide on p-type Si(111)

3.3. Resistance of ultrathin transition metal layers during growth on Si(111)

Introduction

One of the most fundamental physical properties of a thin film is its conductivity. For example, Gergen et al. [146] used in-situ resistance measurements to characterize evaporated Ag and Ti films on hydrogen-terminated Si(111). In-situ measurements are particularly interesting because they allow measurement of thin film properties with a quasi-continuous resolution of thickness, and they are not affected by the breaking of vacuum or other corrupting processes. They also allow investigation of the very early stage of evaporation, which is the focus of our work. At this stage of evaporation, percolation effects [147] may occur, where separate areas of conductive evaporated material connect and allow conduction through them.

In most existing studies pristine, ultra-clean surfaces without any faults and with perfect surface reconstruction have been used. The results are not easily transferable to conventional semiconductor device fabrication processes. In this work, we focus on compatibility with conventional Si processes by using standard Si surface cleaning and evaporation equipment in an ultra-high vacuum (UHV) environment. The primary goal is to investigate the growth modes of ultrathin films of Ag, Au, Cr, Ir, Pt, and Ti by analysing the time dependent in-situ resistance. The measurements are performed with a resolution in the sub-nm region.

One of the goals of this work is to identify the percolation threshold and continuity threshold of thin films. The work of Ingason *et al.* [148] proposes a model where the resistance of the thin film used as the relevant value to produce plots from which the percolation and the continuity threshold can be directly identified. We propose a simple model to calculate the thin film resistance R_f from the measured resistance R_m.

The experimental setup for this measurement is described in section 2.10. The measured resistance R_m is taken as the resistance of a parallel circuit between the

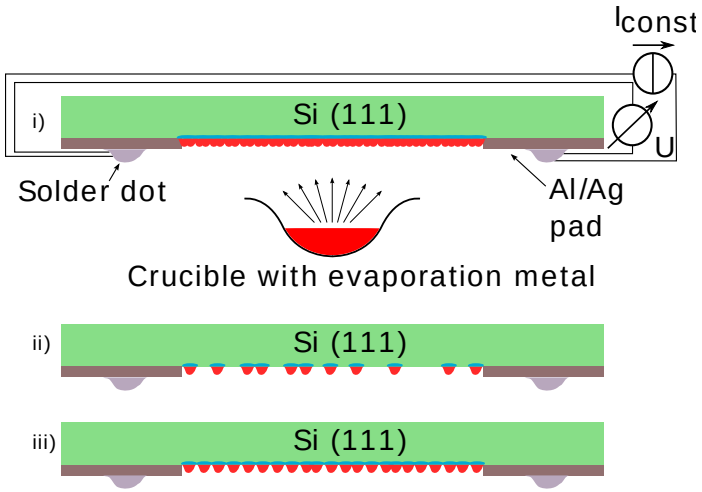


Figure 3.38.: i) Second percolation point as well as the principle of the evaporation and measurement setup
ii) Situation before percolation
iii) First percolation point

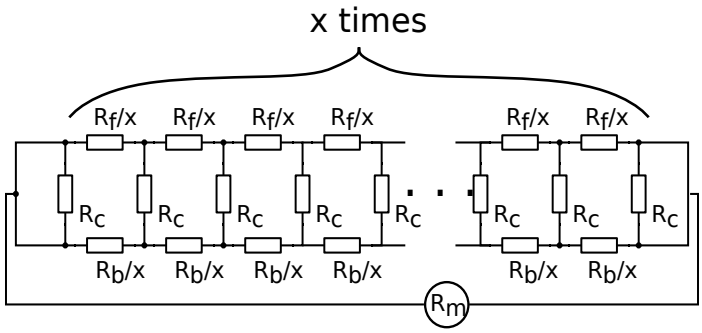


Figure 3.39.: The resistor network model for metal-on-silicon, see Ingason *et al.* [148]

silicon itself and the metal on the surface. The bulk silicon resistance R_B is defined by the resistance of the Si sample before the starting point of the deposition at time $t = 0\ s$. In order to determine the resistance of the film, only the bulk and the film resistance are separated by using a model system. For the model it is needed to assume that the thin film as well as the bulk are homogeneously distributed along the current path in between the two contact pads. Although this macroscopic simplification does not reflect the microscopic morphology it is assumed that local inhomogeneities are balanced along the about 2 cm long current path. A resistor network model can be proven by considering these two layers as a series of x resistors as shown in figure 3.39.

The resistors R_C representing the contact resistance between the bulk and the

Table 3.4.: Deposited metals, their crucibles and evaporation rates. "-" marks that no crucible is used.

Material	Crucible	Rate [ML/sec]
Ag	Molybdenum	0.012
Au	Carbon	0.011
Cr	Carbon	0.016
Ir	-	0.015
Pt	Carbon	0.010
Ti	-	0.008

film which can be neglected as almost no potential difference across them is expected resulting in no current flow. Thus the resistance network turns into a parallel circuit consisting of x resistors with the value R_m/x in series together with x resistors with the value R_b/x in series which is a parallel circuit of R_f and R_b where R_b is the bulk silicon resistance (i.e. the resistance at $t = 0$) and R_f represents the thin film resistance (diverging at $R_m = R_b$). The thin film resistance can be calculated from the measured resistance R_m as

$$R_f = \frac{R_m R_b}{R_b - R_m} \tag{3.1}$$

At first results for the evaporation of Ti, Ag, Au, Pt, Ir and Cr on 1-10 Ω·cm p-type silicon are displayed in figure 3.40 (a,b,c). Figure 3.40a shows the relative resistance R_m/R_{m0} versus the thickness measured in nm. The resistance value is normalized to the initial resistance at $t = 0$ s in order to compensate the influence of sample preparation irregularities which can change the initial resistance value up to 10% (a typical resistance value before evaporation is 240 Ω). Several conclusions can be drawn from this figure. At first, the plot can be divided into three regions. Notably in the first region, the resistance does not decrease as expected but rather increases. This behaviour will be analysed in a further section of this work.

In the second region a huge drop happens where the resistance decreases sharply. Subsequently, in the third region the resistance is stabilizing to a value

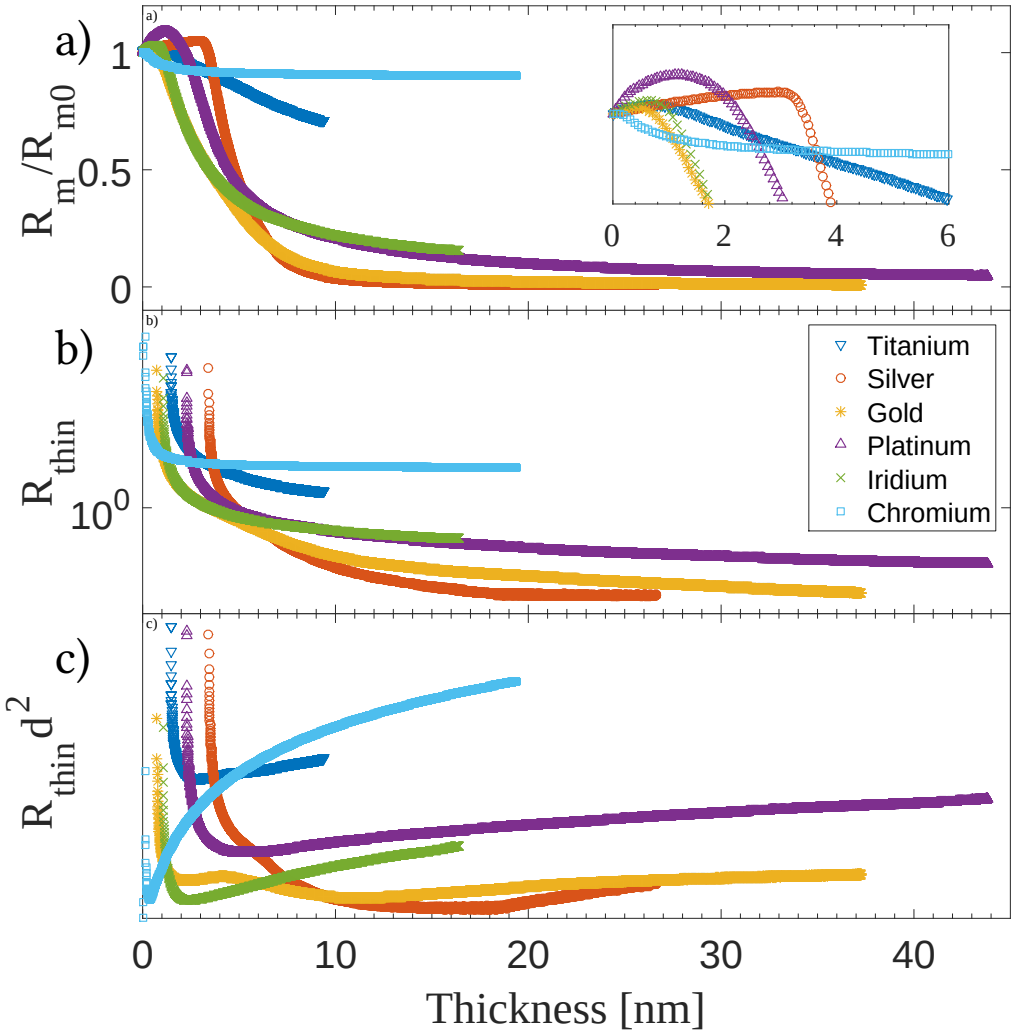


Figure 3.40.: a) In-situ measured resistance versus thickness for Ti, Ag, Au, Pt, Ir, and Cr. The inset shows only every 10^{th} data point.
b) The calculated thin film resistance (diverging for $d \rightarrow 0$) for all metals, and c) $R_{thin}d^2$ plot for all metals.

less than 10% of the initial value and does not show any longer significant relative changes even though the film thickness increases.

According to the model of Ingason *et al.* [148], plotting the product of the resistance R and the square of the evaporation time t^2 is used to identify the percolation point as well as the point where the silicon surface is completely covered with deposited metal. They are indicated by the local maximum and the local minimum of the Rt^2-plot, respectively. For a constant evaporation rate $d \sim t$ can be assumed, so that the film thickness d (either in nm or ML) instead of

the time t can be used. As we are measuring on a semiconducting surface, the thin film resistance R_{thin} acts as the base value for the Rd^2-plot. Therefore the percolation point cannot be found in a local maximum as R_{thin} and $R_{\text{thin}}d^2$ are approaching infinity at the same point were the local maximum of R exists. For thicknesses d before $\max(R(d))$ the thin film resistance R_{thin} is negative, thus we exclude this region from the R_{thin} and $R_{\text{thin}}d^2$-plots.

The first approach to describe this behaviour is a percolation effect (see A. Kapitulnik *et al.* [149]). As reported by Stauffer *et al.* [150], three growth modes for metal films are defined: (a) Volmer-Weber (VW: island formation), (b) Frank-van der Merwe (FM: layer-by-layer), and (c) Stranski-Krastanov (SK: layer-plus-island). For the metals in Figure 3 different growth modes can be assigned. For Ti, Ag and Pt their respective percolation points are rather high which means that already a few monolayers have been deposited on the Si surface before the electrical percolation is achieved. Therefore a Volmer-Weber film growth mode can be assumed where small islands form on the hydrogen-terminated silicon surface. Similar behaviour has been also reported for Ag on h-Si [151], in contrary to pristine Si(111) where Stranski-Krastanov growth with a wetting layer takes place [152]. At the percolation point, where R_m peaks we assumed first that the islands start to connect, forming an electrically continuous surface (though not physical flat). Later on in this work we will continue the discussion on this point. Cr is different to all other materials because it already shows percolation at a very low thickness of less than half a nanometre. This leads us to the assumption that Cr grows on h-Si in the Frank van der Merwe mode, which makes it an excellent material to cover h-Si with a very thin layer of metal. Au and Ir are difficult to assign a growth mode. Their percolation point is about 1 nm, which corresponds to 2-3 MLs of thickness. We suspect that they also grow in the Volmer-Weber mode but in different morphology causing them to achieve the percolation point earlier.

Influences on the resistance of the grown thin films

To enhance the understanding of these findings, we made different experiments to investigate influences on the behaviour of the $R(d)$ curves, all with Ag as

evaporation material.

At first the influence of the evaporation rate was investigated on 111-n-Si with 1-10 Ω·cm resistivity. As shown in figure 3.41, the influence of the evaporation rate is only minor and does not change the overall appearance of the plot. Particularly, the position of the transition point between region 1 and 2 does not change at all and remains at 4 nm.

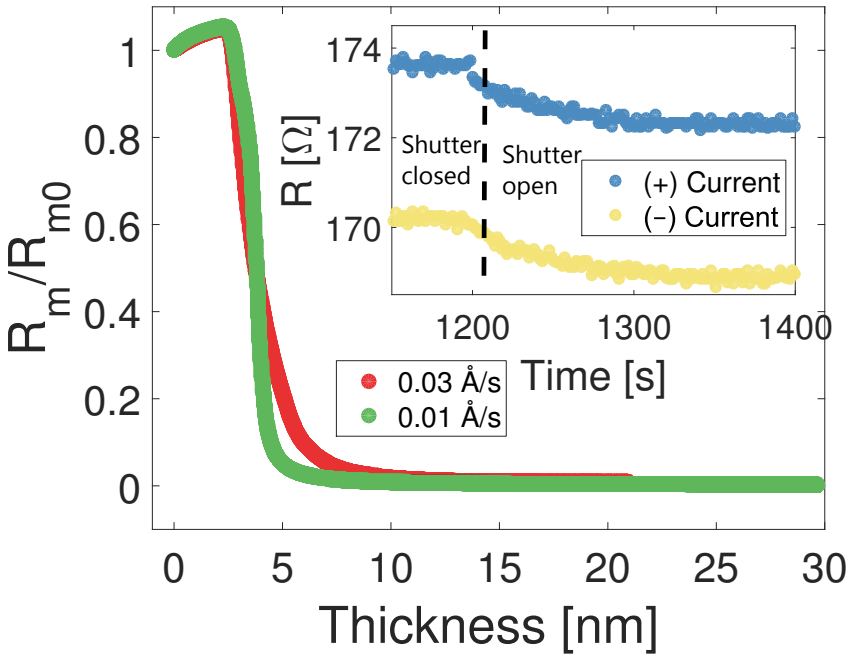


Figure 3.41.: Measurement of the evolution of the resistance during deposition of Ag on p-Si versus film thickness. Note the sharp decrease after depositing 3 nm . The inset shows the resistance change with opened shutter on n-Si.

A source of resistivity change could be induced by the light emitted by the evaporation source when the shutter is opened as it could generate charge carriers. In the inset of Figure 4 one can see that there is a resistance change after the shutter is opened, but the change is negligible and does not change the observed resistance characteristics.

The dopant concentration plays the most important role in understanding the resistance behaviour of the underlying Si. Thus the dopant concentration was changed by using a 3-5 kΩ·cm 111-Si wafer with a dopant concentration of 10^{12} cm^{-3} which is 4 orders of magnitude lower compared to the higher doped Si which has been used before. As visible in figures 3.41 and 3.42, the relative resis-

tance during evaporation of Ag on p- and n-type Si behaves differently for the two types of doping. Ag on p-type silicon shows the mentioned slight increase before the first drop, while Ag on n-type silicon shows a slow decrease only until a first sharp decline in resistance is visible, which takes place at more than twice the layer thickness than for p-type silicon. For high-resistivity p-type Si, a new region can be identified: until about 3 nm, the resistance increases slightly up to a maximum in resistance, followed by a sharp decrease of the resistance by about one order of magnitude. Within the next 4 nm, the resistance only decreases slightly until a second point is reached where another strong decrease in resistance is observed. For low doped Si wafers, we see a significant increase in resistance within the first nm followed by a massive drop at about 2.25 nm which is stronger pronounced in comparison to the drop of the highly doped Si. Also a second drop in resistance is visible at around 7 nm.

The resistance as function of the metal thickness can be well explained by assuming the following mechanisms: i) for not very high doped Si the current path is located next to the Si surface. This can be also proven as even in case of negligible metal deposition the resistance changes significantly. ii) Schottky-barriers forms under the surface regions where an Ag droplet condensates able to induces a space charge region which forms a conductive inversion layer [151]. It is well known that the space charge region width can be significant, for instance the width for Ag on p-type Si (with 4 kΩ·cm resistivity) amounts to 8.4 µm [152].

Therefore the first percolation points (marker (a) in figure 3.42) visible for Ag on p-type Si most likely indicates the connection of former separated space charge regions able to transport minority carriers within the conductive inversion channel as schematically shown in figure 3.38b. We suspect that the forming of the inversion channel only occurs in case of p-type silicon as here the difference in the Fermi level of the metal and p-type Si is significant. The lower the p-type dopant concentration the more mobile minority carriers can be generated resulting in a more pronounced drop in resistance as seen from figure 3.42. In contrast for n-type silicon, the band bending is not strong enough to accumulate mobile minority carriers above the Fermi level and only the classical percolation point occurs. The second percolation point (marker (b) in figure 3.42) is

the classical one, were the metal islands which are already substantially thick (mean thickness 7 nm) connect and reduce the resistance by several orders of magnitude.

To compensate any effects of the current direction we measured the current in both directions for each point, resulting in no differences as shown in figure 3.42.

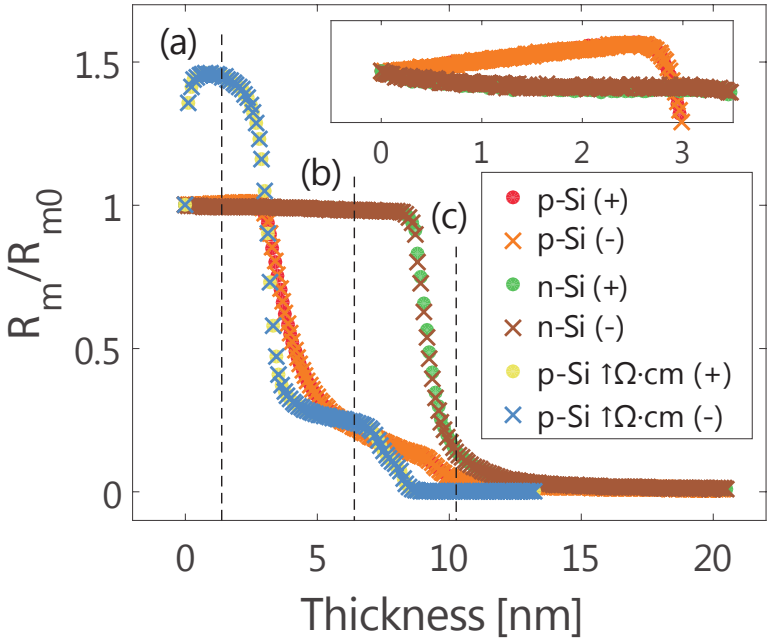


Figure 3.42.: In-situ measurement of the relative resistance for p and n-type silicon, both current directions measured, indicated by (+) or (-) in the legend. The p-Si with a high resistivity (3000 – 5000 $\Omega \cdot cm$) is indicated by $\uparrow \Omega \cdot cm$. Markers (a) and (b) show the onset of the first and second percolation region, respectively. Marker (c) shows the end of percolation region 2 where the major current transport occurs in the metal. Only each 5^{th} data point is shown.

To the best of our known the increase of the resistance during the first monolayers is not analysed elsewhere in literature. Data about the conductivity of titanium and vanadium films on carbon and silicon dioxide substrates is reported in [153], where a similar increase of the resistance at the very beginning of film growth is observed which, however, was not addressed by the authors. A possible explanation for the initial increase of resistance on p-type Si is that the formation of the localized Schottky barriers before the first percolation point may effectively scatter the charge carriers. This suggested scattering mechanism dif-

fers significantly from the type as claimed by Jnawali *et al.* [154]. Hence, the slow decrease before the percolation point is most likely attributed to the fact that charge carriers are going partially through already metallized regions but still has to pass through the highly resistive semiconductor. The more of the surface is covered, the more the current is able to flow through low-resistivity regions which slightly decreases the resistance until the percolation point.

Power-law behaviour

Another interesting interpretation of the measured data is possible by the analysis of the double logarithmic plots.

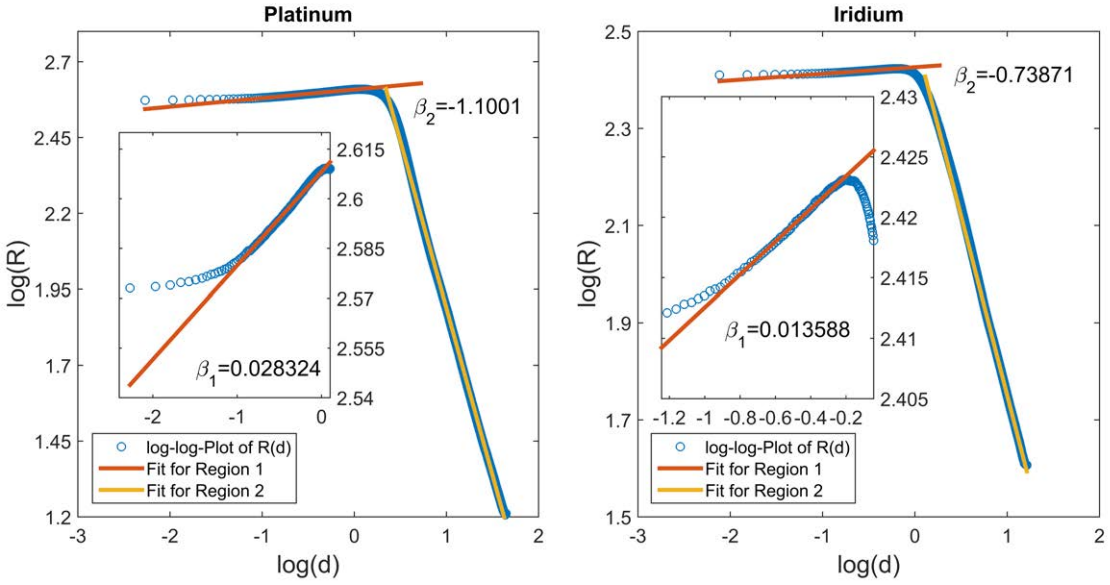


Figure 3.43.: Double logarithmic plot of R(d) for Pt and Ir with linear fits

Figure 3.43 shows the time-dependent resistance of Pt and Ir in a double logarithmic plot. As predicted by scaling theory [150, 155], the fractional coverage x during evaporation is proportional to $A \cdot d^{\beta}$ with A being a constant, β being a fixed scaling coefficient, and d being the thickness. As both the increase of the resistance as well the decrease after percolation is caused by the growth of islands on the silicon surface, a power law behaviour of the resistance is expected. If we assume that the thickness-dependent resistance R(d) evolves proportional to d^{β}, a $R(d)$-plot in double logarithmic representation is a linear curve where the slope is β. The first fit shown by the red curve in Figure 3.43 corresponds to the first

monolayers of evaporation where the resistance is increasing and the second fit (yellow line) belongs to the case after percolation. Similar plots have been made for in-situ resistance measurements [156].

Table 3.5.: Extracted Power law factors β_1 and β_2. β_1 corresponds to region 1 and β_2 to region 2 of the film growth characteristics.

Material	β_1	β_2
Titanium	0.00475	-0.300
Silver	0.02136	-3.473
Gold	0.00553	-1.549
Platinum	0.02832	-1.100
Iridium	0.01359	-0.739
Chromium	0.00064	-0.029

As already mentioned, this confirms our assumptions that i) the relevant growth mode during evaporation is the Volmer-Weber-mode with small islands and ii) the resistance increase before the percolation threshold is due to small metallic islands. The values for the power law factors β_1 and β_2 depend heavily on the metal which is evaporated. Figure 3.44 shows also double logarithmic plots for $R(d)$ in this case for Cr and Ag. Notably, Cr shows a very low percolation threshold as depicted in the inset of figure 3.44 (left) as well as in figure 3.40. The power law factors β_1 and β_2 of all employed metals are enlisted in table 3. β_2 can be attributed to resistivity of the thin metal (which can be substantially different compared to the bulk value). While Ag and Au have high absolute values for β_2 corresponding to the low resistivity of these metals as a bulk (15.87 nΩ·cm for Ag and 22.14 nΩ·cm for Au [21]), for Cr a much lower absolute value of β_2 is expected as its higher bulk resistivity is 125 nΩ·cm leading to a 120 times lower β_2 value than for Ag. For Ir one would expect a lower value for β_2 as its resistivity is 420 nΩ·cm. β_1 is more difficult to interpret as it involves all the described processes which induce the resistance increase by the first monolayers.

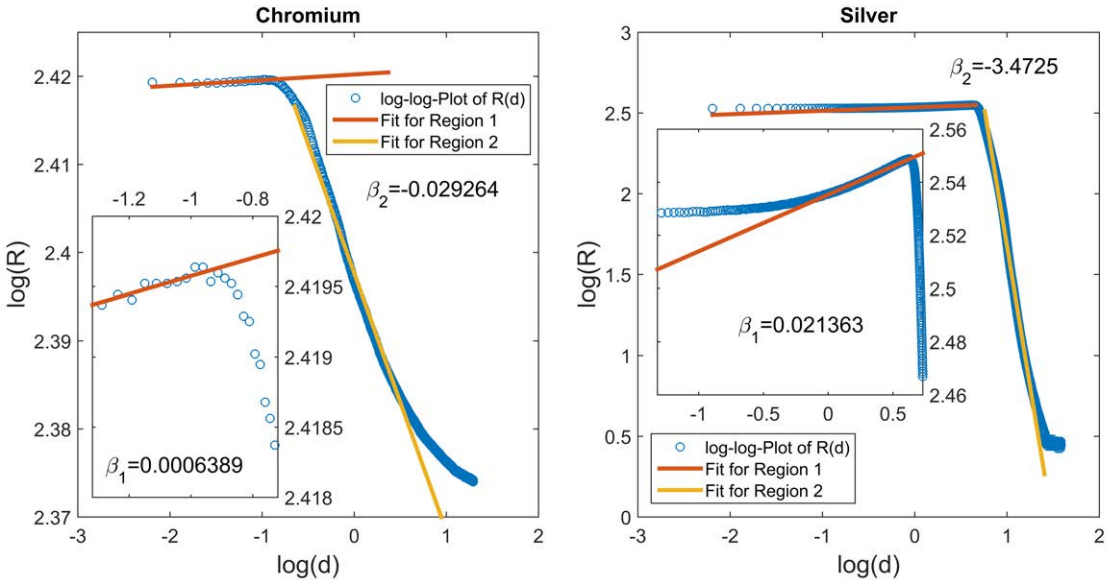


Figure 3.44.: Double logarithmic-Plot of R(d) for Cr and Ag with linear fits.

AFM Analysis of silver films

Ex-situ AFM imaging has been performed for deposited Ag films. Figure 3.45 shows the surface topology of Ag on Si (111) after deposition of 3 nm (left) and 6 nm (right) which correspond to different states in growth regions as discussed above. At 3 nm thickness, the island formation is clearly recognizable. This region corresponds to a high resistance in the $R(d)$-plot as the primary conduction takes place by the silicon substrate without connection of the islands. In contrast, at 6 nm the islands are connected and form a sponge-like structure, affirming the "kinetically limited layer growth mode" for Ag on Si(111) at RT as mentioned by Gergen *et al.* [146]. Electrically, this layer is conductive and therefore the resistance decreases sharply. This observation confirms that percolation takes place during the growth of silver films.

Conclusion

A possible outlook on this study would be the utilization of other materials for the evaporation process to identify further candidates which show electrical continuity at very low thicknesses. Furthermore, a temperature-dependence study

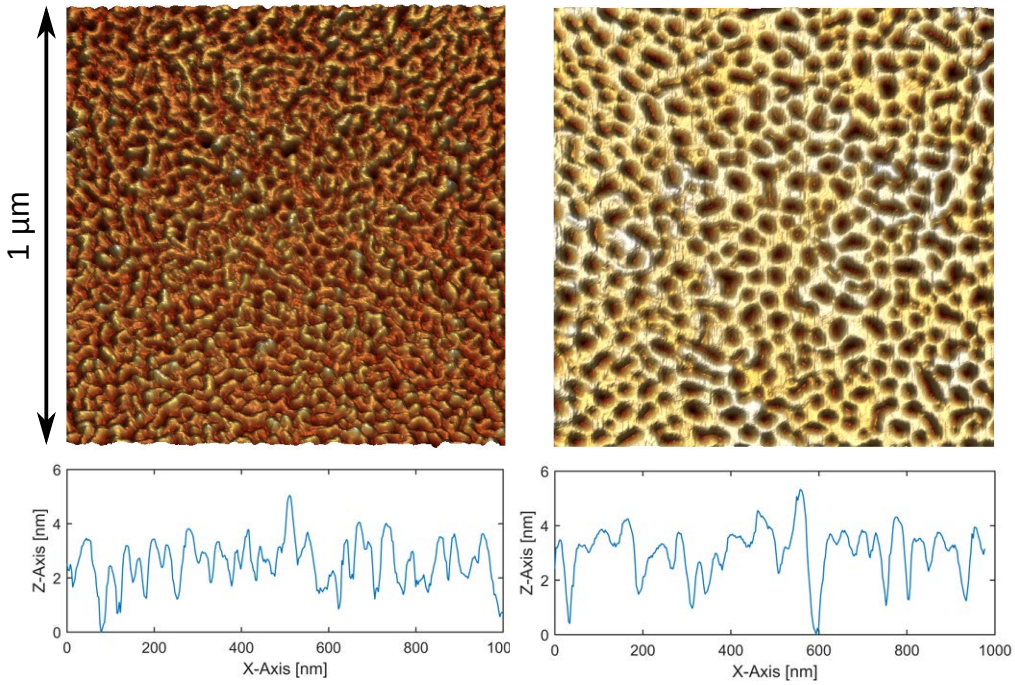


Figure 3.45.: AFM images of Ag films with 3 nm (left) and 6 nm (right) thickness. Although maximum height values for both samples are similar, the height values are more evenly distributed around the mean level for the 3 nm compared to the 6 nm sample, thus resulting in a different overall colour impression.

on the growth modes would be desirable [146] including investigations about the annealing behaviour of these thin films as a different film growth mode is expected at different temperatures. Also other semiconducting materials like Germanium or III-V-semiconductors could be employed to acquire knowledge if the observed effects also take place on other semiconductor substrates as expected. In summary, the in-situ resistance behaviour of ultra-thin metal films during growth on hydrogen-terminated Si(111) for Ti, Ag, Au, Pt, Ir and Cr at very low evaporation rates were discussed. From the resistance versus thickness curves Cr shows the earliest electrical continuity already achieved at 1 ML. It is shown that the qualitative characteristic of the resistance during evaporation is heavily dependent on the type of the evaporated metal, as well as on the dopant type and dopant concentration of the Si substrate. Remarkable, on p-type Si two drops in resistance have been found dependent on the dopant concentration. It has been found out that the first electrical percolation point differs from the morphological percolation point. The very high resolution of data points allows the

investigation of an unusual resistance increase during the first monolayers on p-type silicon in great detail. The formation of Schottky barriers inducing charge regions at the Si surface has been suggested to be the main mechanism of these phenomena.

3.4. XPS of an ultra-thin Cr layer under Al_2O_3 on Si(111)

XPS measurements are discussed in the following for better understanding of the best performing one-sided Cr-layer ZrO_2 stack.[2] The same highly doped Si wafer was utilized as for the MIM capacitors. 150 nm Cr were deposited by sputtering and transferred within 1 min into the ALD or XPS vacuum system. Four samples were analysed by XPS: i) sample with Cr only, ii) sample with pure ZrO_2 and iii) two samples with Cr and 15 cycles of ZrO_2 on top which is thin enough to detect the Cr-ZrO_2 interface without etching. One of the two Cr-ZrO_2 samples was annealed for 2 minutes at 500 °C in Ar atmosphere to investigate the effects of thermal treatment.

In figure 3.46a, subfigure i), the spectrum of the $Cr2p_{3/2}$ core level of pure Cr is shown. The pronounced peak is indicating unoxidized Cr metal with only a small shoulder corresponding to Cr_xO_y compounds. This confirms that the Cr layer already oxidises partially during sample transfer in air. If 15 cycles of ZrO_2 are deposited onto the Cr layer, the oxide concerning feature is increasing significantly (figure 3.46a, subfigure ii) which means that during deposition of ZrO_2 the Cr layer is strongly oxidized by the ALD process. This is most likely due to H_2O vapour used as oxidizing agent in the ALD process delivering oxygen in excess, which is rather not used for the formation of zirconium oxide but for the chromium oxide layer instead. By applying an Ar annealing the oxidation process is even stronger as the metallic state decreases further and instead a strong oxidized component is visible (figure 3.46a, subfigure iii). Hence, we conclude that the annealing, even in the non-oxidising atmosphere of argon, leads to fur-

[2] The work in this section is published in[157].

ther reaction between the zirconium oxide and the chromium layers including the diffusion of oxygen interstitials to the ZrO_2/Cr-interface.

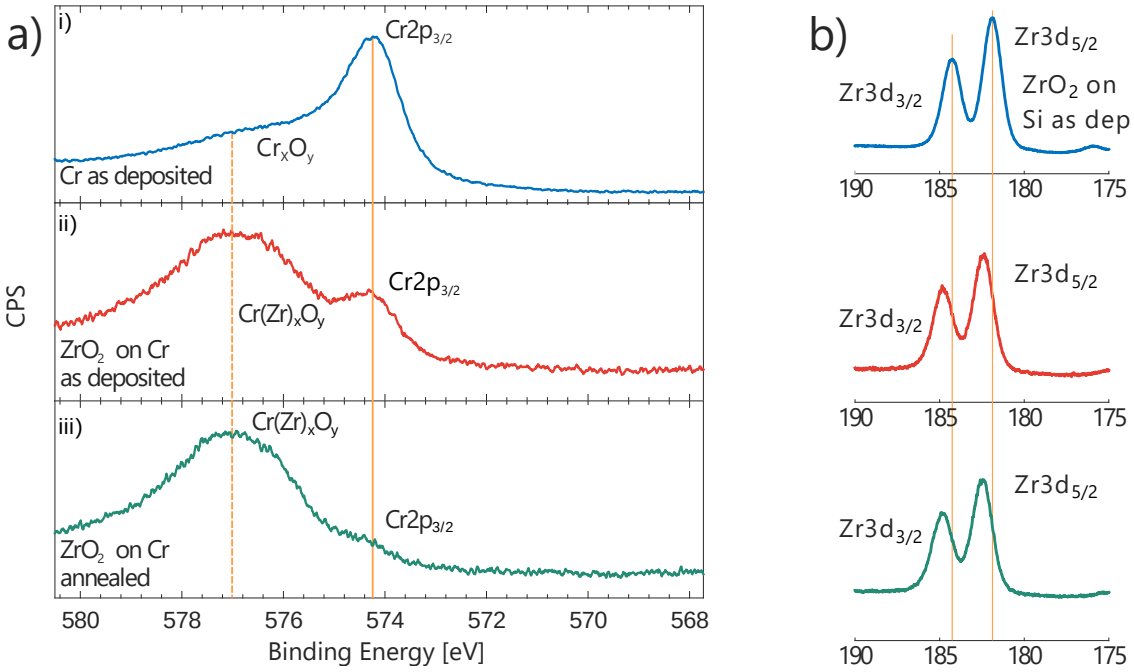


Figure 3.46.: XPS spectra showing the $Cr2p_{3/2}$ (a) and the $Zr3_d$ core-level (b). i) Cr as deposited, ii) ZrO_2 on Cr as deposited, and iii) ZrO_2 on Cr annealed for 2 minutes at 500 °C in Ar at-mosphere.
Subfigure i) of b) shows the Zr3d state of 20 nm ZrO_2 as deposited on Si.

In the figure 3.46b, the evolution of the $Zr3d_{3/2}$ and $Zr3d_{5/2}$ core level is shown. The peaks for the ZrO_2/Cr samples are slightly shifted to higher binding energies in comparison to 20 nm ZrO_2 deposited on Si (figure 3.46b) which clearly indicates that $Cr(Zr)_xO_y$ compounds are already formed during ALD at the Cr/ZrO_2 interface as Cr has higher electron negativity than Zr [21].

3.5. SCM of ultrathin metal/ALD-oxide stacks on Si(100) and Si(111)

The Scanning Capacitance Microscopy technique mentioned in sections 1.3.11 and 2.9 is exploited to analyse MOSCAP stacks with and without an intermediate ultrathin metal layer. After cleaning and BHF dipping to remove the native oxide (like in the former sections), silicon samples are put into the ALD load lock. A

part of the samples receive a chromium layer by e-beam evaporation (see section 2.1.3) with about 1 ML (0.3 nm) thickness. Afterwards, aluminium oxide (Al_2O_3) is deposited by ALD (also by the same process as in the previous sections), resulting in a thickness of 2 nm. The samples are directly transferred from the e-beam evaporation chamber into the ALD chamber to prevent oxide formation of the Cr layer. After the deposition of the oxide layer, the samples are put out the ALD chamber and placed in the SCM setup, where they are characterised.

In figure 3.47, CV curves of samples with Si(100) and Si(111) and with or without chromium interlayer are shown. Those measurement curves are the product of a series (30-100) of single measurement which are then averaged. Figure 3.47a and 3.47b are very similar, which means that the electrical behaviour of the MOSCAP (see section 1.3.3) does not change with crystal orientation of semiconductor surface.

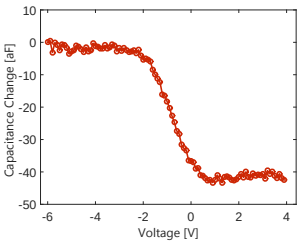
On the other hand, figures 3.47c and 3.47d are very different in their electrical behaviour. While figure 3.47d looks like an ordinary MIM capacitor (see section 1.3.4), figure 3.47c displays a curve one would expect for a low-frequency measurement of a MOSCAP as explained in section 1.3.3.

[8] predicts a very high mobility for a Si(111) surface which is capped by an ultra-thin metal layer which is assumed to be the explanation for the behaviour of the sample measured for figure 3.47c. Charge carriers are fast enough (due to the a unusual high mobility in silicon) to prevent depletion, therefore it looks like low-frequency quasistatic CV measurement like in figure 1.7.

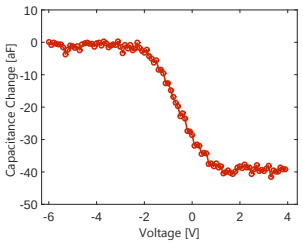
3.6. MIS/MIM-Transition by varying interfacial metal layer thickness

The introduction of ultra-thin metal interlayers into a MOSFET gate stack is complementary to a transition of Metal-Insulator-Semiconductor (MIS/MOS) capacitor to a Metal-Insulator-Metal (MIM) capacitor. A description of those two capacitor types can be found in sections 1.3.3 and 1.3.4. Although an intensive enquiry

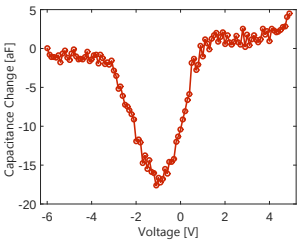
a) Si(111) No Cr Typical "high frequency" MOSCAP-CV-curve



b) Si(100) No Cr Typical "high frequency" MOSCAP-CV-curve



c) Si(111) with 1 ML chromium Looks like a "low-frequency" quasistatic CV-measurement suggesting high mobility of charge carriers



d) Si(100) 1 ML Chromium Looks like a MIM curve As theory predicts, Si(111) is needed

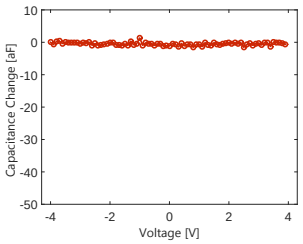


Figure 3.47.: CV curves measured by capacitive AFM of Si(100) and Si(111) samples with and without an interfacial monolayer (0.3 nm) of chromium.

has been done, no previous work studying the transition from MIS to MIM could be found so far in literature.

Silicon(111) (p-type) was used to investigate this transition. The samples were dipped in buffered hydrofluoric acid, after which they were transferred into the ALD load lock. A varying thickness (0-330 nm) of chromium metal was then deposited onto the samples by means of e-beam evaporation (see section 2.1.3). On top of this metal layer (or in the case of no metal evaporation, onto the semicondcutor surface), 20 nm of Al_2O_3 where deposited by means of ALD. Using lithography, Pt metal contacts where formed on top of the oxide layer by sputtering and subsequent lift-off. The used metal electrodes where circular in shape and 50 µm in diameter.

The electrical characterisation was performed by the already in section 2.5 described probe station with a measurement frequency f = 1 MHz at room temperature. The resulting curves are shown in Figure 3.48.

The thickness of the chromium interlayer varies between 1 nm and 330 nm, a sample with no chromium is also made for comparison purposes. It is clear that the sample without chromium behaves like an ordinary MOS capacitor while the

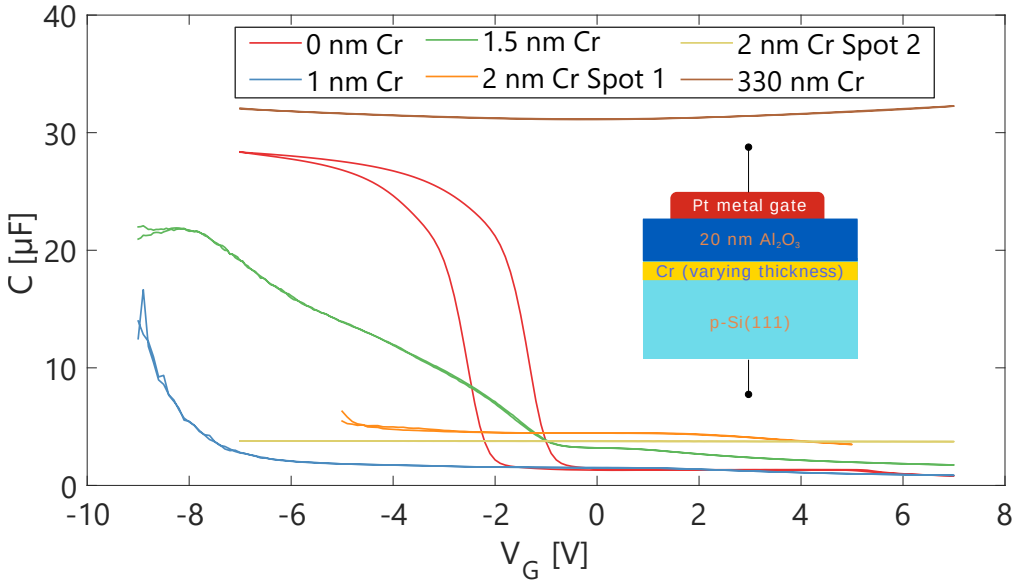


Figure 3.48.: The impact of the thickness variation on the CV curve, ranging from no Cr metal interlayer (0 nm) to a very thick layer (330 nm)

sample with a very thick Cr layer (330 nm) acts like a MIM capacitor. What is interesting is the transition which is represented by the sample with only some layers of chromium in Figure 3.48. Figure 3.49 shows a zoomed part of Figure 3.48. The 1 nm sample (blue) seems still like a MOS capacitor, but with a very strongly shifted flat band voltage (in the negative direction). The extreme left end of the curve shows something like the onset of a MOS depletion. The 1.5 nm sample (green) again still looks more like a MOS capacitor, but in this case the flat band voltage is not shifted that much while the depletion mode is lasting for a long voltage span. For the 2 nm sample, two somewhat different zones have been found on the sample so figures 3.48 and 3.49 depict two different curves (ochre and orange). At this metal thickness, the curves already looks much more like a MIM capacitor, but with a very low capacitance density compared to the sample with 330 nm Cr (brown).

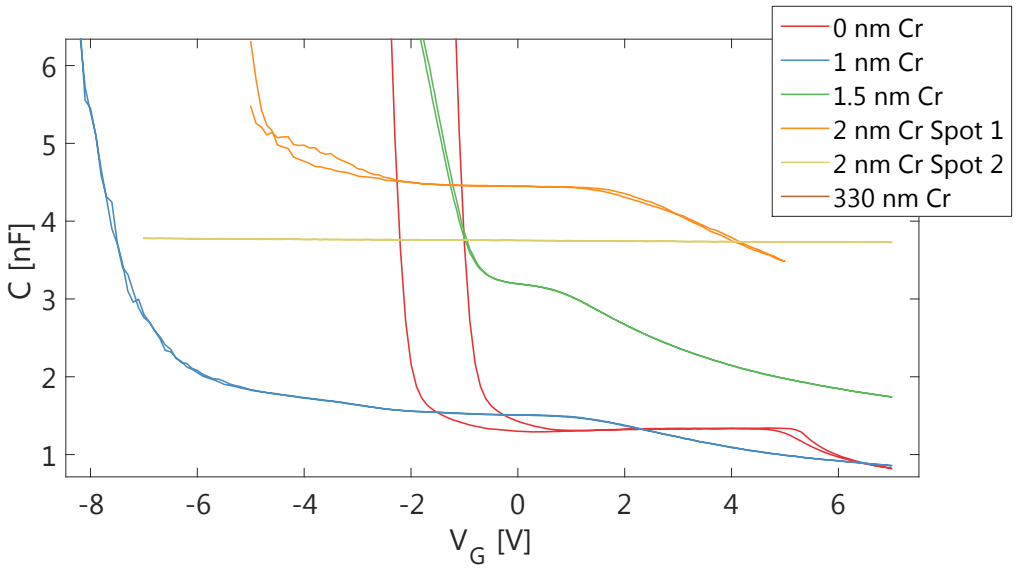


Figure 3.49.: Enlarged section of figure 3.48

3.7. SB-MOSFET with interfacial chromium layer on Si(111)

Following section 3.6 where the transition between a MOS and MIM is analysed, this section discusses the transition behaviour of a MOSFET which contains an inserted metal layer, similar like in the former section. Three samples are processed and analysed, ranging from no interfacial layer to a thick layer of chromium, see table 3.6 and figure 3.50. The used lithography layout can be found in the appendix A.1.2.

The MOSFET structure is very similar to the structure described in section 3.2, containing a bilayered oxide as a gate and Si(111) as semiconducting material. Alumina is deposited by ALD at 250°C to obtain a thickness of 15 nm while only 3.8 nm of yttrium oxide are deposited. Similar to the former section, the interfacial layer was deposited after a BHF-dip of the sample before it was transferred into the load-lock of the ALD/e-beam system. The first oxide (yttrium oxide) was deposited directly after the deposition of the interfacial metal layer without breaking the vacuum.

The electrical characterisation was again performed by the already described probe station at room temperature. For the V_{GS}-I_D measurements, the source-

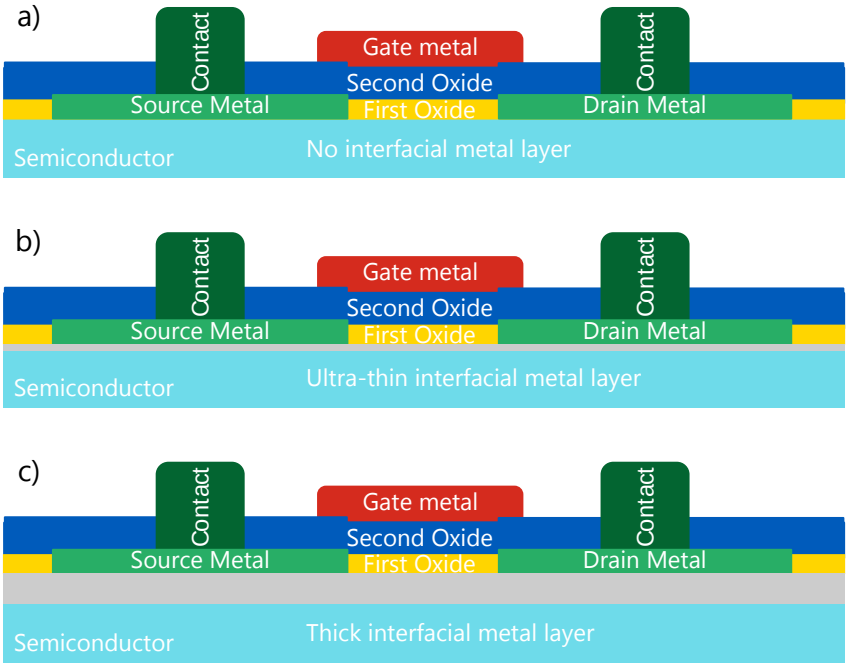


Figure 3.50.: Schematic of a MOSFET without, with a thin and with a thick interfacial metal layer

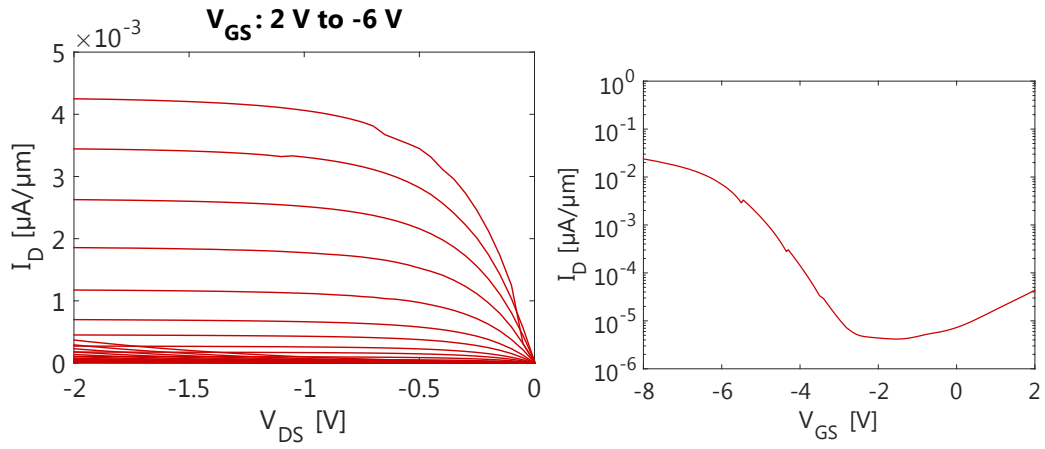
Table 3.6.: List of the thicknesses of the interfacial layer

Evaporation Time [s]	Thickness [nm]
0	0
30	0.33 nm
2000	22.2 nm

drain voltage V_{DS} was kept at -0.5 V for all samples, the measurement frequency of the capacitance was f = 1 MHz.

i) No interfacial metal layer

At first, a MOSFET with no intentional interfacial metal layer was produced and characterised. This corresponds to the sample with no Cr in section 3.6. The measured sample was a rectangular shaped MOSFET (see the appendix A.1.2) with a gate length of 30µm.



(a) Output **(b)** Transfer

Figure 3.51.: V_{DS}-I_D and V_{GS}-I_D of a MOSFET without interfacial metal layer

The MOSFET characteristic is quite similar to samples like in section 3.2, but the drain current is very low, being 3 orders of magnitude lower than in the samples in section 3.2. This may be attributed to processing problems, contact problems of the S/D contacts or a bad gate/semiconductor interface. Nevertheless, it still looks like a proper MOSFET device. Figure 3.51 shows the V_{DS}-I_D and V_{GS}-I_D of a MOSFET without interfacial metal layer while figure 3.52 depicts the mobility depending on the gate-source voltage V_{GS}. The CV curve in figure 3.53 does not exhibit any unusual features, the flat band voltage V_{FB} lies around +0.5 V.

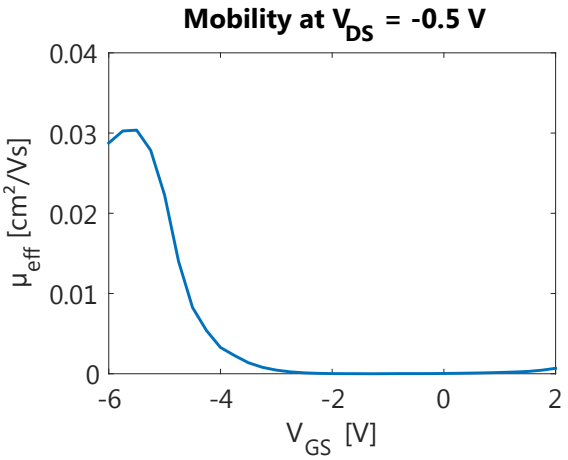


Figure 3.52.: Mobility μ_{eff} of a MOSFET without interfacial metal layer

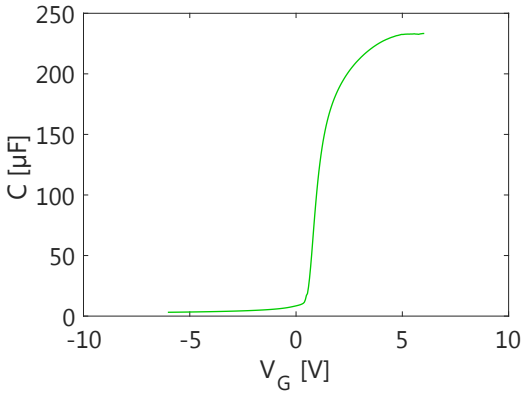


Figure 3.53.: C-V_G curve of the gate of the MOSFET without interfacial metal layer

ii) Thin interfacial layer - 0.3 nm Cr (30 s)

To study similarities between the MOS/MIM-transition section 3.6, a sample with MOSFETs is created where a 0.3 nm layer of Cr in incorporated. This layer changes the MOSFET properties already dramatically. The measured sample was a rectangular shaped MOSFET (see the appendix A.1.2) with a gate length of 20µm.

The resulting curves are very interesting, see figure 3.54 where especially the V_{GS}-I_D graph shows an unusual appearance. The maximum drain current (which is again pretty low at 3 x 10^{-4} µA/µm) shows a minimum at a gate-source voltage V_{GS} of -1 V. The V_{DS}-I_D curve does not show a saturation behaviour as expected by a MOSFET and as seen for the sample without chromium, it exhibits on the other hand a much more linear behaviour.

Also the calculated mobility, shown in figure 3.55, is extremely low, although one has to take into account that the mobility calculation in section 2.6.2 incorporates values like the charge carrier density in the channel which is taken from the corresponding CV-curve. This is a rough estimation; in this MOSFET it is not clear where the charge carriers are located which conduct current from the source to drain. It may also be possible that the current is conducted in the ultra-thin metal film between the S/D contacts, where the probably less charge carriers are existent because of the low thickness (although it is a metal which typically has a very high charge carrier density). The linear behaviour of the V_{DS}-I_D graph

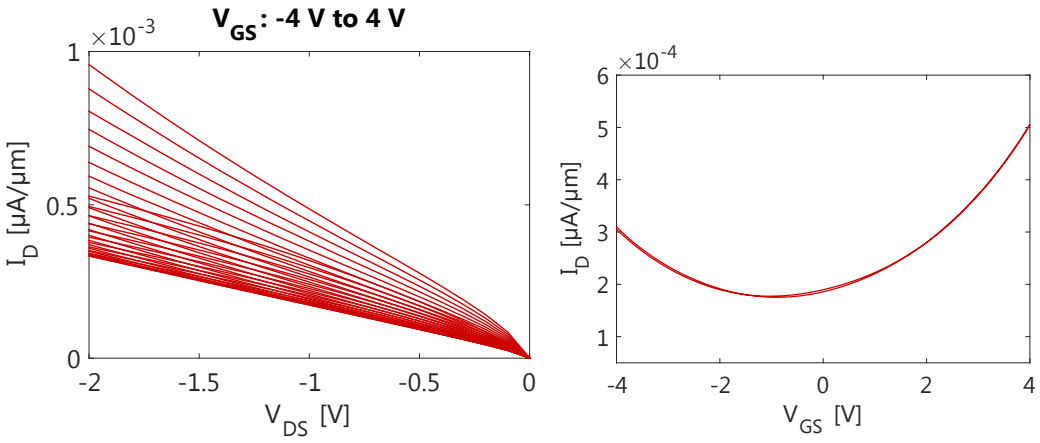


Figure 3.54.: V_{DS}-I_D and V_{GS}-I_D of a MOSFET with a very thin (0.3 nm) interfacial Cr metal layer

may be a hint for a high mobility, as no saturation of the current can be found. Unfortunately, with this structure a more profound analysis of this issue is not possible.

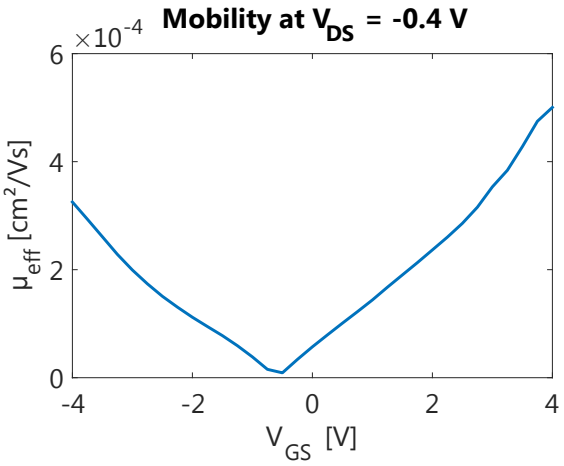


Figure 3.55.: Mobility μ_{eff} of a MOSFET with a very thin (0.3 nm) interfacial Cr metal layer

Looking at the CV-curve in figure 3.55, one may consider this still as in the norm for a MOS-like gate capacity, although the flat band voltage seems to be shifted to a value bigger around 2 V.

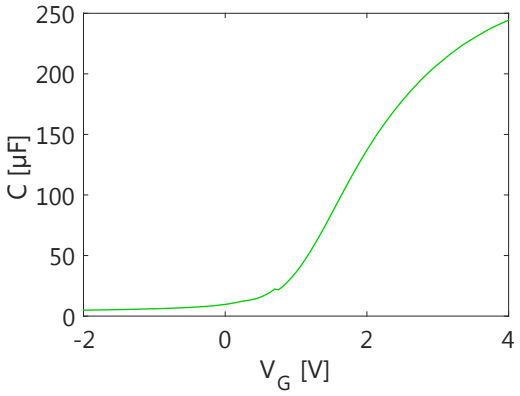


Figure 3.56.: C-V_G curve of the MOSFET gate with a very thin (0.3 nm) interfacial Cr metal layer

iii) Thick interfacial layer - 22 nm Cr (2000 s)

A comparatively thick metal layer changes again the electrical behaviour of the MOSFET (here again a rectangular MOSFET with 20 µm gate length is characterised). The 22 nm thick interfacial layer is already enough to shortcut the channel and to create a V_{DS}-I_D curve (see figure 3.57) which is typical for a short-cut situation. This curve also renders the calculation of the mobility useless; thus the mobility graph which is shown for the other two samples is omitted here. V_{GS}-I_D shows a practically constant drain current I_D which is also caused by the short-cut situation.

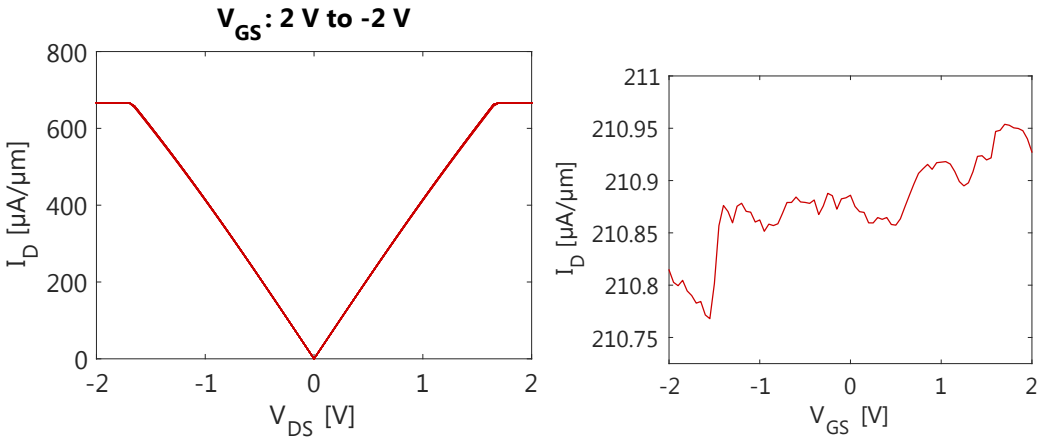


Figure 3.57.: V_{DS}-I_D and V_{GS}-I_D of a MOSFET with a very thick (22 nm) interfacial Cr metal layer

The CV-curve in figure 3.58 is a typical sample for a MIM capacitor, as one

would expect from such a thick interfacial layer between the oxide and the semiconductor.

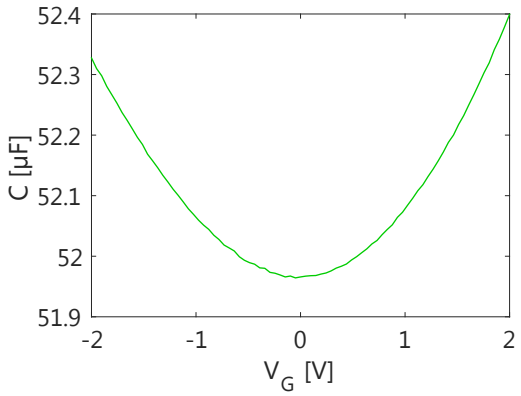


Figure 3.58.: C-V_G curve of the MOSFET gate with a very thick (22 nm) interfacial Cr metal layer

3.7.1. Summary

Comparing the three MOSFET devices with no metal layer (i), a thin (ii) and a thick one (iii), all of them behaved mostly like expected. It seems that there were some production problems, especially with the first sample, where the current is unusually low. The thick layer sample was also very like expected, basically a short-circuited device. The most interesting was probably the one with a very thin layer. First even this very thin layer of 0.3 nm, which approximately corresponds to a monoatomic layer, is able to dramatically change the electrical characteristics of the MOSFET device. The CV curve itself of this device did not change that much; only the flat band voltage was shifted to a positive value. An hypothesized high-mobility MOSFET as claimed by [9] based on the paper by [8] could unfortunately not be confirmed. Further experiments with a bigger variation of the thickness could be sensible, especially with metal thicknesses in the order of 1-5 nm.

4. Summary, Conclusion and Outlook

4.1. Reiteration of the motivation of this work

In semiconductor science, the trend is going to further miniaturisation and further scaling of devices. Future technologies like ubiquitous computing or the Internet of Things (IoT) need cheap, small and yet fast devices. It is very important for the progress of scaling to increase the mobility of the most important single active semiconductor element in a microchip, the FET device.

In the search for a higher mobility in Si-channel MOSFETs, several steps have already been done. Based on the paper by Kim [8], the idea was born to establish a high-mobility MOSFET based on the promising concept of integrating a ultra-thin metal layer between the semiconductor and the gate oxide, which should lead to a hybridisation of states. Kim *et al.* stated that electrons with a nearly linear dispersion and an effective mass of about $1/20^{\text{th}}$ compared to bulk Si are achieved if a ultra-thin metal layer is brought in contact with Si(111). This effect is accounted to an overlapping of surface states at the silicon-metal interface.

Equipped with this idea, this work tried to implement this concept, but it was clear that a lot of preliminary work was needed to approximate this task. Dragoman *et al.* did fundamental experiments in their paper [9] by establishing such an high-mobility device. This paved the way for further progress in the subject of silicon-based high mobility MOSFET as well as provided a basis for this work.

The scope of this thesis was extended to a broader thematic spectrum, e.g. rhodium germanide Schottky contacts were also considered a sensible subject;

thus some parts of this work have been more a fruitful side-project than an actual step in the way to establish a MOSFET with an interfacial metal layer.

4.2. Summary

This document starts by the introductory chapter 1, where several theoretical aspects in connecting to this work are discussed. First, a brief review of the properties of the two mostly used semiconductor materials, silicon and germanium is given. The connection of a metal and a semiconductor, a Schottky contact, is then described as it is a prerequisite for a so-called Schottky-barrier MOSFET. This section also includes the thermionic emission theory, which is extensively used by later for analysing Schottky contacts.

In the next step, two capacitive devices, Metal-Oxide-Semiconductor (MOS) and Metal-Oxide-Metal (MIM) capacitors are introduced. This forms the theoretical background for an discussion of MOSFET gate oxide structures with and without an interfacial layer. The FET principle together with the special case of a MOSFET and the mobility in those devices are the next topic in this first chapter. After that, the chapter emphasizes on the formation of high-k oxides by Atomic Layer Deposition (ALD) and the characterisation of those by means of X-ray Photoemission Spectroscopy and Scanning Capacitance Microscopy. For all of those experimental methods, a brief introduction in their physical and/or chemical background is given.

After introducing various concepts, chapter 2 extensively discusses the experimental issues of this work. Embedded in the formation of contacts and oxides, several techniques of the field of semiconductor science and nanotechnology are covered. Deposition of metal by e-beam evaporation and sputtering, lithography or plasma oxidation are examples of topics connected to the constitution of Schottky-barrier contacts while the oxide formation section greatly emphasizes on the parameters of the various used ALD processes.

The chapter continues by explaining the schematics of the Field-Effect transistor (FET) device used in this topic, containing a profound illustration of the

various steps in processing such an device. The electrical characterisation and parameter extraction are the next topics which are a key issue in generating information about the performance of the processed devices in terms of mobility or drain current.

To complete the experimental section, the already theoretically discussed techniques like SCM and XPS are described from an experimental point of view. A description of another experimental method, Time of Flight Secondary Ion Mass Spectroscopy (TOF-SIMS), is also contained in this chapter.

The measurement of the resistance of a thin metal film in-situ during evaporation onto a semiconductor surface is also discussed in great detail, as it forms a major part of the results of this thesis.

Chapter 3 presents the results obtained during the dissertation. At first, results regarding Schottky contacts are written. The experimental determination of suitable contacts for the following MOSFETs are described in section 3.1.1. This was deemed important, as Schottky barrier contacts which show good properties (e.g. the on/off ration) even without any annealing are needed the MOSFET devices mentioned later in this chapter. During the work, the interesting subject of rhodium germanide Schottky barriers showed up, which why it is discussed as a separate section 3.1.2. In this section, contacts between rhodium (a platin-like metal) and Ge (100) surfaces are extensively discussed, covering the subjects of its deposition and the characterisation by means of electrical measurements, TOF-SIMS, XRD, HR-TEM, AFM and optical microscopy. The formation of RhGe Schottky barriers has never been described in literature, therefore this section is mostly exploratory and not focusing on the applications of those contacts. Many of the measurements have been performed for samples which have been annealed in N_2H_2 at different temperatures ranging from 450 °C up to 800 °C, which is aimed as exploring the optimal processing parameters for this type of contact. A formation of polycrystalline Rh-germanide Rh_xGe_y phases has been proven. At 500 °C germanidation temperature, an effective SBH of 0.59 eV is extracted together a high current ratio of $5{\times}10^3$ and a remarkable low ideality factor of 1.07.

Having discussed the connection between a metal contact and the semiconductor, the next logical step was the development and manufacturing of SB-MOSFETs without an interfacial metal layer in section 3.2. From a processing point of view, it was rather successful, but this MOSFET concept still has a comparable low mobility (highest value 24 cm^2/Vs). The highest drain current was 8 µA/µm, the highest On/Off-ratio $2 \cdot 10^3$. Regarding this very simple design (no etching into the semiconductor bulk, no annealing) compared to other MOSFETs, these values are still remarkable. Most of the results in this sections were MOSFETs based on n-type Si (PFET); NFETs on p-type Si have been also tried but this approach produced less promising results.

A section (3.3) of a different nature was the growth of ultra-thin metal layers, where the in-situ resistance behaviour of ultra-thin metal films during growth on hydrogen-terminated Si(111) for Ti, Ag, Au, Pt, Ir and Cr at very low evaporation rates was discussed. Several resistance versus thickness curves were made, were resistance was measured in-situ between two contacts on a Si(111) sample while a e-beam metal eposition process onto the sample was going on. The earliest electrical continuity already achieved at 0.3 nm while using chromium metal. The specific properties of the evaporated metal play a crucial role concerning the qualitative characteristic of the resistance during evaporation. Furthermore, the dopant type and dopant concentration of the Si substrate are important factors which change the resistance behaviour. The measurements were conducted with a high resolution not found so far in literature, with several measurements per second, allowing a to measure the resistance change based on a fraction of a nanometre of thickness growth. A very interesting feature that was found during these experiments was the increase of the resistance during the first few atomic layers of growth, which was also theoretically discussed to be caused by effects of band bending.

Along with the in-situ resistance measurement, a short AFM analysis of a deposited Ag-film was done. The thickness-dependent resistance curves where also analysed mathematically and a power-law behaviour was found, which corresponds to previous findings of other authors.

As a preparation for the integration of an ultra-thin metal film into the gate

stack, XPS measurements of such a metal layer based on chromium metal capped by zirconium oxide (ZrO_2) was performed in section 3.4. Being of essential nature for the conclusions which can be drawn from this work, those measurements showed that the deposition of an oxide by ALD onto a ultra-thin metal layer oxidises this layer, at least partially. A diploma thesis by S. Simsek [31], where MIM-capacitors with different electrodes are discussed, is based to some extent on this section.

Thanks to a fruitful collaboration with Prof. Smoliner, the highly sophisticated technique of Scanning Capacitance Microscopy (SCM), or also known as Capacitive AFM, was used on ultrathin metal stacks in section 3.5. A similar stack like in the previous section (Cr and Al_2O_3) was deposited onto Si(111) and Si(100). The findings of this section were quite remarkable: The mobility of the charge carriers depends seemingly on the crystal orientation of the silicon interface, changing the behaviour from an expected high-frequency one to one which resembles a low-frequency quasistatic CV measurement.

In section 3.6, the transition of a MOS capacitor into a MIM capacitor by varying the thickness of the ultra-thin metal layer was studied. A MOSCAP based on alumina with a platinum electrode was modified by inserting a chromium layer. CV-curves of those MOSCAP structures were measured and compared. For those macroscopic (compared to the SCM measurement) devices, Cr layers in the range of 1-2 nm still produced MOS-like CV-curves, but with heavily modified properties like shifted flat band voltages or capacitance densities.

As the last step, MOSFETs with an interfacial metal layer have been produced for section 3.7. Unfortunately, the results did not fulfil the expectations which have been set beforehand into the integration of an ultra-thin metal layer into a MOSFET. First, a device without a metal layer has been produced. The electrical properties of this device seems to be acceptable, although the drain current is very low compared to the MOSFETs in section 3.2, a fact which was accounted to production issues. By integrating a 0.3 nm layer of chromium metal, the properties of the MOSFET already change extensively: The well-known V_{DS}-I_D graph changes which exhibits a saturation behaviour for higher drain-source voltages changes into a more linear behaviour, which may be a hint for high-mobility

charge carriers combined with a bad contact from the S/D-contacts into the channel. The calculated mobility is very low, although the indeterminability of the charge carrier density of the channel must be taken into account for interpretation of this value. As a last step, a sample with a very thick metal layer (22 nm) has been manufactured as well. Here, an expected short-cut behaviour of the channel can be seen in the V_{DS}-I_D and V_{GS}-I_D graphs.

4.3. Conclusion and Outlook

Concluding this work, one has to ask if the questions which have been raised have been successfully answered. Considering the production of a high-mobility device, the result can be considered be a success, although the answer is not the one one would expect. The paper by Dragoman *et al.* [9] showed encouring results which fostered this work. Results similar to their work could be reproduced, if one looks at the MOSFET with 0.3 nm Cr metal in section 3.7. The volume of new information gathered makes it possible to explain the problems of this approach, where it was tried to integrate a ultra-thin metal layer into the MOSFET by conventional methods [9]. So the question has to be if is it possible to create a high-mobility MOSFET by limited means; while the reached values are still not in the expected region, the will certainly be a good foundation for further work.

Although the primary aim of this thesis was not completely fulfilled, a plenty of new information has been gathered explaining the many problems in forming such a high mobility MOSFET. Furhermore, a lot of new research results apart from this device were collected.

It was necessary to examine S/D contacts beforehand. These measurements were very successful experiments, especially the elaborate work in creating RhGe-contacts. This part of the thesis also proved as a foundation for a diploma thesis of Markus Hummer where the interplay between oxide and Schottky contacts was discussed in detail [158], something which has been only described lately in literature [159].

The other fundamental investigations regarding the growth behaviour of ultra-thin metal films (by in-situ measurement) or by analysing the behaviour of capacitive devices which incorporate such a film also brought new insights. For the in-situ measurements, a possible outlook on this study could be, as already mentioned, to use other metals or, more importantly, to use other semiconductor substrates like germanium or III-V semiconductors. The dependence on the growth temperature could also be worthwhile for continuing investigations.

Additionally, the study of MOS stacks by SCM could be also be continued, as a lot of parameters could be changed to generate new knowledge: semiconductor, oxide, thicknesses or the interfacial metal properties by changing the deposition method or parameters.

The MOSFET with the interfacial layer behaved not as expected previously. The various problems causing this could be identified in this work and may also have been encountered by Dragoman *et al.* in their fundamental work:
At first, it is very difficult to grow a sufficiently flat, clean and defect free metal film on pristine silicon without highly sophisticated equipment. In the work by Kim *et al.*, the metal film was deposited on a surface which was treated by several vacuum cleaning processes and the deposition happened at an extremely low base pressure in an extremely clean environment. As the aim of this thesis was to produce a MOSFET which could be manufactured by conventional semiconductor industry technology, the idea was to try if with relaxed conditions (e.g. lower base pressure, preparation of the Si(111) surface by BHF) it is still possible to establish a MOSFET with a high mobility channel, resulting in different findings which suggest that under these conditions the constitution of such a device is impossible.

Another, even bigger issue is that it may be impossible for the ultra-thin metal film to withstand the ALD process which deposits the oxide if one considers the results of section 3.4. There it is proven that the metal layer (at least of this system, but this could be extrapolated to other systems) becomes oxidised during the ALD process. There may be a trade-off between using a reactive material which forms high-quality monolayers (due to the high probability for interaction with other atoms, the Frank-van-der-Merwe growth mode is prefered, but this also is

a key to oxidisation of the metal layer) and a non-reactive material like platinum, which is very difficult or impossible to grow as a flat monoatomic layer. An approach to overcome this could be a sacrificial layer, where metal is selectively oxidised to that only a monolayer is left over. Another approach could be a much more controlled environment for growth or other growth techniques, but this may interfere with the goal to establish a method to produce this high-mobility MOSFET by conventional semiconductor industry techniques.

Concluding, the two most important results of this work are:
First, the influence of very thin layers onto devices which are related to a MOS capacitor was investigated, where the main conclusion is that very thin layers change the properties of respective devices already tremendously.
The second message would be that in order to establish high-mobility MOSFETs based on the work by Kim *et al.*, there is still a lot of work ahead to achieve this goal. The approach in this thesis produced some encouraging basic results, which will act as a base for further research.

Summarizing everything again together, this work is believed to foster not only further research considering high-mobility MOSFETs with integrated ultra-thin metal layers, but also brought new insights considering rhodium-germanide contacts, the behaviour of thin metals films during ALD deposition or in-situ measurements of the resistance during the deposition of metal onto Si(111).

A. Lithography Masks

All lithography masks used for this work where drawn in AutoCAD® 2013 and produced by means of laser writing (Heidelberg DWL66) on chrome-coated glass mask templates.

A.1. MOSFET masks

For the production of MOSFET devices as described in the chapters 2 and 3, masks for the lithographical patterning are needed. In figures A.1, A.2 and A.3, the 2D drawings of the three masks used in this work are shown. The different colours represent different layers, which are described in the right section of the drawings.

These masks not only contain structures for the formation of rectangular and circular MOSFETs, but also for MOSCAP devices (circles and rectangulars of magenta colour), structures for sheet resistance measurement (e.g. cloverleaf structure) and for markers for alignment (notably the big cross).

Each of these drawings is duplicated several times to fill the whole available surface of the mask. The mask itself is split up in different regions, where the different layers (identified by colours) are separately located.

A.1.1. Version 1

The first mask contains not only MOSFET structures, but also structures for sheet resistance measurement. The rectangular MOSFET gate length ranges from 5 to 40 µm; the length of the circular devices between 10 and 40 µm, respectively.

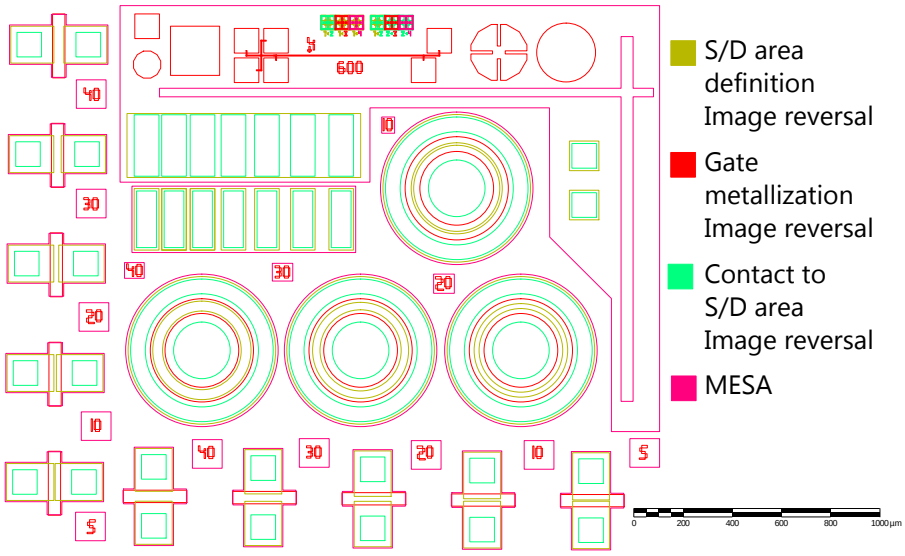


Figure A.1.: Drawing of the first version of the mask used for the formation of MOSFET devices

A.1.2. Version 2

The second mask version is different to the first one by omitting e.g. the clover-leaf structure, as it became clear during the formation of MOSFET devices that it was not necessary. Additional MOSFET devices were added instead, so that the MOSFET channel length for rectangular devices ranges from 2 to 40 µm. The circular devices were extended by a devices which uses a tongue-like structure for the gate, which was used to implement a gate metal contact structure which does not directly lie over the channel.

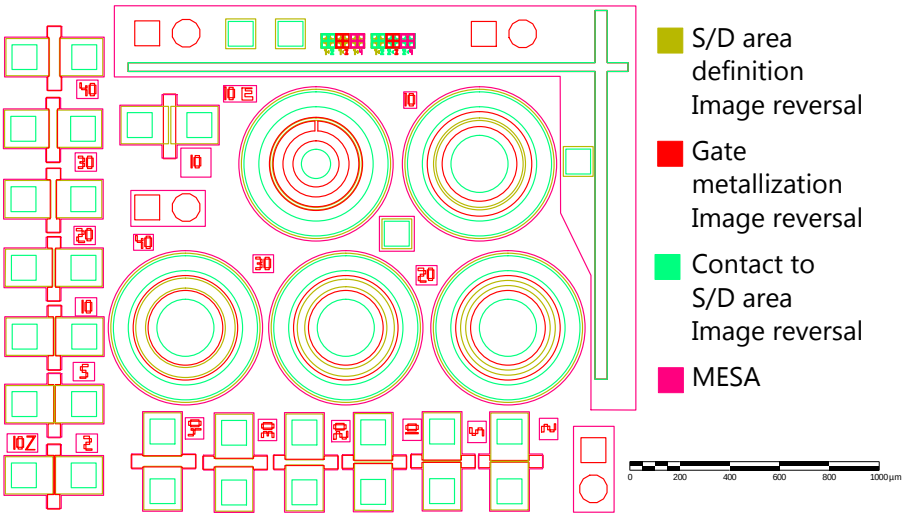


Figure A.2.: Drawing of the second version of the mask used for the formation of MOSFET devices

A.1.3. Version 3

The third version again changes the devices, based on the experiences gained during the formation of devices with the previous mask types. A gate recess layer was added, while the circular MOSFET with 10 µm gate length was omitted.

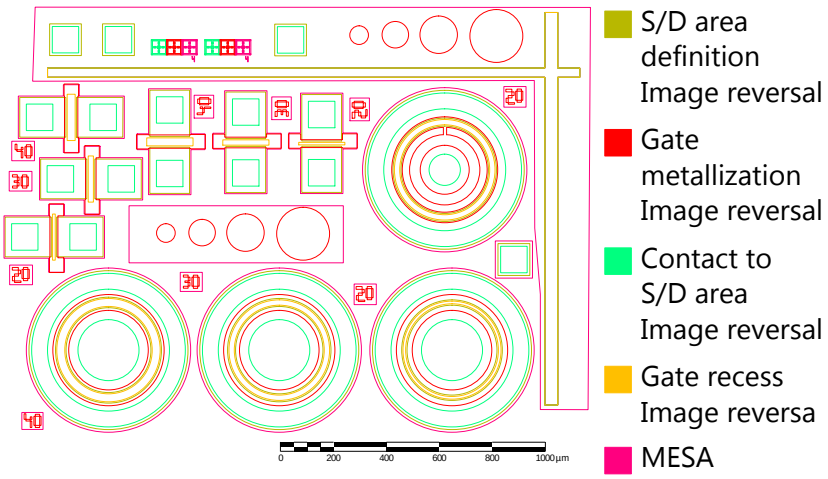


Figure A.3.: Drawing of the third version of the mask used for the formation of MOSFET devices

A.1.4. Comparison

As one can see in figure A.4, the design of the rectangular MOSFET devices evolved with the different mask versions. At first, the MESA structure was rectangular, which also covered a part of the S/D-regions. This was identified as problematic, therefore this was changed in version 2. Version 3 is similar, but adds the already mentioned gate recess layer to the design.

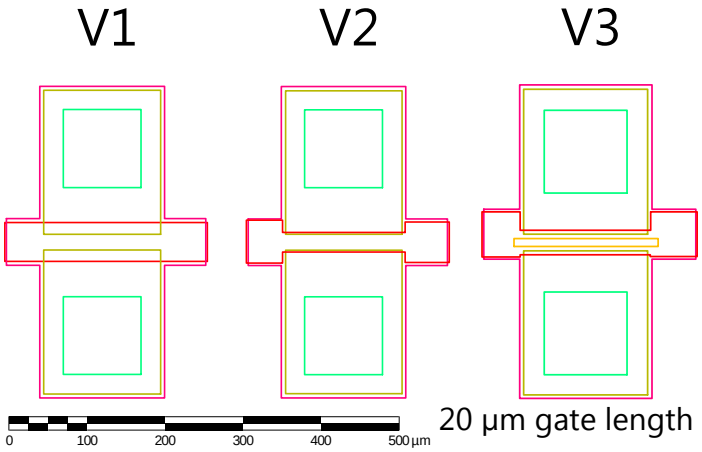


Figure A.4.: A schematical drawing of the working principle of SCM

A.1.5. Table of MOSFET gate lengths

In table A.1, the gate lengths for all mask versions mentioned are listed.

Table A.1.: Table listing gate lengths for round and rectangular MOSFETs, Z stating a special tongue-like structure for the gate metal for a round MOSFET.

Mask V1		**Mask V2**		**Mask V3**	
Rect.	*Round*	*Rect.*	*Round*	*Rect.*	*Round*
		2			
5		5			
10	10	10	10		
20	20	20	20	20	20
30	30	30	30	30	30
40	40	40	40	40	40
		10Z			20Z

B. Curriculum Vitae

Dipl.-Ing. Bernhard Lutzer, BSc

Personal data:

Date of birth:	23.05.1989
Place of birth:	Krems/Donau, Austria
Citizenship:	Austrian

Education:

since 2013	Doctoral programme in engineering sciences at TU Wien: *"Schottky Barrier MOSFETs with Atomic Layer Grown High-k Oxides and Ultrathin Metal-Interlayers on Silicon (111)"*
Dec. 2012	Graduated as MSc. at TU Wien: *"Measurements and Irradiations for the CMS Tracker Upgrade"*; pass with distinction
2011	Erasmus student exchange programme; ETH Zurich
2010 – 2012	Master's programme Technical Physics at TU Wien
2007 – 2010	Bachelor's programme Technical Physics at TU Wien

Research experience:

since 2012	Institute of Solid State Electronics, TU Wien, Vienna, Austria; FWF project assistant in the future device technology group of Prof. Emmerich Bertagnolli *"Stabilization of the High-k Phase in ALD-grown Rare-Earth Based Oxides"* FWF project Nr: P24506 – "STAPHASE"
2011 – 2012	Institute of High Energy Physics (HEPHY) Vienna, Austria; Diploma thesis: "Measurements and Irradiations for the CMS Tracker Upgrade"
2010	European Organization for Nuclear Research (CERN) Geneva, Switzerland; Project in establishing an IT test infrastructure for the CMS trigger
2009	Institute for Applied Physics, TU Wien Vienna, Austria; Bachelor thesis "Construction of a Sagnac interferometer for the student's bachelor lab"

C. List of Own Publications

Journal Contributions

[I] O. Bethge, C. Zimmermann, B. Lutzer, S. Simsek, J. Smoliner, M. Stöger-Pollach, C. Henkel, E. Bertagnolli: "Effective reduction of trap density at the Y_2O_3/Ge interface by rigorous high-temperature oxygen annealing"; Journal of Applied Physics, **116** (2014), p. 214111-1 - 214111-7.

[II] O. Bethge, C. Zimmermann, B. Lutzer, S. Simsek, S. Abermann, E. Bertagnolli: "ALD Grown Rare-Earth High-k Oxides on Ge: Lowering of the Interface Trap Density and EOT Scalability"; ECS Trans., **64** (2014); p. 69 - 76.

[III] B. Lutzer, M. Hummer, S. Simsek, C. Zimmermann, A. Amsuessb, H. Hutter, H. Detz, M. Stoeger-Pollach, O. Bethge, and E. Bertagnolli, "Rhodium Germanide Schottky Barrier Contacts"; ECS J. Solid State Sci. Technol., **4** (2015), p. 387 - 392. DOI: 10.1149/2.0181509jss.

[IV] B. Lutzer, S. Simsek, C. Zimmermann,M. Stoeger-Pollach, O. Bethge, E. Bertagnolli, "Linearity optimization of ALD-grown ZrO_2 MIM capacitors by inserting interfacial Zr-doped chromia layers"; Journal of Applied Physics , **119** (2016), p. 125304-1 - 125304-7. DOI: 10.1063/1.4944803.

[V] C. Zimmermann, O. Bethge, K. Winkler, B. Lutzer, E. Bertagnolli: "Improving the ALD-grown Y_2O_3/Ge interface quality by surface and annealing treatments"; Applied Surface Science, **369** (2016), p. 377–383.

[VI] C. Zimmermann, O. Bethge, B. Lutzer, E. Bertagnolli: "Platinum-assisted Post Deposition Annealing of the n-Ge/Y_2O_3 Interface"; Semicond. Sci. Technol., **31** (2016), p. 075009.

[VII] B. Lutzer, O. Bethge, C. Zimmermann, J. Smoliner and E. Bertagnolli, "Effect of Schottky-Barrier Formation on the in-situ resistance of ultrathin metal films on differently doped Si(111) during physical vapour deposition"; Manuscript submitted for publication

Oral Presentations

[I] B. Lutzer, O. Bethge, C. Zimmermann, E. Bertagnolli: "Ohmic contacts for resistance measurements of ultra-thin metal-on-silicon layers"; Annual Meeting of the ÖPG/SPS, Linz, Austria, 03.06-06.06.2013

[II] B. Lutzer, O. Bethge, C. Zimmermann, S. Simsek, J. Smoliner, E. Bertagnolli: "Characterization of Ultra-Thin Metal on Silicon Structures for Future Field Effect Devices"; XII International Conference on Nanostructured Materials (NANO 2014), Moscow, Russian Federation; 13.07.2014 - 18.07.2014

[III] B. Lutzer, O. Bethge, C. Zimmermann, E. Bertagnolli: "ALD grown bilayer gate stacks for Schottky-barrier Si and Ge MOSFETs"; Annual Meeting of the ÖPG/SPS, Vienna, Austria, 01.09-04.09.2015

[IV] B. Lutzer, O. Bethge, C. Zimmermann, E. Bertagnolli: "Schottky-barrier Si and Ge MOSFETs with ALD grown bilayer gate dielectrics"; International workshop Atomic Layer Deposition Russia 2015 (ALD Russia 2015), Moscow, Russian Federation, 21.09-23.09.2015

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