DISSERTATION

Electromigration Reliability Issue in Interconnects for Three-Dimensional Integration Technologies

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Dedicated to my loving parents.

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Kurzfassung

Über viele Jahrzehnte hinweg ermöglichten Innovationen in Halbleiterindustrie das Skalieren von Transistoren entsprechend dem Mooreschen Gesetz. Darüber hinaus gibt es seit kürzerem intensive Bemühungen um verschiedenartige Funktionalitäten auf einem einzelnen Chip zu vereinen. Versuche dies in einer Ebene zu realisieren, verursachen Verdichtungen von elektrischen Leitungen und erhöhen Rauschen und Verzögerungen der Schaltungen. Diese Probleme können durch ein vertikales Stapeln der verschiedenen Technologien auf verschiedenen Ebenen des Chips gelöst werden, wobei auch für die elektrischen Leitungen drei Dimensionen genutzt werden. Diese Verbindungstechnologie zur dreidimensionalen Integration bietet zwar bedeutende Vorteile, wie bei vielen neuen Technologien kann es aber auch zu einigen Zuverlässigkeitsproblemen kommen. Ein wesentliches Zuverlässigkeitsproblem in modernen Leitungsstrukturen ist der Einfluss der Elektromigration, ein Effekt der bei hohen elektrischen Strömen zu Massentransport in metallischen Verbindungen führt, auf die Lebenszeit von Geräten. Die Vorhersage von elektromigrationsbedingter Lebenszeit ist damit wichtig um die Zuverlässigkeit von elektrischen Leitungen zu beurteilen. Beschleunigte Elektromigrationstests werden seit Jahrzehnten genutzt, um festzustellen welche Faktoren die Lebenszeit von elektrischen Verbindungen bestimmen, jedoch ist es sehr schwierig die Mechanismen hinter den Fehlern zu identifizieren. Hier bietet sich physikalische Modellierung als der praktikabelste Weg an.

Das multiphysikalische Problem der Elektromigrationsmodellierung teilt sich in zwei Phasen. In der frühen Phase entstehen Leerstellen und in der späten Phase kommt es zu einer Entwicklung der Leerstellen. Das Entstehen der Leerstellen in der ersten Phase ist bedingt durch die Entwicklung von Zugspannungen, im Besonderen in Bereichen geringer Adhäsion zwischen Metalllagen und umgebenden Material. Das Wachstum dieser Leerstellen in der späten Phase führt dann zu beträchtlichen Veränderungen des Leitungswiderstandes bis hin zu einer Unterbrechung des Schaltkreises. Die Lebenszeit elektrischer Verbindungen wird bestimmt durch einen maximalen Widerstandswert der in einer gegebenen Schaltung toleriert werden kann. Die Entwicklung des Zwei-Phasen-Modells für die Elektromigration und dessen Implementierung in kommerzieller Finite-Elemente-Methoden basierter Software ermöglicht effiziente numerische Simulationen.

In dieser Arbeit werden Elektromigrationssimulationen von realistischen Verbindungen in Integrationsarchitekturen durchgeführt, um deren Zuverlässigkeit abzuschätzen. Hierbei sind Fallstudien von hohlen Silizium-Durchkontaktierungen und Flip-Chip Lötkugeln besonders interessant. Bei ersteren treten elektromigrationsbedingte Fehler in der Nähe der Metallisierungsbarriere zwischen Durchkontaktierungen und den anliegenden Metallen auf. Sobald sich eine Leerstelle gebildet hat, wird deren Wachstum durch den elektromigrationsinduzierten Fluss von Vakanzen entlang der Oberfläche der Leerstelle verursacht. Die Kombination der Kinetik der beiden Fehlerphasen ermöglicht eine gute Abschätzung der Lebenszeit von elektrischen Verbindungen. Bei Flip-Chip Lötkugel-Technologien fördert die elektromigrationsbedingte Veränderung der Materialzusammensetzung die Bildung von Leerstellen an den Grenzschichten zwischen Lötkugeln und intermetallischen Verbindungen. Die Analyse zeigt, dass die Lebenszeit der Lötkugeln stark durch die frühe Fehlerphase bestimmt wird. Darüber hinaus wird eine bedeutsame Vergleichsstudie präsentiert, die den Einfluss von Geometrie und Mikrostruktur auf die Entwicklung von elektromigrationsbedingten Fehlern in normalen elektrischen Verbindungen untersucht. Simulationen ermöglichen die Abbildung von Elektromigrationsphänomenen in verschiedenen Strukturen und stellen aussagekräftige Ergebnisse über die Zuverlässigkeit sicher.

Abstract

Innovation in the semiconductor industry has enabled transistor scaling along Moore's law for many decades. More recently, significant effort has been dedicated to the introduction of diversified functionality on a single chip. Attempts to realize this on a single plane results in interconnect congestion as well as increased circuit noise and delay. These issues could be overcome by vertically stacking multiple technologies located on different planes of the chip and providing electrical interconnection by making use of the third dimension. Although interconnect technologies for three-dimensional integration show significant advantages, there are several reliability concerns, as is often the case in emerging technologies. A key reliability issue in modern conducting structures is the influence of electromigration, which is the process of mass-transport-induced failure caused by high current flow in metal lines, on device lifetimes. The prediction of the electromigration lifetime becomes crucial for the assessment of interconnect reliability. Accelerated electromigration testing has been used for decades to determine the factors which affect the lifetime of interconnects, but the mechanisms governing the failure are extremely difficult to identify. The most feasible way is provided by the use of physical modeling.

In general, electromigration modeling represents a multiphysics problem which can be divided into two phases, namely, the early phase of void nucleation and the late phase of void evolution. During the first phase, stable voids nucleate in the interconnect due to the development of tensile stress, particularly at those locations where the adhesion between the metal layer and the surrounding material is weak. In turn, the late phase is governed by the void evolution mechanism which leads to extremely high changes in the interconnect resistance until an open circuit failure is noted. The lifetime of the interconnect is found after reaching a maximum resistance value tolerable in the given circuit. The development of the two-phase-model for electromigration and its implementation in a commercial software, based on the finite element method, allows to carry out numerical simulations in an efficient way.

In this work, electromigration simulations are performed for realistic interconnect geometries for integration architectures in order to assess their reliability. Case studies of particular interest are open through silicon vias and flip-chip solder bumps. For the first case, electromigration failure is observed to initiate close to the metallization barrier between the via and the adjacent metal level. Once the void has nucleated, its growth is caused by the electromigration-induced-vacancy flux along the void surface. The combination of kinetics of both phases of failure provides a good estimation of the interconnect lifetime. In flip-chip solder bump technologies, electromigration enhances material composition changes which leads to a void nucleation at the bump/intermetallic compound interface. The analysis shows that the solder bump lifetime is dominated by the early phase failure. Furthermore, a newsworthy comparative study regarding the impact of geometry and microstructure on the electromigration failure development in standard interconnect lines is presented. Simulations are capable of reproducing the electromigration phenomenon in diverse structures and ensure meaningful results for the evaluation of their reliability.

Riassunto

L'innovazione nel settore dei semiconduttori ha consentito la riduzione di scala del transistore in accordo con la legge di Moore per molti decenni. Di recente, un significativo sforzo é stato dedicato all'introduzione di funzionalitá diversificate all'interno di un unico chip. I tentativi di realizzare questo su un unico piano risultano nella congestione di interconnessioni, nonché ad un aumento di disturbi e ritardi nel circuto. Queste difficoltà potrebbero essere superate mediante l'impilamento verticale di molteplici tecnologie situate su piani diversi del circuito in modo da garantire la connessione elettrica tra loro facendo uso della terza dimensione. Sebbene queste interconnessioni utilizzate nel campo dell'integrazione tridimensionale mostrano significativi vantaggi, diversi problemi di affidabilità sono presenti, come spesso accade nelle tecnologie emergenti. Un problema chiave di affidabilità nelle moderne strutture metalliche è rappresentato dall'influenza che l'elettromigrazione, nota come il processo di avaria causato dal trasporto di atomi indotto dal passaggio di corrente nelle linee metalliche, ha sulla durata del dispositivo. La previsione del tempo di vita dell'interconnessione metallica perturbata dall'elettromigrazione diventa fondamentale per la valutazione della sua affidabilità. Test sperimentali che accelerano il processo di elettromigrazione nelle interconnessioni sono stati utilizzati per decenni per determinare i fattori che ne influenzano la loro durata, ma i meccanismi che ne regolano il guasto sono estremamente difficili da identificare. Il modo piú semplice per riconoscerli viene fornito dai modelli fisici.

In generale, modellare il fenomeno di degradazione dovuto all'elettromigrazione rappresenta un problema multifisico che può essere suddiviso in due fasi, vale a dire, la prima fase di nucleazione di un microporo e la fase successiva relativa alla sua evoluzione. Durante la prima fase, stabili microvuoti nucleano nell'interconnessione a causa dello sviluppo di sforzo dovuto a trazione, in particolare in quei siti in cui l'adesione tra la linea metallica e il materiale circostante è debole. Successivamente, la seconda fase è regolata dal meccanismo di evoluzione del microvuoto che comporta altissime variazioni nella resistenza elettrica dell'interconnessione fino a rilevare un guasto di circuito aperto. Il tempo di vita dell'interconnessione è valutato dopo aver raggiunto un valore massimo di resistenza tollerabile nel circuito dato. Lo sviluppo del modello a due fasi per l'elettromigrazione e la sua implementazione in un software commerciale, basato sul metodo degli elementi finiti, consentono di eseguire simulazioni numeriche in modo efficiente.

In questo lavoro, simulazioni riguardanti il fenomeno dell'elettromigrazione vengono eseguite in realistiche geometrie di interconnessione per architetture integrate al fine di valutare la loro affidabilità. Casi di studio di particolare interesse sono rivolti verso strutture quali through silicon vias (fori passanti su wafers di silicio) e flip-chip solder bumps (raccordi

puntuali saldati). Per il primo caso, l'iniziazione del guasto causato dall'elettromigrazione si osserva vicino alla barriera metallica interposta tra la via e l'adiacente livello di metallizzazione. Una volta che il microporo è nucleato, la sua crescita è causata dal flusso di vacanze lungo la superficie del microvuoto indotto dall'elettromigrazione. Combinando le cinetiche di entrambe le fasi di fallimento, una buona stima della durata dell'interconnessione è ottenuta. Nelle tecnologie di saldatura, l'elettromigrazione comporta modifiche sostanziali nella composizione del materiale che conduce ad una nucleazione di un microporo all'interfaccia esistente tra il bump ed il composto intermetallico. L'analisi mostra che il tempo di vita della specifica interconnessione è dominato dalla fase di nucleazione del microporo. Inoltre, un interessante studio comparativo riguarda l'impatto della geometria e della microstruttura di interconnessioni standard sullo sviluppo del fallimento causato dall'elettromigrazione. Le simulazioni sono in grado di riprodurre il fenomeno dell'elettromigrazione in diverse strutture e garantire risultati significativi per la valutazione della loro affidabilità.

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List of Symbols

Roman Symbols

A_n	Area of the given diffusion path n
B	Bulk modulus
C	Capacitance
C_a	Atomic concentration
C_iklm	Components of the elastic stiffness tensor
C_L	Lattice site concentration
c_P	Specific heat capacity
C_V	Vacancy concentration
$C_\mathrm{V,eq}$	Equilibrium vacancy concentration
C_V^T	Trapped vacancy concentration
d	Diameter
D_a	Atomic diffusion coefficient
D_V	Vacancy diffusion coefficient
$D_\mathrm{V,0}$	Pre-exponential factor for vacancy diffusion
E	Young’s modulus
E	Electric field
e	Electron charge
E_a	Activation energy for diffusion

F	Force
f	Relaxation factor
G	Vacancy source/sink term
j	Electric current density
J_a	Atomic flux
J_V	Vacancy flux
k_B	Boltzmann constant
k_T	Thermal conductivity
$k_\mathrm{T,0}$	Thermal conductivity at the reference temperature T_0
l	Length
n	Current density exponent
n_a	Number of atoms
n_V	Number of vacancies
p	Hydrostatic pressure
Q^*	Transport heat
R	Electric resistance
R_P	Radius of a circular patch
S_iklm	Components of the elastic compliance tensor
T	Temperature
t	Thickness
T_0	Reference temperature
u	Displacement
u_i	Component of the displacement vector
V	Volume
v	Velocity
V_E	Electric potential

w	Width
Z^*	Effective valence

Greek Symbols

α	Linear temperature coefficient
α_{th}	Coefficient of thermal expansion
$\bar{\mu}$	Electrochemical potential
β	Quadratic temperature coefficient
Δ	Change of any changeable quantity
δ	Grain boundary/interface thickness
δ_{ik}	Kronecker delta function
$\varepsilon_{\mathrm{di}}$	Diffuse interface thickness parameter
$\varepsilon_{\mathrm{ik}}$	Components of the total strain tensor
Γ	Interface
γ_{m}	Interfacial free energy of the metal
γ_{ik}	Components of the engineering shear strain tensor
γ_{s}	Surface energy
κ	Relative permittivity or dielectric constant of a material
μ	Chemical potential
∇	Vector differential operator
ν	Poisson ratio
Ω	Domain
Ω_{a}	Atomic volume
ω_{R}	Release rate
ω_{T}	Trapping rate
Ω_{V}	Vacancy volume
ϕ	Order parameter

ρ	Electrical resistivity
ρ_{m}	Mass density
σ	Trace of the hydrostatic mechanical stress tensor
σ_{E}	Electrical conductivity
$\sigma_{\mathrm{E},0}$	Electrical conductivity at the reference temperature T_0
σ_{ik}	Components of the elastic stress tensor
σ_{thr}	Threshold stress for void nucleation
τ_{ik}	Components of the shear stress tensor
τ_{V}	Vacancy relaxation time
θ_{C}	Equilibrium contact angle

Other Symbols

exp	Exponential
$\mathscr{F}$	Free energy functional
∞	Infinite symbol
$\hat{n}$	Normal vector
$\overline{\overline{T}}$	Tensor T
$Tr(\overline{\overline{T}})$	Trace of the tensor T
$\vec{v}$	Vector v

Acronyms / Abbreviations

1D	One dimensional
2.5D	Two and a half dimensional
2D	Two dimensional
3D	Three dimensional
BEOL	Back end of line
CAD	Computer aided design
CMOS	Complementary metal oxide semiconductor

CPU	Central processing unit
DE	Differential equation
FEM	Finite element method
FEOL	Front end of line
IC	Integrated circuit
IMC	Intermetallic compound
MTTF	Mean-time-to-failure
NoC	Network on chip
PDE	Partial differential equation
PoP	Package on package
P	Packaging
RDL	Redistribution layer
SIC	Stacked integrated circuit
SiP	System in package
SoC	System on chip
SOI	Silicon on insulator
SSI	Small scale integration
TCAD	Technology computer aided design
TSV	Through silicon via
TTF	Time-to-failure
UBM	Under bump metallization
ULSI	Ultra large scale integration
VLSI	Very large-scale integration
WLP	Wafer level packaging

Chapter 1

Introduction

Over the past century, electronic devices have penetrated every aspect of our lives and the use of electronic products has expanded while their size has continuously decreased [122]. The scaling trend leads to an increase of the density of on-chip interconnects from generation to generation of modern integrated circuits (ICs). The combined need for miniaturization of digital functionalities, such as logic and memory storage, and functional diversification requires a decrease in both interconnect width and length, which can be achieved through the introduction of three-dimensional (3D) integration technologies. The interconnect system in a 3D design is arranged in different levels of metallization which provides the vertical connections of devices in a single wafer or between stacked wafers [131]. Due to the continuous shrinking of interconnect sizes in 3D stacking, a wide spectrum of product opportunities became possible, but several reliability issues introduced from the fabrication process as well as from the device operative conditions arose. In particular, when a sufficient high current density passes through a metal interconnect, a failure mechanism is initiated by the resultant material transport in the direction of the current flow. This failure process known as electromigration is one of the main reliability issues in interconnects for 3D integration technologies. It became of technological interest when semiconductor companies observed electromigration damage in ICs. Since then, improvements have been made in developing new interconnect design, integration processes, and novel materials in order to reduce the electromigration effect in interconnects and predict their long term behavior.

In the following, a brief introduction regarding the technological development of integrated circuits and 3D integration approaches is presented. This is followed by the description of the interconnections composing the 3D layout and their main reliability issues. After that, a description of the physical phenomena behind the electromigration is provided.

1.1 Integration Technology

The "big bang" of electronics can be traced to the invention of the first point-contact transistor in 1947 by J. Bardeen, W. Brattain, and W. Shockley [8]. The transistor is an active electrical component in an integrated circuit which acts as a switch. The invention of the transistor was considered a revolution and it quickly replaced the vacuum tube, on which much of the electronics at the time were based [117].

The development of several types of semiconductor devices followed in the years after the invention of the first transistor [122]. Electrical engineers realized advanced electrical circuits consisting of discrete components connected together with metal traces [117]. Although these innovative devices could be more reliable compared to the pre-transistor era electronics, problems started to arise as the complexity of the circuits grew. In particular, limitations on performance due to the size of the interconnect wires, as well as the impossibility to assemble the vast number of tiny components required in the circuit, limited the full exploitation of the device capabilities.

A solution to the problem of increasing circuit complexity was found in 1958 by J. S. Kilby [90], whose groundbreaking idea was to make all components of the electrical circuit out of the same block of semiconductor material and add the metal connection as a layer on top of. This resulted in the well-known integrated circuit (IC). The integration of all necessary devices within silicon no longer required individual discrete components and wires which must be assembled manually.

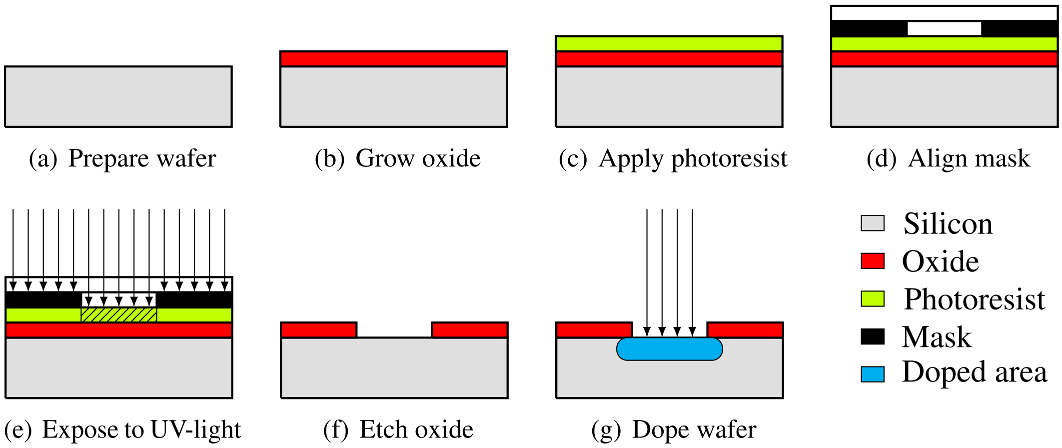
Later improvements in the fabrication process of ICs were achieved at Intel under the supervision of G. Moore and R. Noyce [54]. In order to make the IC more suitable for mass production and answer to the profound need of more general and broader application, they introduced the concept of a microprocessor in 1971 by releasing the Intel 4004, the first central processing unit (CPU) [54].

ICs and microprocessors have significantly improved since Kilby's prototype, demonstrating higher performance and enhanced reliability.

1.1.1 Semiconductor Fabrication

The individual components of an IC are extremely small and its production demands precision at an atomic level [117]. IC fabrication is a complex process during which electronic circuits are created in and on a wafer made out of very pure semiconducting material, typically silicon. The manufacturing is a multiple-step sequence which can be divided into two major processing stages, namely front-end-of-line (FEOL) processing and back-end-of-line (BEOL) processing.

FEOL refers to the construction of the components of the IC directly inside the wafer [5], as depicted in Figure 1.1. The mono-crystal silicon wafer is polished in order to obtain a substrate with its surface as regular and flat as possible (Figure 1.1(a)). The top of the wafer is then prepared for photolithography by covering it with an insulating layer to serve as a mask, typically an oxide (Figure 1.1(b)), and a subsequent covering film of protective material which is sensitive to light, called photoresist (Figure 1.1(c)). A photomask with the circuit pattern for one layer of the chip is loaded and aligned with the wafer (Figure 1.1(d)). The exposure process of the wafer to intense UV light through the mask allows to remove the exposed photoresist area (Figure 1.1(e)). The unprotected insulating material is then striped away using a chemical etching process and the remaining photoresist is removed by a developer solution (Figure 1.1(f)). In general, there are two types of photoresist: negative and positive. When exposed to UV light, the negative photoresist becomes polymerized and more difficult to dissolve in developer solution than the positive resist. For negative resist, the developer solution removes only the unexposed areas. In this way, it is possible to create a pattern of non-protected silicon wafer areas surrounded by regions of non-conducting material. Then, the modification of the electrical properties of the exposed areas involves doping processes, such as ion implantation which is used to create sources and drains of the transistor (Figure 1.1(g)). Other conducting or insulating layers may also be added. A new layer of material is added and the entire photolithography process, which includes imaging, deposition, etching, and doping, is repeated to create many different components of the chip, layer by layer.



(a) Prepare wafer (b) Grow oxide (c) Apply photoresist (d) Align mask

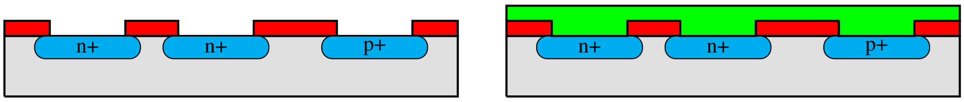
(e) Expose to UV-light (f) Etch oxide (g) Dope wafer

Figure 1.1: Basic steps of the FEOL fabrication process.

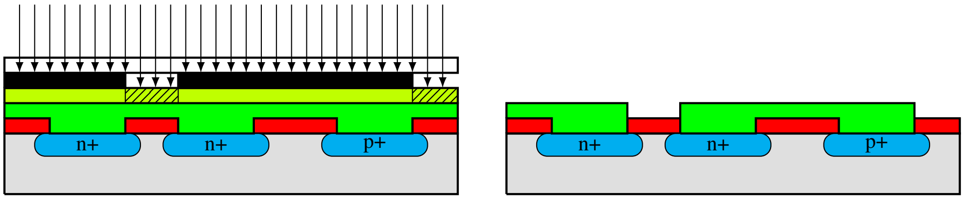
Once all the components of the IC are ready, the BEOL processing step is performed to deposit the metal wiring between the individual devices in order to interconnect them, with a process called metallization [5], as illustrated in Figure 1.2. Common metals used in the semiconductor industry are copper and aluminum, but recently many other metals are being tested for applicability for metal interconnects at the nano-scale. The second stage of the chip fabrication also includes the formation of contacts and dielectric structures. BEOL processing generally begins when the first layer of a conducting metal is deposited on top of the wafer (Figure 1.2(b)). A layer of UV-sensitive photoresist is added on the top of the metal. Then, in a manner similar to the processing of the components during the FEOL processing, a UV-light source is exposed to the photoresist through a mask describing the desired layout of the metal wires; the exposed section of the positive photoresist is then removed in the subsequent chemical etching step (Figure 1.2(c)). The etching process eliminates the unprotected metal to obtain a pattern of wires described by the mask which connects the different components of the chip (Figure 1.2(d)). Most ICs need more than one layer of wires to form all the necessary connections. In real chips, as many as 5-12 layers are added in the BEOL process [117]. Typically, metal interconnecting wires are isolated by dielectric layers to prevent the wires from creating a short circuit with other metal layers.

The various metal layers are interconnected by etching holes, called vias, in the insulating material (Figure 1.2(e)).

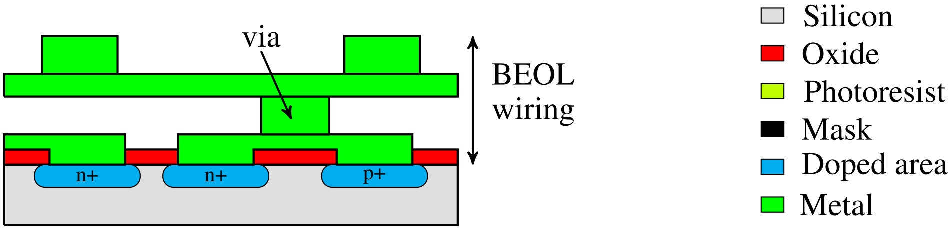
After the BEOL processing, the post-fab process is performed, which includes wafer testing, die separation, die testing, IC packaging, and final device testing.



(a) Three devices (b) Deposit metal



(c) Photolitography (d) Etch metal



(e) Chip with different metal layers

Figure 1.2: Basic steps of the BEOL fabrication process.

1.1.2 Shrinking Features

Today, ICs can be made very compact and the most advanced ICs can contain several billions of electrical components on an area of about 1cm^2 [6]. The density of individual components which can be electrically connected in an IC is related to the device half-pitch [2]. It represents the half of the distance between the parallel conducting metal lines at the first metallization level which carry the electrons to the chip, as depicted in Figure 1.3. It is an important feature in the semiconductor industry because, with the shrinking of the ICs, other terms, such as node and gate width, resulted no more universally accepted metrics that specialists use to measure their transistors due to the continued reduction of their sizes [2]. A node indicates the size of the smallest part of the transistor on the chip, while the gate width is the distance between the source and the drain of the transistor. For example, in 2005, the node on an Intel microprocessor was 65nm, the gate width was 32nm, but the half pitch was 105nm [2]. Therefore, since the half pitch was becoming bigger than the node and gate width, these concepts were no longer meaningful descriptors of the evolution of the miniaturized chip fabrication lines. The average device half-pitch on chips became smaller and smaller as the technology advanced, reducing to around 14nm in 2014 [83].

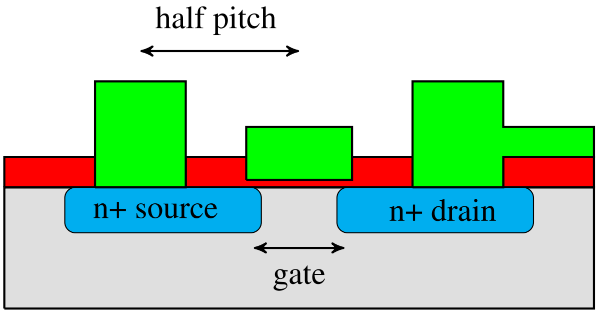


Figure 1.3: The half pitch of the first metallization layer is the defining feature for chips. The gate width represents the smallest feature.

This shrinking trend of the feature size of the chip over the years is commonly related to Moore's Law. In 1965 Gordon Moore, the co-founder of Intel, predicted that the number of components of a dense IC will double every year [114]. The forecast was extended to eighteen months to accommodate real conditions in 1975 [113]. As the technology progressed, the number of components contained on a single chip has been increased from 10 in 1964 to several billions in the 1980s. This led to the classification of different generations of ICs, giving rise to new design methods from the early small-scale integration (SSI) to the more complex ultra-large-scale integration (ULSI) and three-dimensional integrated circuit (3D-IC). The key technology of the development reflects on the further evolution in the complexity of ICs by building systems in which all the individual components are assembled in circuit blocks, such as memory and logic, and included in a single chip substrate.

Moore's prediction was an elegant statement of how ICs would become smaller and cheaper over the years. The law has been used in the semiconductor industry to set targets for product development for several decades and represents a technological driving force for social change and economic growth [89]. The fascinating technology evolution was essentially supported by the maturation of the chip fabrication process, but physical limitations of device shrinking were starting to affect IC performance and reliability [122].

1.1.3 Interconnects in Integrated Circuits

In general, as a consequence of the Moore's law, the continuous device scaling implies reduced cost per transistor, increased operating speed, and lower power consumption [47]. From this point of view, the interconnect wires, manufactured during the BEOL processing, play a key role.

The main goal of the metal wiring in an IC is to create electrical connections among the active devices in order to transmit and distribute signals and power across the circuit. Due to the shrinking and high signal speed requirements of modern ICs, the interconnect structures are becoming the bottleneck for delay and noise in chips, making the metal interconnect an obstacle for increasing IC speed and performance [122]. The characteristic RC delay of the interconnect is given by the product of its resistance (R) and capacitance (C) and is quadratic in proportion to its length. As the chip feature sizes are reduced, the capacitance between neighboring wires enhances along with the interconnect resistance, leading to a sharp increase in the RC delay [6]. A variety of methodologies at the material and design levels have been adopted to reduce interconnect RC delay, noise, and power consumption.

The introduction of new materials at the BEOL manufacturing stage can help to improve the chip performance. Innovations were made to the materials used for both the metal wires and the dielectric insulation in order to meet conductivity requirements and reduce the dielectric permittivity [6]. The replacement of aluminum as an interconnect metal with pure copper contributed to a reduction in the interconnect RC delay and, in turn, an increase in the IC speed; copper has a lower resistivity compared to aluminum resulting in an improved chip performance. Furthermore, its higher electrical conductivity, when compared to aluminum, leads to better resistance to electromigration phenomena. However, the transition to copper as a metal conductor was not sufficient for a significant decrease in RC delays. For this purpose, new insulating materials with lower dielectric permittivity (κ) than silicon dioxide are needed for wire insulation as the chip scales further in size.

The different interconnect-related problems described above can be considerably mitigated by employing innovative architectures and design approaches [122]. The use of multi-interconnect architectures, obtained by the stacking of more metal layers with different cross sections, is useful means to manage the interconnects' characteristics, such as a decrease in the resistance and power consumption. Furthermore, the introduction of repeaters within the interconnect and the use of interconnect shielding techniques can improve the propagation of the signal along the line and mitigate the resulting noise.

Despite the numerous benefits of these new designs, the primary concern of the interconnect today remains the length of the wire with respect to its cross-section. A long wire with a small cross-section results in a high resistance. Novel design solutions are required to provide better connections among devices within the chip.

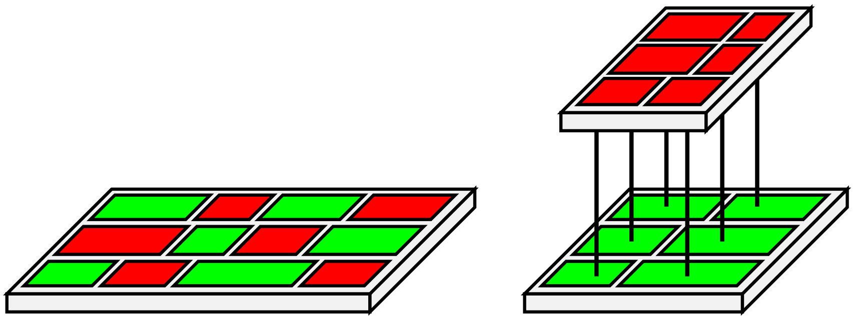
1.1.4 New Research Domains

Since transistor feature sizes and interconnect dimensions approach their physical limits expected at about the 5-7nm node, Moore's law will no longer be valid as the driving force for chip performance improvements [122, 131]. The "more Moore" research domain introduces a new trend to work around the manufacturing and material limitations of silicon-based ICs by developing new technologies at the device level. These new transistor architectures are related to further scaling of complementary metal-oxide-semiconductor (CMOS) technologies, such as silicon on insulator (SOI) transistor and fin field electric transistor (FinFET), which use new materials, such as metal gates and high-κ dielectrics, to improve IC performance and continue scaling [131].

In addition to trying to go beyond the CMOS capabilities, the interconnect congestion in the circuit at the design and package levels is also a limiting factor, where interconnect RC delay dominates the overall scaling. By following a "more than Moore" approach, many researchers are attempting to incorporate multiple functionality beyond memory and logic on a single die. The functionality can involve sensors, radio-frequency (RF) circuitry, microelectromechanical systems (MEMS), among others and their integration. This approach requires new interconnect schemes based on a heterogeneous integration of various technologies in order to provide higher connectivity among circuit blocks located on different planes [122]. Examples of novel interconnection strategies are network on chip (NoC), optical interconnects, and 3D integration. The wide variety of opportunities and advantages that 3D integration offers to IC design is discussed in the following section. It should be pointed out that the functional diversification, offered by the "more than Moore" research domain, goes in parallel to the shrinking path provided by the "more Moore" approach.

1.2 Three-Dimensional Integration

Continuous miniaturization along Moore's law has enabled the integration of different digital functional components, such as logic and memory storage, on a monolithic single chip through 2D-system-on-chip (SoC). The continued shrinking of physical feature sizes of the digital functionalities, referred as "more Moore" research domain, provides improved density, performance, and reliability values of the IC to the applications. The "more than Moore" approach leverages the scaling capabilities derived from the "more Moore" developments to incorporate digital functionalities into compact systems. A prominent strategy to continue along this trend is provided by the integration of a large number of functions of the chip by efficiently using the third dimension. System integration is the method of integrating together different circuit blocks of a chip and is one of the major applications of 3D integration [150]. 3D integration is a new design paradigm which simply consists of the process of vertically stacking multiple layers of active devices of the chip and forming electrical connections between them, either through the silicon die or through the multilayer interconnect with an embedded die [9]. It provides a space transformation of the traditional 2D planar IC implementation to 3D stacking, as illustrated in Figure 1.4.



(a) 2D-SoC (b) 3D-SoC

Figure 1.4: Conceptual view of the space transformation of (a) 2D planar SoC to (b) 3D-SoC.

Using short vertical metal interconnects in the novel 3D design, the distance between different device layers becomes relatively small when compared to 2D-ICs and allows for faster communication between different circuits blocks. These shorter electrical connections employed in 3D integration technologies provide many benefits, such as increased interconnect density and bandwidth which enable the reduction of the average load capacitance and resistance, resulting in higher speed and lower power consumption when compared to a typical 2D chip [122, 131]. Furthermore, the ability of these systems to include disparate circuit blocks with different performance requirements enables the unique opportunity for heterogeneity and diversification of technologies.

1.2.1 Interconnect Hierarchy

In 3D integration, the communication among the stacked sections of the chip requires vertical interconnections [131]. The interconnect design in 3D integration is organized in a hierarchical manner, which is related to the industrial semiconductor supply chain, as depicted in Figure 1.5. The wafer fabrication stage requires 3D connections from narrow and short local interconnects between electrical components of the circuit block to wide and long intermediate and global interconnect layers in order to connect different circuit blocks [84]. Connections between adjacent interconnect planes are realized through "vias" which allow for the 3D stacking of interconnect levels. The most popular and innovative type of 3D technology at this stage is a special type of "via", which penetrates through an entire silicon wafer, known as a through silicon via (TSV). At the wafer-level packaging and assembly stages, different bond-pad and package interconnect structures are used, such as wire bonding, solder bumps, metal pillars, and redistribution layers (RDLs).

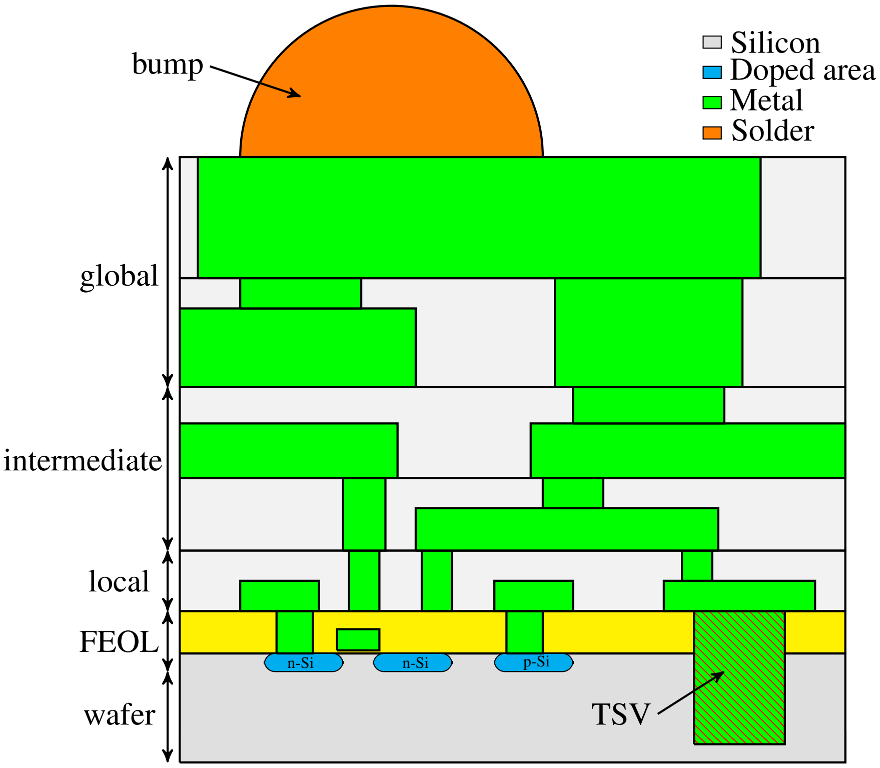


Figure 1.5: Classification of interconnects.

1.2.2 Classification and Designs

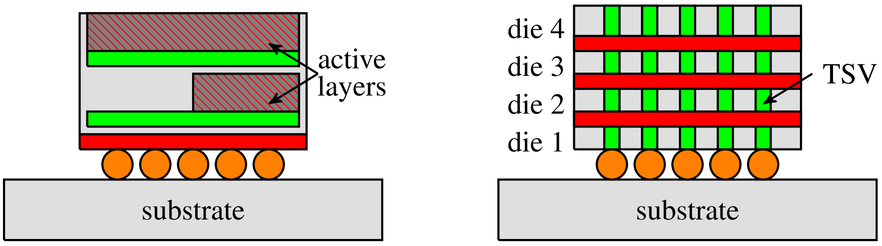
A 3D electrical integration system represents the entire chip divided into different blocks, which are the device layers of the chip with different functionalities. Each block is placed on an independent silicon layer and is stacked on the top of each other by making use of the vertical dimension [131]. There are a number of approaches to arrange circuit blocks in a vertical stack to obtain 3D integration. Based on the diverse functional requirements of each block and the processing stage during stacking, the International Technology Roadmap for Semiconductor (ITRS) proposed a classification of the wide spectrum of technologies in 3D integration [84]. There are different ways to realize 3D technologies based on their level of interconnect hierarchy and various stages of processing [150]:

1. 3D-integrated-circuit (3D-IC): integration approach which uses direct stacking of device layers using connections at the density level of local interconnects. It is generally described as the BEOL interconnect stack on multiple layers of FEOL devices during the wafer fabrication process. Since it is a process where stacked 2D device layers are connected together in the third dimension on a single semiconductor wafer, the 3D system obtained is treated as a monolithic structure, as depicted in Figure 1.6(a) [122].

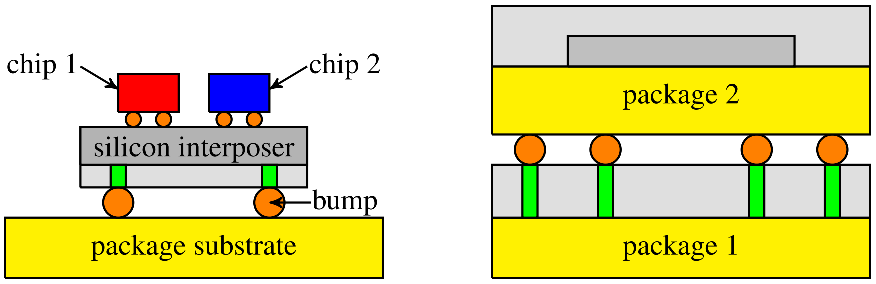
2. 3D-stacked-integrated-circuit (3D-SIC): 3D stack which is characterized by the sequential piling-up of multiple dies or wafers using vertical interconnects at the global and intermediate levels in order to achieve communication between different stacked layers (Figure 1.6(b)). These interconnects are typically TSVs with various diameters. Usually, high-density short and thin TSVs are required at the intermediate level, while long and wide, low-density TSV structures are needed at the higher hierarchical level [122]. The integration scheme is therefore a sequence of alternating FEOL devices and BEOL layers during wafer fabrication. Stacking approaches of ICs are die-to-die, die-to-wafer, and wafer-to-wafer [150].

3. 3D-wafer-level-packaging (3D-WLP): it extends the wafer fabrication process using RDLs and bumping processes to form interconnects at the bond-pad level. An interesting example of this strategy is the 2.5D interposer, where dies are mounted side by side on a silicon interface using TSVs through the interposer, as illustrated in Figure 1.6(c). The TSV density requirement is typically lower than that of the 3D-SIC system.

4. 3D-packaging (3D-P): integration scheme which achieves vertical stacking by relying on the traditional interconnect technologies at the package level, such as wire bonding, metal pillars, and solder bumps [106]. This includes 3D-system-in-package (3D-SiP), which is formed by stacking dies containing ICs with metal wires which are bonded to the package, and package-on-package (PoP), where the packages (SiPs) are stacked and interconnected using wire bond or flip-chip processes (Figure 1.6(d)).



(a) 3D-IC (b) 3D-SIC



(c) 3D-WLP (d) 3D-P

Figure 1.6: Schematic representations of the main 3D integration approaches: (a) 3D-IC, (b) 3D-SIC, (c) 3D-WLP, and (d) 3D-P.

1.3 Interconnect Technologies

The vertical electrical interconnections can be created in several ways and at different stages of the fabrication process flow to make 3D integration a reality. In the following sections, descriptions of two important classes of 3D interconnect technologies used at the wafer and/or package fabrication level will be described. Starting from the bottom-most layer, a particular interest comes from the TSV structure, which is used for 3D-SIC and 3D-WLP technologies and represents the most common and successful interconnect approach for 3D integration. TSV design is at the heart of 3D integration and has gained much attention over the last decades in industrial application in the field of electronics, optoelectronics, medical systems, sensor, MEMS, etc. [115]. By following the metallization stacking process until the packaging level, flip-chip solder bumps offer better opportunities as peripheral vertical interconnects between dies or packages to overcome the constraints of wire bonding [122]. Recently, the demand on the 3D integration to use a combination of TSVs and micro-bumps has been increased to obtain better electrical performance and smaller form factors even at the wafer level [141].

1.3.1 Through Silicon Vias Approaches

The most innovative and efficient way in which to exploit the third dimension in wafer and die level 3D integration techniques is to employ the TSV, a direct vertical connection between different levels of a chip. It consists of a conducting via which passes through the silicon substrate and connects the two sides of the wafer. Typically, the interplane via is etched and filled with metal, such as tungsten (W) or copper (Cu) [122].

In Figure 1.7, the general design of a TSV is shown as a cylinder of conducting material which is electrically isolated from the silicon wafer by an isolation layer, typically made of silicon dioxide (SiO_2) and called TSV liner, surrounding the TSV conductor [84].

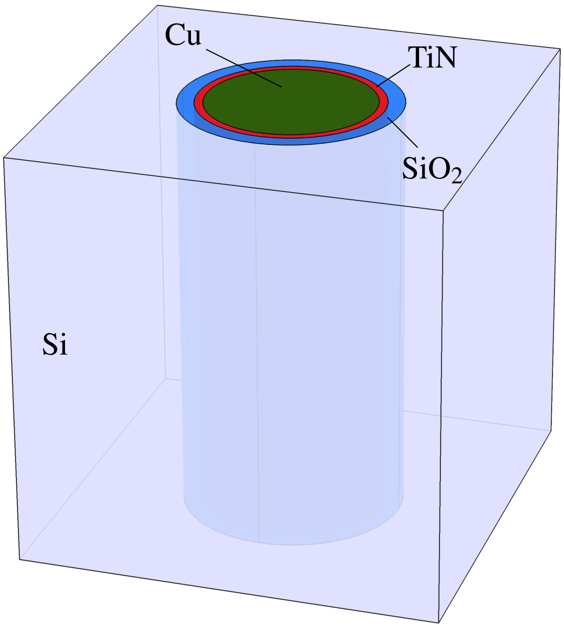


Figure 1.7: 3D view of a TSV structure.

The function of the insulator is to prevent leakage and resistive coupling through the silicon [131]. Furthermore, a barrier layer, typically titanium nitride (TiN), between the liner and the conductor avoids the metal diffusion into the silicon substrate. The features of a TSV are dependent of its electrical parameters, such as metal conductivity and dielectric permittivity, and geometrical characteristics. In particular, the pitch and the aspect ratio of the TSV have a strong impact on the distribution of the TSVs during the fabrication process. TSV pitch is defined as the distance between two TSVs, while the TSV aspect ratio is determined as the ratio of the depth to the diameter of the TSV cavity. Usually, TSV structures are manufactured as an array in a silicon substrate [131]. Depending on the application and technology requirements, the maximum number of TSVs in the array is achieved only when the smallest TSV diameter with the minimum pitch is used [159]. Large size TSVs have diameters larger than 10μm, small aspect ratios of about 1 or 2, and serve as bond-pad interconnects in 3D-WLP technologies [155]. In 3D-SICs, medium size TSVs are used as global interconnects with diameters between 2μm and 10μm, while the smallest size TSVs are used at the local interconnect level.

3D integration technologies with TSVs can be realized by employing several methods, which usually involve a sequence of wafer thinning and handling, TSV formation, stacking orientation, and bonding [150]. The sequence of these basic technology modules may vary, resulting in different fabrication process flows. Diverse process approaches can be developed by changing the order of the TSV fabrication with respect to the device wafer fabrication to obtain the so-called "via first", "via middle", or "via last" process sequences. Another fabrication decision is related to the different options for stacking orientation, namely face-to-face and back-to-face alignments. Furthermore, different methods of 3D bonding, which joins two die or wafer surfaces together, depend on the key requirements of chip size, alignment accuracy, and the operations of temporary or permanent bonding [84].

A 3D system with vertical interconnects implemented as TSVs provides higher interconnect bandwidth, increased integration density, and higher performance per unit area, as well as a reduced interconnect length and power consumption when compared to the packaging level vias. Furthermore, another advantage of this approach is its resulting low contact resistance [95]. Besides its many benefits, big concerns in 3D integration with TSVs are influences of metal contamination and mechanical stress generation in the region surrounding the TSV [94]. In particular, significant thermo-mechanical stresses are induced around the TSV, when the structure is subject to temperature loading during thermal processing, due to the large mismatch in the coefficients of thermal expansion between the TSV conductor and the silicon wafer. These stresses can be high enough to influence the reliability of TSV-based 3D integration technologies. Furthermore, the TSV has limited width and thickness, due to limitations in the etching and metal deposition processes, respectively.

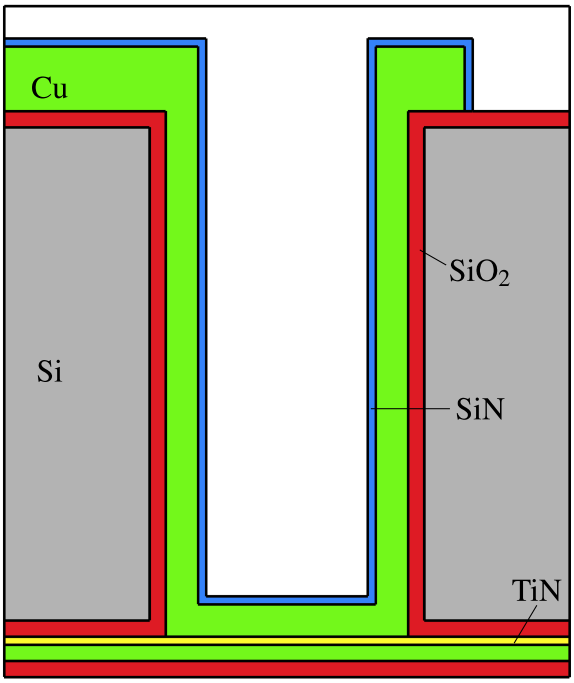


Figure 1.8: Cross section view of an open TSV structure.

In order to overcome the thermo-mechanical issues induced by the thermal processing steps, a new concept for wafer-to-wafer integration, based on unfilled TSV technologies has been introduced in the last years [24, 95, 109]. The new TSV design depicted in Figure 1.8

shows how the vertical cylinder of conducting material is replaced by a metallization layer, deposited by electroplating on the cylindrical wall of the structure, resulting in a hollow cylinder closed on the bottom side [162]. By implementing an unfilled TSV design, the so-called open TSV, the thermo-mechanical issues induced by the materials properties are minimized. Furthermore, distinctive benefits of this specific TSV technology include a relatively large TSV sidewall surface area and a thin metal layer.

1.3.2 Solder Bumps

Wire bonding is considered the most common technique for making interconnections between an IC and its packaging during the fabrication process. Due to the increased number of dies on a SiP, bonding wires can exhibit parasitic impedance and reduced interconnect bandwidth [122]. The introduction of new interconnect technologies permits to overcome the limitations of wire bonding. The typical communication mechanism among different dies or packages of the 3D stack is realized in a flip-chip manner through solder bumps, which is in contrast to the older wire bonding technology. In particular, a greater number of dies can be integrated by employing an area array of solder bumps to connect silicon chips to the first level packaging substrates [34].

Flip-chip is a 3D-WLP bonding technique which provides the connections among the levels of the 3D stack with solder bumps [153]. Once the ICs are created on the wafer, the chip pads are metallized on the top side of the ICs during the final wafer processing step [122]. Solder bumps are deposited on each of the chip pads. Then, in order to attach the wafer to another substrate, it is "flipped" or faced down and aligned so that the solder bumps are facing the bond pads on the substrate [122], as depicted in Figure 1.9(a). Bumps are remelted and, in most cases, the mounted chip is underfilled with an electrically non-conductive material.

Figure 1.9(b) shows the details of a solder bump structure. The bump is typically realized as a solder interconnect, formulated in binary, ternary or quaternary alloy system with different combinations of tin (Sn), silver (Ag), and Cu [31]. A thin film under-bump-metallization (UBM), which is usually made of nickel (Ni), is introduced on the chip bond pads during the solder bumping process in order to separate the bump from the surrounding metal interconnect lines on the chip side. The selection of an appropriate UBM layer becomes a key process for the development of reliable flip-chip solder bumps. The main function of the UBM layer is to reduce the current crowding effect and maximum hot-spot temperature near the contact between the bump and the surrounding metal line in order to improve the lifetime of the technology [32]. In turn, on the substrate side, the metallic bond pad enables the contact between the solder bump and the metallization on the substrate.

Solder bumps constitute important elements of the 3D stacking process since they serve several functions in the flip-chip assembly [126]. Bumps provide both the electrically and thermally conductive paths to carry electrical current and heat from the chip to the substrate. In addition, they guarantee the mechanical support during the mounting of the die to the substrate, because they mitigate the mechanical strain between chip and substrate. Furthermore, the height of the solder bump core provides the necessary space between successive layers, preventing the electrical contact between their conductors.

The typical diameter of a flip-chip solder bump for 3D-WLP technologies is in the range from 100μm to 200μm [122]. Advancements in the bonding processing technique have resulted in a decreased diameter of solder bumps to a range between 30μm and 50μm. In recent years, bumps containing a plastic solder ball have been introduced in order to extend the reliability of the flip-chip technology used in electronic products [158]. However, the trend of miniaturization continues to scale down the bump diameter, increasing current density in the solder bump.

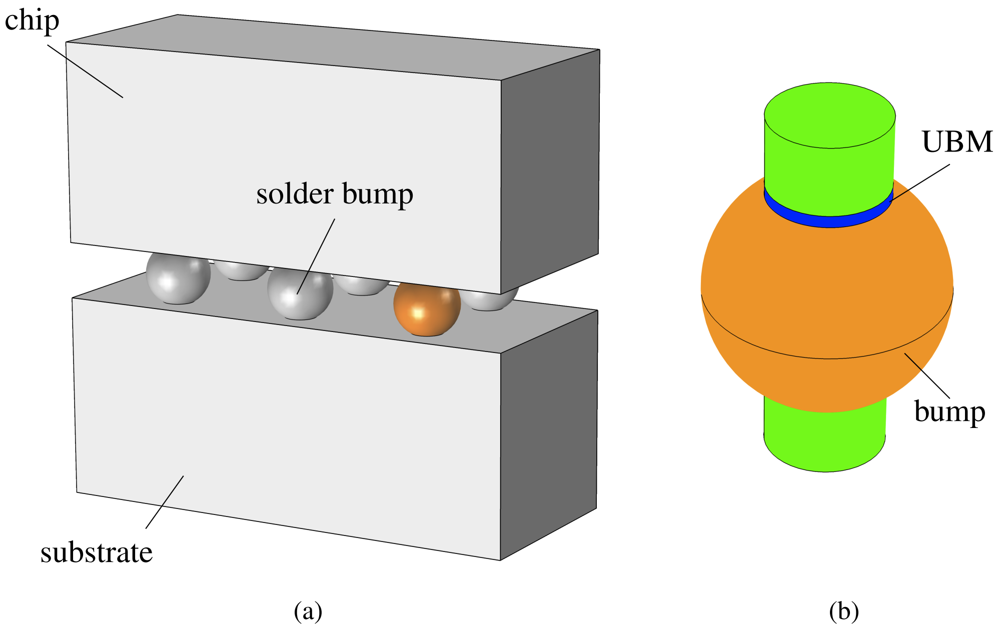


Figure 1.9: (a) Example of 3D integration with solder bumps. (b) Zoomed-in detailed profile view of a solder bump.

1.3.3 Reliability Issues

Although 3D interconnect technologies show distinct advantages and their manufacturing process has almost reached the status of mass production, there are several reliability concerns, as is often the case in emerging technology. Failures in interconnects are the result of the continued increase in interconnect density in the 3D integration design and the necessity of more intense device operative conditions due to the ongoing miniaturization. Reliability issues in interconnects are related to the changes of material properties of metals and dielectrics, such as metal resistivity and dielectric permittivity, beyond critical values, which prevent the intended functions of the ICs, leading to wear-out and defect-related problems. Both metal and dielectric layers play an important role in the reliability of the interconnect system [84]. Metal reliability is typically evaluated by investigating the electrical properties of the material which affect the current density that the metal can carry and, consequently, the resistance of the entire interconnect system. The resulting wear-out failure mechanisms, which occur under the operation of the device, are electromigration and stress induced degradation. As already discussed in Section 1.1.3, the importance of introducing low-κ dielectric materials increases with reduced dimension and material scaling, which influences the reliability of the interconnect causing defect-related problems, such as leakage and dielectric breakdown. The general issue of low-κ materials is that they are generally soft and weakly bonded to the silicon or metal lines [6]. The poor adhesion between the metal and the dielectric material results in the development of mechanical stress at their interface.

All 3D interconnect structures described in the previous sections have their specific reliability issues. In TSV-based integrations, reliability concerns are typically identified at the interface of the TSV and at the adjacent metallization levels [61], while electromigration induces voiding at the contact window on the chip side in solder bumps with UBM layer [26]. The main reliability issues in such 3D interconnect structures can be summarized in three categories:

- Stress related degradation: mechanical stress effects which result in local failures affecting the stability and performance of the interconnect system. Several reliability studies [24, 61, 95] recognize different local wear-out phenomena in interconnects related to thermo-mechanical issues, such as delamination and cracking at the TSV interface or inside solder bumps. Furthermore, the variation of the mechanical strength of the chip, which depends on the design of the interconnect arrays, can cause reliability concerns in the system, such as crack propagation and changes in the mobility of carriers [26].

- Electromigration related failure: it is a wear-out and failure mechanism which is typically related to the high current density which flows in a metal interconnect [84]. Electromigration is a key aspect of interconnect reliability assessment. It is described as the biased motion of atoms towards the anode or cathode of metal lines [46]. A characteristic of electromigration wear-out mechanism is that it causes failure by inducing the nucleation of voids in the metal line. Voids nucleate in the interconnect due to the development of tensile stress, particularly at those locations where the adhesion between the metal layer and the surrounding material is weak [63]. For TSV-based integrations, these sites are observed close to the metallization barrier between the TSV and the adjacent metal RDL [61]. Electromigration behavior in flip-chip solder bumps is expected to be different. During electromigration, an intermetallic compound (IMC) is formed due to the current-induced stress [110, 111]; the nucleation of a void due to the induced stress may occur at the interface between the bump and the IMC [84].

- Heat transfer related degradation: the components of a chip which generate heat are solder bumps, contact metallization, metal interconnects, and transistors. Heat generation increases with the number of chips in the 3D stack and heat dissipation is a challenging issue. Heat degradation mechanism is a consequence of the multiple effect of the increased temperature during electromigration- and stress-induced degradation processes. On one hand side, the effect of an increased temperature gradient in a 3D design intensifies the material transport by increasing diffusion coefficients; on the other hand side, it activates dislocation movements resulting in plastic effects in the metal interconnects [26]. It is clear that heat transfer problems must be addressed to electromigration and stress-related issues.

Electromigration and stress-induced wear-out phenomena, which affect the interconnect reliability, act together leading to changes in the electrical characteristics of the materials composing the interconnect structure [26]. Since the physics behind the electromigration phenomenon is well understood, it can be employed to the comprehension of the electromigration failure mechanisms in 3D integration technologies. Furthermore, it can provide a stronger basis for design of reliable interconnects and contributes for explaining experimental observations. Therefore, design engineers need to be aware of the active wear-out failure mechanisms which result from electromigration phenomenon. Electromigration becomes a limiting factor for high current density flow in interconnects and reduces the lifetime of the technology. The identification of failure modes and the prediction of reliability limits related to electromigration are therefore a crucial necessity in 3D integration. The electromigration phenomenon will be dealt with in more detail in the following section.

1.4 Electromigration Failure

In an interconnect subjected to a high electrical current, a motion of metal atoms takes place in the same direction as the current flow [29]. This phenomenon is called electromigration, which is the process of mass transport due to current flow towards the anode of a metal line and is the most important cause of failure in interconnects.

Fundamentally, electromigration is a quantum mechanical effect caused by the action of the local electric field and the resulting scattering of conducting electrons on lattice atoms. The contributions of these two microscopic processes on the atoms result in the electromigration driving force, which acts on metal ions and causes their migration in the metal line. Beside this driving force, electromigration is a complex multiphysics problem which includes the actions of other mechanisms responsible for the material transport inside the metal, such as diffusion, thermo-migration, and stress-migration [20]. The driving force of diffusion is represented by the vacancy concentration gradient, while the driving forces of thermo- and stress-migration are gradients in temperature and mechanical stress, respectively.

In a typical interconnect composed of conducting and insulating dielectric materials, the mass transport leads to an accumulation of atoms at the anode end of the metal line, due to the constraints imposed by the surrounding layer which prevents metal migration into the dielectric [84]. At the same time, depletion of atoms occurs at the cathode end of the line. The material transport culminates in the build-up of mechanical stress in the structure which results in two distinctive failures. Compressive stress arises due to atom accumulation and causes the formation of a hillock at the anode end of the metal, degrading the surrounding dielectric material and resulting in a short circuit. On the other end of the line, depletion of atoms induces the development of tensile stress, leading to void nucleation. The tensile stress for void nucleation is lower than that for extrusion formation and can be easily reached in an interconnect under electromigration [64, 118]. Therefore, the nucleation of a void is the dominant mechanism of electromigration failure rather than the formation of a hillock. Once the void has formed, its eventual propagation across the interconnect width can cause extremely high changes in the interconnect resistance and even open circuit failure.

1.4.1 Failure Phases

The electromigration failure development is normally characterized by the increase in the resistance in the interconnect line as a function of time. The electromigration resistance trace can be obtained by monitoring the electrical resistance of an interconnect under accelerated test conditions of increased temperature and current density [61]. Two periods are observed in the electromigration resistance trace: a first flat constant section, followed by a sudden non-linear increase period (Figure 1.10).

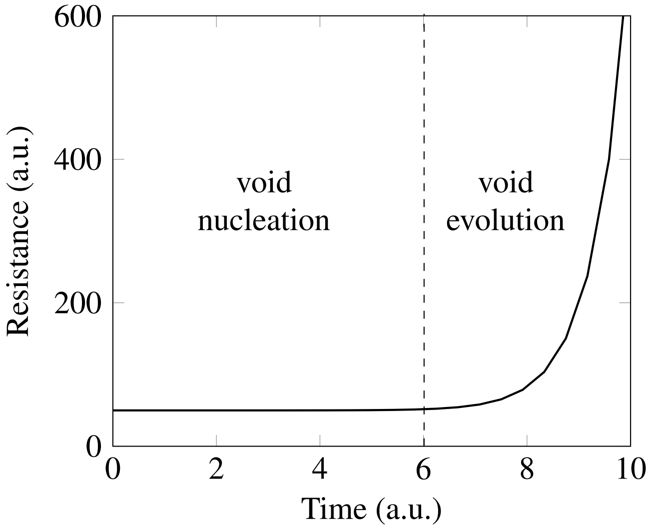


Figure 1.10: Typical electromigration resistance change with time for a given interconnect. Two electromigration failure phases are shown.

The first stage, namely the void nucleation or initiation phase, is characterized by the nucleation of a void which remains electrically undetectable. Therefore, the interconnect resistance remains constant during the entire void nucleation period. The nucleation of a void is the beginning of the second stage, which is called void evolution phase. During this phase, the void evolution mechanism leads to a morphological change of the void surface at a constant void volume. As soon as the void size becomes larger, a measurable resistance increase with time begins. The interconnect fails after a maximum tolerable resistance level is reached. The time-to-failure (TTF) is defined as the time needed to achieve this maximum tolerable resistance value. Consequently, the prediction of the electromigration TTF becomes crucial for the assessment of the interconnect reliability. The complete evaluation of the electromigration failure time of the given interconnect requires the summation of both void nucleation and void evolution times. The contribution of each component in the electromigration lifetime estimation depends on different kinetic and physical effects related to the different phases of failure.

1.4.2 Accelerated Lifetime Test

The electromigration lifetime of an interconnect at normal operating conditions of temperature and current density is usually more than ten years. In order to identify the different mechanisms involved in the electromigration failure and their impact on the interconnect reliability for a period much shorter than its expected lifetime, the use of accelerated electromigration tests is necessary [52]. The electromigration tests are carried out using a group of interconnects with similar features, subjected to stress conditions more severe than would normally be encountered in use in order to accelerate the electromigration failure. For copper-based interconnects, the accelerated test requires temperatures in the range from 200°C to 350°C and current densities in the order of $5\text{mA}/\mu\text{m}^2$ to $45\text{mA}/\mu\text{m}^2$ [29, 149].

As described in Section 1.4.1, the electromigration TTF of a given interconnect is determined by monitoring its resistance change with time. The electromigration lifetime test of interconnect lines is the most commonly used method for evaluating their resistance change [48]. Other test methods related to the industrial assessment of electromigration reliability of the interconnects are the classic resistometric method (CRM) [128], the temperature-ramp resistance analysis to characterize electromigration (TRACE) method [121], the breakdown energy of metal (BEM) method [80], the standard wafer-level electromigration acceleration test (SWEAT) method [127], and the wafer-level isothermal Joule heated electromigration test (WIJET) method [86].

Electromigration lifetime-testing includes precise resistance measurements under accelerated test conditions. The electrical resistance of a metal line changes with time under the influence of an electric current. Such changes come primarily from the material transport due to electromigration along the conductor which leads to the nucleation of voids. When some of them reach a certain size required to form a stable void, which is able to grow under continued electromigration conditions, the interconnect resistance increases. This increase is due to the cross sectional area of the line being reduced due to the presence of the newly-created void, forcing the current to flow through the resistive surrounding layer. In performing an electromigration test, a given percentage change in resistance of an interconnect under stress conditions forms the failure criterion. Typically, interconnect failure occurs when a resistance increase of 20% is attained [152]. The electromigration test is stopped after reaching the given failure criterion and the TTF of the given test structure is therefore determined by the time necessary to achieve this threshold value. Since the electromigration test is carried out for a sample of similar interconnect structures in order to ensure the credibility of test data in a reasonable time frame [149], the results of the experiments are usually given in terms of mean-time-to-failure (MTTF), which is the time needed to reach the failure of the half of the group of similar structures [79], and the standard deviation of a lognormal distribution of electromigration lifetimes for the given sample. The distribution of lifetimes obtained from accelerated test has to be related to the use conditions, in order to estimate the interconnect lifetime under real operating temperatures and current densities.

1.4.3 Black's Equation

The dependence of the MTTF of the lognormal lifetime distribution on the acceleration parameters of temperature T and current density j is normally described by an Arrhenius-like semi-empirical equation originally formulated by Black [12–14] and then modified by Blair [15] in the form

$$MTTF = Aj^{-n} \exp\left(\frac{E_{\mathrm{a}}}{k_{\mathrm{B}}T}\right), \tag{1.1}$$

where A is a constant which contains several physical and geometrical properties of the materials, n is the current density exponent, E_{a} is the activation energy for electromigration-induced failure, and k_{B} is the Boltzmann constant. Black's original empirical work predicted a failure time following a j^{-2} dependence [12], while later experimental studies estimated values of n generally lying between 1 and 3 [138].

The estimation of the current density exponent n can be determined from the results of the electromigration accelerated tests by taking the natural logarithm of equation (1.1) as follows

$$\ln MTTF = \ln A - n \ln j + \frac{E_{\mathrm{a}}}{k_{\mathrm{B}}T}. \tag{1.2}$$

The sample estimate for the current density exponent n can be obtained from a linear regression analysis for one independent variable [52]. The analysis requires lifetime data from several electromigration tests conducted at different stress conditions of current density, while the stress temperature of the test structures is kept constant. A plot of the MTTF as a function of current density represents data points aligned along a straight line, which is the best fit to the data, as depicted in Figure 1.11. The angular coefficient of the line determines the current density exponent n.

It has been shown that a current density exponent n value close to 2 indicates a lognormal lifetime distribution, which corresponds to a nucleation time dominated failure [36, 63, 138], while a value close to 1 indicates that the dominant phase of the electromigration failure time is the void evolution [51, 104]. At a constant given temperature, Black's equation generalizes to

$$MTTF = t_{\mathrm{N}} + t_{\mathrm{E}} = Bj^{-2} + Cj^{-1}, \tag{1.3}$$

where B and C are materials constants, t_{N} is the void nucleation time, and t_{E} is the void evolution time. The model in equation (1.3) assumes that the phases which dominate the electromigration-induced failure under accelerated test conditions are the same of those under device operating conditions [79].

1.4.4 Test Data Analysis and Lifetime Extrapolation

The primary interest for performing an accelerated electromigration test is to ensure the reliability of the interconnect by analyzing its lifetime under realistic use conditions [149]. The data resulting from the electromigration experiments should therefore be extrapolated to the device operating conditions, which are usually at room temperature and at a current density stress below $5\mathrm{mA}/\mu\mathrm{m}^2$ [79].

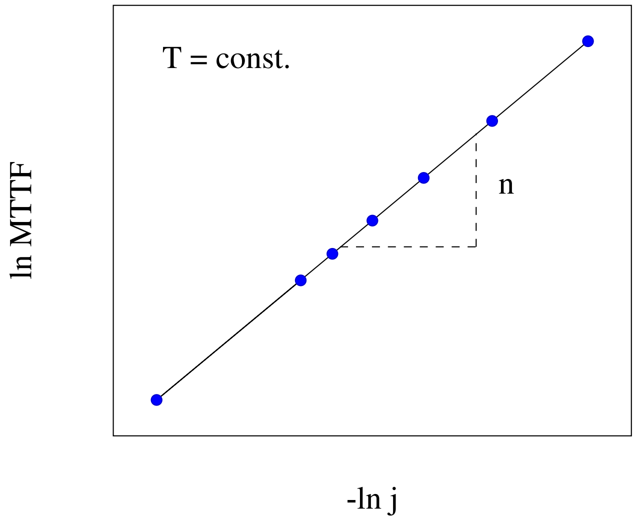


Figure 1.11: Time to failure dependence on current density illustrates the behavior of equation (1.2) for a constant test temperature. The line indicates the fitting to the data from which the determination of the current density exponent is obtained from its angular coefficient.

The extrapolation is generally performed based on a lognormal statistical distribution of the measured individual lifetimes obtained for each structure of the sample [44, 51, 56, 75]. The sample estimates for the MTTF and the standard deviation σ of a lognormal distribution are calculated from the average and the standard deviation of the natural logarithm of the individual lifetimes data, respectively, obtained from several electromigration stress tests with different stress conditions, as follows [52]

$$\ln MTTF = \frac{\sum_{k=1}^{S} \ln TTF_k}{S} \tag{1.4}$$

and

$$\sigma = \sqrt{\frac{\sum_{k=1}^{S} (\ln TTF_k - \ln MTTF)^2}{S-1}}, \tag{1.5}$$

where S is the sample size and TTF_k is the lifetime of the k^{th} interconnect test structure of the sample. The lifetime lognormal distribution is characterized by a probability density function (PDF) in the form [73]

$$PDF(t) = \frac{1}{\sigma t \sqrt{2\pi}} \exp\left(-\frac{(\ln t - \ln MTTF)^2}{2\sigma^2} \right) \tag{1.6}$$

and the corresponding cumulative density function (CDF), which represents the probability that a randomly chosen part of the sample will fail by a time t', is given by

$$CDF(t) = \int_0^{t'} \frac{1}{\sigma t \sqrt{2\pi}} \exp\left(-\frac{(\ln t - \ln MTTF)^2}{2\sigma^2}\right) \mathrm{d}t. \tag{1.7}$$

Solving the integral from equation (1.7), we obtain

$$CDF(t) = \Psi\left(\frac{\ln(t/MTTF)}{\sigma}\right), \tag{1.8}$$

where Ψ is the integral of the Gaussian function [29, 73]. Once the MTTF and the deviation standard are determined, the extrapolation of the electromigration lifetime from testing ($stress$) to operative ($oper$) conditions is calculated, based on Black's equation, as follows [75]

$$TTF_{oper} = MTTF_{stress}\left(\frac{j_{stress}}{j_{oper}}\right)^n \exp\left[\frac{E_\mathrm{a}}{k_\mathrm{B}}\left(\frac{1}{T_{stress}} - \frac{1}{T_{oper}}\right) + \Psi^{-1}(f_{max})\sigma\right], \tag{1.9}$$

where $\Psi^{-1}(f_{max})$ is the inverse of the normal cumulative distribution function at a given maximum tolerable percentile of cumulative failure f_{max} at real operating conditions. The last exponential term in equation (1.9) allows to extrapolate the failure of the accelerated test (50%) to a small percentage accepted under operative conditions (0.01%) [40]. The lifetime under use conditions TTF_{oper} can be controlled by adjusting the parameters governing the lognormal distribution in equation (1.9). Its value is intensified by increasing the MTTF as well as reducing the standard deviation.

Electromigration lifetimes are usually described by a lognormal distribution, but multi-lognormal [160] and bimodal distributions [57] can also be used to statistically describe and analyze the lifetimes obtained from experimental tests.

The goal of the extrapolation methodology is to obtain the parameters relating the dominant physical effects which affect the electromigration induced failure. These parameters are the current density exponent n, related to the dominant phase of failure, and the activation energy E_a, related to the dominant mechanism of material transport in the interconnect line [40]. These parameters are extracted from the accelerated tests and are also valid at real operating conditions. The procedure for the estimation of the current density exponent n and its impact on the lifetime prediction is described in Section 1.4.3. The activation energy E_a can be determined in a similar manner [52]; its influence on the electromigration lifetime is related to the dependence of the transport of the material caused by electromigration on different available diffusivity paths in the interconnect.

1.4.5 Impact of Microstructure and Material Interfaces

Testing a group of metal structures at different stress temperatures, for a constant applied current density, permits to extract the activation energy E_a as the angular coefficient of the line-fit to the data of the $\ln MTTF$ vs $1/T$ plot [52]. The activation energy E_a, obtained from the results of the electromigration stress tests, can be taken as a useful parameter to determine the dominant diffusion path for electromigration-induced material transport in the interconnect. One or more diffusion paths for metal atoms dominate the electromigration failure and they can be summarized as bulk, grain boundaries, and material interfaces, as illustrated in Figure 1.12.

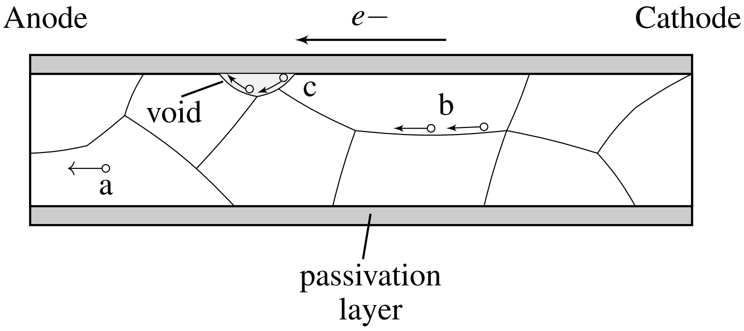


Figure 1.12: Main diffusion paths in a passivated interconnect structure: a) bulk, b) grain boundary, and c) material interface.

For copper-based interconnects, the estimated values of the activation energy for the different diffusion paths are listed in Table 1.1 [105]. For diffusion paths with low values of activation energy, the diffusion of atoms along the given path is energetically favorable because the energy barrier to promote diffusion at this site is lower compared to paths with high values of activation energy. Low values of activation energy lead to fast diffusion paths. Since the diffusion along these paths is fast, the mechanism of electromigration degradation is accelerated reducing the interconnect lifetime. To sum up briefly, low values of activation energy lead to higher diffusivities resulting in shorter MTTFs, while high values enhance the electromigration lifetime estimation. Since the contribution from the bulk diffusion is very small compared to the contribution from the grain boundary and material interfaces, the role of grain boundaries and material interfaces should be taken into account in the reliability assessment of the interconnect under the influence of electromigration.

Table 1.1: Activation energies for various diffusional paths in copper interconnects [105].

Diffusion path	Activation energy E_a (eV)
Bulk	2.1
Grain boundary	1.2
Material interface	0.8-1.2

Several micro-structural features, such as grain size and texture strongly influence the electromigration lifetime [149]. The ratio (r_g), described as the average grain size divided by line width, is an important parameter to quantify the microstructure properties of an interconnect [49]. If the ratio $g > 1$, the grain size is comparable to the line width and the microstructure of the interconnect assumes a bamboo-like pattern. For $g < 1$, the interconnect line presents a polycristalline structure in which the network of small grains provides additional paths for material transport due to the formation of grain boundaries running parallel to the current flow and triple points, generated from the intersection of two or more grains, as sites of void nucleation. Since the grain boundary density in bamboo microstructure lines is smaller than in polycristalline lines, the contribution of mass transport by electromigration along grain boundaries is negligible. Grain boundary diffusion is the dominant transport mechanism for polycristalline lines [1]. Texture and grain size distribution are other important factors which influence the electromigration characteristics, especially in polycristalline structures. In particular, as the grain size distribution becomes broader and the grains are randomly oriented, the standard deviation of the lifetime distribution increases leading to a reduction in the MTTF [92].

Since the activation energy value for diffusion at material interfaces in copper-based interconnects is the lowest value measured (Table 1.1), it is evident that diffusion of atoms in this metallization lines is interface dominated and has an early effect on electromigration failure. As described in Section 1.2, a typical interconnect consists of a metal line surrounded by a passivation layer. The interfaces between the passivation layer and the metal line are the fast diffusion paths and the adhesion between the two materials influences the quality of the interface [99]. If the adhesion between metal and passivation layer is weak, the interface is considered slightly bonded which allows and enhances the material diffusion along the path. At the site of weak adhesion, void nucleation is much easier because the stress necessary to nucleate a stable void is significantly reduced compared to the threshold stress value for void nucleation reached at the grain boundaries. Furthermore, the void evolution mechanism at this site is a consequence of the material diffusion along the void surface, which is faster in the presence of a poorly adhered interface.

1.4.6 Electromigration Modeling

The extensive methodology of electromigration testing, presented in the previous sections, leads to a qualitative understanding of the factors which affect the electromigration reliability of interconnects, especially when the results are extrapolated to real operating conditions. The underlying mechanisms which are interacting during the degradation process, initiated by the electromigration test, are often difficult to identify. Furthermore, the times needed to perform the experimental tests are extremely long. The most viable solution for the recognition of the dominant failure mechanisms of electromigration and their relationship with the interconnect structure and its materials is to employ simulations using physical models. For this purpose, the use of technology computer aided design (TCAD) becomes necessary. It comprises physical modeling, numerical implementation of these models, simulations, and analysis and post-processing of the simulation results with the scope to relate them to experimental observations. TCAD is a useful tool which provides designers with additional information to better understanding the causes and speed of electromigration-induced failure. Models are implemented using the finite element method (FEM), which allows to obtain numerical solutions representing the physical process of degradation of interconnect structures [148]. With the help of FEM, the understanding of the electromigration failure mechanism and the explanation of experimental observations are provided in order to improve design and manufacture of more reliable interconnects. The use of FEM-based tools for electromigration modeling and simulation is therefore a must for a more thorough analysis of the electromigration wear-out failure.

A general electromigration model should be able to reproduce experimental observations of the electromigration failure. As already mentioned, electromigration failure goes through two distinct phases, namely void nucleation and void evolution phase. Each phase is based on different physical phenomena and exhibits a different influence on the operating features of the interconnect [29]. The development of the electromigration model is therefore related to the contribution of each phase on the electromigration-induced failure and requires an analysis in two parts. The goal of electromigration modeling is to determine the interconnect lifetime from the simulation results as the sum of the void nucleation time and the void evolution time, as presented in equation (1.3). These results are related to those obtained from the reliability experimental tests, in order to verify the assumptions made for the simulation of the electromigration failure in the interconnect.

1.5 Outline of the Thesis

The purpose of the work described in this document is to develop a physical model for the investigation of the electromigration problem in interconnects which takes into account all the most relevant effects related to electromigration degradation. The model treats the two phases of failure separately in order to extract essential information from a detailed analysis of each phase. Since the model is influenced by a wide variety of physical phenomena, it is convenient to implement it into a FEM-based simulation tool such as COMSOL Multiphysics® [38], which provides numerical solutions and contributes to the analysis of the results obtained for both failure phases. Moreover, the simulation software provides the ability to design the complex interconnect geometry on which the analysis must be performed. In this way, it is possible to investigate the electromigration failure in a variety of interconnect structures required for a better understanding of reliability in 3D integration technology, such as open copper TSVs and solder bumps.

The body of the thesis is arranged into six chapters as follows. Chapter 2 treats the history and the evolution on the studies of electromigration from early to modern times. Then, a detailed derivation of the driving force governing the electromigration failure and its action on the transport of metal atoms along the available diffusion paths over the interconnect are presented. This is followed by an overview of the state of the art for electromigration modeling, where the impact of the stress build-up due to electromigration, the derivation of the void nucleation condition, and several approaches for void evolution analysis are described.

Chapter 3 presents in detail the full continuum electromigration model, which includes all the mechanisms related to electromigration failure. Since electromigration modeling requires a multiphysics approach, it is most conveniently separated into submodels. The submodels are comprised of the electro-thermal problem, vacancy dynamics problem, and solid mechanics model. The latter permits to determine the void nucleation condition and it therefore represents the beginning of the second phase of failure, the void evolution. The description of three different approaches to model the void evolution mechanism in interconnects is included in this chapter.

In Chapter 4, the numerical implementation of the physical model in a FEM-based tool is described. First, the chapter presents a basic introduction to FEM and gives an example of finite element analysis for a simple problem. Then, the general description of the capabilities of the simulation tool employed for electromigration simulations is introduced, followed by the presentation of a schematic procedure flow for electromigration studies.

Chapter 5 deals with the simulation studies of electromigration, carried out for different interconnect structures. Case studies of particular interest are open through silicon vias and flip-chip solder bumps. Furthermore, a newsworthy comparative study regarding the impact of geometry and microstructure on the electromigration failure development in standard interconnect lines is presented.

Finally, in Chapter 6 the work is summarized and possible further improvements concerning electromigration investigations are presented.

Chapter 2

Physical Description of Electromigration

2.1 The History of Electromigration

Electromigration phenomena have been studied for a long time. The first observation was reported by the french physicist M. Gerardin [79]. In 1861, he discovered electromigration in liquid alloys of lead-tin, potassium-sodium, gold, and bismuth in mercury. He was also the first person who thought in terms of electrostatic interactions between the field and metal ions in liquid metals and molten salts. The work of F. Skaupy [140] in 1914 introduced the idea of an "electron wind", which laid the foundation for the understanding of electromigration. From his studies on mass transport of impurities in molten metals, he underlined the significance of the interaction between atoms and moving charge carriers. In the 1950s, the first systematic studies of electromigration, based on the correlation between the direction of the current flow and the material transport, were presented by W. Seith and H. Wever [136]. By measuring the mass transport of a series of solid alloys and plotting it in a phase diagram, they observed that the direction of transport varies with the sign of the charge carriers, i.e. electrons or holes, in the specific alloy phase. They also introduced the "marker motion" technique, now called vacancy flux method, which permits to measure the electromigration-induced mass transport using the displacement of an indentation on a metal wire [79]. These experiments prompted the concept of an "electron wind" to account for the induced mass transport. The first mathematical formulations of the electromigration driving force have been derived independently by Fiks [55] and Huntington and Grone [82]. These authors treated the electron wind force by developing a "ballistic" approach based on the semiclassical collision process between mobile point defects and charge carriers. The investigations demonstrated the possibility of using electromigration to probe the interaction of moving atoms and charge carriers directly. All these theoretical ideas stimulated considerable technological interest during the 1960s in experimental studies on electromigration in integrated circuits.

2.1.1 1960s: Black's Equation

In 1966 Motorola, IBM, Texas Instruments, and Fairchild independently observed "cracked stripe" problems in aluminium interconnects in ICs. At this time, electromigration was recognized to be one of the main reasons for IC failure which threatened the microelectronics industry. While working for Motorola, J. R. Black was involved in the investigation of the origin of electromigration failure in aluminum conductors. Based on the work of Huntington and Grone [82], he derived a simple semi-empirical model for the time to failure prediction of aluminum film conductors stressed at high current densities and temperatures [12–14]. He assumed an entirely random motion of the electrons, both before and after collisions with ions under influence of the electric field. The electrons are accelerated and impart all of their full momentum to the ions during nearly elastic collisions. The rate of mass transport R_m by a momentum exchange between electrons and thermally activated ions may be expressed as

$$R_\mathrm{m} = FPN_\mathrm{e}N_\mathrm{a}\Sigma, \tag{2.1}$$

where F is a constant, P is the electron momentum, N_e is the number of electrons passing through a unit volume of metal per second, N_a is the number of activated ions available per cm^3, and Σ is the ionic scattering cross section. The momentum picked up by a conducting electron when falling through an electric field E over its mean free path p_f, with an average velocity v, is

$$P = eE\frac{p_\mathrm{f}}{v} = e\rho j\frac{p_\mathrm{f}}{v}, \tag{2.2}$$

where e is the electron charge, ρ is the volume resistivity of the metal, and j is the current density. The number of electrons per seconds available for striking the activated ions is related to j by

$$N_\mathrm{e} = n_\mathrm{e}v_\mathrm{d} = \frac{j}{e}, \tag{2.3}$$

where n_e is the electrons density, and v_d is the drift velocity which perturbs slightly the average velocity v. The equation for the number of activated metal ions which overcome a potential barrier E_a in the metal lattice follows the Arrhenius law

$$N_\mathrm{a} = F_1 \exp\left(-\frac{E_\mathrm{a}}{k_\mathrm{B}T}\right), \tag{2.4}$$

where F_1 contains the diffusion constants, E_a is the activation energy, k_B is the Boltzmann constant, and T is the film temperature. Since the MTTF of a metal conductor is related to the rate of mass transfer and the conducting cross section by

$$R_\mathrm{m} = \frac{F_2wt}{MTTF}, \tag{2.5}$$

where F_2 is a constant, w is the conductor width, and t is the film thickness, equation (2.1) may be rewritten by substituting equations (2.2) - (2.5). By consolidation of the constants, the Black's equation is obtained as follows

$$\frac{1}{MTTF} = Aj^2 \exp\left(-\frac{E_\mathrm{a}}{k_\mathrm{B}T}\right). \tag{2.6}$$

The constant A contains several physical properties such as the metal resistivity, the electron free path, the average velocity, the effective ionic scattering cross section for electrons, and the metal self-diffusion jump frequency factor. Based upon the above theory, experiments were designed and carried out to confirm that the failure rate of a group of identical aluminum stripes, which were exposed to the same electromigration stressing, is proportional to the inverse square of the current density. Furthermore, Black's equation can be an important tool for the design and the fabrication of highly reliable metal conductors for specific stress conditions of temperature and current density, as described in Chapter 1.

2.1.2 1970s: Blech Effect

In the late 1960s, Blech and Sello [17] discovered that electromigration in aluminum thin films could be a leading source of failure in planar semiconductor ICs. After that observation, the interest as well as the direction of electromigration studies have shifted their focus of the investigation to the aspect of electromigration damage in thin film conductors [48]. Different from bulk materials, the analysis of electromigration in thin films has shown that grain boundaries are particularly relevant to damage formation [79]. From the incorporation of copper in aluminum-based interconnects, IBM found out that copper atoms block the fast diffusivity paths at grain boundaries [29]. Furthermore, at that time, the idea of electron-ion interactions as a driving force fascinated material scientists to start to formulate a quantum mechanical approach in order to understand the physical phenomenon. The interest in a quantum mechanical description of electromigration has continued to the present time.

With the development of new interconnect technologies, research activities at Bell Labs led I. A. Blech and his coworkers to discover "immortal wires" in 1976 [16]. They designed electromigration experiments on thin aluminum films deposited onto titanium nitride surfaces. The passage of high electric current through the sample is mostly carried by the conductor layer due to its lower resistivity. The resulting induced atom flow, parallel to the direction of the electron flow, is related to the atom drift velocity v_d as follows

$$v_\mathrm{d} = Me|Z^*|\rho j, \tag{2.7}$$

where M is the mobility, and $e|Z^*|$ is the effective charge of the ions. By measuring the drift velocity responsible for the movement of the aluminum islands, they observed that only one side of the stripe moved according to equation (2.7) so that its length shrank. In turn, at the other end of the line, hillocks were formed. They also found that no electromigration-induced drift occurs below a critical applied current density. In order to explain these observations, the concept of the "back flow" drift velocity v_b, which acts against the electromigration drift velocity influencing the net forward drift velocity v_n, was proposed as follows

$$v_\mathrm{n} = v_\mathrm{d} - v_\mathrm{b} = Me|Z^*|\rho j - \frac{M\Delta F}{l} \approx Me|Z^*|\rho j - \frac{M\Omega_\mathrm{a}\Delta\sigma_\mathrm{xx}}{l}, \tag{2.8}$$

where ΔF is the free energy difference between line ends, l is the line length, Ω_a is the atomic volume, and $\Delta\sigma_\mathrm{xx}$ is the normal hydrostatic mechanical stress difference between line ends when voids and hillocks are formed. When the "back flow" of atoms, due to the presence of back stress in the line, equals the atom flow due to electromigration, the steady-state condition, so-called "Blech condition", is reached. Given the maximum stress σ_{thr} that the aluminum stripe can sustain before yielding, the critical product of current density and wire length for electromigration failure in thin aluminum films, the "Blech product", is given by

$$(jl)_{\mathrm{C}} = \frac{\Omega_{\mathrm{a}}(\sigma_{\mathrm{thr}} - \sigma_0)}{e|Z^*|\rho}, \tag{2.9}$$

where σ_0 is the stress at $x = 0$. Blech and coworkers were able to determine the critical line length l_{B}, well known as the "Blech length", from their measurements. When a line shrinks to the critical value due to the application of a given current density j, the line end stops moving, and electromigration halts. The applied threshold current density j_{C}, which a line can withstand before electromigration failure, can be similarly obtained. By following this approach, it was also possible to estimate the interconnect resistance against electromigration [40], and two electromigration failure modes in interconnects were identified, namely open circuit due to void formation and short circuit due to hillock formation. Furthermore, Blech was the first one to consider stress-migration as an additional driving force acting in the opposite direction of electromigration. The origin, as well as the nature of the mechanical back stress in microelectronic structures, are strongly influenced by the presence of the residual stress coming from the fabrication process, which could give false values of the Blech length and maximum operating current density [103].

2.1.3 1980s: Modification of Black's Equation

In the following ten years, the development of very large-scale integrated (VLSI) circuits led to the investigation of electromigration in small-dimension conductors assembled into a multilayered structure with insulation and barrier layers [79]. With the continuous shrinkage of the interconnect line width, researchers moved toward the improvement of the electromigration lifetime in the miniaturized electronic devices. For this purpose, the incorporation of copper or silicon in pure aluminum interconnects proved to be beneficial [154]. This advantage was mainly due to the significant reduction of the atom flow in fast diffusivity paths, when the grain size of the metal film is similar to the film width [149]. At this time, a drastic improvement in the electromigration performance was provided by the introduction of barrier materials, such as titanium and tungsten [139]. The adoption of refractory materials for metallization resulted in the protection from inter-diffusion between aluminum and silicon in the VLSI circuits, reducing electromigration failure.

With the ongoing miniaturization of ICs as well as the development of new interconnect materials, the validity and reliability of Black's equation, in predicting the interconnect lifetime, were becoming controversial [138]. The original formulation of equation (2.6) had already been modified in 1971 by Blair [15] as follows

$$MTTF = Aj^{-n}\exp\left(\frac{E_{\mathrm{a}}}{k_{\mathrm{B}}T}\right), \tag{2.10}$$

where the current density exponent n is a parameter which can be experimentally determined. He observed that experimental data could be fitted to equation (2.10) by allowing a variable current density exponent in the range between 1 and 2. In the 1980s, the different interpretation of the value of this parameter led to the separation of electromigration lifetime prediction models in three classes. The categorization was based on the impact of the contribution of two electromigration failure phases on the MTTF estimation, namely void nucleation and void evolution. An exponent value close to 2, as in the original Black's equation, means that the contribution of the void nucleation phase, due to the electromigration stress build-up, represents the major portion of the lifetime. In turn, the time necessary to grow a void and trigger a failure strongly dominates the electromigration lifetime estimation after a void was already formed. The void evolution mechanism implies a failure time proportional to the inverse of the current density because the mass transport due to electromigration is linearly dependent on the current density [138]. A failure model for lifetime evaluation based on the combination of the nucleation and the growth mechanisms should provide a more sophisticated understanding of the electromigration behavior [40].

Furthermore, Shatzkes and Lloyd [138] argued the application of both original and modified Black's equations, concluding that significant errors may arise in the lifetime extrapolation from accelerated tests. The experimental determination of A, n, and E_a in equation (2.10) yielded incorrect parameter values and, consequently, an incorrect lifetime estimation. The major shortcoming of Black's equation was that temperature gradients, together with Joule heating effects, were not included in the lifetime expression. From the solution of the continuity equation for the vacancy concentration with a perfectly blocking boundary, and assuming that failure occurs when the critical vacancy concentration value is reached (i.e. the void nucleation condition), the lifetime is obtained as follows

$$MTTF = BT^2 j^{-2} \exp\left(\frac{E_\mathrm{a}}{k_\mathrm{B}T}\right), \tag{2.11}$$

where the T^2 proportionality term does not appear in the original Black's equation. It should be pointed out that the theoretical model proposed by Shatzkes and Lloyd was the first one which rigorously explained the inverse square dependence on current density for the lifetime. Values above 2 can be attributed to extensive Joule heating effects.

2.1.4 From 1990s to Modern Times

In the late 1980s and 1990s, the introduction of pure copper-based interconnects took place. Copper was proposed because of its lower electrical resistivity and, therefore, much lower sensitivity to electromigration than aluminum [149]. These results, together with the development of novel process technologies, encouraged IBM and Motorola in 1997 to replace aluminum with copper in IC interconnects. In parallel to the development of the interconnect technology, new aspects of electromigration physics were introduced to the modeling. Different models of electromigration failure phenomenon for VLSI interconnections, based on the electromigration stress-induced voiding, were carried out [63, 91, 93, 133]. Furthermore, a new class of models based on the void surface evolution theory was initiated in the mid-1990s [3, 11, 71, 107].

In the last 20 years, the main focus of the electromigration study on copper-based interconnections was to improve the processing techniques in order to support the circuit speed requirement, and meet the demand for miniaturization of electronic devices. Furthermore, the advent of emerging interconnect structures, such as TSVs, poses a new challenge regarding electromigration reliability. For this purpose, mathematical modeling can significantly contribute to the comprehension of the electromigration failure mechanism in these new technologies. Since electromigration is influenced by different physical phenomena, modeling has became an extreme challenge. The complexity of the analytical models therefore requires the adoption of numerical simulations. The development of TCAD tools for simulating electromigration in interconnects permits to efficiently solve numerical calculations. In this way, several experimental observations can be explained, and the design of reliable interconnects can be improved.

2.2 Electromigration Driving Force

In a simple picture, electromigration can be described as the atomic migration caused by the contributions of two microscopic forces on mobile defects (Figure 2.1). The microscopic forces arise from the influence of the local electric field and the resulting electron transport in the conductor.

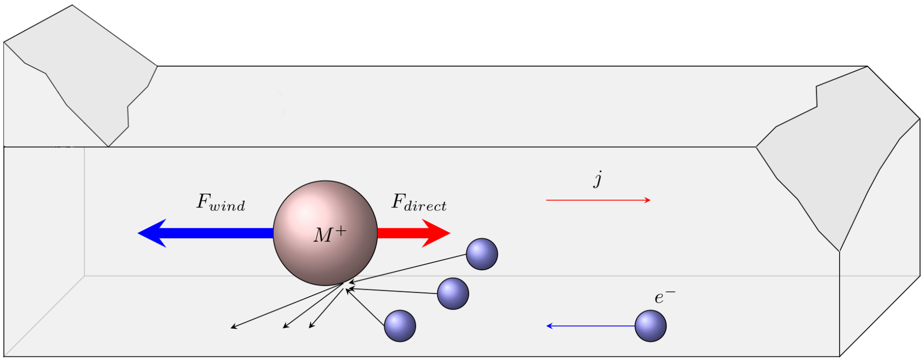


Figure 2.1: The two contributions of the electromigration driving force.

The electric field force $\vec{F}_{\text{direct}}$, often referred to as the "direct force", is caused by the direct action of the external macroscopic field $\vec{E}$ on the charge of the migrating metal ions [142]. The electrostatic force is the result of the interaction between ionic atoms, with valence Z, and the applied electric field, because the valence electrons responsible for electrical conductivity are no longer bound to the atomic nuclei. Furthermore, it takes into account the electrostatic screening s_{e} from the surrounding electrons [87]. The electrostatic force is given by

$$\vec{F}_{\text{direct}} = Z(1-s_{\text{e}})|e|\vec{E} = Z^{*}_{\text{direct}}|e|\vec{E}, \tag{2.12}$$

where Z^*_{direct} is the direct valence related to the nominal valence of the metallic ion when shielding processes are absent.

The second microscopic force responsible for atomic transport is a consequence of the "electron wind", described in Section 2.1. The semi-classical ballistic model of scattering, proposed independently by Fiks [55] and Huntington and Grone [82], is useful in describing the interaction between conducting electrons, carrying the electric current, and the migrating ions. The conducting electrons, driven by the external field, are scattered by point defects, and the resulting momentum transfer per unit time from scattering electrons to the impurities leads to the so-called "wind force" $\vec{F}_{\mathrm{wind}}$ as

$$\vec{F}_{\mathrm{wind}} = \frac{n_{\mathrm{e}}\rho_{\mathrm{d}}m_0}{n_{\mathrm{d}}\rho m^*}|e|\vec{E} = Z^*_{\mathrm{wind}}|e|\vec{E}, \tag{2.13}$$

where n_{e} is the conduction electrons density, ρ is the resistivity of the metal, n_{d} is the defects density, ρ_{d} is the defects resistivity contribution, m_0 is the mass of the free electrons, and m^* is the effective electron mass. The wind valence Z^*_{wind} is related to the magnitude and the direction of the momentum exchange between conducting electrons and point defects. Quantum-mechanical approaches of the electron wind effect were provided by Bosvieux and Friedel [18], Kummar and Sorbello [97], Sham [137], and Schaich [134].

By summing equations (2.12) and (2.13), the total electromigration driving force $\vec{F}_{\mathrm{EM}}$ acting on a metal ion can be written as

$$\vec{F}_{\mathrm{EM}} = \vec{F}_{\mathrm{direct}} + \vec{F}_{\mathrm{wind}} = (Z^*_{\mathrm{wind}} + Z^*_{\mathrm{wind}})|e|\vec{E} = Z^*|e|\vec{E}, \tag{2.14}$$

where Z^* is referred to as the effective valence (or effective charge number) and represents a parameter that comprises the quantum-mechanical effects of the electromigration phenomenon. It describes the ion-electron interaction which can be both theoretically calculated as well as experimentally measured [40]. The sign of the effective valence determines the nature of the transport mechanism. A negative value indicates atomic transport in the direction of the electron flow, i.e. direction opposite to the current flow. Furthermore, the impact of the contribution of the two aforementioned forces in electromigration can be determined from the variation of the effective valence as a function of temperature [149].

2.3 Electromigration Induced Vacancy Transport

Electromigration is a kinetic process which results in the net transport of metal atoms over macroscopic distances due to the correlation of two competing processes, namely diffusion and migration. Since metal atoms migrate via a vacancy exchange mechanism [20], the atomic flux can be expressed in terms of vacancy species. The vacancy flux is in the opposite direction to the atomic transport. In the following, an expression of the vacancy flux induced by the contributions of vacancy diffusion and electromigration will be provided.

Diffusion is a non-equilibrium process, and it ceases when the system reaches the full thermodynamic equilibrium. The laws of diffusion are mathematical relationships which relate the rate of diffusion to the concentration gradient responsible for the mass transfer [65].

Vacancies flow from regions of high concentration to regions of low concentration. According to the first Fick's law, the flux of vacancies $\vec{J}_\mathrm{V}^\mathrm{D}$, due to diffusion in any part of the system, is proportional to the gradient of the vacancy concentration C_V as follows

$$\vec{J}_\mathrm{V}^\mathrm{D} = -D_\mathrm{V} \nabla C_\mathrm{V}, \tag{2.15}$$

where D_V is the vacancy diffusion coefficient or vacancy diffusivity. Diffusion coefficients are related to temperature by the Arrhenius law

$$D = D_0 \exp\left(-\frac{E_\mathrm{N}}{k_\mathrm{B} T}\right), \tag{2.16}$$

where D_0 is the pre-exponential factor and E_N is the activation energy for diffusion of a given diffusive species N.

The action of the electromigration driving force $\vec{F}_\mathrm{EM}$, presented in Section 2.2, on the vacancies gives rise to an extra velocity component $\vec{v}_\mathrm{d}$ for the affected diffusive species, in the direction of the force. Using the Nerst-Einstein relationship, the drift velocity is given by

$$\vec{v}_\mathrm{d} = M \vec{F}_\mathrm{EM} = \frac{D_\mathrm{V}}{k_\mathrm{B} T} Z^* |e| \vec{E}, \tag{2.17}$$

and the vacancy flux $\vec{J}_\mathrm{V}^\mathrm{EM}$ due to electromigration is calculated as follows

$$\vec{J}_\mathrm{V}^\mathrm{EM} = C_\mathrm{V} \vec{v}_\mathrm{d} = \frac{C_\mathrm{V} D_\mathrm{V}}{k_\mathrm{B} T} Z^* |e| \vec{E}. \tag{2.18}$$

In a stress-assisted diffusion condition, the migration process is superimposed on diffusion. The tendency of vacancies to diffuse is opposite to their tendency to migrate under the influence of the electromigration force.

Therefore, the net vacancy flux $\vec{J}_\mathrm{V}$ in any part of the system due to the competition of Fickian diffusion and electromigration is given by

$$\vec{J}_\mathrm{V} = \vec{J}_\mathrm{V}^\mathrm{D} + \vec{J}_\mathrm{V}^\mathrm{EM} = -D_\mathrm{V} \nabla C_\mathrm{V} + \frac{C_\mathrm{V} D_\mathrm{V}}{k_\mathrm{B} T} Z^* |e| \vec{E}. \tag{2.19}$$

Diffusion and electromigration fluxes cause a redistribution of the vacancies in the metal line. Since vacancy concentration is not a conserved quantity, the balance equation for vacancy conservation is given by Fick's second law as

$$\frac{\partial C_\mathrm{V}}{\partial t} = -\nabla \cdot \vec{J}_\mathrm{V} + G, \tag{2.20}$$

where G is the sink/source term which models the creation and annihilation of vacancies at particular sites inside the metal line [20]. These sites are grain boundaries, extended defects, and interfaces. Vacancies will accumulate or deplete depending on whether the divergence operator has a negative or positive sign, respectively.

The equations (2.19) and (2.20) are the fundamental continuum model equations which describe the vacancy concentration behavior resulting in accumulation or depletion of vacancies due to diffusion and electromigration, together with the contribution of vacancy generation/annihilation, along an interconnect line.

Shatzkes and Lloyd [138] investigated the transport of vacancies to the end of a semi-infinite line and derived the first solution of equation (2.20) with a zero sink/source term. As a consequence of their model, the expression of Black's equation with the current density exponent $n = 2$ was obtained (equation (2.11)). Another interesting analytic solution of equation (2.20), for the case where G is null, was obtained by Clement for a finite line with blocking boundary conditions at both ends of the line [37]. The solutions of the two aforementioned models are calculated by imposing the steady-state condition of vacancy saturation, i.e. the vacancy concentration reaches a certain critical value significantly higher than the initial value. However, the models are inadequate because the time evaluated to reach the steady-state vacancy supersaturation is smaller than that observed experimentally in [129].

Rosenberg and Ohring [129] provided improvements on the previous models by introducing the source/sink term in the continuity equation as follows

$$\frac{\partial C_{\mathrm{V}}}{\partial t} = -\nabla \cdot \vec{J}_{\mathrm{V}} + \frac{C_{\mathrm{V,eq}} - C_{\mathrm{V}}}{\tau_{\mathrm{V}}}, \tag{2.21}$$

where $C_{\mathrm{V,eq}}$ is the equilibrium vacancy concentration, and τ_{V} the vacancy relaxation time. The second term of the right-hand side of equation (2.21) describes the process of vacancy annihilation or generation at the sites acting as sinks or sources of vacancies. In such a way, if the vacancy concentration is smaller than its equilibrium value, vacancies are generated near vacancy sources and reach the steady-state condition in a time regulated by τ_{V}. Typically, the magnitude of τ_{V} is milliseconds and the vacancy supersaturation is reached quickly [20]. Furthermore, the maximum saturation level is low and it cannot be used to determine the void nucleation condition for electromigration failure. Solutions for these shortcomings will be shown in the next sections, with a consideration of the stress build-up mechanism at the sites of vacancy generation/annihilation. Before, a general overview concerning the fast diffusivity paths inside the metal line, along which vacancies are mainly transported, is provided.

2.4 Effect of Diffusion Paths

There are several transport paths along which vacancies may flow in metallic interconnects. These paths are considered as sources or sinks for vacancies in metal lines. Typical paths are dislocations, grain boundaries, and interfaces. In Section 1.4.5, it has been shown that the properties of microstructure, such as grain size distribution, crystal orientation in the grains, and structure of interfaces, have a strong impact on vacancy transport in the line.

The vacancy flow is directly proportional to the vacancy diffusion coefficient, which is related to several possible diffusion mechanisms. The dominant diffusion mechanism is determined by the fastest diffusivity path. Therefore, vacancy transport due to electromigration is a function of the available diffusivity paths which cause vacancy accumulation or depletion in the metallization. One or more vacancy diffusivity paths dominate the electromigration failure while others remain ineffective [149]. The different diffusivity paths depend on several factors:

- path type,
- path width,
- path thickness,
- activation energy,
- effective charge number.

In order to reduce the complexity of a system where different diffusion paths are available and active, the vacancy flux in equation (2.19) through these paths is expressed as follows

$$\vec{J}_{\mathrm{V}} = -\frac{D_{\mathrm{V}}Z^*}{k_{\mathrm{B}}T}\left(\frac{\nabla C_{\mathrm{V}}k_{\mathrm{B}}T}{Z^*} - C_{\mathrm{V}}|e|\vec{E}\right), \tag{2.22}$$

where

$$D_{\mathrm{V}}Z^* = \sum_n D_{\mathrm{V}}^{\mathrm{n}} Z_{\mathrm{n}}^* f_{\mathrm{n}}. \tag{2.23}$$

The effective diffusion coefficient $D_{\mathrm{V}}^{\mathrm{n}}$ and the effective charge number Z_{n}^* are different for each diffusion path n, and are related to the fraction of vacancies f_{n} diffusing through a given pathway. The main diffusion paths n are bulk (b), grain boundaries (gb), material interfaces (i), surfaces (s), and dislocations (d).

2.5 Stress Build-up due to Electromigration

In Section 2.3, it is shown that the vacancy flux induced by the electromigration driving force results in a redistribution of the vacancy concentration in the metal line. Furthermore, vacancies are created or annihilated at those locations which act as vacancy sources or sinks in the line. In the absence of sources and sinks of vacancies, vacancy accumulation should rise at the cathode end of the line (Figure 2.2). In turn, at the anode end of the line, vacancy depletion occurs [40].

When an atom moves to the end of the line under the influence of electromigration, it leaves behind a vacancy at the opposite side [148]. Similar to the thermal expansion-induced stress, volumetric relaxations occur in the lattice site due to differences between the atomic volume and the vacancy volume [20]. Consequently, at the cathode end of the line, vacancy accumulation produces a volume contraction of the line due to the relaxation of the neighboring atoms surrounding the vacancy. At the same time, vacancy depletion creates a volume expansion of the line. In confined metal interconnects deposited on a silicon substrate and covered by different passivation layers (Figure 2.2), the response of the metal to these

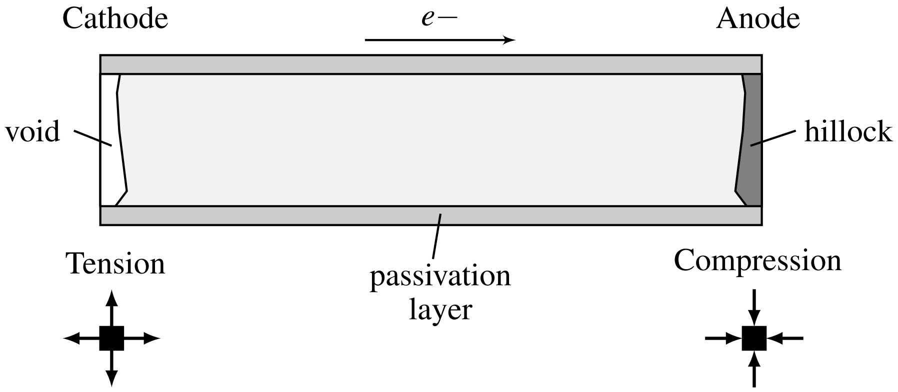


Figure 2.2: Stress build-up due to vacancy accumulation and depletion in a passivated metal line. Tensile stresses lead to void formation.

volumetric changes results in the development of mechanical stresses in the line. Because of the mechanical constraints imposed by the surrounding layers, volume contraction is not accommodated, and the metal line is under tension with a tensile stress at the cathode end. The vacancy accumulation, and the consequent tensile stress development, leads to the formation of a void at the cathode end. At the opposite side, compressive stress arises resulting in the creation of a hillock.

The stress generated due to electromigration influences the driving force for vacancy transport, and its incorporation into the electromigration model should solve the shortcoming regarding the criterion for void nucleation. Different approaches for the analysis of the effect of the stress during electromigration were proposed in literature.

2.5.1 Kirchheim Back Stress

In the work of Blech, presented in Section 2.1.2, it was found that electromigration gives rise to back stresses which may delay device failure. The nature and the origin of the stress were not clear. Kirchheim [91] was the first who incorporated the effect of the transient back stress build-up in a single model. Considering the movement of an atom, with an atomic volume Ω_a, from the grain boundary to the surface, the relaxation of the neighboring atoms within the grain boundary leads to a volume contraction of $f\Omega_a$ around the formed vacancy. The total volume change due to lattice relaxation is $(1-f)\Omega_a$, where f is the relaxation factor which represents the ratio between the vacancy volume and the atomic volume $(0 < f < 1)$. From the local strain field, induced by the volumetric change at the lattice site, a stress gradient is produced. The gradient of the mechanical stress acts as an additional driving force $\vec{J}_V^{\sigma}$ in the total vacancy flux equation, as follows

$$\vec{J}_V = \vec{J}_V^{D} + \vec{J}_V^{EM} + \vec{J}_V^{\sigma} = -D_V \nabla C_V + \frac{C_V D_V}{k_B T} Z^* |e| \vec{E} - \frac{C_V D_V}{k_B T} f \Omega_a \nabla \sigma, \tag{2.24}$$

where σ is the spherical part of the mechanical stress tensor. Considering a vacancy sink/source similar to that presented in equation (2.21), the continuity equation can be rewritten as

$$\frac{\partial C_{\mathrm{V}}}{\partial t} = -\nabla \cdot \left(-D_{\mathrm{V}} \nabla C_{\mathrm{V}} + \frac{C_{\mathrm{V}} D_{\mathrm{V}}}{k_{\mathrm{B}} T} Z^{*} |e| \vec{E} - \frac{C_{\mathrm{V}} D_{\mathrm{V}}}{k_{\mathrm{B}} T} f \Omega_{\mathrm{a}} \nabla \sigma \right) + \frac{C_{\mathrm{V,eq}} - C_{\mathrm{V}}}{\tau_{\mathrm{V}}}, \tag{2.25}$$

where the expression for the equilibrium vacancy concentration in the grain boundary is related to the mechanical stress as follows [7]

$$C_{\mathrm{V,eq}} = C_{\mathrm{V,0}} \exp \left(\frac{(1-f)\Omega_{\mathrm{a}} \sigma}{k_{\mathrm{B}} T} \right), \tag{2.26}$$

and $C_{\mathrm{V,0}}$ is the initial vacancy concentration in the absence of stress.

The rate of the volumetric change $\Delta V/V$, produced by the generation of a vacancy within a grain of diameter d, is related to the rate of vacancies accumulation within the grain boundary of thickness δ by

$$\frac{1}{V} \frac{\partial V}{\partial t} = (1-f)\Omega_{\mathrm{a}} \frac{\delta}{d} \frac{C_{\mathrm{V,eq}} - C_{\mathrm{V}}}{\tau_{\mathrm{V}}}. \tag{2.27}$$

Using Hooke's law [151]

$$\mathrm{d}\sigma = B \frac{\mathrm{d}V}{V}, \tag{2.28}$$

the time evolution of the stress build-up due to the deviation of the vacancy concentration from its equilibrium is given by

$$\frac{\partial \sigma}{\partial t} = B(1-f)\Omega_{\mathrm{a}} \frac{\delta}{d} \frac{C_{\mathrm{V,eq}} - C_{\mathrm{V}}}{\tau_{\mathrm{V}}}, \tag{2.29}$$

where B is the bulk modulus of the metal line.

By coupling the stress development (equation (2.29)) with the vacancy concentration dynamics (equation (2.25)) along the metal line, analytical solutions relating the mechanical stress to the production/annihilation of vacancies in the grain boundary can be derived for a few limiting cases. Furthermore, Kirchheim identified the three phases for vacancy concentration and stress evolution which significantly contribute to the understanding of the electromigration phenomenon in 3D interconnects.

2.5.2 Korhonen's Model

The equations in Kirchheim's work were only capable to describe 1D finite lines blocked at both ends. The values of vacancy concentration and stress build-up due to electromigration were observed to be identical for every section on the line, because of the assumption of spherical stress. Further, the stress evolution equation succesfully incorporates the impact of the sink/source reactions, but neglects the contribution of the vacancy flow inside the line.

Korhonen [93] proposed a slightly different model than Kirchheim. He investigated the action of the stress gradient caused by electromigration in a narrow interconnect line deposited onto an oxidized silicon substrate, and covered by a rigid passivation layer. The formulation of the electromigration driving forces was based on the atomic flux instead of the vacancy flux. The major difference to Kirchheim's work was to consider the change of lattice sites per unit volume as source of deformation instead of the vacancy change. The material transport due to the passage of electric current along the line was assumed to be affected by grain boundary diffusion alone, as

$$D_{\mathrm{a}} = \frac{\delta D_{\mathrm{gb}}}{d}, \tag{2.30}$$

where D_{a} and D_{gb} are the atomic bulk diffusivity and the atomic grain boundary diffusivity, respectively. In this way, the atoms are deposited predominantly at the grain boundaries. The flux of atoms increases due to the differences in the chemical and electrical potentials between diverse locations of the interconnect line. Assuming thermal equilibrium of the vacancies ($\mu_{\mathrm{V}} = 0$), the chemical potential function μ is given by [76]

$$\mu = \mu_{\mathrm{a}} - \mu_{\mathrm{V}} = \mu_0 - \Omega_{\mathrm{a}}\sigma, \tag{2.31}$$

where μ_{a} is the atomic chemical potential, μ_0 is the chemical potential at a stress free state, and σ is the tensile stress acting across the grain boundary. Including the impact of electric potentials due to electromigration, the atomic flux $\vec{J}_{\mathrm{a}}$ is given by

$$\vec{J}_{\mathrm{a}} = -\frac{C_{\mathrm{a}} D_{\mathrm{a}}}{k_{\mathrm{B}} T}\left(\nabla\mu + Z^*|e|\vec{E}\right), \tag{2.32}$$

where C_{a} is the atomic concentration and D_{a} is the atomic diffusion coefficient.

In thermal equilibrium, the chemical potential is constant inside all grain boundaries. This implies that the deposition of atoms at the grain boundary is independent of its orientation. Furthermore, by including the effect of the rigid dielectric layer on the metallization line, the generation/annihilation of atoms in grain boundaries creates changes in the lattice sites concentration C_{L} per unit volume, resulting in the development of a uniform mechanical stress according to Hooke's law as follows

$$\frac{\mathrm{d}C_{\mathrm{L}}}{C_{\mathrm{L}}} = -\frac{\mathrm{d}\sigma}{B}. \tag{2.33}$$

Since the lattice site occupied by an atom or a vacancy is assumed to have the same volume [102], the constitutive equation between stress and lattice site concentration leads to the reformulation of the vacancy continuity equation (equation (2.20)) as follows

$$\frac{\partial C_{\mathrm{V}}}{\partial t} = -\nabla\cdot\vec{J}_{\mathrm{V}} + G = -\nabla\cdot\left(\frac{C_{\mathrm{V}} D_{\mathrm{V}}}{k_{\mathrm{B}} T}\left(\nabla\mu + Z^*|e|\vec{E}\right)\right) - \frac{C_{\mathrm{L}}}{B}\frac{\partial\sigma}{\partial t}. \tag{2.34}$$

Assuming that vacancy concentration is in thermal equilibrium with the stress inside the grain, then

$$C_{\mathrm{V}} = C_{\mathrm{V,eq}} = C_{\mathrm{V,0}} \exp\left(\frac{\Omega_{\mathrm{a}}\sigma}{k_{\mathrm{B}}T}\right). \tag{2.35}$$

Substituting C_{V} (equation (2.35)) and μ (equation (2.31)), equation (2.34) becomes

$$\left(\frac{C_{\mathrm{V}}\Omega_{\mathrm{a}}}{k_{\mathrm{B}}T} + \frac{C_{\mathrm{L}}}{B}\right)\frac{\partial\sigma}{\partial t} = \nabla\cdot\left(\frac{C_{\mathrm{V}}D_{\mathrm{V}}}{k_{\mathrm{B}}T}\left(\Omega_{\mathrm{a}}\nabla\sigma - Z^{*}|e|\vec{E}\right)\right). \tag{2.36}$$

Including the further assumption that just a very small number of vacancies is necessary to restore the vacancy equilibrium and to create stress ($C_{\mathrm{V}}\Omega_{\mathrm{a}}/k_{\mathrm{B}}T \ll C_{\mathrm{L}}/B$), the first term in the brackets on the left hand side of equation (2.36) is negligible. Taking into account that $C_{\mathrm{L}} = C_{\mathrm{a}} = 1/\Omega_{\mathrm{a}}$, the expression of the stress evolution along a metal line induced by electromigration is given by

$$\frac{\partial\sigma}{\partial t} = \nabla\cdot\left(\frac{D_{\mathrm{a}}B}{k_{\mathrm{B}}T}\left(\Omega_{\mathrm{a}}\nabla\sigma - Z^{*}|e|\vec{E}\right)\right), \tag{2.37}$$

where $D_{\mathrm{a}} = D_{\mathrm{V}}C_{\mathrm{V}}/C_{\mathrm{L}}$.

Korhonen provided analytical solutions of equation (2.37) for several cases in order to estimate the stress build-up during electromigration. An interesting result is given with the solution for a semi-infinite line at $x = 0$. Figure 2.3 shows the stress build-up with time according to Korhonen's model. The inclusion of the stress dependence in the sink/source term of the continuity equation leads to a time-scaling change of the stress build-up. The lifetime predicted from Korhonen is calculated in hours, rather than in minutes obtained from the models presented in Section 2.3. The stress exhibits linear growth with time as predicted by Blech [16]. After a certain time, the stress starts to increase with the square root of time. Furthermore, reaching certain stress levels in the interconnect line represents a usual requirement for electromigration void nucleation.

The model well describes the origin of the stress development in a metal line. A closed equation was obtain for the stress distribution during electromigration, and the interconnect failure was associated with the build-up of a threshold stress value. The model does not consider the evolution of the components of the stress tensor which is influenced by external constraints imposed by passivation layers. An extended formulation of the problem which include contributions from different components of the stress tensor is therefore required.

2.5.3 Mechanical Constitutive Equations

Sarychev [132, 133] treated the stress build-up due to electromigration similar to the thermal expansion-induced stress, and extended the previous works within the scope of a standard 3D continuum model. The vacancy flux as well as the creation and annihilation of vacancies lead to local volume changes inside a metal line and induce its deformation. The total strain tensor $\varepsilon_{\mathrm{ik}}$ has an inelastic component $\varepsilon_{\mathrm{ik}}^{\mathrm{V}}$ due to vacancy migration and generation/annihilation

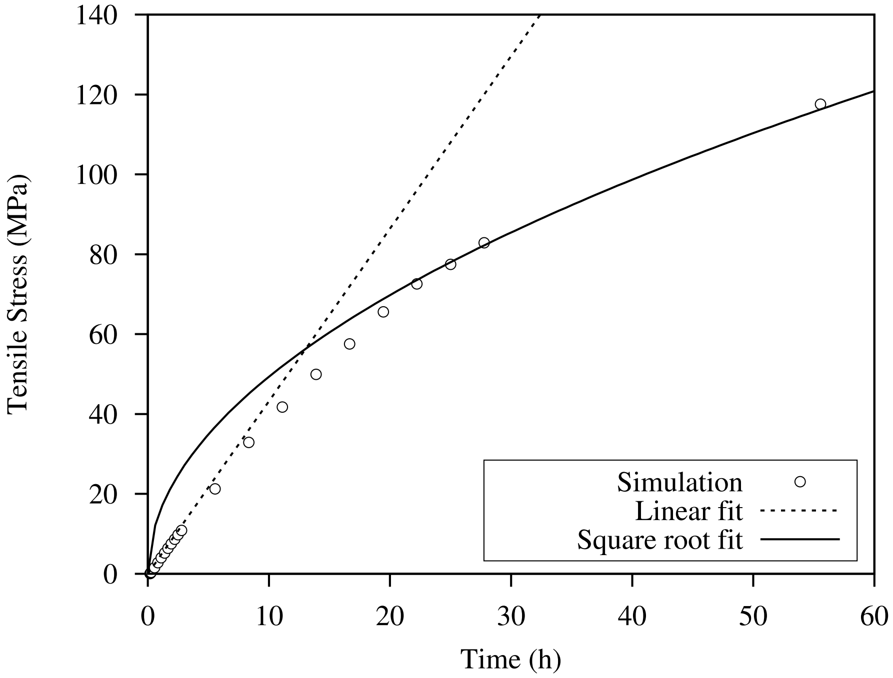


Figure 2.3: The time evolution of the stress build-up in a semi-infinite line at $x = 0$.

processes and a purely elastic component $\varepsilon_{\mathrm{ik}}^{\sigma}$ due to the direct action of mechanical stress

$$\varepsilon_{\mathrm{ik}} = \varepsilon_{\mathrm{ik}}^{\mathrm{V}} + \varepsilon_{\mathrm{ik}}^{\sigma}. \tag{2.38}$$

The rate of the inelastic strain tensor $\varepsilon_{\mathrm{ik}}^{\mathrm{V}}$ includes contributions from both the pile up and the generation/annihilation of vacancies, and is described by the following kinetic equation

$$\frac{\partial \varepsilon_{\mathrm{ik}}^{\mathrm{V}}}{\partial t} = \frac{\Omega_{\mathrm{a}}}{3}\left(f\nabla\cdot\vec{J}_{\mathrm{V}} - (1-f)\frac{C_{\mathrm{V}} - C_{\mathrm{V,eq}}}{\tau_{\mathrm{V}}}\right)\delta_{\mathrm{ik}}, \tag{2.39}$$

where δ_{ik} is the Kronecker delta function. The inelastic strain tensor is diagonal with equal diagonal entries. The equation (2.39) is therefore replaced by a single kinetic equation as follows

$$\frac{\partial \varepsilon_{\mathrm{kk}}^{\mathrm{V}}}{\partial t} = \Omega_{\mathrm{a}}\left(f\nabla\cdot\vec{J}_{\mathrm{V}} - (1-f)\frac{C_{\mathrm{V}} - C_{\mathrm{V,eq}}}{\tau_{\mathrm{V}}}\right). \tag{2.40}$$

The inhomogeneities in the vacancy concentration distribution and the interaction of the metal with the surrounding medium produce volumetric elastic strains in the line. According to Hooke's law [151], metals respond to elastic strains by a build-up of stresses as follows

$$\varepsilon_{\mathrm{ik}}^{\sigma} = S_{\mathrm{iklm}}\sigma_{\mathrm{lm}}, \tag{2.41}$$

where S_{iklm} is the matrix of elastic compliances. The rate of the elastic strain tensor is given by

$$\frac{\partial \varepsilon_{\mathrm{ik}}^{\sigma}}{\partial t} = S_{\mathrm{iklm}} \frac{\partial \sigma_{\mathrm{lm}}}{\partial t}. \tag{2.42}$$

Substituting equations (2.40) and (2.42) into equation (2.38), and performing the inversion of the tensor S_{iklm}, the rate of mechanical stress becomes

$$\frac{\partial \sigma_{\mathrm{ik}}}{\partial t} = C_{\mathrm{iklm}} \left(\frac{\partial \varepsilon_{\mathrm{lm}}}{\partial t} - \Omega_{\mathrm{a}} \left(f \nabla \cdot \vec{J}_{\mathrm{V}} - (1-f) \frac{C_{\mathrm{V}} - C_{\mathrm{V,eq}}}{\tau_{\mathrm{V}}} \right) \right), \tag{2.43}$$

where C_{iklm} is the matrix of elastic stiffness. The substitution of equation (2.41) into equation (2.38) results in the important stress-strain relationship given by

$$\sigma_{\mathrm{ij}} = -B \varepsilon_{\mathrm{kk}}^{\mathrm{V}} \delta_{\mathrm{ij}} + \lambda \varepsilon_{\mathrm{kk}} \delta_{\mathrm{ij}} + 2\mu \varepsilon_{\mathrm{ij}}, \tag{2.44}$$

where λ and μ are the Lamé constants, and $B = (3\lambda + 2\mu)/3$ is the bulk modulus. Since the accelerations are small during electromigration, the mechanical equilibrium equation [98] is obtained by

$$\sum_{j=1}^{3} \frac{\partial \sigma_{\mathrm{ij}}}{\partial x_{\mathrm{j}}} = 0. \tag{2.45}$$

Substituing equation (2.44) into equation (2.45), and using the small displacement approximation

$$\varepsilon_{\mathrm{ik}} = \frac{1}{2} \left(\frac{\partial u_{\mathrm{i}}}{\partial x_{\mathrm{k}}} + \frac{\partial u_{\mathrm{k}}}{\partial x_{\mathrm{i}}} \right), \tag{2.46}$$

the three equations which define the displacement vector $\vec{u} = (u_1, u_2, u_3)$ are obtained as follows

$$B \frac{\partial \varepsilon_{\mathrm{kk}}^{\mathrm{V}}}{\partial x_{\mathrm{i}}} = \mu \nabla^2 u_{\mathrm{i}} + (\mu + \lambda) \frac{\partial}{\partial x_{\mathrm{i}}} (\nabla \cdot \vec{u}). \tag{2.47}$$

In this way, a set of 3D self-consistent equations (2.25), (2.40), (2.47), and (2.44) for the evolution of mechanical stress inside the passivated metal line during electromigration is obtained.

The main innovation of the model was to connect the evolution of all the components of the stress tensor with the vacancy transport, by including the impact of the geometry of the metallization and imposed displacement boundary conditions. Furthermore, Sarychev's model is the first general 3D model for describing the electromigration stress build-up, which can be applied for an arbitrary 3D geometry.

Similarly to Sarychev's work, Sukharev [144–147] independently developed a model for describing the electromigration stress build-up where different diffusion paths for bulk, interfaces, and grain boundaries were considered. Sukharev distinguished between different vacancy concentrations for bulk $C_{\mathrm{V}}^{\mathrm{b}}$ and the others fast diffusivity paths $C_{\mathrm{V}}^{\mathrm{n}}$. Plated atoms were introduced to describe the atomic exchange between bulk and fast diffusivity paths. In this way, the vacancy generation/annihilation is represented by atom plating/removal from those locations where the activation energy for diffusion is lower. The rate of the plated atom exchange has the standard form of the G term presented in Section 2.3

$$G_{\mathrm{n}} = -\frac{C_{\mathrm{V}}^{\mathrm{n}} - C_{\mathrm{V,eq}}}{\tau_{\mathrm{V}}}. \tag{2.48}$$

Considering immobile plated atoms with a concentration C_{pl}, the plated atom continuity equations for bulk and diffusivity paths are given by

$$\frac{\partial C_{\mathrm{pl}}^{\mathrm{b}}}{\partial t} = 0 \tag{2.49}$$

and

$$\frac{\partial C_{\mathrm{pl}}^{\mathrm{n}}}{\partial t} = \frac{C_{\mathrm{V}}^{\mathrm{n}} - C_{\mathrm{V,eq}}}{\tau_{\mathrm{V}}}, \tag{2.50}$$

respectively. Following this approach, Sukharev obtained an equation which combines the electromigration-induced strain tensor with the vacancy concentration and the plated atom concentration as follows

$$\varepsilon_{\mathrm{ik}}^{\mathrm{V}} = \Omega_{\mathrm{a}}((f-1)(C_{\mathrm{V}}^{\mathrm{n}} - C_{\mathrm{V,0}}^{\mathrm{n}}) + (C_{\mathrm{pl}} - C_{\mathrm{pl,0}})\delta_{\mathrm{ik}}, \tag{2.51}$$

where $C_{\mathrm{V,0}}^{\mathrm{n}}$ and $C_{\mathrm{pl,0}}$ are the vacancy concentration and the atom concentration in the plated layer at zero stress, respectively. He concluded that the evolution of the plated atom concentration is mainly responsible for the electromigration stress build-up.

The models independently developed by Sarychev and Sukharev allow for the study of the stress build-up due to electromigration in complex 3D interconnect structures. Further aspects concerning the coupling to the electro-thermal problem and extensions with the fast diffusivity paths approach will be presented in Chapter 3.

2.6 Void Initiation Condition

It has been shown in Section 2.3 that the condition for void nucleation was attributed to reaching a certain critical vacancy supersaturation concentration during the process of vacancy accumulation at sites of flux divergence, leading to vacancy condensation [37, 129, 138]. The void nucleation criterion requires an unrealistically high concentration of vacancies to reach the maximum saturation level for condensation and consequent spontaneous formation of a void [129]. Therefore, the condition of electromigration void nucleation based on the vacancy condensation mechanism was inappropriate since it cannot be justified from a thermodynamic point of view.

Several authors have recognized the importance of the electromigration stress build-up in an interconnect as the major cause for void nucleation [77, 81, 91, 93, 124]. The formation of a void occurs after a tensile stress threshold is reached. Different approaches for stress-driven void nucleation by vacancy condensation were discussed in literature [66, 74]. All of those works were derived from the nucleation theory based on classical thermodynamics [50]. By employing this theory, Gleixner [63, 64] analyzed the nucleation rates at various locations within passivated aluminum interconnects. For this case, the free energy change ΔF upon the creation of an embryo in the aluminum line is given by

$$\Delta F = \Delta F_v V_\mathrm{e} + \gamma_{Al} A_{Al} + (\gamma_{Al_2O_3} - \gamma_{Al-Al_2O_3}) A_i - \gamma_{gb} A_{gb}, \tag{2.52}$$

where ΔF_v is the Helmholtz free energy change per unit volume of the embryo, V_e is the volume of the embryo, γ_{Al}, $\gamma_{Al_2O_3}$, $\gamma_{Al-Al_2O_3}$, and γ_{gb} refer to the interfacial free energies of the metal, passivation layer, metal/passivation interface, and grain boundary, respectively, and A_{Al}, A_i, and A_{gb} are the areas of interfaces created/destroyed upon embryo formation. In the case of vacancy coalescence in a stressed material, ΔF_v is related to the hydrostatic stress in the line by

$$\Delta F_v = -\sigma. \tag{2.53}$$

This expression represents the energy released by the dissipation of the elastic strain energy in the metal. For positive σ, the free energy in equation (2.52) increases until a critical embryo volume value is reached. The maximum value referred to as the critical embryo is determined by the energy barrier for void nucleation ΔF^*, which is given by the condition

$$\Delta F^* = \Delta F|_{\partial(\Delta F)=0}. \tag{2.54}$$

Once the energy barrier and the site geometry are known, the void nucleation rate per unit volume at various sites within an interconnect can be calculated.

Small rates for nucleation are observed at metal/passivation interfaces, at grain boundaries, and at triple points, i.e. intersections between grain boundaries and metal/passivation layer interfaces. This means that void nucleation by vacancy condensation at these locations is not possible.

The last case is particularly interesting, since voids are typically observed to nucleate at the triple points [35]. An analysis carried out by Flinn [59] was useful to solve this apparent discrepancy by introducing a new concept for the understanding of void nucleation. The author suggested the idea that a flaw could form on the interface between the metal and the passivation layer with no adhesion. The so-called pre-existing adhesion-free patch can be the result of contamination or surface defect during the interconnect fabrication, which leads to weak adhesion between the metal and surrounding layer. By considering a circular patch of radius R_P, Flinn [59] derived an expression for the threshold stress σ_thr for void nucleation as follows

$$\sigma_\mathrm{thr} = \frac{2\gamma_{Al}}{R_\mathrm{P}}. \tag{2.55}$$

The formula is valid as long as the void grows in the region of weak adhesion. An extended version of the model proposed by Clemens [36] considered the void growth beyond the free surface of the contaminate region once the equilibrium contact angle θ_C is reached (Figure 2.4). θ_C is in the range between 0 and 90° leading to a decreased threshold stress value given by

$$\sigma_\mathrm{thr} = \frac{2\gamma_{Al}\sin\theta_\mathrm{C}}{R_\mathrm{P}}. \tag{2.56}$$

If the stress is above the threshold value, the energy barrier between the embryo and a stable-growing void vanishes, leading to the formation of a void at different sites within an interconnect.

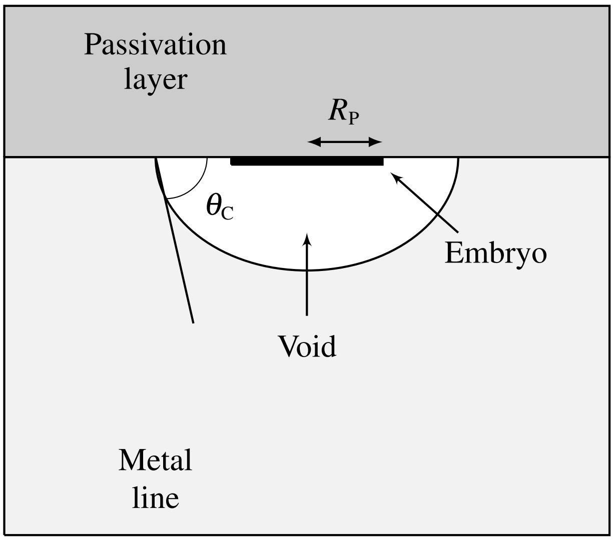


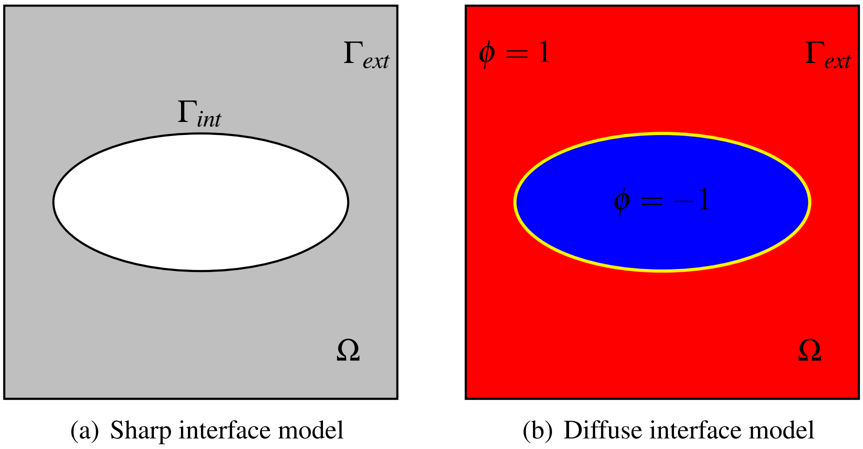
Figure 2.4: Schematic of the embryo at the line/passivation interface.

2.7 Void Evolution

Once the fatal void has nucleated, the void evolution mechanism is the ultimate cause for electromigration induced interconnect wear-out failure which results in open circuit failure. The electromigration void evolution mechanism is typically related to the development of the interconnect resistance as a function of time. As soon as the void grows, a rapid non-linear interconnect resistance increase begins. The interconnect fails after a maximum tolerable resistance level is reached.

The void evolution mechanism leads to the line failure as the result of a competition between growth, shape change, and motion of the void [3]. Given the different influences on the void evolution, modeling interconnect failures poses a challenging task. Two different modeling methodologies for electromigration void evolution have been developed in the 1990s.

The first approach is the sharp interface method which attempts to model the void surface Γ_{int} as a sharp discontinuity between the metal and the empty space in the void, as shown in Figure 2.5(a) [62, 71, 96, 135, 156]. It requires a direct tracking of the void surface during its evolution with a continuously re-adapted mesh as the structure changes its shape [62]. Applications of this method provided numerical simulations of the void shape change and well explained some experimental observations. Due to the complexity of the surface tracking as the void is subjected simultaneously to motion, shape change and growth, the sharp interface model tends to have poor numerical stability and hence is cumbersome.



(a) Sharp interface model (b) Diffuse interface model

Figure 2.5: Sharp (a) and diffuse (b) description of the void interface.

The diffuse interface method (or phase field method) offers an attractive alternative to the sharp interface model for solving the electromigration void surface evolution problems. The idea of a sharp interface between the conductor material and the empty void is abandoned. The entire domain Ω is described by a continuous variation of an order parameter ϕ (or phase field variable) from $+1$ in the metal "phase" to -1 in the void "phase" over a narrow metal-void interfacial layer associated with the void surface, as shown in Figure 2.5(b) [107]. The value of the order parameter defines the material and the void at any point on a fixed grid and therefore the diffuse interface model does not require exact tracking of the surface elements and their geometry. In general, the diffuse interface model is an approximation to the sharp interface model. Furthermore, in the limit of vanishing interface thickness, the two models will show matching physical behavior. Diffuse interface models for the electromigration void evolution analysis successfully predicted void motion and growth in Al and Cu interconnects [10, 11, 107, 108].

For the last 20 years, new methodologies [42, 43, 45, 60, 61, 152], based on semi-empirical modeling, were employed for the simulation of void evolution and resistance increase in interconnects. Semi-empirical methods are analytical expressions which are partially derived from purely theoretical assumptions and partially obtained from empirical evidence as a result of experimental observations or by fitting to the experimental results. For those reasons, void evolution semi-empirical based methods are capable to numerically calculate the growth of the void and the consequent resistance increase efficiently.

In the next chapter, the different approaches for modeling the void surface evolution as well as a simple semi-empirical model for void growth will be presented in details.

Chapter 3

Modeling Electromigration Using TCAD

In the previous chapter a description of the various physical phenomena related to the electromigration failure mechanism were described. The different physical models proposed allow to obtain analytical solutions and may only be applied to investigate simple structures. Since the scope of this thesis is to analyze complex interconnect geometries, the derivation of analytical solutions does not provide appropriate results. For this purpose, the development of an electromigration model, adapted for the implementation in a technology computer aided design (TCAD) tool, is necessary in order to simulate complicated interconnect structures. Since different physical effects are responsible for electromigration failure, modeling electromigration constitutes a multiphysics analysis which can be divided into different blocks. Initially a description of the electro-thermal problem allows to determine the distributions of electric potential, current density, and temperature inside the structure. Then, the vacancy balance equation is solved, which takes into account all the various driving forces for vacancy transport and the effects of the different fast diffusivity paths. This is followed by the determination of the distribution of the electromigration-induced stress build-up in the structure obtained from solid mechanics modeling. Reaching of a threshold stress implies void nucleation and the beginning of the second phase of failure. The different methodologies adopted for modeling the void evolution mechanism are fully described in this chapter. Finally, an overview of the model blocks, which must be solved numerically with the TCAD tool, is briefly presented.

3.1 Electro-Thermal Problem

As discussed in Section 2.2, the electromigration driving force acting on the metal atoms is caused by the contribution of two microscopic forces, namely "direct force" and "electron wind". The "direct force" refers to the direct action of the local electric field $\vec{E}$ on the migrating ions in the conducting metal line. The action of the local electric field on the metal atoms is related to the electric current density $\vec{j}$ by Ohm's law [70] with

$$\vec{j} = \sigma_{\mathrm{E}}\vec{E}, \tag{3.1}$$

where σ_E is the electrical conductivity of the metal. Since the electric field has zero curl and is a conservative vector field, it can be expressed as a function of the electric potential V_E such that

$$\vec{E} = -\nabla V_\mathrm{E}. \tag{3.2}$$

The principle of charge conservation states that electric charge can neither be created nor destroyed at every point in the line. Considering a region with no charges, the charge continuity equation, which is related to the distribution of current density in the line at any time [70], reduces to

$$\nabla \cdot \vec{j} = 0. \tag{3.3}$$

By applying the divergence theorem, together with equations (3.1) and (3.2), the distribution of the electric potential in the metal line is given by

$$\nabla \cdot (\sigma_\mathrm{E} \nabla V_\mathrm{E}) = 0. \tag{3.4}$$

Under the assumption of constant electrical conductivity along the line, equation (3.4) reduces to Laplace's equation for electric potential

$$\nabla^2 V_\mathrm{E} = 0. \tag{3.5}$$

The electric potential distribution in the metal interconnect line is subjected to the insulating surface boundary condition. If the space surrounding the metal line is taken to be non-conducting, charge would not be leaking out into it and the current density on the surface, with normal vector $\hat{n}$, should vanish by obeying the following boundary condition [70]

$$\vec{j} \cdot \hat{n} = 0. \tag{3.6}$$

Hence, by applying equation (3.5), equation (3.6) implies that the normal derivative of the electric potential vanishes on the surface as follows

$$\frac{\partial V_\mathrm{E}}{\partial n} = 0. \tag{3.7}$$

A potential which satisfies Laplace's equation and has a specific normal derivative on all boundaries is a uniquely defined electrostatic potential [70].

The temperature distribution within the metal line is determined by the solution of the heat equation. The heat equation is derived from the conservation law of heat energy for materials and Fourier's law [23]. The heat equation is a differential statement of thermal energy balance. The thermal energy of a metal line can change only if heat is conducted in/out through its surface boundary or heat is generated or adsorbed within the line [120]. The net outflow of thermal energy through the bounding surfaces of the line should therefore be balanced by its internally-generated heat and its ability to store some of this heat. This is stated by the law of conservation of heat energy for the metal line as follows

$$\nabla \cdot \vec{q} = q_\mathrm{gen} - \frac{\partial Q}{\partial t}, \tag{3.8}$$

where $\vec{q}$ is the heat flux, q_{gen} is the rate of heat generation within the line, and Q is the thermal energy stored within the metal per unit volume. The change in thermal energy in time is related to the capacity of the line to store heat by raising its temperature T as follows

$$\frac{\partial Q}{\partial t} = \rho_{\text{m}} c_{\text{P}} \frac{\partial T}{\partial t}, \tag{3.9}$$

where ρ_{m} is the metal mass density, and c_{P} is the metal specific heat capacity. The net heat conducted out of the line implies a temperature gradient. When there exists a temperature gradient within the line, heat energy flows from regions of high temperature to regions of low temperature. Therefore, the rate of flow of heat energy through the line is related to the temperature gradient across it by Fourier's law

$$\vec{q} = -k_{\text{T}} \nabla T, \tag{3.10}$$

where k_{T} is the metal thermal conductivity. By substituting equations (3.9) and (3.10) in equation (3.8), the heat equation is rewritten as

$$\nabla^2 T - \frac{\rho_{\text{m}} c_{\text{P}}}{k_{\text{T}}} \frac{\partial T}{\partial t} = -\frac{q_{\text{gen}}}{k_{\text{T}}}. \tag{3.11}$$

The temperature T at a given location in the line changes over time as heat spreads throughout the metal. The heat generated in the interconnect is related to Joule heating, which is described as the heat released in the conductor when an electric current passes through it and is given by

$$q_{\text{gen}} = \vec{j} \cdot \vec{E} = \sigma_{\text{E}} \vec{E} \cdot \vec{E} = \sigma_{\text{E}} ||\vec{E}||^2 = \sigma_{\text{E}} (\nabla V_{\text{E}})^2. \tag{3.12}$$

Joule heating is included in the heat equation (3.11), and couples the electrical problem with the thermal problem as follows

$$\nabla^2 T - \frac{\rho_{\text{m}} c_{\text{P}}}{k_{\text{T}}} \frac{\partial T}{\partial t} = -\frac{\sigma_{\text{E}}}{k_{\text{T}}} (\nabla V_{\text{E}})^2. \tag{3.13}$$

The temperature distribution in the line is determined by setting thermal boundary conditions to the metal line and taking into account the Joule heating effect. A Dirichlet boundary condition for the temperature specifies the values along the boundaries of the domain. The effect of Joule heating in the thermal problem is properly considered by including portions of the dielectric material surrounding the metal line. Both the electrical and thermal conductivities are assumed to be temperature dependent parameters in the forms

$$\sigma_{\text{E}}(T) = \frac{\sigma_{\text{E},0}}{1 + \alpha_{\text{E}}(T - T_0) + \beta_{\text{E}}(T - T_0)^2} \tag{3.14}$$

and

$$k_{\text{T}}(T) = \frac{k_{\text{T},0}}{1 + \alpha_{\text{T}}(T - T_0) + \beta_{\text{T}}(T - T_0)^2}, \tag{3.15}$$

where $\sigma_{\mathrm{E},0}$ and $k_{\mathrm{T},0}$ are the conductivities at the reference temperature T_0, α_{E} and α_{T} are the linear temperature coefficients, and β_{E} and β_{T} are the quadratic temperature coefficients [40].

By solving the non-linear system of equations (3.3), (3.5), and (3.13) which describe the electro-thermal model, it is possible to obtain the current density, the electric potential, and the temperature distributions in the interconnect line.

3.2 Vacancy Dynamics Problem

Since atomic diffusion in copper metallization is a result of the vacancy exchange mechanism [20], the mass transport which occurs in the interconnect during electromigration can be modeled in terms of vacancy transport. The vacancy flux is caused by the contributions of vacancy diffusion and vacancy migration due to the action of different driving forces.

The electromigration driving force, presented in Section 2.2, is not sufficient to quantitatively describe the vacancy migration which opposes to the Fickian diffusional vacancy flux. Other contributions can be obtained from the general expression of the electrochemical potential $\bar{\mu}$ of a vacancy in the bulk [20], which is a thermodynamic measure of the chemical potential μ taking into account the contribution of electrostatic energy, as follows

$$\bar{\mu} = \bar{\mu}_0 + \bar{\mu}_{\mathrm{E}} + \bar{\mu}_{\mathrm{T}} + \bar{\mu}_{\sigma}, \tag{3.16}$$

where $\bar{\mu}_0$, $\bar{\mu}_{\mathrm{E}}$, $\bar{\mu}_{\mathrm{T}}$, and $\bar{\mu}_{\sigma}$ are the electrochemical potentials related to the reference state, electromigration, thermomigration, and stress-migration, respectively. Any electrochemical potential relates to the respective driving force $\vec{F}_{\mathrm{m}}$ for vacancy migration [20] as follows

$$\vec{F}_{\mathrm{m}} = -\nabla\bar{\mu} \tag{3.17}$$

and, by using the Nerst-Einstein relationship, to the vacancy flux along the line due to the different migration processes $\vec{J}_{\mathrm{V}}^{\mathrm{m}}$ as

$$\vec{J}_{\mathrm{V}}^{\mathrm{m}} = \frac{D_{\mathrm{V}} C_{\mathrm{V}}}{k_{\mathrm{B}} T} \vec{F}_{\mathrm{m}}, \tag{3.18}$$

where D_{V} is the diffusion coefficient, C_{V} is the vacancy concentration, and k_{B} is the Boltzmann constant. Adding the Fickian term $\vec{J}_{\mathrm{V}}^{\mathrm{D}}$, the total vacancy flux $\vec{J}_{\mathrm{V}}$ is obtained by

$$\vec{J}_{\mathrm{V}} = \vec{J}_{\mathrm{V}}^{\mathrm{D}} + \vec{J}_{\mathrm{V}}^{\mathrm{m}} = \vec{J}_{\mathrm{V}}^{\mathrm{D}} + \vec{J}_{\mathrm{V}}^{\mathrm{EM}} + \vec{J}_{\mathrm{V}}^{\mathrm{T}} + \vec{J}_{\mathrm{V}}^{\sigma}. \tag{3.19}$$

The first flux term represents the typical flux of vacancies due to diffusion, and is expressed by the first Fick's law as follows

$$\vec{J}_{\mathrm{V}}^{\mathrm{D}} = -D_{\mathrm{V}} \nabla C_{\mathrm{V}}. \tag{3.20}$$

The second flux contribution is the flux induced by the electromigration driving force $\vec{F}_{\mathrm{EM}}$ in the form

$$\vec{J}_{\mathrm{V}}^{\mathrm{EM}} = \frac{D_{\mathrm{V}}C_{\mathrm{V}}}{k_{\mathrm{B}}T}\vec{F}_{\mathrm{EM}} = -\frac{D_{\mathrm{V}}C_{\mathrm{V}}}{k_{\mathrm{B}}T}|Z^*|e\nabla V_{\mathrm{E}}, \tag{3.21}$$

where Z^* is the effective valence and e is the elementary charge. The third and the fourth flux terms are related to the driving forces of thermomigration $\vec{F}_{\mathrm{T}}$ [32] and stress-migration $\vec{F}_{\sigma}$ [112], respectively, as follows

$$\vec{J}_{\mathrm{V}}^{\mathrm{T}} = \frac{D_{\mathrm{V}}C_{\mathrm{V}}}{k_{\mathrm{B}}T}\vec{F}_{\mathrm{T}} = -\frac{D_{\mathrm{V}}C_{\mathrm{V}}}{k_{\mathrm{B}}T}\frac{Q^*\nabla T}{T} \tag{3.22}$$

and

$$\vec{J}_{\mathrm{V}}^{\sigma} = \frac{D_{\mathrm{V}}C_{\mathrm{V}}}{k_{\mathrm{B}}T}\vec{F}_{\sigma} = -\frac{D_{\mathrm{V}}C_{\mathrm{V}}}{k_{\mathrm{B}}T}f\Omega_{\mathrm{a}}\nabla\sigma, \tag{3.23}$$

where Q^* is the heat transport, f is the vacancy relaxation factor, Ω_{a} is the volume of an atom, and σ is the hydrostatic mechanical stress. The heat transport Q^* is described as the isothermal heat generated during the movement of the atom in the process of jumping a lattice site [20]. Assuming that a vacancy is compared to a substitutional atom with smaller volume in the crystal lattice, the vacancy relaxation factor represents the relationship between the volume of a vacancy and the atomic volume. Typical values of f are in the range between 0 and 1. The total vacancy flux due to the combination of the different driving forces is given by

$$\vec{J}_{\mathrm{V}} = -D_{\mathrm{V}}\left(\nabla C_{\mathrm{V}} + \frac{C_{\mathrm{V}}|Z^*|e}{k_{\mathrm{B}}T}\nabla V_{\mathrm{E}} + \frac{C_{\mathrm{V}}Q^*}{k_{\mathrm{B}}T^2}\nabla T + \frac{C_{\mathrm{V}}f\Omega_{\mathrm{a}}}{k_{\mathrm{B}}T}\nabla\sigma\right). \tag{3.24}$$

The vacancy diffusion coefficient D_{V} in equation (3.24) depends on the temperature and the hydrostatic stress build-up through the exponential dependence given by the Arrhenius law [40]

$$D_{\mathrm{V}} = D_{\mathrm{V},0}\exp\left(\frac{(1-f)\Omega_{\mathrm{a}}\sigma - E_{\mathrm{a}}}{k_{\mathrm{B}}T}\right), \tag{3.25}$$

where $D_{\mathrm{V},0}$ is the pre-exponential factor, and E_{a} is the activation energy for the diffusion of a vacancy.

The driving forces cause a redistribution of the vacancy concentration in the interconnect line. The vacancy concentration distribution obeys the material balance equation as follows

$$\frac{\partial C_{\mathrm{V}}}{\partial t} = -\nabla\cdot\vec{J}_{\mathrm{V}} + G. \tag{3.26}$$

The local vacancy concentration changes due to the contribution of two mechanisms. The first term on the right hand side of equation (3.26) represents the vacancy accumulation/depletion due to the existence of flux divergence during vacancy transport. The second term, G, is the source/sink term (also known as the Rosenberg-Ohring term [129]) which models the vacancy generation/annihilation processes due to the change of lattice sites at particular locations in the interconnect. This term describes the production/annihilation of vacancies, when their concentration is larger/lower than the equilibrium value $C_{\mathrm{V,eq}}$, respectively, and is given by

$$G = \frac{C_{\mathrm{V,eq}} - C_{\mathrm{V}}}{\tau_{\mathrm{V}}}, \tag{3.27}$$

where τ_{V} is the characteristic generation/annihilation time. The equilibrium concentration of vacancies $C_{\mathrm{V,eq}}$ is given by the Arrhenius law

$$C_{\mathrm{V,eq}} = C_{\mathrm{V,0}} \exp\left(\frac{(1-f)\Omega_{\mathrm{a}}\sigma - E_{\mathrm{a}}}{k_{\mathrm{B}}T}\right), \tag{3.28}$$

where $C_{\mathrm{V,0}}$ is the equilibrium vacancy concentration in the absence of stress.

By assuming that the redistribution of vacancies, caused by vacancy accumulation/depletion as well as generation/annihilation of vacancies, takes place only along the x-direction of the interconnect metal line of length l, equation (3.26) reduces to

$$\frac{\partial C_{\mathrm{V}}(x,t)}{\partial t} = \frac{\partial J_{\mathrm{V}}^{x}(x,t)}{\partial x} + \frac{C_{\mathrm{V,eq}}(x,t) - C_{\mathrm{V}}(x,t)}{\tau_{\mathrm{V}}}. \tag{3.29}$$

The initial and boundary conditions for equation (3.29) for different cases can be summarized as follows [149]:

- Initial condition:

  $C_{\mathrm{V}}(x, t=0) = C_{\mathrm{V,0}}$,

- Boundary conditions:

  1. $J_{\mathrm{V}}^{x}(0,t) = 0$,
  2. $C_{\mathrm{V}}(-\infty,t) = C_{\mathrm{V,0}}$,
  3. $J_{\mathrm{V}}^{x}(-l,t) = 0$,
  4. $C_{\mathrm{V}}(-l,t) = C_{\mathrm{V,0}}$.

The initial condition and the boundary condition 1. are common to all cases. Analytical solutions to equation (3.29) with boundary condition 2. represent the case of vacancy flow in the region of a purely blocking boundary at $x = 0$. The semi-infinite solution was reported by Shatzkes and Lloyd [138]. Solutions with boundary conditions 3. and 4. are for the case of a finite interconnect length [37]. Solutions of all three cases are shown in Figure 3.1.

3.2.1 Vacancy Sources and Sinks

The vacancy source/sink term given in equation (3.27) models vacancy generation/annihilation processes, which occur only inside the fast diffusivity paths in the interconnect. Typical diffusion paths, which act as sources and sinks for vacancies in metals, are grain boundaries, interfaces, and dislocations [7]. The properties of microstructure and diffusion paths have

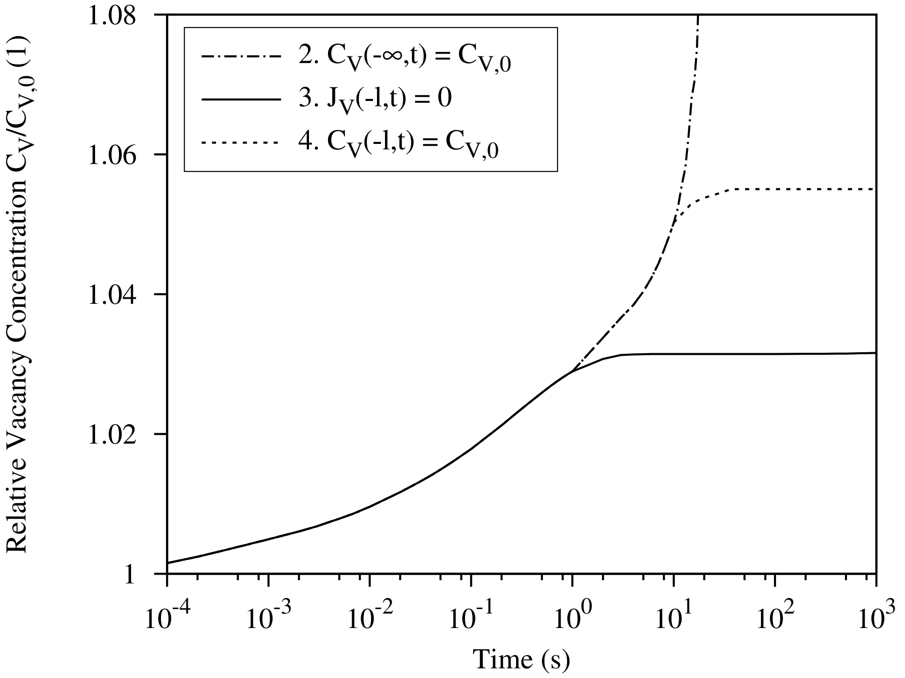


Figure 3.1: The time evolution of the stress build-up in a semi-infinite line at $x = 0$.

a strong impact on vacancy transport in the interconnect line. Vacancy dynamics at these locations are composed of three different mechanisms:

- Vacancy diffusion along the fastest diffusivity path,
- Exchange of vacancies between the source/sink site and the bulk material,
- Vacancy generation/annihilation inside the site.

As discussed in Section 2.4, each diffusion path has a different effective vacancy diffusion coefficient $D_{\mathrm{V}}^{\mathrm{n}}$ and an effective charge number Z_{n}^{*}. It is therefore possible to describe the distribution of vacancy concentration $C_{\mathrm{V}}^{\mathrm{n}}$ independently for each region of the interconnect line in the following way

$$\frac{\partial C_{\mathrm{V}}^{\mathrm{n}}}{\partial t} = \nabla\cdot\left[D_{\mathrm{V}}^{\mathrm{n}}\left(\nabla C_{\mathrm{V}}^{\mathrm{n}} + \frac{C_{\mathrm{V}}^{\mathrm{n}}|Z_{\mathrm{n}}^{*}|e}{k_{\mathrm{B}}T}\nabla V_{\mathrm{E}} + \frac{C_{\mathrm{V}}^{\mathrm{n}}Q^{*}}{k_{\mathrm{B}}T^{2}}\nabla T + \frac{C_{\mathrm{V}}^{\mathrm{n}}f\Omega_{\mathrm{a}}}{k_{\mathrm{B}}T}\nabla\sigma\right)\right] + G_{\mathrm{n}}, \qquad (3.30)$$

where n represents the available diffusion path in the interconnect. In copper-based interconnects, typical diffusion paths are bulk (b), grain boundaries (gb), and material interfaces (i). The diffusion of vacancies along the various available paths must be taken into account in order to understand the impact of each region on the distribution of vacancies in the interconnect line. The fastest diffusivity path will dominate the development of electromigration failure in the interconnect.

For this purpose, a detailed model is presented in the following section which describes the effect of two diffusivity paths, grain boundary and interface. These paths affect the vacancy dynamics and the consequent build-up of mechanical stress inside the interconnect line.

Grain Boundary Model

The network of grain boundaries influences the electromigration-induced transport of vacancies during electrical operation [41]. The vacancy diffusion inside the grain boundary is faster than the bulk diffusion, because the barrier energies for the formation and migration of vacancies inside grain boundaries are lower than those for the bulk material. This is due to the larger diversity of vacancy exchange mechanisms into the grain boundary [143]. The combination of the works of Herring [76], Fisher [58], and Ceric [25] enables to understand the vacancy dynamics in the presence of grain boundaries. The grain boundary model is developed by considering diffusion in a semi-infinite bulk line containing a single grain boundary of width δ normal to the surface, as illustrated in Figure 3.2.

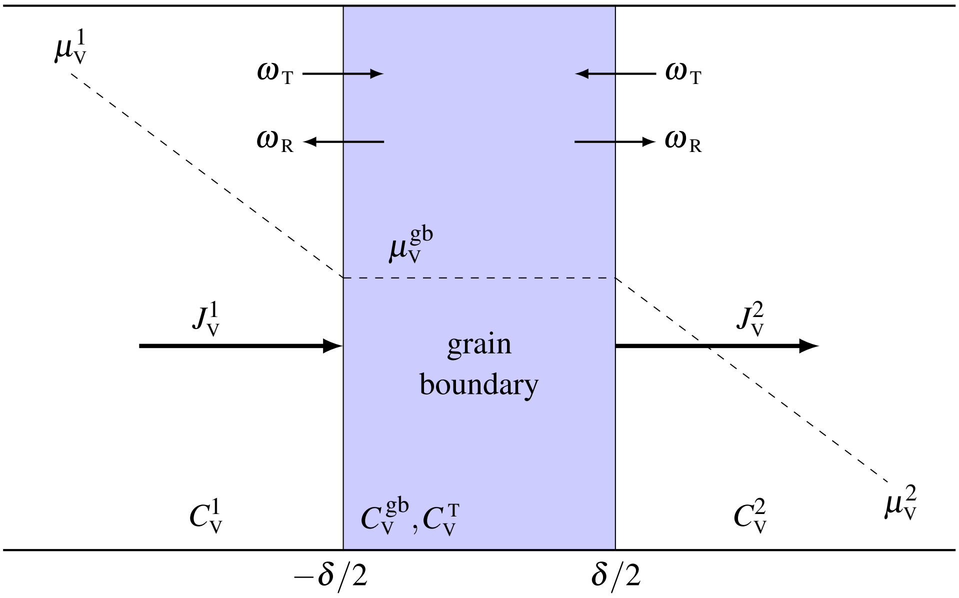


Figure 3.2: Grain boundary of width δ embedded in a bulk. The fluxes J_V^1 and J_V^2 change the concentration of the mobile vacancies (C_V^1 and C_V^2) and immobile vacancies (C_V^T). Vacancies are trapped into the grain boundary with trapping rate ω_T and released to the grains with release rate ω_R.

Herring [76] obtained a relationship for the chemical potential of a vacancy on the grain boundary μ_V^{gb} by investigating the equilibrium during the process of material exchange between the grain boundary and grain bulk. In the case that vacancy concentration varies along the grain boundary, the relationship can be expressed as follows

$$\mu_{\mathrm{V}}^{\mathrm{gb}} = \mu_0 + \Omega_{\mathrm{a}}\sigma_{\mathrm{nn}} + k_{\mathrm{B}}T\ln\left(\frac{C_{\mathrm{V}}^{\mathrm{gb}}}{C_{\mathrm{V},0}}\right), \tag{3.31}$$

where μ_0 is the reference chemical potential, $\sigma_{\mathrm{nn}} = \hat{n}\cdot\overline{\overline{\sigma}}\cdot\hat{n}$, $\hat{n}$ is the normal to the grain surface, $\overline{\overline{\sigma}}$ is the stress tensor, and $C_{\mathrm{V}}^{\mathrm{gb}}$ is the vacancy concentration in the grain boundary. The expression for the chemical potential of a vacancy in the bulk μ_{V} [100] is given by

$$\mu_{\mathrm{V}} = \mu_0 + \frac{1}{3}f\Omega_{\mathrm{a}}\mathrm{Tr}(\overline{\overline{\sigma}}) + k_{\mathrm{B}}T\ln\left(\frac{C_{\mathrm{V}}}{C_{\mathrm{V},0}}\right), \tag{3.32}$$

where $\mathrm{Tr}(\overline{\overline{\sigma}})$ is the trace of the stress tensor. When $\mu_{\mathrm{V}}^{\mathrm{gb}} = \mu_{\mathrm{V}}$, the local equilibrium between surface stress and vacancy concentration [7] permits to obtain the equilibrium concentration of vacancies inside the grain boundary $C_{\mathrm{V,eq}}^{\mathrm{gb}}$ as follows

$$C_{\mathrm{V,eq}}^{\mathrm{gb}} = C_{\mathrm{V},0}\ \exp\left(-\frac{\Omega_{\mathrm{a}}\sigma_{\mathrm{nn}}}{k_{\mathrm{B}}T}\right). \tag{3.33}$$

By following equation (3.18), the general expression for the vacancy flux along the grain boundary $J_{\mathrm{V}}^{\mathrm{gb}}$ is given by

$$J_{\mathrm{V}}^{\mathrm{gb}} = \frac{D_{\mathrm{V}}^{\mathrm{gb}}C_{\mathrm{V}}^{\mathrm{gb}}}{k_{\mathrm{B}}T}\frac{\partial\mu_{\mathrm{V}}^{\mathrm{gb}}}{\partial x}, \tag{3.34}$$

where $D_{\mathrm{V}}^{\mathrm{gb}}$ is the vacancy diffusion coefficient for the grain boundary.

The grain boundary model of Fisher [58] is able to describe the vacancy transport inside the grain boundary by considering the contribution of the vacancy exchange mechanisms between grain boundary and grain bulk, and vice versa. The material balance equation that drives the vacancy concentration distribution inside the grain boundary is given by

$$\frac{\partial C_{\mathrm{V}}^{\mathrm{gb}}}{\partial t} = -\frac{\partial J_{\mathrm{V}}^{\mathrm{gb}}}{\partial x} - \frac{J_{\mathrm{V}}^{2} - J_{\mathrm{V}}^{1}}{\delta}, \tag{3.35}$$

where J_{V}^{2} and J_{V}^{1} are the normal components of the flux from both sides of the grain boundary (Figure 3.2). The second term on the right hand side of equation (3.35) represents the recombination rate of vacancies at the grain boundary region due to the diffusing fluxes from/to the bulk. In the continuum modeling approach, the chemical potential on the grain boundary (equation (3.31)) is constant throughout the width δ, and is equal to the chemical potential in the bulk (equation (3.32)) at the interfaces between bulk material and grain boundary such that

$$\mu_{\mathrm{V}}^{1}(-\delta/2) = \mu_{\mathrm{V}}^{2}(\delta/2) = \mu_{\mathrm{V}}^{\mathrm{gb}}. \tag{3.36}$$

The difference of the vacancy fluxes on both sides of the grain boundary in equation (3.35) corresponds to the gain/loss of vacancies localized at the grain boundary and approximates the vacancy generation/annihilation rate G in equation (3.27) with

$$G = -\frac{J_{\mathrm{V}}^2 - J_{\mathrm{V}}^1}{\delta} = -\frac{D_{\mathrm{V}} C_{\mathrm{V}}}{\delta k_{\mathrm{B}} T} (\nabla \mu_{\mathrm{V}}^2 - \nabla \mu_{\mathrm{V}}^1). \tag{3.37}$$

Ceric [25] provided a different interpretation of the last term by introducing the concept of trapped vacancies inside the grain boundary, with concentration $C_{\mathrm{V}}^{\mathrm{T}}$, in order to enable a more convenient numerical implementation of the grain boundary model. The model is based on the theory of segregation at the interfaces developed by Lau [101]. The grain boundary is assumed to be able to trap vacancies from both sides of the grain boundary with trapping rate ω_{T} and release them to the grains with release rate ω_{R}. The fluxes in equation (3.37) can therefore be expressed as follows

$$J_{\mathrm{V}}^1 = \omega_{\mathrm{T}} (C_{\mathrm{V,eq}}^{\mathrm{gb}} - C_{\mathrm{V}}^{\mathrm{T}}) C_{\mathrm{V}}^1 - \omega_{\mathrm{R}} C_{\mathrm{V}}^{\mathrm{T}}, \tag{3.38}$$

$$J_{\mathrm{V}}^2 = -\omega_{\mathrm{T}} (C_{\mathrm{V,eq}}^{\mathrm{gb}} - C_{\mathrm{V}}^{\mathrm{T}}) C_{\mathrm{V}}^2 + \omega_{\mathrm{R}} C_{\mathrm{V}}^{\mathrm{T}}, \tag{3.39}$$

where C_{V}^1 and C_{V}^2 are the vacancy concentrations in each grain. By substituting equations (3.38) and (3.39) into equation (3.37), it is possible to obtain the vacancy source/sink term as follows

$$G = \frac{\partial C_{\mathrm{V}}^{\mathrm{T}}}{\partial t} = \frac{\omega_{\mathrm{T}} (C_{\mathrm{V}}^1 + C_{\mathrm{V}}^2)}{\delta} \left(C_{\mathrm{V,eq}}^{\mathrm{gb}} - C_{\mathrm{V}}^{\mathrm{T}} \left(1 + \frac{2\omega_{\mathrm{R}}}{\omega_{\mathrm{T}} (C_{\mathrm{V}}^1 + C_{\mathrm{V}}^2)} \right) \right). \tag{3.40}$$

Since the grain boundary represents the interface between grains, $C_{\mathrm{V}}^1 = C_{\mathrm{V}}^2 = C_{\mathrm{V}}$, and equation (3.40) simplifies to

$$G = \frac{1}{\tau_{\mathrm{V}}^{\mathrm{gb}}} \left(C_{\mathrm{V,eq}}^{\mathrm{gb}} - C_{\mathrm{V}}^{\mathrm{T}} \left(1 + \frac{\omega_{\mathrm{R}}}{2\omega_{\mathrm{T}} C_{\mathrm{V}}} \right) \right), \tag{3.41}$$

where

$$\tau_{\mathrm{V}}^{\mathrm{gb}} = \frac{\delta}{2\omega_{\mathrm{T}} C_{\mathrm{V}}} \tag{3.42}$$

is the characteristic time of vacancy generation/annihilation for the grain boundary. Small values of $\tau_{\mathrm{V}}^{\mathrm{gb}}$ indicates that the grain boundary acts as an efficient source/sink of vacancies.

Material Interface Model

The vacancy dynamics in the presence of material interfaces can be described by using the same approach employed above for the grain boundary model. Typically, interfaces separate materials with different properties. Interfaces have higher diffusion coefficients than the bulk material, and act as sources/sinks for vacancies. If the interface separates a conducting material from a non-conducting one, the interface acts as a blocking boundary for vacancy transport from the metal line to the interface (Figure 3.3). Furthermore, since there is no flux of vacancies due to electromigration in the non-conducting material, the flux term J_{V}^{2} in equation (3.37) vanishes. In this situation, equation (3.41) reduces to

$$G = \frac{J_{\mathrm{V}}^{1}}{\delta} = \frac{1}{\tau_{\mathrm{V}}^{\mathrm{i}}}\left(C_{\mathrm{V,eq}}^{\mathrm{i}} - C_{\mathrm{V}}^{\mathrm{T}}\left(1 + \frac{\omega_{\mathrm{R}}}{\omega_{\mathrm{T}} C_{\mathrm{V}}}\right)\right), \tag{3.43}$$

where

$$\tau_{\mathrm{V}}^{\mathrm{i}} = \frac{\delta}{\omega_{\mathrm{T}} C_{\mathrm{V}}} \tag{3.44}$$

is the characteristic generation/annihilation time for the material interface.

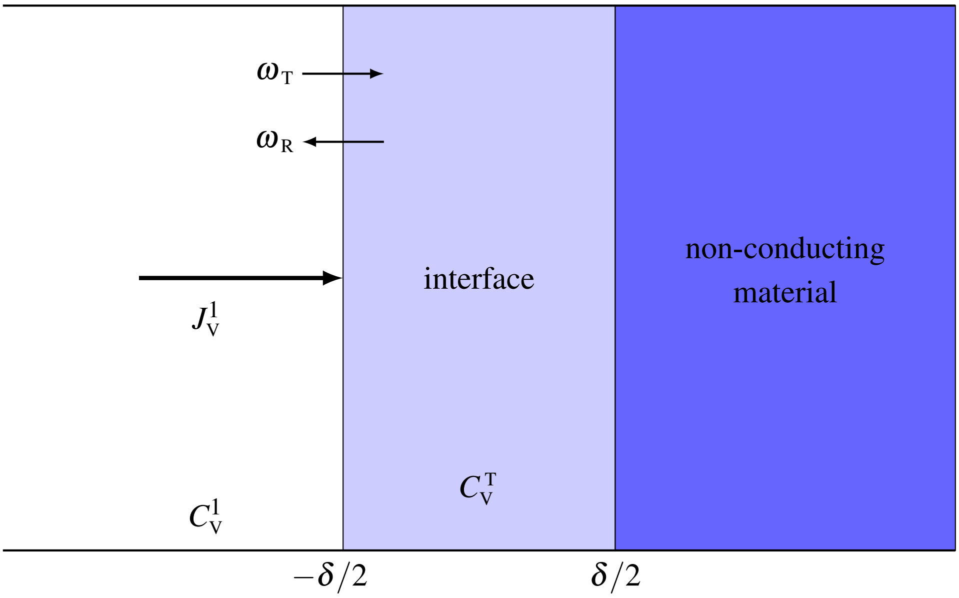


Figure 3.3: Schematic representation of an interface of width δ between two materials. The flux J_{V}^{1} changes the concentration of the mobile vacancies (C_{V}^{1}) and immobile vacancies ($C_{\mathrm{V}}^{\mathrm{T}}$). Vacancies are trapped into the material interface with trapping rate ω_{T} and released to the bulk with release rate ω_{R}.

It should be noted that under the condition

$$\frac{\omega_{\mathrm{R}}}{\omega_{\mathrm{T}} C_{\mathrm{V}}} \ll 1, \tag{3.45}$$

equations (3.41) and (3.43) reduce to the Rosenberg-Ohring term presented in equation (2.21) in Section 2.3. The grain boundary and material interface models presented above include the effect of fast diffusivity paths as vacancy sinks/sources into the bulk vacancy transport model.

Furthermore, this behavior is important for the mechanical stress calculations, described in the following section.

3.3 Solid Mechanics Model

In Section 3.2, it is stated that the redistribution of vacancy concentration in the interconnect line is mainly caused by the contributions of two mechanisms: vacancy accumulation/depletion, due to the vacancy-atom exchange process, and the generation/annihilation of vacancies, due to the source/sink process. As previously discussed in Section 2.5, the vacancy flow as well as the creation and annihilation of vacancies inside an interconnect lead to the development of volumetric strain in the metal line. Therefore, the strain induced by electromigration at any point in an interconnect occurs either by vacancy transport or by vacancy generation/annihilation. Metals respond to strains by deforming and/or by the build-up of stress.

3.3.1 Effect of Vacancy Transport

When an atom moves in an ideal crystal lattice, under the influence of the electromigration force, it leaves behind a vacancy. Considering a small test volume V in the crystal lattice, the number of atoms n_a which leave the volume is replaced by the number of vacancies n_V entering it [27]. Since the volume of a vacancy Ω_V is smaller than the volume of the atom by about 20-40% [91], the new test volume V' is given by

$$V' = V - n_\mathrm{a}\Omega_\mathrm{a} + n_\mathrm{V}\Omega_\mathrm{V} = V - n_\mathrm{a}\Omega_\mathrm{a} + n_\mathrm{V} f \Omega_\mathrm{a}, \tag{3.46}$$

where $0 < f = \Omega_\mathrm{V}/\Omega_\mathrm{a} < 1$. The relative volumetric change of the test volume ΔV, due to the vacancy exchange mechanism and associated to the change in vacancy concentration is given as follows

$$\frac{\Delta V}{V} = \frac{V' - V}{V} = -(1-f)\Omega_\mathrm{a}\frac{n_\mathrm{V}}{V} = -(1-f)\Omega_\mathrm{a}\Delta C_\mathrm{V}. \tag{3.47}$$

A local volumetric strain ε^m is induced by the local volumetric changes caused by vacancy transport and is given by

$$\frac{\Delta V}{V} = \varepsilon^\mathrm{m}_\mathrm{xx} + \varepsilon^\mathrm{m}_\mathrm{yy} + \varepsilon^\mathrm{m}_\mathrm{zz} = 3\varepsilon^\mathrm{m}, \tag{3.48}$$

when the material is considered linear and isotropic. By evaluating the time derivative of equations (3.47) and (3.48), it is possible to obtain the mechanical relationship between volume change and strain

$$\frac{\partial \varepsilon^\mathrm{m}}{\partial t} = -\frac{1}{3}(1-f)\Omega_\mathrm{a}\frac{\partial C_\mathrm{V}}{\partial t}. \tag{3.49}$$

As discussed in Section 3.2, since the vacancy accumulation/depletion mechanism due to transport is described by the flux divergence during the vacancy flow in the form

$$\frac{\partial C_{\mathrm{V}}}{\partial t} = -\nabla \cdot \vec{J}_{\mathrm{V}}, \tag{3.50}$$

the components of the transport strain rate in equation (3.49) are given by

$$\frac{\partial \varepsilon^{\mathrm{m}}_{\mathrm{ik}}}{\partial t} = \frac{1}{3}(1-f)\Omega_{\mathrm{a}} \nabla \cdot \vec{J}_{\mathrm{V}} \delta_{\mathrm{ik}}, \tag{3.51}$$

where δ_{ik} is the Kronecker delta function, which has the properties

$$\delta_{\mathrm{ik}} = \begin{cases} 1 & \text{for } i = k, \\ 0 & \text{for } i \neq k. \end{cases} \tag{3.52}$$

This function permits to reduce equation (3.51) to a single kinetic equation in terms of the trace of the transport strain tensor $\mathrm{Tr}(\varepsilon^{\mathrm{m}})$, when the transport strain tensor is diagonal with equal diagonal entries.

3.3.2 Effect of Vacancy Generation/Annihilation

The generation/annihilation of vacancies inside the test volume is caused by the change in the concentration of lattice sites. The new test volume V', due to the addiction/removal of lattice sites inside the initial volume V, is given by

$$V' = V \pm n_{\mathrm{V}} f \Omega_{\mathrm{a}}. \tag{3.53}$$

The relative volumetric change of the test volume caused by the generation/annihilation process is obtained by following the same procedure used to derive equation (3.47) to obtain

$$\frac{\Delta V}{V} = \frac{V' - V}{V} = \pm(1-f)\Omega_{\mathrm{a}} \Delta C_{\mathrm{V}}. \tag{3.54}$$

Taking the time derivative of equation (3.54), the rate of the strain ε^{m} caused by vacancy recombination is given by

$$\frac{\partial \varepsilon^{\mathrm{m}}}{\partial t} = \pm \frac{1}{3} f \Omega_{\mathrm{a}} \frac{\partial C_{\mathrm{V}}}{\partial t}. \tag{3.55}$$

Since the change in vacancy concentration due to the generation/annihilation process is related to the source/sink term G of equation (3.26)

$$\frac{\partial C_{\mathrm{V}}}{\partial t} = G, \tag{3.56}$$

the components of the recombination strain rate are given by

$$\frac{\partial \varepsilon_{\mathrm{ik}}^{\mathrm{m}}}{\partial t} = \pm\frac{1}{3} f \Omega_{\mathrm{a}} G \delta_{\mathrm{ik}}. \tag{3.57}$$

The complete kinetic relation for the strain ε^{v} induced by electromigration is given by the sum of the vacancy transport strain rate (equation (3.51)) and the vacancy recombination strain rate (equation (3.57)) as follows

$$\frac{\partial \varepsilon_{\mathrm{ik}}^{\mathrm{v}}}{\partial t} = \frac{\Omega_{\mathrm{a}}}{3}\Big((1-f)\nabla\cdot\vec{J}_{\mathrm{v}} \pm fG\Big)\,\delta_{\mathrm{ik}}. \tag{3.58}$$

The strain induced by variations in vacancy concentration ε^{v} can be determined from equation (3.58).

3.3.3 Stress-Strain Relation

In general, in addition to the influence of the electromigration induced strain, the total strain ε of the line has contributions from the thermal strain $\varepsilon^{\mathrm{th}}$ and the elastic strain ε^{σ} [20]. Thus, the total strain is given by

$$\varepsilon = \varepsilon^{\sigma} + \varepsilon^{\mathrm{th}} + \varepsilon^{\mathrm{v}}. \tag{3.59}$$

A temperature change of ΔT, with respect to a reference temperature T_0 for which thermal strains are assumed to be zero, produces a thermal strain expressed in the form

$$\varepsilon_{\mathrm{ik}}^{\mathrm{th}} = \alpha_{\mathrm{th}} \Delta T \,\delta_{\mathrm{ik}}, \tag{3.60}$$

where α_{th} is the coefficient of thermal expansion. Assuming that the metal line is linearly elastic and isotropic, the mechanical behavior of the material is described by a constitutive equation, which relates the stress to an imposed history of strain and other sources which cause inelastic strains, such as material transport due to electromigration and temperature [161]. Hooke's law applies to elastic strains, so that

$$\sigma_{\mathrm{ik}} = C_{\mathrm{iklm}} \varepsilon_{\mathrm{lm}}^{\sigma} = C_{\mathrm{iklm}}(\varepsilon_{\mathrm{lm}} - \varepsilon_{\mathrm{lm}}^{\mathrm{th}} - \varepsilon_{\mathrm{lm}}^{\mathrm{v}}), \tag{3.61}$$

where C_{iklm} are the components of the stiffness tensor defined by

$$C_{\mathrm{iklm}} = \lambda \delta_{\mathrm{ik}} \delta_{\mathrm{lm}} + \mu(\delta_{\mathrm{il}} \delta_{\mathrm{km}} + \delta_{\mathrm{im}} \delta_{\mathrm{kl}}), \tag{3.62}$$

where λ and μ are the Lamé parameters expressed in terms of the Young's modulus E and the Poisson ratio ν using

$$\lambda = \frac{\nu \mathrm{E}}{(1+\nu)(1-2\nu)}, \quad \mu = \frac{\mathrm{E}}{2(1+\nu)}. \tag{3.63}$$

For linear isotropic materials, the stress-strain relation simplifies to

$$\sigma_{\text{ik}} = \lambda \delta_{\text{ik}} (\varepsilon_{\text{ll}} - \varepsilon_{\text{ll}}^{\text{th}} - \varepsilon_{\text{ll}}^{\text{v}}) + 2\mu (\varepsilon_{\text{ik}} - \varepsilon_{\text{ik}}^{\text{th}} - \varepsilon_{\text{ik}}^{\text{v}}). \tag{3.64}$$

In matrix notation, Hooke's law for isotropic materials can be written as

$$\begin{bmatrix} \sigma_{\text{xx}} \\ \sigma_{\text{yy}} \\ \sigma_{\text{zz}} \\ \tau_{\text{xy}} \\ \tau_{\text{yz}} \\ \tau_{\text{zx}} \end{bmatrix} = \begin{bmatrix} \lambda+2\mu & \lambda & \lambda & 0 & 0 & 0 \\ \lambda & \lambda+2\mu & \lambda & 0 & 0 & 0 \\ \lambda & \lambda & \lambda+2\mu & 0 & 0 & 0 \\ 0 & 0 & 0 & \mu & 0 & 0 \\ 0 & 0 & 0 & 0 & \mu & 0 \\ 0 & 0 & 0 & 0 & 0 & \mu \end{bmatrix} \begin{bmatrix} \varepsilon_{\text{xx}} \\ \varepsilon_{\text{yy}} \\ \varepsilon_{\text{zz}} \\ \gamma_{\text{xy}} \\ \gamma_{\text{yz}} \\ \gamma_{\text{zx}} \end{bmatrix} - B(\varepsilon^{\text{th}} + \varepsilon^{\text{v}}) \begin{bmatrix} 1 \\ 1 \\ 1 \\ 0 \\ 0 \\ 0 \end{bmatrix}, \tag{3.65}$$

where τ_{ik} are the shear stresses, $\gamma_{\text{ik}} = \varepsilon_{\text{ik}} + \varepsilon_{\text{ki}} = 2\varepsilon_{\text{ik}}$ $(i \neq k)$ are the "engineering" shear strains, and B is the bulk modulus expressed in the form

$$B = \frac{3\lambda + 2\mu}{3} = \frac{\text{E}}{3(1-2\nu)}. \tag{3.66}$$

3.3.4 Mechanical Deformation

In mechanical theory, when atoms of a solid body move as a response to an applied force, their movement produces local strain which leads to changes in the body's shape and size [19]. This means that the body is subjected to deformation. In order to quantitatively study the deformation of a solid, the displacement field $\vec{u}$ at each point in the strained body, with respect to the initial position in the unstrained state, should be introduced. In linear elasticity, it is common to assume small displacement fields from the original configuration such that the total strain tensor is

$$\varepsilon_{\text{ik}} = \frac{1}{2}\left(\frac{\partial u_{\text{i}}}{\partial x_{\text{k}}} + \frac{\partial u_{\text{k}}}{\partial x_{\text{i}}}\right). \tag{3.67}$$

The infinitesimal strain theory [67] describes the deformation of a solid body in which the displacements of the material are assumed to be much smaller than the body's dimensions. The evolution of the displacement vector is determined by the equation of motion derived from Newton's second law as follows

$$\rho_{\text{m}} \frac{\partial^2 \vec{u}}{\partial t^2} = \nabla \cdot \overline{\overline{\sigma}} + \vec{F}_{\text{B}}, \tag{3.68}$$

where $\vec{F}_{\text{B}}$ is the body force per unit volume which acts throughout the volume of a body, in contrast to the divergence of the stress tensor $\overline{\overline{\sigma}}$ within the same volume. During electromigration, the accelerations in the structure are small and no external forces are acting on the line [133]. Equation (3.68) therefore reduces to the well known mechanical equilibrium equation in the form

$$\nabla \cdot \overline{\overline{\sigma}} = 0. \tag{3.69}$$

3.3.5 Model Equations

Substituiting the stress-strain relation (equation (3.64)), and the standard relationship between the total strain tensor and the displacement field (equation (3.67)) into equation (3.69), the equation for the displacement field in the metal line is obtained [132]

$$\mu \nabla^2 u_\mathrm{i} + (\lambda + \mu) \frac{\partial}{\partial x_\mathrm{i}} (\nabla \cdot \vec{u}) = B \frac{\partial \mathrm{Tr}(\varepsilon^\mathrm{th} + \varepsilon^\mathrm{v})}{\partial x_\mathrm{i}}. \tag{3.70}$$

This is the Navier-Cauchy equation which enables the determination of the total line displacement in terms of the trace of the non-elastic stress tensors for given boundary conditions.

The stresses in the line can also be obtained by solving the mechanical equilibrium equation (3.69). In this way, 3D equations for the mechanical stress distribution inside the metal line, subjected to specific boundary conditions, can be derived [133]. In particular, the three normal components of the stress tensor determine the hydrostatic pressure p acting on the line as follows

$$p = \pm \frac{\sigma_\mathrm{xx} + \sigma_\mathrm{yy} + \sigma_\mathrm{zz}}{3}, \tag{3.71}$$

where the positive sign results in tension, and the negative one in compression.

3.3.6 Void Nucleation

As described in Section 2.6, the void nucleation condition represents the transition from the first to the second phase of electromigration failure [25]. From the early days of electromigration modeling, the void nucleation condition has been derived from careful investigations based on the classical nucleation theory [36, 59, 63, 64]. In particular, the authors of the nucleation theory have determined the cause for void nucleation by the tensile stress σ_thr reaching a threshold value at those sites of the interconnect where the adhesion between the metal and passivation layers is weak. The expression for the threshold stress for void nucleation [36] is given by

$$\sigma_\mathrm{thr} = \frac{2\gamma_m \sin\theta_\mathrm{C}}{R_\mathrm{P}}, \tag{3.72}$$

where γ_m is the interfacial free energy of the metal, θ_C is the critical contact angle, and R_P is the radius of the adhesion-free patch. Figure 3.4 shows the time evolution of the stress build-up caused by electromigration. If the stress is below the threshold value ($\sigma < \sigma_\mathrm{thr}$), the energy barrier for stable void formation exists. The stress build-up increases with time until it reaches the threshold value for void nucleation. For $\sigma > \sigma_\mathrm{thr}$, the energy barrier decreases leading to the nucleation of a stable void at the interface between the metal and the passivation layer. The void nucleation condition is therefore useful to determine the time needed to nucleate a stable void. By assuming the adhesion-free patch with a radius of 10nm in a typical copper interconnect, the stress needed to nucleate a void in the interconnect is in the order of 330MPa, and can already be reached by the thermal stress alone [25]. Lower threshold stresses, which can be reached by electromigration, are obtained by considering bigger patch radii.

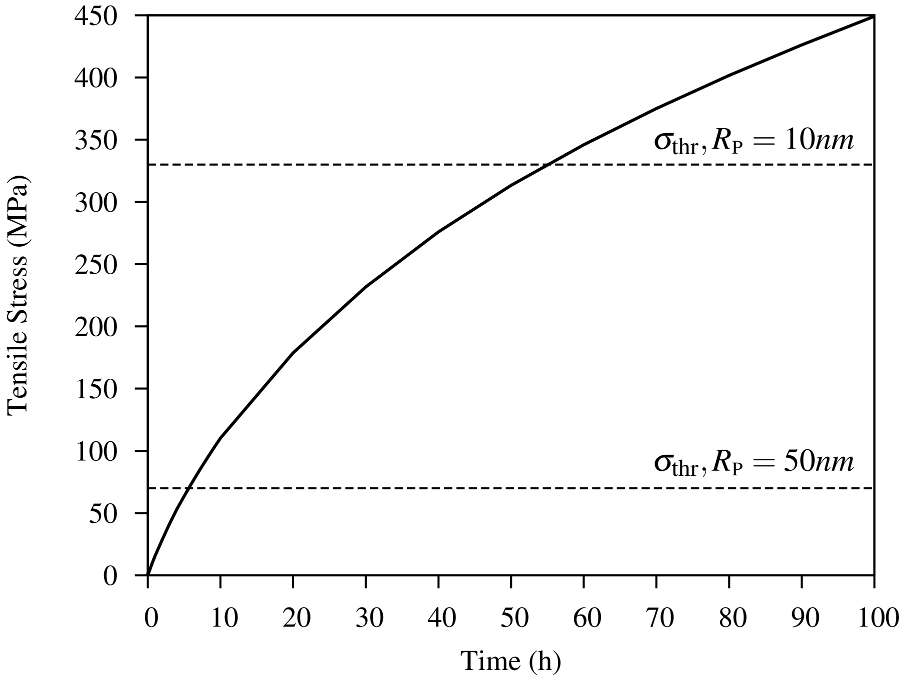


Figure 3.4: Time evolution of the stress build-up due to electromigration in a copper interconnect. Two different threshold tensile stresses for differing patch radii R_{P} are presented.

3.4 Void Evolution Models

Voids nucleate in the interconnect due to the development of tensile stress, particularly at those locations where the adhesion between the metal layer and the surrounding material is weak. Stable voids nucleate when the stress build-up due to voiding, defined by equation (3.72), becomes critical. Once the void has nucleated, the failure development due to electromigration enters the second phase, namely void evolution. During this phase, voids can grow, migrate, and change shape due to vacancy transport along its surface driven by the electromigration force, the temperature gradient, the vacancy concentration gradient, and the mechanical stress gradient. The void evolution mechanism leads to a significant increase in the interconnect resistance, triggering complete open circuit failure.

The void evolution mechanism is complex, since it is initiated as the result of a competition between growth, shape change, and motion of the voids [3]. Furthermore, vacancy transport may occur along different paths, such as void surfaces, bulk, grain boundary, and metal/passivation layer interfaces [29], influencing the behavior of the void evolution. Various numerical approaches for the simulation of void evolution due to electromigration in interconnect structures have been developed [10, 45, 61, 62, 71, 108, 135, 152]. These methods can be divided in two different categories: void surface evolution methodologies, such as sharp interface [62, 71, 135] and diffuse interface [10, 11, 107, 108] models, and semi-empirical approaches [42, 43, 45, 60, 61, 152]. Each numerical model focuses on a particular mechanism or on the combination of multiple mechanisms, when it comes to the void evolution. In the following, the three different methods for describing the electromigration void evolution phenomenon in interconnects are presented. The calculation of the change in resistance due to the growing void is obtained from numerical calculations based on the void evolution models.

3.4.1 Sharp Interface Model

Most of the existing models for electromigration void evolution are based on sharp interface approaches [62, 71, 96, 135, 156]. They model the void surface as a distinct sharp boundary between the material of the metal line and the empty space in the void. The surface is described by specifying a large number of points on it. Thus, sharp interface methods require an explicit tracking of void surfaces during their evolution and those surfaces define moving boundary problems. As nucleated voids can grow, migrate, and change shape during the course of the evolution, the void surface tracking can be demanding and needs automatic adaptive mesh generation to trace the large shape modifications which normally occur [148].

Before describing the physical principles behind the sharp interface model, an overview of the assumptions which underlie the analysis should be provided [11]. The interconnect line is assumed to function as a 2D conducting deformable solid, with a void surface located inside the line, as illustrated in Figure 3.5. The interconnect line is subjected to a voltage ΔV_{E} applied across its ends, inducing a local electrical field $\vec{E}$ in the line. The metal line is idealized as an isotropic, linear elastic solid, and diffusion in the bulk of the line is neglected. Under the influence of the induced electrical field, the void evolution mechanism due to electromigration is mainly related to surface diffusion. Surface diffusion is also influenced by the mechanical stress gradient and the void curvature. The diffusion of atoms along the void surface causes it to change its shape, leading to void growth. Another small contribution governing the void growth arises from feeding the void with vacancies from the bulk. Additional features can also contribute to the evolution of the void, such as grain boundary diffusion and anisotropic surface diffusivity.

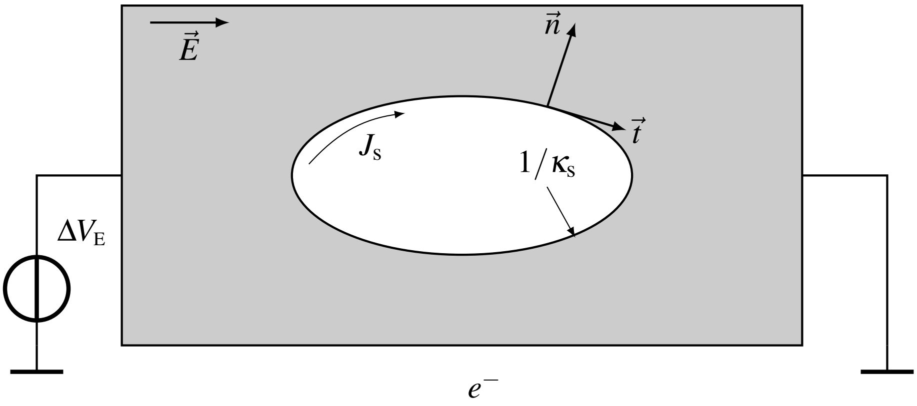


Figure 3.5: Idealization of the void surface in a 2D conducting interconnect line.

In the absence of electric currents, the transport of atoms lying on the void surface is driven by the gradient of the chemical potential. The chemical potential μ_{s} of an atom on the surface is given by [62]

$$\mu_{\rm s} = \mu_0 - \Omega_{\rm a}\gamma_{\rm s}(\theta)\kappa_{\rm s} + \frac{\Omega_{\rm a}(\overline{\overline{\sigma}} : \overline{\overline{\varepsilon}})}{2}, \tag{3.73}$$

where μ_0 is the reference chemical potential, $\gamma_{\rm s}(\theta)$ is the orientation angle θ dependent constant related to the surface energy, $\kappa_{\rm s}$ is the local curvature of the metal/void interface, and the double-dot product is defined for the tensors $\overline{\overline{\sigma}}$ and $\overline{\overline{\varepsilon}}$ as follows

$$\overline{\overline{\sigma}} : \overline{\overline{\varepsilon}} = \sum_{i,j} \sigma_{\rm ij}\varepsilon_{\rm ij}. \tag{3.74}$$

The second term on the right hand side of equation (3.73) refers to the free energy of the surface on which $\kappa_{\rm s}$ assigns negative curvature to convex surfaces and positive curvature to concave surfaces. The third term is related to the local elastic strain energy. Electric current provides an additional driving force for surface transport, namely the electron wind force. The surface chemical potential and the electromigration driving force relate to the total atomic flux $J_{\rm s}$ along the metal/void interface as follows

$$J_{\rm s} = \frac{D_{\rm s}(\theta)\delta_{\rm s}}{k_{\rm B}T}\left(-\nabla_{\rm s}\mu_{\rm s} + Z^* e\nabla_{\rm s}V_{\rm E}\right). \tag{3.75}$$

Here, $\nabla_{\rm s}$ is the surface Laplacian operator, $\delta_{\rm s}$ is the thickness of the diffusion layer, and $D_{\rm s}(\theta)$ is the temperature and orientation dependent constant related to the surface diffusion coefficient through the Arrhenius law

$$D_{\rm s}(\theta) = D_{\rm s,0}\left[1 + m\left(1 - \cos(n\theta - \theta_0)\right)\right] \exp\left(-\frac{Q_{\rm s}}{k_{\rm B}T}\right), \tag{3.76}$$

where $D_{\rm s,0}$ is the pre-exponential coefficient for surface diffusion, m is the degree of anisotropy, n is the crystallographic symmetry, θ_0 is the orientation of the interconnect line with respect to the face-centered-cubic crystal planes, and $Q_{\rm s}$ is the activation energy for surface diffusion [62]. The isotropic medium is a special case in which $\gamma_{\rm s}$ is a constant and $m = 0$. The assumption of a dense network of grain boundaries, where all the grains are equally distributed in every direction, permits to neglect anisotropic effects and grain boundary diffusion in the line. As a consequence, the diffusion along the void surface leads to void growth and changes of the void shape due to anisotropic and grain boundary diffusivities should be neglected.

The resulting atomic flux along the void surface is therefore proportional to the component of the electrical field $E_{\rm s} = \vec{E}_{\rm s} \cdot \hat{t}$ in the tangential surface direction $\hat{t}$ [25]. The normal velocity $v_{\rm n}$ at each point of the void surface can be obtained from equation (3.75) as follows

$$v_{\rm n} = -\nabla_{\rm s}J_{\rm s} = -\frac{D_{\rm s}\delta_{\rm s}}{k_{\rm B}T}\left(-\nabla^2_{\rm s}\mu_{\rm s} + Z^* e\nabla^2_{\rm s}V_{\rm E}\right), \tag{3.77}$$

where D_s is the isotropic surface diffusivity ($m = 0$ in equation (3.76)). This equation implies conservation of the void size during important morphological void changes [11]. The void surface moves as a result of the contributions of the unbalanced fluxes due to gradients in the curvature, elastic strain energy, and electrical potential. It should be pointed out that elastic strain energy effects have been shown to dominate electromigration in passivated copper lines during the void nucleation period, while for void evolution, electron wind becomes the major driving force [118, 152]. The effect of mechanical stress on the void evolution mechanism can therefore be neglected, when performing an analysis of a copper interconnect line.

As mentioned before, sharp interface modeling appears convenient to describe the void shape changes during void evolution, but special techniques to track the metal/void interface for every simulation time step are required. The front tracking problem requires re-meshing at every time step, which gives rise to converging issues and is generally difficult to handle. It should be mentioned, however, that the computational demands of surface tracking through a sharp interface model have been largely addressed by combining the front tracking method with more efficient methods of solving the corresponding boundary-value problems with which the surface evolution problem is coupled. Such an example is the state-of-the-art boundary-integral methods with numerous applications to the void dynamics problem in the literature [4, 68, 69]. The boundary-integral method has found an advantage over the finite-element method (FEM) when it comes to tracking the interface corresponding to the void surface.

3.4.2 Diffuse Interface Model

The diffuse interface method, or phase field method, offers an attractive alternative to the sharp interface model for solving problems related to the electromigration evolution of the void surface. Various authors [10, 11, 107, 108] have applied the diffuse interface approach to predict the motion and growth of voids in interconnects due to electromigration and stress-induced surface diffusion. It should be pointed out that the diffuse interface model is viewed as an approximation to the sharp interface model of Section 3.4.1.

The interconnect line is idealized as a two-phase system consisting of the material "phase" and the void "phase". The introduction of a smooth order parameter field ϕ (or phase field variable) to describe the void structure circumvents the surface tracking used in the sharp interface method. The order parameter takes on constant values in the material phase ($\phi = +1$) and in the void phase ($\phi = -1$) in the entire domain Ω and changes rapidly from one to the other over a narrow interfacial layer which represents the void surface, as illustrated in Figure 3.6. The basic concept of the diffuse interface approach involves the spread of the sharp metal/void interface into a narrow interfacial layer between the metal phase and the void phase. In the limit of vanishing interface layer thickness, the two models will perfectly match.

The form of the equations governing the dynamics of the order parameter is based on the microforce balance principle of Gurtin [72]. Inhomogeneous systems involve domains of well-defined phases separated by a narrow interface (Figure 3.6). If the phases are driven out

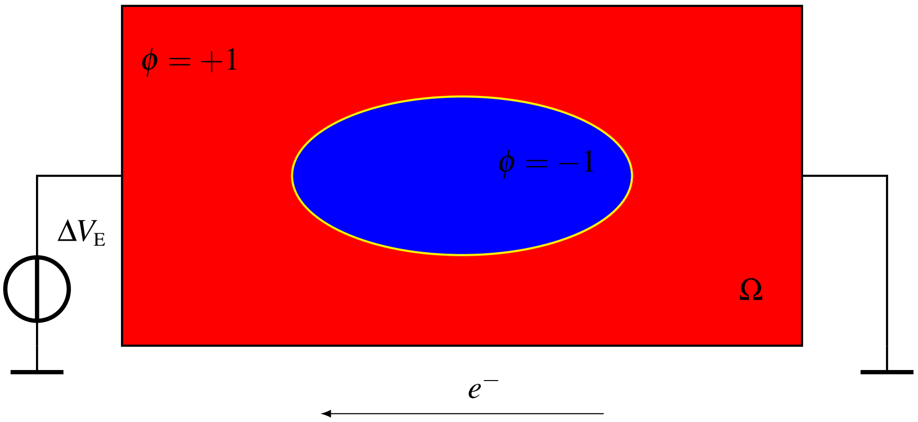


Figure 3.6: Order parameter distribution in a 2D conducting metal line.

of equilibrium, one phase will grow at the cost of the other. Thermodynamic equilibrium is reached if the state of a system remains constant [53]. Therefore, the system tends to move towards the equilibrium condition. During this transition, the free energy of the system is minimized. The minimization of the free energy rate yields the dynamics equations governing the evolution of the near-equilibrium system [130]. Diffuse interface models are introduced to study systems out of equilibrium. Traditional diffuse interface models are connected to thermodynamics by a phenomenological free energy functional written in terms of the order parameter, its gradient, and the local strain. The free energy functional $\mathscr{F}$, which divides the entire domain Ω in Figure 3.6 into two regions of constant order parameter value separated by a narrow metal-void interface [107], is chosen as

$$\mathscr{F}(\phi, \nabla\phi, \bar{\bar{\varepsilon}}) = \int_\Omega \left[\frac{2\gamma_\mathrm{s}}{\varepsilon_\mathrm{di}\pi} \left(\frac{1}{4}(\phi^2 - 1)^2 + \frac{1}{2}\varepsilon_\mathrm{di}^2 |\nabla\phi|^2 \right) + \frac{\bar{\bar{\sigma}} : \bar{\bar{\varepsilon}}}{2} \right] \mathrm{d}\Omega, \tag{3.78}$$

where γ_s is the isotropic surface energy and ε_di is the parameter which scales with the thickness of the interface located at the void surface. For reasons mentioned in the previous section, the effect of the elastic strain energy on the free energy functional is neglected, when it comes to the analysis of the void evolution mechanism for passivated copper lines. For simplicity, both surface energy and surface diffusivity are assumed to be isotropic.

The two terms in round brackets in the free energy functional equation (3.78) describe the surface free energy. The surface free energy represents the energy cost associated with the addition or removal of material from the void surface [130]. The first surface free energy term in equation (3.78) is related to the bulk free energy. Conventionally, it is taken to be a quartic double well potential [107] which drives phase separation, with two minima corresponding to the material and the void phases. Bhate [10, 11] employed an alternative form of the bulk free energy function based on the double obstacle potential proposed by Oono [119]. By choosing a bi-quadratic function, order parameter solutions different from ±1 are penalized, as shown in Figure 3.7. The presence of the bulk free energy term, as a bi-quadratic function, in the free energy functional equation (3.78) requires the order parameter to be computed throughout the bulk of the line, not only within the narrow interfacial layer marking the void surface. The second surface free energy term in equation (3.78) represents the gradient energy (or interfacial energy), which denotes the contribution of the diffuse interface [53]. The void interface is located at those sites in the domain with nonzero gradients. As a result, the order parameter is defined in such a way that the volume fractions of the material and void phases are $(1+\phi)/2$ and $(1-\phi)/2$, respectively. Significant deviations of the order parameter from either $+1$ or -1 occur only within the metal-void interface.

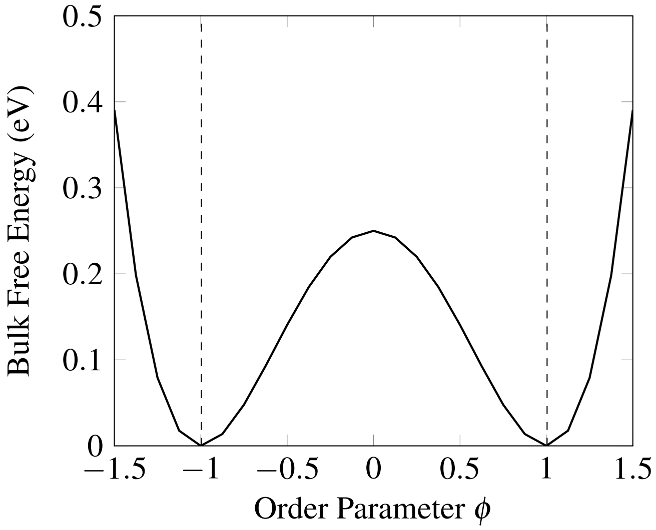


Figure 3.7: Quartic double well potential for the free energy function.

The free energy functional provides an expression for the chemical potential μ_s of an atom in the interfacial region, which is the functional derivative of the free energy functional with respect to the order parameter function, and is given by

$$\begin{aligned}\mu_\mathrm{s} &= 2\Omega_\mathrm{a}\frac{\delta\mathscr{F}}{\delta\phi} = 2\Omega_\mathrm{a}\left(\frac{\partial\mathscr{F}}{\partial\phi} - \nabla\cdot\left(\frac{\partial\mathscr{F}}{\partial\nabla\phi}\right)\right) \\ &= \frac{4\gamma_\mathrm{s}\Omega_\mathrm{a}}{\varepsilon_\mathrm{di}\pi}\left(\phi(\phi^2-1) - \varepsilon_\mathrm{di}^2\nabla^2\phi\right).\end{aligned} \tag{3.79}$$

The factor of 2 multiplying Ω_a in the chemical potential equation is introduced as the order parameter transition from $+1$ in the material to -1 in the void across a narrow interface [11]. As described above, the elastic strain energy term of equation (3.78) is not considered in the further development of the model.

The chemical potential relates to the driving force of diffusion $\vec{F}_\mathrm{D} = -\nabla\mu_\mathrm{s}$. In fact, as discussed in Section 3.4.1, atoms diffuse on the void surface from high chemical potential regions to low chemical potential regions. In Section 3.2 it has been shown that the material transport responsible for electromigration failure occurs due to a combination of different driving forces, such as the electron wind, the mechanical stress gradient, and the temperature gradient. The electromigration force $\vec{F}_\mathrm{EM}$ is the most dominant driving force with regards to the mass flux responsible for electromigration-induced void evolution [118]. Stress and temperature gradients are therefore not taken into account as driving forces for mass transport [62]. Furthermore, the electromigration-induced material transport on the void surface is assumed to be faster than diffusion in the bulk of the metal line [71]. In the presence of electromigration the total driving force leads to the mass flux $\vec{J}_{\mathrm{s}}$ along the void surface as

$$\vec{J}_{\mathrm{s}} = \frac{2D_{\mathrm{s}}(\phi)}{\varepsilon_{\mathrm{di}}\pi}\left(\vec{F}_{\mathrm{D}} + \vec{F}_{\mathrm{EM}}\right) = -\frac{2D_{\mathrm{s}}(\phi)}{\varepsilon_{\mathrm{di}}\pi}\left(\nabla\mu_{\mathrm{s}} - e|Z^{*}|\nabla V_{\mathrm{E}}\right), \tag{3.80}$$

In order to confine diffusion to the void surface only, the isotropic surface diffusivity function $D_{\mathrm{s}}(\phi)$ is set to

$$D_{\mathrm{s}}(\phi) = \begin{cases} \dfrac{D_{\mathrm{s}}\delta_{\mathrm{s}}}{k_{\mathrm{B}}T} & \text{if } |\phi|<1, \\ 0 & \text{otherwise.} \end{cases} \tag{3.81}$$

Note that the function $D_{\mathrm{s}}(\phi)$ vanishes outside the interfacial region [10]. Since the order parameter is a conserved quantity, its evolution can be described as a consequence of divergences in the surface flux by the following equation

$$\frac{\partial\phi}{\partial t} = -\,\nabla\cdot\vec{J}_{\mathrm{s}} = \frac{2D_{\mathrm{s}}(\phi)}{\varepsilon_{\mathrm{di}}\pi}\nabla\cdot\left(\nabla\mu_{\mathrm{s}} - e|Z^{*}|\nabla V_{\mathrm{E}}\right) + \frac{2}{\varepsilon_{\mathrm{di}}\pi}\nabla D_{\mathrm{s}}(\phi)\cdot\left(\nabla\mu_{\mathrm{s}} - e|Z^{*}|\nabla V_{\mathrm{E}}\right). \tag{3.82}$$

This equation is the so-called Cahn-Hilliard equation [21, 22], which is a 4th-order PDE with modifications due to the presence of an electrical potential gradient. Since $\nabla D_{\mathrm{s}}(\phi)$ is a distribution the second term on the right hand side of equation (3.82) is a flux term modeling inflow or outflow of atoms through the metal-void interface. The above equation (3.82) is supplemented with no-flux boundary conditions and initial values for the order parameter field in the entire domain Ω (Figure 3.6) as follows

$$\hat{n}\cdot\vec{J}_{\mathrm{s}} = 0 \quad \text{on} \quad \Gamma_{ext}, \tag{3.83}$$

$$\phi(x,0) = \phi^{0}(x) \in [-1,1] \quad \forall x \in \Omega, \tag{3.84}$$

where $\hat{n}$ is the outward normal vector at the surface. The no-flux boundary condition leads to the conservation of the void's area. In this way, the solution of ϕ in equation (3.82) possesses the properties that the total free energy of the metal-void system diminishes to maintain thermodynamic equilibrium and that the total mass $\int_{\Omega}\phi\,\mathrm{d}\Omega$ is conserved. Further boundary conditions which relate void growth due to electromigration-driven diffusion to an appropriate case study are presented in detail in Chapter 5.

In addition, the evolution equation for the order parameter which describes the void's change in shape or the void's drift along the metal line must be related to the equation determining the electric current induced mass transport in the metal line. As discussed in Section 3.1, the electric potential at any point in the interconnect is related to the electric current density $\vec{j}$ by Ohm's law

$$\vec{j} = -\sigma_{\mathrm{E}}(\phi)\nabla V_{\mathrm{E}}, \tag{3.85}$$

where σ_{E} is the electrical conductivity of the metal. In this way, the current density distribution can be evaluated in the entire domain. In the sharp interface model, the void surface acts as an insulating boundary for the electric current flowing through the line. In order to incorporate the no current flux boundary condition at the void surface in the diffuse interface model [10], the electrical conductivity is chosen to vary as the order parameter goes from $+1$ in the material to -1 in the void by

$$\sigma_{\mathrm{E}}(\phi) = \frac{\sigma_{\mathrm{E}}^{\star}}{2}(\phi + 1). \tag{3.86}$$

This simple linear function reduces conductivity to its bulk value $\sigma_{\mathrm{E}}^{\star}$ in the metal "phase", but vanishes within the void "phase". For small values of the $\varepsilon_{\mathrm{di}}$ parameter this condition ensures an appropriate boundary condition at the void surface. As described previously, the evolution of the void is due mainly to material transport at the void surface, driven by the electromigration force. The mass flux $\vec{J}_{\mathrm{s}}$ along a void surface is assumed to be proportional to the component of the current density tangential to the surface j_{es}. By assuming a zero normal current density at the void surface, the tangential current density j_{es} is described as the average current density over the void surface [28] given by

$$j_{\mathrm{es}} = 2\frac{\int_{\Omega} \|\vec{j}\| (1-\phi^2)\mathrm{d}\Omega}{\int_{\Omega}(1-\phi^2)\mathrm{d}\Omega}, \tag{3.87}$$

where the term $1-\phi^2$ is non-zero only at the void-metal interface. Equations (3.85) and (3.87) allow one to determine the current density distributions in the metal-void system and at the void surface, respectively. Since electric charge should be conserved, the distribution of electric potential in the line is determined by the Laplace equation

$$\nabla \cdot (\sigma_{\mathrm{E}}(\phi)\nabla V_{\mathrm{E}}) = 0. \tag{3.88}$$

The order parameter distribution in the line is therefore determined for each time step by coupling the solutions of the dynamic equation of the order parameter (3.82) together with the solutions of the electrical problem (equations (3.85) - (3.88)).

The capabilities of the diffuse interface model are validated by performing two convenient tests of numerical accuracy on a simple 2D rectangular metal line, in order to evaluate the different impacts of surface energy and electromigration on the diffusion underlying the evolution of the void in the interconnect. First, the evolution of a non-circular void towards its equilibrium shape is examined, in the absence of any electrical potential gradient in the metal line. Simulations are performed using the diffuse interface model. The results, depicted in Figure 3.8, represent the zero contours of the order parameter at different time steps. Under conditions of surface energy driven diffusion, the system tends to minimize the surface free energy by minimizing the void surface. As a result, the elliptical void is expected to relax to a circular void in time [11], which is exactly what the simulation shows.

Next, the migration of a circular void in a rectangular metal interconnect, subjected to an electromigration force, is analyzed by tracking the order parameter distribution in the

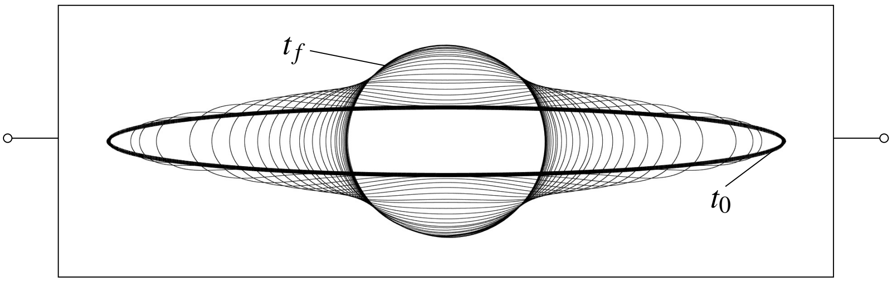


Figure 3.8: Evolution of an elliptical void in a non-electrically conducting line. The ellipse collapses into a circle due to surface energy driven diffusion.

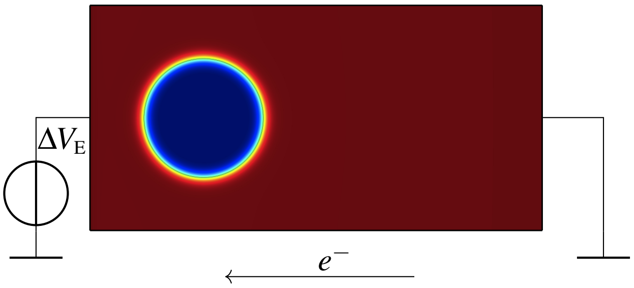
structure. The electromigration effect is induced in the line by applying a voltage ΔV_{E} across its ends (Figure 3.9). In this case, the resulting void evolution is a consequence of a complex coupling of driving factors: migration due to the electromigration force counteracted by a predisposition towards minimizing the surface of the void [11]. Figure 3.9 shows the typical numerical test results at different time steps. The void surface remains morphologically stable and the void moves towards the cathode at a constant velocity due to the electrical potential gradient, without undergoing additional changes in shape. This behavior is in accordance with the analysis of Ho [78], who has demonstrated that the evolving void maintains a stable circular shape and that the migration velocity v_{n} is linearly proportional to the applied electrical potential gradient ∇V_{E} and inversely proportional to the void radius r_{V} as follows

$$v_{\mathrm{n}} = 2\frac{D_{\mathrm{s}}\delta_{\mathrm{s}}}{r_{\mathrm{V}}k_{\mathrm{B}}T}Z^{*}e\nabla V_{\mathrm{E}}. \tag{3.89}$$

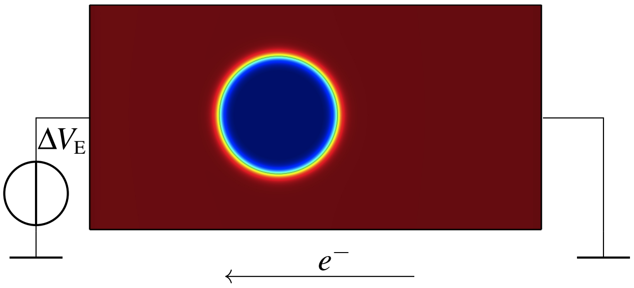
In order to demonstrate the proportionality, the migration velocity is calculated by increasing the applied voltage ΔV_{E} in the line at different void radii, as illustrated in Figure 3.10. The fit of the curves to equation (3.89) indicates that the velocities obtained from the simulations are in good agreement with the solution provided by Ho [78]. As expected, the numerical tests demonstrate the accuracy of the diffuse interface model within the limit as the interface width vanishes.

3.4.3 Semi-Empirical Method

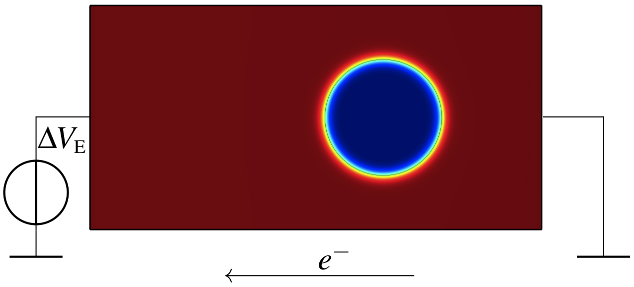
Another method used to investigate the void evolution phenomenon caused by electromigration in interconnects is derived from a semi-empirical approach. Semi-empirical models for void evolution offer analytical expressions of measurable quantities (electrical resistance, time-to-failure,etc.) derived partially from theoretical aspects and partially obtained from experimental observations or by fitting to experimental results. The main difference from the void surface evolution models described previously is that semi-empirical methods involve approximations and assumptions in the physical theory, behind the model itself, in order to simplify the numerical calculation or to yield a result in accordance with experimental observations.



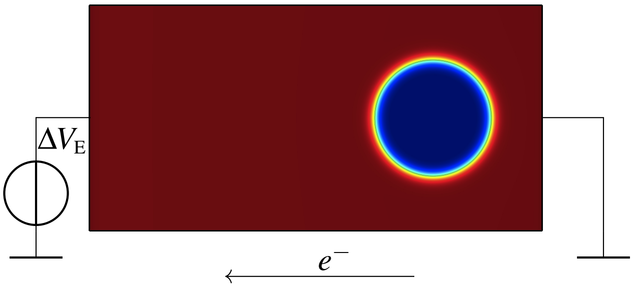
(a) t = 0 s.



(b) t = 1 s.



(c) t = 2 s.



(d) t = 20 s.

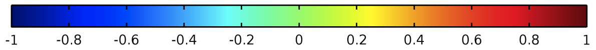


Figure 3.9: Order parameter distribution of an evolving stable circular void in an interconnect line under electrical loading ΔV_{E}. The void profiles are plotted at (a) $t = 0$s, (b) $t = 1$s, (c) $t = 2$s, and (d) $t = 20$s. The void maintains its circular shape as it migrates through the line due to a combination of the surface energy gradient and the electromigration force.

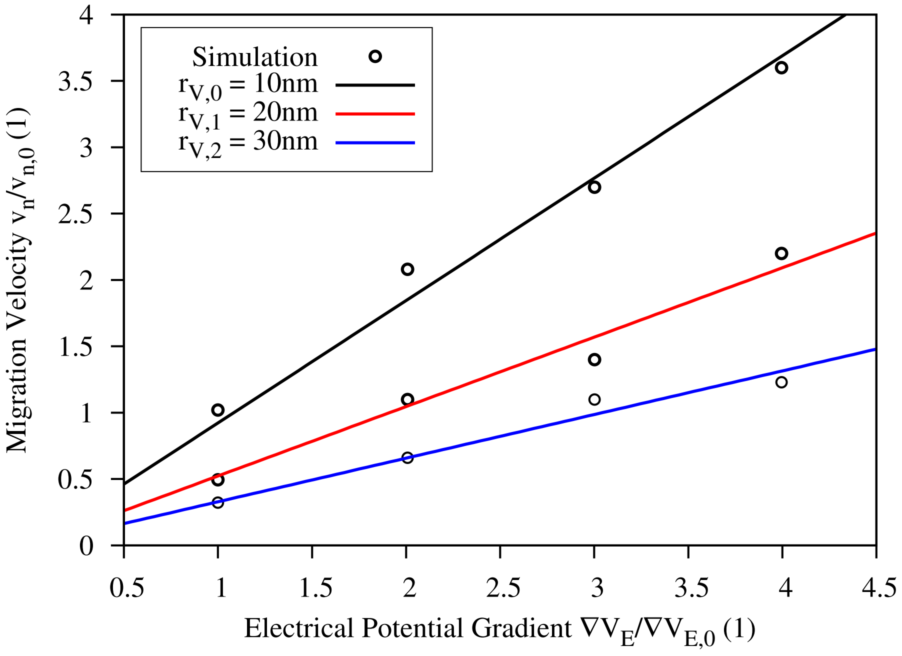


Figure 3.10: Migration velocity v_n as a function of electrical potential gradient for different void radii r_V. The lines indicate the fit according to equation (3.89).

In this section, a semi-empirical analytical model describing the time required to grow a void in a passivated metal line, based on the void size dependence of the incoming flux of vacancies due to electromigration, is presented. The development of the model is mainly based on experimental studies presented in the work of Frank *et al.* [60].

In Section 3.2, the general expression of the vacancy flux responsible for electromigration failure in a metal line was obtained from equation (3.24). It has been shown that the electromigration force is the most dominant driving force in the vacancy flux responsible for the electromigration void evolution failure [118]. Therefore, in this context the other flux terms in equation (3.24), representing the components of the back-flux [16], can be neglected. The vacancy flux driven by electromigration can be written as

$$\vec{J}_\mathrm{V} = \frac{D_\mathrm{V} C_\mathrm{V} |Z^*| e \rho_\mathrm{E} \vec{j}}{k_\mathrm{B} T}, \tag{3.90}$$

where ρ_E is the electrical resistivity of the metal. The vacancy flux induces the void nucleation in the section of the interconnect, where the highest vacancy flux divergence is expected. The flow of electric current transports the vacancies towards this region, where they are captured at the void surface. They may diffuse along the void surface, causing the void to grow. The void volume V_V change in time, due to the captured vacancies at the void surface, is given by

$$\frac{\partial V_\mathrm{V}}{\partial t} = f \Omega_\mathrm{a} A_\mathrm{i} \|\vec{J}_\mathrm{V}\| = f \Omega_\mathrm{a} A_\mathrm{i} \frac{D_\mathrm{V} C_\mathrm{V} |Z^*| e \rho_\mathrm{E} \|\vec{j}\|}{k_\mathrm{B} T}, \tag{3.91}$$

where A_i is the cross sectional area of a given interconnect. Considering the case of an initial spherical void spanning the line (Figure 3.11), it is possible to approximate its evolution and local geometric features; a quarter-spherical void grows as

$$\frac{\partial V_\mathrm{V}}{\partial t} = \pi r_\mathrm{V}^2 \frac{\partial r_\mathrm{V}}{\partial t}, \tag{3.92}$$

where r_V is the radius of the void.

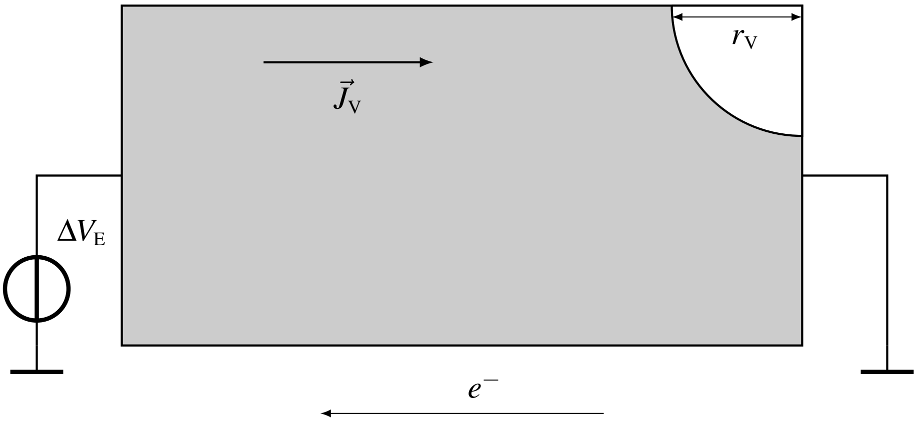


Figure 3.11: Schematic cross section view of a conducting metal line with an initial small void of radius r_V.

Using equations (3.91) and (3.92), the void radius change in time is expressed as

$$\frac{\partial r_\mathrm{V}}{\partial t} = f\Omega_\mathrm{a} A_\mathrm{i} \frac{e|Z^*|D_\mathrm{V} C_\mathrm{V} \rho_\mathrm{E} \|\vec{j}\|}{\pi r_\mathrm{V}^2 k_\mathrm{B} T}. \tag{3.93}$$

The flux of vacancies captured by the void surface strongly depends on the void size, additionally influencing the changes in current density and vacancy concentration distributions around the void itself [45]. Assuming a variable vacancy flux and integrating equation (3.93), the analytical model describing the time t necessary to grow a void with a given radius becomes

$$t = t_0 + \frac{\pi}{\alpha} \int_{r_0}^{r} \frac{r_\mathrm{V}^2}{A_\mathrm{i}(r_\mathrm{V}) C_\mathrm{V}(r_\mathrm{V}) \|\vec{j}(r_\mathrm{V})\|} \mathrm{d}r_\mathrm{V}, \tag{3.94}$$

where

$$\alpha = f\Omega_\mathrm{a} \frac{e|Z^*|D_\mathrm{V} \rho_\mathrm{E}}{k_\mathrm{B} T}, \tag{3.95}$$

and r_0 is the initial void radius corresponding to time t_0.

By following the described modeling approach, an initial spherical void is placed at the location of void nucleation and its radius is increased. The time necessary to grow a void of a given volume can be obtained by performing numerical simulations of the vacancy flux around the void for different void sizes and applying equation (3.94).

3.5 Model Summary

The model equations presented in the chapter are implemented in a TCAD tool (COMSOL Multiphysics® [38]) in order to simulate the electromigration failure phenomenon in realistic 3D interconnect structures. Since electromigration modeling and simulation constitute a multiphysics problem, they can be conveniently separated in several submodels. In the following a brief summary of the general model, with the main model equations which are numerically solved for the simulations, is presented.

Electro-Thermal Model

The distributions of current density $\vec{j}$, electric potential V_{E}, and temperature T in the interconnect line are determined by the solutions of the non-linear system of equations

$$\nabla \cdot \vec{j} = 0, \tag{3.96}$$

$$\nabla^2 V_{\mathrm{E}} = 0, \tag{3.97}$$

$$\nabla^2 T - \frac{\rho_{\mathrm{m}} c_{\mathrm{P}}}{k_{\mathrm{T}}} \frac{\partial T}{\partial t} = -\frac{\sigma_{\mathrm{E}}}{k_{\mathrm{T}}} (\nabla V_{\mathrm{E}})^2, \tag{3.98}$$

as presented in Section 3.1.

Vacancy Dynamics Model

The vacancy transport $\vec{J}_{\mathrm{V}}$, responsible for electromigration failure is induced by different driving forces and is described as follows

$$\vec{J}_{\mathrm{V}} = -D_{\mathrm{V}} \left(\nabla C_{\mathrm{V}} + \frac{C_{\mathrm{V}} |Z^*| e}{k_{\mathrm{B}} T} \nabla V_{\mathrm{E}} + \frac{C_{\mathrm{V}} Q^*}{k_{\mathrm{B}} T^2} \nabla T + \frac{C_{\mathrm{V}} f \Omega_{\mathrm{a}}}{k_{\mathrm{B}} T} \nabla \sigma \right). \tag{3.99}$$

The change of vacancy concentration C_{V} caused by the vacancy flux in the structure is expressed by the continuity equation

$$\frac{\partial C_{\mathrm{V}}}{\partial t} = -\nabla \cdot \vec{J}_{\mathrm{V}} + G. \tag{3.100}$$

The effect of the fast diffusivity path n, which affects the vacancy dynamics inside an interconnect line, is taken into account by setting appropriate diffusion coefficients $D_{\mathrm{V}}^{\mathrm{n}}$ and source/sink terms as follows

$$G^{\mathrm{n}} = \frac{1}{\tau_{\mathrm{V}}^{\mathrm{n}}} \left(C_{\mathrm{V,eq}}^{\mathrm{n}} - C_{\mathrm{V}}^{\mathrm{T}} \left(1 + \frac{\omega_{\mathrm{R}}}{\omega_{\mathrm{T}} C_{\mathrm{V}}} \right) \right). \tag{3.101}$$

By following the model described in Section 3.2, the vacancy concentration distribution in the structure can be determined.

Solid Mechanics Model

It has been shown in Section 3.3 that the mechanical stress σ and displacement $\vec{u}$ distributions in the line are obtained by solving the following system of equations

$$\frac{\partial \varepsilon_{\mathrm{ik}}^{\mathrm{v}}}{\partial t} = \frac{\Omega_{\mathrm{a}}}{3}\left((1-f)\nabla \cdot \vec{J}_{\mathrm{v}} \pm fG\right)\delta_{\mathrm{ik}}, \tag{3.102}$$

$$\sigma_{\mathrm{ik}} = \lambda \delta_{\mathrm{ik}}(\varepsilon_{\mathrm{ll}} - \varepsilon_{\mathrm{ll}}^{\mathrm{th}} - \varepsilon_{\mathrm{ll}}^{\mathrm{v}}) + 2\mu(\varepsilon_{\mathrm{ik}} - \varepsilon_{\mathrm{ik}}^{\mathrm{th}} - \varepsilon_{\mathrm{ik}}^{\mathrm{v}}), \tag{3.103}$$

$$\nabla \cdot \overline{\overline{\sigma}} = 0, \tag{3.104}$$

$$\varepsilon_{\mathrm{ik}} = \frac{1}{2}\left(\frac{\partial u_{\mathrm{i}}}{\partial x_{\mathrm{k}}} + \frac{\partial u_{\mathrm{k}}}{\partial x_{\mathrm{i}}}\right), \tag{3.105}$$

$$\mu \nabla^2 u_{\mathrm{i}} + (\lambda + \mu)\frac{\partial}{\partial x_{\mathrm{i}}}(\nabla \cdot \vec{u}) = B\frac{\partial \mathrm{Tr}(\varepsilon^{\mathrm{th}} + \varepsilon^{\mathrm{v}})}{\partial x_{\mathrm{i}}}. \tag{3.106}$$

From the time evolution of the stress build-up due to electromigration and the accompanying driving forces in the line, the void nucleation condition can be determined. The void nucleates in the structure as soon as the stress reaches the threshold value

$$\sigma_{\mathrm{thr}} = \frac{2\gamma_m \sin\theta_{\mathrm{C}}}{R_{\mathrm{P}}}. \tag{3.107}$$

Void Evolution Model

The diffuse interface model and a semi-empirical model are applied to a structure with an already-nucleated void for the simulation of the electromigration-induced void evolution mechanism, as presented in Section 3.4. The diffuse interface model provides the distribution of the order parameter ϕ in the interconnect by solving the set of equations

$$\frac{\partial \phi}{\partial t} = -\nabla \cdot \vec{J}_{\mathrm{s}}, \tag{3.108}$$

$$\vec{J}_{\mathrm{s}} = -\frac{2D_{\mathrm{s}}(\phi)}{\varepsilon_{\mathrm{di}}\pi}(\nabla \mu_{\mathrm{s}} - e|Z^*|\nabla V_{\mathrm{E}}). \tag{3.109}$$

The development of a semi-empirical model, based on the void size dependence of the incoming flux of vacancies due to electromigration, provides numerical solutions of the time

t needed to grow a void of a given void radius r_V as follows

$$t = t_0 + \frac{\pi}{\alpha}\int_{r_0}^{r} \frac{r_\mathrm{V}^2}{A_\mathrm{i}(r_\mathrm{V})C_\mathrm{V}(r_\mathrm{V})\|\vec{j}(r_\mathrm{V})\|}\mathrm{d}r_\mathrm{V}, \tag{3.110}$$

where

$$\alpha = f\Omega_\mathrm{a}\frac{e|Z^*|D_\mathrm{V}\rho_\mathrm{E}}{k_\mathrm{B}T}. \tag{3.111}$$

The model equations are used to determine the change in the interconnect resistance with time, due to the growing void in the structure. Consequently, the prediction of the interconnect lifetime can be obtained.

Chapter 4

Numerical Implementation with Finite Element Method

The mathematical description of most engineering problems mainly takes the form of integrals or partial differential equations (PDEs) defined on geometrically complicated domains of interest. Depending on the inherent physics of the problem and the corresponding mathematical formulation, numerical solutions to such models can be obtained by employing numerical methods. Finite difference method is the most common numerical technique for solving such mathematical problems. It replaces the PDEs by approximating them with difference equations using grid information [148]. This method requires high accuracy of the solution and it is difficult to implement when the geometry becomes more complex.

Considering the model equations proposed in Chapter 3 and the complicated interconnect structures described in Chapter 1, the finite element method (FEM) constitutes a powerful numerical analysis technique for obtaining approximate solutions to such problems. FEM is based on the discretization of the domain of interest into finite elements and uses variational methods to find an approximate solution within each element by minimizing an associated error function. It can be applied to a wide range of engineering problems and handles complex geometries with different types of boundary conditions.

In the next sections, after a brief introduction to the FEM, a rigorous mathematical analysis for the derivation of an approximate solution for a 1D boundary value problem is described. The mathematical background for the derivation of the FEM equations is provided by referring to several books [85, 88, 116, 123, 125, 148, 161]. Then, the description of the numerical implementation of the governing model equations for electromigration in a FEM-based simulation tool, such as COMSOL Multiphysics®, is presented.

4.1 General Theory of Finite Element Method

4.1.1 Introduction to Finite Element Method

The development of scientific computing has increased the possibilities to efficiently solve specific mathematical and engineering problems through numerical methods implemented in computers by using TCAD [85]. Computer-implemented mathematical models allows one to simulate and analyze complicated systems in order to significantly improve the design and operation of a device or process. The simulation provides access to physical quantities that cannot be measured and strongly supports insight into the physical phenomenon [88]. The purpose of a simulation software is to reduce the number of tests that have to be run during the design and optimization of a device or process.

TCAD mathematical models need numerical methods. Normally, analytical solutions of the model equations can easily be found by making some assumptions in very simple cases. In general, numerical techniques have to be applied for problems with complicated geometries, loadings, and material properties in order to find approximate solutions for PDEs where exact analytical solutions can not be obtained. Numerical methods of analysis transform the PDE governing a physical problem to a set of equations of a discrete model of the problem that has to be solved [125]. Variational methods have been developed for this purpose. They provide simple means of finding approximate solutions to physical problems. The approximate solutions are continuous functions over particular domains and are obtained by a linear combination of basis functions and unknown coefficients. In the solution of a PDE by means of the variational method, the governing equation is transformed into a weighted-integral statement in order to determine the unknown coefficients by minimizing the error introduced in the approximate solution of the PDE.

FEM is a computational technique that makes use of variational methods. Using FEM as a numerical solving procedure is convenient for complex mathematical models in complicated geometrical domains. FEM is a standard numerical technique for solving a wide spectrum of problems which are described by PDEs, defined in a domain of interest, and subjected to specified boundary conditions. The domain is represented as an assembly of finite elements [116]. FEM can handle irregular geometries with different boundary conditions and material behaviors. It is extensively used for solving problems in many areas of science and engineering, such as diffusion processes and solid mechanics, and it is often integrated in CAD tools. Furthermore, its diversity and flexibility as an analysis tool permits its application to multidisciplinary problems, such as the electromigration phenomenon in microelectronic structures which involves electro-thermal-mechanical analysis [148]. FEM can therefore be employed for the implementation of the electromigration model for more complete investigation on different interconnect structures.

4.1.2 Principles of Finite Element Method

The basic idea of FEM is to discretize the domain of interest, where the PDE is defined, in order to obtain an approximate solution of the PDE by a linear combination of basis functions defined within each subdomain. Then, the assembly of subdomains, which is based on the process of putting the finite elements back into their original positions, results in a discrete set of equations which are analogous to the original mathematical problem.

The entire domain under investigation is approximated as an assembly of discrete elements, so-called finite elements, interconnected at points common to two or more elements, so-called nodes, as illustrated in Figure 4.1. Each finite element is an independent geometric region of the domain over which equations with unknown variables of the given problem are defined using the governing equations of the mathematical model of interest.

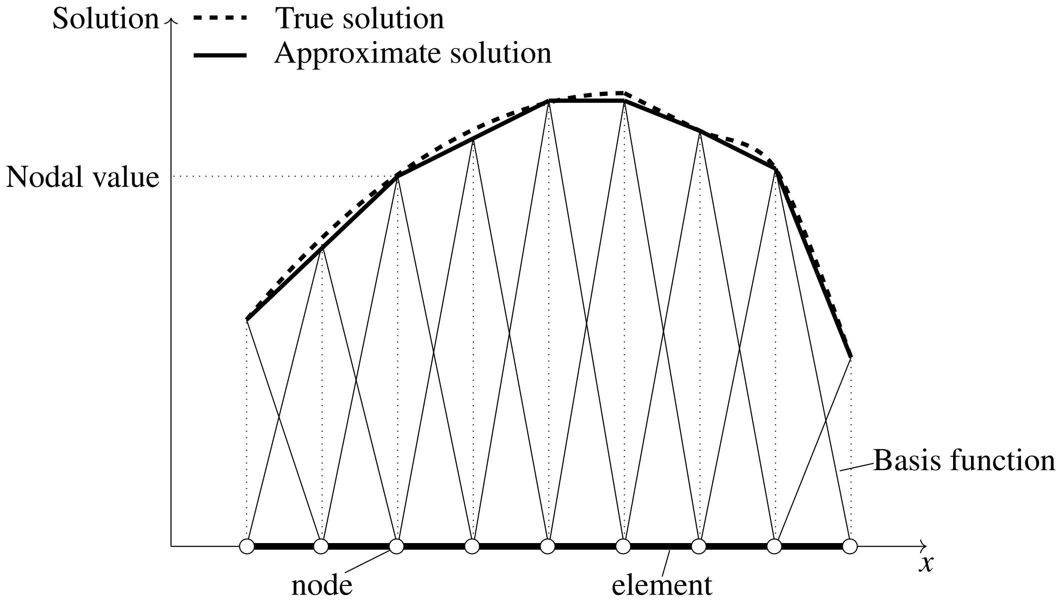


Figure 4.1: Schematic view of the linear discretization of the domain in elements and nodes. The true solution is represented as a continuous function (dotted line) and the approximate solution is described as a piecewise polynomial (solid line).

In each finite element, these equations are solved by assuming basis functions which interpolate the unknown variables over the finite element, in order to approximate the solution of the problem within the element. The basis function is defined within the finite element using the values of the unknown variables at the nodes. The approximate solution to the problem within the element is obtained as a linear combination of nodal values of the variables and the basis functions for the element. The equations for the finite element relate the nodal values of the variables to other parameters. The formulation of the finite element analog of a model equation follows two main approaches, namely weighted-residual and weak formulation [116]. Then, with appropriate loadings, boundary, and initial conditions applied to the elements/nodes, the local element equations for all the finite elements are assembled together and solved simultaneously to obtain a continuous solution in terms of its values at the nodes.

During the finite element analysis, errors can be introduced due to the approximations of the domain discretization, the solutions of the element equations, and the solution of the assembled system of equations. The estimation of these errors is not simple and, therefore, the exact solution of the problem can not be obtained in most of the cases (Figure 4.1).

4.2 Finite Element Analysis for a 1D Problem

In general, the steps involved in the FEM analysis of a typical problem can be summarized as follows [116]:

1. Introduce the mathematical problem defined in a domain;
2. Discretize the domain into finite elements;
3. Derive the element equations over each finite element in the domain;
4. Assemble the element equations to obtain equations for the entire problem;
5. Impose boundary conditions of the problem;
6. Solve the global system of equations.

A step-by-step FEM procedure for the formulation and the solution of a boundary value problem in 1D domain subject to specified boundary conditions is shown in the following subsections.

4.2.1 1D Boundary Value Problem

A physical phenomenon can normally be described by a mathematical problem. Consider a simple elliptic mathematical problem [85] of finding the unknown function $\varphi(x)$ that satisfies the governing differential equation (DE) of the phenomenon

$$-\frac{\mathrm{d}}{\mathrm{d}x}\left(a(x)\frac{\mathrm{d}\varphi}{\mathrm{d}x}\right)+b(x)\varphi=f(x) \quad \text{for} \quad 0<x<L, \tag{4.1}$$

in the one-dimensional domain $\Omega=(0,L)$ subject to a set of boundary conditions at the boundary points $x=0$ and $x=L$ as follows

$$\begin{aligned} \varphi(0)&=0 \quad \text{at} \quad x=0,\\ \left(a(x)\frac{\mathrm{d}\varphi}{\mathrm{d}x}\right)\Bigg|_{x=L}&=\beta_{\mathrm{L}} \quad \text{at} \quad x=L, \end{aligned} \tag{4.2}$$

where x is the independent variable, $a(x)$, $b(x)$ are the material or physical properties of the system, $f(x)$ is a given source function, and β_{L} is the boundary load which is given by the problem. For simplicity, the known functions $a(x)$, $b(x)$, and $f(x)$ will be called a, b, and f. The first boundary condition in equation (4.2), associated with the DE, is commonly called a Dirichlet boundary condition which requires that a solution needs to take a specific value at the boundary of the domain, while the second boundary condition term is the Neumann boundary condition which specifies the value that the derivative of a solution can take at the boundary of the domain.

The mathematical problem described above is stated in its strong form. It consists of the DE governing the system dynamics, the associated boundary conditions, and the initial conditions of the problem.

4.2.2 Discretization of the Domain

The domain $\Omega = (0, L)$ of interest is divided into a collection of finite elements. The set of subintervals in a domain is called the finite element mesh of the domain. The mesh depends on the geometry of the domain and on the desired accuracy of the solution [125]. A linear element Ω_i is located between the nodes k and $k+1$, with coordinates x_k and $x_\mathrm{k+1}$, respectively, with a length $h_\mathrm{i} = x_\mathrm{k+1} - x_\mathrm{k}$. The discretization of the domain allows one to calculate approximate solutions over each subdomain rather than over the entire domain. The solutions on the subdomains are represented by continuous functions at the nodes of these subdomains. In the present 1D case, the discretization of the straight line is obtained by constructing the proper finite element mesh and by defining the elements and the nodes of the domain in order to seek an approximation of the solution to the governing DE over each subdomain. For simplicity, a fine element mesh of two elements (Ω_1 and Ω_2) and three nodes (1, 2, and 3) is proposed, as shown in Figure 4.2.

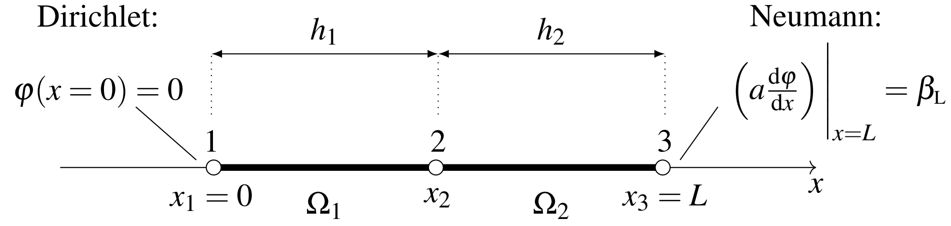


Figure 4.2: Schematic view of the finite element mesh of the domain $\Omega = (0, L)$, with the definition of the boundary conditions at the endpoints.

4.2.3 Derivation of Equations over an Element

The derivation of algebraic equations in a finite element approach associated with the model DE, defined by equations (4.1) and (4.2), over a mesh element involves a three-step approach [125]:

1. Construction of the weak formulation of the DE;
2. Choice of the form of the approximate solution over the finite element;
3. Derivation of the finite element equations in matrix form by substituting the approximate solution into the weak formulation.

In the following, the construction of the algebraic equations over the isolated element Ω_1 with two nodes 1 and 2, whose endpoints have coordinates $x = x_1$ and $x = x_2$, is presented.

Step 1 - Weak Formulation

Different variational methods, such as the Ritz-Galerkin and weighted-residual, provide a background for the development of the algebraic equations over the element [116]. In all these methods, the basic idea is to seek a polynomial approximation φ_{h}^1 of the solution to equation (4.1) within the finite element Ω_1 in the form

$$\varphi_{\mathrm{h}}^1 = \sum_{k=1}^{2} c_{\mathrm{k}}^1 u_{\mathrm{k}}^1(x), \tag{4.3}$$

where c_{k}^1 are the unknown nodal values of the solution $\varphi(x)$ at the nodes of the element Ω_1 and u_{k}^1 are the basis functions over the element. The scope of any variational method is to determine the nodal values c_{k}^1 in order to find an approximate solution φ_{h}^1 that best satisfies the DE at every point of the element Ω_1 of interest. The strong solution to equation (4.1) must be as smooth as required by the DE. In the present case, the solution should be continuously differentiable until at least the second derivative. To avoid such a requirement, the weak formulation of the problem is introduced. The main advantage compared to the strong form is that the weak form lowers the demand on continuity of the solution to only the first derivative.

The construction of the weak formulation of the problem requires one to recast the DE in a weighted-integral form [125]. The weighted-integral statement of the DE is constructed as follows

$$\int_{x_1}^{x_2} w_{\mathrm{j}}(x) R(x, c_{\mathrm{k}}^1) \mathrm{d}x = 0, \quad \text{for} \quad j = 1, 2, ..., n, \tag{4.4}$$

where

$$R(x, c_{\mathrm{k}}^1) = -\frac{\mathrm{d}}{\mathrm{d}x}\left(a \frac{\mathrm{d}\varphi_{\mathrm{h}}^1}{\mathrm{d}x}\right) + b\varphi_{\mathrm{h}}^1 - f. \tag{4.5}$$

$R(x, c_{\mathrm{k}}^1)$ is called residual of approximation of the DE within the element Ω_1 and $w_{\mathrm{j}}(x)$ is the weight function. The integral statement of equation (4.4) allows one to choose n linearly independent functions $w_{\mathrm{j}}(x)$ and obtain a set of n equations for c_{k}^1 by making $R(x, c_{\mathrm{k}}^1)$ equal to zero at the selected points of the element. It therefore requires that the basis function u_{k}^1 be such that the approximate solution φ_{h}^1 is twice differentiable. Note that the weighted-integral statement of (4.4) is equivalent to the DE and does not include any boundary conditions. The boundary conditions will come into play subsequently.

Due to the different choices of the weight function $w_{\mathrm{j}}(x)$ and/or the basis function u_{k}^1, the system of algebraic equations within the element will have different characteristics when different variational methods are used [125]. A general weighted-residual method is a variational method which requires only the weighted-integral statement of the DE to determine the nodal values c_{k}^1 of the approximation. The weight functions $w_{\mathrm{j}}(x)$ can be chosen from an independent set of functions, but are required to be linearly independent, otherwise the set of n equations for c_{k}^1 will not be solvable due to the underdetermination of the system of equations [88]. The Ritz-Galerkin method is a weighted-residual method which uses a set of weight functions $w_\mathrm{j}(x)$ equal to the set of basis functions u_k^1 such that the weighted-integral statement (4.4) reduces to

$$\int_{x_1}^{x_2} u_\mathrm{j}(x)\left[-\frac{\mathrm{d}}{\mathrm{d}x}\left(a\frac{\mathrm{d}\varphi_\mathrm{h}^1}{\mathrm{d}x}\right)+b\varphi_\mathrm{h}^1-f\right]\mathrm{d}x=0, \quad \text{for} \quad j=1,2,...,n. \tag{4.6}$$

The weighted-residual approach provides residual minimization by integrating over the element. Using the integration by parts [148], the order of differentiation in φ_h^1 is reduced as follows

$$\int_{x_1}^{x_2}\left(a\frac{\mathrm{d}u_\mathrm{j}(x)}{\mathrm{d}x}\frac{\mathrm{d}\varphi_\mathrm{h}^1}{\mathrm{d}x}+bu_\mathrm{j}(x)\varphi_\mathrm{h}^1\right)\mathrm{d}x=\int_{x_1}^{x_2}u_\mathrm{j}(x)f\mathrm{d}x+\left[au_\mathrm{j}(x)\frac{\mathrm{d}\varphi_\mathrm{h}^1}{\mathrm{d}x}\right]_{x_1}^{x_2}. \tag{4.7}$$

In this way, it is necessary that the basis functions u_k^1 be such that the approximate solution φ_h^1 is only once-differentiable, and not twice differentiable as in equation (4.6). Equation (4.7) represents the weak formulation of the problem. The term "weak" refers to the reduced or weakened continuity of u_k^1 such that φ_h^1 is differentiable as many times as called for the original DE in the weighted-integral statement [125].

Step 2 - Approximate Solution

The approximate solution φ_h^1 within the finite element Ω_1 must be found in a way that the approximate solution of the problem φ_h is convergent to the actual solution φ as the number of elements increase. For this purpose it is required to satisfy the following conditions [125]:

- Continuous over the element and differentiable, in order to ensure a regular coefficient matrix;
- Complete polynomial which includes all lower-order terms;
- Equal at both sides of each element node, so that the continuity of the solution is enforced when approximate solutions from each element are connected;
- Satisfy all the boundary conditions of the problem.

Consider the element Ω_1 composed of two nodes at x_1 and x_2, as depicted in Figure 4.3. Since only the first derivatives of φ_h^1 are involved in equation (4.7), the solution φ_h^1 within the element Ω_1 is approximated using a linear polynomial as follows

$$\varphi_\mathrm{h}^1(x)=g_1^1+g_2^1x \qquad x_1\leq x\leq x_2, \tag{4.8}$$

where g_1^1 and g_2^1 are unknown coefficients. The expression (4.8) fulfills the first two conditions of an approximation described above. The third condition is satisfied if the unknown coefficients g_1^1 and g_2^1 are expressed in terms of nodal values of the solution $\varphi_1^1(x_1)$ and

$\varphi_2^1(x_2)$. The nodal values are given by

$$\begin{aligned} \varphi_1^1(x_1) &= c_1^1 = g_1^1 + g_2^1 x_1, \\ \varphi_2^1(x_2) &= c_2^1 = g_1^1 + g_2^1 x_2. \end{aligned} \tag{4.9}$$

By solving the system of equations (4.9) and using $h_1 = x_2 - x_1$, the unknown coefficients can be obtained as follows

$$g_1^1 = \frac{c_1^1 x_2 - c_2^1 x_1}{h_1}, \qquad g_2^1 = \frac{c_2^1 - c_1^1}{h_1}. \tag{4.10}$$

The substitution of equations (4.10) into equation (4.8) permits one to approximate the solution within the element as follows

$$\begin{aligned} \varphi_{\mathrm{h}}^1(x) &= \frac{c_1^1 x_2 - c_2^1 x_1}{h_1} + \frac{c_2^1 - c_1^1}{h_1} x = \frac{x_2 - x}{h_1} c_1^1 + \frac{x - x_1}{h_1} c_2^1 = \\ &= u_1^1(x) c_1^1 + u_2^1(x) c_2^1 = \sum_{k=1}^{2} u_{\mathrm{k}}^1(x) c_{\mathrm{k}}^1, \end{aligned} \tag{4.11}$$

where $u_1^1(x)$ and $u_2^1(x)$ are the basis functions or interpolation functions [116].

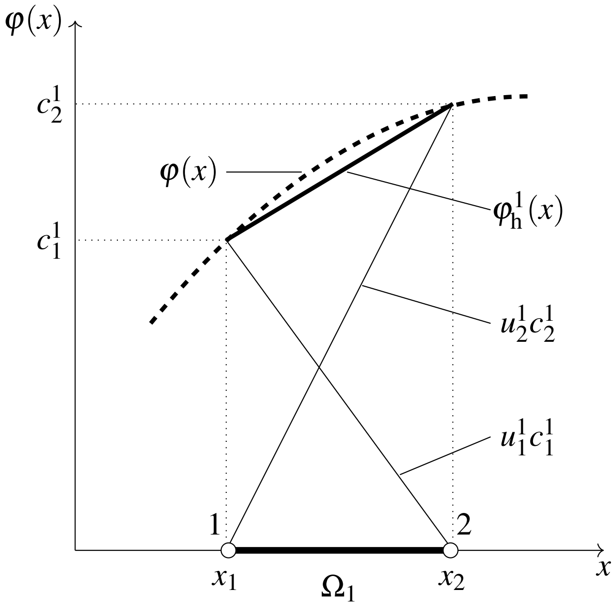


Figure 4.3: Schematic view of the linear finite element approximation. The true solution $\varphi(x)$ (dotted line) and the construction of the approximate solution $\varphi_{\mathrm{h}}^1(x)$ (solid line), within the element Ω_1, are presented.

The interpolation property of these functions requires that $u_{\mathrm{k}}^1(x)$ is unity at the k^{th} node and zero at the other node of the given element. Another property of the interpolation functions is that their sum is unity ($\sum_{k=1}^{n} u_{\mathrm{k}}^1(x) = 1$). In this way, the solution $\varphi_{\mathrm{h}}^1(x)$ is interpolated using its nodal values c_1^1 and c_2^1, is approximated by a piecewise linear polynomial, and its gradient is constant within the element. The geometric representation of the approximate solution inside the element Ω_1 is shown in Figure 4.3.

Step 3 - Ritz-Galerkin Method

Once the form of the approximate solution φ_{h}^1 within the element Ω_1 is known, the application of the Ritz-Galerkin method allows one to derive the set of algebraic equations over the finite element. The substitution of equation (4.11) into equation (4.7) will give the set of equations among the nodal values of the element as follows

$$\sum_{k=1}^{2}\left[\int_{x_1}^{x_2}\left(a\frac{\mathrm{d}u_{\mathrm{j}}(x)}{\mathrm{d}x}\frac{\mathrm{d}u_{\mathrm{k}}^1}{\mathrm{d}x}+bu_{\mathrm{j}}(x)u_{\mathrm{k}}^1\right)\mathrm{d}x\right]c_{\mathrm{k}}^1=\int_{x_1}^{x_2}u_{\mathrm{j}}(x)f\mathrm{d}x+\sum_{k=1}^{2}u_{\mathrm{j}}(x_{\mathrm{k}})\beta_{\mathrm{k}}^1, \tag{4.12}$$

where

$$\beta_{\mathrm{k}}^1=\left(a\frac{\mathrm{d}u_{\mathrm{k}}^1}{\mathrm{d}x}\right)\Bigg|_{x=x_{\mathrm{k}}} \tag{4.13}$$

are the unknown source terms. Usually, such a relation for the finite element Ω_1 is presented as a matrix equation [161] of the form

$$[K^1]\{c^1\}=\{f^1\}+\{\beta^1\}, \tag{4.14}$$

where

$$[K^1]=\int_{x_1}^{x_2}\left(a\frac{\mathrm{d}u_{\mathrm{j}}(x)}{\mathrm{d}x}\frac{\mathrm{d}u_{\mathrm{k}}^1}{\mathrm{d}x}+bu_{\mathrm{j}}(x)u_{\mathrm{k}}^1\right)\mathrm{d}x, \tag{4.15}$$

$$\{f^1\}=\int_{x_1}^{x_2}u_{\mathrm{j}}(x)fdx, \tag{4.16}$$

and

$$\{\beta^1\}=\sum_{k=1}^{2}u_{\mathrm{j}}(x_{\mathrm{k}})\beta_{\mathrm{k}}^1. \tag{4.17}$$

The matrix $[K^1]$, which is called coefficient matrix, and the vector $\{f^1\}$, which is the source vector, can be determined for the given element and known functions a, b, and f. The relation (4.14) provides two equations for the finite element used to determine four unknowns: $c_1^1, c_2^1, \beta_1^1, \beta_2^1$. For a linear element, the matrix form is written as follows

$$\begin{bmatrix}K_{11}^1 & K_{12}^1\\ K_{21}^1 & K_{22}^1\end{bmatrix}\begin{Bmatrix}c_1^1\\ c_2^1\end{Bmatrix}=\begin{Bmatrix}f_1^1\\ f_2^1\end{Bmatrix}+\begin{Bmatrix}\beta_1^1\\ \beta_2^1\end{Bmatrix}, \tag{4.18}$$

where the coefficients of the matrix (K_{jk}^1) and the source vector (f_{j}^1) can be easily evaluated for the given element from equations (4.15) and (4.16), respectively, by using the values of the constants a, b, and f.

4.2.4 Assembly of Elements

Equation (4.14) can not be solved without using the equations from other finite elements [125]. The assembling of elements is a method to obtain the equations for the complete set of elements of the total problem [161]. The connectivity of elements provides the finite element equations of the total problem by putting the elements back into their original position in order to get rid of the extra unknowns [125]. For this purpose, the procedure requires that the solution is continuous and the unknown source terms β_{k}^{i} are balanced at nodes common to several elements where they are connected to each other.

Consider the simple case of two linear elements Ω_1 and Ω_2 connected at the node 2, as shown in Figure 4.4. For a mesh of linear finite elements, the continuity of the solution requires that node 2 of the element Ω_1 is connected to node 1 of the element Ω_2 such that $c_2^1 = c_1^2 = c_2$, where c_2 is the unknown nodal value at the common nodal point. For the same mesh of elements, the balance of the unknown source terms β_{k}^{i} at connecting nodes requires that

$$\beta_2^1 + \beta_1^2 = \begin{cases} 0 & \text{if no external source is applied,} \\ \beta_{\mathrm{F}} & \text{if an external source is applied,} \end{cases} \tag{4.19}$$

where β_{F} is the magnitude of the external applied source.

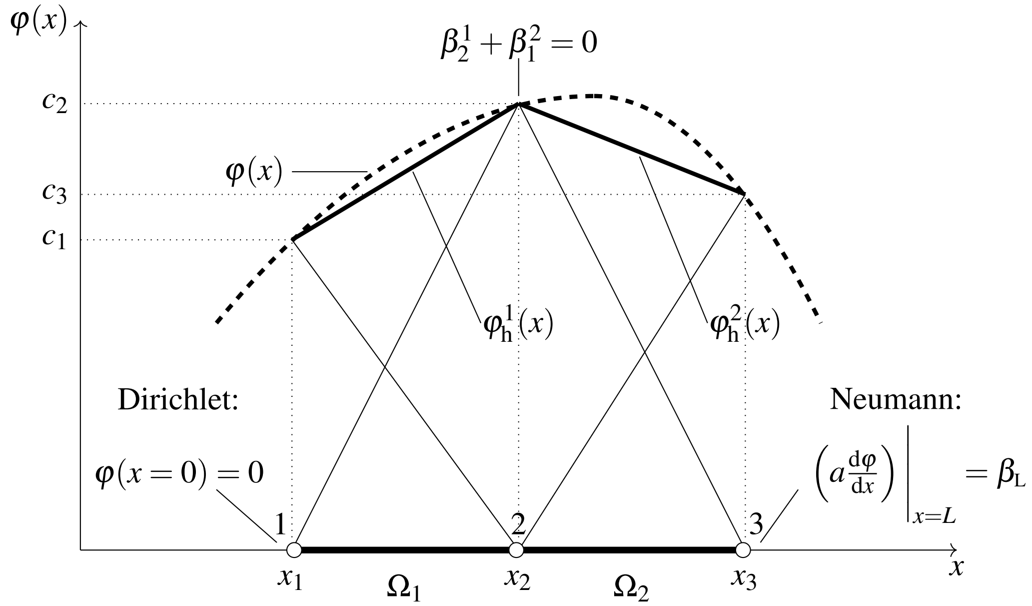


Figure 4.4: Schematic view of the assembly of two linear elements Ω_1 and Ω_2. The definition of the boundary conditions at the endpoints, the balance of the unknown source terms, and the continuity of the solution at node 2 are presented.

Considering the case of two linear elements and adopting relation (4.14), the matrix form for the algebraic equations of the elements Ω_1 and Ω_2 are

$$\begin{bmatrix} K_{11}^1 & K_{12}^1 \\ K_{21}^1 & K_{22}^1 \end{bmatrix} \begin{Bmatrix} c_1^1 \\ c_2^1 \end{Bmatrix} = \begin{Bmatrix} f_1^1 \\ f_2^1 \end{Bmatrix} + \begin{Bmatrix} \beta_1^1 \\ \beta_2^1 \end{Bmatrix}, \tag{4.20}$$

and

$$\begin{bmatrix} K_{11}^2 & K_{12}^2 \\ K_{21}^2 & K_{22}^2 \end{bmatrix} \begin{Bmatrix} c_1^2 \\ c_2^2 \end{Bmatrix} = \begin{Bmatrix} f_1^2 \\ f_2^2 \end{Bmatrix} + \begin{Bmatrix} \beta_1^2 \\ \beta_2^2 \end{Bmatrix}, \tag{4.21}$$

respectively. For a mesh of two linear finite elements connected in series, the interelement continuity of the solution requires that

$$c_1^1 = c_1, c_2^1 = c_1^2 = c_2, c_2^2 = c_3, \tag{4.22}$$

and the balance of the unknown source terms at the global points, in this case only node 2, is interpreted as follows

$$\beta_2^1 + \beta_1^2 = 0. \tag{4.23}$$

The second equation of the matrix (4.20) for the element Ω_1 must be added to the first equation of the matrix (4.21) for the element Ω_2, in order to reduce the number of equations from $2N$ to $N+1$ in a mesh of N linear elements. In terms of the global nodal values, the sum of equation (4.20) and equation (4.21) results in the assembled global equation system for the domain with two elements and three nodes as follows

$$\begin{bmatrix} K_{11}^1 & K_{12}^1 & 0 \\ K_{21}^1 & K_{22}^1 + K_{11}^2 & K_{12}^2 \\ 0 & K_{21}^2 & K_{22}^2 \end{bmatrix} \begin{Bmatrix} c_1 \\ c_2 \\ c_3 \end{Bmatrix} = \begin{Bmatrix} f_1^1 \\ f_2^1 + f_1^2 \\ f_2^2 \end{Bmatrix} + \begin{Bmatrix} \beta_1^1 \\ 0 \\ \beta_2^2 \end{Bmatrix}. \tag{4.24}$$

These are called assembled equations, which contain the sum of coefficients and source terms at the global point to two elements. The assembly matrix contains three equations in five unknowns: $c_1, c_2, c_3, \beta_1^1, \beta_2^2$.

4.2.5 Imposition of the Boundary Conditions

The set of boundary conditions at the boundary points $x = 0$ and $x = L$, presented in equation (4.2), can be imposed on the assembled set of finite element equations (4.24), as depicted in Figure 4.4. The Dirichlet boundary condition ($\varphi(x = 0) = 0$) implies that $c_1 = 0$, while the Neumann boundary condition requires that

$$\left. \left(a \frac{\mathrm{d}u_2^2}{\mathrm{d}x} \right) \right|_{x=x_3} = \beta_\mathrm{L} \quad \text{at} \quad x_3 = L. \tag{4.25}$$

The application of the boundary conditions of the problem on the assembled set of equations reduces equation (4.24) to

$$\begin{bmatrix} K_{22}^{1}+K_{11}^{2} & K_{12}^{2} \\ K_{21}^{2} & K_{22}^{2} \end{bmatrix} \begin{Bmatrix} c_2 \\ c_3 \end{Bmatrix} = \begin{Bmatrix} f_2^1+f_1^2 \\ f_2^2 \end{Bmatrix} + \begin{Bmatrix} 0 \\ \beta_{\mathrm{L}} \end{Bmatrix}. \tag{4.26}$$

In this way, the assembled matrix contains two equations in two unknowns c_2 and c_3, which are the nodal values of the solution.

4.2.6 Solution of the Linear Equations System

The nodal values can be determined by solving the system of equations (4.26). Once they are known, they can be substituted in the finite element approximation φ_{h}^{i} within each element (equation (4.3)) in order to determine an appropriate approximate solution that best satisfies the original DE in the domain of interest. The linear system of equations (4.26) has only two unknowns and can easily be solved. In general, matrices have thousands of unknowns and finding the solution of such a system of linear equations constitutes the most computationally demanding part of FEM. In general, a linear system of N equations with N unknowns, c_{N}, can be written in matrix notation [148] as

$$[K]\{c\} = \{f\} + \{\beta\} = \{L\}, \tag{4.27}$$

where $\{L\}$ is the load vector. The solution of the global matrix equations computes the unknowns as follows

$$\{c\} = [K]^{-1}\{L\}. \tag{4.28}$$

There are two fundamental classes of algorithms which are employed to solve equation (4.28), namely iterative method and direct method. An iterative method, such as the Jacobi method, generates a sequence of approximate solutions of the problem and uses a given initial approximation to generate the successive ones. It therefore approaches the solution gradually until the sequence of approximations converges for the given initial approximate solution. A direct method, such as Gaussian elimination, provides the exact solution of the problem by a finite number of operations. It typically uses more memory than the iterative solvers.

4.3 Simulation Implementation in COMSOL Multiphysics®

The procedure to perform a finite element analysis presented in Section 4.2 is not straight forward, because it requires a strong comprehension of both the theory and mathematics behind of the FEM. Furthermore, the extension of the finite element analysis to 2D and 3D modeling makes the FEM procedure even more complicated.

Due to the prevalence of advanced computer hardware and software, performing a finite element analysis is accessible even for users without much knowledge of the FEM [148]. Powerful hardware provides analysis for complicated structure and/or physical phenomena as well as faster calculations. The rapid development of commercial FEM softwares enables users to perform finite element analysis by hiding the finite element formulation of the problem of interest. The FEM procedure is hidden in the commercial software, which provides only the results of the analysis. In this way, it is possible to focus on the structure, material properties, physics, and boundary conditions under analysis.

COMSOL Multiphysics® [38] is a commercial finite element analysis software for modeling and simulating a wide spectrum of FEM-based physical problems, especially coupled phenomena, in the engineering field, including automotive and electronics. It has a user-friendly multiple windows interface incorporating geometry generation, physics model, meshing, solver, and post-processing. COMSOL Multiphysics® has the capability to solve coupled multiphysics problems, such as electro-thermal and thermo-mechanical phenomena. Its library of physics models is really huge and it can be useful for different analysis and applications. However, where a preset physics model is not available, it is possible to create new physics model interfaces by directly implementing the physical governing PDEs of the problem of interest for setting up simulations from first principles.

4.3.1 Finite Element Method Procedure in COMSOL Multiphysics®

The application of FEM for the modeling and simulation of different physical phenomena in interconnect structures by using COMSOL Multiphysics® is discussed here. The finite element analysis in COMSOL Multiphysics® is performed by following a procedural flow, as depicted in Figure 4.5.

The method can be split into three basic steps, namely pre-processing, solver, and post-processing [38]. The pre-processing step enables the user to build the model. Since it contains all the information regarding the FEM application for interconnect study, it is convenient to divide it into smaller sub-steps. The first sub-step involves the creation of the interconnect geometry (1D, 2D, or 3D), to represent the domain under study, and assign the material properties to the domain. Then, the physical environments of the problem under investigation are generated by assigning the underlying physics (or multiphysics), mathematical equations, and finite element formulation to the model. Typically, the latter is hidden among the core of the commercial software. After that, the application of appropriate loadings, boundary and initial conditions to the domain under study, as well as its discretization into finite elements, determines the matrix equation governing the model, in a similar form of the one presented in equation (4.27).

This step is followed by solving the set of algebraic equations, which provides the physics-related nodal solutions of the model. COMSOL Multiphysics® mainly employs two methods to obtain the model solution, namely segregated step method and fully coupled method. The segregated step method generates the set of algebraic equations for every physical model under consideration and calculates the resulting solutions for each of those models by following a sequence specified by the user. The fully coupled method generates the single set of algebraic equations for all the involved physical models and implements them in a single iteration scheme which is repeated until convergence is reached.

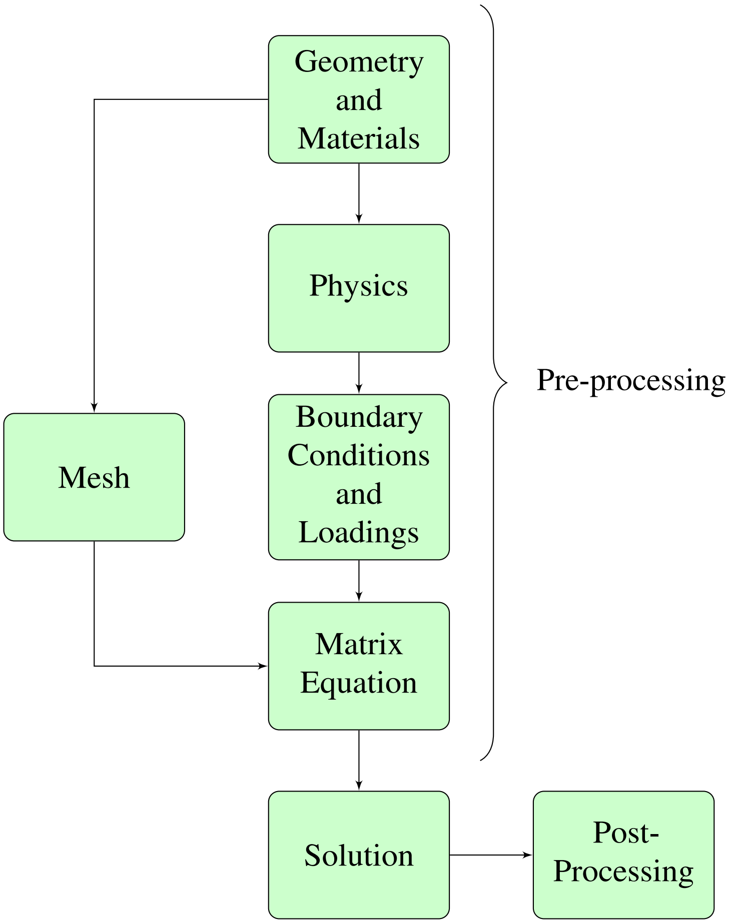


Figure 4.5: Basic steps to perform a finite element analysis in COMSOL Multiphysics®.

Once the solutions of the problems are determined, the post-processing step enables the user to evaluate the results of the finite element analysis by means of plotting and data exporting tools.

4.3.2 Finite Element Analysis for Electromigration Study

Electromigration is a complex physical phenomenon governed by various PDEs and involves an electro-thermo-mechanical analysis. The models presented in Chapter 3 describe the electromigation phenomenon well and show its peculiarity to be a multiphysics problem. The solutions of these models cannot be easily obtained by employing analytical approaches because of the different physical effects related to electromigration. Furthermore, the impact of complex interconnect structures and constraints imposed by the surrounding layers on the derivation of analytical solutions does not produce proper results. For this purpose, FEM can be adopted to obtain numerical solutions of the problem. In particular, a FEM-based software, such as COMSOL Multiphysics® [38], is able to solve the coupled-field analysis and handle complicated 2D and 3D geometries.

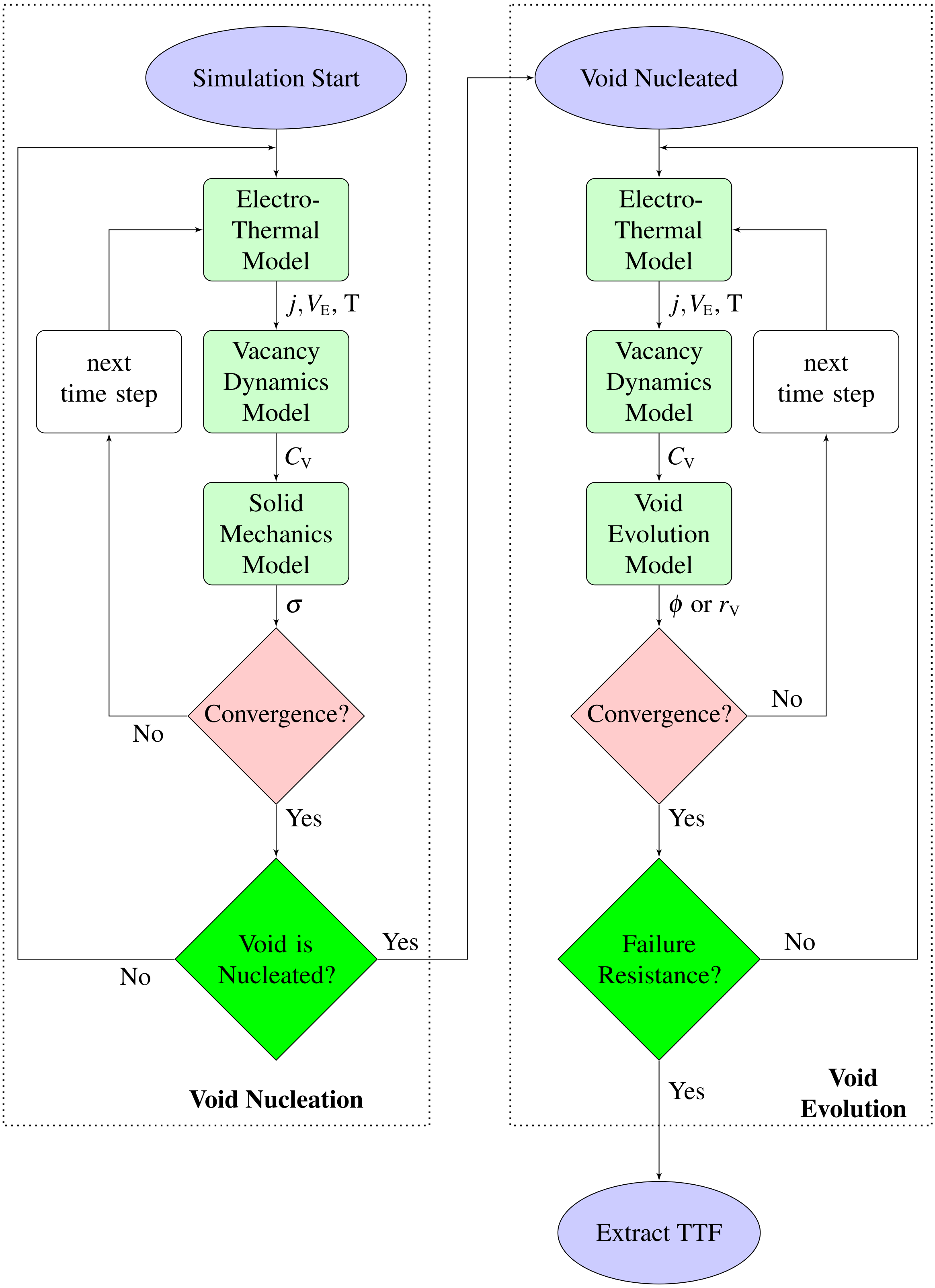


Figure 4.6: Flow chart of the full procedure for electromigration simulation in COMSOL Multiphysics®. The two phases of the electromigration problem, void nucleation and void evolution, are presented.

As described in Chapter 1, electromigration induced failure is typically divided in two phases, namely, the early mode of void nucleation and the late mode of void evolution. During the first mode, voids can nucleate at some locations in the interconnect due to stress. This phase lasts until a stable void is nucleated. The time for a void to nucleate is called void nucleation time. The nucleation of a void is the beginning of the late mode, which is governed by the void evolution mechanism. During this phase, the propagation of the void across the interconnect width causes extremely high changes in the interconnect resistance. A morphological change of the void surface at a constant void volume leads to a rapid, non-linear increase in the electrical resistance of the interconnect. The interconnect fails after a maximum tolerable resistance level is reached. The time needed to achieve this maximum resistance is called void evolution time.

Since different physical effects are responsible for each phase of failure development, modeling and simulating electromigration by using FEM-based numerical calculations constitutes a multiphysics analysis which can be divided into the void nucleation phase and the void evolution phase, as depicted in the scheme presented in Figure 4.6. In this way, the complete electromigration time-to-failure (TTF) estimation is obtained by summing the void nucleation time and the void evolution time. The contribution of each component in the electromigration lifetime evaluation depends on different kinetic and physical effects. The modeling of each phase of failure development is necessary for a more precise lifetime prediction and for a better understanding of their impact on the electromigration failure mechanism.

Void Nucleation

Simulations start with solving the electro-thermal model presented in Section 3.1 in order to obtain the current density $\vec{j}$, electric potential V_E, and temperature T distributions in the interconnect from equations (3.3), (3.5), and (3.13), respectively. Then, the vacancy dynamics model, described in Section 3.2, has to be solved in order to determine the distribution of vacancy concentration C_V in the structure. This step is important because it solves the vacancy balance equation (3.26) which takes into account all the various driving forces for vacancy transport (equation (3.24)). The vacancy dynamics problem is followed by the solution of the system of equations (3.58) - (3.70) of the solid mechanics model to obtain the stress σ distribution due to electromigration in the interconnect, as presented in Section 3.3. The simulation continues until the threshold stress for void nucleation is reached at some location in the interconnect. Reaching the threshold stress (equation (3.72)) implies void nucleation and the beginning of the second phase of failure development at this location.

Void Evolution

Once the void is formed, the void evolution phase begins. In a typical simulation procedure for void evolution, it is convenient to assume an initial small void located at the site of void nucleation. Since the void locally changes the electric current density and vacancy concentration distributions around itself, the electro-thermal and vacancy dynamics analysis have to again be carried out before the evolution is tracked. Then, the void evolution model has to be solved. Depending on the numerical approach, this step of the procedure can be performed in different ways. In Section 3.4, two methodologies are adopted for simulating void evolution in interconnects:

- Diffuse interface model: it employs a particular FEM-based numerical scheme which computes the evolution of the order parameter ϕ (equation (3.82)) together with the solutions of the electro-thermal and vacancy dynamics problems, as presented in Section 3.4.2. The parameter $\varepsilon_{\mathrm{di}}$ controlling the interface thickness in equation (3.82) has to be chosen so as to be sufficiently small to ensure that the diffuse interface model provides a suitable approximation to the sharp interface model, described in Section 3.4.1. In fact, in the limit of vanishing interface thickness, the two models exhibit matching physical behavior [107]. In general, small values of $\varepsilon_{\mathrm{di}}$ require short time steps and a fine finite element mesh in the computation of the order parameter field. In turn, the electric potential, temperature, and vacancy concentration fields must only be computed throughout the entire interconnect and do not vary within the void surface as rapidly as the order parameter. They may therefore be interpolated with a coarser mesh. The fine mesh density employed for the order parameter field computation is obtained by a regular refinement method of the coarser mesh used for the solutions of the electro-thermal and vacancy dynamics problems, as depicted in Figure 4.7. Since the accuracy of the solution of the problem that can be obtained from a finite element analysis depends on the element size, as these elements are made smaller and smaller, the error between the exact solution and the approximation is minimized.

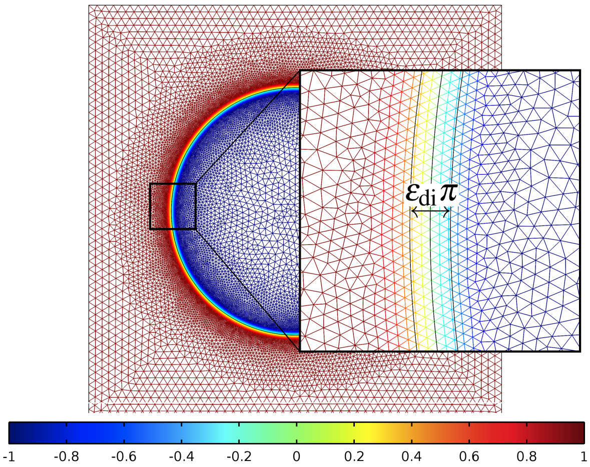


Figure 4.7: Order parameter distribution in an interconnect line. Different mesh densities employed in the numerical calculations are shown. The coarse mesh density used to calculate the voltage distribution through the bulk is refined for the computation of the order parameter along the metal-void interface. The inset zoom shows the details of the mesh density at the interface thickness.

- Semi-empirical method: in contrast to the diffuse interface model, this approach, presented in Section 3.4.3, involves approximations in the physical theory in order to simplify the numerical calculation. In this case, the method is based on the assumption that the radius r_V of the initial small void is increased for each time step in equation (3.93). Performing numerical simulations of the vacancy flux around the void as a function of void size, it is possible to obtain the time necessary to grow a void of a given radius from equation (3.94).

During the simulated void evolution, the resistance of the interconnect can be monitored at each time step. The void evolution procedure is repeated continuously until the resistance of the interconnect increases to a given threshold value which represents the failure criterion. Typically, interconnect failure occurs when a resistance increase of 20% is reached. Subsequently, the lifetime of the interconnect is determined as the time necessary to achieve the maximum tolerable resistance value.

Chapter 5

Case Studies of Electromigration in Interconnects

The full electromigration model described in Chapter 3 and the simulation procedure presented in Chapter 4 are employed in order to investigate electromigration failure in three different cases of significant technological interest. The first two cases are related to the reliability assessment of interconnects in 3D integration systems, including a copper-lined open through silicon via (TSV) and a solder bump. The investigations are focused on the identification of the locations in such interconnect structures, where electromigration has the highest probability to lead to the development of failure. These analyses enable to estimate the lifetimes of the interconnects, which are compared to Black's equation in order to determine the most dominant mechanism in electromigration failure. The third case is related to the influence of current crowding and the role of the microstructure of a simple interconnect line on the prediction of the electromigration lifetime.

5.1 Electromigration Failure in Open TSVs

Open TSV structures are composed of different materials and their design comprises various corners and material interfaces. These regions of the interconnect structure represent potential technology weaknesses which break the homogeneity of the current flow and promote electromigration failure. The electromigration wear-out failure mechanism is normally examined by considering an initial nucleation of the void and its subsequent growth, which triggers an open circuit type of failure. Voids nucleate in the interconnect due to the development of tensile stress, particularly at those locations, where the adhesion between the metal layer and the surrounding material is weak [63]. Once the void has nucleated, the void evolution mechanism leads to a rapid increase in the interconnect resistance eventually resulting in an open circuit failure. After the maximum tolerable resistance level is exceeded, the interconnect is deemed to fail. The time-to-failure (TTF) of the interconnect is defined as the time required to reach the threshold resistance.

It is convenient to analyze the electromigration problem in the open TSV structure by treating the two phases of failure, namely the early phase of void nucleation and the late phase of void evolution, separately, as discussed in previous chapters.

5.1.1 TSV Design and Simulation Parameters

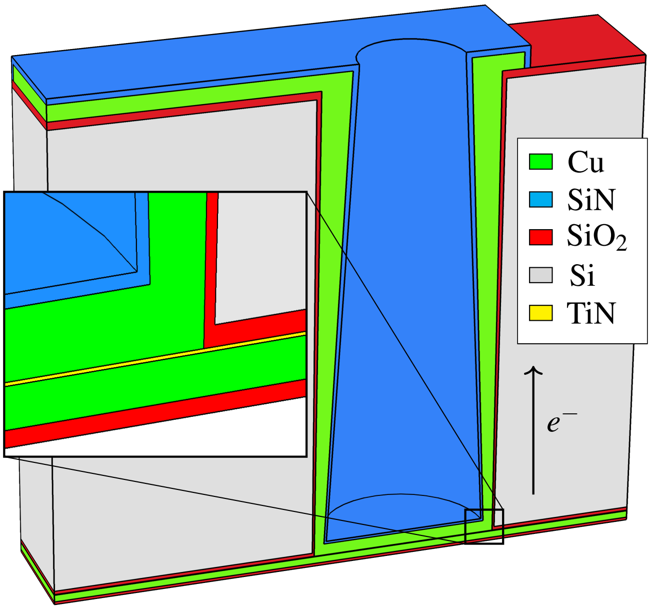


Figure 5.1: Diagonal cut-through profile view of the analyzed open copper TSV structure. The upper part of the interconnect layout is known as TSV top while the lower side is the TSV bottom. The TSV aspect ratio is 2.5:1 (TSV height / TSV diameter). The zoomed-in detail view of the TSV bottom depicts the front side layers stack. The arrow shows the direction of the electron flow.

A schematic overview of the 3D integrated technology using a TSV including the front side rerouting layer and the back side redistribution layer (RDL) is shown in Figure 5.1. In general, the upper part of the structure is referred to as the TSV top while the lower part is the TSV bottom. It is normally considered that the TSV top is where the TSV comes out to the back side thick copper RDL, and the TSV bottom is the part of the TSV in contact with the front side rerouting layer. The TSV aspect ratio considered in our study is 2.5:1 (TSV height / TSV diameter). The TSV top is opened with a silicon etch process, followed by the deposition of a silicon dioxide insulation layer. The subsequent barrier layer (titanium nitride), metallization (copper) and passivation (silicon nitride) are deposited on the TSV surfaces using electrodeposition and PECVD (plasma enhanced chemical vapor deposition), respectively. Below the TSV (see the zoomed-in detail view in Figure 5.1) the front side layers stack (TiN/Cu/SiO_2) is formed. In turn, on the top, the copper backside RDL is placed and passivated. The back side RDL will by convention be the side on which a solder bump is mounted to connect the other wafers.

The set of materials parameters, used by the models discussed in Chapter 3, are presented in Table 5.1 and Table 5.2 and are chosen from recent literature. Since the electromigration phenomenon occurs in the conducting lines and copper has higher sensitivity to electromigration, when compared to other conductors used in the given TSV structure, the parameters related to vacancy dynamics and the void evolution models are listed only for copper.

Table 5.1: Materials parameters for the electro-thermal and solid mechanics models [38, 40].

Model	Parameter	Cu	SiN	SiO_2	Si	TiN
Electro-thermal	$\sigma_{E,0}$ [$S{\cdot}m^{-1}$]	$5.35{\cdot}10^{7}$	0	0	6.67	$2.91{\cdot}10^{5}$
	$k_{T,0}$ [$W{\cdot}(m{\cdot}K)^{-1}$]	379	20	1.4	130	-
	α_E [K^{-1}]	$4.3{\cdot}10^{-3}$	0	-	-	-
	α_T [K^{-1}]	0	0	-	-	-
	β_E [K^{-2}]	0	0	-	-	-
	β_T [K^{-2}]	0	0	-	-	-
	ρ_m [$Kg{\cdot}m^{-3}$]	8920	3100	2200	2200	5430
	c_P [$J{\cdot}(Kg{\cdot}K)^{-1}$]	385	700	730	700	601.71
Solid mechanics	E [GPa]	130	120	72	170	600
	ν	0.35	0.24	0.18	0.28	0.25
	α_{th} [$10^{-6}K^{-1}$]	16.5	2	0.55	2.6	0

Table 5.2: Materials parameters for the vacancy dynamics and diffuse interface models [40].

Model	Parameter	Cu
Vacancy Dynamics	$D_{V,0}$ [$cm^2{\cdot}s^{-1}$]	0.52
	E_a [eV]	0.89
	Z^*	-5
	Q^* [J]	$1.2{\cdot}10^{-20}$
	f	0.4
	Ω_a [cm^3]	$1.18{\cdot}10^{-23}$
	$C_{V,0}$ [cm^{-3}]	$1{\cdot}10^{16}$
	τ_V [s]	1
Diffuse Interface	γ_s [N/m]	1.65
	ε_{di} [m]	$2{\cdot}10^{-9}$
	D_s [$cm^2{\cdot}s^{-1}$]	$0.52{\cdot}10^{5}$
	δ_s [m]	$2{\cdot}10^{-9}$

Once the geometry has been imported into the FEM simulator and meshed, the simulation procedure described in Section 4.3.2 is applied to the open copper TSV structure in order to analyze the electromigration failure mechanism. The operating conditions for electromigration simulations are set by imposing boundary conditions over appropriate regions of the studied geometry. All external surfaces of the structure are assumed to be under isothermal conditions ($T_0 = 473\text{K}$). The outer materials surrounding the copper lines are taken to be rigid while the inner surface of the TSV (silicon nitride layer) is free to move. For the electrical loading, the left side of the copper at the TSV top is maintained at a current density of $j_0 = 1\text{MA/cm}^2$ and the right side of the copper rerouting layer under the TSV bottom is set as the ground contact.

The final goals of the analysis are to estimate the interconnect lifetime and determine the most dominant mode of failure in the open TSV by extrapolating the current density exponent n from equation (1.2). For this purpose, the analysis requires data from several simulations of the interconnect structure at different current density conditions.

5.1.2 Void Nucleation Analysis

In open TSV technologies, the fabrication process induces imperfections and the severe mismatch of geometric features between metallic layers at the TSV bottom can lead to the nucleation of a small void under the TSV, initiating the electromigration failure mechanism. Voids nucleate especially at those locations in the structure where the adhesion between the copper line and the surrounding layer is weak. These sites are generally observed close to the metallization barrier between the TSV and the adjacent metal film [61]. The identification of void nucleation sites in a typical passivated metal line is related to the primary material transport path along which electromigration acts, namely the fast diffusivity path, which is recognized to be the surface of the nucleated void close to the metal/barrier interface [40]. Consequently, material interfaces, in addition to the void surface, play a key role when it comes to understanding the mechanism by which electromigration failure progresses in interconnects.

Vacancy Accumulation at the TSV Bottom

The copper film in the TSV structure is surrounded by titanium nitride layer (barrier) at the bottom and by silicon dioxide layer (capping) at the sides. These interfaces act as blocking boundaries for the electromigration vacancy flux causing accumulation of vacancies at these interfaces. As discussed in Section 3.2, the vacancy dynamics model describes the local change of vacancy concentration in time due to the contribution of the vacancy transport as well as the generation/annihilation processes inside the fast diffusivity path, as presented in equation (3.26). In Figure 5.2, three distinctive stages of the time evolution of the maximum relative vacancy concentration are recognizable. These stages are explained according to [91] and can be related to the impact of the different driving forces governing the vacancy flux $\vec{J}_\text{V}$ associated with equation (3.24).

In the first stage (A), the transport of vacancies is dominated by the flux induced by the electromigration driving force. The reaction of the material in this stage, due to the gradients of the stress and the vacancy concentration, is considerably smaller than the electromigration itself. As a result vacancies tend to accumulate close to the interface region between copper and titanium nitride (Figure 5.2(a)). After about 1s the vacancy concentration reaches a quasi-steady state (stage B). During this stage, the response of the material tends to perfectly balance electromigration (Figure 5.2(b)). The quasi-steady state is

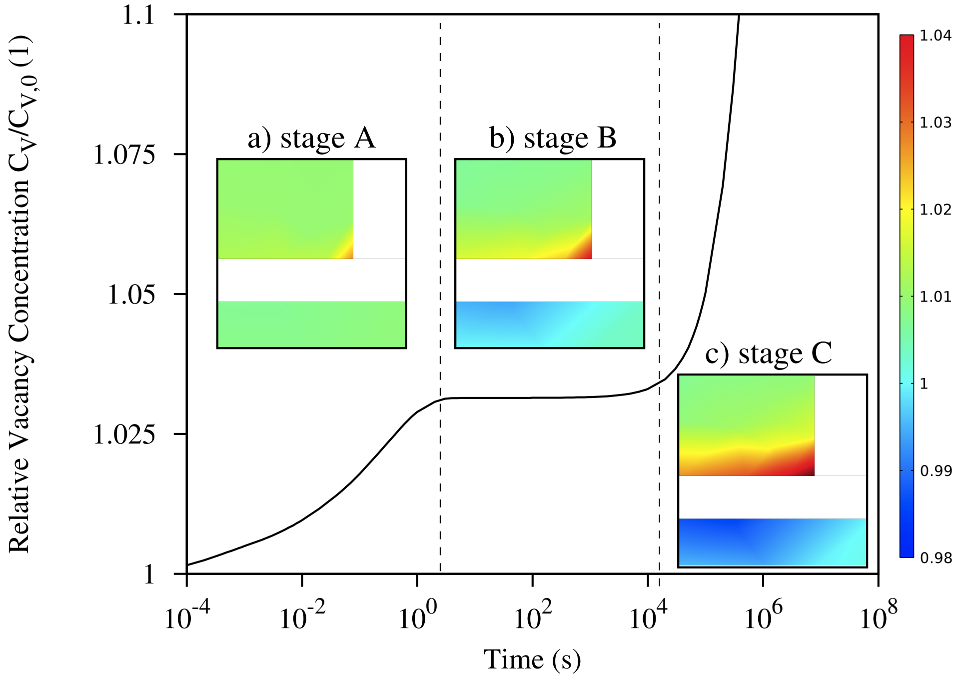


Figure 5.2: Maximum relative vacancy concentration change over time in the simulated structure. The cross section views show the relative vacancy concentration distribution at the TSV bottom during the three phases of vacancy dynamics. The peak values are located close to the copper/titanium nitride (metal/barrier) interface.

followed by a rapid growth of the vacancy concentration (stage C) caused by stress-activated vacancy sources (Figure 5.2(c)). During this stage, the source/sink term in equation (3.26), which models vacancy generation/annihilation processes, leads to a higher accumulation of vacancies close to the interface region which results in a rapid development of stress in the structure. The flux induced by the stress gradient is the dominant term of the vacancy flux equation (3.24) during this stage.

Stress Build-Up due to Electromigration

As presented in Section 2.5.2 Korhonen *et al.* [93] derived a model which provides the time evolution of the stress build-up during the three phases of the vacancy dynamics, observed in Figure 5.2. During the first two phases the maximum stress exhibits linear growth with time, as depicted in Figure 2.3. After a certain time the stress increases with the square root of time, until reaching a threshold value. In the following, the reasons for the stress development in the structure and the idea behind why reaching a certain threshold value is considered a requirement for electromigration void nucleation will be explained.

By monitoring the distribution of the hydrostatic stress in the TSV structure (Figure 5.3), the locations with the highest probability of void formation are identified. Void nucleation mainly occurs in those locations where vacancies accumulate. In the case study, the site of vacancy accumulation is at the TSV bottom, where the TSV intersect the capping and the barrier layers. Due to the slight relaxation of the lattice surrounding a vacancy, vacancy accumulation produces a volume contraction of the structure resulting in the development of tensile stress in these areas. Here, the tensile stress increases from the periphery, which is closed to the interface, towards the interface regions of the copper and titanium nitride. In turn, at the specular interface sides, a compressive stress is observed due to the volume expansion of the structure produced by vacancy depletion.

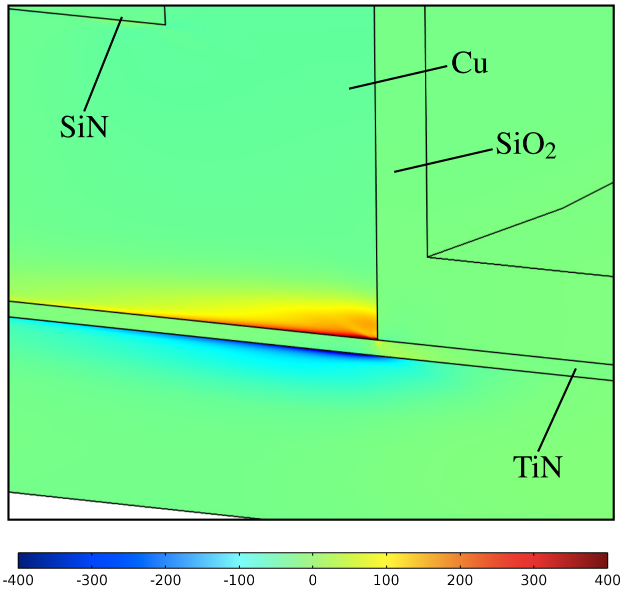


Figure 5.3: Profile view of the mechanical stress (MPa) distribution at the open copper TSV bottom after 10000 hours of current flow. The maximum tensile stresses are located at the Cu/TiN/SiO_2 intersection.

Therefore, the Cu/TiN/SiO_2 corner intersection is identified as the location with the highest probability of void formation in the open copper TSV structure. It has been experimentally shown that this is the typical site for void nucleation in copper dual-damascene structures with TSVs mainly due to the lower cohesive energies of the surrounding layers and fabrication defects [61].

Void Nucleation Time

In order to estimate the void nucleation time, the stress distribution at such sites in the structure is monitored by an increase of the current density by 30%. From the simulation results, the time evolution of the stress build-up due to electromigration is obtained for a total of four current densities (Figure 5.4). As expected [93], the maximum tensile stress increases with the square root of time, until it reaches the threshold value for void initiation. Following equation (3.72) [63] and assuming an initial adhesion-free patch R_P of 10nm, an interfacial free energy of copper γ_{Cu} of 1.65N/m, and a critical contact angle θ_C of 90°, the threshold stress σ_{thr} calculated for the particular case study is 0.33GPa. The electromigration void

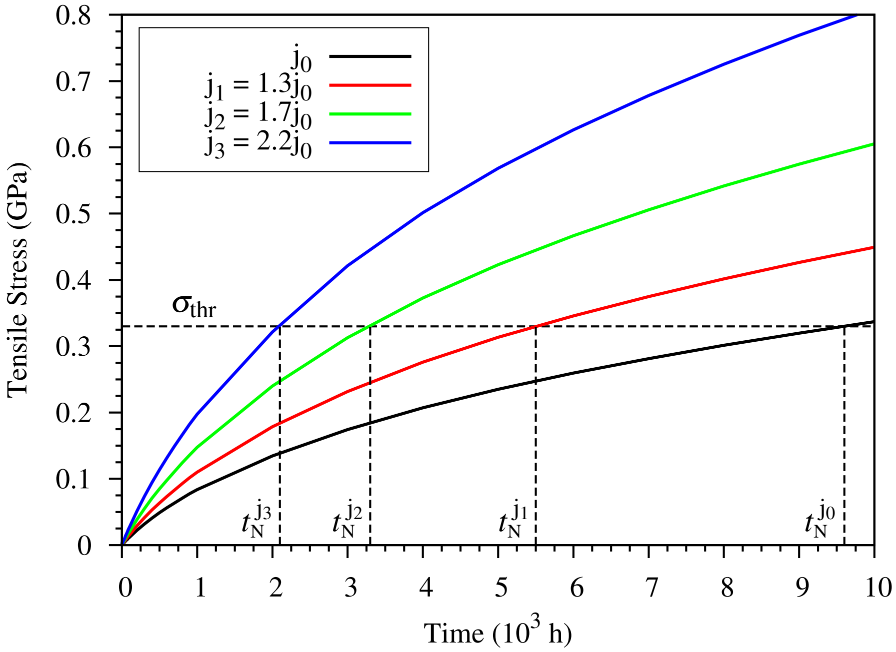


Figure 5.4: Evolution of the maximum tensile stress in the analyzed structure for different applied current densities. The electromigration void nucleation times t_E obtained for each curve profile are shown in the x-axis.

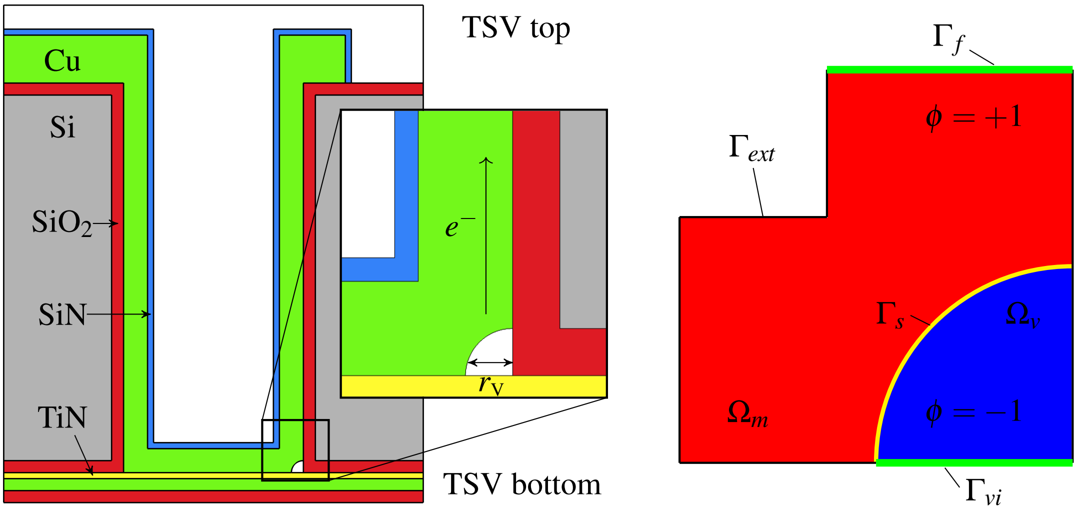
nucleation time t_N for a given applied current density is determined as the time needed to reach this limit. Applying lower current densities means that a longer time is needed to reach the threshold stress for void nucleation. Furthermore, it should be noted that during this time period the TSV resistance does not change. The void has been nucleated and its small size is not able to produce a significant increase of the electrical interconnect resistance.

5.1.3 Void Growth Analysis

Once the location of void nucleation in the interconnect structure is identified, electromigration-induced proceeds and failure is ultimately caused by the growth of the fatal void. As discussed in Chapter 3, the mechanism of void growth due to electromigration is mainly related to surface diffusion during this phase of failure. Atoms are transported to the void surface and diffuse along it until they reach the material interface. The responsible driving forces are the electric current flow, the stress gradient, and the surface curvature gradient. The diffusion of atoms along the void surface causes it to change its shape resulting in the void growth. Another small contribution governing the void growth is represented by feeding the void with vacancies coming from the bulk. The evolution of voids due to electromigration-induced surface diffusion can be modeled by employing two different methodologies, namely diffuse interface and semi-empirical models, as discussed in Chapter 3. In the following, both methods will be applied to study the void evolution mechanism in the open TSV structure under accelerated test conditions of increased temperature and current density.

Diffuse Interface Model

The diffuse interface model is employed to simulate the dynamics of pre-existing voids in open TSVs. In order to investigate the resistance change due to the void evolution dynamics in an open TSV structure, a 2D diffuse interface model is constructed to describe the void growth caused by vacancy accumulation near the Cu/TiN interface at the TSV bottom. The configuration considered in the diffuse interface calculations is illustrated in the highlighted area in Figure 5.5(a).



(a) (b)

Figure 5.5: (a) General cross section view of a through silicon via. The portion of the structure with the initial void under consideration for simulation is highlighted. (b) The cross-sectional view of the considered 2D domain Ω with the applied boundary conditions.

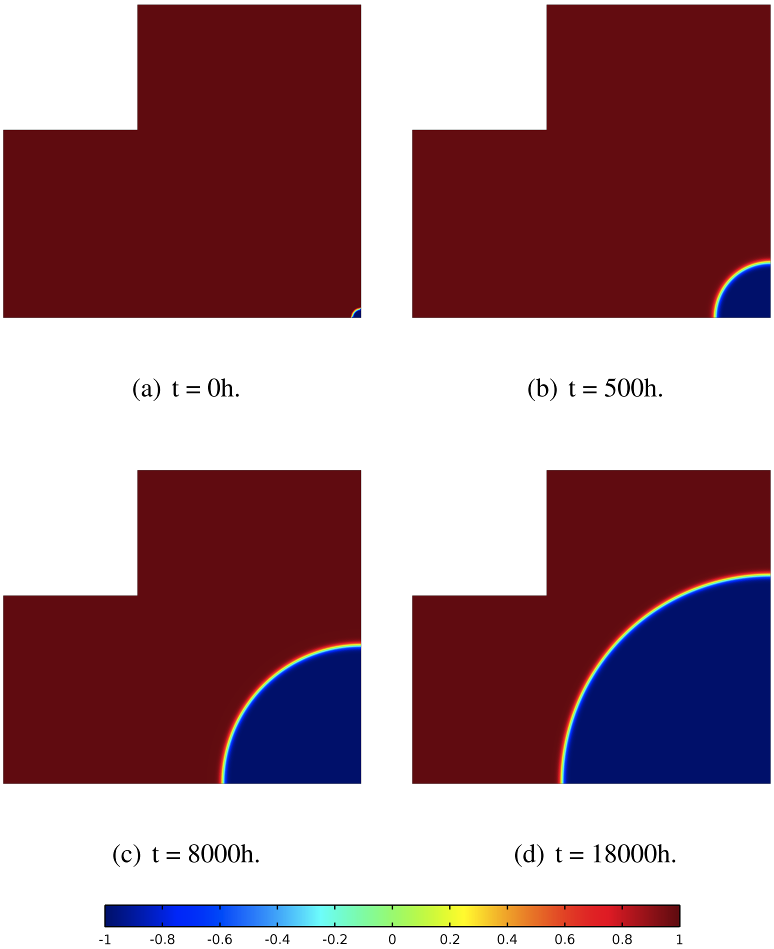
The portion of the open copper TSV structure analyzed is represented geometrically as a copper interconnect surrounded by passivation (SiN), insulation (SiO_2), and barrier (TiN) layers. The outer material interfaces surrounding the copper line are taken to be rigid. A small void is placed at the site of void nucleation within the metallization (Cu/TiN interface) with its surface free to move. The initial void radius r_V is assumed to be 10nm. Since copper is much more susceptible to electromigration than titanium nitride, the flux of vacancies is considered only in the copper line of the structure depicted in Figure 5.5(a). The computation of the order parameter field is therefore only restricted to the copper domain of the structure, as illustrated in Figure 5.5(b). Since the analysis is restricted to a 2D portion of the copper domain which contains a quarter of a circular void extending throughout the width of the interconnect line, the case study reduces to an unpassivated metal line. This approximation leads one to neglect the effect of mechanical stress in the unconfined line. This also allows to neglect the effects of grain boundaries and lattice diffusion, because diffusion at the void surface is considered to be much faster than in the bulk and the grain boundaries [62]. Furthermore, the study is restricted to the case of an isotropic medium.

The setting of the initial values for the order parameter in the domain serves as an initial condition for the simulation. The initial value of the order parameter in the void region Ω_v of the domain is indicated with $\phi = -1$ (blue region in Figure 5.5(b)), while the initial order parameter value in the bulk material Ω_m is defined with $\phi = +1$ (red region in Figure 5.5(b)). The initial position of the metal-void interface Γ_s is therefore represented with the value $\phi = 0$ (yellow line in Figure 5.5(b)). No-flux boundary conditions (3.83) are applied to the external surfaces of the domain. If no-flux boundary conditions are established at all external boundaries, the void modeled by the solution ϕ of the Cahn-Hilliard equation (3.82) does not grow, but keeps its volume constant in time. In order to predict the growth of the void, when it is on the edge of the domain, the Cahn-Hilliard equation should be extended with a source term which allows the creation of the order parameter. For this purpose, Dirichlet boundary conditions are applied at the boundaries Γ_f and Γ_{vi} of the domain (thick green lines in Figure 5.5(b)). Dirichlet and no-flux boundary conditions related to the case study can be summarized as follows

$$\phi = 2V_\mathrm{f} - 1 = \begin{cases} +1 & \text{for } V_\mathrm{f} = 1 \quad \text{on} \quad \Gamma_f \\ -1 & \text{for } V_\mathrm{f} = 0 \quad \text{on} \quad \Gamma_{vi} \end{cases} \quad \text{and} \quad \hat{n} \cdot \vec{J}_\mathrm{s} = 0 \quad \text{on} \quad \Gamma_{ext}, \tag{5.1}$$

where V_f is the volume fraction of the material and void phases. A value $V_\mathrm{f} = 1$ specifies the solution ϕ along the Γ_f boundary at the lower side of the metal phase, while a value $V_\mathrm{f} = 0$ represents the order parameter at the Γ_{vi} boundary representing the Cu/TiN interface of the void phase. The source term allows for the creation of the order parameter and, consequently, allows for the void to expand. No-flux boundary conditions are applied to the other boundaries Γ_{ext} of the domain (black lines in Figure 5.5(b)) in order to maintain the conservation of total mass. Operating conditions for electromigration simulations are set by imposing boundary conditions over appropriate regions of the case studied. All external surfaces of the structure are assumed isotherm. For electrical loading, the lower side of the copper line is maintained at $J_0 = 1\mathrm{MA/cm}^2$, and the Cu/TiN interface is set as ground. The Cu/TiN interface acts as an electromigration blocking boundary and prevents the void from propagating into the barrier layer while current flows through the copper line. The configuration presented in Figure 5.5 represents the starting point of the FEM simulation, where resistance increase due to the growth and evolution of a void at the TSV bottom is investigated by employing the diffuse interface method.

Figure 5.6(a) shows the position of the initial void in the interconnect. Since higher electromigration-induced stress levels are observed at the TSV bottom close to the Cu/TiN interface, as discussed in the previous section, the initial void is placed at the corner of the copper, barrier, and insulation layers. Within the structure, the void begins to grow due to electromigration and moves in the same direction as the electron flow. After some time, the void gradually increases in size as illustrated in Figure 5.6(b) and Figure 5.6(c). The choice of the no-flux boundary conditions together with the Dirichlet boundary conditions, at the prescribed boundaries of the domain presented above, for the solution of the Cahn-Hilliard



(a) t = 0h.

(b) t = 500h.

(c) t = 8000h.

(d) t = 18000h.

Figure 5.6: Order parameter distribution of the evolving void at the bottom of the TSV structure presented in Figure 5.5(a). (a) A small initial void is placed within the structure. (b) After 500h, it begins to move in the direction of the electron flow. (c) Following this phase, vacancies tend to accumulate at the void surface whereby it grows further. (d) Due to an increase in the distribution of the current density along the void surface, void propagation accelerates triggering open circuit failure.

equation (3.82) allows for the simulation growth of the void caused by the action of the electromigration force. The creation of the order parameter at these boundaries enforces the non-conservation of the order parameter in the domain and allows for the change of the void's area in time. Without these boundary conditions, the void would not grow, but would instead keep its area constant in time because of the conservation of the total mass of the bulk material. In real interconnects, the void is not conserved and its evolution is related to the fact that the electric current flow drives the vacancies towards the Cu/TiN interface, where they are captured at the void surface. In turn, at the opposite side, the increased atom flux would generate a hillock. Vacancies may diffuse along the void surface causing it to change its shape and leading to the void growth [62]. In addition, the surface minimizing diffusion term tends to maintain a stable circular shape throughout the growth process. Then, the void spreads across the full width of the metal-barrier interface leading to open circuit failure (Figure 5.6(d)). This evolution of the void influences the conducting metal cross section and therefore affects the interconnect resistance. Since diffusion on the void surface is assumed to be isotropic, the void has a rounded morphology and remains rounded throughout its evolution.

Semi-Empirical Method

Another method used to simulate the growth of the void in the open copper TSV structure is based on a semi-empirical approach, as described in Section 3.4.3. The semi-empirical method assumes that the volumetric growth of the void is due to changes in the vacancy concentration distribution on the void surface driven by the electron wind force. The growing void depends on the rate at which vacancies reach the void and transport along its surface, caused by changes in the current density around the void itself. The rate of vacancy transport along the surface is therefore mainly due to electromigration and is taken to be proportional to the tangential component of the current density at the surface, as mentioned in Section 3.4.2.

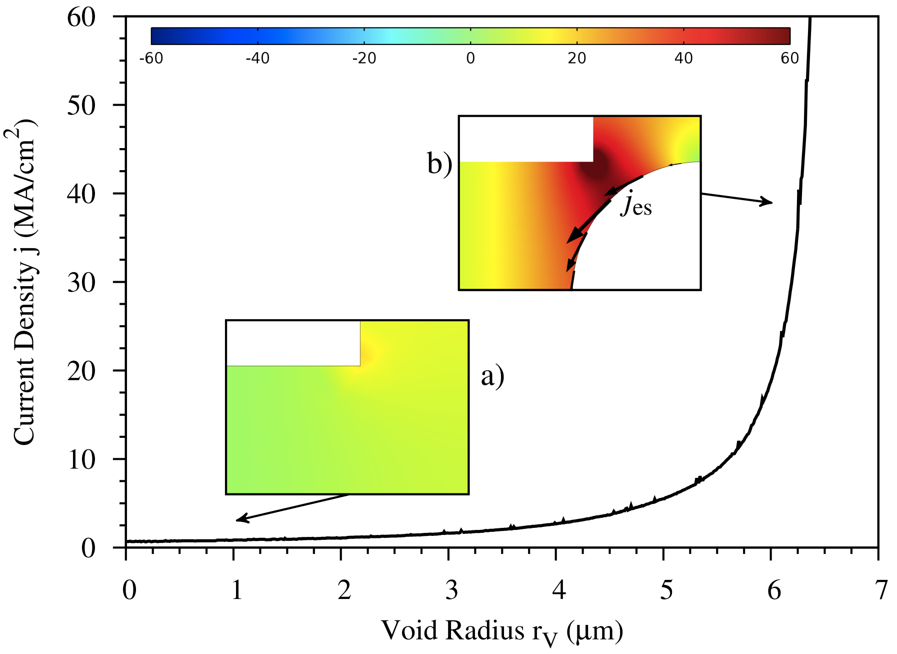


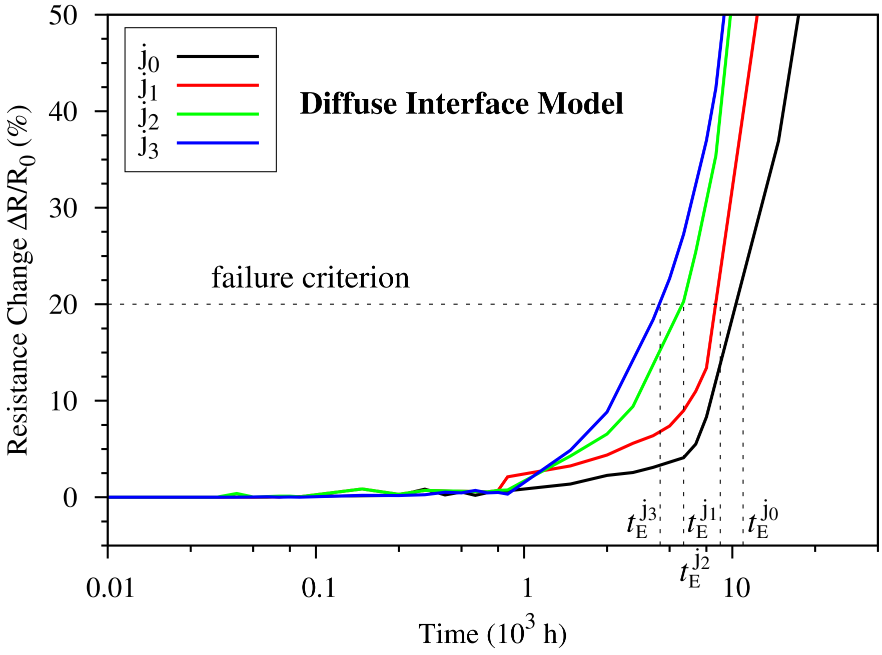
Figure 5.7: Current density dependence on the void radius for the initial applied electrical loading j_0. Cross section views of the current density distribution are shown at two different void radii r_V: a) 10nm and b) 6μm. Current crowding increases as soon as the void becomes larger. The distribution of the average current density over the void surface is represented by the arrows.

By following the modeling approach described in Section 3.4.3, an initial spherical void of radius $r_V = 10$nm is placed at the location of void nucleation and its radius is increased (Figure 5.5(a)). Figure 5.7 shows the current density distribution close to the void nucleation location for different void sizes in the simulated structure. Electron flow leads to current crowding at the TSV bottom, towards the corner, where the void, copper, and barrier layers meet, even if the radius of the void is small in size (Figure 5.7(a)). Current crowding arises especially at the TSV bottom close to the sites of void nucleation because of the diverse layers' varying geometries and electrical conductivity properties. The current flow tends to feed the void surface with vacancies, implying vacancy transport along it and consequently increasing the volume of the void. As soon as the void becomes larger, current density divergences are more prominent around the void surface, as shown in Figure 5.7(b). The average current density over the void surface can be monitored at every point along the surface itself. Figure 5.7(b) shows that the main driving force affecting the diffusion of vacancies along the void surface is observed to be proportional to the tangential component of the current density to the surface. Peak values of j_{es} are located at the metal-void interface, where current crowding is higher. This is in good agreement with the simulation results obtained by means of FEM simulations using a diffuse interface approach in [28]. The electromigration driving force causes significant void growth as the void propagates through the line. The growing void reduces the effective TSV conducting area at the bottom of the TSV, leading to higher current crowding in these regions.

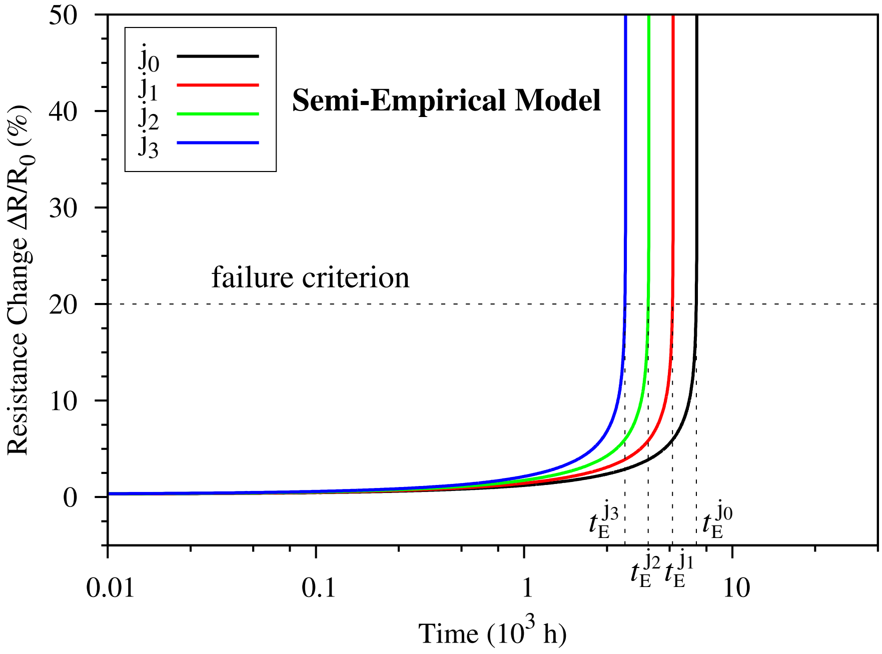
Resistance Increase and Void Evolution Time

Under these circumstances it is obvious that as the line nears complete failure, the resistance of the interconnect increases non-linearly with time. The resistance change with time is associated to the growth of the void located at the Cu/TiN/SiO_2 intersection at the TSV bottom. The open TSV fails after the maximum tolerable resistance level is exceeded, typically a resistance increase of 20%. The electromigration void evolution time t_E is determined as the time needed to reach the maximum tolerable resistance value. The determination of the resistance/time curves is based on the simulation results regarding the growth of the void obtained from the two different approaches described above under different stress conditions of current density, as illustrated in Figure 5.8. The resistance increase of the given interconnect is monitored by increasing the initial current loading by 30%. In this way, it is possible to extract the different void evolution times.

Numerical solutions of equations (3.85) - (3.88), together with the solution of the Cahn-Hilliard equation (3.82), allows one to determine the change in the interconnect resistance during void evolution by following the diffuse interface method. At each time step, it is possible to extract the position of the void and the interconnect resistance from the computation of the order parameter and from the numerical solution of the electrical problem, respectively. In this way, the change in interconnect resistance throughout the entirety of void growth is obtained, as depicted in Figure 5.8(a). In addition, increasing the applied current density results in a decrease in the time required to reach the failure criterion. Here, an increase in the resistance is accelerated due to a more intense electromigration flux induced by higher current densities.



(a) Diffuse interface model



(b) Semi-empirical model

Figure 5.8: Interconnect resistance change as a function of time for different applied electrical loadings obtained by following (a) the diffuse interface method and (b) a semi-empirical approach. The failure criterion is a 20% increase in resistance. The electromigration void evolution times t_E obtained for each curve profile are shown on the x-axis.

In a similar way, the resistance/time curves during the void evolution period are obtained by following a semi-empirical approach, as depicted in Figure 5.8(b). The numerical simulation results for the vacancy flux captured by the void surface which produces changes in the current density and vacancy concentration distribution are inserted into equation (3.94). By performing a numerical integration, it is possible to obtain the time necessary to grow a void of a given volume. Furthermore, numerical solutions of the electrical problem (Section 3.1) allow to determine the interconnect resistance change during the void evolution period. In this way a relationship between the open copper TSV resistance and time for different initial electrical loadings can be observed, as plotted in Figure 5.8(b).

5.1.4 Lifetime Estimation

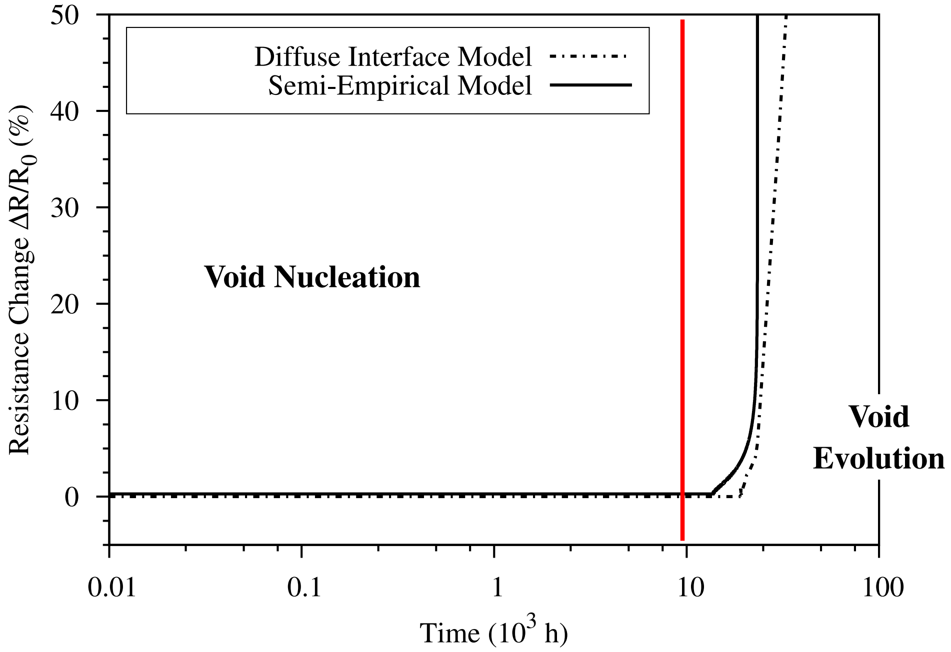


Figure 5.9: Complete electromigration resistance trace profile for the initial applied current density j_0 by following the two methodologies describing the void growth. The two phases of failure are shown.

Once both void nucleation t_{N} and void evolution t_{E} times are determined, the electromigration failure time evaluation of the open copper TSV structure can be determined. The total electromigration TTF can be expressed as the sum of the void nucleation and the void evolution times. The void nucleation and void evolution times are of about the same order of magnitude. This highlights the importance of including both contributions in the complete electromigration TTF estimation of the given interconnect structure. Figure 5.9 shows the interconnect resistance as a function of time for a given applied current density. The two

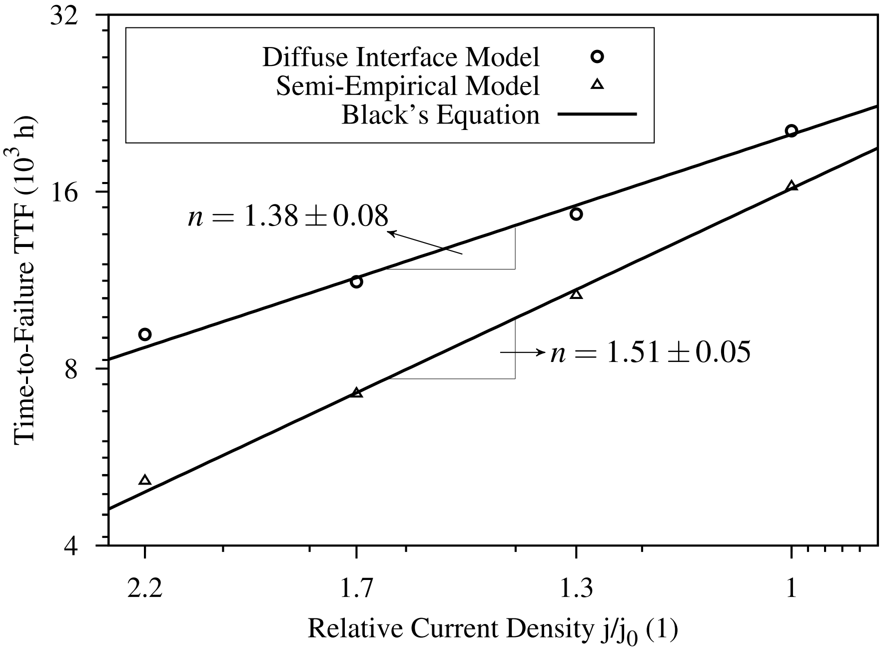


Figure 5.10: TTF depends on the current density. The line indicates the fit according to Black's equation and the current density exponent *n* is its angular coefficient.

curves are obtained by following the two methodologies describing the void evolution mechanism due to electromigration. As expected, the resistance curve can be analyzed by dividing it in two parts. The latency period is characterized by the void nucleation phase. During this period the void is nucleating and any resistance change is electrically undetectable. Therefore, at the beginning, changes in resistance with time are very small. After a void has nucleated, the void evolution phase begins. The resistance of the TSV progressively increases with time. Here, the void is growing and its size influences the electric performance of the interconnect. After this, an abrupt jump in the interconnect resistance is observed. At this stage an open circuit failure due to electromigration is already noticeable, and the electric current does not flow in the interconnect.

The electromigration TTFs for different applied current densities are determined by the times required to reach the maximum tolerable resistance level. Lifetimes are extracted from the resistance/time curves. The TTFs obtained with the two methods are of about the same order of magnitude, even if the mechanisms involved in the methodologies are different. The TTF versus current density curves are subsequently fitted to Black's equation, as shown in Figure 5.10. The result yields a current density exponent *n* of 1.38 for the analysis of the void growth which employees the diffuse interface method, while a value close to 1.5 is estimated using the semi-empirical model. It has been shown in Section 1.4.3 that a value close to 1 indicates that void evolution is the most dominant mechanism of electromigration failure, while a value close to 2 corresponds to a nucleation time dominated failure. Both results yield values between 1 and 2 which confirm that both void nucleation and void evolution are important mechanisms in the electromigration failure. The development of the electromigration model based on the combination of void nucleation together with the void growth mechanism well describes the electromigration failure analysis in open copper TSV technologies. Furthermore, the estimation of electromigration TTF in such structures follows Black's behavior, as shown in Figure 5.10. The difference between the two curves presented in Figure 5.10 is related to the methodology adopted for simulating the void evolution mechanism in the TSV structure. It should be noted that since the semi-empirical method involves approximations in the physical theory in order to simplify the numerical calculation, results obtained by using this approach are less accurate than results obtained by following the diffuse interface model. However, the semi-empirical model is useful because it speeds the simulation analysis.

5.2 Electromigration Reliability of Solder Bumps

As described in Section 1.3.2 flip-chip solder bump technologies are essential components for 3D integration because they enable a conductive contact between vertically stacked wafers. The technology consists of three components: solder bump, metallic bond pad on the substrate side, and thin film under-bump-metallization (UBM) on the chip side. The UBM, which separates the bump itself from the on-chip metallization, is important for the layout attached to the solder bump, because it reduces the current crowding near the contact between the solder bump and the surrounding metallization and contributes to longer electromigration lifetimes.

Although the solder bump with UBM show significant advantages, the mechanical and electrical properties of solder bumps influence the overall reliability of 3D integration technologies, as discussed in Section 1.3.3. A characteristic of solder bumps is that during the technology processing and use conditions, their material composition changes [31]. This compositional transformation is enhanced by electromigration. In particular, it has been shown that the formation of an intermetallic compound (IMC), caused by the material transport driven by the electric current density and the stress gradient, occurs at the interface between the solder bump and the UBM [34, 110, 111]. The IMC growth at this interface is accompanied by the formation of voids, which can cause a complete failure of the solder bump.

As described in Section 1.4.1, and further discussed in Section 5.1, the evolution of electromigration failure in a copper interconnect takes place in two distinct phases: a void nucleation phase and a void evolution phase. During the initial phase no effective resistance increase can be observed. The situation is quite different in the case of electromigration failure evolution in a solder bump, where an IMC layer is also present [32, 33]. From the initiation of electromigration stressing, under accelerated conditions of increased temperature and current density, a continuous increase in the bump resistance is observed. After a certain period of electromigration stressing, the bump resistance starts to increase with a significantly steeper slope. Chen *et al.* [32, 33] assume that the two slopes of the resistance growth represent two different stages of failure development: void nucleation combined with IMC growth and void evolution with IMC dissolution. Since interconnect electromigration resistance change with time is primarily determined by the void nucleation mechanism, the understanding of the early failure mode becomes decisive for a precise reliability assessment. The solder bump lifetime is influenced by the early phase of failure due to the presence of the IMC layer. Consequently, the prediction of the void nucleation time provides a realistic electromigration lifetime estimation of a given interconnect.

The electromigration-induced voiding at the interface between the IMC and the solder material plays an important role in controlling the electromigration lifetime of flip-chip solder bump technologies. The goal of the investigation of electromigration in solder bumps is to establish an accurate compact model for the prediction of the interconnect lifetime by means of theoretical analysis and FEM-based simulations.

5.2.1 Geometry and Simulation Parameters

The flip-chip solder bump structure used in electromigration analysis is sketched in Figure 5.11. Pure tin (Sn) has been identified as the best material for ultra fine pitch solder bumps, due to its baseline advantages of being electrodeposited and due to its low melting temperature [32]. The top and the bottom of the spherical bump contact the cathode and the anode copper metallization, respectively. On the top, the Sn solder bump is connected to the cathode through an UBM, which consists of a nickel (Ni) barrier layer. At the interface between Ni and Sn, an IMC will form due to electromigration and this region plays a key role when it comes to understanding the mechanism by which electromigration failure proceeds in solder bumps.

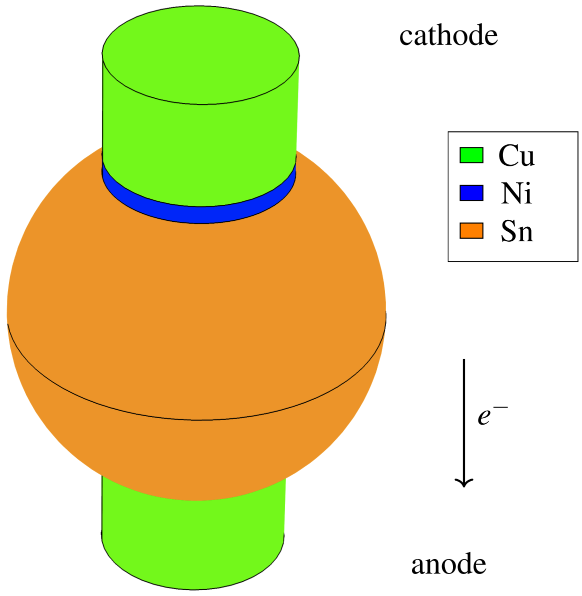


Figure 5.11: Profile view of the solder bump geometry used for simulations. On the top of the Sn bump, a Ni UBM layer is placed. The arrow shows the direction of the electron flow.

Table 5.3: Materials parameters for the electro-thermal, vacancy dynamics, and solid mechanics models [31, 38, 40].

Model	Parameter	Cu	Sn	Ni
Electro-thermal	$\sigma_{\mathrm{E},0}$ [S·m^{-1}]	$5.35\cdot10^{7}$	$3.8\cdot10^{7}$	$1.38\cdot10^{7}$
	$k_{\mathrm{T},0}$ [W·(m·K)$^{-1}$]	379	63.2	90.7
	α_{E} [K^{-1}]	$4.3\cdot10^{-3}$	0	-
	α_{T} [K^{-1}]	0	0	-
	β_{E} [K^{-2}]	0	0	-
	β_{T} [K^{-2}]	0	0	-
	ρ_{m} [Kg·m^{-3}]	8920	5770	8900
	c_{P} [J·(Kg·K)$^{-1}$]	385	0.777	445
Solid mechanics	E [GPa]	130	41.6	219
	ν	0.35	0.33	0.31
	α_{th} [10^{-6}K^{-1}]	16.5	0	13.4
Vacancy Dynamics	$D_{\mathrm{V},0}$ [cm^{2}·s^{-1}]	0.52	$3.7\cdot10^{-8}$	2.9
	E_{a} [eV]	0.89	0.25	2.88
	Z^{*}	-5	-79	-10
	Q^{*} [J]	$1.2\cdot10^{-20}$	$1.2\cdot10^{-20}$	$1.2\cdot10^{-20}$
	f	0.4	0.5	0.5
	Ω_{a} [cm^{3}]	$1.18\cdot10^{-23}$	$1.18\cdot10^{-23}$	$1.18\cdot10^{-23}$
	$C_{\mathrm{V},0}$ [cm^{-3}]	$1\cdot10^{16}$	$1\cdot10^{16}$	$1\cdot10^{16}$
	τ_{V} [s]	1	$1\cdot10^{10}$	1

Table 5.3 lists the materials parameters obtained either by experimental or theoretical studies. The parameters are presented for the electro-thermal model, the vacancy dynamics model, and the solid mechanics model, as described in Chapter 3.

The simulation procedure presented in Section 4.3.2 is applied to the study of electromigration in the solder bump structure depicted in Figure 5.11. Since failure analysis [32, 33] have shown that failure in Sn bumps is mainly dominated by the mechanism of void nucleation at the bump/UBM interface, the simulation procedure is reduced to the case of void nucleation alone. Simulation starts by solving the electro-thermal problem in order to obtain the electric potential, current density, and temperature distributions in the structure. Then, the vacancy dynamics problem must be solved, followed by the mechanical stress problem in order to determine the distributions of vacancy concentration and stress, respectively. The simulation continues until the threshold stress for void nucleation is reached. Reaching the threshold stress implies void nucleation and the initiation of the rapid failure development at this location.

Electromigration simulations are carried out under accelerated test conditions, which are set by imposing the following boundary conditions to the solder bump structure in Figure 5.11. The temperature is kept constant at $T_0 = 473$K for all external surfaces of the structure and the initial electric current density $j_0 = 0.003$MA/cm^2 is set at the anode end (copper metallization at the bottom of Figure 5.11). In turn, the zero electric potential condition is set at the top side of the cathode end (copper metallization at the top of Figure 5.11). For the mechanical problem, all outer surfaces of the structure are mechanically fixed.

The scope of this analysis is to identify the location with the highest probability of void nucleation in the structure by monitoring the distribution of the stress build-up due to electromigration. Then, the analytical solution of the model by Korhonen *et al.* [93] presented in Section 2.5.2, which describes the stress behavior in time, is a convenient reference for an initial guess in designing a compact model to predict the lifetime of the solder bump under the influence of electromigration.

5.2.2 Location of Void Nucleation

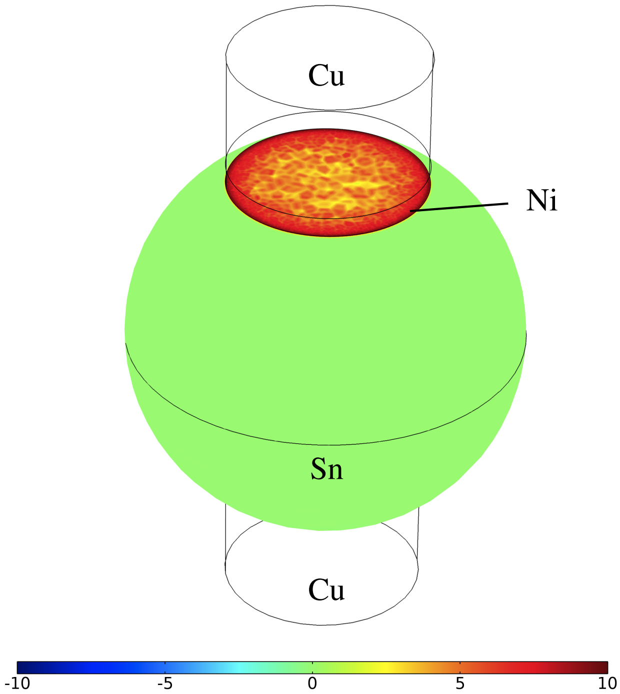


Figure 5.12: Profile view of the mechanical stress (MPa) distribution in the solder bump geometry after 14 hours of current flow. The maximum tensile stress is located at the top of the Sn bump beneath the Ni UBM layer.

As discussed before, the nucleation of a void is related to the formation and growth of the IMC at the interface between the UBM layer and the Sn bump. Other authors have demonstrated that the growth of an IMC inside the bump under the influence of electromigration is mainly caused by the atomic fluxes of the different materials composing the geometry ($\vec{J}_{\mathrm{Cu}}$, $\vec{J}_{\mathrm{Ni}}$, and $\vec{J}_{\mathrm{Sn}}$), which are driven by gradients of the chemical potentials (μ_{Cu}, μ_{Ni}, and μ_{Sn}) and the electromigration force [30, 31, 110, 111]. The Cu and Ni atoms penetrate into the Sn bump and segregate just below the UBM/bump contact surface. The dynamics of the subsequent IMC growth is determined by the chemical reactions which convert Cu, Ni, and Sn into an IMC, typically consisting of Cu_6Sn_5 or Ni_3Sn_4. The model presented in [30, 31] assumes that all the transport processes take place inside the Sn bump. During the formation of the IMC, the interaction between Cu, Ni, and Sn causes hydrostatic stress because of the resulting volume change. The accumulation of atoms may give rise to compressive stresses within the solder or at the solder/UBM interface and consequent hillock formation. In turn, at the specular side of the interface, vacancy accumulation would produce tensile stress and subsequent void nucleation. The hydrostatic stress distribution in the structure is monitored as can be seen in Figure 5.12. A tensile stress increases from the center towards the periphery of the interface between the bump and the UBM layer, which leads one to the conclusion that a void most probably nucleates at the bump/UBM interface.

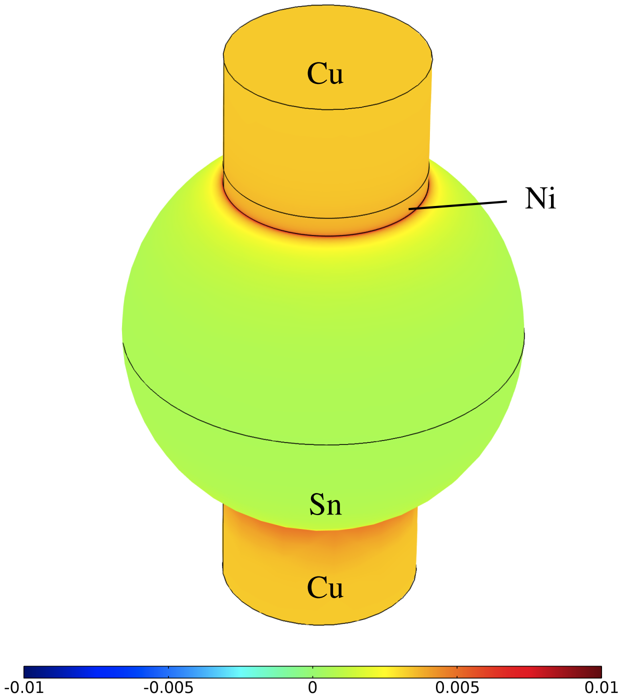


Figure 5.13: Profile view of the current density (MA/cm^2) distribution in the solder bump geometry after 14 hours of current flow. Current crowding is observed close to the top of the Sn bump beneath the Ni UBM layer.

The void nucleation sites are also the locations of current crowding. This outcome can be verified by analyzing the current density distribution in the flip-chip solder bump structure, as illustrated in Figure 5.13. Due to the different electrical conductivity of the Sn bumps and the Ni UBM layer, current crowding arises close to the interface regions of void nucleation. In fact, in the areas where the UBM layer is mechanically fixed to the Sn bump the current is mainly flowing in the bump due to its lower electrical resistance. In this way, the current flow tends to accumulate vacancies at these locations leading to a rise in tensile stresses and accordingly void nucleation [157, 158].

5.2.3 Compact Model for Lifetime Estimation

In order to derive an expression for the solder bump lifetime, it is important to define a failure condition. While the ultimate failure condition of any interconnect is an increase of its resistance, the physical condition which must be fulfilled for an initialization of the early phase of failure in solder bumps (i.e. void nucleation) is the attainment of a threshold stress.

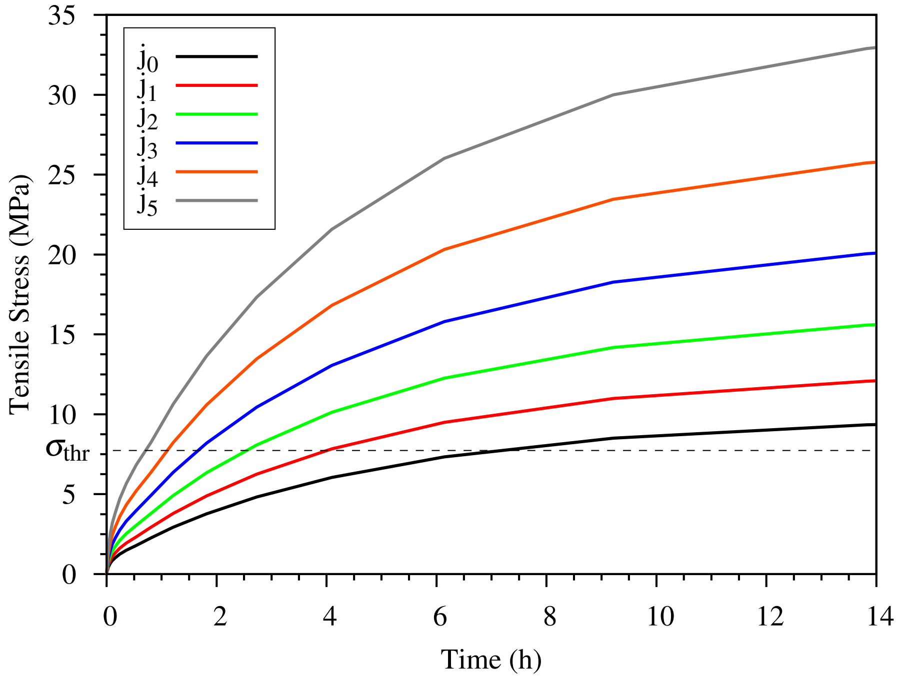


Figure 5.14: Time evolution of the maximum tensile stress in the analyzed structure for six applied current densities. The threshold stress σ_{thr} for void nucleation is shown in the y-axis.

An analytical solution of Korhonen's model [93] describes the time evolution of the stress σ build-up due to electromigration in a 1D structure as follows

$$\sigma(x,t) = \frac{2|Z^*|e\rho j\pi}{\Omega_a}\sqrt{\frac{kt}{\pi}}, \tag{5.2}$$

where Z^* is the effective valence, e is the electron charge, ρ is the electrical resistivity, Ω_a is the atomic volume, and k is a constant. The mechanical stress along the 1D interconnect increases until it reaches a threshold value, which is a usual condition for electromigration void nucleation. In the case of a 3D geometry, more vacancies are available in the cross section of the structure and $\sigma \sim jR^2\sqrt{t}$. By following equation (5.2) the compact model describing the time needed to reach the threshold stress σ_{thr} value in a solder bump, which depends on its radius, is obtained as follows

$$TTF = \frac{A\sigma_{\text{thr}}^2}{j^2R^4}, \tag{5.3}$$

where the constant A contains several material properties related to the solder bump.

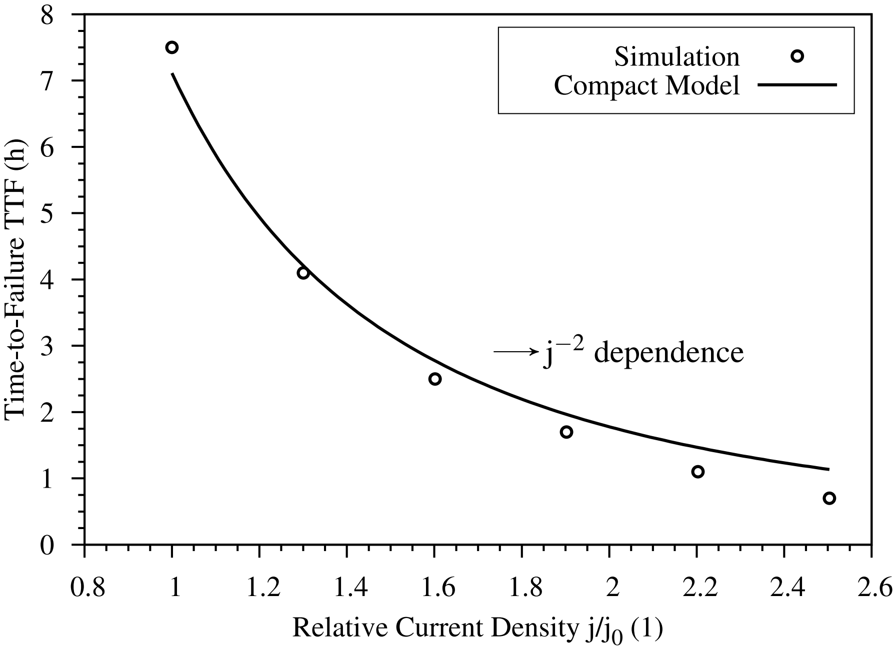
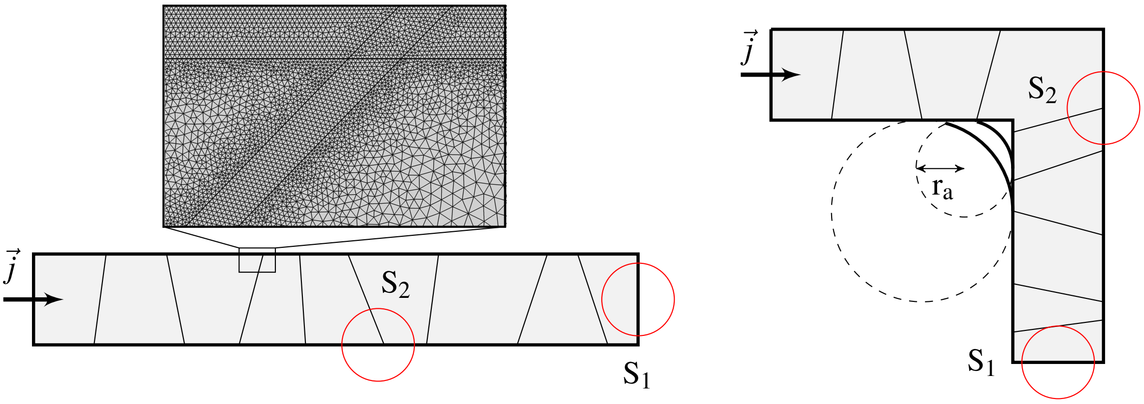


Figure 5.15: TTF depends on the current density. The solid line indicates the fit according to the compact model for lifetime prediction presented in equation (5.3).

The time evolution of the stress built-up due to electromigration for a total of six applied current densities is shown in Figure 5.14. As expected, at the initial stage the maximum stress exhibits linear growth with time. Subsequently, the stress increases in proportion to the square root of time, until it reaches the threshold value for void nucleation [93]. The value of the stress threshold σ_{thr} is 7.7MPa and is obtained from equation (3.72) [63] by using values of the initial adhesion-free patch R_P of 10nm, the interfacial free energy of tin γ_{Sn} of 0.0545N/m, and the critical contact angle θ_C of 45°. At higher current densities the threshold stress for void nucleation is obtained in less time than at lower current densities. This implies that under higher current density stress conditions, the electromigration-induced vacancy transport at the bump/UBM interface is more efficient, since more vacancies are available in a cross section of the bump. Lifetimes are extracted from the stress/time curves and are fitted to the compact model for lifetime prediction presented in equation (5.3). The results obtained from simulations are in good agreement with the compact model. Furthermore, similar to Black's original empirical work [12], the failure time in equation (5.3) follows a j^{-2} dependence, which indicates that the void nucleation is the dominant mechanism of electromigration failure in the bump. Therefore, the development of a compact model for the prediction of the void nucleation time is beneficial for the estimation of the TTF for solder bump technologies.

5.3 Effect of Current Crowding and Microstructure

Electromigration degradation and failure in modern interconnect structures are the result of several physical phenomena acting simultaneously. In the case of dual-damascene technologies, both geometry and microstructure of the interconnect play an important role in determining the development of electromigration degradation. Different types of failure can arise from the effects each of these factors. An impact of the geometry can be observed in the case of a dual-damascene interconnect structure where the liner separates two copper regions and interrupts the material transport. This configuration leads to material depletion and void formation. Furthermore, when the dimensions of modern interconnects are on a scale where the material properties at the microscopic and atomistic levels are gaining importance, the impact of current crowding on the development of electromigration-induced voiding can be significant. The scaling of geometrical features enhances the impact of microstructure of the metal interconnect on the electromigration failure. The microstructure introduces a diversity of possible electromigration paths and local mechanical properties depending on the crystal orientation of the grains. Grain boundaries act as fast diffusivity paths and vacancy recombination sites. The diffusion of vacancies in the grain boundary is faster compared to diffusion in the grain bulk, because a grain boundary generally exhibits a larger diversity of point defect migration mechanisms. Formation energies and migration barriers of the atoms inside the grain boundaries are on average lower than those for the crystal lattice [143].



(a) Linear

(b) L-shaped

Figure 5.16: Schematic view of the (a) linear and (b) L-shaped geometry used in this analysis. The zoomed-in detail view of a triple point depicts the mesh density employed in the numerical calculations. The arrows show the direction of the current density. The red circles S_1 and S_2 represent the spots where peak values of vacancy concentration and stress are extracted.

In this work, state-of-the-art models of electromigration are used to investigate the impact of current crowding and microstructure in electromigration performance in simple single layer dual-damascene copper structures. In particular, the electromigration performance of a standard linear structure is compared to a L-shaped geometry. Both interconnect structures are analyzed and the results are compared with the original experimental observations provided by Croes *et al.* [39].

5.3.1 Geometries and Model Parameters

The geometries used in the comparative study are shown in Figure 5.16. The reference interconnect structure is a simple straight copper line without a via (Figure 5.16(a)). The second geometry is proposed by adding a 90° angle in the line (Figure 5.16(b)). In both interconnect structures, the network of grain boundaries is indicated. By assuming the interconnect width of 80nm, the grain boundaries can be assumed to be distributed in a near bamboo formation, as it could be expected for copper interconnects with a grain size comparable to line width (Section 1.4.5). Furthermore, the triple point, generated from the intersection between two grains and the material interfaces, becomes important when the location of void nucleation in the structure must be found. This is illustrated in the zoomed-in detail view of Figure 5.16(a). Material interfaces and grain boundaries of the structure have to be supplied with an appropriately fine mesh. This is necessary to provide sufficient accuracy for the results along the triple point regions.

Table 5.4: Materials parameters for the vacancy dynamics model [25, 40].

Model	Parameter	Cu
Vacancy Dynamics	$D_{\mathrm{V},0}^{\mathrm{b}}$ [cm^2·s^{-1}]	0.52
	$D_{\mathrm{V},0}^{\mathrm{gb}}$ [cm^2·s^{-1}]	0.52·10^2
	$D_{\mathrm{V},0}^{\mathrm{i}}$ [cm^2·s^{-1}]	0.52·10^3
	$E_{\mathrm{a}}^{\mathrm{b}}$ [eV]	0.89
	$E_{\mathrm{a}}^{\mathrm{gb}}$ [eV]	0.7
	$E_{\mathrm{a}}^{\mathrm{i}}$ [eV]	0.5
	Z^*	-5
	Q^* [J]	1.2·10^{-20}
	f	0.4
	Ω_{a} [cm^3]	1.18·10^{-23}
	$C_{\mathrm{V},0}$ [cm^{-3}]	1·10^{16}
	$\tau_{\mathrm{V}}^{\mathrm{b}}$ [s]	1
	$\tau_{\mathrm{V}}^{\mathrm{gb}}$ [s]	1
	$\tau_{\mathrm{V}}^{\mathrm{i}}$ [s]	1
	ω_{R} [m^4·s^{-1}]	5·10^{-33}
	ω_{T} [m·s^{-1}]	5·10^{-11}
	δ [m^{-9}]	1

Since the scope of this work is to investigate the impact of current crowding and microstructure during the void nucleation mechanism induced by electromigration in the described geometries, the simulation procedure of void nucleation described in Section 4.3.2 is applied to study the electromigration failure development in these structures. In particular, the models derived in Section 3.2.1 have been used to describe the vacancy dynamics in the presence of grain boundaries and material interfaces. The derivation of these models is based on the segregation model [101] and the approach applied in this work consists of the expression for the vacancy annihilation/recombination term, as presented in equations (3.41) and (3.43) [25]. The models parameters for electro-thermal and solid mechanics models are the same of those presented for copper in Table 5.1, while the parameters for the vacancy dynamics model are summarized in Table 5.4. Electromigration simulations are performed at a temperature T of 573K and current density j of 4MA/cm^2.

5.3.2 Current Crowding

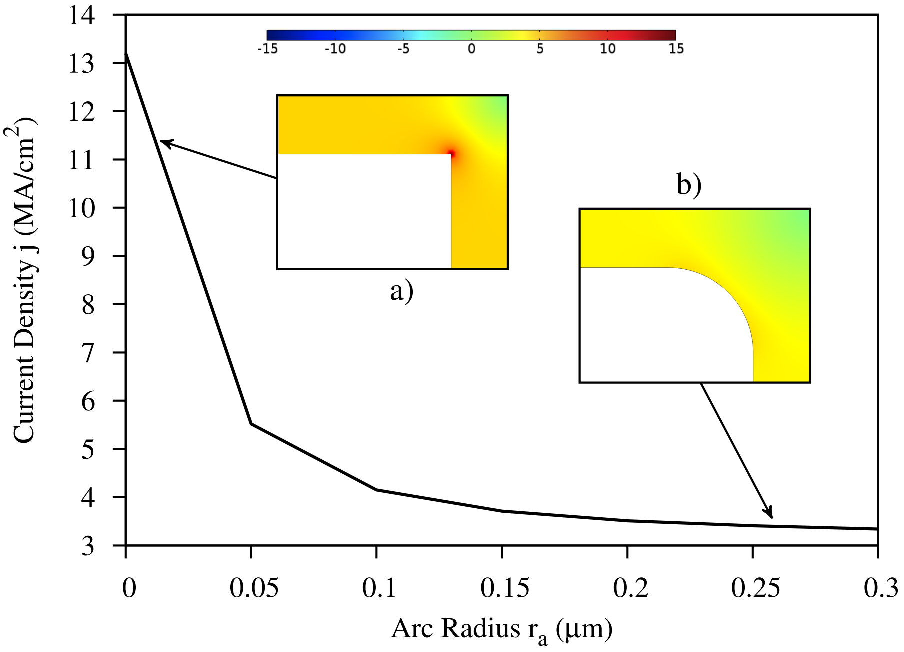


Figure 5.17: Current density dependence on arc radius r_a. Cross section views of the current density distribution are shown for two different arc radii r_a: a) 0μm and b) 0.25μm. Current crowding decreases as soon as the arc radius increases.

The first step of this analysis is to investigate the impact of current crowding on electromigration degradation. Current crowding is the effect of peaks in the current density due to regions of elevated electrical field strength. Corners are typical areas where current crowding occurs. Right angles in interconnect structures are sites where current density can become very high. The exact solution of the Laplace equation (3.3) of the electro-thermal model presented in Section 3.1 produces for these sites a singularity in the current density. The approximate solution obtained by FEM analysis cannot produce singularities, but instead produces high finite values for the current density in this area. By monitoring the distribution of the current density in the L-shaped geometry, the peak values are observed close to the corner of the right angled line, as depicted in Figure 5.17(a). Interconnect technology can never produce a perfect, sharp right angle. In Figure 5.16, the L-shaped line is shown with varying angle sharpness, which depends on the radius r_a of the arc that is created, tangent between the two straight lines. The current density distribution close to the corner of the L-shaped structure for different arc radii is illustrated in Figure 5.17. As soon as the arc radius r_a increases, the current density divergences become less prominent around the corner of the angled line (Figure 5.17(b). However, even if one defines an angle with a small circular fillet, the peak in current density increases very quicky with a smaller arc radius r_a, as presented in Figure 5.17. Since the vacancy flux induced by electromigration increases due to the higher value of current density according to

$$|\vec{J}_\mathrm{V}| \sim \frac{eZ^*}{k_\mathrm{B}T}|\vec{j}|, \tag{5.4}$$

it is plausible to expect that electromigration degradation is significantly intensified in the presence of right angles in the interconnect.

In the experimental study of Croes *et al.* [39], the development of electromigration failure has been investigated in both straight and angled interconnects under identical test conditions. It was natural to expect that current crowding produced in the right angle interconnect corner would intensify electromigration and lead to a shorter lifetime of the studied structure. However, in the lognormal probability plots of the failure times obtained on both the standard linear and angled structure no difference in failure times is observed [39]. This indicates that the current crowding and current density gradient induced in the angled structure have no effect on electromigration lifetime estimation, also not in the lower percentile. Furthermore, the determination of the location of void nucleation was performed by using top-down scanning electron microscopy (SEM) after removing the top passivation layers. No voiding has been observed directly in the interconnect corner of the L-shaped structure. Voids seem to appear randomly along the interconnect line [39]. Other factors, such as grain boundaries and material interfaces, have a significant influence on the electromigration failure in the given case study.

5.3.3 Impact of Microstructure

The experimental observations implies that even if current crowding and consequent intensive material transport are expected close to the interconnect corner, their effect on electromigration failure is negligible. From these observations, one may conclude that, while both microstructural and geometric factors play important roles, microstructure has the most significant impact on the electromigration failure. As previous studies have shown [25], sites where grain boundaries meet the liner or the etch-stop are natural points of weak adhesion.

High values of vacancy concentration and tensile stress are observed close to these locations. This implies that voids most probably nucleate at these sites.

The application of the simulation procedure, which includes the grain boundary and material interfaces models, to the geometries described before allows one to investigate the void nucleation process in multigrain structures. The solutions of the full physical electromigration model are identified in values of vacancy concentration and tensile stress. The peak values of vacancy concentration and corresponding peaks of tensile stress are extracted at the geometrical ends of the studied interconnect shapes (spot S_1 in Figure 5.16) and at the triple points of microstructures (spot S_2 in Figure 5.16). In the studied case the peaks at triple points are more important, particularly those which are distributed in the vicinity of current crowding region.

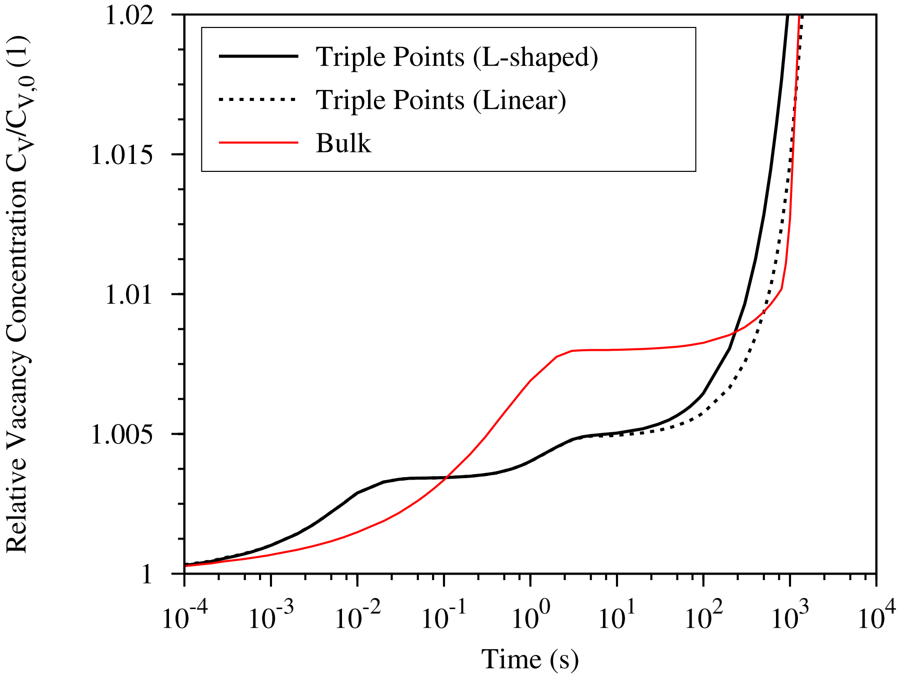


Figure 5.18: Maximum relative vacancy concentration change over time in the simulated structures. The peak values of vacancy concentration are extracted at the geometrical ends and at the triple points for both cases.

The time evolution of the maximum relative vacancy concentration in both linear and angled lines is illustrated in Figure 5.18. As expected, by monitoring the local change of vacancy concentration in time close to the cathode end of the line, the three stages of vacancy dynamics are observed (red curve in Figure 5.18). Such a behavior was already discussed in Section 5.1.2, where it was referred to as the quasi-steady state. When the primary material transport paths along which electromigration acts are recognized to be the grain boundaries and material interfaces, a different behavior in vacancy dynamics is observed (black curves in Figure 5.18). According to the models presented in Section 3.2.1 the difference in the vacancy dynamics for this case is due to the fact that grain boundaries and interfaces are able to trap and release vacancies with a rate which corresponds to the generation/annihilation term [40]. Since the value of release rate ω_R is much lower than the trapped rate ω_T (see Table 5.4), the trapped vacancy concentration within the triple point increases. The vacancy trapping/release events at the triple point lead to the generation of tensile stress. As observed in Figure 5.18, the peak vacancy concentration, extracted at the triple point, develops in a different manner compared to the trend shown for the vacancy concentration obtained at the geometrical end. In the latter the transition from the quasi-steady state to the phase of rapid growth of stress occurs later. According to this result, it is obvious that a defect site, such as a triple point, indicates the location where a rapid increase in stress and vacancy concentration initially takes place.

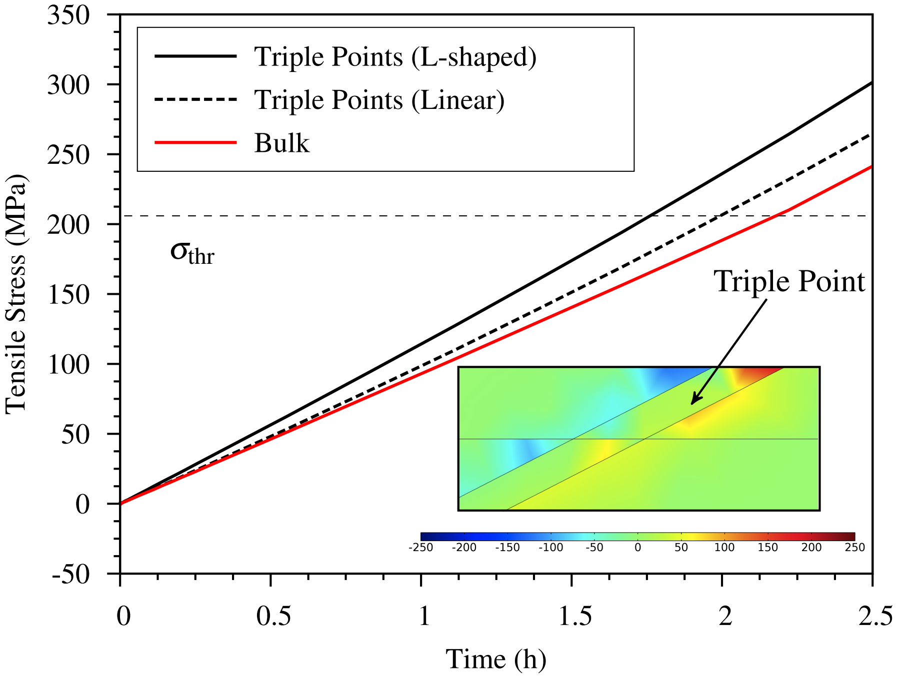


Figure 5.19: Time evolution of the maximum tensile stress in the analyzed structures. The peak values of tensile stress are extracted at the geometrical ends and at the triple points for both cases. The cross section view shows the hydrostatic stress distribution (MPa) in the region close to the triple point after 2.5 hours. The peak values of tensile stress are located inside the triple point.

The primary goal is to confirm that the triple point represents the site where the stress, and the consequent void nucleation, develops prior to other locations. The time evolution of the tensile stress in both structures is depicted in Figure 5.19. Using a threshold stress value σ_{thr} of 200MPa as the failure criterion, it is possible to conclude that the electromigration lifetime of the given structures is represented as the time required to reach the threshold value for void nucleation. The behavior of the stress evolution in the structure follows the local changes in time of vacancy concentration. As shown in Figure 5.19, the time necessary to reach the threshold stress for void nucleation at the triple point is lower compared to the time needed to reach the same stress value at the geometrical end of the lines. This means that a void most probably nucleates at sites away from the cathode end of the line. The stress build-up follows the increase in the trapped vacancy concentration and develops at the triple point, as can be seen in the cross section view of the triple point in Figure 5.19. As presented in Section 1.4.5 void nucleation is observed at locations where there is an available site of weak adhesion. Grain boundaries and material interfaces are typical features which provide such sites. In particular, triple points are formed by the intersection between grain boundaries and material interfaces and represent natural locations of weak adhesion. The simulation results are therefore able to explain the reason behind void nucleation at sites away from the geometrical ends of the lines.

Furthermore, by comparing the simulation results obtained for the linear and L-shaped geometries, the time needed to nucleate a stable void in linear geometries is more time than necessary for void nucleation in angled structures. This leads to a conclusion that void nucleation primarily occurs in L-shaped structures at the same applied stress conditions of increased temperature and current density. Under these stress conditions, it should be pointed out that the differences between failure times (i.e. void nucleation times) observed in the linear and angled interconnects are quite small, approximately in the range of minutes.

The introduction of the grain boundary network into the geometries, together with the application of grain boundary and material interface models, provides an improvement of the analysis and permits one to explain the experimental observations regarding electromigration-induced void nucleation. Electromigration voiding in the two simulated interconnect geometries is not determined by the presence of current crowding at the interconnect corner, but rather it depends on the influence of the grain boundary network, in particular triple points. In addition, with the help of this improved model, it is possible to determine the location of void nucleation in the structures and to provide a qualitative estimation of their lifetimes.

Chapter 6

Summary and Outlook

Moore's law has been a key indicator of the miniaturization trend of the transistor feature size for many decades. Since the continuous shrinking of transistor feature sizes and interconnect dimensions are approaching their physical limitations, Moore's law is expected to no longer be the main driving force for IC performance improvement. Alternative research directions for technological developments have been introduced to advance IC performance beyond only feature size scaling. One of those research domains, dubbed "More than Moore", has gained importance in recent years. It consists of the heterogeneous integration of multiple non-digital functionalities, such as sensors and MEMS, into devices and contributes to the functional diversification of technologies in a single package which do not scale according to Moore's law. A prominent strategy to continue along this trend is enabled through 3D integration technology. 3D integration is a new design paradigm which is based on the process of vertically stacking multiple functional technologies located at different planes of the chip and forming electrical connections between them, either through the silicon die or through the multilayer interconnect with an embedded die. Since the communication between the stacked sections of the chip requires vertical interconnections, a number of new interconnect designs have been introduced into the existing fabrication process flow to make 3D integration a reality, such as TSVs and solder bumps. Although 3D interconnects present distinct advantages, several reliability concerns, introduced from the fabrication process as well as from the device operating conditions, still occur in these emerging technologies. Electromigration-induced failure has been one of the main reliability issues in interconnects for 3D integration technologies since its potential degradation mechanism in metallization of ICs is initiated by the transport of atoms due to the high current density which passes through the metal film. Electromigration becomes a limiting factor for high current density flow in interconnects because it affects the long term interconnect behavior. As a consequence, more reliable interconnects, resistant against electromigration damage, must be developed in order to improve the technology lifetime.

The aims of this work were to investigate the physical mechanisms behind the electromigration induced degradation which influence the device lifetime and, consequently, its reliability. Traditionally, accelerated electromigration testing has been used to predict the electromigration lifetime of an interconnect. These experimental tests demand time, are expensive, and must be designed very carefully in order to ensure meaningful results for reliability evaluation. The use of modeling and simulation of the electromigration phenomenon is an alternative tool to aid in the design and fabrication of reliable metallizations and to understand the electromigration failure mechanisms with less time and cost than the experimental alternative. In this context, a description of the state-of-the-art modeling of electromigration was presented in detail, identifying its main advantages and weaknesses. The history of electromigration modeling has been treated starting from Black's equation to modern continuum models. Based on this groundwork, a fully 3D mathematical model for electromigration has been provided by taking into account the wide variety of physical effects which must be considered for the electromigration problem. Generally, electromigration modeling and simulation constitutes a multiphysics problem which can be separated into two main phases, namely, the early phase of void nucleation and the late phase of void evolution. During the first phase, the material transport caused by electromigration leads to a significant increase in the mechanical stress at those locations in the interconnect where the adhesion between the conducting metal and the surrounding material is weak. The build-up of mechanical stress induces the nucleation of voids inside the interconnect line. The second phase of failure involves the evolution of the void inside the metallization. During this phase, the mechanism of void growth leads to extremely large changes in the interconnect resistance until reaching a maximum value which does not fully interrupt the IC operation. The lifetime of the interconnect is then determined as the time needed to achieve the maximum critical value tolerable for a given circuit. The two-phase model equations were derived and numerically described using the finite element method. Then, the mathematical model for electromigration was implemented in a commercial TCAD tool which allows one to carry out numerical simulations. Electromigration simulations were performed for different case studies including an open TSV, a solder bump, and a corner interconnect with a defined microstructure. The devices vary in the way the electromigration failure is triggered.

Electromigration reliability was assessed for an open TSV structure, which represents one of the emerging interconnect technologies employed for 3D integration. For this purpose a two-step approach based on the full electromigration model has been employed. In the first step, the locations with the highest probability of void nucleation were identified by monitoring the stress build-up due to electromigration in the structure. Simulation results have shown that vacancy accumulation and the consequent development of mechanical stress are recognized to be close to the interface between the copper line and titanium nitride layer at the TSV bottom. This interface acts as an electromigration blocking boundary which stops the vacancy flux at the barrier layer. Therefore, vacancies accumulate at this location and lead to volume contraction of the structure resulting in the build-up of tensile stress. The electromigration void nucleation time is the time necessary to reach the threshold stress value for void nucleation. Assuming a critical stress in the order of 300MPa, the void nucleation time obtained for the case study varies between approximately one year and 80 days under accelerated conditions of current density j from 1MA/cm^2 to 2.2MA/cm^2, respectively. The second step of the analysis is characterized by the evolution of the void. Two methodologies have been employed in order to investigate resistance change due to the dynamics of void evolution in an open TSV structure. First, a diffuse interface method was developed to numerically study the time evolution of voids under electromigration in the open TSV structure. The second method consisted in the derivation of a semi-empirical analytic model based on the void radius dependence of the incoming vacancy flux due to electromigration to describe the time needed to grow a void of a given volume. A small initial void was placed at the void nucleation site, and its evolution was tracked, including the current-crowding effect and the resistance increase. When a current loading is applied to the edge of a conducting metal line, the electromigration force leads to the growth of the void, which spans the line, and triggers electrical failure. It has been shown that the electromigration driving force increases the void by feeding its surface with vacancies. From the simulation, it was determined that current crowding is more pronounced when the void becomes larger. As a result, interconnect resistance grows sharply as the line nears a failure. Interconnect resistance changes in time until it reaches the common failure criterion of a 20% increase in resistance. Electromigration void evolution time is related to the time elapsed until this value is reached. The void evolution time is at about the same order of magnitude as the void nucleation time, which suggests that both stages, void nucleation and void evolution, are important to determine the open TSV's time-to-failure. Once both void nucleation and void evolution times were obtained, the evaluation of the complete electromigration lifetime was completed and the results were fitted to Black's equation. A comparison of the simulation results with Black's equation revealed that the model based on the combination of kinetics of void nucleation and void evolution provides a good tool for the estimation of electromigration TTF in open copper TSV structures.

Another case study of particular interest was a flip-chip solder bump technology. A key feature of this structure is that electromigration failure is primarily determined by the void nucleation mechanism combined with the formation of an IMC at the interface between the Sn solder bump and the Ni UBM layer. Therefore, electromigration analysis was carried out by using the model describing void nucleation in order to simulate the mechanical stress build-up driven by the dynamics of vacancies in the solder bump. From the simulation results, the location of void nucleation was identified close to the interface between the solder and UBM layer. Furthermore, this location was also observed to be the region of current crowding. When a threshold stress in the order of 8MPa was reached at this site, the time necessary to nucleate a void was estimated in the range between 7 hours and 1 hour under stress conditions of current density from 0.003MA/cm^2 to 0.008MA/cm^2, respectively. The scope of this study was the development of an analytical compact model for the estimation of the lifetime of the solder bump. The compact model was designed by an adaptation of the Korhonen's model and it was calibrated through a comparison with the TTF/current density curves obtained from the simulation analysis. The developed compact model allows for the prediction of the void nucleation time and thereby provides a convenient method for the evaluation of the solder bump lifetime.

An original study regarding the impact of current crowding and microstructure on the electromigration damage was carried out. The analysis of electromigration failure was performed on two different interconnect geometries: a linear interconnect and an angled (or L-shaped) interconnect. The L-shaped geometry produced a high current crowding close to the corner of the structure and consequently an increased material transport induced by electromigration. This result suggests an increased electromigration degradation in the presence of right angles in the interconnect. However, experimental observations showed that no voids have been nucleated directly in the interconnect corner, but voiding appeared at random locations along the metal line. The inclusion of material interfaces and grain boundaries as paths of higher vacancy transport in the electromigration model was useful to explain some experimental observations of electromigration-induced voiding in the given interconnects. Simulations produced peaks in vacancy concentration and mechanical stress dynamics at the triple points formed by the intersection between the material interfaces and grain boundaries. Since triple points were considered to be sites capable of trapping and releasing vacancies, it was shown that void nucleation materialized at those locations, away from the cathode end of the line. This analysis demonstrated that electromigration voiding was not determined by the presence of current density divergence at the interconnect corner, but by the influence of the interconnect microstructure. Furthermore, assuming a threshold stress value for void nucleation of 200MPa, a failure occurred after operating under accelerated conditions for 2 hours and 100 minutes in the case of the straight and L-shaped geometries, respectively, when a current density of 4MA/cm^2 was applied. This leads to the conclusion that, even if a small difference in time between the two simulated structures is observed, the comparative study provided a qualitative estimation of their lifetimes.

The results obtained from the simulations of electromigration failure in the different case studies demonstrated the validity and capabilities of the TCAD electromigration model for the prediction of the electromigration lifetime of modern interconnects for 3D integration technology. In spite of the successful realization of interconnects for 3D integration and well-proven simulation models, further improvements should be considered both in the fabrication process as well as physical modeling. During the fabrication process, metal lines are deposited and covered with a passivation layer at a high temperature. Due to the large difference in thermal expansion coefficients between the metal line and surrounding material, a significant thermal stress is induced in the conducting line, when it is cooled to room temperature. In addition, the influence of a residual stress on the nucleation and propagation of voids in the metal line is present even in the absence of electric current and, therefore, electromigration. These stresses must be included in the simulation procedure. Future studies concerning the development of the electromigration model should address the extension of the void evolution model by including the gradient in electromigration-induced, thermal, and residual stress build-up as additional driving forces for the void evolution mechanism and to suit the model for 3D simulations. This task demands special numerical methods beyond FEM, such as the boundary-integral method. Furthermore, in real face-centered-cubic metals like copper, surface diffusion is strongly anisotropic and its impact on the electromigration-driven morphological evolution of voids has important consequences. Voids form in grains with a preference for certain crystallographic orientations and open circuit failure occurs when the void changes its shape to become a slit running perpendicular to the length of the metal line. Furthermore, it has been shown that the choice of appropriate crystal orientation with respect to the applied electric field might increase the lifetime of metal interconnects. Therefore, future works should address the effect of anisotropy and its implications for the void evolution problems.

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List of Publications

[1] **Rovitto, M.**, Papaleo, S., and Ceric, H. (2016). Diffuse Interface Model for Electromigration Void Evolution in Open Through Silicon Vias. *IEEE Trans. Device Mater. Rel*, submitted.

[2] Papaleo, S., Filipovic, L., Zisser, W. H., **Rovitto, M.**, Ceric, H., and Selberherr, S. (2016). Modeling Intrinsic Stress Build-Up During Tungsten Deposition in Open Through Silicon Vias. *Thin Solid Films*, submitted.

[3] **Rovitto, M.** and Ceric, H. (2016). Electromigration Induced Voiding and Resistance Change in Three-Dimensional Copper Through Silicon Vias. In *Proc. ECTC*, 550–556.

[4] Papaleo, S., **Rovitto, M.**, and Ceric, H. (2016). Mechanical Effects of the Volmer-Weber Growth in the TSV Sidewall. In *Proc. ECTC*, 1617–1622.

[5] Ceric, H., de Orio, R. L., and **Rovitto, M.** (2016). TCAD Approach for the Assessment of Interconnect Reliability. In *Proc. IRSP*, T21.

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[7] **Rovitto, M.**, Zisser, W. H., and Ceric, H. (2015). Analysis of Electromigration Void Nucleation Failure Time in Open Copper TSVs. In *Proc. IPFA*, 434–438.

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Curriculum Vitae

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