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Modeling the CMOS Inverter using Hybrid Systems

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1 Introduction

We are currently trying to determine the analog output of a CMOS inverter (see Figure 1) based on the analog input with as little effort as possible. Unfortunately an accurate formula $V_{out}(V_{in})$ can not be derived for the whole voltage range because the inverter, or more specifically the N- and PMOS transistors, have several operation regions with significantly different behavior. For that reason, we will primarily model the output voltage trajectory by applying the "Hybrid Systems" approach [3] studied by Sayan Mitra [4].

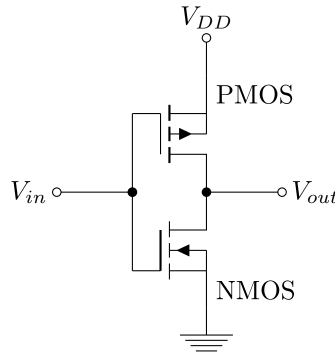

Figure 1: CMOS Inverter

This text is organized in the following way: Section 2 provides information on transistors and their operation regions. In Section 3 we derive a non-hybrid continuous model for an inverter, followed by a listing of applied simplification in Section 4. A detailed analysis of an appropriate hybrid model representation of the inverter is carried out in Section 5. For the constants used in the calculations measured values are presented in Section 6. At last a summary of the achieved guards, states and invariants as well as a graphic interpretation of the states is shown in Section 7.

2 Background

To describe the inverter appropriately it is first necessary to characterize single transistors, which was already carried out in detail in the past (see [6]). With decreasing feature size the characteristics of the field effect transistors however have changed significantly, making it necessary to adapt the formulas, as shown in [2]. This model is very accurate but requires thorough parametrization. Therefore, we use a simplification, presented for example in [5], here, which mainly considers effects due to carrier velocity saturation in the channel.

In general two kind of transistors are distinguished (Figure 2): PMOS and NMOS. Both can be in one of three operation regions: sub-threshold (ST),

Figure 2: CMOS Transistors

ohmic (OHM) and saturation (SAT).[1] In the first region (ST) the transistor is nearly an open circuit, i.e., only a very small amount of current is propagated. In the second region (OHM) the current is proportional to the applied voltage, and finally in the last one (SAT) the current is constant independently of the applied voltage. Table 1 shows the necessary conditions for each single region. V_G denotes the gate voltage and controls the conductance of the transistor. It is defined as the voltage difference between gate G and source S, where in the case of an NMOS this voltage is measured from G to S, i.e. $V_G = V_{GS}$, whereas it is measured from S to G, i.e., $V_G = V_{SG}$, for a PMOS. V_T, the so called threshold voltage, marks the point when the (ST) region is left. It can be assumed constant in this simplified model, albeit it differs between NMOS and PMOS transistors (denoted as V_{Tn} respectively V_{Tp}). V_D finally stands for the voltage difference between source S and drain D. For the NMOS it is measured from S to D, i.e., $V_D = V_{SD}$, and for the NMOS in the reverse direction, i.e., $V_D = V_{DS}$. In conjunction with the gate voltage, V_D determines the current that flows through the transistor. If V_D exceeds V_{Dsat}, providing a suitable V_G, the transistor enters the (SAT) region, thus delivering a constant current independent of V_D.

region	condition
(ST)	$V_G < V_T$
(OHM)	$V_G > V_T$ and $V_D < V_{Dsat}$
(SAT)	$V_G > V_T$ and $V_D > V_{Dsat}$

Table 1: Operation regions of NMOS and PMOS transistors

To model modern devices perfectly a lot of different short channel and narrow width effects have to be considered. Some, but not nearly all of them, have been considered in [1], which yields less complex formulas that will be used in the following. They were chosen because no fitting parameters are required while improving the accuracy significantly. An even more elaborate model based on physical parameters can for example be found in [2].

In the subthreshold region the transistor is assumed to behave as an open circuit, i.e., that

[1] Please note that the break through regions for very high or low gate voltages are not considered here.

$$I_D = 0 \tag{1}$$

holds. In the ohmic region the current is calculated as

$$I_D = \left(\frac{\mu_s\, C_{ox}\, W}{L}\right) \left(1 + \frac{\mu_s}{L\, v_{sat}} V_D\right)^{-1} (V_G - V_T - 0.5\alpha V_D) V_D \tag{2}$$

Beside the width (W), length (L) and gate oxide capacitance per unit area (C_{ox}) the saturation velocity (v_{sat}) and the low field mobility

$$\mu_s = \frac{\mu_0}{1 + \theta(V_G - V_T)}$$

is used. θ is an empirical parameter in the range of $0.03 \ldots 0.1 V^{-1}$. Please note that these parameters are all different for N- and PMOS. This will be indicated in the following by subindices $_n$ respectively $_p$.

By defining I_{Dsat} according to Eq. (2) with $V_D = V_{Dsat}$ the current in the saturation region can be expressed as

$$I_D = I_{Dsat} \frac{L}{L - l_d} \tag{3}$$

with

$$l_d = \sqrt{\frac{V_D - V_{Dsat}}{a}} \quad , \quad a = \frac{qN_b}{2\epsilon_0 \epsilon_{si}}$$

In this formula the increase of the current in the saturation region due to short channel effects is considered by the parameter l_d which uses the electron charge (q), the bulk doping (N_b) and the dielectric permittivity of silicon (ϵ_{si}). The saturation voltage, i.e., the value of V_D when the transistor enters the saturation region, is thereby defined as

$$V_{Dsat} = \left(\frac{L\, v_{sat}}{\mu_s}\right) \left(\left[1 + 2\frac{\mu_s}{\alpha\, L\, v_{sat}}(V_G - V_T)\right]^{1/2} - 1\right) \tag{4}$$

In Section 6 suitable values for the parameters presented so far for to the utilized technology will be presented.

3 Uniform Transistor Model

The main difficulty when calculating the trajectory of the output voltage arises from the different operation regions of the single transistors with their individual current formulas. This problem is avoided by the uniform model presented in [1], which uses a single expression for all three operation regions. In detail it is just a slightly modified version of Eq. (2), more specifically

$$I_D = \frac{W\,\mu_s\,C_{ox}}{(L-l_d)}\left(1+\frac{V_{Dx}\,\mu_s}{(L-l_d)v_{sat}}\right)^{-1}(V_{Gx}-V_T-0.5\,\alpha\,V_{Dx})V_{Dx}$$

Herein $V_{Gx} = V_{Gx}(V_G)$ and $V_{Dx} = V_{Dx}(V_D)$ denote functions that realize smooth transitions defined as

$$V_{Gx}(V_G) = \eta\,V_t\,ln\left[1+exp\left(\frac{V_G-V_T}{\eta\,V_t}\right)\right]+V_T$$
$$V_{Dx}(V_D) = V_{Dsat}\left\{1-\frac{1}{B}ln\left[1+e^{A(1-V_D/V_{Dsat})}\right]\right\}$$

V_{Dsat} is still computed according to Eq. 4 with V_G replaced by V_{Gx}. For l_d a differing approach can be used in this case, i.e.,

$$l_d = L\,ln\left[1+\left(\frac{V_D-V_{Dsat}}{V_P}\right)\right]$$

with V_P being a fitting parameter, which will be defined in Section 6.

In V_{Dx} two additional parameters, namely A (a constant) and $B = ln(1+e^A)$, are introduced. A large value of A thereby marks a steep transition between the linear and saturation region whereat a small one reults in smooth transition. A typical value is $A = 10$. For high values of V_D the transistor operates in its (SAT) region and V_{Dx} collapses to V_{Dsat}. The achieved results are very similar to the ones of Eq. (3), only differing in the applied length scaling. As V_D decreases and approaches zero, also V_{Dx} drops, resulting in no output current. This is according to the real world behavior.

In V_{Gx} the parameter $\eta = 1+\frac{C_d}{C_{ox}}$ is used with C_d being the depletion region capacitance. Typical values range from 1 to 3. V_t represents the thermal voltage $\frac{k_B\,T}{q}$ which is about 26 mV at room temperature. For high values of V_G the expression can be reduced to $V_{Gx} = V_G$, for small values V_{Gx} approaches V_T. By plugging $V_{Gx} = V_T$ into Eq. (4) it can be observed that V_{Dsat} becomes zero, resulting in no current. Again this is in accordance to the behavior of an actual transistor.

4 Model Refinement

In the formulas presented in Section 2-3 several simplifications have been applied to keep the resulting expressions as simple as possible. However, they could be lifted to achieve an even more accurate model:

- The subtreshold current, i.e. when the transistor is in its (ST) region, is not considered because the current for completely transparent transistors is in general several magnitudes bigger.
- The formulas for the current presented earlier are only valid for the static case. For precise dynamic analysis one would also have to consider the capacitances inside the circuit, as these consume or provide additional currents. A detailed analysis of those is also provided in [6]. For simplicity reasons they are neglected for now, except for the external output capacitance C_L.

5 Hybrid Model

In the following the inverter shown in Figure 3 shall be described using the hybrid model. Therefore it has to be defined in which regions the single transistors operate and how the resulting current looks like, which will eventually lead to seven different states A-G (see Figure 4). The output voltage is thereby derived according to the capacitance equations as

$$C_L \frac{\mathrm{d}}{\mathrm{d}t} V_{out} = I_{out}$$

meaning that a positive output current charges the capacitance and a negative one discharges it. Due to this definition I_{out} can be defined as

$$I_{out} = I_{PMOS} - I_{NMOS}$$

which is shown in Figure 3. As already mentioned these currents depend on the operation region and the type of the single transistors. In the following the subindices $_n$ and $_p$ will be used for N- respectively PMOS transistor and the operation region will be stated in parantheses, e.g $I_{Dn}(OHM)$ for an NMOS in its ohmic region or $I_{Dp}(SAT)$ for a PMOS in saturation. Further it has to be noticed that for NMOS transistors V_G has to be substituted by V_{in} and V_D by V_{out}. For PMOS ones V_G has to replaced by $V_{DD} - V_{in}$ and V_D by $V_{DD} - V_{out}$.

The possible states of the circuit are analyzed and described in detail in the successive subsections, which follow the naming scheme

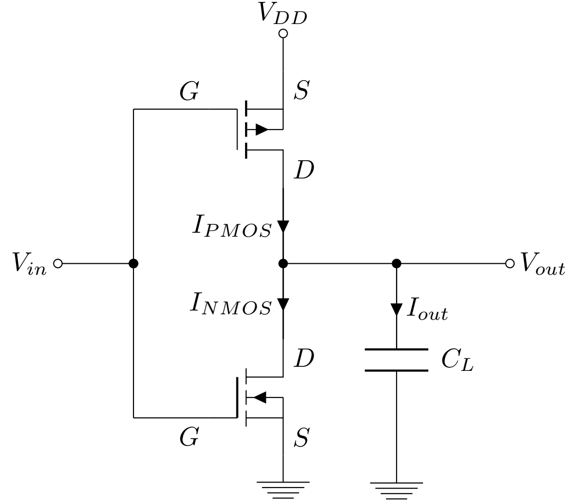

Figure 3: CMOS Inverter showing currents and attached capacitance

"State" <name> <operation region PMOS>, <operation region NMOS>

Please note that in Section 7 a summary of the most important parameters as well as a graphical representation is presented. These might already be sufficient for some readers or, if that is not the case, might help to properly understand the relations between the single states.

Furthermore it is important to consider, that for each single state only the guards are presented. It is however necessary to leave each state immediately after the first guard triggered because otherwise it might happen that several guards are activated simultaneously and the scheduler then decides indeterministically on the succeeding state and the switching time, which however does not represent a valid physical solution. For that purpose the opposite of each guard is also implemented as invariant, i.e., $X > Y$ is complemented by the invariant $X \leqslant Y$ and $X < Y$ by $X \geqslant Y$.

5.1 State A (OHM), (ST)

Let us assume for this first state that the input is LO, i.e. at ground voltage, and the output is HI, i.e. at V_{DD}, causing the PMOS to be in its (OHM) and the NMOS in its (ST) operation region. By applying the corresponding formulas stated earlier the output current evaluates to

$$I_{out} = I_{Dp}(OHM)$$

Please note, that this state is actually valid for all values $V_{DD} - V_{Dsatp} <$

$V_{out} < V_{DD}$ and $0 < V_{in} < V_{Tn}$. The first condition — stating that V_{out} drops below $V_{DD} - V_{Dsatp}$ while $V_{in} < V_{Tn}$ — can however only be violated in theory and not in physical circuits, due to the fact that according to our simplifications, the NMOS is completely closed in this case, so only a charging current to the output capacitance is possible. Therefore the only way to leave this state is by violating the second condition, i.e. by increasing V_{in} above V_{Tn}. Therefore the single guard[2] for leaving this state can be written as

name	condition	goal state
A1	$V_{in} > V_{Tn}$	B

Please note that a state with $V_{out} < V_{DD} - V_{Dsatp}$ and $0 < V_{in} < V_{Tn}$ — as will be defined later as state C — does indeed exist, however it is not reachable from this state, but only for an input voltage that drops below V_{Tn}.

5.2 State B (OHM), (SAT)

As the input voltage V_{in} rises above V_{Tn} while being in state A the NMOS starts to conduct, whereat it is immediately operating in its (SAT) region. Due to the fact that the PMOS stays in its (OHM) region the output current I_{out} results to

$$I_{out} = I_{Dp}(OHM) - I_{Dn}(SAT)$$

This state is left if (i) V_{in} drops again below V_{Tn} causing the NMOS to switch back to its (ST) operation region, or (ii) if $V_{DD} - V_{Dsatp} > V_{out}$ becomes true. In the latter case the output voltage drops to the point where the PMOS enters its (SAT) region. Please note that theoretically it would also be possible to leave this state as the NMOS reaches its (OHM) operation region, i.e., when $V_{out} < V_{Dsatn}$ becomes true. This condition however can only be satisfied after the change of the PMOS at $V_{DD} - V_{Dsatp} > V_{out}$, resulting in the above mentioned state switch, according to (ii): After all, we have a rising input transition and thus a falling output one, and both saturation voltages are smaller than $V_{DD}/2$. Overall the guards for leaving this state are

name	condition	goal state
B1	$V_{in} < V_{Tn}$	A
B2	$V_{DD} - V_{Dsatp} > V_{out}$	D

[2]The notation for the guards is the region name followed by an increasing number starting with 1.

5.3 State C (SAT), (ST)

This state can only reached from state D by a steep falling input transition compared to the output one and represents the case that the NMOS is in its (ST) and the PMOS in its (SAT) operation region. Due to these facts the output current results to

$$I_{out} = I_{Dp}(SAT)$$

If V_{in} stays below V_{Tn} then V_{out} will eventually reach the point where the PMOS enters its (OHM) region (i.e. $V_{DD} - V_{Dsatp} < V_{out}$). If V_{in} starts rising fast enough, however, it is possible that the NMOS enters its (SAT) operation region. The guards for this state therefore are

name	condition	goal state
C1	$V_{DD} - V_{Dsatp} < V_{out}$	A
C2	$V_{in} > V_{Tn}$	D

5.4 State D (SAT), (SAT)

In this state, finally both transistors operate in their (SAT) region. This leads to an output current of

$$I_{out} = I_{Dp}(SAT) - I_{Dn}(SAT)$$

Depending on the behavior of the input different successor states are possible. If the input rises very fast, $V_{in} > V_{DD} - V_{Tp}$ becomes true causing the PMOS to enter its (ST) region. If the rising input slope is small however the condition $V_{out} < V_{Dsatn}$ will be fulfilled first, causing the NMOS to enter its (OHM) operation region. When V_{in} decreases while in state D it is possible — with appropriate values of V_{Tn} and V_{Tp} as well as fitting input and output slopes — that V_{in} drops below V_{Tn} without falsifying the condition $V_{DD} - V_{Dsatp} > V_{out}$. In that particular case the NMOS enters its (ST) region while the PMOS stays in (SAT). If the condition is violated before the input reaches V_{Tn} however then a switch to state B takes place. Overall the guards for leaving state D are

name	condition	goal state
D1	$V_{DD} - V_{Dsatp} < V_{out}$	B
D2	$V_{in} < V_{Tn}$	C
D3	$V_{out} < V_{Dsatn}$	E
D4	$V_{in} > V_{DD} - V_{Tp}$	F

5.5 State E (SAT), (OHM)

When starting in state D and V_{out} drops below V_{Dsatn} the NMOS enters its (OHM) region, while the PMOS stays in its (SAT) one. The current then results to

$$I_{out} = I_{Dp}(SAT) - I_{Dn}(OHM)$$

If V_{in} further increases $V_{in} > V_{DD} - V_{Tp}$ eventually becomes true causing the PMOS to close, i.e. enter its (ST) operation region. The other possibility, of course, is to reduce V_{in} again until the NMOS returns to its (SAT) operation region. The guards for this state are

name	condition	goal state
E1	$V_{out} > V_{Dsatn}$	D
E2	$V_{in} > V_{DD} - V_{Tp}$	G

5.6 State F (ST), (SAT)

This state is solely reachable from state D by a rising input transition that is steep compared to the output one and represents the case where the NMOS is in its (SAT) region while the PMOS is not conducting, i.e. in its (ST) region. Considering these circumstances the current results to

$$I_{out} = -I_{Dn}(SAT)$$

As V_{in} increases the output voltage drops below V_{Dsatn} causing the NMOS to enters its (OHM) region. If V_{in} drops however, it will eventually become smaller than $V_{DD} - V_{Tp}$ causing the PMOS to enter its (SAT) operation region. Therefore the guards for leaving state F are

name	condition	goal state
F1	$V_{in} < V_{DD} - V_{Tp}$	D
F2	$V_{out} < V_{Dsatn}$	G

5.7 State G (ST), (OHM)

Finally, when the transition is nearly finished, this state is entered where the NMOS operates in its (OHM) and the PMOS in its (ST) region. The current then results to

$$I_{out} = -I_{Dn}(OHM)$$

The only way to leave this state is to reduce V_{in} below $V_{DD} - V_{Tp}$ such that the PMOS starts conducting again. It is not possible to drive the NMOS back into its (SAT) operation region since this is equivalent to increasing V_{out} for $V_{in} > V_{DD} - V_{Tp}$. For this input voltage, however, solely the NMOS is conducting, making it only possible to discharge the capacitance at the output. Considering this the single guard is

name	condition	goal state
G1	$V_{in} < V_{DD} - V_{Tp}$	E

6 Parameter Values

Lots of parameters have been used in the formulas of Section 2. Therefore reasonable values suitable for the technology used in the simulations are presented in this section. Some of them can be directly derived from SPICE parameters like the width (W) and length (L) of the MOSFETs, the low field mobility mu_0 (SPICE: $u0$), the bulk doping N_b (SPICE: $ndep$), and the gate capacitance per unit area $C_{ox} = \epsilon_{ox}/t_{ox}$ (SPICE: $epsrox/toxm$). The corresponding values can be found in table 2.

	$\mu_0\,[cm^2/Vs]$	$C_{ox}\,[F/cm^2]$	$W\,[cm]$	$L\,[cm]$	$N_b[cm^{-3}]$
NMOS	349.85	$1.5\,e9$	$4.5\,e{-5}$	$6\,e{-6}$	$1.68\,e17$
PMOS	104.45	$1.42\,e9$	$6.3\,e{-5}$	$6\,e{-6}$	$3.99\,e17$

Table 2: Parameters determined from SPICE parameters

Other parameters, especially the empirical ones, were not so easy to derive. It was, for example, necessary to estimate the values for α and θ since empirical

data was missing. a was computed using the electron charge $q = 1.602 \times 10^{-19}$ J as well as the permittivity values $\epsilon_{si} = 11.68$ and $\epsilon_0 = 8.854 \times 10^{-14}$ F/cm. Unfortunately the result were not reasonable, which made it necessary to estimate suitable ones. The threshold voltage V_T, in contrast, was fitted to simulation results. The corresponding values can be found in Table 3.

	α	θ	$a\,[V/cm^2]$	$v_{sat}\,[cm/s]$	$V_T\,[V]$	η	$V_t\,[V]$	A	$V_P\,[V]$
NMOS	1	0.6	$1\,e11$	$8\,e6$	0.4	1.5	$26\,e{-3}$	10	1
PMOS	1	0.8	$1\,e11$	$6\,e6$	0.47	1.5	$26\,e{-3}$	10	1

Table 3: Parameters determined from simulations or assumptions

7 Summary

The above described states A-G are all reachable ones, meaning that only seven of the possible $3^2 = 9$ states are valid. The state where both NMOS and PMOS are in their (ST) region would be only reachable if $V_{Tn} > \frac{V_{DD}}{2}$ and $V_{Tp} > \frac{V_{DD}}{2}$, which is however not reasonable in real applications. Similarly the state where both are in their (OHM) region requires $V_{Dsatp} > \frac{V_{DD}}{2}$ and $V_{Dsatn} > \frac{V_{DD}}{2}$, which is not achieved by a large margin in modern technologies. This was also verified by simulations. Please note that the same set of states is achieved if the transition starts from a HI input signal and a LO output one, with the only difference that they occur in the reverse order.

Tables 4 and 5 finally summarize all important parameters in each state. The saturation voltages for N- and PMOS can be calculated as

$$V_{Dsatp} = \left(\frac{L_p\, v_{satp}}{\mu_{sp}}\right) \left(\left[1 + 2 \frac{\mu_{sp}}{\alpha_p\, L_p\, v_{satp}} (V_{DD} - V_{in} - V_{Tp}) \right]^{1/2} - 1 \right)$$

and

$$V_{Dsatn} = \left(\frac{L_n\, v_{satn}}{\mu_{sn}}\right) \left(\left[1 + 2 \frac{\mu_{sn}}{\alpha_n\, L_n\, v_{satn}} (V_{in} - V_{Tn}) \right]^{1/2} - 1 \right)$$

from state	guard name	condition	to state
A	A1	$V_{in} > V_{Tn}$	B
B	B1	$V_{in} < V_{Tn}$	A
	B2	$V_{DD} - V_{Dsatp} > V_{out}$	D
C	C1	$V_{DD} - V_{Dsatp} < V_{out}$	A
	C2	$V_{in} > V_{Tn}$	D
D	D1	$V_{DD} - V_{Dsatp} < V_{out}$	B
	D2	$V_{in} < V_{Tn}$	C
	D3	$V_{out} < V_{Dsatn}$	E
	D4	$V_{in} > V_{DD} - V_{Tp}$	F
E	E1	$V_{out} > V_{Dsatn}$	D
	E2	$V_{in} > V_{DD} - V_{Tp}$	G
F	F1	$V_{in} < V_{DD} - V_{Tp}$	D
	F2	$V_{out} < V_{Dsatn}$	G
G	G1	$V_{in} < V_{DD} - V_{Tp}$	E

Table 4: Guards of each state

state	invariant name	condition
A	AI1	$V_{in} \leqslant V_{Tn}$
B	BI1	$V_{in} \geqslant V_{Tn}$
	BI2	$V_{DD} - V_{Dsatp} \leqslant V_{out}$
C	CI1	$V_{DD} - V_{Dsatp} \geqslant V_{out}$
	CI2	$V_{in} \leqslant V_{Tn}$
D	DI1	$V_{DD} - V_{Dsatp} \leqslant V_{out}$
	DI2	$V_{in} \geqslant V_{Tn}$
	DI3	$V_{out} \geqslant V_{Dsatn}$
	DI4	$V_{in} \leqslant V_{DD} - V_{Tp}$
E	EI1	$V_{out} \leqslant V_{Dsatn}$
	EI2	$V_{in} \leqslant V_{DD} - V_{Tp}$
F	FI1	$V_{in} \geqslant V_{DD} - V_{Tp}$
	FI2	$V_{out} \geqslant V_{Dsatn}$
G	GI1	$V_{in} \geqslant V_{DD} - V_{Tp}$

Table 5: Invariants of each state

Table 6 shows I_{out} for each state separately. For better readability the expressions $I_p(V_D)$ and $I_n(V_D)$, obtained from Eq. (2) by plugging in $V_G = V_{DD} - V_{in}$ and $V_G = V_{in}$ respectively, are used.

$$I_p(V_D) = \left(\frac{\mu_{sp}\, C_{oxp}\, W_p}{L_p}\right) \left(1 + \frac{\mu_{sp}}{L_p\, v_{satp}} V_D\right)^{-1} (V_{DD} - V_{in} - V_{Tp} - 0.5\alpha V_D) V_D$$

$$I_n(V_D) = \left(\frac{\mu_{sn}\, C_{oxn}\, W_n}{L_n}\right) \left(1 + \frac{\mu_{sn}}{L_n\, v_{satn}} V_D\right)^{-1} (V_{in} - V_{Tn} - 0.5\alpha V_D) V_D$$

$$l_{dp} = \sqrt{\frac{V_D - V_{out} - V_{Dsatp}}{a}} \qquad l_{dn} = \sqrt{\frac{V_{out} - V_{Dsatn}}{a}}$$

state	I_{out}
A	$I_p(V_{DD} - V_{out})$
B	$I_p(V_{DD} - V_{out}) - I_n(V_{Dsatn})\frac{L}{L-l_{dn}}$
C	$I_p(V_{Dsatp})\frac{L}{L-l_{dp}}$
D	$I_p(V_{Dsatp})\frac{L}{L-l_{dp}} - I_n(V_{Dsatn})\frac{L}{L-l_{dn}}$
E	$I_p(V_{Dsatp})\frac{L}{L-l_{dp}} - I_n(V_{out})$
F	$-I_n(V_{Dsatn})\frac{L}{L-l_{dn}}$
G	$-I_n(V_{out})$

Table 6: I_{out} in each state

Figure 4 shows a graphical interpretation of the states and their interconnections. The labels at the edges mark the guards that have to be violated for the transition to occur. In the nodes the state as well as the operation region of both transistors is shown.

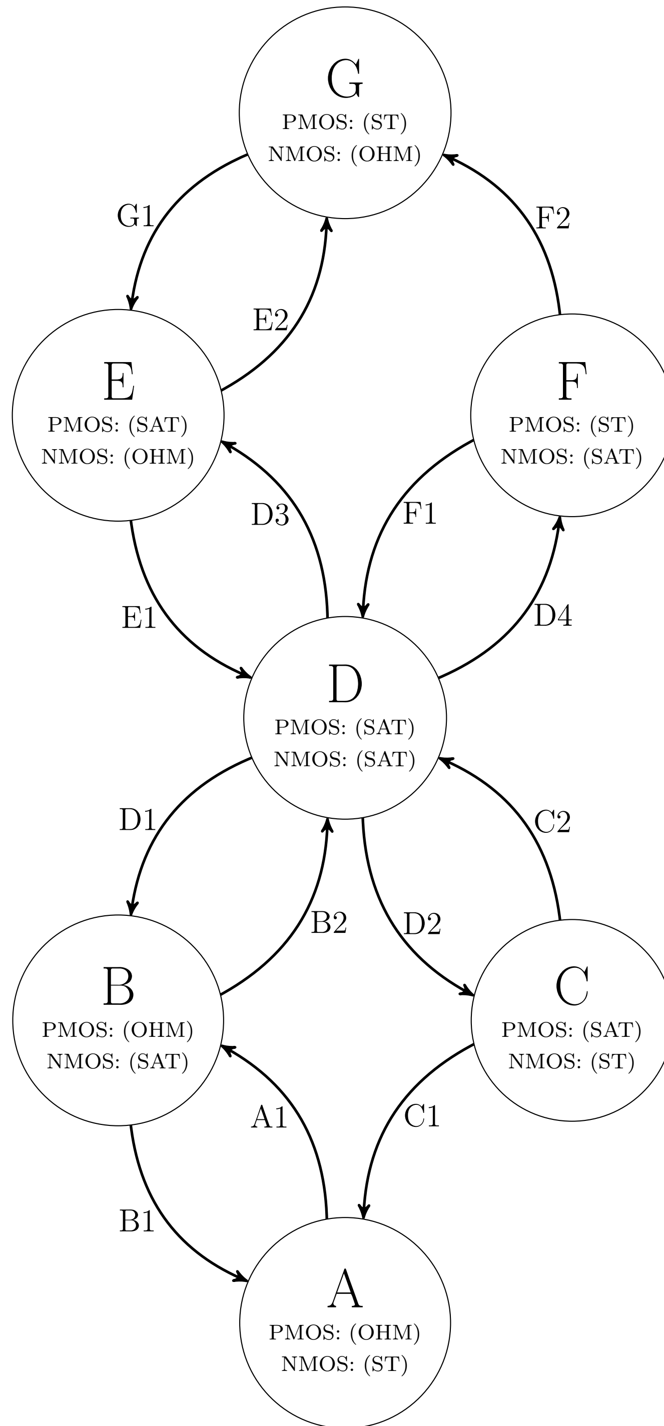

Figure 4: graphic representation of state model, nodes contain state name as well as operation region of NMOS and PMOS

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