TECHNISCHE UNIVERSITÄT WIEN

Diplomarbeit

Regelung von Schaltverstärkern mit Ausgangsfiltern höherer Ordnung

Control of Switched-Mode Power amplifier with High-Order LC output filter

ausgeführt zum Zwecke der Erlangung des akademischen Grades eines

Diplom-Ingenieurs

unter der Leitung von

Ao. Univ. Prof. Dipl.-Ing. Dr. techn. Johann Ertl

(E370 - Institut für Energiesysteme und Elektrische Antriebe)

eingereicht an der Technischen Universität Wien

Fakultät für Elektrotechnik und Informationstechnik

von

Mohammad Sadigh Eisazadeh

Matr.Nr. (1329830)

Wien, im February 2019

_____

Mohammad Sadigh Eisazadeh

Mohammad Sadigh Eisazadeh 1329830

TECHNISCHE UNIVERSITÄT WIEN

Ich habe zur Kenntnis genommen, dass ich zur Drucklegung meiner Arbeit unter der Bezeichnung

Diplomarbeit

Hiermit erkläre ich, dass die vorliegende Arbeit "*Regelung von Schaltverstärkern mit Ausgangsfiltern höherer Ordnung*" ohne unzulässige Hilfe Dritter und ohne Benutzung anderer als der angegebenen Hilfsmittel, angefertigt wurde. Die aus anderen Quellen direkt oder indirekt übernommenen Daten und Konzepte sind unter Angabe der Quelle gekennzeichnet.

Die Arbeit wurde bisher weder im In– noch im Ausland in gleicher oder in ähnlicher Form in anderen Prüfungsverfahren vorgelegt.

Wien, im February 2019

_____

Mohammad Sadigh Eisazadeh

Mohammad Sadigh Eisazadeh 1329830

Acknowledgment

I am deeply grateful to my supervisor Professor Dipl.-Ing. Dr. techn. Johann Ertl at Vienna University of Technology for his positive attitude, encouragement and, providing me such a good opportunity to do this interesting research project and for reviewing my thesis report. The door to Prof. Ertl office was always open whenever I ran into a trouble spot or had a question about my work. I also thank all the M.Sc. Thesis Committee members for reviewing this report.

I am grateful to my best friends, Mahdi Omidi and Behzad Parvin at Vienna University of Technology for their help and encouragement during last three years.

Finally, for their love, support and encouragement, no matter what the circumstance, my family, especially my parents receive my appreciation and gratitude that can't be expressed by words. Without their support it would have been impossible to finish my study abroad.

Abstract

A Class-D amplifier is a technical realization of a power amplifier that today can combine most of the requirements simultaneously such as efficiency and stability, compared to traditional linear amplifiers.

The goal is to redesign the Class D amplifier using higher and more complex filters and to consider the final system for inputs and loads in terms of stability, sustainability boundaries, and as far as possible ideal output signals.

We focused on the output filter of this amplifier and try to improve the output signal. In this work different Butterworth filters including 2nd order, 4th order and two 2nd order in series are used and the result are having been compared. Our method in this thesis is to obtain the circuit parameters in order to design the system for each filter, which we will then find the system transfer function and use it to calculate the parameterized the system.

After completing design of each filter, several PSpice simulations were created. These simulations allowed for various methods and components to be tested, ultimately saving valuable time in the final design. Finally, each system in no load condition and with different load types were tested.

Thus, the second order filter case had the least time-lag while the 4th order filter cases have higher time-lag. In other words, the higher the order of system, the more time-lag the step response shows. This means one of the disadvantages of the higher order system is that the response of system will be slower. On the other hand, the fact that a higher order system can remove the snitching noise, is a great advantage.

The result was that the amplifier met most of the specifications. In other word, the theory behind the design does prove that the performance and implementation is achievable.

Table of Contents

List of Figures

List of tables

List of abbreviations

MOSFET	Metal oxide semiconductor field effect transistor
BJT	Bipolar Junction Transistor
LPF	Low pass Filter
CDA	Class-D amplifier
SPS	switching power supply
PA	Power amplifier

1 Introduction

1.1. Background and introduction

In many technical applications, electrical signals must be amplified to achieve specific purpose. For this reason, so-called power amplifiers are used. Today, power amplifiers have become one of the most important electronic power devices due to their applications in industry, and we have seen significant advances in this area in recent years. If we take a glance at the history of power amplifiers, it's clear that over time, the features of power amplifiers have been improved.

Amplifiers have to fulfill various requirements at the same time, such as:

- They should change the original signal as little as possible,
- They should have high efficiency at low cost,
- They should cause a low amount of electromagnetic interference, and
- They should be small in size while maintaining high performance.

Especially in mobile applications, the efficiency and the size are decisive factors for the choice of technology used. Nowadays, we achieve high power, low weight, high efficiency and high reliability with low heat losses in power amplifiers and this route continues. A Class-D amplifier is a technical realization of a power amplifier that today can combine most of the above requirements simultaneously. Class-D amplifiers were first invented, proposed and developed in the year 1958. Regarding very high losses of the used bipolar BJT, Class-D amplifier had a very poor results. Finally, MOSFETs were produced in 1960 and they were in the Market first in 1970, so by this time, the biggest hurdle (losses) had already been decreased significantly and it was possible to achieve up to 90% efficiency. As a result, Class-D amplifiers became popular in the following years and formed the most basic components in all of the electronic systems.

It is also one of the most recent amplifiers that is used extensively because of its high efficiency, which can reach up to 100% when designed theoretically and can reach up to over 90% when it is put to the test and in practice. Losses in this amplifier have been greatly reduced because of using MOSFETs for switching. However, the Class-D amplifier comes at a cost. One must pay a price for this high degree of efficiency. This amplifier has more of a complex design compared to the other types of amplifiers, and this makes it expensive. Class-D amplifier for modulation, PMW (Pulse width modulation) method is used, which, consequently, requires an output filter for "demodulation" the pulse signal in the analog output signal.

For demodulation the signal Class-D amplifier's output use a variety of options such as multi-stage, Hybrid filters. Frequently, low pass filters, as the Butterworth filter are chosen, which is used also in this thesis.

1.2. Motivation and thesis goal

The main purpose of this work is to study the possibilities of designs and to find a way to implement them using a switched-mode power amplifier and a low pass filter. By providing a new design for a Class-D amplifier with high order output filter, we intend to improve system stability and increase its efficiency, as well as give a plan for reducing losses and idealizing amplifier output.

In a previous thesis on Class-D amplifiers, a lot of the applications of this amplifier were considered as, e.g. audio amplifiers. Also, in most studies, they have been used applying second-order outputs filter. But in this thesis, our main focus is on designing the system using high-order filters. The goal is to redesign the system using higher and more complex filters and to consider the final system for inputs and loads in terms of stability, sustainability boundaries, and as far as possible ideal output signals.

In order to do this, we will focus on the output filter of this amplifier and try to improve the output signal. We chose the Butterworth filter as an output filter because compared to other types of filters, this one has a monotonic amplitude response and it has a quick roll-off around the cut-off frequency, which improves with increasing the order of the filter.

In the first step, we designed and simulated the amplifier using the Butterworth second-order filter, then we figured out the transfer function. By using the transfer function and by making some comparisons, we found the unknown parameters of the circuits, like L and C. Finally, we simulated the circuit and we discussed the output signal of the amplifier in real time for both the power supplies. The stability of the system was also discussed.

The next step was to use the fourth order filter in the design of the amplifier. Similar to the system with second-order filters, we designed, parameterized and simulated the system and discussed the results of both the real time and frequency area.

Finally, we used two second-order filters in series and did the same thing as we did in the previous steps. At the end we made comparisons between these three types of filters.

Our method in this thesis is to obtain the circuit parameters in order to design the system for each filter, which we will then find the system transfer function and use it to calculate the parameterized the system.

1.3. Outlines and thesis structure

The objective task of this project is to develop a functional Class-D amplifier. The circuit is first simulated in the electronics simulator Pspice from the outset to draw attention to errors in the design. After a brief introduction on this thesis, Chapter 2 will provide an overview of the basic principles of amplifiers such as classification of amplifiers, power efficiency, energy balance and effect of loads, the principle of operating a Class-D amplifier and essential components, as well as the design of the Butterworth filter with and without active damping. The general operation and performance of a Class-D amplifier will be stated and compared with linear amplifiers, and the switched-mode amplifier will also be discussed. This will be focused mainly on the power efficiency of the particular amplifier. Discussion on the dissipation of power amplifiers and increasing efficiency on the Class-D amplifier will also be included in Chapter 2. Additionally, a summary of the design theory that will be used in designing this Class-D amplifier will be included. This will state the derivation of a Class-D operation concept from an AC-AC converter, methods of modulation such as PWM, output filter design considerations, and a close loop control.

In Chapter 3, the case study, principles of operation of the Class-D amplifier will be discussed. The detail of the design approach, calculating transfer functions and analysis of systems in frequency domain, and the selection of components will be also stated in this Chapter. The design approach will break into difference stages accordingly. From the input stage or PWM stage, power driver stage, demodulation stage or output filter stage as well as the close loop control for the entire circuit design will be enclosed.

In Chapter 4, the Class-D amplifier with the desired methods of control for three different types of Butterworth output filters will be discussed. First, a Class D amplifier with a second order Butterworth will be designed. Then we will increase the order of the Butterworth filter and design the system with a fourth order Butterworth filter. The final attempt will be to redesign the system with two second order Butterworth filters in series.

In Chapter 5, the three designed systems will be tested in no load condition and with different loads. The result found from the testing of the design will be discussed and compared. Based on these results, a discussion on the close loop design as well as the circuit performance and output signal for mentioned controllers will be stated. Finally, based on the testing result, we will conclude with which controller regarding the stability of closed-loop design, is able to increase the performance of the existing Class-D amplifier more efficiently.

2. Basic principles of amplifiers

Amplifiers are still the most common electronic circuits that are used in most electronic devices we have today. An amplifier by itself is a device that increases the power of the reference signal. It increases the amplitude of the signals involved and makes them stronger by using amplification, thus creating a stronger output signal. An amplifier only increases the amplitude of a signal; it should not change any other parameters of the waveform such as the frequency or the wave shape. The main characteristics of most amplifiers are efficiency, linearity, signal gain, and the power output. To design an ideal amplifier, the reference signal must be amplified in such a way that the output signal is identical to the input signal. In order to achieve this, the amplifiers should be minimally distorted, they should not change the original signals in any form, whether it be a linear or even non-linear reference signal, and the impact of noises should be minimized, while at the same time the system should be kept stable and reliable for different loads. Also, the amplifier should characterize by a very high degree of efficiency at a much-reduced cost. In some applications like mobile applications, the amplifiers have a very small design that have a high efficiency. Therefore, the low heat wasted, as well as the achievable power density, are very important, especially for an audio system. A Class-D amplifier, which we will introduce later, is a very successful technical realization that is able to combine several of the factors discussed above.

Many amplifiers usually need to produce an output power in the region of 1 watt to a maximum of several hundreds of watts. However, with radio frequency amplifiers, the transmitters can produce up to a thousand kilowatts. Amplifiers are unique and custom-made according to how their output stages are configured and operated. In some cases, amplifiers make output levels that correspond with the load. For example, for a typical loudspeaker that has an impedance of 4-8 ohms, the amplifier should be able to supply high peak current for the loudspeaker.

2.1. Amplifier

As we mentioned in the previous part, an amplifier receives a signal from an input source as a reference signal and provides the same signal with a larger amplitude in the output. In some applications, the input signal has a very small domain of a few millivolts and should be amplified enough to supply the output device. In this case, the voltage amplifier amplifies the input voltage and provides the output with voltage in order to supply the loads. Now in order to study the amplifiers more extensively, it's necessary to define what exactly small signal amplifiers and large signal amplifiers are.

In small signal amplifiers, the main characteristics are linearity and gain. For these types of amplifiers, the current and the voltage is small, so it is important to take the power efficiency and power handling into consideration. While large signal amplifiers provide

high power to drive the load on the output, the main features of this amplifier type is the power efficiency and how the amplifier can deliver maximum power to the loads.

2.2. Characteristics of amplifiers

Bandwidth:

Bandwidth is the frequency through which an amplifier can operate.

Noise:

Noise refers to the unwanted signal that makes disturbances to the output signal content. This signal is always included in the output signal and the performance of the amplifier relies on it.

Slew rate:

Slew rate is the rate of response to an abrupt change of input level (Voltage changes with respect to time)

Gain:

Gain refers to the ration that exists between the input and the output signal. This is the most important aspect in amplifiers.

Stability:

Stability refers to the ability of the amplifier to provide a reliable and constant output signal to a dedicated or arbitrary load.

2.3. Power Amplifiers

To understand and describe amplifiers one must be familiar with the type of signal it amplifies. This means that one should have knowledge of the band of frequencies that an amplifier can handle and the functions that the amplifiers perform within an electronic system. Various types of amplifiers include A.F. amplifiers (audio frequency amplifiers), I.F amplifiers (the intermediate frequency amplifiers), and buffer amplifiers.

Power amplifiers are the most common types of amplifiers. They need to produce a very high power to be able to drive the output device or load. To enhance the performance of the power amplifiers in the power output circuits, there are various techniques that can be used. In order to understand one of these effective techniques, for example when a voltage amplifier increases the amplitude of a signal, most of the time it may not be able to achieve and drive an output such as the motor or a loudspeaker on its own. Therefore, if a voltage amplifier has a gain of about 100, it can amplify a 150 mV signal to a maximum amplitude of up to 15V. Then, the amplifier can feed the 15V signal to a load of 10 k**Ω** and

if this value is changed to 10 ohms, the voltage amplifier is not necessarily able to provide an extra current or even provide the additional current that is necessary for maintaining a 15V across a 10 ohm. Compared to a current amplifier that has a gain of about 100 and can amplify a 10μA signal to a 10mA when there is a very low output voltage, this type of amplifier can supply a 1mA signal at a voltage of 10. Consequently, the two current amplifiers without sufficient power then the voltage and current amplifiers can make and utilize some small resistor which does not draw a huge amount of power. Small resistors usually have a small junction that cannot handle all the power required to drive some a certain amount of output without overheating. In order to achieve low losses, a Class-D amplifier is absolutely necessary. A Class-D amplifier can combine elements like low electromagnetic interference and high degrees of efficiency.

2.4. Classification of Power Amplifiers

Because not all amplifiers are the same, the best way to distinguish them is through a class system. All amplifiers are categorized according to their method of operation and to their circuit's configurations. This classification is useful in that it ranges from linear to nonlinear operations.

Although we will not discuss the details of this classification system, we will provide a brief overview of the theoretical issues, and we will look at some of the important components that go into designing amplifiers.

Then, in Chapters 3 and 4 we will look at how these same components function in the amplifiers we have designed.

As we have discussed previously, there are several classes of amplifiers. Below are their definitions and their characteristics.

- Class A

In this type of amplifier, the bias current is set to output at the output of the full 360˚ output swing. This class is purely linear and has a minimal amount of distortion. but its efficiency is very low and is between 25% -50%.

- Class B

In this type of amplifier, no bias current is set resulting in an 180˚ output swing. Within the 180˚ internal this amplifier is similar to the class A line, but the amplifier shows converter-distortion at the zero-crossing internal. Therefore, the distortion in this class is more than class A. The efficiency is up to 78.5%.

- Class AB

In this amplifier class, the output is more than half a cycle, that is, at output 180˚-360˚ output swing. This class is linear. The Distortion and Power efficiency is between classes A and B. Its power efficiency ranges from 25% to 78.5%.

· Class C

In this class, the output is less than half a cycle, that is, at output less than 180˚ output swing. This amplifier is found mostly in radio and in telecommunication transmitters.

· Class D

A pulse signal is used in this class. In fact, this class is also called switching or PWM (Pulse Width Modulation) amplifier, because the PWM method generates square/pulse signals by switching.

Because in this amplifier the keys are either completely OFF or ON, the output power loss is sharply reduced. The efficiency of this class of amplifiers is theoretically 100%, but in practice this is not possible and usually exceeds is around 90% or above. The high efficiency of this class of amplifiers makes it one of the most attractive and ideal amplifiers.

2.5. Power efficiency

The efficiency of an amplifier refers to the ratio that exists between the output power and the power that is consumed by the amplifier. In other words, efficiency is defined as the ratio of the output power to the input power, and if we go from the class A amplifier to the class D, we see that the power efficiency increases. A significant amount of power is consumed by bias in the amplifier class A, even when the input signal is not applied. So the power efficiency is quite low - especially when the input signal is small.

The maximum efficiency of Class A power occurs when the largest voltage and output current, with a direct load of 25% and with a transformer connection of 50%. And in the case of Class B, the maximum efficiency with no DC bias power may reach up to 78.5%.

A Class-D amplifier with efficiency of more than 90% has the highest efficiency among the amplifiers mentioned. Also, for the amplifier Class AB, which performs between Class A and Class B, has an efficiency between 25% and 78.5%.

The following table shows the comparison between amplifiers from A to D:

	A	AB	B	C	D
Operation cycle	360 ˚	180 ˚ -360 ˚	180 ˚	<180 ˚	PWM
Power efficiency	25%-50%	25%-78.5%	78.5%		Over 90%

Table 2.1 Comparison of amplifier classes

2.6. Power balance

Let's consider a typical chain of output signal reproduction as in the figure below. In every typical amplifier there are three main stages, including an input source, amplification, the input signal and an output low pass filter (LPF).

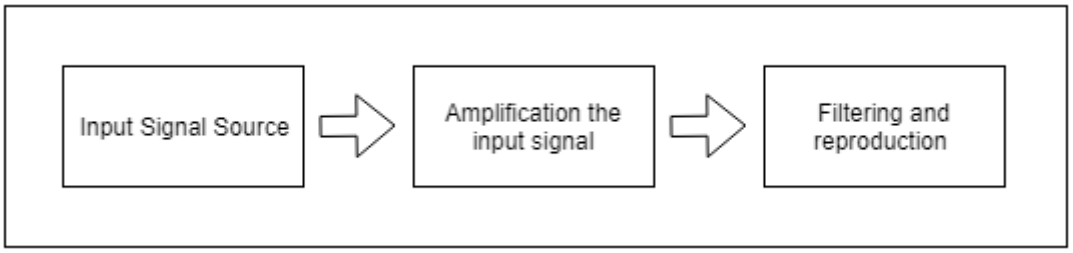

Figure 2.1 basic example of a reproduction chain for an input signal.

For any system, such as an amplifier, the most important parameter is efficiency, otherwise known as energy exchanges over time. In other words, the entire amplification and reproduction process of an input signal involves power. Efficiency is defined here as the ratio between the power absorbed or input power of system and the useful power delivered to the load or outgoing power from the system. It is known that real systems have efficiency less than 100% due to the energy conservation law, which means that any system is inherently dissipative. There is a non-zero contribution of input power that is dissipated, for example, in the form of heat. The chain of signal reproduction that we are considering is a system that gets power from the input and supplies load at the output. Each element of the chain has its own efficiency that combines with the efficiencies of the other elements; This means that every element of the chain helps to increase the dissipated power, and as a result, there is a decrease in power efficiency.

The energy balance of a chain of signal reproduction is shown in Figure below.

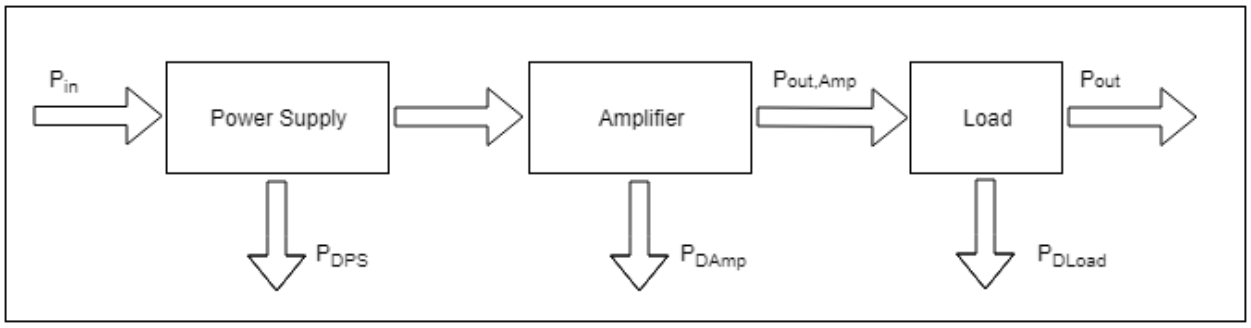

Figure 2.2 Power balance of the signal reproduction chain.

Now we will discuss the various contributions of absorbed, delivered and dissipated power of each single element of the signal reproduction chain, Figure 2.2. We omitted the input signal source because it is not relevant to the energy balance. On the left side, we consider the input power contributions or power absorbed by the power Supply, represented as P_{IN}, and on the right side (output side), the contributions of useful power

delivered, represented as P_{OUT}. The contributions of dissipated power, represented as P_{DPS}, P_{DAmp} and P_{DLoad}, are the sum of all the dissipative subsystems that make up the chain.

Every single element of the chain can be described in greater detail. The amplifier is essentially composed of two parts: a power Supply, which has the task of supplying power in such a way that it is usable, and the actual amplifier part. Each individual subsystem of the amplifier is described in terms of energy balance, and being systems themselves. Dissipation of the whole system will be the sum of dissipation of each individual subsystem. As we can see in Figure 2.3, the power supply will dissipate a power P_{DPS} (Dissipation of power supply), while the actual amplifier will dissipate a power P_{DAmp}. The power supplied by the amplifier to the load, indicated in the figure as $P_{OUT,Amp}$, is absorbed by the load.

Since all the elements of the above chain are dissipative, it is necessary to concentrate on improving the efficiency of the amplifier in order to reduce its dissipative contribution. To do this, it is useful to concentrate only on the amplifier part, thus we are going to restrict the "boundaries" of the system in consideration, as shown in Figure 2.3.

The efficiency of a typical chain is the ratio between the delivered power and the absorbed power. At this point the power $P_{OUT,Amp}$, or the power supplied by the Amplifier system, is the output power that should be considered so in this case the efficiency of chain will now defined as the ratio of

$$\eta = \frac{P_{OUT,Amp}}{P_{IN}}$$

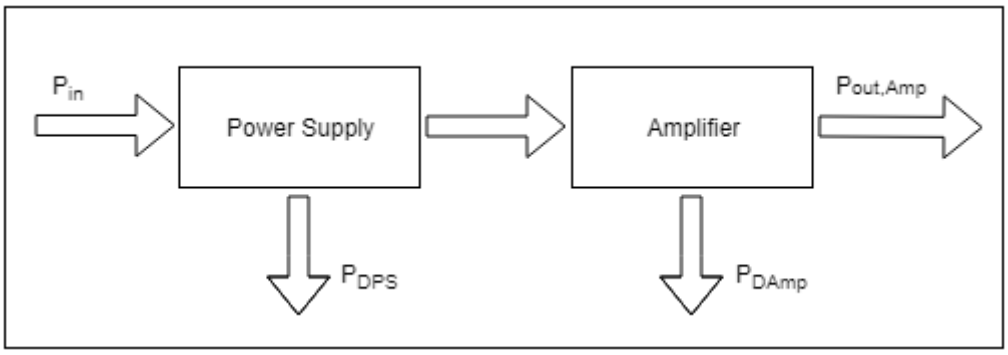

Figure 2.3 Energy balance of the power amplifier (without load).

Energy balance of power amplifier is described in this part, now it's clear that any amplifier has dissipation in each stage, especially dissipation of the transistors or power switches that are the key element of any amplifier, which will be discussed later in detail.

Now that we have looked at the energy balance of power, we can see that amplifiers have dissipation in each stage, especially dissipation of the transistors or power switches. This concept is the key element of any amplifier, which will be discussed later in detail.

2.7. Switched-mode vs. Linear amplifiers

We know that efficiency is one of the most important parameters in term of designing any amplifier. There is another classification of amplifiers based on the transistors that are used in amplifiers:

- Linear amplifier that typically uses bipolar transistors (Figure 2.4) and
- Switch-mode amplifiers that use MOSFETs (Figure 2.5).

Since we have been using a Class D amplifier -a switch-mode amplifier- we should be aware of the reasons why we chose it. Let's look at the differences between switch-mode and linear amplifiers from a topological point of view and form in terms of energy.

2.7.1. Differences from topological point of view

Switch-mode amplifiers are designed to improve efficiency. For this purpose, mainly the MOSFET is used. In order to amplify input signal using a switch-mode amplifier, power should be provided in three parts of the process. In the first part, power is needed to modulate the input signal, power is required to drive the MOSFETs in the second part, and in the third part, power is required for the modulator stage. However, this amount of energy in the switched-mode amplifier is less than the energy required for bias linear amplifiers.

In this amplifier, any input signal must first be converted to rectangular signal form and this rectangular signal is used to drive MOSFETs. Finally, with the help of a low pass output filter, the original signal is reproduced with large amplitude.

The following figure shows the simple schematics of a switched-mode amplifier.

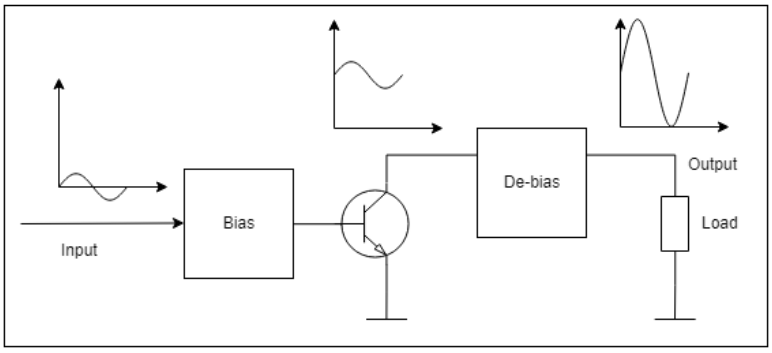

Figure 2.4 Simple schematics the final stage of a power amplifier of linear amplifier.

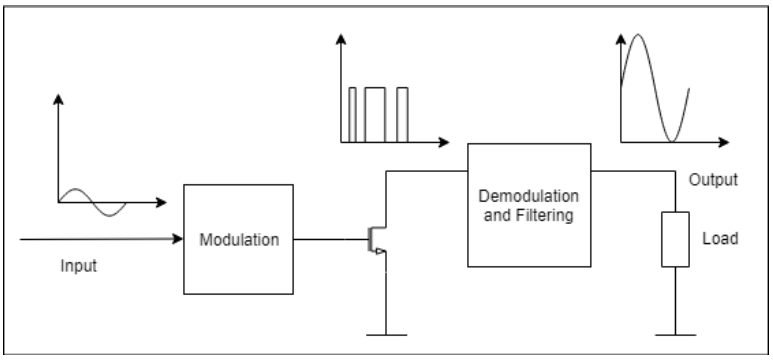

Figure 2.5 Simple schematics of the final stage of a power amplifier of switched-mode amplifier.

2.7.2. Differences from energy point of view

In terms of energy, there are significant differences between linear amplifiers, e.g., Class-AB, and switched-mode amplifiers, like Class-D, based on their operating principle.

The power amplifier absorbs energy from the power supply and is able to condition it and deliver it to its load with a trend over time equal to that of the input signal. This conditioning, as already mentioned, is not ideal and a part of absorbed power is dissipated.

Let us consider and compare the output stages of a simple Class-AB linear amplifier and a Class-D amplifier. As it is shown in Figure 6, there are no major topological differences between the two output stages; what changes is the driving mechanism of the power stage.

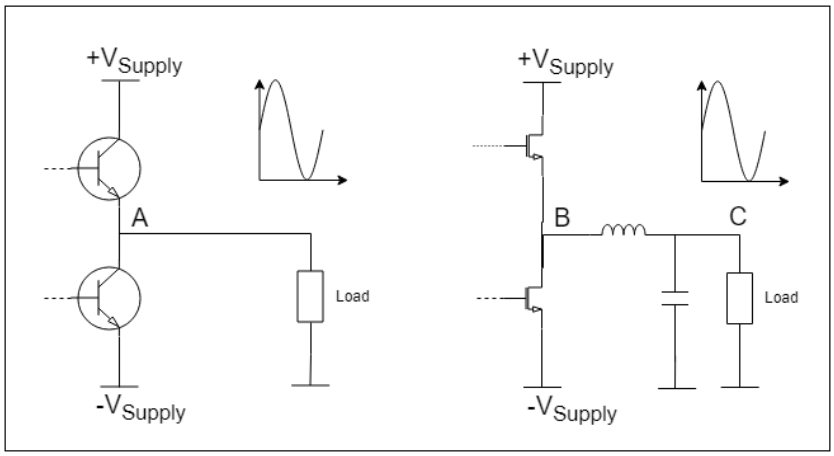

Figure 2.6 Comparison between the final stages of a linear amplifier and a switching amplifier.

In the linear amplifier, V_{OUT} voltage at the ends of the load and the voltage at the point A between the two power MOSFETs is the same. The current flowing in the load depends on the voltage and the impedance of the load (which we can assume purely resistive) R_L, or

$$I_{OUT} = \frac{V_{Out}}{R_L}$$

This I_{OUT} current is provided by the V_{SUPPLY} (power supply) for which $I_{SUPPLY} = I_{OUT}$. Therefore, the power which has been supplied by the power Supply or V_{SUPPLY} is

$$P_{SUPPLY} = V_{SUPPLY} \times I_{OUT}$$

and so the power which has been supplied to the load is therefore

$$P_{OUT} = V_{OUT} \times I_{OUT}$$

The power dissipated by the amplifier is therefore the difference between the two, namely:

$$P_{DISS} = P_{SUPPLY} - P_{OUT} = (V_{SUPPLY} - V_{OUT}) \times I_{OUT}$$

Thus, it is important to note that the linear amplifier behaves as a variable resistance and acts as a purely dissipative element.

To find $(V_{SUPPLY} - V_{OUT})$ we need to go back to the gate driver stage and consider the inner function of the driving circuit. The driving circuit supplies the signal with the appropriate waveform to the two power transistors.

Suppose that a sinusoidal signal is being amplified. As it is shown in Figure 2.7, the amplitude of the power supply is greater than the voltage on the load. This is a fundamental requirement because if a greater voltage on the load is desired, the power supply must have a sufficient margin to avoid causing the saturation phenomenon or clipping of the output voltage.

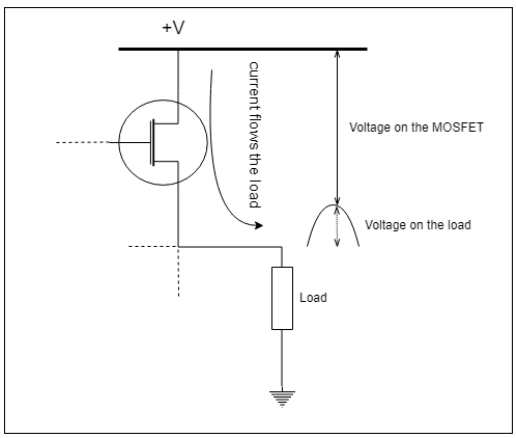

Figure 2.7 Comparison between Voltage on the MOSFETs and voltage on the load in linear amplifier.

Basically power dissipation of a transistor in a Class-D system consists of two main parts; switching losses and resistive losses which can be calculated in the form

$$P_{DISS} = P_{Switching} + P_{Rloss}.$$

The current that flows through the load is supplied by the transistors and the transistors themselves have Drain-Source voltage (VDS) and Drain current (ID). So in these conditions, the power dissipation of a transistor is

$$P_{DISS} = V_{DS} \times I_D.$$

We should point out that the cause of power dissipation of the transistor is comes from the difference between the voltage on the load and the Supply voltage in the equation

$$P_{DISS} = P_{SUPPLY} - P_{OUT} = (V_{SUPPLY} - V_{OUT}) \times I_{OUT}.$$

It seems trivial, that this evaluation is the milestone that has led to the use the Class-D amplifiers. From now it is clear that if we are able to reduce this difference, we would be able to reduce also the power dissipation as well. Therefore, with the same power supplied to the load, we are able to increase the efficiency of the amplifier.

In the output stage of the *Class-D amplifier*, there is a significant difference between the wave form and the amplitude between the central node point (B) (between the two power MOSFETs) and the end point (C) or load. As we have seen previously, the output voltage of a Class-D amplifier depends on the input voltage through the duty cycle factor D, so we can neglect other factors,

$$V_{OUT} = D \times V_{IN}$$

The current flowing through the load is always given by the ratio between the voltage at its terminals, in this case at the point (C) and the impedance of the load. As we know a theoretical Class-D amplifier has a 100% efficiency, therefore, it does not dissipate and all the power supplied by the power Supply will be transferred to the load, so

$$P_{SUPPLY} = P_{OUT}.$$

In conclusion, the difference between a linear amplifier and a switched-mode amplifier, from an energy point of view, is that the linear amplifier (for example in class AB), the current is constant between power Supply and load but in switched-mode (class D) amplifier, the power is constant.

2.8. Amplifier Distortion

Any signal that varies less than 360˚ full cycle has been distorted. The ideal amplifier receives the ideal sinusoidal signal at the input and after amplifying it, will generate the ideal sinusoidal (single frequency) in the output. When distortion occurs, the output signal (or the signal amplitude) will be different from the input signal. There are two types of distortions:

-Amplitude Distortion: When the characteristics of the system are not linear, there is a probability of occurrence in all classes of amplifiers.

-Frequency Distortion: When the amplifier responds differently to the input signal of/with different frequencies.

2.9. Effect of loads on efficiency

The actual loads of the amplifiers usually are reactive. Without proposing electro-technical calculations, the substance is that the speakers have, in addition to having a dissipative part, also have a part capable of storing energy and returning it back. In a first glance this may seem like a positive aspect for the efficiency of the system, it can be shown that it is a pejorative aspect. Those who are more familiar with the meaning of the reagent, will understand that the presence of a reactive part in the impedance of the load means that the voltage at its ends and current flowing there are not in phase. It can be shown that this phase shifting is the cause of greater power dissipation in amplifiers that deliver power over speakers (as it is right in context) and not on a pure resistor.

2.10. Increase efficiency

First of all, to increase efficiency it is necessary to reduce the dissipation of the power transistors in the final stages of the amplifiers. When reconsidering Figure 2.5 and considering that the dissipated power is the product between the voltage across the transistor and the current flowing in it, it is clear that to reduce the power dissipation there are two solutions: zero current or zero voltage. No current means there will be no supplying load at the output, because if we discontinue the current flowing in the power transistor, we would also discontinue the current flowing in the load.

The other solution is the only one that can be used, that is, to reduce the voltage at the ends of the power transistors to zero (or as low as possible). To achieve this, there are two possibilities:

1. the supply voltage "follows" the voltage on the load as much as possible;

2. the voltage on the load "follows" the supply voltage as much as possible.

The first path leads to the invention of various classes of amplifiers (class G, class H, etc.). The second leads to the use of switching technology in amplifiers, like Class-D amplifiers. Figure 2.8 tries to schematize these reflections.

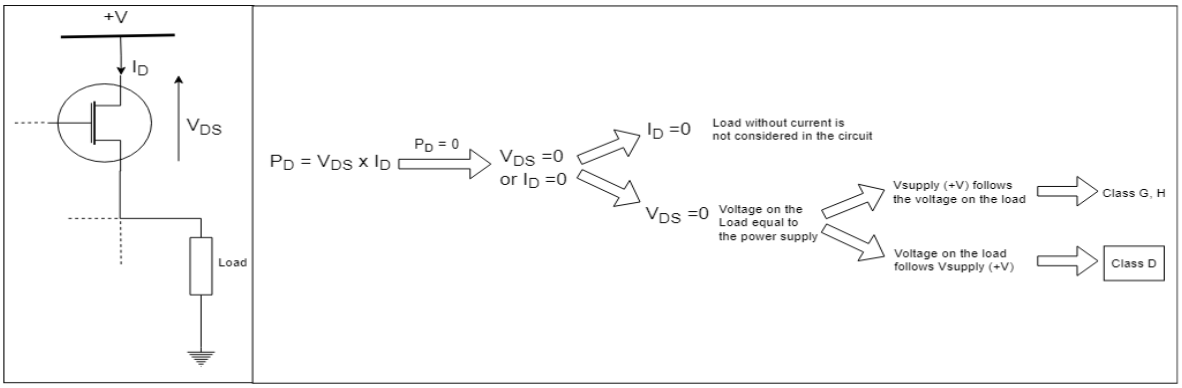

Figure 2.8 Road to the "Class-D amplifier" solution.

In fact, by making this intellectual step, which underlies modern switching amplifiers, a Class-D amplifier is established. The whole path followed to find the solution, the Class-D amplifier which based on our need to find a more energy efficient solution compared to traditional linear amplifiers. This type of amplifier, compared to traditional linear amplifiers, is better in terms of efficiency of energy.

In this chapter we wanted to explain, in the most elementary terms, what were the calculated steps that led to the idea of using MOSFETs in the field of power amplification, thus giving light to the Class-D amplifier.

3. Case study: Class-D amplifier with Butterworth low pass filter

3.1. Basic and history

Class-D amplifiers were first proposed and developed in the year 1958. They became popular in the following years and formed the most basic components in all the electronic systems. Compared to other classes of amplifiers, such as Class-A and Class-B, Class-D has a very high degree of efficiency. The amplifiers in that class can reach in theory up to 100%, and can reach up to 90% when it is put to the test and in practice. However, the Class-D amplifier comes at a cost. You must pay the price for this high degree of efficiency. The design is much more complex and larger compared to the other types of amplifiers, and this makes it expensive. Also, this type of amplifier is affected very much by noise and distortion, which is unpleasant. Despite all these issues, we found out in the previous chapter that a Class-D amplifier is the best and most reliable solution.

Class-D amplifiers have a very wide application, especially in mobile applications. This is because a Class-D amplifier uses very little energy and is highly optimal. Also in mobile phones and portable audio devices where Class-D is very common, there is limited space. Therefore, the Class-D amplifier is usually characterized by its low power consumption, as well as the ability to eliminate the heat sink. However, to eliminate unnecessary costs and keep costs as low as possible, Class-D amplifiers must be made with very high, and the most current, technology. However, due to the many applications that rely on these amplifiers and the progression of technology, competition has increased.

Class-D amplifiers were invented in 1958 for audio applications, but it was impossible to use such an amplifier for the entire audio range and for the components that did not exist yet. In terms of losses, the results of bipolar transistors were very poor and the bandwidth of the amplifiers were limited by the low possible switching frequency. The first MOSFET was produced in 1960 and it came onto the market in 1970. MOSFETs are the only components that are able to work at high switching frequencies with less switching losses. Although MOSFETs were a step closer to Class-D amplifiers, an amplifier for the audio range was still difficult to construct. It is necessary to have a full H-bridge to switch at a frequency of 200 to 300 kHz if you want to cover the entire audible range. In MOSFETs, pulse gate current is about 1 A, so to keep switching losses of the power amplifier in a small time frame, the currents must be turned within a few nS (nanosecond) and be switched off when necessary. This means that there must be an amplifier with a bandwidth of many MHz. The first Class-D was built relatively early despite there being major problems, in the control of asynchronous motors in the form of frequency converters. In this application, no high switching frequencies are necessary. A frequency converter makes it possible to use bipolar transistors in the output stage.

The importance of high efficiency of the amplifier makes it necessary to use a Class-D amplifier. During this time the Class-D experienced a real boom. All major semiconductor manufacturers like ST, Philips, TI, Maxim, Intersil, offered products for a Class-D amplifier. Till this day, the new technology is used in many products, and the number of products is on the rise.

In this thesis, we are studying Class-D amplifiers using PWM with Butterworth filter. We would now like to speak extensively about Class-D amplifiers, also known as switch-mode amplifiers. The fundamental question is: "why do we need Class-D amplifiers?". It is best to answer this question in technical terms. The idea behind the high efficiency of a Class-D amplifier was to provide a voltage signal at the output of the amplifier that can only assume positive and negative power values, i.e. + V_{SUPPLY} and -V_{SUPPLY}. Obviously, this voltage signal, if supplied directly to the loads, would not result in the desired supply of loads.

To obtain the desired result, i.e. high efficiency and a correct signal to the supply load, a modulation operation must incorporate a voltage signal that can only assume the values + V_{SUPPLY} and - V_{SUPPLY}, and at the end, use a low pass filter to initiate demodulation.

3.2. Principles of operation of the Class-D amplifier

The Class-D amplifier is reinforced to create a different signal from the signal that is amplified at very high frequencies. Therefore, it is enhanced to make sure that there is a very low loss. In most cases the amplifiers modulating a voltage or a current signal are usually presented at the input. In the next stage a PWM signal is generated using various methods. Modulating is not 100% perfect. Dead time may cause loops that are usually generated and integrated into the circuits, therefore, correcting the errors.

The operation of the Class-D amplifier consists of three stages:

- Modulation or PWM generation
- Gate Driver and Power supply
- Demodulation and filtering

In the first stage, using a comparator and a high frequency carrier (here, saw-tooth), the input signal or reference signal is modulated. Then the gate driver uses the output signal of the first stage, PWM to switch the MOSFETs ON or OFF. In the second stage with the help of +V_{SUPPLY} and -V_{SUPPLY}, the PWM signal is amplified. In this thesis we are using a Half Bridge, which is shown in Figure 3.1 consisting of two MOSFETs. In the last stage, the amplified PWM signal is demodulated and the input signal is reproduced to the desired amplitude.

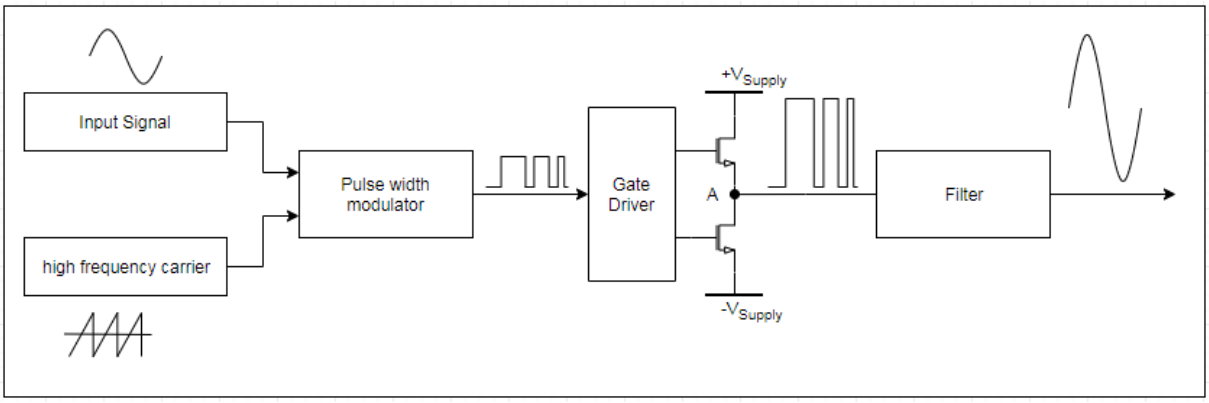

Figure 3.1 Simplified block diagram of a Class-D amplifier, with the waveforms at each stage.

Figure 3.1 above shows the basic block diagram for a Half Bridge Class-D amplifier, with the waveforms at each stage. As you can see, the basic components are a Modulator, a Power Driver and a Demodulator.

Required components to design a Class-D amplifier include

- Saw-tooth/Triangle generator
- PWM generator
- Power Driver
- Power supply
- Active damping
- Low pass filter
- Negative feedback
- PI controller

We will start with the basic open loop circuit of a Class D amplifier and then we will append all other components respectively.

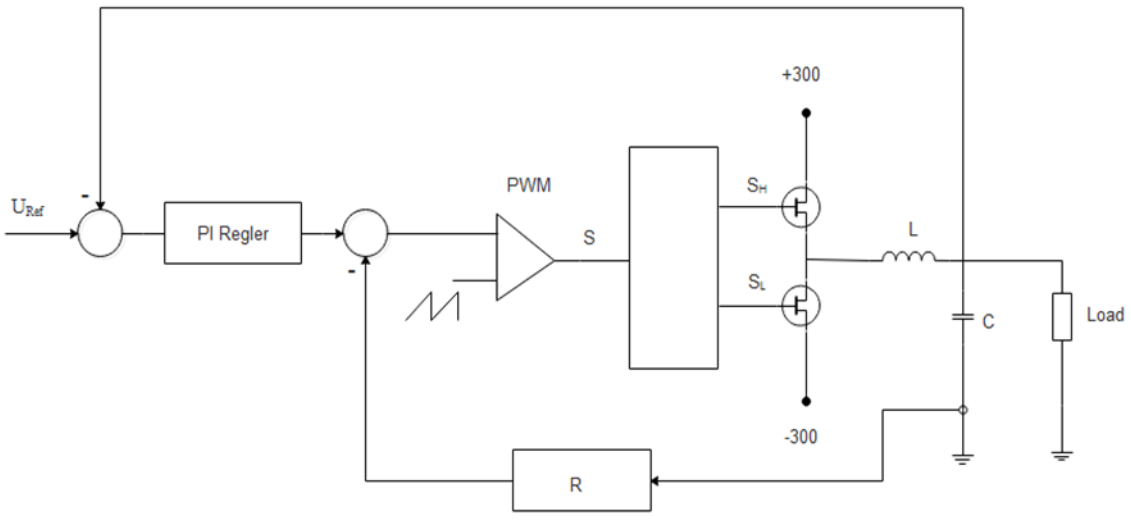

Figure 3.2 Block diagram of controlled Class-D amplifier with PI controller.

Figure above shows the Class-D amplifier in more detail. This circuit uses feedback from the output filter to help compensate for variations in the bus voltages.

3.3. First stage: PWM

In this stage we are going to modulate the analog reference signal, using PWM technic. The output of this stage is a set of pulses which we will discuss later about its properties in great detail.

3.3.1. Pulse Width Modulation

In order to explain the principle of PWM modulation, it is necessary to clarify the meaning of some terms, in particular the duty-cycle. In the case of PWM modulation, modulation takes place by modifying the duty cycle of set of voltage pulses generated by the interaction between the modulating signal and the carrier signal.

3.3.2. The duty-cycle

The duty cycle is a characteristic of periodic signals with a rectangular wave and represents the ratio between the time T_{ON}, during which the signal is at high a level, and the period T of the signal itself. This ratio is typically indicated with the letter D and is expressed in percentage terms:

$$D = \frac{T_{ON}}{T} \times 100.$$

Figure below shows some examples of rectangular signals with duty-cycles of 25%, 50% and 75%.

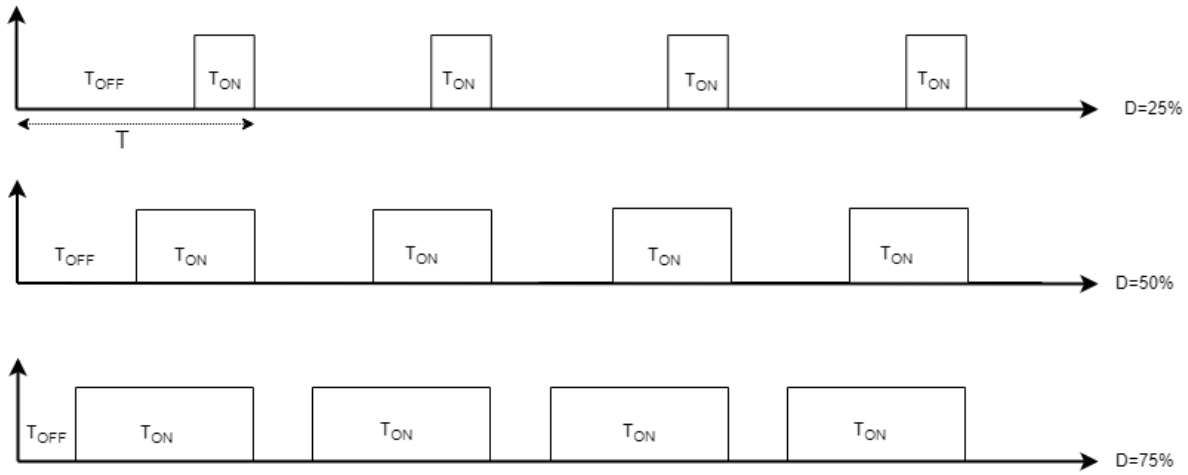

Figure 3.3 Example of signals with different duty cycles

Note that duty cycle is not a characteristic of rectangular signals, but is a feature of analog signals. This clarification is essential and will be clarified in detail later.

3.3.3. Basic operation of PWM

The PWM modulator frequently is nothing more than a comparator. It is an analog circuit that can be considered an open loop operational amplifier. The comparator is the fundamental element of Pulse width modulation and should be explained in detail.

A comparator is a device able to generate an electrical signal at the output that can take only two values, corresponding to the two high and low supply voltages + V_S and -V_S. With reference to Figures 3.4 and 3.5, the signal generated by the comparator is +V_S if the input signal to the positive terminal V_{IN+} is greater than the input signal to the negative terminal V_{IN-}, in other words $V_{IN+} > V_{IN-}$. And vice versa; when the signal at the positive terminal is lower than the signal at the negative terminal ($V_{IN+} < V_{IN-}$), the output is the low value -V_S.

The comparator output is a periodic rectangular wave, that its where the period is equal to the period of the reference signal ($T_{PWM}=T_{Ref}$) however, the frequency of the PWM is equal to the frequency of the carrier signal ($f_{PWM}=f_{Carrier}$). In our design we use ±1 for comparator so +V_S = 1V and -V_S = -1V.

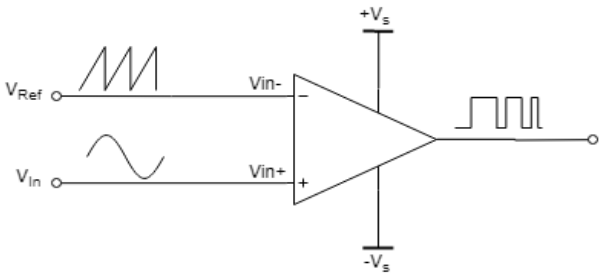

Figure 3.4 Comparator and waveforms.

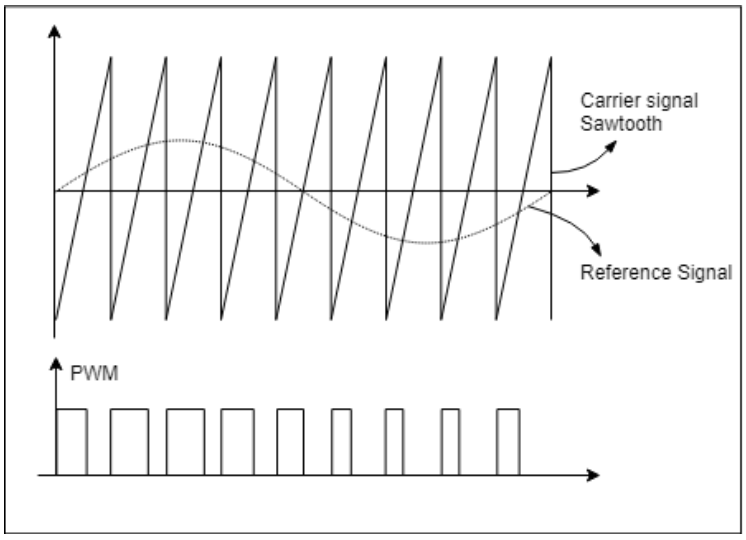

Figure 3.5 PWM generation using a sinusoidal signal and a saw-tooth signal; PWM signal is high as long as the reference signal is greater that carrier signal.

In the example shown in Figure 3.5, a sinusoidal signal as a reference signal is applied to the positive terminal of the comparator, and a saw-tooth as a carrier signal is applied to the negative terminal. The basic PWM generation is shown in Figure 3.6. In this example,

if the sinusoidal signal is higher than the saw-tooth, PWM is 1 and if the sinusoidal signal is lower than the saw-tooth signal, PWM is 0.

3.3.4. Two special examples of PWM generation

In the Class-D amplifier, the slow signal is the reference signal and the fast signal is the high frequency carrier. The result of the modulation is a rectangular or rectangular signal with a duty cycle variable over time. In order to better understand the application of the comparator in Class-D amplifier, the following illustrations will be useful.

- Slow sinusoidal with fast saw-tooth

Suppose that the saw-tooth signal has a frequency of 100kHz and that the sinusoidal signal has a frequency of 5kHz, as in Figure 3.6. This means that during a period of sinusoidal signal, the saw-tooth will reach 20 periods.

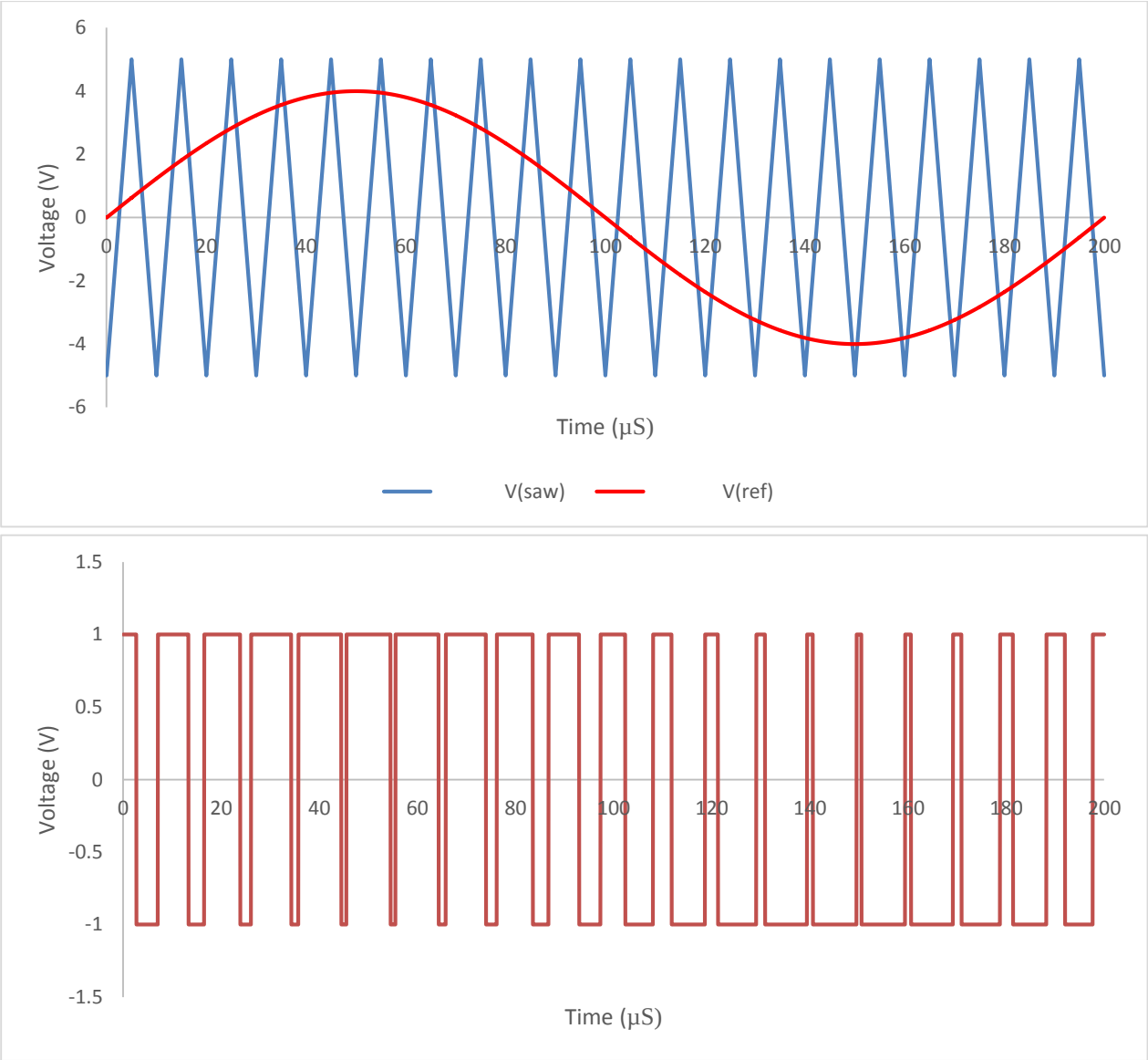

Figure 3.6 PWM produced by "slow" sinusoidal signal of 5 kHz compared with "fast" saw-tooth signal of 100 kHz in Pspice.

- Fast sinusoidal with slow saw-tooth

Suppose that the sinusoidal signal has a frequency of 100 kHz, and suppose now that the reference signal is a saw-tooth signal with a frequency of 5 kHz that varies between $+V_S$=5V and $-V_S$=-5V. This means that the saw-tooth signal will take a full cycle to get all the values from + V_S and -V_S. In the meantime, the sinusoidal signal will have performed 20 cycles.

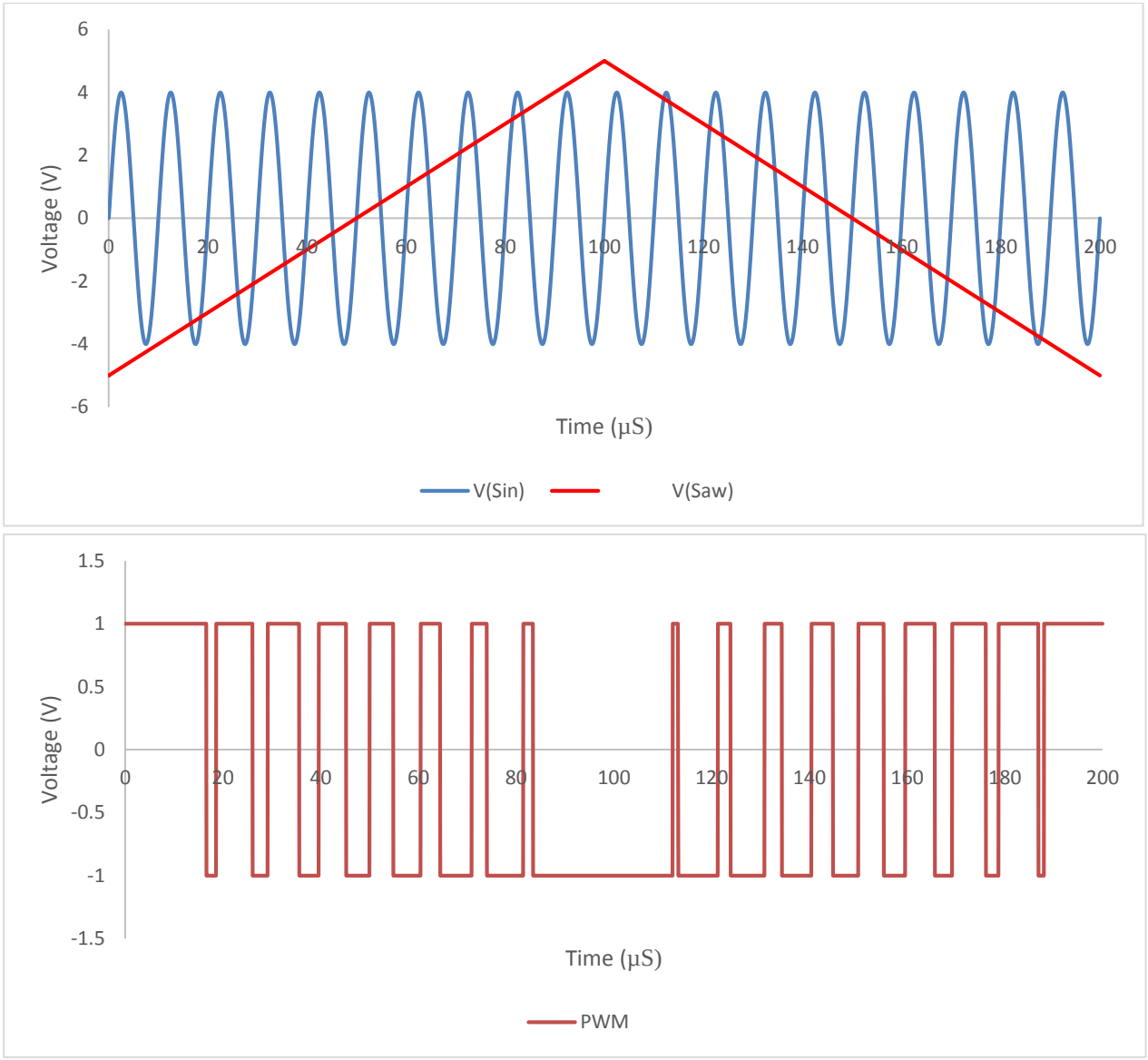

Figure 3.7 PWM generation by "fast" sinusoidal signal of 100 kHz compared with "slow" saw-tooth signal of 5kHz in Pspice.

We should note that the frequency of the PWM signal is equal to the frequency of the "fast" input signal. So in the first example, it is the frequency of the saw-tooth wave. In the case of consideration 2, it is the frequency of the sinusoidal signal.

By looking at the foregoing examples, it is now possible to explain the operating principle of the most basic example of a PWM modulator that is applied in a Class-D amplifier.

The next Figures show that if the frequency of the fast signal or carrier signal is more than 100 times bigger than frequency of the reference signal, the reference signal can be considered as a constant signal.

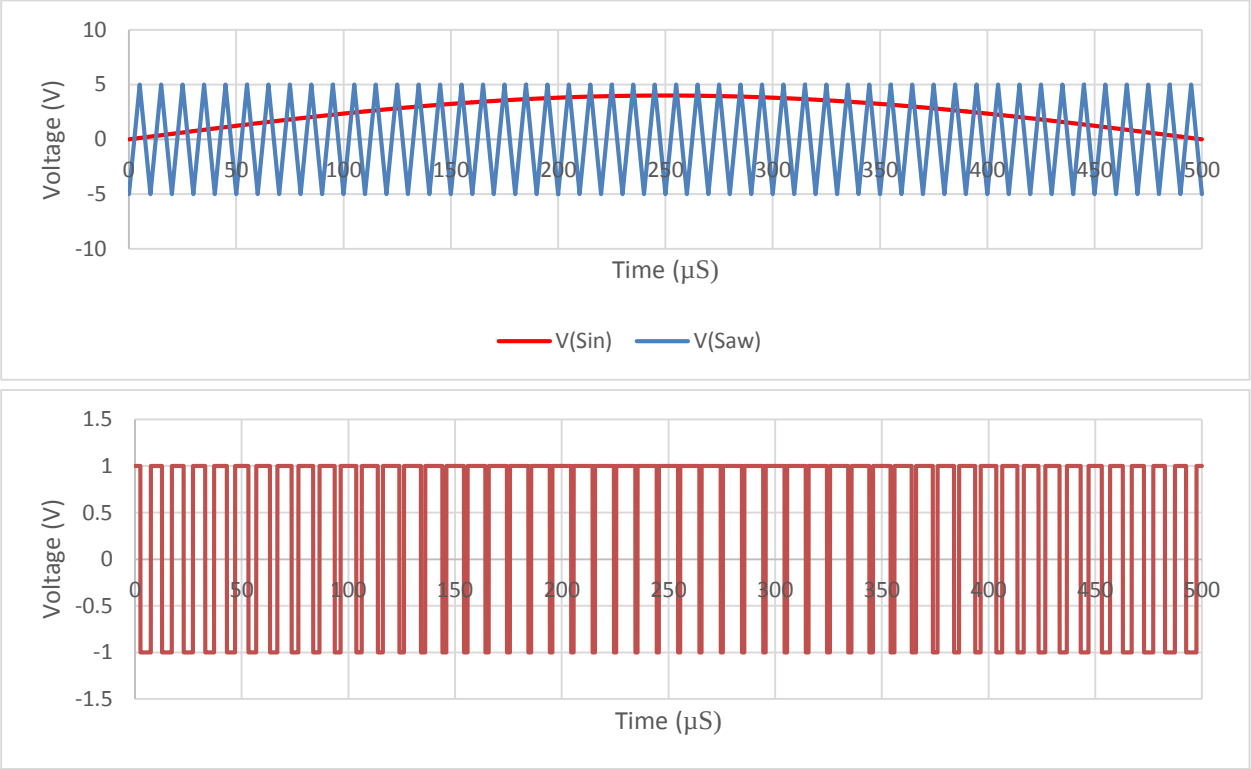

Figure 3.8 PWM produced by "slow" sinusoidal signal of 1 kHz compared with "fast" saw-tooth signal of 100 kHz in Pspice.

The amplitude of the sinusoidal signal is almost constant during a period of the saw-tooth signal. The comparator output (PWM) is therefore exclusively linked to the average value of the sinusoidal signal during a period of the saw-tooth signal.

In this case, the PWM signal has a frequency equal to the frequency of the fast saw-tooth signal,

$$f_{PWM} = f_{fast\ carrier\ signal} = f_{Sawtooth}$$

However, the duty cycle does not depend on the frequency of the saw-tooth signal nor on the frequency of the sine wave, but depends only on their amplitudes, and it varies during several periods. So for each period duty cycle, it will be:

$$D = \frac{V_{Reference}}{V_{Carrier}} = \frac{V_{Sin}}{V_{Saw}}.$$

This consideration can be repeated for each period of the saw-tooth signal, during which the sinusoidal signal will be "slow" and can be considered constant, with respect to the variations of the saw-tooth signal.

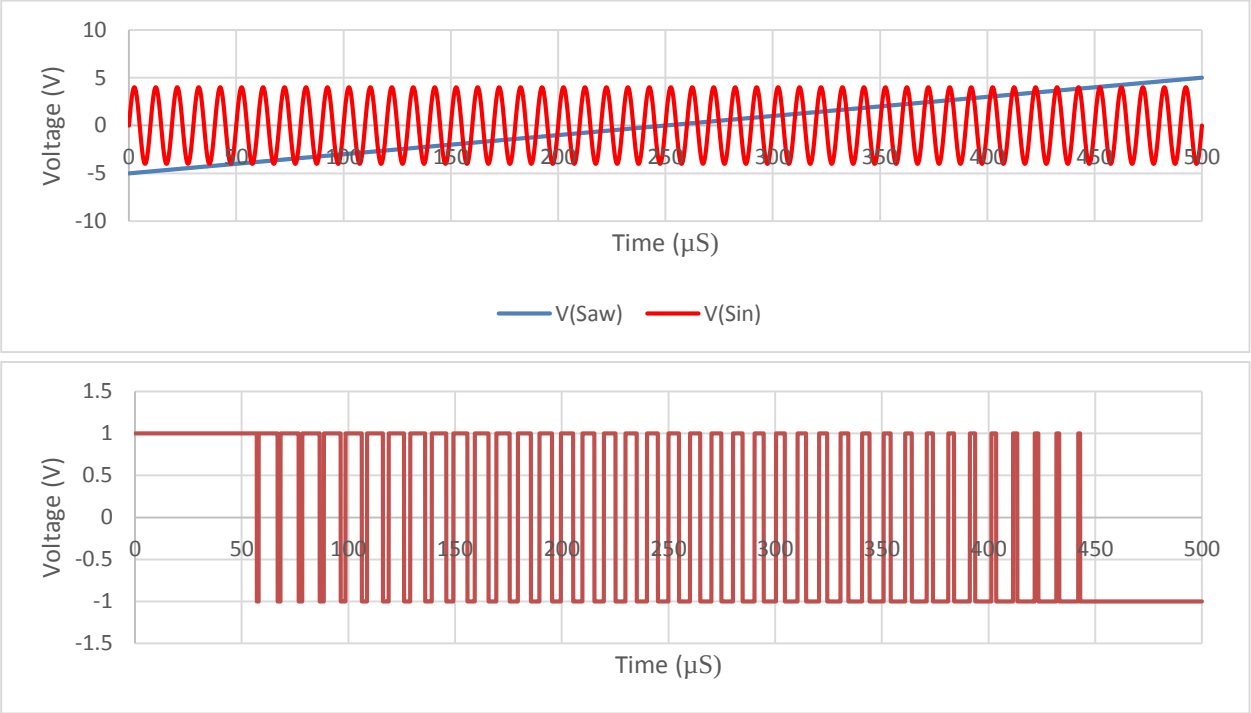

Figure 3.9 PWM generation by "fast" sinusoidal signal of 100 kHz compared with "slow" Saw-tooth signal of 1 kHz in Pspice.

And in Figure 3.9, the Saw-tooth signal during the sinusoidal signal's period is considered almost constant.

The signal resulting in output to the comparator is a set of rectangular pulses whose frequency is equal to the frequency of the fast signal or the sinusoidal signal

$$f_{PWM} = f_{fast\ carrier\ signal} = f_{Sin}$$

and as we mentioned before, the duty cycle for each period is calculated according to the ratio between the amplitude of the slow reference signal (saw-tooth) and the fast carrier signal (sinusoidal).

$$D = \frac{V_{Reference}}{V_{Carrier}} = \frac{V_{Saw}}{V_{Sin}}$$

Therefore, the duty cycle is in effect information carried within the rectangular signal at the output of the comparator. This information is not constant but varies over time with

a law of temporal evolution linked to in relation to the frequency and amplitude of the sinusoidal signal (the "slow" signal). By beginning with a fast saw-tooth signal and then using a comparator, we managed to generate a fast pulse signal where the duty signal is not constant.

The duty cycle of the PWM signal varies in terms of the frequency of the slow sinusoidal signal which represents the reference signal that needs to be amplified. This means that we transformed our analog voltage signal into another analog signal in the form of a set of pulses. This signal has a frequency equal to that of the fast Saw-tooth signal, which is an analog signal whose duty-cycle, during several periods, varies with a law directly related to the amplitude and frequency of the sinusoidal signal of entrance.

It is important to remember that the purpose of this stage in the Class-D amplifier is to transform the reference signal into a form of pulses and prepare it to the next stage, or the power stage. This operation occurs with factors of low voltage and low current, whereas in order to drive a load, it is necessary to have high voltage and current. To do this, there must be a suitable power amplification circuit. How the gate driver and power supply these pulses will be discussed later in the next part “Power stage”.

The modulation operation described above did not involve any digital processing, nor did it convert any signal into a digitized signal, everything remained in the analogue domain.

3.4. Second stage: Gate Driver

Let’s suppose that the input signal of a comparator is a sinusoidal signal with an amplitude of 5V. As we mentioned in the last part, the PWM signal is a pulse signal that can take +1V and -1V. Obviously these voltages are not suitable for supplying a load, and even if they were suitable in some applications, a comparator would not be able to supply the necessary current to transfer the right power from the amplifier to the load.

To achieve this, between PWM and output we need a middle stage, which is called the power stage. It is composed of a gate driver and two power transistors, for example two MOSFETs and a power supply ($\pm V_{Supply}$). A modulating reference signal, a PWM generation and an amplification of the PWM signals occur in this stage and it can be said that this stage is the heart of a Class-D amplifier.

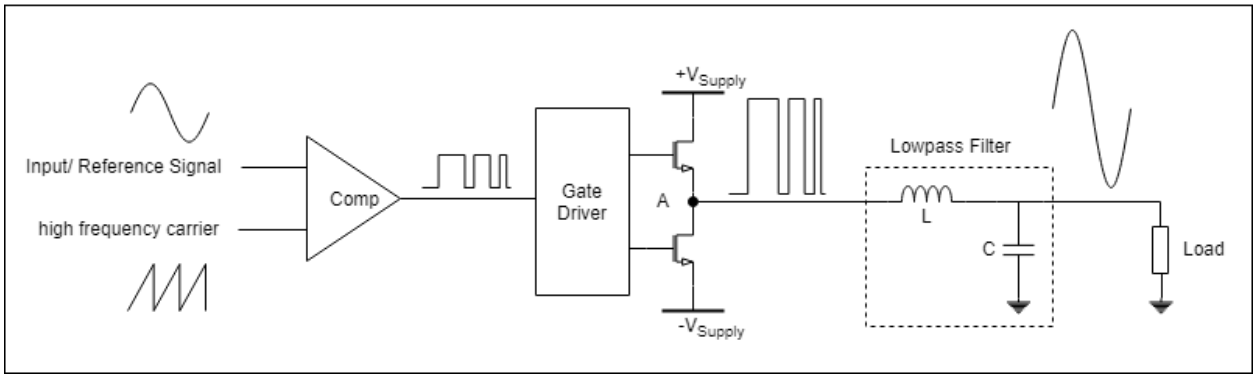

Figure 3.10 Elementary diagram of a Class-D amplifier. 3 stages of amplification in Class-D amplifier. First stage or the comparator stage, which operates between +1V and -1V., second stage or Power stage amplifies the output signal of the comparator to ±300V. The third stage or filtering stage which include low-pass filter to retrieve the output signal of power driver stage.

3.4.1. Gate driver circuit

The Gate Driver is a circuit capable of properly controlling the gates of MOSFETs. The purpose of these power transistors is to supply necessary power to the load. Control here means that the gate driver switches the MOSFETs ON or OFF in high frequency with respect to the fact that just one of them can be switched ON at a dedicated time instant.

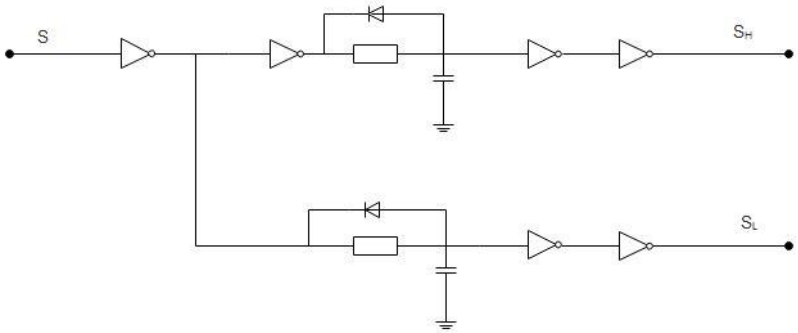

Figure 3.11 Circuit of the gate driver in Class-D amplifier in order to drive MOSFETs.

To make it easier to discuss the function of the gate driver and each of the MOSFETs, we need to name the lower MOSFET as M1 and the upper MOSFET, as M2. According to Figure 3.11, when the input signal to the gate driver or PWM is high (in our case +1V), the gate driver makes S_H high and S_L low; when S_H is high, M1 is switch ON or closed, so M1 behaves like a short circuit. Thus on the output node (A) there is a voltage equal to $+V_{SUPPLY}$=+300V and the current flows from the positive power supply through S_H to the load, and vice versa. When the input signal to the gate driver or PWM is low (in our case -1V), the gate driver makes S_L high and S_H low; when S_L is high, M2 is switch ON or closed, so M2 behaves like a short circuit. Thus on the output node (A) there is a voltage equal to $-V_{SUPPLY}$ =-300V and the current flows from the negative power supply through S_L to the load.

This operation in fact does nothing more than reflect the same input signals to the gate driver at node (A), but instead it assumed the values +1V and -1V and the corresponding values how are +300V and -300V.

3.4.2. Dead-time

It is clear that the power switches (MOSFETs) of the driver gate in the amplifier should not be turned on simultaneously. In practical applications, a short dead time, as shown below, is needed to avoid completely any interference of switching states, like “shoot-through” faults or otherwise known as a short circuit. Dead time is inserted at the positive edges of the gate voltage (Fig. 3. 12). The length of the dead time is determined by the behavior of the switching components. Obviously, the insertion of the dead time in each PWM cycle causes distortion in the output voltage.

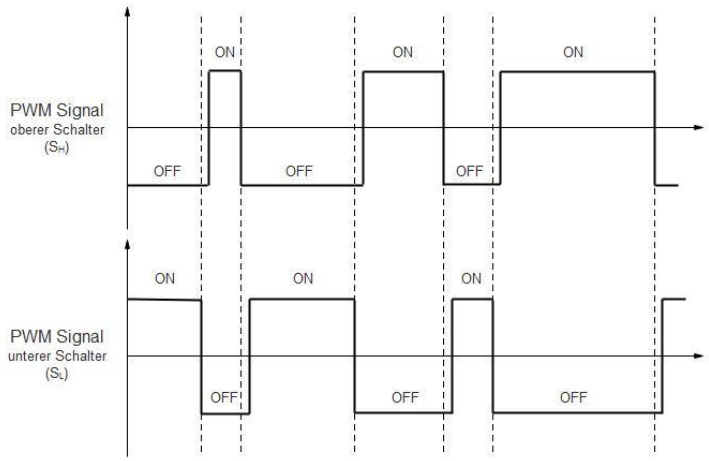

Figure 3.12 Dead Time Illustration for upper and lower switch.

This dead time delays the switch-on of the MOSFET. With this type of signal conditioning, one of the MOSFETs will certainly be off before the complementary MOSFET turn on. The dead time inevitably leads to voltage distortion The smaller the dead time is, the higher the probability of a short circuit (shoot-through), but the lower the distortion can be. Thus there must be a balance between the safe operation and the quality of the gain of the system.

3.5. Third stage: Demodulation and filtering

After modulation and amplification of the PWM signal, the next step is to reproduce the reference signal. In order to do this, it is necessary to demodulate and reconstruct the reference signal by using a low pass filter. But first, we must look at how the signal is reconstructed.

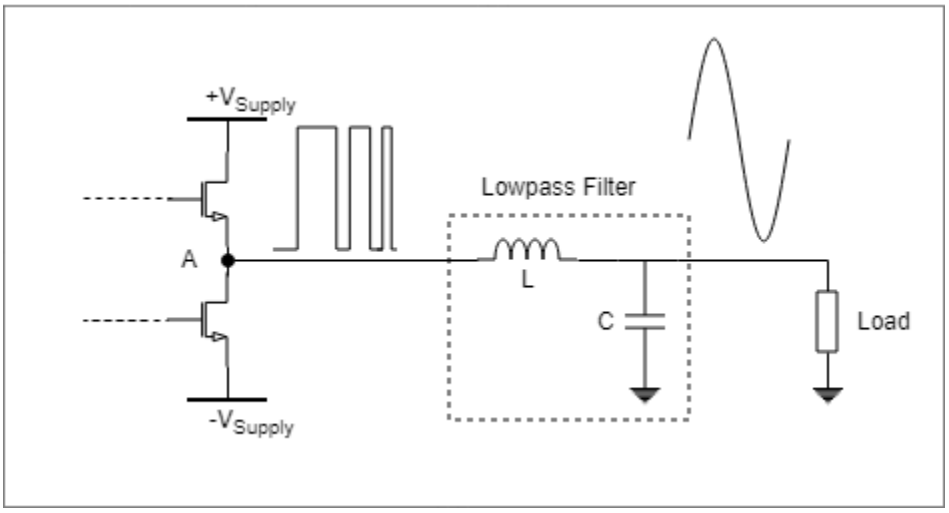

Figure 3.13 Demodulation and filtering stage using LC filter.

As mentioned before, the signal output to the amplifier is not a suitable signal to be sent directly to load. It is necessary to recover the low frequency signal incorporated inside the rectangular wave high frequency PWM signal.

The most intuitive operation is to filter the rectangular wave signal, with a low pass filter, since the duty cycle signal is a low frequency signal, with respect to the frequency of the saw-tooth signal.

3.5.1. Demodulation and average output voltage analysis

One method to demodulate the amplified PWM signal is to use a 2nd order low pass filter (LPF). The LPF acts as an integrator which "integrates" the PWM. Since the amplified sinusoidal-modulated PWM signal is a rectangular signal form, the LPF would transform the PWM into a sinusoidal waveform signal.

Another aspect of the low pass filter is that it can perform signal average function. In frequency domain mean value is equal to signal power spectral component at ω=0 and it's clear that in Fourier analysis the DC term of a periodic signal is the average of the signal thus one of the reason why we use low pass filter, is to pass the DC term and its low frequency terms and attenuate the high frequency terms.

Because the duty-cycle of the PWM signal varies over time, the signal is dependent on the amplitudes of the reference signal and the carrier signal. In a general form, the average output voltage of the demodulator is

$$\overline{V_{OUT}} = D \times V_{Supply} + (1 - D) \times (-V_{Supply})$$

Therefore, the output signal after the demodulator filter is

$$\overline{V_{OUT}} = G \times V_{Reference}$$

$$\text{Which } G = \frac{V_{Supply}}{V_{Reference}}$$

The interesting outcome here is that the reference signal ($V_{Reference}$) varies over time and it is not constant. This statement can be justified analytically by studying the spectrum of a PWM signal.

Suppose that we have a constant reference (2.5V), a saw-tooth signal with a frequency of 100kHz, and an amplitude between -5V to +5V. The output signal will be a rectangular signal form with a 75% duty-cycle. (Figure 3.14)

The average value of the output voltage is given by

$$\overline{V_{OUT}} = 0.75 \times (+5\text{V}) + 0.25 \times (-5\text{V}) = 2.5\text{V},$$

which is exactly the constant reference signal.

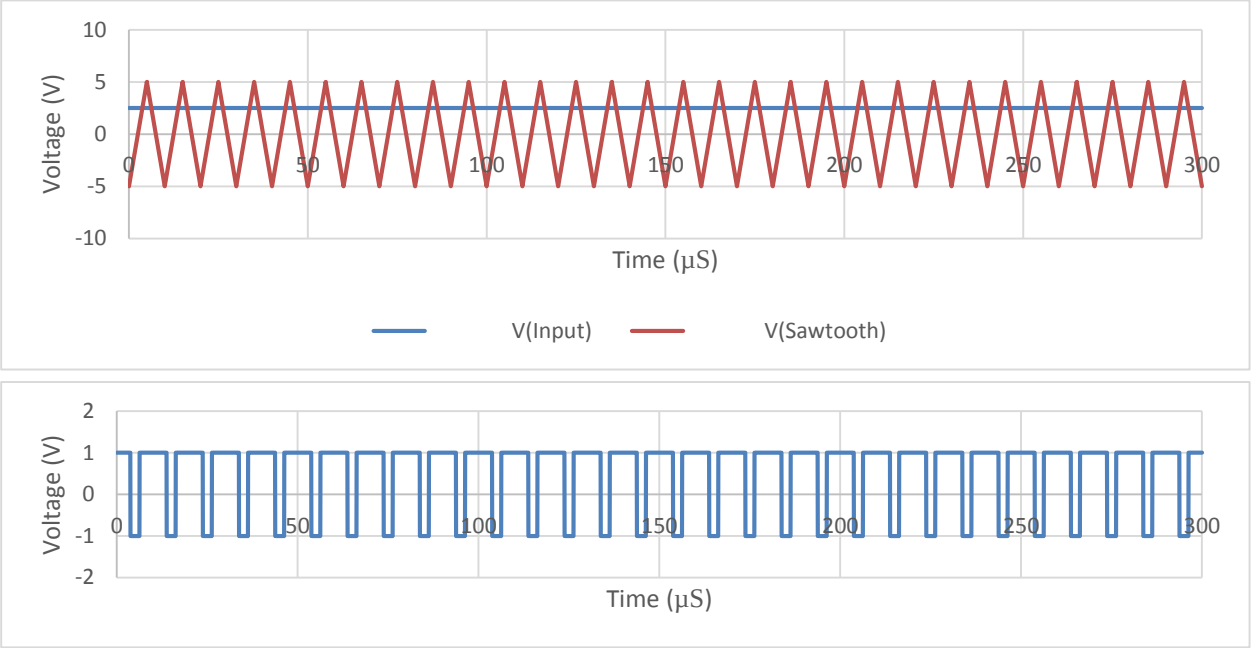

Figure 3.14 Comparison between fast saw-tooth signal and slow 2.5V signal.

The operation of averaging, as we have shown in the last example, is implemented as an electronic circuit in the form of a low-pass filter with the cut-off frequency lower than the frequency of the saw-tooth wave. This is because a low pass filter is, in effect, a moving average operator.

Now if the reference voltage was 0V (Figure 3.15), the duty cycle is would be 50%. After low pass filtering, or after the average operation, the output voltage is would be equal to

$$\overline{V_{OUT}} = 0.5 \times (5\text{V}) + 0.5 \times (-5\text{V}) = 0\text{V}.$$

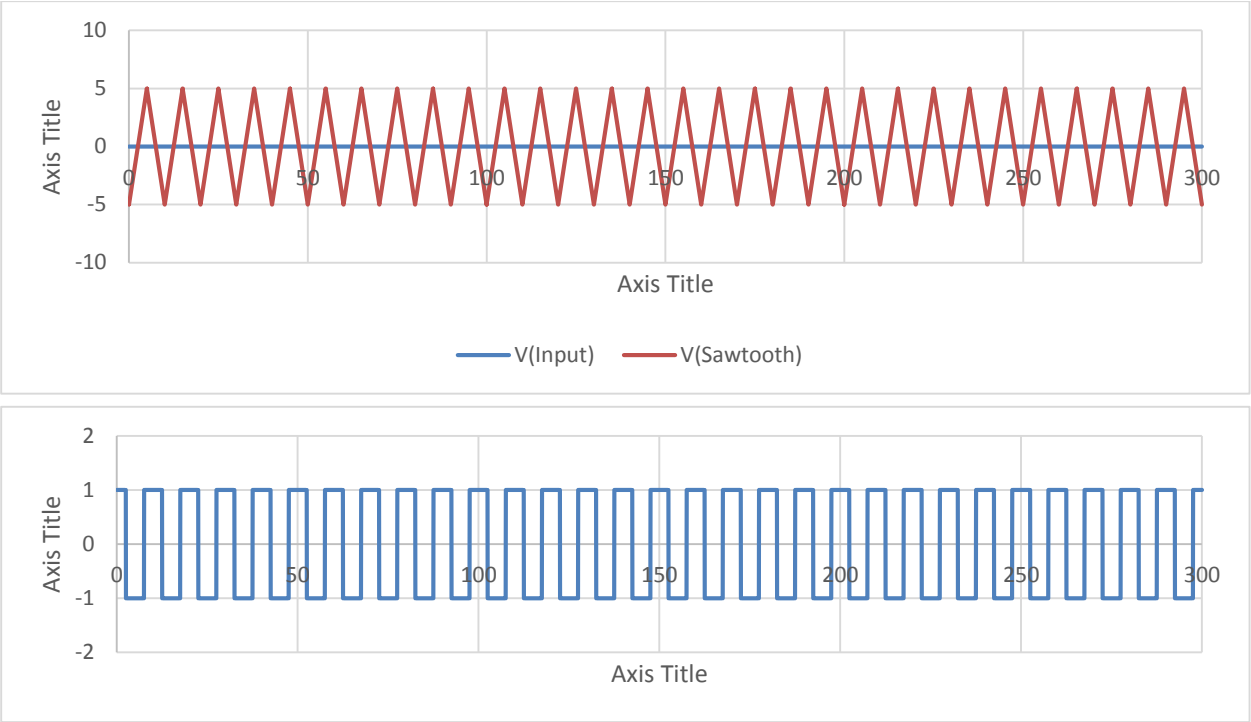

Figure 3.15 Comparison between fast saw-tooth signal and slow 0V signal.

What immediately becomes clear is that by means of low pass filtering (with a cut-off frequency less than the frequency of the rectangular signal form, i.e. the "fast" saw-tooth signal), we are able to recover the amplified reference signal of good quality at the output of the amplifier.

In practice, the reference signal or the input signal of the Class-D amplifier is not constant. As in the previous examples and the two considerations of part 3.3.4., if the frequency of the carrier signal is sufficiently larger than the frequency of the reference, the reference signal is considered almost constant within the cycle of the carrier. Thanks to this approximation, we are able to reproduce the reference signal through a low pass filter.

3.5.2. Low pass filter

As we have mentioned before, the amplified square signal is not suitable for a load, thus the amplifier needs a low pass filter to adjust the output signal for the load. It is known that switching MOSFETs or other transistors create high frequency harmonics and noise in output voltage waveform. By using a low pass filter, we can significantly attenuate the higher order harmonics while allowing signal (with frequency less than cut-off frequency) to create an output with minimal attenuation. In this part we will discuss the mechanics of a low pass filter and its characteristics.

- First order low pass filter

The order of a low pass filter is the highest order of ω or s in the denominator of its transfer function, and normally it is equal to the number of capacitors and inductors.

Usually, the first order LPF consists of a resistor and a capacitor so the transfer function has one pole. According to Figure 3.16, the transfer function is

$$F(s) = \frac{1}{1 + sRC}$$

Therefore, the cut off frequency is

$$\omega_c = \frac{1}{RC}, (\mathrm{f_c} = \frac{1}{2\pi \mathrm{RC}})$$

- Second order low pass filter

The main difference of the first order LPF and the second order LPF is the rate of roll off, which in the first order LPF is -20dB/decade, and in the second order LPF is -40dB/decade. A typical second order LPF is shown below consisting of a capacitor and an inductor. The transfer function is

$$F(s) = \frac{1}{1 + RCs + LCs^2}$$

Therefore, the cut off frequency is

$$\omega_c = \frac{1}{\sqrt{LC}}, (\mathrm{f_c} = \frac{1}{2\pi\sqrt{\mathrm{LC}}})$$

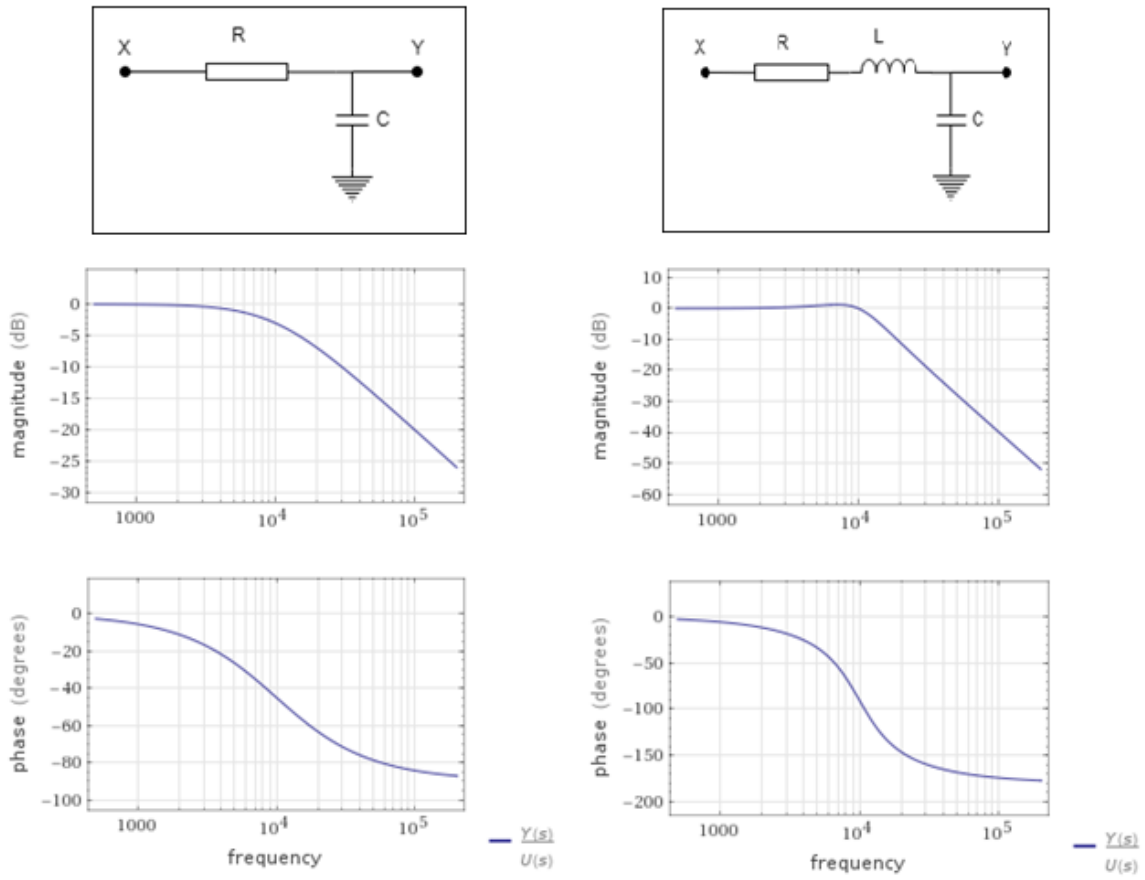

Figure 3.16 Comparison of 1st order LPF and 2nd order LPF with cut off frequency of 10kHz. Frequency response of 2nd order LPF (RLC) provides -40dB/decade roll-off rate for cut off frequency of 10kHz.

The frequency response of the Butterworth Filter approximation function is also often referred to as "maximally flat" (no ripples) because the pass band is designed to have a frequency response which is as flat as mathematically possible in the cut-off frequency range.

3.5.3. Design of the second order LPF

Basics

Suppose that we want to design an output filter for the amplifier in this thesis. The output filter is provided after amplifying the pulse signal with an amplitude of -300v to +300v and 100 kHz frequency. So based on the equation

$$U = L\,\frac{di}{dt}$$

We know that U is a partially constant voltage, therefore the inductor's current will be linear. (Figure 3.17 and Fig. 3. 18)

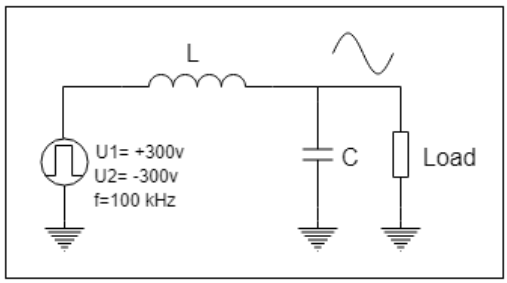

Figure 3.17 An illustration of resonance and how it can be used to changed signals, in this case rectangular signal signals into sine wave signals.

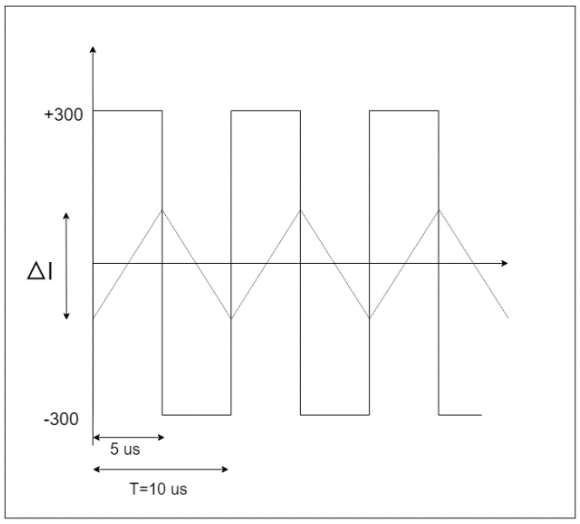

Figure 3.18 Inductance current and amplified PWM signal

Now suppose that $\Delta I = 5A$. Then by using a half cycle of the pulse signal, L can be calculated easily.

$$L = U\,\frac{dt}{di} = 300\ \times \frac{5\mu s}{5A} = 300\ \mu H$$

Instead of L=300 µH we use L=400 µH and C=1µF as the standard value for L and C for our design.

3.5.4. Design of output filter without active damping

In this part we will find the transfer function of the LPF without active damping (for load and no-load condition).

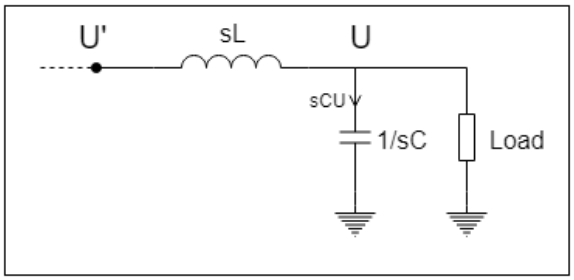

Figure 3.19 Output filter without active damping

- Without load analysis:

Let's consider a LC second order LPF (Figure 3.19) without a load. The circuit is a LC resonance, which in the previous part L and C were parameterized, so the next step is to find the cut-off frequency or resonance frequency for the circuit (LC filter).

Using the equations

$$f_s = \frac{1}{2\pi\sqrt{LC}}, Z_0 = \sqrt{\frac{L}{C}},\ L = 400\ \mu H \text{ and } C = 1\mu F,$$

we can find f_s and Z_0

$$f_s = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\ 20\ \mu s} \approx 8kHz$$

$$Z_0 = \sqrt{\frac{L}{C}} = \sqrt{\frac{400\ \mu H}{1\mu F}} = 20\ \Omega.$$

Now we need the transfer function of the LC resonance circuit in Laplace domain (Figure 3.19).

$$U' - U = sLI$$

We know the current through the capacitor is $I = sCU$, so

$$U' - U = s^2LCU$$

The transfer function, F(s), is

$$F(s) = \frac{U}{U'} = \frac{1}{1 + s^2LC}$$

The transfer function has no zeros, so in order to find the poles of the system

$$1 + s^2LC = 0 \Rightarrow S^2 = \frac{1}{LC},$$

The system has to have a pair of imaginary poles at

$$S_{1,2} = \pm j\frac{1}{\sqrt{LC}}$$

It is known that an imaginary pole pair that is lying on the imaginary axis generates an oscillatory component with a constant amplitude. (Figure 3.20)

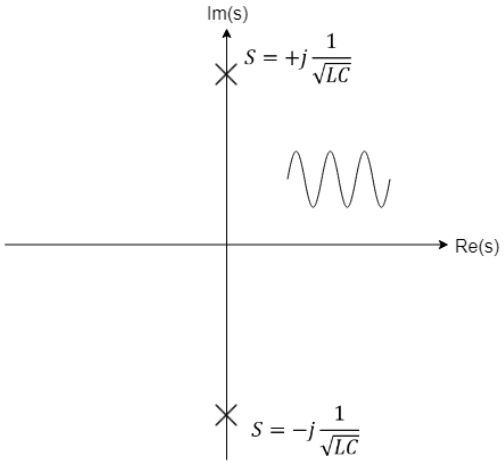

Figure 3.20 The pole-zero plot for LPF without active damping with an imaginary pole pair.

So an LPF without active damping acts as an oscillator that has a cut-off frequency of

$$Cut\ off\ frequency\ \ \omega_c = \frac{1}{\sqrt{LC}} = 5 \times 10^4\ Hz = 50\ kHz.$$

The frequency response of the transformation function $F(s) = \frac{1}{1+s^2LC}$ with cut off frequency of 50 kHz is shown in Figure 3.21.

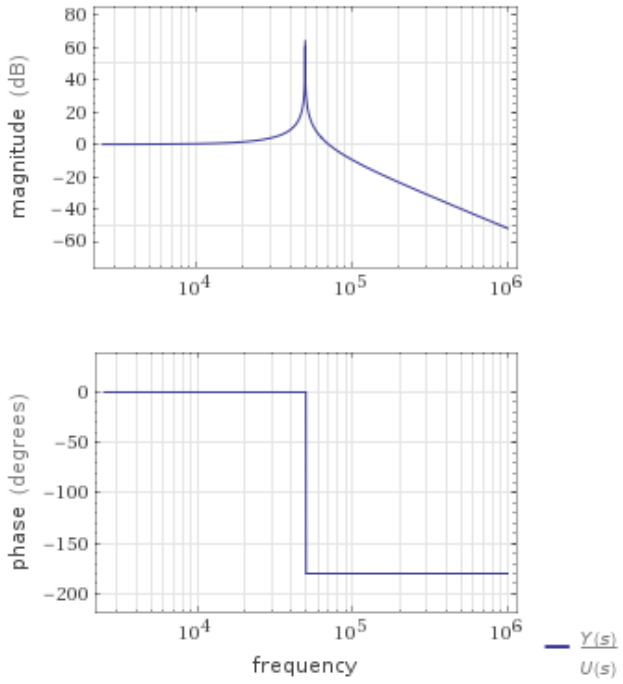

Figure 3.21 Bode plot of transformation function F(s)=1/(1+s^2 LC) with cut off frequency of 50 kHz.

The location of poles is an important factor when analyzing the stability of a system. The stability of a linear system may be determined directly by its transfer function. A nth order

linear system is asymptotically stable only if all of the components in the homogeneous response from a finite set of initial conditions decay to zero as time increases.

The figure below gives an overview of the impact of the location of the poles on the stability of a system:

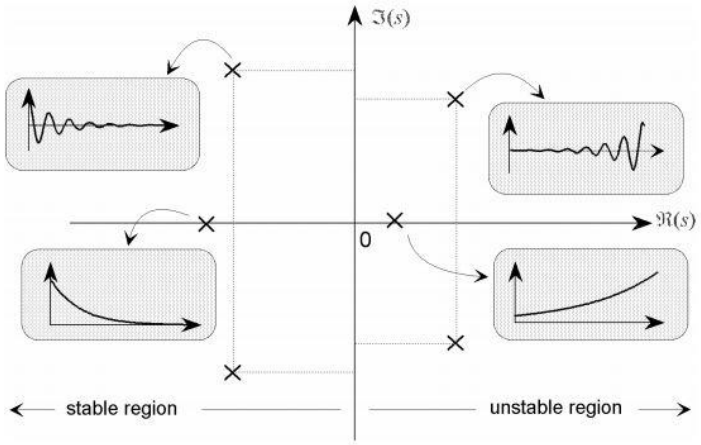

Figure 3.22 The specification of the form of components of the homogeneous response from the system pole locations on the pole-zero plot.[1]

In a stable system all components of the homogeneous response must decay to zero as time increases. If any pole has a positive real part, a component in the output that increases without bound, causes the system to be unstable.

In order for a linear system to be stable, all of its poles must have negative real parts, that is they must all lie within the left-half of the s-plane. An "unstable" pole lying in the right half of the s-plane generates a component in the system, causing a homogeneous response that increases without bound from any finite initial condition. A system having one or more poles lying on the imaginary axis of the s-plane has non-decaying oscillatory components in its homogeneous response, and is defined to be marginally stable.

The figure above illustrates that the system without active damping is marginally stable and will produce sustained oscillations in the output. In order to improve system stability, we have to move the poles to the left-half of the s-plane.

- With load analysis:

[1] Massachusetts Institute of technology, Department of Mechanical Engineering, 2.14 Analysis and Design of Feedback Control Systems
http://web.mit.edu/2.14/www/Handouts/PoleZero.pdf

Now suppose that there is a common load at the output, which in this case is called Z. First we have to determine the transfer function based on Figure 3.19

$$U' - U = sLI$$

We know the current through the capacitor is $I = (sCU + \frac{U}{Z})$, so

$$U' - U = sL(sCU + \frac{U}{Z})$$

$$U' = U(1 + s\frac{L}{Z} + s^2LC)$$

The transfer function, F(s), is

$$F(s) = \frac{U}{U'} = \frac{1}{1 + s\frac{L}{Z} + s^2LC}$$

Therefore, the system has a just pair of poles based on the value of Z, which can determine the location of the poles

$$1 + s\frac{L}{Z} + s^2LC = 0$$

In order to simplify the equation above, we must replace

$$Z_0 = \sqrt{\frac{L}{C}} \ \ and \ \ x = s\sqrt{LC}, \text{ so}$$

$$1 + s\sqrt{LC}\frac{\sqrt{\frac{L}{C}}}{Z} + s^2LC = 0$$

The final equation is

$$1 + \frac{Z_0}{Z}x + x^2 = 0$$

We can consider three possibilities for this equation based on the value of Z:

a) $Z = \infty \ \Rightarrow \ 1 + x^2 = 0 \ \Rightarrow x_{1,2} = \pm j \ (without \ load)$

An imaginary pole pair, that generates an oscillator, which is marginally stable.

b) $Z = R = Z_0 \Rightarrow \ 1 + x + x^2 = 0 \ \Rightarrow \ x_{1,2} = \frac{-1 \pm j\sqrt{3}}{2}$, has no problem with stability, for compared to Z=∞, the poles are on the left-half of the s-plane (stable half).

A complex conjugate pole pair (σ ± jω) generates a response component that is a decaying sinusoid of the form $Ae^{-\sigma t}\sin(\omega t + \varphi)$.

c) $Z = R = \frac{Z_0}{2} \Rightarrow 1 + 2x + x^2 = 0 \Rightarrow (1+x)^2 = 0 \Rightarrow x_{1,2} = -1$

A real pole −σ (negative pole) generates an exponentially decaying component, $Ae^{-\sigma t}$. Like part b it is also stable due to location of the poles. If σ were to be much larger than the ω transient response, then oscillation would occur.

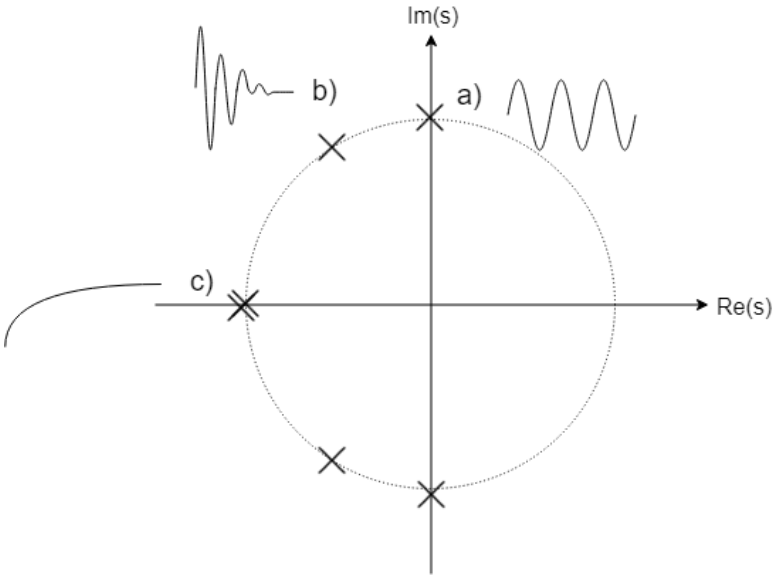

Figure 3.23 The pole-zero plot for second order LPF without active damping with different loads.

If we compare the three possibilities for designed Class-D amplifier in time domain, as shown in Figure 3.24, the circuit without the load cause oscillation and it generates an undesired sinusoidal at the output. For Z=20Ω= Z_0 amplifier generates a response component that is a decaying sinusoid of the form $Ae^{-\sigma t}\sin(\omega t + \varphi)$. And for Z=10Ω it generates an exponentially decaying component, $Ae^{-\sigma t}$. In conclusion, the best solution is to have the complex pole pair fall in the left-half of s plane and the σ be much larger than ω in order to avoid oscillation.

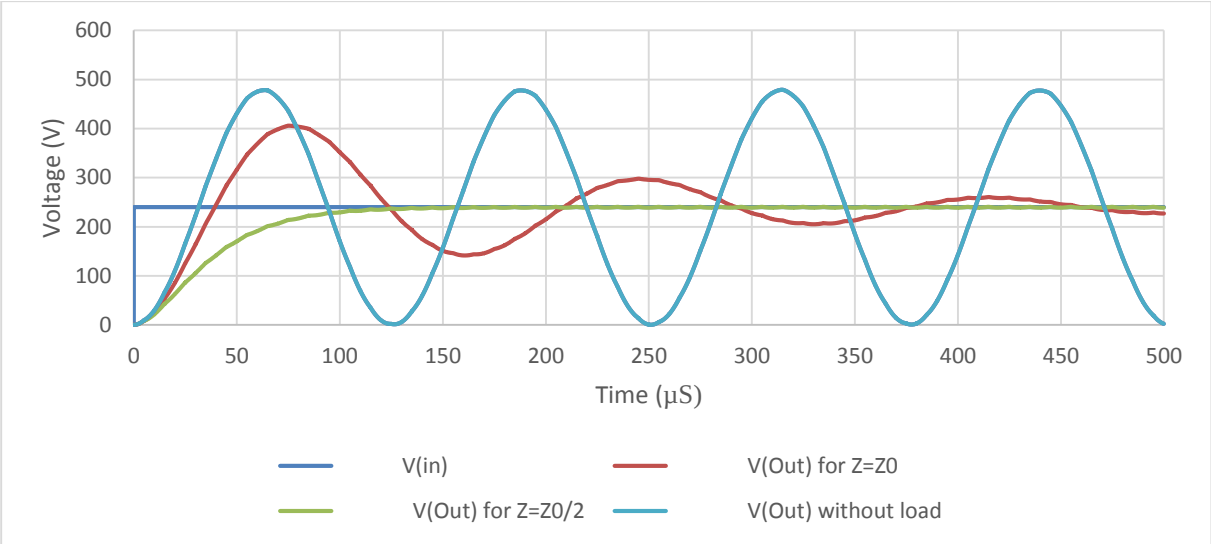

Figure 3.24 Output voltage of Class-D amplifier without active damping without load vs. with different load for Z=$\frac{Z_0}{2}$, $Z = Z_0$.

3.5.5. Design of output filter with active damping

In the previous part we faced a problem in our design: losing system stability. In order to solve this problem, we moved the location of the poles to the left-half of the s-plane by using a proper load. Examining proper damping also in no-load condition, our system needs active damping, for example from a current-controlled voltage source (CCVS).

The CCVS is an ideal dependent current-controlled voltage source, because it maintains an output voltage equal to some multiplying constant (R) times a controlling current input generated elsewhere within the connected circuit. Then the output voltage "depends" on the value of the input current, again making it a dependent voltage source.

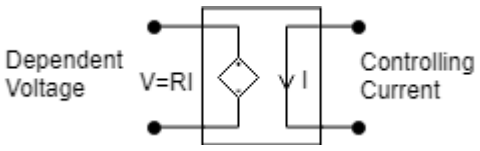

Figure 3.25 Schematic of current-controlled voltage source

As a controlling current, I_{IN} determines the magnitude of the output voltage V_{OUT} times the magnification constant R. This allows us to model a current-controlled voltage source as a trans-resistance amplifier as the multiplying constant, R gives us the following equation: $V_{OUT} = RI_{IN}$. This multiplying constant R has the units of Ohm's because

$R = \frac{V_{out}}{I_{IN}}$, and its units will therefore be $\frac{\text{volts}}{\text{amperes}}$.

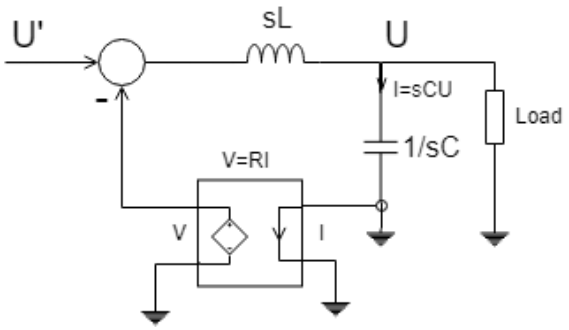

Figure 3.26 Output filter with active damping.

- No-load analysis:

Now we need the transfer function of the second order LPF in Laplace domain based on figure 3.26. In our design we use the current of the capacitor in the output filter as a controlling current and, the current of the capacitor, as well as the current of inductor, is

$$I_C = sCU, \text{ so}$$

$$U' - RsCU = sL(sCU) + U$$

$$U' - RsCU = s^2LCU + U$$

$$U' = U(1 + RsC + s^2LC).$$

The transfer function, F(s), is

$$F(s) = \frac{U}{U'} = \frac{1}{1 + RsC + s^2LC}$$

Transfer function has no zeros, the poles of the system are given by

$$1 + sRC + s^2LC = 0$$

Again the system has a complex conjugate pole pair on the left-half of the s-plane

$$s_{1,2} = \frac{-RC \pm j\sqrt{4LC - (RC)^2}}{2LC}.$$

Figure 3.27 and 3.28 show the frequency response and pole-zero plot of the system using active damping without load.

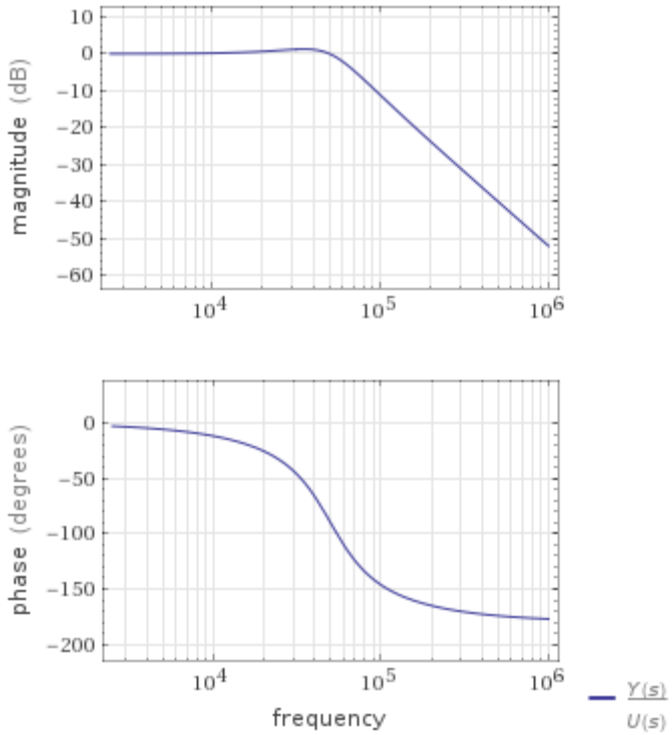

Figure 3.27 Bode plot of transformation function F(s)= 1/(1+RsC+s^2 LC) with cut off frequency of ω= 50 kHz for R=20.

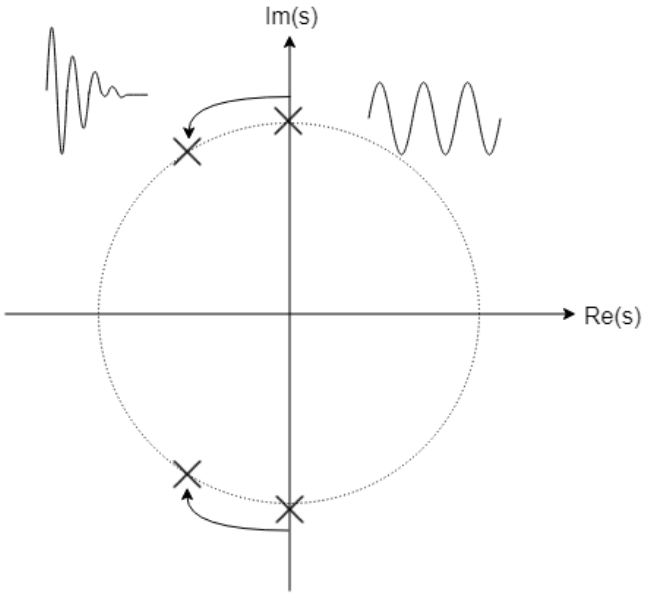

Figure 3.28 Pole-zero plot for the output filter with active damping without load.

- With load analysis:

Like in the previous part, we are trying to find the transfer function while considering the load at the output. The current of the inductor in this case is $I_L = sCU + \frac{U}{Z}$, so

$$U' - RsCU = sL(sCU + \frac{U}{Z}) + U$$

$$U' = U(1 + s(RC + \frac{L}{Z}) + s^2LC)$$

The transfer function, F(s), calculates to

$$F(s) = \frac{U}{U'} = \frac{1}{1 + s(RC + \frac{L}{Z}) + s^2LC}$$

Therefore, the system again has just a pair of poles based on the value of Z, so we can determine the location of the poles.

$$1 + s(RC + \frac{L}{Z}) + s^2LC = 0$$

In order to simplify above equation, we must rewrite the equation with parameters including: $Z_0 = \sqrt{\frac{L}{C}}\ \ and\ \ x = s\sqrt{LC}$, so

$$1 + (\frac{Z_0}{Z} + \frac{R}{Z_0})x + x^2 = 0$$

I. $Z = \infty \Rightarrow 1 + \frac{R}{Z_0}x + x^2 = 0 \Rightarrow x_{1,2} = \frac{-\frac{R}{Z_0} \pm j\sqrt{(\frac{R}{Z_0})^2 - 4}}{2}$ (without load which we discussed before)

II. $\frac{Z_0}{Z} + \frac{R}{Z_0} = 0 \Rightarrow 1 + x^2 = 0 \Rightarrow x_{1,2} = \pm j$

Du to positive amount of loads it's clear that with active damping no oscillation occurs at the output because

$$\frac{Z_0}{Z} + \frac{R}{Z_0} = 0 \Rightarrow Z = -\frac{{Z_0}^2}{R}\ (Z_0 > 0, R \geq 0)$$

Although with a negative resistor the amplifier is marginally stable, it is not a likely situation for the system, and we also cannot use a negative resistor as a load at the output. Thus by using active damping, the problem of oscillation is solved completely.

III. $\frac{Z_0}{Z} + \frac{R}{Z_0} = 1 \Rightarrow Z = \frac{{Z_0}^2}{Z_0 - R} \Rightarrow 1 + x + x^2 = 0 \Rightarrow x_{1,2} = \frac{-1 \pm j\sqrt{3}}{2}$

This is a special example that shows poles are moved from imaginary axis to left-half of the s-plane.

IV. $\frac{Z_0}{Z} + \frac{R}{Z_0} = 2 \Rightarrow Z = \frac{{Z_0}^2}{2Z_0 - R} \Rightarrow 1 + 2x + x^2 = 0 \Rightarrow (1 + x)^2 = 0 \Rightarrow x_{1,2} = -1$

Because the denominator is Hurwitz polynomic, system will be stable. The larger $\frac{Z_0}{Z} + \frac{R}{Z_0}$ the nearer first pole to the zero point of coordinate system will be and the farther the second pole from the zero point of the coordinate system will be.

In conclusion, active damping has a great influence on the stability of an amplifier. This part can be summarized below:

- $\frac{Z_0}{Z} + \frac{R}{Z_0} = 0$, marginal stable with a pole pair on the imaginary axis in the case of a negative resistor or in case there is a negative resistor
- $0 < \frac{Z_0}{Z} + \frac{R}{Z_0} < 2$, stable with a complex conjugate pole pair on the left-half of the s-plane
- $\frac{Z_0}{Z} + \frac{R}{Z_0} > 2$, stable with a pole pair on the real axis

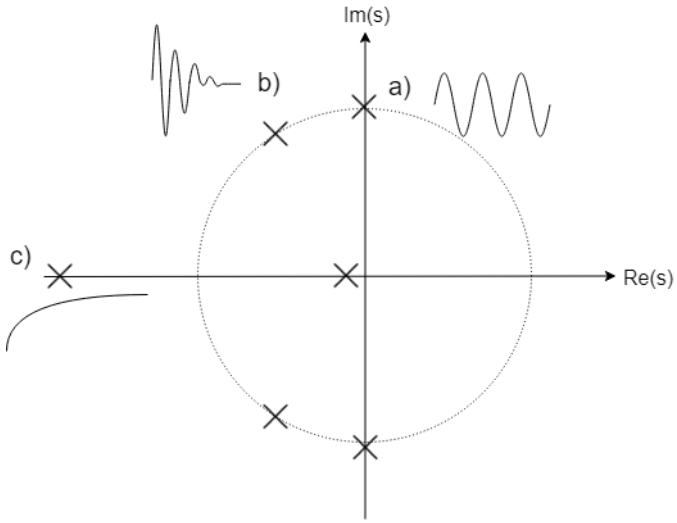

Figure 3.29 Pole-zero plot for the output filter with active damping with different loads.

a) $\frac{Z_0}{Z} + \frac{R}{Z_0} = 0$ ($in\ case\ of\ negative\ resistor$), b) $0 < \frac{Z_0}{Z} + \frac{R}{Z_0} < 2$, and c) $\frac{Z_0}{Z} + \frac{R}{Z_0} > 2$.

Figure 3.30 shows the impact of active damping on the transient response of the Class-D amplifier in time domain. In comparison to the case without active damping, the new

designed LPF is more stable and reliable. One of the biggest advantages of the new design LPF is that the oscillation problem of an unloaded amplifier has been solved.

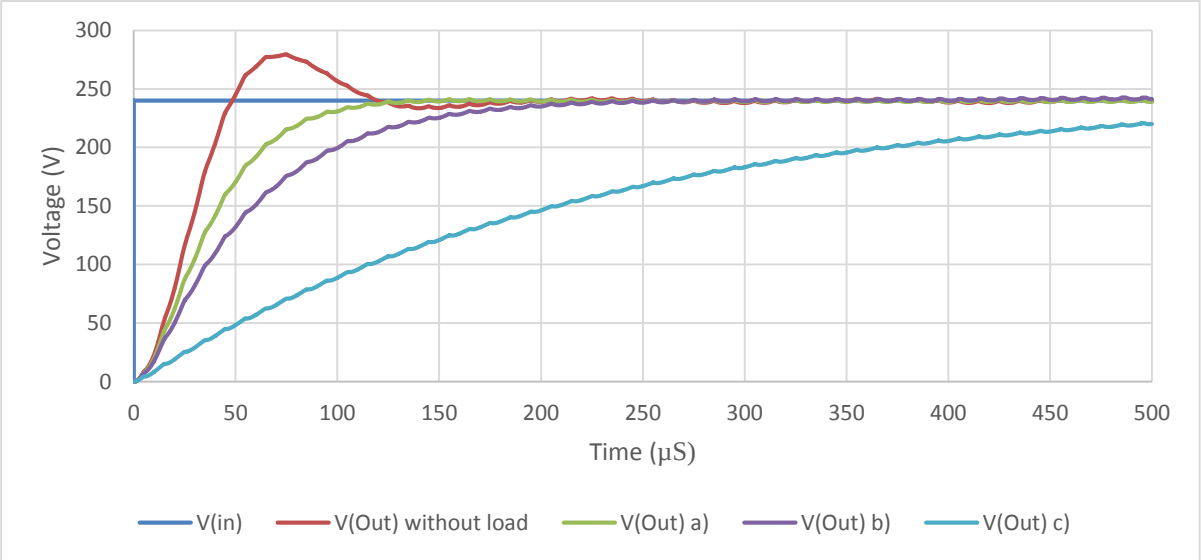

Figure 3.30 Output voltage with active damping without load vs. with different loads. a) $\frac{Z_0}{Z}+\frac{R}{Z_0}=1$ **b)** $\frac{Z_0}{Z}+\frac{R}{Z_0}=2$ **and c)** $\frac{Z_0}{Z}+\frac{R}{Z_0}=10$

3.5.6. Some other properties of amplifier

Gain of amplifier

The gain of a Class-D amplifier depends on the following parameters:

(i) Duty cycle (D),
(ii) Supply voltage of the Power Driver (V_{SUPPLY}) and
(iii) Maximum voltage of the carrier signal (in our case Saw-tooth) $V_{Saw,max,}$ so

$$G = D \times \frac{V_{Supply}}{V_{Saw,max}}.$$

This means that if for any reason the V_{SUPPLY} power supply voltage changes, the amplifier gain will also change.

Power Supply Rejection Ratio (PSRR)

The amplifier is completely transparent to variations in the power supply, in which the output signal is modulated by the supply voltage. It is used to describe this susceptibility known as Power Supply Rejection Ratio (PSRR) and defined as:

$$PSRR = \frac{\Delta V_{Supply}}{\Delta V_{out}}$$

A good amplifier has small variations of output voltage (ΔV_{OUT}) to go against the variations in supply voltage ΔV_{Supply}, therefore it has a high PSRR. The PSRR is typically expressed in dB, and good amplifiers are typically 60dB or higher. In our case, a Class-D amplifier,

which was described in previous parts, has a variation in output voltage that is exactly the same with the variation of the Supply voltage, which means

$\Delta V_{OUT} = \Delta V_{Supply}$, i.e. the PSRR = 1 = 0dB.

3.6. Switch-mode power supply vs. Class-D amplifier

Let us consider the block diagram of a Class-D amplifier with two different inputs. We have seen before that the output voltage, after the demodulation and filtering depends on the duty cycle D of the PWM signal generated at the output of the amplifier. We did an approximation that (in a special situation) shows that the slow reference signal is constant.

If the reference signal is constant, then the comparator would generate a PWM signal with a constant duty cycle. In order to obtain a circuit capable of generating an appropriate amplified constant voltage at the output, capable of delivering the necessary current to the load.

A circuit of this type is nothing more than a DC power supply. In fact, the PWM technique is effectively used in both Class-D amplifiers and switch-mode power supplies. Due to the high efficiency of the system, it is possible to obtain high power feeders with small transformers and low weight, and equally small and light power amplifiers.

The power supplies that use PWM technique or similar switching techniques are called Switched-Mode Power Supplies (SMPS) and they have many advantages compared to the classic linear power supply.

In Figure 3.31, we see a comparison between a switch-mode power supply and a Class-D amplifier where the operating principle is basically the same.

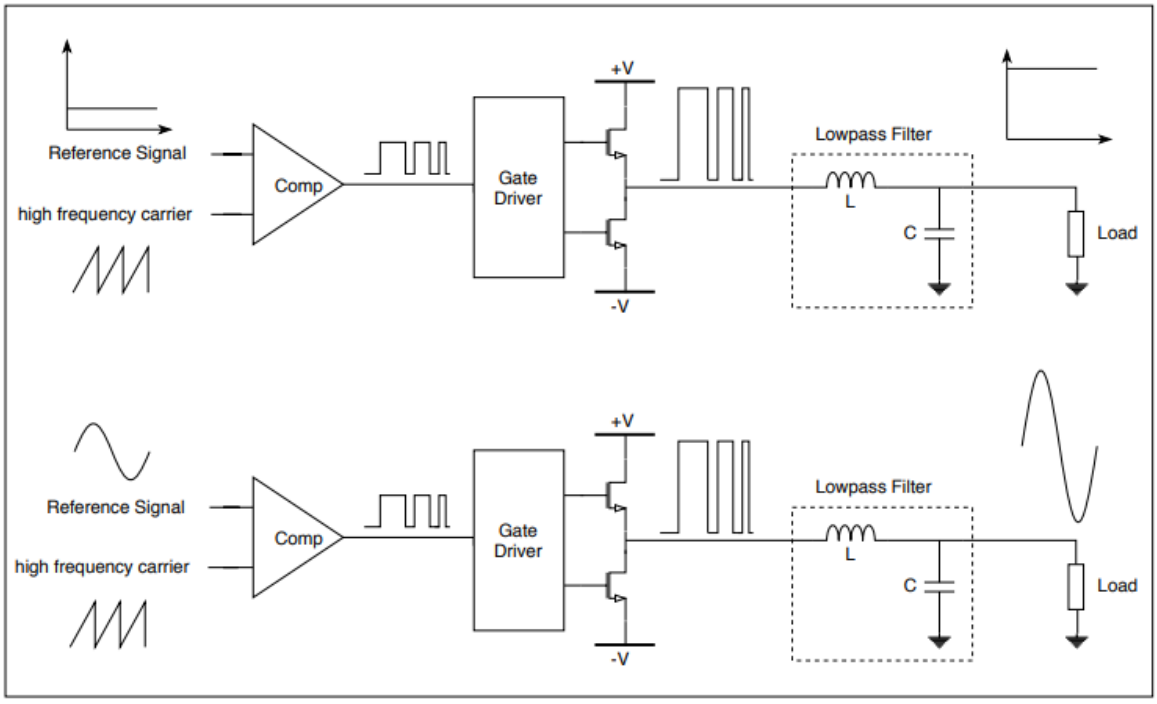

Figure 3.31 Comparison between a switching power supply (SPS) and a simple Class-D amplifier.

In the case of the switch-mode power supply, the reference input signal usually is a constant unipolar voltage. Thus the duty cycle of the output PWM signal is constant, unlike the variable duty cycle of the Class-D amplifier - which is the biggest difference between these two circuits.

Another difference between a switch-mode power supply and a Class-D amplifier is that a switch-mode power supply is designed to provide a constant voltage and needs to be controlled only to cope with small unwanted variations of the output voltage, whereas in a Class-D amplifier such variations are desired.

3.7. Negative feedback

Up until now, the basis of all calculations, designs, and simulations was that the system is open-loop and works without output voltage feedback. It is obvious that sensitivity to noise of the open-loop system is high, so if there is a disturbance or some noise, the system cannot track a reference signal well, and in some cases, the system even will become unstable. The best solution of to this problem is to implement a feedback and a PI controller to the open-loop system to counteract disturbance signals that may affect the output signal and to stabilize the unstable system (Figure 3.32).

A close-loop system is formed by a passive feedback circuit and a configured operational amplifier as supplements, or as a low pass filter. In this way it is possible to fix both the general gain of the low frequency stage and the bandwidth of the frequency response of the amplifier.

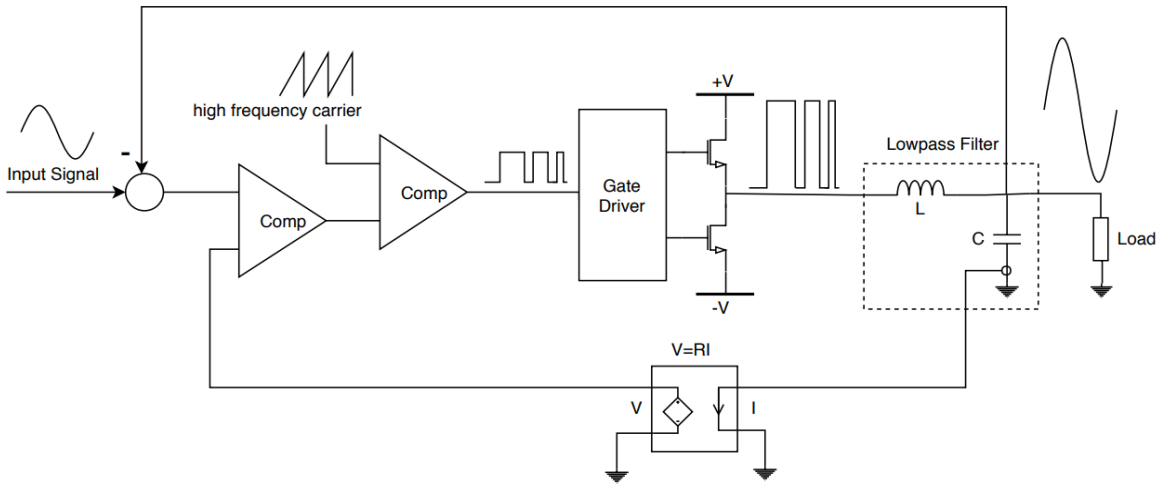

Figure 3.32 The basic block diagram for a Half Bridge Class-D amplifier, with the waveforms at each stage. This circuit uses feedback from the output of the half-bridge to help compensate for variations in the bus voltages.

It is known that open-loop gain of real amplifiers is a function of frequency. Magnitude response drops off and phase shift increases at high frequencies. When feedback is applied to the open-loop amplifier, undesirable frequency responses, as well as undesired transient responses can occur.

Considering frequency dependence, the closed-loop gain of a feedback amplifier should be re-formatted as a function of Laplace variable S, like in the following open-loop transfer function:

$$F_O(s) = \frac{b_0}{a_2 s^2 + a_1 s + a_0}$$

$$F_O(s) = K \frac{{\omega_n}^2}{s^2 + 2\xi\omega_n s + {\omega_n}^2}$$

Where $\omega_n = \frac{a_0}{a_2}$, $\xi = \frac{a_1}{2\sqrt{a_2 a_0}}$, $K = \frac{b_0}{a_0}$ $(open - loop\ gain)$

Now assume that the feedback ratio is 1, then the closed-loop transfer function results to

$$F_C(s) = \frac{F_o(s)}{1 + F_{o(s)}} = K \frac{{\omega_n}^2}{s^2 + 2\xi\omega_n s + (K+1){\omega_n}^2}$$

The zeros and poles of the closed loop transfer function are the key to understanding the behavior of a Class-D amplifier with feedback.

Negative feedback has a great effect on the location of the poles, which consequently affects the transient response and frequency response of the amplifiers. Let's try to see these effects on the Class-D amplifier. Considering a second order LPF, the open loop gain is in the form

$$F_O(s) = K \frac{{\omega_n}^2}{s^2 + 2\xi\omega_n s + {\omega_n}^2} = K \frac{{\omega_n}^2}{(s + \omega_n(\xi + \sqrt{\xi^2 - 1})(s + \omega_n(\xi - \sqrt{\xi^2 - 1})}$$

and evaluated transfer function of the closed loop

$$F_C(s) = \frac{F_o(s)}{1 + F_{o(s)}} = K \frac{{\omega_n}^2}{s^2 + 2\xi\omega_n s + (K+1){\omega_n}^2}$$

$$= K \frac{{\omega_n}^2}{(s + \omega_n(\xi + \sqrt{\xi^2 - (K+1)})(s + \omega_n(\xi - \sqrt{\xi^2 - (K+1)})}$$

As parameter K increases, the poles of the transfer function move together until they meet at a point in the middle point. Further increase causes the poles to become complex, moving away from the real axis along the vertical line across the meeting point. (root locus)

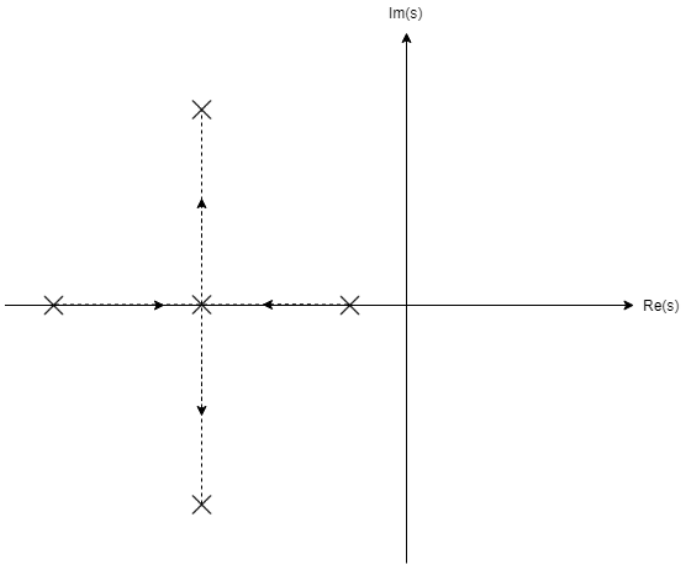

Figure 3.33 Root locus diagram of the close-loop Class-D amplifier (second order LPF).

Usually feedback amplifiers are designed so that K is much larger than 1, which is usually necessary to achieve gain stabilization, impedance control, nonlinear distortion reduction etc.

3.8. PI controller

In addition to feedback, overdamped processes are necessary because there is no tendency to have oscillation, and self-regulation is needed because we are looking for a steady state operating level as well. The block diagram of the closed loop Class-D amplifier with a PI controller is shown in Figure 3.34.

$$PI - Controller \ \rightarrow \ R(s) = K_P \ \frac{1+sT}{sT},$$

where K_P is Proportional gain and T is integral time.

The PI controller is ideal because it may eliminate oscillation, it has fast responses due to proportional parts, and it has a zero steady state error, due to integral parts/an integral part. However, the PI controller is nonlinear in case of override (wind-up) and the integral part has a negative effect on the speed of the amplifier. Thus, it is a more useful when the speed of response of the system is not an important issue.

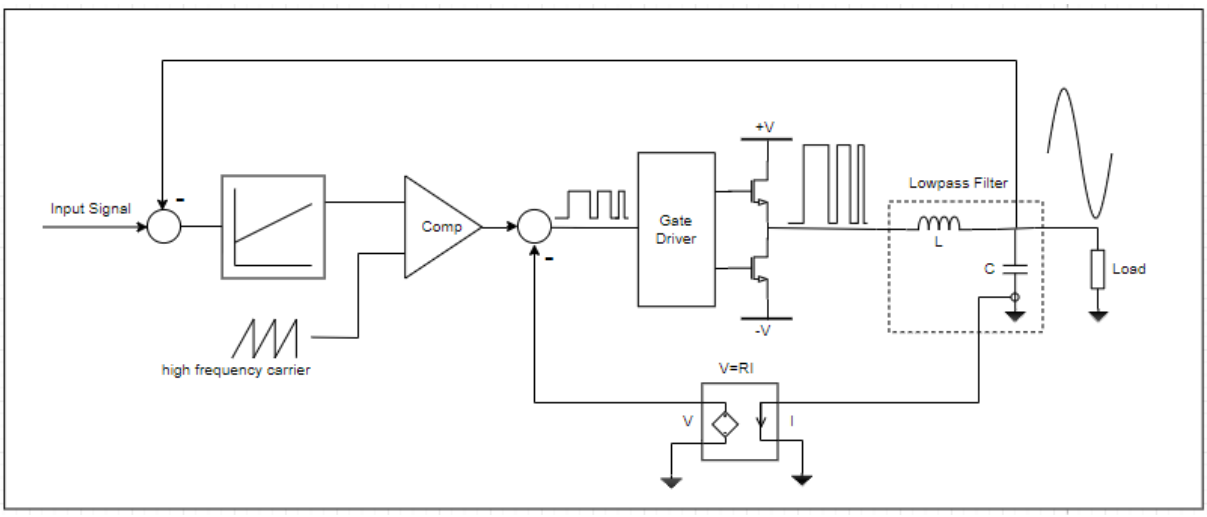

Figure 3.34 Schematic of Class-D amplifier with negative feedback and PI controller.

4. Design of Class D amplifier with higher order Butterworth filter

4.1. Basics

In some applications we need a filter to shape the frequency spectrum of a special signal. But if a first order filter is used, the width of the roll-off would be too wide. So if we go one step further and design a filter that has more than one stage, we have a higher order filter. The complexity of a filter is usually defined by the filter order. A higher order filter, or nth order filter, has n reactive components (capacitor or inductor) in its design. Consequently, the rate of roll off depends on the order of the active filter. Thus nth order filter has a roll off rate of 20n/decade. One way to make a higher order LPF, for example fourth order filter, is to cascade two second order low pass filters.

In order to design an ideal LPF and find the transfer function, there are some mathematical approximations that need to be made, like Butterworth, Chebyshev and Bessel. In this thesis, a low pass Butterworth filter has been used because it has the best approximation of the transfer function a Class D amplifier usually requires. Another advantage of a low pass Butterworth filter is that the frequency response of this filter is maximally flat, (compare to other approximations) which means it has no ripple until the cut-off frequency. Not surprising then is that the low pass Butterworth filter achieves a maximally flat frequency response at the expense of a relatively wide transition region from pass band to stop band, with average transient characteristics.

Note that the higher the Butterworth filter order, the more the reactive components in the filter design are required, but the closer the frequency response of the Butterworth filter is to the ideal “brick wall” response.

4.2. Butterworth filter and its operation[2]

The transfer function of a low pass filter has the general form

$$A(S) = \frac{A_0}{1 + c_1 S + c_2 S^2 + \cdots + c_n S^n} \qquad (1)$$

Where $c_1, c_2 \ldots c_n$ are positive and real. The order of the filter is equal to the highest power of S. The best way to design the filter is to have the denominator polynomial in factored form. If complex poles are also permitted, a separation into linear factors, as in the equation

[2] Electronic Circuits design and applications U.Tietze, Ch. Schenk, Springer-Verlag Berlin, Heidelberg 1991

$$A(S) = \frac{A_0}{(1+\alpha_1 S)(1+\alpha_2 S) \dots (1+\alpha_n S^n)} \qquad (2)$$

is no longer possible, and a product of quadratic expressions is obtained:

$$A(S) = \frac{A_0}{(1+a_1 S+b_1 S^2)(1+a_2 S+b_2 S^2) \dots} \qquad (3)$$

Where a_i and b_i are positive and real. For odd orders n, the coefficient b_1 is zero. There are several different theoretical aspects with respect to which the frequency response can be optimized. Any such aspect leads to a different set of coefficient a_i and b_i. As we will demonstrate, the conjugate complex poles will arise. They cannot be realized by passive RC elements. One way of implementing conjugate complex poles is to use RLC networks. For high frequencies, the design of the necessary inductances usually presents no difficulties, but in the low frequency range, large inductances are often required. Although large inductances are unwieldy and have poor electrical properties, the use of inductances with low frequencies can be avoided by adding active elements to the RC network. Such circuits (RLC network) are called active filters. One of the most important optimized frequency responses is the Butterworth low pass filter. Butterworth low pass filters have an amplitude-frequency response which is flat for as long as possible and falls off sharply just before the cut-off frequency. Their step response shows a considerable overshoot that reaches up to a higher-order filter.

The absolute value of the gain of a nth order low pass filter has the general form

$$\left|\underline{A}\right|^2 = \frac{{A_0}^2}{1+k_2\Omega^2+k_4\Omega^4+\cdots+k_{2n}\Omega^{2n}} \qquad (4)$$

Odd powers of Ω do not occur since the square of $\left|\underline{A}\right|$ must be an even function. Below the cutoff frequency of the Butterworth low pass filter, the function $\left|\underline{A}\right|^2$ must be maximally flat. Because in this range $\Omega < 1$, this condition is best fulfilled if $\left|\underline{A}\right|^2$ is dependent only on the highest power of Ω. The reason being that for $\Omega < 1$, the lower powers of Ω contribute most to the denominator and consequently, to the fall-off in gain. Hence

$$\left|\underline{A}\right|^2 = \frac{{A_0}^2}{1+k_{2n}\Omega^{2n}}$$

The coefficient k_{2n} is defined by the "normalizing condition", which means that the gain at $\Omega = 1$ is reduced by 3 db. Thus

$$\frac{{A_0}^2}{2} = \frac{{A_0}^2}{1+k_{2n}},$$

$$k_{2n} = 1.$$

Therefore, the square of the gain of n-th order Butterworth low pass filter is given by

$$\left|\underline{A}\right|^2 = \frac{{A_0}^2}{1 + \Omega^{2n}} \quad (5)$$

To implement a Butterworth low pass filter, a circuit must be designed in which the square of the gain has the form given above. However, the circuit analysis initially gives the complex gain $\underline{A}$, and not the gain squared, $\left|\underline{A}\right|^2$.

Therefore, it is necessary to know the complex gain involved in Eq. (5). This is found by calculating the absolute value of Eq. (1) and by comparing the coefficients with those of Eq. (5). In this way, the desired coefficients $c_1 \ldots c_n$ can be defined. The denominators of Eq. (1) are then the Butterworth polynomials, of which the first four orders of which are shown in table below.

n	
1	$1 + S$
2	$1 + \sqrt{2}S + S^2$
3	$1 + 2S + 2S^2 + S^3 = (1+S)(1+S+S^2)$
4	$1 + 2.613S + 3.414S^2 + 2.614S^3 + S^4 = (1 + 1.848S + S^2)(1 + 0.765S + S^2)$

Table 4.1 Table of coefficients of Butterworth filter for n=1 to n=4.

The coefficients of the Butterworth polynomials up to the order 10 are shows in Figure below.

It can be seen that the first-order Butterworth low pass filter is a passive low pass filter having the transfer function of

$$A(S) = \frac{1}{1 + S}.$$

The higher Butterworth polynomials possess conjugate complex zeros. The comparison in with Eq. 1 shows that such denominator polynomials cannot be implemented by pure passive RC networks, because in the case of the latter, all the zeros are real. In such cases, the only choice is to use RLC circuits with all of their disadvantages, or active RC filters. The frequency response of the gain is shown below in Figure 4.1.

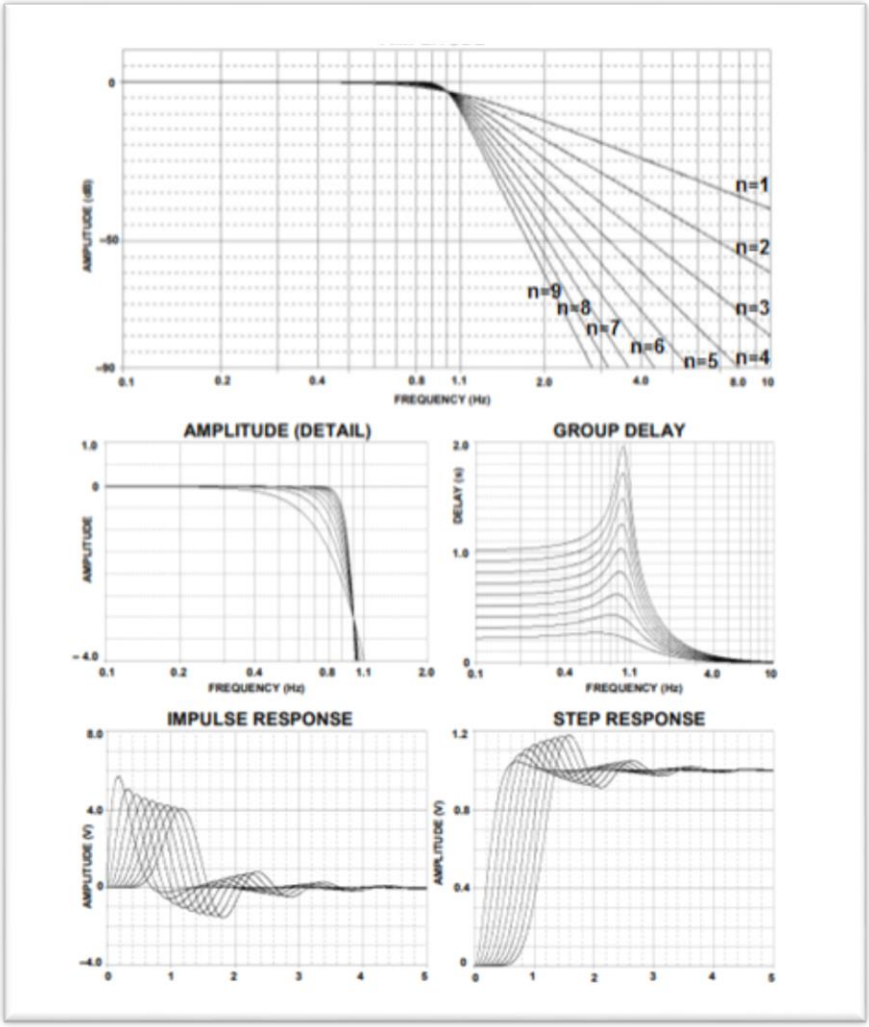

Figure 4.1 Butterworth responses[3].

4.3. Class D amplifier with second order low pass Butterworth filter

In order to make it easier to understand the function and to find the transfer function of the control system, the control system below is used. In this simplified system we are using active damping, a PI controller and feedback.

[3] **Hank Zumbahlen, Basic linear design, Editor, 2007, Analog Devices, Inc. ISBN 0-916550-28-1**

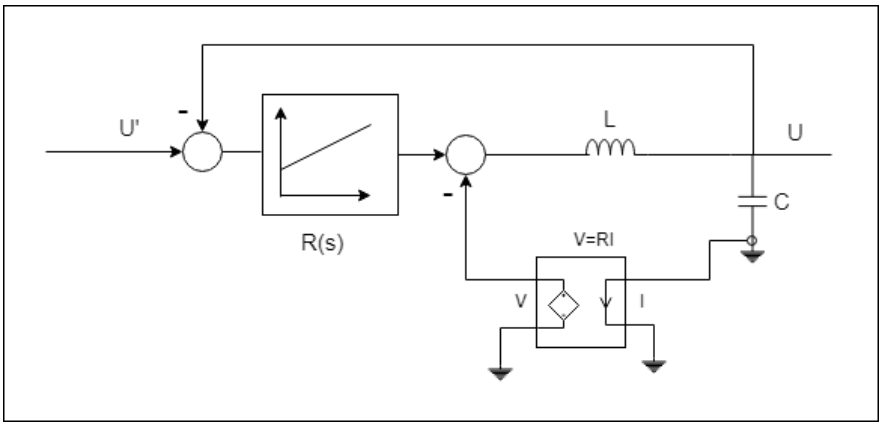

Figure 4.2 Voltage Regulator with 2nd order Butterworth filter.

The input signal U' needs to be amplified and regulated. G(s) is the transfer function of the second stage, which includes the low pass Butterworth filter with active damping and R(s) representing the transfer function of PI controller. This is given by the following relation

$$PI - Controller \rightarrow R(s) = \frac{1 + sT}{sT}$$

Using control theory, the transfer function of this amplifier can be found easily with a low pass 2nd order Butterworth. The values of the inductor and capacitor are selected from our design in chapter 3 (L=400µH and C=1µF). A closed loop transfer function of the above circuit is

$$F(s) = \frac{U}{U'} = \frac{F_o}{1+F_o} = \frac{Z}{Z+N}.$$

Here Fo is open loop transfer function and defined as

$$F_o = R(s).G(s) = \frac{Z}{N}$$

Now using the given values of L and $L = 400\ \mu H$, $C = 1\ \mu F$, cut-off frequency is

$$\omega_0 = \frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{400\ \mu H * 1\ \mu F}} = \frac{1}{20\ \mu s} = 50\ kHz$$

$$(f_0 = \frac{1}{2\pi\sqrt{LC}} = 8\ kHZ\ \ resonance\ frequency)$$

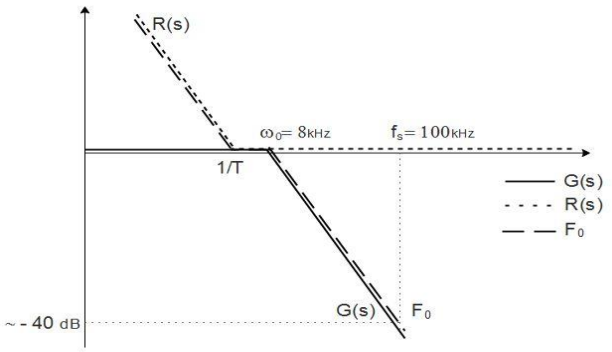

Figure 4.3 Bode plot for Voltage Regulator with 2nd order Butterworth filter.

If we define the T coefficient of the PI controller as:

$$T = \frac{1}{\omega_0} \rightarrow T = \ 20\ \mu s$$

the transfer function of PI controller will be:

$$PI - Regulator \ \rightarrow \ R(s) = \frac{1 + 20\ \mu s.S}{20\ \mu s.S}$$

The second stage has two reactive components so the transfer function includes two poles. Now to find G(s) -just like the design of LPF- with an active damping transfer function is

$$G(s) = \frac{1}{1 + sRC + s^2\,LC}.$$

We suggest to change the variables using $X = s\sqrt{LC}$, so PI controller will be

$$R(s) = \frac{1 + cX}{cX}$$

And damping coefficient of G(s) is

$sRC = \ s\sqrt{LC}\ \frac{RC}{\sqrt{LC}} = X\ \frac{R}{Z_0}$, $(Z_0 = \sqrt{\frac{L}{C}}\ Z_0$ is the characteristics impedance of the filter)

Now writing $G(s)$ in terms of X

$$G(s) = \frac{1}{1 + aX + bX^2}$$

And open loop transfer function in terms of x is

$$F_o = R(s).G(s) = \frac{1 + cX}{cX}\ \frac{1}{1 + aX + bX^2} = \frac{Z}{N}$$

With the help of F_o, the closed loop transfer function is

$$F_w = \frac{Z}{N+Z} = \frac{1+cX}{1+2cX+acX^2+cX^3} = \frac{1+cX}{1+cX+(cX+acX^2+cX^3)}$$

where the denominator of F_w is of third order. It is known that the transfer function has no zeros, so the denominator should have the same pole in order to simplify term (1+cX) from the denominator and numerator of the fraction. Thus, the final simplified closed loop transfer function is

$$F_W{}' = \frac{(1+cX)}{(1+cX)(1+AX+X^2)} = \frac{1}{1+AX+X^2}.$$

By comparing coefficients of denominator of $F_w \; and \; F_W{}'$

$$(1+cX)(1+AX+X^2) = 1+cX+AX+cAX^2+X^2+cX^3$$
$$= 1+X(c+A)+X^2(cA+1)+cX^3 \triangleq 1+2cX+acX^2+cX^3$$

We realize that.

$for\ X$: $\quad 2c = c + A \Rightarrow \quad c = A$

$for\ X^2$: $\quad cA + 1 = ac \Rightarrow \quad a = A + \frac{1}{c} = A + \frac{1}{A}$

Base on the Table 4.1 for Butterworth 2nd order filter: $A = \sqrt{2}$ we can find a, c and R.

$$a = A + \frac{1}{A} = \sqrt{2} + \frac{1}{\sqrt{2}} = 2.1213$$

$$a = \frac{R}{Z_0} = 2.1213 \Rightarrow R = a * Z_0 = 2.1213 * 20\Omega = 42.43 \frac{V}{A}$$

In order to determine the coefficient of the PI controller:

$$sT = cX = cs\sqrt{LC} = \sqrt{2} * 20\mu s = 28.28\mu s$$

So the transfer function of PI controller will be: $R(s) = \frac{1+cX}{cX} = \frac{1+28.28\mu s.S}{28.28\mu s.S}$.

As all the coefficients are known now so schematic of the designed close loop control system of Class D amplifier with second order Butterworth filter is given as:

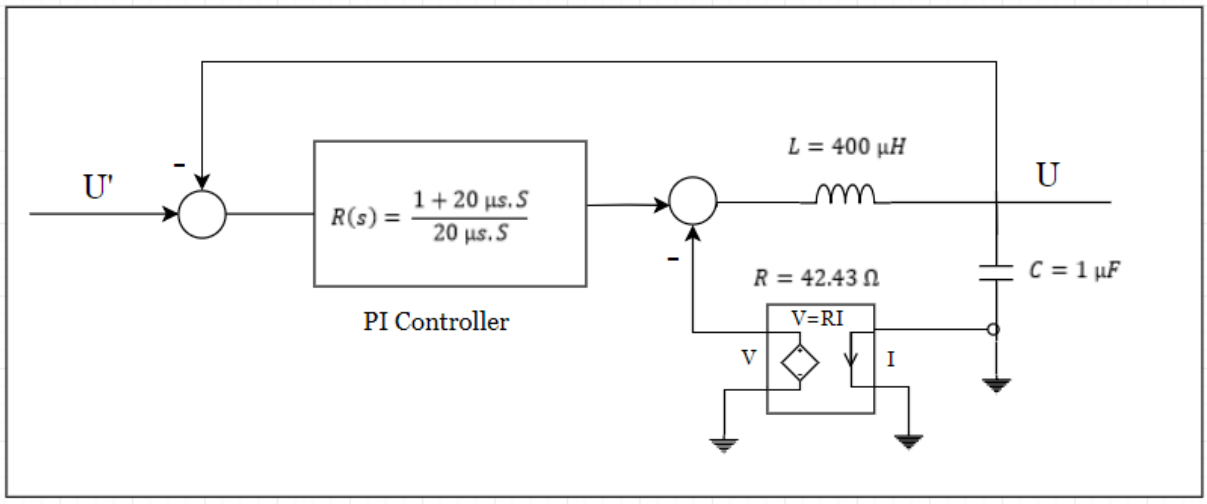

Figure 4.4 Designed control system with 2nd order low pass Butterworth filter.

4.1. Class D amplifier with fourth Order Butterworth filter

We mentioned that the complexity of a filter is usually defined by the filter order or the number of reactive components, which include the capacitors as well as the inductors in its design. A fourth order filter can be designed using the same steps as a second order; the passive components just need to be rearranged.

The closed loop system design using a Butterworth filter of the 4th order is given in Fig 4.6.

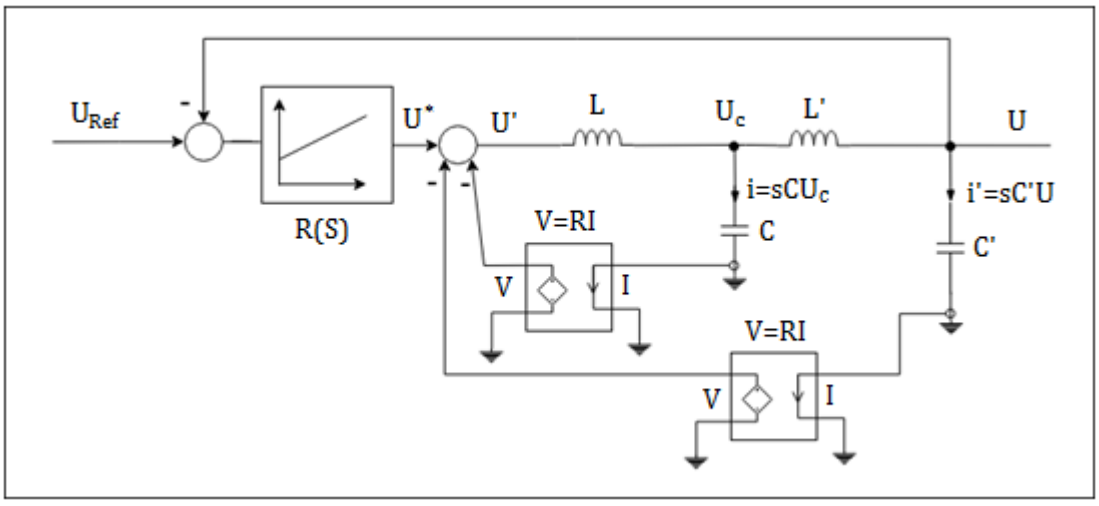

Figure 4.5 Basic schematic of Class D amplifier with fourth order low pass Butterworth filter.

As it is a higher order circuit, the double combination of passive components is used here in the design. By using control theory, we are going to find the closed loop transfer function with a low pass Butterworth filter and by using coefficients of the fourth order Butterworth filter (Table 4.1). The final aim of the mathematical calculation below is to find a relationship between U and U'.

First we need to determine flowing currents through capacitors. So in s domain

$$i' = sC'U \text{ is the current of C'}$$

Therefore, voltage of C will be

$$U_c = U + sL'(sC'U) = U + s^2L'C'U = U(1 + s^2L'C'),$$

Now using U_c flowing current through C is

$$i = sCU_c = sCU\ (1 + s^2L'C'),$$

So current of inductor L is

$$\begin{aligned} i_L = i + i' &= sC'U + sCU(1 + s^2L'C') = U(sC' + sC + s^3CL'C') \\ &= U\big(sC' + sC\ (1 + s^2L'C')\big) \end{aligned}$$

With the help of i_L, U^* can be easily found

$$\begin{aligned} U^* = U_c + sLi_L &= U\ (1 + s^2L'C') + sL\ \big(sC' + sC\ (1 + s^2L'C')\big)U \\ &= U(1 + s^2(L'C' + LC' + LC) + s^4LCL'C') \end{aligned}$$

It's clear that U^* can be found using active damping factors:

$$U^* = U' - sUR'C' - sURC\ (1 + s^2L'C')$$

So

$$U' = U^* + sUR'C' + sURC\ (1 + s^2L'C') = U^* + sU(RC + R'C') + s^3URCL'C'$$

Now relationship between U and U' or input- output relation is given by

$$U' = U\ (1 + s^2L'C' + s^2LC' + s^2LC + s^4LCL'C' + sR'C' + sRC + s^3RCL'C')$$

$$U' = U\ (1 + s(R'C' + RC) + s^2(L'C' + LC' + LC) + s^3\ RCL'C' + s^4LCL'C')$$

$$\frac{U'}{U} = 1 + s(R'C' + RC) + s^2(L'C' + LC' + LC) + s^3\ RCL'C' + s^4LCL'C'$$

And transfer function is the ratio of output to input therefore

$$G(s) = \frac{U}{U'} = \frac{1}{1 + s(R'C' + RC) + s^2(L'C' + LC' + LC) + s^3\ RCL'C' + s^4LCL'C'}$$

The denominator of the transfer function has four poles, so now we want to find the coefficients using Table 4.1 for the Butterworth fourth order.

$$G(s) = \frac{U}{U'} = \frac{1}{1 + aX + bX^2 + cX^3 + X^4}$$

Equating coefficients of both equations give

$$a = R'C' + RC, \qquad b = L'C' + LC' + LC, \qquad c = LCL'C'$$

Now we need an open loop and a closed loop transfer function for our designed system. In this case we have to consider the PI controller in our calculations:

$$PI - Controller \rightarrow R(s) = \frac{1 + sT}{sT} = \frac{1 + dX}{dX}$$

So the open loop transfer function is

$$F_o(s) = R(s) * G(s) = \frac{1 + dX}{dX} \frac{1}{1 + aX + bX^2 + cX^3 + X^4}$$

And the close loop transfer function, considering feedback is

$$F_c(s) = \frac{1 + dX}{1 + dX + dX(1 + aX + bX^2 + cX^3 + X^4)}$$

$$F_c(s) = \frac{1 + dX}{1 + 2dX + adX^2 + bdX^3 + cdX^4 + dX^5}$$

Like the Butterworth second order, the transfer function has a zero and a denominator of the $F_c(s)$ is fifth order. So the term (1+dX) should be simplified from the denominator and numerator of the fraction. Thus, the final simplified closed loop transfer function is

$$F_c(s) = \frac{1 + dX}{(1 + dX)(1 + AX + BX^2 + AX^3 + X^4)} = \frac{1}{(1 + AX + BX^2 + AX^3 + X^4)}$$

By comparing denominator s of $F_c(s)$

$$1 + 2dX + adX^2 + bdX^3 + cdX^4 + dX^5 = (1 + dX)(1 + AX + BX^2 + AX^3 + X^4)$$

$$= 1 + (A + d)X + (B + dA)X^2 + (A + Bd)X^3 + (Ad + 1)X^4 + dX^5$$

Again by equating coefficients

$$A + d = 2d \Rightarrow A = d$$

$$B + dA = ad \Rightarrow a = \frac{B}{A} + A$$

$$A + Bd = bd \Rightarrow b = B + 1$$

$$Ad + 1 = cd \Rightarrow c = A + \frac{1}{A}$$

In Butterworth 4th order filter:

$$F_w(s) = \frac{1}{1 + 2.613X + 3.414X^2 + 2.613X^3 + X^4}$$

It means $A = 2.613,\ B = 3.141$, so

$$d = 2.613, \qquad a = \frac{3.141}{2.613} + 2.613 = 3.815, \qquad b = 1 + 3.141 = 4.141,$$
$$c = 2{,}613 + \frac{1}{2.613} = 2.995$$

Now we can parameterize capacitors and inductors.

$$LC = 400\mu\mu,\ \ L'C' = 166\mu\mu$$

And

$$X^4 = LCL'C's^4 \ \Rightarrow\ X = 16\mu s$$

We know that $a = RC + R'C'$, so

$$aX = s(RC + R'C') \Rightarrow 3.815 * 16\mu s = s(RC + R'C')$$

$$RC + R'C' = 61.24\mu s$$

And we know that $b = L'C' + LC' + LC\ and\ c = LCL'C'$, we also use C=1$\mu F$ and L=400μH in our parameterization so

$$4.141X^2 = s^2(L'C' + LC' + LC)$$

$$4.141 * 258\mu\mu * s^2 = s^2(L'C' + LC' + LC)$$

$$1066.7\mu\mu = L'C' + LC' + LC \Rightarrow\ \ LC' = 500.7\mu\mu$$

$$C' = \frac{500.7\mu\mu}{400\mu} = 1.25\ \mu F\ \Rightarrow\ L' = \frac{166\mu\mu}{1.25\mu} = 132.6\mu H$$

Now all the reactive components are known.

$$L = 400\mu H, \qquad C = 1\mu F, \qquad L' = 133\mu H, \qquad C' = 1.25\mu F$$

Let's find the active damping factors

$$cX^3 = s^3\ RCL'C'\ \Rightarrow\ 2.995 * (16\mu)^3 *\ s^3 =\ s^3\ RCL'C'$$

$$2.995 * (16\mu)^3 =\ R * 1\mu F * 166\mu\mu \Rightarrow R = 74.6\Omega$$

$$RC + R'C' = 61.24\mu\ \Rightarrow R' = \frac{61.23\mu - 74.6\mu}{1.25\mu F} = -10.7\Omega$$

And finally PI controller will be

$$d = 2.613\ \Rightarrow dX = 2.613 * 16.05\mu s * s$$

$$dX = 42\mu s$$

Hence the transfer function for PI controller is

$$R(s) = \frac{1 + 42\mu s.S}{42\mu s.S}$$

Final schematic is given as

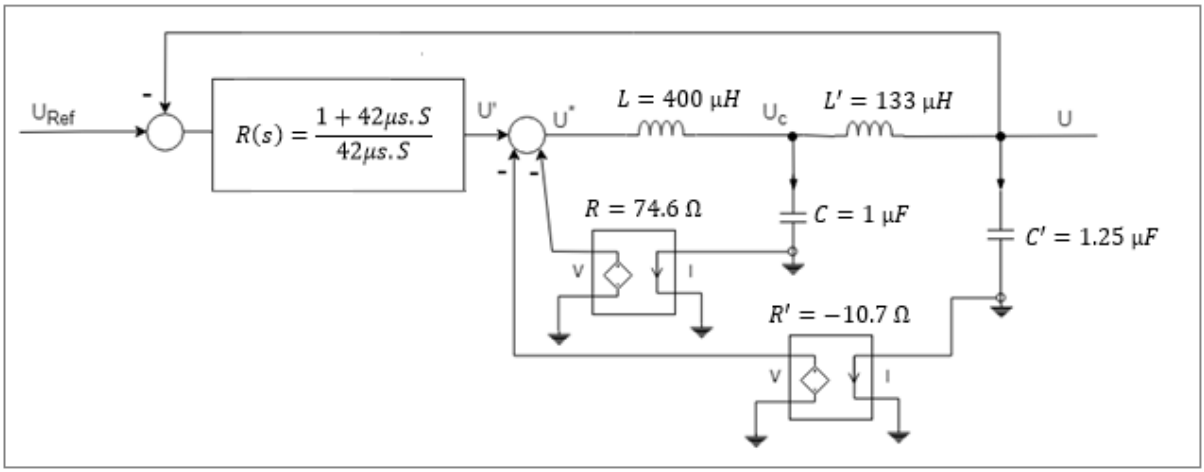

Figure 4.6 Final schematic of Class D amplifier with fourth order low pass Butterworth filter.

4.2. Class D amplifier with two second order Butterworth filters in series

Schematic of the two second order LPF is like the fourth order LPF, but in calculation and parameterization of the elements of the circuit, we consider the two second order LPF as two separate blocks.

The schematic for the two second order low pass Butterworth filters in a series combination is given as

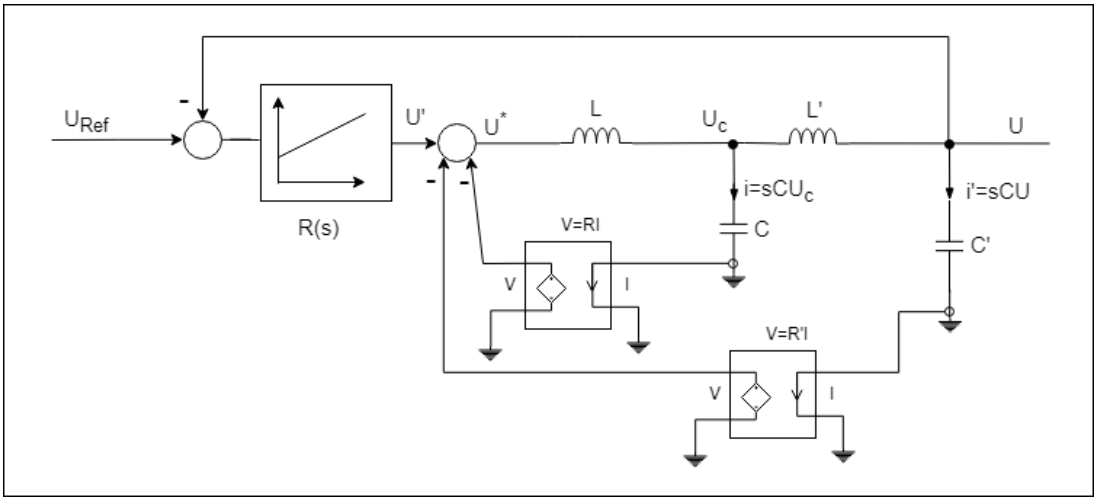

Figure 4.7 Class D amplifier with two 2nd order LP Butterworth filters in series.

Again by using control theory, the transfer function can be found easily. Based on Table 4.1, for the second order low pass Butterworth filter B=2 and its transfer function will be

$$\frac{1}{1+\sqrt{2}x+x^2}$$

Since two second order LPFs have been used in this design, we can multiply their transfer function to find G(s).

$$\frac{1}{1+\sqrt{2}x+x^2} * \frac{1}{1+\sqrt{2}x+x^2} = \frac{1}{1+2\sqrt{2}x+4x^2+2\sqrt{2}x^3+x^4}$$

$$G(s) = \frac{1}{1+2\sqrt{2}x+4x^2+2\sqrt{2}x^3+x^4}$$

Consider the PI controller, the open loop transfer function is

$$F_0 = G(s) * R(s) = \frac{1+dx}{dx}\frac{1}{1+ax+bx^2+cx^3+x^4}$$

And close loop transfer function considering feedback is

$$F_c(s) = \frac{1+dx}{(1+dx)+dx(1+ax+bx^2+cx^3+x^4)}$$
$$= \frac{1+dx}{1+2dx+adx^2+bdx^3+cdx^4+dx^5}$$

Like the previous designs, the transfer function has a zero and a denominator of the Fc is fifth order. So the term (1+dX) should be simplified from the denominator and numerator of the fraction. Thus, the final simplified closed loop transfer function is

$$F_c(s) = \frac{(1+dx)}{(1+dx)(1+Ax+Bx^2+Ax^3+x^4)}$$

By comparing denominator s of $F_c(s)$

$$1+2dx+adx^2+bdx^3+cdx^4+dx^5 = (1+dx)+(1+Ax+Bx^2+Ax^3+x^4)$$

$$= 1+(d+A)x+(Ad+B)x^2+(Bd+A)x^3+(Ad+1)x^4+dx^5$$

Again by equating coefficients

$$2d = d+A \rightarrow A = d$$

$$Ad+B = ad \rightarrow a = A+\frac{B}{A}$$

$$Bd+A = bd \rightarrow b = B+1$$

$$Ad+1 = cd \rightarrow c = A+\frac{1}{A}$$

From G(s) we know that $A = 2\sqrt{2}$ & $B = 4$, Therefore

$$a = 3\sqrt{2} = 4.243, \qquad b = 5, \qquad c = 3.182, \qquad d = 2\sqrt{2} = 2.828$$

For two second order Butterworth filter connected in series like fourth order low pass Butterworth filter, transfer function is

$$G(s) = \frac{U}{U'} = \frac{1}{1 + s(R'C' + RC) + s^2(L'C' + LC' + LC) + s^3\, RCL'C' + s^4 LCL'C'}$$

we have

$$U^* = U\{1 + s(R'C' + RC) + s^2(L'C' + LC' + LC) + s^3(RCL'C') + s^4(LCL'C')\}$$

By comparing with standard equation to above equation it can deduce that

$$x^4 = s^4(LCL'C') \;\&\; LC * L'C' = 166\mu\mu * 400\mu\mu \;\rightarrow x = 16.05\ \mu s$$

$$ax = s(R'C' + RC) \rightarrow 4.243 * 16.05\ \mu s = s(R'C' + RC) \rightarrow (R'C' + RC) = 68.1\mu s$$

$$bx^2 = s^2(L'C' + LC' + LC) \rightarrow 5 * (16.05\mu s)^2 = s^2(166\mu\mu + LC' + 400\mu\mu) \rightarrow LC' = 722.0125\mu\mu$$

Now if we choose

$$C = 1\mu F \;\&\; L = 400\mu H$$

Then

$$C' = 1.805\mu F \;\&\; L' = 91.965\mu H$$

$$cx^3 = s^3(RCL'C') \rightarrow 3.182 * (16.05\mu s)^3 = s^3(RCL'C') \rightarrow R = 79.25$$

As

$$(R'C' + RC) = 68.1\mu s\ so\ R' = -6.177$$

And at the end

$$dx = 2.828 * 16.05\mu s = 45.39\mu s$$

Hence the transfer function of PI-Controller is

$$R(s) = \frac{1 + 45.39\mu s.S}{45.39\mu s.S}$$

Final schematic is given as

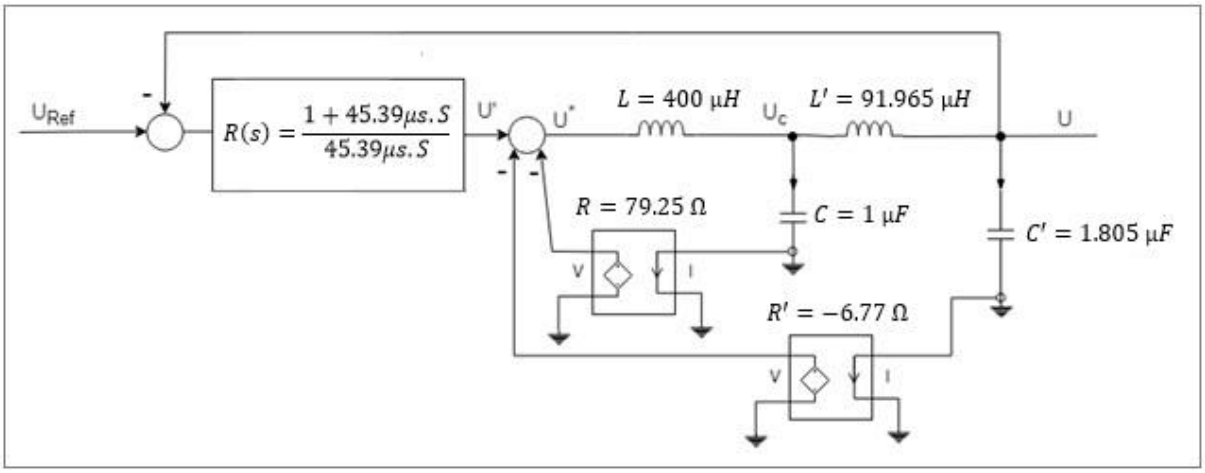

Figure 4.8 Final schematic of Class D amplifier with two 2nd order LP Butterworth filters in series.

5. Comparison of designed amplifier with linear loads

5.1. Basics

In the previous chapter three types of CDA (Class D amplifier) were designed using passive components and the Butterworth filters were named as:

- CDA with second order Butterworth filter
- CDA with fourth order Butterworth filter
- CDA with two second order Butterworth filters in series

In this chapter, we will study and compare how our designed Class D amplifiers perform in different situations. First we will test them without load and discuss the characteristics of the response, speed and stability. Then we will test them with different loads, including linear and reactance loads.

5.2. No-load analysis

Initially, no load is applied at the output of these regulators so that their response can be observed under no load condition. Input-Output characteristics of these 3 types of voltage regulators under no load condition is given as:

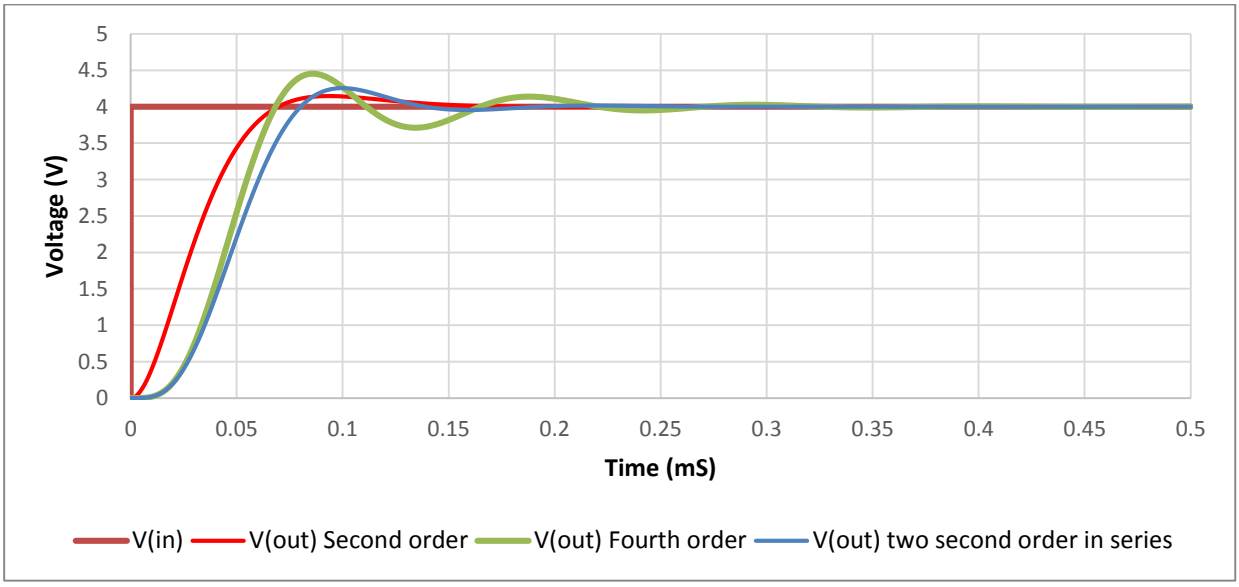

Figure 5.1 Comparison between steps responds of CDA with different LPFs.

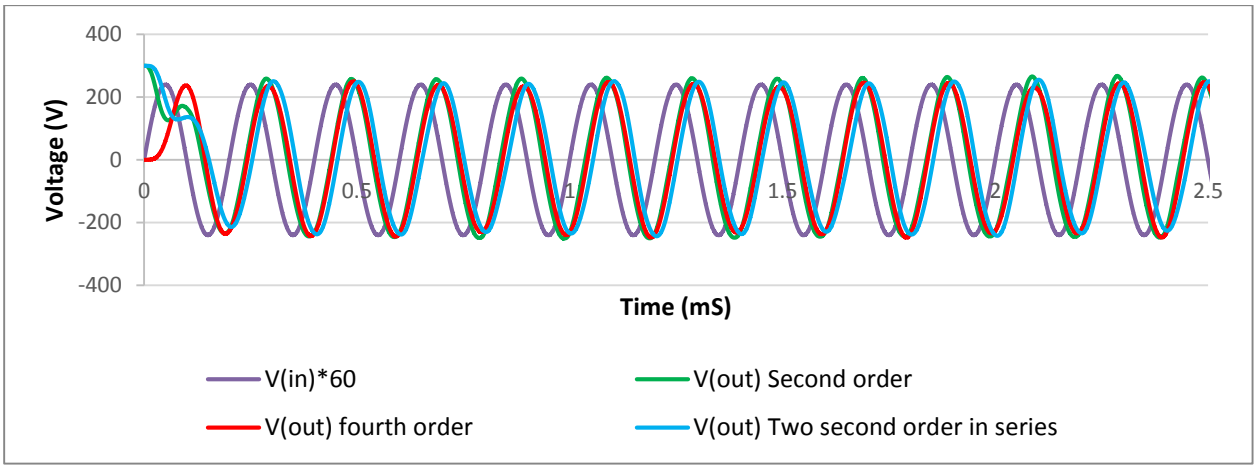

Figure 5.2 Comparison of output voltages for no-load condition and sine-response.

From the results for no-load condition (Fig 5.1) it can be deduced that CDA with second order Butterworth filter gives the best underdamped response compared to input and response of other amplifiers. In this system, output of the system overshoots from its steady state value and after reaching the peak value comes to steady state after some oscillations. Its steady state error, rise time and overshoot is smaller compared to other amplifiers. So based on the results of simulations, the best performance would be without load. One of the reasons is that it's more simple and it has less reactive components in its design.

CDA with fourth order Butterworth filter and CDA with two second order Butterworth filters can also give an underdamped response under no load condition. But CDA with a fourth order Butterworth filter has less rise time and overshoot compared to CDA with two second order Butterworth filters in series, and it also comes to a steady state earlier.

In terms of stability, it can be said that under no load condition all three types of voltage regulators are stable as error is dying with increase in time. As time approaches infinity, response of the amplifiers become stable and work under forced response.

5.3. Analysis under loaded condition

5.3.1. Characteristic Impedance of Class D amplifier

Effect of load depends on the characteristic impedance of the amplifier. Delivery of maximum power to load is basically one of the main purposes of the design of the amplifier that should be considered. In order to transfer the maximum amount of power from input to load, the load impedance should match the characteristic impedance. In case there is a mismatch between characteristic impedance and load, distortion at the output can occur and even may bring the amplifier to unstable operation. As a consequence, a part of power that is not delivered to load, can be reflected back and cause a loss in the amplifier.

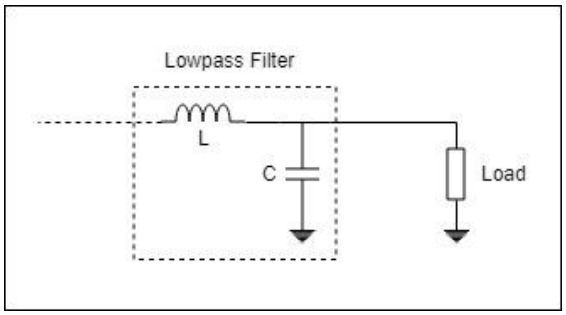

Figure 5.3 Regulator with Load.

In a such lossless network like LC filter, characteristic impedance is

$$Z_0 = \sqrt{\frac{L}{C}}.$$

Therefore, characteristic impedance of CDA with second order low pass Butterworth filter is

$$Z_L = Z_0 = \sqrt{\frac{400\mu H}{1\mu F}} = 20\Omega.$$

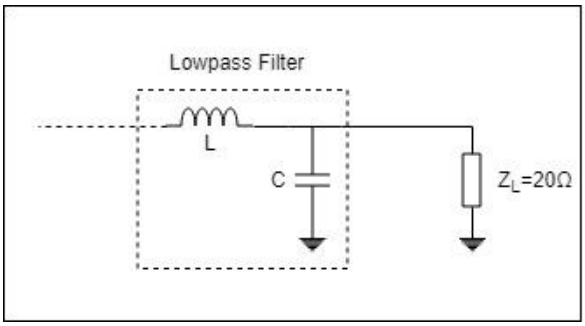

Figure 5.4 Regulator with Characteristic impedance of CDA.

5.3.2. Linear loads for CDA with second and fourth order LPF

Linear load

A linear load contains just resistors, inductors and capacitors. If a pure sinusoidal voltage is given to a linear load, a pure sinusoidal current flows to the load with the same frequency as the voltage. In inductive or capacitive loads, phase shifting between voltage and current may occur. Based on characteristic impedance of CDA and cutoff frequency, it will be possible to characterize elements of different loads such as resistive, inductive and capacitive loads.

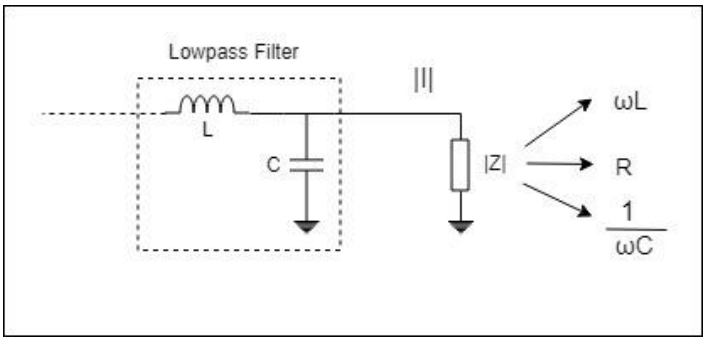

Figure 5.5 Different possible loads for CDA.

Effect of resistive loads on the CDA

Suppose that the load is pure resistive with an amount of R=ZL=20Ω. It is the simplest load for the designed systems that is independent from cutoff frequency. In this case, a comparison between the regulators can be shown as Figure below.

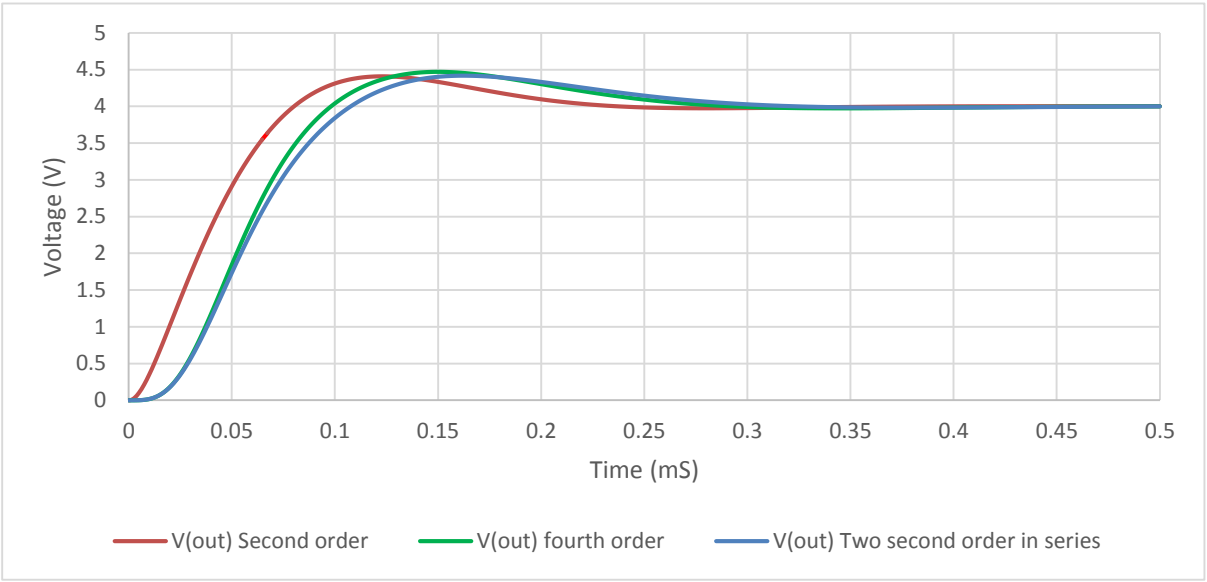

Figure 5.6 Comparison of step responses for resistive load.

Caused by the additional damping of the load all the variants show about similar step response.

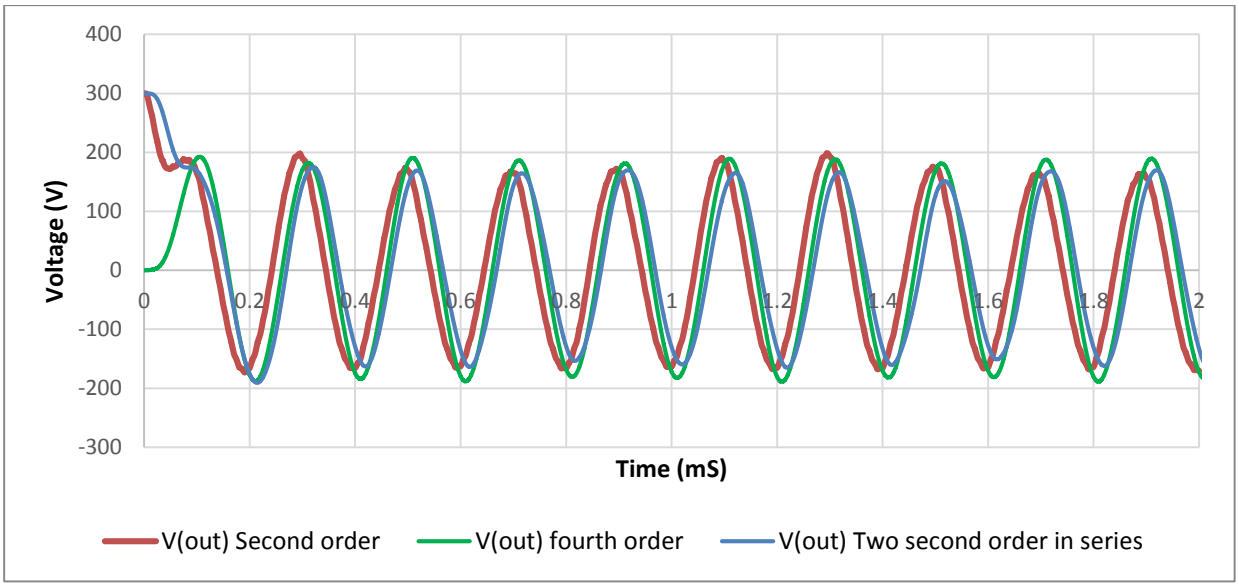

Figure 5.7 Comparison of output voltages for resistive load, sine-response.

Effect of inductive loads on the CDA

In order to show the effect of inductive loads on the CDA, a parallel RL load is used. First Inductance should be parameterized. In our calculations and design, cut-off frequency is 8kHz, so

$$\omega L = Z_L = 20\ \Omega$$

$$L = \frac{20\Omega}{2\pi.8kHz} \simeq 1mH.$$

And schematic of final circuit with a parallel RL is shown below, (Fig 5.8).

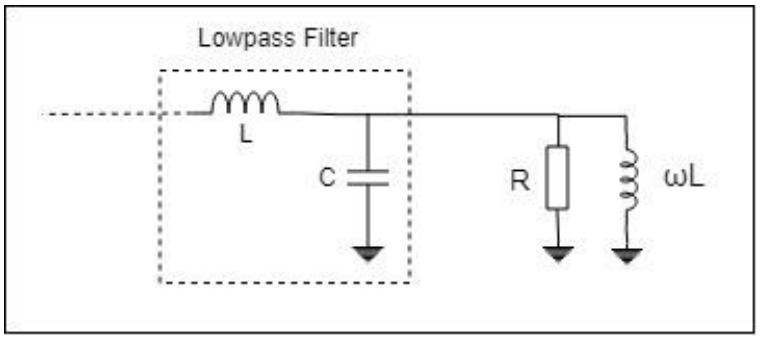

Figure 5.8 CDA with a parallel RL load.

Diagram of output voltage and step responses of designed voltage regulators under inductance load condition is given in Fig 5.9.

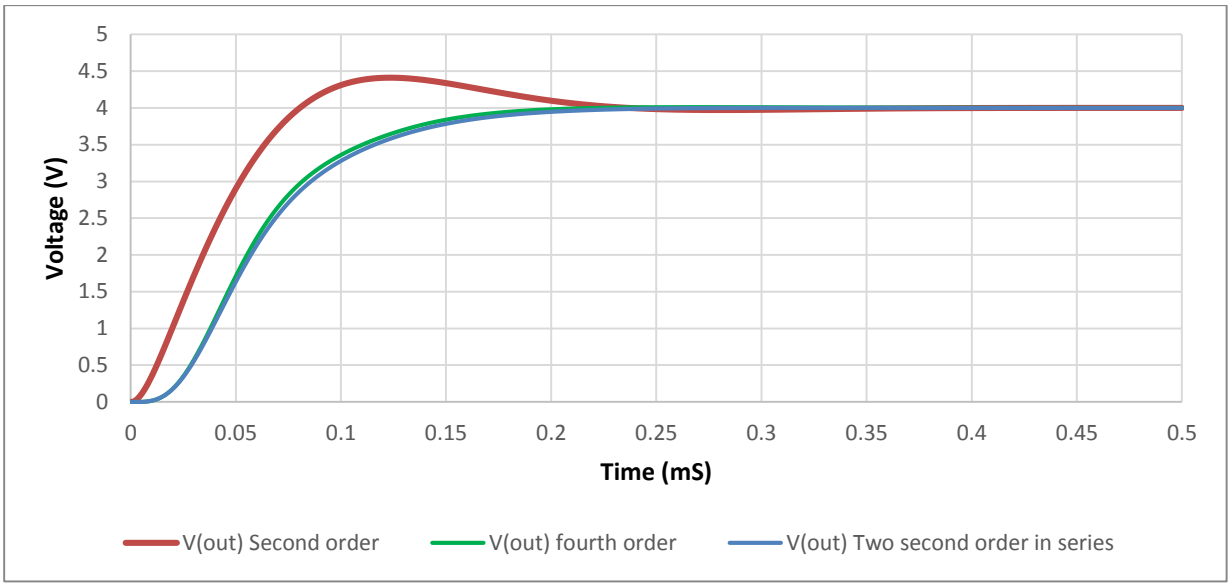

Figure 5.9 Comparison of step responses for inductive load.

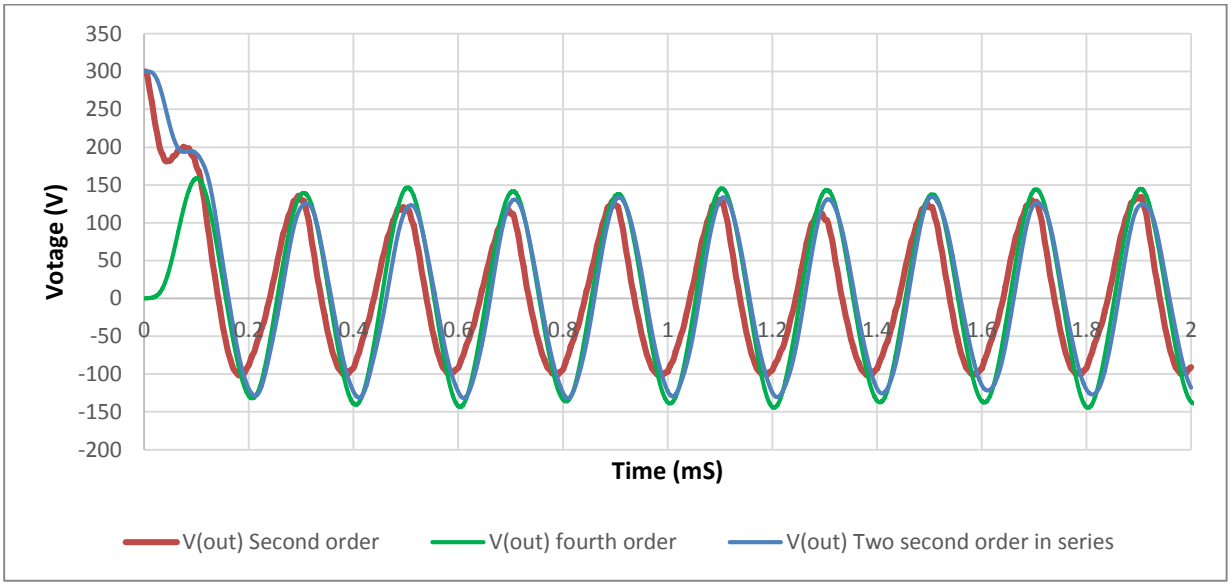

Figure 5.10 Comparison of output voltages for inductive load, sine-response.

Effect of capacitive loads on the CDA

The third solution is to study designed systems with a small capacitive load. A suitable capacitive load for this case is a parallel RC load which is dependent on cut-off frequency like RL load. If the cut-off frequency is 8kHz, the capacitor can be parameterized simply.

$$\frac{1}{\omega C} = 20\Omega$$

$$C = \frac{1}{2\pi . 8kHz . 20\Omega} \simeq 1\mu F$$

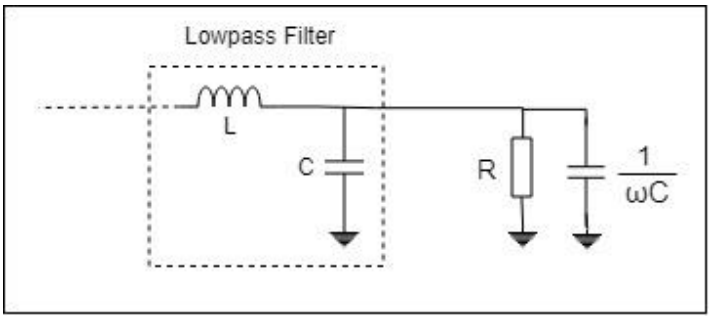

Figure 5.11 CDA with a parallel LC load.

Diagram of output voltage and step responses of designed voltage regulators under capacitance load condition is given as:

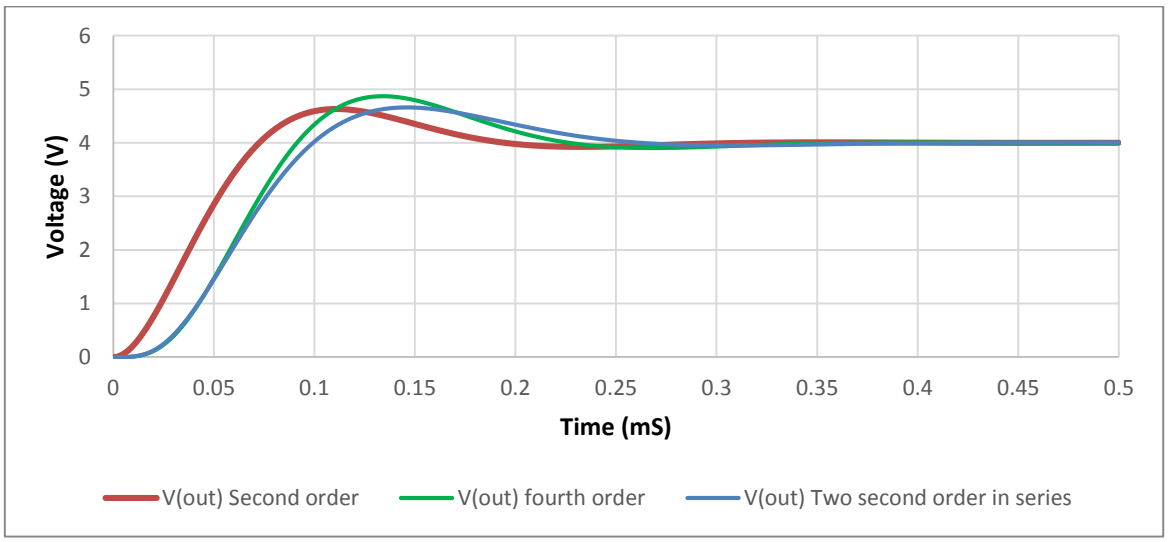

Figure 5.12 Comparison of step responses for capacitive load.

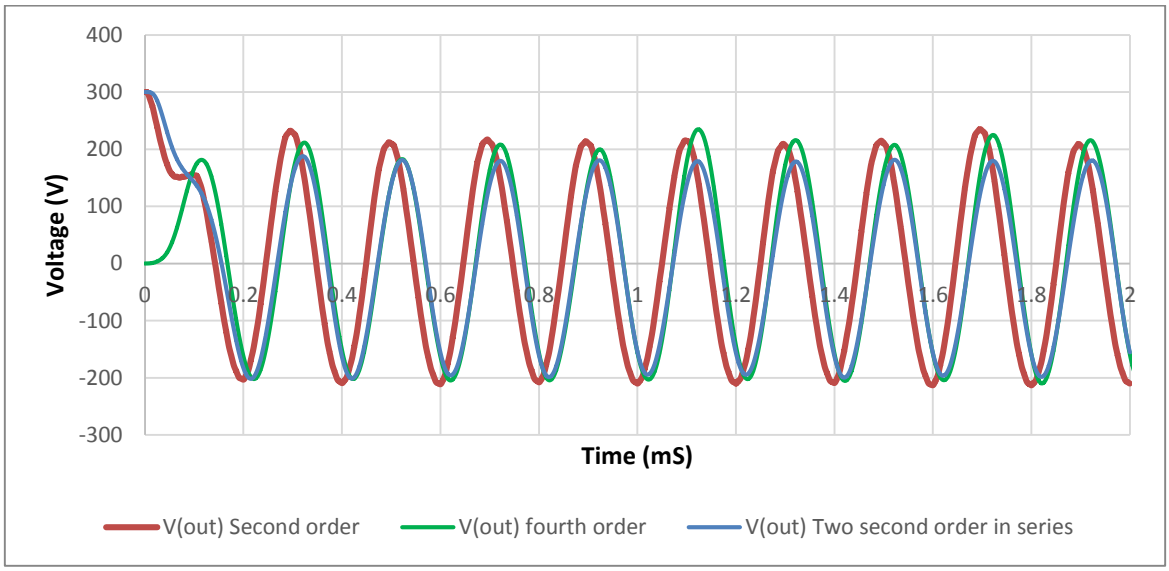

Figure 5.13 Comparison of output voltages for capacitive load, sine-response.

5.4. Discussion about result

The purposes of this investigation were to compare the time domain responses of different voltage regulators, which were designed using Butterworth filters of 2nd, 4th order and two 2nd order in series, on a known set of data. Different loads, which included resistive, inductive and capacitive loads are used to comparison.

In order to see the effects of changing the order of Butterworth filter on output, a comparison can be made with the step response, which is ideal in terms of regulators.

Thus, the second order filter case had the least time-lag while the 4th order filter cases have higher time-lag. In other words, the higher the order of system, the more time-lag the step response shows. This means one of the disadvantages of the higher order system is that the response of system will be slower. On the other hand, the fact that a higher order system can remove the snitching noise much more effectively, is a great advantage.

5.5. Conclusion

The ultimate goal of this project was to design a fully functional and stable Class D power amplifier with verification by simulation. One of the original goals of this project was to find the best option for an output filter. Another goal was to find a pure sinusoidal output voltage and a pulse response with a good rise time and without an overshoot. A test plan was also developed in order to determine if these goals and specifications were met and to determine if this project was successful.

The first step in accomplishing this project was to develop an understanding of how a power amplifier, and especially Class D amplifiers, operate. This was accomplished by researching past projects as well as commercial products. Once we had a better understanding of Class D amplifiers, we tried to understand the function of different methods of modulation like PWM. The next step was to study different output filters, in our case, low pass filters. The optimal option for our case was a Butterworth low pass filter.

After completing our research on the above topics, we decided to design the system with three types of Butterworth filters, including second order, fourth order and two second order Butterworth filters in series. A special design and calculation of the transfer function of the system was made for each of these filters. Then the elements of filter are parameterized.

After completing our design for each filter, several PSpice simulations were created. These simulations allowed for various methods and components to be tested, ultimately saving valuable time in the final design. Finally, each system in no load condition and with different load types were tested. The result was that the amplifier met most of the

specifications, therefore, this project was successful. In other word, the theory behind the design does prove that the performance and implementation is achievable.

While the accomplishments of this project are significant, there are several areas of future research that were beyond the scope of the project.

5.6. Future works

While this project was successful in designing a fully functional Class D amplifier with a Butterworth low pass filter, there are many additional areas that can be explored to complement the completed Class D amplifier. The focus of this project was to develop an amplifier to drive a 20Ω load. However, a working amplifier is a component that can be used in many different products. This section will discuss several of the ideas for future work concerning Class D audio amplifiers.

There is another new type of amplifier that is called Class T amplifier, which has a few superior performances compared to Class D amplifiers, such as better power efficiency and less distortion in the output. This would be a good research area to look into if we wanted to consider replacing the existing Class D power amplifier design.
As was previously discussed in chapter 5.2, the Class D amplifier in this thesis developed and tested just with linear loads. Thus, future work can be done with studying a Class D amplifier with nonlinear loads.
The proposed design tested the theoretical equation through the simulations, being somewhat theoretical. Therefore, the circuit design should be implemented in the layout process and validated.

Bibliography

1. Zumbahlen. H.: Linear Circuit Design Handbook, Chapter 8 analog filters, Newnes ISBN: 9780750687034, August 2011
2. Billings. K, Morey. T: Switchmode Power Supply Handbook, 3rd Edition, McGraw-Hill, ISBN: 978-0-07-163972-9, 2011
3.
4. Van Valkenburg. M. E.: Analog Filter design, Holt-Saunders International Edition, Japan, 1982
5. Tietze U, Schenk, C, Gamm, E: Halbleiter-Schaltungstechnik, Berlin, Springer, 2012
6. Wangenheim L. v, Aktive Filter und Oszillatoren, Springer-Verlag, Berlin Heidelberg, 2008
7. Cipriani E, Colantonio P, Giannini F and Giofre R: The Switched Mode Power Amplifiers, Advanced Microwave and Millimeter Wave Technologies Semiconductor Devices Circuits and Systems, Moumita Mukherjee (Ed.), ISBN: 978-953-307-031-5, InTech, 2010
   http://www.intechopen.com/books/advanced-microwave-and-millimeter-wave-technologies-semiconductordevices-circuits-and-systems/the-switched-mode-power-amplifiers
8. Billings, K, Morey, T: Switchmode Power Supply Handbook, Third Edition, ISBN: 978-0-07-163972-9, McGraw-Hill, 2011
9. Grebennikov, A, O. Sokal, N: Switchmode RF Power Amplifiers, Elsevier Inc, 2007
10. Choi D. K, High Efficiency Switched-Mode Power Amplifiers for Wireless Communications, Ph.D. Dissertation, University of California, Santa Barbara, March 2001.
11. Gaalaas, E: Class D Audio Amplifiers: What, Why, and How, Analog Dialogue 40-06, June 2006
    http://www.analog.com/en/analog-dialogue/articles/class-d-audio-amplifiers.html
12. Marshall Leach W. Jr: Introduction to Electroacoustics and Audio Amplifier Design, Second Edition, Kendall/Hunt, 2001
13. Honda, J, Adams, J: Class D Audio Amplifier Basics, Application Note AN-1071, International IOR Rectifier, 2005
    www.irf.com
14. 4. Pressman, A. I.: Switching and Linear Power Supply, Power Converter Design, Haydon, ISBN 0-8104-5847-0, 1977.
15. Dixon, L. H., Potel R.: Unitrode Switching Regulated Power Supply Design Seminar Manual, 1985.
16. Severns, R. P.: and Bloom, G E.: Modern DC-to-DC Switchmode Power Converter Circuits, Van Nostrand Reinhold, New York, ISBN 0-422-21396-4, 1985.

17. Hnatek, E. R., Design of Solid-State Power Supplies, 2d Ed., Van Nostrand Reinhold, New York, ISBN 0-442-23429-5, 1981.
18. Shepard, J. D.: Power Supplies, Restin Publishing Company, 1984. ISBN 0-8359-5568-0.
19. Chryssis, G.: High Frequency Switching Power Supplies, McGraw-Hill, New York, 1984. ISBN 0-07-010949-4.
20. Kit Sum, K.: Switchmode Power Conversion, Marcel Dekker, New York, 1984. ISBN 0-8247-7234-2
21. Class D Amplifiers: Fundamentals of Operation and Recent Developments, Application Note 3977, Maxim Integrated, 2007
22. Gondane, R.: Types of Amplifiers and their Circuits with Working. Edgefx Kits Official Blog. Retrieved 1 November 2017 http://www.edgefxkits.com/blog/different-types-of-amplifiers/
23. Zumbahlen, H: Basic linear design, 2007, Analog Devices, Inc. ISBN 0-916550-28-1