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DISSERTATION

Active Circuit Extension for Unity Power Factor Operation of Passive Three-Phase Diode Rectifiers

ausgeführt zum Zwecke der Erlangung des akademischen Grades
eines Doktors der technischen Wissenschaften

unter der Leitung von
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Kurzfassung

Die Relevanz von Systemen zur netzfreundlichen Umformung von Dreiphasen-Wechselstrom in Gleichstrom ist gerade in der jüngsten Zeit durch die Thematik der erneuerbaren Energieerzeugung/ Smart-Grids/ Elektromobilität bzw. der Zunahme der Leistungselektronik bei der Erzeugung und Distribution elektrischer Energie stark angestiegen. Ganz allgemein basiert heute ein hoher Anteil der in Industrie und allgemeinen Anwendungen eingesetzten elektrischen Prozesse (z.B. Antriebe, Stromversorgung für Internet- und Telekommunikationseinrichtungen, Ladestationen in der Elektromobilität, Solarbatteriespeicher etc.) auf der Verwendung von Gleichstrom und bedarf deshalb moderner Gleichrichtersysteme mit niedrigen Netzstromharmonischen. Eine besondere Rolle spielen solche Systeme auch im Bereich der eMobility zur Implementierung von Schnelllade-Station für Fahrzeuge. Hier werden zum Beispiel im Moment immer noch sehr häufig passive Strukturen wie zum Beispiel der dreiphasige Diodengleichrichter mit DC-seitigem LC Ausgangsfilter implementiert (einfach, robust, billig). Allerdings entstehen durch die Verwendung solcher passiver Topologien wesentliche Nachteile bei der maximalen Auslastung und Stabilität des Netzes aufgrund enormer Belastung durch Blindströme (erhöhter Blindleistungsbedarf etc.). Typische Auslegungen solcher passiver Gleichrichter sehen THD_i (Total Harmonic Distortion) Werte von $\approx 48\,\%$ vor, was zu einer deutlich erhöhten Belastung des Netzes durch Netzharmonische führt und daher einen unerwünscht hohen Anteil an Blindleistung im Netz bedeutet.

Zur Vermeidung dieser eben genannten Nachteile besteht die Möglichkeit der Verwendung aktiver Gleichrichterkonzepte. Diese bisher bekannten Strukturen lassen aber die Adaption/Erweiterung eines bereits bestehenden passiven Gleichrichters nicht zu und fordern daher ein komplett neues Design. Die bereits implementierte passive Struktur kann somit nicht mehr wiederverwendet werden. Besonders vorteilhaft erscheint also, eine Ergänzung einer bereits bestehenden passiven Gleichrichterstufe mittels aktiver Konverter-Injektionsstufe. Diese optionale aktive Leistungsstufe garantiert sinusförmige Eingangsströme, einen $THD_i < 5\,\%$, einen Leistungsfaktor von nahezu "1" (reine Wirkleistungsübertragung - "Unity Powerfactor") und erlaubt es, bereits bestehende passive dreiphasige Gleichrichter zu einer Struktur mit niedrigen Netzstromharmonischen "upzugraden".

Die Dissertation beschäftigt sich daher mit der Analyse von aktiven Dreiphasengleichrichtern auf dem Prinzip der gleichspannungsseitigen "Third Harmonic Current Injection". Attraktive Konzepte werden daher diskutierte und analytisch behandelt. Die zwei vielversprechendsten Topologien werden leistungselektronisch aus-

gelegt, hardwaretechnisch implementiert und getestet. Die realisierten forschungsdienlichen Prototypen sollen die eingangs erwähnten Vorteile einer solchen Struktur zum Erhalt eines leistungselektronischen Gesamtkonzepts, das es ermöglicht, Vorteile beider leistungselektronischer Topologien (passiver Gleichrichter und aktive Injektionsstufe) auszuschöpfen ("Unity Powerfactor", $THD_i < 5\,\%$, keine hochfrequente Common-Mode Spannung am Gleichrichterausgang, ...), bestätigen.
Im Rahmen der Dissertation wurden nicht nur neue leistungselektronische Schaltungskonzepte und Regelkonzepte vorgeschlagen und implementiert, analysiert und funktionsfähige Prototypen entwickelt, sondern wirtschaftlich relevante Anforderungen berücksichtigt wie zum Beispiel optimierte Baugrösse für die benötigte Eingangsfilterstruktur unter Ausnützung von Netzimpedanzanteilen, Eingangsstromverzerrungsfreie und dynamische Spannungsregelung inkl. aktiver Spannungsbalancierkonzepte, Vergleich der errechneten Bauteilauslegungen mittels thermischer Messungen, optimierte Baugrösse des Gesamtkonzepts und Injektionsdrosseln durch optimierte Kühlkonzepte und gekoppelte Spulenimplementierung, Berücksichtigung möglicher Netzspannungsunsymmetrien und Störungen.

Abstract

Especially in recent times, modern societies are more and more longing for substitution of pollutive technology (coal-fired power plants, gasoline driven automotives,...) by eco-sensitive solutions. This balancing act, between fulfilling the need of current energy expenditure and expected increasing power demand should be satisfied and optimized via solutions as e.g. renewable energy, the smart grid vision, e-mobility etc. Therefore, a grid harmonic free three-phase AC- to DC-conversion is highly requested as a lot of today's technologies are assuming a DC power supply and/or at least a common DC-link (battery systems, motor applications, miscellaneous DC power supplies,...). Three-phase rectifier applications also play an important role for e.g. e-mobility fast charging stations. Such stations often use passive three-phase rectifiers with adjacent passive filter (low-cost, simple, robust). Due to a high reactive power demand and higher order harmonics (which mainly result in a low-cost and volume optimized design of the passive topology – $\mathrm{THD_i} \approx 48\,\%$) such systems tend to impair the stability and highly pollute the grid.

These mentioned drawbacks can be overcome or at least reduced if active rectifier solutions are implemented. Commonly known active rectifiers, however, do not allow the extension of such a passive system, and thus in general assume the substitution of the total AC- to DC-conversion path. The already manufactured passive system is hence not reusable. An optional upgrade which allows both, either a high efficiency or unity power factor and low harmonic input currents (on demand) therefore might appear as attractive solution for such already existing passive systems.

From this reason, this PhD-thesis is engaged in such an enhancement for passive three-phase rectifiers with DC-side smoothing inductor by employing the third harmonic injection concept. Several promising solutions are discussed and analytically described. The most promising solutions are selected for laboratory prototype verification. The implemented circuits should confirm the proposed advantages of such a hybrid system (improved efficiency, low harmonic input currents $\mathrm{THD_i} < 5\,\%$, unity power factor, no high frequency common-mode voltage with switching frequency at the output of the total system).

Within the scope of this PhD-thesis, not only novel hybrid power electronics concepts have been proposed, but also dedicated control concepts have been analyzed and verified. Furthermore, the laboratory prototypes also considered different important practical aspects as e.g. optimized input filter design due to exploitation of mains impedance, design of a highly dynamic control (voltage/current), ac-

tive voltage balancing, comparison of designed and implemented components via thermal measurements, optimized injection inductors, advanced cooling concepts (optimized air cooled) and unbalanced mains input voltages.

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Chapter 1

Introduction

Active three-phase rectifier circuits have gained more and more importance during the last decade as a consequence of raising penetration of power electronic controlled loads connected to the supply grid and, in general, due to ongoing increasing consumption of electric energy. Especially applications like e.g. switch-mode power supplies, AC drives, smart grid systems, electromobility units etc. where increasingly (i) low harmonic input/line currents ($\mathrm{THD_i} < 5$), (ii) high power factor ($\lambda > 0.99$) and (iii) high efficiency ($\eta > 95\,\%$) are mandatory (cf., [1]), rely on effective AC/DC-conversion provided by active rectifiers.

Power electronics converters per definition form an interconnection unit between an electric power source like a single- or three-phase public supply grid and a power consumption unit (e.g. an induction motor). In practical systems however usually a number of different intermediate steps are required to guarantee the aimed frequency and power conversion (50 Hz/60 Hz AC to DC and/or DC to variable frequency AC). The total power transfer solution in general furthermore should satisfy the requirements of a small in volume, reliable, highly efficient and low-cost unit. A typical state-of-the-art mains input to machine output concept for a variable speed drive system, e.g., is illustrated in in **Fig. 1.1(a)** and **Fig. 1.1(b)**. The energy conversion mentioned could e.g. be facilitated by using a matrix converter topology (cf., **Fig. 1.1(a)**), which allows a direct energy transfer between the 50/60 Hz three-phase power supply grid to the generated variable frequency three-phase AC power system feeding the drive. Due to some drawbacks – not mentioned here for the sake of brevity – matrix converter topologies however did not achieve wide spread in industrial converter systems up to now.

A much more commonly used solution today is depicted in **Fig. 1.1(b)** where a rectifier (AC to DC conversion) feeds a short-time energy storage system actually decoupling the line power electronics from the load side power electronics. Therefore, in general a specific storage device is required (constant voltage: DC link capacitor, constant current: DC-link inductor) which opens also the opportunity for smoothing of power flow fluctuations as will appear in case of a non-symmetric

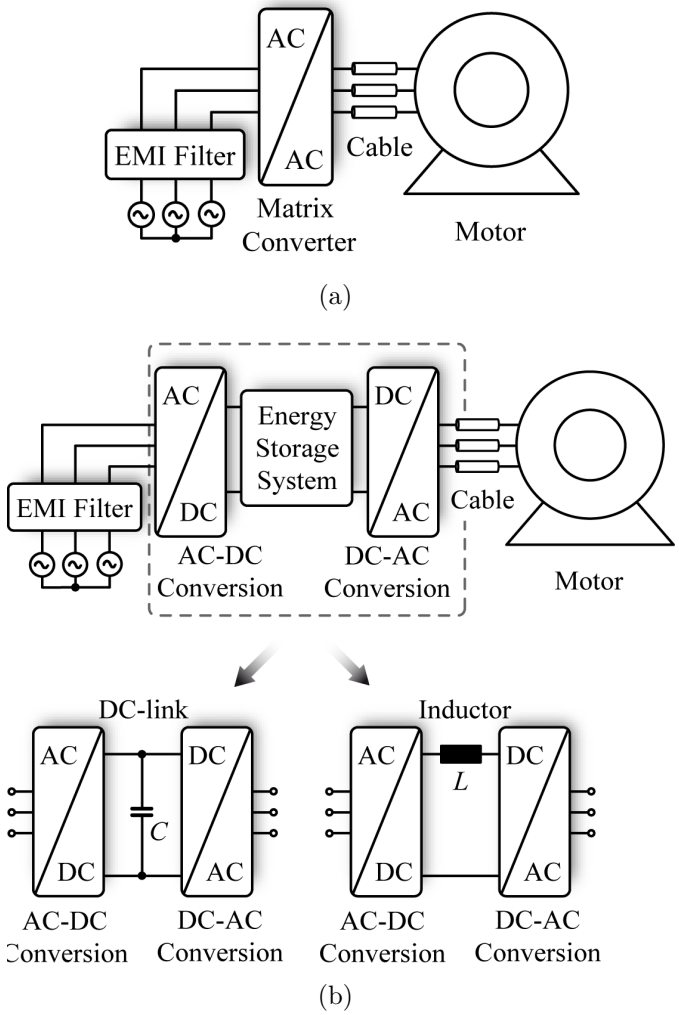

Fig. 1.1: Typical power transfer from mains input to power consuming device (output).

three-phase AC supply. The passive energy storage is followed by an DC to AC converter topology. The dedicated *rectifier* can be implemented as either passive or active topology. If a specific output voltage level and/or sinusoidal input currents are required, *active* PFC rectifiers offer an attractive solution. Depending on the required DC output characteristics (and appropriate power level), the PFC unit can be implemented as either two-level, three-level or multilevel concept.
However, in many applications a rectifier device is preferred which mainly is characterized by low cost and high efficiency. A passive three-phase diode bridge B6 rectifier (with LC output filter or AC-side inductors) seems to be attractive for that purpose if the non-controlled output voltage level of the B6 rectifier satisfies the needs of the fed motor inverter. An additional DC-DC (either step up or down) converter could be applied between rectifier and inverter if the output voltage of the B6 bridge has to be customized.
A further application, where such passive rectifier circuits are also required are e.g. (fast) charging stations for electrical vehicles (EVs). Three different concepts for such a (fast) charging station (with either a high frequency transformer

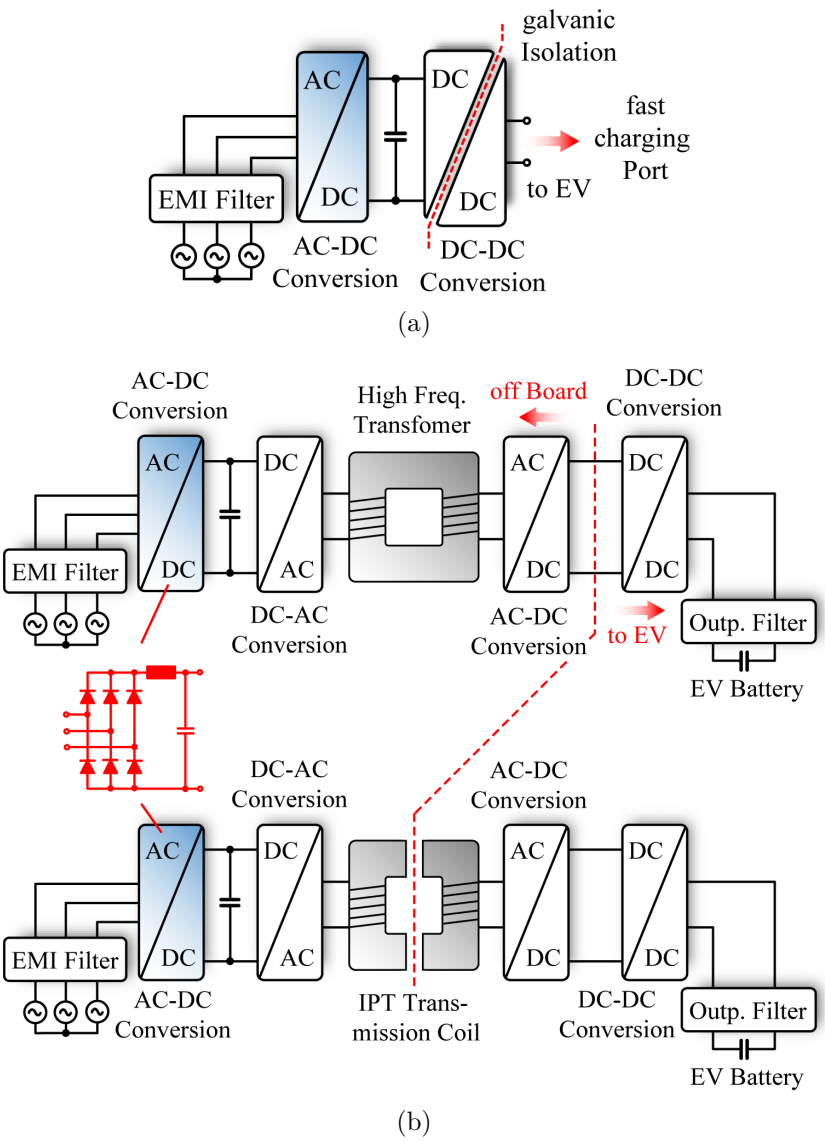

Fig. 1.2: Three different concepts for a (fast) charging station for electrical vehicles with (a) AC to DC rectification followed by an isolated DC/DC converter, (b) a high frequency transformer or (c) wireless charging as presented in [2].

(**Fig. 1.2(a)** and **Fig. 1.2(b)**) or wireless charging (cf., **Fig. 1.2(b)**)) are presented and discussed in [2]. Also a bipolar DC bus solution as proposed in [3] may serve as feasible concept, where multiple vehicles can be charged at the same time. As mentioned in [2] a passive rectifier could become handy if a cost efficient DC power supply is required (additional DC-DC converter with galvanic isolation required).

A severe drawback of such passive rectifier systems is, that they highly pollute the AC mains by harmonic currents resulting in a poor $\mathrm{THD_i}$ of typically 48 % or higher (at nominal load, for a minimized output inductor) and even higher values for partial and light load operation (up to $\mathrm{THD_i} > 100\,\%$). Additionally, also the power factor of the system is limited to $0.9 \ldots 0.95$ and deteriorates to $\lambda \approx 0.7$ for partial/light loads. Nonetheless, passive rectifiers (cf. **Fig. 1.3(a)**) today are

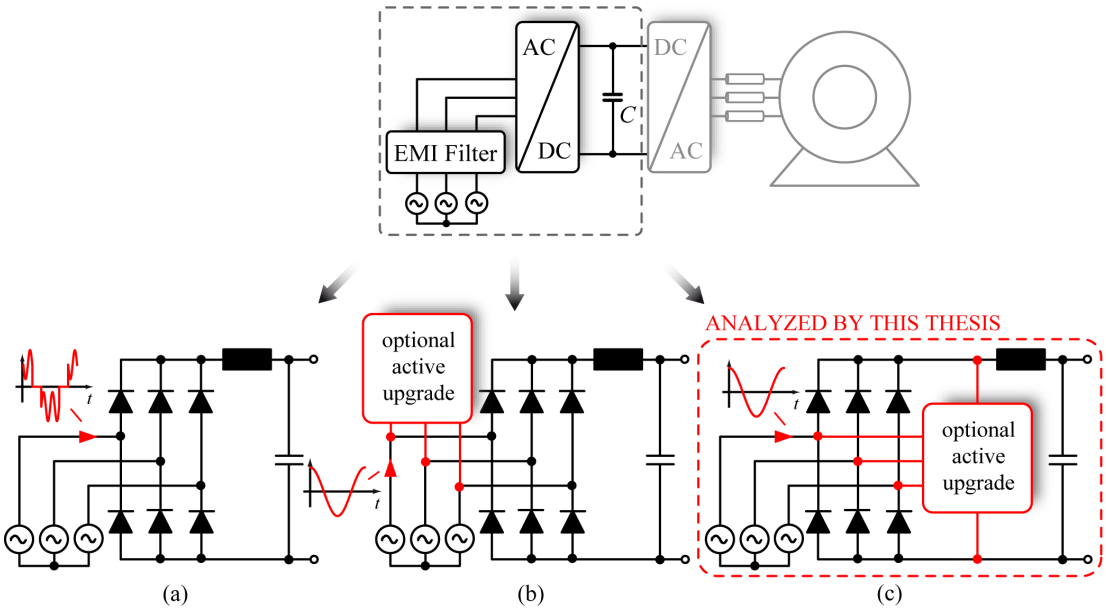

Fig. 1.3: AC to DC rectification by (a) a passive three-phase rectifier (b) an active (shunt) power filter or (c) a power circuit based on the third harmonic injection principle.

widely used in industry due to simplicity, robustness and low-cost manufacturing effort for a large number of different applications. Each application furthermore has to fulfill a set of constraints, especially limits concerning input current harmonics. These limits are predefined according to several specific standards defined by international standard committees. Nearly every year, new standards are resolved or existing standards for several applications are further restricted. Thus, it may apply that specific applications (whose input stage was formerly implemented by a passive three-phase rectifier) now have to guarantee sinusoidal input currents and unity power factor. The simplest solution in such a case would be a replacement of the passive B6 rectifier by an active PFC unit. For small quantities it could be much more cost effective if the passive system is upgraded by an optional active enhancement as illustrated in **Fig. 1.3(b)** or **Fig. 1.3(c)**. The active upgrade can be connected at either three (cf., **Fig. 1.3(b)**) or five (shown in **Fig. 1.3(c)**) points of the passive system which are generally accessible. As both filtering concepts are suitable for harmonic current suppression of passive three-phase rectifiers, differences are addressed and discussed in [4]. It is stated that despite increased complexity, a concept as depicted in **Fig. 1.3(c)** is characterized by advantages as

i. reduced switch stress

ii. increased compensation capacity and

iii. improved compensation performance.

Furthermore, AC-side (shunt) active filters (cf., **Fig. 1.3(b)**) highly may affect the mains input impedance, which may inflict additional issues on paralleled (passive and/or active) rectifier circuits and is hence not further discussed in this work. Alternatively, a DC-side located optional active upgrade as illustrated in **Fig. 1.3(c)**

for a passive rectifier is discussed, analyzed and implemented within this thesis. Different topologies are proposed and examined which are all based on the third harmonic injection concept and able to fulfill the requirements of a low harmonic input stage with unity power factor.
The implemented laboratory prototypes are designed for 10 kW nominal load and may serve as scaled demonstrator for higher power ratings (e.g. 200 kW).

1.1 Relevant Harmonic Standards

In order to reduce electric pollution in mains grids and guarantee undistorted operation of industrial environment, common EMI standards posing fundamental constraints for power electronic applications for low-voltage systems have been defined. The EC 61000-3-2 specifies limits for harmonic currents produced by equipment connected to public low-voltage systems with input currents smaller 16 A ([5] and [6]). In [7] an overview and comparison of grid harmonics and conducted EMI standards considering IEEE 519, IEEE 1547 [8] (both $\geq$ 100 Hz), the technical guideline "Generating Plants Connected to the Medium-Voltage Network" from BDEW (100 Hz-9 kHz) and CISPR 11 (150 kHz – 30 MHz) is provided. As for frequencies between 9 kHz and 150 kHz no applicable standards exist up to now (however are in discussion at present) additional limits are furthermore proposed in [8].

1.2 New Contributions of this Work

Main objective of this thesis is to develop and investigate optional active circuits for upgrading passive B6 rectifiers to achieve low harmonic input currents. The upgraded system has to fulfill constraints as $\mathrm{THD_i} < 5\,\%$ and $\lambda > 0.99$ under nominal load operation. New contributions of these work are:

- Derivation of several new topologies (based on the third harmonic injection concept).
- Investigation and analysis of appropriate circuits.
- Deduction of dedicated control concepts for such hybrid power devices.
- Development of design guidelines and dimensioning relations.
- Implementation of the two most promising topologies as 10 kW laboratory prototype.
- Determination of appearing side effects during circuit operation (unbalanced voltages, light/no-load condition, etc.)
- Comparison to a standard active PFC rectifier.

1.3 Research Objectives and Outline

The thesis is organized and structured in the following. In **chapter 2** the state of the art of active and hybrid rectifier topologies are listed and discussed to give an overview of already existing technology (which also includes already available rectifiers based on the used third harmonic principle forming the point of origin of the performed research. **Chapter 3** analyzes the behaviour of passive three-phase rectifiers (B6 diode bridge with LC output filter) in detail which is inevitable to understand fundamental effects during operation for the further discussions of an active third harmonic injection upgrade for such a passive system. Most important attributes are therefore derived analytically and compared to experimental results.
In **chapter 4** the third harmonic injection principle is introduced (basic principle – current injection device (CID)/current shaping network (CSN), fundamental waveforms, etc.). Furthermore, a brief discussion about different basic solutions for a proper input filter design are mentioned. Finally, design, control and implementation of the current injection device is analyzed.
Subsequently, seven topology variants for current shaping implementation are developed and examined in **chapter 5** (full-bridge, series connected half-bridges, a "Flying" Converter Cell (FCC), three different 3-level converter stages (neutral point clamped (NPC), T-type, flying capacitor), multi cell topologies). Besides design guidelines and simulation results, also topology properties and differences and fundamental issues are highlighted and illustrated for each concept.
The two most promising solutions (FCC – IGBT 10 kW/10 kHz , series connected half-bridges – SiC 10 kW/72 kHz) have been implemented as a laboratory prototype and are described in detail in **chapter 6** and **chapter 7**. Measurement results (nominal load, partial load, light load and load steps (full load steps etc.)) and rectifier characteristics (power factor, total harmonic distortion of input currents, efficiency) are discussed. Furthermore, important parasitic effects (as e.g. reduced efficiency for light loads, unbalanced mains voltages, etc.) are addressed, briefly discussed and demonstrated by measurement results.
Chapter 8 finally gives a comparative evaluation of a selected unidirectional three-phase PFC rectifier (VIENNA rectifier) to one specific implementation of a rectifier system based on the proposed upgrade (THI) principle (two half-bridge branches). Besides benefits and drawbacks also numerous performance indices are chosen, in order to allow a more reliable characterization and benchmarking of the THI system. It has to be noted that a comparison of these two active rectifiers should not identify a favorite concept (which is indeed not possible due to completely different attributes of both rectifiers). The investigation should merely reveal benefits and drawbacks of the THI circuit by comparing the upgraded B6 rectifier to an already industrial established standard PFC concept.

1.4 Awards

- ECCE 2014 Oral Session Student Winner (Presented Paper: DC Voltage Balancing of Flying Converter Cell)
- ECCE 2014 Best Paper Award 3rd Place (Paper: DC Voltage Balancing of Flying Converter Cell)
- APEC 2016 Outstanding Presentation Award (Presented Paper: Hardware Implementation and Characterization of SiC-Based Hybrid Three-Phase Rectifier Employing Third Harmonic Injection)

1.5 Conference and Journal Publications

1. M. Makoschitz, M. Hartmann, H. Ertl, and R. Fehringer, "Analysis of a New Third Harmonic Injection Active Rectifier Topology Based on an NPC Three-Level Converter Cell," in Proceedings of the Conference for Power Electronics, Intelligent Motion, Power Quality (PCIM), Nuernberg, Germany, May 14-16 2013, pp. 1133-1140.
2. M. Hartmann, R. Fehringer, M. Makoschitz and H. Ertl, "Design and Experimental Verification of a Third Harmonic Injection Rectifier Circuit Using a Flying Converter Cell," in Proceedings of the Twenty-Ninth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), 2014, pp. 920-927.
3. M. Makoschitz, M. Hartmann, H. Ertl, and R. Fehringer, "DC Voltage Balancing of Flying Converter Cell," in Proceedings of the Energy Conversion Congress and Exposition (ECCE), 2014, pp. 4071-4078.
4. M. Makoschitz, M. Hartmann and H. Ertl, "Analysis of a Three-Phase Flying Converter Cell Rectifier Operating in Light/No-Load Condition," in Proceedings of the Thirtieth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), 2015, pp. 92-100.
5. M. Makoschitz, M. Hartmann and H. Ertl, "Topology Survey of DC-Side Enhanced Passive Rectifier Circuits for Low-Harmonic Input Currents and Improved Power Factor," in Proceedings of the Conference for Power Electronics, Intelligent Motion, Power Quality (PCIM), Nuernberg, Germany, 2015, pp. 1-8.
6. M. Makoschitz, H. Ertl and M. Hartmann, "A Passive Three-Phase Rectifier Enhanced by a DC-side High Switching Frequency Add-On SiC-Converter Stage for Unity Power Factor Applications," in Proceedings of the Seventeenth European Conference on Power Electronics and Applications (EPE/ ECCE Europe), Geneva, Switzerland, 2015, pp. 1-8.
7. M. Makoschitz, M. Hartmann and H. Ertl, "Effects of Unbalanced Mains Voltage Conditions on Three-Phase Hybrid Rectifiers Employing Third Harmonic Injection," in Proceedings of the 2015 International Symposium on Smart Elec-

tric Distribution Systems and Technologies (EDST), Vienna, Austria, 2015, pp. 417-424.

8. M. Makoschitz, M. Hartmann and H. Ertl, "Total harmonic distortion reduction add-on unit for three-phase diode rectifiers," IET Journals & Magazines, Electronics Letters, Vol. 52, Issue 4, 2016, pp. 306-308.
9. M. Makoschitz, M. Hartmann and H. Ertl, "Hardware Implementation and Characterization of SiC-Based Hybrid Three-Phase Rectifier Employing Third Harmonic Injection," in Proceedings of the Thirty-First Annual IEEE Applied Power Electronics Conference and Exposition (APEC), 2016, pp. 1-8.
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Chapter 2

Active Three-Phase Rectifier Topologies

This chapter gives a brief summary of state-of-the-art three-phase AC to DC topologies for applications which require high power factor and low input current distortions in order to define a point of origin of the performed research and developments.

2.1 Overview of AC-DC Converters

AC-DC converter circuits can be classified into systems with bidirectional and systems with unidirectional power flow capability (**Fig. 2.1** and **Fig. 2.2**, respectively).

Bidirectional three-phase rectifier systems are mainly based on *two* (six-switch rectifier, z-source converter) or *three-level* (neutral point clamped (NPC), flying capacitor (FC), T-type, active NPC (ANPC), bridge leg inductor (BLI)) topologies where all switching components are implemented as active switches to provide four-quadrant operation. The specific type of switch which is going to be used depends on the according application (e.g. MOSFETs for low power applications, IGBTs at higher voltage and power level). These types of rectifiers frequently are denominated as active front end (AFE). In general they are used as an option for motor inverters (pump/turbine combinations, low harmonic drives, downhill conveyors, winches, escalators, crane applications,...). These active circuits are mandatory if energy has to be transferred from the output of the system to the AC grid which is i.e. the case for regenerative breaking. Typical characteristics of these systems are:

- Power factor of $\cos(\Phi) = 1$ independent of the load and the energy direction.

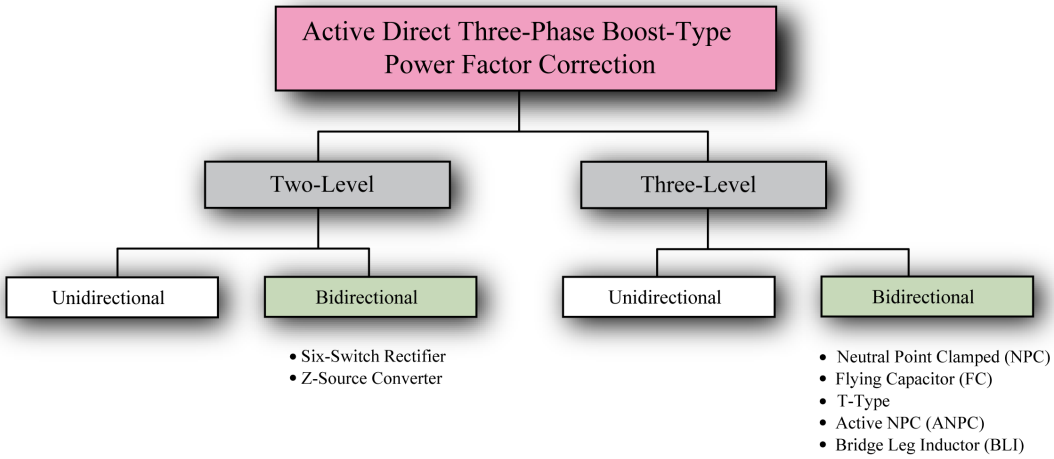


Fig. 2.1: Active direct three-phase boost type power factor correction implemented as two- or three-level converter topology which allows (depending on design considerations) either bidirectional or unidirectional powerflow as discussed in [9].

- THD_i of less than 5 %.
- High robustness against grid voltage notches and surges.
- Operation for a wide frequency range.

If some switches are replaced by diodes we obtain systems with **unidirectional** AC to DC power flow. Unidirectional three-phase rectifiers may be implemented as *passive*, *hybrid* or *active systems* and in general consist of at least one passive diode bridge with additional passive or active components to achieve sinusoidal input currents or at least input currents with reduced harmonic distortions.
A purely *passive system* consists of e.g. a single diode bridge with AC-side or DC-side smoothing inductor or is designed as multipulse rectifier system with pulse multiplication. In general, this pulse multiplication is implemented as series connection of passive diode bridges or alternatively by multiple diode bridges connected in parallel via an interphase transformer on the DC-side of the system (IPT). These topologies require specific transformers (Yy (star-star), Yd (star-delta) or Dy (delta-star) transformer connection) which provides phase shifted AC voltages and isolation.
Active systems for unidirectional power flow can be grouped into direct three-phase systems and into phase modular systems (e.g. y-rectifier, delta rectifier,...). Direct three-phase systems can be furthermore separated into current source and voltage source types which include either boost or buck-type topologies in each of the three mains phases power flow path. Depending on their operating mode these concepts can moreover be divided into continuous/discontinuous current mode (CCM/DCM) and continuous/discontinuous voltage mode (CVM/DVM) operation. In especial the VIENNA rectifier by now is a very popular unidirectional active three-phase rectifier. It is characterized by boost type operation and impressed AC currents.

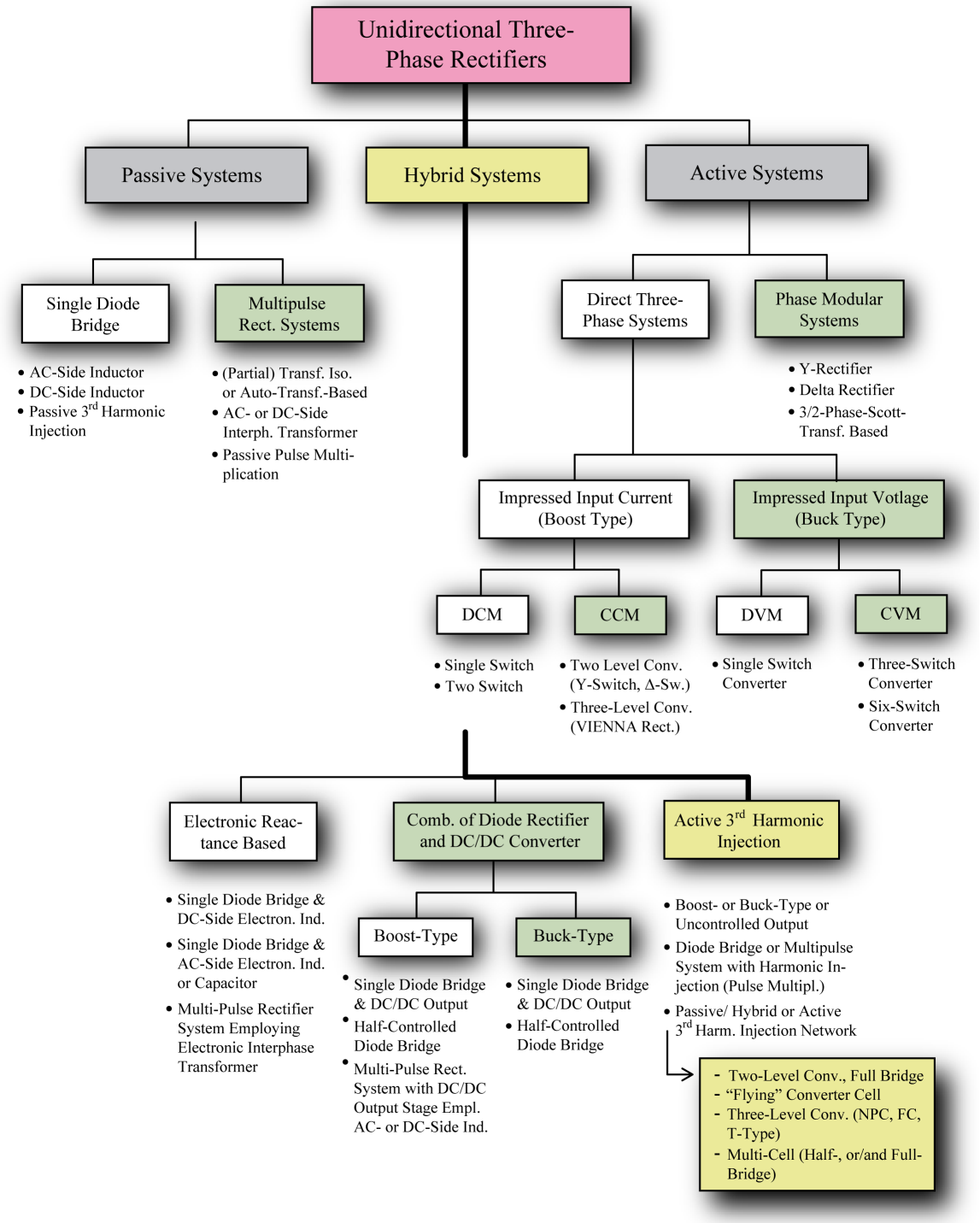


Fig. 2.2: Overview of unidirectional three-phase rectifier systems implemented as either passive, hybrid or active systems as discussed in [9].

Hybrid systems merge passive rectifiers with active converter topologies. Consequently, this subcategory is only able to process active power in one direction (unidirectional power flow). Electronic reactance based hybrid rectifiers, e.g. consist of a single B6 diode bridge and DC-side electronically emulated inductor. This "electronic inductor" is in general realized by a simple full-bridge stage where two

switches can be replaced by diodes due to the unidirectional power flow of the total system (according to [10]).
The last class of hybrid rectifiers are systems employing third harmonic injection which are the circuits of major concern in this thesis (marked yellow in **Fig. 2.2**). The third harmonic injection network can be implemented either as active, passive or hybrid device and would be also applicable for multipulse rectifiers. The third harmonic injection network generally consists of a current shaping and a current injection stage. Both circuits can be implemented as either passive or active setup. Converter systems based on this technique can hence be classified into (i) active current injection - active current shaping (SWISS rectifier, "Flying" Converter Cell (FCC) active rectifier, multi-cell implementation, two/three-level arrangements) (ii) passive current injection - active current shaping (MINESOTA rectifier) (iii) active current injection - passive current shaping and (iv) passive current injection - passive current shaping.
Besides [9], also [11–19] give a comprehensive overview of bidirectional and unidirectional power factor correction systems either implemented as AC- or DC-side active or passive filter topologies. In the following, the mentioned concepts are discussed on a more detailed basis.

2.2 Active Three-Phase Rectifier Circuits

Fig. 2.3 depicts three active three-phase power factor correction (PFC) rectifier topologies allowing bidirectional power flow implemented as bidirectional two-level topology (**Fig. 2.3(a)**, (VSI)), neutral point clamped (NPC) three-level stage (**Fig. 2.3(b)**) or T-type three-level bridge leg (**Fig. 2.3(c)**).
Fig. 2.3(a), also known as six-switch active rectifier, is a state-of-the-art circuit for low-voltage grid applications. Due to simplicity, robustness and low complexity it is widely used in industry and active components are available as combined power modules from many manufacturers. This topology however results in large volume of input inductors and shows limited maximum switching frequency (mentioned in [9]). In terms where efficiency gains more and more importance (due to increasing energy costs and environmental issues) three-level topologies (i.e. **Fig. 2.3(b)** or **Fig. 2.3(c)**) have been analyzed and described as interesting alternative solution (cf., [20]). Positive perspectives of three-level topologies are e.g. reduced volume of passive components for the EMI input filter to attenuate the switching current harmonics, resulting also in reduced filter losses and volume. Furthermore, lower switching losses and reduced voltage stress of switching devices (e.g. $V_\mathrm{o}/2$ for horizontal switches of T-type leg) have to be highlighted. Additionally, proper efficiency can be achieved for increased switching frequencies which makes them attractive for compact rectifier units. Furthermore, also common-mode voltage v_CM and differential-mode ripple $v_{\mathrm{DM}\sim}$ of three-level converters is much lower in comparison to two-level stages. Due to the increased number of switches, losses are distributed over many semiconductor dies. This leads to a comparatively

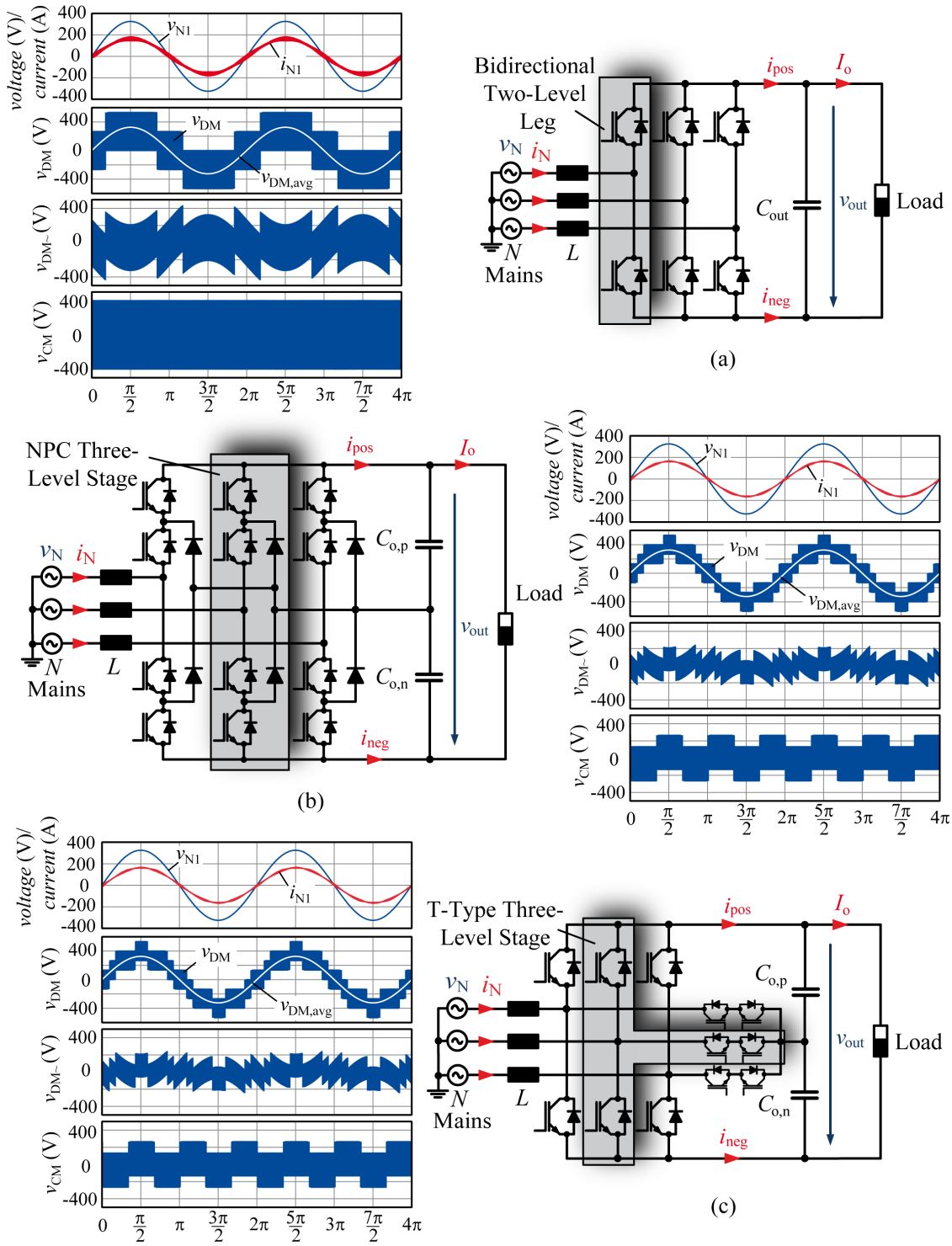


Fig. 2.3: Active direct three-phase boost-type power factor correction (PFC) rectifier systems implemented as (a) bidirectional two-level converter topology, (b) neutral point clamped (NPC) three-level stage and (c) T-type three-level bridge leg for 200 µH AC-side inductance (L), 400 V_{LL} mains voltages, 10 kHz switching frequency f_s and 73 kW output power P_o. Furthermore shown: Input voltage v_{N1}, AC-side mains current i_{N1}, differential-mode voltage v_{DM} and common-mode voltage v_{CM} of both, two-level and three-level systems (simulation results).

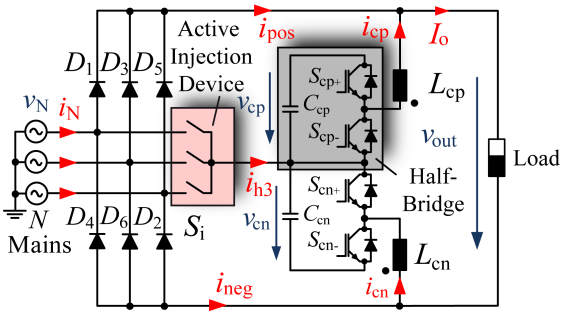


Fig. 2.4: Three-phase rectifier circuits employing third harmonic injection with implemented active current shaping and active current injection network.

small increase of the semiconductors junction temperature. An optimized chip area concept (smaller chip area results in reduced cost) for active semiconductor components can be considered which is proposed and discussed in [21]. It has to be kept in mind that these three-level concepts result in increased number of active components (more gate drive units), potential higher conduction losses, DC-link voltage balancing effort, increased control complexity and possibly enhanced cost compared to a two-level implementation.

2.3 Hybrid Rectifiers Employing Third Harmonic Injection

In this section, various types of hybrid rectifiers which are based on the third harmonic injection (THI) principle are listed. The most relevant and important variants are highlighted and briefly discussed. All of these hybrid versions rely on a standard passive three-phase diode bridge connected to the AC mains. The THI principle is based on a current injection network and a current shaping network. Both networks can be implemented as passive or active electronic stage. Therefore, converter systems based on this technique can be classified into

i. Active Current Injection - Active Current Shaping
ii. Passive Current Injection - Active Current Shaping
iii. Active Current Injection - Passive Current Shaping
iv. Passive Current Injection - Passive Current Shaping

2.3.1 Active Current Injection - Active Current Shaping

Besides [22–25] (which are going to be extensively discussed later in this thesis), numerous versions of DC-side active power filters with active current shaping and active current injection have been proposed up to now. Three popular variants given in **Fig. 2.4**-**Fig. 2.6**. References [4, 26–30] are analysing filter topology of **Fig. 2.4** consisting of two half-bridge branches which inject such amount of

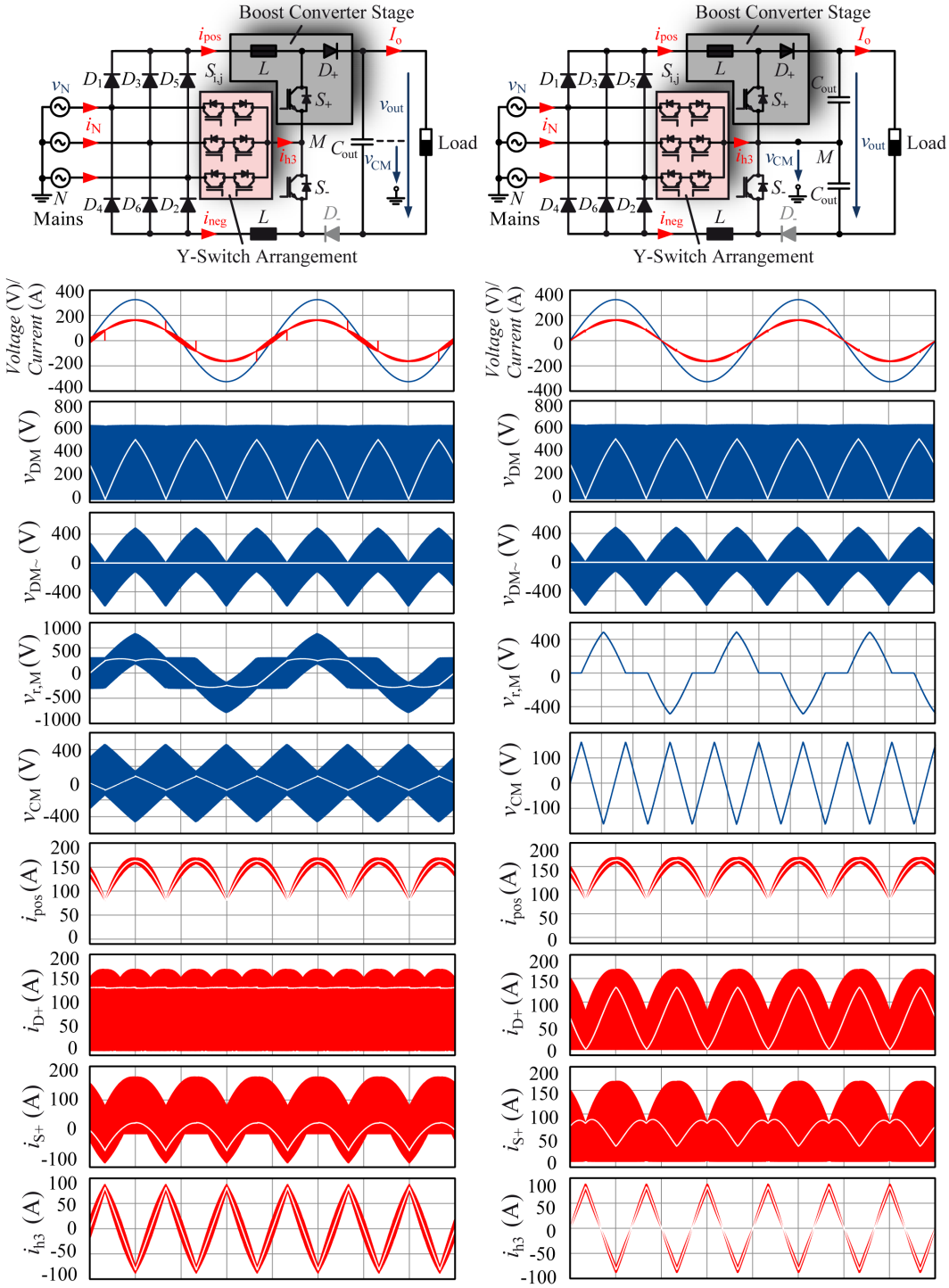


Fig. 2.5: Third harmonic injection including boost converter topology directly located at output of B6 rectifier bridge.

current into the positive and negative busbar 120°-sinusoidal wave shapes appear at the DC output of the B6 bridge and inject the resulting third harmonic current via S_i into that mains phase which does not conduct current in this 120° interval. This circuit expects an inductive load at the output, otherwise sinusoidal mains input currents cannot be guaranteed for low switching frequency operation. The

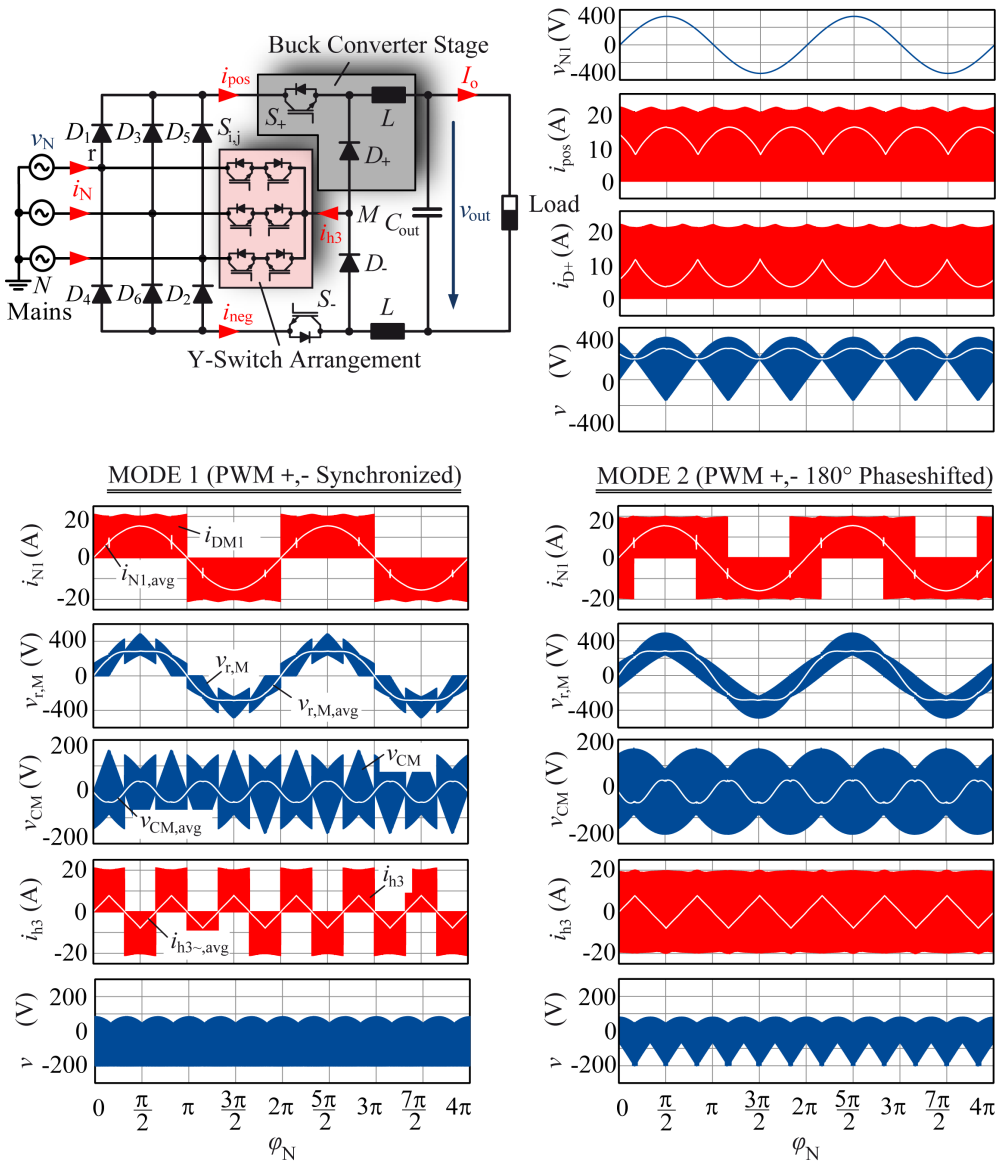


Fig. 2.6: SWISS-rectifier (third harmonic injection plus buck converter circuit).

output voltage v_{out} is still showing high 6th-harmonic spectral components due to the missing output filter. If a LC-tank would be applied at the DC-side of the circuit (to guarantee constant output voltage V_{o} and current I_{o}) low switching frequencies $< 20\,\text{kHz}$ are not applicable which mainly results due to the additional low frequency voltage component appearing due to the non-ideal injection inductance L_{cp}, L_{cn}.

Fig. 2.5 illustrates a different concept (cf., [31]) where a boost converter is located directly at the output of the B6 rectifier, similar to the Minnesota rectifier (with passive current injection circuit). Due to boost converter operation principle (pulsed output currents) output capacitor C_{o} is required now in order to absorb AC current ripple components. As illustrated in **Fig. 2.5** there are two variants of implementation for this circuit. Firstly, both boost converter topologies are directly connected to the midpoint of the third harmonic injection network

(**Fig. 2.5(left)**) and secondly, the output capacitors are realized as center tapped arrangement where the midpoint M of the split DC-link is directly connected to both switch-mode stages (**Fig. 2.5(right)**). As indicated with this midpoint connection the circuit shows a common mode output voltage v_{CM} without any switching frequency components. This topology however requires a rather high constant output voltage level of

$$V_{\mathrm{out,min}} = V_{\mathrm{o,p}} + V_{\mathrm{o,n}} > 3\hat{V}_{\mathrm{N}} = 975\,\mathrm{V}. \tag{2.1}$$

As each capacitor stage is connected to one switch-mode stage, both capacitor output partial voltages can be controlled separately. The midpoint M is fixed according to the AC-side mains voltage situation and hence not controllable. The minimum output voltage of topology **Fig. 2.5(left)** is defined by the maximum rectifier output voltage ($\max(v_{\mathrm{rec}})$), due to the missing connection of the AC input to the DC output side and hence results in a much lower voltage of

$$V_{\mathrm{out,min}} > \sqrt{3}\hat{V}_{\mathrm{N}} = 563\,\mathrm{V}. \tag{2.2}$$

Fig. 2.6 shows one of the most popular DC-side filter concepts, namely the SWISS rectifier ([32, 33]). The SWISS-rectifier consists of two buck converter topologies and bidirectional switches (active current injection network). This low frequency switching semiconductors (gated at twice of the mains frequency) cyclically connect the midpoint M of the system to the AC-side mains and injects current i_{h3}, which shows pulsed characteristics due to the buck stage. The buck converter is characterised by a pulsed current waveform at the input and a pulsed current of each free-wheeling diode D_+ and D_-. The positive buck converter has to form the averaged current signal of i_{pos} and the negative buck converter of i_{neg}. The output inductor L could also be implemented as one single choke ($2L$). If it is however split evenly between the positive and negative output bus, symmetric attenuation impedance is provided for improved common-mode noise behavior. Due to pulsed currents i_{pos}, i_{h3} and i_{neg}, a sophisticated EMI filtering is stringent necessary. Switching frequency current ripple and harmonics have to be suppressed substantially to meet the CISPR 22 Class B limit. The output voltage range of the system is limited by the minimal value of the B6 output voltage v_{rec}. It has to be mentioned that topologies **Fig. 2.5** and **Fig. 2.6** both allow output voltage regulation, whereas, the output voltage of topology **Fig. 2.4** is fixed according to the mains voltages. The third harmonic injection boost rectifier (**Fig. 2.5**) shows a higher minimum output voltage compared to topologies **Fig. 2.4** and **Fig. 2.6** due to its additional boost stage.

2.3.2 Passive Current Injection - Active Current Shaping

References [34–51] mention different types of rectifier topologies applying the third harmonic injection principle where passive current injection and active current shaping is applied. In the following, two different versions of these ”Minnesota

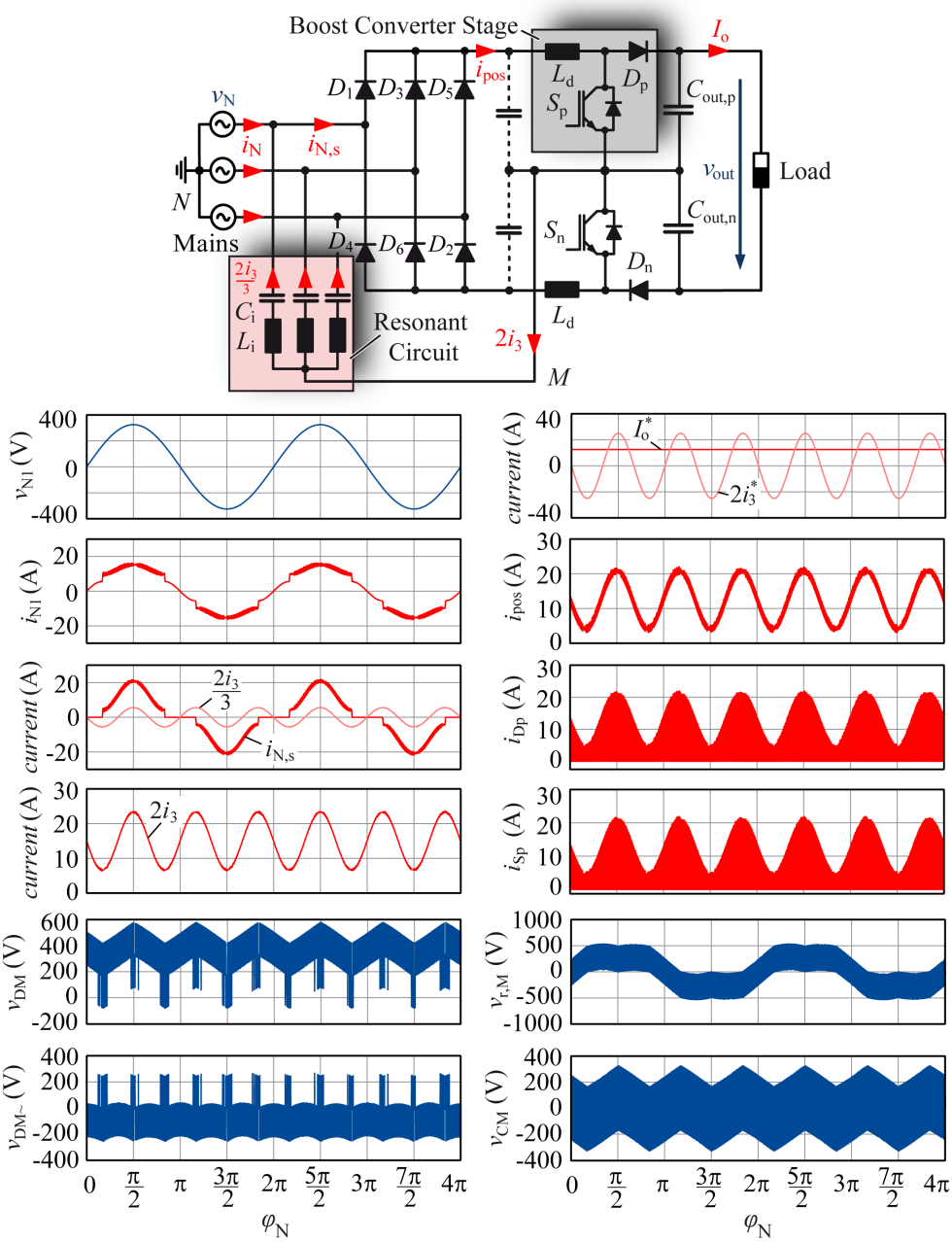


Fig. 2.7: Minnesota rectifier [34–38] consisting of a boost stage and a LC injection network.

rectifiers" [34–38] and [41–43, 45] are briefly discussed.

Fig. 2.7 and **Fig. 2.8** illustrate two different basic circuit implementations of the Minnesota rectifier. In **Fig. 2.7** at the output of the B6 bridge two boost converter stages are located which are directly connected via the midpoint M formed by capacitors $C_{\text{out,p}}$, $C_{\text{out,n}}$. Due to the boost converter topologies, the output voltage of the system v_{out} is controllable. The voltage transfer function of the switch-mode stage results in

$$\frac{v_{\text{out}}}{v_{\text{rec}}} = \frac{1}{2\,(1-\delta)}, \tag{2.3}$$

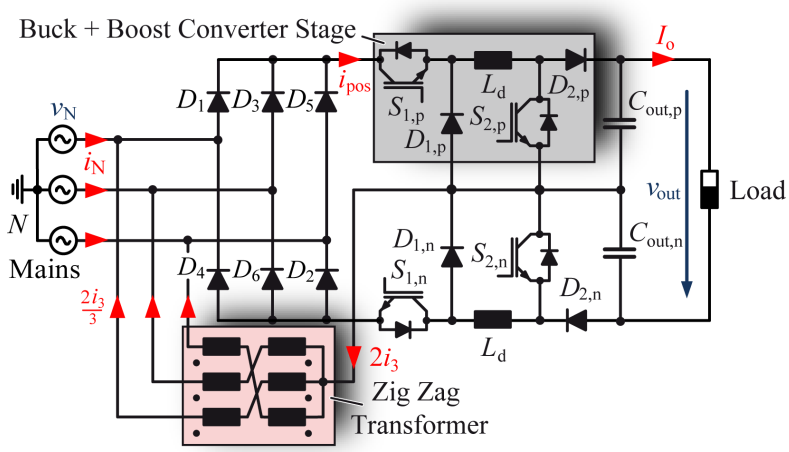


Fig. 2.8: Minnesota rectifier with additional buck converter stage located at the output of the passive three-phase rectifier topology and zig-zag transformer [41–43, 45].

which leads to a restricted minimum output voltage level of $v_{\mathrm{out,min}} = \sqrt{3}\hat{V}_{\mathrm{N}}$. The currents in the positive and negative busbar are modulated such to fulfill $I_{\mathrm{o}} + i_{\mathrm{h3}}$ and $I_{\mathrm{o}} - i_{\mathrm{h3}}$, respectively, where i_{h3} is defined by

$$i_{\mathrm{h3}} = \hat{I}_{\mathrm{h3}} \cos\left(3\omega_{\mathrm{N}} t + \phi_{\mathrm{h3}}\right). \tag{2.4}$$

This results in $2i_{\mathrm{h3}}$ in the third harmonic injection current path. The third harmonic injection network here is implemented as series connected LC circuit, tuned close to the 3rd harmonic of the mains frequency. The third harmonic injection current $2i_{\mathrm{h3}}$ is uniformly distributed among all three injection legs, each path has to carry $\frac{2}{3}i_{\mathrm{h3}}$. Small capacitors (dashed) at the output of the B6 bridge are necessary to provide a optional path for the switching ripple. These small capacitors however shall not affect the current waveform of the 3rd harmonic current which is modulated by the switch-mode stages. Furthermore, it has to be noticed that the presence of a finite grid input inductance L_{N}, results in an overlap commutation interval of the diode rectifier which even lead to slightly reduced line current distortions. Two different aspects affect the $\mathrm{THD_i}$ of input currents:

- $\hat{I}_3 / I_{\mathrm{d}}$
- (inductive) grid impedance L_{N}.

The minimum $\mathrm{THD_i}$ can be achieved for $\hat{I}_3 / I_{\mathrm{d}} \approx 0.72$, resulting in $\mathrm{THD_i} \approx 4.8\,\%$ for $L_{\mathrm{N}} = 0$. Influence of the input inductance L_{N} on $\mathrm{THD_i}$ of mains currents is demonstrated by:

- $L_{\mathrm{N,pu}} = 1\,\%$; minimum $\mathrm{THD_i} = 4.6\,\%$
- $L_{\mathrm{N,pu}} = 4.9\,\%$; minimum $\mathrm{THD_i} = 4\,\%$.

A phase-shift ϕ_{h3} of the third harmonic current of a few degrees (e.g. due to improper control), does not have any appreciable effects on the $\mathrm{THD_i}$ of input currents. As both converter stages are linked to the center of the output capacitors, a switching frequency common mode voltage v_{CM} can be observed. The impedance

of each injection path is defined as

$$Z_{\mathrm{i}}(\mathrm{s}) = R_{\mathrm{DC}} + \mathrm{s}L_{\mathrm{i}} + R_{\mathrm{ESR}} + \frac{1}{\mathrm{s}C_{\mathrm{i}}} \tag{2.5}$$

This impedance has to be designed, to act as short circuit ($Z_{\mathrm{i}} \to 0$) for the third harmonic current and tend to infinite ($Z_{\mathrm{i}} \gg 0$) for all other frequencies. Both values (capacitance and inductance), however, have to be selected such that the resonance of the circuit is not directly placed at the third harmonic frequency (e.g. $4 \cdot f_{\mathrm{N}}$ instead of $3 \cdot f_{\mathrm{N}}$) in order to avoid large unbalance of the currents through the injection branches caused by small differences of the LC branch parameters. For a chosen capacitance of e.g. 33 µF the appropriate inductance calculates to

$$L_{\mathrm{i}} = \frac{1}{\left(2\pi\left(4 \cdot f_{\mathrm{N}}\right)\right)^2 C_{\mathrm{i}}} = 19.2\,\mathrm{mH}. \tag{2.6}$$

The passive injection network is furthermore also affecting the power factor of the system. The input displacement power factor is hence defined by:

$$\cos\left(\Phi_1\right) = \frac{P_{\max}}{\sqrt{P_{\max}^2 + Q_{\mathrm{cap}}^2}} \quad \text{with} \quad Q_{\mathrm{cap}} = \frac{3}{2}\frac{\hat{V}_{\mathrm{N}}^2}{\left(\frac{1}{3\omega_{\mathrm{N}}C_{\mathrm{i}}} - 3\omega_{\mathrm{N}}L_{\mathrm{i}}\right)}. \tag{2.7}$$

The second version of the considered Minnesota rectifier (**Fig. 2.8**) employs a buck converter stage at the output of the B6 bridge, followed by a boost topology. Both DC-DC converters are sharing the smoothing inductor (L_{d}) and the output capacitor (C_{out}). Only one of both converter stages is in switching operating at the same time. If the output voltage is higher than the instantaneous rectifier voltage ($v_{\mathrm{out}} > v_{\mathrm{rec}}$), the buck-type converter switch is continuously closed and the boost stage is responsible for current modulation. When v_{out} on the other hand is below v_{rec}, the boost switch is opened and the buck stage is regulating the current waveforms. Both buck and boost converter may also operate at the same time (operating as fly-back converter) which increases the inductor current ripple. The current injection network here consists of a zig-zag transformer, which is connecting the injection path to each phase. Both current injection networks (LC network and zig-zag transformer) are stressed with equal current values $\frac{2}{3}i_{\mathrm{h3}}$.

2.3.3 Active Current Injection - Passive Current Shaping

In [52] an extension circuitry for three-phase diode bridge rectifiers consisting of an active current injection network (implemented as bidirectional switch arrangement) and a passive current shaping network is proposed (cf., **Fig. 2.9**). The passive network is composed of three resistors and two capacitors. The capacitors are mandatory in order to remove the DC components of both voltages v_{ac} and v_{bc}. For design of the required resistors it is assumed that the capacitance of C is sufficient that its voltage can be considered to remain constant ($v_{\mathrm{Cap}} = 1/2 v_{\mathrm{out}}$).

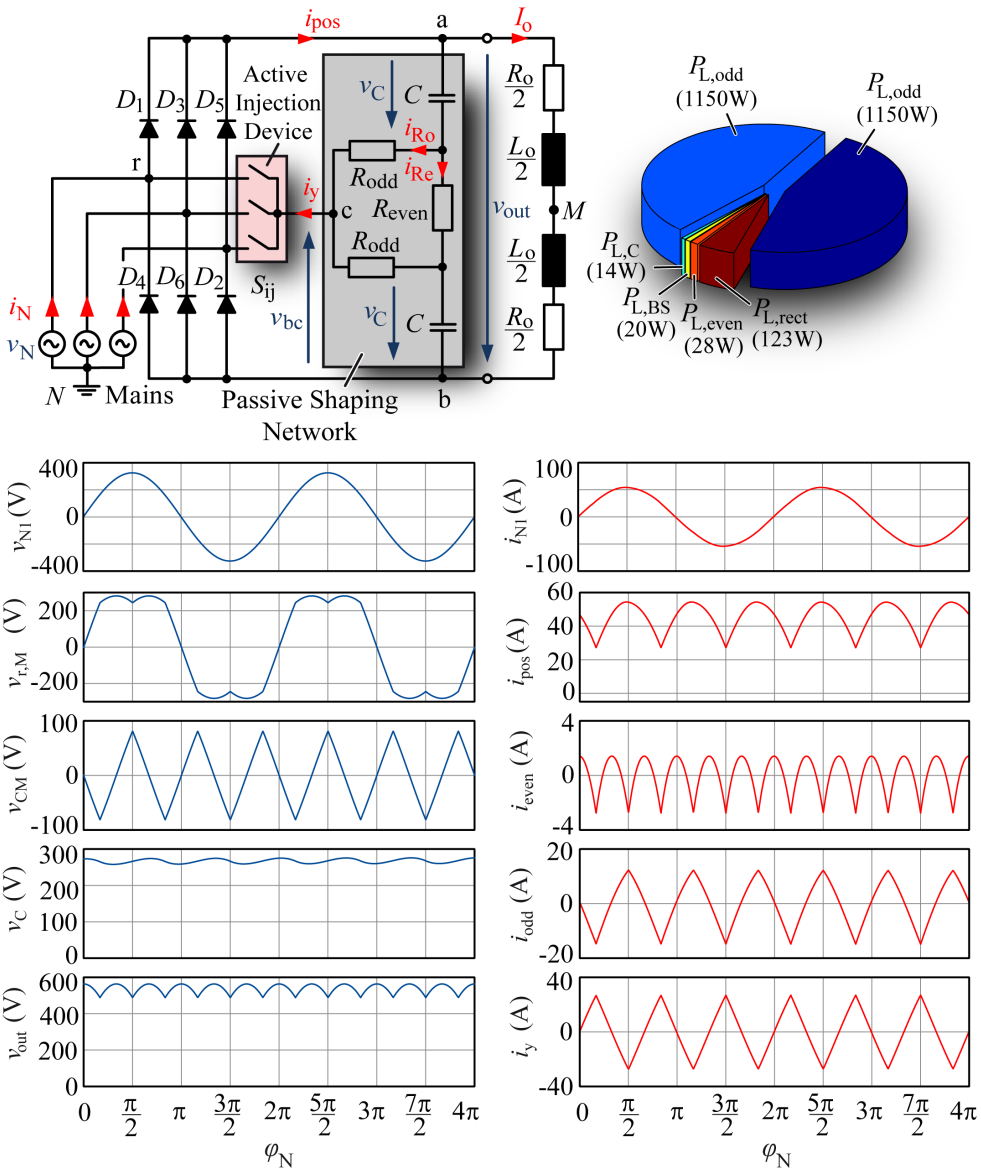


Fig. 2.9: Hybrid rectifier system employing passive current shaping network and active current injection device (bidirectional switches) [52].

Values of the resistors then result in $R_{\text{even}} = R_{\text{odd}} = 3R_{\text{e}}$ and sinusoidal input currents can hence be expected. R_{e} denotes the impedance observed by each phase which should be linear and purely resistive

$$R_{\text{e}} = \frac{\hat{V}_{\text{N}}}{\hat{I}_{\text{N}}} \,. \tag{2.8}$$

One of the major drawbacks of this circuit is the poor efficiency due to the resistive implementation. Simulation results are performed for a 27 kW input power (P_{in}) system. As no output LC output filter is used, the B6 voltage v_{rec} is directly fed to the load. If capacitor voltages v_{C} are assumed to remain approximately constant, the voltage across R_{even} shows no DC-component and results in $v_{\text{even}} = v_{\text{rec}} - v_{\text{out}}$. Due to the absence of high frequency switching semiconductors no switching fre-

quency ripple has to be attenuated. Furthermore, no switching frequency common mode or differential mode voltage component exists. Distortions of input currents are dependent on the design parameter γ. A graph which represents the correlation $\mathrm{THD_i}\,(\gamma)$ is given in [52]. Extracting the required parameters of this graph will result in $\gamma = 8.5$ for a $\mathrm{THD_i}$ of 0.6 %. According to

$$\gamma = 3\omega_0 C R_\mathrm{e} \tag{2.9}$$

and for a desired input power of 27 kW ($R_\mathrm{e} \approx 6\,\Omega$), C results in a capacitor value of 1.5 mF whereas ω_0 is corresponding to $2\pi f_\mathrm{N}$. Simulation results of the input current finally implicate a $\mathrm{THD_i}$ of 0.64 %. As already mentioned, one of the major drawbacks (besides the non suppressed output voltage ripple) is the very low system efficiency of the circuit. Based on **Fig. 2.9** total system losses $P_\mathrm{L,sys}$ can be calculated to ≈ 2.5 kW which results in an efficiency of only

$$\eta_\mathrm{sys} = \frac{P_\mathrm{in} - P_\mathrm{L,sys}}{P_\mathrm{in}} \approx 90.5\,\%\,. \tag{2.10}$$

This poor efficiency is mainly evoked due to resistors R_odd as they represent almost 91 % of the total system losses. If an improved efficiency of the current shaping network is required, all resistors could hence be implemented as switch-mode resistance emulators, which would increase the complexity of the enhanced circuit significantly.

2.3.4 Passive Current Injection - Passive Current Shaping

There are several hybrid rectifier topologies known which are based on the passive current injection/passive current shaping concept. These rectifier systems are extensively discussed in [52–63]. One specific rectifier, which is illustrated in **Fig. 2.10** and analyzed in [58] is going to be briefly discussed in this work. The current injection network is implemented as simple and well known star/delta (YD) transformer (where the secondary side appears to be short-circuited) and forms the interconnection between the AC- and the DC-side of the B6 bridge. Due to its passive implementation the complexity of the circuit is very low. The main challenge of this circuit is the proper design of the resonant circuit provided by L_f in connection with C_p and C_n.
The third harmonic current is generated according to the instantaneous state of the passive rectifier and the design of the implemented passive components. Due to its purely passive implementation no controller is necessary. The generated circulating third harmonic current is simultaneously going to be injected into all three mains phases with one-third of the fundamental magnitude of i_f. A total harmonic input current distortion of $< 5\%$ is achievable if the ratio between third harmonic current $I_\mathrm{f,rms}$ and output current I_o is close or equal to $1 (= I_\mathrm{f,rms}/I_\mathrm{o})$ which can be only reached due to a proper design of the LC resonant circuit. This circuit has to be tuned close to the third harmonic frequency ($3f_\mathrm{N}$). For the circuit

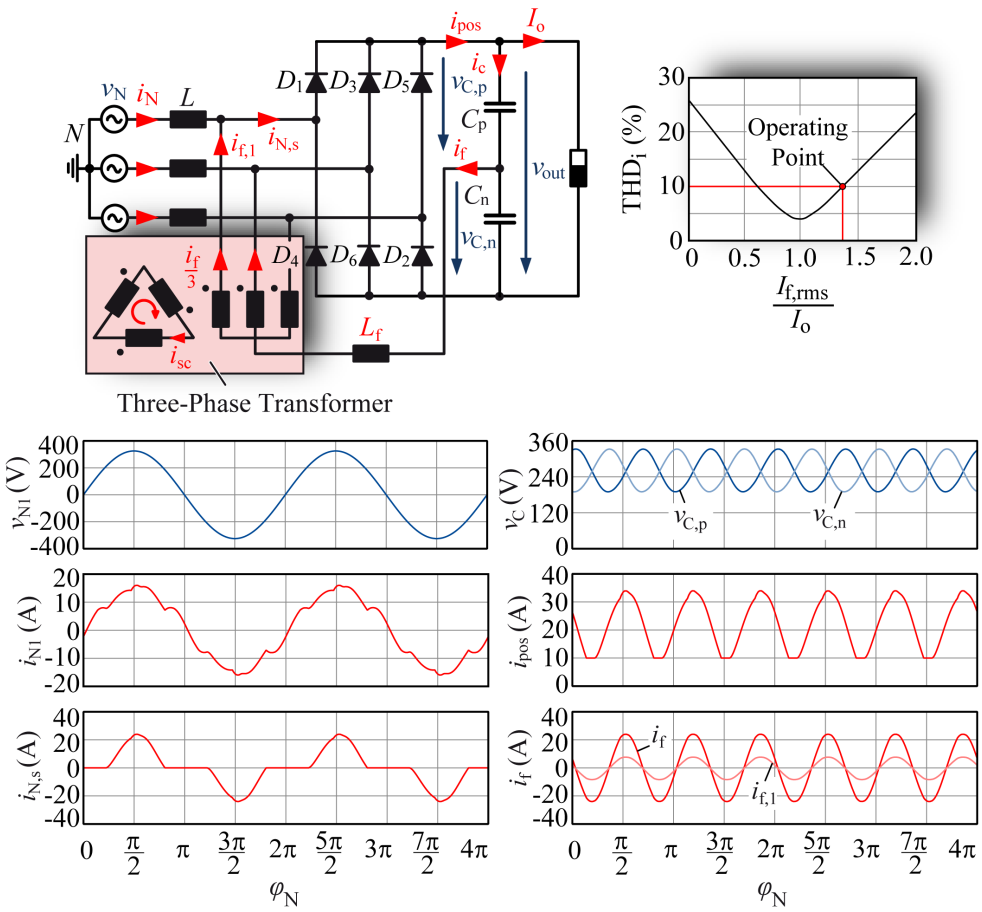


Fig. 2.10: Three-phase power factor correction circuit considering the THI principle employing a three-phase transformer [58].

at hand L_{inj} is selected to 3 mH ($= L_f + L_{stray} = 2.8\,\text{mH} + 200\,\mu\text{H}$) and a output capacitance of $C_p = C_n = 270\,\mu\text{F}$ is used which results in a resonance frequency of

$$f_{res} = \frac{1}{2\pi\sqrt{L_{inj}C_p}} = \frac{1}{2\pi\sqrt{L_{inj}C_n}} = 176\,\text{Hz}. \tag{2.11}$$

This resonance frequency has to be chosen slightly higher than the third harmonic frequency $3f_N$ for proper operation. The amplitude of $I_{f,rms}$ can be calculated to 17 A for an output current of 12 A which leads to a third harmonic to output current ratio of

$$\frac{I_{f,rms}}{I_o} = 1.416, \tag{2.12}$$

resulting in a THD$_i$ of the mains input currents i_{Ni} of 10.6 %. The dependency of THD$_i$ on the ratio of $I_{f,rms}/I_o$ is depicted in **Fig. 2.10(top)**. The kVA rating of the injection Yd-transformer is defined by

$$\text{Transformer VA Rating} = 3\left(\frac{V_{LL,rms}}{\sqrt{3}}\right)\frac{I_{f,rms}}{3} \approx 4\,\text{kVA}. \tag{2.13}$$

In order to obtain the optimum operation under varying load conditions it is essential to adjust the magnitude of the circulating third harmonic current i_{f}. This can be accomplished i.e. by the use of a saturable reactor or a magnetic amplifier. The size of the reactor can be considered reasonably small at third harmonic frequencies.
It has to be mentioned that one of the main drawbacks is the required very precise tuning of the LC resonance network. It is highly sensitive to low frequency grid harmonics as its resonance frequency is close to the 150 Hz.

2.4 Multipulse Topologies - Passive/Hybrid Rectifiers

Three-phase multipulse rectifier systems typically come with two (e.g. [64]) or even more passive B6 rectifiers (cf, [65]). They furthermore require a specific transformer arrangement (as mentioned in [65]) and may be implemented in series or parallel configuration. For parallel configuration an interphase transformer is required. In this specific case (cf., [64]) the transformer arrangement consists preferably of a Ydy-transformer. The multipulse rectifier shown in **Fig. 2.11** is extended by two additional IGBT half-bridges which serve as controllable current source. These two DC-DC converters have to compensate the 300 Hz components of the output inductor current $i_{\mathrm{L,f}}$ and provide a triangular shaped current i_{rec}. This triangular waveform is defined by

$$i_{\mathrm{rec1}}\left(\varphi_{\mathrm{N}}\right) = I_{\mathrm{L}} + I_{\mathrm{L}} \cdot tri\left(6\varphi_{\mathrm{N}}\right) \tag{2.14}$$

and can be calculated by

$$i_{\mathrm{rec1}}\left(\varphi_{\mathrm{N}}\right) = I_{\mathrm{L}} - 4I_{\mathrm{L}} \sum_{k=1}^{\infty} \frac{1-(-1)^{k}}{k^{2}\pi^{2}} \cos\left(6k\varphi_{\mathrm{N}}\right). \tag{2.15}$$

The current waveshape of i_{rec2} equals i_{rec1} with a 180° phase shift ($i_{\mathrm{rec1}}\left(\varphi_{\mathrm{N}}+\pi\right)$). These currents are generated by a current-controlled inverter which injects the compensational currents into the three positive terminals of the diode bridges in order to improve the quality of the AC line currents). The output voltage of the total system is twice that one of one single B6 bridge and hence

$$V_{\mathrm{o}} = 2\frac{3\sqrt{3}}{\pi}\hat{V}_{\mathrm{N}} \tag{2.16}$$

The input currents of both B6 diode bridges result in triangular shaped currents $i_{\mathrm{a,b,c,1}}$ and $i_{\mathrm{a,b,c,2}}$ with 60° zero gaps. The lower passive bridge is connected to the star arrangement of the secondary side, the output currents of the transformer are equal to the input currents of the bridge ($i_{\mathrm{N1y}} = i_{\mathrm{a2}}$). As the upper diode bridge is connected to a delta arranged winding, the B6 input currents are defined by

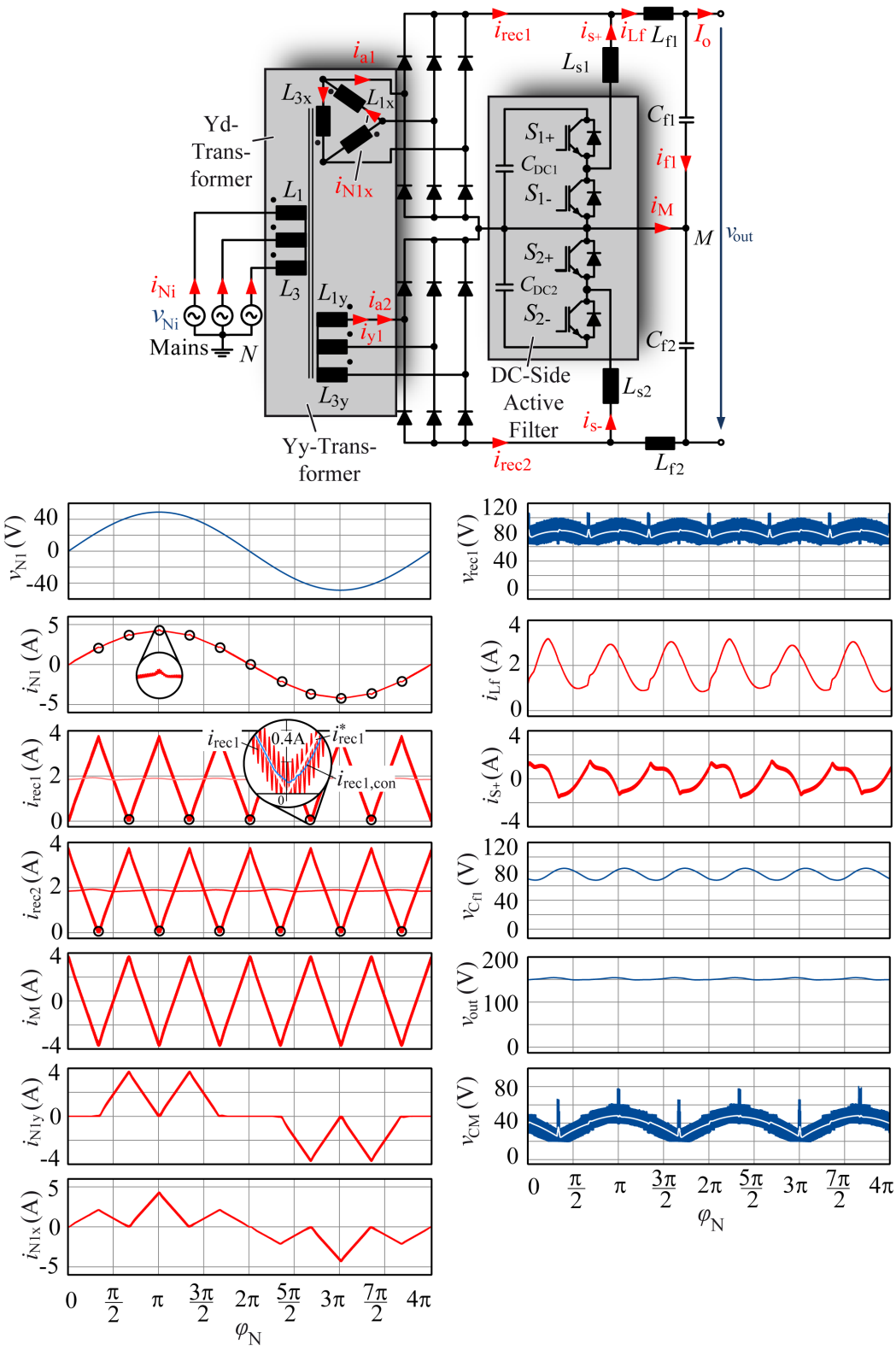


Fig. 2.11: Three-phase passive 12-pulse rectifier systems enhanced by additional DC-side active power filter for sinusoidal mains currents.

$i_{a1} = i_{N1x} - i_{N3x}$, $i_{b1} = i_{N2x} - i_{N1x}$, and $i_{N1x} + i_{N2x} + i_{N3x} = 0$. This leads to

output currents of the transformer which calculate to

$$i_{\mathrm{N1x}} = \frac{i_{\mathrm{a1}} - i_{\mathrm{b1}}}{3}. \tag{2.17}$$

Waveshapes and magnitudes of these currents are shown in **Fig. 2.11**. The input current at the primary side of the Ydy-transformer is formed by

$$i_{\mathrm{N1}} = \frac{N_{\mathrm{2x}}}{N_1} i_{\mathrm{N1x}} + \frac{N_{\mathrm{2y}}}{N_1} i_{\mathrm{N1y}} \tag{2.18}$$

and furthermore equal to the mains input currents. As purely sinusoidal AC input currents have to be achieved, the relation of primary and secondary windings of the system is predefined by

$$N_1 = N_{\mathrm{2y}} = N \quad \text{and} \quad N_{\mathrm{2x}} = \sqrt{3}N. \tag{2.19}$$

It has to be noted that only a minimum $\mathrm{THD_i}$ of 2 % can be achieved. This fundamentally originates from the required triangular signal i_{rec1} and i_{rec2}. The current controller is not able to properly adjust currents close to zero because, currents smaller than zero (which would apply for the superimposed current ripple with switching frequency) will be entirely blocked by the diode bridge. This will lead to current distortions of i_{rec1} and i_{rec2} and consequently to a increased input current $\mathrm{THD_i}$ (cf., mains current distortions every $\pi/6$ – highlighted graph in **Fig. 2.11**). Multipulse topologies furthermore, in general result in very high complexity and implementation effort due to their high number of active an passive components (diodes, switches, transformer,...) despite their promising performance.

2.5 VIENNA Rectifier

The VIENNA rectifier was first published in 1994 (cf., [66]) and is characterized as active AC to DC boost-type conversion system with unidirectional power flow (due to its diode arrangement, **Fig. 2.12**). In course of time, several circuit variants have been reported (denoted here VIENNA rectifier I, II, III) operating at switching frequencies from a couple of kilohertz (optimized for efficiency) to 1 MHz (optimized for power density). As there are dozens of publications available which are engaged in analysis concerning current/voltage-control (cf., [67, 68]), optimization issues regarding volume/efficiency/power density etc., [69–73] are therefore listed here as most relevant PhD-theses in this field of interest. The basic topology (VIENNA I) consists of six diodes and a single MOSFET for each leg. Due to the additional diodes the voltage stress across the active switch is cut in half which allows the implementation of 600 V MOSFET technology compared to the six switch rectifier where each switch is stressed with the total output voltage V_{o} (resulting usually in an IGBT implementation at much lower switching frequencies). Due to the diode arrangement, only unidirectional power flow is possible. The rectifier can be considered as three-phase diode bridge rectifier ($D_{\mathrm{F}\pm}$) with

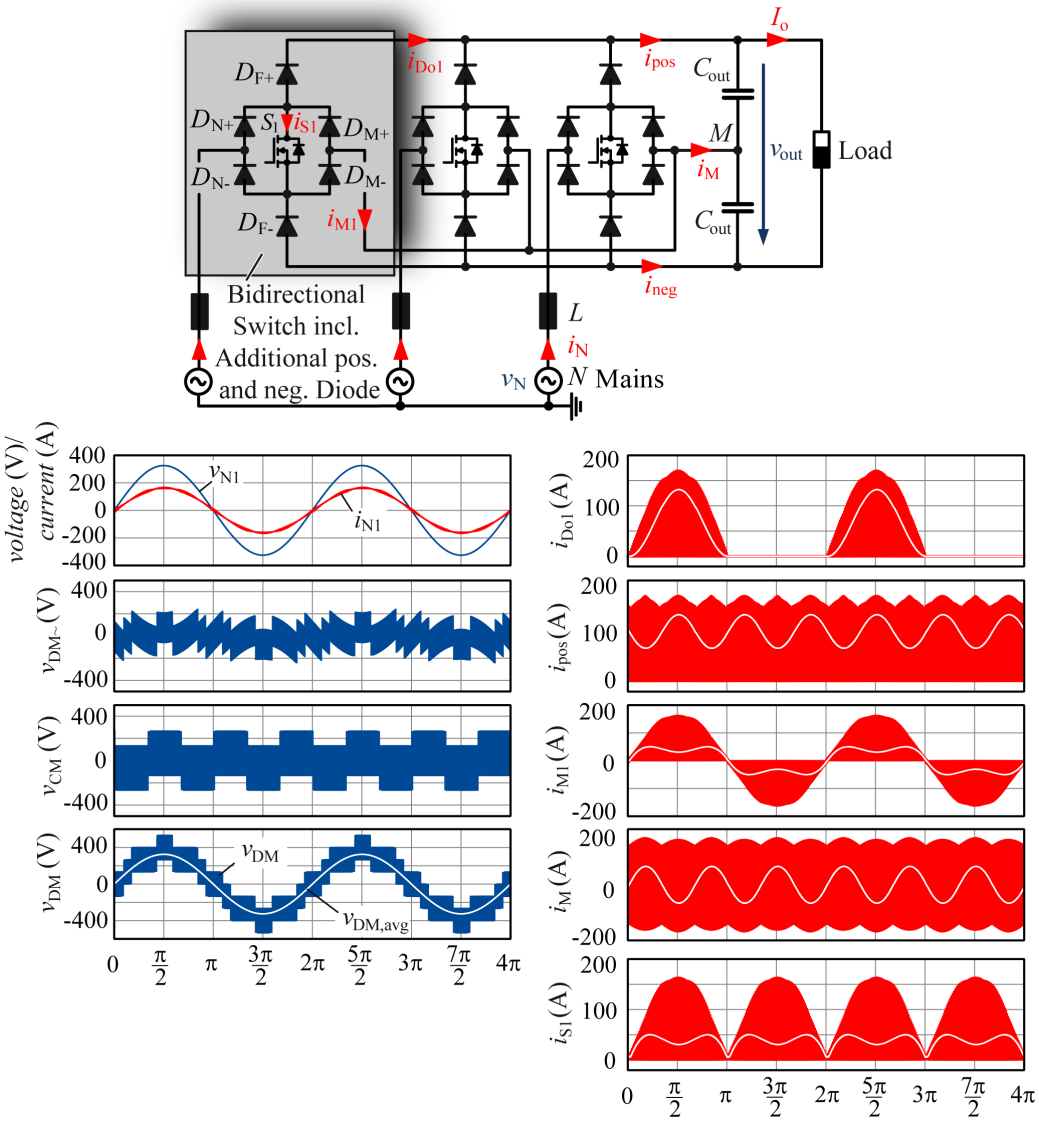


Fig. 2.12: VIENNA Rectifier I implemented as three bidirectional switches and two additional diodes for each switching leg.

integrated bidirectional switch ($D_{N\pm}$, S_i, $D_{M\pm}$). The bidirectional switches are furthermore connected to the AC-side boost inductors via the two diodes $D_{N\pm}$ at the input and directly clamped to the midpoint of the split DC capacitor output M by $D_{M\pm}$. The diode D_{N+} is permanently conducting during the positive half-wave of i_{N1} and D_{N-} during the negative half-wave. Therefore, line-frequency diodes with low forward voltage and hence low conduction losses can be applied. Diodes $D_{F\pm}$ and $D_{M\pm}$ are commutated with switching frequency and have to be selected as high-speed types to reduce switching losses.

If the MOSFET is turned off, $V_o/2$ (for positive currents I) and $-V_o/2$ (for negative currents $-I$) appears across the transistors. If the device is turned on, the boost inductor is directly connected to the midpoint M (0 V). The VIENNA rectifier, hence, results in a three-level topology reducing the switching frequency ripple in L. Furthermore, V_{out} shows a switching-frequency common mode voltage which

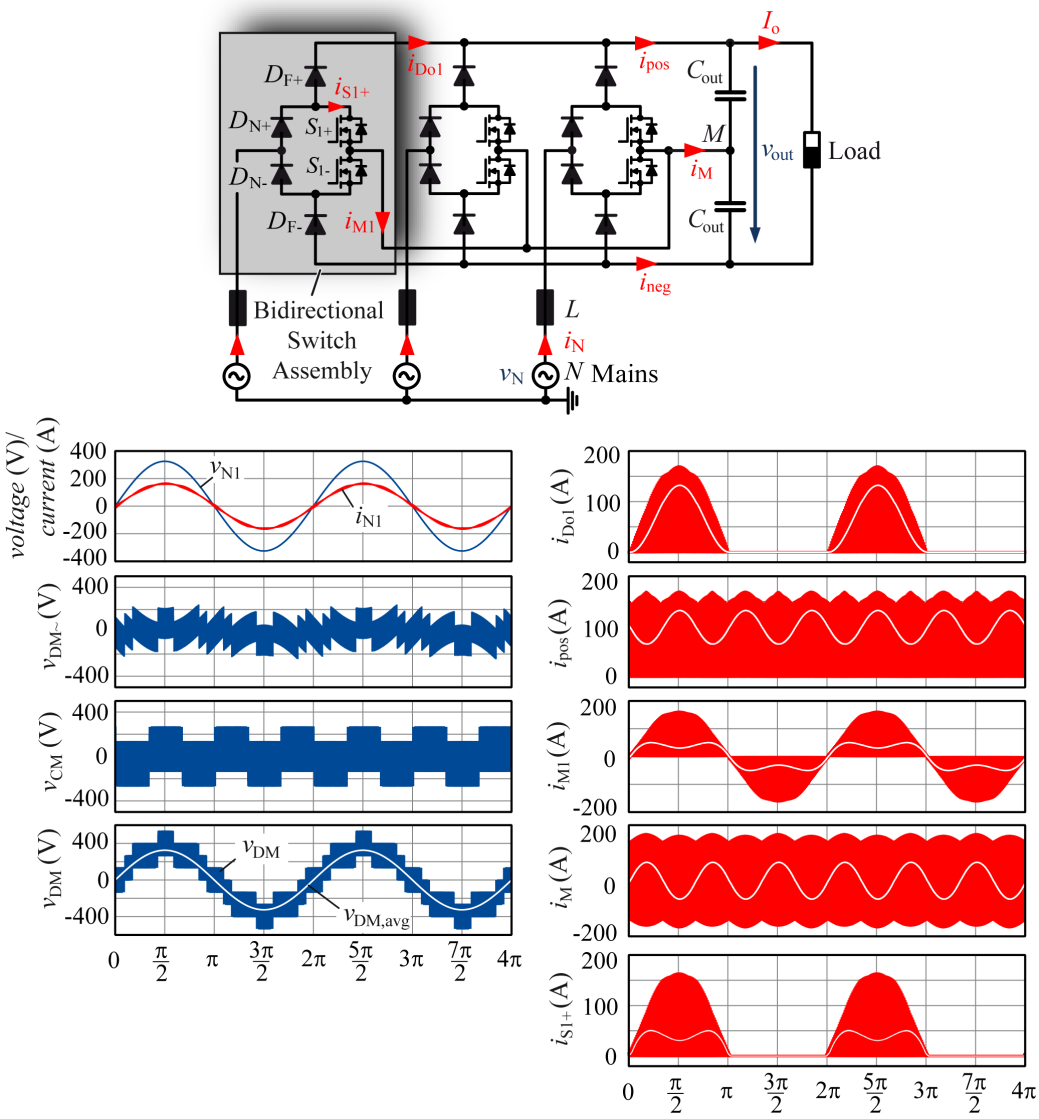


Fig. 2.13: VIENNA Rectifier II implemented as bidirectional switch assembly with two active switches and two additional diodes for each switching leg.

has to be considered in the design of the EMI filtering. The VIENNA rectifier could also be operated in DCM which however requires a specific control method which is discussed in [68].

If conduction losses of the circuit have to be improved, the two diodes D_M can be replaced by an additional switch (**Fig. 2.13**, cf., [74]). Current and voltage waveforms of this VIENNA II are very similar to the VIENNA I with the exception that the positive MOSFET S_{i+} is turned on only for positive currents i_{Ni} whereas S_{i-} is active for negative half-waves of i_{Ni}.

If these two active switches are implemented as back-to-back arrangement, the diodes connected to the AC-side $D_{N\pm}$ can be omitted which is leading to the circuit of **Fig. 2.14**, denoted as VIENNA III. This topology shows a low number of components (six diodes and six switches). The diodes connected to the positive and negative bus are nevertheless still commutated with switching frequency and

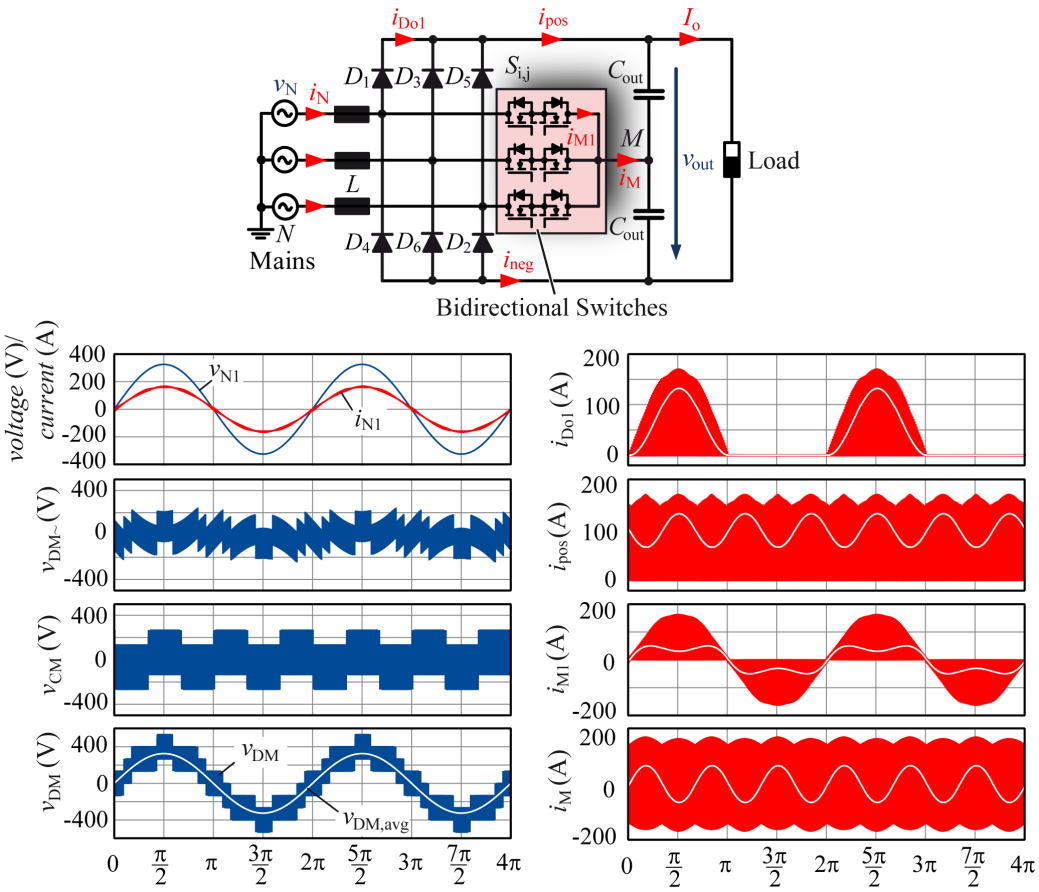


Fig. 2.14: VIENNA Rectifier III utilizing three bidirectional switches directly clamped to the center of the DC-link output capacitors.

have to be dimensioned regarding the full DC-link voltage V_{out}.

2.6 AC-side (Shunt) Active Power Filter

Alternatives for achieving low harmonic input currents and high power factor are AC-side (shunt) active power filters as discussed, e.g., in [75–84]. These concepts in general are characterized by an apparent lower complexity compared to DC-side filter structures. E.g. a simple six-switch PWM converter (VSI) arranged in parallel to a diode bridge rectifier can be used to compensate the rectifiers input harmonics resulting in sinusoidal mains currents of the total system (**Fig. 2.15**). The required currents for the paralleled power electronics circuit are

$$i_{\text{f,i}}\left(\varphi_{\text{N}}\right) = \hat{I}_{\text{N}} \sin\left(\varphi_{\text{N}} + \Phi_{\text{i}}\right) - i_{\text{D,i}}\left(\varphi_{\text{N}}\right). \tag{2.20}$$

If a B6 diode bridge rectifier with DC-side inductance is assumed the commutation interval is much shorter than that for a B6 with AC-side smoothing inductances. This results in a much higher $\mathrm{d}i/\mathrm{d}t$ rate while B6 input currents are commutating from one phase to the next. The bandwidth of the VSI has to be much higher than for a VSI compensating a B6 rectifier with AC-side chokes (remark: the maximum

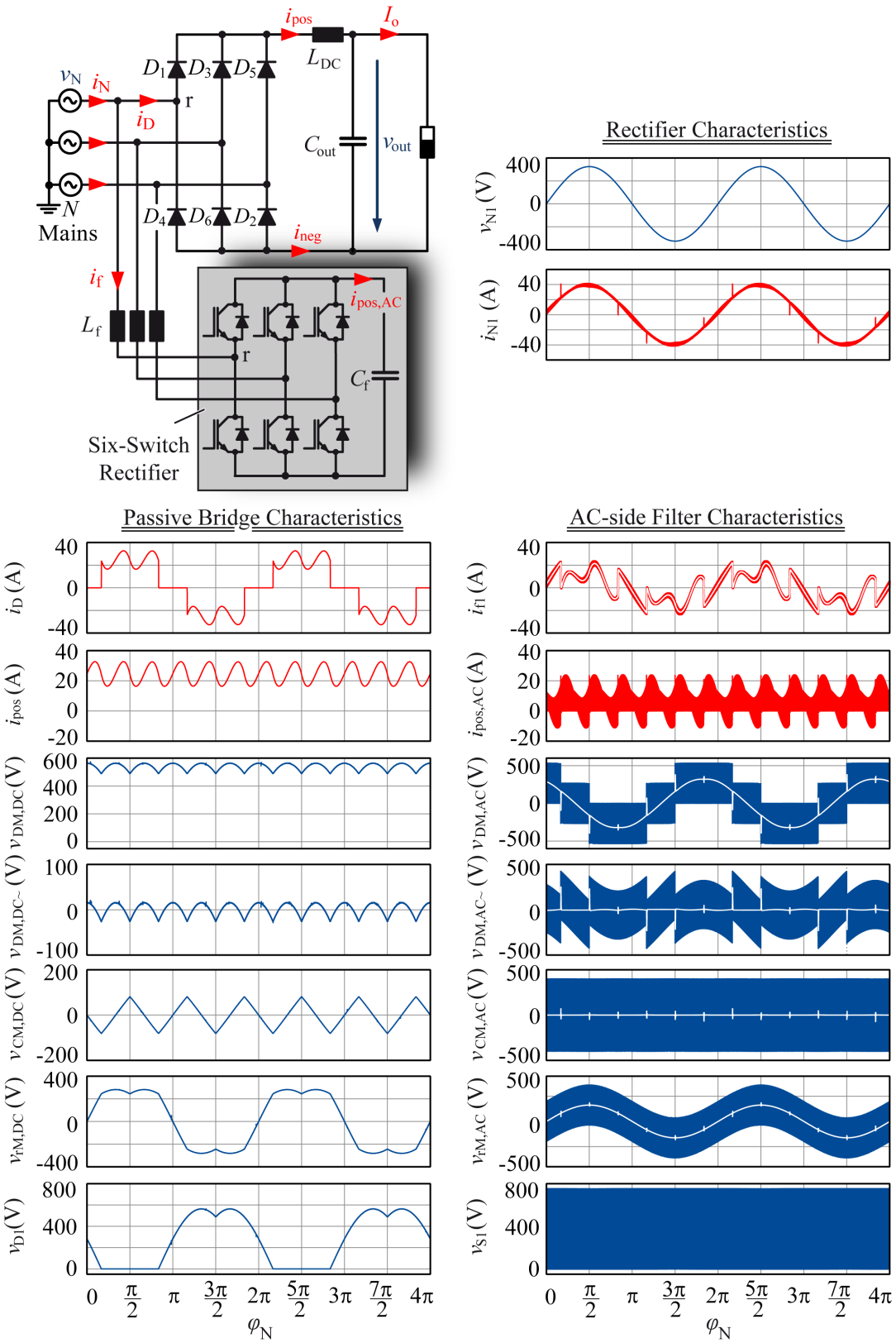


Fig. 2.15: Six-switch PWM converter arranged in parallel to a diode bridge rectifier (AC-side active filtering) for compensation of the B6 input current harmonics resulting in sinusoidal mains currents of the total system.

current harmonic order which should be compensated determines the required VSI bandwidth).
The required input current peak value can be calculated by measuring the instantaneous output current $i_{\mathrm{L,avg}}(= I_{\mathrm{o}})$. If losses of passive and active components are neglected

$$P_{\mathrm{in}} = 3V_{\mathrm{N,rms}}I_{\mathrm{N,fund,rms}} \approx P_{\mathrm{o}} = V_{\mathrm{o}}I_{\mathrm{o}} \tag{2.21}$$

is valid. Simplification and elimination of input and output voltages finally leads to a input peak current of

$$\hat{I}_{\mathrm{N}} = \frac{2\sqrt{3}}{\pi}I_{\mathrm{o}}. \tag{2.22}$$

This current amplitude can now directly be fed as a reference value to the current controller of the VSI. A comparison of characteristics of the passive bridge and the active filter unit is given in **Fig. 2.15**. If the AC-side filter is used as an add-on extension of a passive rectifier, an additional LC filter for suppressing the switching frequency components of i_{f} is required (which restricts the bandwidth of the active filter topology).
As both (AC- or DC-side) filtering concepts are suitable for harmonic current suppression of passive three-phase rectifiers differences are addressed and discussed in [4]. It is stated that besides increased complexity DC-side active filters show advantages as

i. reduced switch stress
ii. increased compensation capacity and
iii. improved compensation performance.

2.7 Additional Improved Power Quality Converters (IPQC)

In [85–89], there are numerous other rectifier circuits (hybrid and active) described which may support suppression of harmonic input current components. These IPQC-topologies, are listed here for sake of completeness but not discussed in this work.
Remaining IPQCs as listed are as follows:

- **Bidirectional Converters:**
  - Four-switch bidirectional boost converter
  - Four-wire bidirectional boost converter
  - Four-legged bidirectional boost converter
  - GTO-based bidirectional buck converter
  - IGBT-based bidirectional buck converter

  - Four-pole bidirectional buck converter
- **Bidirectional Multilevel Converters:**
  - Five-level diode-clamped bidirectional converter
  - Five-level flying capacitor bidirectional converter
- **Bidirectional Multipulse Converters:**
  - 24-pulse bidirectional midpoint reactor converter
  - 48-pulse bidirectional converter.
- **Unidirectional Converters:**
  - Unidirectional boost converter using isolated Scott connection transformers
  - Single-switch unidirectional buck converter
  - Three-phase CSI-based unidirectional buck converter
  - Four-switch unidirectional buck-boost converter
  - SEPIC derived unidirectional buck-boost converter
  - Flyback-derived unidirectional buck-boost converter
  - Isolated Cuk-derived unidirectional buck-boost converter
  - Matrix-converter-based bidirectional buck-boost converter
  - Unidirectional five-level converter
  - Y-Switch rectifier [90]
  - Delta-Switch rectifier [31, 32, 90–102]
  - Electronic smoothing inductor (ESI) [10, 103, 104]
- **Unidirectional Multipulse Converters:**
  - Unidirectional 12-pulse converter
  - Unidirectional 18-pulse converter
  - Unidirectional 24-pulse converter

Within this chapter 2 a survey of most interesting concepts for achieving AC-to-DC conversion with low-harmonic mains currents is given to describe the present state-of-the-art and define a starting point for the development and research novelties treated in the following chapters where several topology variants of add-on circuits for B6 rectifiers with DC smoothing inductors are proposed which are derived from or slightly relate to the principle of **Fig. 2.4**. At first a prior detailed analysis of the exact operation and properties of B6 diode rectifiers is required and topic of the following chapter 3.

Chapter 3

The Passive Three-Phase Rectifier

In this chapter now the operation of passive three-phase rectifiers (B6 diode bridge with LC filter) is analyzed in detail which is required for understanding the further discussions and developments of active third harmonic injection units for such passive B6 rectifiers. For this, the most important attributes of B6 circuits are derived analytically and verified by simulations and experimental results.
In [105] some major aspects considering passive three-phase rectifier systems are listed and discussed. Besides analysis of continuous conduction mode (CCM) operation further also current and voltage waveforms considering discontinuous conduction mode I and II are addressed and explained.
For power supply applications where only unidirectional power flow is required (e.g. motor applications, water pumping systems etc.) passive three-phase rectifier systems are very well suited. On the one hand, passive rectification typically shows the advantage of low cost. Diodes which are optimized for low conduction losses (available as fully assembled diode bridge chip/module), offer a very high efficiency ($\eta \approx 99\,\%$), robustness and low complexity (compared to active structures - no controller circuits, additional digital hardware, gate drives, auxiliary power supply etc.). On the other hand, however, such rectifiers are characterised by limited power factor ($\lambda < 0.9 \ldots 0.95$), relatively poor input current quality ($\mathrm{THD_i} > 31\,\%$, typically $\mathrm{THD_i} \approx 45\%$) and uncontrolled output voltage defined by the mains voltages. Applications as for example AC-drives basically do not require a controlled DC voltage, hence, an uncontrolled DC-link voltage must not be seen as a substantial drawback. In general, there are two different types of passive three-phase diode bridge systems:

- Passive three-phase rectifiers with **DC-side inductor**.
- Passive three-phase rectifiers with **AC-side chokes**.

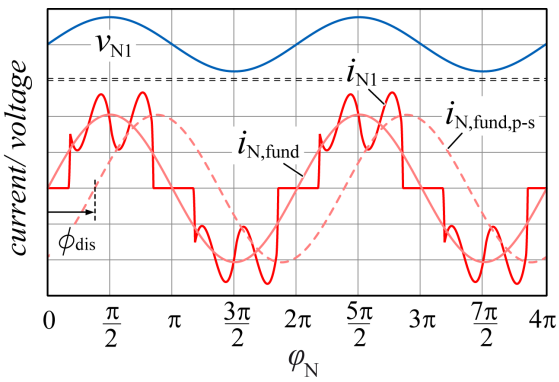


Fig. 3.1: Illustration for explaining the displacement angle ϕ_{dis} being defined in general by the angle between fundamental input current ($i_{N,fund}$, $i_{N,fund,p-s}$) only assumed here and mains voltage (v_N). Also shown: input currents $i_{N,i}$ of a B6 rectifier with DC-side located inductor, leading to $\phi_{dis} \approx 0\,°$.

The following section hence briefly investigates and compares main characteristic quantities of passive three-phase rectifiers with either AC- or DC-side smoothing chokes.

3.1 Comparison of B6 with AC- or DC-Side Smoothing Inductor

As mentioned, the power factor of the passive three-phase diode bridge is limited typically to 0.9 . . . 0.95. This limitation is given by the THD_i of the system and the fundamental current-to-voltage displacement angle ϕ_{dis}. As depicted in **Fig. 3.1**, input currents $i_{N,i}$ (and their corresponding fundamental waveforms) of a B6 rectifier lead to $\phi_{dis} \approx 0\,°$. As will be explained later in this chapter, the THD_i of the B6 rectifier is limited to

$$THD_{i,min} = \sqrt{\frac{\pi^2}{9} - 1} = 0.311. \tag{3.1}$$

The appropriate power factor of a B6 bridge (for balanced input currents and voltages) calculates to

$$\lambda = \frac{P_{in}}{S_{in}} = \frac{3V_{N,rms}I_{N,fund,rms}}{3V_{N,rms}I_{N,rms}} \cos(\phi_{dis}) = \frac{I_{N,fund,rms}}{I_{N,rms}} \cos(\phi_{dis}), \tag{3.2}$$

where P_{in} denotes the active input power, S_{in} the apparent power and $I_{N,fund,rms}$ the RMS value of the fundamental component of the input current. Furthermore, the total harmonic input current distortion of input currents (THD_i) is defined by

$$THD_i = \frac{\sqrt{I_{N,rms}^2 - I_{N,fund,rms}^2}}{I_{N,fund,rms}}, \tag{3.3}$$

which can be transferred to

$$I_{\mathrm{N,fund,rms}} = I_{\mathrm{N,rms}} \frac{1}{\sqrt{1+\mathrm{THD}_{\mathrm{i}}^2}}. \tag{3.4}$$

If the fundamental current component is substituted by **Eq. 3.2**, λ is defined as a function of the fundamental displacement factor and input current distortion which is given by

$$\lambda = \frac{1}{\sqrt{1+\mathrm{THD}_{\mathrm{i}}^2}} \cos\left(\phi_{\mathrm{dis}}\right). \tag{3.5}$$

Hence, the maximum power factor of a passive three-phase rectifier ($\phi_{\mathrm{dis}} = 0\,^\circ \rightarrow \cos\left(\phi_{\mathrm{dis}}\right) = 1$) calculates to

$$\lambda_{\mathrm{max}} = \frac{1}{\sqrt{1+\frac{\pi^2}{9}-1}} \cdot 1 = \frac{3}{\pi} \approx 0.95. \tag{3.6}$$

In general, passive three-phase diode bridge rectifiers can be implemented with either three AC-side inductors (**Fig. 3.2(a)**) or using a single DC-side current smoothing inductor (**Fig. 3.2(b)**). Even though a rectifier with DC-side located choke seems to be far more practical (only one coil needed, less winding copper necessary, less output voltage drop due to shorter diode bridge commutation time,...) both topologies are commonly used in industry. As illustrated in **Fig. 3.2**, both variants show rather different characteristics concerning output voltage v_{o} and power factor λ. For B6 rectifiers with DC-side inductor (**Fig. 3.2(a)**), the output power is rather constant for a wide range of DC-side inductance values. This is merely owed due to the short current commutation interval u_{d} which is defined by the AC-side inductances. If B6 rectifiers with DC-side LC filter (as depicted in **Fig. 3.2(a)**)are considered, u_{d} is defined according to the mains impedance (L_{N}) and/or cable inductance, input voltage and output current. Thus, u_{d} is independent of the design of L_{DC} as long as CCM operation applies. Hence also the output voltage v_{o} is approximately constant for different values of L_{DC} during CCM (cf., **Fig. 3.2(a)**). Compared to a B6 with DC-side LC output filter, a passive rectifier with AC-side inductors as shown in **Fig. 3.2(b)** directly influences u_{d} according to the design of L_{AC}. The additional AC-side inductance L_{AC} leads to a more perceiving current commutation interval u_{d} and hence a reduced output voltage v_{o}. Besides slightly varying current waveforms of the different B6 topologies (with AC-side and DC-side inductor), also the increased current commutation interval u_{d} is affecting the characteristics of λ and v_{o} and hence directly impairing the $\mathrm{THD_i}$ – λ is directly dependent on the respective $\mathrm{THD_i}$ value (cf., **Eq. 3.2**) – of input currents i_{Ni}.

In this work, however, only rectifiers with DC-side located chokes are further analyzed as this type of passive rectifier is defined to be upgraded by active third harmonic injection circuits.

Fig. 3.3 therefore depicts a conventional passive three-phase rectifier system composed of a diode bridge (B6) consisting of six line-frequency diodes (D_1-D_6) connected to the three-phase grid (grid inductance $L_{\mathrm{N}} \approx 60\,\mu\mathrm{H}$), a DC-side located

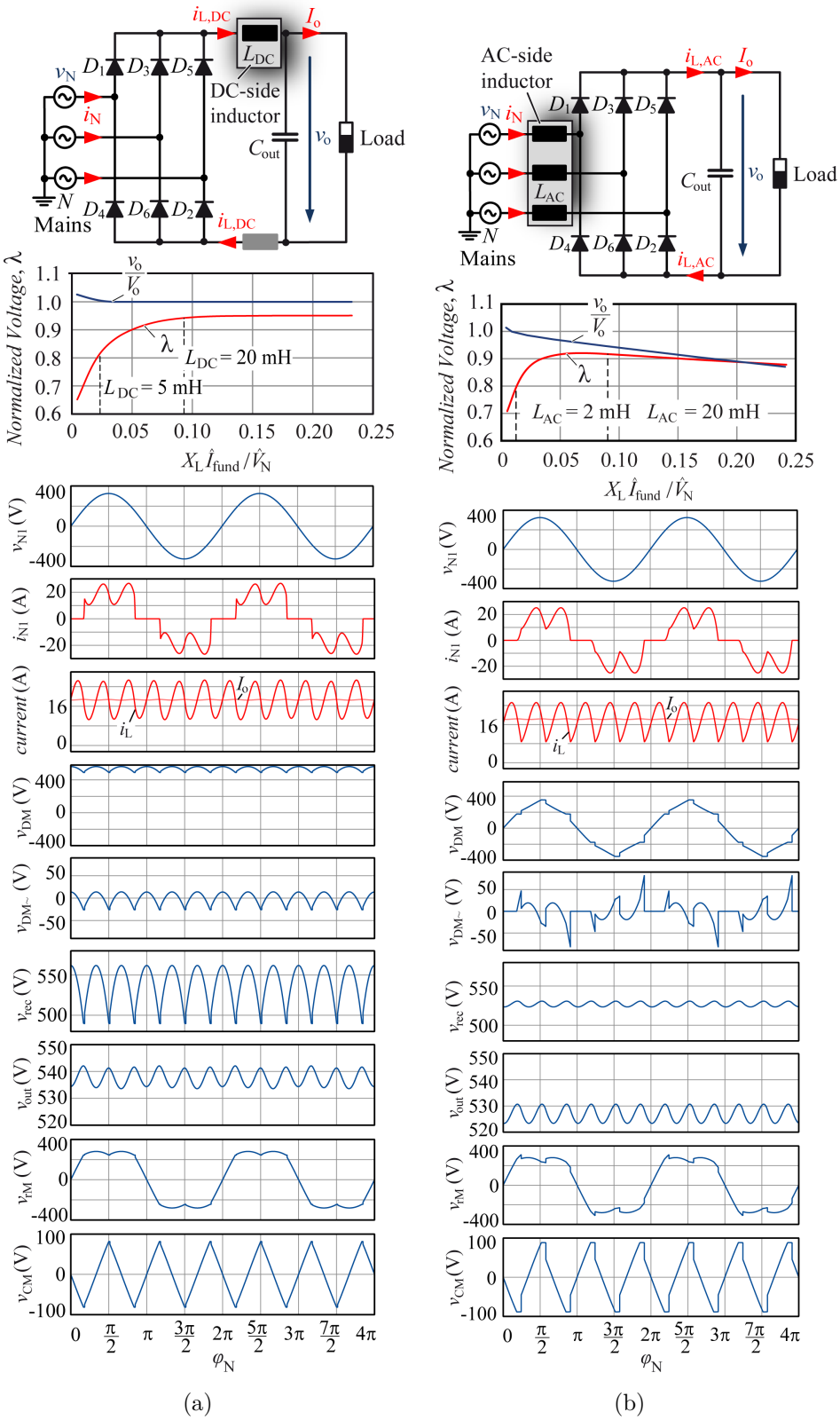


Fig. 3.2: Implementation, output voltage v_o and power factor λ characteristics of the passive three-phase rectifier topology (as illustrated in [18]) with (a) three AC-side located inductors and (b) one single DC side smoothing inductor.

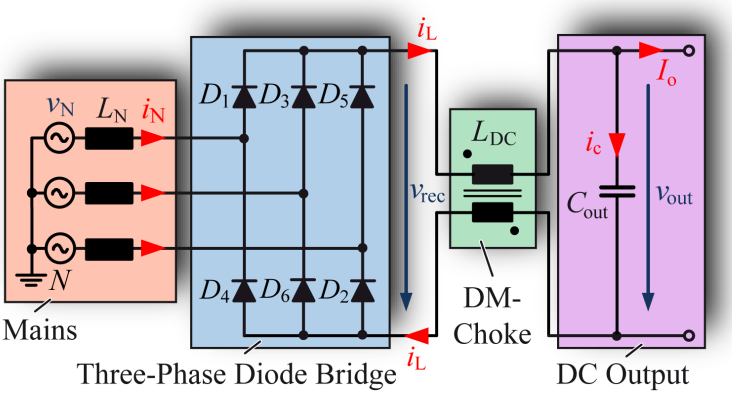


Fig. 3.3: A passive three-phase rectifier with DC-side smoothing inductance (implemented here as differnetial-mode choke) and output capacitor. L_{DC} here is denoted to the total effective inductance value.

(differential-mode (DM)) choke L_{DC} limiting the 300 Hz inductor current ripple and an output voltage capacitor C_o, providing a low ripple output voltage V_o and acting commonly as a DC-link.
Finally, it can be concluded that a passive three-phase rectifier with DC-side output filter comprises the following **advantages**

- high efficiency,
- widely used in industry,
- low cost, robust and simple,
- fixed output voltage according to mains situation
- and frequency of output common-mode voltage $v_{CM,k} = 3kf_N$

and **drawbacks**

- no output voltage control,
- minimum $THD_{i,min} = 31\,\%$,
- and maximum power factor $\lambda = 95.5\,\%$.

The following sections will give a very specific look (concluding calculations, simulation results and measurement results) for different prospects, states and issues that can emerge for such a rectifier topology.

3.2 Continuous Conduction Mode

The term "continuous conduction mode" (CCM) is used typically referring to the state of the rectifier's inductor current. For a passive three-phase rectifier, CCM is applicable if the DC-side smoothing inductor current i_L is permanently of positive value (> 0) during a whole period $[0 \ldots 2\pi]$. The so called "discontinuous conduction mode" (DCM) typically shows at least one interval where the current of the

DC inductor equals zero which is in general evoked due to blocking diodes of the circuit. The CCM to DCM boundary can hence be determined if the output current of the system equals the maximum peak current of the smoothing inductance ($I_\mathrm{o} = \hat{I}_\mathrm{L,AC}$).
Before a detailed investigation of the different modes is performed, the following section is briefly going to discuss, compare and try to quantify three different mathematical approaches ("fourier coefficient-theory", "sector-by-sector description" and "approximation of the DC-side smoothing inductance current i_L"). The derived equations are required for proper design of the passive three-phase rectifier and applicable for upcoming examinations. A set of basic equations is postulated which is also required and useful in order to properly specify the optional active rectifier upgrade for a B6 bridge which is going to be discussed in chapter 4.

3.2.1 Mathematical Investigation Strategies

In order to give a closed mathematical description of the passive three-phase rectifier system for voltage and current waveforms different promising analysis methods are possible. The difference between these methods regarding mathematical accuracy is discussed while different important quantities characterizing B6 rectifiers are presented.

Fourier Coefficients

In general, fourier series (applying fourier coefficients) can be used to describe a periodic signal utilizing the sum of sets of sinusoidal functions (valid for all values of φ_N ($\varphi_\mathrm{N} \in [-\infty \ldots \infty]$)). According to Fourier-theory, coefficients $\underline{c}_\mathrm{k}$ can be calculated using

$$\underline{c}_k = \frac{1}{2\pi}\int_0^{2\pi} f\left(\varphi_\mathrm{N}\right) e^{-jk\varphi_\mathrm{N}}\,\mathrm{d}\varphi_\mathrm{N} = a_k + jb_k \tag{3.7}$$

whereby k denotes a continuous index representing all multiples of the fundamental frequency. The analog is expressed by the sum of fundamental and harmonics (k) and the DC level (c_0 at $k = 0$, $c_0 = a_0$ and $b_0 = 0$)

$$f\left(\varphi_\mathrm{N}\right) = c_0 + \sum_{k=1}^{\infty} \frac{\left|\underline{c}_k\right|}{2} \sin\left(k\varphi_\mathrm{N}\right) \tag{3.8}$$

Applying these equations for obtaining output voltages of the positive and negative busbar of the passive rectifier ($v_\mathrm{pos} = \max\left(v_\mathrm{Ni}\right)$ and $v_\mathrm{neg} = \min\left(v_\mathrm{Ni}\right)$) and the third harmonic voltage v_h3 (as discussed in chapter 4, e.g. **Fig. 4.2**), the respective signals finally calculate to

$$v_\mathrm{pos}\left(\varphi_\mathrm{N}\right) = \frac{3\sqrt{3}\hat{V}_\mathrm{N}}{\pi}\left(\frac{1}{2} + \sum_{k=1,2,3,\ldots}^{\infty} \frac{\left(-1\right)^{k+1}}{\left(3k\right)^2 - 1}\cos\left(3k\varphi_\mathrm{N}\right)\right)$$

$$v_\mathrm{neg}\left(\varphi_\mathrm{N}\right) = \frac{3\sqrt{3}\hat{V}_\mathrm{N}}{\pi}\left(-\frac{1}{2} + \sum_{k=1,2,3,\ldots}^{\infty} \frac{1}{\left(3k\right)^2 - 1}\cos\left(3k\varphi_\mathrm{N}\right)\right)$$

$$v_{\mathrm{h3}}\left(\varphi_{\mathrm{N}}\right) = -\frac{3\sqrt{3}\hat{V}_{\mathrm{N}}}{\pi}\left(\sum_{k=1,3,5,\ldots}^{\infty}\frac{2}{(3k)^2-1}\cos\left(3k\varphi_{\mathrm{N}}\right)\right). \tag{3.9}$$

The rectifier output voltage v_{rec} can now easily be calculated by $v_{\mathrm{pos}} - v_{\mathrm{neg}}$ and hence yields

$$v_{\mathrm{rec}}\left(\varphi_{\mathrm{N}}\right) = \frac{3\sqrt{3}\hat{V}_{\mathrm{N}}}{\pi}\left(1-\sum_{k=1,2,3,\ldots}^{\infty}\frac{2}{(6k)^2-1}\cos\left(6k\varphi_{\mathrm{N}}\right)\right). \tag{3.10}$$

Taking a closer look at the assessed equations it can be seen that the voltages v_{pos}, v_{neg} and v_{h3} show only third order harmonics whereas v_{rec} is defined by multiples of sixth order spectral components. It can be assumed that i_{L} is also showing this dominant sixth order harmonic which has to be compensated by the current injection network.
The mean value of the output voltage V_{o} of the system for balanced input voltages results in

$$V_{\mathrm{o}} = \frac{1}{2\pi}\int_0^{2\pi} v_{\mathrm{pos}}\,\mathrm{d}\varphi_{\mathrm{N}} - \frac{1}{2\pi}\int_0^{2\pi} v_{\mathrm{neg}}\,\mathrm{d}\varphi_{\mathrm{N}} = \frac{3\sqrt{3}}{\pi}\hat{V}_{\mathrm{N}}\,. \tag{3.11}$$

These equations allow to obtain the DC-side smoothing inductance voltage $v_{L_{\mathrm{DC}}} = v_{\mathrm{rec}} - V_{\mathrm{o}}$ and the output filter current i_{L} hence can be calculated by

$$i_{\mathrm{L}}\left(\varphi_{\mathrm{N}}\right) = \frac{1}{\omega_{\mathrm{N}}L_{\mathrm{DC}}}\int v_{L_{\mathrm{DC}}}\left(\varphi_{\mathrm{N}}\right)\mathrm{d}\varphi_{\mathrm{N}} \tag{3.12}$$

which finally leads to

$$i_{\mathrm{L}}\left(\varphi_{\mathrm{N}}\right) = I_{\mathrm{o}} - \frac{3\sqrt{3}\hat{V}_{\mathrm{N}}}{\pi\omega_{\mathrm{N}}L_{\mathrm{DC}}}\sum_{k}^{\infty}\frac{2}{(6k)^3-6k}\sin\left(6k\varphi_{\mathrm{N}}\right). \tag{3.13}$$

Thus, the output voltage ripple of C_{o}, which is defined by

$$v_{\mathrm{o,ac}}\left(\varphi_{\mathrm{N}}\right) = \frac{1}{\omega_{\mathrm{N}}C_{\mathrm{o}}}\int\left(i_{\mathrm{L}} - I_{\mathrm{o}}\right)\left(\varphi_{\mathrm{N}}\right)\mathrm{d}\varphi_{\mathrm{N}}\,, \tag{3.14}$$

for ideally smoothed output current I_{o} is characterised by the current ripple in L_{DC} and computes to

$$v_{\mathrm{o,ac}}\left(\varphi_{\mathrm{N}}\right) = \frac{3\sqrt{3}\hat{V}_{\mathrm{N}}}{\pi\omega_{\mathrm{N}}^2L_{\mathrm{DC}}C_{\mathrm{o}}}\sum_{k}^{\infty}\frac{2}{(6k)^4-(6k)^2}\cos\left(6k\varphi_{\mathrm{N}}\right). \tag{3.15}$$

The rectifiers output voltage can now be described by

$$v_{\mathrm{o}}\left(\varphi_{\mathrm{N}}\right) = V_{\mathrm{o}} + v_{\mathrm{o,ac}}\left(\varphi_{\mathrm{N}}\right). \tag{3.16}$$

The input currents i_{Ni} are constituted by shapes of i_{L}. Evaluating the converging values of the appropriate sum-function after integrating the squared value of i_{Ni},

the input RMS currents values can be finally analytically determined – after some calculation effort – to

$$I_{\mathrm{Ni,rms}} = \sqrt{\frac{2}{3}I_{\mathrm{o}}^2 + \left(\frac{\hat{V}_{\mathrm{N}}}{\pi\omega_{\mathrm{N}}L_{\mathrm{DC}}}\right)^2 \left(\frac{7}{6}\pi^2 + \frac{9\sqrt{3}}{2}\pi - 36\right)}\,. \tag{3.17}$$

The RMS value of the input current's fundamental may be evaluated using

$$c_1 = \frac{1}{\sqrt{2}}\left|\frac{1}{2\pi}\int_0^{2\pi} f\left(\varphi_{\mathrm{N}}\right) e^{-j\varphi_{\mathrm{N}}}\,\mathrm{d}\varphi_{\mathrm{N}}\right| \tag{3.18}$$

which finally yields

$$I_{\mathrm{Ni,fund,rms}} = \sqrt{\frac{6}{\pi^2}I_{\mathrm{o}}^2 + \frac{2}{\pi^2}\left(\frac{3\sqrt{3}\hat{V}_{\mathrm{N}}}{\pi\omega_{\mathrm{N}}L_{\mathrm{DC}}}\right)^2 \left(\frac{\pi}{4} - \sqrt{3} + \frac{\pi^2}{6\sqrt{3}}\right)^2}\,. \tag{3.19}$$

The total harmonic distortion ($\mathrm{THD_i}$) of the passive B6 bridge then computes to

$$\mathrm{THD_i} = \sqrt{\frac{I_{\mathrm{o}}^2\left(\frac{2}{3} - \frac{6}{\pi^2}\right) + \left(\frac{\hat{V}_{\mathrm{N}}}{\pi\omega_{\mathrm{N}}L_{\mathrm{DC}}}\right)^2 \left(\frac{2}{3}\pi^2 + 3\sqrt{3}\pi - \frac{171}{8} + 27\sqrt{3}\frac{1}{\pi} - 162\frac{1}{\pi^2}\right)}{\frac{6}{\pi^2}I_{\mathrm{o}}^2 + \left(\frac{\hat{V}_{\mathrm{N}}}{\pi\omega_{\mathrm{N}}L_{\mathrm{DC}}}\right)^2 \left(\frac{1}{2}\pi^2 + \frac{3\sqrt{3}}{2}\pi - \frac{117}{8} - 27\sqrt{3}\frac{1}{\pi} + 162\frac{1}{\pi^2}\right)}} \tag{3.20}$$

using **Eq. 3.3**. **Eq. 3.20**, is only valid as long as continuous conduction mode of the rectifier is applicable. The CCM to DCM transition will be discussed in section 3.3.

A major design issue for a B6 rectifier is the selection of the DC-side smoothing inductance L_{DC}. On the one hand a large value is preferred to minimize the input current distortions ($\mathrm{THD_i}$). On the other hand, a large inductance consequently leads to an increased inductor volume ($V_{L_{\mathrm{DC}}}$). Nevertheless a specific $\mathrm{THD_i}$ is required to fulfill the IEEE standards for passive diode bridge rectifier applications. To guarantee a specific $\mathrm{THD_i}$ (for a required nominal power), the DC-side smoothing inductor L_{DC} has to be chosen accordingly. The inductance value is hence located as close to the maximum IEEE standard limit for $\mathrm{THD_i}$ to minimize the volume (and hence cost of the total system). As can be seen from **Eq. 3.20**, a dependency between L_{DC} and $\mathrm{THD_i}$ is already given and therefore, the equation just needs to be reorganized. The DC-side inductance can be written as

$$L_{\mathrm{DC}} = \frac{\hat{V}_{\mathrm{N}}^2}{\omega_{\mathrm{N}}P_{\mathrm{N}}}\frac{3}{\pi}\cdot\ldots$$
$$\cdot\sqrt{\frac{\frac{\pi^2}{3} + \frac{3\sqrt{3}\pi}{2} - \frac{171}{16} + \frac{27\sqrt{3}}{2\pi} - \frac{81}{\pi^2} + \mathrm{THD_i^2}\left(-\frac{\pi^2}{4} - \frac{3\sqrt{3}\pi}{4} + \frac{117}{16} + \frac{27\sqrt{3}}{2\pi} - \frac{81}{\pi^2}\right)}{1 + \mathrm{THD_i^2} - \left(\frac{\pi}{3}\right)^2}}\,. \tag{3.21}$$

The $\mathrm{THD_i}$ in practical systems usually shows values between $0.31\ldots0.6$, which results in $0.1\ldots0.36$ for $\mathrm{THD_i^2}$. Therefore, comparing both terms of the numerator of **Eq. 3.21**, the following simplification

$$\frac{\pi^2}{3}+\frac{3\sqrt{3}\pi}{2}-\frac{171}{16}+\frac{27\sqrt{3}}{2\pi}-\frac{81}{\pi^2}\gg \mathrm{THD_i^2}\left(-\frac{\pi^2}{4}-\frac{3\sqrt{3}\pi}{4}+\frac{117}{16}+\frac{27\sqrt{3}}{2\pi}-\frac{81}{\pi^2}\right) \tag{3.22}$$

is applicable. With this L_{DC} finally can be determined by

$$L_{\mathrm{DC}}=\frac{\hat{V}_{\mathrm{N}}^2}{\omega_{\mathrm{N}}P_{\mathrm{o}}}\frac{3}{\pi}\sqrt{\frac{\frac{\pi^2}{3}+\frac{3\sqrt{3}\pi}{2}-\frac{171}{16}+\frac{27\sqrt{3}}{2\pi}-\frac{81}{\pi^2}}{\mathrm{THD_i^2}-\mathrm{THD_{i,min}^2}}}. \tag{3.23}$$

According to **Eq. 3.2** the power factor λ can be calculated to

$$\lambda=\frac{1}{\sqrt{\left(\frac{\pi}{3}\right)^2+\left(\frac{\hat{V}_{\mathrm{N}}}{\omega_{\mathrm{N}}L_{\mathrm{DC}}I_{\mathrm{o}}}\right)^2\left(\frac{7}{36}\pi^2+\frac{3\sqrt{3}}{4}\pi-6\right)}}. \tag{3.24}$$

Remark: These analytical evaluations are only valid for CCM of a B6 rectifier.

Sector by Sector Description

One of the easiest ways to describe voltage and current waveforms of a power electronic circuit is "sector by sector" evaluation. As the name already indicates, voltage and current waveforms are calculated by merely considering a specific sector (e.g. $\varphi_{\mathrm{N}}\in\left[0\ldots\frac{\pi}{3}\right]$) of the signal. The major advantage of this method is that the mathematical description typically shows a very low grade of complexity for a simplified model of the rectifier (neglecting parasitic components and effects etc.). As all signals show an (at least) 2π-periodicity, manageable calculation effort has therefore be taken into account which (in general) does not require high sophisticated mathematical software to achieve utilizable results. The voltage signals of the rectifier to be analyzed ($v_{\mathrm{pos}}=\max\left(v_{\mathrm{Ni}}\right)$, $v_{\mathrm{neg}}=\min\left(v_{\mathrm{Ni}}\right)$ and $v_{\mathrm{h3}}=-v_{\mathrm{pos}}-v_{\mathrm{neg}}$) for the sector $\varphi_{\mathrm{N}}\in\left[0\ldots\frac{\pi}{3}\right]$ are given by

$$\begin{aligned} v_{\mathrm{pos}} &= \hat{V}_{\mathrm{N}}\cos\left(\varphi_{\mathrm{N}}\right)\\ v_{\mathrm{h3}} &= \hat{V}_{\mathrm{N}}\cos\left(\varphi_{\mathrm{N}}-\frac{2\pi}{3}\right)\\ v_{\mathrm{neg}} &= \hat{V}_{\mathrm{N}}\cos\left(\varphi_{\mathrm{N}}-\frac{4\pi}{3}\right). \end{aligned} \tag{3.25}$$

The instantaneous diode bridge output voltage can be described by

$$v_{\mathrm{rec}}=-\sqrt{3}\hat{V}_{\mathrm{N}}\sin\left(\varphi_{\mathrm{N}}-\frac{2\pi}{3}\right) \tag{3.26}$$

and the mean output voltage of the system for one mains period (2π) can hence be assessed by

$$V_{\mathrm{o}}=\frac{3\sqrt{3}\hat{V}_{\mathrm{N}}}{\pi} \tag{3.27}$$

which perfectly equals the determined output voltage V_o considering "fourier series" approach. The DC-side smoothing inductor current i_L computes to

$$i_\mathrm{L} = I_\mathrm{o} + \frac{3\sqrt{3}\hat{V}_\mathrm{N}}{\omega_\mathrm{N} L_\mathrm{DC}} \left(\frac{1}{6} + \frac{1}{3} \cos\left(\varphi_\mathrm{N} - \frac{2\pi}{3}\right) - \frac{1}{\pi}\varphi_\mathrm{N} \right) \tag{3.28}$$

and the resulting instantaneous output voltage ripple computes to

$$\begin{aligned} v_\mathrm{o,ac} = \frac{3\sqrt{3}\hat{V}_\mathrm{N}}{2\omega_\mathrm{N}^2 L_\mathrm{DC} C_\mathrm{o}} \Bigg(& \varphi_\mathrm{N}^2 + \frac{1}{3}\varphi_\mathrm{N} + \ldots \\ & \ldots + \frac{2}{3}\sin\left(\varphi_\mathrm{N} - \frac{2\pi}{3}\right) - \left(\alpha_\mathrm{C}^2 + \frac{1}{3}\alpha_\mathrm{C} + \frac{2}{\pi}\right) \Bigg) \end{aligned} \tag{3.29}$$

where α_C denotes the angle where $V_\mathrm{o} = v_\mathrm{rec}$, and hence, $v_\mathrm{o}(\varphi_\mathrm{N}) = V_\mathrm{o}$ is valid. The maximum value of i_L ($i_\mathrm{L,max}$) is also located at this specific time instant α_C. α_C is determined by

$$\alpha_\mathrm{C} = -\frac{\pi}{3} + \arcsin\left(\frac{3}{\pi}\right) . \tag{3.30}$$

Similar to the "fourier series" approach, the input currents i_Ni are assembled by fractions of i_L. Finding the squared root of integrated squared shapes of i_L over one mains period (2π) leads to an input current rms value of

$$I_\mathrm{Ni,rms} = \sqrt{\frac{2}{3} I_\mathrm{o}^2 + \left(\frac{\hat{V}_\mathrm{N}}{\pi\omega_\mathrm{N} L_\mathrm{DC}}\right)^2 \left(\frac{7}{6}\pi^2 + \frac{9\sqrt{3}}{2}\pi - 36\right)} \tag{3.31}$$

with a fundamental mains current rms of

$$I_\mathrm{Ni,fund,rms} = \sqrt{\frac{6}{\pi^2} I_\mathrm{o}^2 + \frac{2}{\pi^2}\left(\frac{3\sqrt{3}\hat{V}_\mathrm{N}}{\pi\omega_\mathrm{N} L_\mathrm{DC}}\right)^2 \left(\frac{\pi}{4} - \sqrt{3} + \frac{\pi^2}{6\sqrt{3}}\right)^2} . \tag{3.32}$$

It has to be noted, that results from "fourier series" signal evaluation of course resemble those of "sector-by-sector" analysis. Hence, analytical forms of $\mathrm{THD_i}$ and dimensioning of DC-side inductance can also be expected to be of same size and/or value.

Approximation of i_L

The last approach for analysing B6 rectifiers tries to combine both previously discussed investigation strategies ("fourier series" and "sector-by-sector"). On the one hand, the typical section-by-section analysis may be applied. On the other hand, the DC-side smoothing inductor current i_L can be rewritten as an approximation of the fourier series results (which merely considers the fundamental component $\sin(6\varphi_N)$). As proposed in [22] and advantageously exploit previously made assumptions, the output inductor current i_L can be written as

$$i_\mathrm{L} = I_\mathrm{o} + \hat{I}_\mathrm{L,ac} \sin(6\varphi_N) \tag{3.33}$$

TABLE 3.1: Comparison of main quantities of B6 rectifier systems applying different investigation strategies including "fourier series" (FS), "sector by sector evaluation" (SbS) or simple "approximation of i_L" (Approx). Numerical evaluation of $I_\mathrm{Ni,rms}$, $I_\mathrm{Ni,fund,rms}$ and $\mathrm{THD_i}$ has been performed at $V_\mathrm{N,rms} = 230\,\mathrm{V}$, $f_\mathrm{N} = 50\,\mathrm{Hz}$, $P_\mathrm{o} = 10\,\mathrm{kW}$, $L_\mathrm{DC} = 2.25\,\mathrm{mH}$. L_DC has been calculated for $V_\mathrm{N,rms} = 230\,\mathrm{V}$, $f_\mathrm{N} = 50\,\mathrm{Hz}$, $P_\mathrm{o} = 10\,\mathrm{kW}$ and $\mathrm{THD_i} = 40\,\%$.

Comparison of Results			
	FS	SbS	Approx
$I_\mathrm{Ni,rms}$ (A)	15.752	15.752	15.737
$I_\mathrm{Ni,fund,rms}$ (A)	14.530	14.530	14.525
$\mathrm{THD_i}$ (%)	41.943	41.943	41.696
L_DC (mH)	2.507	2.507	2.485

(neglecting all higher order harmonics beyond order of 6). The peak value of the current ripple can easily be computed via

$$\hat{I}_\mathrm{L,ac} = \frac{1}{\omega_\mathrm{N} L_\mathrm{DC}} \int_{-\arccos\left(\frac{3}{\pi}\right)}^{\arccos\left(\frac{3}{\pi}\right)} \left(v_\mathrm{rec}\left(\varphi_\mathrm{N}\right) - V_\mathrm{o}\right)\left(\varphi_\mathrm{N}\right) \mathrm{d}\varphi_\mathrm{N} \tag{3.34}$$

which finally leads to

$$\hat{I}_\mathrm{L,ac} = \frac{3\sqrt{3}\hat{V}_\mathrm{N}}{\pi\omega_N L_\mathrm{DC}} \left[\sqrt{\left(\frac{\pi}{3}\right)^2 - 1} - \arccos\left(\frac{3}{\pi}\right)\right]. \tag{3.35}$$

The rms value of the AC-side mains currents then results in

$$I_\mathrm{Ni,rms} = \sqrt{\frac{2}{3} I_\mathrm{o}^2 + \frac{1}{3}\hat{I}_\mathrm{L,ac}^2} \tag{3.36}$$

and the fundamental component of the input currents can be calculated to

$$I_\mathrm{Ni,fund,rms} = \frac{\sqrt{6}}{35\pi}\sqrt{\left(35 I_\mathrm{o}\right)^2 + \left(6\hat{I}_\mathrm{L,ac}\right)^2}. \tag{3.37}$$

Total harmonic distortion of mains currents yield

$$\mathrm{THD_i} = \sqrt{\frac{\left(\frac{2}{3} - \frac{6}{\pi^2}\right) I_\mathrm{o}^2 + \hat{I}_\mathrm{L,ac}^2\left(\frac{1}{3} - 6\left(\frac{6}{35\pi}\right)^2\right)}{\frac{6}{\pi^2} I_\mathrm{o}^2 + 6\hat{I}_\mathrm{L,ac}^2\left(\frac{6}{35\pi}\right)^2}}. \tag{3.38}$$

Finally, the rectifiers design parameter L_DC computes to

$$L_\mathrm{DC} = \frac{\hat{V}_\mathrm{N}^2}{\omega_\mathrm{N} P_\mathrm{o}} \frac{3}{\pi} \sqrt{\frac{\frac{9}{2} - \left(\frac{54}{35\pi}\right)^2\left(1 + \mathrm{THD_i^2}\right)}{1 + \mathrm{THD_i^2} - \left(\frac{\pi}{3}\right)^2}} \left[\sqrt{\left(\frac{\pi}{3}\right)^2 - 1} - \arccos\left(\frac{3}{\pi}\right)\right]. \tag{3.39}$$

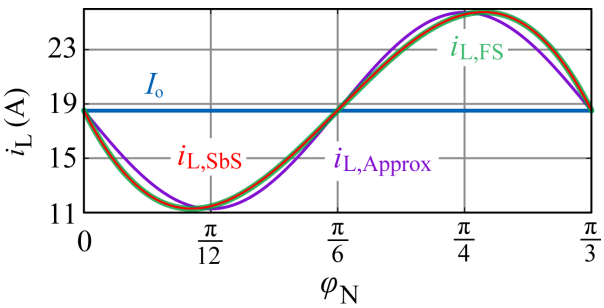


Fig. 3.4: DC-side smoothing inductor current i_L considering "sector by sector" ($i_{L,SbS}$), "fourier series" ($i_{L,FS}$) and "current approximation" ($i_{L,Approx}$) for 10 kW output power (P_o).

Comparison of Results

In order to compare the previously discussed results, analytically derived formulas for quantities as input current rms ($I_{Ni,rms}$), input currents fundamental rms ($I_{Ni,fund,rms}$), total harmonic distortion (THD_i) and DC-side smoothing inductance (L_{DC}) have been evaluated numerically. As can be seen from **TABLE 3.1** there is no loss of accuracy while choosing either "fourier series" or "sector by sector" signal evaluation. A minor deviation/loss of information can be observed if the approximation of i_L is applied (compared to e.g. "sector by sector" analysis). The relative error $I_{Ni,rms}$ and $I_{Ni,fund,rms}$ amounts to only 0.1 % and 0.04 %, respectively. For THD_i and L_{DC} a mismatch of 0.59 % and 0.87 % can be noticed, respectively. It can hence be concluded that the achieved results of all three applied mathematical instruments are totally valid and merely varying in complexity. Depending on accuracy, there is not much difference for numerically evaluated values. Only the current waveform of the approximated DC-side smoothing inductance current i_L slightly differs, compared to evaluated currents regarding "sector by sector" or "fourier series" computation (cf. **Fig. 3.4**). It can be observed that data extracted out of "fourier series" and "sector by sector" are perfectly aligned from a graphical point of view. "Current approximation" shows a purely sinusoidal signal characteristic and is hence missing its higher harmonics (and therefore some information). It is slightly diverging compared to exact evaluated waveforms. It should be noted that independent of the mathematical approach, all inductor currents ($i_{L,FS}$, $i_{L,SbS}$ and $i_{L,Approx}$) show identical zero crossings ($i_L - I_o = 0\,\mathrm{A}$ for a specific sector $\left(\varphi_N \in \left[0 \ldots \frac{\pi}{3}\right]\right)$).

3.2.2 Output voltage

In this section the generation of the output voltage of the rectifier system is briefly discussed. For this section commutation effects and AC-side mains grid inductance are considered. The B6 output voltage v_{rec} is basically defined by

$$v_{rec} = \max\left(v_{N1-3}\right) - \min\left(v_{N1-3}\right). \tag{3.40}$$

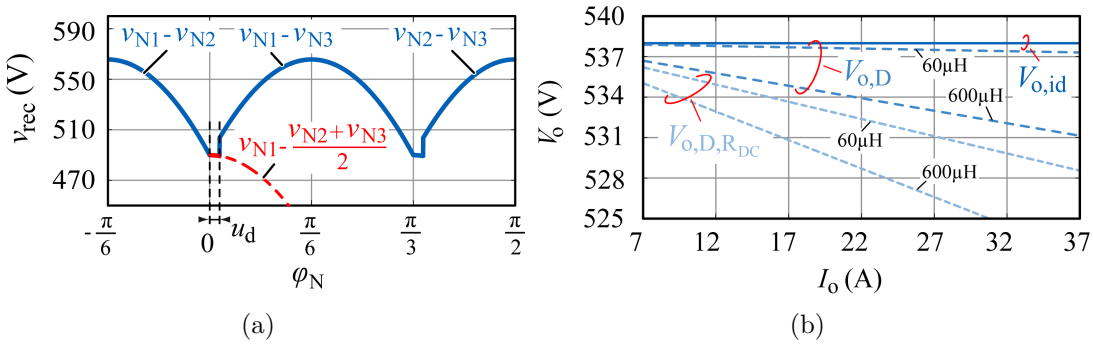


Fig. 3.5: (a) Rectifier output voltage v_{rec} for different sectors of φ_{N}, considering AC-side current commutation interval u_{d} for an assumed AC-side grid inductance of $L_{\mathrm{N}} = 60\,\mu\mathrm{H}$ and an output power of 10 kW. (b) Output voltage drops according to Dällenbach ($V_{\mathrm{o,D}}$) and parasitic resistance of DC-side smoothing coil ($V_{\mathrm{o,D,R_{DC}}}$) for $L_{\mathrm{N}} = 60\,\mu\mathrm{H}/600\,\mu\mathrm{H}$ compared to the ideally calculated output voltage $V_{\mathrm{o,id}}$.

This is not true during time intervals where the current commutation between two phases takes place. All occurring current commutations are quantified as follows:

- $\varphi_{\mathrm{N}} = \pi/3$, conducting diodes: D_1, D_2, current commutation: $D_1 \rightarrow D_3$
- $\varphi_{\mathrm{N}} = 2\pi/3$, conducting diodes: D_2, D_3, current commutation: $D_2 \rightarrow D_4$
- $\varphi_{\mathrm{N}} = \pi$, conducting diodes: D_3, D_4, current commutation: $D_3 \rightarrow D_5$
- $\varphi_{\mathrm{N}} = 4\pi/3$, conducting diodes: D_4, D_5, current commutation: $D_4 \rightarrow D_6$
- $\varphi_{\mathrm{N}} = 5\pi/3$, conducting diodes: D_5, D_6, current commutation: $D_5 \rightarrow D_1$
- $\varphi_{\mathrm{N}} = 2\pi$, conducting diodes: D_6, D_1, current commutation: $D_6 \rightarrow D_2$

During these intervals u_{d} where the current commutation occurs, both diodes (e.g. D_1 and D_3 for $\varphi_{\mathrm{N}} = \pi/3$) are conducting. Simultaneously, the applying voltage is defined by $v_{\mathrm{N1}} - v_{\mathrm{N2}}$ ($= v_{\mathrm{N12}}$), $i_{\mathrm{N1}} = I_{\mathrm{o}}$ and $i_{\mathrm{N2}} = 0\,\mathrm{A}$. If the commutation process is finished (for $\varphi_{\mathrm{N}} = \pi/3 + u_{\mathrm{d}}$) $i_{\mathrm{N1}} = 0\,\mathrm{A}$ and $i_{\mathrm{N2}} = I_{\mathrm{o}}$ is valid. Furthermore the following equations apply:

$$i_{\mathrm{N1}} + i_{\mathrm{N2}} = I_{\mathrm{o}}, \quad \frac{\mathrm{d}i_{\mathrm{N1}}}{\mathrm{d}t} + \frac{\mathrm{d}i_{\mathrm{N2}}}{\mathrm{d}t} = 0, \quad v_{\mathrm{N12}} + L_{\mathrm{N}}\left(\frac{\mathrm{d}i_{\mathrm{N2}}}{\mathrm{d}t} - \frac{\mathrm{d}i_{\mathrm{N1}}}{\mathrm{d}t}\right) = 0. \tag{3.41}$$

The mains current i_{N1} can be written as

$$i_{\mathrm{N1}} = \frac{1}{2L_{\mathrm{N}}}\int v_{\mathrm{N12}}\,\mathrm{d}\varphi_{\mathrm{N}}. \tag{3.42}$$

After determining the integration constant "$+C$" (at $\varphi_{\mathrm{N}} = \frac{\pi}{3}$, $i_{\mathrm{N1}} = I_{\mathrm{o}}$) the current i_{N1} results in

$$i_{\mathrm{N1}} = I_{\mathrm{o}} - \frac{\sqrt{3}\hat{V}_{\mathrm{N}}}{2\omega_{\mathrm{N}}L_{\mathrm{N}}}\left(1 - \sin\left(\varphi_{\mathrm{N}} + \frac{\pi}{6}\right)\right) \tag{3.43}$$

for the applied sector $\varphi_{\mathrm{N}} \in \left[\frac{\pi}{3} \ldots \frac{\pi}{3} + u_{\mathrm{d}}\right]$. The commutation interval u_{d} can furthermore be evaluated if i_{N1} is calculated at $\varphi_{\mathrm{N}} = \frac{\pi}{3} + u_{\mathrm{d}}$ ($i_{\mathrm{N1}} = 0$) which results

in

$$u_\mathrm{d} = \arccos\left(1 - \frac{2\omega_\mathrm{N} L_\mathrm{N} I_\mathrm{o}}{\sqrt{3}\hat{V}_\mathrm{N}}\right). \tag{3.44}$$

The interval u_d (cf., **Fig. 3.5(a)**) is dependent on the mains inductance L_N, the instantaneous output current I_o and mains voltage $\hat{V}_\mathrm{N}$. The rectifier output voltage v_rec during this interval is defined by

$$v_\mathrm{rec} = \frac{v_\mathrm{N1} + v_\mathrm{N2}}{2} - v_\mathrm{N3} \tag{3.45}$$

for the sector $\varphi_\mathrm{N} \in \left[\frac{\pi}{3} \ldots \frac{\pi}{3} + u_\mathrm{d}\right]$. The averaged output voltage V_o is dependent on the mains inductance value L_N and I_o and can be calculated by

$$\begin{aligned} V_\mathrm{o} = \frac{1}{\frac{\pi}{3}} \Bigg(& \int_0^{u_\mathrm{d}} \left[v_\mathrm{N1}(\varphi_\mathrm{N}) - \frac{v_\mathrm{N2}(\varphi_\mathrm{N}) + v_\mathrm{N3}(\varphi_\mathrm{N})}{2} \right] \mathrm{d}\varphi_\mathrm{N} + \ldots \\ & + \int_{u_\mathrm{d}}^{\frac{\pi}{3}} \left[v_\mathrm{N1}(\varphi_\mathrm{N}) - v_\mathrm{N3}(\varphi_\mathrm{N}) \right] \mathrm{d}\varphi_\mathrm{N} \Bigg). \end{aligned} \tag{3.46}$$

Only one of the six available sectors has to be considered due to the $\frac{\pi}{3}$-periodicity of v_rec. Evaluation of the determined integral leads to a commutation voltage drop of

$$V_\mathrm{o,D} = \frac{3\sqrt{3}\hat{V}_\mathrm{N}}{\pi}\left(1 - \frac{\omega_\mathrm{N} L_\mathrm{N} I_\mathrm{o}}{\sqrt{3}\hat{V}_\mathrm{N}}\right) \tag{3.47}$$

Furthermore, an additional voltage drop at the output appears due to the appearing series resistance of the implemented inductor winding resistance R_DC. The output voltage hence eventually is defined by

$$V_{\mathrm{o,D},R_\mathrm{DC}} = \frac{3\sqrt{3}\hat{V}_\mathrm{N}}{\pi}\left(1 - \frac{\omega_\mathrm{N} L_\mathrm{N} I_\mathrm{o}}{\sqrt{3}\hat{V}_\mathrm{N}}\right) - \frac{\pi}{3} R_\mathrm{DC} I_\mathrm{o}. \tag{3.48}$$

Fig. 3.5(b) illustrates the discussed issues of V_o (during CCM) for different loads and mains impedance values with

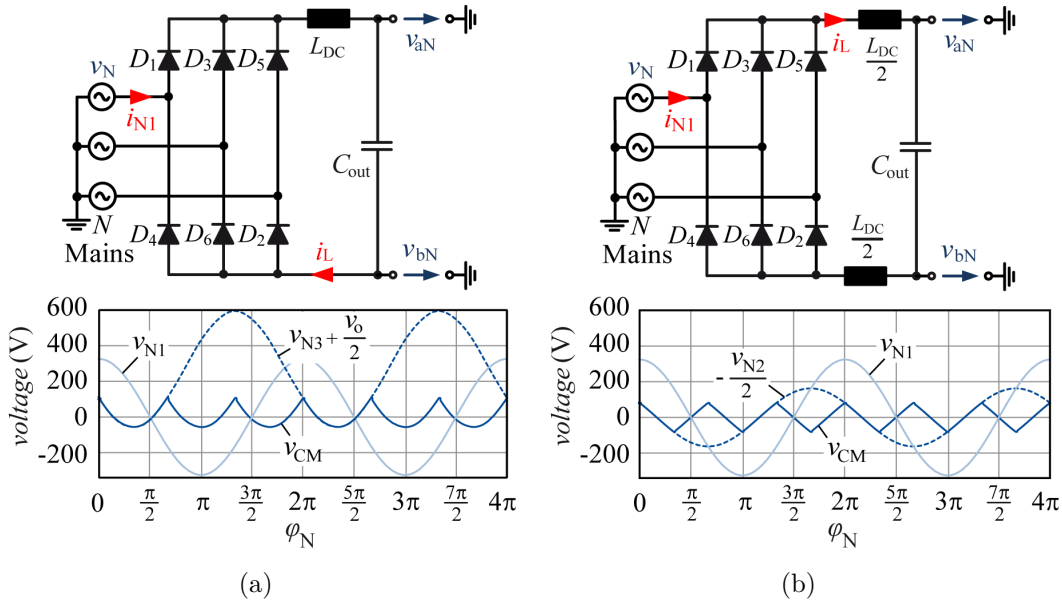
$$V_\mathrm{o,id} = \frac{3\sqrt{3}}{\pi}\hat{V}_\mathrm{N}. \tag{3.49}$$

For sake of simplicity the B6 diodes forward voltage drops have been neglected for these calculations.

3.2.3 Common-Mode Voltage

In order to quantify the common mode output voltage of the system, the positive output is marked as "a" and the negative output as "b". The common mode output voltage v_CM is then defined by

$$v_\mathrm{CM} = \frac{v_\mathrm{aN} + v_\mathrm{bN}}{2}. \tag{3.50}$$



(a) (b)

Fig. 3.6: v_{CM} of a three-phase passive rectifier with (a) single (positive output bus) or (b) separated (positive and negative output bus) DC-side output choke L_{DC}.

If a simple and standard DC-side choke is implemented (which is merely located between positive output of B6 and "a"), v_{aN} and v_{bN} compute to

$$v_{aN} = v_{N1} - v_{L_{DC}}, \quad v_{bN} = v_{N3} \tag{3.51}$$

for the specific sector $\varphi_N \in \left[0 \ldots \frac{\pi}{3}\right]$. The common mode voltage for this sector therefore results in

$$v_{CM} = \frac{-v_{N2} - v_{L_{DC}}}{2} = v_{N3} + \frac{V_o}{2}. \tag{3.52}$$

If the DC-side choke is separated into two inductors with $L_{DC}/2$ each (i.e. each output of the B6 contains one part of the inductor), the common-mode voltage results in

$$v_{CM} = \frac{v_{N1} + v_{N3} - \frac{v_{L_{DC}}}{2} + \frac{v_{L_{DC}}}{2}}{2} = -\frac{v_{N2}}{2}. \tag{3.53}$$

Fig. 3.6 illustrates the difference in the appearance of the common-mode voltage v_{CM} of the three-phase rectifier with a single DC-side choke (cf., **Fig. 3.6(a)** - L_{DC}) and a split choke assembly (cf., **Fig. 3.6(a)** - $L_{DC}/2$ located within each busbar). Both options result in an averaged common-mode voltage of zero.

$$v_{CM}(\varphi_N) = v_{N3}(\varphi_N) + \frac{V_o}{2} \qquad \varphi_N \in \left[0 \ldots \frac{\pi}{3}\right] \tag{3.54}$$

$$v_{CM,avg} = \frac{3}{\pi} \int_0^{\frac{\pi}{3}} \hat{V}_N \cdot \cos\left(\varphi_N - \frac{4\pi}{3}\right) \mathrm{d}\varphi_N - \frac{3\sqrt{3}}{2\pi} \hat{V}_N = 0\,\mathrm{V} \tag{3.55}$$

$$v_{CM}(\varphi_N) = -\frac{v_{N2}(\varphi_N)}{2} \qquad \varphi_N \in \left[0 \ldots \frac{\pi}{3}\right] \tag{3.56}$$

$$v_{\mathrm{CM,avg}} = \frac{3}{\pi}\int_{0}^{\frac{\pi}{3}} -\frac{\hat{V}_{\mathrm{N}}\cdot\cos\left(\varphi_{\mathrm{N}}-\frac{2\pi}{3}\right)}{2}\,\mathrm{d}\varphi_{\mathrm{N}} = 0\,\mathrm{V}. \tag{3.57}$$

In **Fig. 3.6(a)**, the negative output of the rectifier is directly and permanently clamped to one of the mains input phases (neglecting parasitic passives due to wiring, diode capacitance and on-state resistance) and hence results in the dominant waveform which resembles v_{neg} according to its characteristic.

3.3 Continuous/Discontinuous Conduction Mode Boundary

In general, the CCM/DCM boundary is defined as the state of a B6 rectifier where the amplitude of the 300 Hz current ripple

$$i_{\mathrm{L,ac}}(\varphi_{\mathrm{N}}) = -\frac{3\sqrt{3}\hat{V}_{\mathrm{N}}}{\pi\omega_{\mathrm{N}}L_{\mathrm{DC}}}\sum_{k=1}^{\infty}\frac{2}{(6k)^3-6k}\sin(6k\varphi_{\mathrm{N}}) \tag{3.58}$$

of the DC-side inductor ($\hat{I}_{\mathrm{L,ac}}$) equals the output load current (I_{o}). As discussed in one of the previous subsections, the difference between the ideal and real averaged voltage drop during the commutation process is negligibly small (due to small values of L_{N} and hence short commutation instant u_{d}) and not taken into account for further discussions.
As mentioned, the CCM to DCM boundary is located at $I_{\mathrm{o}} = \hat{I}_{\mathrm{L,ac}}$. $\hat{I}_{\mathrm{L,ac}}$ is defined according to the mains voltage situation, the output voltage and the designed inductance L_{DC}. The threshold power level between CCM and $\mathrm{DCM_I}$ ($P_{\mathrm{o,CCM/DCM_I}}$) of a B6 rectifier can be found at $i_{\mathrm{L,CCM}}(\varphi_{\mathrm{N}}) = 0\,\mathrm{A}$ which yields an appropriate output power level of

$$P_{\mathrm{o,CCM/DCM_I}} = \frac{3(3\hat{V}_{\mathrm{N}})^2}{\pi\omega_{\mathrm{N}}L_{\mathrm{DC}}}\left(\frac{1}{\pi}\arcsin\left(\frac{3}{\pi}\right)-\frac{1}{2}+\frac{1}{\pi}\sqrt{\left(\frac{\pi}{3}\right)^2-1}\right) \tag{3.59}$$

The derived formula is neglecting the DC-link voltage ripple ($C_{\mathrm{o}} \to \infty$). If a passive system for a rated output power of 10 kW and a DC-side smoothing inductance of 2.25 mH for an appropriate $\mathrm{THD_i}$ of 48 % is assumed, the CCM to $\mathrm{DCM_I}$ threshold computes to

$$P_{\mathrm{o,CCM/DCM_I}}\Big|_{L_{\mathrm{DC}}=2.25\,\mathrm{mH}} \approx 4\,\mathrm{kW}. \tag{3.60}$$

3.4 Discontinuous Conduction Mode

The following section briefly discusses the discontinuous conduction mode (DCM) of a B6 rectifier with DC-side located inductor. According to definition, the DCM

shows at least one interval in between a signals period where the current of the inductor equals zero.
As will be shown in upcoming subsections, the discontinuous conduction mode of the rectifier can be separated into two different states. The difference between those two discontinuous operation modes is defined by the input or DC-side smoothing inductance current characteristic.

- **state 1 -** $\mathrm{DCM_I}$**:** The rectifier output voltage v_{rec} and the DC-side inductance current i_{L} consist of four different sectors (I-IV) for $\mathrm{DCM_I}$.
- **state 2 -** $\mathrm{DCM_{II}}$**:** Considering $\mathrm{DCM_{II}}$ only two different sectors can be found anymore, which is defined due to the increased zero current gap and the hence missing commutation process of the passive diode bridge.

The boundary between these two discontinuous modes is characterized by

$$i_{\mathrm{L}}\left(\varphi_{\mathrm{N}} = \gamma = k\frac{\pi}{3}\right) = 0\mathrm{A} \qquad \text{for } k \in \mathbb{Z} \tag{3.61}$$

which leads to a specific output power value

$$\begin{aligned} P_{\mathrm{o,DCM_{I/II}}} =& \frac{3\sqrt{3}\hat{V}_{\mathrm{N}}V_{\mathrm{o}}}{\pi\omega_{\mathrm{N}}L_{\mathrm{DC}}}\left(\frac{V_{\mathrm{o}}}{\sqrt{3}\hat{V}_{\mathrm{N}}} - \frac{\sqrt{3}}{2} + \left(\frac{\pi}{3} - \alpha_{\mathrm{D}}\right)\sqrt{1 - \frac{1}{3}\left(\frac{V_{\mathrm{o}}}{\hat{V}_{\mathrm{N}}}\right)^2}\right) + \ldots \\ \ldots + & \frac{3V_{\mathrm{o}}^2}{\pi\omega_{\mathrm{N}}L_{\mathrm{DC}}}\left(\left(\frac{\pi}{3} - \alpha_{\mathrm{D}}\right)\alpha_{\mathrm{D}} - \frac{\left(\frac{\pi}{3}\right)^2 - \alpha_{\mathrm{D}}^2}{2}\right) \end{aligned} \tag{3.62}$$

which can be approximately calculated to 1.9 kW for a given DC-side smoothing inductor value of 2.25 mH, negligence of output voltage ripple ($C_{\mathrm{o}} \to \infty$) and $\alpha_{\mathrm{D}} = -\frac{\pi}{3} + \arcsin\left(\frac{V_{\mathrm{o}}}{\sqrt{3}\hat{V}_{\mathrm{N}}}\right)$. It has to be mentioned that $V_{\mathrm{o}} = \frac{3\sqrt{3}\hat{V}_{\mathrm{N}}}{\pi}$ is no longer valid for discontinuous conduction mode and has to be evaluated numerically considering **Eq. 3.61**. Obviously, the previous defined instant α_{C} is no longer valid, as V_{o} is deviating from $\frac{3\sqrt{3}V_{\mathrm{o}}}{\pi}$ for a specific output power P_{o} during DCM. Hence the time instant where $v_{\mathrm{rec}} = V_{\mathrm{o}}$ is defined by

$$\alpha_{\mathrm{D}} = -\frac{\pi}{3} + \arcsin\left(\frac{V_{\mathrm{o}}}{\sqrt{3}\hat{V}_{\mathrm{N}}}\right). \tag{3.63}$$

Furthermore, the commutation time $u_{\mathrm{d,DCM}}$ (announced in a previous section) for DCM equals the commutation time for CCM ($u_{\mathrm{d,CCM}}$).

3.4.1 DCM State 1 - $\mathrm{DCM_I}$

$\mathrm{DCM_I}$ shows considerably higher complexity compared to $\mathrm{DCM_{II}}$ as there are 4 different sections (I-IV) within one period (of the DC-side smoothing inductance current $i_{\mathrm{L,DCM_I}}$) which is defined e.g. from $\varphi_{\mathrm{N}} \in \left[0 \ldots \frac{\pi}{3}\right]$.
The first sector (sector I - $\mathrm{S_I}$) defines the commutation process of the input current

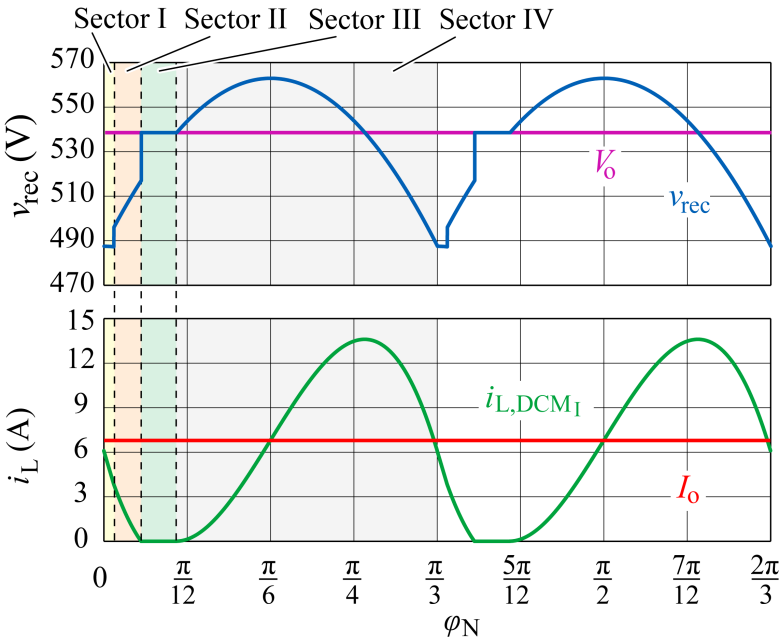


Fig. 3.7: Calculated DC-side smoothing inductor current i_{L,DCM_I}, rectifier voltage v_{rec}, output current and output voltage waveforms of the passive three-phase rectifier system for discontinuous conduction mode DCM_I ($V_o = 538.5\,V$ and $I_o = 6.56\,A$).

i_{Ni} between two different mains phases and is hence defined for the sector $\varphi_N \in [0 \ldots u_d]$. The DC-side current for this sector ($i_{L,DCM_I,S_I}(\varphi_N)$) calculates to

$$i_{L,DCM_I,S_I}(\varphi_N) = \frac{\sqrt{3}\hat{V}_N}{\omega_N L_{DC}} \left(\frac{1}{2} + \frac{\sqrt{3}}{2} \sin(\varphi_N) + \sqrt{1 - \frac{1}{3}\left(\frac{V_o}{\hat{V}_N}\right)^2} \right) - \ldots$$
$$\ldots - \frac{V_o}{\omega_N L_{DC}} \left(\frac{\pi}{3} + \varphi_N - \alpha_D \right). \tag{3.64}$$

For the rectifiers output voltage v_{rec} the defined voltage level

$$v_{rec} = v_{N1}(\varphi_N) - \frac{v_{N2}(\varphi_N) + v_{N3}(\varphi_N)}{2} \tag{3.65}$$

applies. The second sector (sector II - S_{II}) is defined for ($\varphi_N \in [u_d \ldots \gamma_D]$), whereas γ_D is that time instant where i_L reaches $0\,A$. The inductor current for this time fraction computes to

$$i_{L,DCM_I,S_{II}}(\varphi_N) = \frac{\sqrt{3}\hat{V}_N}{\omega_N L_{DC}} \left(\frac{1}{2} + \frac{\sqrt{3}}{2} \sin(\varphi_N) + \cos\left(\varphi_N - \frac{2\pi}{3}\right) - \ldots \right.$$
$$\ldots - \cos\left(u_d - \frac{2\pi}{3}\right) + \left. \sqrt{1 - \frac{1}{3}\left(\frac{V_o}{\hat{V}_N}\right)^2} \right) - \ldots \tag{3.66}$$
$$\ldots - \frac{V_o}{\omega_N L_{DC}} (\varphi_N - \alpha_D).$$

The output voltage of the B6 bridge (v_{rec}) during this time instant is defined by $v_{\mathrm{N1}} - v_{\mathrm{N3}}$. If $\varphi_{\mathrm{N}} = \gamma_{\mathrm{D}}$, all diodes of the rectifier are blocking. The DC-side inductor current for this sector (sector III - $\mathrm{S_{III}}$) hence yields

$$i_{\mathrm{L,DCM_I},S_{\mathrm{III}}}\left(\varphi_{\mathrm{N}}\right) = 0\,\mathrm{A} \tag{3.67}$$

and applies as long as $v_{\mathrm{N1}} - v_{\mathrm{N3}} < V_{\mathrm{o}}$ is valid. During this time the diode bridge output voltage v_{rec} equals the passive three-phase rectifier's output voltage V_{o}. If $v_{\mathrm{N1}} - v_{\mathrm{N3}} = V_{\mathrm{o}}$ (at time instant $\varphi_{\mathrm{N}} = \alpha_{\mathrm{D}}$), the appropriate diodes are starting to operate again (sector IV - $\mathrm{S_{IV}}$). The DC-side inductor current for this sector ($\varphi_{\mathrm{N}} \in \left[\alpha_{\mathrm{D}} \ldots \frac{\pi}{3}\right]$) calculates to

$$\begin{aligned} i_{\mathrm{L,DCM_I},S_{\mathrm{IV}}}\left(\varphi_{\mathrm{N}}\right) = \frac{\sqrt{3}\hat{V}_{\mathrm{N}}}{\omega_{\mathrm{N}} L_{\mathrm{DC}}} \left(\cos\left(\varphi_{\mathrm{N}} - \frac{2\pi}{3}\right) + \sqrt{1 - \frac{1}{3}\left(\frac{V_{\mathrm{o}}}{\hat{V}_{\mathrm{N}}}\right)^2} \right) - \ldots \\ \ldots - \frac{V_{\mathrm{o}}}{\omega_{\mathrm{N}} L_{\mathrm{DC}}} \left(\varphi_{\mathrm{N}} - \alpha_{\mathrm{D}}\right). \end{aligned} \tag{3.68}$$

Fig. 3.7 depicts two 60° intervals of the DC-side inductor current (considering all four previously discussed sections) for an output power of 3.5 kW. As can be observed, the DCM output voltage V_{o} is slightly increased compared to the output voltage in CCM ($\frac{3\sqrt{3}\hat{V}_{\mathrm{N}}}{\pi}$). Due to the already discussed subdivided current $i_{\mathrm{L,DCM_I},S_{\mathrm{I-IV}}}$, the averaged current $I_{\mathrm{o,DCM_I}}$ calculates to

$$\begin{aligned} I_{\mathrm{o,DCM,S1}} = \frac{9\hat{V}_{\mathrm{N}}}{2\pi\omega_{\mathrm{N}} L_{\mathrm{DC}}} \Bigg[1 - \cos\left(u_{\mathrm{d}}\right) + \left(\gamma_{\mathrm{D}} - u_{\mathrm{d}}\right)\sin\left(u_{\mathrm{d}}\right) \Bigg] - \ldots \\ \ldots - \frac{3V_{\mathrm{o}}}{\omega_{\mathrm{N}} L_{\mathrm{DC}}} \left[\left(\frac{\pi}{3} - \alpha_{\mathrm{D}}\right) \left(\frac{1}{2}\left(\frac{\pi}{3} - \alpha_{\mathrm{D}}\right) + \gamma_{\mathrm{D}} \right) + \frac{\gamma_{\mathrm{D}}^2}{2} \right] + \ldots \\ \ldots + \frac{3\sqrt{3}\hat{V}_{\mathrm{N}}}{\pi\omega_{\mathrm{N}} L_{\mathrm{DC}}} \Bigg[\sin\left(\gamma_{\mathrm{D}} - \frac{2\pi}{3}\right) - \sin\left(u_{\mathrm{d}} - \frac{2\pi}{3}\right) + \ldots \\ \ldots + \gamma_{\mathrm{D}} \left(\frac{1}{2} - \cos\left(u_{\mathrm{d}} - \frac{2\pi}{3}\right) + \sqrt{1 - \frac{1}{3}\left(\frac{V_{\mathrm{o}}}{\hat{V}_{\mathrm{N}}}\right)^2} \right) + \ldots \\ \ldots + u_{\mathrm{d}} \cos\left(u_{\mathrm{d}} - \frac{2\pi}{3}\right) - \frac{\sqrt{3}}{2} - \sin\left(\alpha_{\mathrm{D}} - \frac{2\pi}{3}\right) + \ldots \\ \ldots + \left(\frac{\pi}{3} - \alpha_{\mathrm{D}}\right) \sqrt{1 - \frac{1}{3}\left(\frac{V_{\mathrm{o}}}{\hat{V}_{\mathrm{N}}}\right)^2} \Bigg] \end{aligned} \tag{3.69}$$

3.4.2 DCM State 2 - $\mathrm{DCM_{II}}$

As previously mentioned, there is also a second operational state during discontinuous conduction mode ($\mathrm{DCM_{II}}$) that can be observed. For this second state, the DC-side smoothing inductor current reaches zero, before the mains currents initiate the upcoming commutation process. Hence, no commutation takes place, as

i_L is already zero. Therefore, only two different sectors are mandatory for $\mathrm{DCM_{II}}$. For the first sector ($\varphi_\mathrm{N} \in [\gamma_\mathrm{D} \ldots \alpha_\mathrm{D}]$), $i_{\mathrm{L,DCM_{II}},S_\mathrm{I}}$ is

$$i_{\mathrm{L,DCM_{II}},S_\mathrm{I}}\left(\varphi_\mathrm{N}\right) = 0\,\mathrm{A} \tag{3.70}$$

and hence all diodes are blocking. The second sector can be found at $\varphi_\mathrm{N} \in [\gamma_\mathrm{D} \ldots \alpha_\mathrm{D}]$. Similar to $\mathrm{DCM_I}$ (sector IV), the diodes are re-conducting again if $v_\mathrm{N1} - v_\mathrm{N3} \geq V_\mathrm{o}$ applies. The inductor current therefore calculates to

$$\begin{aligned} i_{\mathrm{L,DCM_{II}},S_\mathrm{II}}\left(\varphi_\mathrm{N}\right) = \frac{\sqrt{3}\hat{V}_\mathrm{N}}{\omega_\mathrm{N} L_\mathrm{DC}} \left(\cos\left(\varphi_\mathrm{N} - \frac{2\pi}{3}\right) + \sqrt{1 - \frac{1}{3}\left(\frac{V_\mathrm{o}}{\hat{V}_\mathrm{N}}\right)^2} \right) - \ldots \\ \ldots - \frac{V_\mathrm{o}}{\omega_\mathrm{N} L_\mathrm{DC}} \left(\varphi_\mathrm{N} - \alpha_\mathrm{D}\right). \end{aligned} \tag{3.71}$$

The rms value of the the mains current (necessary to evaluate $\mathrm{THD_i}$ and λ) $I_{\mathrm{Ni,rms,DCM_{II}}}$ was computed finally and results in

$$\begin{aligned} I^2_{\mathrm{Ni,rms,DCM_{II}}} = \frac{2}{\pi} \Bigg(& A^2 \Bigg[\frac{\gamma_\mathrm{D} - \alpha_\mathrm{D}}{2} + \ldots \\ & \ldots + \frac{\sqrt{3}}{8}\left(\cos^2\left(\gamma_\mathrm{D}\right) - \cos^2\left(\alpha_\mathrm{D}\right)\right) - \frac{\sqrt{3}}{8}\left(\sin^2\left(\gamma_\mathrm{D}\right) - \sin^2\left(\alpha_\mathrm{D}\right)\right) - \ldots \\ & \ldots - \frac{1}{4}\left(\cos\left(\gamma_\mathrm{D}\right)\sin\left(\gamma_\mathrm{D}\right) - \cos\left(\alpha_\mathrm{D}\right)\sin\left(\alpha_\mathrm{D}\right)\right) \Bigg] - \ldots \\ & \ldots - A^2 B \Big[\sin\left(\gamma_\mathrm{D}\right) - \sin\left(\alpha_\mathrm{D}\right) + \sqrt{3}\left(\cos\left(\gamma_\mathrm{D}\right) - \cos\left(\alpha_\mathrm{D}\right)\right) \Big] - \ldots \\ & \ldots - ABC \Big[\gamma_\mathrm{D} - \alpha_\mathrm{D}\Big]^2 - A^2 B^2 \Big[\gamma_\mathrm{D} - \alpha_\mathrm{D}\Big] - C^2 \Big[\gamma_\mathrm{D} - \alpha_\mathrm{D}\Big]^3 + \ldots \\ & \ldots + AC \Big[\cos\left(\gamma_\mathrm{D}\right) - \cos\left(\alpha_\mathrm{D}\right) - \sqrt{3}\left(\sin\left(\gamma_\mathrm{D}\right) - \sin\left(\alpha_\mathrm{D}\right)\right) + \ldots \\ & \ldots + \sqrt{3}\cos\left(\gamma_\mathrm{D}\right)\left(\gamma_\mathrm{D} - \alpha_\mathrm{D}\right) + \sqrt{3}\sin\left(\gamma_\mathrm{D}\right)\left(\gamma_\mathrm{D} - \alpha_\mathrm{D}\right) \Big] \Bigg) \end{aligned} \tag{3.72}$$

whereas the coefficients A, B and C are defined by

$$A = \frac{\sqrt{3}\hat{V}_\mathrm{N}}{\omega_\mathrm{N} L_\mathrm{DC}}, \quad B = \sqrt{1 - \left(\frac{V_\mathrm{o}}{\sqrt{3}\hat{V}_\mathrm{N}}\right)^2}, \quad C = \frac{V_\mathrm{o}}{\omega_\mathrm{N} L_\mathrm{DC}}\,. \tag{3.73}$$

Due to the high complexity grade and calculation effort for both discontinuous conduction mode states (state 1 and state 2) neither the $\mathrm{THD_i}$ nor the power factor λ are evaluated analytically. If a closed mathematical form of these two parameters is required, it could still be performed using **Eq. 3.3** and **Eq. 3.5**. Finally, calculated inductor current $i_{\mathrm{L,DCM_{II}}}$ and B6 output voltage v_rec are both plotted in **Fig. 3.8** for both occurring sections (I/II) and the interval $\left[0 \ldots \frac{2\pi}{3}\right]$.

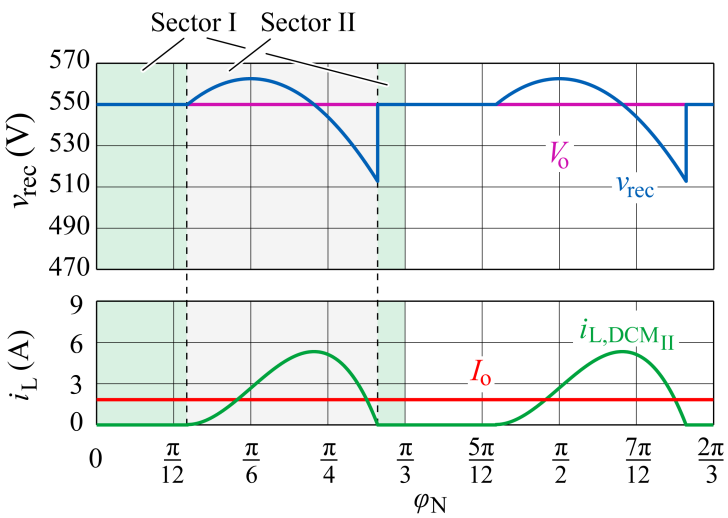


Fig. 3.8: Calculated DC-side smoothing inductor current $i_{L,DCM_{II}}$, rectifier voltage v_{rec}, output current and output voltage waveforms of the passive three-phase rectifier system for discontinuous conduction mode DCM_{II} ($V_o = 550\,V$ and $I_o = 1.81\,A$).

For the derived current $i_{L,DCM_{II}}$, the averaged value yields

$$I_{o,DCM_{II}} = \frac{3\sqrt{3}\hat{V}_N}{2\pi\omega_N L_{DC}}\left[\sin\left(\gamma_D - \frac{2\pi}{3}\right) - \sin\left(\alpha_D - \frac{2\pi}{3}\right) + \ldots \right.$$
$$\left. \ldots + (\gamma_D - \alpha_D)\sqrt{1 - \frac{1}{3}\left(\frac{V_o}{\hat{V}_N}\right)^2}\right] - \frac{3V_o}{2\omega_N L_{DC}}\left[\gamma_D - \alpha_D\right]^2 . \tag{3.74}$$

3.5 Input/Output Characteristics

The previous sections discussed and illustrated different operational modes (CCM, DCM_I,DCM_{II}) occurring for different output loads. **Fig. 3.9** now depicts the calculated V_o-I_o output characteristic dependent on the instantaneous output power P_o. As can be seen, during CCM the output voltage is slightly decreasing for increased output power (due to commutation effects dependent on AC-side mains inductance L_N and output current I_o).[1] Regarding DCM, the output voltage is increasing until

$$V_o = \max\left(u_{rec}\right) = \sqrt{3}V_o = 562.9\,V \tag{3.75}$$

has been reached (considering balanced mains voltages and neglecting charge-pump effects by diode capacitances etc.).

Fig. 3.10 illustrates a 10 kW B6 rectifier implemented laboratory prototype. **Fig. 3.11** gives a comparison between expected and measured results of total harmonic input current distortion THD_i and power factor λ for the designed prototype. Main system specifications of the rectifier are mentioned in **TABLE 3.2**.

[1]Remark that parasitic components are neglected for sake of simplicity.

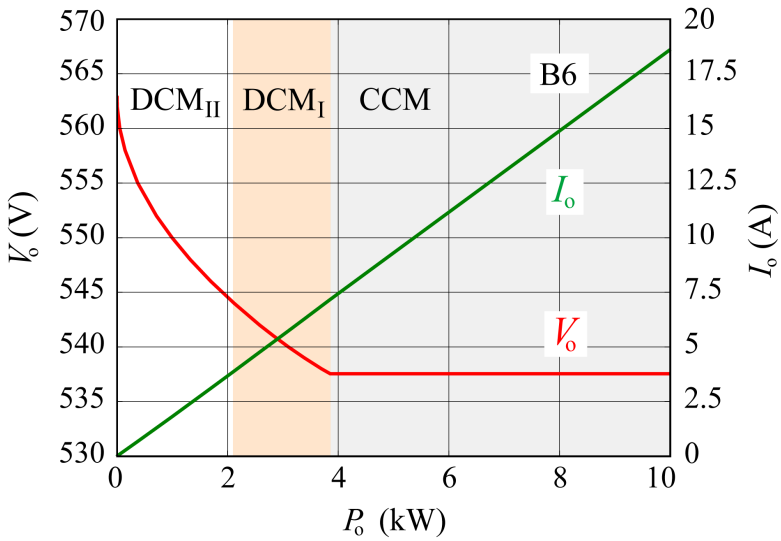


Fig. 3.9: Calculated output characteristics V_o and I_o of a passive three-phase rectifier system for an output power range of 0 W to nominal load (10 kW) considering continuous and discontinuous conduction mode.

TABLE 3.2: Design specifications of the manufactured passive three-phase rectifier system.

System Specifications	
Mains voltage:	$V_{LL} = 400\,V_{rms}$
Mains frequency:	$f_N = 50\,Hz$
Output power:	$P_o = 10\,kW$
DC-side smoothing inductance:	$L_{DC} = 2.25\,mH$
Output capacitor:	$C_o = 1.1\,mF$

It can be observed that calculated ($THD_{i,calc}$, $\lambda_{i,calc}$) and real ($THD_{i,meas}$, $\lambda_{i,meas}$) characteristics slightly differ. The deviation is mainly based on an ideal derivation which is neglecting e.g. effects of output voltage ripple ($C_o \to \infty$), unbalance of mains voltages (described in the following section) etc. Additional measurement results of e.g. input/output currents and voltage waveforms are provided in [106]. The implemented passive three-phase rectifier system as depicted in **Fig. 3.10**, basically consists of a B6 diode bridge with additional snubber circuit, the required DC-side smoothing inductor, balancing resistors, charging resistors and appropriate charging resistor short circuit relay. The obviously large heatsink is not necessary for cooling efforts but used here just as an assembly plate.

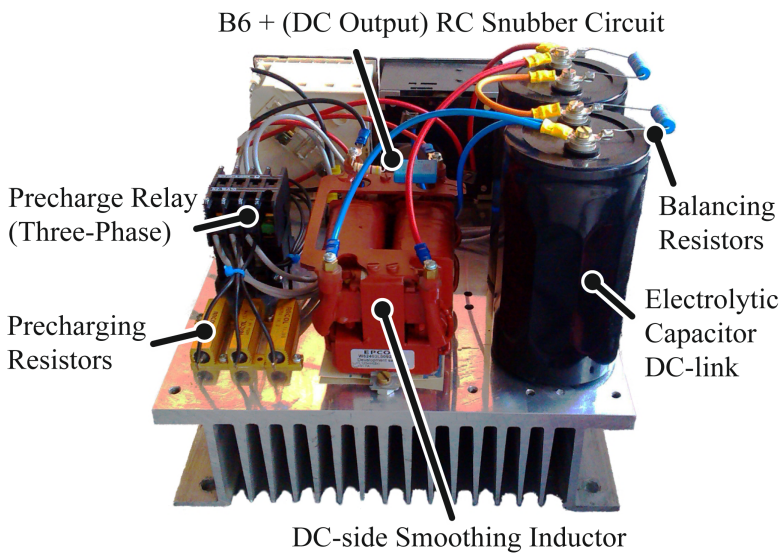


Fig. 3.10: Prototypical realization of a 400 V_{rms}/10 kW passive three-phase rectifier system including B6 diode bridge, rectifier output voltage snubber circuit, DC-side smoothing inductor, balancing resistors, charging resistors and appropriate charging resistor short circuit relay.

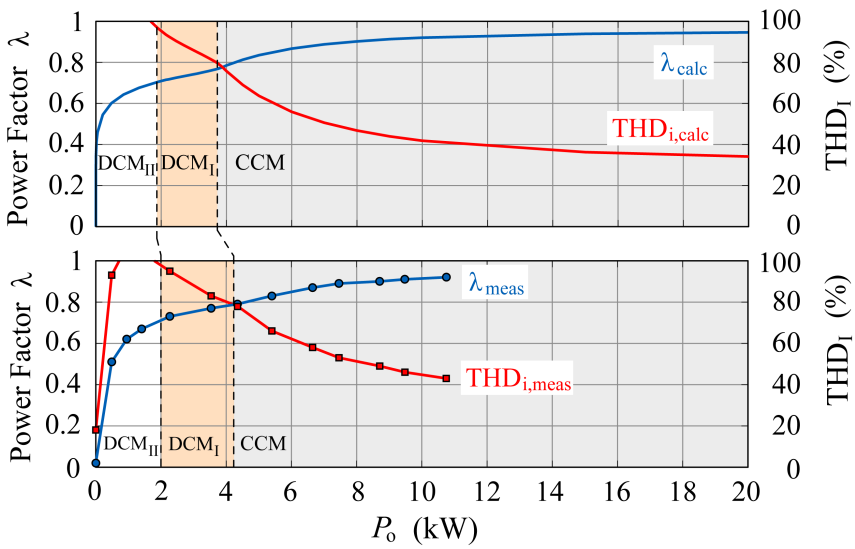


Fig. 3.11: Comparison between the calculated values and measurement results (given for a 10 kW passive three-phase rectifier system) of total harmonic input current distortion THD_i and power factor λ

3.6 Design Parameters

In order to evaluate expected system losses of the passive system, current stress of passive and active components are derived and listed. The following equations are only valid for continuous conduction operating mode of the passive system.

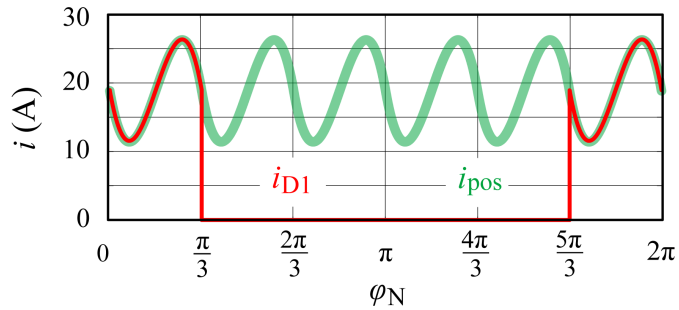


Fig. 3.12: Positive busbar current waveform i_{pos} of a three-phase diode bridge rectifier and appropriate semiconductor current of diode D_1 (i_{D1}) which forms the interconnection between positive busbar and phase 1 for a nominal output power of 10 kW and DC-side smoothing inductance value of 2.25 mH.

3.6.1 Current Stress of Components

All calculations performed in this section, are based on the "fourier series" evaluated current $i_L(\varphi_N)$ given in **Eq. 3.13**. If balanced mains voltages ($V_{Ni,rms} = 230\,V$) are assumed, all six diodes diodes are equally stressed (AVG $I_{D1-6,avg}$ and rms $I_{D1-6,rms}$).

$$I_{D1-6,avg} = \frac{I_o}{3} \tag{3.76}$$

$$I_{D1-6,rms} = \sqrt{\frac{1}{3}I_o^2 + \left(\frac{\hat{V}_N}{\pi\omega_N L_{DC}}\right)^2 \left(\frac{7}{12}\pi^2 + \frac{9\sqrt{3}}{4}\pi - 18\right)} \tag{3.77}$$

The current waveshape of one diode (e.g. Diode i_{D1}) compared with the DC-side choke current i_L is depicted in **Fig. 3.12** (i_{D1} - red, i_L - light green). Averaged and rms values of DC-side smoothing inductance current ($i_{L,avg}$ and rms $i_{L,rms}$, respectively) as defined in **Eq. 3.13**, compute to

$$I_{L,avg} = I_o \tag{3.78}$$

$$I_{L,rms} = \sqrt{I_o^2 + \left(\frac{\hat{V}_N}{\pi\omega_N L_{DC}}\right)^2 \left(\frac{7}{4}\pi^2 + \frac{27\sqrt{3}}{4}\pi - 54\right)}. \tag{3.79}$$

The output DC-link capacitor current (i_{C_o}) can be determined by $i_L - I_o$ and is characterised by

$$i_{C_o}(\varphi_N) = -\frac{3\sqrt{3}\hat{V}_N}{\pi\omega_N L_{DC}} \sum_{k=1,2,3,\ldots}^{\infty} \frac{2}{(6k)^3 - 6k} \sin(6k\varphi_N). \tag{3.80}$$

Consequently, the current stress of the output DC-link capacitors of the rectifier system computes to

$$I_{C_o,avg} = 0\,A \tag{3.81}$$

$$I_{C_o,rms} = \left(\frac{\hat{V}_N}{\pi\omega_N L_{DC}}\right) \sqrt{\left(\frac{7}{4}\pi^2 + \frac{27\sqrt{3}}{4}\pi - 54\right)}. \tag{3.82}$$

Averaged and rms values of AC-side input currents calculate to

$$I_{\mathrm{Ni,avg}} = 0\,\mathrm{A} \tag{3.83}$$

$$I_{\mathrm{Ni,rms}} = \sqrt{\frac{2}{3}I_{\mathrm{o}}^2 + \left(\frac{\hat{V}_{\mathrm{N}}}{\pi\omega_{\mathrm{N}}L_{\mathrm{DC}}}\right)^2\left(\frac{7}{6}\pi^2 + \frac{9\sqrt{3}}{2}\pi - 36\right)} \tag{3.84}$$

3.6.2 Passive Components

As previously discussed, a typical design issue for a B6 rectifier is the selection of the DC-side choke L_{DC} and the output capacitor C_{o}. Three main characteristics have to be considered for a proper design of L_{DC} and C_{o}. Firstly, a large value of L_{DC} is preferred to lower current distortions ($\mathrm{THD_i}$) of mains currents. Secondly, a large inductance consequently results in an increased inductor volume with consequently leads to undesirable high cost. An optimum between (i) and (ii) therefore has to be found. Thirdly, quantities as resonance frequency $f_{\mathrm{res}} = 1/\left(2\pi L_{\mathrm{DC}}C_{\mathrm{o}}\right)$ and output impedance $Z_{\mathrm{o}} = \sqrt{L_{\mathrm{DC}}/C_{\mathrm{o}}}$ have to be considered (load step characteristic etc.). Nevertheless a specific $\mathrm{THD_i}$ is required to fulfill the IEEE standards for passive diode bridge rectifier applications. To guarantee a specific $\mathrm{THD_i}$ (for a required nominal power), the DC-side smoothing inductor L_{DC} which can be calculated by

$$L_{\mathrm{DC}} = \frac{\hat{V}_{\mathrm{N}}^2}{\omega_{\mathrm{N}}P_{\mathrm{o}}}\frac{3}{\pi}\sqrt{\frac{\frac{\pi^2}{3} + \frac{3\sqrt{3}\pi}{2} - \frac{171}{16} + \frac{27\sqrt{3}}{2\pi} - \frac{81}{\pi^2}}{\mathrm{THD_i^2} - \mathrm{THD_{i,min}^2}}} \tag{3.85}$$

as derived in **Eq. 3.23** has to be chosen accordingly (with $\mathrm{THD_{i,min}}$ as the minimum $\mathrm{THD_i}$ of 0.31 as derived in **Eq. 3.1**). Value and volume of L_{DC} are hence dependent of desired nominal load P_{N} and required $\mathrm{THD_i}$. **Fig. 3.13** depicts the multidimensional issue in three different plots. The upper left figure illustrates $L_{\mathrm{DC}}\left(\mathrm{THD_i}, P_{\mathrm{N}}\right)$. Obviously, L_{DC} starts to vastly increase for diminutive loads (due to the $\frac{1}{x}$ dependency). Similar assumptions are valid for a $\mathrm{THD_i}$ close to $\sqrt{\frac{\pi}{9}^2 - 1}$. Although L_{DC} can be extracted from this equation for specific values of $\mathrm{THD_i}$ and P_{N}, this figure does not allow any prediction about the volume of the DC-side choke. A "volume inductor index" k_{i} (as defined in [107]), which is represented by

$$k_{\mathrm{i}} = L_{\mathrm{DC}}\hat{I}_{\mathrm{L}}^2 \tag{3.86}$$

is therefore introduced using

$$\hat{I}_{\mathrm{L}}^2 = \hat{I}_{\mathrm{o}}^2 + 2I_{\mathrm{o}}I_{\mathrm{L,ac}} + \hat{I}_{\mathrm{L,ac}}^2. \tag{3.87}$$

If **Eq. 3.39** is used for L_{DC}, **Eq. 3.35** for $\hat{I}_{\mathrm{L,ac}}$ and

$$I_{\mathrm{o}} = \frac{\pi}{3\sqrt{3}\hat{V}_{\mathrm{N}}}P_{\mathrm{o}} \tag{3.88}$$

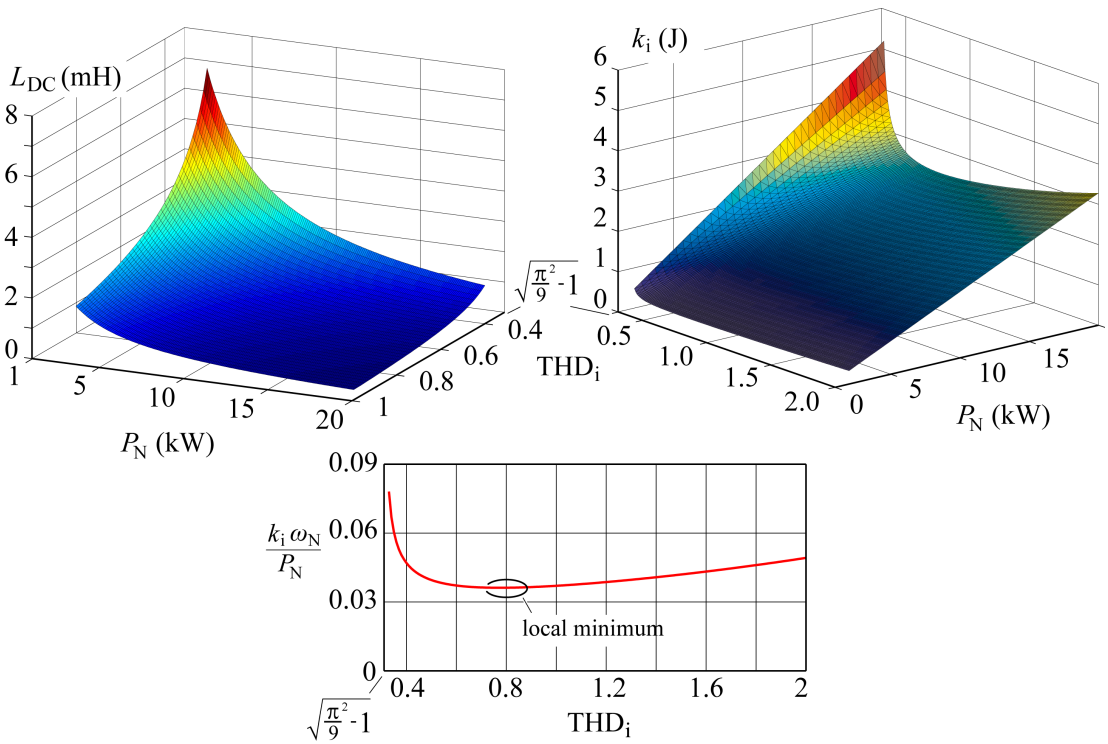


Fig. 3.13: Graphical illustration of DC-side smoothing inductance $L_{DC}(\mathrm{THD_i}, P_N)$ (3D - upper left), volume inductance index $k_i(\mathrm{THD_i}, P_N)$ (3D - upper right) and power related value of k_i (2D).

the power related value of k_i finally results in

$$\frac{k_i \omega_N}{P_o} = \left(2 + \frac{\pi}{9}\sqrt{\zeta_k(\mathrm{THD_i})} + \frac{9}{\pi\sqrt{\zeta_k(\mathrm{THD_i})}}\right)\left(\mathrm{THD_{i,min}} - \arccos\left(\frac{3}{\pi}\right)\right). \tag{3.89}$$

The minimum of this function (which represents a minimum volume of the required smoothing inductor) can be found at $\partial k_i / \partial \mathrm{THD_i}$ which results in a $\mathrm{THD_{i,opt}}$ of ≈ 0.8. The parameter ζ_k which is dependent on the $\mathrm{THD_i}$ is defined by

$$\zeta_k(\mathrm{THD_i}) = \frac{\frac{9}{2} - \left(\frac{54}{35\pi}\right)^2\left(1 + \mathrm{THD_i^2}\right)}{1 + \mathrm{THD_i^2} - \left(\frac{\pi}{3}\right)^2}. \tag{3.90}$$

If a specific value for L_{DC} has been chosen (considering, standards, cost and volume), the output capacitor can now be designed. One parameter which is dependent on C_o is the maximum allowable output voltage ripple of the system. In general, an output capacitor of $C_o \to \infty$ is assumed and desired to achieve a purely DC output voltage ($v_o = V_o$). A far more practical approach is the implementation of a capacitor which is designed such to allow a reasonable compromise between output voltage ripple, output capacitor bank volume and rated voltage (V_R).
The dependency of the output capacitor value C_o considering the maximum ac-

ceptable peak to peak output voltage ripple $\Delta V_{\mathrm{o,pkpk}}$ is given by

$$C_{\mathrm{o}}\left(\Delta v_{\mathrm{o,ac}}\right) = -\frac{3\sqrt{3}\hat{V}_{\mathrm{N}}}{\pi\omega_{\mathrm{N}}^{2} L_{\mathrm{DC}} \Delta V_{\mathrm{o,pkpk}}}\left(\frac{1}{27}\pi^{2} + \frac{2}{\sqrt{3}}\pi - 4\right) \tag{3.91}$$

whereas the appropriate ESR of the capacitor has been neglected. The maximum rated voltage (V_{R}) of the DC-link output has to be satisfy the maximum occurring instantaneous output voltage ($V_{\mathrm{o,max}}$) which can appear due to e.g. load steps, energy feed-back due to regenerative breaking of motor application (which typically means an increased voltage of the output DC-link) etc. Therefore, V_{R} of the total DC-link has at least suffice

$$V_{\mathrm{o,max}} = V_{\mathrm{o}} + \hat{v}_{\mathrm{o,ac}} + Z_{\mathrm{o}} \Delta I_{\mathrm{o}} \tag{3.92}$$

with $Z_{\mathrm{o}} = \sqrt{L_{\mathrm{DC}}/C_{\mathrm{o}}}$ and ΔI_{o} the maximum expectable load current change. If a number of series connected electrolytic capacitors (n_{S}) with additional number of parallel strings (n_{P}) is allowed, the mentioned quantities for a proper design are given by

$$n_{\mathrm{S}} = \frac{V_{\mathrm{o,max}}}{V_{\mathrm{R}}}, \quad n_{\mathrm{P}} = n_{\mathrm{S}} \frac{C_{\mathrm{o,min}}}{C}, \quad R_{\mathrm{o,ESR}} = \frac{n_{\mathrm{S}}}{n_{\mathrm{P}}} R_{\mathrm{ESR}} \tag{3.93}$$

with a total number of required capacitors of $n_{\mathrm{S}} \cdot n_{\mathrm{P}}$.

3.6.3 Total System Losses

In this section, major loss components of the passive three-phase rectifier are going to be addressed and discussed. Most relevant components are

- diode bridge (diodes $D_1 - D_6$)
- DC-side inductor(s)
- DC-side capacitor(s)
- balancing resistors.

The diode bridge rectifier is generally characterized by a combination of 6 single diodes. These diodes can either be implemented separately, or are commercially available as one single module with five terminals (3 x AC input, positive/negative output). For loss calculation each diode can be described by a piecewise linear model, consisting of a forward voltage $V_{\mathrm{F}}\left(T_{\mathrm{j}}\right)$, a forward resistance $R_{\mathrm{D}}\left(T_{\mathrm{j}}\right)$ and an ideal switch connected in series. T_{j} is defined as the junction temperature of the device. The voltage across the conducting diode is defined by

$$V_{\mathrm{D}}\left(T_{\mathrm{j}}, i_{\mathrm{D}}\right) = V_{\mathrm{F}}\left(T_{\mathrm{j}}\right) + R_{\mathrm{D}}\left(T_{\mathrm{j}}\right) i_{\mathrm{D}}. \tag{3.94}$$

The B6 rectifier is typically optimized for slow switching operations (switching losses negligibly) and therefore mainly characterized by pure conduction losses $P_{\mathrm{L,B6,con}}$. Losses of the diode bridge hence are defined by

$$P_{\mathrm{L,B6}} \approx P_{\mathrm{L,B6,con}} = 6 \cdot \left(V_{\mathrm{F}}\left(T_{\mathrm{j}}\right) I_{\mathrm{D1-6,avg}} + R_{\mathrm{D}}\left(T_{\mathrm{j}}\right) I_{\mathrm{D1-6,rms}}^{2}\right). \tag{3.95}$$

TABLE 3.3: List of components of the designed passive three-phase rectifier structure in order to evaluate a proper loss model.

	Components
B6	Vishay 36MT140, 36 A, 1400 V, $V_{\mathrm{F}} = 1.13\,\mathrm{V}$, $R_{\mathrm{D}} = 5.2\,\mathrm{m\Omega}$
L_{DC}	DM Iron Inductor, 2x1.125 mH
C_{o}	Felsic O39, 2x2.2 mF, 400 V, $R_{\mathrm{ESR,max}} = 2\mathrm{x}85\,\mathrm{m\Omega}$
R_{bal}	2x47 kΩ, 5 W

The DC-side choke is implemented as an air-gaped iron core inductor. Losses of such an inductor can be split into iron ($P_{\mathrm{L,FE}}$) and copper losses ($P_{\mathrm{L,DC}}$).

$$P_{\mathrm{L},L_{\mathrm{DC}}} = R_{\mathrm{L,DC}} I_{\mathrm{L,rms}}^2 + P_{\mathrm{FE}}. \tag{3.96}$$

The total losses of the DC-side located choke have been experimentally evaluated to $\approx 49\,\mathrm{W}$ at a nominal output power of 10 kW. As there are no switching frequency parts stressing the choke, the mentioned loss fractions are a sufficed description of the overall inductor losses (no proximity effect, skin-effect, fringing effect etc. needs to be taken into account).
Output capacitor (C_{o}) losses are defined by the equivalent series resistance of the implemented electrolytic capacitor ($R_{\mathrm{o,ESR}}$). Losses according to output capacitors are given by

$$P_{\mathrm{L},C_{\mathrm{o}}} = \frac{n_{\mathrm{S}}}{n_{\mathrm{P}}} R_{\mathrm{o,ESR}} I_{\mathrm{C_o,rms}}^2. \tag{3.97}$$

As previously mentioned, balancing resistors are required to guarantee properly distributed voltage levels for series connected electrolytic capacitors. If a series arrangement of capacitors is required for implementation of the DC-link output capacitor bank ($n_{\mathrm{S}} > 1$) losses according to a passive balancing circuit can be determined by

$$P_{\mathrm{L},R_{\mathrm{o,bal}}} = \frac{27\hat{V}_{\mathrm{N}}^2}{n_{\mathrm{S}}\pi^2 R_{\mathrm{o,bal}}}. \tag{3.98}$$

Fig. 3.14 illustrates the calculated loss distribution (according to **TABLE 3.3**) of the B6 rectifier system. Obviously, the predominant share (94 %) of the rectifier system consists of losses due to the inductor (48.5 %) and B6 diode bridge (45.5 %). Losses regarding output capacitors and balancing resistors are contributing only a small fraction compared to the total system losses and can hence be considered as negligibly small. Considering the calculated losses, the efficiency of the B6 rectifier system for an output power of 10 kW, computes to

$$\eta_{\mathrm{B6}} = \frac{P_{\mathrm{out}}}{P_{\mathrm{out}} + P_{\mathrm{L,tot}}} \approx 99\,\%\,. \tag{3.99}$$

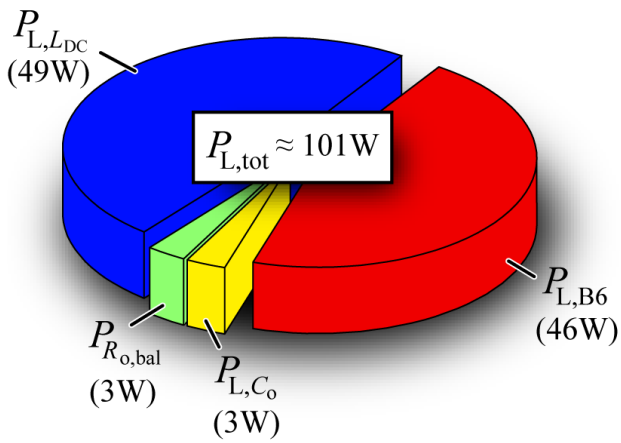


Fig. 3.14: Calculated loss distribution of a passive three-phase rectifier system at nominal output load (10 kW).

It has to be mentioned, that in idle mode[2] ($i_{Ni} \approx 0\,A$, $i_L = 0\,A$), only losses evoked due to balancing resistors are present. The required active input power hence results in

$$P_{in} = P_{L,tot,idle} = P_{L,R_{o,bal}}. \tag{3.100}$$

3.7 Phase Loss

The phase loss condition is one of the most critical situations for a B6 rectifier. The three-phase diode bridge has to transmit the required active power ($P_o = i_{L,avg} v_{rec,avg}$) from the AC- to the DC-side during absence of one bridge leg (due to the missing phase). This finally leads to a single phase operation and results in a permanent discontinuous conduction mode and tremendously higher peak current values. Furthermore, power factor λ and THD_i are substantially worsened compared to the typical CCM operation.
For further investigations a loss of phase 2 is assumed which results in $i_{N2} = 0\,A$. D_3 and D_6 are hence permanently blocking. As no current path for phase 2 is available anymore only $i_{N1} = -i_{N3}$ is valid. Hence, merely those active states are available where D_1,D_2 or D_4,D_5 are conducting:

- $\varphi_N = [\approx 0 \ldots \approx \pi/3]$, conducting diodes: D_1/D_2, $i_{N1} = -i_{N3} = i_L$
- $\varphi_N = [\approx \pi/3 \ldots \approx \pi]$, conducting diodes: –/–, $i_{N1} = i_{N2} = i_{N3} = 0\,A$
- $\varphi_N = [\approx \pi \ldots \approx 4\pi/3]$, conducting diodes: D_4/D_5, $-i_{N1} = i_{N3} = i_L$
- $\varphi_N = [\approx 4\pi/3 \ldots \approx 2\pi]$, conducting diodes: –/–, $i_{N1} = i_{N2} = i_{N3} = 0\,A$.

As can be seen, the conducting intervals are not anymore located "exactly" at $0, \pi/3, \ldots$. Diodes D_1 and D_2 e.g., are starting to conduct current when $v_{N1} -$

[2]idle mode: AC-side mains voltages are still applied, but no output load is connected ("no load operation")

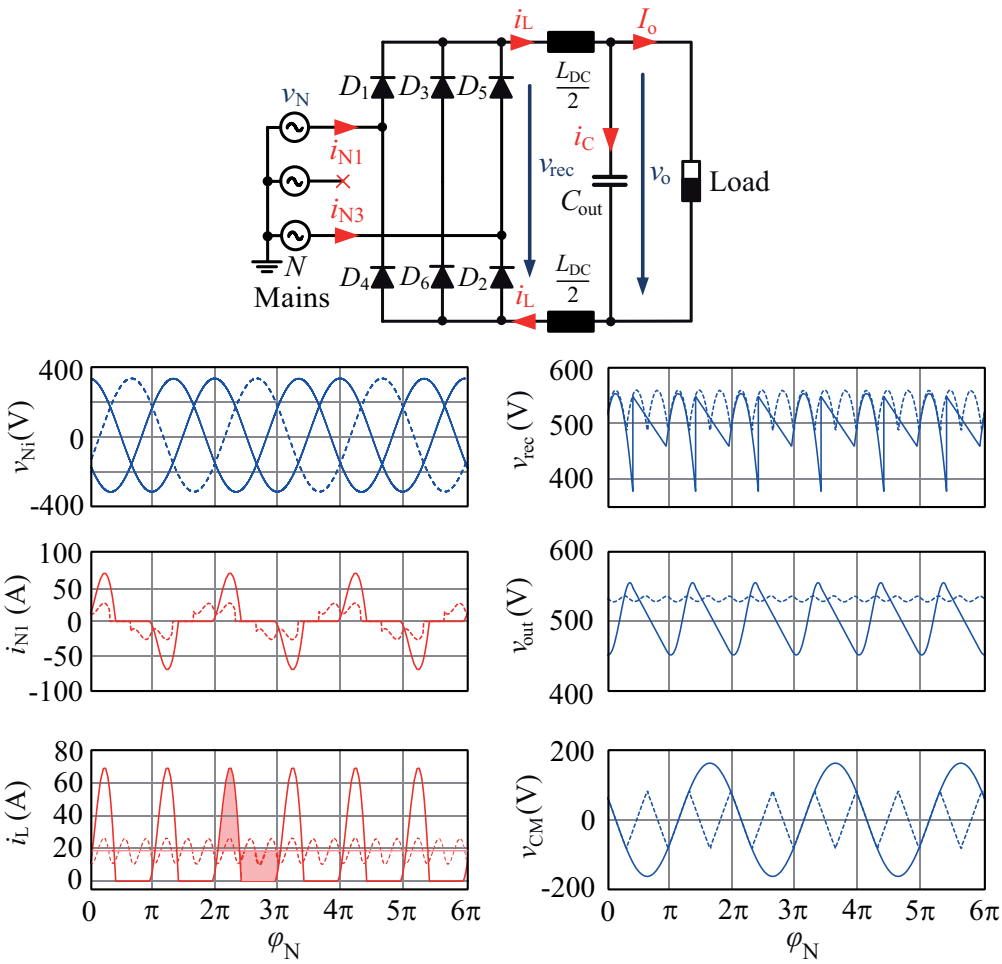


Fig. 3.15: Comparison of passive three-phase rectifier voltage and current waveforms for 10 kW operation with (dashed) and without phase 2 (solid).

$v_{N3} > 0$ and $v_{rec} = v_{N1} - v_{N3}$. Due to the increased output voltage ripple of v_o during a missing phase operation, $v_{rec} - (v_{N1} - v_{N3}) = 0$ applies for $\varphi_N < 0$. The current i_L then is defined by

$$i_L = \frac{1}{\omega L_{DC}} \int (v_{N1} - v_{N3} - v_o)\, \mathrm{d}\varphi_N \tag{3.101}$$

and the output voltage ripple is given according to

$$v_o = \frac{1}{\omega C_o} \int (i_L - I_o)\, \mathrm{d}\varphi_N. \tag{3.102}$$

$D_1 + D_2$ are going to block again when the energy, which is stored within L_{DC} during $v_{N1} - v_{N3} - v_o > 0$ is completely depleted ($i_L = 0\,\mathrm{A}$) again. While all diodes are blocking,

$$v_{rec} = v_o \tag{3.103}$$

applies. During this time the DC-link output capacitors are discharged by I_o. **Fig. 3.15** depicts current (i_{N1}, i_L) and voltage waveforms (v_{Ni}, v_o, v_{rec}, v_{CM}) for

either standard CCM (dashed) or phase loss operation (solid). As can be seen, the common mode voltage v_{CM} is defined (according to the appropriates lost phase) by

$$v_{\mathrm{CM}} = -\frac{v_{\mathrm{N2}}}{2}. \tag{3.104}$$

Chapter 4

Third Harmonic Injection Principle

Passive three-phase rectifier systems with LC output filter are basically

- highly efficient ($\eta \approx 99\,\%$)
- robust
- simple
- and utilize a very cost effective mains input stage

for feeding the DC-link (formed in general by electrolytic capacitors) of e.g. switch-mode power supplies or drives. Furthermore, usually no additional transformer (as e.g. Yd, Dy, Dz, etc.) is required due to the fact that the mains currents do not show any DC component (i_{Ni}). The B6 rectifier circuit is, therefore, commonly and widely used for industrial applications. As given in the previous chapter, the B6 rectifier is characterized by a limited power factor λ of $0.9 \ldots 0.95$ and by rather high harmonic input current components ($\mathrm{THD_i}$ in general up to $48\,\%$ or higher for nominal load operation). Both the input current quality and power factor of the system are mainly influenced by the DC-side located inductance L_{DC}. Further improvements of both quantities beyond $45\,\%$ and close to 0.95 would hence result in a large smoothing inductor volume and is in principal limited to a

$$\mathrm{THD_{i,B6}} \geq \sqrt{\frac{\pi^2}{9} - 1} \approx 31\,\%, \quad \lambda_{\mathrm{B6}} \leq \frac{3}{\pi} \approx 0.95, \quad \text{for} \quad L_{\mathrm{DC}} \to \infty\,. \tag{4.1}$$

Consequently, it is not possible to provide sinusoidal input currents and a unity power factor by such B6 rectifiers. Instead, a large quantity of circuit variants of <u>active</u> three phase rectifiers exist (e.g., cf., [18, 19] and *chapter 2*). Active three-phase PFC rectifier systems as, e.g., the VIENNA rectifier (unidirectional power flow) [66], the six-switch boost-type PFC rectifier (bidirectional power flow) [9], six-switch buck-type PFC rectifier (unidirectional power flow, for positive DC

output voltage)[9], SWISS Rectifier (unidirectional power flow) [32] or the "hybrid third harmonic current injection active-filter rectifier" (unidirectional power flow) [18, 28] are perfectly suitable to fulfill the IEC61000-3-2 standard [5], [6] for mitigation of input current harmonics. Major drawbacks of these rectifier circuits are however that (at least) two active semiconductor components have to process the full amount of output power and none of these structures can be used to extend an already existing B6 rectifier to a low harmonic input stage. A simple upgrade of e.g. a B6 rectifier to sinusoidal mains currents is not possible as the passive rectifier diodes/inductors would not be able to sustain the appearing high switching frequencies being essential for sinusoidal active current shaping. The active circuit hence has to be completely redesigned.
Therefore, for specific applications a low harmonic circuit may be preferred which allows to upgrade the B6 rectifier to allow harmonic device without fully redesigning the passive bridge. The third harmonic injection (THI) principle offers an adequate solution to fulfill the applicable standards for active rectifier systems.

4.1 Basic Principle

The basic idea of the third harmonic injection principle allows the extension of an existing passive three-phase diode bridge rectifier to a low-harmonic current input stage by adding an additional active converter stage to the DC-side of the passive circuit at five points which are typically accessible. Most important noticeable benefits of the concept can hence be addressed by:

- No redesign of the passive rectifier is required as the active optional circuit acts as an upgrade/extension.
- The active system only needs to process some small amount of active and reactive power compared to the rated output power ($P_{\mathrm{THI}} = 6\,\%P_{\mathrm{o}}$, $Q_{\mathrm{THI}} = 16\,\%P_{\mathrm{o}}$) and an improved efficiency compared to a conventional active rectifier can hence be expected.
- A unity power factor $\lambda > 0.99$ and low harmonic input currents ($\mathrm{THD_i} < 5\,\%$) can be achieved.
- No common mode voltage with switching frequency at the output of the total system exists.

The optional active circuit extension is formed by three different parts (cf., **Fig. 4.1**):

- The current shaping network (CSN),
- the current injection device (CID)
- and the required input filter to suppress high switching frequency components of rectifiers mains input currents.

This *current shaping network* generates currents $i_{\mathrm{cp}}/i_{\mathrm{cn}}$ (injected into the positive and negative busbar of the passive bridge) in order to compensate the unfavorable

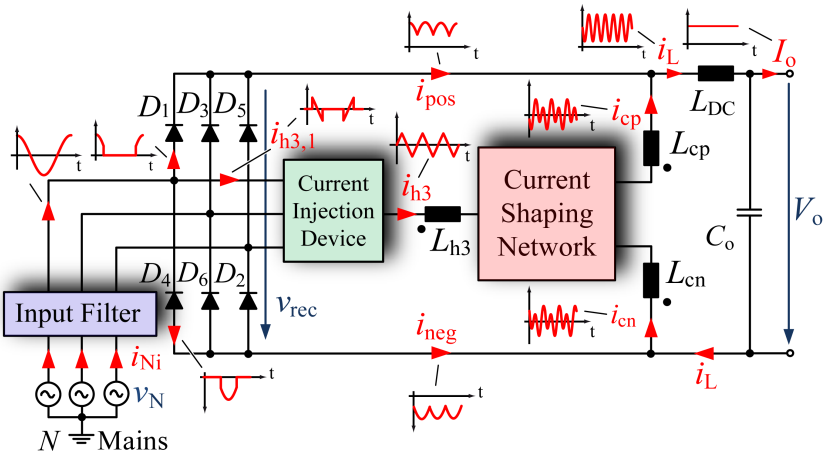


Fig. 4.1: Basic schematic of passive three-phase rectifier employing an active current shaping and injection network in order to achieve sinusoidal mains currents i_{Ni}.

300 Hz harmonic current of the LC output filter (of the passive system)

$$\Delta i_{\mathrm{L}}\left(\varphi_{\mathrm{N}}\right) = -\frac{3\sqrt{3}\hat{V}_{\mathrm{N}}}{\pi\omega_{\mathrm{N}}L_{\mathrm{DC}}}\sum_{k=1}^{\infty}\frac{2}{(6k)^3-6k}\sin\left(6k\varphi_{\mathrm{N}}\right) \quad \text{for} \quad k\in\mathbb{N} \tag{4.2}$$

and forms 150 Hz ($2\pi/3$) sinusoidal wave shapes $i_{\mathrm{pos}}/i_{\mathrm{neg}}$ intervals, respectively. Injection currents i_{cp} and i_{cn} are therefore defined by

$$i_{\mathrm{cp}} = i_{\mathrm{L}} - i_{\mathrm{pos}} \tag{4.3}$$

and

$$i_{\mathrm{cn}} = i_{\mathrm{L}} + i_{\mathrm{neg}}. \tag{4.4}$$

The injection currents i_{cp} and i_{cn} are furthermore linked to each other according to Kirchhoff's law by

$$i_{\mathrm{cp}} = i_{\mathrm{h3}} + i_{\mathrm{cn}}. \tag{4.5}$$

The third harmonic current i_{h3} is formed accordingly by

$$i_{\mathrm{h3}} = i_{\mathrm{cp}} - i_{\mathrm{cn}}. \tag{4.6}$$

If i_{pos} and i_{neg} consist (due to appropriate current control) of $2\pi/3$-sinusoidal fractions, the achieved third harmonic current i_{h3} calculates to

$$i_{\mathrm{h3}} = i_{\mathrm{L}} - i_{\mathrm{pos}} - \left(i_{\mathrm{L}} + i_{\mathrm{neg}}\right) = -i_{\mathrm{N1}} - i_{\mathrm{N3}} = i_{\mathrm{N2}} \tag{4.7}$$

for the regarded sector $\varphi_{\mathrm{N}} \in [0\ldots\pi/6]$ ($i_{\mathrm{pos}} = i_{\mathrm{N1}}$, $i_{\mathrm{neg}} = i_{\mathrm{N3}}$)[1]. The current i_{h3} therefore is equal to i_{N2} in the investigated sector. It is hence shown and proofed that also i_{h3} consists of sinusoidal wave shapes by proper control of injection currents $i_{\mathrm{cp}}/i_{\mathrm{cn}}$.

[1] $i_{\mathrm{N1}} + i_{\mathrm{N2}} + i_{\mathrm{N3}} = 0$

The required *current injection device* is located in-between AC-side mains and current shaping network and consists of three bidirectional switches S_{1-3}. Each of the bidirectional switches has to process parts of the generated third harmonic current i_{h3}. Hence, S_{1-3} cyclically connect the current shaping network to the systems AC input. With this bidirectional device, the current i_{h3} can be fed into the AC-side mains also during those time intervals where a standard diode rectifier would show its 60 °/zero current-gap. Hence, only one of the bidirectional switches is turned-on at the same time and the switches are controlled according to the mains voltage situation. The bidirectional switches are operated with a switching frequency of only 100 Hz. Thus, switching losses of the current injection device are negligibly small. This allows an optimization of the implemented semiconductors with large chip area in order to minimize the predominant conduction losses.
For proper operation of passive and active switches and adequate current control of injected currents, one sequence ($\varphi_{\mathrm{N}} \in [0 \ldots 2\pi]$) of the assembled input current i_{N1} is given below:

$$i_{\mathrm{N1}} = i_{\mathrm{pos}}, \varphi_{\mathrm{N}} \in [0 \ldots \pi/3] \tag{4.8}$$
$$i_{\mathrm{N1}} = i_{\mathrm{h3}},\ \varphi_{\mathrm{N}} \in [\pi/3 \ldots 2\pi/3] \tag{4.9}$$
$$i_{\mathrm{N1}} = i_{\mathrm{neg}}, \varphi_{\mathrm{N}} \in [2\pi/3 \ldots 4\pi/3] \tag{4.10}$$
$$i_{\mathrm{N1}} = i_{\mathrm{h3}},\ \varphi_{\mathrm{N}} \in [4\pi/3 \ldots 5\pi/3] \tag{4.11}$$
$$i_{\mathrm{N1}} = i_{\mathrm{pos}}, \varphi_{\mathrm{N}} \in [5\pi/3 \ldots 2\pi]\,. \tag{4.12}$$

Finally, the last part of the proposed active converter concept is the required input filter in order to attenuate the occurring current ripple with switching frequency. This EMI filter can be implemented as e.g. star connected (foil) capacitor bank together with small inductances at the AC-side. The third harmonic principle advantageously allows to exploit the mains input impedance (L_{N}) to form the required LC filter structure and hence no additional AC-side inductor may be required (depending on impedance characteristic and required attenuation). Only an additional RC damping leg may be necessary for damping the occurring ringing according to the resonant circuit.
As the implemented input filter only has to be formed by a RC/C-filter topology, the active upgrade can be manufactured as an individual extension which includes all mandatory devices ((i) shaping network + appropriate inductors $L_{\mathrm{cp}}/L_{\mathrm{cn}}/L_{\mathrm{h3}}$ (ii) injection device and (iii) input filter).

4.2 Fundamental V/I Waveforms

In this section the most relevant current and voltage waveforms, in order to fundamentally understand the proposed rectifier concept, are presented. **Fig. 4.2** illustrates some of these averaged (low frequency) current and voltage waveforms. A set of basic equations are derived in order to provide the most important quantities which are necessary for a proper circuit design in the following sections.

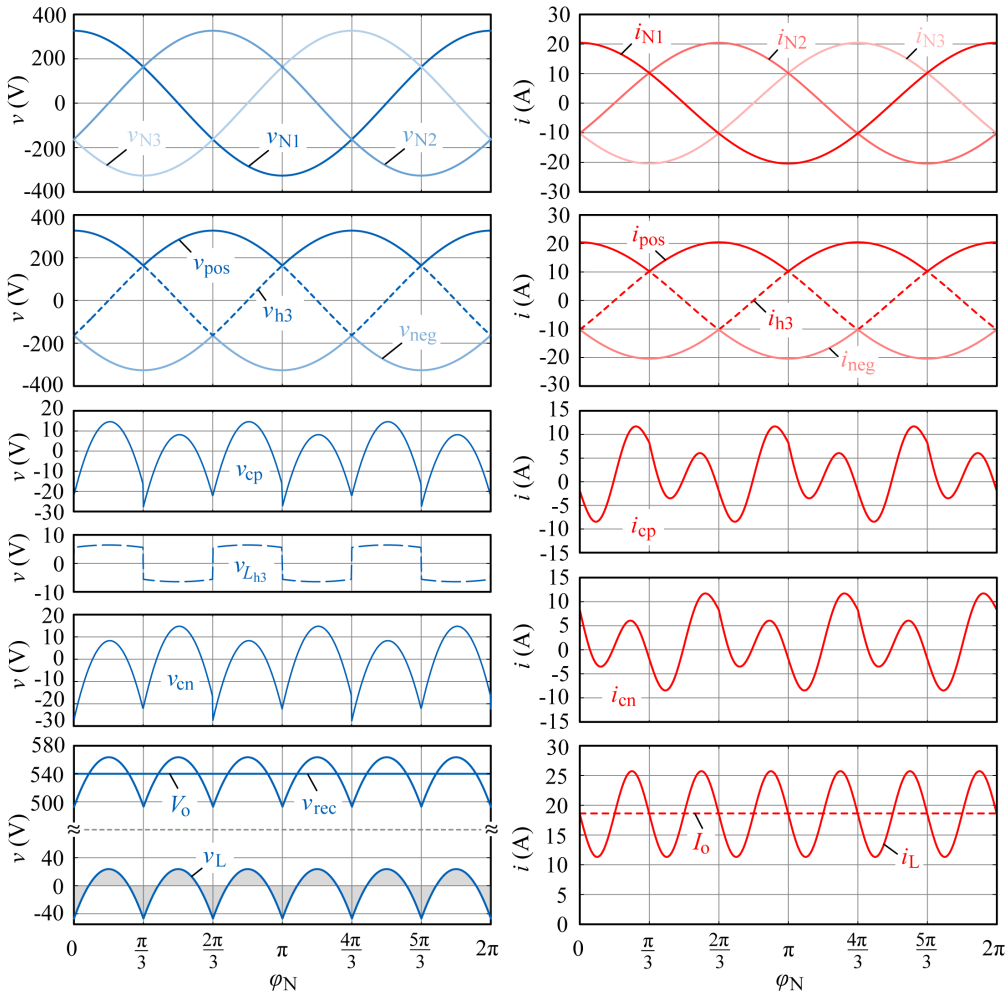


Fig. 4.2: Current and voltage waveforms for a 10 kW active third harmonic injection rectifier, with a DC-side choke L_{DC} of 2.25 mH and assumed 1 mH injection inductors L_{cp}, L_{h3}, L_{cn}.

For proper evaluation of averaged (avg) and root mean square (rms) values, the fundamental equations

$$x_{avg}(\varphi_N) = \frac{1}{2\pi}\int_0^{2\pi} x(\varphi_N)\, d\varphi_N. \tag{4.13}$$

and

$$x_{rms}(\varphi_N) = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} [x(\varphi_N)]^2\, d\varphi_N}. \tag{4.14}$$

have been used, whereas 2π denotes a full mains period.
The mains phase voltages are defined by

$$v_{N1} = \hat{V}_N \cos(\varphi_N) \tag{4.15}$$

$$v_{N2} = \hat{V}_N \cos\left(\varphi_N - \frac{2\pi}{3}\right) \tag{4.16}$$

$$v_{N3} = \hat{V}_N \cos\left(\varphi_N - \frac{4\pi}{3}\right) \tag{4.17}$$

whereas $\hat{V}_\mathrm{N}$ conforms with

$$\hat{V}_\mathrm{N} = \sqrt{\frac{2}{3}} \cdot V_\mathrm{LL,rms}. \tag{4.18}$$

If proper current control of the third harmonic injection device is assumed, the mains input currents basically resemble the mains voltage waveforms and only vary by a constant factor. This constant factor is introduced and denoted as "equivalent conductance value" g_e. The mains input currents can therefore be described by

$$i_\mathrm{N1} = g_\mathrm{e}\hat{V}_\mathrm{N}\cos(\varphi_\mathrm{N}) = \hat{I}_\mathrm{N}\cos(\varphi_\mathrm{N}) \tag{4.19}$$

$$i_\mathrm{N2} = g_\mathrm{e}\hat{V}_\mathrm{N}\cos\left(\varphi_\mathrm{N} - \frac{2\pi}{3}\right) = \hat{I}_\mathrm{N}\cos\left(\varphi_\mathrm{N} - \frac{2\pi}{3}\right) \tag{4.20}$$

$$i_\mathrm{N3} = g_\mathrm{e}\hat{V}_\mathrm{N}\cos\left(\varphi_\mathrm{N} - \frac{4\pi}{3}\right) = \hat{I}_\mathrm{N}\cos\left(\varphi_\mathrm{N} - \frac{4\pi}{3}\right) \tag{4.21}$$

with $\hat{I}_\mathrm{N} = g_\mathrm{e}\hat{V}_\mathrm{N}$. In order to verify g_e, the output power quantities I_o and V_o have to be derived in advance. Therefore, the proposed rectifier system does not offer a controlled output voltage. The output voltage is hence defined according to the mains voltage situation. The B6 output voltage v_rec is defined by

$$v_\mathrm{rec} = v_\mathrm{pos} - v_\mathrm{neg} \tag{4.22}$$

which results in an averaged output voltage (according to **Eq. 3.11**) of

$$V_\mathrm{o} = \frac{3\sqrt{3}}{\pi}\hat{V}_\mathrm{N} \tag{4.23}$$

of the total system. If losses of actives and passives are neglected, it can be assumed that the required input power is going to be transferred to the output without any deficiency ($P_\mathrm{o} = P_\mathrm{in}$). If a constant power load is assumed, the output current calculates to

$$V_\mathrm{o}I_\mathrm{o} = 3V_\mathrm{N,rms}I_\mathrm{N,rms}, \tag{4.24}$$

$$I_\mathrm{o} = \frac{3\hat{V}_\mathrm{N}\hat{I}_\mathrm{N}}{2V_\mathrm{o}}, \tag{4.25}$$

$$I_\mathrm{o} = \frac{\pi}{2\sqrt{3}}\hat{I}_\mathrm{N}. \tag{4.26}$$

If the equivalent conductance value g_e is per definition $\hat{I}_\mathrm{N}/\hat{V}_\mathrm{N}$, it can now be converted into term which is related to the required output power

$$g_\mathrm{e} = \frac{\hat{I}_\mathrm{N}}{\hat{V}_\mathrm{N}} \cdot \frac{\hat{V}_\mathrm{N}}{\hat{V}_\mathrm{N}} = \frac{P_\mathrm{o}}{3V_\mathrm{N,rms}^2}. \tag{4.27}$$

For unbalanced mains voltages, the denominator of the term has to be adapted and results in

$$g_\mathrm{e} = \frac{P_\mathrm{o}}{\sum_{i=1}^{3} V_\mathrm{Ni,rms}^2}. \tag{4.28}$$

As g_e is now defined, the positive and negative busbar currents i_pos and i_neg can examined in more detail. As already known, i_pos and i_neg have to show 120° sections with sinusoidal shape to finally achieve sinusoidal mains currents. These wave shapes are given by

$$i_\mathrm{pos} = g_\mathrm{e}\hat{V}_\mathrm{N}\cos(\varphi_\mathrm{N}) \qquad \varphi_\mathrm{N} \in [0\ldots\pi/3] \tag{4.29}$$

$$i_\mathrm{pos} = g_\mathrm{e}\hat{V}_\mathrm{N}\cos\left(\varphi_\mathrm{N} - \frac{2\pi}{3}\right) \qquad \varphi_\mathrm{N} \in [\pi/3\ldots\pi] \tag{4.30}$$

$$i_\mathrm{pos} = g_\mathrm{e}\hat{V}_\mathrm{N}\cos\left(\varphi_\mathrm{N} - \frac{4\pi}{3}\right) \qquad \varphi_\mathrm{N} \in [\pi\ldots5\pi/3] \tag{4.31}$$

$$i_\mathrm{pos} = g_\mathrm{e}\hat{V}_\mathrm{N}\cos(\varphi_\mathrm{N}) \qquad \varphi_\mathrm{N} \in [5\pi/3\ldots2\pi] \tag{4.32}$$

and

$$i_\mathrm{neg} = g_\mathrm{e}\hat{V}_\mathrm{N}\cos\left(\varphi_\mathrm{N} - \frac{4\pi}{3}\right) \qquad \varphi_\mathrm{N} \in [0\ldots2\pi/3] \tag{4.33}$$

$$i_\mathrm{neg} = g_\mathrm{e}\hat{V}_\mathrm{N}\cos(\varphi_\mathrm{N}) \qquad \varphi_\mathrm{N} \in [2\pi/3\ldots4\pi/3] \tag{4.34}$$

$$i_\mathrm{neg} = g_\mathrm{e}\hat{V}_\mathrm{N}\cos\left(\varphi_\mathrm{N} - \frac{2\pi}{3}\right) \qquad \varphi_\mathrm{N} \in [4\pi/3\ldots2\pi] \tag{4.35}$$

for one mains period. The averaged and rms values of both current waveforms i_pos and i_neg thus easily calculate to (by applying **Eq. 4.13** and **Eq. 4.14**)

$$I_\mathrm{pos,avg} = \hat{I}_\mathrm{N}\frac{3\sqrt{3}}{2\pi}, \qquad I_\mathrm{pos,rms} = \hat{I}_\mathrm{N}\sqrt{\frac{4\pi+3\sqrt{3}}{8\pi}}, \tag{4.36}$$

$$I_\mathrm{neg,avg} = -\hat{I}_\mathrm{N}\frac{3\sqrt{3}}{2\pi}, \qquad I_\mathrm{neg,rms} = \hat{I}_\mathrm{N}\sqrt{\frac{4\pi+3\sqrt{3}}{8\pi}}. \tag{4.37}$$

The positive and negative busbar peak current values equal the input current peak value ($\hat{I}_\mathrm{pos} = -\hat{I}_\mathrm{neg} = \hat{I}_\mathrm{N}$). In a next step the third harmonic current i_h3 is going to be determined analytically. As the relation $v_\mathrm{N1} + v_\mathrm{N2} + v_\mathrm{N3} = 0$ applies, the third harmonic voltage results in

$$v_\mathrm{h3} = -v_\mathrm{pos} - v_\mathrm{neg} \tag{4.38}$$

and therefore i_h3 can be assessed and results in

$$i_\mathrm{h3} = g_\mathrm{e}v_\mathrm{h3} = -g_\mathrm{e}v_\mathrm{pos} - g_\mathrm{e}v_\mathrm{neg} = -i_\mathrm{pos} - i_\mathrm{neg}. \tag{4.39}$$

Major characteristics as averaged, peak and rms value of i_h3 are therefore defined by

$$I_\mathrm{h3,avg} = 0\,\mathrm{A}, \quad \hat{I}_\mathrm{h3} = \frac{\hat{I}_\mathrm{N}}{2}, \quad I_\mathrm{h3,rms} = \frac{\hat{I}_\mathrm{N}}{2}\sqrt{2 - \frac{3\sqrt{3}}{\pi}} \tag{4.40}$$

The DC-side smoothing inductor current i_L is defined by the excited voltage waveforms v_rec and V_o ($v_\mathrm{L} = L_\mathrm{DC}\frac{\mathrm{d}i_\mathrm{L}(\varphi_\mathrm{N})}{\mathrm{d}\varphi_\mathrm{N}}$, with $v_\mathrm{L} = v_\mathrm{rec} - V_\mathrm{o}$). For upcoming calculations and sake of simplicity only the fundamental component of i_L is considered. i_L can therefore be expressed by

$$i_\mathrm{L} = I_\mathrm{o} - \hat{I}_\mathrm{L,ac}\sin(6\varphi_N) \tag{4.41}$$

with the 300 Hz peak current ripple of

$$\hat{I}_{\mathrm{L,ac}} = \frac{3\sqrt{3}\hat{V}_{\mathrm{N}}}{\pi\omega_N L_{\mathrm{DC}}}\left[\sqrt{\left(\frac{\pi}{3}\right)^2 - 1} - \arccos\left(\frac{3}{\pi}\right)\right]. \tag{4.42}$$

Quantities of i_{L} as averaged, peak and rms values are then defined by

$$I_{\mathrm{L,avg}} = \frac{\pi}{2\sqrt{3}}\hat{I}_{\mathrm{N}}, \quad \hat{I}_{\mathrm{L}} = \frac{\pi}{2\sqrt{3}}\hat{I}_{\mathrm{N}} + \hat{I}_{\mathrm{L,ac}}, \quad I_{\mathrm{L,rms}} = \frac{1}{2}\sqrt{\frac{\pi^2}{3}\hat{I}_{\mathrm{N}}^2 + 2\hat{I}_{\mathrm{L,ac}}^2}. \tag{4.43}$$

The output filter capacitor current is characterized by

$$I_{C_{\mathrm{o}},\mathrm{avg}} = 0\,\mathrm{A}, \qquad \hat{I}_{C_{\mathrm{o}},\mathrm{avg}} = \hat{I}_{\mathrm{L,ac}}, \quad \text{and} \quad \hat{I}_{C_{\mathrm{o}},\mathrm{rms}} = \frac{\hat{I}_{\mathrm{L,ac}}}{\sqrt{2}}. \tag{4.44}$$

As already mentioned the injection currents i_{cp} and i_{cn} are defined by

$$i_{\mathrm{cp}} = i_{\mathrm{L}} - i_{\mathrm{pos}} \tag{4.45}$$

$$i_{\mathrm{cn}} = i_{\mathrm{L}} + i_{\mathrm{neg}}. \tag{4.46}$$

Both i_{cp} and i_{cn} show $2\pi/3$-periodicity, due to the sector-wise defined busbar currents i_{pos} and i_{neg}. Averaged and rms current values compute to

$$\begin{aligned} I_{\mathrm{c}\frac{\mathrm{p}}{\mathrm{n}},\mathrm{avg}} &= \hat{I}_{\mathrm{N}}\frac{\sqrt{3}\left(\pi^2 - 9\right)}{6\pi}, \\ I_{\mathrm{c}\frac{\mathrm{p}}{\mathrm{n}},\mathrm{rms}} &= \hat{I}_{\mathrm{N}}\sqrt{\frac{2\pi^3 - 24\pi + 9\sqrt{3}}{24\pi} + \frac{1}{2}\left(\frac{\hat{I}_{\mathrm{L,AC}}}{\hat{I}_{\mathrm{N}}}\right)^2}. \end{aligned} \tag{4.47}$$

As i_{cp} and i_{cn} consist of a combination of constant values and trigonometric functions with different angular frequency, zero crossings and peak values of the respective currents can only be determined numerically. An analytical form is hence only possible if a simple approximation as the Taylor Series for sine and cosine is applied and performed in the following. Using the very compact sigma notation of Taylor Series

$$P_{\mathrm{f}}(x) = \sum_{n=0}^{\infty}\frac{f^{(n)}(a)}{n!}(x-a)^n \tag{4.48}$$

where $n!$ signifies the factorial of n and $f^{(n)}(a)$ denotes the nth derivative of f evaluated at a specific point a, sine and cosine can be approximated with

$$\cos(x) = 1 - \frac{x^2}{2!} + \frac{x^4}{4!} - \frac{x^6}{6!} + \cdots \tag{4.49}$$

$$\sin(x) = x - \frac{x^3}{3!} + \frac{x^5}{5!} - \frac{x^7}{7!} + \cdots. \tag{4.50}$$

As depicted in **Fig. 4.2**, the injection current i_{cp} shows four zero-crossings in the sector $\varphi_{\mathrm{N}} \in \left[-\frac{\pi}{3}\cdots\frac{\pi}{3}\right]$ if

$$i_{\mathrm{cp}}(\varphi_{\mathrm{N}}) = I_{\mathrm{o}} - \hat{I}_{\mathrm{L,ac}}\sin(6\varphi_{\mathrm{N}}) - \hat{I}_{\mathrm{N}}\cos(\varphi_{\mathrm{N}}) = 0\,\mathrm{A} \tag{4.51}$$

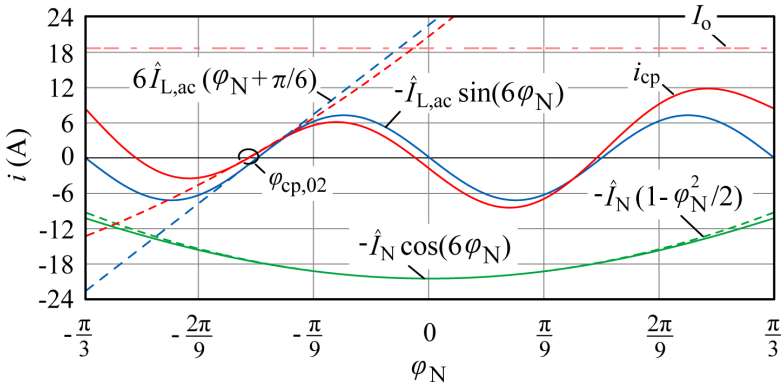


Fig. 4.3: Analyticaly derived zero crossing $\varphi_{cp,02}$ of i_{cp} (red-solid), by piecewise approximation of defined function (applying Taylor Series). Assumed system specifications: $P_o = 10\,\text{kW}$, $V_{LL} = 400\,\text{V}_{rms}$, $L_{DC} = 2.25\,\text{mH}$.

applies. To obtain an applicable analytical form, each cosine must only be approximated to a maximum of grade 2, and each sine of grade 1. If these rules are considered for **Eq. 4.51**, the approximated equation for one zero crossing of i_{cp} (e.g. $\varphi_{cp,02}$) results in

$$I_o + 6\hat{I}_{L,ac}\left(\varphi_N + \frac{\pi}{6}\right) - \hat{I}_N\left(1 - \frac{(\varphi_N)^2}{2}\right) = 0\,\text{A}. \tag{4.52}$$

which is located close to $\varphi_N = -0.5$ in the sector $\varphi_N \in [-\pi/3 \ldots 0]$ (cf., **Fig. 4.3**). The regarded equation finally results in

$$\varphi_{cp,02} = \frac{-6\hat{I}_{L,ac} + \sqrt{2\hat{I}_N^2 - 2\pi\hat{I}_{L,ac}\hat{I}_N - 2\hat{I}_N I_o + 36\hat{I}_{L,ac}^2}}{\hat{I}_N}. \tag{4.53}$$

If the same method is applied for all remaining zero crossings, the following equations can be obtained:

$$\begin{aligned}
\varphi_{cp,01} &= \frac{-9\pi\hat{I}_{L,ac} - \frac{1}{2}\sqrt{8\hat{I}_N^2 + (296 - 9\pi^2)\,\hat{I}_{L,ac}\hat{I}_N - 8I_o\hat{I}_N - 288\hat{I}_{L,ac}\left(\hat{I}_o - \hat{I}_{L,ac}\right)}}{36\hat{I}_{L,ac} + \hat{I}_N} \\
\varphi_{cp,03} &= \frac{6\hat{I}_{L,ac} - \sqrt{2\hat{I}_N^2 - 2\hat{I}_N I_o + 36\hat{I}_{L,ac}^2}}{\hat{I}_N} \\
\varphi_{cp,04} &= \frac{-6\hat{I}_{L,ac} + \sqrt{2\hat{I}_N^2 + 2\pi\hat{I}_{L,ac}\hat{I}_N - 2\hat{I}_N I_o + 36\hat{I}_{L,ac}^2}}{\hat{I}_N}.
\end{aligned} \tag{4.54}$$

Zero crossings of i_{cn} can be derived in the same manner.
Furthermore, it is mandatory to find the peak values of i_{cp} and i_{cn} which are important for a comprehensive choke design. In order to find the local maxima of injection currents i_{cp} and i_{cn},

$$\frac{\partial f\,(x_{max})}{\partial x_{max}} = 0, \qquad f\,(x_{max}) = f_{max} \tag{4.55}$$

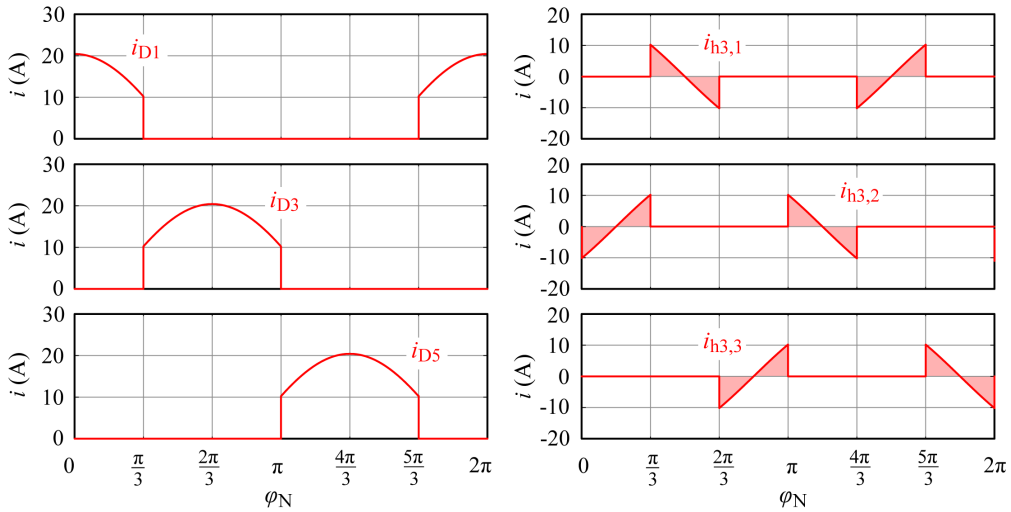


Fig. 4.4: Currents of B6 diode bridge (D_1, D_3, D_5) (employing the THI principle) and third harmonic current wave shapes of current injection network (bidirectional switches connected to phase 1-3) for 10 kW output power.

can be used. For the sector $\varphi_N \in \left[-\frac{\pi}{3} \cdots \frac{\pi}{3}\right]$ (where the maximum value of i_{cp} is expected) the adapted equation results in

$$\frac{\partial i_{cp}(\varphi_{max})}{\partial \varphi_{max}} = -6\hat{I}_{L,ac}\cos(6\varphi_{max}) + \hat{I}_N \sin(\varphi_{max}) = 0 \tag{4.56}$$

if the respective Taylor approximation is utilized. φ_{max} results in

$$\varphi_{max} = \frac{\pi\hat{I}_N - 72\hat{I}_{L,ac}^2 + 2\sqrt{2\hat{I}_N^2 - 18\pi\hat{I}_{L,ac}\hat{I}_N + \left(36\hat{I}_{L,ac}\right)^2}}{2\hat{I}_N}. \tag{4.57}$$

$i_{cp}(\varphi_{max}) = I_{cp,max}$ can now be determined which leads to the local peak current value of

$$\begin{aligned} I_{cp,max} =& I_o - \hat{I}_{L,ac}\left(\frac{9}{8}\pi^2 + 27\pi + 35\right) + \frac{\left(36\hat{I}_{L,ac}\right)^2}{\hat{I}_N}\left(\frac{\pi}{2} + 1\right) - \ldots \\ \ldots &- \frac{\left(36\hat{I}_{L,ac}\right)^3}{\hat{I}_N^2} + \frac{\pi^2}{8}\hat{I}_N + \sqrt{2\hat{I}_N^2 - 18\pi\hat{I}_{L,ac}\hat{I}_N + \left(36\hat{I}_{L,ac}\right)^2} \cdot \ldots \\ \ldots &\cdot \left(\left(\frac{36\hat{I}_{L,ac}}{\hat{I}_N}\right)^2 - \frac{\hat{I}_{L,ac}}{\hat{I}_N}(9\pi + 36) + \frac{\pi}{2}\right). \end{aligned} \tag{4.58}$$

The given equations are only considering the peak current of the 150 Hz signal. The additional switching frequency current ripple is neglected (as infinite inductor values of L_{cp} an L_{cn} are assumed for this evaluation).
As depicted in **Fig. 4.2**, voltage steps are obviously occurring within the waveforms of v_{cp} and v_{cn}. These steps are apparently required in order to follow the abrupt change in sign of the current gradient of i_{pos} during $\varphi_N = \frac{(2k-1)\pi}{3}$ for

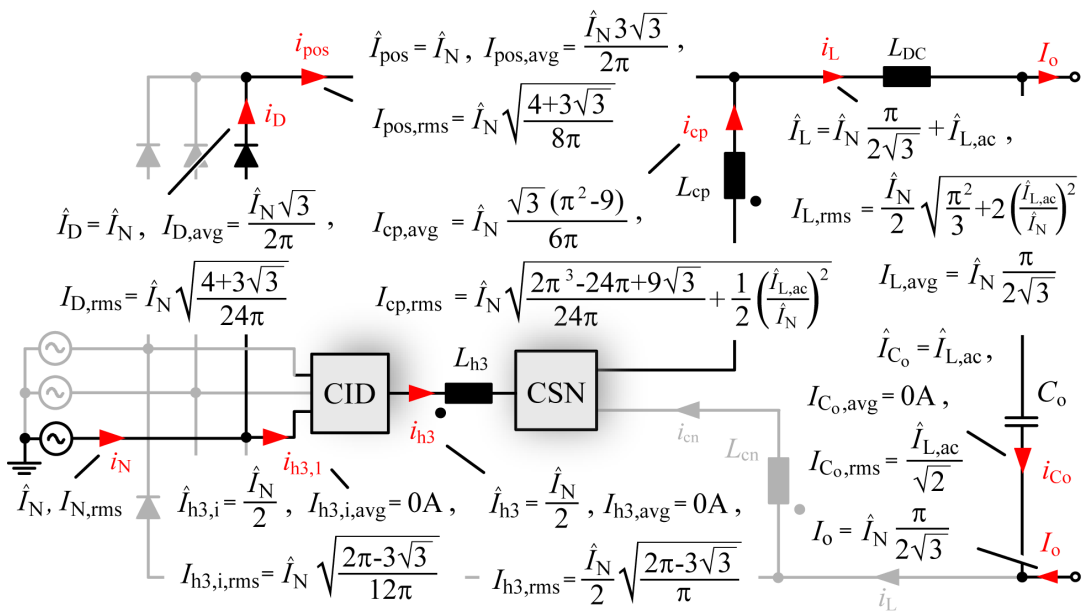


Fig. 4.5: Overview of discussed current stress characteristics of a B6 rectifier with LC output filter, upgraded to an active rectifier based on the third harmonic injection principle.

$k \in \mathbb{Z}$. Hence, the time-dependent derivatives of injection currents show step characteristics at each $\varphi_N = \frac{(2k-1)\pi}{3}$ for $\frac{\mathrm{d}i_{cp}(\varphi_N)}{\mathrm{d}\varphi_N}$ and at $\varphi_N = \frac{2k\pi}{3}$ for $\frac{\mathrm{d}i_{cn}(\varphi_N)}{\mathrm{d}\varphi_N}$.

$$\left.\frac{\mathrm{d}i_{pos}(\varphi_N)}{\mathrm{d}\varphi_N}\right|_{\varphi_N=\frac{\pi}{3}-} < 0 \quad \text{and} \quad \left.\frac{\mathrm{d}i_{pos}(\varphi_N)}{\mathrm{d}\varphi_N}\right|_{\varphi_N=\frac{\pi}{3}+} > 0. \tag{4.59}$$

Since $v_{cp}(\varphi_N)$ and $v_{cn}(\varphi_N)$ are characterized by

$$v_{cp}(\varphi_N) = L_{cp}\frac{\mathrm{d}i_{cp}(\varphi_N)}{\mathrm{d}\varphi_N} \quad \text{and} \quad v_{cn}(\varphi_N) = L_{cn}\frac{\mathrm{d}i_{cn}(\varphi_N)}{\mathrm{d}\varphi_N}, \tag{4.60}$$

an arising step at each 120° sector transitions can be observed. The magnitude of the respective step is linearly dependent on the appropriate injection inductance (L_{cp}, L_{cn}, L_{h3}) and hence smaller inductance values would be preferred. It has to be considered that this effect could lead to minor distortions at each 60° transitions if an inappropriate controller is implemented.

In order to characterize the current stress of B6 rectifier diodes, current waveforms of D_{1-6} have to be evaluated and are depicted in **Fig. 4.4**. The averaged and rms currents thus can be determined to be

$$I_{D1-6,avg} = \hat{I}_N \frac{\sqrt{3}}{2\pi} \tag{4.61}$$

$$I_{D1-6,rms} = \hat{I}_N \sqrt{\frac{4\pi + 3\sqrt{3}}{24\pi}}. \tag{4.62}$$

These results are valid for all six diodes of the three-phase bridge. Compared to a standard passive three-phase rectifier implementation, B6 diodes for the topology

employing THI benefit from a reduced current stress, due to the properly sinusoidal shaped currents.
The third harmonic current i_{h3} is uniformly apportioned to the three bidirectional switches of the current injection device CID. Current waveforms are illustrated in **Fig. 4.4**. As can be seen, each phase has to transfer some small amount of current during those time instants where the standard B6 rectifier (passive rectification) would not conduct current. Averaged and rms current values therefore compute to

$$I_{\mathrm{S1-3,avg}} = 0\,\mathrm{A}, \quad \text{and} \quad I_{\mathrm{S1-3,rms}} = \hat{I}_{\mathrm{N}}\sqrt{\frac{1}{6} - \frac{\sqrt{3}}{4\pi}}. \tag{4.63}$$

Fig. 4.5 finally as an overview illustrates a graphical summary of all discussed major current waveform characteristics (peak, averaged and rms values) of the proposed standard passive three-phase rectifier with LC filter output filter utilizing an active rectifier based on the third harmonic injection principle.

4.3 Input Filter

The following section shortly discusses main considerations for an appropriate input filter design of a B6 rectifier enhanced by an optional active third harmonic injection circuit. Due to the optional active circuitry, the input current i'_{Ni} shows superimposed current components with switching frequency f_{s}. These high frequency current components (f_{s} + multiples of f_{s}) have to be attenuated by an additional input filter, usually a LC filter of at least second order. The filter stage typically consists of a series inductances and shunting capacitors C_{f} in order to block-off switching-frequency noise from the mains terminals. An additional (commonly passive) resistive damping element is required in order to minimize the occurring resonance which is occurring peak at

$$f_{\mathrm{r}} = \frac{1}{2\pi\sqrt{(L_{\mathrm{N}} + L_{\mathrm{f}})\,C_{\mathrm{f}}}}. \tag{4.64}$$

In general parasitic elements as the capacitor's ESR or the series resistance of the inductor would also limit the magnitude of the occurring resonance peak of the LC filter. However, the magnitude of the filter impedance usually is still quite large in regions close to the resonant frequency f_{r}. **Fig. 4.6** therefore illustrates several common single stage LC filter topologies including feasible passive damping solutions as additional damping resistance R_{f} across C_{f} or L_{f}, R_{S}-C_{S} parallel damping, R_{f}-L_{b} parallel damping or R_{f}-L_{b} series damping. Obviously, a simple resistance in parallel to the output capacitance appears to be a very simple solution for passive damping (**Fig. 4.6(top, right)**). Unfortunately, the power dissipation in R_{f} is much higher than for all the other topologies as the mains input voltage is permanently applied across R_{f}.
If a R_{S}-C_{S} parallel damping circuit is used, losses can be reduced and the additional filter inductance L_{f} can be omitted, if the mains input impedance is already

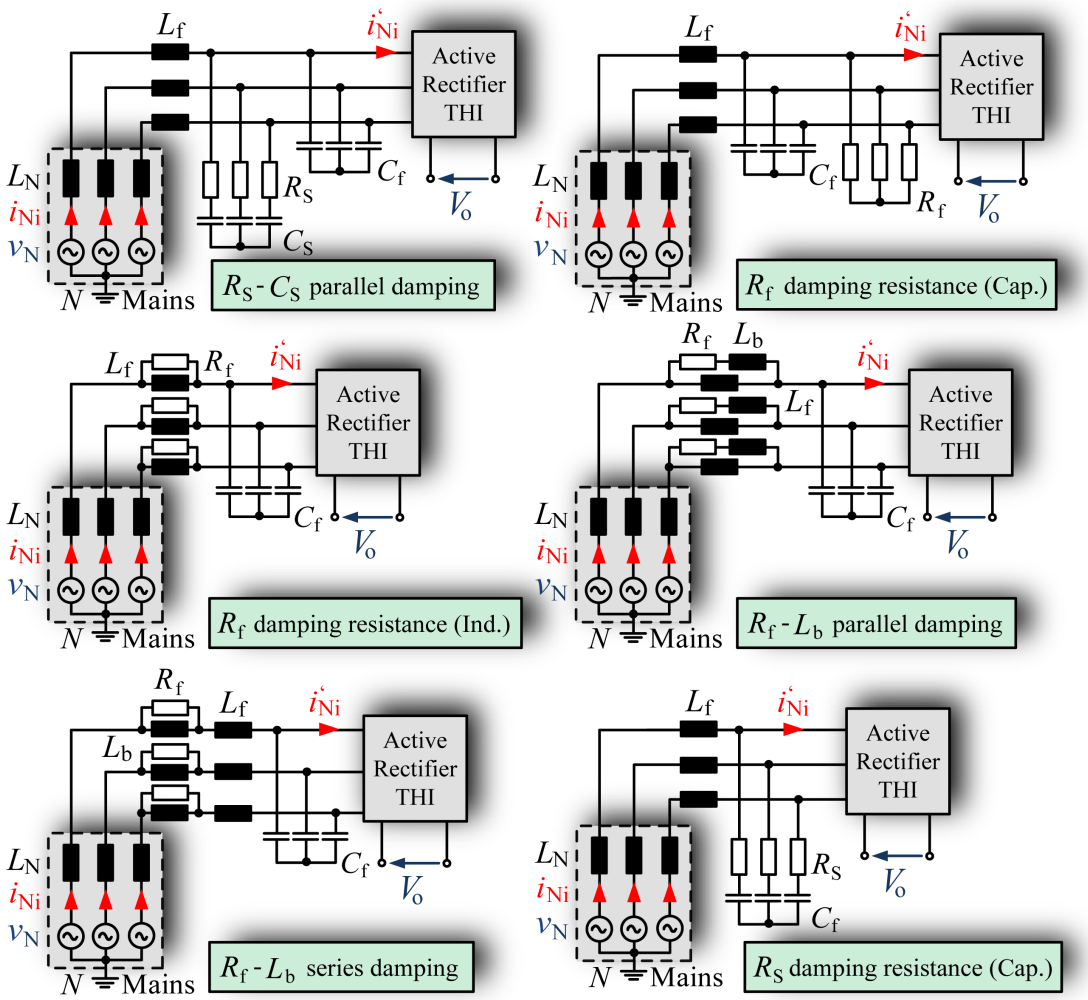


Fig. 4.6: Several common single stage filter topologies including feasible passive damping solutions as additional damping resistance R_f across C_f or L_f, R_S-C_S parallel damping, R_f-L_b parallel damping or R_f-L_b series damping as discussed in [108, 109].

precisely identified and of sufficient value. This may be of interest if a volume optimized design of the input filter is required. A RC-snubber circuit hence seems to be a feasible opportunity for LC input filter damping. The required filter stage is therefore assumed to consist of a $L_N C_f$-tank (consisting of mains impedance Z_N and filter capacitor C_f) and is equipped by a $R_S C_S$ parallel damping snubber circuit. C_S denotes the snubber capacitor, R_S the appropriate snubber resistor, C_f (=C_F) the filter capacitor and L_N the inductance value of the line-impedance. The simplified transfer function (for e.g. phase 1), neglecting capacitor ESR value and the ohmic part of the mains input impedance results in

$$G_{\text{filt}}(s) = \frac{i_{N1}(s)}{i'_{Ni}(s)} = \frac{1 + sR_S C_S}{1 + sR_S C_S + s^2 L_N (C_S + C_F) + s^3 C_S C_F R_S L_N} \tag{4.65}$$

and the output impedance Z_o

$$Z_o(s) = \frac{sL_N + s^2 R_S C_S L_N}{1 + sR_S C_S + s^2 L_N (C_S + C_F) + s^3 R_S C_S C_F L_N}. \tag{4.66}$$

A typical design approach to evaluate the required snubber components for the above two frequency characteristics would be to define the filter components close to a third order butterworth characteristic which results in

$$G_1 G_2 = \frac{1}{1+s} \cdot \frac{1}{1+s+s^2} = \frac{1}{1+2s+2s^2+s^3}, \tag{4.67}$$

i.e., normalized poles are located at $p_1 = -1$ and $p_{2,3} = -1/2 \pm j\sqrt{3}/2$. By equating polynomial coefficients the following dimensioning rules can be obtained:

$$C_\mathrm{S} = 3C_\mathrm{F}, \quad R_\mathrm{S} = \sqrt{\frac{8}{9}} Z_\mathrm{0f}, \quad Z_\mathrm{0f} = R_\mathrm{0f} = \sqrt{\frac{L_\mathrm{N}}{C_\mathrm{F}}}\,. \tag{4.68}$$

It has to be considered, that the regarded filter cut off frequency (f_C) needs to be much lower than the switching frequency (e.g. $f_\mathrm{C} = f_\mathrm{S}/10$) to achieve sufficient noise attenuation. Low switching frequencies therefore tend to tremendously enlarge the required filter volume due to high capacitor values which have to sustain mains voltage levels including high peak surges. Attenuation of the switching frequency current is guaranteed only if at least

$$C_\mathrm{F} > \frac{1}{4\pi^2 f_\mathrm{S}^2 L_\mathrm{N}} \tag{4.69}$$

applies. Just to give a simple example, the minimum filter capacitor for a 10 kHz switching prototype with a line inductance of (e.g.) 60 µH would results in a capacitance value of $C_\mathrm{F} = 4.2\,\mu\mathrm{F}$.
Furthermore it can be concluded that the interconnection between filter capacitance C_F and snubber capacitance C_S is defined by the quantity n_S

$$n_\mathrm{S} = \frac{C_\mathrm{S}}{C_\mathrm{F}} \quad \text{with} \quad n_\mathrm{S,opt} = 3. \tag{4.70}$$

$C_\mathrm{S} = 3C_\mathrm{F}$ only applies for optimal Butterworth damping. If the size of the snubber circuit has to be minimized to improve the filter volume also

$$C_\mathrm{S} = C_\mathrm{F} \tag{4.71}$$

is sufficient. However, it shows increased ringing for current frequency components close to f_C.
A different approach for proper filter design is discussed in [110] and [111]. In this case, not the poles of the system are characterizing the design procedure but the required output impedance Z_o – namely the value of the peak output impedance $|Z_\mathrm{o}|_\mathrm{max}$. The factor n_S can than be found according to

$$n_\mathrm{S} = \frac{R_\mathrm{0f}^2}{|Z_\mathrm{o}|_\mathrm{max}^2} \left(1 + \sqrt{1 + 4\frac{|Z_\mathrm{o}|_\mathrm{max}^2}{R_\mathrm{0f}^2}}\right) \tag{4.72}$$

whereas R_0f is defined by

$$R_\mathrm{0f} = \sqrt{\frac{L_\mathrm{f}}{C_\mathrm{f}}}. \tag{4.73}$$

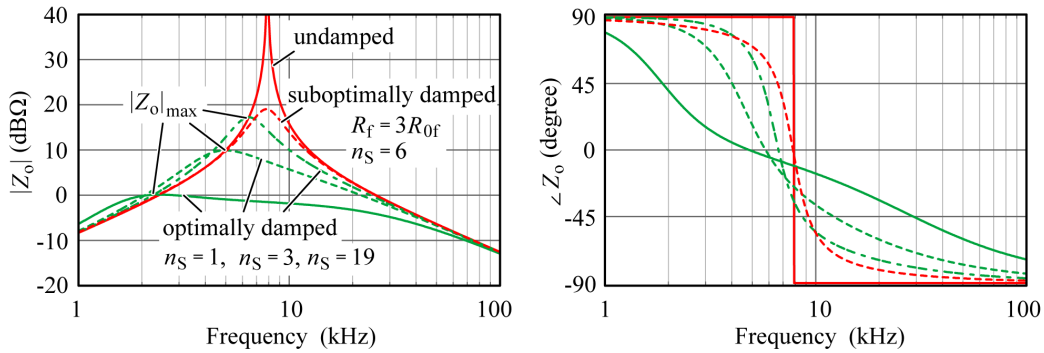


Fig. 4.7: Ouput impedance Z_o and appropriate phase diagram for different snubber circuit implementations (optimal and suboptimal damped). A set of assumed maximum values $|Z_\mathrm{o}|_\mathrm{max} = \left[\sqrt{6},\ \sqrt{\frac{10}{9}},\ \sqrt{42}/19\right] \cdot R_\mathrm{0f}$ has been considered.

The value of the dedicated snubber resistance R_S can then be derived and results in

$$R_\mathrm{S} = R_\mathrm{0f}\sqrt{\frac{(2+n_\mathrm{S})\,(4+3n_\mathrm{S})}{2n_\mathrm{S}^2\,(4+n_\mathrm{S})}}. \tag{4.74}$$

Again a simple example for illustrating this approach is given. It is assumed that the filter was designed for $L_\mathrm{N} = 60\,\mu\mathrm{H}$ which results in a filter capacitance of $6.8\,\mu\mathrm{F}$ for $|G\,(j\omega_\mathrm{S})| \approx -4\mathrm{dB}$ damping of a 10 kHz current ripple (which seems to be sufficient in the case at hand due to a rather high chosen value of the injection inductances L_cp, L_cn and L_h3). R_0f hence results in approximately $3\,\Omega$. If a maximum output impedance of e.g. $4\,\Omega$ is required which is located at

$$f_\mathrm{max} = f_\mathrm{r}\sqrt{\frac{2}{2+n_\mathrm{S}}}, \tag{4.75}$$

the quantity n_S is obtained by 2.1 and the snubber resistance is given by $2.6\,\Omega$. These equations furthermore reveal the following correlation:

$$\text{if} \quad n_\mathrm{S} < 3 \quad \rightarrow \quad |Z_\mathrm{o}|_\mathrm{max} > \sqrt{\frac{10}{9}}R_\mathrm{0f} \tag{4.76}$$

$$\text{if} \quad n_\mathrm{S} = 3 \quad \rightarrow \quad |Z_\mathrm{o}|_\mathrm{max} = \sqrt{\frac{10}{9}}R_\mathrm{0f} \tag{4.77}$$

$$\text{if} \quad n_\mathrm{S} > 3 \quad \rightarrow \quad |Z_\mathrm{o}|_\mathrm{max} < \sqrt{\frac{10}{9}}R_\mathrm{0f}. \tag{4.78}$$

In **Fig. 4.7** the output impedance Z_o for different filter implementations (optimal and suboptimal damped) are illustrated for different maximum values $|Z_\mathrm{o}|_\mathrm{max} = \left[\sqrt{6},\ \sqrt{\frac{10}{9}},\ \sqrt{42}/19\right] \cdot R_\mathrm{0f}$.
The input filter output impedance can be a crucial design parameter as this value should always stay much smaller than the converter input impedance Z_i in order not to change the dynamics of the total converter system (and e.g. degrade controller performance).

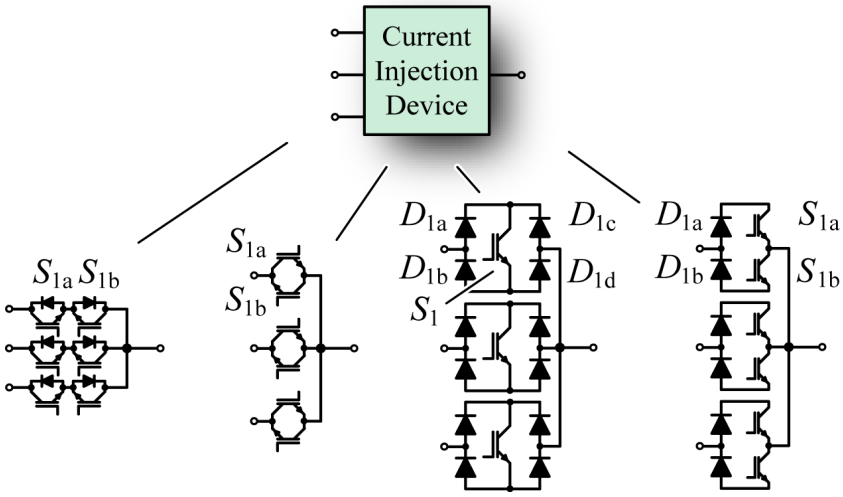


Fig. 4.8: Current injection device implemented as (bidirectional current bipolar voltage switches) either (from left to right) back-to-back, reverse blocking semiconductors, single switch or two switch assembly.

It has to be noted that one drawback of such a discussed filter implementation is the (in most cases) imprecise (or not specified) mains impedance. Furthermore, the mains impedance can vary according to the rectifiers place of installation. Therefore, an additional input inductor could be used for defining the "grid" inductance, at least a minimum value for it.

4.4 The Current Injection Device

The current injection device (CID) forms the interconnection between AC-side input of the passive rectifier and DC-side current shaping network. It is supposed to inject some amount (e.g. i_{N1} in the sector $\varphi_{\mathrm{N}} \in [\pi/3 \ldots 2\pi/3] \cup [4\pi/3 \ldots 5\pi/3]$) of current to guarantee sinusoidal mains currents. As each phase of the CID output shows zero current intervals switching device is required which is able to actively control the injection sequence. The CID therefore consists of three bidirectional switches S_{1-3}. Each bidirectional switch can be implemented (cf., **Fig. 4.8**) as either

- back-to-back IGBTs/SiC MOSFETs (reverse conducting IGBTs applicable, only one DC/DC converter is required for gate drive of both switches because source of both IGBTs shows equal potential)
- reverse blocking IGBTs (resulting in lower conduction losses, however showing increased gate drive implementation effort)
- bidirectional switch using one IGBT/SiC MOSFET and four diodes (high number of semiconductors and furthermore increased conduction losses)
- bidirectional switch using two IGBTs/SiC MOSFETs and two diodes(two

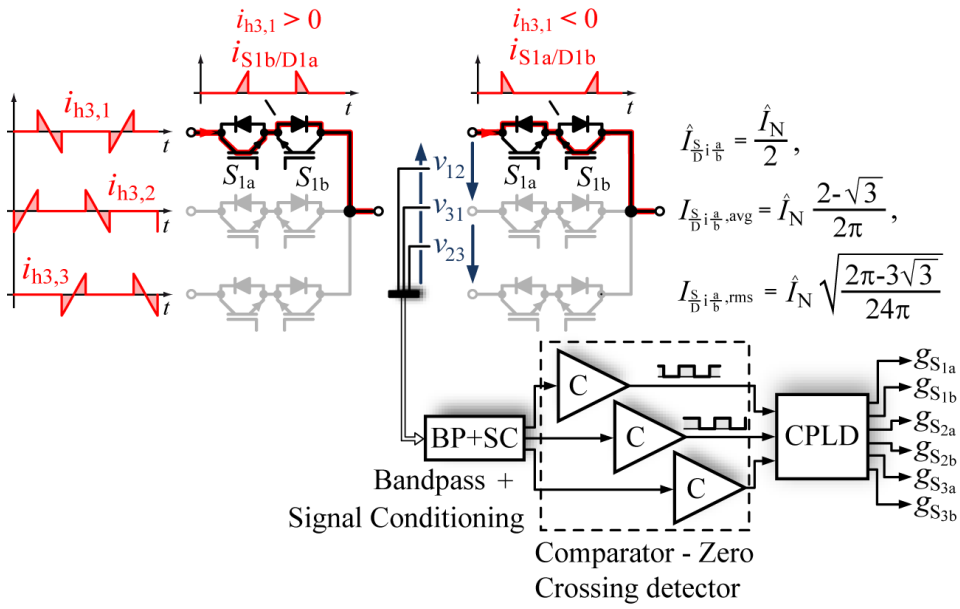


Fig. 4.9: Current waveforms of Diodes and Switches for each bidirectional switch S_{1-3} and control-oriented model of hardware prototype implementation of signal generation for $S_{\frac{S}{D}i\frac{a}{b}}$.

switches and two external diodes necessary).

For further discussions, the back-to-back IGBT formation is going to be evaluated. In order to reduce the conduction losses, reverse conducting IGBTs could be used alternatively [112]. The implemented bidirectional switch circuit is depicted in **Fig. 4.9**. As can be seen, only fractions of the phase current $i_{h3,i}$ are stressing dedicated diodes and switches. If e.g. $i_{h3,1} > 0$, current flow through S_{1a} and D_{1b} appears. For $i_{h3,1} < 0$, D_{1a} and S_{1b} are conducting. The appropriate averaged and rms current values can hence be derived and result in

$$\hat{I}_{S_{Di}^{a}_{b}} = \frac{\hat{I}_N}{2}, \tag{4.79}$$

$$I_{S_{Di}^{a}_{b},avg} = \hat{I}_N \frac{2-\sqrt{3}}{2\pi}, \tag{4.80}$$

$$I_{S_{Di}^{a}_{b},rms} = \hat{I}_N \sqrt{\frac{2\pi-3\sqrt{3}}{24\pi}} \ . \tag{4.81}$$

As each switch is turned-on and -off only twice a period (for a duration of $\pi/3$), devices with large chip-area are applicable (because the switching losses are low despite the semiconductor's capacitance) resulting in low on-state losses. In order to properly control the bidirectional switches a voltage detector circuit to measure line-to-line voltages v_{12}, v_{23}, v_{31} is required. This control circuit mainly transforms the $\pm 565\,\mathrm{V}$ waveforms to a $0\,\mathrm{V}$-$3\,\mathrm{V}$ voltage signal, which is filtered by a (followed) second order bandpass filter. The filtered $50\,\mathrm{Hz}$ signals are now going to be processed by a zero crossing detector (which can be implemented as simple comparator). For all signals $v > 0$ the comparator outputs $v_{comp,i} = 1$. $v < 0$

results in $v_{\text{comp,i}} = 0$. As illustrated in **Fig. 4.10**, the sequence of each bidirectional switch is dependent on a combination of the line-to-line mains voltages. The derived progression is defined by:

$$\begin{aligned} S_{1\text{ab}} = \text{ON}: \quad & v_{12} > 0 \;\&\; v_{31} > 0 \\ & v_{12} < 0 \;\&\; v_{31} < 0 \\ S_{2\text{ab}} = \text{ON}: \quad & v_{12} > 0 \;\&\; v_{23} > 0 \\ & v_{12} < 0 \;\&\; v_{23} < 0 \\ S_{3\text{ab}} = \text{ON}: \quad & v_{23} > 0 \;\&\; v_{31} > 0 \\ & v_{23} < 0 \;\&\; v_{31} < 0\,. \end{aligned}$$

As the control of the bidirectional switches depends on the applied input voltages across the CID, the switching behavior of S_{1-3} (cf., **Fig. 4.9**) is similar to the commutation process of a matrix converter. Hence a four step commutation as described in [113] is required (cf., **Fig. 4.10**).
Thus, the commutation process at a specific time instant (e.g. $\varphi_{\text{N}} \approx 3\pi$ - as shown in **Fig. 4.10**) is discussed.

- **Step 1:** Before the derived sequence is initiated ($\varphi_{\text{N}} < 3\pi$) phase 3 is conducting current. Hence, $S_{3\text{ab}} = \text{ON}$, $v_{31} > 0$, $v_{23} > 0$, $i_{\text{h3,3}} > 0$ and $i_{\text{h3,3}} = i_{\text{h3}}$ applies.
- **Step 2:** As $S_{3\text{b}}$ is currently not conducting current it can be turned OFF in advance. If the applied voltage v_{23} changes in sign or equals $\approx 0\,\text{V}$ the passive three-phase rectifier diodes start to commutate current from (mains) phase 2 to phase 3. Consequently, the CPLD has to initiate the current commutation of the bidirectional switches from (CID) phase 3 to phase 2.
- **Step 3:** Therefore, the appropriate switch which would be able to conduct positive currents ($i_{\text{h3,2}} > 0$) is going to be turned ON. The current now commutates (according to the existing parasitic inductance values and mains voltage levels) from (CID) phase 3 to phase 2.
- **Step 4:** If the commutation process is not finished after a specific time instant, the remaining switch $S_{3\text{a}}$ is turned OFF and the current i_{h3} is then forced to flow through $S_{2\text{a}}$ and $D_{2\text{b}}$ (hard switching operation).
- **Step 5:** The remaining IGBT of phase 2 $S_{2\text{b}}$ can now be turned ON.
- **Step 6:** If $i_{\text{h3,2}}$ ($= i_{\text{h3}}$) changes in sign, the current is stressing $S_{2\text{b}}$ and $D_{1\text{a}}$. One sequence of the CID is hence completed and an upcoming current commutation from (CID) phase 2 to phase 1 can be expected, which will restart this multiple step commutation sequence (step1).

It is important to notice that the commutation process has to be initiated rapidly as the commutation of the bidirectional switches should ideally start at the same time instant when the passive diode bridge starts their commutation (between two different phase legs). If there is a small delay, current peaks are occurring at the input. These peaks have to be attenuated by the input filter and consequently

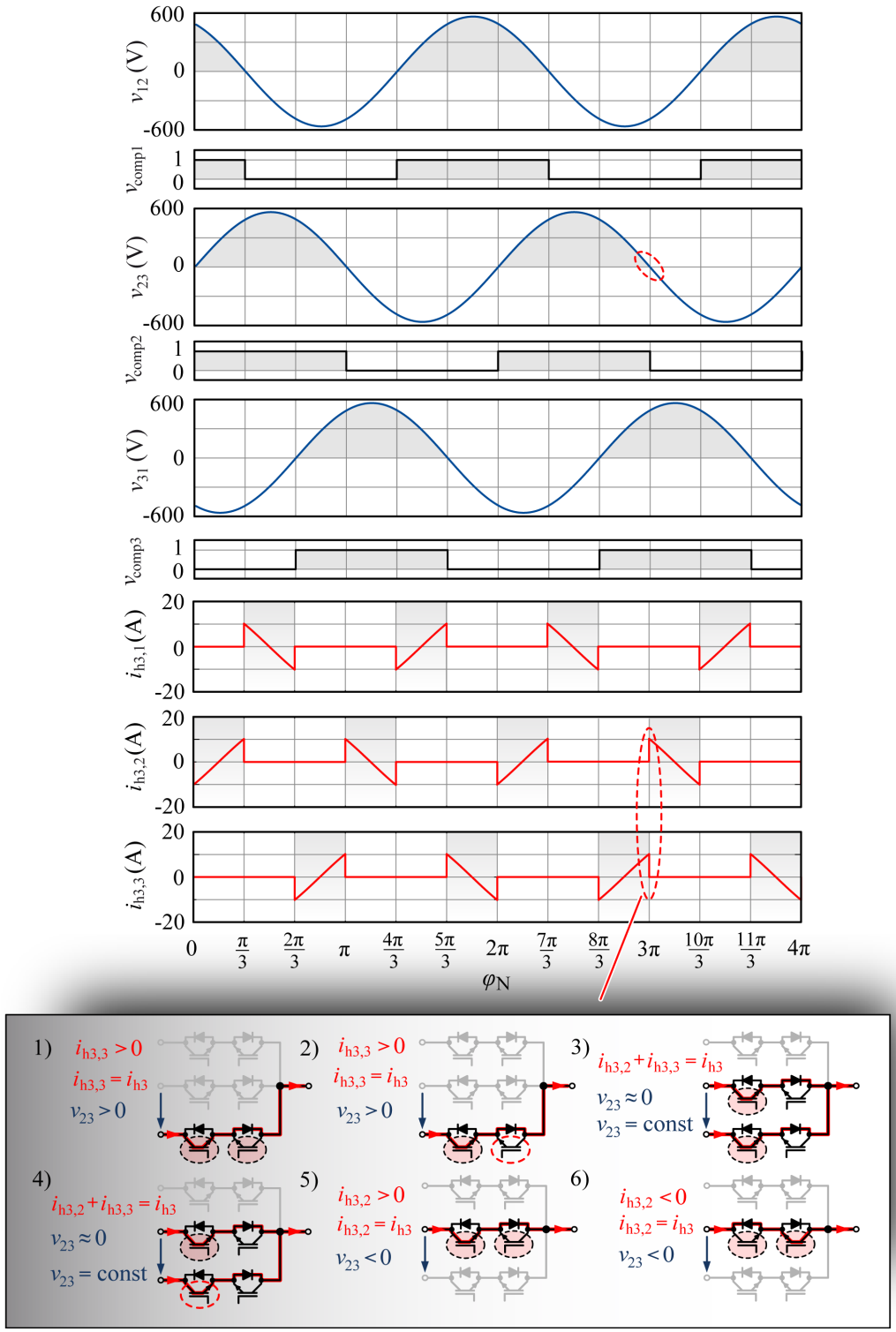


Fig. 4.10: Input line-to-line voltages v_{12},v_{23}, v_{31}, dedicated CID phase currents $i_{\mathrm{h3,1-3}}$ and appropriate comparator output signals $v_{\mathrm{comp,1-3}}$. A multi-step current commutation sequence known from matrix converters is applied to the CID bidirectional switch assembly.

result in worsened $\mathrm{THD_i}$ values of all three mains currents $i_{\mathrm{N1-3}}$. S_{1-3} can hence not be controlled easily by a digital signal processor (DSP -unless a rather high

switching frequency is applied). Therefore, the bidirectional switch controller has to be implemented as either complex programmable logic device (CPLD) or field programmable gate array (FPGA). These fast updating devices take advantage of parallel computing and hence are able to initiate the commutation process significantly faster than the DSP which is already responsible for system start-up and control, PWM generation etc.

Chapter 5

THI-Rectifier Topologies

In this chapter different active third harmonic injection circuits based on the THI principle (active implementation of current shaping network and current injection device as discussed in [114]) are discussed. The main focus in this chapter relies on the implementation of the CSN and most relevant benefits and drawbacks of the different circuits (see **Fig. 5.1**).

- **Topology A:** This implementation is the most basic solution because the optional DC-side power filter is designed as simple "center-tapped" full-bridge stage. The DC-link is formed by two capacitors C_{cp}, C_{cn} in series with midpoint M connected directly to the injection device. This topology yields lowest complexity of all proposed circuits and is suitable for both high and low switching frequency applications. The semiconductors, however, are stressed with the total DC-link voltage $v_{\mathrm{cp}} + v_{\mathrm{cn}}$. For standard 400 V low-voltage mains (line voltage $\hat{V}_{\mathrm{N}} = 325\,\mathrm{V}$) and expecting a typical modulation index of 0.8125 ($= 3/2 \cdot \hat{V}_{\mathrm{N}}/V_{\mathrm{c}}$) a DC-link voltage of 1200 V ($= v_{\mathrm{cp}} + v_{\mathrm{cn}} = 2V_{\mathrm{c}}$) is required for proper operation and hence at least 1700 V IGBTs would be necessary in practice. It has to be noted that this topology shows the highest current ripple of all proposed solutions as the total DC-link voltage (1200 V) is fully applied to both current injection chokes L_{cp} and L_{cn}.
- **Topology B:** In order to reduce the drawbacks of Topology A, a serial connection of two half-bridges appears to be preferable. Both half-bridge legs (connected individually to C_{cp} and C_{cn}) are now stressed by only 600 V ($v_{\mathrm{cp}} = v_{\mathrm{cn}} = V_{\mathrm{c}}$). Hence, 1200 V IGBTs or SiC-MOSFETs can be used. The two bridge legs can generate bipolar output currents i_{cp}, i_{cn}. The output voltages, however, are uni-polar with respect to the midpoint M (the output voltage of the cell fed by C_{cp}, e.g. is limited to the range $0 \ldots V_{\mathrm{cp}}$). The respective half-bridge connected to L_{cp} has to compensate sinusoidal wave shapes as well as 300 Hz current components due to the DC-side smoothing inductance ($L_{\mathrm{DC}} \neq \infty$) current i_{L}. Considering the non-ideal case ($L_{\mathrm{cp}} \neq 0$) the voltage drop across L_{cp} would result in a negative duty cycle, which

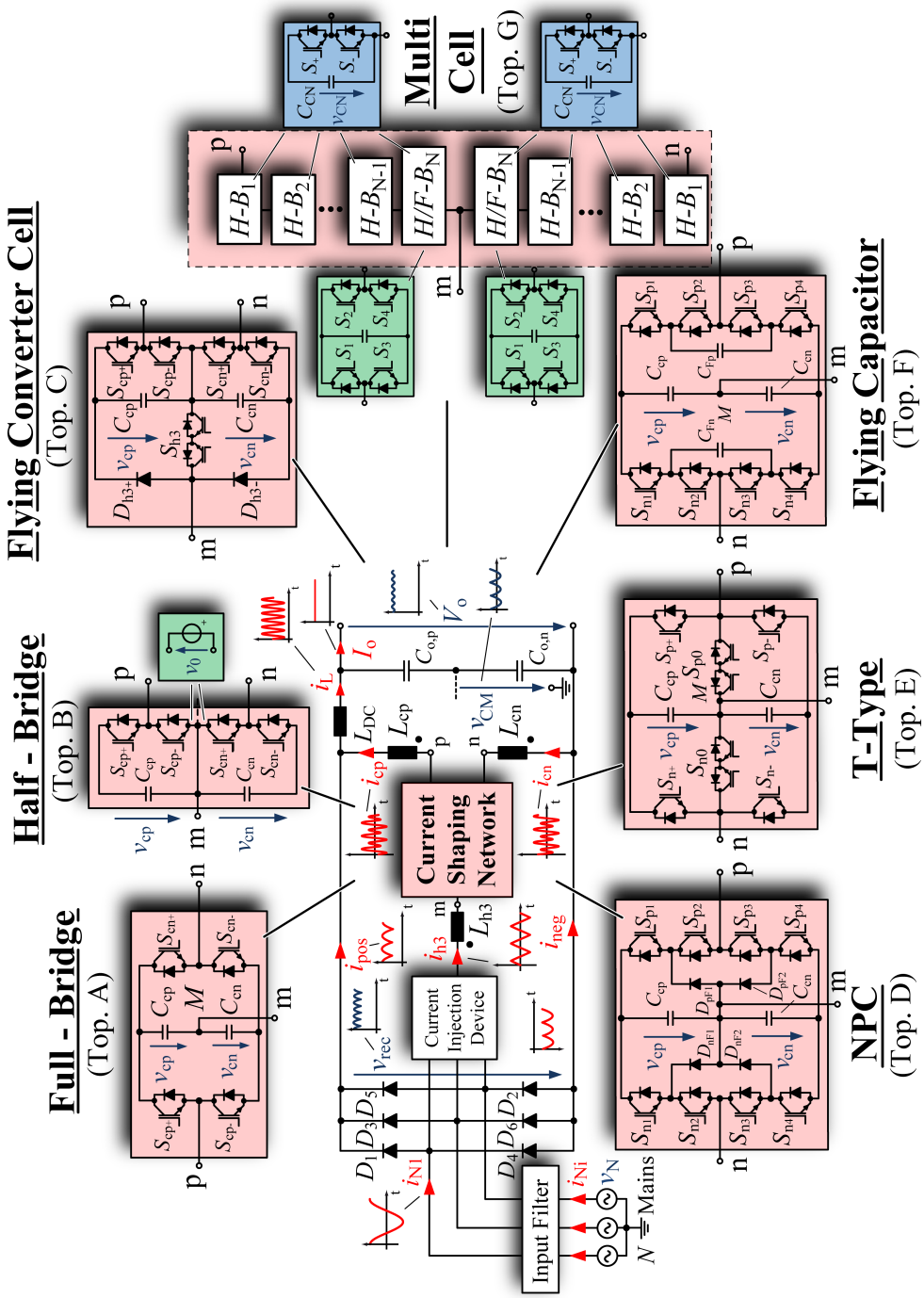


Fig. 5.1: Add-on circuit extensions for passive diode bridge rectifiers based on the 3rd harmonic injection principle. Current shaping network implementation as (Top. A) full bridge converter cell, (Top. B) based on two half-bridges in series connection, (Top. C) as "Flying" Converter Cell Topology, (Top. D-F) based on three-level converter topologies NPC, T-Type or Flying Capacitor, or (Top. G) implemented as Multi-Cell.

however is limited to the range $[0 \ldots 1]$ (0 means upper switch $S_{\mathrm{cp}+}$ opened and lower switch ($S_{\mathrm{cp}-}$) closed and vice versa). Consequently, the voltage drop across L_{cp} and L_{cn} cannot be adjusted by the half-bridges anymore due

to duty cycle limitations which lead to unfavorable distortions in i_{pos}, i_{neg} and subsequently results in augmented input/mains current distortions. This issue can be solved/improved by either increasing the switching frequency f_{s} (which causes depreciated impact of the 300 Hz voltage drop due to reduced injection inductance values ($L_{\mathrm{cp}} \rightarrow 0$ for $f_{\mathrm{s}} \rightarrow \infty$)) or, alternatively, by adding an additional constant voltage source in series to each half-bridge connected to the cell midpoint M. The required voltage drop is defined by mains voltages, injection currents, and DC-side smoothing inductance and calculates to

$$v_0 = \hat{V}_{\mathrm{N}} \frac{L_{\mathrm{c}}}{L_{\mathrm{DC}}} \left(\frac{3}{2} - \frac{3\sqrt{3}}{\pi} \right) - \frac{\sqrt{3}}{2} \omega_{\mathrm{N}} L_{\mathrm{c}} \hat{I}_{\mathrm{N}} \,. \tag{5.1}$$

The proposed additional voltage source could be e.g. implemented as dual active or single active bridge connected to its dedicated half-bridge capacitors (C_{cp} and C_{cn}). With this voltage source, the current shaping cell could operate for a wide frequency range and can still achieve input current distortions of $< 5\,\%$. Two additional converter stages, however, would mean a high increase in complexity due to additional voltage controllers and furthermore a vast number of power semiconductor devices (20 switches instead of 4) is required.

- **Topology C:** Alternatively, in order to optimize the mentioned current distortions and further minimize the DC-voltage level of the shaping cells an unidirectional 3-level bridge can be added, which is directly connected to the current injection network ($S_{\mathrm{i,ab}}$) via L_{h3} – generally referred to as Flying Converter Cell (FCC) Active Rectifier, proposed in [22]. The midpoint voltage v_{MN} now can be controlled such (by an additional voltage controller) that a reduction of the DC-voltage levels from $600\,\mathrm{V_{DC}}$ to $400\,\mathrm{V_{DC}}$ is possible. The additional three-level bridge furthermore allows voltage balancing of both capacitor branches (C_{cp} and C_{cn}) instead of lossy balancing resistors. Due to reduced DC voltages of the FCC, 600 V IGBTs, GaN or SiC switching components are applicable. This topology therefore is also promising for applications which rely on very high switching frequencies (e.g. for systems of very high power density) where the switching losses are dominant in comparison to the conduction losses. Most obvious drawbacks of the FCC are its higher complexity, the increased number of semiconductor components and control effort compared to Topology A and B.
- **Topology D-F:** Input current distortions as appearing for Topology B can be furthermore avoided if the current shaping cell consists of two 3-level converter branches. Feasible circuit opportunities offering satisfying $\mathrm{THD_i}$ characteristics may be e.g. the neutral point clamped (NPC), T-Type or Flying Capacitor three-level converter. All of these proposed 3-level stages result in a $600\,\mathrm{V_{DC}}$ DC-voltage for each cell capacitor.
  The Flying Capacitor 3-level converter solution (Topology F), causes almost twice as much capacitor volume compared to Topologies D and E due to its

additional capacitor banks. Moreover, two further voltage sensors and controllers are necessary in order to guarantee fixed DC voltage levels of both C_{cp}, C_{cn} and C_{Fp}, C_{Fn}.
The T-Type Converter Cell variant (Topology E) yields low complexity and least number of switches compared to D and F. Different to the bidirectional "midpoint-switches" S_{n0}, S_{p0} where 1200 V devices are sufficient, the high-side and low-side semiconductors $S_{\mathrm{n}\pm}$ and $S_{\mathrm{p}\pm}$ have to be implemented as 1700 V IGBTs (including switching transients and safety margins), due to required 600 $\mathrm{V_{DC}}$ DC voltage levels of each cell capacitor. 1700 V devices are necessary as each semiconductor has to block the full DC voltage ($2 \cdot 600\,\mathrm{V_{DC}}$) of the cell which results in reduced attractiveness of this circuit concerning switching losses and switching frequency range of the total active system.
Compared to the Flying Capacitor cell solution, the NPC 3-level converter arrangement (Topology D) shows less capacitor bank volume and advantageously 1200 V IGBTs or SiC-MOSFETs can be applied for all semiconductors. This topology, however, expects the largest number of semiconductors as additional diodes are required to directly clamp the NPC stage to the cell's midpoint potential M.

- **Topology G:** The last topology mentioned is a THI-based circuit implemented as multi-cell converter stage. The current shaping network consists of $2 \cdot N$ half-bridge cells (marked blue) where N denotes the number of half-bridges per injection leg. Optionally, a single switching cell (e.g. the innermost cells connected to the midpoint M marked green) can be designed as full-bridge converter. Due to the additional full-bridge stage it is possible to generate an output voltage of the cell chain which may show minor negative values. Consequently, current distortions originated by the voltage across L_{cp}, L_{cn} and duty cycle limitations finally leading to input/mains current distortions as described before can be avoided. This concept (which can also be implemented such that only two cells, i.e. one full-bridge cell and one half bridge cell, are combined), therefore is of interest especially for low switching frequency applications ($f_{\mathrm{s}} < 20\,\mathrm{kHz}$) or for medium-voltage systems. Advantageously, the N cells are operated in interleaved PWM mode, i.e., the PWM carrier signals have to be phase shifted by $2\pi k/N$ ($k = 1, 2, 3 \ldots N$) resulting in a significant current ripple and/or inductor size reduction due to the ripple cancellation (the maximum current ripple shows a $1/N^2$-dependency). The semiconductor switches of each half/full-bridge are stressed with a DC-link voltage of only $600\,\mathrm{V}/N$. Therefore, the application of ultra-low-$R_{\mathrm{DS,on}}$-low-voltage MOSFETs would be possible for higher values of N, whereas in case of $N = 2$ (or for medium-voltage systems) fast 600 V-IGBTs, SiC-MOSFETs or GaN power switches are applicable. Due to the series arrangement, each converter stage has to process the full current i_{cp} or i_{cn}. Even though the rated DC-link voltage of each half-bridge capacitor bank is reduced, its voltage ripple is mainly defined due to the predominant 300 Hz current ripple.

TABLE 5.1: Overview of proposed topologies concerning applying semiconductor device voltage ratings (V_{DS}), applicable devices (Appl. Dev.) and number of switches and diodes (No. of Sw., D.).

	V_{DC}	**Appl. Dev.**	**No. of Sw., D.**
Top A:	1200 V	I	4, 0
Top B:	600 V	I, S	4, 0
Top C:	400 V (Sw.) 800 V (D.)	I, S, G	6, 2
Top D:	600 V	I, S	8, 4
Top E:	1200 V	I	12, 0
Top F:	600 V	I, S	8, 0
Top G:	600 V/N	I, S, G	4N, 0

The required DC-link capacitance for each cell hence is increasing for an advanced number of cells to achieve equal relative maximum voltage ripple rates.

TABLE 5.1 summarizes the previously mentioned facts on applicable devices (Appl. Dev.), number of switches and diodes (No. of Sw., D.) and required semiconductor voltage ratings (V_{DS}) for a DC-link voltage (V_{c}) of 600 V (Topology A,B,D-G) or 400 V (Topology C). Letters I, S and G denote IGBT, SiC and GaN power devices, respectively.

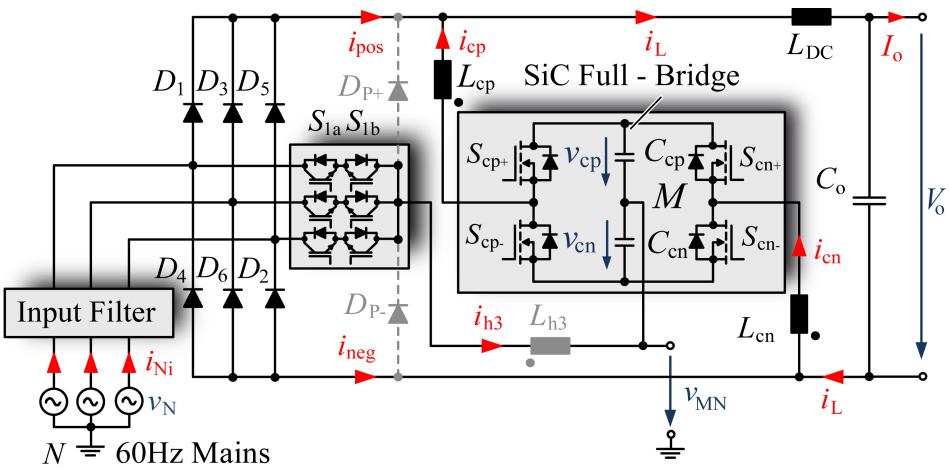


Fig. 5.2: Passive three-phase diode bridge rectifier system employing a "center-tapped" silicon-carbide (SiC) or IGBT full-bridge converter (C_{cp}, C_{cn}), considering either a two (L_{cp}, L_{cn}) or a three inductor (L_{cp}, L_{h3}, L_{cn}) arrangement.

5.1 CSN Implementation - Full Bridge

One feasible realization of the third harmonic injection circuit is an implementation of the CSN as "center tapped" full bridge converter (Topology A of **Fig. 5.1**). **Fig. 5.2** depicts the proposed hybrid rectifier system ([115]) equipped with an optional full-bridge (as e.g. presented in [116–119]) enhancement based on the third harmonic injection principle. This novel low frequency harmonic suppression unit stands out due to simplicity, low number of switches and is applicable for both high and low-power applications. As however stated in the previous section, a line-to-line voltage of 400 V_{LL} however requires 1700 V switching devices. Detailed analyses revealed that this third harmonic injection topology is therefore very well suited for supply grids of lower voltage level (i.e. 200 V_{LL} – 220 V_{LL}) mains.

5.1.1 Full-Bridge Characteristics

Due to its low complexity the full-bridge converter is an attractive power electronics topology which is a common standard in industry applications. Active components are available as combined power modules from several manufacturers. The full-bridge topology is, furthermore, integrated in well-known power stages as the dual active bridge or AC-DC multi-cell arrangements.
It hence appears to be attractive to serve as active current suppression *extension/option* for three-phase low-voltage applications.
Additional diodes ($D_{P\pm}$, connected to the positive and negative busbar of the rectifier) are highly recommended to be integrated as they are offering an alternative current path to prevent either irreversible damage of coil or injection network if the injection device is forced to stop operation due to some kind of fault detection.
The CSN is designed as simple "center-tapped" (concerning "mid-point" M) full-

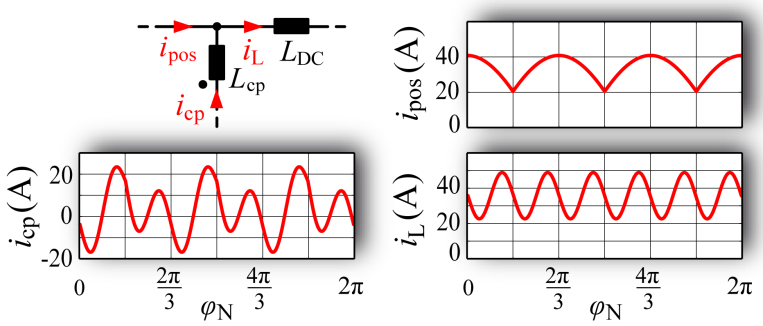


Fig. 5.3: Calculated current waveforms i_{pos}, i_{cp} and i_L of the 10 kW hybrid rectifier full-bridge topology for 208 V_{LL}/60 Hz input characteristics.

bridge stage and injects current i_{cp}, i_{cn} into the positive and negative busbar of the B6 rectifier (cf., **Fig. 5.3**). The DC-link of the converter is formed by two capacitors C_{cp}, C_{cn} in series with midpoint M directly connected to the injection device ($S_{i,ab}$). Considering line-to-line mains voltages of 200 V_{rms} – 220 V_{rms}, a maximum DC-link voltage of 600 V is fully sufficient. Each capacitor C_{cp} and C_{cn}, therefore, has to endure 300 V which allows utilization of 400 V / 450 V electrolytic capacitors (no additional series connection of capacitors required). Furthermore, 900 V IGBTs or Silicon Carbide (SiC) MOSFETs are applicable as the switches are stressed with 600 V DC voltage. As GaN switching devices are only available for 650 V up to now, the utilization of this technology is not possible for the third harmonic injection network at the moment. As, however, discussed in [120], 900 V / 1200 V GaN high voltage/high power devices can be expected to be commercially available within the next years.
As indicated in **Fig. 5.2** a third inductor L_{h3} can be used and is directly located between the midpoint M of the full-bridge stage and the third harmonic injection device. This additional inductor advantageously allows a volume reduced design, if the three independent coils are formed as one coupled (e.g. iron) three-phase choke.
In the following, some basic considerations regarding operation and design of the proposed topology are discussed. The system specifications are defined as

- **Mains Characteristic:** 208 V_{LL}/60 Hz
- **DC-link Voltage:** $V_{cp} = V_{cn} = 300$ V
- **Switching Frequency:** $f_s = 10$ kHz.

A rather low switching frequency of 10 kHz has been chosen for improved efficiency of the system. The duty cycle of the positive switch S_{cp+} assigned to the injection choke L_{cp} can be assessed by

$$\delta_{cp,L_{h3}} = \frac{1}{2} + \frac{v_{pos} - v_{h3} + v_{L_{cp,LF}}}{V_{c,tot}} + \frac{v_{L_{h3}}}{V_{c,tot}} \,. \tag{5.2}$$

The appropriate duty cycle for the dedicated lower switch (S_{cp-}) can be easily calculated by $1 - \delta_{cp,L_{h3}}$. $V_{c,tot}$ is the total DC voltage $V_{c,tot} = V_{cp} + V_{cn} = 600$ V.

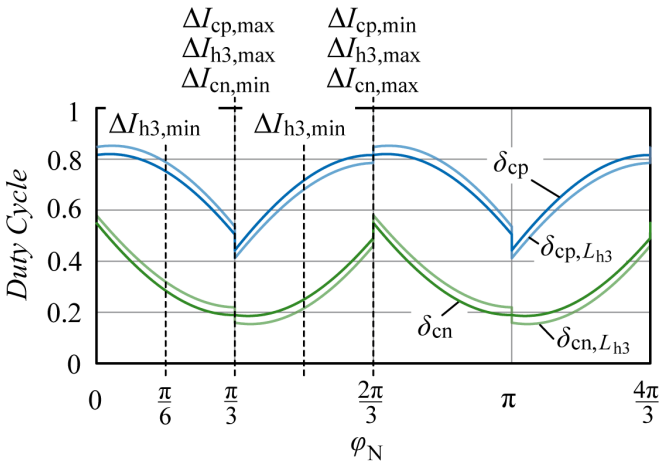


Fig. 5.4: Duty cycles δ_{cp} and δ_{cn} of switches $S_{\mathrm{cp}\pm}$ connected to L_{cp} and switches $S_{\mathrm{cn}\pm}$ connected to L_{cn}, respectively. For an advanced design with implemented third inductance L_{h3}, adapted duty cycles $\delta_{\mathrm{cp},L_{\mathrm{h3}}}$ and $\delta_{\mathrm{cn},L_{\mathrm{h3}}}$ are additionally illustrated. All functions are plotted for 10 kW output power, 208 $\mathrm{V_{LL}}$/60 Hz mains voltages, a DC-side smoothing choke L_{DC} of 500 µH, injection inductance values of $L_{\mathrm{cp}} = L_{\mathrm{cn}} = L_{\mathrm{h3}}$ of 800 µH and a total DC-link voltage $V_{\mathrm{c,tot}} = 600\,\mathrm{V}$.

$\delta_{\mathrm{cp},L_{\mathrm{h3}}}$ is the duty cycle of $S_{\mathrm{cp}+}$ considering an additional inductance L_{h3}. This additional coil L_{h3} results in an additional voltage drop $v_{L_{\mathrm{h3}}}$ which has to be compensated by both half-bridges. The duty cycle of the half bridge connected to the negative output of the passive rectifier ($S_{\mathrm{cn}\pm}$), similarly calculates to

$$\delta_{\mathrm{cn},L_{\mathrm{h3}}} = \frac{1}{2} + \frac{v_{\mathrm{neg}} - v_{\mathrm{h3}} + v_{L_{\mathrm{cn,LF}}}}{V_{\mathrm{c,tot}}} + \frac{v_{L_{\mathrm{h3}}}}{V_{\mathrm{c,tot}}}\,. \tag{5.3}$$

Duty cycles for both switches $S_{\mathrm{cp}+}$ and $S_{\mathrm{cn}+}$ are illustrated in **Fig. 5.4** (duty cycles δ_{cp} and δ_{cn} for a two inductor arrangement ($L_{\mathrm{h3}} = 0$) are depicted also). As very well known from literature the maximum current ripple of a half-bridge appears at $\delta_{\mathrm{HB}} = \frac{1}{2}$. Considering that only two injection inductors are used ($L_{\mathrm{h3}} = 0$) this is obviously the case if $v_{\mathrm{pos}} = v_{\mathrm{h3}}$ (at $\varphi_{\mathrm{N}} = \pi/3, \pi, \ldots$) and $v_{\mathrm{neg}} = v_{\mathrm{h3}}$ (at $\varphi_{\mathrm{N}} = 0, 2\pi/3, \ldots$) applies, for the half-bridge connected to L_{cp} and L_{cn} respectively.

5.1.2 Comprehensive Inductor Design

As the duty cycles δ_{cp} and δ_{cn} are now available, the dedicated current ripple $\Delta I_{\mathrm{c}\frac{\mathrm{p}}{\mathrm{n}}}(\varphi_{\mathrm{N}})$ can now be derived. Therefore, a specific switching state is assumed (e.g. $S_{\mathrm{cp}+}$ turned-on, $S_{\mathrm{cp}-}$ turned-off). Considering the inductor equation $v_{\mathrm{L}} = L\Delta i_L/\Delta t$, the dedicated current ripple of $\Delta I_{\mathrm{cp}}(\varphi_{\mathrm{N}})$ hence results in

$$\Delta I_{\mathrm{cp}}(\varphi_{\mathrm{N}}) = \frac{-v_{\mathrm{pos}}(\varphi_{\mathrm{N}}) + v_{\mathrm{h3}}(\varphi_{\mathrm{N}}) + V_{\mathrm{cp}}}{L_{\mathrm{cp}} f_{\mathrm{s}}}\,\delta_{\mathrm{cp}}(\varphi_{\mathrm{N}}) \tag{5.4}$$

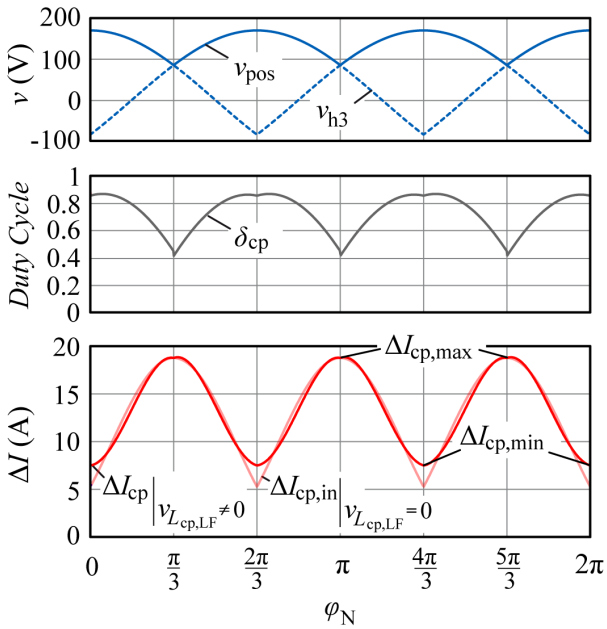


Fig. 5.5: Required voltage and duty cycle waveforms in order to calculate the dependent current ripple waveform of injection leg currents i_{cp} and i_{cn}. Characteristics are depicted for 10 kW output power, 208 V_{LL}/60 Hz mains voltage characteristics, $L_{DC} = 500\,\mu H$, injection inductance values of $L_{cp} = L_{cn} = 800\,\mu H$, $L_{h3} = 0$ and a DC-link capacitor voltage for each branch of $V_{cp} = V_{cn} = 300\,V$.

and $\Delta I_{cn}(\varphi_N)$ computes to

$$\Delta I_{cn}(\varphi_N) = \frac{v_{neg}(\varphi_N) - v_{h3}(\varphi_N) + V_{cn}}{L_{cn} f_s}\left(1 - \delta_{cn}(\varphi_N)\right) . \tag{5.5}$$

However, these peak current ripples $\Delta I_{c\frac{p}{n}}$ include the 150 Hz low frequency current change in i_{cp}, i_{cn}. A very simple solution to get rid of the 150 Hz gradient is to average both ascending (upper switch closed) and decreasing (lower switch closed) current ripple functions over one switching cycle with switching frequency T_s:

- $\Delta I_{cp,in}$ - S_{cp+} closed, S_{cp-} opened
- $\Delta I_{cp,de}$ - S_{cp+} opened, S_{cp-} closed

The switching frequency current ripple then can be calculated and results in

$$\begin{aligned}\Delta I_{cp,f_s}(\varphi_N) &= \frac{|\Delta I_{cp,in}| + |\Delta I_{cp,de}|}{2} \\ &= \frac{|(-v_{pos}(\varphi_N) + v_{h3}(\varphi_N) + V_{cp})\,\delta_{cp}(\varphi_N)|}{2L_{cp} f_s} + \ldots \\ &\ldots + \frac{|(-v_{pos}(\varphi_N) + v_{h3}(\varphi_N) - V_{cp})\,(1 - \delta_{cp}(\varphi_N))|}{2L_{cp} f_s} .\end{aligned} \tag{5.6}$$

The minimum current ripple (as shown in **Fig. 5.5**) is obviously located at $\varphi_N = 0$. The duty cycle as derived in **Eq. 5.2** at $\varphi_N = 0$ results in $\delta_{cp}(0)$ and finally leads

to

$$\delta_{\mathrm{cp}}(0) = \frac{V_{\mathrm{c}} + \frac{3}{2}\hat{V}_{\mathrm{N}} + \sqrt{3}\hat{V}_{\mathrm{N}}\frac{L_{\mathrm{c}}}{L_{\mathrm{DC}}}\left(\frac{\sqrt{3}}{2} - \frac{3}{\pi}\right)}{2V_{\mathrm{c}}}. \tag{5.7}$$

with the averaged voltage $v_{\mathrm{L,cp,LF}}$

$$v_{L_{\mathrm{cp,LF}}}(\varphi_{\mathrm{N}}) = \omega_{\mathrm{N}} L_{\mathrm{c}} \frac{\mathrm{d}\left(i_{\mathrm{L}}(\varphi_{\mathrm{N}}) - i_{\mathrm{pos}}(\varphi_{\mathrm{N}})\right)}{\mathrm{d}\varphi_{\mathrm{N}}} \tag{5.8}$$

$$= -\sqrt{3}\frac{L_{\mathrm{c}}}{L_{\mathrm{DC}}}\hat{V}_{\mathrm{N}}\left(\sin\left(\varphi_{\mathrm{N}} - \frac{2\pi}{3}\right) - \frac{3}{\pi}\right) - \hat{I}_{\mathrm{N}}\sin(\varphi_{\mathrm{N}}) \tag{5.9}$$

$$v_{L_{\mathrm{cp,LF}}}(0) = \frac{L_{\mathrm{c}}}{L_{\mathrm{DC}}}\hat{V}_{\mathrm{N}}\left(\frac{3}{2} - \frac{3\sqrt{3}}{\pi}\right). \tag{5.10}$$

As can be seen, a specific term $L_{\mathrm{c}}/L_{\mathrm{DC}}$ occurs. This term becomes noticeable especially for low switching frequencies where $L_{\mathrm{c}} \approx L_{\mathrm{DC}}$ or $L_{\mathrm{c}} > L_{\mathrm{DC}}$. For high switching frequencies, the size of the injection inductor generally decreases by $1/f_{\mathrm{s}}$ and hence the influence of $L_{\mathrm{c}}/L_{\mathrm{DC}}$ becomes negligibly small ($L_{\mathrm{c}} \ll L_{\mathrm{DC}}$). The minimum and maximum current ripple can be finally calculated which results in

$$\Delta I_{\mathrm{cp},f_{\mathrm{s}},\mathrm{min}} = \frac{V_{\mathrm{c}}\left(1 - M^2 - 2M^2\frac{L_{\mathrm{c}}}{L_{\mathrm{DC}}}\left(\frac{1}{2} - \frac{\sqrt{3}}{\pi}\right)\right)}{2L_{\mathrm{c}}f_{\mathrm{s}}}. \tag{5.11}$$

For the maximum current ripple (at $\varphi_{\mathrm{N}} = \pi/3$), it obviously barely matters if $v_{\mathrm{L,cp,LF}}$ is considered or not, as detailed analyzes showed that

$$\Delta I_{\mathrm{cp},f_{\mathrm{s}},\mathrm{max}} = \max\left[\frac{|\Delta I_{\mathrm{cp,in}}| + |\Delta I_{\mathrm{cp,de}}|}{2}\right]\Bigg|_{v_{L_{\mathrm{cp,LF}}}\neq 0} \approx \tag{5.12}$$

$$\approx \max\left[\frac{|\Delta I_{\mathrm{cp,in}}| + |\Delta I_{\mathrm{cp,de}}|}{2}\right]\Bigg|_{v_{L_{\mathrm{cp,LF}}}=0} = \tag{5.13}$$

$$= \max\left[\Delta I_{\mathrm{cp,in}}\right]\Bigg|_{v_{L_{\mathrm{cp,LF}}}=0}. \tag{5.14}$$

The maximum current ripple of i_{cp} with switching frequency hence calculates to

$$\Delta I_{\mathrm{max}} = \frac{V_{\mathrm{c}}}{2L_{\mathrm{c}}f_{\mathrm{s}}}. \tag{5.15}$$

The calculated minimum and maximum current ripple values for e.g. $V_{\mathrm{LL}} = 208\,\mathrm{V_{rms}}$, $f_{\mathrm{s}} = 10\,\mathrm{kHz}$, $L_{\mathrm{DC}} = 500\,\mu\mathrm{H}$, $L_{\mathrm{c}} = 800\,\mu\mathrm{H}$ and an output power of $P_{\mathrm{o}} = 10\,\mathrm{kW}$ lead to

$$\Delta I_{\mathrm{cp},f_{\mathrm{s}},\mathrm{min}} = 7.49\,\mathrm{A}, \tag{5.16}$$

$$\Delta I_{\mathrm{cp},f_{\mathrm{s}},\mathrm{max}} = 18.75\,\mathrm{A} \tag{5.17}$$

and perfectly conform with the simulated results illustrated in **Fig. 5.6**. It should be mentioned that the maximum current ripple of $i_{\mathrm{N1-3}}$ is much higher than the

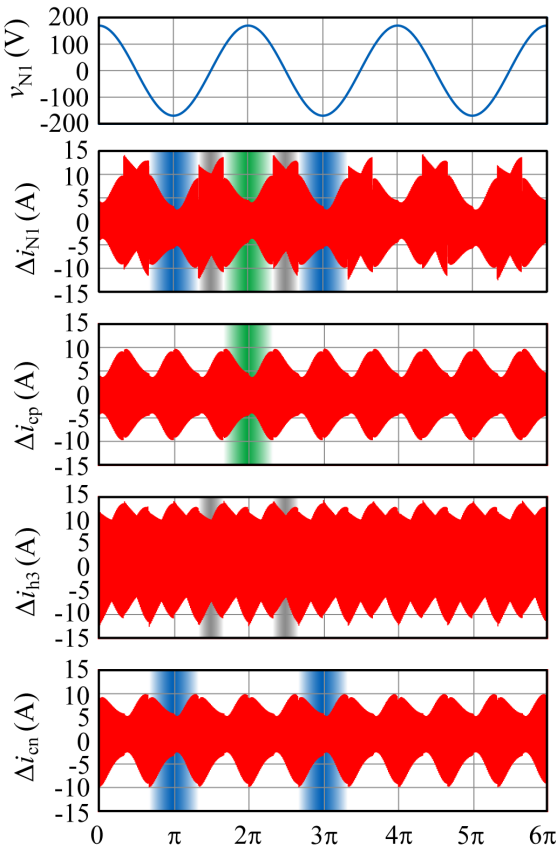


Fig. 5.6: Simulated current ripple information of i_{N1}, i_{cp}, i_{h3} and i_{cn}. The composited mains input current ripple Δi_{N1} consequently consists of parts of injection current ripple waveshapes Δi_{cp} (green shaded area), Δi_{h3} (grey shaded area) and Δi_{cn} (blue shaded area). Simulation results are performed for $P_o = 10\,\text{kW}$, $208\,\text{V}_{LL}/60\,\text{Hz}$ mains voltages, $L_{DC} = 500\,\mu\text{H}$, $L_{cp} = L_{cn} = 800\,\mu\text{H}$, $L_{h3} = 0$, double edge PWM mode and $V_{cp} = V_{cn} = 300\,\text{V}$.

calculated 18.75 A (cf., **Fig. 5.6**) as Δi_{N1-3} consist of parts of injection current ripple wave shapes Δi_{cp} (green shaded area), Δi_{h3} (grey shaded area) and Δi_{cn} (blue shaded area). Obviously, the maximum current ripple of i_{N1} cyclically appears close to the sector boundaries of $\varphi_N = \pi/3,\ 2\pi/3,\ 4\pi/3,\ 5\pi/3, \ldots$. This maximum current ripple of i_{Ni} is evoked due to the current ripple of the cyclically injected current i_{h3}. As already mentioned, i_{h3} is defined by $i_{cp} - i_{cn}$. Therefore the maximum current ripple of i_{Ni} can be determined by

$$\Delta I_{N,f_s,\max} = \Delta I_{h3,f_s,\max} = \Delta i_{cp,f_s} - \Delta i_{cn,f_s,\min} \qquad t \in \left[\frac{T_s}{2} \ldots T_s\right] \tag{5.18}$$

whereas only some fraction of $\Delta i_{cn,f_s,\min}$ is affecting the maximum current ripple of i_{h3} and hence i_{Ni} (cf., **Fig. 5.7** - grey shaded area). Therefore, maximum current ripple of i_{h3} can be evaluated (e.g. at $\varphi_N = \pi/3$) and results in

$$\Delta I_{h3,f_s,\max} = \left(\frac{-v_{pos}\left(\frac{\pi}{3}\right) + v_{h3}\left(\frac{\pi}{3}\right) - V_c}{L_c f_s} - \frac{v_{neg}\left(\frac{\pi}{3}\right) - v_{h3}\left(\frac{\pi}{3}\right) + V_c}{L_c f_s}\right) \delta_{cp}\left(\frac{\pi}{3}\right)$$

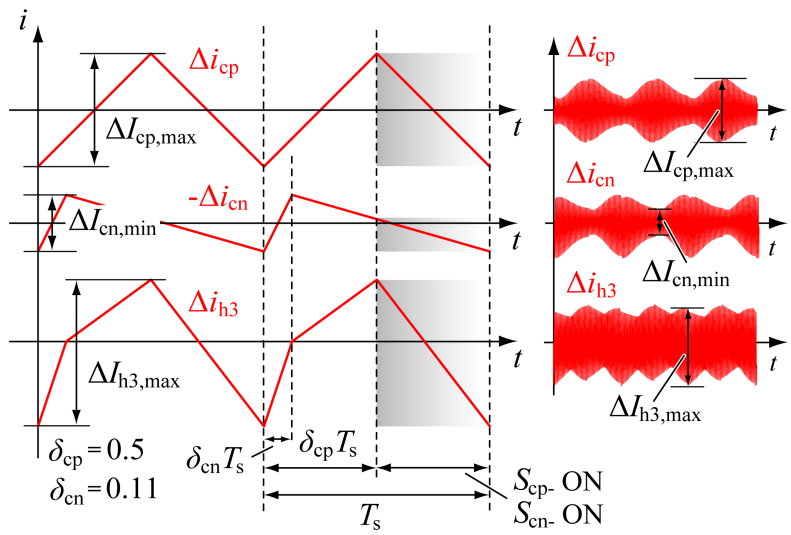


Fig. 5.7: Qualitative analysis for determination of current ripple characteristics of injection current Δi_{h3}. Evaluation of $\Delta I_{\mathrm{h3,max}}$ by means of current ripple sections extracted from Δi_{cp} and Δi_{cn}.

$$= \frac{V_{\mathrm{c,tot}}\left(1-\frac{M}{2}\right)}{2L_{\mathrm{c}}f_{\mathrm{s}}} \,. \tag{5.19}$$

The maximum current ripple of i_{h3} and therefore i_{Ni} is defined by $\Delta I_{\mathrm{h3},f_{\mathrm{s}},\mathrm{max}} = 21.6\,\mathrm{A}$ for $V_{\mathrm{cp}} = V_{\mathrm{cn}} = 300\,\mathrm{V}$, $L_{\mathrm{c}} = 800\,\mu\mathrm{H}$ and $f_{\mathrm{s}} = 10\,\mathrm{kHz}$, which is $\approx 15\,\%$ higher than the maximum current ripple of i_{cp}, i_{cn}. In order to reduce the appearing current ripple of i_{h3}, i_{cp} and i_{cn}, for the same size of the determined inductance value, an additional coil could be applied. Considering both coil utilization possibilities (L_{cp}, L_{cn}, L_{h3} - L_{cp}, L_{cn}, $L_{\mathrm{h3}} = 0$), three (i-iii) different concepts for a proper inductor design of L_{cp}, L_{cn} and L_{h3} are applicable. For further discussions a standard "double edge" pulse width modulation (PWM) is assumed.
(i) is the standard 2 choke implementation (L_{cp}, L_{cn}, $L_{\mathrm{h3}} = 0$) which assumes all PWM signals (δ_{cp}, δ_{cn}) being synchronized. The inductance of both coils then results in

$$L_{\mathrm{c}} = \frac{V_{\mathrm{c,tot}}\left(1-\frac{M}{2}\right)}{2f_{\mathrm{s}}\Delta I} \,. \tag{5.20}$$

(ii) resembles **(i)**, however, PWM carrier signals of both injection legs are operated at 180° phase shift leading to a $\approx 12\,\%$ reduction of the inductance value $L_{\mathrm{c},180^\circ}$ which is calculated by

$$L_{\mathrm{c},180^\circ} = \frac{V_{\mathrm{c,tot}}}{4f_{\mathrm{s}}\Delta I} \,. \tag{5.21}$$

The last design effort **(iii)** is utilizing an additional third choke L_{h3} which is going to be directly located between CID and CSN. The inductance value of each choke now is reduced by 47 % compared to case **(i)**. Inductance values for the appropriate three chokes compute to

$$L_{\mathrm{c},L_{\mathrm{h3}}} = \frac{V_{\mathrm{c,tot}}\left(1+M\right)}{12f_{\mathrm{s}}\Delta I} \,. \tag{5.22}$$

It has to be noted that only attempt **(iii)** allows the implementation of a three-phase inductor. The injection inductance value results in $L_c \approx 1700\,\mu\text{H}$, $L_{c,180^\circ} = 1500\,\mu\text{H}$ or $L_{c,L_{h3}} \approx 900\,\mu\text{H}$ (depending on the respective design procedure), for a total DC voltage of $V_{c,tot} = 600\,\text{V}$, a switching frequency (f_s) of the cell of 10 kHz and a maximum current ripple (ΔI) of $25\,\%\hat{I}_N$ ($\approx 10\,\text{A}$).
Moreover, also the existing four power semiconductors of the full-bridge converter have to be characterized to guarantee a promising selecting of appropriate transistors. Therefore, current (avg, rms - conduction losses and i_{cp}, i_{cn} - switching losses) and voltage stress of the appropriate switches is required. Current stress calculations of all semiconductor components of the full-bridge stage ($S_{cp\pm}$ and $S_{cn\pm}$) have to be accomplished numerically as zero crossings of i_{cp} and i_{cn} cannot be characterized in a closed analytical way. A design example is, therefore, given for a $208\,\text{V}_{LL}/60\,\text{Hz}/10\,\text{kW}$ system. Averaged and rms values of the switches are defined as follows:

- **AVG:** $S_{cp+}/S_{cn-} = 1.6\,\text{A}$; **RMS:** $S_{cp+}/S_{cn-} = 10\,\text{A}$
- **AVG:** $S_{cp-}/S_{cn+} = 1.6\,\text{A}$; **RMS:** $S_{cp-}/S_{cn+} = 7\,\text{A}$.

Additionally, the voltage stress of each semiconductor (neglecting DC-link voltage ripple and/or ringing due to fast $\mathrm{d}v/\mathrm{d}t$ rates):

- **maximum Voltage across SC:** $S_{cp+}/S_{cp-} = 600\,\text{V}_{DC}$
- **maximum Voltage across SC:** $S_{cn+}/S_{cn-} = 600\,\text{V}_{DC}$.

Due to the expected voltage stress of $V_{cp} + V_{cn} = 600\,\text{V}$ for each switch, either CREEs C2M0080120D, ROHMs SCT2080KE, or the recently released 900 V series by Cree/Wolfspeed hence appear to be perfectly applicable for a 10 kW system.

5.1.3 Simulation Results

The last section includes some simulation results of the proposed system in order to give a short outlook if the proposed topology is capable of fulfilling the required IEEE standards. Fundamental parameters are derived and defined as follows:

- **Mains Characteristics:** $208\,\text{V}_{LL}/60\,\text{Hz}$
- **CSN:** Full-Bridge (SiC-MOSFETs)
- **CID:** Back-to-Back IGBTs/MOSFETs
- **Switching Frequency:** $f_s = 10\,\text{kHz}$
- **DC-side Smoothing Inductance:** $L_{DC} = 500\,\mu\text{H}$
- **Injection Inductor Implementation:** Coupled Three-Phase Inductor
- **Injection Inductance:** $L_c = 800\,\mu\text{H}$
- **DC-Link Voltage:** $V_{cp} = V_{cn} = 300\,\text{V}$

Fig. 5.8 depicts most important current waveforms of the 10 kW hybrid rectifier (mains voltages v_{Ni}, input currents i_{Ni}, positive busbar current i_{pos}, nominal pos-

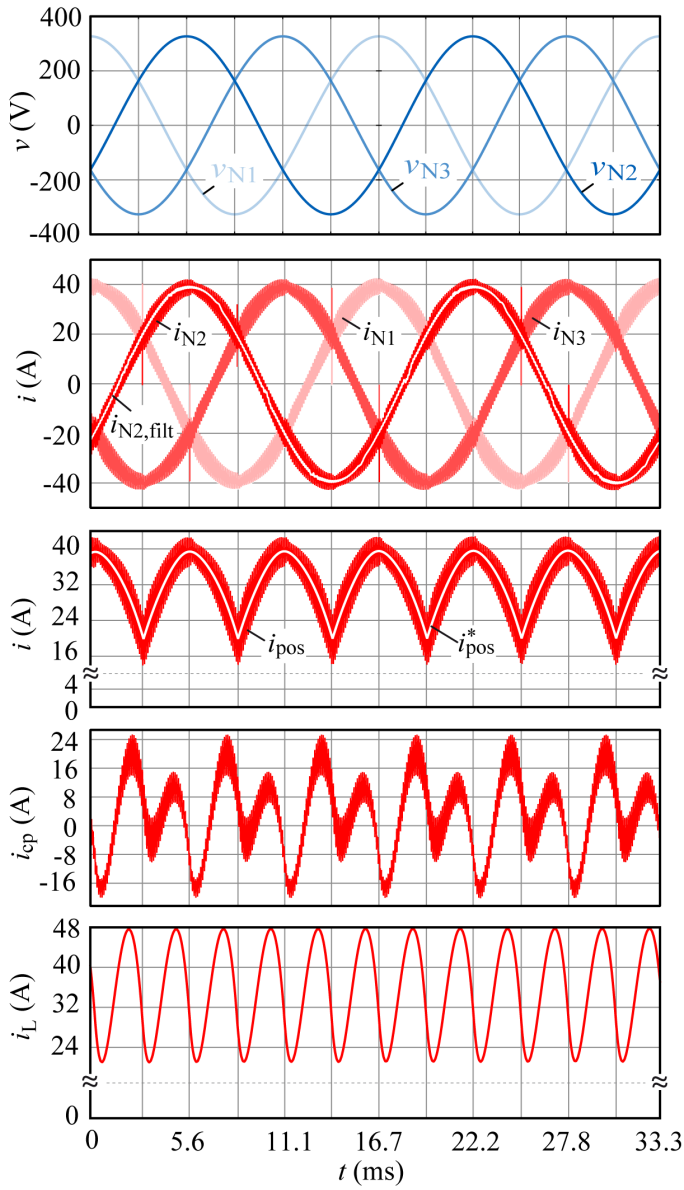


Fig. 5.8: Simulated current waveforms of hybrid three-phase rectifier for 500 µH DC-side smoothing inductance (L_{DC}), 10 kHz switching frequency f_{s} and injection inductance values of 800 µH.

itive busbar current i^*_{pos}, injection current of positive output bus i_{cp} and DC-side smoothing inductor current i_{L}). The output filter current i_{L} is formed by an averaged part which equals the output current (I_{o}) and multiples of $6f_{\mathrm{N}}$ which are evoked due to the rectifiers output voltage components. These 6th harmonic current components are hence dependent on the size of L_{DC}. The spectral components are compensated and suppressed by i_{cp} and result due to proper control concepts in $2\pi/3$ sinusoidal current waveshapes (i_{pos}). At the AC-side after proper switching frequency filtering, sinusoidal input currents ($i_{\mathrm{N2,filt}}$) with a total harmonic distortion ($\mathrm{THD_i}$) of 1.3 % and power factor λ of 0.999 are achieved.

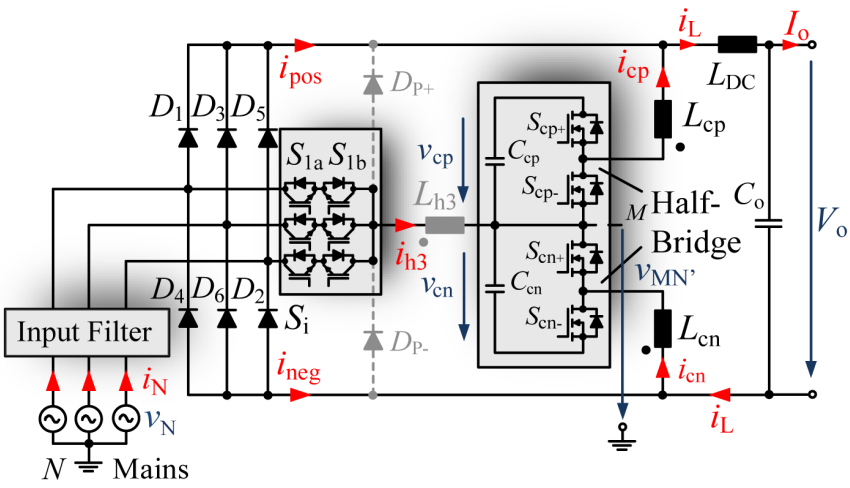


Fig. 5.9: Passive three-phase rectifier with DC-located LC output filter equipped by an optional third harmonic injection circuit consisting of two half-bridge stages, three bidirectional switches in back-to-back arrangement and two (or optionally three) injection inductors.

5.2 CSN Implementation - 2 x Half Bridge

Fig. 5.9 depicts a B6 diode bridge rectifier with LC output filter (as proposed in [121]), upgraded by a circuit based on Topology B of **Fig. 5.1**. The CSN here is realized by two half-bridge (as discussed in [122–126]) legs connected in series, whereas the output of the upper converter stage is connected to the positive bus bar and the output of the lower bridge leg is linked to the negative output of the B6 (via two chokes L_{cp} and L_{cn}, respectively). The interconnection between AC-side mains and midpoint M of the shaping network is formed via three bidirectional switches $S_{i,ab}$, which are implemented in this specific case as back-to-back IGBTs or SiC-MOSFETs (current injection device CID). Also different solutions like reverse blocking IGBTs etc. are applicable.
The output voltage V_o of the rectifier is defined due to the mains voltage level and calculates to

$$V_o = \frac{3\sqrt{3}\hat{V}_N}{\pi}. \tag{5.23}$$

The DC-side smoothing inductance current i_L is characterized according to B6 output voltage v_{rec} and V_o and hence defined by

$$i_L(\varphi_N) = I_o - \frac{3\sqrt{3}\hat{V}_N}{\pi\omega_N L_{DC}} \sum_k^{\infty} \frac{2}{(6k)^3 - 6k} \sin(6k\varphi_N) \tag{5.24}$$

according to **Eq. 3.13**. The current ripple of i_L is mainly given by a 300 Hz spectral component, evoked due to the 300 Hz passive three-phase rectifier voltage v_{rec}. The half-bridge leg connected to the DC capacitor C_{cp}, has to facilitate a compensational current i_{cp}, which completely suppresses the 300 Hz current ripple

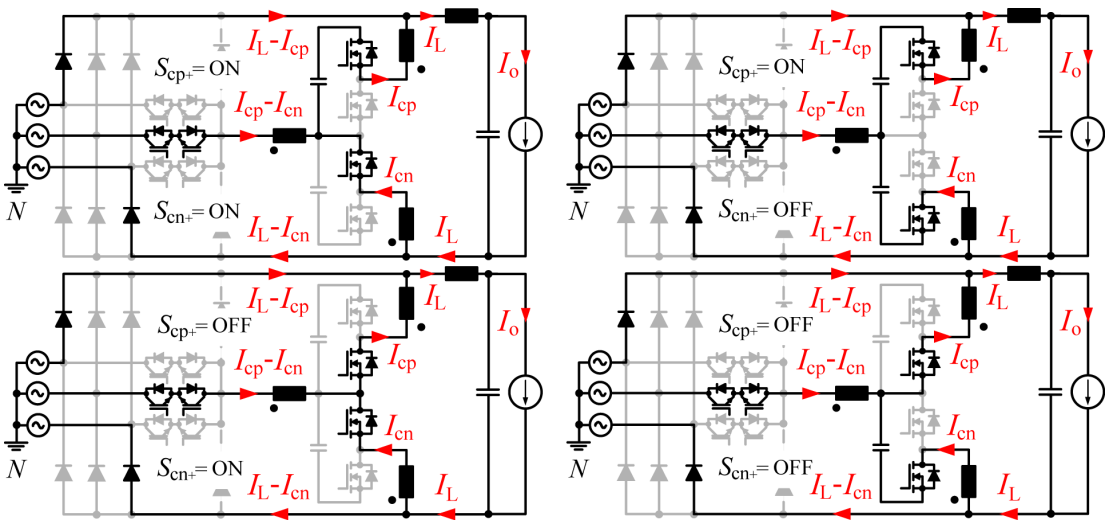


Fig. 5.10: Feasible switching states of third harmonic injection based rectifier for the sector $\varphi_N \in [0 \ldots \frac{\pi}{3}]$.

and guarantees 120 ° width sinusoidal wave shape intervals e.g.

$$i_{\text{pos}} = \hat{I}_{\text{N}} \cdot \cos(\varphi_{\text{N}}) \quad \text{for} \quad \varphi_N \in \left[-\frac{\pi}{3} \ldots \frac{\pi}{3}\right]. \tag{5.25}$$

The current of the positive bus-bar i_{pos} is hence constituted by fractional parts of $\cos(\varphi_{\text{N}})$, $\cos\left(\varphi_{\text{N}} - \frac{2\pi}{3}\right)$ and $\cos\left(\varphi_{\text{N}} - \frac{4\pi}{3}\right)$. i_{pos} is therefore now defined by $\max(i^*_{\text{N1}}, i^*_{\text{N2}}, i^*_{\text{N3}})$ and hence results in

$$i_{\text{pos}} = g_{\text{e}} \frac{3\sqrt{3}\hat{V}_{\text{N}}}{\pi} \left(\frac{1}{2} + \sum_{k}^{\infty} \frac{(-1)^{k+1}}{(3k)^2 - 1} \cos(3k\varphi_{\text{N}}) \right) \tag{5.26}$$

with g_{e} which denotes the equivalent conductance value and defined by $\hat{I}_{\text{N}}/\hat{V}_{\text{N}}$. Equal assumptions are applicable for injection current i_{cn} and generate bus-bar current i_{neg}. The third harmonic injection current i_{h3} is defined according to $i_{\text{cp}} - i_{\text{cn}}$ and similarly (as i_{pos} and i_{neg}) results in sinusoidal wave shape sections. This third harmonic current i_{h3} is going to be injected into the appropriate mains phase which is instantaneously not conducting current. Sinusoidal mains input current for e.g. phase 1 is therefore assembled according to the following sequence:

- $i_{\text{N1}} = i_{\text{pos}}$ for $\varphi_N \in [-\pi/3 \ldots \pi/3]$
- $i_{\text{N1}} = i_{\text{h3}}$ for $\varphi_N \in [\pi/3 \ldots 2\pi/3]$
- $i_{\text{N1}} = i_{\text{neg}}$ for $\varphi_N \in [2\pi/3 \ldots 4\pi/3]$
- $i_{\text{N1}} = i_{\text{h3}}$ for $\varphi_N \in [4\pi/3 \ldots 5\pi/3]$.

The sequence at hand (**Fig. 5.10**) indicates that diodes of the passive rectifier are only switched with f_{N}(=50 Hz) and the bidirectional switches ($S_{\text{i,ab}}$) of the current injection device with $2f_{\text{N}}$(=100 Hz). Consequently, only the two half-bridge legs are operating with switching frequency f_{s}. All possible occurring switching states for one sector, e.g. $\varphi_N \in [0 \ldots \frac{\pi}{3}]$, available for proper current shaping of i_{pos} and

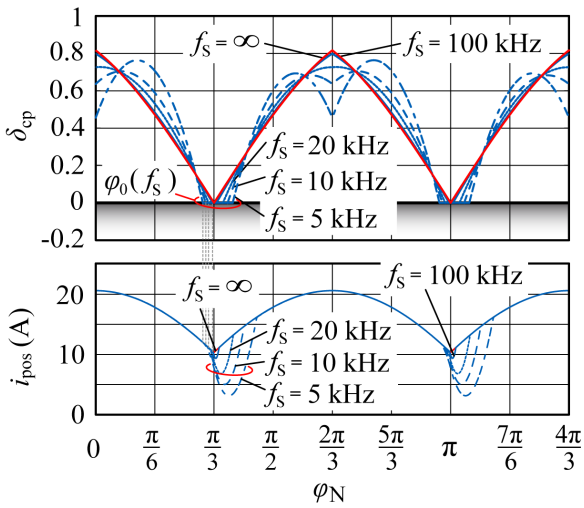


Fig. 5.11: (Top) – Ideal (red) and real duty cycles δ_{cp} considering voltage drop $v_{L,cp}$, for different switching frequencies (resulting in different inductance values – $f_s = 5\,\text{kHz} \mathrel{\widehat{=}} L_{cp} = 9.6\,\text{mH}$, $f_s = 100\,\text{kHz} \mathrel{\widehat{=}} L_{cp} = 480\,\mu\text{H}$), if two inductors and synchronized pulse width modulation signals are used. (Bottom) – Appropriate calculated current distortions (no voltage/current controller considered).

i_{neg}, are therefore depicted in **Fig. 5.10**.
Finally, it has to be mentioned that due to the basically line-frequency commutation of the passive rectifier bridge no switching-frequency CM voltage appears at the output V_o.

5.2.1 Fundamental Topology Issues

As the main operating principle of the proposed third harmonic injection circuit has been discussed, some major operating boundaries are now specified.
The required duty cycles for proper current shaping of the system are defined by

$$\delta_{cp}(\varphi_N) = \frac{v_{pos}(\varphi_N) - v_{h3}(\varphi_N)}{V_c} \tag{5.27}$$

$$\delta_{cn}(\varphi_N) = 1 + \frac{v_{neg}(\varphi_N) - v_{h3}(\varphi_N)}{V_c}\,. \tag{5.28}$$

These functions are applying for an ideal consideration of L_{cp} and L_{cn} (i.e, neglecting their low-frequency voltage components). If δ_{cp} is is analyzed in detail, $\delta_{cp,min} = 0$ can be found at multiples of $(2k-1)\pi/3$ and the maximum ($\delta_{cp,max} = M = \frac{3\hat{V}_N}{2V_c} = 0.8125$) at multiples of $2k\pi/3$ for $k \in \mathbb{Z}$ (cf., **Fig. 5.11** - (top) red waveform). For a non-ideal consideration of L_{cp}, an additional voltage drop has to be considered (depicted in **Fig. 5.11** - (top) blue waveforms for different values of L_{cp}) which results in a minimum duty cycle of

$$\delta_{cp,min} = -\omega_N L_{cp} \frac{\frac{3\sqrt{3}}{\pi\omega_N L_{DC}}\left(1 - \frac{\pi}{2\sqrt{3}}\right)\hat{V}_N + \frac{\sqrt{3}}{2}\hat{I}_N}{V_c}\,. \tag{5.29}$$

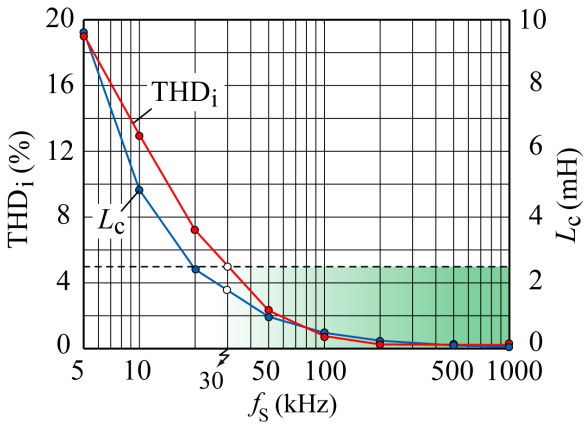


Fig. 5.12: Dependency of mains input current distortion $\mathrm{THD_i}$ on injection chokes $L_{\mathrm{cp}} = L_{\mathrm{cn}} = L_{\mathrm{c}}$ and (hence) switching frequency f_{s} (assumption: two inductors L_{cp}, L_{cn} and synchronized PWM).

As $(1 - \frac{\pi}{2\sqrt{3}})$ is > 0, $\delta_{\mathrm{cp,min}}$ is always < 0 for $L_{\mathrm{cp}} > 0$. Each half-bridge, however, is only able to facilitate a duty cycle range of $[0 \ldots 1]$, whereas "0" means upper switch ($S_{\mathrm{cp+}}$) off and lower switch ($S_{\mathrm{cp-}}$) on and vice versa for "1". A duty cycle < 0 will be not possible and hence this effect leads to current distortions of positive and negative busbar currents i_{pos} and i_{neg} which is illustrated in **Fig. 5.11** (top - calculated duty cycles and bottom - resulting current distortions of i_{pos} for different values of $L_{\mathrm{cp}}\,(f_{\mathrm{s}})$). It is therefore highly preferable to implement an injection choke whose inductance is as small as possible. This can be achieved using high switching frequencies f_{s} if a specific maximum current ripple of e.g. 30 % is allowed. According to **Fig. 5.12**, a $\mathrm{THD_i} < 5\,\%$ is obtainable for switching frequencies $> 30\,\mathrm{kHz}$. As discussed in [121] the inductance value of L_{cp} and L_{cn} can be further reduced if a third inductor L_{h3} is used. While the total volume of a three inductor implementation (if three independent chokes are utilized) hardly shrinks, the inductance value of L_{cp} and L_{cn} can be remarkably reduced by $\approx 70\,\%$ which can be expressed by

$$L_{\mathrm{c}\frac{\mathrm{p}}{\mathrm{n}},\mathrm{h3}} = \chi_{\mathrm{L}} \cdot L_{\mathrm{c}\frac{\mathrm{p}}{\mathrm{n}}}, \quad \chi_{\mathrm{L}} = \frac{1}{2\sqrt{3}\left(\sqrt{3} - M\right)}, \quad M = \frac{3}{2}\frac{\hat{V}_{\mathrm{N}}}{V_{\mathrm{c}}}\,. \tag{5.30}$$

This reduction mainly is caused by the injection cell voltage v_{MN} (characterized by voltage levels 0 and $\pm\frac{V_{\mathrm{c}}}{3}$) which is no longer directly clamped to the AC-side mains which would result in $v_{\mathrm{MN}} = v_3$. If optimized inductors are considered in the design of the injection cell, a minimum switching frequency for $\mathrm{THD_i} < 5\,\%$ can hence be reduced to $\approx 15 - 20\,\mathrm{kHz}$.

However, it has to be mentioned that a proper design of the injection inductors is not the only stringent requirement for proper operation of the injection cell. Imbalance of mains input voltages is also evolving as noticeable issue for this type of converter stage. For this investigation an ideal duty cycle is assumed, ignoring injection chokes ($L_{\mathrm{c}\frac{\mathrm{p}}{\mathrm{n}}} \to 0$ ($f_{\mathrm{s}} \to \infty$)). The variable $k_{\mathrm{v,i}}$ is introduced which describes the relative mains unbalance from the nominal value $230\,\mathrm{V_{rms}}$

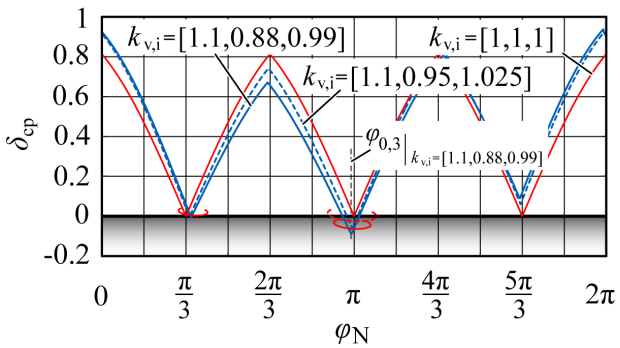


Fig. 5.13: (Duty cycles δ_{cp} (L_{cp},L_{cn} = 0) considering unbalanced (e.g. $k_{v,1} = 1.1$ means $V_{N,rms} = 230\,V + 10\,\%$) mains voltages (red – balanced mains voltages $k_{v,i} = 1$).

(e.g. $k_{v,1} = 1.1$ results in a mains voltage of $253\,V_{rms}$ and hence an increase of $10\,\%$). This, however, directly affects the duty cycle of both half-bridges (δ_{cp} and δ_{cn}). The minimum of δ_{cp} now is no longer characterized by 0. Considering the modified commutation time instants of the B6 the minimum of the duty cycle can be approximated by

$$\delta_{cp,min}\left(\varphi_{0,3}\right) \approx \frac{2}{3} M \left(k_{v,2} - k_{v,1}\right) \tag{5.31}$$

for the sector $\varphi_N \in [\varphi_{0,2} \ldots \varphi_{0,3}]$ which correlates with the sector $\varphi_N \in \left[\frac{2\pi}{3} \ldots \pi\right]$ for balanced mains voltages ($k_{v,i} = 1$, also depicted in **Fig. 5.13** - red waveform). $\varphi_{0,3}$ is the altered commutation time instant next to π and is defined by

$$\varphi_{0,3} = \frac{2\pi}{3} + \arctan\left(\frac{2k_{v2} + k_{v3}}{\sqrt{3}k_{v3}}\right). \tag{5.32}$$

Fig. 5.13 depicts different duty cycles for varying imbalance of mains voltages with $k_v = [1.1, 0.88, 0.99]$ and k_v =[1.1, 0.95, 1.025]. It can be seen that for the appropriate sector $\varphi_N \in [\varphi_{0,2} \ldots \varphi_{0,3}]$, the minimum duty cycle is of negative value if $k_{v,1} > k_{v,2}$. Again, it should be pointed out that each half-bridge is only able to facilitate a duty cycle between $[0 \ldots 1]$. Negative duty cycle values, hence, lead to increased input current distortions and hence worsened THD_i.
The THD_i for unbalanced mains voltages could however be improved if a negative voltage source v_0 in each half-bridge leg (as depicted in **Fig. 5.14**) would be added. Such a negative voltage source is discussed here for the sake of completeness but not implemented. This additional voltage source allows the half bridge to increase the duty cycle by

$$\delta_0 = \frac{v_0}{V_c}. \tag{5.33}$$

The required voltage v_0 has to be chosen such to equalize the most negative occurring duty cycle δ_{min}. Therefore, a direct coupling between the DC-link voltage V_c v_o is favored. This could be implemented, e.g., via a dual (DAB) or single active bridge (SAB) leg for each half-bridge DC voltage link (shown in **Fig. 5.14**).

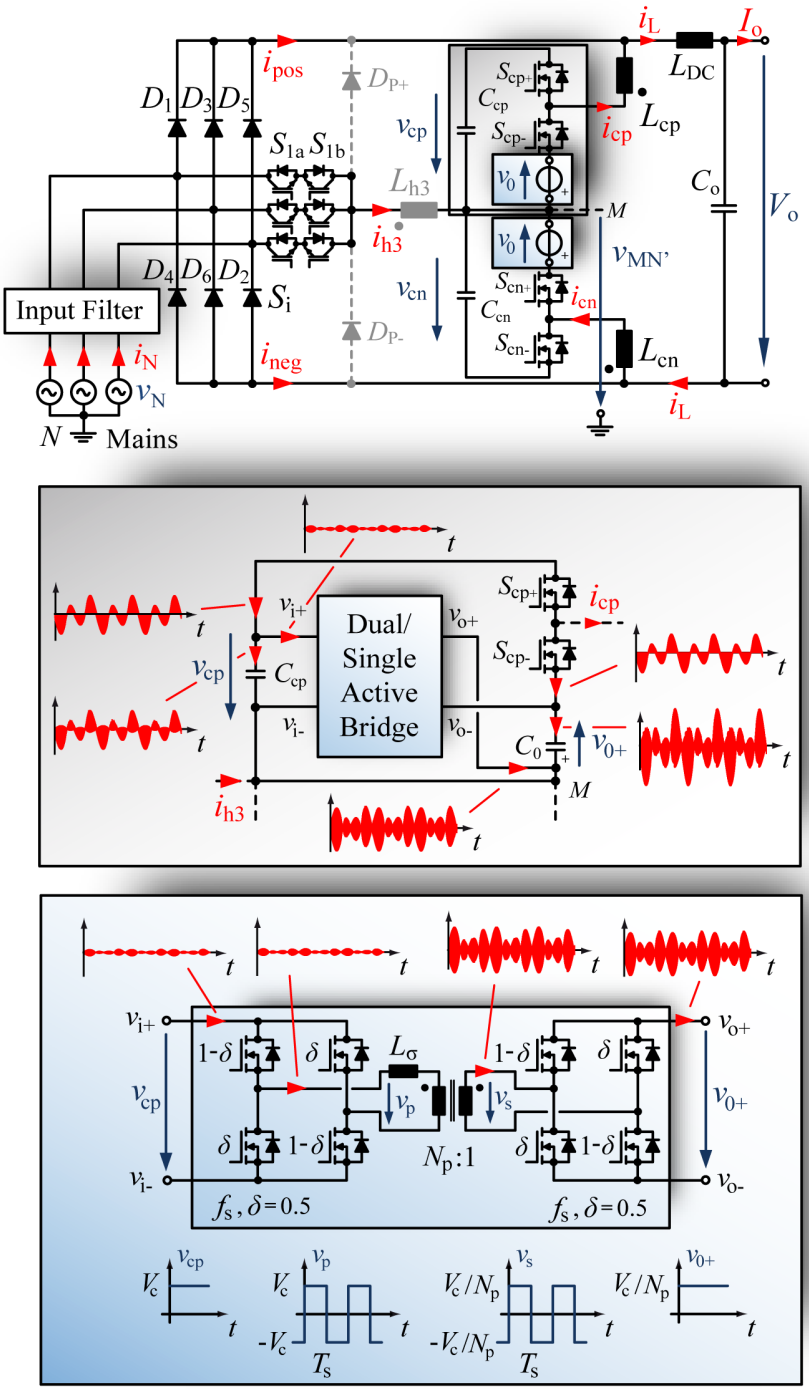


Fig. 5.14: A passive three-phase rectifier based on the third harmonic injection principle, realized via two half-bridge employing two additional voltage sources v_o for disturbance reduction, implemented as either dual or single active bridge leg.

The example is illustrated and simulated using a DAB. A fixed duty cycle with e.g. switching frequency can be utilized. The high frequency transformer can be chosen such to e.g. fulfill

$$N_p = \frac{1}{\delta_{min}} \tag{5.34}$$

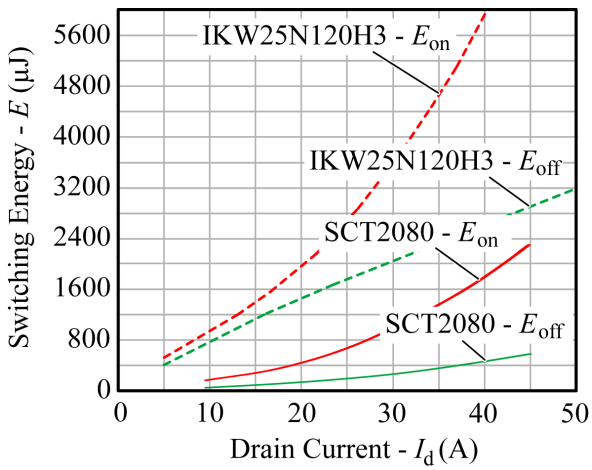


Fig. 5.15: Comparison of switching losses of an 1200 V/28 A (@100 °C) SiC-MOSFET (SCT2080KE - losses recorded @ 600 V DC voltage, $R_G = 0\,\Omega$, $V_{GS} = 18/0\,\text{V}$, $L = 500\,\mu\text{H}$) and a 1200 V/25 A (@100 °C) IGBT (IKW25N120H3 (high speed switching series) - losses recorded @ 600 V DC voltage, $R_G = 23\,\Omega$, $V_{GS} = 15/0\,\text{V}$, L =n/a).

which could e.g. result in

$$N_p = \frac{V_c}{\hat{V}_N \frac{L_c}{L_{DC}} \left(\frac{3}{2} - \frac{3\sqrt{3}}{\pi}\right) - \frac{\sqrt{3}}{2}\omega_N L_c \hat{I}_N} \,. \tag{5.35}$$

However, it has to be considered that this implementation (either way – DAB or SAB) requires an unfavorable additional passive and active component effort. Therefore, an e.g. CSN implementation as three-level bridge leg seems to be far more practical.

5.2.2 SiC-MOSFET- or IGBT-Application

The SiC-MOSFET at present is commercially available for blocking voltages from 900 V to 1200 V. This allows the application of SiC-MOSFETs for half-bridge legs with DC voltage levels 600 V . . . 800 V and offers an operation with increased switching frequency with lower switching losses compared to conventional IGBTs. This is also depicted in **Fig. 5.15** which shows a comparison of turn-on and turn-off losses of a SCT2080KE[1] (SiC-MOSFET) and a IKW25T120H3[2] (reverse blocking IGBT) with about similar basic characteristics ($V_{max} = 1200\,\text{V}, I_{d,max@100°C} \approx 25\,\text{A} - 28\,\text{A}$). It can be observed that both, turn-on and turn-off energies of the SiC-MOSFET are significantly smaller than those of an IGBT. The SiC-MOSFET, furthermore, shows ohmic turn-on characteristic which will result in improved conduction losses in the partial-load mode (compared to an Si-IGBT for equal full-load mode conduction losses). The implementation of a SiC-MOSFET hence may lead to smaller and less expensive cooling system/volume. It is e.g. stated in

[1] http://www.rohm.com/web/eu/products/-/product/SCT2080KE

[2] http://www.infineon.com/cms/en/product/power/igbt/igbt-discrete/discrete-igbt-with-anti-parallel-diode/IKW25N120H3

[127] that with a 1.2 kV SiC-MOSFET, a reduction in power loss of greater than 50 % (with dies that are less than half the size of Si IGBTs) can be achieved. The improved switching loss behaviour will hence lead to an increased efficiency of the total system compared to a conventional IGBT for approximately equal switching frequency. Similar to standard MOSFETs the SiC-MOSFET is characterized by a parasitic bipolar body diode due to its physical implementation. As, however, this body diode shows rather good switching behaviour and is only conducting during the dead time of the half-bridge stage, usually no external diode is required and the SiC-MOSFET seems to be very well applicable for the half-bridge topology. The bidirectional switches of the current injection device can also advantageously be implemented by SiC-MOSFETs in order to reduce conduction losses. It has to be mentioned that the emerging GaN technology could also serve as promising solution for the current shaping network, however, is yet not commercially available for DC voltage levels greater than 650 V as required here.

5.2.3 Current Controller

In this subsection, the current control of the proposed injection cell is briefly discussed. The third harmonic injection circuit consists of two half-bridge legs (cf., **Fig. 5.9**). The half-bridge connected to C_{cp} is therefore responsible for proper control of i_{cp} whereas the converter stage linked to C_{cn} has to properly adjust i_{cn}. Thus, two independent current controllers have to be designed.
If a simplified model is applied which is neglecting parasitic effects and components, the basic equations result in

$$\begin{aligned} L_{\mathrm{cp}}\frac{di_{\mathrm{cp}}}{dt} &= \delta_{\mathrm{cp}} v_{\mathrm{cp}} + v_{\mathrm{h3}} - v_{\mathrm{pos}} \\ L_{\mathrm{cn}}\frac{di_{\mathrm{cn}}}{dt} &= \left(1-\delta_{\mathrm{cn}}\right) v_{\mathrm{cn}} - v_{\mathrm{h3}} + v_{\mathrm{neg}}. \end{aligned} \tag{5.36}$$

If it is now assumed that the DC voltages v_{cp} and v_{cn} are regulated such – by the superimposed voltage controller with reduced dynamic – that they show a fixed level $V_{\mathrm{cp}} = V_{\mathrm{cn}} = V_{\mathrm{c}}$, the equations above can be simplified by applying Laplace Transform which finally results in

$$\mathrm{s}L_{\mathrm{cp}} i_{\mathrm{pos}} = -\delta_{\mathrm{cp}} V_{\mathrm{c}} + v_{\mathrm{pos}} - v_{\mathrm{h3}} + \mathrm{s}L_{\mathrm{cp}} i_{\mathrm{L}}. \tag{5.37}$$

If v_{N1}, v_{N2}, v_{N3} (which are required for the generation of an equivalent conductance value, which represents the power demand of the circuit) and i_{L} are measured, v_{pos}, v_{h3} and $\mathrm{s}L_{\mathrm{cp}} i_{\mathrm{L}}$ can serve as feedforward signals of the respective current control structure. The hereby resulting model can be described by

$$\delta_{\mathrm{cp}} = -\frac{\mathrm{s}L_{\mathrm{cp}}}{V_{\mathrm{c}}} i_{\mathrm{pos}} + \delta_{\mathrm{ff}}, \quad G_{\mathrm{i}}\left(\mathrm{s}\right) = \frac{V_{\mathrm{c}}}{sL_{\mathrm{c}}} \tag{5.38}$$

with the feedforward signal δ_{ff}

$$\delta_{\mathrm{ff}} = \frac{1}{V_{\mathrm{c}}}\left(v_{\mathrm{pos}} - v_{\mathrm{h3}}\right) + \frac{\mathrm{s}L_{\mathrm{cp}}}{\left(\mathrm{s}T_1 + 1\right) V_{\mathrm{c}}} i_{\mathrm{L}}. \tag{5.39}$$

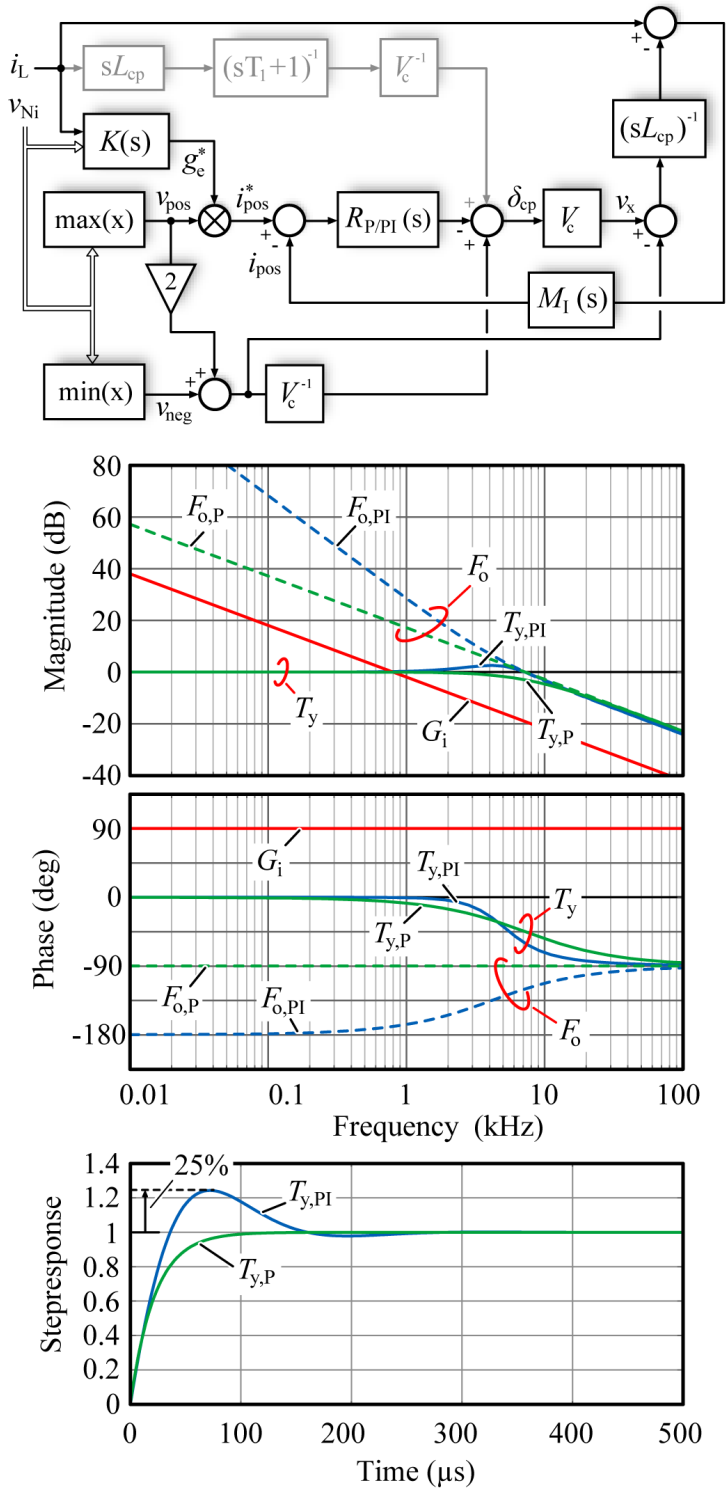


Fig. 5.16: Basic structure of current control circuit (top). Bode plot (middle) and step-response (bottom) of the designed current controller for a switching frequency of 72 kHz and an inductance value L_{cp} of 200 µH and a gain crossover frequency of 7 kHz), for either P- or PI-type with maximum overshoot of 25 % and minimum phase margin of 60 °).

The additional filter part $1/(sT_1+1)$ is required to guarantee suppression of high frequency noise and/or disturbance. Furthermore, it has to be noticed that the

feedforward part which includes i_L could also be omitted for very small values of L_c if it is preferred to reduce the number of current sensors. In **Fig. 5.16** (top) the basic structure of the proposed current controller is depicted. Furthermore, bode plot (middle) and step-response (bottom) of the designed controller are given (for a switching frequency of 72 kHz and an inductance value L_c of 200 µH and a gain crossover frequency f_c of 7 kHz), for either P- or PI-type (maximum overshoot of 25 %, minimum phase margin 60°) implementation. F_o denotes the open loop characteristic and T_y the closed loop transfer function of controlled current i_pos which is defined by

$$T_\mathrm{y,P/PI}\left(\mathrm{s}\right) = \frac{R_\mathrm{P/PI}\left(\mathrm{s}\right) G_\mathrm{i}\left(\mathrm{s}\right)}{1 + M_\mathrm{I}\left(\mathrm{s}\right) R_\mathrm{P/PI}\left(\mathrm{s}\right) G_\mathrm{i}\left(\mathrm{s}\right)}, \quad M_\mathrm{I} = \frac{1}{sT_\mathrm{I} + 1} \tag{5.40}$$

where M_I denotes the measurement circuit transfer function (which can be expressed in general by a low pass filter behaviour). The reference currents are generated by a superimposed voltage controller. This voltage controller indirectly determines the power demand by measuring the voltage of the DC-link capacitor.

5.2.4 Inductor Design

As indicated in **Fig. 5.9**, different solutions to implement the injection inductor arrangement exist (similar as discussed in section 5.1). In the following, only pulse width modulation (PWM) technique is considered for further calculations. The three most promising prospects for implementing these chokes (resulting currents illustrated in **Fig. 5.17**) are:

- **(i)**: Two inductor arrangement L_cp and L_cn ($L_\mathrm{h3} = 0$). PWM of positive and negative half-bridge synchronized.
- **(ii)**: Two inductor arrangement L_cp and L_cn ($L_\mathrm{h3} = 0$) with PWM of both half-bridges 180° phase shifted.
- **(iii)**: Three inductor arrangement L_cp, L_cn, and L_h3. Both PWMs synchronized.

Approach **(i)** shows lowest complexity regarding implementation issues. Only two chokes are required and the midpoint voltage of the cell (v_MN) is directly connected to the third harmonic injection network and the midpoint voltage therefore is equal to v_h3, i.e. only low harmonic components exist in v_MN. The maximum current ripple occurring in i_N is defined by the injection current i_h3 for synchronized PWMs (synchronization of triangular-shaped carrier signals) and not by the currents i_cp and i_cn. The duty cycles of both half-bridges (δ_cp and δ_cn) are approximately 0.5 (maximum ripple current) at the same time instant

$$\varphi_\mathrm{N} = \frac{\pi}{3} - \arcsin\left(\frac{\sqrt{3}}{4M}\right) \approx \frac{\pi}{6} \tag{5.41}$$

with $M = 3\hat{V}_\mathrm{N}/2V_\mathrm{c}$ and 600 V DC voltage levels (V_c) of the cell. The current i_h3, therefore, shows a comparatively high superimposed current ripple of $\Delta i_\mathrm{h3,max} =$

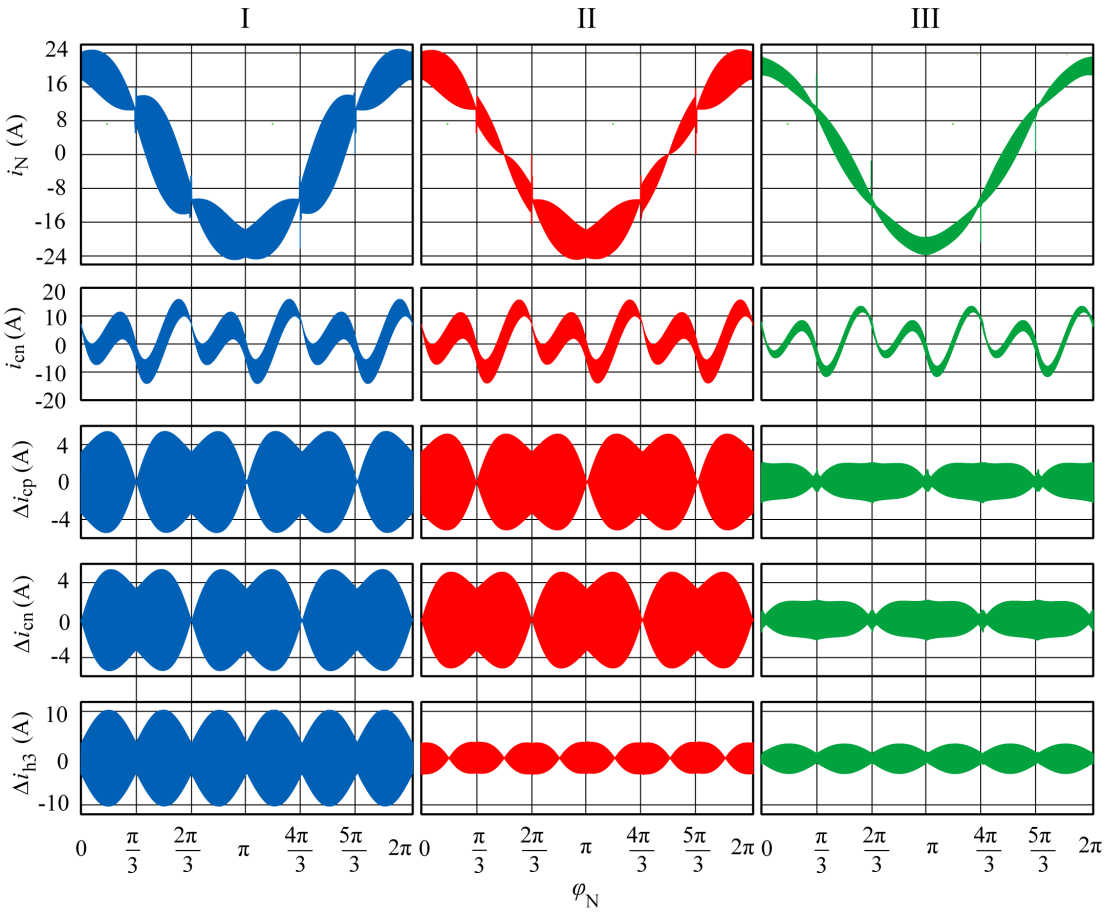


Fig. 5.17: Simulation results of a 10 kW/ 72 kHz active rectifier with 200 µH injection chokes. Unfiltered mains input current i_N for one mains period $\varphi_N \in [0 \ldots \pi]$. Mains current ripple Δi_{Ni} is defined by different sections of i_{pos}, i_{h3} and i_{neg} and therefore defined by $\max(\Delta i_{pos}, \Delta i_{h3}, \Delta i_{neg})$. Current ripple characteristics of i_{pos} and i_{neg} are, however, defined via specifications of Δi_{cp} and Δi_{cn} of injection inductance L_{cp}, L_{cn}, respectively. For I, II and III refer to description.

$\Delta i_{cp,max} + \Delta i_{cn,max} = 2\Delta i_{cp,max}$ at $\varphi_N = \pi/6$. The injection inductor value, for the two chokes, then results in

$$L_{cp} = L_{cn} = \frac{\hat{V}_N\left(\sqrt{3} - M\right)}{f_s \Delta i_{N,max}} \,. \tag{5.42}$$

This inductance value could be reduced if the triangular carrier signals of both half-bridges are phase shifted by 180° **(ii)**. The current ripple for this worst-case time instant $(\pi/6)$ now calculates to $\Delta i_{h3}(\varphi_N = \pi/6) = 0\,\mathrm{A}$ which means that maximum current ripples of both half-bridges completely compensate. The injection inductance is, therefore, given by

$$L_{cp} = L_{cn} = \frac{1}{2}\frac{\hat{V}_N\left(\sqrt{3} - M\right)}{f_s \Delta i_{N,max}} \,. \tag{5.43}$$

The size of the injection inductors can be reduced by 50 % if the triangular carrier signals are phase shifted by 180°. The maximum current ripple of i_{h3} is, however,

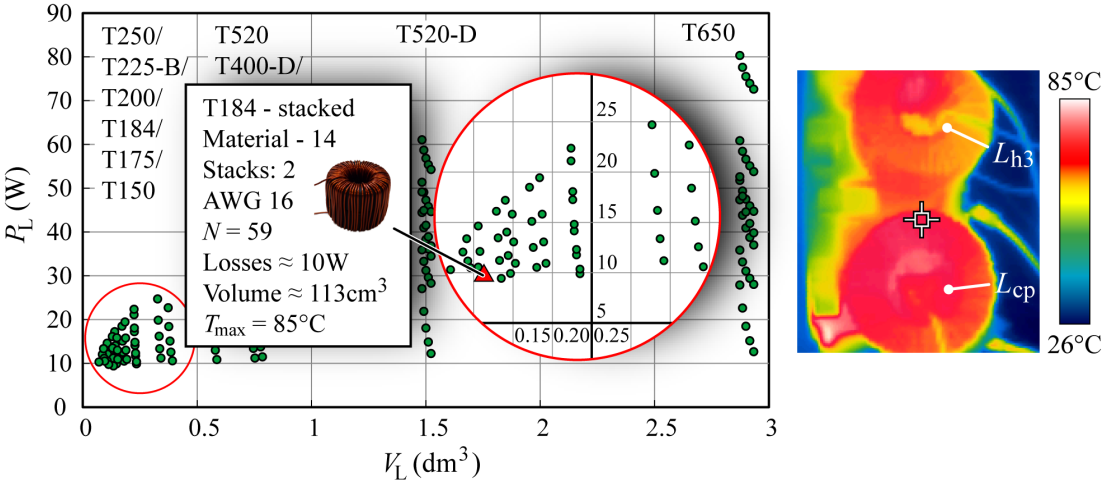


Fig. 5.18: Evaluation of optimized choke for different toroidal-stacked cores T20-T650, iron powder core materials 14-52 and solid conductors AWG16-AWG20 according to GeckoMAGNETICS and implemented inductor (boxed).

now given at the $\pi/3$ sector transitions, which results in worsened $\mathrm{THD_i}$ of the active rectifier system, as the current ripple of the positive busbar current shows a minimum at this time instant ($\Delta i_{\mathrm{pos}}\,(\varphi_{\mathrm{N}} = \pi/6) = 0\,\mathrm{A}$).
Approach **(iii)** using 3 chokes is therefore proposed which allows to shrink the inductance value of each choke by additional 40 % compared to approach **(ii)** (70 % compared to approach **(i)**). Even though the volume of the overall choke arrangement decreases by 5 % compared to **(ii)** as there are now three inductors required, the input current quality is improved considerably. The inductance value of each half-bridge choke is given by

$$L_{\mathrm{cp}} = L_{\mathrm{cn}} = L_{\mathrm{h3}} = \frac{V_{\mathrm{c}} M}{3\sqrt{3} f_{\mathrm{s}} \Delta i_{\mathrm{N,max}}} \,. \tag{5.44}$$

Input current i_{N}, injection current i_{cn} and current ripple of all three injection currents (Δi_{cp}, Δi_{cn}, Δi_{h3}) are depicted in **Fig. 5.17** for all three proposed design possibilities [**(i)**-blue, **(ii)**-red, **(iii)**-green] for $L_{\mathrm{cp}} = L_{\mathrm{cn}} = L_{\mathrm{h3}} = 200\,\mu\mathrm{H}$, a switching frequency of 72 kHz and an output power of 10 kW. The volume of all three chokes could further be minimized if a coupled three-phase choke is used. To design such an inductor a more sophisticated finite element method simulation software as e.g. FEMM, Maxwell, ANSYS would be required in order to precisely determine inductance and core losses for a high frequency switching system.
As the inductance value of each choke is reduced by 69 % compared to approach **(i)**, input current distortions using approach **(iii)** are reduced significantly resulting in a $\mathrm{THD_i}$ of $< 4\,\%$ for a 10 kW/10 kHz system with a peak-to-peak current ripple of 6 A. This arrangement is therefore also an attractive topology for higher power active rectifier systems with low switching frequencies.

In a next step a core selection for a 10 kW injection coil design is performed. A stacked toroidal iron powder core (implementation of $L_{\mathrm{c}} = L_{\mathrm{c}\frac{\mathrm{p}}{\mathrm{n}}} = L_{\mathrm{h3}}$) finally has been selected which basically allows reduced losses and rather high current

saturation limits (compared to ferrite material) which may be necessary due to unbalanced grid voltages and load step behaviour of the total system (discussed in [25] and [128]). In order to minimize input current distortions a maximum inductance of 200 µH has been chosen. The number of turns N for one choke can be calculated by

$$N = \sqrt{\frac{V_\mathrm{c} M}{3\sqrt{3} f_\mathrm{s} k_\mathrm{i} \Delta i_\mathrm{N,max} A_\mathrm{L,2xT184}}} \tag{5.45}$$

where V_c denotes the DC voltage of the cell (600 V), f_s the switching frequency (72 kHz), $k_\mathrm{i}\Delta i_\mathrm{N,max}$ the maximum current ripple (e.g. $25\,\% \cdot 20.54\,\mathrm{A}$), M the modulation index (0.8125) and $A_\mathrm{L,2xT184}$ the core nominal inductance ($2 \cdot 28\,\mathrm{nH}$). The basic equation to evaluate the required number of turns is given according to

$$L_\mathrm{c} = N^2 \cdot A_\mathrm{L}. \tag{5.46}$$

Fig. 5.18 illustrates an inductor optimization which was performed with Gecko-MAGNETICS for different toroidal-stacked cores T20-T650, iron powder core materials 14-52 and solid conductors AWG16-AWG20. The red triangle marks the implemented choke which is depicted in **Fig. 5.18**.
The chosen inductor (N=59, T184-14 x2 stacked, solid enameled copper wire ($d_\mathrm{cu} = 10\,\mu\mathrm{m}$ insulation thickness), AWG16 equivalent to $d_\mathrm{w} = 1.25\,\mathrm{mm}$).
The core losses for full-load operation of such an inductor calculate to $\approx 3\,\mathrm{W}$ if appropriate material characteristics[3] are used.
The DC-resistance of the coil calculates to

$$R_\mathrm{DC} = N \frac{\rho_\mathrm{cu} l_\mathrm{T}}{k_\mathrm{litz} \pi \left(\frac{d_\mathrm{w}}{2}\right)^2} = 90\,\mathrm{m\Omega} \tag{5.47}$$

with $k_\mathrm{litz} = 1$ as a solid conductor is used, ρ_cu the electrical conductivity of "hot" copper which is given by $0.02\,\frac{\Omega\mathrm{mm}^2}{\mathrm{m}}$ and l_T the effective wire length for one winding which is $\approx 0.095\,\mathrm{m}$.
As no air gap is used no fringing effect occurs and/or is rather small for $f < 100\,\mathrm{kHz}$. Two issues which have, however, to be considered for the design of the inductor and are eventually occurring are the skin and the proximity effect (eddy-current effects). The skin effect of a conductor is caused by the magnetic field which is induced by its own current. The proximity effect is evoked due to the magnetic fields which are induced by currents from adjacent conductors. Both effects lead to a nonuniform current density in conductors (impact depends on frequency components of currents) which finally results in an increased resistivity of the appropriate conductor. For low frequency (or DC-) currents both effects are negligibly small (current density in the conductor is uniform).
Furthermore it has to be considered, that the resistivity additionally increases with temperature of the conductor T_c

$$\rho_\mathrm{T_c} = \rho_\mathrm{T_{c0}} \left(1 + \alpha_\mathrm{T} \left(T - T_0\right)\right) \tag{5.48}$$

[3] www.micrometals.com

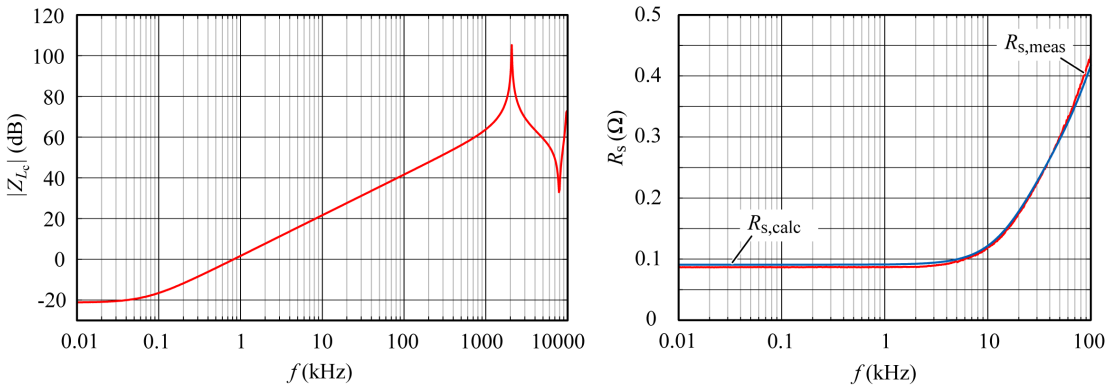


Fig. 5.19: Imepdance of one implemented injection inductor L_c and dedicated calculated and measured series resistance $R_{s,calc}$ ($N_L = 1$, $k_{litz} = 1$, $d_{cu} = 10\,\mu m$, $d_w = 1.25\,mm$, $N = 59$, $l_T = 0.095\,m$, $\rho_{cu} = 0.02\,\frac{\Omega mm^2}{m}$) and $R_{s,meas}$, respectively.

whereas α_T denotes the temperature coefficient of copper ($\approx 0.4\,\%/°C$), and $\rho_{T_{c0}}$ is the conductor resistivity at e.g. room-temperature T_0. As the conductor resistivity is dependent of the instantaneous temperature of the conductor, also the skin depth

$$\delta_w = \sqrt{\frac{\rho_{cu}}{\pi \mu_0 f_s}} = \sqrt{\frac{\rho_{T_{c0}} \left(1 + \alpha_T \left(T - T_0\right)\right)}{\pi \mu_0 f_s}} \tag{5.49}$$

is (in addition to its frequency obedience) temperature dependent. At high frequencies the current which is flowing through a round solid conductor (or) litz wire is hence forced to occur within the skin depth close to the surface of the conductor. The inner part of the conductor therefore does not contribute to the effective conduction area of the wire anymore. The effective cross sectional area of the AC-current is hence defined by

$$A_{e,ac} = \pi r_w^2 - \pi \left(r_w - \delta_w\right)^2 = \pi \delta_w \left(d_w - \delta_w\right). \tag{5.50}$$

The approximated (simplified) AC resistance $R_{AC,skin}$ due to the occurring skin effect can hence be written (according to [129]) as

$$R_{AC,skin} = N \frac{\rho_{cu} l_T}{k_{litz} \pi \left(d_w - \delta_w\right) \delta_w}. \tag{5.51}$$

For increasing current frequencies also the proximity effect has to be considered which results in the well-known AC resistance (also listed in [129])

$$R_{AC} = R_{DC} A_0 \left[\frac{\sinh\left(2A_0\right) + \sin\left(2A_0\right)}{\cosh\left(2A_0\right) - \cos\left(2A_0\right)} + \frac{2\left(N_L^2 k_{litz} - 1\right)}{3} \cdot \frac{\sinh\left(A_0\right) - \sin\left(A_0\right)}{\cosh\left(A_0\right) + \cos\left(A_0\right)}\right] \tag{5.52}$$

(shown in **Fig. 5.19**, with parameters, $N_L = 1$, $k_{litz} = 1$, $d_{cu} = 10\,\mu m$, $d_w = 1.25\,mm$, $N = 59$, $l_T = 0.095\,m$, $\rho_{cu} = 0.02\,\frac{\Omega mm^2}{m}$) where N_L denotes the number

of layers of the inductor ($N_\mathrm{L} = 1$) and the coefficient A_0 is defined by

$$A_0 = \left(\frac{\pi}{4}\right)^{\frac{3}{4}} \frac{d_\mathrm{w}}{\delta_\mathrm{w}} \sqrt{\frac{1}{1 + 2\frac{d_\mathrm{cu}}{d_\mathrm{w}}}}. \tag{5.53}$$

In order to determine the appropriate stray or self-capacitance (which is required to evaluate the inductor's resonance frequency, it is necessary to determine the turn-to-turn capacitance C_tt of a single layer inductor in advance. This turn-to-turn capacitance (as discussed in [129]) results in

$$C_\mathrm{tt} = \frac{2\pi\epsilon_0 l_\mathrm{T}}{\pi\sqrt{\left(\frac{1}{\epsilon_\mathrm{r}}\ln|1 + 2\frac{d_\mathrm{cu}}{d_\mathrm{w}}| + 1\right)^2 - 1}} \mathrm{atan}\left(\sqrt{1 + \frac{2}{\frac{1}{\epsilon_\mathrm{r}} + \ln|1 + 2\frac{d_\mathrm{cu}}{d_\mathrm{w}}|}}\right) \tag{5.54}$$

According to [130], the self capacitance C_s can be finally evaluated by introducing an additional coefficient ζ_s which can be evaluated numerically and is in the range between about 0.5 and 2 which reflects practical effects, not covered by standard idealized/simplified geometry. The theoretically calculated resonance of the designed inductor can therefore be obtained by

$$f_\mathrm{res} = \frac{1}{2\pi\sqrt{L_\mathrm{c}\zeta_\mathrm{s}C_\mathrm{tt}}} \approx 2.1\,\mathrm{MHz} \tag{5.55}$$

with $L_\mathrm{c} = 190\,\mu\mathrm{H}$ and $C_\mathrm{tt} \approx 22\,\mathrm{pF}$. It has to be noted that ζ_s is given by 1.366 for a single-layer inductor with a core or a shield. Furthermore, ζ_s results in 1.618 for two-layer core-less inductor $N \geq 10$, 1.83 for two-layer inductor with conductive core $N \geq 10$ and 0.5733 for three-layer inductor with conductive core $N \geq 10$. The resonance $f_\mathrm{res,meas}$ of the realized inductor has been finally measured an results in 2 MHz (depicted in **Fig. 5.19**).

5.2.5 Midpoint Voltage

According to **Fig. 5.9** the midpoint voltage v_MN is dependent on the conduction states of the active switches of both half-bridge topologies if three chokes (L_cp, L_cn and L_h3) are used. The midpoint voltage v_MN for using three chokes, hence, also shows switching frequency voltage components. These components highly depend on the relation between $L_{\mathrm{c}\frac{\mathrm{p}}{\mathrm{n}}}$ and L_h3 which is analytically shown in this subsection. For this aspect, the switching states S_cp and S_cn are defined where $S_\mathrm{cp} = 0$ denotes upper switch ($S_\mathrm{cp+}$) is turned off and lower switch ($S_\mathrm{cp-}$) is turned on. Same assumptions are valid for S_cn. The midpoint voltage in sector $\varphi_\mathrm{N} \in [0 \ldots \pi/6]$ ($i_\mathrm{N1}(\varphi_\mathrm{N}) > 0$, $i_\mathrm{N2}(\varphi_\mathrm{N})$, $i_\mathrm{N3}(\varphi_\mathrm{N}) < 0$) for the switching state (00) can hence be calculated by

$$-L_\mathrm{cp}\frac{\mathrm{d}i_\mathrm{cp}}{\mathrm{d}t} = v_\mathrm{pos} - v_\mathrm{MN} \tag{5.56}$$

$$L_\mathrm{cn}\frac{\mathrm{d}i_\mathrm{cn}}{\mathrm{d}t} = v_\mathrm{neg} - v_\mathrm{MN} + V_\mathrm{c} \tag{5.57}$$

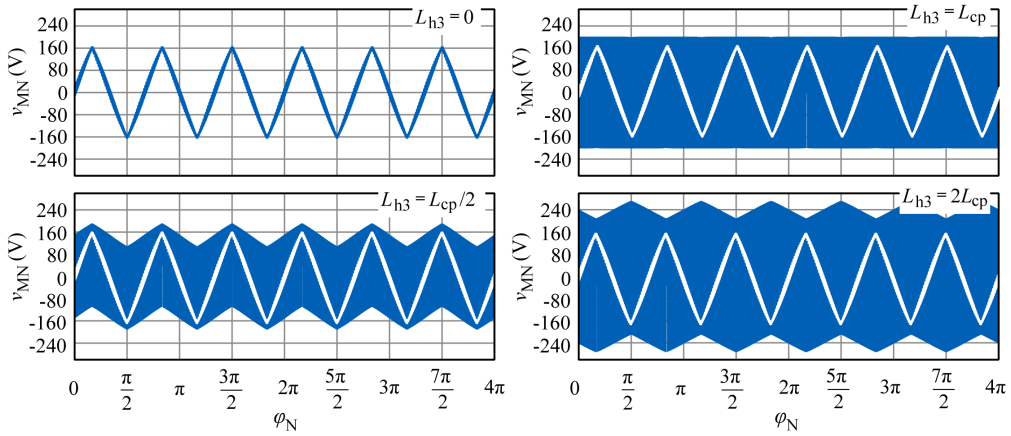


Fig. 5.20: Midpoint voltage v_{MN} of current injection cell for several implemented inductor variations of L_{h3} (e.g. $L_{h3} = 0$, $L_{h3} = L_{cp}/2$, $L_{h3} = L_{cp}$ or $L_{h3} = 2L_{cp}$).

$$-L_{h3}\frac{\mathrm{d}i_{h3}}{\mathrm{d}t} = v_{h3} - v_{MN}\,. \tag{5.58}$$

These calculations can be done for all three remaining states (10, 01 and 11). The instantaneous midpoint voltage level is hence directly dependent on v_{pos}, v_{h3}, v_{neg}, L_{cp}, L_{h3}, L_{cn} and V_c. A summary of all different feasible states is given below:

$$(00) \qquad v_{MN} = \frac{v_{pos}\left(-1+\frac{L_{h3}}{L_{cp}}\right) + v_{neg}\left(-1+\frac{L_{h3}}{L_{cn}}\right) + V_c\frac{L_{h3}}{L_{cn}}}{1+\frac{L_{h3}}{L_{cp}}+\frac{L_{h3}}{L_{cn}}} \tag{5.59}$$

$$(01) \qquad v_{MN} = \frac{v_{pos}\left(-1+\frac{L_{h3}}{L_{cp}}\right) + v_{neg}\left(-1+\frac{L_{h3}}{L_{cn}}\right) + V_c\left(\frac{L_{h3}}{L_{cn}}-\frac{L_{h3}}{L_{cp}}\right)}{1+\frac{L_{h3}}{L_{cp}}+\frac{L_{h3}}{L_{cn}}} \tag{5.60}$$

$$(10) \qquad v_{MN} = \frac{v_{pos}\left(-1+\frac{L_{h3}}{L_{cp}}\right) + v_{neg}\left(-1+\frac{L_{h3}}{L_{cn}}\right)}{1+\frac{L_{h3}}{L_{cp}}+\frac{L_{h3}}{L_{cn}}} \tag{5.61}$$

$$(11) \qquad v_{MN} = \frac{v_{pos}\left(-1+\frac{L_{h3}}{L_{cp}}\right) + v_{neg}\left(-1+\frac{L_{h3}}{L_{cn}}\right) - V_c\frac{L_{h3}}{L_{cp}}}{1+\frac{L_{h3}}{L_{cp}}+\frac{L_{h3}}{L_{cn}}}\,. \tag{5.62}$$

The midpoint voltage levels yield 0 V and $\pm 1/3V_c$ for a designed inductor considering $L_{cp} = L_{h3} = L_{cn} = L_c$. A DC voltage of 600 V will therefore result in 0 V and ± 200 V voltage steps of v_{MN}.

If the third harmonic inductance L_{h3} is omitted ($L_{h3} = 0$), the midpoint M is directly clamped to the AC-side mains and therefore results in $v_{MN} = v_{h3}$ (approach **(i)** and **(ii)**). The midpoint voltage now does not show any high frequency switching components anymore. This results, however, in a higher inductance value for $L_{cp} = L_{cn}$ and therefore increased distortions of the AC-side mains currents. Variations of midpoint voltage levels v_{MN} for different implementation results of L_{h3} (e.g. $L_{h3} = 0$, $L_{h3} = L_{cp}/2$, $L_{h3} = L_{cp}$, $L_{h3} = 2L_{cp}$) are depicted in **Fig. 5.20**. It has furthermore to be noted that an increased inductance value L_{h3} results in a smaller current ripple of i_{pos}, i_{neg} and i_{h3} due to increasing midpoint voltages for each switching state.

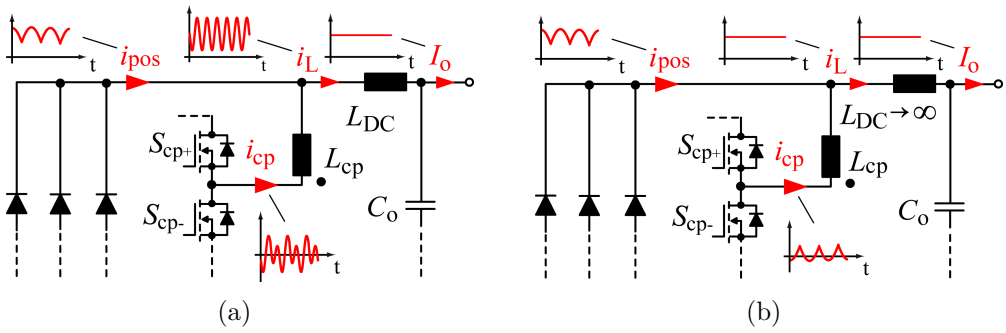


Fig. 5.21: Current waveforms of (a) passive three-phase rectifier system characterised by its 300 Hz dominant DC-side smoothing inductance ripple and (b) simplified passive system considering an infinitely high output inductance $L_{DC} \to \infty$ which enables an analytical description of current stress of active switches.

5.2.6 Current Stress of Passive Components and Capacitor Design

Current stress formulas for MOSFET and capacitors are either rather complex or can only be calculated numerically. A simplification, however, allows to evaluate the current stress of these components analytically. A very promising analytical calculation effort is hence briefly discussed which takes advantage of combining simplified analytical evaluation with numerical calculation. The DC-side smoothing inductor current is thereto assumed to be infinitely high which completely eliminates its 300 Hz current component (compare **Fig. 5.21(a)** and **Fig. 5.21(b)**). The DC-side smoothing inductance can hence be rewritten as $i_L(\varphi_N) = I_o$, which results in an injection current $i_{cp}(\varphi_N)$ with zero crossings at $2\pi k/3 \pm \arccos\left(\pi/(2\sqrt{3})\right)$ with $k \in \mathbb{Z}$. **Fig. 5.22(left)** illustrates numerically and simplified analytically computed current stress of semiconductor components of the respective half-bridge connected to C_{cp} and its dedicated capacitor design. It can be seen that all values show linear dependency on the nominal output power P_N. Furthermore, it can be seen that simplified analytically and numerically evaluated values cohere by a linear "correction" factor ξ. As the real current stress of passive components is dependent on L_{DC}, ξ is also linked to L_{DC}. The design of L_{DC} is dependent on AC-side mains input current distortions (B6-THD$_i$), voltages (V_{LL}), frequency (f_N) and nominal output power (P_N) of the passive rectifier. ξ is, hence, also dependent on input current distortions (B6-THD$_i$). As L_{DC} shows $1/x$ dependency of f_N and P_N and a quadratic dependency of V_{LL}, ξ (B6-THD$_i$) is independent of these values. Rms and averaged current ratings of the upper (S_{cp+}) and lower MOSFET (S_{cp-}) therefore yield

$$I_{cpp,avg} = 0\,\mathrm{A}\,, \tag{5.63}$$

$$I_{cpp,rms} = \xi_{I_p} P_N \sqrt{\frac{1}{\hat{V}_N V_c}\left(\frac{5}{3\sqrt{3}\pi} - \frac{\pi}{6\sqrt{3}}\right)} \tag{5.64}$$

$$I_{cpn,avg} = I_{cp,avg}\,, \tag{5.65}$$

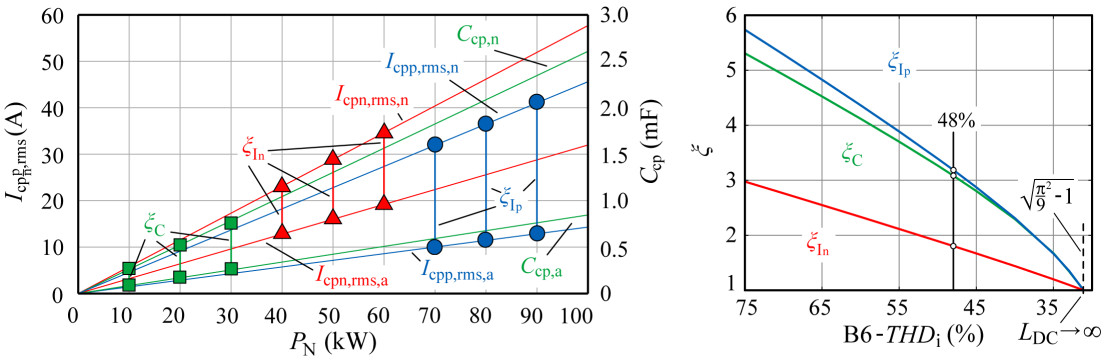


Fig. 5.22: (left) Numerically and simplified analytically computed current stress ($I_{cp\frac{p}{n},rms,\frac{a}{n}}$) of semiconductor components of positive and negative switch $S_{cp\pm}$ and designed appropriate capacitance value $C_{cp,\frac{a}{n}}$ for 400 V V_{LL}, B6-THD$_i$ of 48 % and appropriate L_{DC} value, $V_c = 600$ V and $f_N = 50$ Hz. (right) "Correction" coefficients ξ_{I_p}, ξ_{I_n} and ξ_C dependency on B6-THD$_i$ of mains input currents of a passive three-phase rectifier system.

$$I_{cpn,rms} = \xi_{I_n} P_N \sqrt{\frac{1}{\hat{V}_N V_c}\left(-\frac{5}{3\sqrt{3}\pi} + \frac{\pi}{6\sqrt{3}} + \frac{V_c}{\hat{V}_N}\left(\frac{\pi^2}{27} - \frac{4}{9} + \frac{1}{3\sqrt{3}\pi}\right)\right)}. \tag{5.66}$$

Injection cell capacitor values $C_{c\frac{p}{n}}$ and current stress can furthermore be calculated to

$$I_{ccp,rms} = I_{cpp,rms}\,, \tag{5.67}$$

$$C_{c\frac{p}{n}} = -\xi_C \frac{P_N}{\omega_N k_c}\left(\frac{\pi^2}{12\sqrt{3}} + \pi\left(\sqrt{\frac{1}{12} - \left(\frac{\pi}{12}\right)^2} - \frac{1}{3}\right) + \frac{1}{\sqrt{3}} - \arccos\left(\frac{\pi}{2\sqrt{3}}\right)\right) \tag{5.68}$$

where k_c represents the maximum allowable voltage ripple. Considering a total harmonic input current distortion of the passive rectifier of 48 % and a line-to-line input voltage of 400 V$_{rms}$, required ξ coefficients can be determined to ξ_C (48 %) = 3.084, ξ_{I_p} (48 %) = 3.187 and ξ_{I_n} (48 %) = 1.804. Coefficients ξ_{I_p}, ξ_{I_n} and ξ_C for different values of B6-THD$_i$ are plotted in **Fig. 5.22(right)**. A very simple linear approximation regarding $y = k \cdot x + d$ of e.g. ξ_{I_n} yields

$$\xi_{I_n}\,(\text{B6-THD}_i) = \frac{8}{3}\frac{1}{1 - \frac{4}{3}\sqrt{\frac{\pi^2}{9} - 1}} \cdot \text{B6-THD}_i + \frac{1 - 4\sqrt{\frac{\pi^2}{9} - 1}}{1 - \frac{4}{3}\sqrt{\frac{\pi^2}{9} - 1}} \tag{5.69}$$

$$= 4.554 \cdot \text{B6-THD}_i - 0.416 \tag{5.70}$$

ξ_{I_p} and ξ_C can be approximated in the exact same manner. In order to evaluate the accuracy of the stated calculation method, a comparison between calculated and simulated values for different values of L_{DC} considering for nominal output power of 10 kW, $V_{LL} = 400$ V, $V_c = 600$ V and $f_N = 50$ Hz has been performed. Results are recorded in **TABLE 5.2**. As can be seen calculated and simulated values are fitting very well, especially for smaller values of L_{DC}.

TABLE 5.2: Calculated and simulated values of $I_{\mathrm{cpp,rms}}$, $I_{\mathrm{cpn,rms}}$, and ΔV_{c} (for a specific designed capacitor $C_{\mathrm{cp}}/C_{\mathrm{cn}}$) considering $P_{\mathrm{N}} = 10\,\mathrm{kW}$, $V_{\mathrm{LL}} = 400\,\mathrm{V}$ and $V_{\mathrm{c}} = 600\,\mathrm{V}$.

	Calculated		
B6-THD$_{\mathrm{i}}$	$\boldsymbol{I_{\mathrm{cpp,rms}}}$	$\boldsymbol{I_{\mathrm{cpn,rms}}}$	$\boldsymbol{\Delta V_{\mathrm{c}}\ (C_{\mathrm{cp}}/C_{\mathrm{cn}})}$
35 %	2.32 A	3.51 A	30 V / 84.5 µF
48 %	4.56 A	5.77 A	30 V / 260 µF
70 %	7.56 A	8.83 A	30 V / 416 µF
	Simulated		
B6-THD$_{\mathrm{i}}$	$\boldsymbol{I_{\mathrm{cpp,rms}}}$	$\boldsymbol{I_{\mathrm{cpn,rms}}}$	$\boldsymbol{\Delta V_{\mathrm{c}}\ (C_{\mathrm{cp}}/C_{\mathrm{cn}})}$
35 %	2.52 A	3.66 A	29.42 V
48 %	4.68 A	5.88 A	30.01 V
70 %	7.76 A	9.04 A	30.18 V

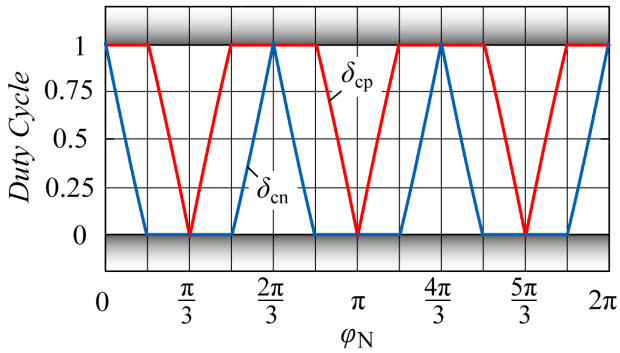


Fig. 5.23: Duty Cycle δ_{cp} of injection cell before charging DC capacitor stages C_{cp}, C_{cn}.

5.2.7 Start-Up Sequence of Rectifier

In this subsection the required and relatively complex start-up sequence of such an upgrade (employing two half bridge branches) during B6 operation (e.g. 10 kW) is briefly discussed. Furthermore, both capacitor stages (output stage and injection cell) have already been pre-charged in advance with AC-side located resistors to the 540 V voltage level. These charging resistors are short circuited if the charging process is finished and hence not available anymore in order to boost the DC-link to the required 1200 V level. An alternative strategy is hence required which is able to control the DC voltage link of the injection cell, even if the B6 is already operating and the appropriate voltage levels have not been properly set yet.
As the active converter acts as optional enhancement, it should be able to be turned on and/or off while the B6 is operating under different load conditions. Prior the active circuit is operating, the injection cell capacitor stages are (as already mentioned) pre-charged to the averaged B6 output voltage of only 540 V (280 V for each stage C_{cp}, and C_{cn}). As depicted in **Fig. 5.23**, the injection cell is not able to properly control the injection currents as

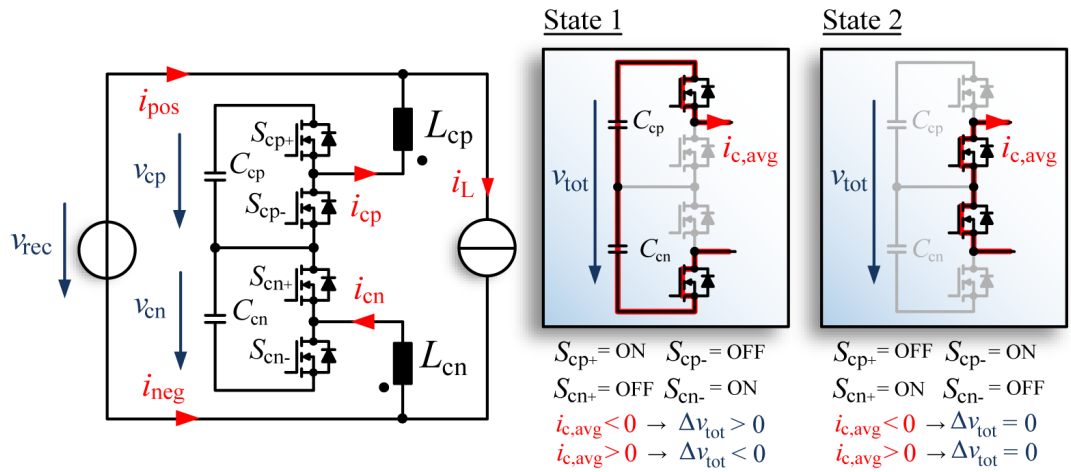


Fig. 5.24: Simplified model of rectifier system during start-up operation and feasible appropriate switching sates.

- $\delta_{cp}(\varphi_N) = 1,\ \varphi_N = -\pi/6 \ldots \pi/6$
- $\delta_{cn}(\varphi_N) = 1,\ \varphi_N = \pi/6 \ldots \pi/2$
- $\delta_{cp}(\varphi_N) = 1,\ \varphi_N = \pi/2 \ldots 5\pi/6$ etc.

applies, which can lead to inevitable damage of the total rectifier system. Therefore, a different controller strategy is required for DC-link capacitor charging of both half-bridge branches.
This concept has to be applied to the MOSFETs of the cell until each capacitor reaches a minimum tolerable voltage

$$V_{c,min} = \frac{3}{2}\frac{\hat{V}_N}{M_{max}} = 487.5\,\mathrm{V}\,. \tag{5.71}$$

This is the minimum voltage for each capacitor ($M_{max} = 1$) which has to be reached, before the already discussed current control is able to function properly. In order to avoid an additional circulating current path, the bidirectional switches have to be turned off during the whole charging process ($< 500\,\mathrm{V}$). The two existing half-bridges are hence not able anymore to independently control the injection currents i_{cp} and i_{cn}, as the current equations according to Kirchhoff's law are now defined by

$$i_{h3} = 0\,\mathrm{A}\,, \tag{5.72}$$

$$i_{cp} = i_{h3} + i_{cn} \quad \rightarrow \quad i_{cp} = i_{cn} = i_c\,, \tag{5.73}$$

$$i_{pos} = -i_{neg}\,. \tag{5.74}$$

The duty cycles of the existing MOSFETs therefore, have to be adapted. Two switches (one of each half-bridge) have to be turned on and off simultaneously, whereas the two remaining switches are exactly inversely switched. Therefore, only two different switching states can be obtained (cf., **Fig. 5.24**). The appropriate system equation now results in

$$2sL_c i_c = -\delta V_{tot} - v_{rec} + V_{tot}\,. \tag{5.75}$$

The current i_c can be expressed by

$$i_\mathrm{c} = i_\mathrm{L} - i_\mathrm{pos} \ . \tag{5.76}$$

Both, the DC-side smoothing inductor current i_L and the positive busbar current i_pos are measured quantities and can hence be used for proper control during start-up of the system without using an additional current sensor. If **Eq. 5.75** is used, the current controller transfer function results in

$$\frac{i_\mathrm{c}\left(s\right)}{\delta_\mathrm{c}\left(s\right)} = -\frac{V_\mathrm{tot}}{2sL_\mathrm{c}} \tag{5.77}$$

with the dedicated feed-forward signal

$$\delta_\mathrm{ff,su} = 1 - \frac{v_\mathrm{rec}}{V_\mathrm{tot}} \ . \tag{5.78}$$

By inspecting **Fig. 5.24**, it becomes obvious that during the DC-link charging process, no balancing of both capacitor stages C_cp and C_cn is possible. The appropriate voltage controller hence has to be designed such, that the dynamic of the controller is relatively high as parasitic effects of the capacitor stage may cause imbalance of capacitors (leakage currents, etc.) which cannot be controlled during the initial boost. Furthermore, the current of the injection cell i_c is smaller than the positive busbar current i_pos. i_pos consists of current parts of $I_\mathrm{L,avg}$, $\hat{I}_\mathrm{L,ac}$, $I_\mathrm{c,avg}$ and $\hat{I}_\mathrm{c,ac}$. The voltage controller gain $k_\mathrm{p,su}$ defines the maximum averaged current i_c and hence the worst case busbar current $I_\mathrm{pos,max}$. $k_\mathrm{p,su}$ has hence to be chosen in such way that the maximum occurring current values are lower than the limiting currents of MOSFETs and diodes of the system ($I_\mathrm{pos,max} < I_\mathrm{B6,max}$ and $I_\mathrm{c,max} < I_\mathrm{MOS,max}$).
The according transfer function of the voltage controller is defined by

$$\frac{v_\mathrm{tot}\left(s\right)}{i_\mathrm{c}\left(s\right)} = -\frac{2}{sC_{\mathrm{c}\frac{\mathrm{p}}{\mathrm{n}}}} \ . \tag{5.79}$$

In order to properly design $k_\mathrm{p,su}$, information of the high frequency current ripple Δi_c is required. Δi_c is defined by

$$\Delta i_\mathrm{c}\left(\varphi_\mathrm{N}\right) = \frac{v_\mathrm{tot} - v_\mathrm{rec}\left(\varphi_\mathrm{N}\right)}{2L_\mathrm{c}f_\mathrm{s}}\left(1 - \frac{v_\mathrm{rec}\left(\varphi_\mathrm{N}\right)}{v_\mathrm{tot}}\right) \ . \tag{5.80}$$

The current ripple is hence dependent of φ_N and v_tot, if v_tot is not of constant value. Firstly, we have to find the maximum current ripple during one period of v_rec (v_tot assumed to be fixed). The maximum current ripple in the sector $\varphi_\mathrm{N}\left[\pi/3 \ldots 2\pi/3\right]$ can be evaluated, as v_rec is defined by

$$v_\mathrm{rec} = \sqrt{3}\hat{V}_\mathrm{N}\sin\left(\varphi_\mathrm{N}\right) \ . \tag{5.81}$$

φ_max yields $k\pi/3$ with $k \in \mathbb{Z}$ (cf., **Fig. 5.25**). The appropriate current ripple $\Delta i_\mathrm{c}\left(\varphi_\mathrm{N}\right)$ for different injection cell DC-link voltages can then be illustrated

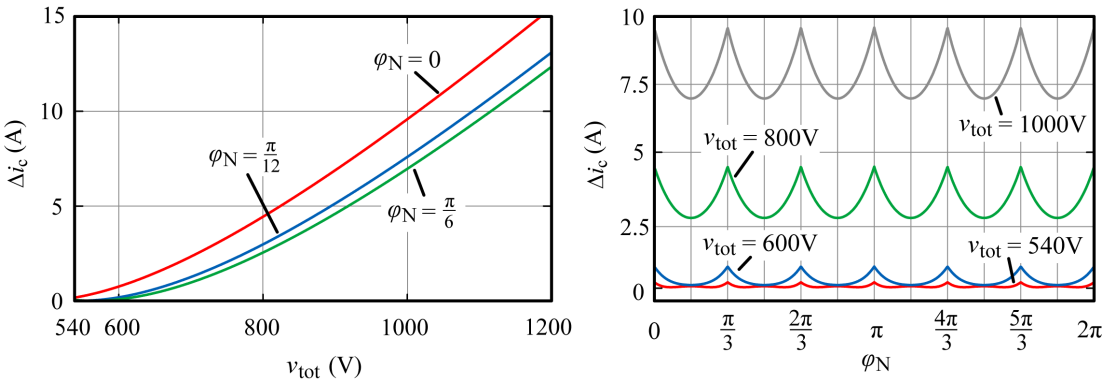


Fig. 5.25: Current ripple during start-up operation of third harmonic injection rectifier.

(depicted in **Fig. 5.25**). Obviously, the DC-link voltage during start-up should be controlled in such way that it is as small as possible (e.g. $v_{tot,su} = 1.05 \cdot 3\hat{V}_N$ $(+5\,\% V_{tot,su,min})$) as the dedicated current ripple during this process increases with x^2. The current ripple for a rectifier output voltage of 540 V and a DC-link voltage of $v_{tot} = 1000\,\mathrm{V}$, would result in $\Delta i_c \approx 8\,\mathrm{A}$.
If the maximum allowable busbar current is e.g. defined by $I_{pos,max} = 2I_o$, the maximum voltage controller gain results in

$$k_{p,su} = \frac{2I_o - I_o - \frac{\Delta I_L}{2} - \frac{\Delta I_c}{2}}{3\hat{V}_N\left(\xi_{su} - \frac{\sqrt{3}}{\pi}\right)} \approx 0.0125\,\mathrm{A/V} \tag{5.82}$$

which to leads to a maximum averaged peak current $I_{c,avg,max} \approx 6\,\mathrm{A}$. ξ_{su} is the deviation from the minimum required DC-link voltage for proper operation (e.g. 5 %, which results in $\xi_{su} = 1.05$), which should be chosen as small as possible to maintain a rather small current ripple with switching frequency. If the required minimum DC-voltage is reached, the already discussed control algorithm for sinusoidal input current regulation and dedicated bidirectional switch operation can be used again. Simulation results of the described start-up operation of the rectifier are illustrated in **Fig. 5.26**. In the following one feasible start-up sequence of the total rectifier system is discussed:

- Start-up (pre-charging) of passive rectifier with 1 kΩ resistors (one for each mains phase). Both $C_{cp} + C_{cn}$ and C_o are set to 540 V. Bidirectional switches are deactivated and both half-bridges are not operating. Not depicted in **Fig. 5.26**.
- Short circuiting of 1 kΩ resistors. Bidirectional switches are still deactivated and both half-bridges are not operating. Not depicted in **Fig. 5.26**.
- E.g. 10 kW B6 standalone operation. Bidirectional switches are deactivated and both half-bridges are not operating. Illustrated in **Fig. 5.26** (0 ms-10 ms).
- After approximately 10 ms, the third harmonic injection cell initiates its DC-link charging operation, which is going to boost the total DC-link up to 1 kV. After this minimum required DC-link voltage is reached, the required duty

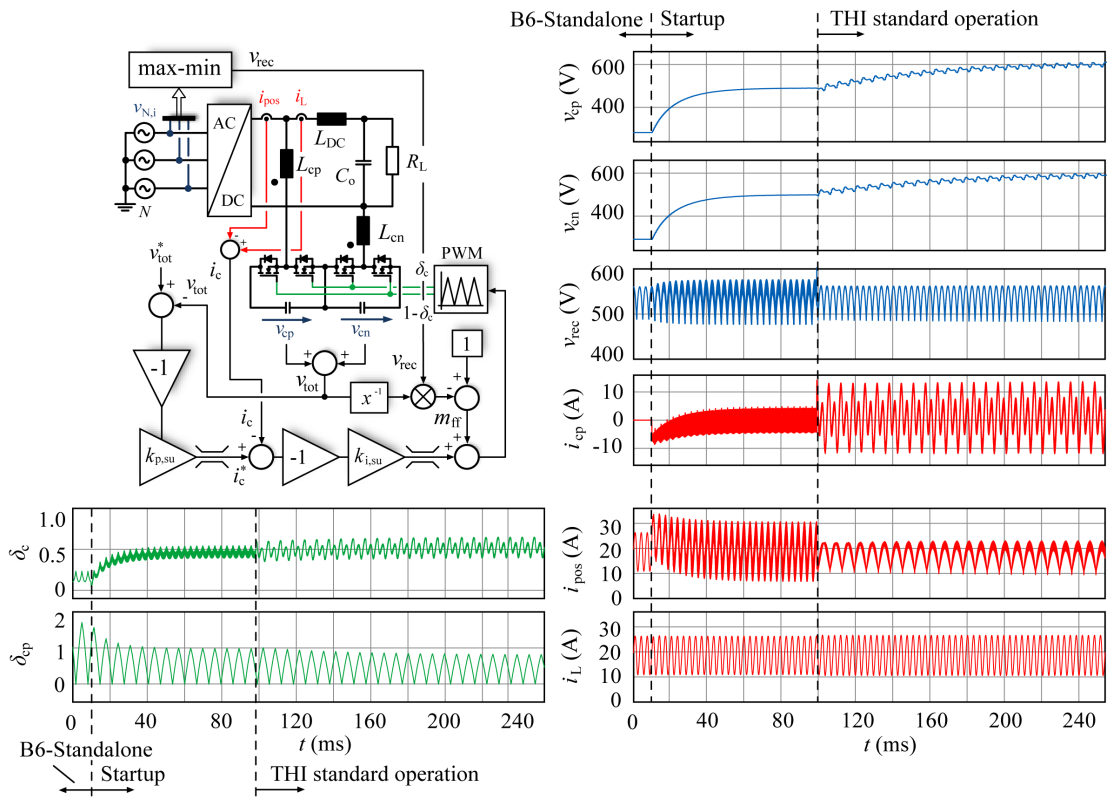


Fig. 5.26: Simplified model of rectifier system during start-up operation (10 ms-100 ms).

cycle δ_{cp} for sinusoidal input current control would no longer violate the upper boundary "1". Bidirectional switches are deactivated and both half-bridges are operating in the previously discussed combined mode (δ_c for S_{cp-} and S_{cn+}, $1-\delta_c$ for S_{cp+} and S_{cn-}). Illustrated in **Fig. 5.26** (10 ms-100 ms).

- The THI standard, control can now be applied. Bidirectional switches are activated and both half-bridges are controlled separately (δ_{cp} for S_{cp+} and δ_{cn} for S_{cn+}). Illustrated in **Fig. 5.26** ($>$ 100 ms).

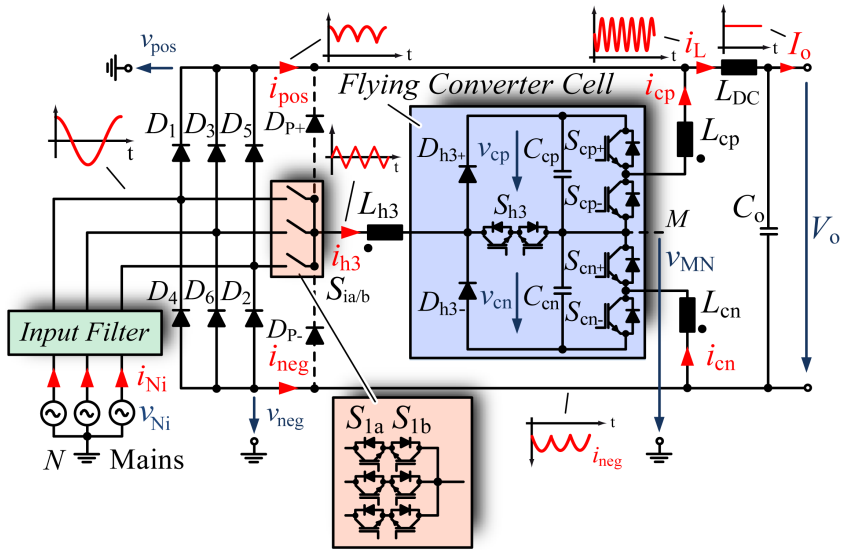


Fig. 5.27: Passive three-phase rectifier enhanced by an active FCC.

5.3 CSN Implementation - FCC

The Topology C in **Fig. 5.1** ("Flying Converter Cell" – FCC, cf., [25, 121, 128, 131]) consists of two half bridges ($S_{\mathrm{cp}\pm}$ and $S_{\mathrm{cn}\pm}$) connected to the positive and negative busbar at the output of the passive diode bridge (D_1-D_6). The interconnection between B6 and the current shaping network again is formed via injection inductors (L_{cp}, L_{cn} and L_{h3}). The current shaping network (here denoted as "Flying Converter Cell", FCC) now shows an additional three-level bridge leg (S_{h3}, $D_{\mathrm{h3}\pm}$). The three-level leg is cyclically connected to one of the three mains phases (which shows 0 A gaps according to passive rectification) by three bidirectional switches (S_1-S_3). The third harmonic inductor L_{h3} forms the interconnection between AC-side connected bidirectional switches and DC-side located current injection cell. The unidirectional three-level bridge leg consists of one bidirectional switch and two diodes. The implemented unidirectional branch actually originates from a 3-level T-type converter stage. Therefore, the outer diodes have to withstand the total DC voltage of $2V_{\mathrm{c}}$, whereas each component of the bidirectional switch (diodes and transistors) is stressed by V_{c}.
This additional three-level bridge allows the regulation of the midpoint to neutral point voltage v_{MN}. The averaged voltage $v_{\mathrm{MN,avg}}$ could be controlled in a range of $\pm V_{\mathrm{c}}$.

5.3.1 Topology Design

If e.g. $v_{\mathrm{MN,avg}}$ is (advantageously) controlled to be 0 V, the appropriate duty cycles of positive and negative half-bridge branches are going to change from

$$\delta_{\mathrm{cp}} = \frac{v_{\mathrm{pos}} - v_{\mathrm{h3}}}{V_{\mathrm{c}}} \tag{5.83}$$

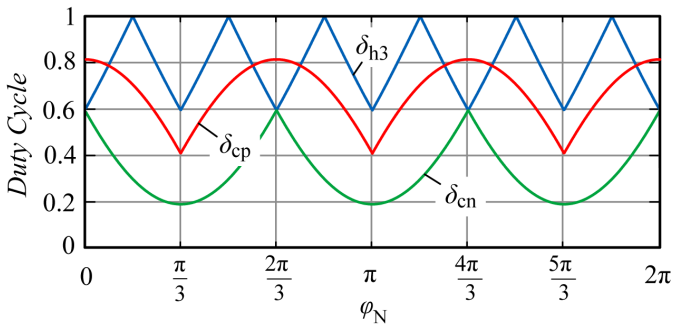


Fig. 5.28: Duty cycles of FCC converter stages considering $v_{\mathrm{MN,avg}} = 0\,\mathrm{V}$. δ_{cp}, δ_{cn}, δ_{h3} are appropriate duty cycles of half-bridge connected to C_{cp}, C_{cn} and three-level bridge leg, respectively.

$$\delta_{\mathrm{cn}} = 1 + \frac{v_{\mathrm{neg}} - v_{\mathrm{h3}}}{V_{\mathrm{c}}} \tag{5.84}$$

to

$$\delta_{\mathrm{cp}} = \frac{v_{\mathrm{pos}}}{V_{\mathrm{c}}} \tag{5.85}$$

$$\delta_{\mathrm{cn}} = 1 + \frac{v_{\mathrm{neg}}}{V_{\mathrm{c}}} \tag{5.86}$$

regarding an ideal inductor consideration ($L_{\mathrm{c}\frac{\mathrm{p}}{\mathrm{n}}} = 0$). The modulation index $M = \frac{3\hat{V}_{\mathrm{N}}}{2V_{\mathrm{c}}}$ can be adapted to $M = \frac{\hat{V}_{\mathrm{N}}}{V_{\mathrm{c}}}$, which allows an operation with reduced DC-link voltage levels of $V_{\mathrm{cp}} = V_{\mathrm{cn}} = V_{\mathrm{c}} = 400\,\mathrm{V}$ (compared to Top. A, B and D-F where at least 600 V is required).
For positive currents of i_{h3}, the duty cycle of the three-level bridge leg results in

$$\delta_{\mathrm{h3+}} = 1 - \frac{v_{\mathrm{h3}}}{V_{\mathrm{c}}}\,. \tag{5.87}$$

For negative currents of i_{h3}, $\delta_{\mathrm{h3-}}$ yields

$$\delta_{\mathrm{h3-}} = 1 - \frac{-v_{\mathrm{h3}}}{V_{\mathrm{c}}}\,. \tag{5.88}$$

The duty cycle of δ_{h3} finally results in

$$\delta_{\mathrm{h3}} = 1 - \mathrm{sgn}\left(i_{\mathrm{h3}}\right)\frac{v_{\mathrm{h3}}}{V_{\mathrm{c}}}\,. \tag{5.89}$$

The FCC's dedicated duty cycles for ideal injection inductors ($L_{\mathrm{c}\frac{\mathrm{p}}{\mathrm{n}}} = L_{\mathrm{h3}} = 0$) are depicted in **Fig. 5.28**. As the regulated output current i_{h3} and the derived duty cycle δ_{h3} of the three-level bridge leg is defined by fractions of i_{Ni} and v_{Ni} (which are both originating from sinusoidal waveforms), the current stress of the bidirectional switch (S_{h3}, D_{h3}) and the additional positive ($D_{\mathrm{h3+}}$) and negative ($D_{\mathrm{h3-}}$) freewheeling diodes can be calculated in an analytical way. The averaged and rms current stress of the bidirectional switch (S_{h3} and D_{h3}) yield

$$I_{S_{\mathrm{h3}},\mathrm{avg}} = I_{D_{\mathrm{h3}},\mathrm{avg}} = \hat{I}_{\mathrm{N}}\frac{24 - 12\sqrt{3} - M\left(2\pi - 3\sqrt{3}\right)}{8\pi}, \tag{5.90}$$

$$I_{S_{\mathrm{h3}},\mathrm{rms}} = I_{D_{\mathrm{h3}},\mathrm{rms}} = \frac{\hat{I}_{\mathrm{N}}}{2}\sqrt{\frac{2\pi - 3\sqrt{3}}{2\pi} + M\frac{9\sqrt{3}-16}{2\pi}} \ . \tag{5.91}$$

The current stress of the free-wheeling diodes results in

$$I_{D_{\mathrm{h3}\pm},\mathrm{avg}} = \hat{I}_{\mathrm{N}} M \frac{2\pi - 3\sqrt{3}}{8\pi}, \tag{5.92}$$

$$I_{D_{\mathrm{h3}\pm},\mathrm{rms}} = \frac{\hat{I}_{\mathrm{N}}}{2}\sqrt{M\frac{16-9\sqrt{3}}{2\pi}} \ . \tag{5.93}$$

Similar to already previously discussed rectifier topologies, also the FCC allows an inductor design, with either synchronized or phase shifted PWM signals. The triangular shaped carrier signals of the FCC's three converter stages can be (e.g.) synchronized which allows the optimization of the system behavior with respect to current ripple and/or midpoint voltage v_{MN}. **Fig. 5.29(a)** illustrates the dedicated PWM, the switching sequence and the resulting midpoint voltage v_{MN} at e.g. $\varphi_{\mathrm{N}} = 15\,^{\circ}$. For this specific case it is assumed that all three triangular shaped carrier signals are in phase. **Fig. 5.29(b)** depicts the situation where carrier signal S_{h3} is phase shifted by $180\,^{\circ}$. In order to analyze the system behavior a switching state (s_{cp}, s_{h3}, s_{cn}) can be defined where e.g. $s_{\mathrm{cp}} = 1$ denotes the turn-on state of the switch $S_{\mathrm{cp}+}$ (switch $S_{\mathrm{cp}-}$ is turned off) and $s_{\mathrm{cp}} = 0$ denotes the turn-on state of the switch $S_{\mathrm{cp}-}$ (switch $S_{\mathrm{cp}+}$ is turned off). As shown in **Fig. 5.29(a)** for $\varphi_{\mathrm{N}} = 15\,^{\circ}$ the midpoint voltage shows voltage levels of $\pm V_{\mathrm{c}}/3$, 0 and $\pm 2V_{\mathrm{c}}/3$ (symmetrical FCC DC-link voltages are assumed). If the carrier signal of the three-level bridge-leg is phase shifted by $180\,^{\circ}$ (cf., **Fig. 5.29(b)**) the midpoint voltage v_{MN} only results in $\pm V_{\mathrm{c}}/3$ and 0. On the other hand the current ripple of the injected currents increases considerably if the carrier signals are phase shifted by $180\,^{\circ}$.

If synchronized carrier signals without phase shift are assumed, the maximum current ripple calculates to

$$\Delta i_{\mathrm{c}\frac{\mathrm{p}}{\mathrm{n}},\mathrm{sync}} = \frac{V_{\mathrm{c}} M^2}{4 f_{\mathrm{s}} L} \tag{5.94}$$

$$\Delta i_{\mathrm{h3},\mathrm{sync}} = \frac{V_{\mathrm{c}} \frac{M}{2}\left(1 - \frac{M}{2}\right)}{f_{\mathrm{s}} L} \ . \tag{5.95}$$

If the carrier signals of the three-level bridge-leg result in a $180\,^{\circ}$ phase shift, the maximum current ripples of $i_{\mathrm{c}\frac{\mathrm{p}}{\mathrm{n}}}$ and i_{h3} lead to

$$\Delta i_{\mathrm{c}\frac{\mathrm{p}}{\mathrm{n}},180^{\circ}} = \frac{V_{\mathrm{c}}\left(M\frac{\sqrt{3}}{2} - \frac{1}{3}\right)\left(1 - M\frac{\sqrt{3}}{2}\right)}{f_{\mathrm{s}} L_{\mathrm{c}\frac{\mathrm{p}}{\mathrm{n}}}} \tag{5.96}$$

$$\Delta i_{\mathrm{h3},180^{\circ}} = \frac{V_{\mathrm{c}} \frac{1}{3}\left(1 - M\frac{\sqrt{3}}{2}\right)}{f_{\mathrm{s}} L_{\mathrm{h3}}} \ . \tag{5.97}$$

Therefore, the FCC facilitates an optimization regarding either minimum midpoint voltage v_{MN} or alternatively for minimum current ripple of injection currents.

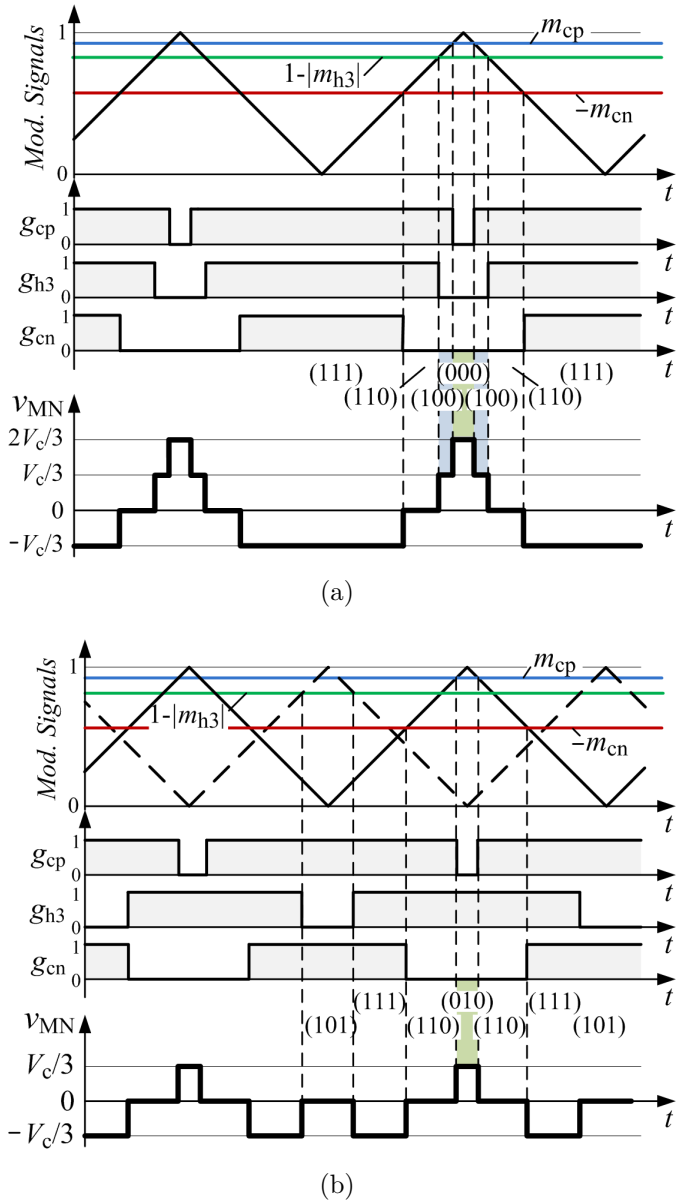


Fig. 5.29: Modulation of the three converter stages of the FCC using synchronized triangular shaped carrier signals at $\varphi_N = 15\,°$. (a) All three converter stages use carrier signals in phase and (b) the three-level bridge-leg uses a carrier signal with a phase shift of 180 deg.

Considering the previously derived equations for a proper inductor design for a rather low switching frequency of 10 kHz (being used because the 10 kW system implemented should act as a hardware demonstrator for a high-power system) of the active converter stage and a maximum allowable current ripple of $\Delta I_{cp,max} = 25\,\% I_{cp,rms}$ the inductance of the injection chokes results in 2.8 mH for L_{cp} and L_{cn}. Moreover, a three-phase iron-core inductor (with a material M400-50A) can be used in order to reduce the maximum volume of the chokes. Characteristics of such an implemented coil are given in **Fig. 5.30** and **Fig. 5.31**. Obviously, the inner leg shows a slightly higher inductance value than the outer ones of

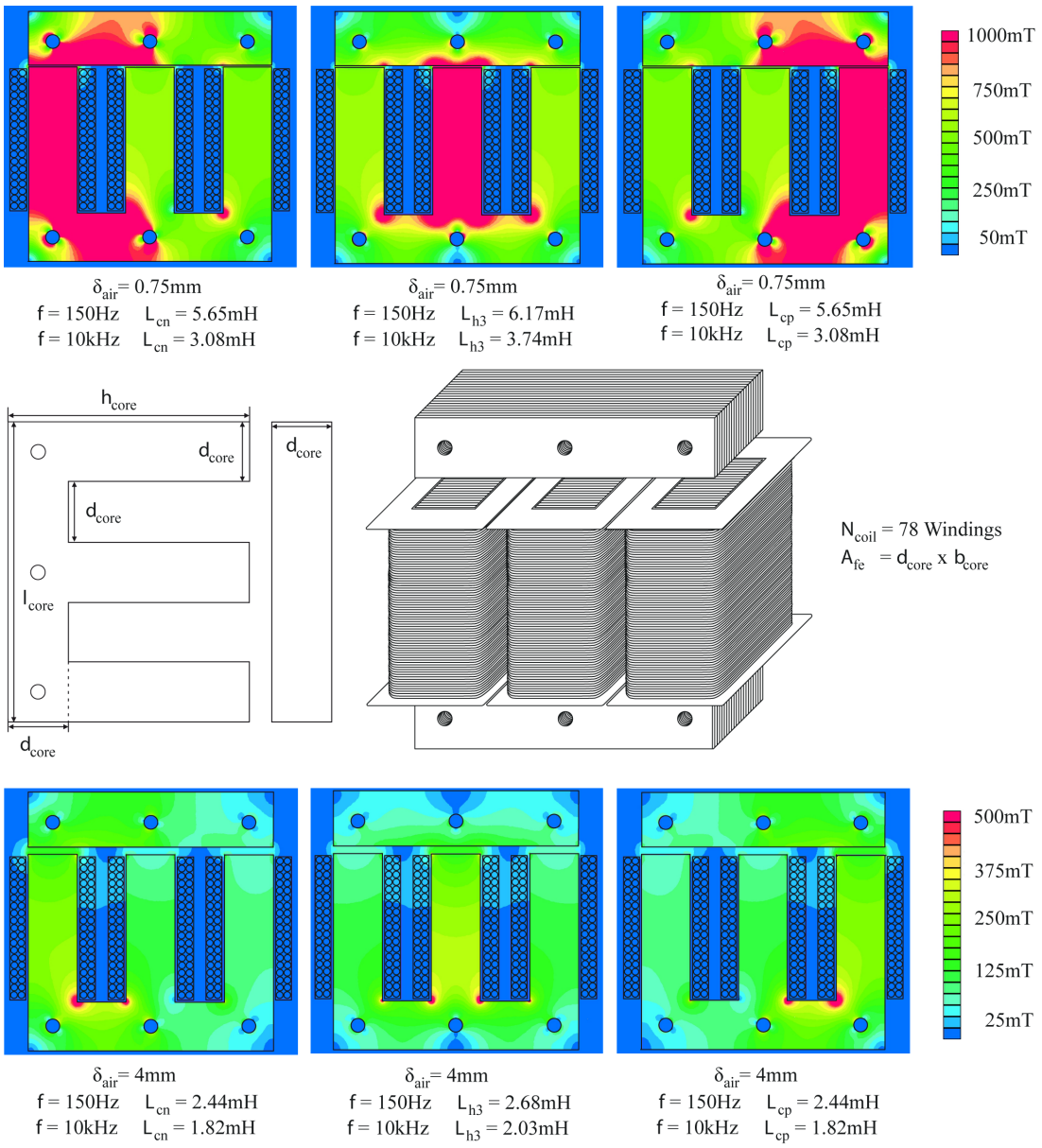


Fig. 5.30: Implemented three-phase inductor – material M400-50A. Illustrated core topology equals S3UI75b.

the EI - core assembly. It is recommended to connect the two respective half-bridges to the outer windings in order to guarantee approximately equal inductors L_{cp} and L_{cn}. Furthermore, one of the main characteristics of the used M400-50A material is a that its permeability is largely dependent on the frequency. This results in a tremendous inductance loss for frequency values at the switching frequency and above. This effect can be reduced if the air gap of the coil is increased (verified by FEMM simulation - cf., **Fig. 5.31**). The respective coils consist of 78 windings each. The appropriate measurement and simulation results are depicted in **Fig. 5.30**, **Fig. 5.31**, **Fig. 5.32(a)** and **Fig. 5.32(b)**.

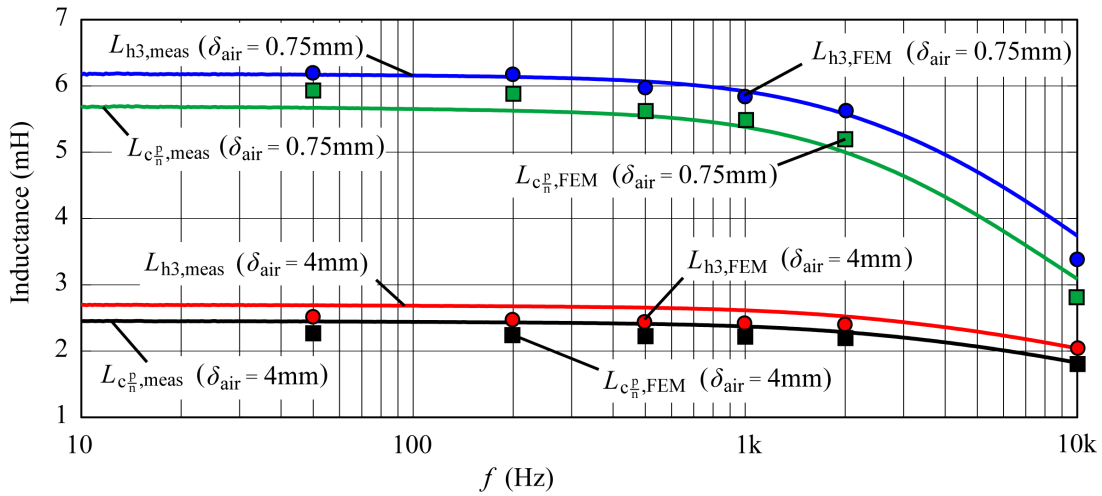
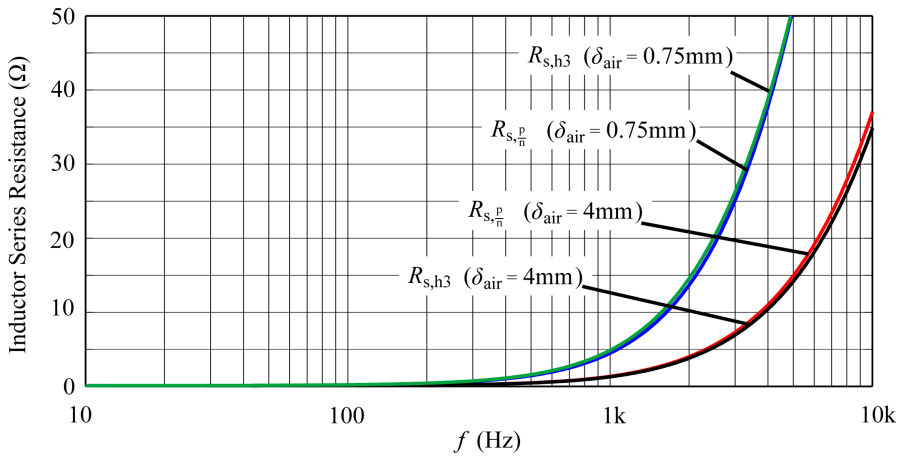
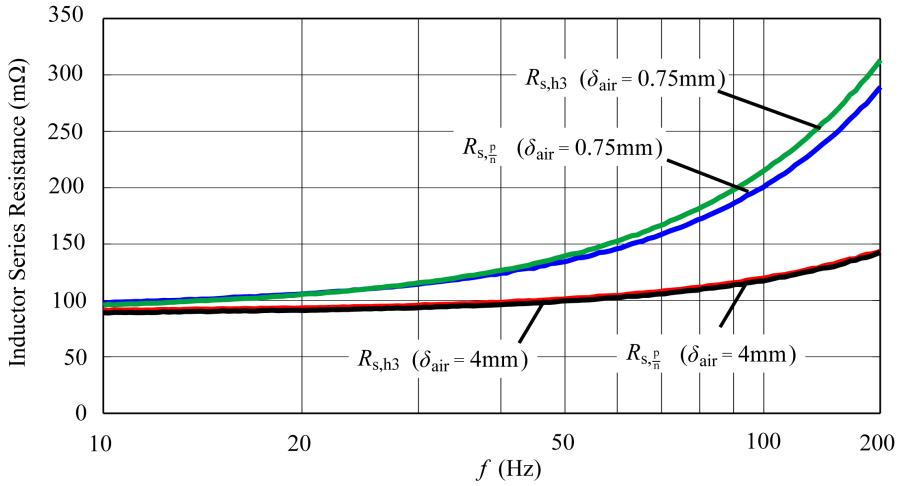


Fig. 5.31: Inductance of the three-phase iron inductor for different air gaps δ_{air}.



(a)



(b)

Fig. 5.32: Series winding resistance of respective three-phase inductor for different air gaps δ_{air}.

5.3.2 Controller Design

Several controllers are required for proper operation of the FCC rectifier. It is obvious that fast-acting current controllers are required to shape the mains currents. Furthermore, also controllers for the FCC DC-link voltages are necessary. A number of current and voltage sensors have to be included in the power circuit. Besides mains voltages $v_{\mathrm{N}i}$ also currents i_{pos}, i_{neg} and i_{L} are measured as well as the rectifier output voltage v_{rec} and also the midpoint voltage $v_{\mathrm{MN'}}$. As the output voltage V_{o} of the system is defined by the mains voltages v_{Ni} and is hence not controllable, sensing of V_{o} is not necessary.

Current Control

In the following the concept of average mode current control is used. The basic idea is to control the output currents i_{pos} and i_{neg} of the diode bridge (to the mentioned $2\pi/3$-periodically sinusoidal shape) by injecting adequate "compensational" currents i_{cp} and i_{cn} into the busbars as $i_{\mathrm{pos}} = i_{\mathrm{L}} - i_{\mathrm{cp}}$ and $i_{\mathrm{neg}} = i_{\mathrm{cn}} - i_{\mathrm{L}}$ applies. The two half bridges are therefore used for current control whereas the three-level bridge-leg is used for balancing of the FCC DC-link voltages and to control the average value of the midpoint voltage $v_{\mathrm{MN,avg}}$ to zero. Two independent current controllers are used for i_{pos} and i_{neg} and the current i_{h3} inherently results due to subtraction of i_{cp} and i_{cn}. For $\varphi_N \in [0 \ldots \frac{\pi}{6}]$ $(i_{\mathrm{N1}}(\varphi_{\mathrm{N}}) > 0;\, i_{\mathrm{N2}}(\varphi_{\mathrm{N}}), i_{\mathrm{N3}}(\varphi_{\mathrm{N}}) < 0)$

$$\begin{aligned}
\delta_{\mathrm{cp}} v_{\mathrm{cp}} + v_{\mathrm{MN,avg}} - v_{\mathrm{pos}} &= L_{\mathrm{c}} \frac{di_{\mathrm{cp}}}{dt} \\
(1 - \delta_{\mathrm{h3}})\,(-v_{\mathrm{cn}}) + v_{\mathrm{MN,avg}} - v_{\mathrm{mid}} &= -L_{\mathrm{c}} \frac{di_{\mathrm{h3}}}{dt} \\
(1 - \delta_{\mathrm{cn}})\,(-v_{\mathrm{cn}}) + v_{\mathrm{MN,avg}} - v_{\mathrm{neg}} &= -L_{\mathrm{c}} \frac{di_{\mathrm{cn}}}{dt}
\end{aligned} \tag{5.98}$$

can be calculated where equal inductors ($L_{\mathrm{c}} = L_{\mathrm{cp}} = L_{\mathrm{cn}} = L_{\mathrm{h3}}$) for the three converter stages are assumed. In sector $\varphi_N \in [0 \ldots \frac{\pi}{6}]$ $v_{\mathrm{pos}} = v_{\mathrm{N1}}$, $v_{\mathrm{mid}} = v_{\mathrm{N2}}$ and $v_{\mathrm{neg}} = v_{\mathrm{N3}}$ applies. Furthermore, equal (constant) voltages $V_{\mathrm{cp}} = V_{\mathrm{cn}} = V_{\mathrm{c}}$ are assumed (which is valid due to DC voltage and voltage balancing controller) for the current controller design. Also the average value of the midpoint voltage $v_{\mathrm{MN,avg}}$ can be treated as constant as it shows much smaller dynamic. Based on this simplification Laplace Transform can be applied. In the following the equation for current i_{cp} is exemplarily analyzed. Similar considerations have to be performed for all remaining currents:

$$sL_{\mathrm{c}} i_{\mathrm{pos}} = sL_{\mathrm{c}} i_{\mathrm{L}} - \delta_{\mathrm{cp}} V_{\mathrm{c}} - V_{\mathrm{MN,avg}} + v_{\mathrm{pos}}\ . \tag{5.99}$$

By inspecting **Fig. 5.27** it is obvious that the upper half bridge of the FCC must generate an average voltage which equals the voltage difference $v_{\mathrm{pos}} - V_{\mathrm{MN,avg}}$ (where $v_{\mathrm{pos}} = \max(v_{\mathrm{Ni}})$, which applies the very well known three-phase passive rectifier positive output bus voltage with respect to mains neutral point) which means that this voltage difference can advantageously be used as feed-forward signal. The current i_{L} acts as a disturbance input of the current control loop and

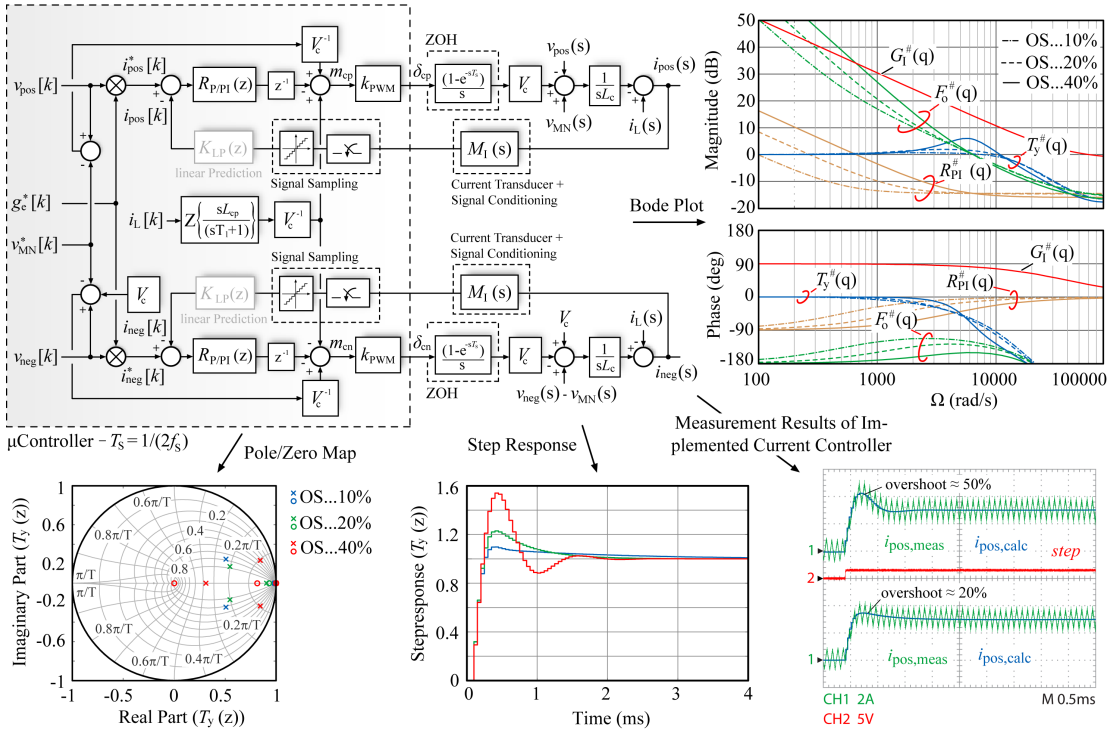


Fig. 5.33: Advanced current controller model, including derived PI-type current controller in q-domain, poles/zeros and step response of the appropriate closed loop transfer function in the z-plane and experimental results which compare measured step response of inductance current of FCC half-bridge with derived and calculated quantities.

disturbance rejection can be applied using the measured current value i_L. Using the resulting feed-forward signal

$$\delta_{cp} = \tilde{\delta}_{cp} + \frac{v_{pos} - V_{MN,avg}}{V_c} + s\frac{L_c i_L}{V_c\,(sT_1 + 1)} \tag{5.100}$$

together with **Eq. 5.99** results in the very simple current loop model

$$G_I(s) = \frac{i_{pos}(s)}{\tilde{\delta}_{cp}(s)} = -\frac{V_c}{sL_c}\ . \tag{5.101}$$

The required derivative block for i_L has to be extended by a low-pass filter T_1 with higher cut-off frequency for noise suppression. In **Fig. 5.33** the derived and advanced model in s- and z-domain (necessary due to signal sampling) is shown which is required for proper current controller design. The current controller $R_{P/PI}$ can be a P-type or a PI-type controller. A convenient PI-type controller design should also include occurring time delays (updated measured value to applied duty cycle, zero order hold ZOH, etc.). All quantities are therefore transferred into the continuous q-domain (also known as w-domain) using

$$G^{\#}(q) = G\left(z = \frac{1 + \frac{T_s}{2}q}{1 - \frac{T_s}{2}q}\right) \tag{5.102}$$

and $q = j\Omega$ whereas $\Omega = 2/T_s \tan(\omega T_s/2)$. This applied bilinear Tustin transformation is the Padè approximation of the term $e^{(j\Omega T_s)}$. The double update PWM

mode of the DSP can be advantageously be used in order to partially compensate the delay of the uniformly sampled PWM. The sample time T_s is defined by $1/\left(2f_\mathrm{s}\right)$. The system should be designed to achieve a rise time of $\approx 200\,\mu\mathrm{s}$ which results in an Ω_c of 6400 rad/s with $\Omega_\mathrm{max} = 0.2 \cdot 2/T_\mathrm{s} = 8000\,\mathrm{rad/s}$. Different controllers are designed for a maximum overshoot of the system step response of 10 %, 20 % and 40 % as depicted in **Fig. 5.33**. The obtained quantities of $R^{\#}_{P/PI}\left(q\right)$ (current controller), and $T^{\#}_{\mathrm{y,i}}\left(q\right)$ (closed-loop transfer-function) have to be transformed back into the z-plane. For a designed maximum overshoot of 40 % of the PI-type controller, actually a maximum overshoot of $\approx 50\,\%$ occurs. This is mainly evoked due to the additional zero in the closed loop transfer function due to the $(qT_\mathrm{I} + 1)$-term of the PI-type controller and the purely integral behaviour of G_I. This behaviour could be compensated or improved by using either pre-filtering technique, linear prediction $K_\mathrm{LP}\left(z\right)$ or a Smith-predictor. In order to verify proper controller design and validity of the derived model, the calculated parameters are implemented in the DSP of the FCC and one half-bridge is used as test circuit. Experimental results as depicted in **Fig. 5.33** are compared with the calculated step response functions of $T_{\mathrm{y,i}}\left(z\right)$.
As can be seen in **Fig. 5.33** the required reference currents $i^*_\mathrm{pos}\left[k\right]$ and $i^*_\mathrm{neg}\left[k\right]$ are generated by the passive rectifier output voltage ($v_\mathrm{pos}\left[k\right]$ and $v_\mathrm{neg}\left[k\right]$) multiplied with an equivalent conductance $g^*_\mathrm{e}\left[k\right]$. This equivalent conductance value can advantageously be used to control charge or discharge of the FCC DC-link capacitors $C_\mathrm{cp}/C_\mathrm{cn}$. The generation of g^*_e and its effects on the DC-link of the FCC is going to be discussed in the following subsection.

DC Voltage Control Structure

As previously discussed, the hybrid rectifier system basically consists of two capacitor stages, the uncontrolled DC-link output voltage V_o and the FCC DC-link voltage $v_\mathrm{cp} + v_\mathrm{cn}$. In order to reduce the number of voltage and current sensors the reference current signals for both half bridges are generated by measuring the three mains voltages $v_\mathrm{N1-3}$ and the DC-side smoothing inductor current i_L. Also the diode bridge rectifier output voltage $v_\mathrm{rec}\left(\varphi_\mathrm{N}\right)$ could be measured instead of $v_\mathrm{N1-3}$. v_rec can be assessed via the mains voltages ($v_\mathrm{rec} = \max(v_\mathrm{N1-3}) - \min(v_\mathrm{N1-3})$) and the transferred power from the AC input to the DC output can hence be determined by $p\left(\varphi_\mathrm{N}\right) = v_\mathrm{rec}\left(\varphi_\mathrm{N}\right) \cdot i_\mathrm{L}\left(\varphi_\mathrm{N}\right)$. The evaluated output power $p\left(\varphi_\mathrm{N}\right)$ is characterized by a low-frequency 300 Hz ripple component. The averaged output power P_o can hence be computed by using a digitally implemented low-pass filter. The dynamics of the developed (e.g. PT2) filter-type is going to define the step response quality of the FCC. The step response of the passive rectifier LC output filter is however affected according to the physical implementation of L_DC and C_o. The stringently required digital low-pass filter therefore has to meet two different objectives. Firstly, the digital filter has to be able to compete with the dynamic behaviour of the passive LC filter. Secondly, it has to perfectly reject the 300 Hz output power ripple. In case of insufficient damping, the generated reference currents (i^*_pos, i^*_neg) and hence the mains input currents (i_Ni) will show increased 5th

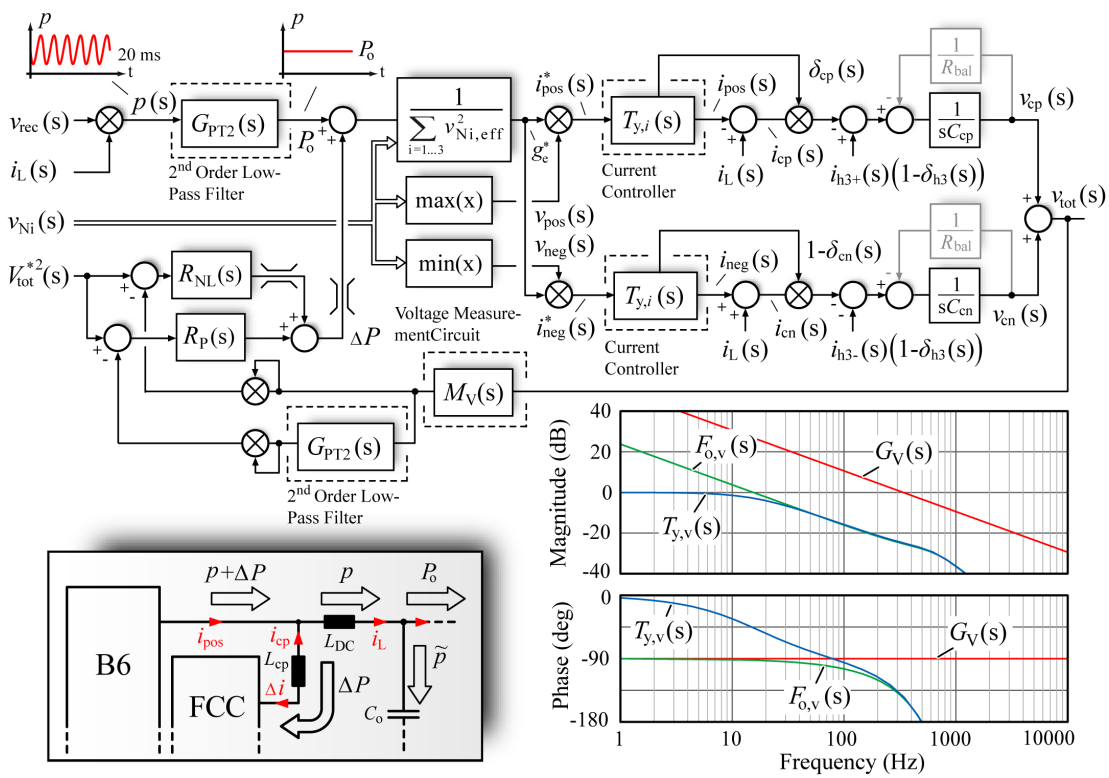


Fig. 5.34: Derived voltage controller model, including inner loop current controller, and superimposed P-type and nonlinear voltage control structure.

and 7th harmonic spectral components and therefore an impaired THD_i would appear (cf., **Fig. 5.34**, which depicts the voltage controller circuit with subsequent current controller). If an substantial lack of FCC system dynamics is considered the FCC DC voltages v_cp/v_cn will show a high deviation of the expected nominal value $V^*_\text{tot}/2$ for load steps of the rectifier which will in turn affect the proper operation of the DC-link voltage if v_cp/v_cn of one half-bridge appears to be $< \hat{V}_\text{N}$. In order to illustrate the discussed issue more accurately, a load step of the active system is briefly discussed. In case of a load step of e.g. 10 kW to 3 kW the passive system immediately reacts with a response time of $\approx$ 2 ms (for e.g. $L_\text{DC} = 2.25\,\text{mH}$, $C_\text{o} = 1.1\,\text{mF}$, $R_\text{o,ESR} = 0.23\,\Omega$ and $R_\text{DC} = 0.3\,\Omega$). If a first order 50 Hz digital low-pass filter structure is assumed for filtering of $p\,(s)$ the proper output power is reached after $\approx$ 100 ms. Till then, the difference of real (p) and fictitious output power ($p + \Delta P$) has to be processed by the FCC ($p_\text{FCC} = p + \Delta P - p$) which results in an increase (if no appropriate voltage controller is applied) of capacitor voltages v_cp and v_cn (as FCC DC capacitors are going to be charged as long as $p_\text{FCC} \neq 0$). The DC-link of the passive system remains almost constant (depending on the load characteristic) for such a load step. Similarly to previously made assumptions, discharging of the FCC DC-link capacitors applies for an increased load step of the system (e.g. 3 kW$\rightarrow$ 10 kW). A load step can therefore be perceived by monitoring the FCC DC voltage levels (v_cp/v_cn).

In order to guarantee not only a properly filtered output power but also a feasible system dynamics the measurement circuit – which evaluates the constant

output power demand – can be extended by a voltage control path which consists of a standard P-type controller (to set the proper averaged DC voltage levels $v_{\mathrm{cp}} + v_{\mathrm{cn}} = V_{\mathrm{tot}}^{*}$) and a nonlinear controller to improve the dynamics of the FCC (which is impaired due to digital power filtering). The nonlinear part of the voltage controller appears to be zero for small variations and sensitive to demonstrative deviations of the nominal DC voltage level (V_{tot}^{*} calculates to 800 V for the given topology, as discussed in [22]). The design of the voltage controller is dependent on the implemented digital low-pass filter which is supposed to provide the averaged output power P_{o}. The dedicated voltage controller generates some fraction of power ΔP which is added to the measured output power which can be used to compensate some instantaneously missing power (due to filtering) during load steps or to increase or decrease the input power to charge or discharge FCC DC voltage link capacitors on purpose. The additional slowly responding P/PI-controller leg accurately adjusts the required DC voltage level of the FCC. Therefore, the low-frequency voltage ripple of the FCC DC voltages evoked due to $\delta_{\mathrm{cp}} i_{\mathrm{cp}}$ and $\delta_{\mathrm{h3}} i_{\mathrm{Dh3+}}$ affects the quality of the mains input currents in the same manner as the previously discussed 300 Hz output power ripple.
Considering all previously made assumptions and concerns, the voltage controller model can be derived and calculates to

$$G_{\mathrm{V}}(s) = \frac{V_{\mathrm{tot}}^{2}}{\Delta P} = \frac{2\left(C_{\mathrm{cp}} + C_{\mathrm{cn}}\right)}{s C_{\mathrm{cp}} C_{\mathrm{cn}}} = \frac{2}{s C_{\mathrm{tot}}}\,. \tag{5.103}$$

The P-type voltage controller gain can hence be easily computed according to the open-loop transfer function. According to **Fig. 5.34**, the closed-loop transfer-function of the slow responding path can be assessed by

$$T_{\mathrm{y,v}} = \frac{\left(s + \frac{1}{T_{\mathrm{I}}}\right)}{s^{3}\frac{\pi^{2} L_{\mathrm{c}} C_{\mathrm{tot}}}{18 k_{\mathrm{p,v}} V_{\mathrm{I}} T_{\mathrm{I}}} + s^{2}\frac{\pi^{2} C_{\mathrm{tot}}}{18 k_{\mathrm{p,v}}} + s\left(\frac{\pi^{2} C_{\mathrm{tot}}}{18 k_{\mathrm{p,v}} T_{\mathrm{I}}} + 1\right) + 1}, \tag{5.104}$$

with V_{I} and T_{I} as values of the designed PI-type current controller $V_{\mathrm{I}}\left(s T_{\mathrm{I}} + 1\right)/s$. Measurement results which compare calculated and measured step-response of the system will be finally illustrated in **Fig. 6.24**. Furthermore, only positive power flow is allowed due to passive diode bridge rectification. The total controller minimum output is hence limited to $P_{\mathrm{min}} = P_{\mathrm{o}} - \Delta P > 0\,\mathrm{W}$. The maximum limit of the voltage controller (P_{max}) mainly depends on physical constraints of the B6 bridge and the FCC active switches. The equivalent electric conductance g_{e}^{*} can be determined by

$$g_{\mathrm{e}}^{*} = \frac{P_{\mathrm{o}} + \Delta P}{\sum\limits_{i=1\ldots3} v_{\mathrm{Ni,eff}}^{2}} \tag{5.105}$$

The reference currents of the FCC hence finally result in $i_{\mathrm{pos}} = g_{\mathrm{e}}^{*} v_{\mathrm{pos}}$, $i_{\mathrm{h3}} = g_{\mathrm{e}}^{*} v_{\mathrm{h3}}$ and $i_{\mathrm{neg}} = g_{\mathrm{e}}^{*} v_{\mathrm{neg}}$. The derived voltage control of the active system is however merely able to manipulate the total DC voltage level of the injection cell ($v_{\mathrm{cp}} + v_{\mathrm{cn}}$). In order to prevent imbalance of both voltages a DC voltage balancing concept has been derived in [25] which is briefly discussed in the following subsection.

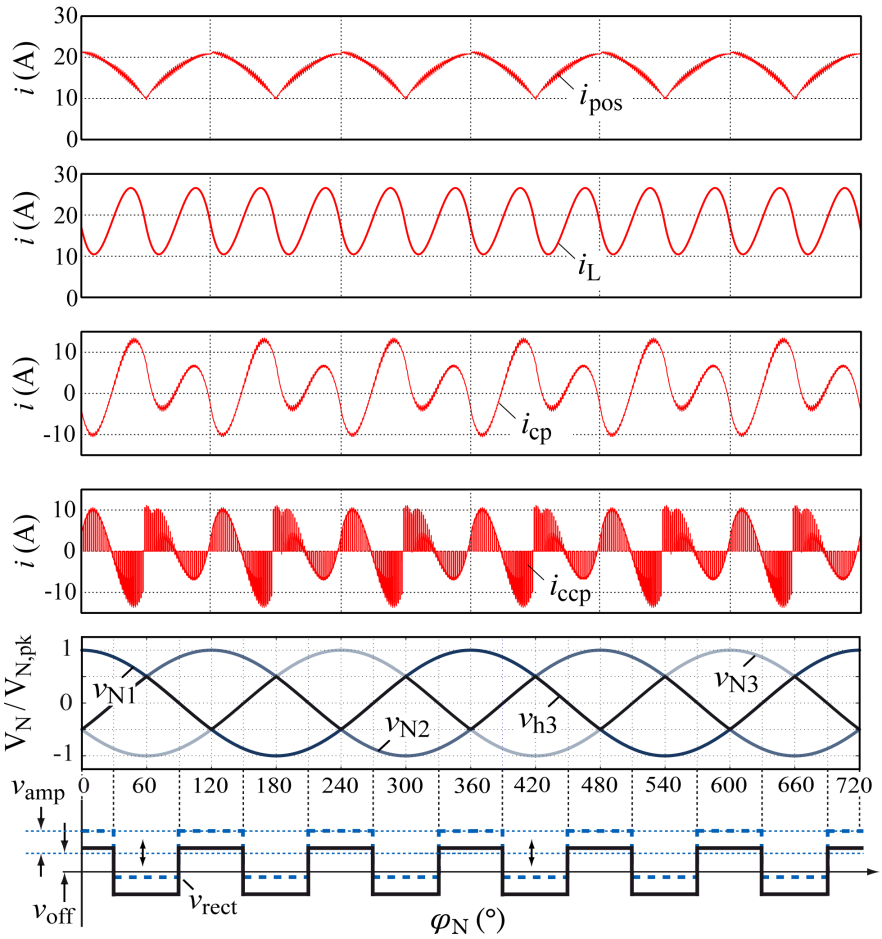


Fig. 5.35: Proposed active voltage balancing algorithm by advantageously regulating the midpoint voltage $v^*_{\mathrm{MN,avg}} = v_{\mathrm{amp}} \cdot \mathrm{rect}\,(\varphi_{\mathrm{N}}) + v_{\mathrm{off}}$ implemented as rectangular signal $v_{\mathrm{rect}} (= v_{\mathrm{amp}} \cdot \mathrm{rect}\,(\varphi_{\mathrm{N}}))$ with corresponding offset v_{off} and appropriate DC-side smoothing inductance current i_{L}, positive DC bus injection current i_{cp} and DC bus input current i_{pos}.

DC Voltage Balancing Concept

Imbalance of DC capacitor voltages typically results due to parasitic effects (e.g. capacitor leakage currents, interlock delay, unsymmetrical PWM signals, gate drives etc.). In order to evaluate the effect due to unsymmetrical parasitic components (e.g. capacitor ESR) considering unbalanced capacitor voltages, an extended model is required which includes inductor voltage drops (v_{Lcp}, v_{Lcn}, v_{Lh3}), DC ($R_{\mathrm{DC,cp}}$, $R_{\mathrm{DC,h3}}$, $R_{\mathrm{DC,cn}}$) and equivalent series resistances ($R_{\mathrm{ESR,cp}}$, $R_{\mathrm{ESR,cn}}$) of coils and capacitors etc. Inductor voltage drops (v_{Lcp}, v_{Lcn}, v_{Lh3}) have to be considered due to the used rather low switching frequency (10 kHz). Consequently, significantly high inductance values (L_{cp}, L_{cn}, L_{h3}) of approximately 2.6mH are assumed. Design guidelines considering the active rectifier injection inductances are discussed in detail in [22]. A calculation of I_{ccp} or I_{ccn} is not possible in an analytical way due to the definition of the currents i_{cp} and i_{cn} and has hence been determined numerically. The maximum current that needs to be regulated by an

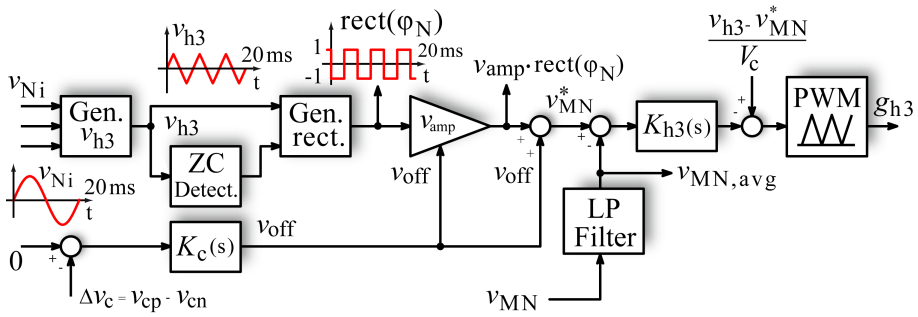


Fig. 5.36: Modified midpoint voltage controller considering the proposed voltage balancing algorithm $v^*_{MN,avg}$.

implemented active balancing concept can be assessed numerically to

$$I_{cc,max} = \frac{I_{ccp} - I_{ccn}}{2} \approx 1.5\,\text{mA}\,(P_o = 10\,\text{kW}) \tag{5.106}$$

for dedicated values $R_{ESR,cp} = 120\,\text{m}\Omega$, $R_{ESR,cn} = 180\,\text{m}\Omega$, $R_{DC,cp} = 152\,\text{m}\Omega$, $R_{DC,cn} = 163\,\text{m}\Omega$ and $R_{DC,h3} = 157\,\text{m}\Omega$. Symmetrical DC and ESR values ($R_{ESR,cp} = R_{ESR,cn}$ and $R_{DC,cp} = R_{DC,cn} = R_{DC,h3}$) would lead to $I_{cc,max} = 0\,\text{A}$. Basically, detailed analyses (of e.g. feasible switching states) revealed that the midpoint voltage v_{MN} can be utilized to achieve different currents in both DC-link capacitors C_{cp} and C_{cn}.

A purely regulated offset can be employed to intensify or reduce hardly applied switching states of the FCC. However, adding a simple offset to all three duty cycles (δ_{cp}, δ_{cn}, δ_{h3}) will permanently violate the upper boundary of δ_{h3} ("1") and hence does not fit the requirements of an undisturbed current generation of i_{cp}, i_{cn} and i_{h3}. This applies for all continuous functions as e.g. sinusoidal, triangular shaped waveforms etc. Therefore, a square wave signal due to its discontinuity (as shown in **Fig. 5.35**) is used to prevent δ_{h3} from exceeding its limit ("1"). An additional offset can now be added to the rectangular shaped modulation signal. The very simple midpoint voltage balancing algorithm (v^*_{MN}) thus can be written as

$$v^*_{MN,avg} = v_{amp} \cdot \text{rect}\,(\varphi_N) + v_{off} \tag{5.107}$$

while v_{amp} denotes the amplitude of the rectangular signal (rect (φ_N)) and v_{off} the adjacent offset. **Fig. 5.35** illustrates most important voltage waveforms and currents i_{pos}, i_L, i_{cp} and i_{ccp} of the system. The generation of the implemented nominal midpoint voltage is depicted in **Fig. 5.36**. The triangular shaped voltage v_{h3} can be generated by measured mains voltages v_{N1-3} and calculates to

$$v_{h3} = -\max\,(v_{N1}, v_{N2}, v_{N3}) - \min\,(v_{N1}, v_{N2}, v_{N3}). \tag{5.108}$$

The rectangular shaped signal (rect (φ_N)) has to be formed in such way, that it has to reverse its sign each time v_{h3} changes in sign ($\frac{\pi}{6}$, $\frac{\pi}{2}$, $\frac{5\pi}{6}$,...). A detector in order to determine zero crossings of v_{h3} is necessary. An additional controller is used in order to compute the required voltage offset value (v_{off}). Ideally, the

calculated value has to equal the magnitude of the rectangular signal ($v_{\text{amp}} = v_{\text{off}}$) depending on the DC-link voltage situation ($\Delta v_{\text{c}} = v_{\text{cp}} - v_{\text{cn}}$). If e.g. v_{cp} (instantaneous capacitor voltage of C_{cp}) shall be increased, a negative voltage offset is required. This negative DC offset will simultaneously lead to capacitor discharging of C_{cn}. In order to evaluate main characteristics of the proposed balancing algorithm a simplified model of the FCC was assumed (neglecting inductor voltage drops, parasitic components and resistances). Averaged currents for C_{cp} and C_{cn} can be found as

$$\begin{aligned} I_{\text{ccp}} &= \frac{1}{6} \cdot \frac{\hat{I}_{\text{N}} \cdot v_{\text{off}} \left(-18 + \pi^2\sqrt{3}\right)}{\pi V_{\text{c}}} \\ I_{\text{ccn}} &= -\frac{1}{6} \cdot \frac{\hat{I}_{\text{N}} \cdot v_{\text{off}} \left(-18 + \pi^2\sqrt{3}\right)}{\pi V_{\text{c}}} \ . \end{aligned} \tag{5.109}$$

Obviously, I_{ccp} and I_{ccn} conform to a linear dependency of v_{off}. The balancing algorithm is furthermore characterized by the rated output power which is indicated by $\hat{I}_{\text{N}}$. The offset v_{off} and the amplitude v_{amp} of $v^*_{\text{MN,avg}}$ can hence not remain fixed for diverging loads. Assuming e.g. an offset (v_{off}) of 8 V (for 10 kW output power), v_{off} has to be increased for partial and light loads to achieve similar induced capacitor currents due to decreased values of $\hat{I}_{\text{N}}$.

In order to guarantee proper operation of the balancing concept the generated rectangular signal has to comply with a set of constraints which are going to be defined in the following. Considering δ_{h3} (cf. **Fig. 5.37(a)**), $v_{\text{amp}} > 0$ (1st constraint) and $v_{\text{amp}} \geq |v_{\text{off}}|$ (2nd constraint) has to be fulfilled. In order to use the maximum balancing capability, the offset v_{off} should be chosen in the same size of the rectangular amplitude v_{amp}, $v_{\text{off}} = v_{\text{amp}}$ (3rd constraint). Considering δ_{cp}, δ_{cn} positive and negative limits for the offset voltage v_{off} can be determined to

$$v_{\text{off,lim}} = \pm \frac{V_{\text{c}} - \sqrt{3}\hat{V}_{\text{N}} \left[\frac{1}{2} + \frac{L_{\text{c}}}{L_{\text{DC}}}\left(1 - \frac{3}{\pi}\right)\right] - \frac{\omega_{\text{N}} L_{\text{c}} \hat{I}_{\text{N}}}{2}}{2} \tag{5.110}$$

(4th constraint). For $P_{\text{o}} = 10$ kW, L_{c} of 2.6 mH, a DC-side smoothing inductance of 2.25 mH and FCC DC voltages (V_{c}) of 400 V, the maximum limit of the midpoint voltage offset $v_{\text{off,lim}}$ approximately results in 40 V. Equation **Eq. 5.110** indicates that even for no load mode of the active system, $v_{\text{off,lim}}$ is merely enlarging to 44 V. As mentioned, a rectangular shaped signal is required to prevent δ_{h3} from exceeding its upper limit ("1"). The occurring step characteristic (in all three duty cycles δ_{cp},δ_{cn} and δ_{h3}) causes small deviations in the modulation signals for i_{pos}, i_{neg} and i_{h3} as the voltage controller of the three-level bridge leg can not ideally follow the implemented step. The unidirectional three-level bridge leg is only able to increase or decrease the midpoint voltage of the FCC with a diminutive delay. It is mandatory to keep v_{amp} as small as possible to minimize current distortions but high enough to guarantee minimum averaged currents for FCC capacitor voltage balancing. The adapted midpoint voltage has to be considered as feed-forward signal for current controllers and midpoint voltage controller (cf., **Fig. 5.33** and **Fig. 5.36**). The corresponding duty cycles (δ_{cp}, δ_{cn}, δ_{h3}) for the

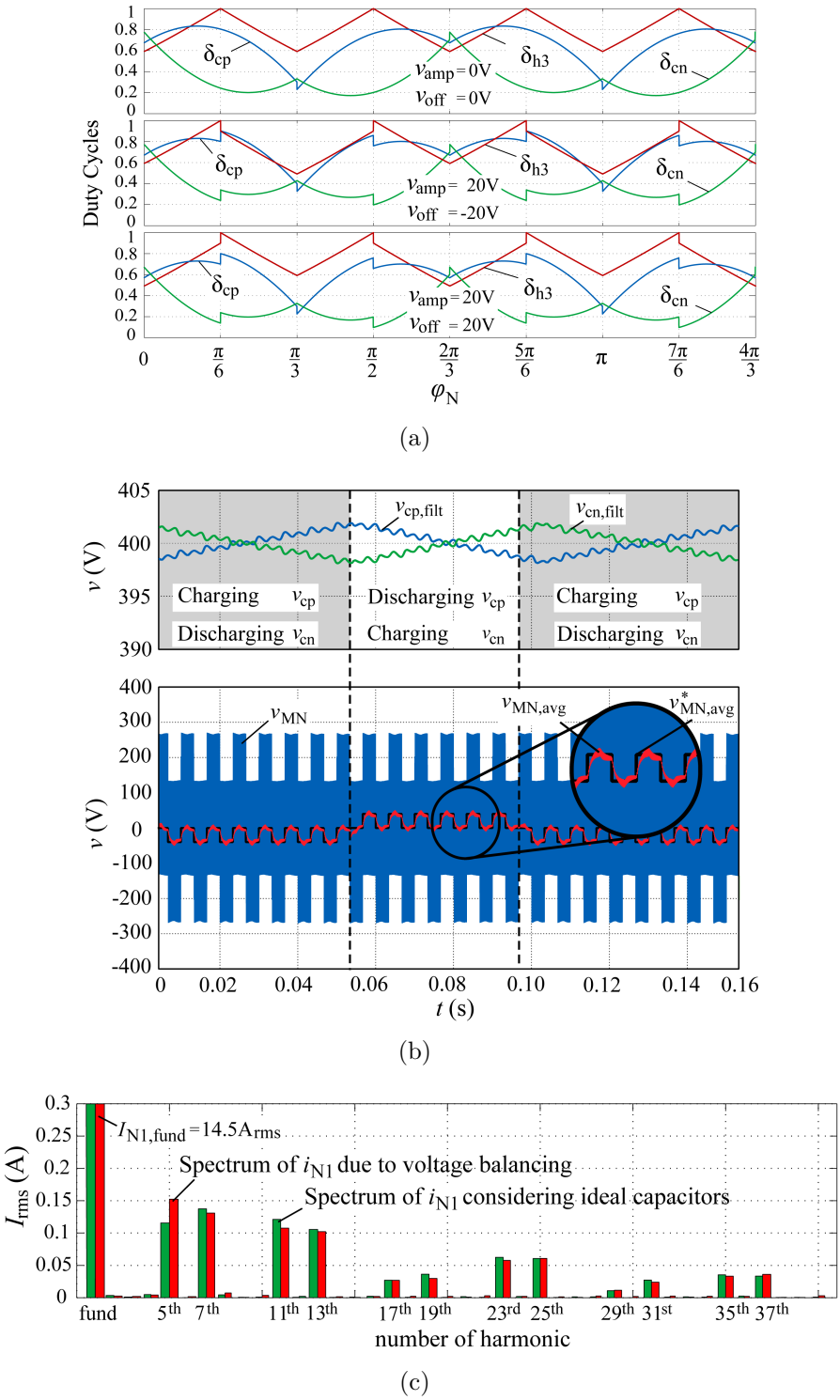


Fig. 5.37: (a) Adapted duty cycles δ_{cp}, δ_{cn} and δ_{h3} considering injection inductor voltage drops and averaged midpoint voltage $v_{\mathrm{MN,avg}}$. (b) Simulation results regarding DC voltage control and balancing (v_{cp},v_{cn}) and appropriate nominal ($v^{*}_{\mathrm{MN,avg}}$) and real signal waveforms of the midpoint to neutral point voltage v_{MN} and $v_{\mathrm{MN,avg}}$. (c) Mains input current (i_{N1}) spectrum.

dedicated current and voltage controllers, regarding deactivated voltage controller ($v_{\mathrm{off}} = v_{\mathrm{amp}} = 0\,\mathrm{V}$), generation of a positive ($v_{\mathrm{off}} = v_{\mathrm{amp}} = 20\,\mathrm{V}$) averaged midpoint voltage v_{MN} and causing a negative offset value ($v_{\mathrm{off}} = -20\,\mathrm{V}$, $v_{\mathrm{amp}} = 20\,\mathrm{V}$), are illustrated in **Fig. 5.37(a)**. In contrast to [22] where inductance voltage drops are neglected the duty cycles depicted in **Fig. 5.37(a)** are considering injection inductance voltage drops which obviously appear as mandatory side effects for low switching frequency (10 kHz) applications.
In **Fig. 5.37(b)**, simulation results of the implemented balancing concept are shown. Both DC voltages v_{cp} and v_{cn}, the averaged ($v_{\mathrm{MN,avg}}$ - red), the nominal averaged ($v^{*}_{\mathrm{MN,avg}}$ - blue) as well as the instantaneous (v_{MN} - green) midpoint voltage are illustrated and depict charging and discharging cycles of the FCC capacitors C_{cp} and C_{cn}. The spectrum of one mains phase input current (i_{N1}) regarding the implemented balancing concept compared to implemented ideal capacitors ($C_{\mathrm{cp}} = C_{\mathrm{cn}} = \infty$) is finally visualized in **Fig. 5.37(c)**. The $\mathrm{THD_i}$ considering the ideal capacitor case was simulated to 1.85 % and regarding voltage controller and balancing concept yields 1.86 %. Hence, virtually no additional input current distortions for a range between 50 Hz and 2 kHz could be observed.

5.4 CSN Implementation - Three-Level Topologies

Previous sections discussed THI circuits where the current shaping network has been implemented as "center-tapped" full-bridge, two half-bridges connected in series, or with an additional unidirectional three-level bridge leg in order to control the midpoint voltage v_{MN} (Topologies A,B,C in **Fig. 5.1**).
The active circuit extension however can also be realized by two three-level branches in back-to-back arrangement (as proposed in [24]), in a similar manner as Topology A which is based on a back-to-back arrangement of two two-level legs. Three different three-level leg types (neutral point clamped (NPC) - [132–136], T-Type - [99, 137–139] and Flying Capacitor - [140]) will be discussed in this work.
The proposed rectifier circuits are depicted in **Fig. 5.38**. All of these three-level converter cells will result in a 600 $\mathrm{V_{DC}}$ DC-voltage for each capacitor C_{cp} and C_{cn}. Each three-level topology is capable of generating $+V_{\mathrm{c}}$, 0 V and $-V_{\mathrm{c}}$ at the output. Therefore these topologies are not limited to a purely positive duty cycle. Their duty cycle range is hence extended to $[-1 \ldots 1]$ compared to a standard half-bridge (which can only facilitate a duty cycle of $[0 \ldots 1]$). Due to the relatively high DC-link voltage it is important to consider the following benefits and drawbacks for the three different solutions:

Flying Capacitor:

+ 4 switches are necessary per leg.
+ Only 900/1200 V switches are required.
− Causes almost twice as much capacitor volume than the T-type or NPC solution. This is mainly evoked due to its additional capacitor banks which are required to achieve the 0 V at the output. Furthermore, 0 V at the output of the three-level branch can only be achieved if all three capacitor stages (C_{cp}, C_{cn} and C_{F}) are perfectly balanced. Even a small imbalance ($> 0\,\%$) leads to deviations and distortions in the generated output voltage, and a highly sophisticated voltage/current controller is hence required.
− Two additional isolated voltage sensors and controllers are necessary in order to guarantee these fixed DC voltage levels of both C_{cp}, C_{cn} and C_{Fp}, C_{Fn}.

T-Type:

+ Rather low in complexity.
+ 4 switches are necessary per leg.
+ 900/1200 V switches can be used for S_{p0} and S_{n0}
− 1700 V switches are required for $S_{\substack{\mathrm{p}\\ \mathrm{n}}\pm}$ due to a maximum blocking voltage stress of 1200 V (considering switching transients and safety margins). These switches tend to result in higher switching and conduction losses compared to their 900/1200 V counterparts. Therefore, also the switching frequency

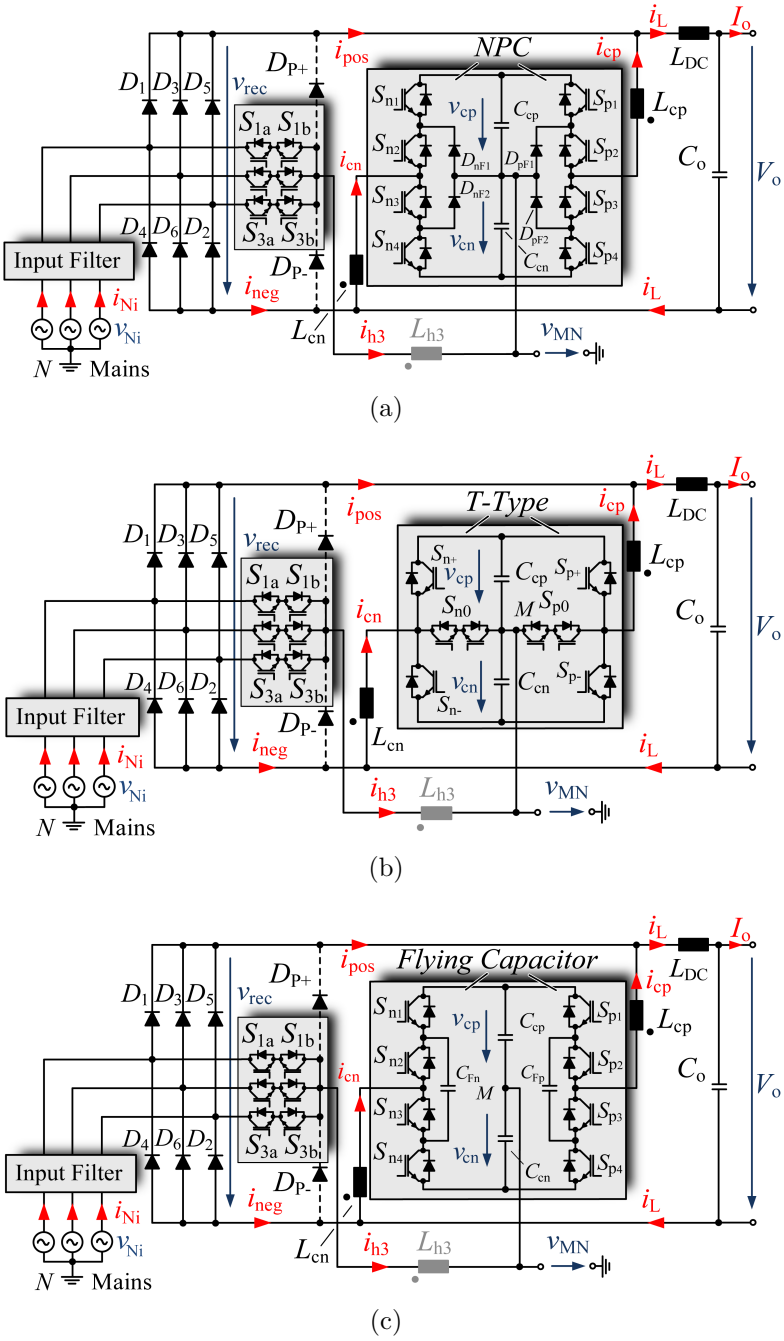


Fig. 5.38: Implementations of the CSN using either (a) NPC, (b) T-Type or (c) Flying Capacitor three-level converter branches.

range of the active system would be limited.

NPC:

+ All switches can be implemented as 900/1200 V IGBTs, SiC-MOSFETs and diodes.
− A higher number of semiconductors is required (four switches and two diodes for each leg) as additional diodes are required to directly clamp the converter structure to the cell's midpoint potential to generate the 0 V potential at the

output of the appropriate stage.

It is stated in [21] that for higher switching frequencies (e.g. $> 40\,\mathrm{kHz}$) the NPC topology results in a higher efficiency than the T-type solution ($\eta_{NPC} \approx 98.5\,\%$, $\eta_{TT} \approx 98.2\,\%$ at $\approx 50\,\mathrm{kHz}$). For lower values of f_s, the T-type may achieve a better performance in efficiency ($\eta_{NPC} \approx 98.8\,\%$, $\eta_{TT} \approx 99.1\,\%$ at $\approx 10\,\mathrm{kHz}$).

5.4.1 Three-Level Converter Switching States

All mentioned three-level branches consist of four active switches and are necessary to generate controllable output voltage levels $+V_\mathrm{c}/0\,\mathrm{V}/-V_\mathrm{c}$ for bipolar output currents. This generally applied control method considers $+V_\mathrm{c}/0\,\mathrm{V}$ to realize positive averaged output voltage levels $v_\mathrm{xM,avg}$ and $0\,\mathrm{V}/-V_\mathrm{c}$ for negative values, respectively. The different valid switching states of each three-level branch are listed in the following:

Flying Capacitor:

- State 1: S_p1 and S_p2 closed: $v_\mathrm{xM} = V_\mathrm{cp}$
- State 2: S_p1 and S_p3 closed: $v_\mathrm{xM} = 0\,\mathrm{V}$
- State 3: S_p2 and S_p4 closed: $v_\mathrm{xM} = 0\,\mathrm{V}$
- State 4: S_p3 and S_p4 closed: $v_\mathrm{xM} = -V_\mathrm{cn}$

As can be seen, there are two different states to generate the 0 V potential. Depending on the respective state, the current-flow through C_Fp is either of positive (State 2) or negative (State 3) value. This redundant switching state allows balancing of the additional capacitor stage C_Fp.

T-Type:

- State 1: $S_\mathrm{p+}$ closed: $v_\mathrm{xM} = V_\mathrm{cp}$
- State 2: S_p0 closed: $v_\mathrm{xM} = 0\,\mathrm{V}$
- State 3: $S_\mathrm{p-}$ closed: $v_\mathrm{xM} = -V_\mathrm{cn}$

NPC:

- State 1: S_p1 and S_p2 closed: $v_\mathrm{xM} = V_\mathrm{cp}$
- State 2: S_p2 and S_p3 closed: $v_\mathrm{xM} = 0\,\mathrm{V}$
- State 3: S_p3 and S_p4 closed: $v_\mathrm{xM} = -V_\mathrm{cn}$

5.4.2 Duty Cycles

Simple mathematical analyses show that the fundamental duty cycles for the different presented topologies considered (Top. D-F) are actually equal. Therefore, the duty cycles of the cell are only derived once in this subsection.
For e.g. the three-level NPC branch connected to L_cp, the required duty cycle δ_p

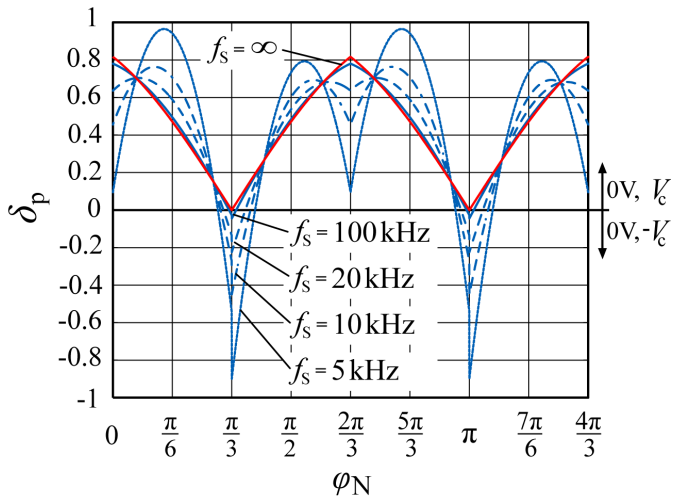


Fig. 5.39: Duty cycle waveforms of the three-level injection cell, for different switching frequencies f_s and dedicated injection inductance (for a maximum current ripple of 20 %).

calculates to

$$\delta_p = \frac{v_{pos} - v_{h3} + v_{Lcp}}{V_c} \,. \tag{5.111}$$

V_c denotes the DC-link voltage ($V_{cp} = V_{cn} = V_c$). Obviously, the duty cycles of the different three-level bridges (Top. D-F of **Fig. 5.1**) equal the duty cycle of Top. B analyzed in section 5.2 . The difference between Top. D-F and Top. B is however defined by the allowable output voltage range and depicted in **Fig. 5.39**. Different from the half-bridge implementation (Top. B), the three-level stages are able to facilitate negative duty cycle values, up to -1. Each individual switch however still can be controlled by a relative turn-on interval $0 \ldots 1$ (1 means appropriate switch closed and 0 implies that the dedicated switch is open). Therefore, the appropriate negative duty cycle cannot be applied directly to the three-level bridge semiconductors. The duty cycle has to be separated into different components which can finally be used for proper control of the active components. One example for such a proper derivation is given in **Fig. 5.40**. In general, the NPC converter is controlled in such way, that for positive voltage operation the upper switch (S_{p1}) is modulated (lower switch S_{p4} permanently opened) and for negative voltage regulation the lower switch (S_{p4}) is going to be adjusted (upper switch S_{p1} permanently opened). Therefore, the duty cycle of δ_{p1} equals δ_p as long as $\delta_p > 0$ applies and $\delta_{p4} = 0$. For $\delta_p < 0$, $\delta_{p4} = \delta_p$ and $\delta_{p1} = 0$. In order to avoid a DC-link capacitor short circuit case, S_{p3} has to be opened each time S_{p1} is closed and vice versa. Equal assumptions are valid for S_{p2} and S_{p4}. Therefore, for the **NPC** converter stage (connected to L_{cp}), the following duty cycles apply for $\delta_p > 0$:

$$\delta_{p1} = \delta_p \tag{5.112}$$

$$\delta_{p4} = 0 \tag{5.113}$$

$$\delta_{p2} = \mathrm{NOT}\,(\delta_{p4}) = 1 - \delta_{p4} = 1 \tag{5.114}$$

$$\delta_{p3} = \mathrm{NOT}\,(\delta_{p1}) = 1 - \delta_{p1} = 1 - \delta_p \,. \tag{5.115}$$

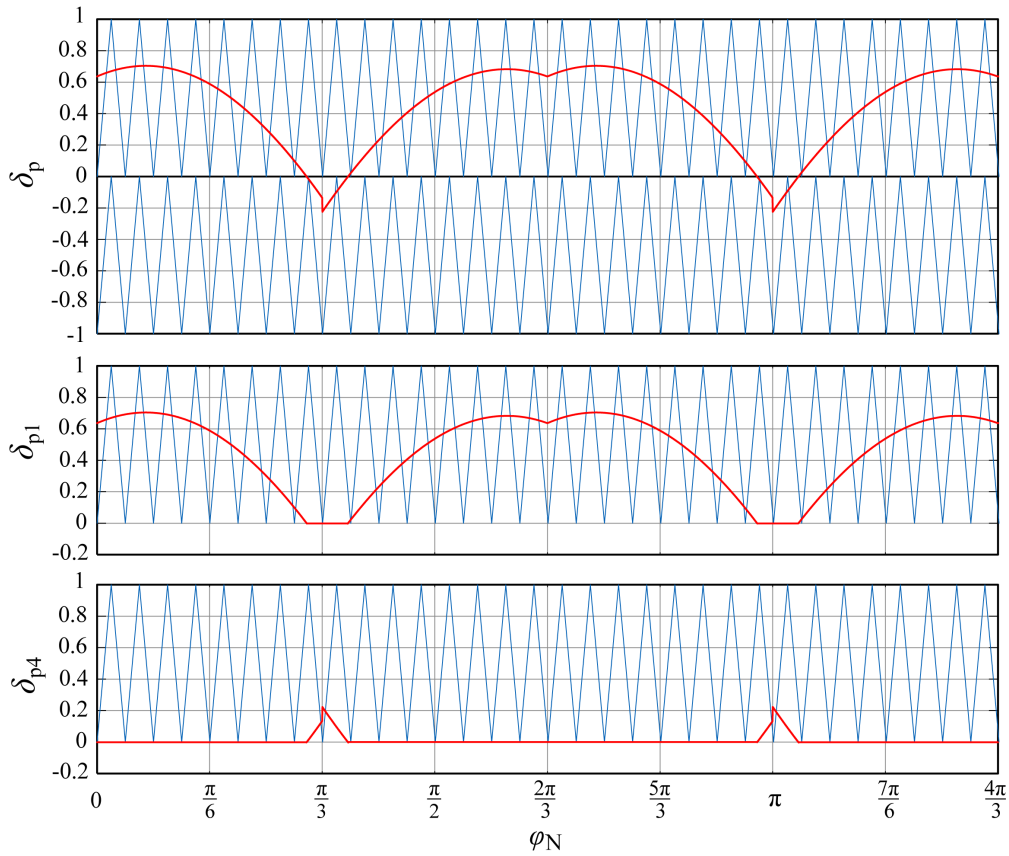


Fig. 5.40: Examplarily illustrated showcase for proper control of appropriate switches for a e.g. NPC three-level converter stage.

Considering $\delta_p < 0$,

$$\delta_{p1} = 0 \tag{5.116}$$

$$\delta_{p4} = |\delta_p| = -\delta_p \tag{5.117}$$

$$\delta_{p2} = \text{NOT}\left(\delta_{p4}\right) = 1 - \delta_{p4} = 1 - |\delta_p| = 1 + \delta_p \tag{5.118}$$

$$\delta_{p3} = \text{NOT}\left(\delta_{p1}\right) = 1 - \delta_{p1} = 1 \tag{5.119}$$

applies. δ_{p1-4} denote duty cycles of appropriate switches S_{p1-4}, respectively. Different feasible switching states for such a NPC switching cell (connected to the injection inductance L_{cp}) are depicted in **Fig. 5.41**. From this illustration several commutation paths can be addressed:

- $\delta_p > 0$, $i_{cp} > 0$: $S_{p1} \Leftrightarrow D_{pF1}$
- $\delta_p > 0$, $i_{cp} < 0$: $D_{p1} \Leftrightarrow S_{p3}$, D_{pF2}
- $\delta_p < 0$, $i_{cp} > 0$: $D_{p4} \Leftrightarrow S_{p2}$, D_{pF1}
- $\delta_p < 0$, $i_{cp} < 0$: $S_{p4} \Leftrightarrow D_{pF2}$

Furthermore, **Fig. 5.42** depicts several occurring sections which are mainly defined due to appropriate injection current i_{cp} and duty cycles δ_{p1-4}. For each section the operated and hence dedicated stressed semiconductors are indicated. Obviously, the negative switch S_{p4} is never going to be used. Only its additional/external

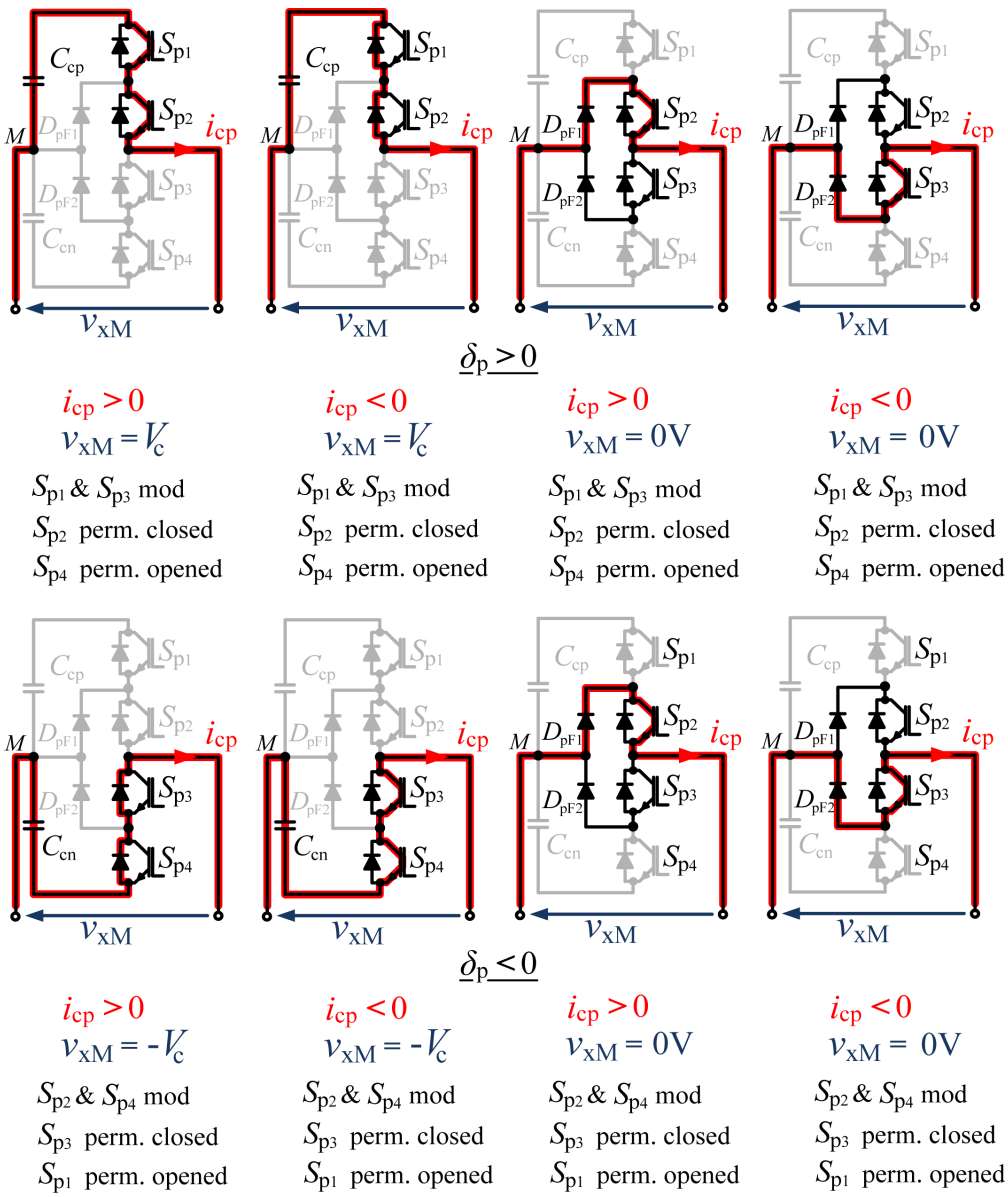


Fig. 5.41: Different feasible switching states of e.g. a NPC three-level bridge converter stage.

diode D_{p4} is required. In addition, switches which are necessary to generate the averaged negative voltage potential of v_{xM} are barely used for higher switching frequencies if the affecting inductor value L_{cp} decreases. For an ideal consideration ($L_{cp} = 0$), S_{p3}, S_{p4}, D_{p3} and D_{p4} are completely ineffective. Thus, it has to be deliberated carefully in advance whether a current shaping network implemented as three-level converter is the most efficient and effective solution for the predefined given specifications (output power, input mains frequency, maximum allowable switching frequency, power density, total converter volume, etc.). This particularly is true if semiconductor modules are used for the implementation of the three-phase branch because such devices usually are designed "symmetrically" concerning the chip size of the upper and lower transistors and diodes.
Similar derivations as the already presented ones for the NPC branch can be

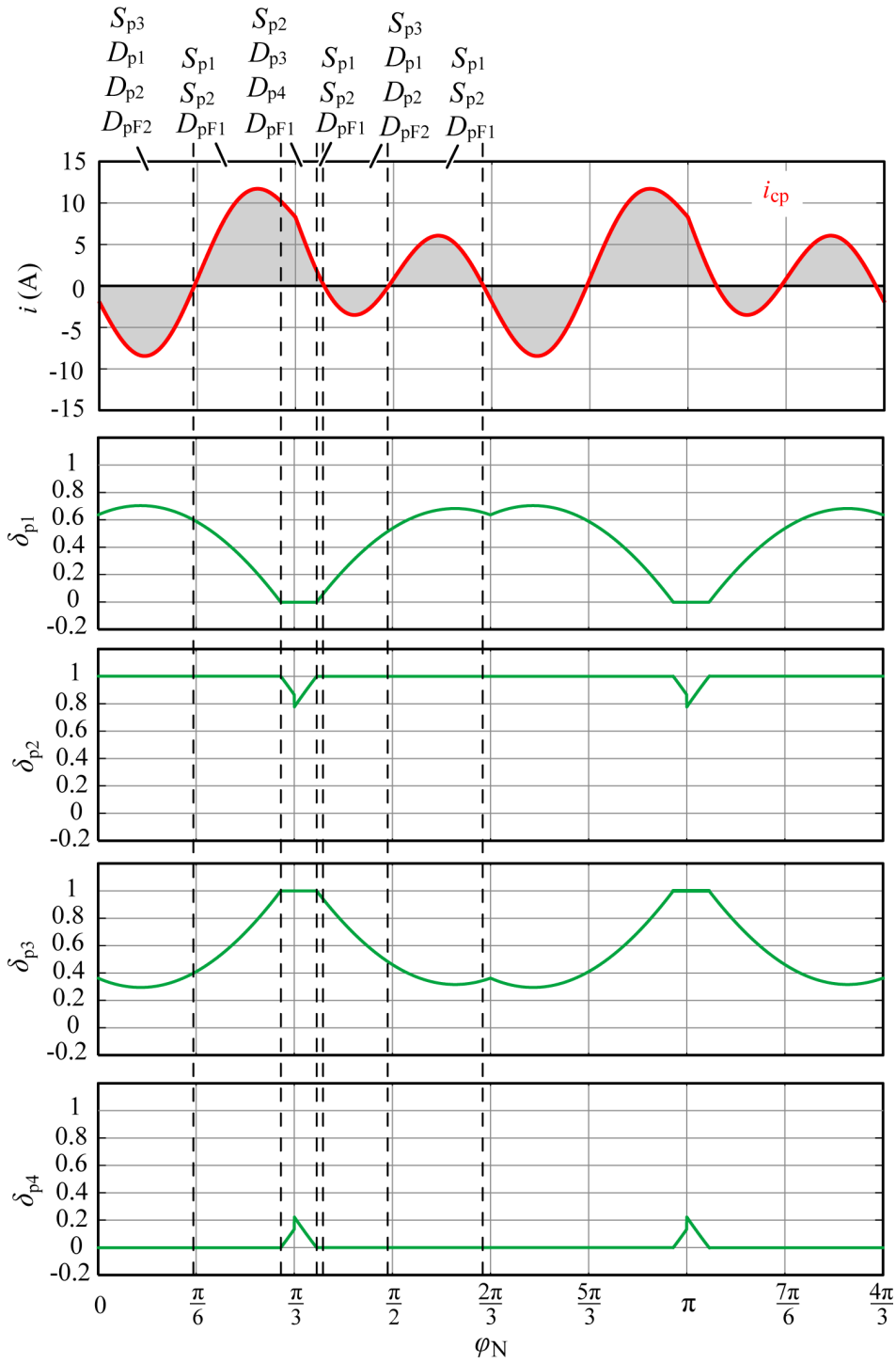


Fig. 5.42: NPC switching sequence and appropriate stressed semiconductors for one $2\pi/3$ period of i_{cp} and δ_p.

performed for the T-type and Flying capacitor stages. Appropriate duty cycles are therefore mentioned for completeness. The duty cycles of the **T-type** topology for $\delta_p > 0$ are defined by

$$\delta_{p+} = \delta_p \tag{5.120}$$

$$\delta_{p0+} = \text{NOT}\left(\delta_{p-}\right) = 1 - \delta_{p-} = 1 \tag{5.121}$$

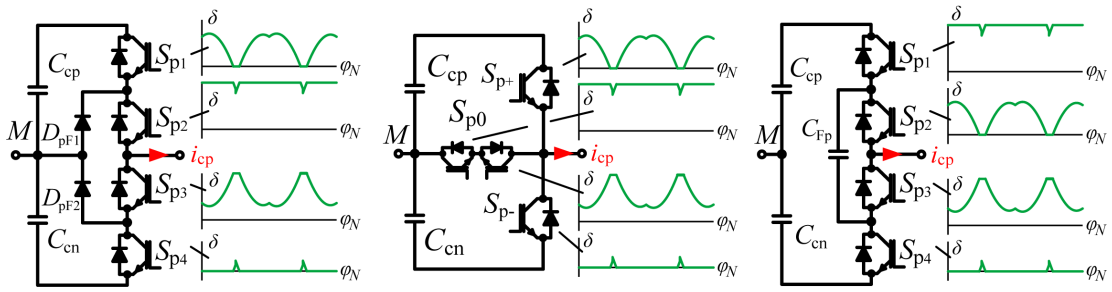


Fig. 5.43: Required duty cycles for NPC, T-type and flying capacitor converter stage (connected to injection choke L_{cp}) for sinusoidal input current control.

$$\delta_{p0-} = \text{NOT}\left(\delta_{p+}\right) = 1 - \delta_{p+} = 1 - \delta_p \tag{5.122}$$
$$\delta_{p-} = 0 \tag{5.123}$$

whereas δ_{p0+} is the duty cycle of the bidirectional switch connected to the midpoint M and δ_{p0-} the semiconductor S_{p0-} which is connected to L_{cp}. Considering $\delta_p < 0$

$$\delta_{p+} = 0 \tag{5.124}$$
$$\delta_{p0+} = \text{NOT}\left(\delta_{p-}\right) = 1 - \delta_{p-} = 1 - |\delta_p| = 1 + \delta_p \tag{5.125}$$
$$\delta_{p0-} = \text{NOT}\left(\delta_{p+}\right) = 1 - \delta_{p+} = 1 \tag{5.126}$$
$$\delta_{p-} = |\delta_p| = -\delta_p \tag{5.127}$$

is valid.
The control of the **flying capcitor** stage is slightly different than that of the NPC or the T-type topology. As the inner switches S_{p2} and S_{p3} are directly connected to the additional capacitor C_{Fp} they cannot be closed at the same time. Therefore, the outer switch states remain constant while the inner switch states are going to be modulated. The duty cycles of the topology hence result in

$$\delta_{p1} = \text{NOT}\left(\delta_{p4}\right) = 1 - \delta_{p4} = 1 \tag{5.128}$$
$$\delta_{p2} = \delta_p \tag{5.129}$$
$$\delta_{p3} = \text{NOT}\left(\delta_{p2}\right) = 1 - \delta_{p2} = 1 - \delta_p \tag{5.130}$$
$$\delta_{p4} = 0 \tag{5.131}$$

for $\delta_p > 0$. Considering $\delta_p < 0$

$$\delta_{p1} = \text{NOT}\left(\delta_{p4}\right) = 1 - \delta_{p4} = 1 - |\delta_p| = 1 + \delta_p \tag{5.132}$$
$$\delta_{p2} = 0 \tag{5.133}$$
$$\delta_{p3} = \text{NOT}\left(\delta_{p2}\right) = 1 - \delta_{p2} = 1 \tag{5.134}$$
$$\delta_{p4} = |\delta_p| = -\delta_p \tag{5.135}$$

applies.
A summary of the required duty cycles for the dedicated current shaping three-level topologies in order to generate appropriate sinusoidal input currents is finally depicted in **Fig. 5.43**.

5.4.3 Injection Inductor Design

For proper injection inductor implementation, five different solutions are found.

- **(i)**: Two inductor arrangement L_{cp} and L_{cn} ($L_{\mathrm{h3}} = 0$). PWM of positive and negative three-level bridge synchronized. Internal PWMs (for one three-level bridge) synchronized.
- **(ii)**: Two inductor arrangement L_{cp} and L_{cn} ($L_{\mathrm{h3}} = 0$). PWM of positive and negative three-level bridge synchronized. Internal PWMs (for one three-level bridge) 180° phase shifted.
- **(iii)**: Two inductor arrangement L_{cp} and L_{cn} ($L_{\mathrm{h3}} = 0$) with PWM of both three-level bridge PWMs 180° phase shifted (d_1). Internal PWMs (for one three-level bridge) synchronized.
- **(iv)**: Two inductor arrangement L_{cp} and L_{cn} ($L_{\mathrm{h3}} = 0$) with PWM of both three-level bridge PWMs 180° phase shifted. Internal PWMs (for one three-level bridge) 180° phase shifted.
- **(v)**: Three inductor arrangement L_{cp}, L_{cn}, and L_{h3}. Both PWMs synchronized.

The internal phase shift (**ii** and **iv**) of the PWMs (e.g. d_{p1} and d_{p4} for the NPC bridge leg) does not result in any performance improvement of the total rectifier. Therefore, internal PWM phase shifts are not further discussed.
As mentioned, the duty cycle for each three-level bridge leg equals the duty cycle for a CSN implementation utilizing two half-bridge branches (Top. B),

$$\delta_{\mathrm{p}} = \delta_{\mathrm{cp}} = \frac{v_{\mathrm{pos}} - v_{\mathrm{h3}} + v_{L_{\mathrm{cp}}}}{V_{\mathrm{c}}} \,. \tag{5.136}$$

As also the high frequency common mode voltage v_{MN} (for a three inductor arrangement) resembles v_{MN} for a half-bridge implementation also the injection inductor design equations are equal. The design equations for the finally considered solutions **(i)**, **(iii)** and **(v)** hence result in

$$L_{\mathrm{c}\frac{\mathrm{p}}{\mathrm{n}}} = \frac{\hat{V}_{\mathrm{N}}\left(\sqrt{3} - M\right)}{f_{\mathrm{s}}\Delta i_{\mathrm{N,max}}} \tag{5.137}$$

$$L_{\mathrm{c}\frac{\mathrm{p}}{\mathrm{n}}} = \frac{1}{2}\frac{\hat{V}_{\mathrm{N}}\left(\sqrt{3} - M\right)}{f_{\mathrm{s}}\Delta i_{\mathrm{N,max}}} \tag{5.138}$$

$$L_{\mathrm{c}\frac{\mathrm{p}}{\mathrm{n}},\mathrm{h3}} = \frac{V_{\mathrm{c}} M}{3\sqrt{3} f_{\mathrm{s}}\Delta i_{\mathrm{N,max}}} \,. \tag{5.139}$$

5.4.4 Semiconductor Stress

Current stress of switches and diodes has to be calculated for the design of each three-level branch. Depending on the given current waveforms for i_{cp} in the interval

$\varphi_{\mathrm{N}} = [\pi/3 \ldots \pi]$

$$i_{\mathrm{cp}}\left(\varphi_{\mathrm{N}}\right) = i_{\mathrm{L}}\left(\varphi_{\mathrm{N}}\right) - \hat{I}_{\mathrm{N}}\cos\left(\varphi_{\mathrm{N}} - \frac{2\pi}{3}\right) \tag{5.140}$$

the zero-crossings of $i_{\mathrm{cp}}\left(\varphi_{\mathrm{N}}\right)$ have to be calculated numerically because the calculation of the rms and avg current ratings cannot be performed in an analytically closed manner. Furthermore, also the given waveform of $i_{\mathrm{L}}(\varphi_{\mathrm{N}})$ is an approximation based on the fundamental ripple component. The converter output voltage V_{o}, the two DC-Link voltages $V_{\mathrm{cp}} = V_{\mathrm{cn}}$ and the switching frequency f_{s} are supposed to remain constant for calculating the current stress of the applied semiconductors and passive components. The required system parameters are given in **TABLE 5.3**.

For a proper derivation of rms and averaged values, **Fig. 5.42** appears to be helpful to find the proper fractions where the appropriate switches are operated and stressed. For e.g. S_{p1} of a NPC three-level bridge this would result in

$$\begin{aligned} I_{\mathrm{Sp1,avg}} = \frac{3}{2\pi}\Bigg(& \int_{-\frac{\pi}{3}}^{\mathrm{zc1}} d_{\mathrm{p1}}\left(\varphi_{\mathrm{N}}\right)\ i_{\mathrm{cp}}\left(\varphi_{\mathrm{N}}\right)\ \mathrm{d}\varphi_{\mathrm{N}} + \ldots \\ & \ldots + \int_{\mathrm{zc2}}^{\mathrm{zc3}} d_{\mathrm{p1}}\left(\varphi_{\mathrm{N}}\right)\ i_{\mathrm{cp}}\left(\varphi_{\mathrm{N}}\right)\ \mathrm{d}\varphi_{\mathrm{N}} + \ldots \\ & \ldots + \int_{\mathrm{zc4}}^{\frac{\pi}{3}} d_{\mathrm{p1}}\left(\varphi_{\mathrm{N}}\right)\ i_{\mathrm{cp}}\left(\varphi_{\mathrm{N}}\right)\ \mathrm{d}\varphi_{\mathrm{N}}\Bigg) \end{aligned} \tag{5.141}$$

and

$$\begin{aligned} I^2_{\mathrm{Sp1,rms}} = \frac{3}{2\pi}\Bigg(& \int_{-\frac{\pi}{3}}^{\mathrm{zc1}} d_{\mathrm{p1}}\left(\varphi_{\mathrm{N}}\right)\ i^2_{\mathrm{cp}}\left(\varphi_{\mathrm{N}}\right)\ \mathrm{d}\varphi_{\mathrm{N}} + \ldots \\ & \ldots + \int_{\mathrm{zc2}}^{\mathrm{zc3}} d_{\mathrm{p1}}\left(\varphi_{\mathrm{N}}\right)\ i^2_{\mathrm{cp}}\left(\varphi_{\mathrm{N}}\right)\ \mathrm{d}\varphi_{\mathrm{N}} + \ldots \\ & \ldots + \int_{\mathrm{zc4}}^{\frac{\pi}{3}} d_{\mathrm{p1}}\left(\varphi_{\mathrm{N}}\right)\ i^2_{\mathrm{cp}}\left(\varphi_{\mathrm{N}}\right)\ \mathrm{d}\varphi_{\mathrm{N}}\Bigg)\ . \end{aligned} \tag{5.142}$$

zc1-4 denote appropriate numerically calculated zero crossings of i_{cp}. As can be seen from **Fig. 5.44** each three-level bridge leg mainly operates as a two-level system. The three-level operation, however, is required for smooth current control at each 60° sector transition. It is evident that the current ratings of the NPC leg components are not "symmetrically" stressed (i.e., equal for upper and lower part, as valid for e.g. drive inverters) which might be seen as a drawback of the proposed concept. It is obvious from the given listing in **Fig. 5.44** that the three-level bridge connected to the negative bus and the switching branch connected to the positive bus bar are stressed cross-symmetrically. I.e., current stress of S_{n1} equals S_{p4}, whereas S_{n2} conforms S_{p3}, respectively. Depending on the calculated current and voltage stress, appropriate IGBTs and diodes for the system can now be chosen. It has to be mentioned that standard three-level IGBT modules may be a cost-effective solution as they are widely used in industry. The expected semiconductor efficiency of the total rectifier (e.g. NPC implementation) has been predicted to 98.9 % (losses 104 W for a 10 kW rectifier) when passive components are not

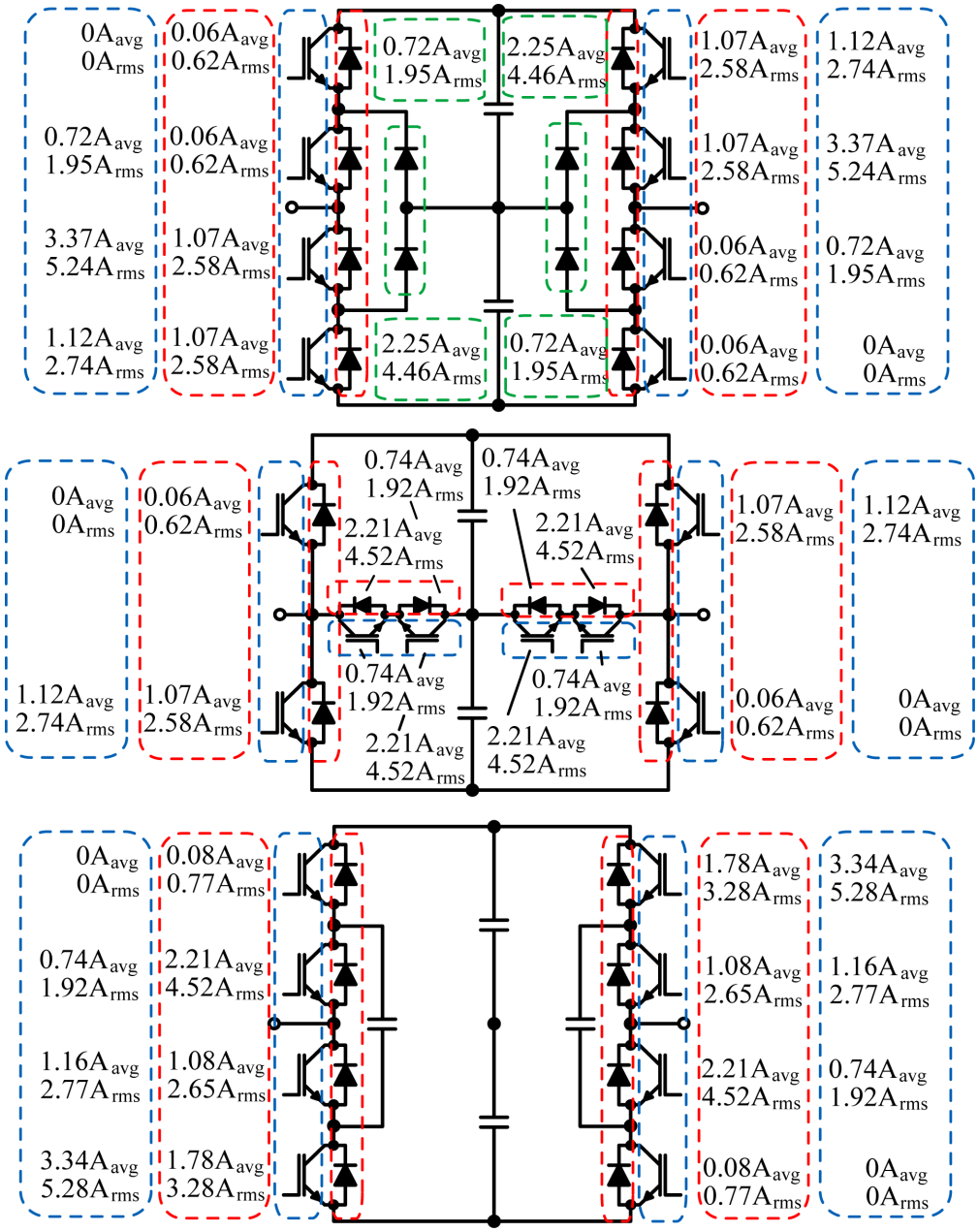


Fig. 5.44: Numerically calculated current stress values for three-level bridge legs NPC, T-type and flying capacitor. Assumed characteristics are as follows: $V_{\mathrm{LL}} = 400\,\mathrm{V_{rms}}$, $f_{\mathrm{N}} = 50\,\mathrm{Hz}$, $f_{\mathrm{s}} = 10\,\mathrm{kHz}$, $L_{\mathrm{c}\frac{\mathrm{p}}{\mathrm{n}}} = 6.3\,\mathrm{mH}$, $L_{\mathrm{h3}} = 0$, $L_{\mathrm{DC}} = 2.25\,\mathrm{mH}$, $V_{\mathrm{cp}} = V_{\mathrm{cn}} = 600\,\mathrm{V}$, $V_{\mathrm{o}} = 3\sqrt{3}\hat{V}_{\mathrm{N}}/\pi$ and $P_{\mathrm{o}} = 10\,\mathrm{kW}$.

taken into account. The bidirectional switches are implemented as two back-to-back connected reverse conducting IGBTs (or standard IGBTs with anti-parallel diode). If reverse blocking IGBTs would be used the semiconductor efficiency could be enhanced to 99 %. The losses of the B6 bridge result in approximately 41 W and therefore highly affect the total semiconductor efficiency.

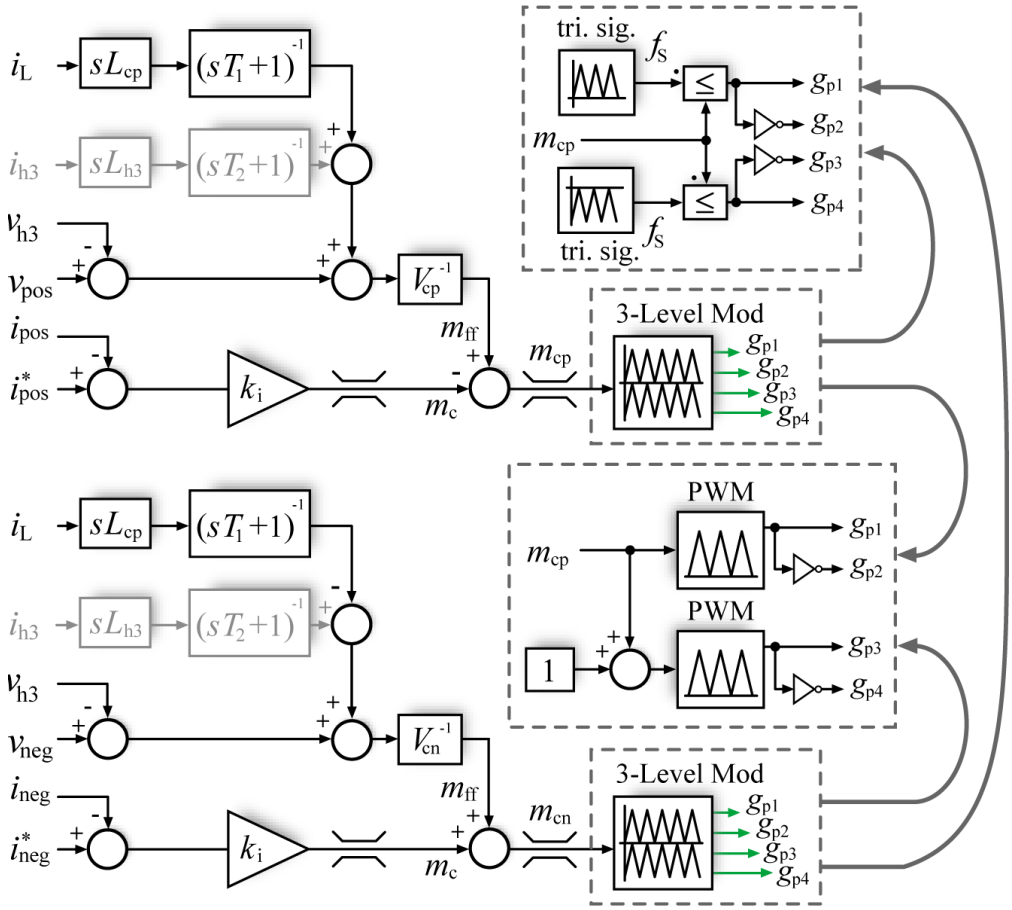


Fig. 5.45: Current control of three-level bridge current shaping network.

5.4.5 System Control

The control of the three-level bridge is actually very similar to the already discussed control of the half-bridge stage implementation. Therefore, this section only briefly highlights and illustrates the typical standard implementation and regulation of the CSN switches S_{p1-4} and S_{n1-4}.

The developed control concept is depicted in **Fig. 5.45**. It can be seen that the derived system equations result in an equal system description as for a simple series connected half-bridge arrangement (Top. B). The only difference is the required modulator (dashed) as a standard half-bridge modulator (which only has one output) to drive two different semiconductors (inverted and non-inverted), is not feeding a "four switch" multilevel stage.

Therefore, a specific three-level PWM modulator is required. The standard implementation (as shown in **Fig. 5.45**) would provide two synchronized triangular signals. The modulation signal (m_{cp} or m_{cn}) is compared with both triangular shaped signals. For e.g. $m_{cp} > 0$ only those switches which are able to apply voltages ≥ 0 are modulated. Typically, digital signal processors already come with one or more integrated PWM modulation units. These components however, generally expect modulation signals ≥ 0 as the internal generated triangular signals

TABLE 5.3: Design Specifications for simulating a third harmonic injection rectifier realized by two three-level converter stages.

Mains voltage:	$V_{\mathrm{LL}} = 400\,\mathrm{V_{rms}}$
Mains frequency:	$f_{\mathrm{N}} = 50\,\mathrm{Hz}$
Switching frequency:	$f_{\mathrm{s}} = 10\,\mathrm{kHz}$.
Injection inductor:	$L_{\mathrm{c}\frac{\mathrm{p}}{\mathrm{n}}} = 5.6\,\mathrm{mH}$, $L_{\mathrm{h3}} = 0$
DC-side choke:	$L_{\mathrm{DC}} = 2.25\,\mathrm{mH}$
Cells DC-link voltage:	$V_{\mathrm{cp}} = V_{\mathrm{cn}} = 600\,\mathrm{V}$
System output voltage:	$V_{\mathrm{o}} = 540\,\mathrm{V}$
Output power:	$P_{\mathrm{o}} = 10\,\mathrm{kW}$

are only of positive values (in order to e.g. reduce the computational expense). As e.g. proposed in [141] the same PWM module can be used for either positive and negative values of m_{cp}, if m_{cp} is up-shifted by "1", for negative values of m_{cp}.

5.4.6 Simulation Results

Operation of the total rectifier system yields very similar results for a CSN implementation based NPC, T-type or Flying capacitor topology. Proper input current generation has been verified by simulation of a 10 kW system according to the parameters given in **TABLE 5.3** using the PLECS simulation software. AC-side filter capacitors $C_{\mathrm{F}} = 6.8\,\mu\mathrm{F}$ (assembled in star-configuration) and an output capacitor of $C_{\mathrm{o}} = 1000\,\mu\mathrm{F}$ is used (to achieve a low output voltage ripple of $\Delta V_{\mathrm{o,pp}} \approx 8\,\mathrm{V}$). **Fig. 5.46** illustrates the simulated results of the diode bridge output currents i_{pos}, i_{neg} and the injection current i_{h3} which are "combined" at the AC-side to achieve the required sinusoidal input currents i_{N1}, i_{N2}, i_{N3}. The input filter C_{F} also has to smooth current distortions originating from the commutation of the bidirectional switches $S_1 \ldots S_3$ every 60° interval transition (due to not perfect commutation of B6 and CID). Furthermore, **Fig. 5.46** demonstrates the good transient behavior of the system, shown for a 10 kW to 2.5 kW output power load step.

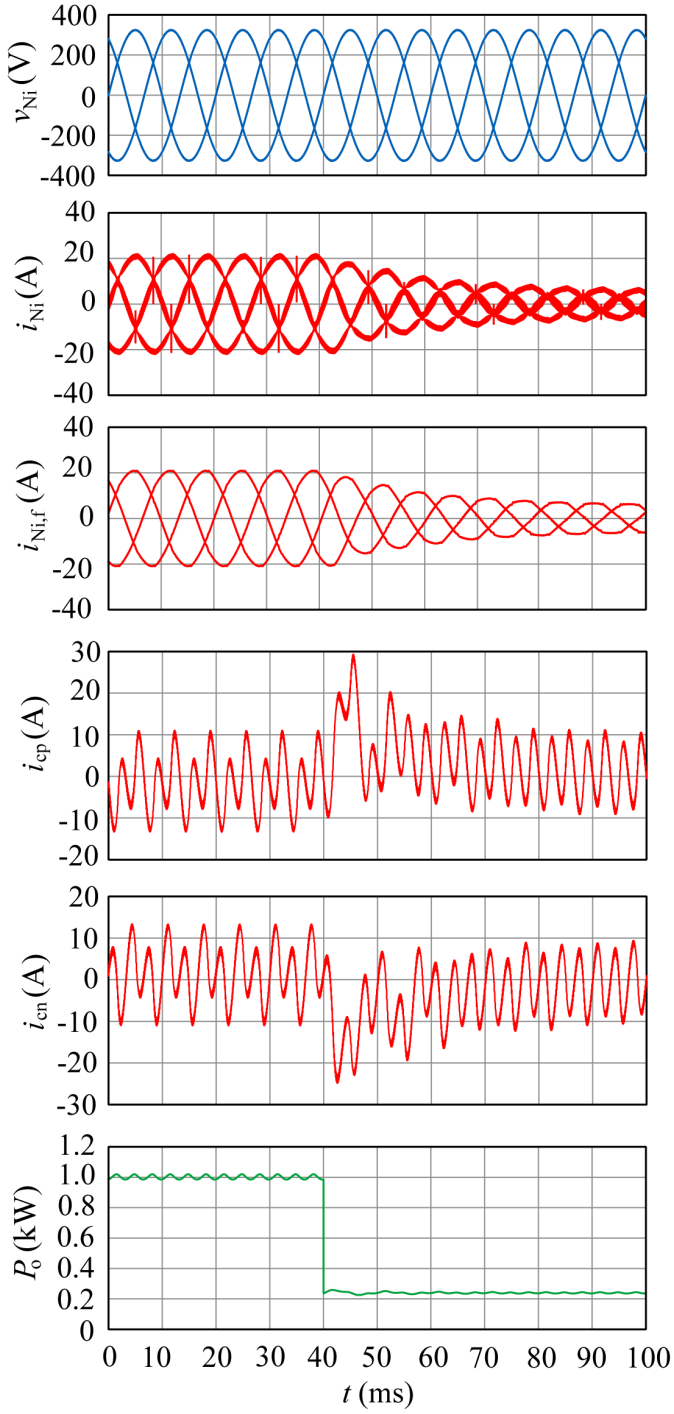


Fig. 5.46: Simulation results of a NPC current shaping cell for a 10 kW to 2.5 kW load step.

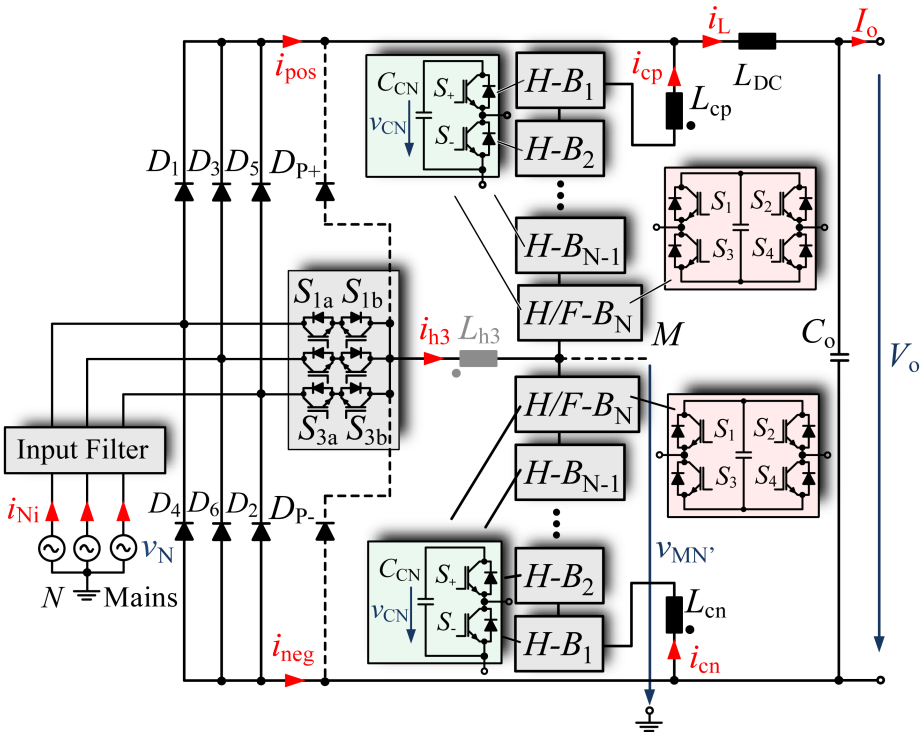


Fig. 5.47: Third harmonic injection rectifier using a multi cell converter string in interleaved PWM mode.

5.5 CSN Implementation - Multi Cell Topology

In this section, a current shaping network implemented as a series connected string of multiple (N) half- and/or full-bridges (as depicted in **Fig. 5.47**) is discussed. In order to reduce the number of component count (MOSFETs, IGBTs or GaN), it is recommended to merely apply not more than one full-bridge converter (as N^{th} switching cell). At least one full-bridge stage is, however, required in order to achieve a slightly negative voltage level in order to minimize the current distortion at the sector transitions.
Feasible cell combinations are as follows:

- 2 half-bridges
- 2 full-bridges
- N half-bridges
- N full-bridges
- $N-1$ half-bridges, 1 full-bridge.

The multi cell (MC) topology is widely known and used in industry and discussed in literature (as e.g. in [142–145]) if converters for e.g. high DC-link voltage levels and/or reduced filter size are required. The main advantage of this topology is

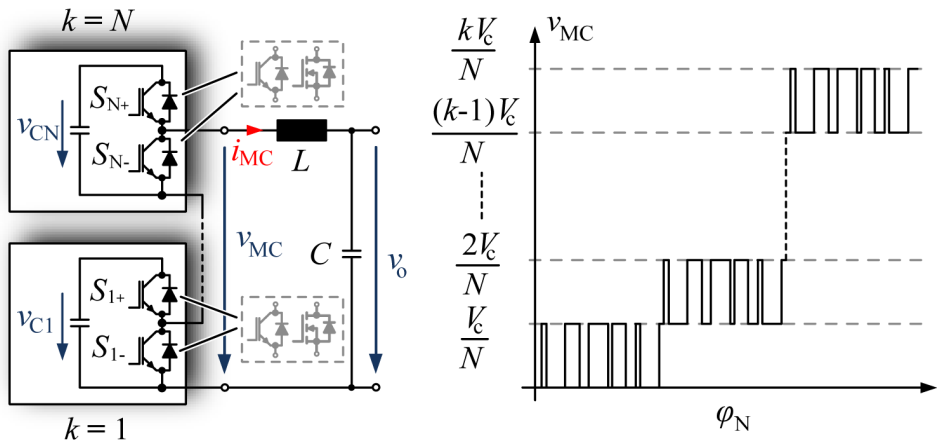


Fig. 5.48: Simplified structure of a multi cell converter (applying either IGBTs or MOSFETs) and appropriate generation of output voltage levels.

that an interleaved PWM results in a multiplication of the fundamentally (cell) switching frequency.
The DC-link voltage for each cell depends on the number of required cells N and therefore results in

$$V_{\mathrm{c,k}} = \frac{V_{\mathrm{c}}}{N} \tag{5.143}$$

with $k = 1, 2, 3, \ldots, N$. If operated in interleaved PWM mode, the generated triangular signals have to be phase shifted by

$$\varphi_{\mathrm{N}} = k\frac{2\pi}{N} \ . \tag{5.144}$$

If e.g. 4 switching cells are used ($N = 4$) and a maximum DC-link voltage of $V_{\mathrm{c}} = 600\,\mathrm{V}$ is required, the voltage level of each capacitor stage results in $150\,\mathrm{V}$ and its appropriate duty cycle has to be phase shifted by 90°. As can be seen, (dependent on the number of cells) ultra-low $R_{\mathrm{DS,on}}$ MOSFETs are applicable. Very low conduction losses can be achieved as the on-resistance of a classical power MOSFET follows its breakdown voltage BV_{DS} according

$$R_{\mathrm{DS,on}} \propto BV_{\mathrm{DS}}^{2.6} \ . \tag{5.145}$$

In **Fig. 5.48** different occuring voltage levels are depicted for a multi cell implemented as series connected half-bridges. Obviously, the different voltage levels for such a string consisting of k half-bridge branches are defined by

$$\frac{V_{\mathrm{c}}}{N}, \quad \frac{2V_{\mathrm{c}}}{N}, \quad \ldots \quad , \quad \frac{(k-1)\,V_{\mathrm{c}}}{N}, \quad \frac{kV_{\mathrm{c}}}{N} \ . \tag{5.146}$$

However, the definition of k highly depends on the implemented type of the string:

- N Full-Bridges: $k = -(N-1), \ldots, -1, 0, 1, \ldots, N$
- N Half-Bridges: $k = 0, 1, 2, 3 \ldots, N$
- $N-1$ Half-Bridges + 1 Full-Bridge: $k = -1, 0, 1, 2, 3 \ldots, N$.

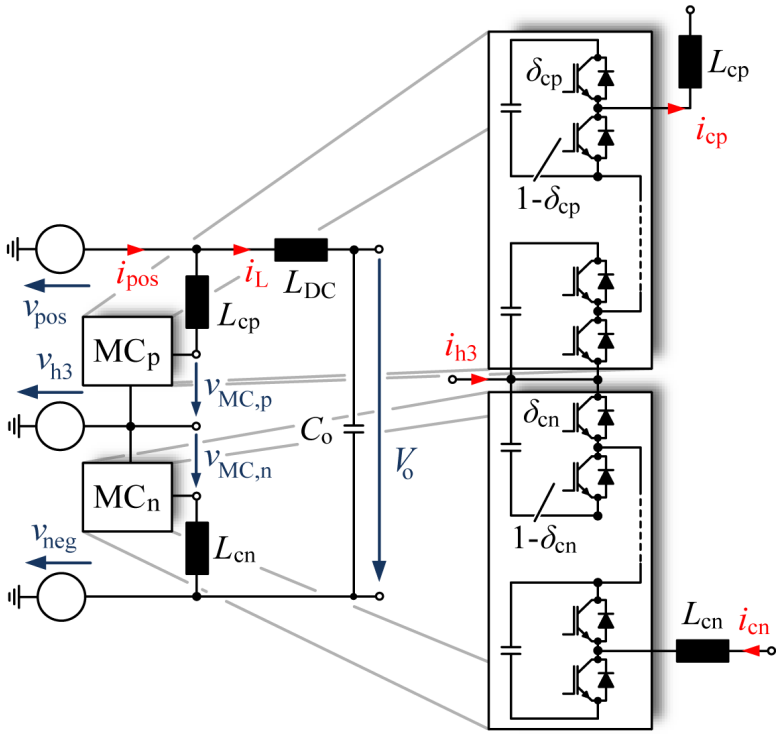


Fig. 5.49: Model of the THI rectifier applying a set of series connected half- and/or full-bridge stages.

Furthermore, appropriate current characteristics of such a stage have to be derived. The voltage across the according inductor of the multi cell is defined by

$$v_{L_{cp}} = v_{MC} - \bar{v}_o = k\frac{V_c}{N} - (v_{pos} - v_{h3}) \ , \tag{5.147}$$

$$v_{L_{cp}} = k\frac{V_c}{N} - \delta' V_c = L_{cp}\frac{\Delta i_{cp}}{\Delta t} \ . \tag{5.148}$$

$\delta' V_c$ is used to represent the averaged (or low frequency) output voltage of the multi cell. Therefore,

$$\delta' V_c = v_{pos} - v_{h3} \tag{5.149}$$

applies (cf., **Fig. 5.49**). In addition, the dedicated time intervals Δt are defined by

$$\Delta t = T_s\left(\delta' - \frac{k-1}{N}\right) \qquad \text{with} \qquad \frac{k-1}{N} \leq \delta' \leq \frac{k}{N} \ . \tag{5.150}$$

However, that the duty cycles of MC_p (multi cell connected to L_{cp}) and MC_n (multi cell connected to L_{cn}) are different. Hence it has to be distinguished between

$$\delta'_{cp} = \frac{v_{pos} - v_{h3}}{V_c} \tag{5.151}$$

and

$$\delta'_{cn} = 1 + \frac{v_{neg} - v_{h3}}{V_c} \ . \tag{5.152}$$

This set of boundary conditions is required to guarantee proper operation of the rectifier. If now **Eq. 5.148** and **Eq. 5.150** are used and transformed, one may receive

$$k\frac{V_\mathrm{c}}{N} - \delta' V_\mathrm{c} = L\frac{\Delta i}{T_\mathrm{s}\left(\delta' - \frac{k-1}{N}\right)} \tag{5.153}$$

which finally results in

$$\Delta i = \frac{k\frac{V_\mathrm{c}}{N} - \delta' V_\mathrm{c}}{L f_\mathrm{s}}\left(\delta' - \frac{k-1}{N}\right) . \tag{5.154}$$

This equation allows to determine the appropriate duty cycle values where the maximum current ripple appears.

$$\frac{\partial \Delta i}{\partial \delta'} \stackrel{!}{=} 0 = \frac{-2\delta'_\mathrm{max} V_\mathrm{c} + k\frac{V_\mathrm{c}}{N} - 0 + \frac{k-1}{N} V_\mathrm{c}}{L f_\mathrm{s}} , \tag{5.155}$$

therefore finally yields

$$\delta'_\mathrm{max} = \frac{2k-1}{2N} . \tag{5.156}$$

If a number of four cells for each switching leg ($N = 4$) is assumed, four different duty cycle instants can be found where the maximum current ripple occurs:

- $\delta'_{\mathrm{max},1} = 0.125$, $@k = 1$
- $\delta'_{\mathrm{max},2} = 0.375$, $@k = 2$
- $\delta'_{\mathrm{max},3} = 0.625$, $@k = 3$
- $\delta'_{\mathrm{max},4} = 0.875$, $@k = 4$.

In a further step, the duty cycle should be found where the minimum current ripple $\Delta i = 0$ occurs. Therefore, no derivation of the original equation is required.

$$\Delta i = \frac{k\frac{V_\mathrm{c}}{N} - \delta' V_\mathrm{c}}{L f_\mathrm{s}}\left(\delta' - \frac{k-1}{N}\right) = 0 \tag{5.157}$$

finally results in a quadratic equation

$$\delta'^2 + \delta'\left(\frac{-2k+1}{N}\right) + \frac{k^2-k}{N^2} = 0. \tag{5.158}$$

Applying

$${}_1x_2 = -\frac{p}{2} \pm \sqrt{\frac{p^2}{4} - q} \tag{5.159}$$

we obtain

$${}_1\delta'_2 = \frac{2k-1}{2N} \pm \frac{1}{2N} \tag{5.160}$$

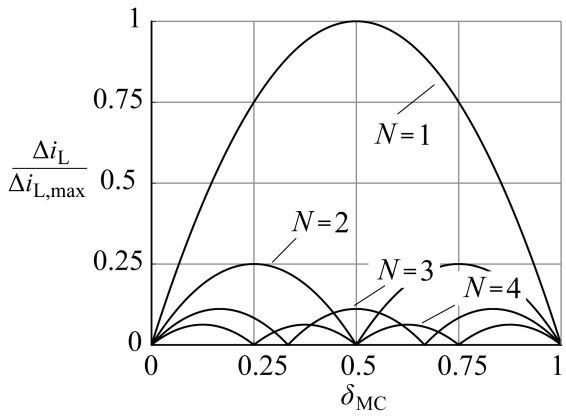


Fig. 5.50: Current ripple Δi of a multi cell current shaping THI rectifier, dependent on number of cells ($k = 1 \ldots N$) and appropriate duty cycle δ_{MC}, if only two chokes L_{cp} and L_{cn} are implemented ($L_{\mathrm{h3}} = 0$). The dedicated graph illustrates normalized current $\Delta i / \Delta i_{\mathrm{L,max}}$ for different multi cell solutions $N = 1, 2, 3$ or 4.

which finally results in

$$\delta' = \frac{k-1}{N} \,. \tag{5.161}$$

If the previously used example ($N = 4$) is referenced again, the minimum and maximum duty cycles of the multi cell is given by

- $@k = 1$, $\delta'_{\mathrm{min},1} = 0$
- $@k = 1$, $\delta'_{\mathrm{max},1} = 0.125$
- $@k = 2$, $\delta'_{\mathrm{min},2} = 0.25$
- $@k = 2$, $\delta'_{\mathrm{max},2} = 0.375$
- $@k = 3$, $\delta'_{\mathrm{min},3} = 0.5$
- $@k = 3$, $\delta'_{\mathrm{max},3} = 0.625$
- $@k = 4$, $\delta'_{\mathrm{min},4} = 0.75$
- $@k = 4$, $\delta'_{\mathrm{max},4} = 0.875$.

As minimum and maximum duty cycles have been determined, the minimum ($\Delta i = 0$) and the maximum current ripple can be calculated. The maximum current ripple, (which is a function of the instantaneous appropriate duty cycle $\Delta i_{\mathrm{max}}\,(\delta'_{\mathrm{max}})$) results in

$$\Delta i_{\mathrm{max}} = \frac{V_{\mathrm{c}}}{L f_{\mathrm{s}}} \left(\frac{k}{N} - \delta'_{\mathrm{max}} \right) \left(\delta'_{\mathrm{max}} - \frac{k-1}{N} \right) \tag{5.162}$$

$$= \frac{V_{\mathrm{c}}}{L f_{\mathrm{s}}} \left(\frac{k}{N} - \frac{2k-1}{2N} \right) \left(\frac{2k-1}{2N} - \frac{k-1}{N} \right) = \tag{5.163}$$

$$= \frac{V_{\mathrm{c}}}{4N^2 L f_{\mathrm{s}}} \,. \tag{5.164}$$

Derived minimum and maximum current ripples (for an implementation regarding two injection chokes L_{cp}, L_{cn}, $L_{\mathrm{h3}} = 0$), its dependency of the number of cells

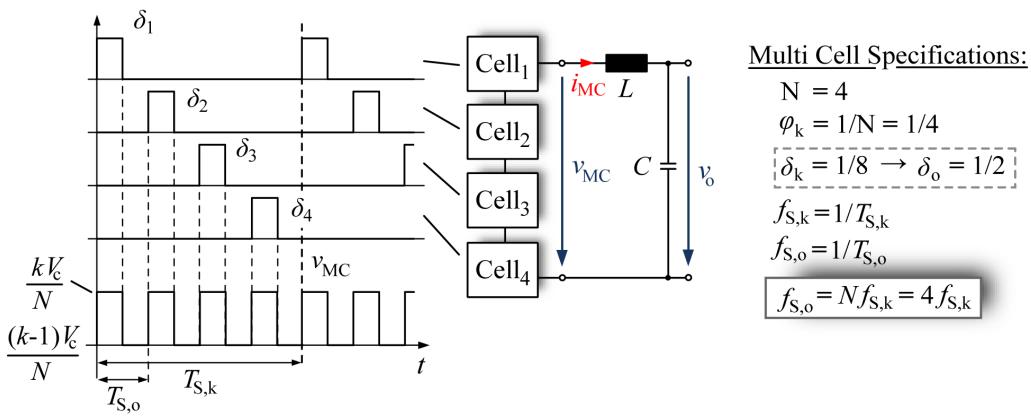


Fig. 5.51: Output voltage of the multi cell rectifier (0.5) for a duty cycle of 0.125 with a dedicated 0.25 phase shift for $N = 4$.

($N = 1, 2, 3$ or 4) and duty cycle instants are illustrated in **Fig. 5.50**.
If the current shaping network shall be realized as string of unipolar full-bridge topologies, the appropriate current ripple time interval Δt has to be adapted and leads to

$$\Delta t = \frac{T_\mathrm{s}}{2}\left(\delta' - \frac{k-1}{N}\right) . \tag{5.165}$$

Due to the now inherently doubled switching frequency, the maximum current ripple is going to be reduced by an additional factor of "2" and results in

$$\Delta i_\mathrm{FB,up,max} = \frac{V_\mathrm{c}}{8N^2 L f_\mathrm{s}} . \tag{5.166}$$

As the third harmonic current i_h3 is defined by

$$i_\mathrm{h3} = i_\mathrm{cp} - i_\mathrm{cn} , \tag{5.167}$$

maximum and minimum current ripple values (as derived in **Eq. 5.164** and **Eq. 5.166**) are not valid for i_h3. Obviously, the maximum current ripple of ΔI_h3 occurs at those time instants where either $\Delta I_\mathrm{cp} = \max$ or $\Delta I_\mathrm{cn} = \max$. As already discussed the maximum current ripple appears at

$$\delta' = \frac{2k-1}{2N} . \tag{5.168}$$

where

$$\delta'_\mathrm{cp} = \frac{v_\mathrm{pos} - v_\mathrm{h3}}{V_\mathrm{c}} \tag{5.169}$$

and

$$\delta'_\mathrm{cn} = 1 + \frac{v_\mathrm{neg} - v_\mathrm{h3}}{V_\mathrm{c}} \tag{5.170}$$

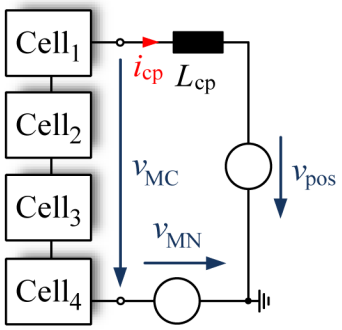


Fig. 5.52: Adapted model for a multi cell topology connected to the positive busbar of the B6 rectifier, considering a 3 coil implementation L_{cp}, L_{cn}, L_{h3}.

applies. The time instants where $\Delta I_{\mathrm{h3,max}}$ will hence appear can be derived by e.g.

$$\delta'_{\mathrm{cn,max}} = 1 + \frac{v_{\mathrm{neg}} - v_{\mathrm{h3}}}{V_{\mathrm{c}}} \stackrel{!}{=} \frac{2k-1}{2N} \tag{5.171}$$

$$= 1 + \frac{\hat{V}_{\mathrm{N}} \cos\left(\varphi_{\mathrm{max}} - \frac{2\pi}{3}\right) - \hat{V}_{\mathrm{N}} \cos\left(\varphi_{\mathrm{max}} - \frac{4\pi}{3}\right)}{V_{\mathrm{c}}} = \frac{2k-1}{2N} \tag{5.172}$$

in the sector $\varphi_{\mathrm{N}} \in [-\pi/3 \ldots 0]$. The time instant where the maximum duty cycles can be expected within the assumed sector can therefore be determined and results in

$$\varphi_{\mathrm{N,max}} = \arcsin\left(\frac{\left(\frac{2k-1}{2N} - 1\right) V_{\mathrm{c}}}{\sqrt{3}\hat{V}_{\mathrm{N}}}\right) \qquad \varphi_{\mathrm{N}} \in [-\pi/3 \ldots 0] \ . \tag{5.173}$$

For $N = 4$, $k = 3$ and the respective sector $\varphi_{\mathrm{N}} \in [-\pi/3 \ldots 0]$, the maximum current ripple appears at $\varphi_{\mathrm{N,max}} = -23.56\,^{\circ}$ with an instantaneous current ripple of i_{cn} which is defined by

$$\Delta I_{\mathrm{cn}}\left(\varphi_{\mathrm{N,max}}\right) = \frac{V_{\mathrm{c}}}{4N^2 L_{\mathrm{c}} f_{\mathrm{s}}} = \frac{V_{\mathrm{c}}}{4^3 L_{\mathrm{c}} f_{\mathrm{s}}} \ . \tag{5.174}$$

The current ripple of ΔI_{cp} at this time instant can be obtained by

$$\Delta I_{\mathrm{cp}} = \frac{V_{\mathrm{c}}}{L_{\mathrm{c}} f_{\mathrm{s}}} \left(\frac{k}{N} - \delta'_{\mathrm{cp}}\left(\varphi_{\mathrm{N,max}}\right)\right) \left(\delta'_{\mathrm{cp}}\left(\varphi_{\mathrm{N,max}}\right) - \frac{k-1}{N}\right) \tag{5.175}$$

with

$$\delta'_{\mathrm{cp}}\left(\varphi_{\mathrm{N,max}}\right) = \frac{v_{\mathrm{pos}}\left(\varphi_{\mathrm{N,max}}\right) - v_{\mathrm{h3}}\left(\varphi_{\mathrm{N,max}}\right)}{V_{\mathrm{c}}} \approx \frac{11}{20} \ . \tag{5.176}$$

As the (maximum) current ripple ΔI_{cn} and the current ripple ΔI_{cp} are both addressed at the respective time instant $\varphi_{\mathrm{N,max}} = -23.56\,^{\circ}$, the remaining maximum current ripple of i_{h3} can be identified and results in

$$\Delta I_{\mathrm{h3,max}} = |\Delta I_{\mathrm{cp}}| + |\Delta I_{\mathrm{cn,max}}| \tag{5.177}$$

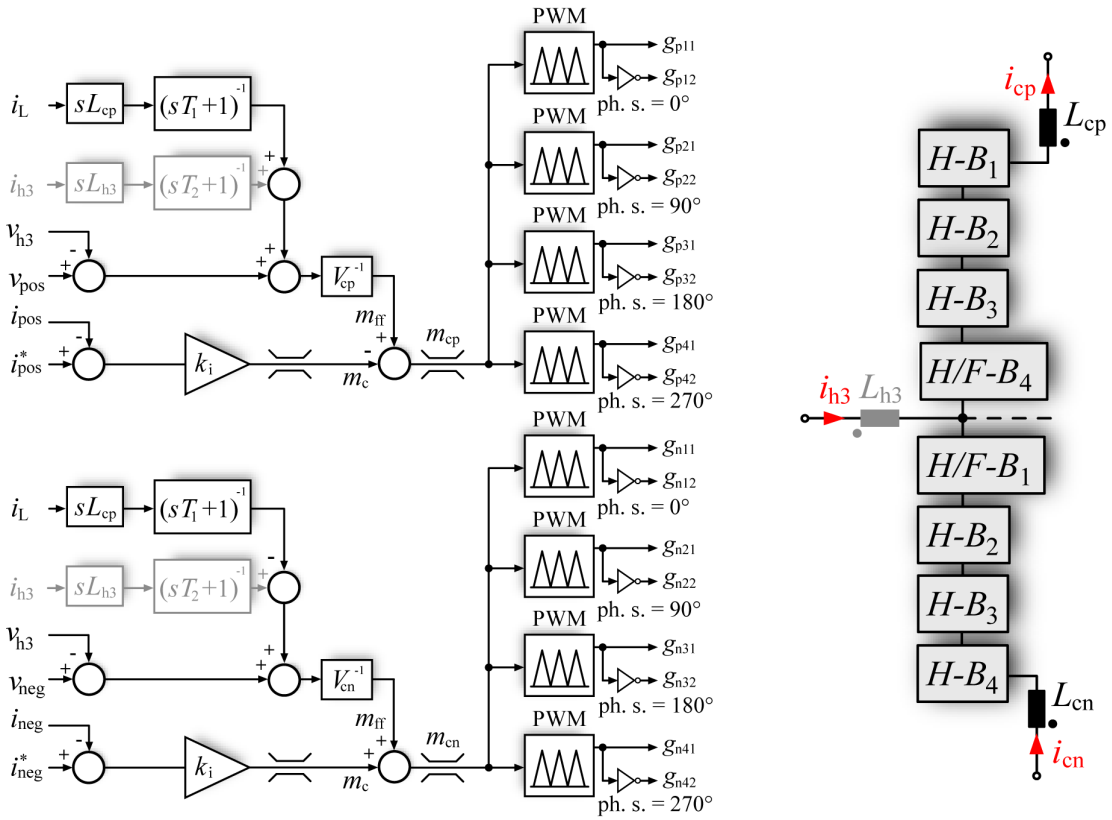


Fig. 5.53: Control concept for multi cell THI rectifier with $N = 4$ whereas one cell can optionally be implemented as full- or half-bridge stage.

$$= \frac{V_c}{L_c f_s}\left(\frac{3}{4} - \frac{11}{20}\right)\left(\frac{11}{20} - \frac{1}{2}\right) + \frac{V_c}{4^3 L_c f_s} \tag{5.178}$$

$$\approx \frac{V_c}{40 L_c f_s} \tag{5.179}$$

Obviously, the current ripple of the third harmonic current i_{h3} is increased in comparison to $\Delta I_{c\frac{p}{n}}$. Therefore, the injection inductors $L_{c\frac{p}{n}}$ should be designed with respect to ΔI_{h3}, from a point of view of the input filter.

Finally, the circuit is also investigated if a third inductor ($L_{h3} \neq 0$) is applied. As already mentioned for the standard application ($L_{h3} = 0$) the maximum current ripple appears if the output voltage of the multi cell is characterized by a 50 % duty cycle which is valid for e.g. $\delta = 0.125, 0.325, \ldots$ during interleaved PWM mode (cf., **Fig. 5.51**). This assumption is, however, no longer true if an additional common-mode voltage with switching frequency ($N \cdot f_s$) occurs (due to the implementation of L_{h3}). The adapted model is shown in **Fig. 5.52**. The maximum current ripple now appears at 40 % output voltage switching as the additional common-mode voltage is affecting the applied voltage across the inductor too. The maximum current ripple can therefore be obtained by

$$v_{L_{cp}} = k\frac{V_c}{N} - v_{pos} + v_{MN} = L\frac{\Delta i}{\Delta t} \tag{5.180}$$

$$= \frac{V_c}{4} - \frac{V_c}{3} + \frac{V_c}{6} = L\frac{\Delta i}{(1-\delta)\,T_s} \tag{5.181}$$

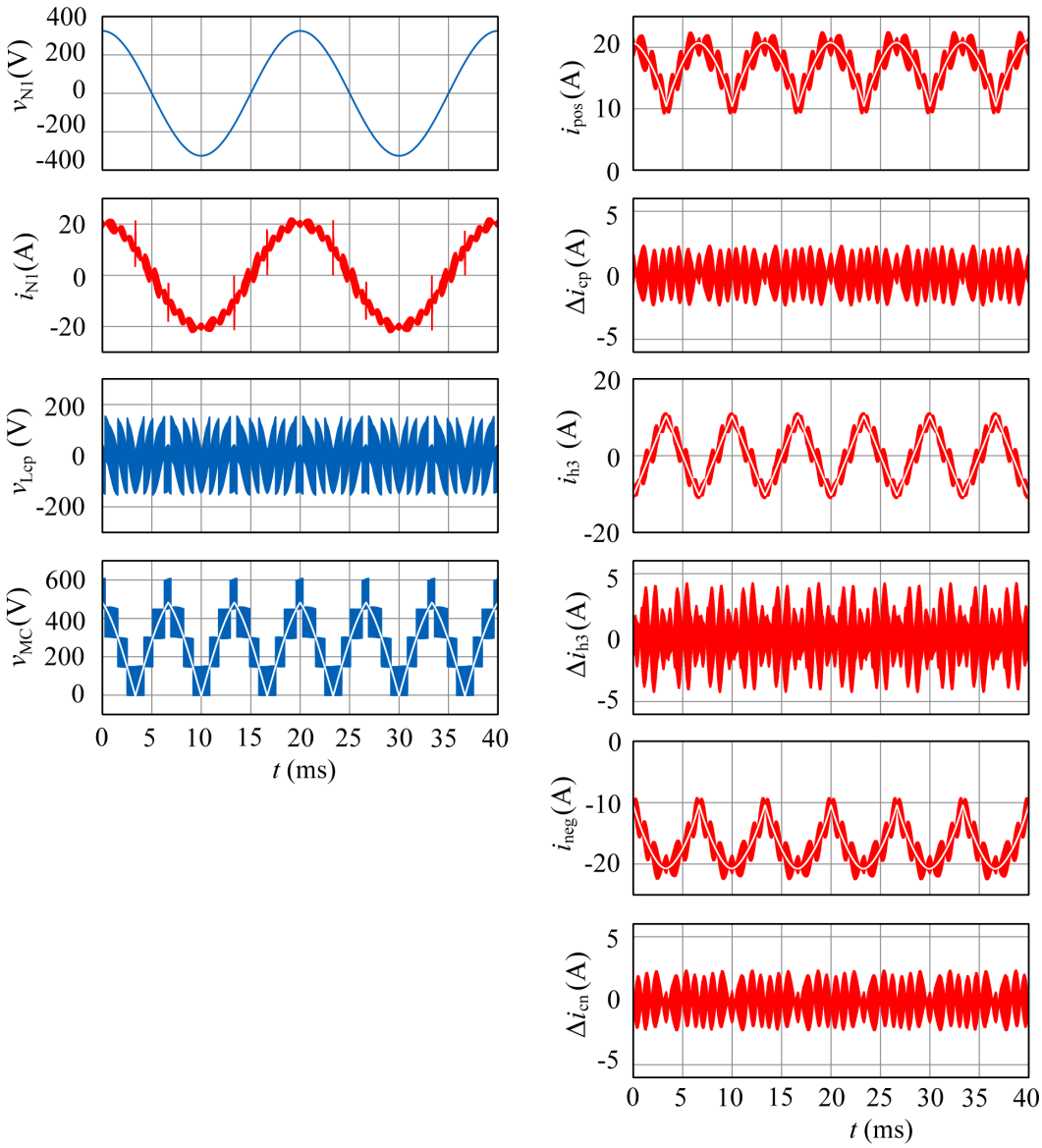


Fig. 5.54: Simulation results of multi cell THI rectifier with $N = 4$ for each injection branch ($f_s = 10\,\text{kHz}$, $f_{s,o} = 40\,\text{kHz}$, $P_o = 10\,\text{kW}$, $V_{LL} = 400\,\text{V}_{rms}$, $L_c = 200\,\mu\text{H}$, $L_c = 0$).

which finally results in

$$\Delta i = \frac{3V_c}{60 L_c f_{s,o}} = \frac{V_c}{20 L_c f_{s,o}}, \qquad \text{with} \qquad f_{s,o} = 4 f_{s,k}\,. \tag{5.182}$$

The appropriate current controller is very similar to the already discussed current control of a CSN implemented as two three-level bridge legs. Solely the implementation of the PWM modulator is different, as each triangular signal has to be phase shifted by $\frac{k}{N}360\,^\circ$ from the fundamental modulation waveform. The proposed realization is depicted in **Fig. 5.53**. Dedicated simulation results of such a rectifier (with $N = 4$ half-bridge stages) are illustrated in **Fig. 5.54**. Besides sinusoidal input currents (i_{N1}), also previously discussed maxima of respective current ripples being typically for a multi-cell converter are demonstrated.

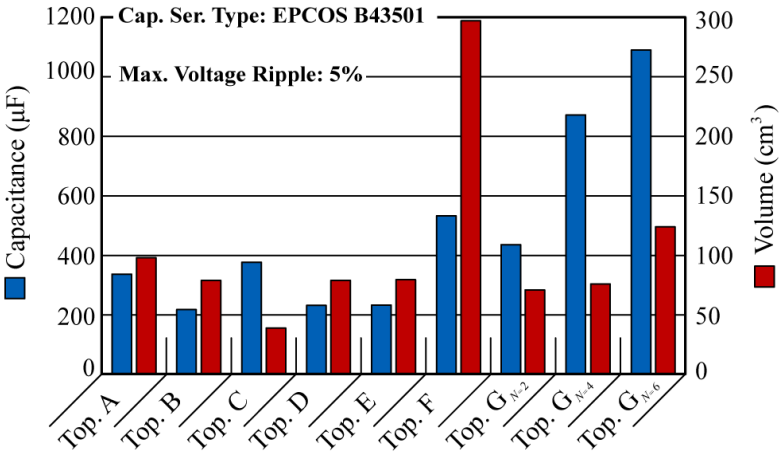


Fig. 5.55: Topology analysis for 10 kW output power of dedicated capacitor design considering EPCOS B43501 for a relative voltage ripple of 5 %.

5.6 Comparison of Topologies

5.6.1 Capacitance/ Capacitor Volume

As discussed in the previous section, the capacitor design appears to be a crucial topic. The capacitor bank volume of the injection cell undoubtedly constitutes a figure of merit for a volume optimized converter design with regard to high switching frequency considerations. Capacitor volume of each proposed topology is mainly defined by the 150 Hz and 300 Hz spectral components of the injection currents i_{cp} and i_{cn} (and therefore nominal output power P_{o}). Capacitor design considerations for THI systems thus are almost independent of the cells switching frequency f_{s} but are determined by the appearing low-frequency (150/300 Hz) DC-link ripple voltage component. Consequently, electrolytic capacitors are used at higher capacitance values due to their higher ESR and not foil capacitors which would show much higher voltage ripple as their properties (low ESR) allow lower capacitance.

Fig. 5.55 gives a line-up of required capacitor values and volumes (for one capacitor stage C_{cp} or C_{cn}) of all proposed active rectifier add-on solutions for a relative DC-link voltage ripple of 5 % and a nominal output power of 10 kW (considering EPCOS B43501 capacitor series). As previously mentioned and also stated in **Fig. 5.55**, Topology F (Flying Capacitor three-level assembly) by far results in highest volume, due to its additional capacitors required for achieving $+V_{\mathrm{c}}$, 0 V and $-V_{\mathrm{c}}$ at the output of the converter. Topologies A,B and D-F suffer from an increased volume because a maximum voltage of typically $\approx$ 450 V is given for electrolytic capacitors and hence a series connection is required at the topology-defined DC-link voltage level of 600 V. It has to be emphasized that the Flying Converter Cell active rectifier (Topology C) shows the lowest capacitor volume of all discussed topologies. Due to its 400 V DC-link voltage level a single 450 V rated voltage capacitor is sufficient (no capacitor series connection required) which min-

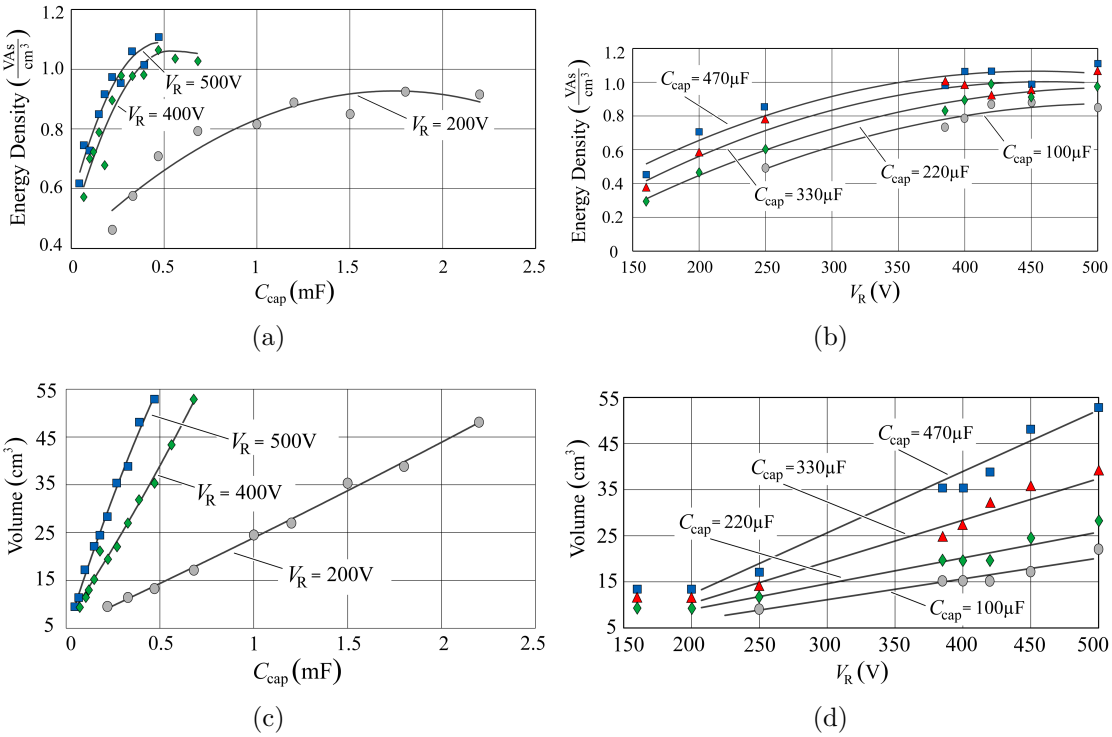


Fig. 5.56: Energy density analysis depending on rated voltage and capacitance of EPCOS B43501 electrolytic capacitor type series.

imizes the total volume of the cell. Furthermore, EPCOS' B43501 capacitor series has been evaluated regarding energy density, rated voltage and capacitance and shows that the maximum energy density can be found for capacitor types at the highest possible voltage level, i.e. 400/500 V types give much higher Ws/cm^3 than 100/200 V capacitors (cf., **Fig. 5.56(a-d)**). A multi-cell arrangement therefore tends to lack in attractiveness for an increased number of cells due to an expected growth of capacitor volume (illustrated in **Fig. 5.55**).

5.6.2 Inductance

Design of the injection inductance L_c is performed for 10 kW output power which results in inductor peak (neglecting current ripple), rms and avg current values of 12.3 A_{pk}, 6.1 A_{rms} and 1.64 A_{avg}, respectively (for L_{DC} of 2.25 mH). Results of the inductor design for a switching frequency of 10 kHz are given in **Fig. 5.57**. Two conspicuities can be observed from this bar plot. Obviously, Topology B, and Topology D-F conform in inductance design characteristics, which is mainly based on parity of their duty cycles (note that three-level bridges primarily act as two level converters if affecting 300 Hz filter output current ripple is neglected for design procedure). As illustrated in **Fig. 5.57** there are three alternative inductor design procedures which are valid for Topology A,B, and D-G:

- A standard two choke implementation which assumes all PWM signals being synchronized (grey).

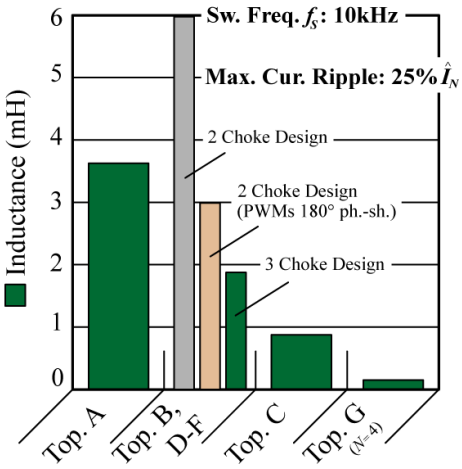


Fig. 5.57: Topology analysis for 10 kW output power of dedicated inductance design for a switching frequency of 10 kHz and a maximum current ripple of 25 % of the mains input peak current.

- As the previous implementation, but PWM carrier signals of both injection legs operated at 180° phase shift allowing a 50 % reduction of the inductance value.
- Utilizing an additional choke L_{h3} in the third harmonic injection path (cf. **Fig. 5.57** - light grey) which allows an additional 40 % inductance reduction for each choke (green).

As Topology C in any case requires a third inductor due to its three-level bridge leg connected to the AC-side, the inductor design considers an additional third choke for all remaining topologies too in order to achieve comparable results. It has to be noted that Topology G provides the smallest inductance value and inductor volume of all listed variants (Topology A-G) if at least $N = 2$ is used (operated in interleaved PWM mode). The interleaved switching operation allows an increased switching frequency at the output ($f_{\mathrm{s,o}} = N f_{\mathrm{s}}$) of the shaping network and hence comes with a smaller inductance (and also inductor volume). If e.g. four switching cells are implemented the inductance value is approximately eight times smaller than that of Topology C.

Chapter 6

FCC Rectifier – Detailed Analysis and Prototype Implementation

As a result of the analyses and simulations given in chapter 5, the dual half-bridge stage (Top. B) and the "Flying Converter Cell" (FCC, Top. C) proved to be the most attractive concepts for THI rectifiers operated at the 400 V mains in the low and medium kVA power region. These two topologies therefore are selected for laboratory prototype verification, starting with the FCC rectifier covered in this chapter. Prior to that however some additional analytical and numerical investigations concerning non-standard operating modes like light-load operation or operation at non-balanced mains voltages etc. are performed which are also valid for the second laboratory prototype based on Top. B and described in chapter 7.

6.1 Light/No-Load Operation

In the following section, light/no-load condition for a hybrid rectifier utilizing a FCC is analyzed in detail. Light load operation of the B6 rectifier has been extensively discussed in *chapter 3* (CCM, $\mathrm{DCM_I}$, $\mathrm{DCM_{II}}$) and is hence only mentioned briefly here to highlight the differences of both rectifiers.
For the passive three-phase rectifier the term CCM is typically referring to the state of the rectifiers inductor current i_L. CCM operation is true if the DC-side smoothing inductor current is of positive value during a full period $[0 \ldots 2\pi]$. The so called "discontinuous conduction mode" typically shows at least one section where the current of the DC inductor equals 0 A. For both CCM and DCM no high frequency common-mode voltage can be observed and the maximum out-

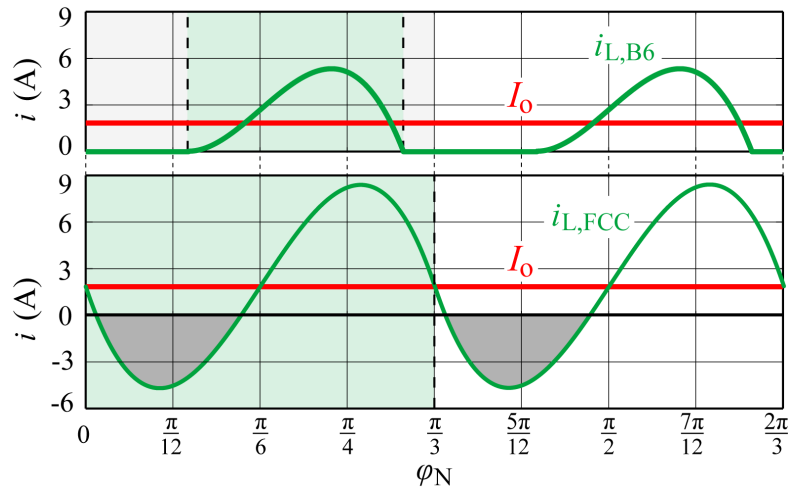


Fig. 6.1: Numerically and analytically calculated DC-side smoothing inductor current regarding passive $i_{L,B6}$ (DCM_{II}) and active rectification $i_{L,FCC}$, respectively, for a rated output power of approximately 1 kW and a DC-side smoothing choke value of 2.25 mH for a 10 kW rectifier system.

put voltage is given due to its physical limitations defined by the mains voltages ($V_{o,max} = \sqrt{3}\hat{V}_N$).
As briefly discussed in [23] this discontinuous state based on the DC-side smoothing inductance current never occurs for the hybrid system due to the active FCC topology which is able to process positive and negative current values, also depicted in **Fig. 6.1**. Furthermore, the B6 rectifier shows a slightly increased output voltage ($V_o \approx 550$ V instead of 537.5 V) for an output power of approximately 1 kW and is operating in DCM_{II} mode, whereas a FCC system still operates in continuous conduction mode (CCM) at 1 kW (for e.g. injection chokes of $L_c = 2$ mH) and hence an output voltage V_o of the expected 537.5 V can be observed. The peak-to-peak 300 Hz DC-side choke current component is, however, considerably higher for FCC operation than for passive rectification which results in increased inductor losses for light loads of the active system and therefore in reduced efficiency η_{FCC}.
The discontinuous mode for the hybrid system is rather related to the current situation of the positive and negative busbar currents i_{pos} and i_{neg}. As these currents are not assigned to any choke, the state is not designated as "discontinuous conduction mode" but rather denominated as "intermittent current operating mode" (ICOM). The FCC can be operated in different modes during ICOM which basically depends on the behaviour of the bidirectional switch arrangement connected to the AC-side of the passive system. In this work three different modes, which are defined as specific "operating mode" (OM), are considered. Three different operating modes are defined by

- **Operating Mode I** (OM_I): FCC fully in operation, however, current injection devices ($S_1 - S_3$) disabled
- **Operating Mode II** (OM_{II}): FCC fully in operation including current injection devices

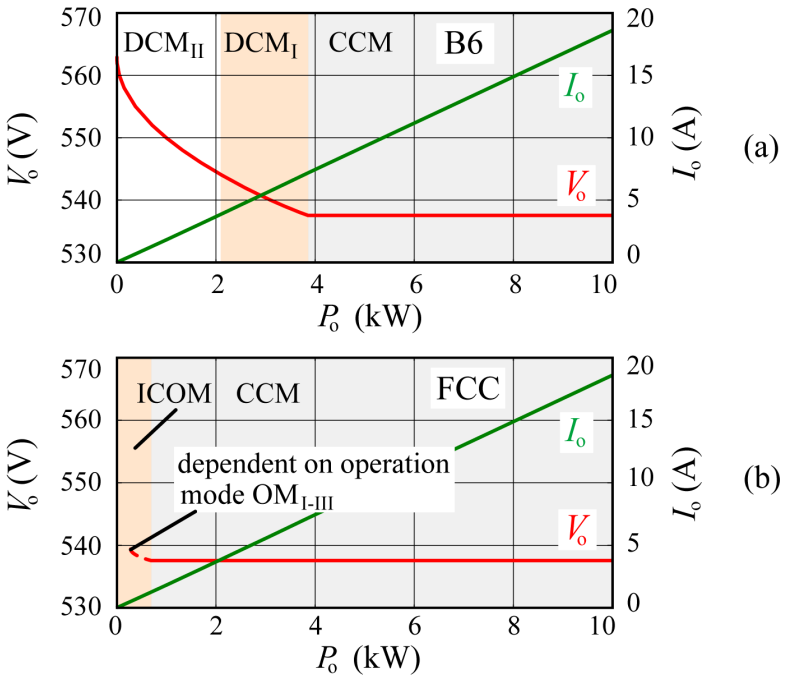


Fig. 6.2: Calculated output characteristics V_o and I_o for an output power range from no-load operation (0 W) to nominal load (10 kW) considering (a) CCM, DCM$_I$ and DCM$_{II}$ of a passive three-phase diode bridge rectifier (upper figure) with $L_{DC} = 2.25$ mH and (b) CCM and ICOM of the hybrid rectifier utilizing a FCC (lower graph) for an injection inductance L_c of 2 mH.

- **Operating Mode III** (OM$_{III}$): FCC operation stopped (only passive diode bridge operating)

Benefits and drawbacks of the appropriate modes are discussed in the following. Additionally, symmetric values of the coupled three-phase injection choke $L_{cp} = L_{cn} = L_{h3} = L_c$ and perfectly balanced FCC DC voltages $v_{cp} = v_{cn} = V_c$ are assumed.

6.1.1 Continuous to Discontinuous Operation Boundaries

Before investigating the different operating modes (OM$_{I-III}$) for intermittent currents i_{pos} and i_{neg} of the hybrid system in detail, an elaborate analyzes for both passive system CCM to DCM boundary (i_L) and active system CCM to ICOM (intermittent current operating mode) boundary (i_{pos},i_{neg}) has to be determined. The DC-side smoothing inductance current i_L for continuous conduction mode is required which calculates to

$$i_{L,CCM}(\varphi_N) = I_o - \frac{3\sqrt{3}\hat{V}_N}{\pi\omega_N L_{DC}} \sum_{k=1}^{\infty} \frac{2}{(6k)^3 - 6k} \sin(6k\varphi_N) \tag{6.1}$$

with $k = 1, 2, \ldots$, where I_o is the output current of the system and ω_N the mains angular frequency. **Eq. 6.1** is valid for both, the passive and the active system

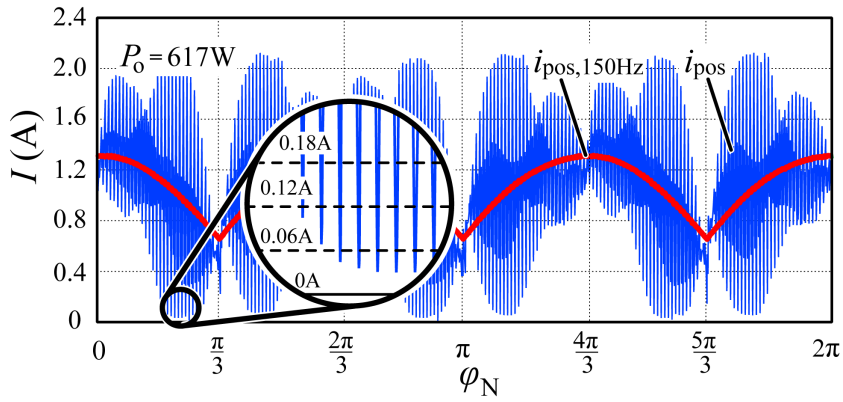


Fig. 6.3: Simulated current i_{pos} for the calculated output power regarding CCM/ICOM boundary. A three-phase injection inductance L_{c} of 2 mH, DC-side smoothing inductance L_{DC} of 2.25 mH, a switching frequency f_{s} of 10 kHz and FCC DC voltages V_{c} of 400 V are assumed.

while operating in CCM. The transition between CCM and DCM of the B6 rectifier can be found at $i_{\mathrm{L,CCM}}(\varphi_{\mathrm{N}}) = 0\,\mathrm{A}$ which yields an appropriate output power level of

$$P_{\mathrm{o,CCM/DCM_I}} = \frac{3(3\hat{V}_{\mathrm{N}})^2}{\pi\omega_{\mathrm{N}}L_{\mathrm{DC}}}\left(\frac{1}{\pi}\arcsin\left(\frac{3}{\pi}\right) - \frac{1}{2} + \frac{1}{\pi}\sqrt{\left(\frac{\pi}{3}\right)^2 - 1}\right). \tag{6.2}$$

If a passive system for a rated output power of 10 kW and a DC-side smoothing inductance of 2.25 mH for an appropriate $\mathrm{THD_i}$ of $\approx 48\,\%$ is assumed the CCM to $\mathrm{DCM_I}$ threshold computes to $P_{\mathrm{o,CCM/DCM_I}}(L_{\mathrm{DC}} = 2.25\mathrm{mH}) \approx 4\,\mathrm{kW}$. Starting from this reference point, the output voltage cannot be considered longer to be $V_{\mathrm{o,max}} = \frac{3\sqrt{3}\hat{V}_{\mathrm{N}}}{\pi} = 537.5\,\mathrm{V}$ but is increasing for decreasing loads and limited to $V_{\mathrm{o,max}} = \sqrt{3}\hat{V}_{\mathrm{N}} = 563\,\mathrm{V}$. The averaged output voltage can only be calculated numerically for discontinuous conduction mode and is plotted in **Fig. 6.2(a)**.
As already announced, the transition from CCM to ICOM for the FCC topology originates from the current situation of the positive and negative busbar currents of the passive diode bridge rectifier. Considering ideal current waveforms neglecting the switching frequency ripple, 0 A sections regarding i_{pos} and i_{neg} can only be found for $P_{\mathrm{o}} = 0\,\mathrm{W}$. This leads to the assumption that the CCM to ICOM boundary does not only depend on the low frequency current component of i_{pos} and i_{neg} but is also dependent on the high switching frequency ripple evoked due to the coupled three-phase injection inductance L_{c} and its design. In order to calculate the mentioned state threshold, the minimum of the positive busbar current $\min(i_{\mathrm{pos,CCM}})$ for CCM light-load conditions needs to be evaluated, which can be found at $\varphi_{\mathrm{N}} \approx \pi/3$. The transition from CCM to ICOM is available if one half of the maximum ripple (at $\pi/3$) equals (or appears to be larger than) the averaged sinusoidal wave shapes i_{pos} during this time instant which can be stated by the following equation

$$\frac{\Delta i_{\mathrm{cp,pkpk}}}{2} = \hat{I}_{\mathrm{N}} \cdot \cos\left(\frac{\pi}{3}\right). \tag{6.3}$$

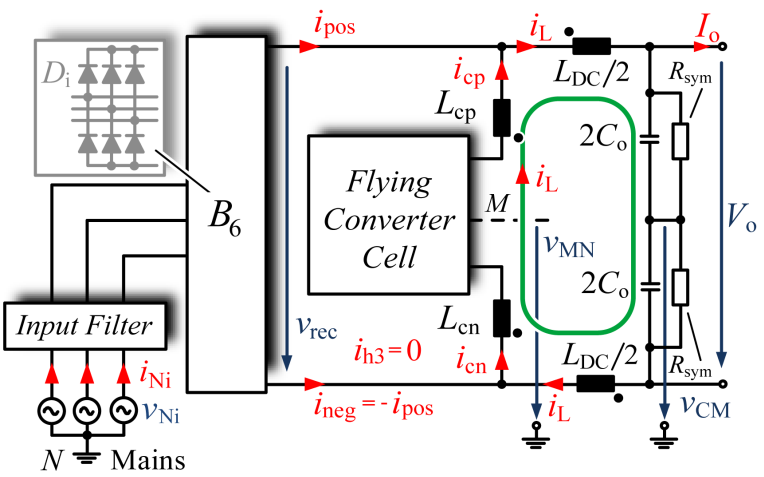


Fig. 6.4: Basic schematic of active rectifier topology during no-load condition while operating in $\mathrm{OM_I}$. Circulating current i_L (green) leads to unfavourable additional losses during no- and light-load mode.

An appropriate power level can hence be assessed by

$$P_{\mathrm{o,CCM/ICOM}} = \frac{MV_c^2\left(\frac{3}{4}M - \frac{1}{2\sqrt{3}}\right)\left(1 - \frac{\sqrt{3}}{2}M\right)}{f_s L_c}\,. \tag{6.4}$$

The CCM to ICOM threshold (cf., **Fig. 6.2(b)**) therefore yields

$$P_{\mathrm{o,CCM/ICOM}}\Big|_{V_c=400\,\mathrm{V},\ L_c=2\,\mathrm{mH},\ f_s=10\,\mathrm{kHz}} \approx 600\,\mathrm{W}. \tag{6.5}$$

In **Fig. 6.3** simulation results of the FCC topology for the given constraints are depicted. Comparing **Eq. 6.2** and **Eq. 6.4** the CCM to DCM boundary of the passive system shows inverse proportional behaviour of the DC-side smoothing inductance L_{DC}, whereas the boundary between continuous to intermittent currents i_{pos} and i_{neg} of the hybrid system is independent of L_{DC} but yields $1/x$-dependency of the coupled three-phase inductor L_c.
The active system can hence operate in CCM for a wide power range if the injection inductance is appropriately designed which mainly results in a very good input current quality for the respective load region.

6.1.2 FCC Operation During No/Light-Load Condition

In contrast to the passive rectifier which could not yield negative inductor current values ($i_{L,B6} \geq 0$, cf., **Fig. 6.1**) due to its semiconductor arrangement (passive diode bridge), the inductor current ($i_{L,FCC}$) of the FCC system never shows zero current gaps during light/no-load condition (**Fig. 6.1**). This is caused by the FCC topology which is able to provide positive and negative current values. While the diode bridge is blocking for negative current intervals of i_{pos} and i_{neg}, i_L occurs as **circulating current** which has to be processed by the FCC, the DC-side smoothing inductor L_{DC} and the DC-link voltage capacitor C_o during no-load condition.

This circular current causes additional losses compared to a passive system during no-load operation (inductor losses L_{DC} and L_{c}, switching and conduction losses etc.) and shows a high frequency current ripple with switching frequency.

A. Operating Mode I ($\mathrm{OM_I}$*)*

In $\mathrm{OM_I}$ (**Fig. 6.4**) the current injection device ($S_1 - S_3$) is disabled during no-load operation and the third harmonic injection current i_{h3} therefore equals zero. This leads to identical busbar current values ($|i_{\mathrm{pos}}| = |i_{\mathrm{neg}}|$) while the diodes are conducting, which can be also verified by

$$\begin{aligned} i_{\mathrm{h3}} = i_{\mathrm{cp}} - i_{\mathrm{cn}} = 0 \implies i_{\mathrm{cp}} &= i_{\mathrm{cn}} \\ i_{\mathrm{pos}} &= i_{\mathrm{L}} - i_{\mathrm{cp}} \\ i_{\mathrm{neg}} &= i_{\mathrm{cn}} - i_{\mathrm{L}} \\ \implies i_{\mathrm{pos}} &= -i_{\mathrm{neg}} \ . \end{aligned} \tag{6.6}$$

Only four different switching states of the FCC occur during no-load mode ($S_{\mathrm{cp+}} = 0$ and $S_{\mathrm{cn+}} = 0$; $S_{\mathrm{cp+}} = 1$ and $S_{\mathrm{cn+}} = 0$; $S_{\mathrm{cp+}} = 0$ and $S_{\mathrm{cn+}} = 1$; $S_{\mathrm{cp+}} = 1$ and $S_{\mathrm{cn+}} = 1$, 1...corresponding switch closed). The passive diode bridge is blocking each time $S_{\mathrm{cp+}} = 1$ and $S_{\mathrm{cn+}} = 0$ is valid, as the maximum FCC DC voltage $2V_{\mathrm{c}} > \sqrt{3}\hat{V}_{\mathrm{N}}$ applies. In section $\varphi_{\mathrm{N}} \in \left[0 \ldots \frac{\pi}{6}\right]$, power flow ($i_{\mathrm{pos}} = i_{\mathrm{neg}} = 0$) from the grid to the DC-side is not possible if $v_{\mathrm{N1}} - v_{\mathrm{N3}} < v_{\mathrm{rec}}$ is valid, which means that the passive rectifier diodes would be stressed with a high frequency component with switching frequency f_{s}.
As the bidirectional switches are not operated anymore, the averaged midpoint voltage of the FCC ($v_{\mathrm{MN,avg}}$) cannot longer be controlled to zero. The different voltage levels of the FCC midpoint voltage v_{MN} are characterized by an additional low frequency 150 Hz voltage component which is given due to the mains voltage situation and further depending on the half-bridge switching states which now yield 0 V, v_{Ni}, $v_{\mathrm{Ni}} \pm V_{\mathrm{c}}/2$ instead of 0 V, $\pm 2V_{\mathrm{c}}/3$, $\pm V_{\mathrm{c}}/3$ for the appropriate FCC control.
The low frequency common-mode voltage v_{CM} is defined by the mains voltage situation (e.g. $v_{\mathrm{CM}} = v_{\mathrm{N2}}/2$ for $\varphi_{\mathrm{N}} \in \left[0 \ldots \frac{\pi}{6}\right]$) during conduction of the passive rectifier diodes and is zero while the passive diode bridge is blocking (due to increased DC-side voltage levels). As can be observed from **Fig. 6.5**, v_{CM} is therefore characterized by a voltage ripple with switching frequency in this mode.
If the diode bridge is not conducting the DC-side choke L_{DC} is stressed by an increased voltage defined due to the DC-side voltage situation which addresses additional high frequent (f_{s}) losses for the DC-side smoothing inductance during no-load mode. Due to the circulating current for no-load mode the inductor losses are defined by

$$P_{L_{\mathrm{DC}}} = P_{\mathrm{Cu,DC}} + P_{\mathrm{Cu,AC}}\left(6 \cdot f_{\mathrm{N}}, f_{\mathrm{s}}\right) + P_{\mathrm{Fe}}\left(6 \cdot f_{\mathrm{N}}, f_{\mathrm{s}}\right) \tag{6.7}$$

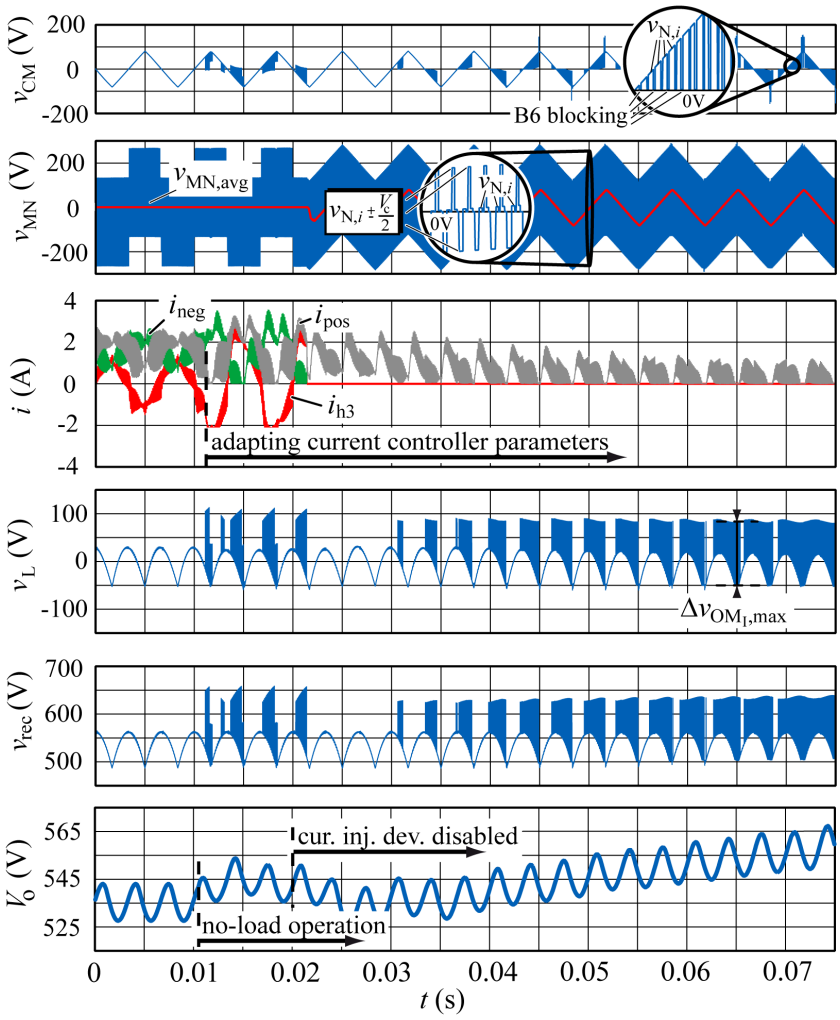


Fig. 6.5: Simulation results considering notable parameters as common-mode output voltage v_{CM}, midpoint to neutral point voltage v_{MN}, DC-side currents i_{pos}, i_{neg}, i_{h3}, rectifier output voltage v_{rec}, DC-side smoothing inductance voltage v_L and output voltage of the active rectifier syste V_o, for continuous conduction mode and no-load mode (OM_I).

The maximum applied peak-to-peak voltage $\Delta v_{OM_I,max}$ as depicted in **Fig. 6.5** is defined by

$$\Delta v_{OM_I,max} = \frac{L_{DC}}{L_c + L_{DC}/2} \cdot \frac{V_c}{2} \,. \tag{6.8}$$

The FCC rectifier system furthermore shows an increase of the output voltage V_o during no-load operation. As the limit for a conventional passive rectifier system is defined by the mains maximum line-to-line voltage level ($V_{o,max} = V_{ij,max} = \sqrt{3}\hat{V}_N = 563\,V$), the maximum output voltage of the active system is characterized by the inductance value of the coupled three-phase inductor L_c and calculates to

$$\Delta V_{o,idle} = V_c \frac{\left(\frac{3\sqrt{3}}{\pi}M - 1\right)\frac{L_{DC}}{L_c+L_{DC}/2}\left(1 - \frac{3\sqrt{3}}{2\pi}M\right)}{1 - \frac{L_{DC}}{L_c+L_{DC}/2}\left(1 - \frac{3\sqrt{3}}{2\pi}M\right)} \tag{6.9}$$

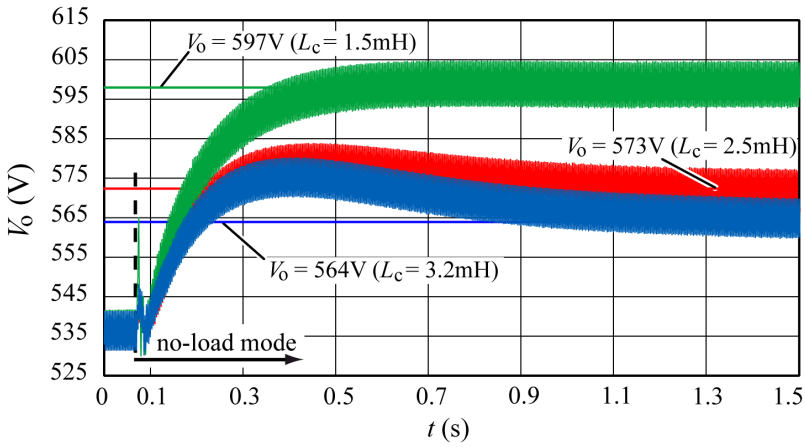


Fig. 6.6: Simulation results of the active rectifier system ($\mathrm{OM_I}$) regarding output voltage V_o for different injection inductance values L_c and appropriate calculated values (colored horizontal lines).

where M denotes the modulation index and is given by $\hat{V}_N/V_c$ (hence $M = \sqrt{2} \cdot 230\,\mathrm{V_{eff}}/400\,\mathrm{V} = 0.813$). **Fig. 6.6** illustrates simulation results considering the output voltage V_o of the active rectifier system while operating in no-load mode for different inductance values L_c. As previously described, increased output voltages can be observed and the steady state output voltage levels are in good conformity with the calculated output voltages using **Eq. 6.9**. The appearing time constant of the load step characteristic (V_o response in **Fig. 6.6**) is caused by the physical and digital implementation of hardware and software of the passive system and the active FCC.
In conclusion, during operation of $\mathrm{OM_I}$ and no-load condition, (i) an increased output voltage V_o, (ii) additional losses due to circulating current i_L with superimposed high frequency current ripple and (iii) a high frequency common-mode voltage v_{CM} have to be expected.

B. Operating Mode II ($\mathrm{OM_{II}}$)

As mentioned, the three different modes $\mathrm{OM_{I-III}}$ are defined by the operating state of the FCC during ICOM. $\mathrm{OM_{II}}$ is valid if ICOM is detected by the system and all bidirectional switches connected to the AC-side of the hybrid system are still operated. In contrast to the control method for the Vienna Rectifier proposed in [68], where the switches are controlled differently for CCM and DCM, the six switches attached to the FCC active rectifier still continue pursuing their 90° low switching duty each phase while operated in $\mathrm{OM_{II}}$. Consequently, the FCC is still connected cyclically to the AC-side mains even for no-load mode operation.
The passive three-phase rectifier can be considered as two M_3-structures (**Fig. 6.7**) with diodes (D_1, D_3, D_5) and forward biased during the positive half-waves and the negative midpoint structure $M_{3,\mathrm{neg}}$ whose diodes (D_2, D_4, D_6) are forward biased during the negative half-waves. It is essential to distinguish between these two diode assemblies, as in contrast to CCM, $\mathrm{OM_I}$ or $\mathrm{OM_{III}}$, both M_3-structures are not only conducting at the same time for $\mathrm{OM_{II}}$ but also conducting separately,

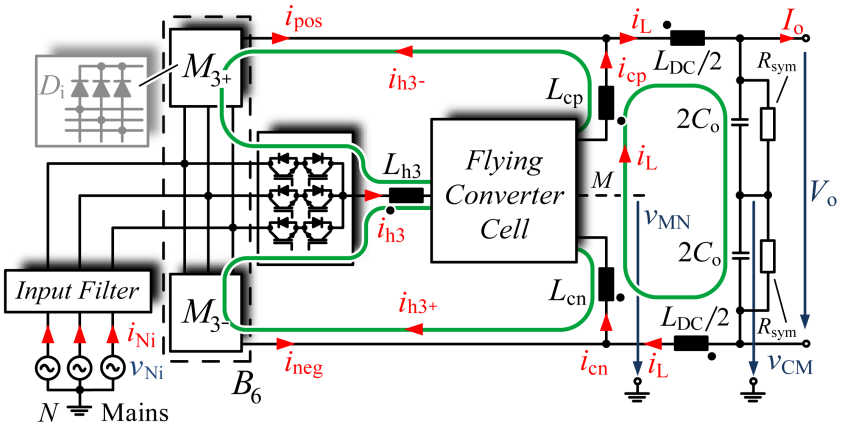


Fig. 6.7: Schematic of FCC active rectifier operating in $\mathrm{OM_{II}}$ during no-load condition. As bidirectional switch topology still active, two different circulating currents occur (i_{h3} and i_L), causing increased losses compared to $\mathrm{OM_I}$.

which is primarily evoked due to the operating three-level unidirectional bridge leg (S_{h3}, $D_{h3\pm}$). Considering ideally controlled currents i_{pos} and i_{neg}, $i_{h3,150Hz}$ can be assumed to equal zero as the electrical conductance value $g_e^* = 0$. The three-level bridge still generates a high frequency current ripple with switching frequency $\Delta i_{h3,f_s}$, which can be compared with no-load characteristics of half- or three-level bridge legs. This continuous current ripple has to be processed by an alternative circuit path during no-load mode which has to be provided by one of the midpoint structures $M_{3,pos}$ or $M_{3,neg}$ (depending on the sign of the third harmonic injection current). The diode assembly is hence offering an alternative current path, depending on the AC- and DC-side voltage situation and the sign of the generated current i_{h3}, very similar to a "Freewheeling" diode of a e.g. buck converter topology. The remaining midpoint structure is blocking and therefore not conducting any current. This high frequent current ripple hence appears as an additional circulating current (cf., **Fig. 6.7**). $\mathrm{OM_{II}}$ hence causes two differing circulating currents i_L and i_{h3}. In order to validate the discussed issues a third harmonic injection current ripple $i_{h3,f_s} < 0\,\mathrm{A}$ is assumed. As previously mentioned, the negative midpoint structure $M_{3,neg}$ is blocking which leads to $i_{neg} = 0$ and i_{cn} can be computed to

$$\begin{aligned} i_{cn} &= i_{neg} + i_L \\ \Longrightarrow\ i_{cn} &= i_L\ . \end{aligned} \tag{6.10}$$

The positive busbar current i_{pos} can be calculated to $i_{pos} = -i_{h3}$. The current i_{pos} hence equals negative injection current i_{h3} if $M_{3,neg}$ is blocking. Similarly, the same assumptions made for $i_{h3,f_s} > 0\,\mathrm{A}$ lead to $i_{cp} = i_L$ and hence $i_{neg} = -i_{h3}$. As the injection inductance (L_{h3}) potential is still defined by the AC-side mains (due to operating bidirectional switches), the midpoint voltage $v_{MN,avg}$ can still be controlled to be zero which is also depicted in **Fig. 6.8**.

Similar to $\mathrm{OM_I}$, the DC-side smoothing inductance L_{DC} shows increased (high frequent (f_s)) losses during no-load mode while operating in $\mathrm{OM_{II}}$ which is basically evoked due to alternating blocking of the two midpoint structures (further

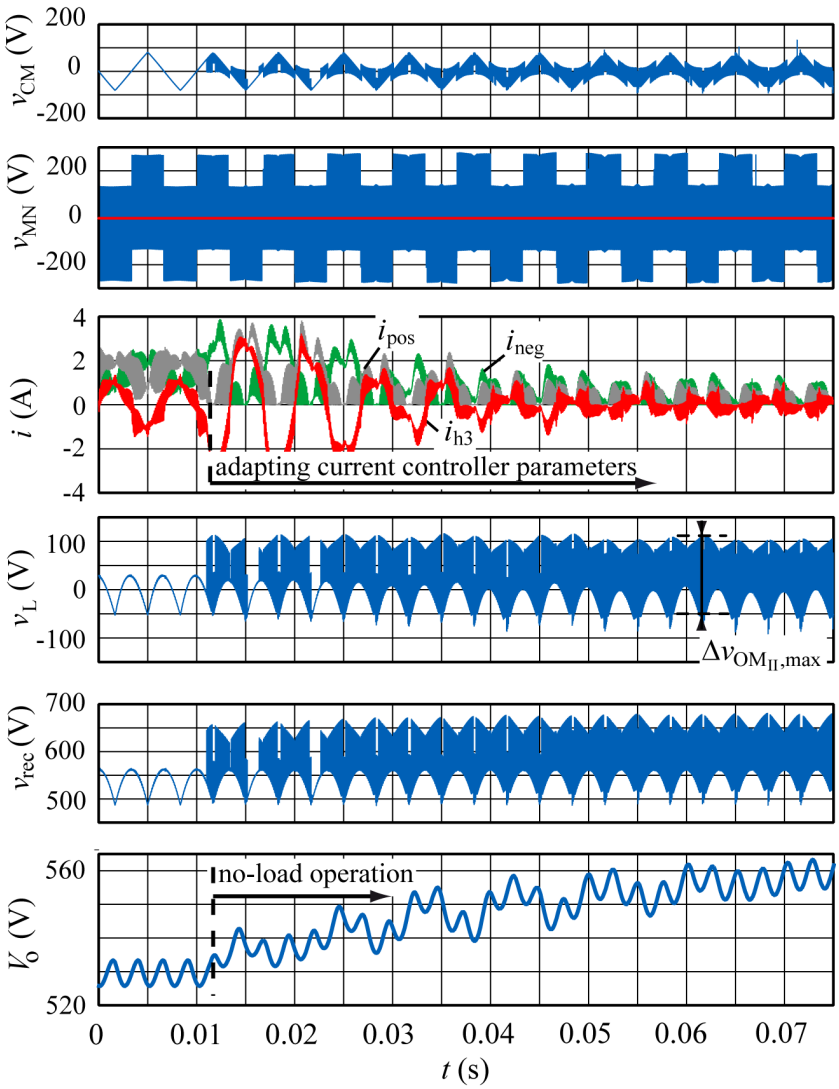


Fig. 6.8: Simulation results considering notable parameters as common-mode output voltage v_{CM}, midpoint to neutral point voltage v_{MN}, DC-side currents i_{pos}, i_{neg}, i_{h3}, rectifier output voltage v_{rec}, DC-side smoothing inductance voltage v_L and output voltage of the active rectifier syste V_o, for continuous conduction mode and no-load mode (OM_{II}).

resulting in a high frequency common-mode voltage v_{CM} with switching frequency f_s shown in **Fig. 6.8**). An increased peak-to-peak voltage v_L can be observed. The maximum voltage $\Delta v_{OM_{II},max}$ across the DC-side choke calculates to

$$\Delta v_{OM_{II},max} = \frac{L_{DC}}{L_c + L_{DC}/2} \frac{3V_c}{5} \tag{6.11}$$

As can be noticed, the maximum applied peak-to-peak voltage $\Delta v_{OM_{II},max}$ is approximately 20 % larger for OM_{II} than for OM_I ($\Delta v_{OM_{II},max} = 1.2 \cdot \Delta v_{OM_I,max}$). Both operating modes furthermore show increased output voltages. The final output voltage V_o is defined by the inductance ratio between L_c and L_{DC} similarly as for OM_I. The output voltage level appears to be much higher as only one duty cycle δ_{cp} or δ_{cn} is mandatory, primarily depending on which midpoint structure is

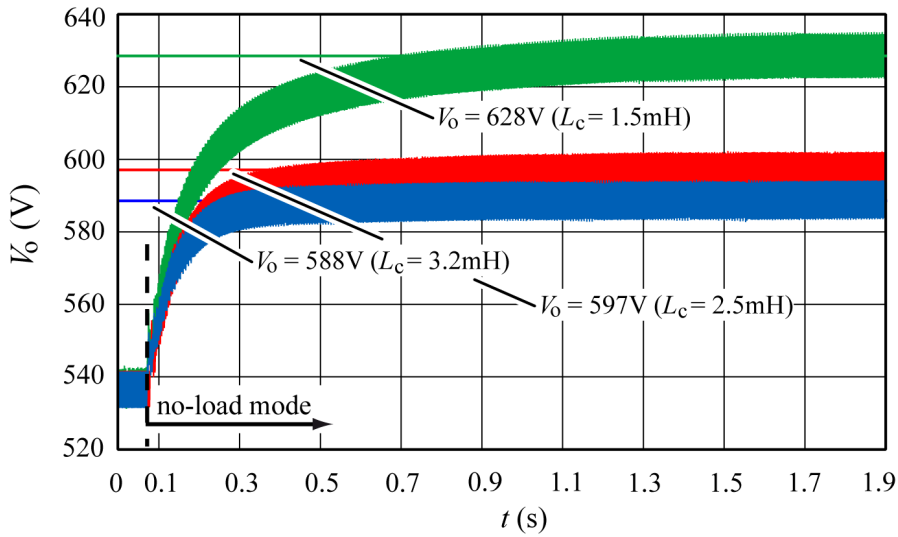


Fig. 6.9: Simulation results of the active rectifier system regarding output voltage V_o while operating in OM_{II} for different injection inductance values L_c and appropriate calculated values (colored horizontal lines) which obviously results in divergent output voltage levels.

blocking. The output voltage $V_{o,idle}$ can hence be computed to

$$\Delta V_{o,idle} = V_c \frac{\frac{3\sqrt{3}}{2\pi} M \frac{L_{DC}}{L_c + L_{DC}/2} \left(1 - \frac{3\sqrt{3}}{2\pi} M\right)}{1 - \frac{1}{2} \frac{L_{DC}}{L_c + L_{DC}/2} \left(1 - \frac{3\sqrt{3}}{2\pi} M\right)} . \tag{6.12}$$

Fig. 6.9 shows simulated and calculated steady state output voltage values for different injection inductance values L_c.

C. Operating Mode III (OM_{III})

For operating mode III, the FCC circuitry is completely switched off (only the passive diode bridge is operating) which means that the system shows discontinuous mode behavior very well known for a passive diode bridge rectifier. Depending on the ICOM boundary, the active system directly enters DCM_I or DCM_{II} when getting disabled. The difference between those two discontinuous operation modes is defined by the input or DC-side smoothing inductance current characteristic as depicted in **Fig. 6.10**. The rectifier output voltage v_{rec} and the DC-side inductance current i_L consist of four different sectors (I-IV) for DCM_I. Considering DCM_{II} only two different sectors can be found anymore, which is defined due to the increased 0 A current gap and the hence missing commutation process of the passive diode bridge. The boundary between these two discontinuous modes is characterized by $i_L\left(\varphi_N = \gamma = k\frac{\pi}{3}\right) = 0\text{A}$ for $k \in \mathbb{Z}$ which leads to a specific output power value $P_{o,DCM12}$

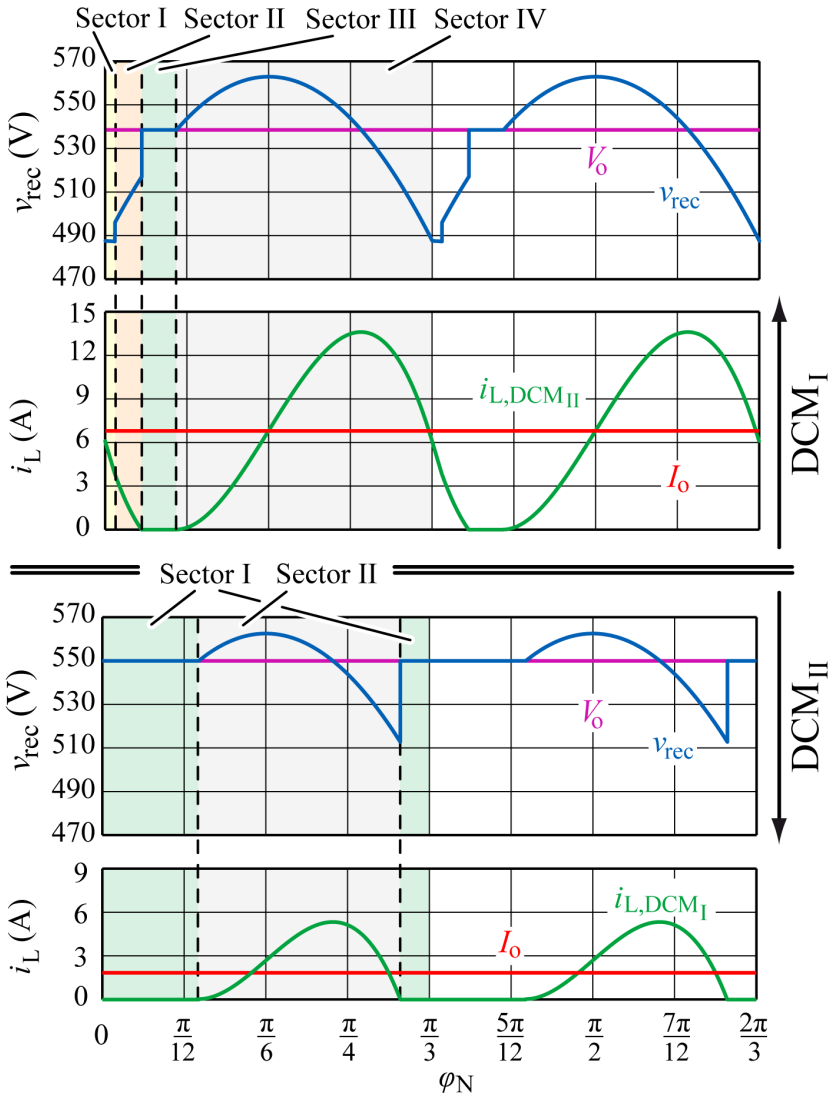


Fig. 6.10: Calculated passive three-phase rectifier bridge voltage v_{rec}, system output voltage V_o and DC-side smoothing inductance current i_L for discontinuous conduction mode I and II of a passive system (FCC deactivated - OM_{III}). Depending on the designed injection inductance L_c, the system enters DCM_I or DCM_{II} during light-load mode if the active topology is deactivated.

$$
\begin{aligned}
P_{o,DCM_{I/II}} = \frac{3\sqrt{3}\hat{V}_N V_o}{\pi\omega_N L_{DC}} \Bigg(& \frac{V_o}{\sqrt{3}\hat{V}_N} - \frac{\sqrt{3}}{2} + \dots \\
& \dots + \left(\frac{\pi}{3} - \alpha_D\right) \sqrt{1 - \frac{1}{3}\left(\frac{V_o}{\hat{V}_N}\right)^2} \Bigg) + \dots \\
& \dots + \frac{3V_o^2}{\pi\omega_N L_{DC}} \left(\left(\frac{\pi}{3} - \alpha_D\right)\alpha_D - \frac{\left(\frac{\pi}{3}\right)^2 - \alpha_D^2}{2} \right)
\end{aligned}
\tag{6.13}
$$

which can be approximately calculated to 1.9 kW for a given DC-side smoothing inductor value of 2.25 mH, negligence of output voltage ripple ($C_o \to \infty$) and

$\alpha_\mathrm{D} = -\frac{\pi}{3} + \arcsin\left(\frac{V_\mathrm{o}}{\sqrt{3}\hat{V}_\mathrm{N}}\right)$. $V_\mathrm{o} = \frac{3\sqrt{3}\hat{V}_\mathrm{N}}{\pi}$ is no longer valid for discontinuous conduction mode and has to be evaluated numerically. Exactly like $\mathrm{OM_I}$ and $\mathrm{OM_{II}}$, also $\mathrm{OM_{III}}$ leads to increased output voltage levels of V_o during discontinuous mode. The output voltage, however, is limited due to the mains situation to $V_\mathrm{o,idle,max} = \sqrt{3}\hat{V}_\mathrm{N}$.
As the FCC is completely disabled, no high frequency common-mode voltage at the output of the system appears. Only the typical low frequency 150 Hz component can be observed which is slightly differing in its characteristic (compared to the conduction mode waveform) due to the blocking passive diode bridge instants. For no-load operation the ideal passive diode bridge does not show any currents or circulating currents and is therefore loss-free, which is not valid for $\mathrm{OM_I}$ and $\mathrm{OM_{II}}$ as discussed in previous sections.

6.1.3 Enhanced Design Guidlines

In the following some guidance to select the inductance value of the three-phase choke L_c is given considering also limitations of operation in light/no-load condition. As mentioned before both operating modes ($\mathrm{OM_I}$ and $\mathrm{OM_{II}}$) show a high dependency on the designed three-phase inductance value L_c. The maximum inductance value of the coupled three-phase choke L_c is usually defined by the maximum ripple current. A specific amount of voltage V_c is required for proper current shaping which limits the inductance L_c for a given FCC DC-link voltage of $V_\mathrm{c} = 400\,\mathrm{V}$. The maximum inductance of the inductor is given by $V_\mathrm{c} > \max\left(v_\mathrm{pos} + v_\mathrm{L,cp} - v_\mathrm{MN}\right)$ and hence calculated by

$$L_\mathrm{c,max} < \frac{1 - \frac{2|v_\mathrm{off}|}{V_\mathrm{c}} - \frac{\sqrt{3}}{2}M}{\frac{\sqrt{3}}{L_\mathrm{DC}}M\left(1 - \frac{3}{\pi}\right) + \frac{\hat{I}\omega}{2V_\mathrm{c}}} \tag{6.14}$$

where v_off is the offset of the midpoint voltage v_MN according to the voltage balancing concept and $\hat{I}_\mathrm{N}$ the AC-side sinusoidal input current peak value depending on the output load situation. Continuous conduction mode (CCM) to discontinuous conduction mode (DCM) boundary can be found if the ripple of i_pos (defined due to the ripple of i_cp) reaches zero. The minimum allowable inductance value is defined by

$$L_\mathrm{c,min} = \frac{MV_\mathrm{c}^2\left(\frac{3}{4}M - \frac{1}{2\sqrt{3}}\right)\left(1 - \frac{\sqrt{3}}{2}M\right)}{f_\mathrm{s}P_\mathrm{o,min}} \tag{6.15}$$

for a given minimum output power $P_\mathrm{o,min}$ (and defined FCC DC voltages V_c), where the described side effects during light/no-load mode do not occur. Considering a rated output power of 10 kW and a switching frequency of 10 kHz, a current ripple of $\Delta i_\mathrm{cp} = 20\,\% \cdot \max\left|i_\mathrm{cp}\left(\varphi_\mathrm{N}\right)\right| = 2.4\,\mathrm{A}$ would lead to a CCM/DCM boundary of 0.68 kW which is 7 % of the rated output power P_o.

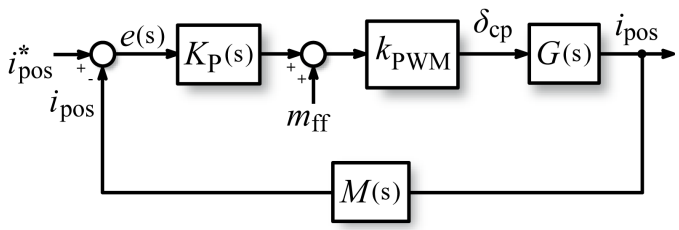


Fig. 6.11: Closed loop current controller structure valid for continuous conduction mode of the active rectifier system using a FCC.

6.1.4 Current/Voltage Controller Issues

A. Voltage/Balancing Controller

As discussed in chapter 5.3, the voltage balancing controller (regarding FCC DC voltages v_{cp} and v_{cn}) capability is defined by a linear dependency of v_{off} and P_{in}. Considering an ideal system, the FCC would not be able the guarantee equal DC voltage levels during no-load mode (due to $P_{\text{in}} = 0$). The real system, however, includes passive symmetry resistors at the output which advantageously serve as minimal load P_{min} ($i_{\text{L,avg}} \neq 0 \rightarrow i_{\text{pos,avg}} \neq 0$) during "no-load" at the output of the system $I_{\text{o}} = 0\,\text{A}$. The non-ideal active system furthermore includes DC- and AC-resistive components of inductors and equivalent series resistances of capacitors which yield additional losses that have to be compensated by the voltage controller which means further increased input power. The equivalent conductance value g^*_{e} and hence the input power P_{in} are not equal zero and therefore the FCC DC voltages can still be controlled and balanced during no- and light-load operation.

B. Current Controller Implementation

As mentioned, the current controller can be implemented as simple P-type controller in combination with the modulation feed forward-term

$$m_{\text{ff}}(\text{s}) = \frac{v_{\text{pos}}}{V_{\text{c}}} + \frac{\text{s}L_{\text{c}} i_{\text{L}}}{V_{\text{c}}\,(1 + \text{s}T_{\text{c}})} \tag{6.16}$$

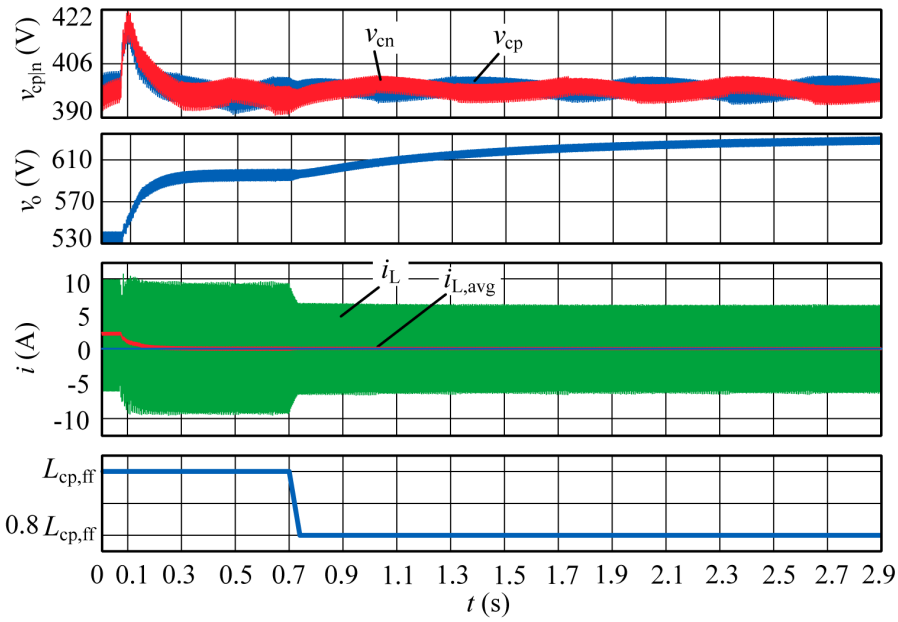
as the system transfer function can be reduced to

$$G(\text{s}) = \frac{i_{\text{pos}}(\text{s})}{\delta_{\text{cp}}(\text{s})} = \frac{V_{\text{c}}}{\text{s}L_{\text{c}}}\,. \tag{6.17}$$

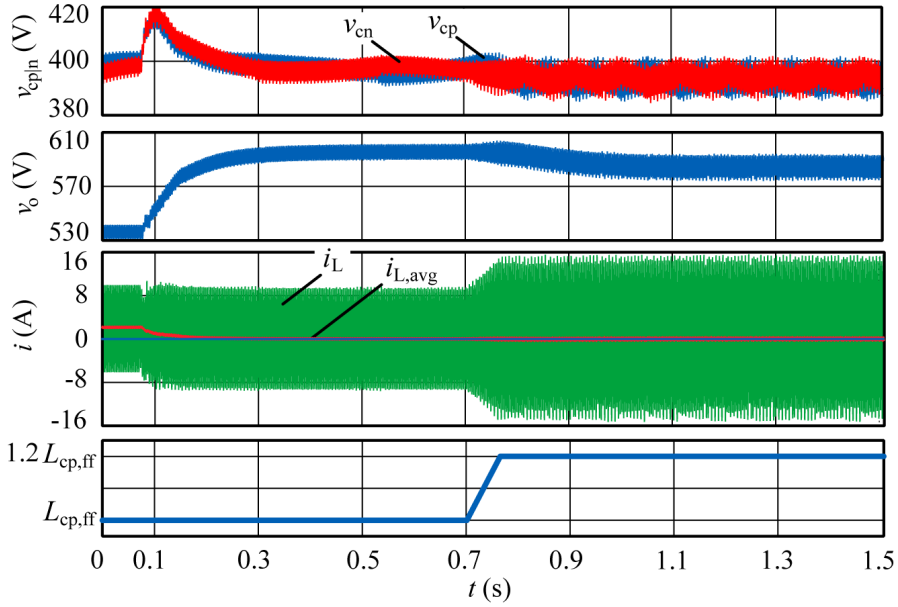
The low-pass filter term $1/(1 + \text{s}T_{\text{c}})$ in the feed forward-term is required to omit amplification of high frequency noise due to the derivative element (D-element) component. Assuming $K_{\text{P}}(\text{s}) = k_{\text{p}}$ (simple P-type controller), the closed loop system calculates to

$$\frac{i_{\text{pos}}}{i^*_{\text{pos}}} = \frac{K_{\text{P}}(\text{s})\,G(\text{s})}{1 + K_{\text{P}}(\text{s})\,G(\text{s})} = \frac{k_{\text{P}}(\text{s})\,G(\text{s})}{1 + k_{\text{P}}(\text{s})\,G(\text{s})} \tag{6.18}$$

and is depicted in **Fig. 6.11**, whereas k_{PWM} is of constant value and generally



(a)



(b)

Fig. 6.12: Load step from 1 kW to 0 W. After approximately 0.7 s, the feedforward inductance value is going to be (a) decreased (resulting in reduced low-frequent current ripple, losses, extenuated FCC DC voltage balancing capability and raised steady state output voltage V_o) or (b) increased (causing higher low frequency current ripple, losses, improved FCC DC voltage balancing capability and diminished steady state output voltage V_o).

assumed to be 1 , and $M(s)$ is the transfer function of the current transducer which is basically modelled as low-pass filter structure is also neglected and assumed as ideal current transducer ("1") for further calculations. The permanent control

deviation $\left(\lim_{\mathrm{s}\to 0} \mathrm{s}\cdot e(\mathrm{s})\right)$ hence calculates to

$$\lim_{\mathrm{s}\to 0} \mathrm{s}\cdot e(\mathrm{s}) = \lim_{\mathrm{s}\to 0} \mathrm{s}\,\frac{1}{\mathrm{s}}\,\frac{1}{1+K_{\mathrm{P}}(\mathrm{s})\,G(\mathrm{s})} = 0 \tag{6.19}$$

A P-type controller would be perfectly applicable, for continuous conduction mode (CCM) and no occurring disturbances of the AC-side mains. During no-load mode, however, the increased output voltage can be observed as disturbance from a point of view of the current controller and basically results in $v_{\mathrm{pos}} + \Delta v_{\mathrm{pos}}$ instead of v_{pos}. If the AC-side mains voltages are measured for generation of v_{pos}, no information about Δv_{pos} is available for the FCC system and hence has to be fully compensated by the controller. Δv_{pos} can furthermore be written as $\Delta v_{\mathrm{pos}} = V_{\mathrm{o,idle}}/2$ for steady state operation. Recalculating the permanent control deviation for disturbed input conditions,

$$\lim_{\mathrm{s}\to 0} \mathrm{s}\cdot e(\mathrm{s}) = \lim_{\mathrm{s}\to 0} \mathrm{s}\,\frac{\Delta v_{\mathrm{pos}}}{V_{\mathrm{c}}}\,\frac{G(\mathrm{s})}{1+K_{\mathrm{P}}(\mathrm{s})\,G(\mathrm{s})} = \frac{1}{\omega_{\mathrm{c}} L_{\mathrm{c}}} \neq 0 \tag{6.20}$$

can then be found. The P-type controller is hence not able to compensate the occurring disturbance and the system cannot be considered to be stable anymore. A PI-type controller ($K_{\mathrm{PI}}(\mathrm{s}) = k_{\mathrm{p}} + \frac{k_{\mathrm{I}}}{\mathrm{s}}$) should therefore replace the P-type controller structure. Considering the adapted conditions (using a PI-type controller) the permanent control deviation for disturbance signals computes to be

$$\lim_{\mathrm{s}\to 0} \mathrm{s}\cdot e(\mathrm{s}) = \lim_{\mathrm{s}\to 0} \mathrm{s}\,\frac{1}{\mathrm{s}}\,\frac{\frac{1}{\mathrm{s}L_{\mathrm{c}}}}{1-\frac{V_{\mathrm{c}}}{\mathrm{s}L_{\mathrm{c}}}\left(k_{\mathrm{p}}+\frac{k_{\mathrm{I}}}{\mathrm{s}}\right)} = 0\,. \tag{6.21}$$

A PI-type controller is hence mandatory to allow the current control system compensation of occurring distortions evoked due to increased output voltage during no-load mode operation.

C. Optimization Issues

During no-load operation the passive diode bridge is alternately conducting and blocking for defined time instants. During the instants where the diodes are blocking, $i_{\mathrm{cp}} = i_{\mathrm{L}}$ and the DC-side smoothing inductance current is hence controlled via the two half-bridge current controllers. The feedforward injection inductance $L_{\mathrm{c,ff}}$ can therefore advantageously be used to increase or decrease the 300 Hz peak-to-peak current ripple of i_{L} by variations of the $L_{\mathrm{c,ff}}/L_{\mathrm{c}}$ ratio during light- or no-load operation. A reduced peak-to-peak current ripple, however, results in an increased steady state output voltage $V_{\mathrm{o,idle}}$ and reduced FCC DC-link voltage balancing capability and vice versa. During no-load operation the current controller hence allows a degree of freedom for either reduced no-load operation losses (due to reduced peak-to-peak DC-side choke) shown in **Fig. 6.12(a)** or reduced steady state output voltage $V_{\mathrm{o,idle}}$ and increased balancing capability (depicted in **Fig. 6.12(b)**). **Fig. 6.13** depicts the DC-side smoothing choke peak-to-peak current value dependency of the feedforward (fictitious, $L_{\mathrm{c,ff}}$) to real injection inductance (L_{c}) ratio. As can be seen, the characteristic can be approximated well

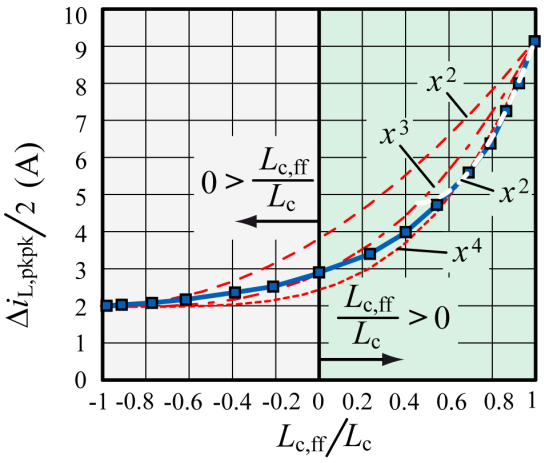


Fig. 6.13: DC-side smoothing inductance peak current characteristic for modified values of the feedforward to implemented injection inductance ratio $L_{c,ff}/L_c$ for an assumed section of $[-1 \ldots 1]$, valid during no-load operation.

by third or fourth order polynomials. If an interpolation for a specific regions is performed (as for example $0.6 < L_{c,ff}/L_c < 1$) an almost quadratic behaviour can be observed which allows an $ax^2 + b$ approximation (cf., **Fig. 6.13**, white dashed line) for this sector. Even for infinitely small negative values of the feedforward inductance, the current ripple never appears to be 0 A as it is still partly defined due to the AC-side mains voltages if the passive bridge is conducting. The minimum value of the achievable low-frequency peak-to-peak current is hence dependent on the blocking time instants evoked due to the FCC.

6.2 Unbalanced Mains Voltages Operating Conditions

According to the EN 50160 standard, it is stated that supply voltage variations should not exceed ±10 % of the nominal voltage $V_{N,rms}$ (periods with interruptions excluded).
In the following, the impact of unbalanced mains voltages on a hybrid three-phase rectifier systems is hence discussed and analyzed and is exemplarily demonstrated by the means of simulation and experimental results of THI rectifier utilizing a FCC.

6.2.1 Output Voltage

In general, time instants where a passive three-phase rectifier is initiating the commutation process between two different phases is defined by $\frac{2\cdot(k-1)\pi}{3}$ $(k \in \mathbb{Z})$, if well-balanced mains voltages are assumed. Due to the fact, that these time instants are dependent on the mains voltage situation, they may easily computed

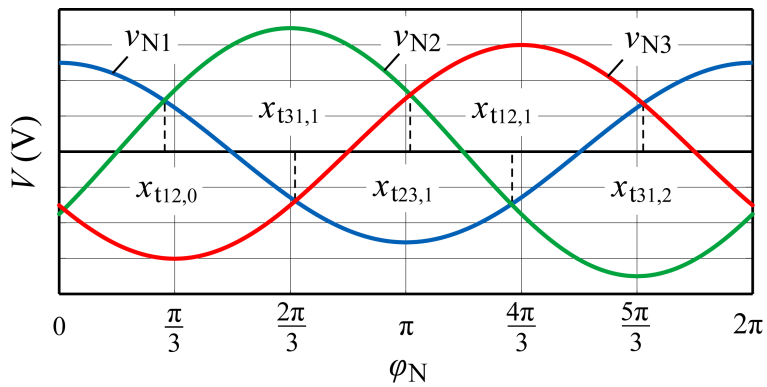


Fig. 6.14: Unsymmetrical mains voltages v_{N1}-v_{N3} applying $V_{N1,rms} \neq V_{N2,rms} \neq V_{N3,rms}$. Calculated new time instants $x_{tij,k}$ are deviating from the typically assumed instants $\frac{2\cdot(k-1)\pi}{3}$ considering balanced mains voltage condition.

to

$$x_{t12,k} = \pi \cdot k + \arctan\left(\frac{1}{\sqrt{3}}\,\frac{2\hat{V}_{N1} + \hat{V}_{N2}}{\hat{V}_{N2}}\right) \tag{6.22}$$

$$x_{t23,k} = \pi \cdot k + \arctan\left(\frac{1}{\sqrt{3}}\,\frac{\hat{V}_{N2} - \hat{V}_{N3}}{\hat{V}_{N2} + \hat{V}_{N3}}\right) \tag{6.23}$$

$$x_{t31,k} = \pi \cdot k - \arctan\left(\frac{1}{\sqrt{3}}\,\frac{2\hat{V}_{N1} + \hat{V}_{N3}}{\hat{V}_{N3}}\right) \tag{6.24}$$

with $k \in \mathbb{Z}$ if imbalance in grid voltages is expected. x_{tij} denotes the respective time instant where $v_{Ni}(\varphi_N) = v_{Nj}(\varphi_N)$ for $i \neq j$.[2] **Fig. 6.14** depicts the discussed unsymmetrical mains situation and shows the computed commutation time instants which are slightly differing from the typical well-known 60° transitions. The given equations are furthermore valid for perfectly aligned mains $V_{N1,rms} = V_{N2,rms} = V_{N3,rms} = V_{N,rms}$ which can be demonstrated by

$$x_{t12,0} = \pi \cdot 0 + \arctan\left(\frac{1}{\sqrt{3}}\,\frac{2\hat{V}_{N1} + \hat{V}_{N2}}{\hat{V}_{N2}}\right) = \arctan\left(\sqrt{3}\right) = \frac{\pi}{3}. \tag{6.25}$$

Calculated time instants ($x_{t31,0}$, $x_{t12,0}\ldots$) now can be used to analytically evaluate the emerging DC-output voltage V_o for unbalanced mains voltages.

$$V_o = \frac{1}{\pi}\left(\int_{x_{t31,0}}^{x_{t12,0}} v_{N1}(\varphi_N)\,\mathrm{d}\varphi_N + \int_{x_{t12,0}}^{x_{t23,1}} v_{N2}(\varphi_N)\,\mathrm{d}\varphi_N + \int_{x_{t23,1}}^{x_{t31,2}} v_{N3}(\varphi_N)\,\mathrm{d}\varphi_N\right) \tag{6.26}$$

Considering a number of addition theorems like

- $\sin(-\varphi_N) = -\sin(\varphi_N)$
- $\sin(\arctan(\varphi_N)) = \frac{\varphi_N}{\sqrt{1+\varphi_N^2}}$
- $\cos(\arctan(\varphi_N)) = \frac{1}{\sqrt{1+\varphi_N^2}}$

[2] $i = 1, 2, 3$, $j = 1, 2, 3$. Both indices i and j indicate one of the three mains phase numbers.

- $\sin(\varphi_x - \varphi_y) = \sin(\varphi_x)\cos(\varphi_y) - \cos(\varphi_x)\sin(\varphi_y)$

the averaged output voltage V_o yields

$$\begin{aligned} V_o = \frac{1}{\pi}\Big(&\sqrt{\hat{V}_{N1}^2 + \hat{V}_{N1}\hat{V}_{N2} + \hat{V}_{N2}^2} + \dots \\ &\dots + \sqrt{\hat{V}_{N1}^2 + \hat{V}_{N1}\hat{V}_{N3} + \hat{V}_{N3}^2} + \dots \\ &\dots + \sqrt{\hat{V}_{N2}^2 + \hat{V}_{N2}\hat{V}_{N3} + \hat{V}_{N3}^2}\Big). \end{aligned} \tag{6.27}$$

Expecting a supply voltage imbalance of 2 %, the averaged output voltage varies by approximately 0.4 % (< 2 V). In order to demonstrate general validity of **Eq. 6.27**, balanced mains voltages are assumed ($V_{N1,rms} = V_{N2,rms} = V_{N3,rms} = V_{N,rms}$) and result in the well known

$$\begin{aligned} V_{o,unbal} = \frac{1}{\pi}\Big(&\sqrt{\hat{V}_N^2 + \hat{V}_N\hat{V}_N + \hat{V}_N^2} + \dots \\ &\dots + \sqrt{\hat{V}_N^2 + \hat{V}_N\hat{V}_N + \hat{V}_N^2} + \dots \\ &\dots + \sqrt{\hat{V}_N^2 + \hat{V}_N\hat{V}_N + \hat{V}_N^2}\Big) = \frac{3\sqrt{3}\hat{V}_N}{\pi}. \end{aligned} \tag{6.28}$$

6.2.2 DC-Side Inductor Current

The analytically gained knowledge acquired due to mathematical investigations of V_o for unbalanced mains voltage conditions can be exploited to evaluate the "sector by sector" characteristics of the DC-side smoothing inductance current (i_L). It must be noted that the calculated inductor current shows $\frac{\pi}{3}$-periodic current characteristics for balanced input voltage waveforms. The DC-side smoothing choke current for unbalanced mains voltage conditions, obviously results in π-periodicity (cf., **Fig. 6.15**). The inductor current ($i_{L,unbal}$) is given by

$$\begin{aligned} i_{L,unbal}(\varphi_N) = I_{o,unbal} &- \frac{V_o}{\omega_N L_{DC}}(\varphi_N - x_{t23,0}) + \dots \\ &\dots + \frac{2\hat{V}_{N1} + \hat{V}_{N3}}{2\omega_N L_{DC}}(\sin(\varphi_N) - \sin(x_{t23,0})) - \dots \\ &\dots - \frac{\sqrt{3}\hat{V}_{N3}}{2\omega_N L_{DC}}(\cos(\varphi_N) - \cos(x_{t23,0})) \end{aligned} \tag{6.29}$$

for 10 kW output power, a sector of $\varphi_N \in [x_{t23,0} \dots x_{t12,0}]$ and an averaged output voltage $V_{o,unbal}$ as derived in **Eq. 6.27**. $I_{o,unbal}$ denotes the adapted constant output current

$$I_{o,unbal} = \frac{P_o}{V_{o,unbal}}. \tag{6.30}$$

For the given equation the output load has been considered to be highly inductive ($I_o \approx$ const) and the output capacitor $C_o \to \infty$. The output voltage ripple hence is assumed to be 0 V. **Fig. 6.15** illustrates the DC-side inductor current of a hybrid

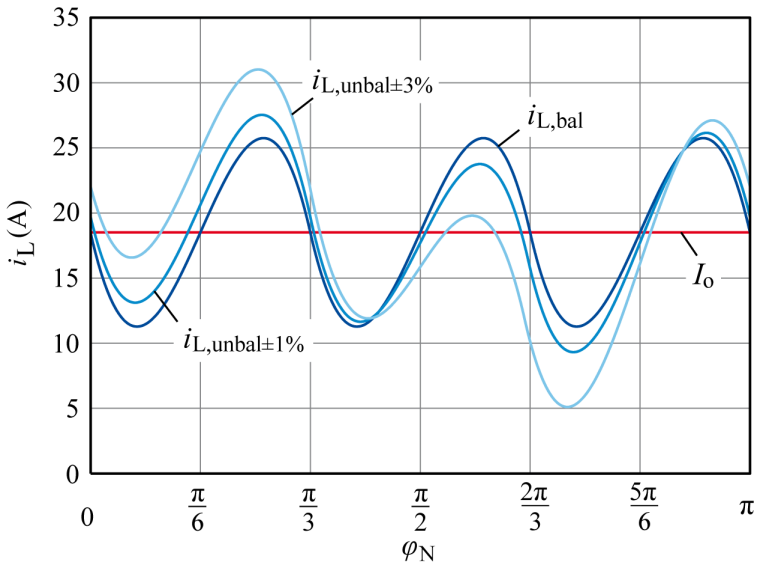


Fig. 6.15: DC-side smoothing inductor current i_L for balanced mains and grid voltage deviations of $\pm 1\,\%$ and $\pm 3\,\%$ ($i_{L,bal}$, $i_{L,unbal\pm 1\,\%}$ and $i_{L,unbal\pm 3\,\%}$, respectively) considering a DC-side smoothing inductance L_{DC} of 2.25 mH, an output power of 10 kW and a constant output voltage V_o.

rectifier system employing third harmonic injection for unbalanced and balanced mains voltages and a nominal output power of 10 kW. Three different mains voltage conditions are considered:

- the perfectly balanced voltage situation,
- a deviation of mains peak voltages of $\pm 1\,\%$
- and a deviation of mains peak voltages of $\pm 3\,\%$.

As can be seen in **Fig. 6.15**, the peak-to-peak current ripple of i_L is strongly increasing, even for small mains voltage imbalance errors. Considering symmetric mains voltages a peak-to-peak current ripple of

$$\Delta I_{L,pkpk} = 14.4\,\mathrm{A} \tag{6.31}$$

appears for $P_o = 10\,\mathrm{kW}$, $L_{DC} = 2.25\,\mathrm{mH}$, $V_{N,rms} = 230\,\mathrm{V}$. If unbalanced mains conditions are expected ($V_{N,rms} \pm 1\%$ and $V_{N,rms} \pm 3\%$) 300 Hz DC-side choke peak-to-peak current ripples compute to

$$\Delta I_{L,pkpk,unbal\pm 1\,\%} = 18.2\,\mathrm{A} \tag{6.32}$$

and

$$\Delta I_{L,pkpk,unbal\pm 3\,\%} = 26.4\,\mathrm{A}, \tag{6.33}$$

respectively. For a grid voltage deviation of $\pm 1\,\%$ and $\pm 3\,\%$, i_L shows an augmented peak-to-peak current ripple of 26 % and 83 %, respectively. These results are assuming an infinitely high output capacitor ($C_o \to \infty$) which results in a

purely DC voltage component of v_o ($= V_o$). If real capacitor values of C_o are supposed, the emerging low harmonic output voltage ripple is inconveniently affecting the DC-side inductor current ripple. $I_{L,pkpk}$ can be presumed to be even higher than the previously computed results.
Summarizing the conditions, unbalanced mains voltages lead to a superimposed 100 Hz voltage component in the DC-side output filter of the passive rectifier circuit resulting in pronounced peak-to-peak current ripple is the DC-side smoothing inductor current i_L and consequently augmented low harmonic AC voltage components of the rectifiers output capacitor (C_o) even for rather low mains voltage imbalance.

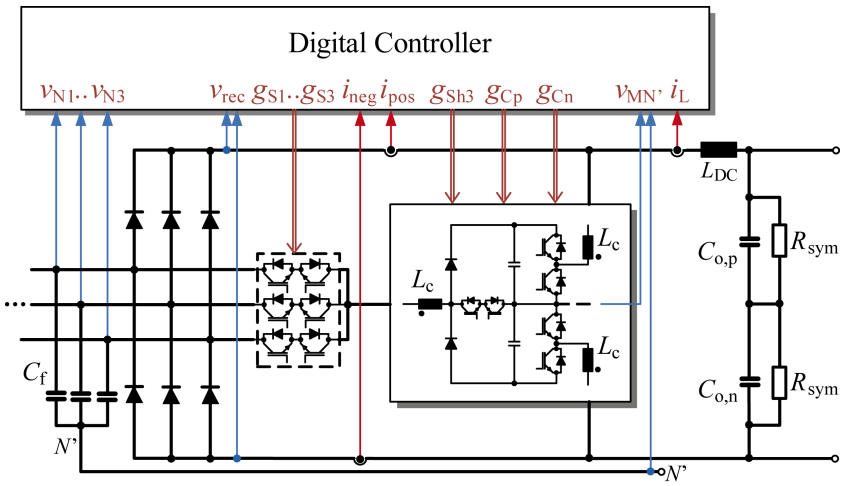
6.2.3 Effects on Active Current Injection Cell

The optional active rectifier – which allows the extension of a passive rectifier to a low harmonic input stage – is basically injecting some amount of current into the positive and negative busbar of the passive rectifier which guarantees sinusoidal wave shapes i_{pos} and i_{neg} (cf., **Fig. 5.27**). The 300 Hz (and evoked 100 Hz) current component of i_L has hence to be compensated by the equipped injection circuit. A simulation model hence has been implemented (cf., **Fig. 6.16(a)**) in order to demonstrate the effects of imbalance in grid voltages on the equipped active enhancement. Considered passive components for the 10 kW/10 kHz simulation model are as follows:

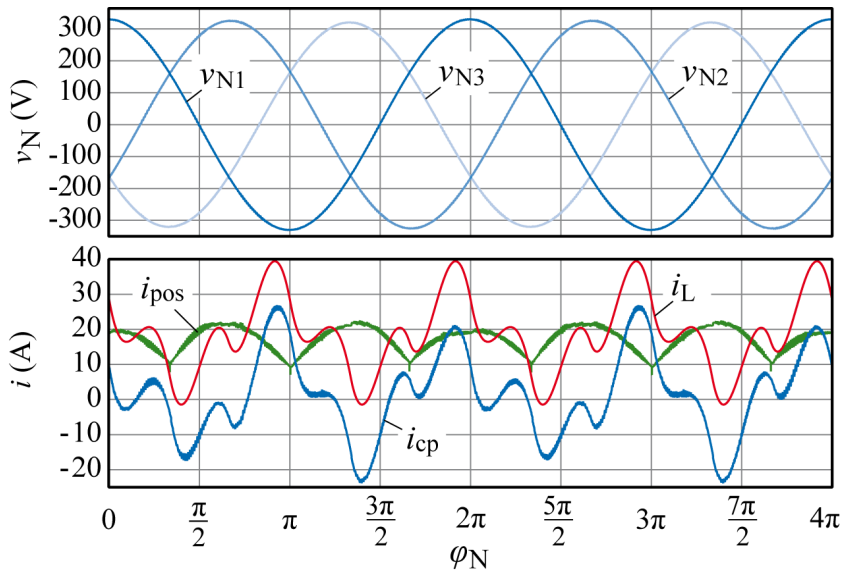
- Current Injection Circuit - FCC
- $L_c = 1.8\,\text{mH}$
- $C_f = 6.8\,\mu\text{F}$
- $L_{DC} = 2.25\,\text{mH}$
- $C_{o,p} = C_{o,n} = 2.2\,\text{mF}$
- $R_{sym} = 47\,\text{k}\Omega$.

Current and voltage controllers of converter topologies are implemented as described in [23] and [25]. Imbalance in mains voltages is defined by $V_{N,rms} \pm 3\%$. **Fig. 6.16(b)** depicts simulation results of injection current i_{cp}, DC-side smoothing inductance current i_L and positive busbar current i_{pos}. As can be seen, i_L shows the previously discussed increased peak-to-peak current ripple which is approximately 41 A for the given configuration. For both, the balanced and slightly unbalanced grid voltage condition, sinusoidal input peak currents ($\hat{I}_N$) are supposed to be $\approx 20\,\text{A}$ for 10 kW output power considering proper current control of the rectifier. For the well-balanced condition this results in an injection current i_{cp} with the following characteristics:

- peak current $\hat{I}_{cp} \approx 12\,\text{A}$
- peak-to-peak current $\Delta I_{cp} \approx 20\,\text{A}$
- rms current $I_{cp,rms} \approx 6\,\text{A}$



(a)



(b)

Fig. 6.16: (a) Implemented simulation model of hybrid rectifier topology in order to discuss effects of unbalanced mains voltages on current injection devices employing third harmonic injection principle. (b) Simulation results of a 10 kW/10 kHz hybrid rectifier utilizing a FCC. Unbalance of mains voltages is defined by $V_{N,rms} \pm 3\%$. Output capacitor is defined by $C_{o,p} = C_{o,n} = 2.2\,\text{mF}$.

- averaged current $I_{cp,avg} \approx 1.6\,\text{A}$.

An input voltage unbalance of $V_{N,rms} \pm 3\%$ is, however, causing a tremendously impaired injection current i_{cp} (and i_{cn}) characteristic which is now defined by

- peak current $\hat{I}_{cp} \approx 26\,\text{A}$ (+116%)
- peak-to-peak current $\Delta I_{cp} \approx 50\,\text{A}$ (+150%)
- rms current $I_{cp,rms} \approx 12\,\text{A}$ (+100%)
- averaged current $I_{cp,avg} \approx 1.6\,\text{A}$. ($\approx +0\%$)

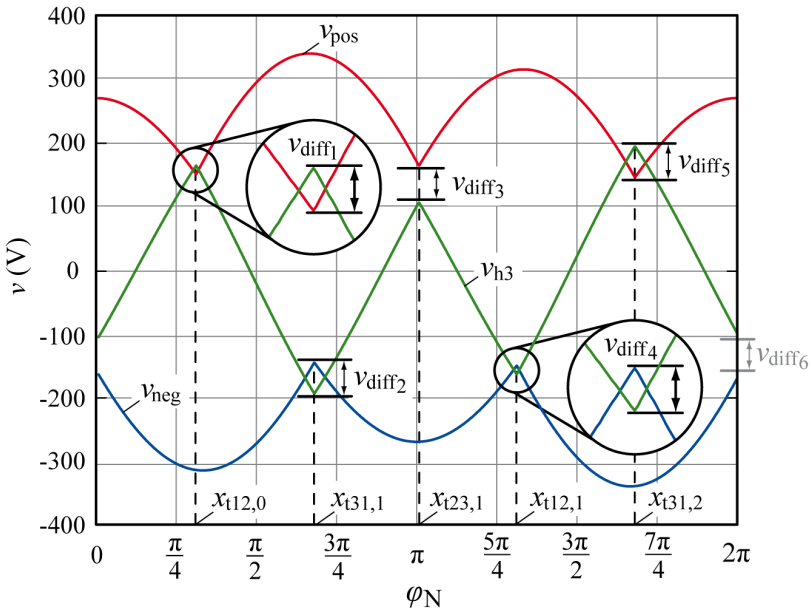


Fig. 6.17: Calculated waveforms of positive and negative output voltage v_{pos} and v_{neg} of the hybrid rectifier and third harmonic voltage v_{h3}. $x_{tij,k}$ denotes adapted commutation time instants for unbalanced mains voltage condition. v_{diff} indicates multiple transition mismatches due to unbalanced mains voltages.

The modified current characteristics, furthermore, result in diminished overall efficiency η_{sys} of the total system due to increased switching and conduction losses of active components and additional resistive losses of passive components. Moreover, increased iron losses of DC-side smoothing and injection inductors can be expected.

6.2.4 Effects of Heavily Unbalanced Mains Voltages on THD of Input Currents

Unbalanced mains voltages as described before, can highly affect DC-side current and voltage waveforms and may even inflict design considerations of the hybrid system. Depending on the implemented control method of the rectifier, an imbalance in grid voltages will furthermore worsen total harmonic distortions (THD) of input currents ($i_{N,i}$). In order to highlight the impact on input currents, heavily unbalanced mains ($\pm 20\,\%$) voltages now are assumed for illustration.
Using the adapted commutation time instants for unbalanced mains voltage conditions $x_{tij,k}$ (according to **Eq. 6.24**), positive and negative output voltage waveforms v_{pos} and v_{neg} can be easily determined and are illustrated in **Fig. 6.17**. The third harmonic voltage v_{h3} is defined by the rectifiers output voltage situation of v_{pos} and v_{neg} and hence given by

$$v_{h3} = -v_{pos} - v_{neg} \,. \tag{6.34}$$

As shown in **Fig. 6.17**, signal waveforms of v_{h3} and v_{pos} (and v_{h3} and v_{neg}) are not matching anymore for those time instants where the voltage transition of two

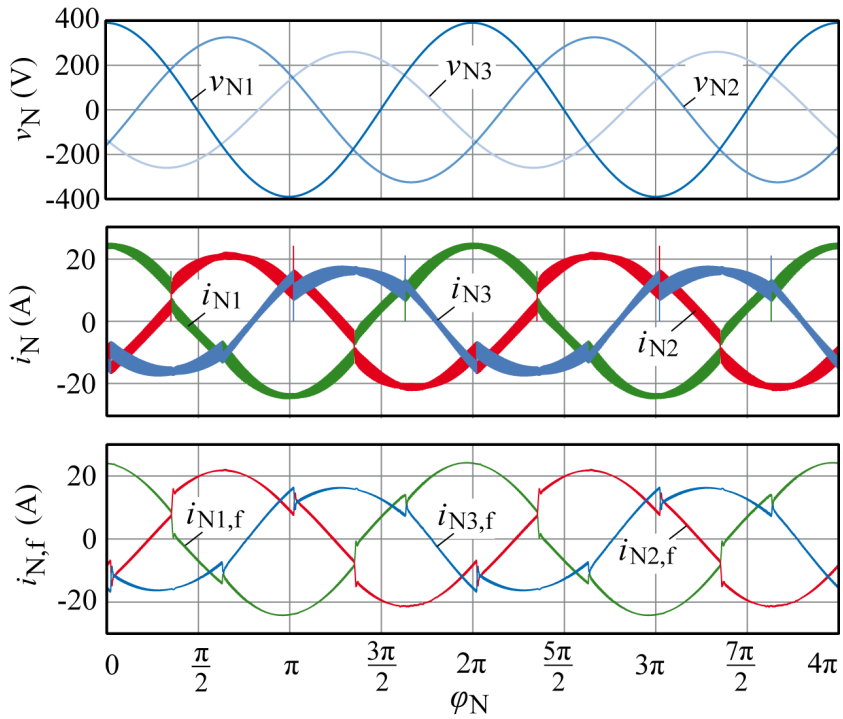


Fig. 6.18: Simulation results of a 10 kW/10 kHz hybrid rectifier utilizing a FCC for heavily unbalanced mains voltages ($V_{N,rms} \pm 20\%$). Filtered AC input currents $i_{Ni,f}$ result in $THD_{i,1} = 10.2\,\%$, $THD_{i,2} = 15.5\,\%$ and $THD_{i,1} = 12.86\,\%$

different phases of the passive diode bridge takes place. This observed deflection is defined as v_{diff} (cf., zoomed regions of **Fig. 6.17**) and occurs at the respective current commutation time instant $x_{tij,k}$. The first voltage mismatch $v_{diff,1}$ can be assessed by

$$v_{diff,1} = v_{pos}\left(x_{t12,0}\right) - v_{h3}\left(x_{t12,0}\right) \tag{6.35}$$

with $v_{h3}\left(x_{t12,0}\right) = -v_{pos}\left(x_{t12,0}\right) - v_{neg}\left(x_{t12,0}\right)$. $v_{diff,1}$ can be computed to

$$v_{diff,1} = \frac{\sqrt{3}}{2}\frac{2\hat{V}_{N1}\hat{V}_{N2} - \hat{V}_{N1}\hat{V}_{N3} - \hat{V}_{N2}\hat{V}_{N3}}{\sqrt{\hat{V}_{N1}^2 + \hat{V}_{N1}\hat{V}_{N2} + \hat{V}_{N2}^2}}\,. \tag{6.36}$$

All remaining voltage deviations $v_{diff,2} - v_{diff,6}$ can be calculated similarly under consideration of **Eq. 6.35**. It has to be noted that $v_{diff,1} = v_{diff,4}$, $v_{diff,2} = v_{diff,5}$ and $v_{diff,3} = v_{diff,6}$.

These voltage deviations are of major importance for generation of current and voltage controller reference signals of the active current injection cell. In conventional active rectifier circuits [18], the reference currents are often generated by a superimposed voltage controller which indirectly determines the power demand by measuring the voltage of the DC-link capacitor. The output voltage of the proposed rectifier system is not controlled, but is dependent on the mains and load situation and is even not measured. The power transferred from the mains to the output of the rectifier is not dependent on the current shape and can be

determined by measurement in both operating modes, operating in diode mode as well as for active current shaping using the FCC. The power demand can be determined using the mains voltages ($v_{\mathrm{N1}}, v_{\mathrm{N2}}, v_{\mathrm{N3}}$) and DC-side current i_{L}

$$p(\varphi_{\mathrm{N}}) = (v_{\mathrm{pos}}(\varphi_{\mathrm{N}}) - v_{\mathrm{neg}}(\varphi_{\mathrm{N}}))\, i_{\mathrm{L}}(\varphi_{\mathrm{N}}) \ . \tag{6.37}$$

The equivalent conductance g_{e}^* can then be calculated to

$$g_{\mathrm{e}}^* = \frac{P_{\mathrm{in}}}{V_{\mathrm{N1,rms}}^2 + V_{\mathrm{N2,rms}}^2 + V_{\mathrm{N3,rms}}^2} \ . \tag{6.38}$$

P_{in} is the low-pass filtered constant value of the instantaneous power demand $p(\varphi_{\mathrm{N}})$. g_{e}^* is finally multiplied with the (calculated) voltages v_{pos} and v_{neg} in order to derive the reference currents i_{pos}^* ($= g_{\mathrm{e}}^* v_{\mathrm{pos}}$) and i_{neg}^*. As

$$i_{\mathrm{pos}} + i_{\mathrm{h3}} + i_{\mathrm{neg}} = 0 \tag{6.39}$$

the same mismatch appearing for DC-side voltages v_{pos}, v_{h3} and v_{neg} hence is also valid for DC-side currents i_{pos}, i_{h3} and i_{neg}. The input currents are supposed to show small current steps during every current transition of the input side of the system. Simulation results of the discussed issues are illustrated in **Fig. 6.18** for heavily (20 %) unbalanced mains voltages of $V_{\mathrm{N1,rms}} = 276\,\mathrm{V}$, $V_{\mathrm{N2,rms}} = 230\,\mathrm{V}$ and $V_{\mathrm{N3,rms}} = 184\,\mathrm{V}$. Filtered AC input currents $i_{\mathrm{Ni,f}}$ finally result in a total harmonic distortion of $\mathrm{THD}_{\mathrm{i,1}} = 10.2\,\%$, $\mathrm{THD}_{\mathrm{i,2}} = 15.5\,\%$ and $\mathrm{THD}_{\mathrm{i,1}} = 12.86\,\%$ which is significantly higher than the officially allowed 5 % according to IEEE standards.

6.3 Input Filter Design

In this section an input filter is designed (for a 10 kW/10 kHz rectifier) for an input mains inductance $L_{\mathrm{N}} = 60\,\mu\mathrm{H}$ (based on the derived equations of chapter 4). Such a design for a simple C_{f} input filter results in a capacitance value of $C_{\mathrm{F}} = 6.8\,\mu\mathrm{F}$ a quantity value $n_{\mathrm{S}} = 1$ and a snubber resistance of $2.8\,\Omega$ (cf., **Fig. 4.6(top, left)**). The effect on the current filter characteristics with variations of C_{f} and L_{N} are depicted in **Fig. 6.19(a-d)**. If no further information about the grid is available the filter should hence consider a minimum cut off frequency of

$$f_{\mathrm{C}} < \frac{f_{\mathrm{S}}}{5 \ldots 10} \tag{6.40}$$

to allow sufficient damping. In this specific case at hand, a cut off frequency of $f_{\mathrm{S}}/2$ is also applicable due to the relatively large injection inductors (and hence rather small current ripple with switching frequency) $L_{\mathrm{c}} \approx 3\,\mathrm{mH}$. An additional series connected inductance could make the input filter much more robust and independent from the mains impedance value.

Finally, the effects of the input filter on the power factor of the total system have to be mentioned. One of the main objectives of the rectifier circuit is to achieve unity

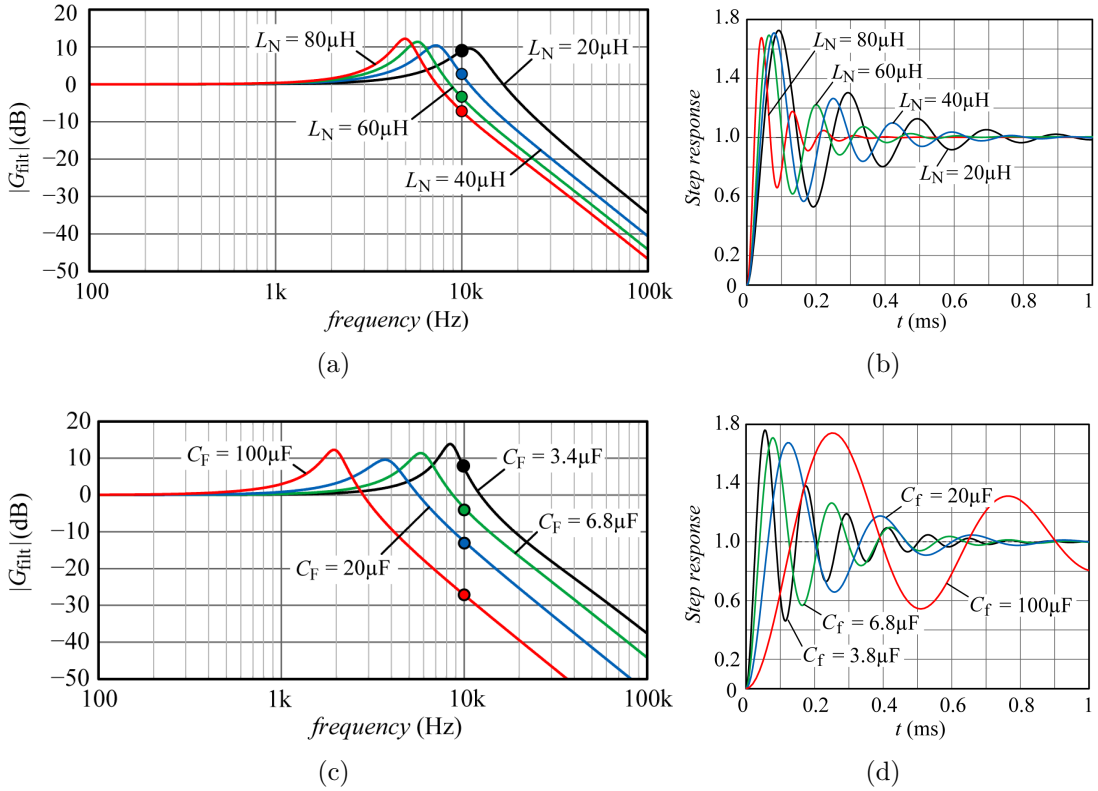


Fig. 6.19: (a) Filter transferfunction including RC snubber network for different values of L_N ($C_S = C_f = 6.8\,\mu F$, $R_S = 2.8\,\Omega$) (b) and appropriate step response and (c) different values of $C_f = C_S$ ($L_N = 60\,\mu H$, $R_S = 2.8\,\Omega$) and (d) and appropriate step response.

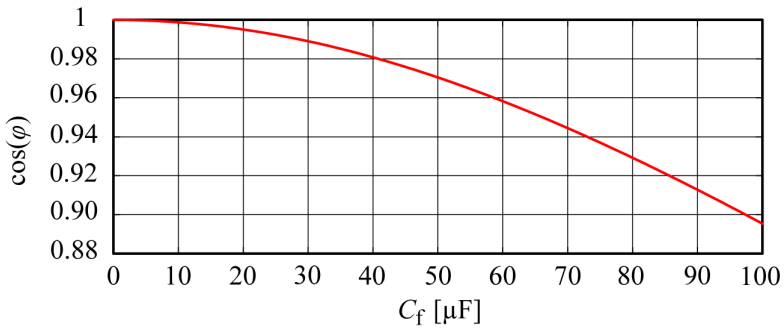


Fig. 6.20: Expected minimum phase shift between fundamental line voltage and mains input currents according to a LC input filter stage.

power factor λ. As the B6 rectifier can only achieve a maximum power factor of approximately 0.95, an active solution should be characterized by at least $\lambda > 0.99$ (for nominal load). Due to the filter capacitor, a phase shift between fundamental input current and voltage however is unavoidable. Even if ideal measurement circuits and current controllers are assumed, the maximum power factor of the system is still limited to:

$$\cos(\Phi) = \cos\left(\arctan\left(\frac{2\pi f_N \hat{U}_N}{\hat{I}_N} C_f\right)\right), \tag{6.41}$$

TABLE 6.1: Design Specifications of the Built Three-Phase Rectifier using a FCC.

Mains voltage:	$V_{\mathrm{LL}} = 400\,\mathrm{V_{rms}}$
Mains frequency:	$f_{\mathrm{N}} = 50\,\mathrm{Hz}$
Switching frequency:	$f_{\mathrm{s}} = 10\,\mathrm{kHz}$.
FCC DC-link voltage:	$V_{\mathrm{cp}} = V_{\mathrm{cn}} = 400\,\mathrm{V}$
Output power:	$P_{\mathrm{o}} = 10\,\mathrm{kW}$

TABLE 6.2: Power Devices Selected for Implementation of the FCC Prototype.

$S_{\mathrm{ia,b}}$	1200 V/40 A IGBT, IKW40T120, Infineon
$S_{\mathrm{c}\frac{\mathrm{p}}{\mathrm{n}}\pm}$	600 V/20 A IGBT, IKW20N60H3, Infineon
$D_{\mathrm{h3}\pm}$	1200 V/15 A, STTH1512W, ST-Microelectronics
$C_{\mathrm{c}\frac{\mathrm{p}}{\mathrm{n}}}$	470 µF/400 V, EPCOS B43501-type
L_{cp}=L_{cn}=L_{h3}	3.2 mH, Iron core 3UI60a, N = 123 turns
C_{F}, C_{S}	6.8 µF/275 $\mathrm{V_{AC}}$, MKP X2, Arcotronics
C_{o}	2.2 mF/400 V, Felsic CO 39 A728848
L_{DC}	2.25 mH, Iron core 2 x UI60a
$D_1 - D_6$	35 A/1600 V, 36MT160, Vishay

where Φ denotes the fundamental current-to-voltage displacement angle. This results in a minimal phase shift between sinusoidal line voltage and input currents of 1.94° (cf., **Fig. 6.20**) for a filter capacitor of 6.8 µF. Obviously a power factor of $\lambda > 0.999$ can be guaranteed if a filter capacitor underlies the condition of $C_{\mathrm{f}} < 8.98\,\mu\mathrm{F}$ (for $L_{\mathrm{N}} = 60\,\mu\mathrm{H}$).

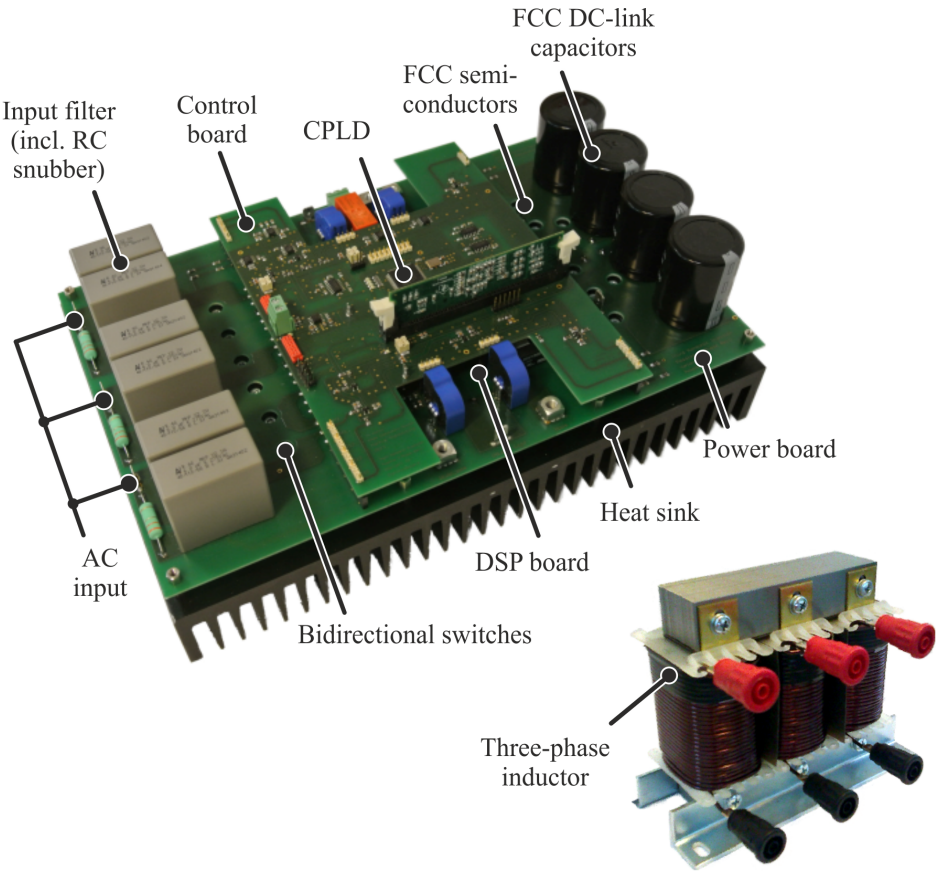
6.4 Laboratory Prototype

Detailed specifications of the active system (shown in **Fig. 6.21(a)**), applied power semiconductor devices and passive components are given in **TABLE 6.1** and **TABLE 6.2**.

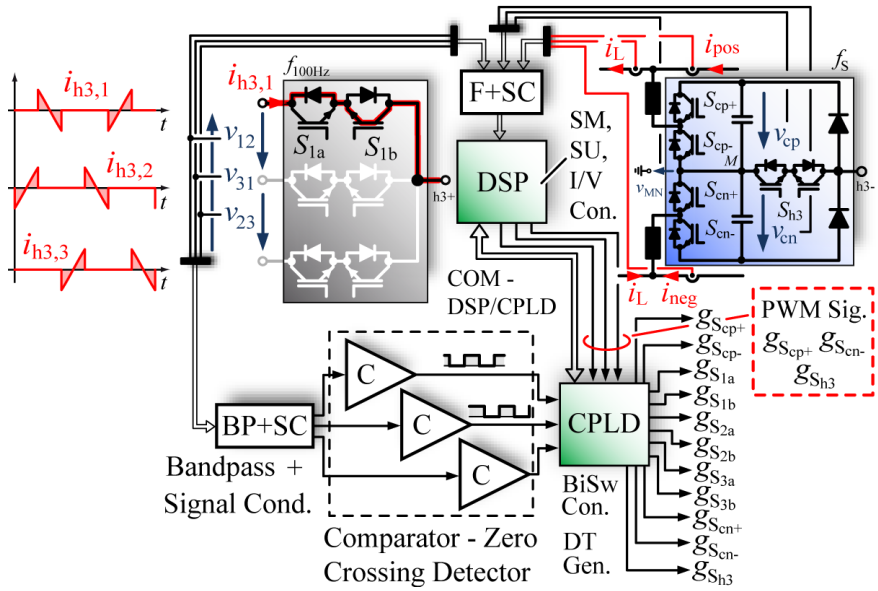
The current injection laboratory prototype mainly consists of two different boards – controller and power board. The controller board contains measurement circuits, auxiliary power supply, DSP control unit (TI 320F2808) and additional hardware as e.g. zero crossing detection of mains line-to-line voltages and bidirectional switch controller (Lattice CPLD – MachXO 2280).

The power board includes main power components as heatsink, IGBTs, gate drives, input filter, current sensors, electrolytic capacitors and further electric circuits which are required for proper start-up operation of the system.

The system has been designed for 400 $\mathrm{V_{LL}}$/50 Hz mains voltages, which results in



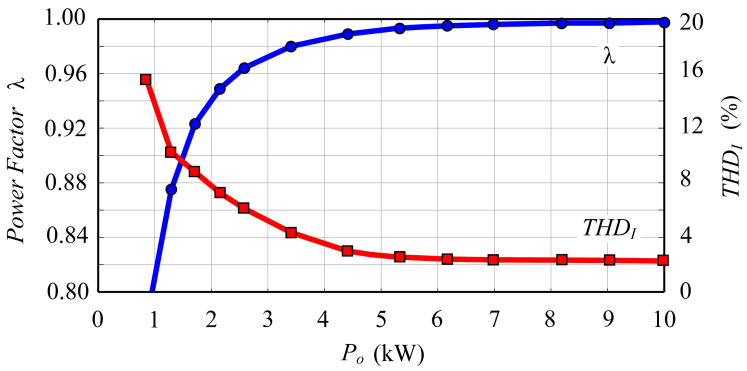
(a)



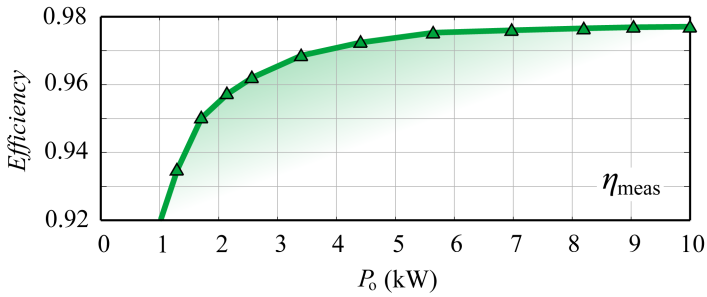
(b)

Fig. 6.21: (a) Constructed 10 kW laboratory prototype of the FCC and used three-phase choke. Dimensions FCC: 300 mm x 200 mm x 97 mm and three-phase choke 120 mm x 50 mm x 100 mm. (b) Simplified schematic of implemented hardware prototype concept of the FCC rectifier.

400 V DC voltage levels for the injection cell capacitors C_{cp} and C_{cn} (if a modulation index $M = 0.8125 = \hat{V}_{\mathrm{N}}/V_{\mathrm{c}\frac{\mathrm{p}}{\mathrm{n}}}$ is assumed).
The relatively low DC voltage of the switching cell furthermore would allows the implementation of GaN or SiC-MOSFETs which are recently available for blocking voltages > 400 V (e.g. ROHMs SCT2120AF, CREEs C3M0065090J, or GaN Systems' GS66508T). This offers an operation with increased switching frequency at lower switching losses compared to a conventional IGBT. The SiC-MOSFET, furthermore, shows ohmic characteristics which will result in improved conduction losses (compared to an Si-IGBT) in the partial load region. The implementation of a SiC-MOSFET can hence lead to a smaller and less expensive cooling system/volume. The bidirectional switches can also advantageously be implemented by e.g. 900 V or 1200 V SiC-MOSFETs in order to reduce losses of the current injection stage (at higher costs). For proper operation, 6 voltage (line-to-line voltages or $v_{\mathrm{N1-3}}$, v_{cp}, v_{cn} and v_{MN}) and 3 current sensors (i_{pos}, i_{neg} and i_{L}) are required. Also a 5 voltage sensor solution would be possible if the third mains phase is calculated by the already measured two remaining ones. A simplified schematic of the implemented concept of the FCC rectifier is depicted in **Fig. 6.21(b)**. It is shown that software algorithms as current/voltage controllers, start-up sequence (SU), and state machine (SM) are implemented in the digital signal processing unit. The DSP is generating the duty cycles with switching frequency for both half bridges and the three-level bridge leg. A CPLD is furthermore required, as the bidirectional switches have to initiate their commutation at the same time instant when the B6 diodes are commutating. A delay which is as small as possible is a stringent requirement in order to prevent input current distortions of the total system. The very fast updating CPLD is hence necessary which has to evaluate the proper (100 Hz) switching sequence dependent on the mains voltage situation. Moreover, the CPLD can be used to realize the required dead time of generated PWM gate signals $g_{\mathrm{cp+}}$ and $g_{\mathrm{cn+}}$ (of appropriate switches $S_{\mathrm{cp+}}$ and $S_{\mathrm{cn+}}$, respectively).
Basic measured characteristics (efficiency η_{meas}, total harmonic distortion of input currents $\mathrm{THD_i}$ and power factor λ) of the implemented rectifier system dependent on the output power are illustrated in **Fig. 6.22(a)** and **Fig. 6.22(b)**. A maximum rectifier efficiency of 97.8 % can be read at the nominal output power of 10 kW. The efficiency of the passive diode rectifier for the same load in B6 standalone operation has been obtained with 98.7 %. The assembled rectifier system furthermore achieves a $\mathrm{THD_i}$ below 5 % down to a output power of ≈ 3 kW. Also a power factor above 0.95 is measured for an output power above 2.2 kW. The constructed FCC shows a good performance even for partial load condition ($P_{\mathrm{o}} = 5\,\mathrm{kW}$) where a $\mathrm{THD_i}$ of 2.7 % and a power factor of $\lambda = 0.992$ can be measured at a good efficiency of $\eta_{\mathrm{meas}} = 97.5\,\%$. As can be observed, the efficiency is decreasing for light load operation (e.g. 95 % for an output power of 1.7 kW). This effect is mainly evoked due to the DC-side smoothing inductance current i_{L}. This current can be of negative value if the FCC is operating, as the FCC is able to process both, positive and negative current values. For light- and no-load condition, fractions of i_{L} hence occur as circulating current which has to



(a)



(b)

Fig. 6.22: (a) Measured power factor λ and input current quality ($\mathrm{THD_i}$) as a function of output power. (b) Measured efficiency η_{meas} of the laboratory prototype for a mains voltage of $V_{\mathrm{LL}} = 400\,\mathrm{V}$.

be processed by the FCC, the DC-side smoothing inductor (L_{DC}) and the DC-link voltage capacitor (C_{o}). This circular current causes additional losses compared to a passive standalone system during no-load operation (inductor losses L_{DC} and L_{c}, switching and conduction losses etc.) as described in section 6.1.2 .

The measured three mains currents $i_{\mathrm{N}i}$ and phase voltage v_{N1} are shown in **Fig. 6.23(a)** for the nominal output power $P_{\mathrm{o}} = 10\,\mathrm{kW}$. The used PI-type controller coefficients for a switching frequency of 10 kHz, double updated PWM mode and a maximum overshoot of 25 % resulted in $R(z) = (0.145 - 0.1373z^{-1})/(1 - z^{-1})$. The currents show (as already discussed) a $\mathrm{THD_i}$ of 2.3 % and a power factor of $\lambda = 0.998$ is achieved. It has to be remarked, that the mains voltages already show a $\mathrm{THD_v}$ of 1.7 %.

Fig. 6.23(b) and **Fig. 6.23(c)** illustrate measurement results of most important injection an regulated currents for 2.6 kW and 1.7 kW, respectively. Furthermore, also the output voltage v_{o} of the system is depicted. It is only characterized by the typical 100 Hz (according to slightly unbalanced input voltages in the lab) and 300 Hz spectral components (being typical for passive three-phase rectifier topologies). The output voltage (which cannot be controlled and is defined according to the mains voltage situation) for 400 $\mathrm{V_{LL}}$ input voltages has been obtained with 529 V. As already discussed, **Fig. 6.23(b)** depicts the mentioned negative values of i_{L}, which are injected by the currents i_{cp} and i_{cn}. The appearing circulating

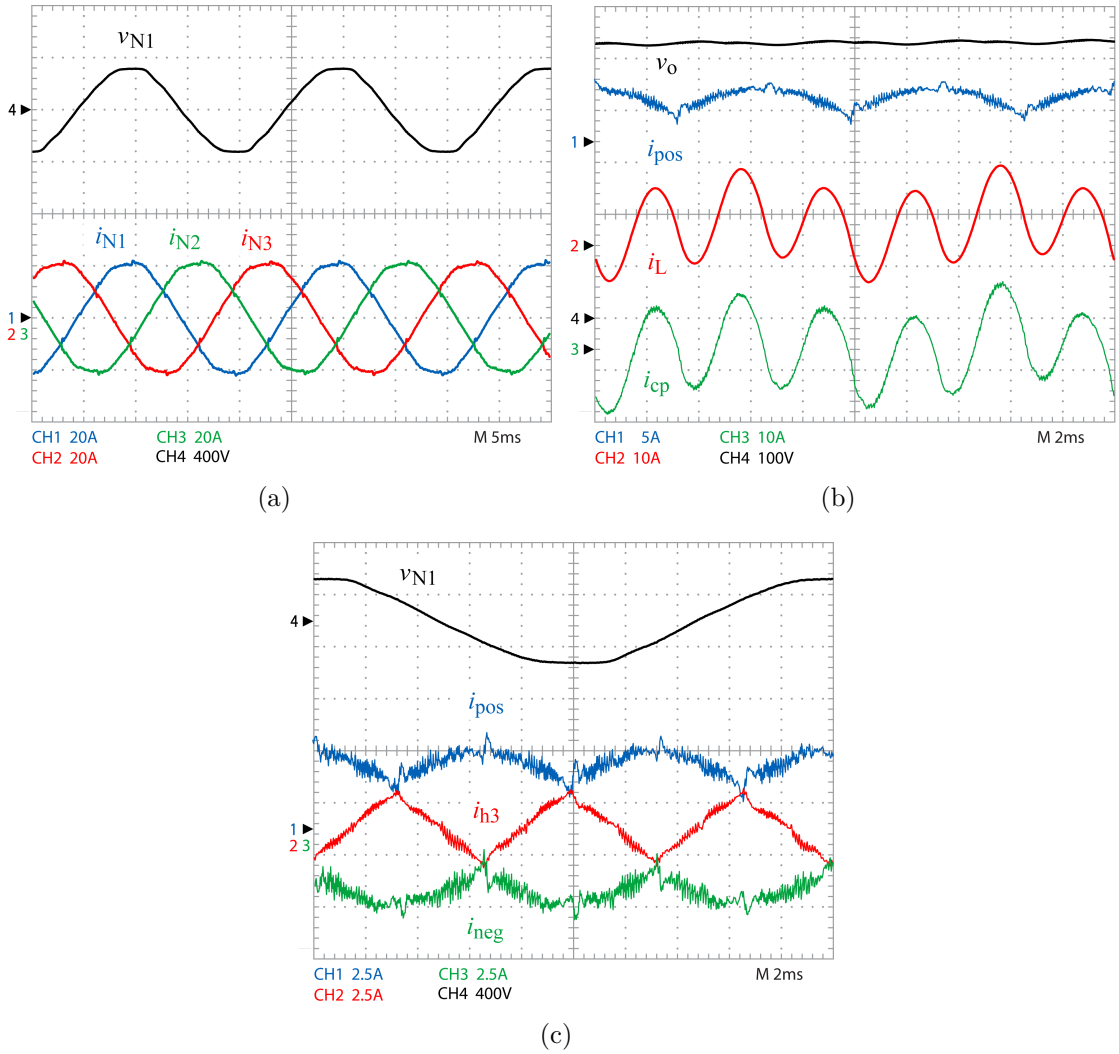


Fig. 6.23: (a) Mains currents i_{N1},i_{N2}, i_{N3} and mains voltage v_{N1} during 10 kW steady state operation ($\mathrm{THD_i} = 2.3\,\%$, $\lambda = 0.998$). (b) Positive busbar current i_{pos}, injection current i_{cp}, DC-side smoothing inductor current i_L and output voltage v_o for 2.6 kW partial load operation. (c) Positive and negative busbar current i_{pos} and i_{neg}, injection current i_{h3} and mains voltage v_{N1} for 1.7 kW partial load operation.

current then results in a reduced system efficiency at light-load and/or no-load condition.

Measurement results of the FCC voltages and input currents during the transition from B6 standalone mode to active regulated FCC operation are depicted in **Fig. 6.24(a)** and **Fig. 6.24(b)**. The transition from passive to active diode bridge mode and the appropriate charging of the FCC DC voltage from 280 V (pre-charge level) to 400 V required for proper generation of injection currents for each half bridge switching leg, are therefore illustrated. The used voltage controller gain is defined by $k_{p,v}$=0.025 (crossover frequency 17 Hz). After the DC voltages are set to the dedicated 400 V limit they are perfectly balanced (v_{cp} = 399.8 V, v_{cn} = 400.1 V). **Fig. 6.24(b)** furthermore illustrates a smooth transition of both FCC DC voltages v_{cp} and v_{cn} without any perceivable overshoot, while

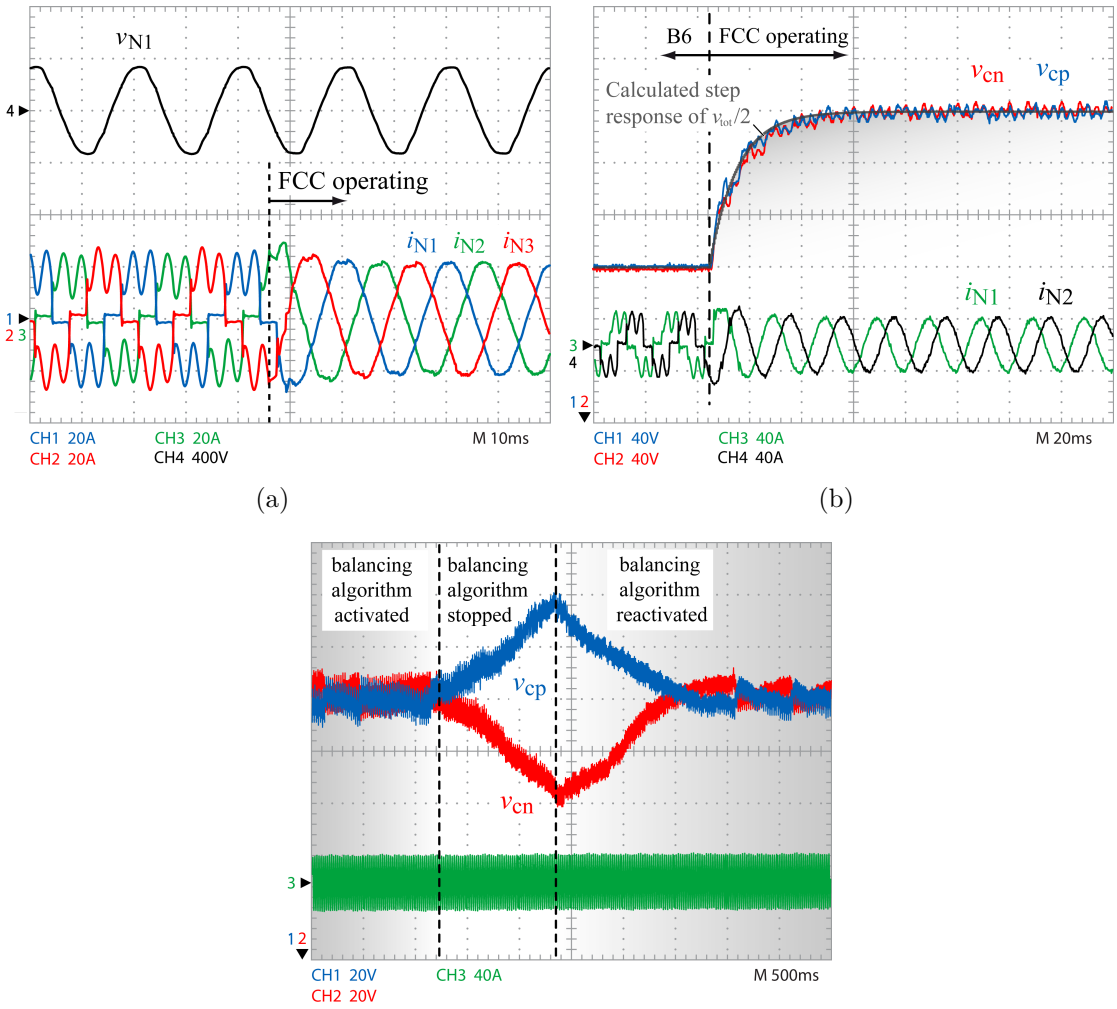


Fig. 6.24: Measurement results taken from the laboratory prototype for nominal output power (10 kW). (a) Input current waveforms for transition from passive diode mode operation (B6 standalone mode) to active current shaping (FCC activated). (b) Transition from passive diode mode operation to active current shaping using the proposed voltage control and balancing concept ($v_{\text{off}} = \pm 10\,\text{V}, v_{\text{MN}} = \pm 10\,\text{V}$). (c) Steady state operation while deactivating the voltage balancing controller and reactivating it after 1 s.

active voltage balancing is operating. The DC voltage balancing quality is verified in **Fig. 6.24(c)**. For the proposed balancing concept both DC voltages of the FCC are perfectly aligned. After deactivating (white area in **Fig. 6.24(c)**) the balancing algorithm ($v_{\text{amp}} = v_{\text{off}} = 0\,\text{V}$) v_{cp} and v_{cn} are starting to drift off the required voltage level of 400 V ($V_{\text{cp}} = 435\,\text{V}$, $V_{\text{cn}} = 365\,\text{V}$). Reactivating the balancing, the system quickly regulates the FCC DC-link voltages back to the desired 400 V voltage level.

Fig. 6.25(a-c) illustrate different load steps of the rectifier system. **Fig. 6.25(a)** depicts a full load step from nominal power (10 kW) to no-load operation. As can be seen, during no-load operation there are still input currents drawn by the sys-

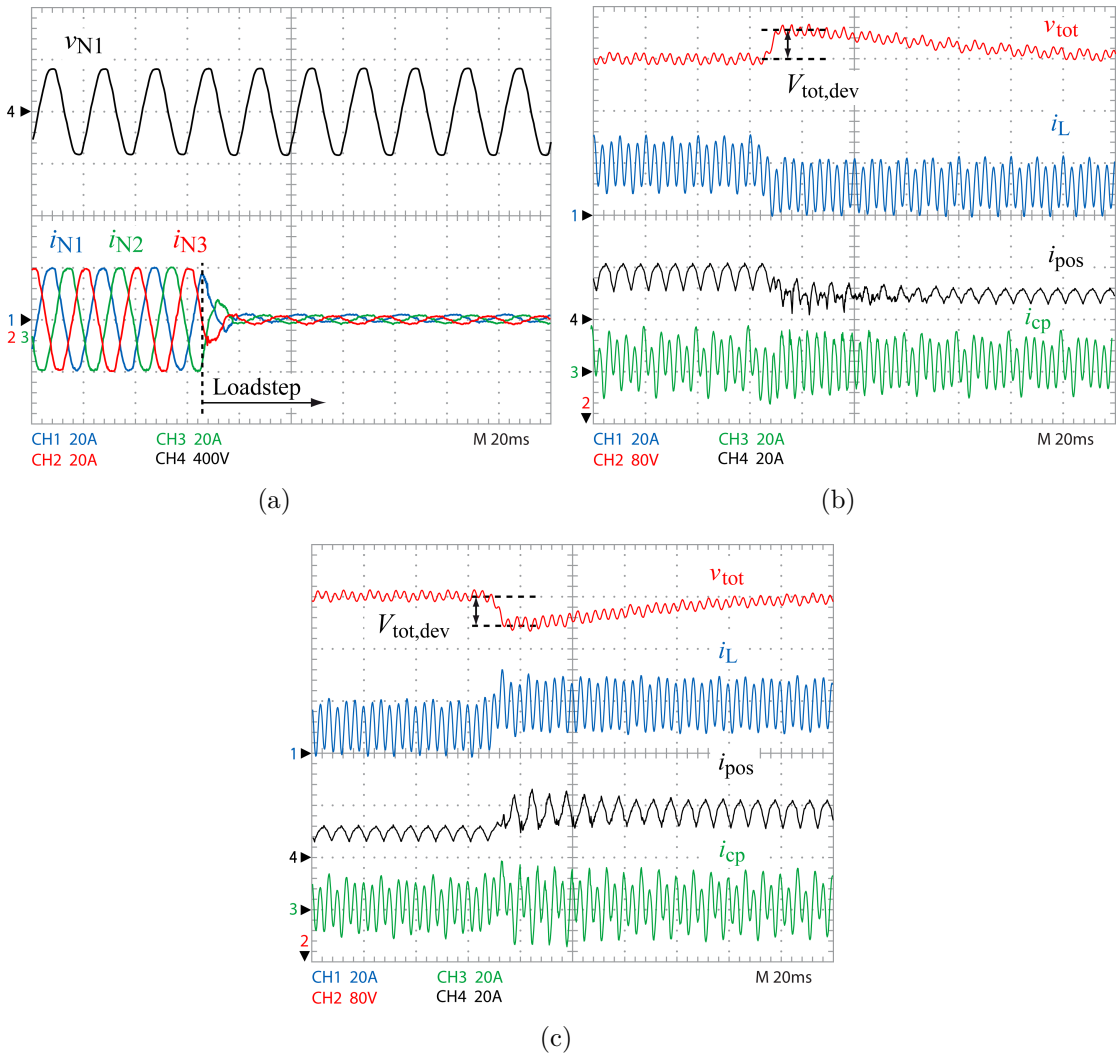


Fig. 6.25: Load step characteristics of the implemented rectifier system. (a) Input current characteristics for a 10 kW to no load operation (0 W) step. (b) Current and voltage characteristics for a 10 kW to 5 kW and a (c) 5 kW to 10 kW load step.

tem which mainly appear due to input filter capacitors (6.8 µF), dedicated filter RC damping network (3 Ω, 6.8 µF) and to cover system losses according to circulating currents, balancing output resistors, etc. Furthermore, the total FCC DC-link voltage v_{tot} is illustrated in **Fig. 6.25(b)** and **Fig. 6.25(c)** for decreasing (10 kW to 5 kW) and increasing (5 kW to 10 kW) load steps, respectively, while taking advantage of the previously discussed implemented voltage controller structure. It can be observed that the voltage deviation of the total FCC DC voltage link is defined by approximately 40 V which is only about 5 % of the defined rated voltage level $V_{tot}^* = V_{cp}^* + V_{cn}^* = 2 \cdot 400\,\text{V} = 800\,\text{V}$. **Fig. 6.26(a)-(c)** illustrate measurement results considering light- and no-load operation (operating in OM_{II}). For an output power of 2.2 kW (cf., **Fig. 6.26(a)**) no 10 kHz current ripple considering DC-side smoothing inductor current i_L can be observed. As given in **Fig. 6.26(c)** no-load operation, however, leads to a superimposed 10 kHz voltage

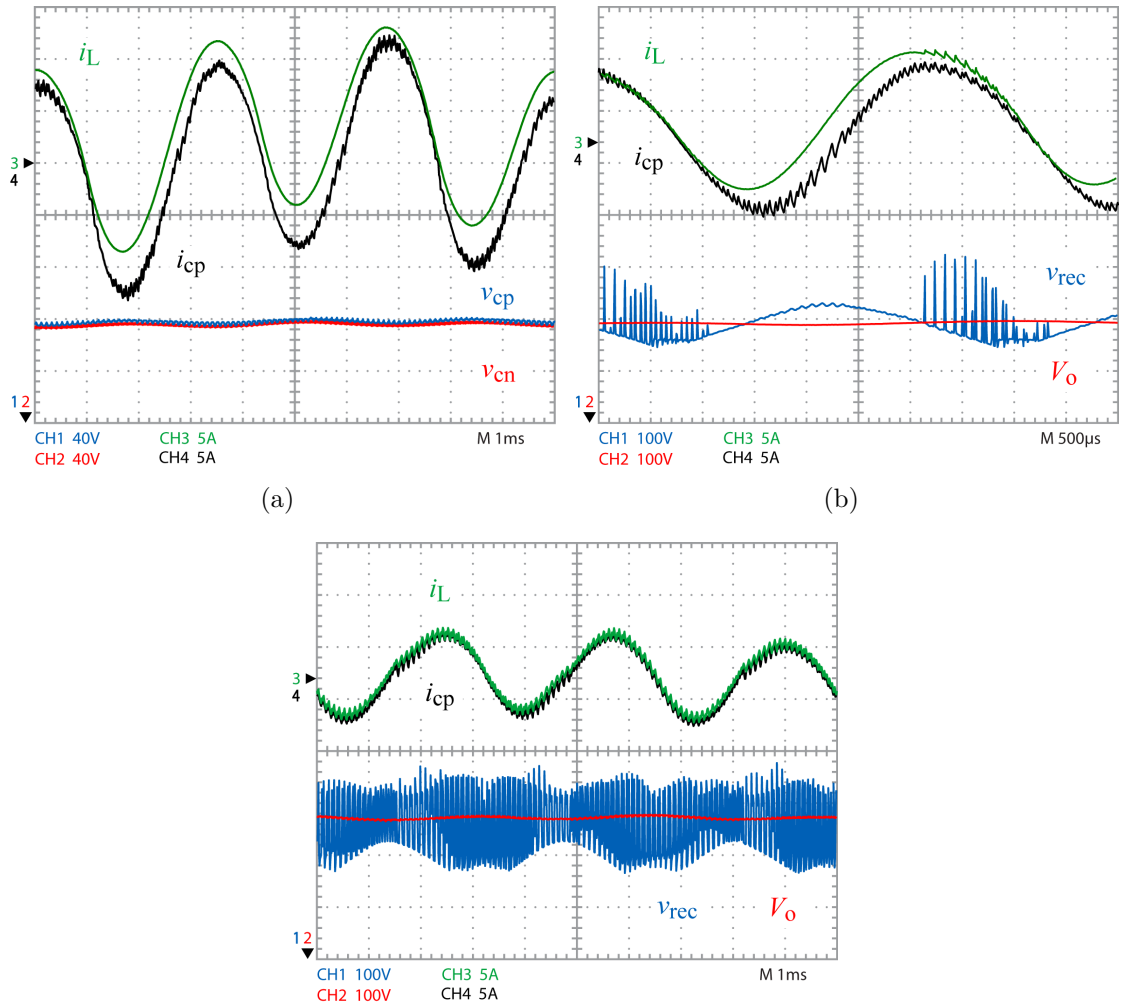


Fig. 6.26: Measurement results of the active system during CCM, ICOM and no-load mode operating in $\mathrm{OM_{II}}$. (a) Injection and smoothing inductance current (i_{cp}, i_L) and FCC DC-link voltages for 1.33 kW output power. No high-frequency components can be observed for i_L during CCM. (b) 0.8 kW output power (ICOM) for an injection inductance value of $< 1.8\,\mathrm{mH}$ @ 10 kHz. The rectifier output voltage v_{rec} and hence v_L shows high frequency voltage ripple with switching frequency during those time instants where i_{pos} yields discontinuous behaviour. (c) No-load operation and according side effects of the active system (circulating inductance current with high frequency current ripple), however, shows reduced 300 Hz peak-to-peak current ripple due to down scaled feed forward value ($L_{c,ff}/L_c \approx 0.64$).

ripple considering v_L and v_{rec} which causes a 10 kHz current ripple of i_L. The 300 Hz DC-side smoothing inductor ripple is still present during no-load mode (circular current). This current causes additional losses in the FCC, the coupled three-phase inductor, the DC-side smoothing inductor and the DC-link (output) capacitor. Hence, measurement results of the active input power yield rather high values of $P_{L,FCC,meas} = 60\,\mathrm{W}$ during no-load operation. A conventional passive three-phase rectifier, on contrary, only causes losses due to passive balancing resis-

TABLE 6.3: Measured Mains Voltage Harmonics (Location: Vienna University of Technology - Power Electronics Laboratory).

Measured Harmonic Components of Mains Voltages			
	v_{N1}	v_{N2}	v_{N3}
Fund. Comp.	231.3 V	230.5 V	229.9 V
3rd ord. harm.	0.33%	0.09%	0.41%
5th ord. harm.	2.22%	2.19%	2.06%
7th ord. harm.	1.32%	1.22%	1.29%
9th ord. harm.	0.22%	0.37%	0.43%
11th ord. harm.	0.22%	0.41%	0.33%
13th ord. harm.	0.47%	0.56%	0.53%
15th ord. harm.	0.14%	0.21%	0.31%
17th ord. harm.	0.16%	0.23%	0.19%

tors of the electrolytic capacitors during idle mode (as $i_L = i_{pos} = i_{neg} = 0$) and has be measured with only $P_{L,B6,meas} = 8\,W$ which is $\approx 13\,\%$ regarding the losses of the active system.

As can be seen from **Fig. 6.26(b)**, even for light-load operation v_{rec} and v_L are stressed with high frequency voltage components during those time instants where i_{pos} shows intermittent sections. Comparing **Fig. 6.26(a)** and **Fig. 6.26(c)** a different $\Delta i_{L,pkpk}$ and an increased output voltage V_o is observable. During continuous conduction mode (CCM) the peak-to-peak current ripple is defined due to the DC-side smoothing inductance and yields $\approx 18\,A$. For no-load operation (OM_{II}) $\Delta i_{L,pkpk}/2$ decreased to $\approx 6\,A$ which results due to optimized loss operation (and hence down scaled feed forward value $L_{c,ff}/L_c \approx 0.64$).

Finally, measurements taken from a three-phase grid at the power electronics lab of the TU-Wien revealed a THD_v of the grid voltages of approximately 2 % and an maximum grid unbalance of less than 1 %. A detailed characterisation of fundamental components and higher harmonics of all three mains phases are listed **TABLE 6.3**. All results have been obtained by a PM-300 power analyzer.

Fig. 6.27 clearly reveals the discussed superimposed 100 Hz component (due to unbalanced mains voltages) of i_L which obviously results in an increased peak-to-peak current ripple $\Delta I_{L,pkpk} = 21\,A$. This furthermore leads to an increased injection current i_{cp} showing a peak-to-peak current ripple $\Delta I_{cp,pkpk}$ of 28 A instead of the expected 21 A.

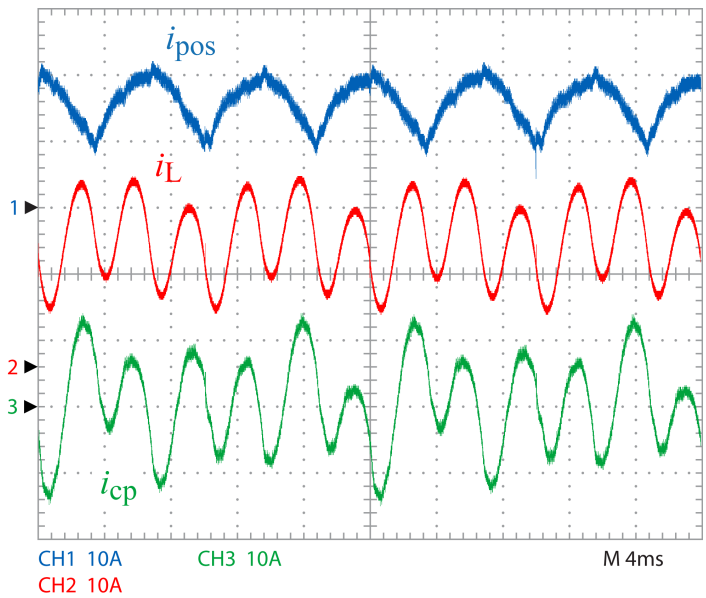


Fig. 6.27: Measured currents i_{pos}, i_L and i_{cp} for an output power of $P_o = 10\,\text{kW}$ and fundamental mains voltage components of $V_{N1,rms} = 231.3\,\text{V}$, $V_{N2,rms} = 230.5\,\text{V}$ and $V_{N3,rms} = 229.9\,\text{V}$.

Chapter 7

Prototypical Implementation – Topology B

As a result of the analyses in chapter 5, two topologies have been identified being most attractive for the aimed voltage/power range and hence selected for verification by laboratory prototype implementation. This chapter describes the second prototype implementation, now based on Top. B (CSN implementation using two half-bridge branches, **Fig. 5.9**) as an alternative to the prototype implementation given in chapter 6 (using FCC concept(Top. C)). Side effects (high frequency common-mode voltage during light/no-load condition, unbalanced mains voltages, etc.) as discussed in chapter 6 for Top. C also apply for Top. B, therefore, this chapter will merely focus only on the required hardware setup.
Design specifications of the built 10 kW/72 kHz three-phase rectifier are given in **TABLE 7.1** and **TABLE 7.2**. The system is constructed for 400 V_{LL}/50 Hz mains voltages, which results in 600 V DC voltage level for the injection cell capacitors C_{cp} and C_{cn} if a modulation index $M = 0.8125$ is assumed.
ROHM's SCT2080KE SiC-MOSFETs are used for implementing the active switches of the half-bridges connected to C_{cp} and C_{cn}. The bidirectional switches $S_{i,ab}$ are operating in back-to-back arrangement using IKW40T120 IGBTs. Also 1200 V or 900 V SiC-MOSFETs would be of advantage and could further reduce losses of the injection device by $\approx 30\,\%$, which is only $2-3\,\%$ of the total system losses, which does not outweigh at present the unfavorable increase in expense of cost per active component.

The B6 rectifier has to be configured such to allow a maximum total harmonic distortion of input currents of approximately 45 % at nominal load (10 kW) (B6-THD_i - standalone operation). The required DC-side smoothing inductance (L_{DC}) results in 2.25 mH. A relatively large output capacitor of 2x2.2 mF in series is chosen representing the DC-link of a, e.g., fed drive inverter.

The laboratory prototype (**Fig. 7.1(a-d)**) mainly consists of two different boards:

TABLE 7.1: Design Specifications of the Built Three-Phase Rectifier.

Mains voltage:	$V_{\mathrm{LL}} = 400\,\mathrm{V_{rms}}$
Mains frequency:	$f_{\mathrm{N}} = 50\,\mathrm{Hz}$
Switching frequency:	$f_{\mathrm{s}} = 72\,\mathrm{kHz}$.
Cells DC-link voltage:	$V_{\mathrm{cp}} = V_{\mathrm{cn}} = 600\,\mathrm{V}$
Output power:	$P_{\mathrm{o}} = 10\,\mathrm{kW}$

TABLE 7.2: Power Devices Selected for Implementation of the passive rectifier and Third Harmonic Injection Cell.

$S_{i\mathrm{a,b}}$	1200 V/40 A IGBT, IKW40T120, Infineon
$S_{\mathrm{c}\frac{\mathrm{p}}{\mathrm{n}}\pm}$	1200 V/20 A SiC-MOSFET, SCT2080, ROHM
$C_{\mathrm{c}\frac{\mathrm{p}}{\mathrm{n}}}$	220 µF/400 V, EPCOS B43508-type
L_{cp}=L_{cn}=L_{h3}	Iron Powder Core 2 x T184-14, N = 59 turns 200 µH
C_{F}, C_{S}	1 µF/275 $\mathrm{V_{AC}}$, MKP X2, Arcotronics
C_{o}	2.2 mF/400 V, Felsic CO 39 A728848
L_{DC}	2.25 mH, Iron core 2 x UI60a
$D_1 - D_6$	35 A/1600 V, 36MT160, Vishay

controller board and power board. The controller board (cf., **Fig. 7.1(c)**) contains measurement circuits, auxiliary power supply, DSP control unit (TI 320F2808), additional hardware as e.g. zero crossing detection of mains line-to-line voltages and bidirectional switch controller (Lattice CPLD - MachXO 2280). Except for the digital signal processor (which is located at the bottom of the control board) all remaining parts are mainly placed top-side of the board. Gate drives of SiC-MOSFETs and IGBTs are located on separate plug-in boards (**Fig. 7.1(a)** and **Fig. 7.1(b)** – one board for each half-bridge stage and one additional board for bidirectional switches $S_{\mathrm{i,ab}}$). The PCB circuits are located in between control and power board (cf., **Fig. 7.2**) in order to minimize the total volume of the cell and reduce parasitic inductances between gate drive circuits, appropriate switches and DC-link electrolytic capacitor bank (C_{cp} and C_{cn}). The power board, which is depicted in **Fig. 7.1(d)**, includes main power components as forced convection cooling system, IGBTs, SiC-MOSFETs, input filter, current sensors, inductors, electrolytic capacitors and additional hardware which is required for start-up operation of the system.

Calculated system losses at nominal load ($P_{\mathrm{N}} = 10\,\mathrm{kW}$) are depicted in **Fig. 7.3**. As can be seen, the highest losses of all included parts are drawn by the DC-side choke ($\approx 50\,\mathrm{W}$) and the passive three-phase rectifier ($\approx 40\,\mathrm{W}$) which have to transfer the main part of the active power. The injection cell only has to process some amount of active an reactive power ($P_{\mathrm{THI}} \approx 6\,\%P_{\mathrm{o}}$, and $Q_{\mathrm{THI}} \approx 17\,\%P_{\mathrm{o}}$) which obviously results in an improved efficiency of the optional configuration compared to PFC circuits where the total power has to be processed by the active switches.

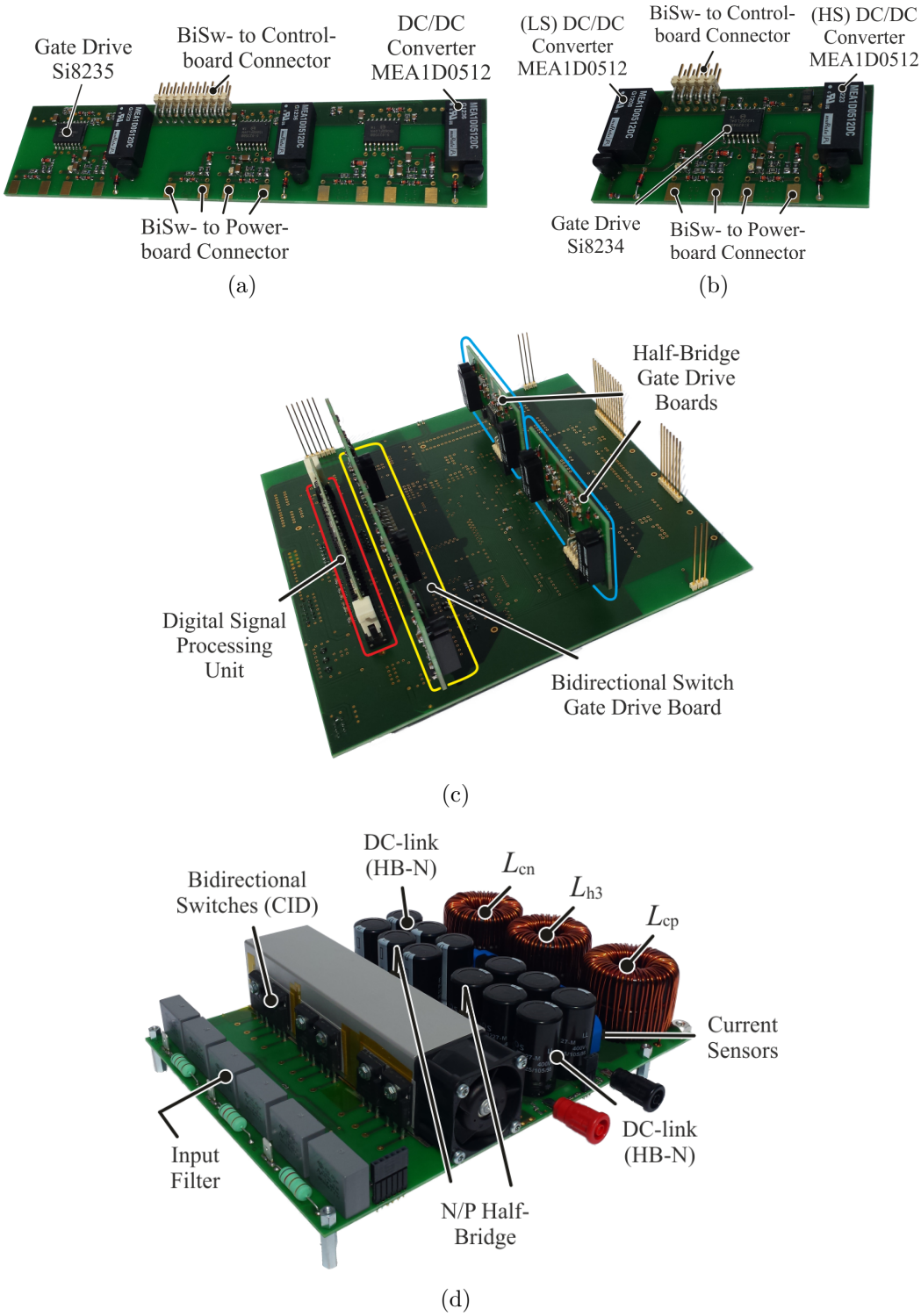


Fig. 7.1: (a) Bidirectional switch gate drive board (only 1 DC/DC converters required for each bidirectional switch assembly). (b) Positive and/or negative half-bridge gate drive board (2 DC/DC converters required for each board – 1 for each SiC-MOSFET). (c) Control board (bottom view) with plug-in DSP board (red), half-bridge gate drive boards (blue) and bidirectional switch boards (yellow). (d) Power board consisting of current sensors, inductors, half-bridge stage, bidirectional switches and input filter.

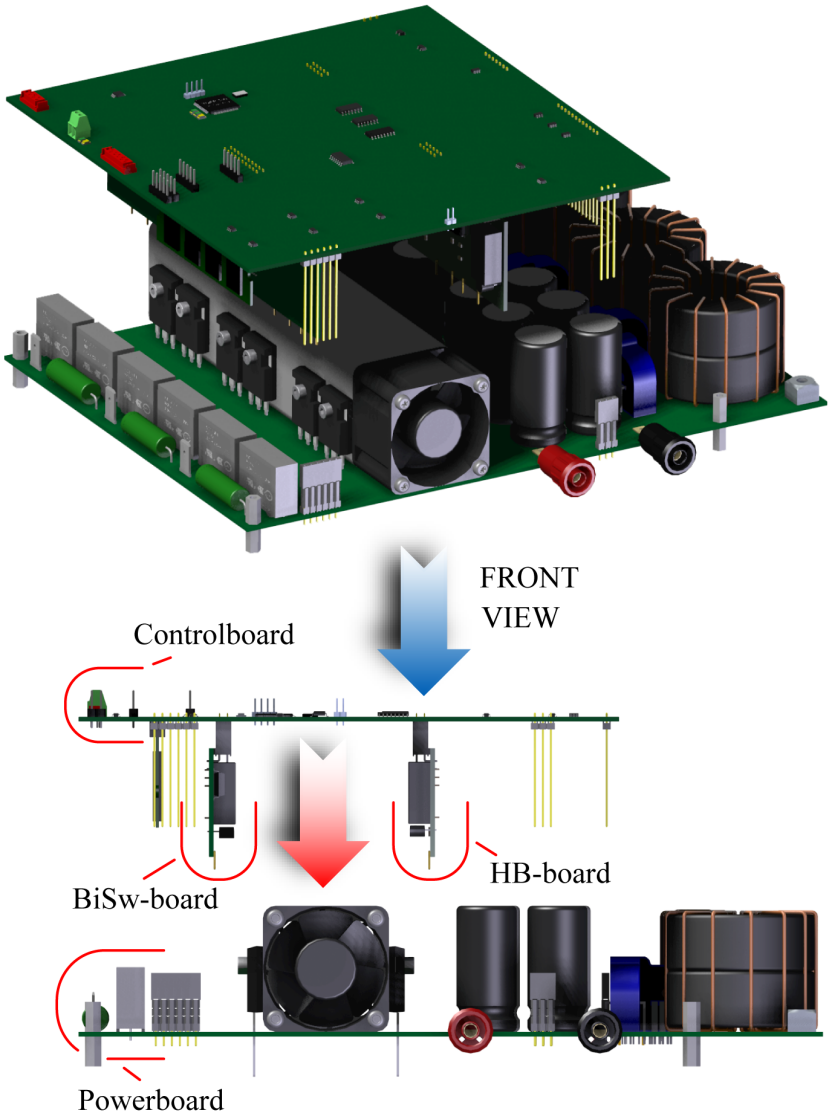


Fig. 7.2: CAD drawing of designed converter which includes the arrangement of the 4 different boards (control board, power board, bidirectional switch gate drive board and half-bridge gate drive board).

According to **Fig. 7.3**, losses are about evenly distributed over both circuits (passive circuit/active circuit - $\approx 50\,\%/50\,\%$, respectively). The total system losses are calculated to 209 W which results in an expected system efficiency η_{calc} of 97.95 %. The performed loss calculation allows the design of the forced convection (air) cooling system. The chosen fan-equipped heatsink serves as loss dissipating surface for SiC-MOSFETs (half-bridges) and IGBTs (bidirectional switches). According to [146] a cooling system performance index (CSPI)

$$\text{CSPI} = \frac{1}{R_{\text{th,hs}} V_{\text{hs}}} \tag{7.1}$$

has been introduced in order to allow a general comparison of different cooling system technologies. A forced convection air cooled heatsink typically results in a CSPI between $5 - 12\,\frac{\text{W}}{\text{K}\cdot\text{dm}^3}$. The CSPI of the chosen LAM4K (150 mm) heatsink

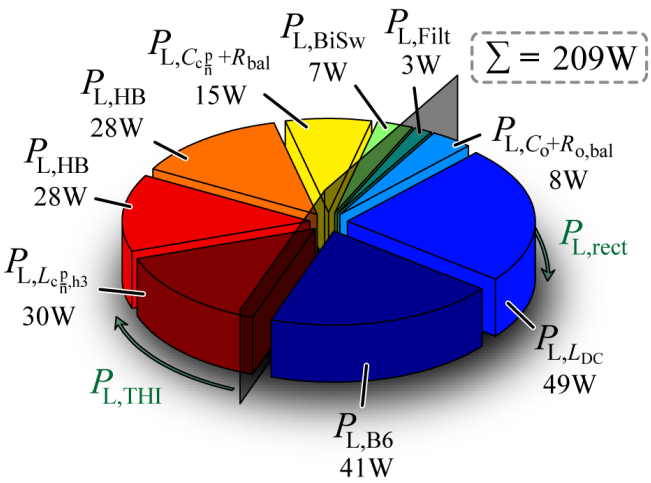


Fig. 7.3: Losses of the three-phase rectifier system for 230 V_{rms}/50 Hz a switching frequency of 72 kHz and 10 kW output power.

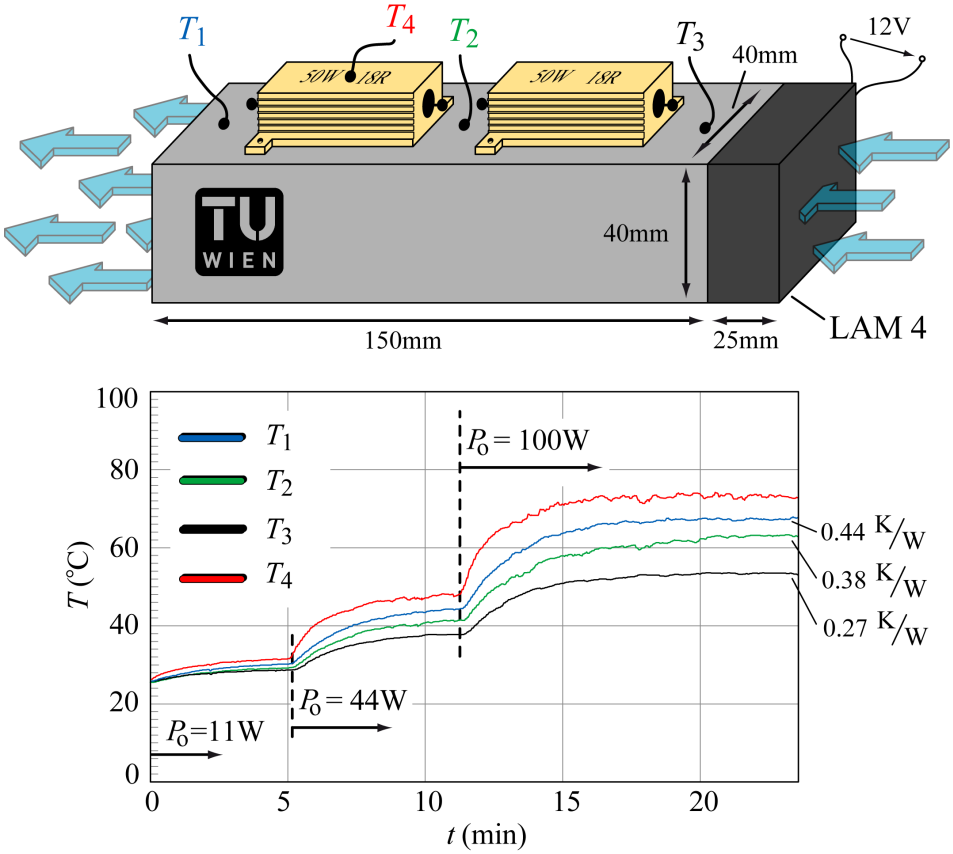


Fig. 7.4: Temperature profile (measurement device: Voltcraft Thermologger K204) of the designed LAM4K air cooled system at different points (e.g. close to mounted fan - T_3). The measured worst case $R_{th,hs}$ was used to evaluate the appropriate maximum cooling temperature.

has been evaluated to 9 $\frac{W}{K \cdot dm^3}$ (cf., **Fig. 7.4**, evaluated temperature profile and maximum $R_{th,hs} = 0.44 \frac{W}{K}$ - measurement device: Voltcraft Thermologger K204). In order to determine the highest $R_{th,hs}$ value of the heatsink, two 50 W resistors

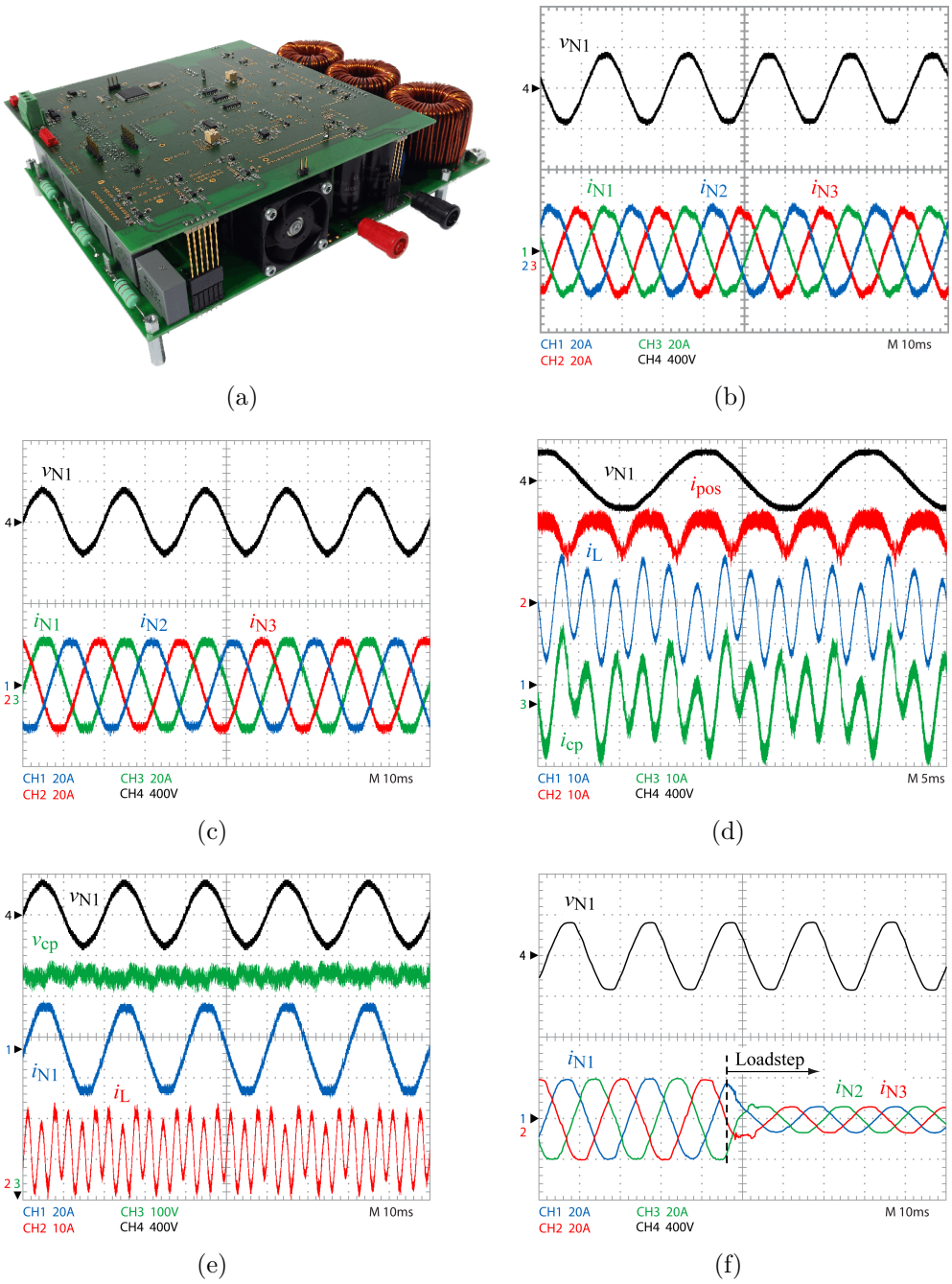


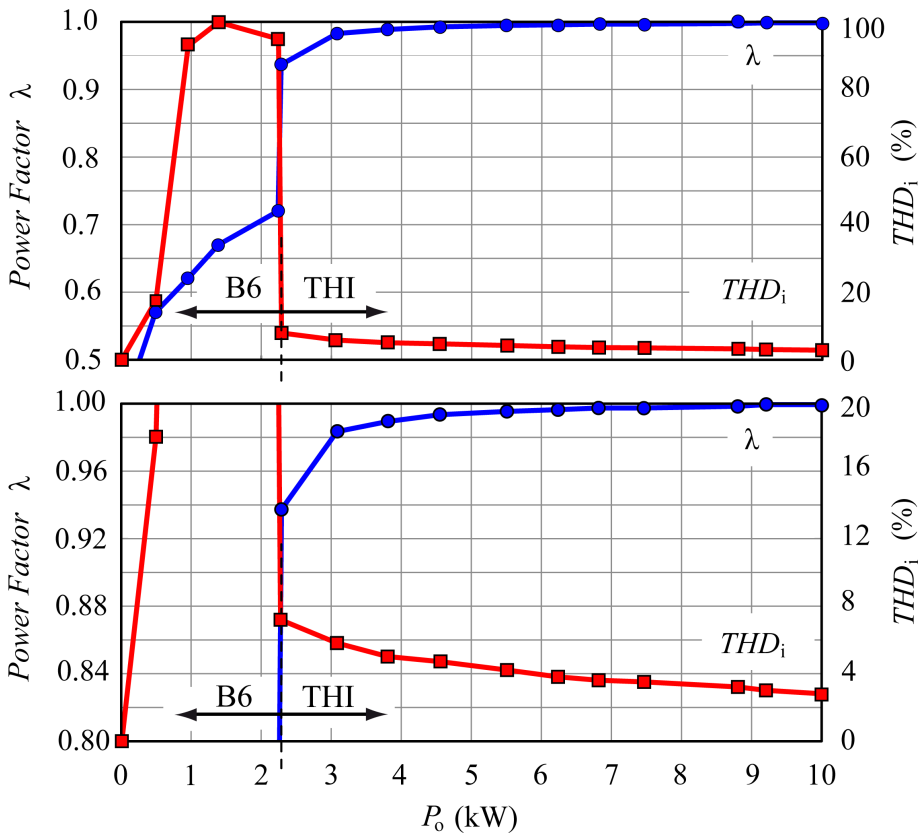
Fig. 7.5: (a) Assembled 10 kW laboratory prototype. (b) Mains currents i_{N1} - i_{N3} and mains voltage v_{N1} for 400 $V_{LL,rms}$ input voltage with implemented P-type controller without feedforward currents results in $THD_i = 3.6\,\%$ and $\lambda = 0.999$. (c) Mains currents i_{N1} - i_{N3} and mains voltage v_{N1} for 230 $V_{LL,rms}$ input voltage with implemented PI-type controller (no feedforward current control) results in $THD_i = 2.8\,\%$, $\lambda = 0.999$. (d) Most important current waveforms of positive half-bridge injection leg i_{pos}, i_{cp} and i_L. (e) Controlled DC-voltage v_{cp} of positive half-bridge connected to capacitor stage C_{cp}. (f) Input currents for a 10 kW to 3 kW load step.

(evenly mounted on the heatsink) have been attached on the optimized heatsink profile. The worst case $R_{th,hs}$ has been spotted for the thermal measurement

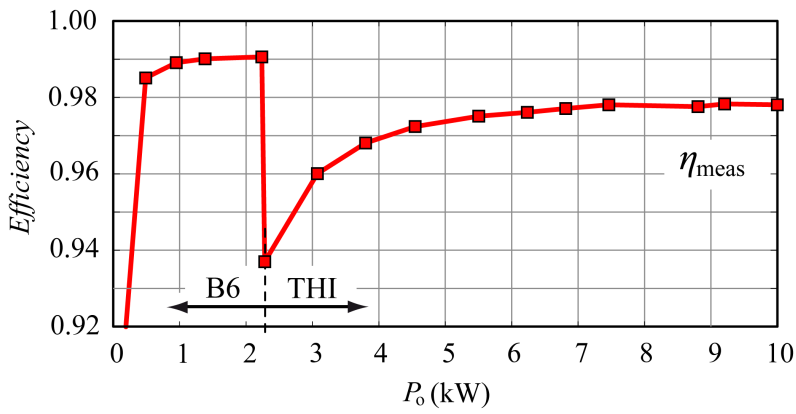
T_1 which was placed farthest from the mounted fan. Considering active switch component losses as illustrated in **Fig. 7.3**, the maximum heatsink temperature T_{hs} results in

$$T_{\mathrm{hs}} = T_{\mathrm{amb}} + \frac{P_{\mathrm{sys}}\left(\eta_{\mathrm{HB+BiSw}}^{-1} - 1\right)}{V_{\mathrm{hs}} \cdot \mathrm{CSPI}} \approx 54^{\circ}\mathrm{C}. \tag{7.2}$$

Therefore, the cooling system would still allow an additional decrease of volume for the given active rectifier topology or an increase in switching frequency (switching losses) up to 200 kHz to stay $< 100\,^{\circ}\mathrm{C}$ heatsink temperature T_{hs}.
The fully assembled prototype (controller board, power board and gate drive boards) is shown in **Fig. 7.5(a)**. Measurement results of the 10 kW/72 kHz laboratory prototype are depicted in **Fig. 7.5(b-f)**. **Fig. 7.5(b)** shows input currents i_{N1} - i_{N3} and mains voltage v_{N1} for 230 $\mathrm{V_{LL,rms}}$ input voltage with an implemented P-type controller without any feedforward of i_{L} and i_{h3}. Nevertheless, input current distortions of only $\mathrm{THD_i} = 3.9\,\%$ could be observed. The power factor λ was measured by 0.999 . Furthermore, a system efficiency η_{meas} of 97.7 % has been determined. Heatsink temperature after 20 min of operation at 10 kW has reached 56 °C and an injection choke inductance temperature of 87 °C has been measured. In order to, verify if input current waveforms could be further improved (by utilizing an improved current controller) a PI-type controller has been implemented (cf., **Fig. 7.5(c)**). As can be seen, indeed input currents waveforms can be further improved and a $\mathrm{THD_i}$ of 2.8 %. **Fig. 7.5(d-f)** show different current and voltage waveforms for nominal load of the 10 kW rectifier. As can be noticed from **Fig. 7.5(d)**, the topology is able to suppress the appearing 100 Hz ripple of i_{L} (due unbalanced mains voltages) as no 100 Hz components can be observed anymore affecting i_{pos}. Furthermore, slight distortions of input currents every $\pi/3$ may appear (cf., i_{pos}) if the duty cycle of the half-bridges violates the upper or lower boundary. This effect mainly appears due to unbalanced input voltages (as already discussed) and cannot be fully eliminated. The $\mathrm{THD_i}$ is also dependent on the mains voltage balancing situation, being the most severe drawback of the used topology especially to, e.g., the FCC concept. **Fig. 7.5(e)** shows the controlled DC-voltage v_{cp} of the positive half-bridge connected to capacitor stage C_{cp}. A load step from 10 kW to 3 kW is finally depicted in **Fig. 7.5(f)**.
Fig. 7.6(a-b) illustrate λ, $\mathrm{THD_i}$ and η characteristics of the implemented THI rectifier. The THI rectifier is put into operation for an output power > 2.3 kW. At approximately 3 kW (power level dependent on implemented coil inductance L_{c}, not on i_{L}) the CCM to DCM boundary of the circuit is located. As the current control at present is not designed for DCM operation of the system, exceeding this boundary leads to a deteriorated performance of the total system ($\mathrm{THD_i}$ and λ). Thus, it is highly recommended to disable the active stage and merely allow B6-standalone operation for light loads (for such a inductor design $L_{\mathrm{c}} = 190\,\mu\mathrm{H}$). Furthermore, increased losses can be observed, as the passive three-phase rectifier is stressed with switching frequency during DCM and hence impairing the efficiency η.



(a)



(b)

Fig. 7.6: Measurement results of the total rectifier circuit for different output power levels P_o. (a) Power factor λ, THD_i and (b) Efficiency η are illustrated for third harmonic injection mode ($\approx 2.2\,kW$ - $10\,kW$) and B6 standalone operation ($< 2.2\,kW$).

Chapter 8

Comprehensive Comparison

One of the most attractive PFC circuits for unidirectional power flow is the VIENNA rectifier (e.g. [66]). The VIENNA rectifier topology as illustrated in **Fig. 8.1** now serves as competitive partner for an opposed comparison of the VIENNA rectifier and a B6 rectifier enhanced by an active optional circuit based on the third harmonic injection principle (employing two half-bridge branches) as analyzed in this thesis. Different performance indices as system efficiency, switching/conduction losses, rated inductor power etc. are used in order to emphasize additional benefits and drawbacks of the THI rectifier concept compared to the active unidirectional PFC rectifier (VIENNA) which is already widely-used in industry today. It has to be noted that a comparison of these two active rectifiers should not identify a superior concept (which is indeed not possible due to completely different attributes of both rectifiers). The investigation should reveal advantages and drawbacks of the THI circuit by comparing the upgradeable rectifier to a today well established industrial standard PFC concept. Such a comparison to the known VIENNA rectifier principle several times has been asked for at conference presentations of the proposed THI concept and shall be included here for the sake of completeness, despite the fact that both principles address different basic features (the VIENNA rectifier performs controlled output voltage whereas the THI principle gives the opportunity to optionally extend an existing B6 rectifier).

8.1 Benchmarking Specifications

A reliable comparison between the two active systems should allow an advanced benchmarking of the THI rectifier. Therefore, different performance indices (which are used for this comparison) are introduced, listed and shortly described in the

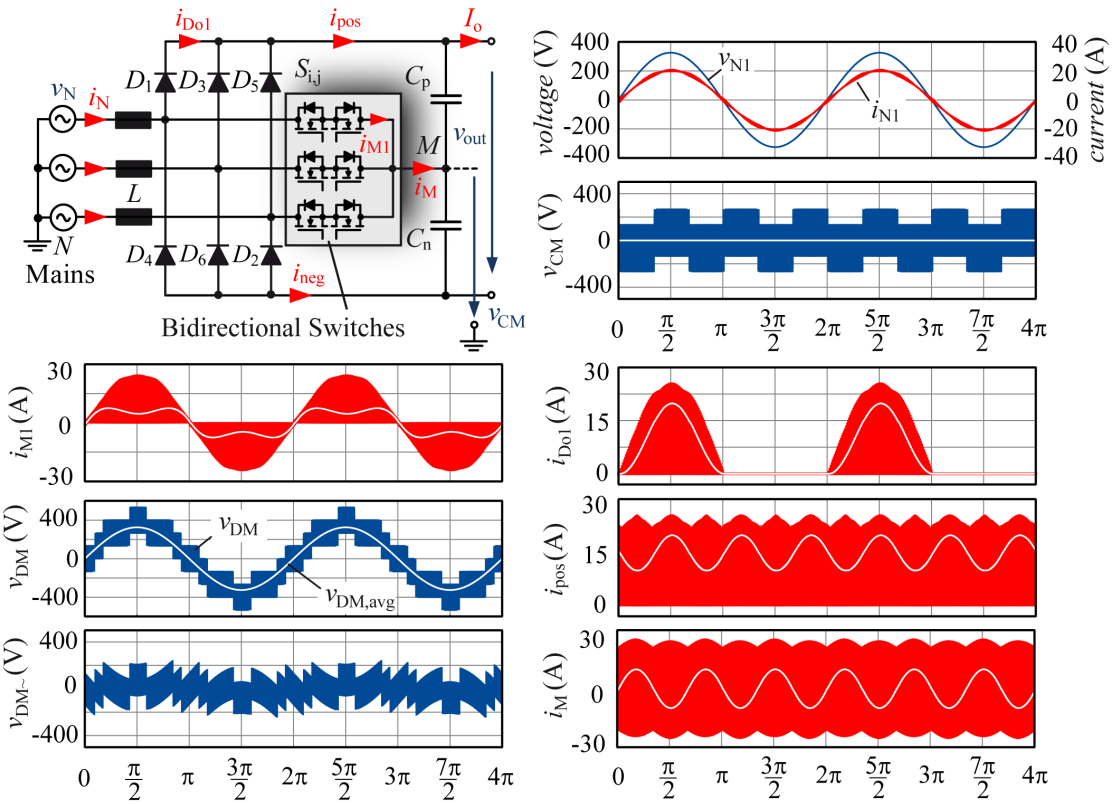


Fig. 8.1: VIENNA rectifier with six 600 V MOSFETs which form the interconnection between AC-side and output capacitors midpoint M and diode bridge (typically implemented fast recovery diodes).

following items using the rated power P_o of the converter/topology and/or rated voltage V_o and/or rated current I_o as normalization quantities:

Diode/MOSFET VA-Ratings

The VA-ratings of a switching element is defined by multiplication of its maximum blocking voltage and peak current. This VA-rating hence gives if normalized a prediction of the relative maximum stress of all diodes (μ_D^{-1}) or transistors (μ_S^{-1}) in a power electronics circuit:

$$\mu_S^{-1} = \frac{\sum_n v_{S,max,n} i_{S,max,n}}{P_o} \quad \text{and} \quad \mu_D^{-1} = \frac{\sum_n v_{D,max,n} i_{D,max,n}}{P_o} \,. \tag{8.1}$$

Rated Inductor Power/Capacitor Current Stress

Two major performance aspects in order to classify inductors and capacitors in an electrical way are to introduce a rated inductor power index ρ_L and a normalized capacitive current stress equivalent ρ_C of all implemented inductors and capacitor

stages within the converter system:

$$\rho_{\mathrm{L}} = \frac{\sum_n \Delta I_{\mathrm{L,pkpk,n}} I_{\mathrm{L,n}} L_{\mathrm{c,n}} f_{\mathrm{s}}}{P_{\mathrm{o}}}, \quad \rho_{\mathrm{C}} = \frac{\sum_n I_{\mathrm{C,rms,n}}}{I_{\mathrm{o}}} \tag{8.2}$$

Inverse Power Density of Inductors

Besides electrical characteristics of inductors, also a volume dependent design might be of interest for evaluation of a implementation of a power electronics circuit. Therefore, the power density of the implemented inductors is selected as promising benchmark indexing.

$$\epsilon_{\mathrm{L}}^{-1} = \frac{\sum_n V_{\mathrm{L,n}}}{P_{\mathrm{o}}} \tag{8.3}$$

Switching Losses of Semiconductors

Furthermore, the switching losses of all impaired semiconductor components are evaluation using the normalized quantity τ_{p} defined as:

$$\tau_{\mathrm{p}} = \frac{\sum_n I_{\mathrm{S,avg,n}} V_{\mathrm{S,n}}}{P_{\mathrm{o}}} \tag{8.4}$$

with V_{S} denoted as the applied maximum blocking voltage of the respective transistor and $I_{\mathrm{S,avg}}$ the averaged current.

Conduction Losses of Diodes and Switches

Conduction losses of switches and diodes can be benchmarked by considering averaged and rms current values related to the output current (cf., [19]).

$$\tau_{\mathrm{c}} = \frac{\sum_n I_{\mathrm{S,rms,n}}}{I_{\mathrm{o}}} \quad \delta_{\mathrm{c}} = \frac{\sum_n I_{\mathrm{D,avg/rms,n}}}{I_{\mathrm{o}}} \tag{8.5}$$

System Efficiency

Finally the performance of the total system is determined by comparing total relative losses of both active systems by using

$$1 - \eta = \frac{P_{\mathrm{in}} - P_{\mathrm{o}}}{P_{\mathrm{in}}}. \tag{8.6}$$

8.2 Comparative Values - THI

In this section, the previously described performance indices are now analytically derived. The VA-ratings of the implemented semiconductor is the first parameter

of interest in this evaluation. The THI rectifier diodes (D_{1-6}) are stressed with a maximum blocking voltage which is dependent according to the peak line-to-line voltage situation ($v_{\mathrm{D,max}} = \sqrt{2}V_{\mathrm{LL}}$) and a maximum current which is equivalent to $\hat{I}_{\mathrm{N}}$. The diodes of one bidirectional switch obtain their maximum while the two remaining bidirectional switches initiate the current commutation of i_{h3}. This commutation however takes place before the applied line-to-line voltage attains its maximum value. The maximum blocking voltage of the diodes (and thus also transistors) of bidirectional switches is hence defined by $3\hat{V}_{\mathrm{N}}/2$, and the maximum current is given according to i_{h3} (whose peak value is $\hat{I}_{\mathrm{N}}/2$). The switches of each half-bridge are stressed with the peak current of injection currents i_{cp}, i_{cn} and the DC voltage of C_{cp}, C_{cn}, respectively. The VA ratings of switches and diodes hence finally lead to

$$\mu_{\mathrm{S}}^{-1} = \frac{9\hat{V}_{\mathrm{N}}\hat{I}_{\mathrm{N}} + 16V_{\mathrm{c}}\hat{I}_{\mathrm{cp}}}{4P_{\mathrm{o}}}\,, \tag{8.7}$$

$$\mu_{\mathrm{D}}^{-1} = \frac{6\hat{V}_{\mathrm{N}}\hat{I}_{\mathrm{N}}\left(8\sqrt{3}+3\right)}{8P_{\mathrm{o}}}\,. \tag{8.8}$$

In order to evaluate the current stress of capacitors, three different capacitor banks have to be considered (C_{cp}, C_{cn} and C_{o}). C_{o} is characterized by $\hat{I}_{\mathrm{L,ac}}/2$. Current stress of half-bridge capacitors C_{cp}, C_{cn}, can only be determined numerically and result in $3.6\,\mathrm{A_{rms}}$ for an output power of $10\,\mathrm{kW}$. The normalized capacitive current stress ρ_{C} of all implemented capacitors of the THI rectifier then results in

$$\rho_{\mathrm{C}} = \frac{\hat{I}_{\mathrm{L,ac}} + 2\sqrt{2}I_{\mathrm{ccp}}}{\sqrt{2}I_{\mathrm{o}}}, \quad \text{with} \tag{8.9}$$

$$\hat{I}_{\mathrm{L,ac}} = \frac{\sqrt{3}\hat{V}_{\mathrm{N}}}{\omega_{\mathrm{N}}L_{\mathrm{DC}}}\left(\sin\left(\arccos\left(\frac{3}{\pi}\right)\right) - \frac{3}{\pi}\arccos\left(\frac{3}{\pi}\right)\right)\,. \tag{8.10}$$

The rated inductor power (of the appropriate implemented chokes L_{cp}, L_{cn}, L_{h3} and L_{DC}) is dependent on current rms values I_{cp}, I_{cn}, I_{h3}, I_{L}, and the appropriate maximum peak-to-peak current ripples ΔI_{cp}, ΔI_{cn}, ΔI_{h3}, ΔI_{L}, at the relevant frequencies f_{s}, $6f_{\mathrm{N}}$. The required dedicated parameters are defined by

$$I_{\mathrm{c}\frac{\mathrm{p}}{\mathrm{n}}} = \hat{I}_{\mathrm{N}}\sqrt{\frac{2\pi^3 - 24\pi + 9\sqrt{3}}{24\pi} + \left(\frac{\hat{I}_{\mathrm{L,ac}}}{\sqrt{2}\hat{I}_{\mathrm{N}}}\right)^2}, \quad \Delta I_{\mathrm{c}\frac{\mathrm{p}}{\mathrm{n}}} = \frac{2V_{\mathrm{c}}M\left(1-M\right)}{3f_{\mathrm{s}}L_{\mathrm{c}\frac{\mathrm{p}}{\mathrm{n}}}} \tag{8.11}$$

$$I_{\mathrm{h3}} = \frac{\hat{I}_{\mathrm{N}}}{2}\sqrt{\frac{2\pi - 3\sqrt{3}}{\pi}}, \qquad \Delta I_{\mathrm{h3}} = \frac{V_{\mathrm{c}}M}{3\sqrt{3}f_{\mathrm{s}}L_{\mathrm{c}\frac{\mathrm{p}}{\mathrm{n}},\mathrm{h3}}} \tag{8.12}$$

$$I_{\mathrm{L}} = \frac{\hat{I}_{\mathrm{N}}}{2}\sqrt{\frac{2\pi^2}{3} + 2\left(\frac{\hat{I}_{\mathrm{L,ac}}}{\hat{I}_{\mathrm{N}}}\right)^2}, \qquad \Delta I_{\mathrm{L}} = 2\hat{I}_{\mathrm{L,ac}}\,. \tag{8.13}$$

The rated inductor power hence calculates to

$$\rho_{\mathrm{L}} = \frac{2I_{\mathrm{c}\frac{\mathrm{p}}{\mathrm{n}}}\Delta I_{\mathrm{c}\frac{\mathrm{p}}{\mathrm{n}}}L_{\mathrm{c}\frac{\mathrm{p}}{\mathrm{n}}}f_{\mathrm{s}} + I_{\mathrm{h3}}\Delta I_{\mathrm{h3}}L_{\mathrm{h3}}f_{\mathrm{s}} + 6I_{\mathrm{L}}\Delta I_{\mathrm{L}}L_{\mathrm{DC}}f_{\mathrm{N}}}{P_{\mathrm{o}}}\,. \tag{8.14}$$

In order to identify conduction losses of switches (rms) and diodes (avg), the current stress of corresponding components is required which can be finally determined by

$$I_{D_{1-6,\mathrm{avg}}} = \frac{\sqrt{3}\hat{I}_\mathrm{N}}{2\pi}, \tag{8.15}$$

$$I_{D_{\mathrm{i,ab,avg}}} = \frac{\hat{I}_\mathrm{N}}{2\pi}\left(2-\sqrt{3}\right), \tag{8.16}$$

$$I_{D_{\mathrm{i,ab,avg}}} = \hat{I}_\mathrm{N}\sqrt{\frac{2\pi-3\sqrt{3}}{24\pi}}\ . \tag{8.17}$$

The current stress of both half-bridge semiconductors can again only be calculated numerically and finally results in 3.6 $\mathrm{A_{rms}}$ and 5 $\mathrm{A_{rms}}$ for the positive (S_+) and negative switch (S_-) of one half-bridge, respectively (10 kW nominal load operation). If all derived characteristics are considered conduction losses of both diodes and transistors thus result in

$$\delta_\mathrm{c} = \frac{6}{\pi}\frac{\hat{I}_\mathrm{N}}{I_\mathrm{o}}\ , \tag{8.18}$$

$$\tau_\mathrm{c} = \frac{3\hat{I}_\mathrm{N}\sqrt{2\pi-3\sqrt{3}}+2\sqrt{6\pi}\left(I_{\mathrm{S}+}+I_{\mathrm{S}-}\right)}{\sqrt{6\pi}I_\mathrm{o}}\ . \tag{8.19}$$

The switching losses of the system can be "qualitatively" determined by utilizing the averaged pulsed current of each switch (assuming linear dependency of the switching losses on the switched current) and applied drain source voltage (during the off state of the transistor). The bidirectional switches of the THI rectifier are only turned on and off twice during one mains period. Switching losses of these device are hence negligibly small. The only devices which are operated with switching frequency f_s are the half-bridge semiconductors (S_+, S_-). The averaged values of these components can be determined numerically and lead to 0 $\mathrm{A_{avg}}$ and 1.6 $\mathrm{A_{avg}}$, respectively. τ_p can be assessed and yields

$$\tau_\mathrm{c} = \frac{2I_{\mathrm{S}-}V_\mathrm{c}}{P_\mathrm{o}}\ . \tag{8.20}$$

The coils of the injection cell are designed such to allow a maximum ripple of 20 % $\hat{I}_\mathrm{N}$ which results in an inductance value of $\approx$ 190 µH for the required power level of 10 kW. The implemented inductor (stacked core assembly) leads to a core volume of 0.074 dm^3 for each inductor (stacked core: 2xT184-14, windings: 59). The necessary passive three-phase rectifier choke is a 300 Hz inductor and hence considerably larger than the injection coils (as it is typically designed for a maximum input current $\mathrm{THD_i}$ value of 48 % for B6 standalone operation). The volume of the implemented inductor results in 0.57 dm^3 (not optimized). The reciprocal power density of all inductors of the THI rectifier is defined by

$$\epsilon_\mathrm{L} = \frac{3V_\mathrm{L}V_{L_\mathrm{DC}}}{P_\mathrm{o}}\ . \tag{8.21}$$

The efficiency of the total system was calculated to be $\approx$ 98 % and 97.8 % has been measured (10 kW/72 kHz prototype) for a nominal load of 10 kW. The total specific losses of the system can therefore be assessed and result in $1-\eta = 2.2\,\%$.

8.3 Comparative Values - VIENNA

The maximum blocking voltage of the VIENNA rectifier diodes (D_{1-6}) is dependent on the required (and controllable) output voltage V_o. The maximum diode current is (as for the THI rectifier topology) the peak mains input current $\hat{I}_N$. Blocking voltage levels of each diode of the bidirectional switches only have to withstand $V_o/2$. Similar assumptions as discussed for diodes of the bidirectional switches also apply for appropriate MOSFETs. The VA-ratings of implemented switches result in

$$\mu_S^{-1} = \frac{3\hat{V}_o\hat{I}_N}{P_o} , \tag{8.22}$$

$$\mu_D^{-1} = \frac{9\hat{V}_o\hat{I}_N}{P_o} . \tag{8.23}$$

The current stress of the VIENNA rectifier output capacitors (both connected to the midpoint M) can be evaluated in an analytical form. The normalized capacitive current stress ρ_C of the required output capacitor stage of the rectifier is defined by

$$\rho_C = 2\frac{\hat{I}_N}{I_o}\sqrt{\frac{5\sqrt{3}M}{4\pi} - \frac{9M^2}{16}} \quad \text{with} \quad M = 2\frac{\hat{V}_N}{V_o} . \tag{8.24}$$

In order to characterize the rated inductor power of the VIENNA rectifier it is assumed that the maximum current ripple appears at $\varphi_N = 0°$, which is valid for a modulation index $M > 0.85$ ($V_o < 760\,\text{V}$). For smaller values of M, $\Delta I_{L,max}$ is located at $\varphi_N = 30°$ which is neglected for the comparison at hand. The inductor rms current is defined by the input current rms and results in $I_{L,rms} = I_{N,rms}$. The rated inductor power then leads to ρ_L of

$$\rho_L = \frac{3}{4\sqrt{2}}\frac{\hat{I}_N V_o}{P_o}\left(\frac{8}{3}M - M^2 - \frac{4}{3}\right) . \tag{8.25}$$

The boost inductors of an 800 V VIENNA, are implemented as Schott 193 type coils. The total volume of all 3 chokes results in $0.285\,\text{dm}^3$, which leads to a reciprocal power density of $0.029\,\text{dm}^3/\text{kW}$.
In a further step the conduction losses of transistors and diodes are going to be calculated. The transistor conduction losses are represented by the rms value of its drawn current for one mains period. The diodes conduction losses are characterized by its averaged current values. The evaluated values of transistors and diodes conduction losses result in

$$\tau_c = 6\frac{\hat{I}_N}{I_o}\sqrt{\frac{1}{4} - \frac{2M}{3\pi}} \tag{8.26}$$

$$\delta_c = \frac{6}{\pi}\frac{\hat{I}_N}{I_o} . \tag{8.27}$$

TABLE 8.1: Specifications of the two benchmarked three-phase rectifier systems.

Mains Voltage:	$V_{\mathrm{LL}} = 400\,\mathrm{V_{rms}}$
Mains Frequency:	$f_{\mathrm{N}} = 50\,\mathrm{Hz}$
Active Rectifier:	VIENNA
THI Rectifier (Shaping Circuit):	2 Half-Bridge Branches
THI Rectifier (Injection Circuit):	3 Bidirectional Switches
Switching Frequency:	$f_{\mathrm{s}} = 72\,\mathrm{kHz}$
THI Cell DC-link Voltage:	$V_{\mathrm{cp}} = V_{\mathrm{cn}} = 600\,\mathrm{V}$
THI Output Voltage (uncontrolled):	$V_{\mathrm{o}} = 540\,\mathrm{V}$
VIENNA Output Voltage (controlled):	$V_{\mathrm{o}} = 650\,\mathrm{V} \ldots 800\,\mathrm{V}$
Output Power:	$P_{\mathrm{o}} = 10\,\mathrm{kW}$

The switching losses can be again "qualitatively" identified by the averaged current of the appropriate semiconductor. The switching losses of S_{1-6} are finally determined and yield

$$\tau_{\mathrm{p}} = 3\frac{\hat{I}_{\mathrm{N}} V_{\mathrm{o}}}{P_{\mathrm{o}}}\left(\frac{1}{\pi} - \frac{M}{4}\right) . \tag{8.28}$$

The efficiency of the VIENNA rectifier for 800 V output voltage was documented in [19] and has been evaluated to be 97.3 %.

8.4 Comparison of Results

Results of the performance evaluation for both rectifiers are summarized in two "radar diagrams" (VIENNA rectifier with 650 V and 800 V regulated output voltage V_{o}) as depicted in **Fig. 8.2** and e.g. used in [147]. The output voltage levels of the VIENNA rectifier are chosen such to provide comparative values for a minimum achievable output voltage (650 V – if midpoint voltage control is not considered) and one commonly used output voltage level (800 V) of the VIENNA rectifier. It is important to bear in mind that the THI rectifier is characterized by a fixed output voltage according to the mains voltage situation (540 V). The variation of the output voltage of the VIENNA rectifier should only illustrate the modification of the selected parameters of the VIENNA in comparison to the THI rectifier. Predefined specifications of the rectifier systems which are used for benchmarking are given in **TABLE 8.1**. Results of the calculated performance indices are listed in **TABLE 8.2**. The performance parameters are chosen such, that a smaller value emphasizes a good system behaviour. One conspicuous feature of the THI rectifier are the small values of conduction and switching losses of diodes and transistors (τ_{p}). This is mainly evoked due to the fact that the active enhancement of the passive rectifier only has to process a rather small amount ($P_{\mathrm{THI}} \approx 6\,\%$, $Q_{\mathrm{THI}} \approx 16\,\%$)

TABLE 8.2: Results of calculated performance indices of a VIENNA and THI rectifier system.

		VIENNA (650 V)	VIENNA (800 V)	THI
VA Rating D.	μ_{D}^{-1}	11.94	14.7	8.43
VA Rating Sw.	μ_{S}^{-1}	3.98	4.90	4.38
Conduction Losses Sw.	τ_{c}	1.53	2.71	1.73
Switching Losses Sw.	τ_{p}	0.27	0.56	0.2
Conduction Losses D.	δ_{c}	2.53	3.12	2.09
Cap. Current Stress	ρ_{c}	0.94	1.41	0.68
Rated Ind. Power	ρ_{L}	0.24	0.15	0.15
Inv. P. D. of Ind.	$\epsilon_{\mathrm{L}}\ \left(\mathrm{dm}^3/\mathrm{kW}\right)$	0.029	0.016	0.057
System Losses	$1-\eta\ (\%)$	-	2.7	2.2

of the totally transferred active power. Additionally, it has to be considered that although rated inductor power values ρ_{L} of both circuits seem to be of similar value the implemented inductor volume ϵ_{L} of the THI rectifier is definitely higher than that of a VIENNA rectifier. This underlies the fact that the THI rectifier system requires an additional 4th inductor (due to passive rectification). This coil is electrically characterized by a 300 Hz current ripple and its size majorly defined according to the required $\mathrm{THD_i}$ for B6 standalone operation. Hence, no shrinking due to increased switching frequency is possible for the volume and design of L_{DC}. As can be read from **TABLE 8.2**, both rectifiers obviously show strong- and weak-points. Drawbacks of the THI rectifier are

- the high inductor volume, which is majorly determined due to the 300 Hz choke (which belongs to the original passive rectifier),
- the relatively large component count (four additional switching devices) compared to the VIENNA rectifier (however six switches S_{ij} of the VIENNA rectifier are stressed with switching frequency, but merely four switches $S_{\mathrm{c}\frac{\mathrm{p}}{\mathrm{n}}\pm}$ of the THI rectifier),
- the high grade of complexity of the total system
- no regulation of output voltage V_{o} (fixed according to mains voltage situation).

Especially the high complexity and the additional switches (which may lead to higher expense of the rectifier system) can be seen as rather crucial point for the decision of application. On the other hand there are numerous aspects which militates in favor of a THI rectifier system, as e.g.

+ robustness (still operable in B6 standalone mode even if injection cell has to be turned off e.g. due to malfunction) which is primarily attributed to its

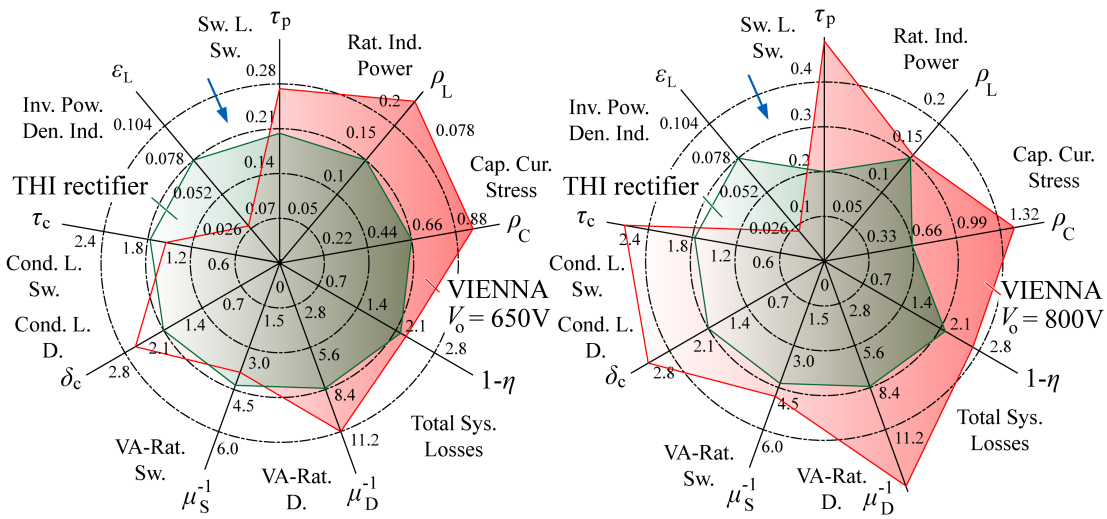


Fig. 8.2: Radar diagram (smaller values characterize a better system behaviour - indicated by blue arrow) consisting of main performance indices to allow a comparative analysis between a 10 kW VIENNA rectifier with 650 V . . . 800 V output voltage and a third harmonic injection rectifier.

+ optional implementation,
+ no high frequency common mode voltage v_{CM} at the output of the total system,
+ only semiconductors $S_{cp\pm}$ and $S_{cn\pm}$ are stressed with switching frequency,
+ the active upgrade only has to process a small amount of the total nominal power P_o,
+ and SiC MOSFETs can be used as attractive efficiency enhancement due to their good properties in bridge-leg structures.

Chapter 9

Conclusion and Outlook

In this thesis, optional active circuitry enhancements for standard B6 diode bridge rectifiers are developed and analyzed. Passive B6 rectifiers – most frequently in combination with a DC-side LC output filter – are simple and robust and widely used in industry today due to low-cost and good efficiency. However, they suffer from poor power factor and high input (mains) current harmonics (THD_i typically 48 %). In applications where very high power factor and low THD_i (i.e., $< 5\,\%$) are necessary to comply with relevant power quality standards, the B6 rectifier typically has to be completely replaced by an active rectifier (three-phase PFC) which cannot be performed in an optional manner to enhance already existing converter devices like, e.g., common drive inverters.
In order to cover all market segments (purely industrial applications as well as applications in grids with strictly limited THD_i) it would therefore be of interest to manufacture converters which are per default equipped with a standard B6 rectifier, but can be easily upgraded for low THD_i operation by an additional "option box". In this thesis several power electronic circuits have been developed and analyzed which can be used for such an optional system. All structures are based on the third-harmonic-injection (THI) principle and using terminals in general accessible in B6 rectifiers. In this work it has been shown that such an upgrade – besides optional applicability – comes with several benefits as

- robustness (due to the possible B6 standalone operation),
- no common-mode output voltage showing switching-frequency components,
- active circuit only has to manipulate active and reactive power as a fractional amount of the rectifier's total output power,
- and hence improved efficiency (in comparison to a conventional active three-phase PFC).

The developed topologies basically consist by combination of a current injection device (CID) with a current shaping network (CSN). Different circuit variants for CID and CSN implementation have been proposed:

Current Injection Device – CID

- back-to-back arrangement standard IGBTs or SiC-MOSFETs,
- parallel arrangement of reverse blocking IGBTs,
- bidirectional switch formed by a single IGBT/SiC-MOSFET and four diodes and
- bidirectional switch using two IGBTs/SiC-MOSFETs and two diodes.

Current Shaping Network – CSN

- Top. A: "Center-tapped" full-bridge stage,
- Top. B: Two half-bridge stages in a series arrangement (with optional negative voltage supply),
- Top. C: "Flying" Converter Cell (FCC) active rectifier consisting of two half-bridge stages in a series arrangement and an additional single unidirectional three-level stage,
- Top. D-F: Several back-to-back connected three-level converters (NPC, T-type, flying capacitor type) and
- Top. G: Multi-cell converter stage (according to Top. B but multiple switching cells per CSN branch, i.e., for each branch either 2 half-bridges, 2 full-bridges, N half-bridges, N full-bridges, or, advantageously, N-1 half-bridges and 1 full-bridge).

For all these systems, sets of design guidelines have been derived and analyses based on developed simulation models have been performed including control modeling and controller design. The two most promising topologies for applications in the low and medium kVA power range operated on a 400 V three-phase AC grid (Top. B and Top. C) finally have been implemented as a laboratory prototype and further analyzed regarding control, steady-state and dynamic system behaviour and parasitic effects (e.g., circulating currents during light-load and no-load operation) etc.

Each of the topologies mentioned above (Top. A - Top. G) comes with its specific advantages and drawbacks. The most-optimal circuit highly depends on the aimed application, predefined system specifications and, last but not least, to the pricing situation of the used semiconductors. (E.g. for higher power systems Top. D/ NPC might be attractive because it three-level IGBT power modules could be used which are available at rather good prices due to their wide utilization in high-power standard drives and wind power systems.)

Concerning systems of smaller power level (like 10 kVA) not only SiC-MOSFETs (Top. A-G) but also GaN semiconductor technology – presently limited to about 650 V_{DC} – seems to be attractive (due to the relative low DC voltage of the switching cell of Top. C and Top. G), e.g., GaN-Systems GS66508T or, alternatively, ROHM's 650V SiC-MOSFET SCT2120AF. This currently upcoming GaN and "low-voltage" SiC technologies would open a way for further improving efficiency or power density (by increasing switching frequency), as has been already demon-

strated by the laboratory prototype of Top. B based on 1200 V SiC-MOSFET SCT2080.
Finally, each of the proposed topologies (Top. A-G) provided proper dimensioning is characterized by unity power factor and THD_i rates complying with actual EMI regulations. Simulation results and measurements taken from the two implemented laboratory prototypes proved that $THD_i < 5\,\%$ and a power factor of $\lambda \approx 0.999$ is achievable.
Finally, it would be interesting to clarify in future research tasks if the proposed rectifier add-on concept is applicable also for passive rectifiers operating at higher grid frequencies, as e.g. used in aircraft applications ($f_N = 360 \ldots 800\,\mathrm{Hz}$). Furthermore, besides THD_i measurements also EMI tests concerning high-frequency conducted noise (tested EMI receiver and rectifier operated at a three-phase line impedance stabilization network - LISN) which may result in the requirement of an additional Hf filter stage have to be performed.

Appendix A

Notation

Abbreviations

AC	Alternating Current.
AFE	Active Front End.
ANPC	Active Neutral Point Clamped.
AVG	Averaged.
AWG	American Wire Gauge.
B6	Standard Passive Three Phase Rectifier.
BLI	Bridge Leg Inductor.
CCM	Continuous Current Mode.
CCM	Continuous Conduction Mode.
CID	Current Injection Device.
CISPR	Comite International Special des Perturbations Radioelectriques.
CM	Common Mode.
CPLD	Complex Programmable Logic Device.
CSI	Current Source Inverter.
CSN	Current Shaping Network.
CVM	Continuous Voltage Mode.
DAB	Dual Active Bridge.
DC	Direct Current.
DCM	Discontinuous Current Mode.
DCM	Discontinuous Conduction Mode.
DM	Differential Mode.
DSP	Digital Signal Processor.
DVM	Discontinuous Voltage Mode.
EMI	Electromagnetic Interference.

ESI	Electronic Smoothing Inductor.
EV	Electric Vehicle.
FC	Flying Capacitor.
FCC	”Flying” Converter Cell.
FPGA	Field Programmable Gate Array.
GTO	Gate Turn-Off.
ICOM	Intermittent Conduction Operating Mode.
IGBT	Insulated Gate Bipolar Transistor.
IPQC	Improved Power Quality Converter.
IPT	Interphase Transformer.
MC	Multi Cell.
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor.
NPC	Neutral Point Clamped.
OM	Operating Mode.
PFC	Power Factor Correction.
PWM	Pulse Width Modulation.
RMS	Root Mean Square.
SAB	Single Active Bridge.
SEPIC	Single-Ended Primary-Inductor Converter.
SiC	Silicon Carbide.
THI	Third Harmonic Injection.
VSI	Voltage Source Inverter.
Yd	Star/Delta-Transformer.
Ydy	Star/Delta/Star-Transformer.

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