DIPLOMARBEIT

Silicon-Carbide-Based Closed-Loop Class-D Power Amplifier

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Abstract

In many laboratories and electric testing centres there is a need for stable and predictive power sources providing power signals of arbitrary shape. This work presents the process of developing and realising a linear power amplifier – based on a class-D amplifier topology – applying the upcoming silicon carbide semiconductor technology. This technology is of special interest for the realisation of power sources due to its structural advantage of providing lower power losses. The developed system supports amplification of any signal sequence – coming from an arbitrary waveform generator – up to 1kHz with a maximum output voltage range of $\pm$400V and a maximum current of $\pm$10A – resulting in up to 4kW output power – at an overall physical size of approximately 2.5 litres.

The requirement for a high efficient amplifier unit demands a switching (Class-D) topology with a loss-less output filter consisting of power inductors and capacitors.

The state of the art silicon-based semiconductor technology is compared to the upcoming silicon-carbide (SiC) technology and the most important differences – that lead to the usage of the latter in the presented amplifier – are pointed out.

The chosen output filter configuration originally represents an only marginally stable system. This characteristic therefore necessitates the introduction of a feedback control structure in order to create a required overall transfer function of proper dynamic behaviour. The design requirements are fast rise and settling times, no remarkable overshoot in case of a step response, low voltage drop in case of a load step, high attenuation of the structural switching harmonics and limited current peaks in case of a square wave to avoid damaging on the semiconductor switches. Therefore, different controller concepts are developed and analysed theoretically. Based on the results, possible configurations are designed and verified by the use of common circuit simulation software. The most promising configuration – a system with a Bessel-like step response – is selected for realisation.

The realisation of the amplifier unit is described in detail. In particular, a specific unique design of the 100µH main filter power inductor is shown, which is optimized to have low core and copper losses even in case of 100kHz 10A peak ripple current. FE-simulations gained by the simulation program FEMM support the design process. A novel gate driver – based on an RF transceiver and receiver isolation concept instead of using optocouplers – is developed in order to benefit from low conduction losses and fast switching times of the SiC-MOSFETs. A PCB-layout which minimizes the parasitic inductances in the connection paths between the DC link capacitors, the semiconductor switches and the gate drivers, guarantees a nearly ideal rectangular-shaped output voltage of the MOSFET half-bridge leg supporting very fast switching speed.

The overall circuit is tested on a broad range of the defined requirements and use cases. The results of the real system corresponds well to the theoretic/simulated ones, proved by oscilloscope measurements which are included in this work. Appearing problems in the test procedures are mentioned and possible improvements are discussed. Especially a full bridge converter topology, consisting of two identic half-bridge amplifier stages, is suggested. This structure would eliminate nearly all disadvantages observed in the test procedures. In addition, it will provide benefits such as an output voltage range being twice as high as the supply voltage range.

The presented amplifier demonstrates a well-working power source and forms a development basis for further researches on this topic, e.g. covering the full bridge converter consideration.

Kurzfassung

Elektrische Laboratorien und Prüfanstalten benötigen vielfach Spannungsquellen für höhere Leistungen um Spannungen im Bereich der Netzspannung mit verschiedensten Signalverläufen bereitstellen zu können. In dieser Diplomarbeit wird der gesamte Entwicklungsprozess einer derartigen Leistungsquelle (Leistungsverstärker) beginnend beim grundsätzlichen Design bis hin zum Aufbau und den verschiedensten Testläufen dargestellt. Die Grundstruktur des Verstärkers basiert auf der des bekannten Klasse-D-Prinzips (Schaltverstärker) mit Reaktanz-Ausgangsfilter zur Unterdrückung der schaltfrequenten Signalkomponenten. Es können Eingangssignale bis zu einer Frequenz von 1kHz auf Ausgangsspannungen von ±400V und einem Ausgangsstrom von ±10A verstärkt werden, wobei das Gesamtsystem ein Volumen von ca. 2,5dm aufweist.

In der Arbeit wird eingangs die momentan in der Industrie etablierte Silizium Technologie für Halbleiterschalter der neuen, immer mehr konkurrenzfähiger werdenden Siliziumkarbid-Technologie (SiC) gegenübergestellt und die wichtigsten Unterschiede – die im konkreten Fall zum Einsatz von SiC-MOSFETs führen – aufbereitet dargestellt.

Das notwendige Ausgangsfilter besteht ausschließlich aus Induktivitäten und Kapazitäten und stellt ein somit grenzstabiles ungedämpftes System dar. Da die Dämpfung des Filters nicht über die Last erfolgt, ist es notwendig eine Regelung zu implementieren, die das Gesamtsystem stabilisiert und das gewünschte dynamische Verhalten (Transfer-Charakteristik) garantiert. Die Regelung wird optimiert auf schnelle Anstiegs- und Einschwingzeiten, auf minimales Überschwingen, geringen Spannungsabfall bei einem Lastsprung, einer hohen Unterdrückung der prinzipbedingten schaltfrequenten Harmonischen sowie der Begrenzung von Stromspitzen bei hohen Rechtecks-Ausgangsspannungen zur Vermeidung von Überströmen in den Halbleiterschaltern. Es werden verschiedene Regelungskonzepte erarbeitet und auf ihre Praxistauglichkeit untersucht, zuerst theoretisch, anschließend unter Zuhilfenahme von gebräuchlichen Schaltungs-Simulatoren. Das aus diesen Untersuchungen hervorgehende optimale Konzept – mit Bessel-ähnlicher Sprungantwort – wird für die Realisierung verwendet.

Alle notwendigen Schaltungsteile des Aufbaus sind im Detail beschrieben, insbesondere auch die Dimensionierung einer speziellen 100µH-Glättungsinduktivität für die erste Filterstufe. Diese wurde mit Hilfe der Simulationssoftware FEMM hinsichtlich möglichst geringer Verluste in Bezug auf die auftretenden Spannungs- und Stromverläufe (100kHz/10A) optimiert. Weiters wurde eine neue Gate-Treiberstufe entwickelt, welche die SiC-MOSFETs unter Verwendung eines IC-Bausteins mit HF-Signalen potentialfrei ansteuert, anstatt der üblicherweise dafür verwendeten Optokoppler. Besonderes Augenmerk wurde auf eine möglichst niederinduktive Kontaktierung der Zwischenkreiskondensatoren mit den Halbleiterschaltern gelegt, um Schaltüberspannungen am Ausgang des Halbbrückenzweiges zu vermeiden.

Der entwickelte Verstärker wurde umfangreichen Tests unterzogen. Die praktischen Messungen stimmen sehr gut mit den simulierten Ergebnissen überein. Die Arbeit beinhaltet die Mess-resultate (Oszilloskop-Messungen), ebenso erfolgt eine Diskussion der bei der Realisierung aufgetretenen Problembereiche. Zur Vermeidung dieser wird eine Verstärkerstruktur vorgeschlagen, die aus zwei Halbbrücken-Stufen besteht. Damit ließen sich praktisch alle wesentlichen Nachteile der realisierten Schaltung beheben.

Der realisierte Leistungsverstärker stellt eine gutfunktionierende Spannungsquelle dar und bietet eine vielversprechende Grundlage für weitere Forschungen und Entwicklungen auf diesem Gebiet.

Acknowledgement

Content

1 Introduction

The objective of this master thesis is to develop a single-phase high efficiency class-D power amplifier. A half-bridge amplifier followed by a lossless filter form the basic topology. The upcoming silicon-carbide (SiC) technology is compared to the state-of-the-art silicon (Si) technology and if advantageous utilized instead of Si.

1.1 Targets and Requirements

The main application of the power amplifier is to provide a 230V 50Hz sine wave without remarkable harmonics for test procedures and laboratory needs.[1] It should form an alternative for the domestic power grid. So, no remarkable voltage drop at load steps is allowed.

Furthermore, it should work over a wide voltage and frequency range for each signal type, e.g. triangle, sine, rectangle, etc. Therefore, different requirements are defined, as summarized in Table 1.1. These values only describe the minimum requirements. The target is a device that achieves the best as technologically possible.

Description	Requirements
Output voltage range	95% of U_{SV}[2]
Maximum continuous output current	$\pm 10A$
Frequency range (ideal amplification of sine wave)	0 … 1kHz
Attenuation of switching harmonics[3]	min. 50dB
Maximum overshoot at full voltage step	$< 5\%$ of U_{∞}
Maximum voltage drop at full load step[4] at peak nominal voltage	$< 10\%$ of $\hat{U}_{nom}$

Table 1.1 Requirements for the power amplifier.

The last entry in the table above describes the test criterion for avoiding voltage drops at load steps. At peak nominal voltage $\hat{U}_{nom}$, a dynamic voltage drop of max. 32,5V[5] is allowed to comply with the requirements.

At the input side, two DC power supplies with a voltage up to 400V form the power supply for the device. The input signal that has to be amplified comes from an external waveform generator.

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[1] This case is further described under nominal voltage U_{nom}.

[2] The DC power supply voltage is called U_{SV}.

[3] To meet the requirement "without remarkable harmonics" an attenuation of the switching harmonic of min. 50dB is defined.

[4] A full load step is defined as a step from 0A to 10A.

[5] $10\% \ of \ \hat{U}_{nom} = 0.1 \cdot \hat{U}_{nom} = 0.1 \cdot \sqrt{2} \cdot 230V = 0.1 \cdot 325.27V \approx 32.5V$.

Signals up to 1kHz with a maximum voltage amplitude of 2V are allowed. For auxiliary circuits a single power supply of +5V is utilized, to reduce external efforts. All input related parameters are noted in Table 1.2.

Description	Values
Supply voltage U_{SV}	± 400V
Input voltage range u_{in}	-2V ... $+2$V
Input frequency range f_{in}	0 ... 1kHz
Supply voltage for auxiliary circuits U_{AV}	$+5$V

Table 1.2 Defined input parameters.

1.2 Guideline through the Work

After declaring the targets and requirements in section 1.1, chapter 2 first describes the theoretical basics of the used amplifier topology and following each part of the amplifier is analysed with regard to the requirements. Problems and tasks for realising a proper filter are brought out clearly. Differences between the Si and SiC technologies are pointed out and the most important facts are explained in detail. In addition, a short outlook in current semiconductor research activities is given.

Chapter 3 provides four different design approaches for a feedback control that create the required transfer characteristic. Based on a theoretical analysis, the configuration with the most promising characteristics of each approach is simulated in a circuit simulator software. The most important parameters – step response rise and settling time, voltage drop, attenuation of the switching harmonic, peak value of the filter input current – are extracted and compared. The configuration with the best overall results is choosen for realisation.

Chapter 4 and chapter 5 describe the implementation of the overall system. Chapter 4 provides an overview of the filter related parts, especially the procedure for self-designing a power inductor is given more in detail. Chapter 5 shows all relevant circuit and sub-circuits and mentions the circuit design considerations. The overall circuit is tested extensively and the results are compared to the theoretic/simulated ones.

Chapter 6 picks up the appeared disadvantages and gives opportunities to improve the overall system. An extended circuit topology – based on the realised one – that eliminates most disadvantages is suggested and simulation results are presented to prove the assumptions.

2 Fundamentals and Current State of Technology

2.1 Amplifier Topology – Modulation Concept

The amplifier topology is similar to a standard Class-D amplifier. An input signal is compared with a triangular signal generated by an on-board triangular wave generator. The comparator creates a rectangular signal with variable pulse width. Therefore, this concept is called Pulse-Width-Modulation (PWM).

Two switches in half-bridge topology amplify the resulting signal. At the end a low-pass filter is placed to attenuate the switching frequency harmonics. In cost sensitive devices, this filter may be omitted. See Figure 2.1.
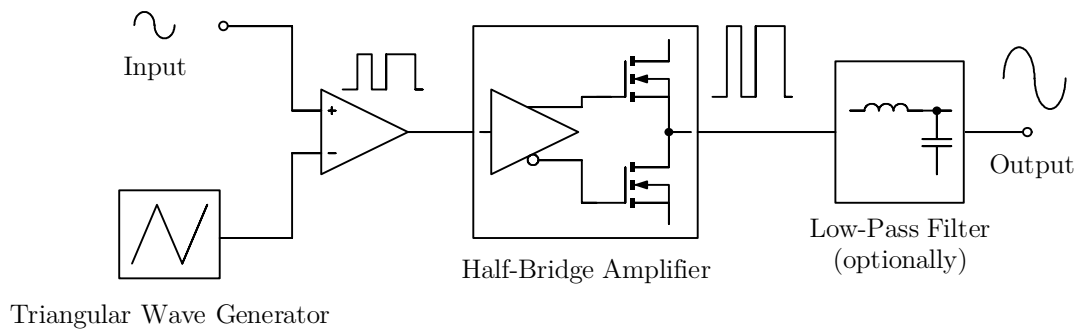

Figure 2.1 Block diagram of a Class-D Amplifier, based on [1, p. 2204].

This concept is proven, well established, and for instance today often used in the audio industry. There the PWM signal either is directly (without low-pass filter) or with a cheap low-pass filter connected to the loudspeaker. The first variant is possible because the loudspeaker dynamics and the human ear act as the required low-pass filter.

In case of this work, however, the output filter is essential to maintain an amplified output signal without substantial harmonics. Therefore, attention is turned especially to the filter design.

For better understanding of the modulation concept, Figure 2.2 shows a sine wave that is compared with a triangular signal and the generated amplified (by the factor of 2) PWM signal.
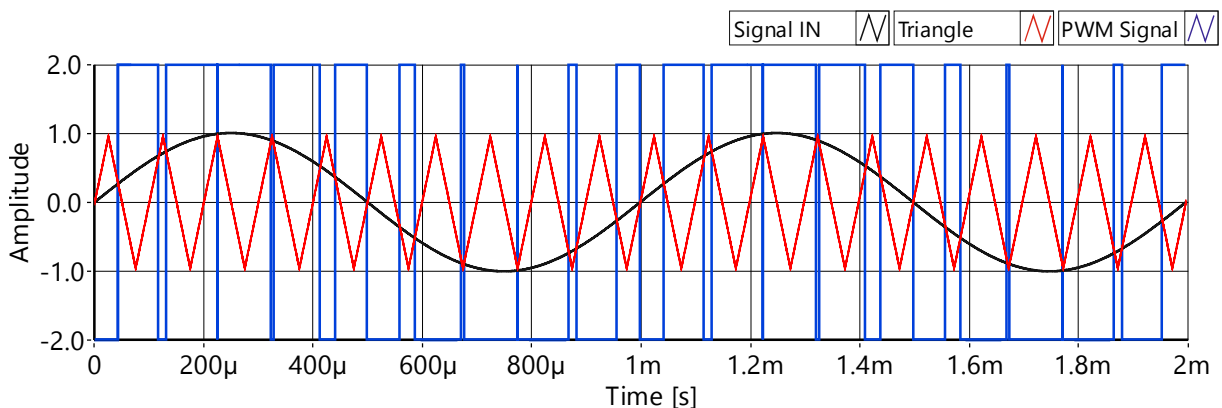

Figure 2.2 Illustration of the function principle of a Class-D amplifier.

The most attractive advantage is its high efficiency, e. g. $\eta = 93\%$ of a 200W amplifier [2]. That means cost savings caused by reduced energy consumption and smaller heat sinks. This also leads to smaller amplifier devices, especially important in portable devices such as music players.

2.2 Analysis of Different Low-Pass Filters

As mentioned above, special effort has to be spent on the filter unit after the half-bridge amplifier to prevent high frequency switching harmonics on the output signal. In this section, different filters are analysed to match the defined requirements. First the frequency responses and the step responses are analysed and after this the realisation of the best match is described.[1]

2.2.1 Ideal Low-Pass Filter

The frequency response of an ideal low-pass filter is characterized by a sharp edge at the cutoff frequency. So, the filter ideally rejects all higher frequency parts. It represents, however, a non-causal system – input signals of the future influence the present output signal. The step response is characterized by raising oscillations before the step is introduced – it is a non-causal system – an amplitude of 0.5 at the step and a decaying oscillation after the step, see Figure 2.3.
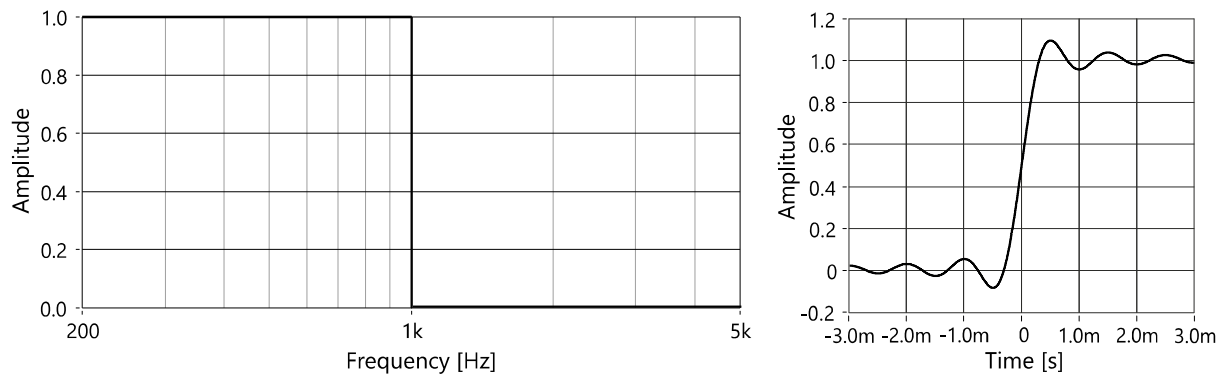

Figure 2.3 Ideal low-pass filter (cutoff frequency 1kHz) and its step response.

At a cutoff frequency of 100kHz the step response is equal, only the time range is divided by 100.
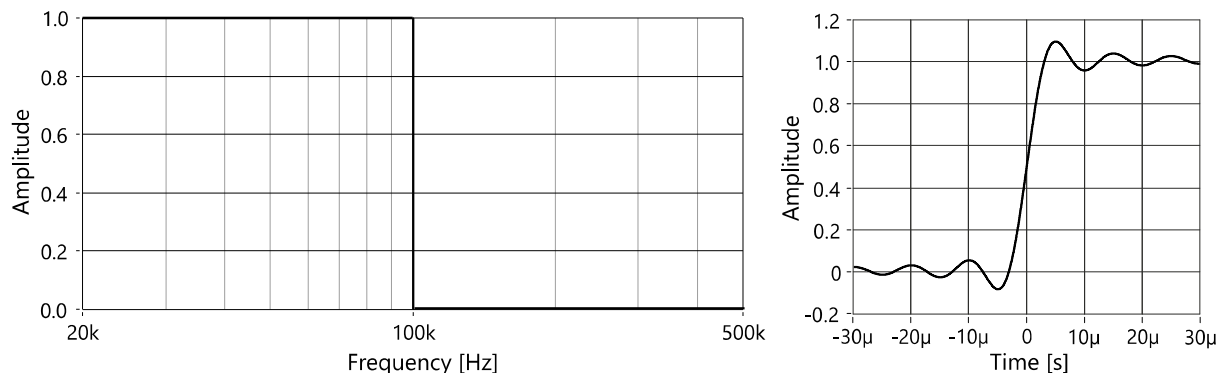

Figure 2.4 Ideal low-pass filter (cutoff frequency 100kHz) and its step response.

This filter cannot be realised due to its non-causal character. It gives, however, an overview about the dynamic of low-pass filters with cutoff frequencies between 1 and 100kHz. In the 100kHz case the step response shows a rise time of approximately 8μs. For possible cutoff frequencies in the range of 10kHz therefore rise times of 80-100μs can be expected.

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[1] All filters are simulated with National Instruments's LabView 2013.

2.2.2 Butterworth Filter

This filter is designed to have a frequency response as flat as possible in the passband, which is beneficial for a good amplitude response up to 1kHz. At the cutoff frequency[1], the frequency response rolls off at multiples of -20dB/decade, depending on the order, e. g. -40dB/decade for a second order filter, see Figure 2.5.
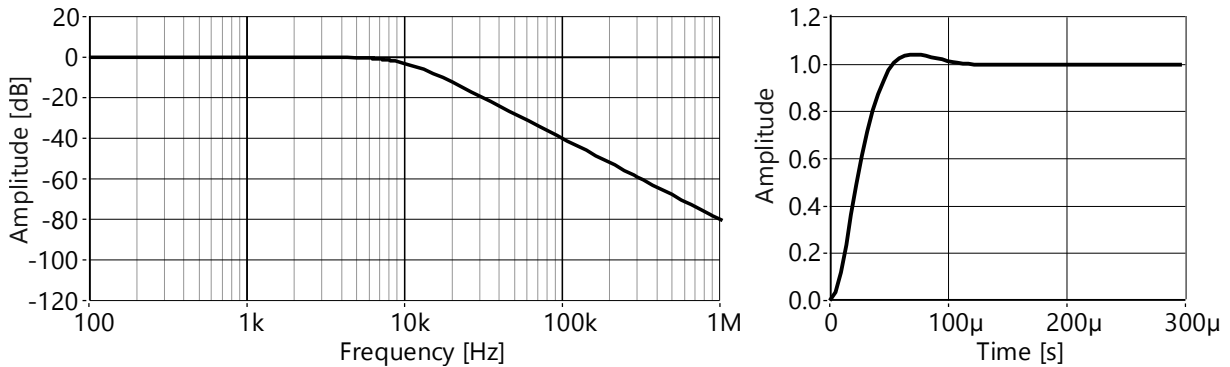
Figure 2.5 Butterworth filter (2nd order, cutoff frequency 10kHz) and its step response.

The step response is much better than for the ideal low pass filter. Less overshoot of 1.05 of the desired amplitude is achieved. On the other hand, the attenuation of higher harmonics is not satisfying. A high switching frequency would be necessary. For instance, a 100kHz switching frequency will be attenuated only by $\frac{1}{100}$. At ± 400V supply voltage, this means a sine wave with an amplitude of approximately 5V on the output signal. That is not acceptable as defined in the requirements. A solution could be an increase of the filter order. Figure 2.6 shows a 4th order Butterworth filter.
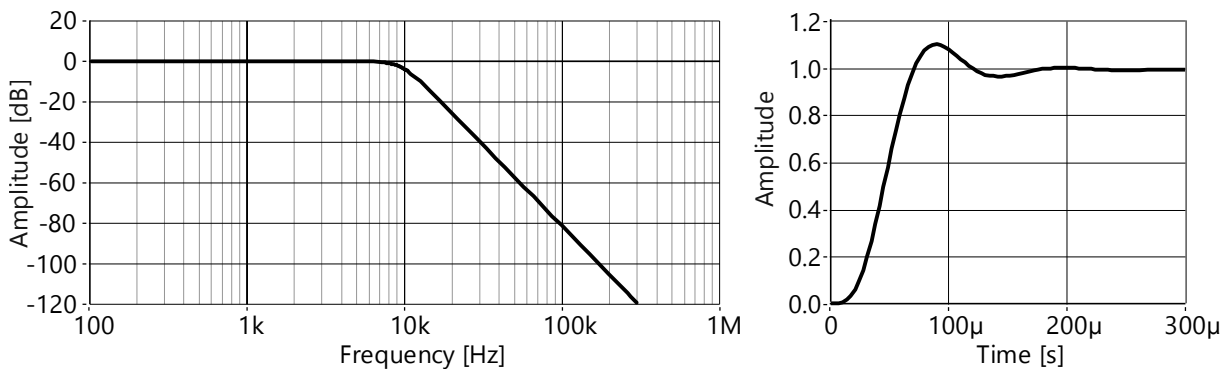
Figure 2.6 Butterworth filter (4th order, cutoff frequency 10kHz) and its step response.

Here the attenuation is -80dB/decade. Compared to the former example, now the amplitude of the 100kHz sine wave is only 50mV, which is excellent. In the step response, however, the overshoot increases at above 1.1 of the desired amplitude and the settling time nearly doubles to 200µs.

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[1] Cutoff frequency is defined as the frequency for which the attenuation of the circuit is 3 dB.

2.2.3 Bessel Filter

A Bessel filter is an analogue linear filter with a maximally flat group/phase delay, which preserves the wave shape of filtered signals in the passband. It has nearly no overshoot which makes it interesting for this purposes. The frequency response is not as flat in the passband and the attenuation not as sharp in the stoppband as in the Butterworth filter. This means less than -20dB/decade per order. Figure 2.7 shows a 4th order Bessel filter of with a cutoff frequency of 10kHz.
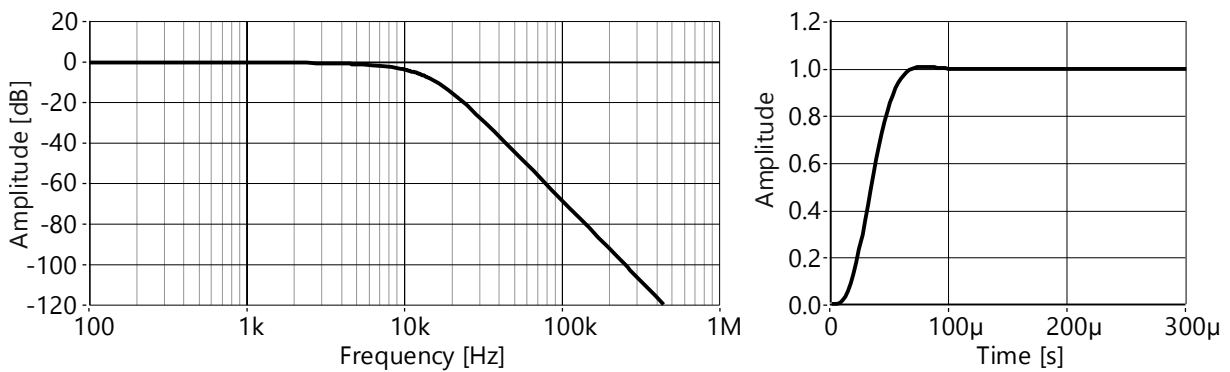

Figure 2.7 Bessel filter (4th order, cutoff frequency 10kHz) and its step response.

At a switching frequency of 100kHz the attenuation is more than 60dB so that the requirement is met. That represents a 100kHz sine wave with an amplitude of 0.5V corresponding to the former example. The step response looks extremely good, with no remarkable overshoot in this resolution. The attenuation in the passband is also nearly zero for frequencies up to 1kHz.

2.2.4 Filter Comparison, Assessment and Decision

The analysed filters with their characteristics are compared for allowing final decision.

Parameters	Ideal Low-Pass 100kHz	Butterworth 2nd order	Butterworth 4th oder	Bessel 4th order
Attenuation at 100kHz	++	−	+	+
Voltage Step Overshoot	−	o	−	+
Voltage Step Curve Shape[1]	−−	o	−	++

Table 2.1 Comparison of the analysed filter types
(++ excellent, + good, o fair, − weak, −− poor)

The Bessel filter complies with all requirements specified for the filter unit and therefore it is selected for the further activities.

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[1] The parameter "curve shape" describes a behaviour such as oscillations (damping factor, duration…) and the dynamic of the step response (rise time, settling time, …).

2.2.5 LC Low-Pass Filter Basics

For the realisation of the required filter some aspects have to be taken into account. First, it has to be a passive filter without operational amplifier, and second, resistors are prohibited to avoid remarkable losses.

Figure 2.8 shows a possible topology of such a filter, consisting of an inductor and a capacitor. Each of them represents an energy storage, so this basic element forms a second order filter.
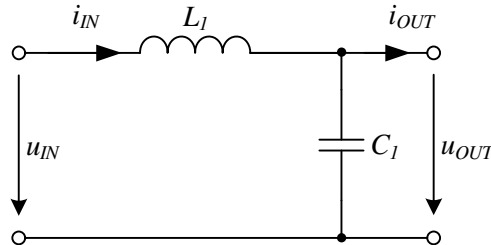

Figure 2.8 Basic element of a 2nd order LC low-pass filter, based on [3, p. 2].

Equation (2.1) shows the circuit's transfer function. It looks similar to the well-known damped oscillation function, but the damping factor, here ξ is zero. Therefore, this structure represents an undamped oscillation with a defined resonance frequency ω_0.

$$G(s) = \frac{U_{OUT}(s)}{U_{IN}(s)} = \frac{1}{1 + s^2 L_1 C_1} = \frac{1}{1 + 2\xi \frac{s}{\omega_0} + \frac{s^2}{\omega_0^2}} \quad \rightarrow \quad \xi = 0, \omega_0 = \frac{1}{\sqrt{L_1 C_1}} \quad (2.1)$$

Figure 2.9 illustrates the frequency response for a filter with $L_1 = 10\text{mH}$, $C_1 = 1\mu\text{F}$. The resonance point is found at an angular frequency of 10krad/s. The poles of that marginally stable system are showed in the Pole-Zero diagram aside.
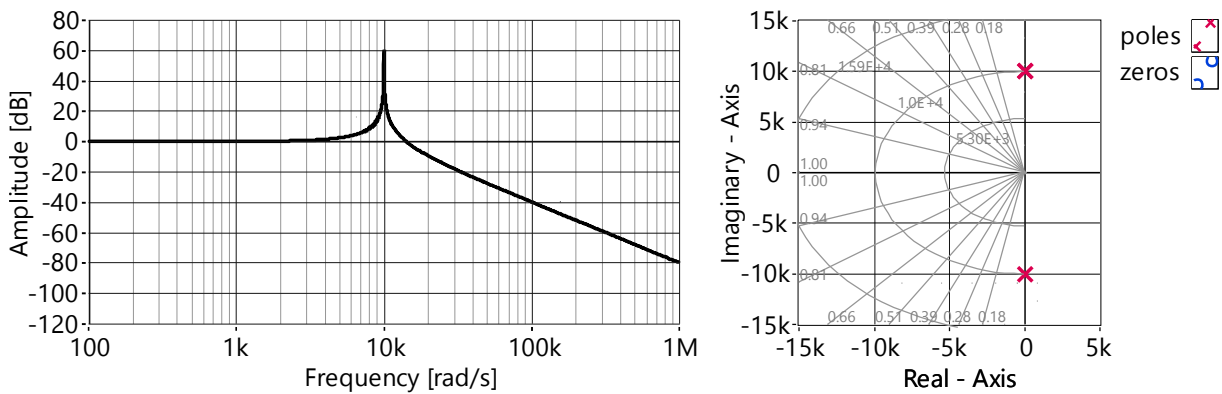

Figure 2.9 Frequency response of a 2nd order LC low-pass filter, with Pole-Zero diagram.

By changing the inductance or the capacitance, it is only possible to change the resonance frequency but not the curve shape. For stabilization reasons, however, it is necessary to change the transfer function. A possibility is to introduce damping resistors, but, as explained, this would lead to losses and because of that to a generation of undesired heat.

An important characteristic of the filter also is the input current i_{IN}[1] in the step response case and the voltage drop of the output voltage in case of a load step.

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[1] The input current i_{IN} is that current which has to be delivered by the half-bridge amplifier.

Equation (2.2) shows the transfer function of the input current and equation (2.3) the related step response in time domain.

$$G(s) = \frac{I_{IN}(s)}{U_{IN}(s)} = \frac{1}{\sqrt{\frac{L_1}{C_1}}} \cdot \frac{s \cdot \frac{1}{\sqrt{L_1 C_1}}}{s^2 + \frac{1}{L_1 C_1}} \tag{2.2}$$

$$i_{IN}(\tau) = \frac{1}{\sqrt{\frac{L_1}{C_1}}} \cdot \sin\left(\frac{\tau}{\sqrt{L_1 C_1}}\right) \quad \text{for } U_{IN}(s) = \frac{1}{s}V \tag{2.3}$$

The important parameter here is the characteristic impedance[1] $\sqrt{\frac{L_1}{C_1}}$, which determines the maximum current. If it is small, a high current will appear which might damage the semiconductor switches.

On the other hand, the voltage drop of the output voltage in case of a load step is analysed. The initial condition for this case is a charged capacitor at the value of the input voltage, so that the input current is equal to zero. Then a load step is introduced. Equation (2.4) shows the response in time domain.

$$u_c(\tau) - u_{IN} = -Z_1 \cdot \sin\left(\frac{\tau}{\sqrt{L_1 C_1}}\right) \quad \text{for } I_{OUT}(s) = \frac{1}{s}A \tag{2.4}$$

Again the term Z_1 occurs, however here, a small value of Z_1 is desired to maintain a small voltage drop. This might be a first constraint, holding the input current small by accepting a higher voltage drop at the output. Equation (2.5) summarizes the conflict.

$$(input\ current\ consideration) \quad a < Z_i < b \quad (voltage\ drop\ consideration) \tag{2.5}$$

In section 2.2.3 a 4th order Bessel filter was proposed. Figure 2.10 shows a simple way to get a 4th order filter by doubling the basic filter element.
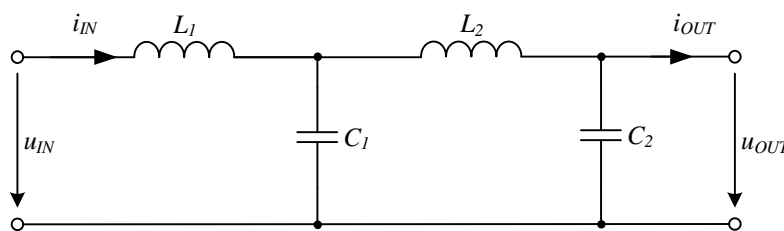

Figure 2.10 4th order passive LC-network.

Equation (2.6) shows the calculated frequency response.

$$G(s) = \frac{U_{OUT}(s)}{U_{IN}(s)} = \frac{1}{1 + s^2(L_1 C_1 + L_2 C_2 + L_1 C_2) + s^4(L_1 L_2 C_1 C_2)} = \frac{1}{\left(1 + \frac{s^2}{\omega_1{}^2}\right)\left(1 + \frac{s^2}{\omega_2{}^2}\right)} \tag{2.6}$$

Important is that $\omega_1{}^2 \neq \frac{1}{L_1 C_1}$ and $\omega_2{}^2 \neq \frac{1}{L_2 C_2}$. It comes to a spread of the resonance frequencies. Figure 2.11 shows a filter with $L_1 = 10\text{mH}, C_1 = 1\text{μF}, L_2 = 100\text{μH}, C_2 = 1\text{μF}$. If this filter is

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[1] From now, the symbol Z_i is used instead of $\sqrt{\frac{L_i}{C_i}}$.

considered as two separate LC filters 2nd order, the resonance frequencies are located at 10krad/s and 100krad/s[1]. In the connected case, however, the new resonance frequencies are 7,06krad/s and 141,6krad/s.
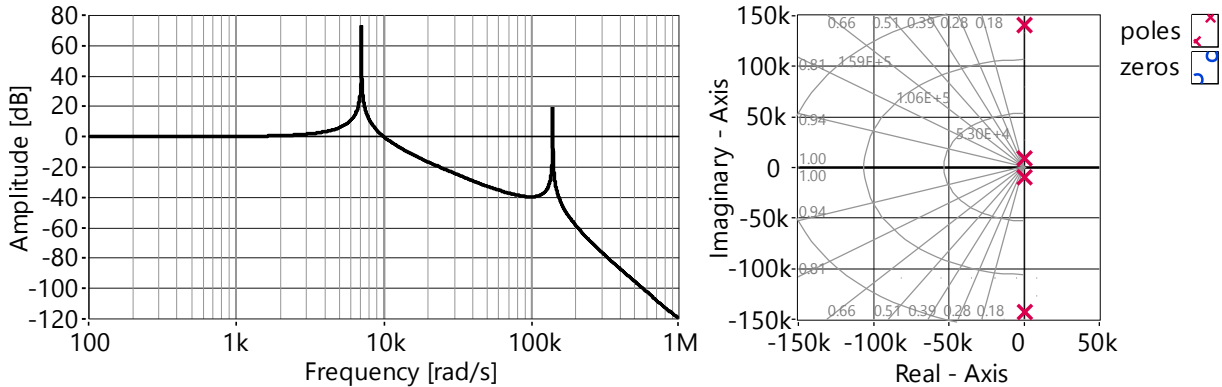

Figure 2.11 Frequency response of a 4th order LC low-pass filter, with Pole-Zero diagram.

Beside Z_1, here also Z_2 influences the input current and the voltage drop in the discussed response cases. Here, however, exists a possibility to solve that conflict by placing Z_1 at the input side higher and Z_2 at the output side lower. So C_1 contributes its charge to hold the voltage drop lower in case of a load step. On the other hand, L_2 holds the maximum input current lower in case of a voltage step.

Table 2.2 summarizes all filter related requirements. It is evident that there are three main factors. The transfer function, high switching frequency and the factors Z_i.

Requirement	Value	Key factors
Stability	✓	transfer function
Attenuation of the switching harmonic	min. 50dB	transfer function, switching frequency
Amplification 0 … 1kHz	const.	transfer function
Maximum overshoot at full voltage step	$< 5\%$ of U_∞	transfer function
Maximum voltage drop at full load step at nominal voltage	$< 10\%$ of U_{nom}	Z_i
Maximum input current at full voltage step	See specifications of switches	Z_i

Table 2.2 Filter requirements and key factors.

The terms Z_i can be easily adjusted by placing L and C. For the desired transfer function, however, an external controller is needed, because it is prohibited to influence the LC transfer function directly with resistors or other active elements.

A high switching frequency requires switches that can deal with them. How to find applicable switches will be discussed in the next chapter.

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[1] This consideration would only be valid if a voltage follower is placed between the filter elements.

2.3 Switches

After the determination of the related requirements, switches are searched and compared. Later switches in SiC technology are analysed and the most suitable switches for this application are chosen.

2.3.1 Switch Related Requirements

Two requirements are already identified: High switching frequency in the 100kHz range and high pulse current capability. A third important requirement is the Drain-Source voltage U_{DS}. Which value is necessary is pointed out in Figure 2.12.
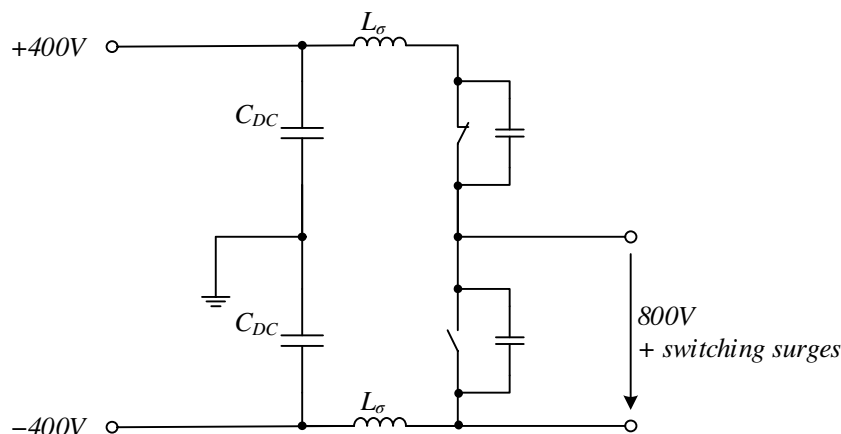

Figure 2.12 Half-Bridge Topology, blocking voltage at worst-case scenario.

If the High-Side switch conducts, the full +400V lies at the output and so 800V at the Low-Side switch. Additionally, switching surges have to be considered. These oscillations occur because of parasitic inductances and capacities and have to be minimized[1]. Therefore, the challenge is to place the DC link capacitors C_{DC} as near as possible to the switches to reduce the wiring inductance L_σ. If necessary, there can be introduced different snubber circuits but this means also losses and so the aim is to well design the Printed Circuit Board (PCB) and avoid snubber. Nevertheless, oscillations have to be expected and therefore the MOSFET voltage stress is calculated with a factor of 1.5. That means a U_{DS} of 1200V.

Another criterion is the maximum continuous current. In the requirements ±10A are declared. For safety reasons the chosen switch should have at least an I_D of 15A.

The last criterion is a fast switching time. This criterion is derived by the first entry of Table 1.1. This requirement implies a maximum duty cycle of 95% or a minimum duty cycle of 5%. At a switching frequency of 100kHz – 10μs per period – 5% represents 500ns. To provide a rectangular shape, even in this case, a maximum switching time of 100ns is allowed.

Consequently, for the selection of a proper switch five values have to be considered. $U_{DS} = 1200$V, $f_s = 100$kHz, I_{PULSE} as high as possible, $I_D > 15$A and a switching time lower than 100ns.

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[1] Attention has to be paid to the analogy with the former discussed LC structure, where undamped oscillations have been discussed. In reality, also the conductive copper path forms a resistance, so that it is more a weakly damped oscillation.

2.3.2 State of the Art Si Switches

In Figure 2.13 typical area boundaries of Si switches are showed. In alignment with the requirements, the MOSFET or the IGBT technology can be used. The limit of the MOSFET technology may be the blocking voltage and for the IGBT the limit is the switching frequency. The IGBT's conduction losses are small and the switching losses are high compared to the MOSFET technology. For this reason, a MOSFET would be preferred, especially if there are types with low conduction resistance to reduce the related on-state losses.
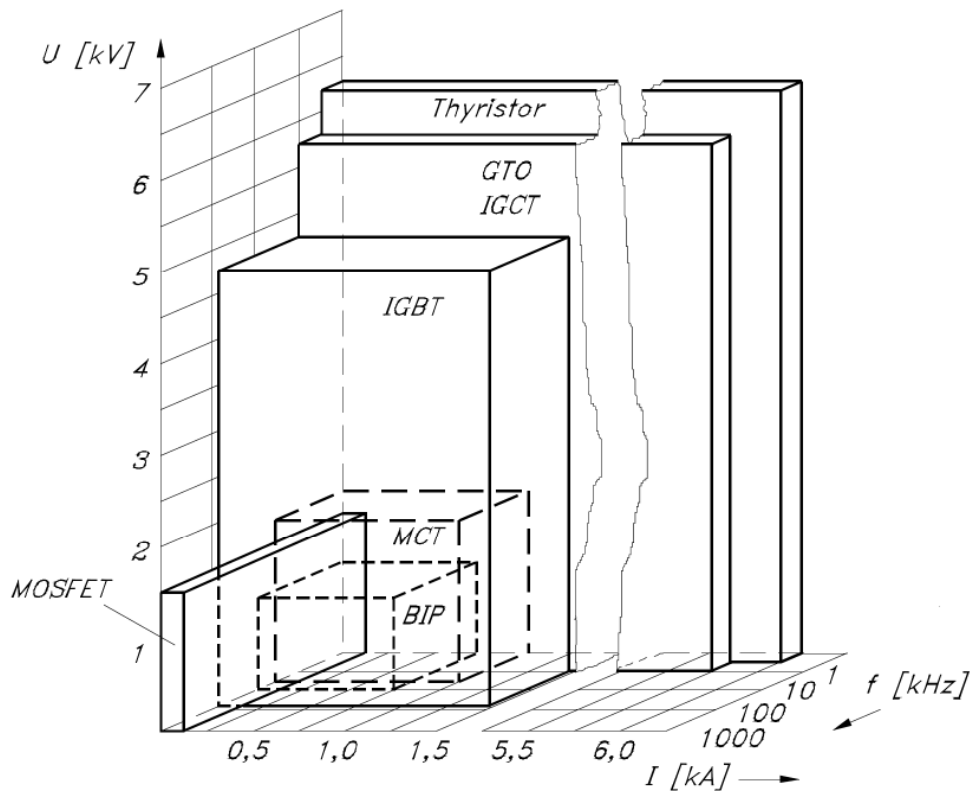

Figure 2.13 Typical area boundaries of silicon semiconductor power switches [1, p. 631].

Table 2.3 shows values for the two selected technologies. Cleary visible is the high conduction resistance of the 1500V MOSFET technology. On the other hand, the IGBT works not loss-optimal at high frequencies and therefore it is only described till ~20kHz.

Properties	MOSFET 500V	MOSFET 1500V	IGBT
Maximum Voltage	−	o	+
	500V	1500V	>3500V
Maximum Continuous Current	o	−	+
	75A	8A	>1000A
Maximum Switching Frequency	+	+	o
	100kHz	100kHz	>20kHz
Maximum Switching Time	+	+	o
	600ns	200ns	2300ns
Conduction Resistance	+	−	+
	100mΩ	1900mΩ	60mΩ

Table 2.3 Comparison of silicon MOSFET and IGBT (+ good, o fair, − weak) [1, p. 630].

2.3.3 SiC MOSFET Technology

In recent time, industry has introduced new SiC MOSFETs at acceptable prices. There are different crystal structures for SiC base material but now the 4H-SiC structure is commonly used to manufacture SiC MOSFETs. [4],[5] Table 2.4 compares the physical parameters.

Properties	Si	4H-SiC
Bandgap E_g [eV]	1.12	3.23
Lattice Const. [Å]	a = 5.43	a = 3.09 c = 10.05
Critical Field E_c [MV/cm]	0.25	3
Electron Mobility μ_n [cm²/Vs]	1450	900
Hole Mobility μ_p [cm²/Vs]	500	120
Dielectric Constant ε_r [1]	11.9	9.66
Thermal Conductivity [W/cmK]	1.56	3.5-5.0

Table 2.4 Comparison of Si and SiC properties [6],[7].

The bandgap of SiC is nearly three times higher than the Si one, a disadvantage at the first sight, because of the expectable higher forward voltages at the basic pn junction. The biggest difference is the 10 times higher critical electric field strength. The carrier mobilities are worse but differ not as much as E_c.

A look at the MOSFETs basics helps to understand which influences have all these differences. Figure 2.14 shows the basic vertical MOSFET structure.[1]
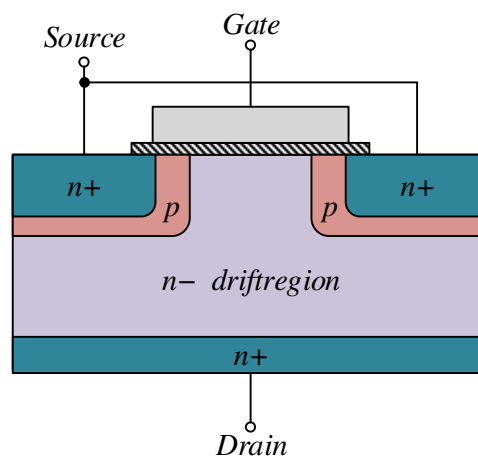

Figure 2.14 Vertical MOSFET with the blocking voltage determining n— driftregion.

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[1] Without further information about the mode of action it is directly discussed the influence of E_c.

The total blocking voltage is located at the n− driftregion. It has to be built as long as necessary to block that voltage. This manner has significant influence to the conduction resistance R_{dson} of the MOSFET.
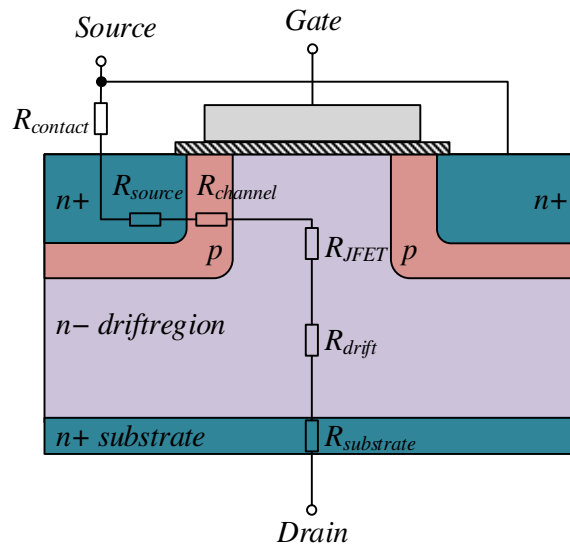

Figure 2.15 Illustration of the resistances in the vertical MOSFET, based on [1, p. 684]. The accumulation layer resistance and the intrinsic junction FET resistance is here combined as R_{JFET}.

In Figure 2.15, the individual resistance parts, which form the R_{dson}, are analysed. Literature studies show that R_{drift}, the resistance of the n− driftregion, counts for almost the whole resistance. The drift zone of a conventional power MOSFET with a blocking voltage of 600V counts for approximately 95% of the total R_{dson} [8]. So, this is the region which should initially be improved to reduce the overall resistance.

2.3.4 Calculation of the Drift-Resistance

Figure 2.16 shows the basic vertical MOSFET structure with the electric field distribution inside homogenously doped regions.
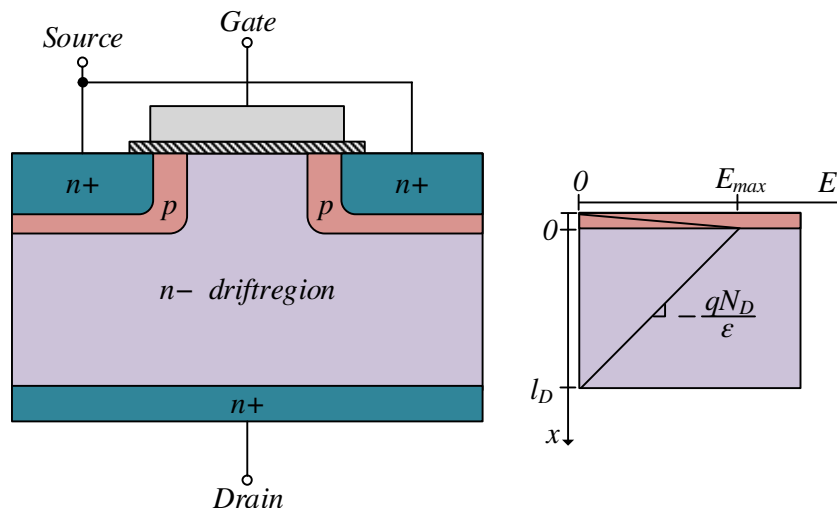

Figure 2.16 Simplified illustration of the electric field gradient in the n− driftregion.

Based on the Poison equation

$$\Delta\varphi(x) = -\frac{\rho(x)}{\varepsilon} \tag{2.7}$$

the assumption of homogenous doping and the permission to reach the maximum electric field strength $E_{max} = E_c$ results in

$$E(x) = -\frac{qN_D}{\varepsilon} \cdot x + E_c \; . \tag{2.8}$$

The Breakdown Voltage U_{BR} is defined as the integration of the electric field over the length of the driftzone, which is the represented as the area under the electric field curve.

$$U_{BR} = \int_0^{L_D} E(x)dx \tag{2.9}$$

After inserting of (2.8) in (2.9) follows

$$U_{BR} = E_c \cdot l_D - \frac{qN_D}{2\varepsilon} \cdot {l_D}^2 = \frac{E_c \cdot l_D}{2} \; . \tag{2.10}$$

Without doping U_{BR} depends only on the length of the driftregion. A high N_D otherwise decreases U_{BR} but improves the conduction and so the resistance of the driftregion[1].
Under the restriction of low resistance at a given U_{BR} first the resistance R_{drift} or better the factor $R_{drift} \cdot A_{chip}$ is analysed [9, p. 14]

$$R_{drift} \cdot A_{Chip} = \frac{l_D}{qN_D\mu_n} \tag{2.11}$$

(2.10) inserted in (2.11) results in

$$R_{drift} \cdot A_{Chip} = \frac{{l_D}^3}{2\varepsilon q\mu_n(E_s l_D - U_{BR})} \tag{2.12}$$

According to C. Hu et al. [10] $R_{drift} \cdot A_{chip}$ can be minimized with (2.13)

$$l_D = \frac{3 \cdot U_{BR}}{2 \cdot E_c} \tag{2.13}$$

to the following important relationship

$$\boxed{R_{drift} \cdot A_{Chip} = \frac{27 \cdot {U_{BR}}^2}{8\varepsilon\mu_n {E_c}^3}} \tag{2.14}$$

This equation shows that the resistance at a given U_{BR} is proportional to the inverse of the cube of E_c. For instance, that means if E_c increases by 10, $R_{drift} \cdot A_{chip}$ decreases by the factor of 1000! Nearly this scenario is given in the comparison of Si and SiC. It was described that R_{drift} counts for ~95% of the whole R_{dson} in Si technology. Ideally considered in SiC technology this part is now in the range of the other resistance parts or even below. So the biggest disadvantage of a MOSFET at high breakdown voltage is eliminated.

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[1] N_D and l_D here interdepend.

2.3.5 SiC Diodes

Forward voltage of a SiC pn junction is in the range of 2-3V [11]. Instead, SiC-Schottky-Diodes have a much lower forward voltage because of the lower barrier-height. Forward voltages of 1.5V can be achieved [10]. Figure 2.17 shows a comparison of Si and SiC diodes specified for 4A and 600V.
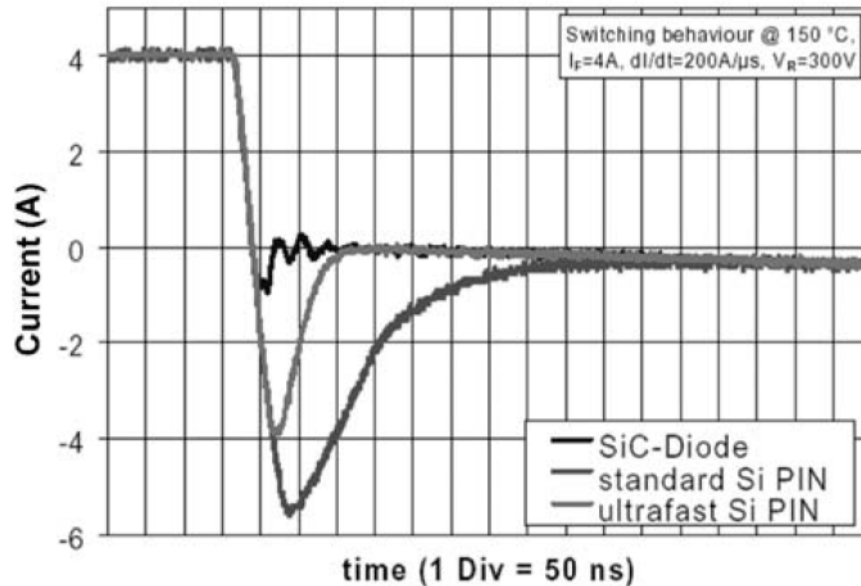

Figure 2.17 Comparison of the switching behaviour of three diodes with the same specifications 4A/600V [11, p. 689].

The advantage is evident. In the PIN diode cases first minority charge carriers have to be injected into the intrinsic zone for low conduction losses. At turn-off – see Figure 2.17 – these carriers have to recover which increases the turn-on losses of the MOSFET.

In the MOSFET case there exists a built-in body diode, a basic pn junction. It was mentioned that for this diode the forward voltage is in the range of 2-3V, higher than in the Si technology. At first view this is a disadvantage. At the second by placing antiparallel an external diode with lower forward voltage this represents a big advantage. The external diode SiC-Schottky-diode with much better characteristics conducts already at lower voltages and eliminates so the worse built-in diode.

Summarized, two major advantages of SiC MOSFETs compared to Si MOSFETs exist. First the lower R_{dson} because of the higher critical field strength and second the possibility to use an optimized external antiparallel diode to reduce switching losses.

Researchers and experts in the industry also support this expertise. For example, according to Schröder [11, p. 695] under 3kV SiC structures are strongly recommended.

2.3.6 Comparison of MOSFET Alternatives

Two SiC MOSFETs are selected for comparison. CREE's C2M0080120D combined with Cree's C4D08120 Schottky Diode and ROHM's SCH2080KE with built-in Schottky-Barrier-Diode (SBD). They are compared with an optimized Super Junction silicon MOSFET, STFW6N120K3 from ST Microelectronics, with equal breakdown Voltage U_{BR}.

Properties	C2M0080120D	SCH2080KE	STFW6N120K3
Technology	SiC	SiC	Si
Drain-Source Voltage[1] U_{DDS} [V]	1200	1200	1200
Continuous Drain Current I_D @ 25°C [A]	31.6	40	6
Gate Source Voltage U_{GS} [V]	-10 / $+25$	-6 / $+22$	$\pm$ 30
Drain-Source ON Resistance R_{dson} [mΩ]	80	80	1950
Total Gate Charge Q_g [nC]	49.2	106	39
Turn ON Time [ns]	41.6	70	42
Turn OFF Time [ns]	35.8	98	90

Table 2.5 Comparison of different 1200V MOSFETs [12] [13] [14].

The difference of the R_{dson} between the two SiC MOSFETs compared to the Si MOSFET is evident, but not as huge as expected. The ST-MOSFET, however, is a silicon Super Junction MOSFET, with many improvements compared to the simple vertical structure, so that the ratio is only 25. A second notable difference can be seen in the comparison of the antiparallel diode. The reverse recovery charge Q_{rr} is much higher than in the SiC variants, see Table 2.6. This leads to higher switching losses proportional to the difference of Q_{rr}. Between the individual SiC MOSFETs the differences are marginal compared to the Si MOSFET. The CREE part has lower turn-on and turn-off times and the half total gate charge. The extra diode has also better properties than the built-in one in the ROHM device. On the other hand, in the latter case only a single semiconductor device has to be considered in the layout and so it can be optimized with regard to disturbances produced by high $\frac{du}{dt}$ values which may disturb the feedback control unit. The higher switching times of the ROHM device are not a big problem. Related to a maximum switching frequency of 100kHz – 10μs per period – <100ns turn off time is less than 1% and complies with the former declared requirements.

Properties	C4D08120	SCH2080KE	STFW6N120K3
Forward Voltage U_{SD} [V]	1.5	1.3	1.6
Forward Current I_D @ 25°C [A]	24.5	40	6
Reverse Recovery Charge Q_{rr} @ 400V [nC]	27	60	9000

Table 2.6 Comparison of the antiparallel Diode combined with the MOSFETs [13] [14] [15].

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[1] In datasheets often V is used for voltage instead of U. In this thesis always U is used for voltage.

2.3.7 Perspectives of SiC MOSFETs

Section 2.3.4 showed that the resistance of the n− driftregion in the SiC technology is in the range of the other resistance parts or even below. So, for a further reduction of R_{dson} the next challenge is to reduce the other resistance parts. One way is the introduction of a trench structure, as shown in Figure 2.18.
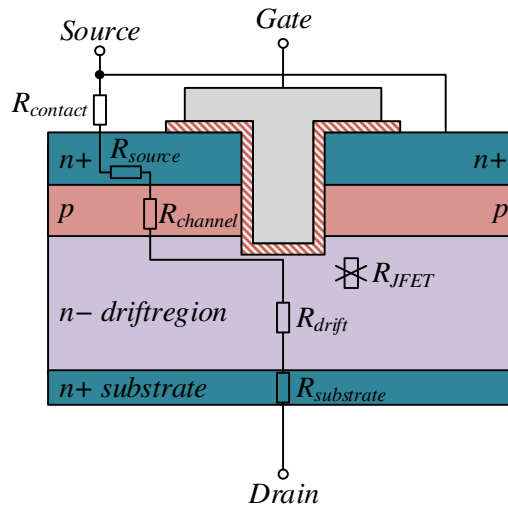

Figure 2.18 MOSFET with trench structure and eliminated R_{JFET}.

The main reason is the elimination of R_{JFET}. This is an already used and common structure, for example in Si-IGBTs [16]. There, the $U_{CE,sat}$ could be reduced by 30% after introducing a gate trench structure.

For MOSFETs in SiC technology the company ROHM has introduced a double trench structure in their 3rd generation SiC MOSFETs [17]. By using only a single trench the electric field strength locally would be too high, which would cause damages in the insulating layer, see Figure 2.19.
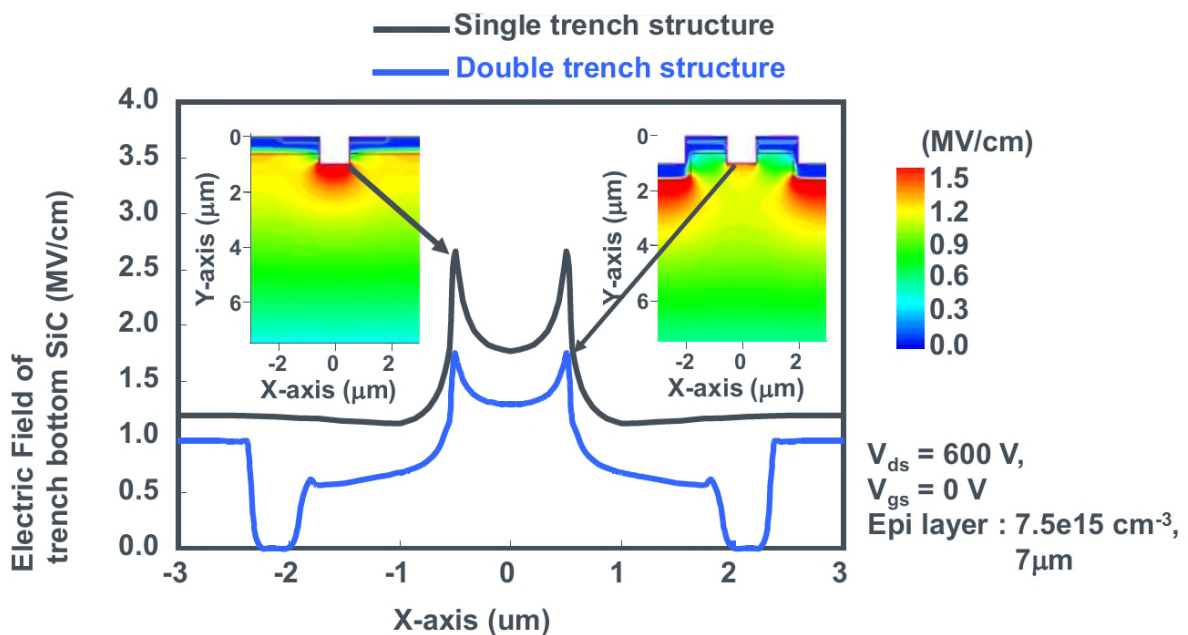
Figure 2.19 Comparison of single and double trench structures in a vertical MOSFET [17].

2.4 Assessed Circuit Topology

The considerations of chapter 2, result in the following circuit scheme.
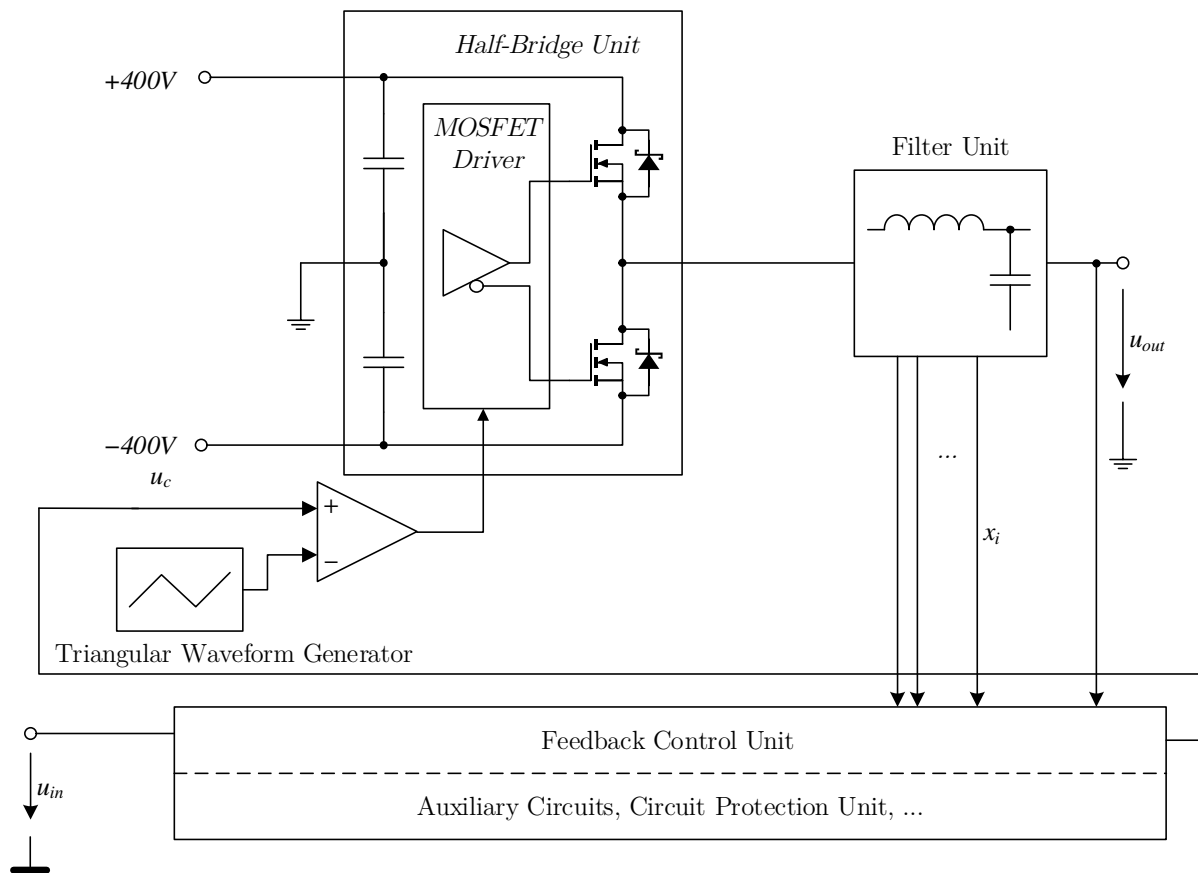
Figure 2.20 Resulting circuit topology with all related units.

The total device is split-up in three major units with their individual tasks:

o	Half-Bridge Unit	Power amplification of the input PWM signal
o	Filter Unit	Lossless filtering of the switching harmonic
o	Feedback Control Unit	Stabilisation of the filter and generation of a desired transfer function

Problems related with the Half-Bridge Unit und the Filter Unit have been already discussed. The most important challenge is to design an appropriate Feedback Control Unit.

The necessary electronic circuits are a triangular waveform generator, an appropriate comparator to generate the PWM signal and auxiliary circuits, e. g. voltage regulation circuits.

Additionally, a protection circuit is introduced. This part is used to protect the device against short circuit at the output terminals and against overload, which means a resulting over-temperature of the MOSFETs, respectively of the cooling element.

3 Concepts for Feedback Control Unit

In chapter 2 different filter types were discussed theoretically. The conclusion was that a 4th order Bessel filter complies with all the requirements. It was shown, however, that the realisation of such filter is not possible only by placing component (L and C) values. The proposed filter structure with inductors and capacitors does not represent a stable system. Therefore, it was suggested to introduce a feedback control.

In this chapter, different controller models are developed to stabilize the system and to create the desired transfer function. First the suggested circuit topology of section 2.4 is transformed into a system model and the related transfer function is given. After this, the control principle to stabilize the system is explained and the boundaries of the method are described. In the following section different filter concepts are developed and compared, first theoretically, then by using a circuit simulator leading to a final decision.

3.1 System Model

Before a feedback control can be developed, all significantly involved parts of the amplifier have to be transformed into an entire system model. Figure 2.20 shows the basic circuit topology with all relevant parts. The transfer function of the filter itself, the inductors and capacitors, was already calculated in Equation (2.6). The Half-Bridge Unit, ideally considered, can be transformed into a simple DC Gain. Figure 3.1 shows the Half-Bridge Unit with the input and output signal.
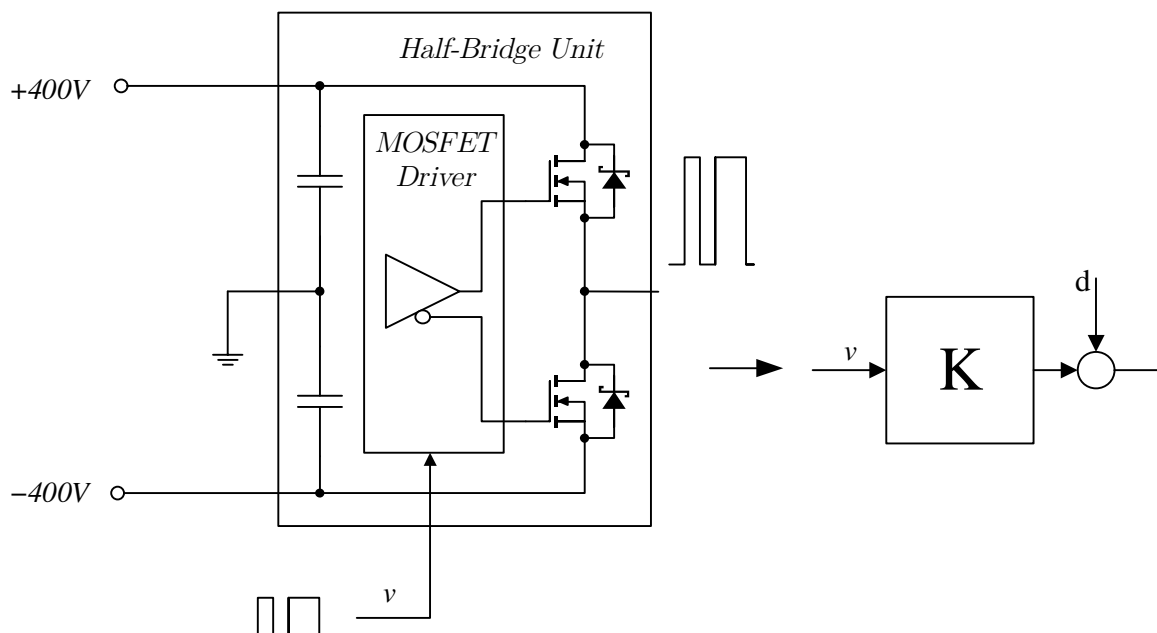
Figure 3.1 Transformation of the Half-Bridge Unit into a DC Gain.

The input signal v is generated by the PWM comparator. The resulting PWM signal is amplified by a factor K considering the DC power supply (± 400V). In addition, a summation node is introduced for calculating the transfer function for the amplified PWM signal. With this, the attenuation of the high frequency switching harmonics can be calculated.

The next step includes the Triangular Wave Generator and the comparator of Figure 2.20, which form a naturally sampled modulator. This modulator transforms the information of the signal u, which is described by its amplitude and phase, into a duty cycle depended information. Ideally considered, the resulting high frequency harmonics are rejected in the filter. It was shown in [18] that such a modulator contributes zero phase lag. This implies that the signal is not changed by the modulation and an ideal filter, neither in the amplitude nor in the phase. Therefore, these parts can be treated as a Unity Gain block. This can only be done because the PWM frequency – here the switching frequency – is at least two times the highest frequency component of the input signal. Figure 3.2 shows the resulting system model.
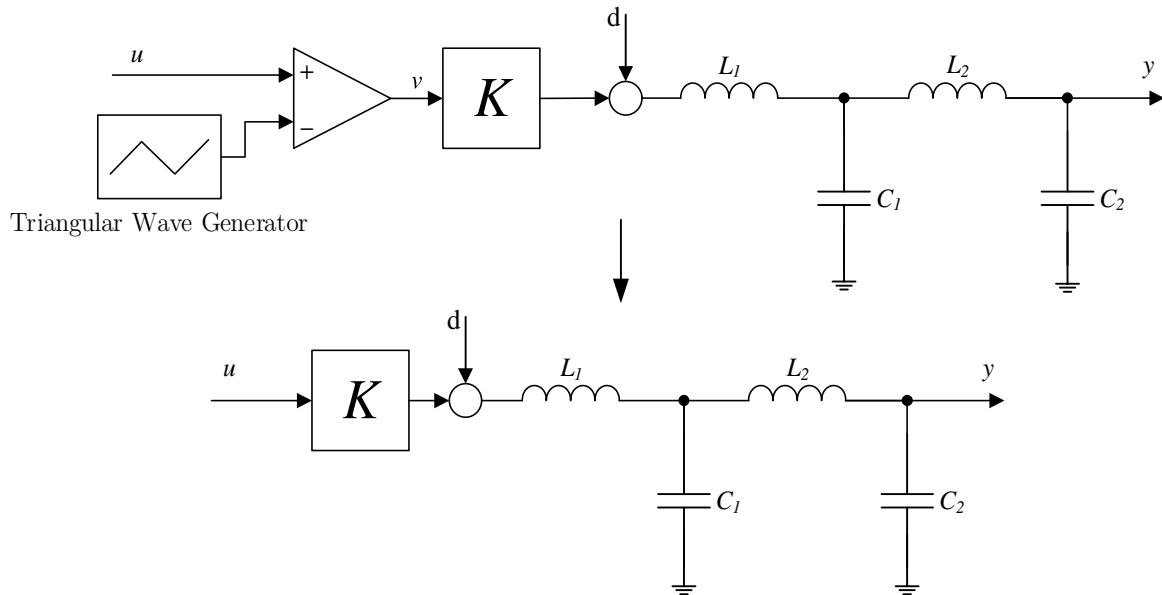
Figure 3.2 Resulting system model of the plant.

Based on Figure 3.2, the transfer functions of interest are calculated. $G_{u,y}(s)$ is the output transfer function related to the input u, which has to be changed into a Bessel transfer function.

$$G_{u,y}(s) = \frac{K}{1 + s^2(L_1C_1 + L_2C_2 + L_1C_2) + s^4(L_1C_1L_2C_2)} \tag{3.1}$$

$G_{d,y}(s)$ represents the transfer function, which is used to calculate the attenuation of the switching harmonics. In the uncontrolled model, it is equal to Equation (2.6).

$$G_{d,y}(s) = \frac{1}{1 + s^2(L_1C_1 + L_2C_2 + L_1C_2) + s^4(L_1C_1L_2C_2)} \tag{3.2}$$

3.2 Basic Control Considerations

The DC Gain can be calculated by dividing the supply voltage U_{SV} by the amplitude of the triangular wave.

$$K = \frac{U_{SV}}{\hat{U}_{triangle}} \tag{3.3}$$

U_{SV} is fixed to 400V. The amplitude of the triangular wave, however, can be chosen freely. In Table 1.2 the voltage for auxiliary circuits is fixed to +5V. Therefore, an amplitude of 2V with a DC offset of 2.5V is chosen. The full voltage of 5V is not utilized to avoid problems with operational amplifiers (OPA) at the supply rails. So the DC gain K results in $K = \frac{400V}{2V} = 200 \frac{V}{V}$.

The basic control scheme for stabilizing the LC–filter is shown in Figure 3.3. There a feedback of the capacitors current is introduced.
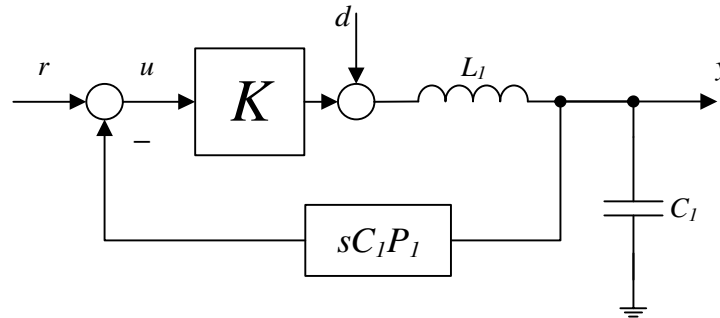
Figure 3.3 2nd order LC-filter with capacitors' current feedback.

The important point is that this creates a term sKP_1C_1 in the denominator of the transfer function. This significates that the damping factor ξ can be affected by the factor P_1. It also depends on the values of the inductor, the capacitor and the DC Gain. The resonance frequency, however, does not change.

$$G_{r,y}(s) = \frac{K}{1 + sKP_1C_1 + s^2 L_1 C_1} = \frac{K}{1 + 2\xi \frac{s}{\omega_0} + \frac{s^2}{\omega_0^2}} \rightarrow \xi = \frac{KP_1}{2}\sqrt{\frac{C_1}{L_1}}, \omega_0 = \frac{1}{\sqrt{L_1 C_1}} \quad (3.4)$$

P_1 has to transform the current into a voltage. This can be realised by a resistor. The resistance then represents the value of P_1. Figure 3.4 shows the relationship in the Pole-Zero diagram for the 2nd order example in section 2.2.5 with $L_1 = 10mH$, $C_1 = 1\mu F$. By increasing P_1 the poles can be pushed into the negative s–plane.
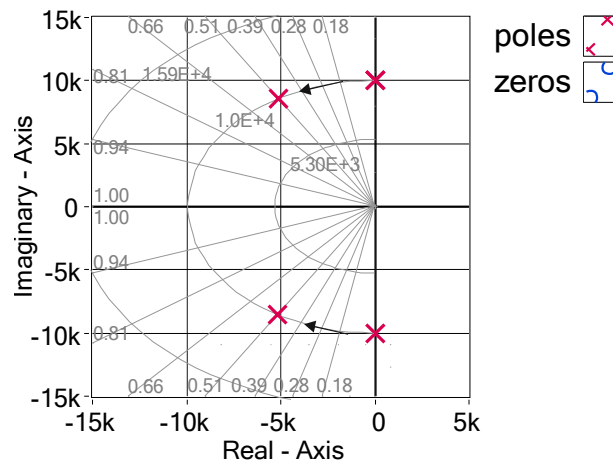
Figure 3.4 Influence of the capacitors current feedback to the poles of a 2nd order LC-filter.

This concludes in the result that the system can be stabilized easily and the damping factor ξ can be set theoretically to any value only by a feedback of the capacitors current.

The model of Figure 3.3 is implemented in a circuit simulator[1] to prove its functional capability. Figure 3.5 shows a typical result of a simulation.
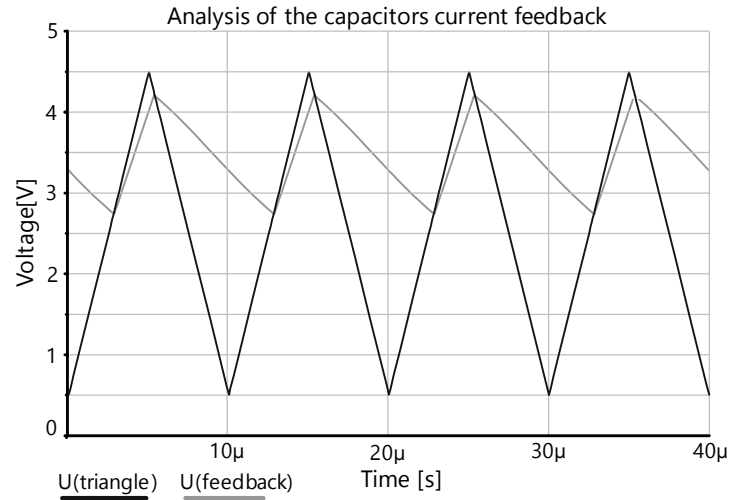

Figure 3.5 Curve analysis of a simulated filter with capacitors' current feedback.

The current of C_1 here is already transformed into a voltage. This voltage is fed back and shown as U(feedback). If P_1 reaches a certain value, the gradient of the feedback curve is higher than the gradient of the triangle curve U(triangle). In this case the feedback curve slides up the triangle curve caused by permanent on-off switching of the MOSFETs. The transfer function is no longer valid. Furthermore, the permanent switching actions means stress to the Half-Bridge Unit, which could lead to thermal damage. Therefore, this case has to be avoided.

To better understand the relationships, the critical value of P_1 is calculated. This is the value where the gradient of the feedback curve is equal to the gradient of the triangle curve. Based on the relationship $u_L = L \cdot \frac{di_L}{dt}$ the maximum feedback gradient for a certain value of P_1 is calculated.

$$\hat{k}_{feedback} = P_1 \cdot \frac{\Delta i}{\Delta t} = \frac{P_1}{L_1} \cdot U_{L_1,max} \tag{3.5}$$

On the other hand, the triangle gradient depends on the triangle amplitude and the switching frequency.

$$k_{triangle} = \frac{\Delta u_{triangle}}{\Delta t} = U_{triangle,p-p} \cdot 2f_s \tag{3.6}$$

The condition for a safe operation is that the gradient of the feedback curve is smaller than the gradient of the triangle curve.

$$\hat{k}_{feedback} < k_{triangle} \tag{3.7}$$

Equation (3.5) and Equation (3.6) inserted in Equation (3.7) leads to Equation (3.8). There the ratio $\frac{P_1}{L_1}$ is expressed.

$$\frac{P_1}{L_1} < \frac{U_{triangle,p-p} \cdot 2f_s}{U_{L_1,max}} \tag{3.8}$$

---

[1] National Instruments Multisim Circuit Simulator is used for this analysis.

The worst case, the highest gradient of the capacitors current, occurs when the output voltage of the amplifier is set near to the supply voltage and the output voltage of the filter is opposite. In this instant, the full 800V lies at the inductor. So, $U_{L_1,max} = 800$V. The switching frequency is defined as $f_s = 100$kHz and the peak-peak voltage of the triangle is $U_{triangle,p-p} = 4$V. This leads to a critical $\frac{P_1}{L_1}$ ratio of $\frac{P_1}{L_1} < 1000$s^{-1}.

Another important point is the dimensioning of the inductor and capacitor values. It was described in section 2.2.5, that Z_i, the carcteristic impedances, should be small to maintain low voltage drop at a load step but high enough to limit the filter input current at step responses. The inductor value L_1 in Figure 3.3, one part of the filter, limits the gradient of the filter input current. It also determines the maximum amplitude of the filter input current, because the switching frequency is constant. Therefore, L_1 has to be dimensioned such that a certain limit of the filter input current is not exceeded. In the requirements a maximum output current of $\pm 10A$ is specified. The ripple current amplitude shall not exceed this value. The highest ripple current occurs at a output voltage $U_{out} = 0V$. Generally the amplitude of the ripple current is defined as

$$\frac{di_L}{dt} = \frac{u_L}{L_1} \quad \rightarrow \quad \hat{I}_{ripple} = \frac{U_{SV} \cdot \Delta t}{2 \cdot L_1} \tag{3.9}$$

To limit the filter current amplitude to 10A the inductor value has to be higher than $L_{1,min} = \frac{U_{SV} \cdot \Delta t}{2 \cdot \hat{I}_{ripple}} = \frac{400\text{V} \cdot 5\text{µs}}{2 \cdot 10\text{A}} = 100$µH. This is already a high value. If, for instance, a characteristic impedance of 5Ω has to be achieved, this means a 4µF capacitor, a charge of 1600µAs is necessary for a voltage step of 400V. At typical rise times of 50µs, noticeable in the filter studies section 2.2, this leads to high current peaks, here 32A for 50µs. In reality, this is not a perfect rectangular shape, so that even higher current peaks are expected. The conclusion is that the inductor value of L_1 has to be placed in the range of 100µH and the capacitor value in the range of 4µF.

3.3 Feedback Control Approaches

Based on the results of section 3.2 four different control approaches are examined. The first approach relies on a faithful reproduction of the theoretical 4th order Bessel filter. The second approach tries to improve the dynamic by leaving the principle of a perfect filter reproduction. There, an approximated 3rd order filter is designed. The third approach looks similar to the second but the calculation principle is different and more applicable than in the 3rd order approach. The fourth approach relies on the others but tries to improve the dynamic of the system by the usage of all discussed control possibilities.

3.3.1 Fourth-Order Bessel Filter

In this approach a perfect reproduction of a 4th order filter is analysed. It bases on a state feedback control. This is possible, because all state variables of the system can be measured easily. The voltages can be measured with OPA circuits such a differential amplifier and the current with current transformers and resistors. Figure 3.6 shows the resulting controller structure.
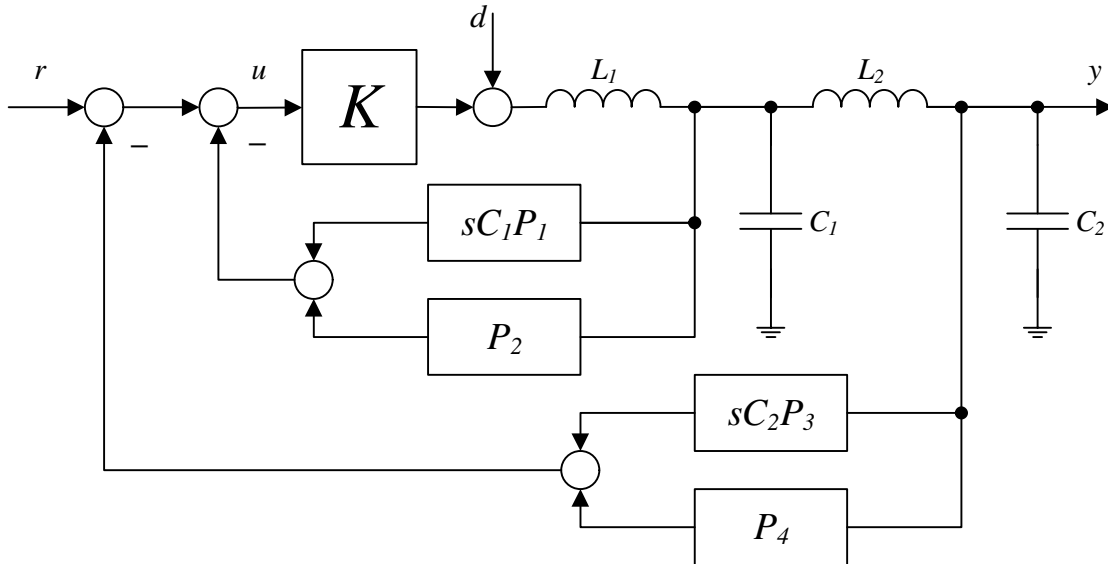
Figure 3.6 State feedback control structure.

All states that are fed-back can be affected by gains P_i. These gains can be realized by OPA circuits or directly by a resistor as shown in section 3.2. The resulting transfer function $G_{r,y}(s)$ is shown in Equation (3.10). The essential point is that every term of the denominator can be set arbitrary, either by P_i or by an inductor or capacitor value

$$G_{r,y}(s) = \cfrac{K}{\begin{array}{c}[1 + K(P_2 + P_4)] + s[K(C_1 P_1 + C_2 P_3)] + \\ s^2[L_1 C_1 + L_2 C_2 + L_1 C_2 + K P_2 L_2 C_2] + s^3[K P_1 C_1 L_2 C_2] + s^4[L_1 C_1 L_2 C_2]\end{array}} \qquad (3.10)$$

The transfer function $G_{d,y}(s)$ looks similar to $G_{r,y}(s)$. Only the factor K is replaced by 1.

$$G_{d,y}(s) = \cfrac{1}{\begin{array}{c}[1 + K(P_2 + P_4)] + s[K(C_1 P_1 + C_2 P_3)] + \\ s^2[L_1 C_1 + L_2 C_2 + L_1 C_2 + K P_2 L_2 C_2] + s^3[K P_1 C_1 L_2 C_2] + s^4[L_1 C_1 L_2 C_2]\end{array}} \qquad (3.11)$$

Generally normalized poles[1] are given for different filter types in filter design handbooks. This leads to a transfer function, which is shown in Equation (3.12).

$$G_{r,y}(s) = \frac{K}{\left(\frac{s}{p_1} + 1\right) \cdot \left(\frac{s}{p_2} + 1\right) \cdot \left(\frac{s}{p_3} + 1\right) \cdot \left(\frac{s}{p_4} + 1\right)} \qquad (3.12)$$

The denominator of this equation, however, cannot be compared with the denominators of Equation (3.10) or Equation (3.11). Therefore, the denominator has to be expanded. This leads to a denominator with parameters A…D which can directly be compared to Equation (3.10) and Equation (3.11).

$$G_{r,y}(s) = \frac{K}{1 + As + Bs^2 + Cs^3 + Ds^4} \quad \rightarrow \quad P_2 = -P_4, \quad \frac{P_1}{L_1} = \frac{C}{K \cdot D} < 1000\text{s}^{-1} \qquad (3.13)$$

This leads to two results. First $P_2 = -P_4$, only the difference of $u_{c_1} - u_{c_2} = u_{c_1} - y$ has to be fed back. This reduces one OPA in the circuit realisation. Second $\frac{P_1}{L_1} = \frac{C}{K \cdot D} < 1000\text{s}^{-1}$. The essential point is that $\frac{P_1}{L_1}$ does not depend on the setting of the other part values, e. g. C_1, L_2 or

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[1] For all calculations the normalized Bessel poles are extracted out of [3, p. 468]

C_2. It depends only on the cutoff frequency of the Bessel filter. If the cutoff frequency is increased, $\frac{P_1}{L_1}$ exceeds the limit of 1000s^{-1} long before the attenuation of the switching frequency reaches the critical value of 50dB. Therefore, $\frac{P_1}{L_1}$ represents the limiting factor in this case.

$\frac{P_1}{L_1}$ is set to a value near 1000s^{-1} to reach the maximum dynamic. L_1 is set to 100µH as described in section 3.2. C_1 is set to 3.3µF. This increases the characteristic impedance by 10% but reduces the current peak in a step response case. The parameter P_2 can be set to zero. Thus, L_2 and C_2 have to be calculated and cannot be set arbitrary. Table 3.1 shows all values and controller parameters for the 4th order Bessel filter attempt.

L_1 [µH]	C_1 [µF]	Z_1 [Ω]	L_2 [µH]	C_2 [µF]	Z_2 [Ω]	P_1 [Ω]	P_2 [1]	P_3 [Ω]	P_4 [1]
100	3.3	5.5	32.8	5.8	2.38	98.59m	0	-12.34m	0

Table 3.1 Part values, characteristic impedances and controller parameters, 4th order Bessel filter approach.

Figure 3.7 shows the related frequency response and step response. It is visible that the only difference between $G_{r,y}(s)$ and $G_{d,y}(s)$ is the gain K.
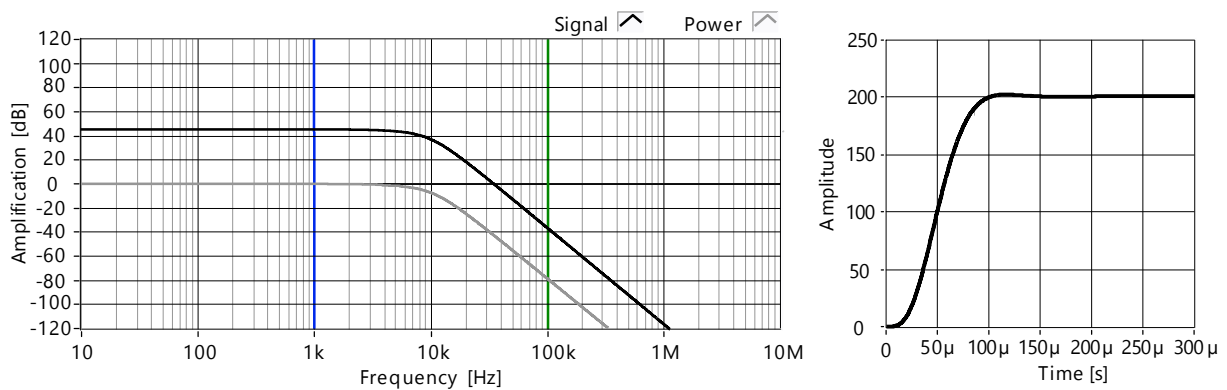
Figure 3.7 Frequency response and step response, 4th order Bessel filter approach[1].

The relevant data of the frequency response is summarized in Table 3.2.

Attenuation at f_s [dB]	DC Amplification [dB]	Amplification at f_m[2] [dB]	Amplification Lack[3] at f_m [dB]
79.8	46.02	45.96	0.06

Table 3.2 Frequency response analysis, 4th order Bessel filter approach.

The attenuation at $f_s = 100$kHz is excellent. Also the amplification lack at f_m is minimal. That means nearly the same amplification of all allowed input frequencies.

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[1] $G_{r,y}(s)$ is represented by the curve *Signal* and $G_{d,y}(s)$ by the curve *Power*.

[2] f_m is the highest frequency that is allowed in the input parameters, $f_m = 1$kHz.

[3] Amplification lack is the difference between the DC amplification and the amplification at f_m.

The step response looks good, as it is expected. The overshoot[1] is under 1%, which is better than required. The settling time[2] is in the range of 100μs. For a 1kHz rectangular input signal – 1ms per period – 20% of the half period is need to reach the set value. In a less strict consideration, the rise time can be used instead of the settling time. Compared to the former example the output only needs 10% of the time to reach the required value. Table 3.3 shows the data of the step response.

Steady State [V]	Peak Value [V]	Overshoot [%]	Peak Time[3] [μs]	Settling Time [μs]	Rise Time[4] [μs]
200	201.66	0.833	116	96.5	52.8

Table 3.3 Step response analysis, 4th order Bessel filter approach.

The limiting factor in this approach is $\frac{P_1}{L_1}$ and not the attenuation at f_s. If it is possible to push the frequency response toward higher frequencies, higher dynamic can be achieved. This means faster settling and rise time. On the other hand, this decreases the attenuation. Lower attenuation, however, does not demonstrate a problem, because there is enough design margin. An attempt with higher order systems does not lead to better results. $\frac{P_1}{L_1}$ decreases even more the cutoff frequency, which results in worse dynamic. Attempts with lower order systems are more promising because of lower $\frac{P_1}{L_1}$ ratios. Therefore, an approximated Bessel filter 3rd order is developed.

3.3.2 Approximated Third-Order Bessel Filter

In the 4th order Bessel filter approach $\frac{P_1}{L_1}$ was the limiting factor. A lower filter order, however, allows to push the cutoff frequency towards higher frequency values. This behaviour is utilized in this approach. Equation (3.14) shows the design principle.

$$G_{r,y}(s) = \frac{K}{(1 + sA + s^2B + s^3C) \cdot \left(1 + \frac{s^2}{\omega_2{}^2}\right)} = G'_{r,y}(s) \cdot \frac{1}{\left(1 + \frac{s^2}{\omega_2{}^2}\right)} \tag{3.14}$$

First, a 3rd order Bessel filter transfer function is designed. Afterwards, the second basic filter element is added to increase the attenuation at f_s. Important is, that the resonance frequency of the second basic filter element is obviously higher than the cutoff frequency of the designed 3rd order Bessel filter. This changes the frequency response at higher frequencies but maintains the characteristic Bessel step response. Therefore, the resulting filter is only an approximated Bessel filter.

The whole Equation (3.14) demonstrates a system 5th order. That makes it necessary to introduce another circuit element. A simple way is the introduction of an integral element with a feedback of the output voltage.

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[1] Overshoot is defined as the ratio between the steady state value and the peak value in percent.

[2] Settling time is defined as the time from the begin of the step to the moment in which the output voltage rests within 1% of the steady state value.

[3] Peak time describes the point in time when the peak value occurs.

[4] Rise time is the time interval between 10% and 90% of the steady state value.

Another aim is to keep the whole system as simple as it is in the 4th order Bessel filter approach. It is tried to set P_2 and P_4 to zero again. It is also possible to set P_3 to zero, because the Bessel filter design is carried out with only one basic filter element. The situation is comparable to the considerations in section 3.2, see also Figure 3.3. The point is that P_1 damps the first and also the second basic filter element. Figure 3.8 shows the resulting system model.
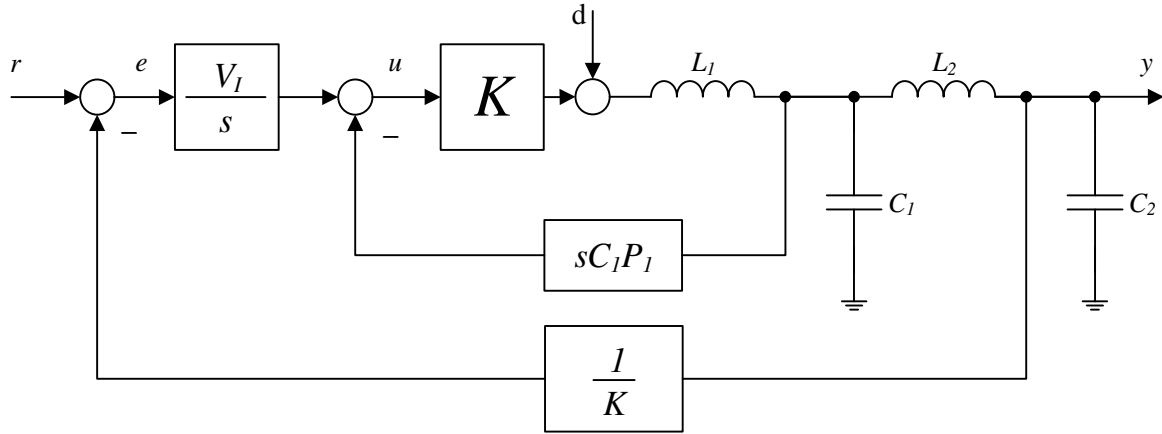

Figure 3.8 Relevant system model, 3rd order Bessel filter approach.

The resulting transfer functions $G_{r,y}(s)$ and $G_{d,y}(s)$ of this system are shown in Equation (3.15) and Equation (3.16).

$$G_{r,y}(s) = \frac{K}{\begin{aligned}1 + s\left[\frac{1}{V_I}\right] + s^2\left[\frac{K}{V_I}C_1P_1\right] + s^3\left[\frac{1}{V_I}(L_1C_1 + L_2C_2 + L_1C_2)\right] + \\ s^4\left[\frac{K}{V_I}P_1C_1L_2C_2\right] + s^5\left[\frac{1}{V_I}L_1C_1L_2C_2\right]\end{aligned}} \tag{3.15}$$

$$G_{d,y}(s) = \frac{s}{V_I \cdot \left\{\begin{aligned}1 + s\left[\frac{1}{V_I}\right] + s^2\left[\frac{K}{V_I}C_1P_1\right] + s^3\left[\frac{1}{V_I}(L_1C_1 + L_2C_2 + L_1C_2)\right] + \\ s^4\left[\frac{K}{V_I}P_1C_1L_2C_2\right] + s^5\left[\frac{1}{V_I}L_1C_1L_2C_2\right]\end{aligned}\right\}} \tag{3.16}$$

The design starts by setting L_2 and C_2 to zero. This leads to a simple 3rd order transfer function, shown in Equation (3.17).

$$G'_{r,y}(s) = \frac{K}{1 + s\left[\frac{1}{V_I}\right] + s^2\left[\frac{K}{V_I}C_1P_1\right] + s^3\left[\frac{1}{V_I}L_1C_1\right]} \tag{3.17}$$

Then the denominator polynomial is calculated for a promising cutoff frequency. After this, $\frac{P_1}{L_1}$ is identified. The result is similar to the previous, $\frac{P_1}{L_1} = \frac{B}{K \cdot C} < 1000\text{s}^{-1}$. Then V_I is determined as $V_I = \frac{1}{A}$. C_1 is set arbitrary and L_1 is calculated. In almost the same manner it is possible to set L_1 arbitrary and calculate C_1. This leads to the transfer function $G'_{r,y}(s)$, which is drawn in a Bode plot to check the result. The next step is to add the second basic filter element. L_2 and C_2, those who determine the resonance frequency of the second filter element, are set to reach the minimum attenuation specified in the requirements. The effect of different values of L_2 and C_2 is observed in the Bode plots of $G_{r,y}(s)$ and $G_{d,y}(s)$. If the resulting attenuation is in the range

of 50...60dB the step response is checked. If needed, caused by a non-satisfying step response, the whole procedure is started again with an adjusted cutoff frequency of the 3rd order Bessel filter. The results for a promising attempt, the part values and controller parameters, are summarized in Table 3.4.

L_1 [μH]	C_1 [μF]	Z_1 [Ω]	L_2 [μH]	C_2 [μF]	Z_2 [Ω]	P_1 [Ω]	P_2 [1]	P_3 [Ω]	P_4 [1]	V_I $[\frac{1}{s}]$
57	3.3	4.16	20	1	4.47	32.25m	0	0	0	18.9k

Table 3.4 Part values, characteristic impedances and controller parameters, 3rd order Bessel filter approach.

For the calculated polynomial, $\frac{P_1}{L_1} = 565\text{s}^{-1} < 1000\text{s}^{-1}$. This result shows that here is no problem with this factor. Figure 3.9 shows the frequency responses $G_{r,y}(s)$ and $G_{d,y}(s)$.
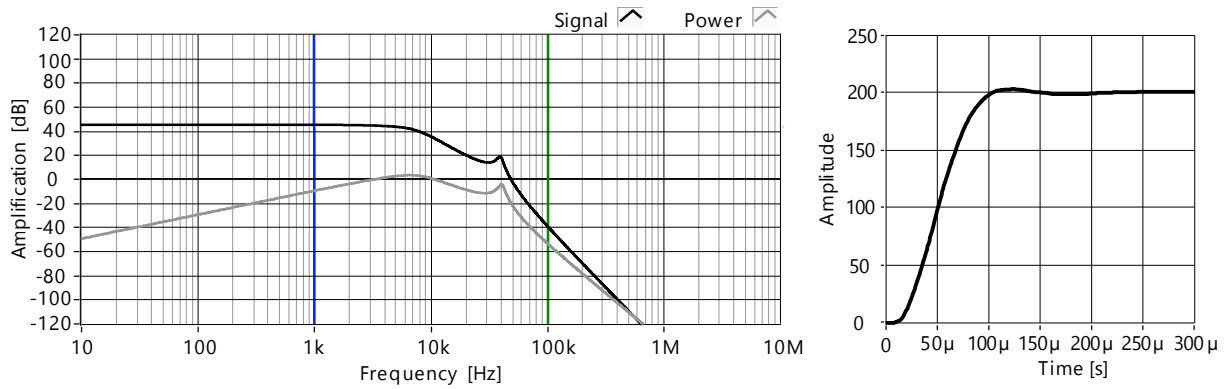
Figure 3.9 Frequency response and step response, 3rd order Bessel filter approach.

In both frequency responses, the resonance frequency of the second filter element is visible. As expected, it is damped without any feedback of the second capacitor's current. The frequency response of $G_{d,y}(s)$, however, has a different curve shape, than the the frequency response of $G_{r,y}(s)$. The reason is visible in Equation (3.16). There a factor $\frac{s}{V_I}$ occurs which means a +20dB/decade gradient of the curve with a pass through zero at $\frac{V_I}{2 \cdot \pi}$. In this case $\frac{V_I}{2 \cdot \pi} \approx 3\text{kHz}$. The attenuation at f_s of the rectangular signal is 53.68dB. The amplification lack is negligible.

Attenuation at f_s [dB]	DC Amplification [dB]	Amplification at f_m [dB]	Amplification Lack at f_m [dB]
53.68	46.02	45.93	0.09

Table 3.5 Frequency response analysis, 3rd order Bessel filter approach.

The analysis results of the step response is shown in Table 3.6. The results are sobering. There is achieved no significant improvement compared to the 4th order Bessel filter approach.

Steady State [V]	Peak Value [V]	Overshoot [%]	Peak Time [μs]	Settling Time [μs]	Rise Time [μs]
200	202.34	1.17	124	131	58.6

Table 3.6 Step response analysis, 3rd order Bessel filter approach.

3.3.3 Approximated Second-Order Bessel Filter

The results of the 3rd order Bessel filter approach are sobering, compared to the results of the 4th order approach. The problem is the small value of V_I. This leads to a relative high value of the amplification of $G_{d,y}(s)$ at the cutoff frequency of the designed 3rd order filter, caused by the +20dB/decade character of $\frac{s}{V_I}$. Another disadvantage is high effort to calculate suitable results. In the approximated 2nd order Bessel filter approach these disadvantages are eliminated.

The design is based on the Bessel transfer function for 2nd order systems, shown in Equation (3.18), extracted out of [19, p. 219].

$$G_{Bessel}(s) = \frac{1}{1 + \sqrt{3} \cdot s + s^2} = \frac{1}{1 + 2\xi \cdot \frac{s}{\omega_0} + \frac{s^2}{\omega_0^2}} \quad \rightarrow \quad \xi = \frac{\sqrt{3}}{2}, \omega_0 = 1 \qquad (3.18)$$

The integral element of the approximated 3rd order Bessel filter approach leads to a 3rd order system without the second basic filter element. This results in the introduction of a s-term in the nominator of the controller. A PI element offers this s-term in the nominator. The advantage is, that there is no additional OPA needed in the circuit realisation. Figure 3.10 shows the resulting system model.
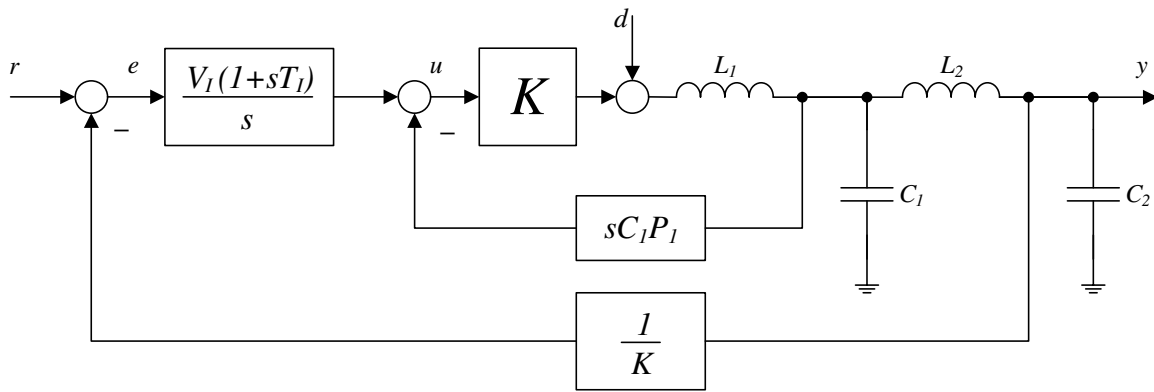
Figure 3.10 Relevant system model, 2nd order Bessel filter approach.

The design starts with an analysis of the open loop with the PI controller, without L_2 and C_2. The term T_I is placed such, that the faster pole p_2 is compensated.

$$F_0(s) = \frac{K \cdot V_I \cdot (1 + sT_I)}{s \cdot \left(\frac{s}{p_1} + 1\right) \cdot \left(\frac{s}{p_2} + 1\right)} \quad with \ T_I = \frac{1}{p_2} \quad \rightarrow \quad F_0(s) = \frac{K \cdot V_I}{s \cdot \left(\frac{s}{p_1} + 1\right)} \qquad (3.19)$$

The open loop $F_0(s)$ then is closed which leads and the coefficients of $G'_{r,y}(s)$ are compared to Equation (3.18).

$$G'_{r,y}(s) = \frac{K \cdot V_I}{V_I + s + \frac{s^2}{p_1}} = \frac{K}{1 + \frac{1}{V_I}s + \frac{s^2}{V_I \cdot p_1}} = \frac{1}{1 + \sqrt{3} \cdot \frac{s}{\omega_0} + \frac{s^2}{\omega_0^2}} \qquad (3.20)$$

The comparison of the coefficients leads to the results in Equation (3.21)

$$V_I \cdot p_1 = \omega_0^2, \qquad \sqrt{3} \cdot V_I = \omega_0 \quad \rightarrow \quad 3 \cdot V_I = p_1 \qquad (3.21)$$

With $V_I \cdot T_I = K_p = 1$[1] the relevant relationship $p_1 = 3 \cdot p_2$ comes up. The task for designing a filter now is very easy. First L_1 and C_1 are set arbitrary. Then P_1 is set such that $\frac{p_1}{p_2} = 3$, carried out with aid of National Instruments' Control Design and Simulation Toolkit. The next step is to set $V_I = p_2 = \frac{1}{T_I}$. At last, the second basic filter element is added to increase the attenuation at f_s. The results for a promising attempt, the part values and controller parameters, are summarized in Table 3.7.

L_1 [µH]	C_1 [µF]	Z_1 [Ω]	L_2 [µH]	C_2 [µF]	Z_2 [Ω]	P_1 [Ω]	P_2 [1]	P_3 [Ω]	P_4 [1]	V_I $[\frac{1}{s}]$	T_I [µs]
100	3.3	5.5	10	3.3	1.74	87.37m	0	0	0	23.73k	42.14

Table 3.7 Part values, characteristic impedances and controller parameters,
2nd order Bessel filter approach.

In this case $\frac{P_1}{L_1} \approx 900 \mathrm{s}^{-1}$, which significates a better utilization of the given range. It is possible to increase V_I to $23.74 \mathrm{ks}^{-1}$. This increases the attenuation at f_s, compared to the approximated 3rd order Bessel filter approach.

The resulting transfer functions of the system are shown in Equation (3.22) and Equation (3.23).

$$G_{r,y}(s) = \frac{K \cdot (1 + sT_I)}{\begin{array}{c} 1 + s\left[\frac{1}{V_I} + T_I\right] + s^2\left[\frac{K}{V_I}C_1P_1\right] + \\ s^3\left[\frac{1}{V_I}(L_1C_1 + L_2C_2 + L_1C_2)\right] + s^4\left[\frac{K}{V_I}P_1C_1L_2C_2\right] + s^5\left[\frac{1}{V_I}L_1C_1L_2C_2\right] \end{array}} \tag{3.22}$$

$$G_{d,y}(s) = \frac{s \cdot (1 + sT_I)}{V_I \cdot \left\{ \begin{array}{c} 1 + s\left[\frac{1}{V_I} + T_I\right] + s^2\left[\frac{K}{V_I}C_1P_1\right] + s^3\left[\frac{1}{V_I}(L_1C_1 + L_2C_2 + L_1C_2)\right] \\ + s^4\left[\frac{K}{V_I}P_1C_1L_2C_2\right] + s^5\left[\frac{1}{V_I}L_1C_1L_2C_2\right] \end{array} \right\}} \tag{3.23}$$

Figure 3.11 shows the related frequency responses.
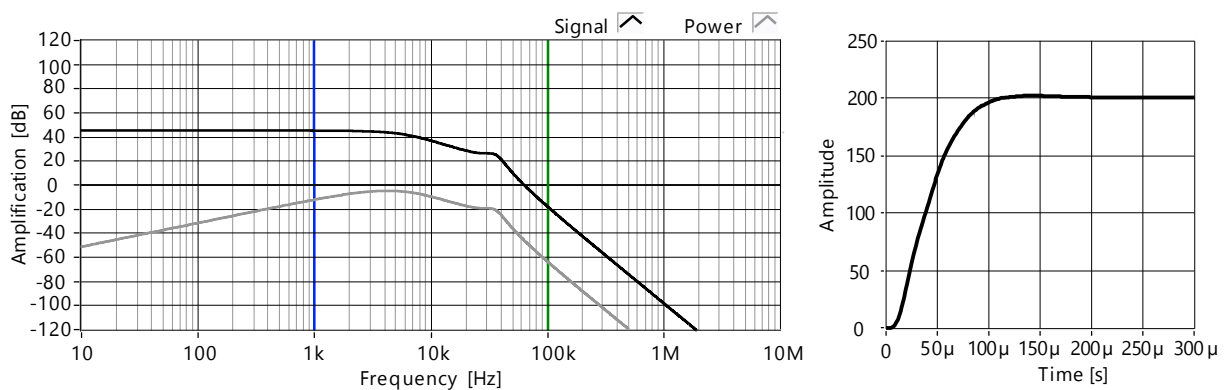
Figure 3.11 Frequency response and time response, 2nd order Bessel filter approach.

The frequency response of $G_{d,y}(s)$ is similar to the frequency response of the approximated 3rd order Bessel filter approach. The difference is a improved attenuation of approximately 10dB. The transfer functions are more damped at the resonance frequency of the second basic filter

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[1] K_P represents the proportional gain of a PI controller.

element. This behaviour, however, was be expected because of the higher P_1 in this case. The step response is also similar to the previous cases.

The analysis of the frequency response shows a better attenuation at f_s and a negligible amplification lack.

Attenuation at f_s [dB]	DC Amplification [dB]	Amplification at f_m [dB]	Amplification Lack at f_m [dB]
63.35	46.02	45.94	0.08

Table 3.8 Frequency response analysis, 2nd order Bessel filter approach.

The analysis of the step response confirms that all discussed approaches result in similar step responses.

Steady State [V]	Peak Value [V]	Overshoot [%]	Peak Time [µs]	Settling Time [µs]	Rise Time [µs]
200	201.37	0.686	142	106	61.1

Table 3.9 Step response analysis, 2nd order Bessel filter approach.

3.3.4 Free Designed Filter – Best Try

After three approaches with similar results, it is tried to improve the step response by the usage of all discussed controller elements, $P_1 \dots P_4$ and the PI controller. Figure 3.12 shows the system model.
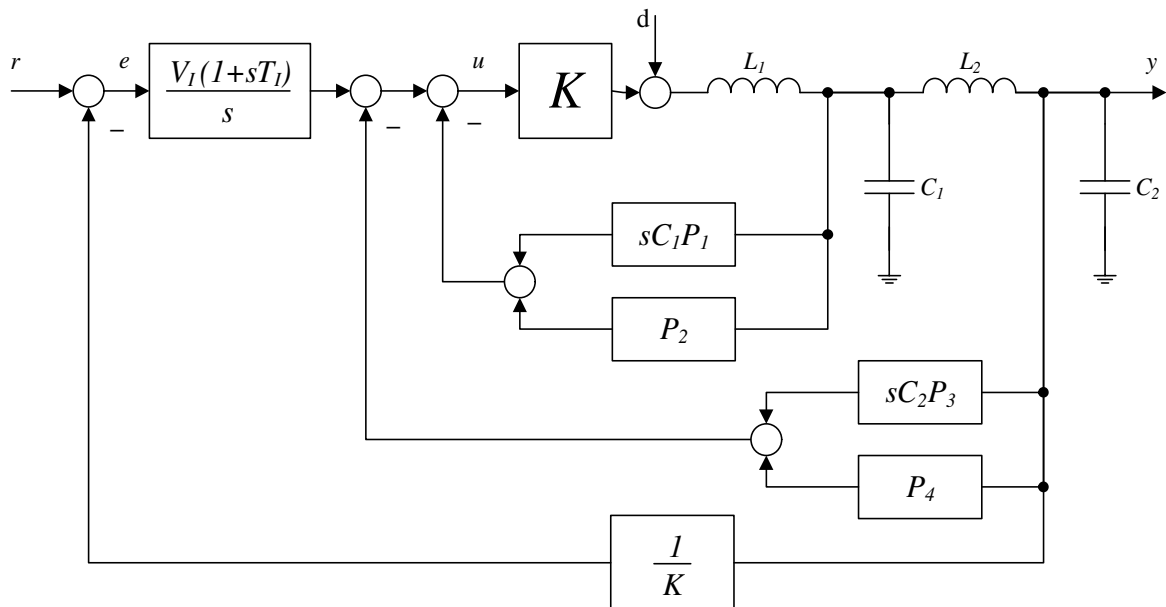
Figure 3.12 Relevant system model, Best Try filter approach.

The controller design here bases on the results of the 2nd order Bessel filter approach. L_1, C_1, L_2, C_2, V_I and T_I first have the same values as in that case. Then $\frac{P_1}{L_1}$ is set to a value near the limit

of 1000s^{-1}. After this, V_I is increased[1]. This action leads to higher overshoot. So, V_I is increased till the overshoot is higher than 5%. Then P_3 is decreased, $P_3 < 0$, until the overshoot is minimal. The introduction of P_3 leads to a higher damping factor of the second resonance frequency. Then P_2 is decreased, $P_2 < 0$. This action pushes the resonance frequency together and produces a Bessel-like step response, with rise times of 40µs and settling times in the range of 70µs. In the requirements 5% overshoot is allowed. This means, oscillations in this range are also allowed. Therefore, the rise time can be decreased again, by decreasing P_3 and P_2.

The transfer functions are shown in Equation (3.24) and Equation (3.25). There, the more difficult character is evident, which leads to a more complicated circuit realisation.

$$G_{r,y}(s) = \frac{K \cdot (1 + sT_I)}{\begin{aligned}&1 + s\left[\frac{1}{V_I}(1 + KP_2 + KP_4) + T_I\right] + s^2\left[\frac{K}{V_I}(C_1P_1 + C_2P_3)\right] + \\ &\quad s^3\left[\frac{1}{V_I}(L_1C_1 + L_2C_2 + L_1C_2) + \frac{K}{V_I}P_2L_2C_2\right] + \\ &\quad s^4\left[\frac{K}{V_I}P_1C_1L_2C_2\right] + s^5\left[\frac{1}{V_I}L_1C_1L_2C_2\right]\end{aligned}} \tag{3.24}$$

$$G_{d,y}(s) = \frac{s \cdot (1 + sT_I)}{V_I \cdot \left\{\begin{aligned}&1 + s\left[\frac{K}{V_I}(1 + KP_2 + KP_4) + T_I\right] + s^2\left[\frac{K}{V_I}(C_1P_1 + C_2P_3)\right] + \\ &\quad s^3\left[\frac{1}{V_I}(L_1C_1 + L_2C_2 + L_1C_2) + \frac{K}{V_I}P_2L_2C_2\right] + \\ &\quad s^4\left[\frac{K}{V_I}P_1C_1L_2C_2\right] + s^5\left[\frac{1}{V_I}L_1C_1L_2C_2\right]\end{aligned}\right\}} \tag{3.25}$$

Table 3.10 shows the part values and controller parameters for the calculated system model.

L_1 [µH]	C_1 [µF]	Z_1 [Ω]	L_2 [µH]	C_2 [µF]	Z_2 [Ω]	P_1 [Ω]	P_2 [1]	P_3 [Ω]	P_4 [1]	V_I [$\frac{1}{s}$]	T_I [µs]
100	3.3	5.5	10	3.3	1.74	97.08m	-41m	-40m	41m	37k	27.03

Table 3.10 Part values, characteristic impedances and controller parameters,
free designed filter – Best Try.

Figure 3.13 shows the frequency responses and the step response. There, it is visible that the resonance frequencies are pushed together.
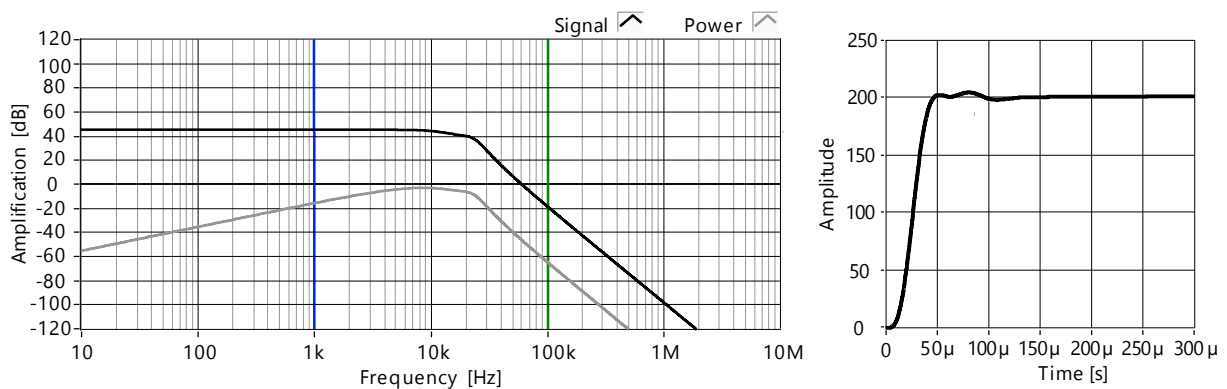
Figure 3.13 Frequency response and time response, free designed filter – Best Try.

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[1] $K_P = V_I \cdot T_I$ is always kept to 1.

Especially the second resonance frequency is simple to identify, because if its weakly damped character. In this case the second resonance frequency is situated at approximately 20kHz. In the 2nd order Bessel filter approach it is situatued at approximately 40kHz. Furthermore, the cutoff frequency is pushed to a higher frequency.

Table 3.11 shows the relevant results of the frequency response analysis. The attenuation at f_s is good and the amplification lack is nearly zero.

Attenuation at f_s [dB]	DC Amplification [dB]	Amplification at f_m [dB]	Amplification Lack at f_m [dB]
64.04	46.02	46.0	0.02

Table 3.11 Frequency response analysis, free designed filter – Best Try.

The analysis of the step response, see Table 3.12, shows a fast rise time of 24µs. This is paid by a higher oscillation amplitude but within the 5% overshoot. The settling time is here not as good as expected because the boundaries are defined as ±1%.

Steady State [V]	Peak Value [V]	Overshoot [%]	Peak Time [µs]	Settling Time [µs]	Rise Time [µs]
200	203.48	1.74	80.9	120	24.1

Table 3.12 Step response analysis, free designed filter – Best Try.

This fast rise time may cause problems because the switching period is only 10µs. That means the full step is executed in 2.5 periods and the controller has only two times the possibility to adapt. Therefore, this case has to be analysed particularly in a circuit simulator. Differences in the step response are expected.

3.4 Circuit Simulation – Comparison

After the theoretical analysis, the four different system models of section 3.3 are implemented in a circuit simulator. There the behaviour of a switching system is analysed.

First, the step response is simulated and the important parameters are pointed out. Differences compared to the results of section 3.3 are explained. The filter input currents are compared and the main parameters – maximum current amplitude, current peak – are discussed. Second, the load responses of each system are simulated and analysed. A rectangular response with the maximum output voltage – 95% of $U_{SV} = ±380$V – and the maximum signal frequency – $f_{in} = 1$kHz – is also simulated to show potentially differences between the step response and this rectangular response.

3.4.1 Step Response

Figure 3.14 shows the simulated step responses of the 4 system models. Generally, the simulation starts with unpredictable values, which may be caused due to improper settings. Therefore, it is important to set the output voltage to zero for the first 200µs to reach the steady state of zero.
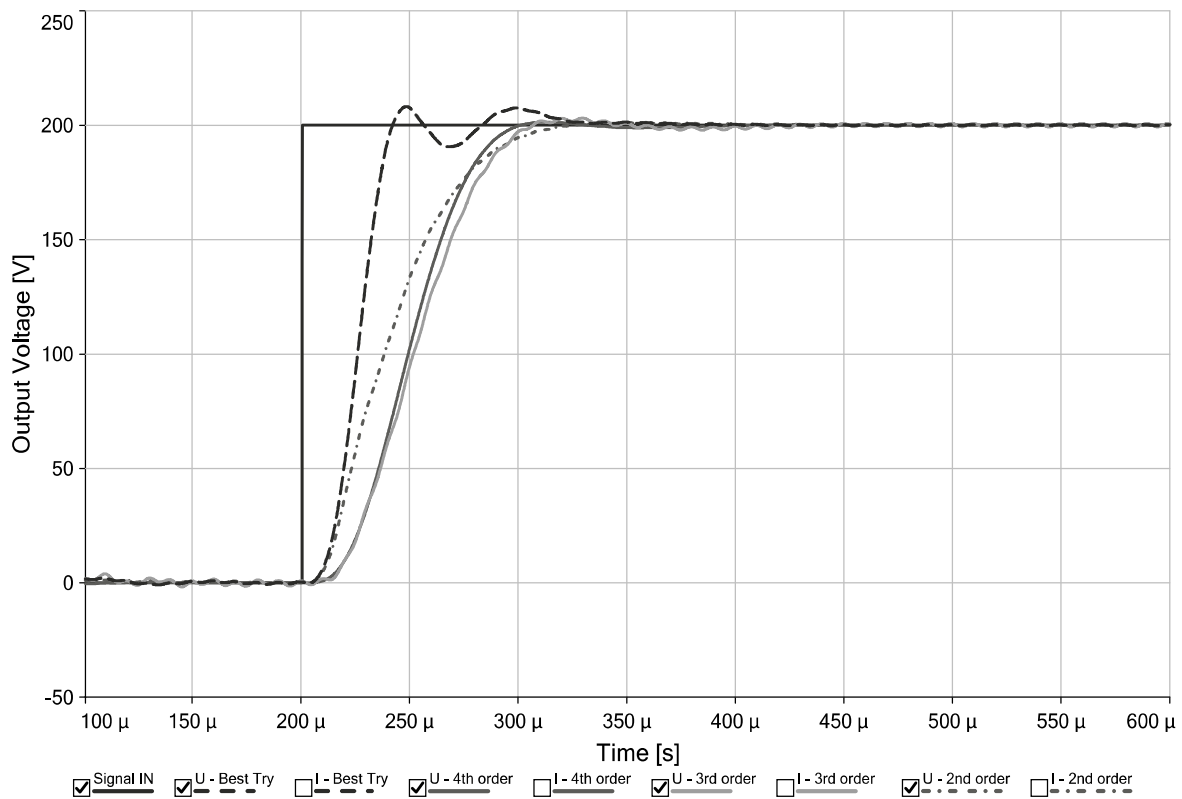
Figure 3.14 Comparison of the step responses of the discussed filters.

The step responses look quite similar to the results of the theoretical analysis. Only the higher overshoot of the Best Try curve annoys. Also visible is the f_s harmonic component on the 3rd order curve. This model shows also the highest rise time. Table 3.13 gives the parameter results. The simulated attenuation is in all cases similar to the theoretic ones but 2 to 3dB higher.

Parameters	$U - 4^{th}$ order	$U - 3^{rd}$ order	$U - 2^{nd}$ order	$U -$ Best Try
Amplitude of f_s Harmonic [mV]	38.5	707.0	253.0	253.0
Simul. Attenuation at f_s[1] [dB]	82.0	56.7	66.1	66.1
Peak Time [μs]	110.8	129.0	149.0	48.0
Peak Value [V]	201.4	203.1	201.2	208.1
Overshoot [%]	0.7	1.6	0.6	4.1
Settling Time [μs]	95.4	195.0	101.0	121.5
Rise Time [μs]	52.6	58.9	62.0	22.0

Table 3.13 Comparison of the step response parameters.

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[1] $Simul. \, Attenuation \, at \, f_s = 20 \cdot \log \left(\frac{amplitude \, of \, f_s \, harmonic}{\frac{4}{\pi} \cdot 400V} \right)$.

The overshoot of the Best Try model is already in the range of the 5% limit. The settling time of the 3rd order approach is higher than the theoretic one due to the high ripple voltage. The rise times are generally faster, e.g. in the Best Try case 22µs compared to 24.1µs of section 3.3.4. Figure 3.15 shows the corresponding filter input currents. There, the reason for the higher overshoot of the Best Try step response, compared to the theory, is visible. Due to the fast rise time – 22µs – the system (switching period 10µs) can not react as fast as necessary to the changing state values. To confirm this assumption a simulation with higher switching frequency was carried out. There, the results of all four simulated step responses precisely match the theoretic ones.
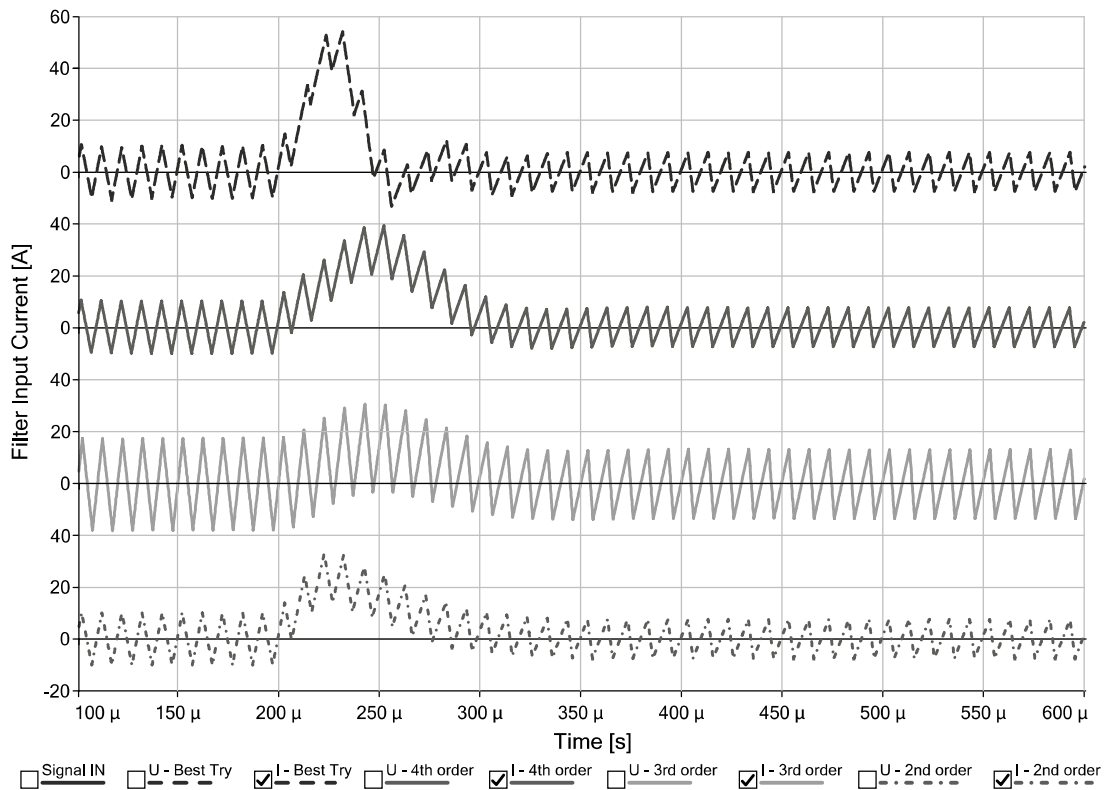
Figure 3.15 Comparison of the filter input currents – step response case.

Table 3.14 show the filter input current parameters. In the theory the maximum current amplitude was calculated to 10A for $L_1 = 100$µH. This result goes well together with the simulated cases, see 4th order, 2nd order and Best Try. The current peak value not only depends on the inductor and capacitor values. The main reason for a high current peak is a fast rise time. The value of 54A in the Best Try case is very high and not preferred for a circuit realisation.

Parameters	$U - 4^{th}$ order	$U - 3^{rd}$ order	$U - 2^{nd}$ order	$U -$ Best Try
Max. Current Amplitude[1] [A]	10.1	17.8	10.0	9.8
Current Peak [A]	39.1	30.9	32.9	54.0

Table 3.14 Comparison of the relevant filter input current parameters – step response case.

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[1] $U_{out} = 0V$.

3.4.2 Load Response

The voltage drop in case of a load step cannot be determined only by setting Z_i. In addition, the controller structure dynamic influences essentially the behaviour of the system. Therefore, a full load step – 0 to 10A – is simulated. The initial condition is a steady state voltage $\hat{U}_{nom} = 325\text{V}$. The simulation is executed to control the compliance with the related requirement, see Table 1.1.
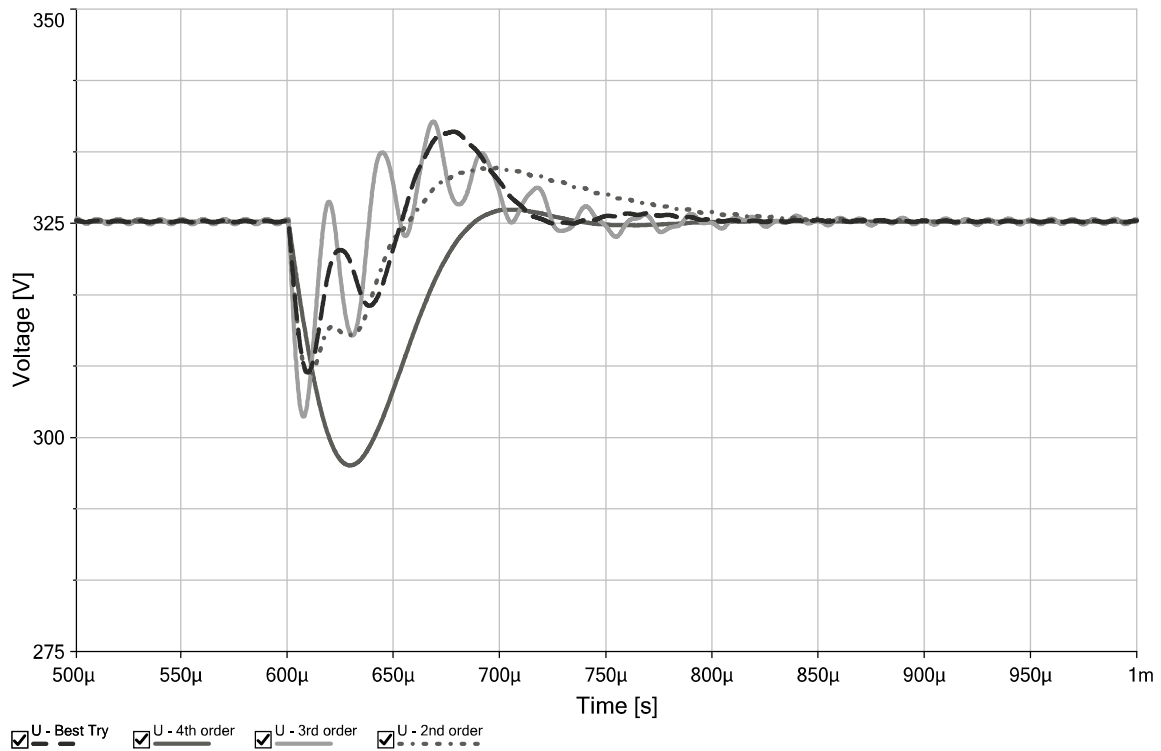
Figure 3.16 Comparison of the load responses at full load step – 10A.

The 4th order system shows the highest voltage drop – 8.7% – which is near the limit of 10% of $\hat{U}_{nom}$. The 3rd order system has oscillations with high amplitude. The Best Try system shows a higher voltage overshoot followed after the maximum voltage drop, which is also not optimal. Only the 2nd order system shows a good reaction. There only the settling time is higher compared to the others.

Parameters	U – 4th order	U – 3rd order	U – 2nd order	U – Best Try
Voltage Drop [V]	28.3	23.0	18	17.6
Voltage Drop [%]	8.7	7.1	5.5	5.4
Voltage Overshoot [V]	1.6	11.0	6.4	10.6
Voltage Overshoot [%]	0.5	3.4	2.0	3.3
Settling Time [µs]	75.0	120.7	152.0	105.0

Table 3.15 Comparison of the load response parameters at full load step – 10A.

3.4.3 Rectangular Response

In this case the most critical signal – rectangular output voltage, $f_{out} = 1\text{kHz}$, $|U_{out}| = 380\text{V}$ – is simulated to check the compliance with the requirements even in this case, see Figure 3.17.
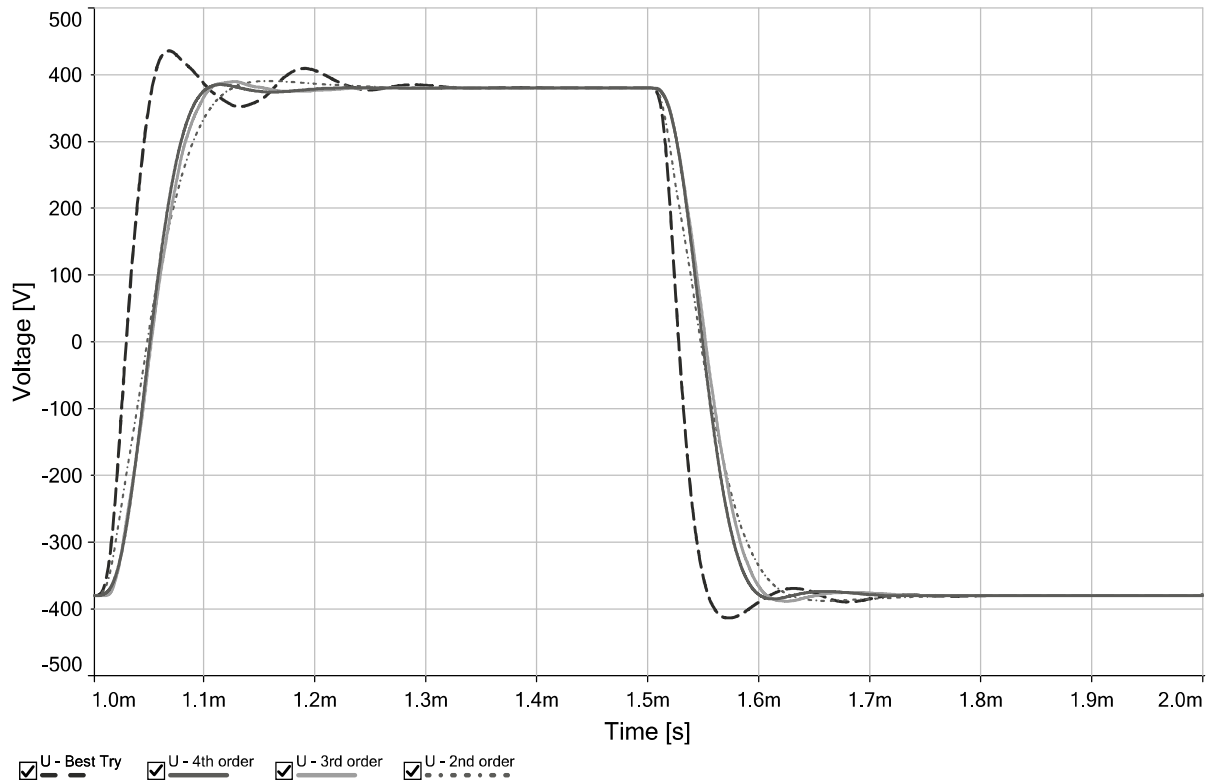
Figure 3.17 Comparison of the full rectangular responses.

At first view the results look equal to the step response simulation. Under closer scrutiny, the overshoot of the 2nd order system and the Best Try system become worse. With 7.2% overshoot, the Best Try system does not meet the requirements. The settling time 5%[1] shows that the Best Try system, which was designed to reduce this value, flops. The result is that the settling time 5% doubles and not – as hoped – halves. Table 3.16 shows the results in more detail.

Parameters	U − 4th order	U − 3rd order	U − 2nd order	U − Best Try
Peak Value [V]	385.0	389	390	435
Overshoot[2] [%]	0.7	1.2	1.3	7.2
Settling Time 5% [μs]	92	97	109	203

Table 3.16 Comparison of the rectangular response parameters.

[1] In this case the settling time is defined as the time from the begin of the step to the moment in which the output voltage rests within 5% of the steady state value. The new boundary of 5% is introduced to show the relation, if the full overshoot range – 5% – is used.

[2] Overshoot is defined as the peak value divided by the full voltage step – 760V – in percent.

3.5 Controller Assessment and Decision

The analysed systems are compared for allowing a decision-making, see Table 3.17.

Parameters	U – 4$^{\text{th}}$ order	U – 3$^{\text{rd}}$ order	U – 2$^{\text{nd}}$ order	U – Best Try
Attenuation at f_s	++	o	+	+
Voltage Step Overshoot	+	o	+	––
Voltage Step Settling Time	+	o	o	–
Voltage Step Filter Current	o	–	+	–
Load Step Voltage Drop	–	o	+	o
Load Step Settling Time	+	o	–	o

Table 3.17 Comparison of the simulated systems' response parameters
(++ excellent, + good, o fair, − weak, −− poor).

The attenuation at f_s is in all cases satisfying, especially the 4$^{\text{th}}$ order system is characterized by an excellent behaviour. The results of the step response and the rectangular response are merged to the voltage step section. The 4$^{\text{th}}$ and the 2$^{\text{nd}}$ order systems have a small voltage overshoot of approximately 1%. The Best Try system, however, shows overshoot values higher than allowed in the requirements. This demonstrates a criterion for exclusion for this system. The 2$^{\text{nd}}$ order filter shows the lowest peak value of the filter input current. This is paid by slower settling times. It has also the lowest voltage drop, which is – for this purpose – more important than 20 or 30μs faster settling times. Therefore, the controller structure of the approximated 2$^{\text{nd}}$ order approach is selected for the circuit realisation.

4 Implementation of Filter Unit

In this chapter, the realisation of the filter related components is examined. Requirements for all components are defined and, based on this, appropriate types are searched in the distributers offers. In case of the inductors a 100µH coil is designed and improved with regard to the total losses.

4.1 Capacitors

There are necessary two identic capacitors with 3.3µF. Beside the capacitance, the rated voltage is an important parameter. The required rated voltage depends on the supply voltage and possible voltage overshoots. These overshoots are small due to the controller design. Nevertheless, a factor 1.5 is selected for safety reasons. Therefore, the rated voltage has to be at least 600V[1]. Based on these parameters an appropriate capacitor is selected [20]. It has a permissible DC voltage of 800V. It is also necessary to check the impedance characteristic of the capacitor at the switching frequency $f_s = 100$kHz, what is shown in Figure 4.1.
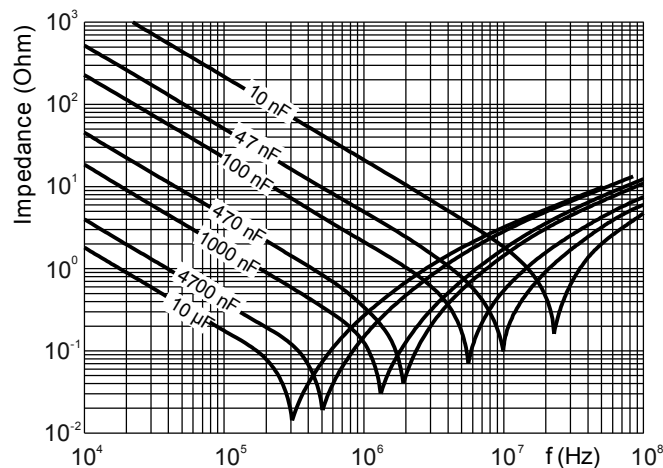
Figure 4.1 Capacitors' Impedance as a function of frequency (typical curve) [20].

The impedance curve of the 3.3µF capacitor is not illustrated there but it is assumed to be situated between the 1000nF and 4700nF curve. The impedance there has the typical $Z = \frac{1}{j\omega C}$ character in the 100kHz region. Also all other parameters, visible in the datasheet, indicate the utilisation of this capacitor.

4.2 Inductors

There are two ways for the selection of appropriate inductors. First, the search for prefabricated power inductors or second, the self-design of dedicated inductors, starting with cores and wires. The first way has the advantage of fully tested and proven parts and simply the saving of time. In the self-design, however, special current characteristics such as high frequency and high ripple current can be considered and their effects to the inductor analysed in detail. Based on this studies, an appropriate inductor can be developed.

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[1] *rated voltage* $= 1.5 \cdot U_{SV} = 1.5 \cdot 400\text{V} = 600\text{V}$

4.2.1 Prefabricated Power Inductors

The important parameters for designing a power inductor are the inductance, the rated current, the DC and AC resistance (conduction losses) and the maximum flux density (hysteresis/core losses). In the requirements table a maximum load current of 10A is specified. Additionally, a 10A peak triangle current, $\approx$6A RMS[1], has to be considered. This may leads to a RMS current of up to 16A. Necessary inductances are 100µH and 10µH. Available electronic distributors do not offer a separate suitable 100µH inductor. It can be found, however, a 10µH inductor with excellent characteristics, Coilcrafts SER2918-103KL [21]. The DC resistance is extremely low around 2.6mΩ. It provides a constant inductance over a wide current range, $I_{sat,10\% \, drop} = 28A$, see Figure 4.2.
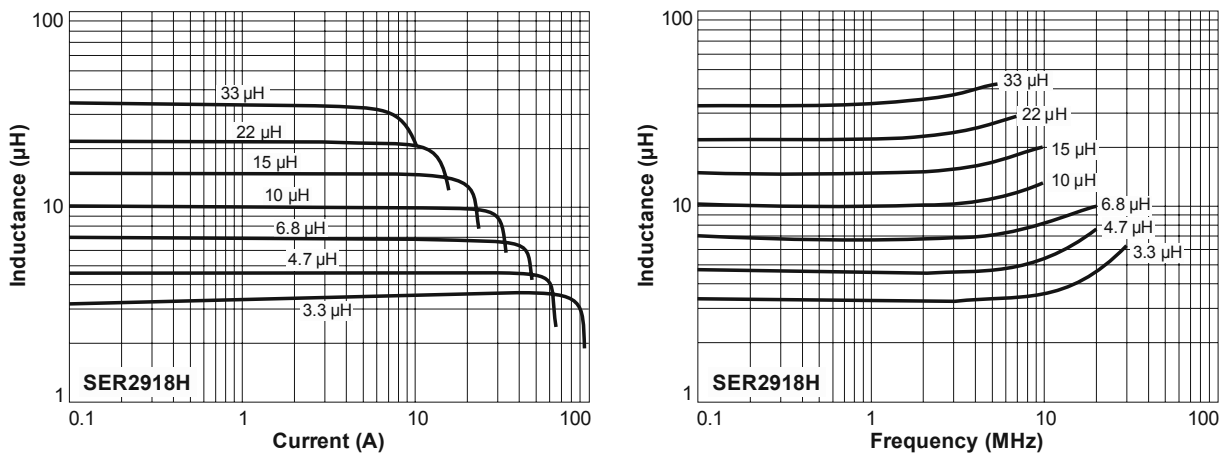
Figure 4.2 Inductance of the SER2918H series as a function of current and frequency [21].

There is also shown the excellent frequency behaviour. The inductance is nearly constant till 3MHz. In the datasheet can be found a diagram that shows the Equivalent Series Resistance (ESR), which indicates the losses of the windings for high frequency currents. The ESR is negligible till 1MHz. This means no critical amount of generated heat in the windings due to the 100kHz triangle current. All these characteristics indicate the utilisation of this inductor. It cannot be found, however, a statement about the core losses in the datasheet. Therefore, the core losses have to be observed attentionally in the testing phase to avoid damages due to overheat.

4.2.2 Inductor Self-Design

Due to the lack of information about the hysteresis/core losses of the selected 10µH inductor and the fact that 10 pieces are needed to form 100µH, a single inductor is designed to avoid possible overheat of the core and to save space. The core relevant parameters are the core material, the core type and the core size. The core material decides the core losses at given parameters such as frequency and maximum flux density. These losses depend on the core temperature. Most core materials have smaller losses at higher temeratures such as 100°C. For this purposes, however, constant losses over the temperature are preferred. Different materials are compared to find an optimal solution.

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[1] $10A \cdot \frac{1}{\sqrt{3}} = 5.77A \approx 6A$

Figure 4.3 shows the losses for the fixed parameters $\widehat{B} = 100\text{mT}$ and $f_s = 100\text{kHz}$ for the ferrite materials 3F3, N87 and 3C95. The best behaviour – nearly constant and low power losses over the temperature – shows the material 3C95. Therefore, it is selected for the inductor design.

Curve of power loss density (kW/m³ or mW/cm³)
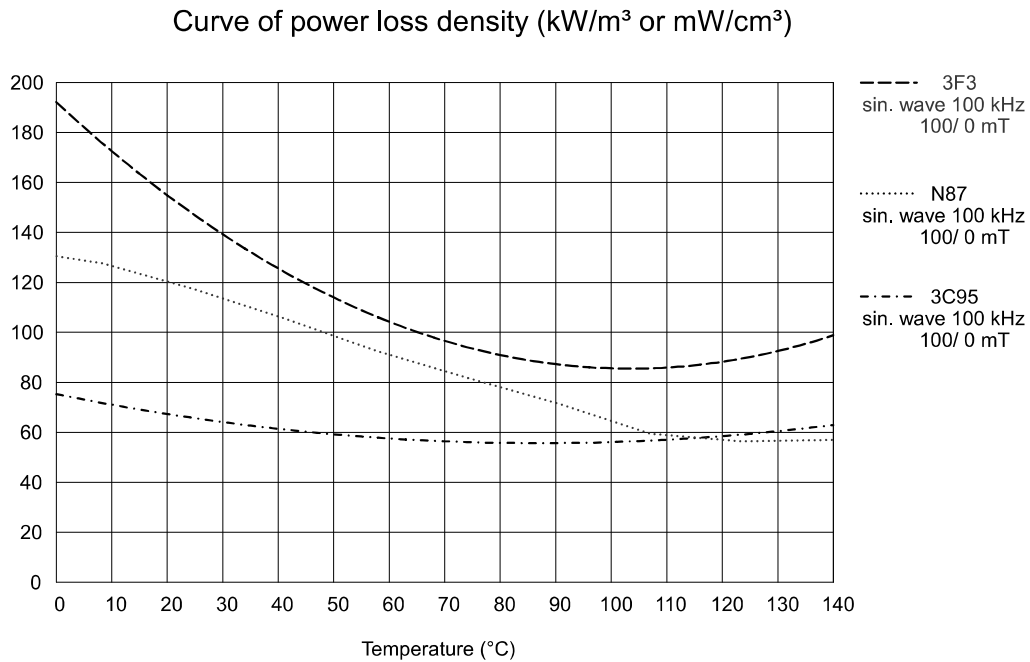
Figure 4.3 Comparison of the power loss densities of the Ferrite materials 3F3 [22, p. 3], N87 [23], 3C95 [24, p. 95].

A standard E core is selected as core type. The next step is the decision of a core size. The determining parameters are the maximum flux density $\widehat{B}$, the effective area A_e and the available winding window/size. The flux density in combination with the effective area A_e decides the number of turns of the winding at given frequency and supply voltage, shown in Equation (4.1).

$$N = \frac{U_{SV}}{4 \cdot A_e \cdot \widehat{B} \cdot f_s} \tag{4.1}$$

$\widehat{B}$, U_{SV} and f_s are fixed. Therefore, the effective area A_e – depended on the core size – decides about the number of turns. For instance, an E32/16/9 core with $A_e = 83\text{mm}^2$ lead to 120 turns.. A necessary cross-section of approximately $A_{wire} = 3\text{mm}^2$ results for the wire, according to the rule of thumb $\frac{I_{eff}}{A_{wire}} = 5\frac{\text{A}}{\text{mm}^2}$ with the effective current $I_{eff} = 16\text{A}$, as calculated before. The necessary winding window would have an area of at least 360mm^2, a value 2.5 times higher than the available winding window of 147mm^2. Possible realisations start with an E42 core. In this case, however, an E55 core is used to minimize the conduction losses, by minimizing the number of turns. The effective volume of the core does not demonstrate a problem, because the other realisation with 10 pieces of the coilcraft coils need more space on the PCB.
Therefore, an E55/28/25 [25] core is selected for the realisation. This leads to 24 turns, according to the former example. A wire with $A_{wire} = 2.54\text{mm}^2$ and a standard coil former is used for winding. The last step is to calculate the necessary air gap for the given 100µH. The determining relationship is shown in Equation (4.2).

$$l_{air} = \frac{N^2 \cdot \mu_0 \cdot \mu_{r,air} \cdot A_e}{L} \tag{4.2}$$

This leads to a resulting air gap of approximately $l_{air} = 3.04$mm what means a 1.5mm gap between the two E55 core halves. Thus, all necessary parameters are calculated.

Before the inductor is realised, a simulation in FEMM[1] is done to prove the design. The first results show a higher inductance in case of a 1.5mm gap, so that the gap is increased to 2mm. Thus, the 100µH inductance is reached. Figure 4.4 shows that the flux density in the air gap is smaller than the calculated one, $\widehat{B}_{air} \approx 90$mT.
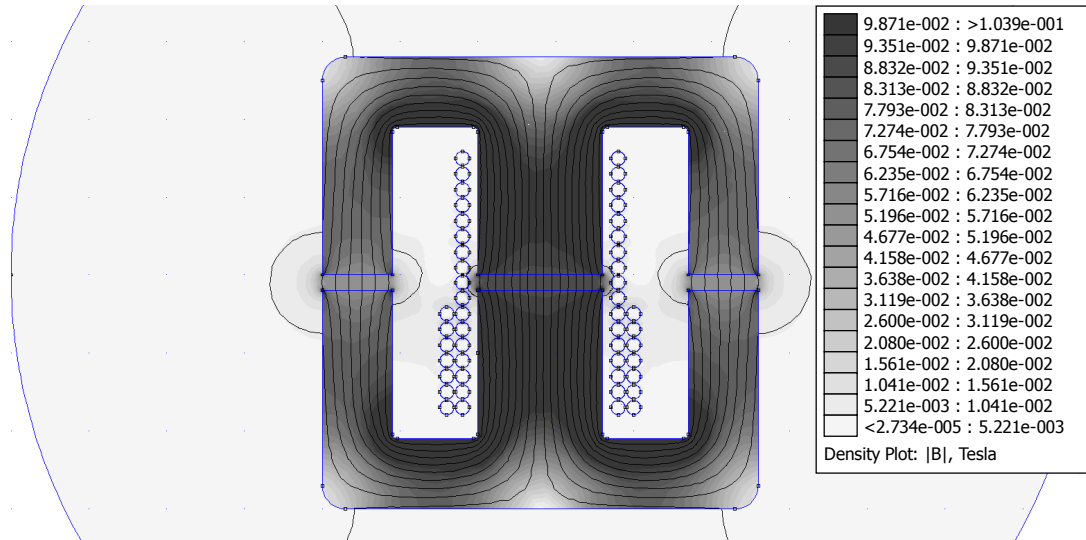
Figure 4.4 100µH inductor with 24 turns – flux density plot.

It is also possible to calculate the total losses – 40W – what is a non-tolerable value. A closer look to the air gap region shows, that the magnetic flux outside the gap penetrates the wires, see Figure 4.5. This leads to an induced voltage, and because of the conductivity of the copper and the high $\frac{dB}{dt}$, to a high current, noticeable by the dent of the flux line outside the air gap.
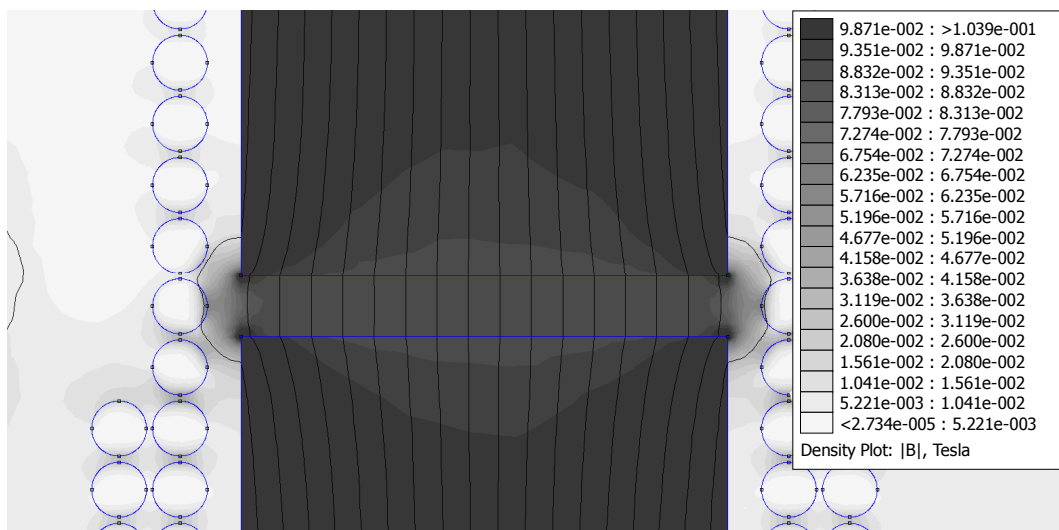
Figure 4.5 100µH inductor with 24 turns – flux density plot with zoomed dent near the air gap.

Finite Elements Method Magnetics[1]

FEMM also allows taking a closer look to the electric current density. To prove the assumption of the shielding current the current density is plotted in Figure 4.6.
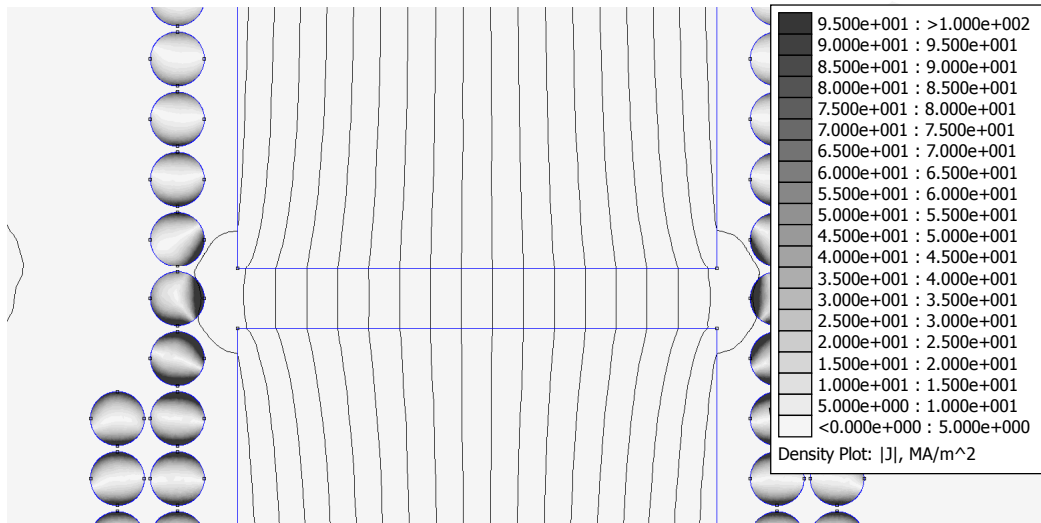
Figure 4.6 100µH inductor with 24 turns – current density plot.

It shows high current densities of above $100\,\frac{\text{A}}{mm^2}$. A total-loss integration in FEMM shows that approximately the halve of the total losses occurs in the three wires next to the air gap. The result is that the distance between the air gap and wires must be increased, to have smaller flux densities and thereby smaller eddy currents in the wires.

Therefore, a new inductor is designed – 2x18 turns with a cross-section of $A_{wire} = 1.25$mm^2 and an air gap of $l_{air} = 1.2$mm. Figure 4.7 shows the resulting current density plot with the same legend as in Figure 4.6. It is evident, that the current densities are smaller. The results for the total losses confirms that assumption – 7.2W total losses.
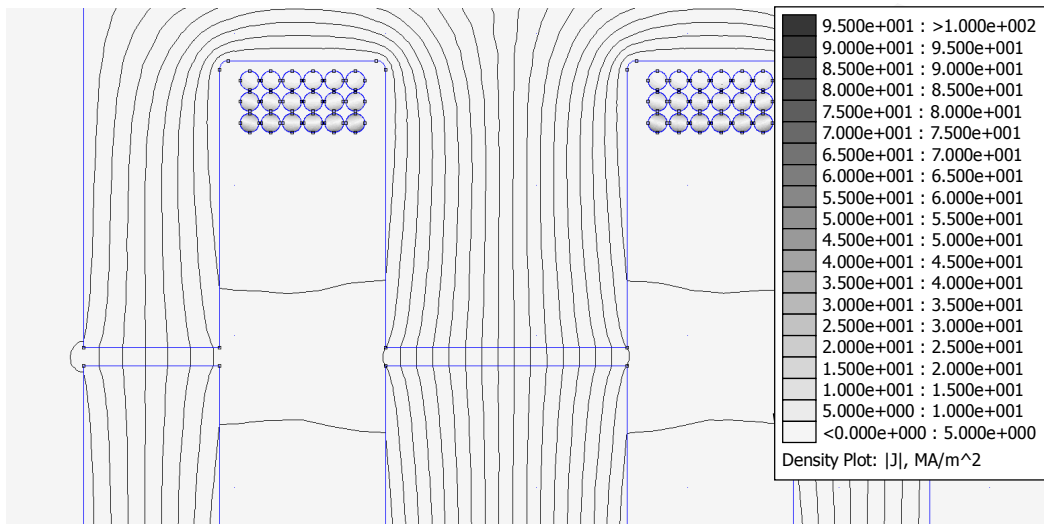
Figure 4.7 100µH inductor with 2x18 turns – current density plot.

The result shows that the total losses depend mainly on the high flux density outside the gap and not on the DC resistance losses – the losses are quartered at a 20% smaller cross section of the wire. Thus, the main task is to shield the winding against this flux – without conductive materials. A possibility would be the introduction of low μ_r materials in the gap. This keeps the flux away from the windings. Further studies and trials are necessary to prove this assumption.

5 Circuit Realisation

In this chapter, the realisation of the Half-Bridge Unit, the Controller Unit, the Circuit Protection Unit and auxiliary circuits is explained. The Half-Bridge Unit is implemented and tested separately. The transformation of the designed controller into an electric circuit is shown on the basis of circuit diagrams. At last the overall device is tested and the measurements are compared to the simulation results. Special advantages and disadvantages are pointed out.

5.1 Half-Bridge

The Half-Bridge consists of the DC-Link – the DC link capacitors with balancing resistors – and the semiconductor switches – ROHM's SCH2080KE with connections for the gate drive. Figure 5.1 shows the circuit diagram with all selected values.
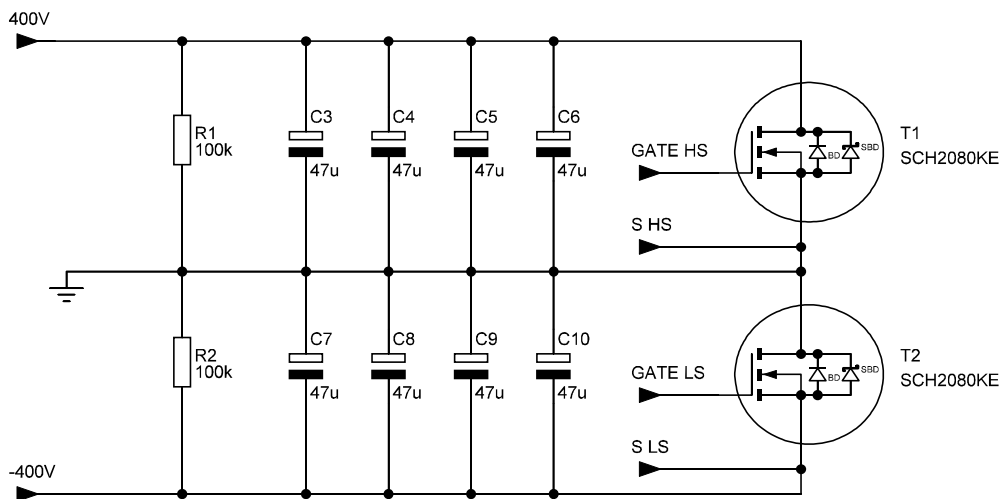
Figure 5.1 Half-Bridge with DC-Link.

For determining the capacitor values, an estimation of the worst case for the voltage drop precedes. Figure 5.2 shows the relevant circuit for this estimation.
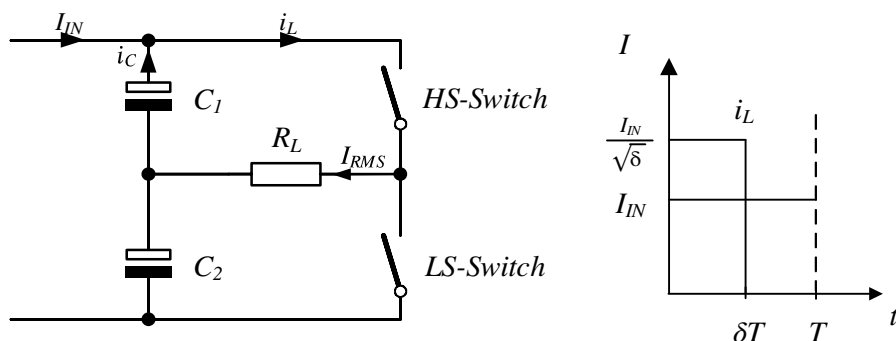
Figure 5.2 Circuit for the estimation of the highest voltage drop at the DC-Link.

Only the High-Side-switch (HS-switch) is considered. For the load current I_{RMS} the maximum value, specified in the requirements table, of 10A is selected. In case of steady state $I_{IN} = I_{RMS} = constant$. The current i_L through the HS-switch depends on the duty cycle δ, and also the current i_C through the capacitor C_1.

$$i_L = \begin{cases} \dfrac{I_{IN}}{\sqrt{\delta}}, & \delta \\ 0, & 1-\delta \end{cases} ; \qquad i_C = \begin{cases} I_{IN} - \dfrac{I_{IN}}{\sqrt{\delta}}, & \delta \\ I_{IN}, & 1-\delta \end{cases} ; \quad 0 < \delta \leq 1 \qquad (5.1)$$

The highest voltage drop occurs at a duty cycle $\delta = \frac{1}{4}$. The value for the voltage drop then is calculated via

$$\Delta U_C = \frac{I_{IN} \cdot T}{C} \left(\delta - \sqrt{\delta}\right) \qquad (5.2)$$

with I_{IN}=10A, C=200µF, T=10µs and $\delta = \frac{1}{4}$ to $\Delta U_{C,max} = 0.125$V, which is a relative small value compared to the 400V supply voltage. So the DC-Link can be considered nearly ideal for all further steps.

Beside the capacitance, the balancing resistors have to be determined. These resistors, R_1 and R_2 of Figure 5.1, are necessary to ensure that the voltages of $C_3 \ldots C_6$ are equal to the voltages of $C_7 \ldots C_{10}$. This voltages can differ due to different R_{ESR}, equivalent series resistance, of each capacitor. This is an already known phenomenon. For determining R_1 and R_2 empirical formulas are used. There exist for example $R_B \cdot C \approx 50$s [26, p. 136] and $R_B \cdot C \approx 10$s [27]. The spread shows that this is not an exact approach but in practice, it is sufficient. For the resistors the arithmetic mean of the results of these formulas is selected, $R_1 = R_2 = 100$kΩ.

There exist also other strategies to maintain equal voltages at the capacitors such as active balancing [28].

5.2 MOSFET Driver

In this master thesis, a special integrated circuit (IC) is used to drive the MOSFETs, a Si8234 from Silicon Labs [29]. It combines two independent, isolated drivers into a single package. The Si8234 is a high-side/low-side driver with a peak output current of 4.0A. Driver outputs can be grounded to the same or separate grounds or connected to a positive or negative voltage. The power supply voltage of the IC has to be in the range of 4.5V to 5.5V. The basic block diagrams are shown in Figure 5.3.
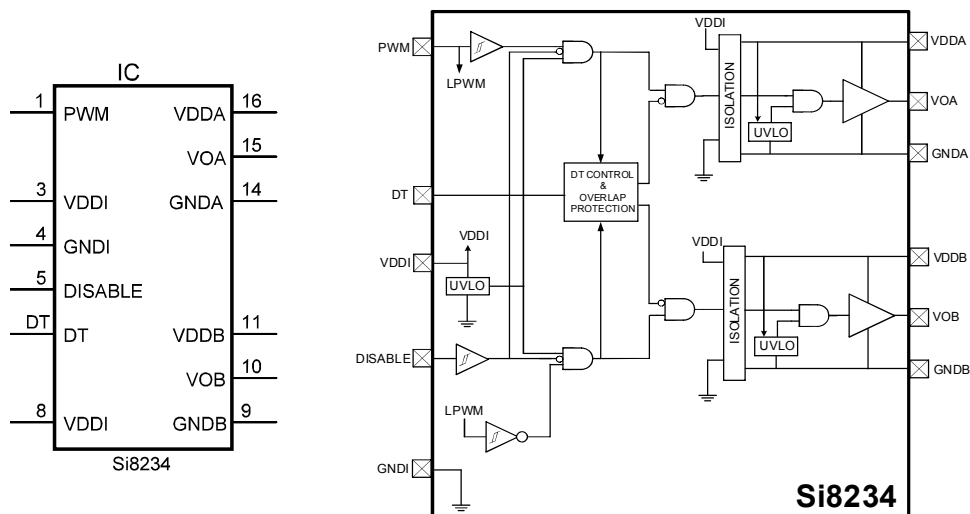
Figure 5.3 Basic block diagrams of the Si8234 [29].

The operation of a Si8234 channel is analogous to that of an optocoupler and gate driver, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up.

It is most important to minimize ringing in the drive path and noise on the Si8234 VDD lines. Care must be taken to minimize parasitic inductance in these parts by locating the Si8234 as close to the MOSFETs as possible.

Undervoltage Lockout (UVLO) is provided to prevent erroneous operation during device startup and shutdown or when VDD is below its specified operating circuits range. The input (control) side, Driver A and Driver B, each have their own undervoltage lockout monitors.

When brought high the disable input unconditionally drives VOA and VOB low regardless of the state of the PWM input.

The Si8234 includes programmable overlap protection to prevent outputs VOA and VOB from being high at the same time. The device also includes programmable dead time generatrion, which adds a user-programmable delay between transitions of VOA and VOB. When enabled, dead time is present on all transitions, even after overlap recovery. The amount of dead time delay (DT) is programmed by a single dead time programming resistor (RDT) connected from the DT input to ground per Equation (5.3).

$$(Dead\ Time\ [\text{ns}])\ DT \approx 10 \cdot RDT\ (Dead\ Time\ Programming\ Resistor\ [\text{k}\Omega]) \quad (5.3)$$

If the dead time pin is tied to VDDI or left floating a nominal dead time of approximately 400ps is provided.[1]

Based on this the circuit configuration for the input side is designed, see Figure 5.4.
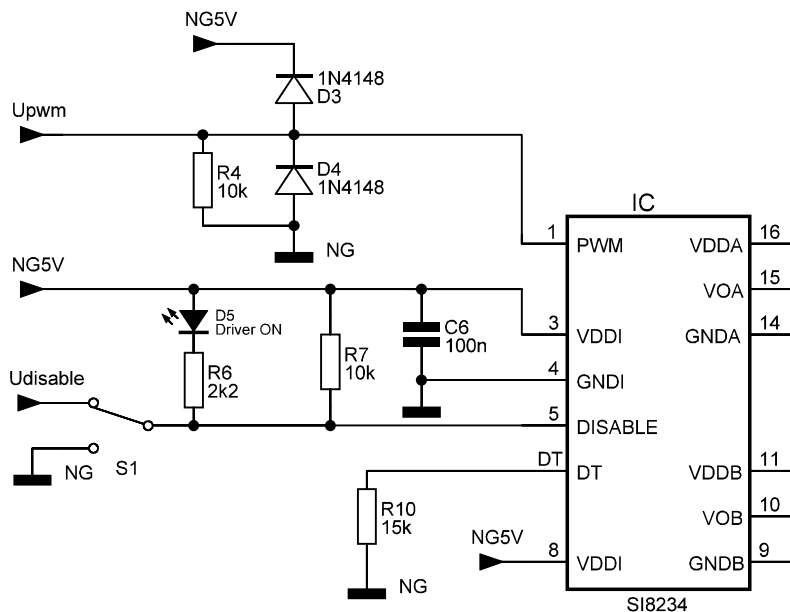
Figure 5.4 Circuit configuration at the input side of the Si8234.

For the protection of the PWM input two diodes are installed. In this configuration the voltage range can be $-0.7\text{V} < U_{PWM} < 5.7\text{V}$. A LED indicates the state of the Si8234 and a 15kΩ resistor determines approximately 150ns dead time. The disable input can be tied automatically to ground, what significates always on, or can be controlled by the controller circuit.

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[1] The information of these paragraph bases on the datasheet of the Si8234 [29].

At the output side two identic circuits are needed to provide the voltage levels and energy for driving the gates of the MOSFETs. Figure 5.5 shows one – for the HS-gate – of these identic circuits.
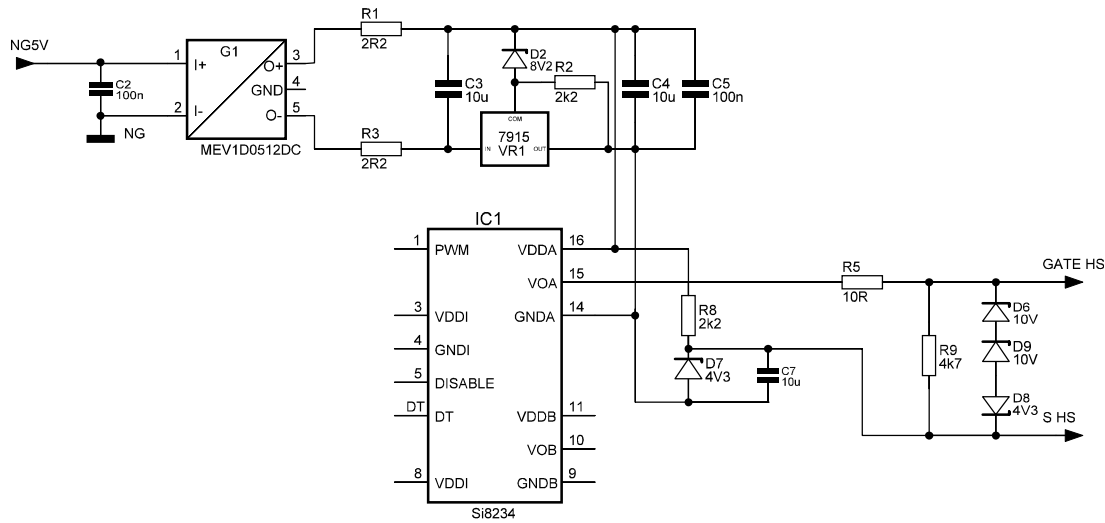
Figure 5.5 Circuit configuration at the output side of the Si8234.

First, the required voltage levels are identified. The gate-source voltage of the SCH2080KE has to be in the range of $-6V$ to $22V$. It is recommended in the datasheet to use gate-source voltages near the limits to benefit from lower conduction losses and faster switching times. On the other hand, the drivers of the Si8234 operate with a maximum supply voltage of 24V. Therefore, the $+5V$ from the power supply are converted first into $\pm12V$ by a DC-DC converter and then, this voltage is regulated to approximately 23.2V by a 7915 voltage regulator and a 8.2V Zener diode. This guarantees that the driver supply voltage does not exceed the 24V maximum. R_8 and the 4.3V Zener diode D_7 form the negative voltage for the gate. Therefore, the voltage levels for the gate are approximately $-4.3V$ and $18.9V$.

R_8 is the gate resistor. The value of 10Ω is selected because of datasheet recommendations. To protect the gates from overvoltage three Zener diodes are inserted. Therefore, the voltages at the gates can be in the range of approximately $-5.7V$ and $20.7V$.

It is mentioned in the Si8234 datasheet that the drivers must be placed as near as possible to the MOSFET gates. Therefore, a special arrangement for the connection of the Driver's PCB and the Power PCB with the MOSFETs is developed, see Figure 5.6.
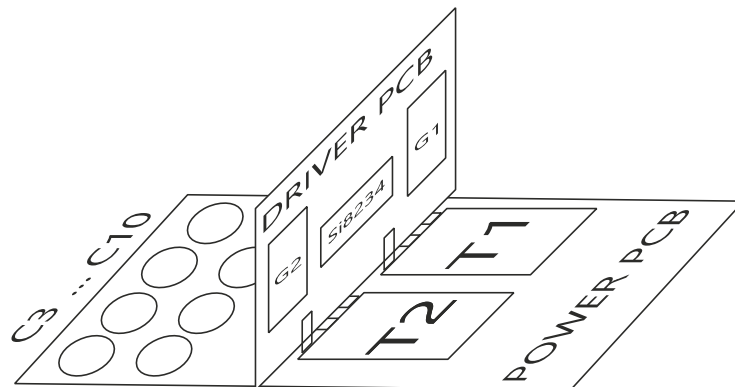
Figure 5.6 PCB Realisation: Schematic sketch of the Half-Bridge Unit.

In this arrangement, the length of the connecting copper paths between the drivers and the gates is minimized. In Addition, there is no demand for additional space, because the Driver's PCB height is almost the same as the height of the capacitors $C_3 \dots C_{10}$.

5.3 Test Procedures – Half-Bridge Unit

The Power PCB and the Driver PCB are connected as shown in Figure 5.6. These parts are separately tested to confirm the functional capability of the combination: MOSFET driver + MOSFETs. In the laboratory is no 400V DC power supply available, thus two 300V DC power supplies with a maximum current of 10A are selected for all test procedures. Figure 5.7 shows the test circuit. It is possible to switch a resistance of $R_L = 40\Omega$ to force a load current i_L. Beside i_L, the voltage u_{out}, that is further connected to the Filter Unit, is measured.
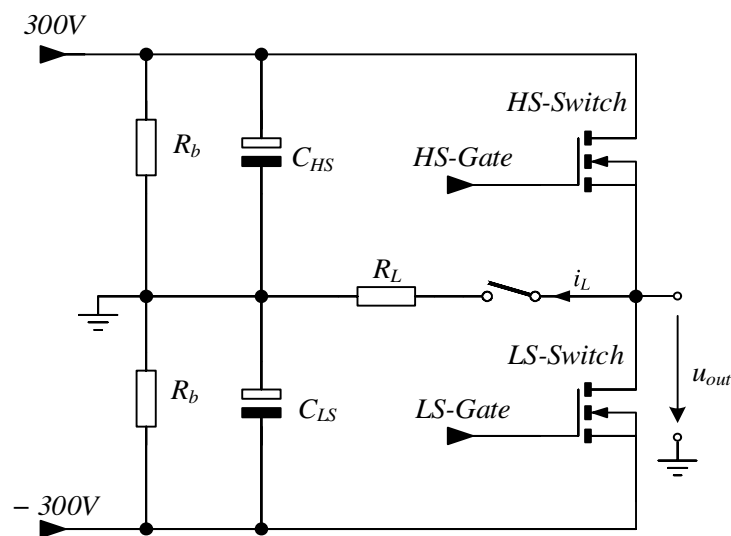
Figure 5.7 Half-Bridge Unit: Test circuit.

Figure 5.8 shows u_{out} at duty cycles of 50% and 5%. The voltage has nearly ideal switching character. Only small switching surges of 20V occur. At 5% duty cycle, the voltage curve has an obvious rectangle shape as well and the surges are equal as for the 50% duty cycle case.
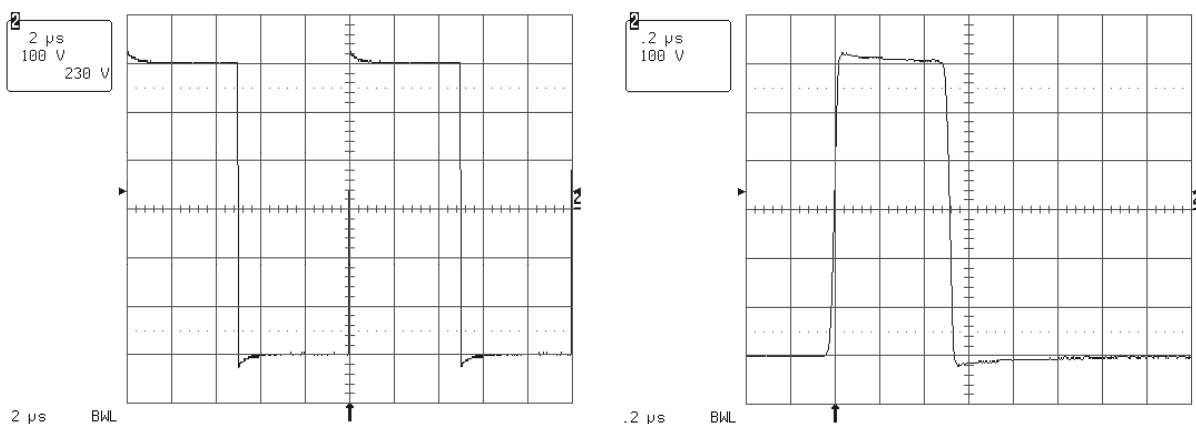
Figure 5.8 Half-Bridge Unit: 50% (left) and 5% (right) duty cycle, no load – u_{out}: channel 2.

Another measurement verifies the data for the rise and fall time of the MOSFETs datasheet [14]. Figure 5.9 shows the zoomed rising edge and falling edge of u_{out}.
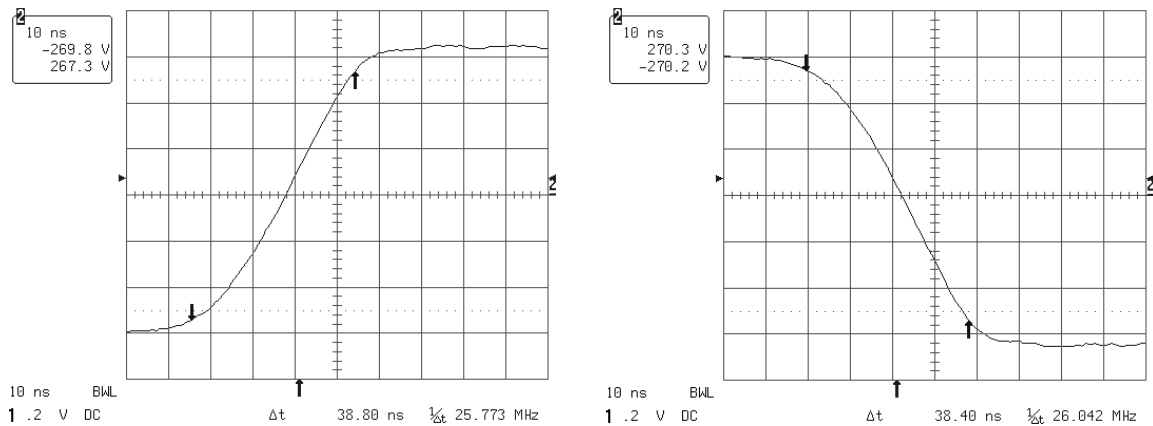
Figure 5.9 Half-Bridge Unit: Verification of the rise and fall time, no load – u_{out}: channel 2.

The measurement result for the rise time is $t_{rise} = 38.8$ns and for the fall time $t_{fall} = 38.4$ns. These values are nearly equal to the values specified in the datasheet. Only the measured fall time is 10ns slower. These results provide more information about the influence of the gate resistance – in the datasheet 6.3Ω, in the realised circuit 10Ω. Generally, a higher gate resistance leads to slower fast and rise times. In this case, however, only the fall time is slower. Nevertheless, the curve shape can be treated as ideal for the system model.

Figure 5.10 shows the switching behaviour for a load resistance of 40Ω. It is interesting, that the switching surges are equal or almost smaller than in the no-load case. Another result is the noticeable inductance of the used resistor. According to $\tau = \frac{L_R}{R_L}$ the inductance calculates with the measured τ=0.1μs and R_L=40Ω to L_R=4μH.
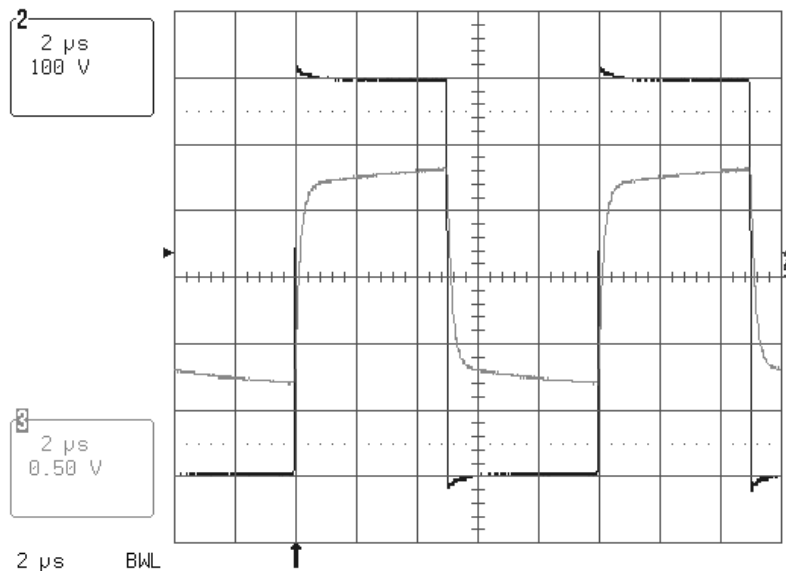
Figure 5.10 Half-Bridge Unit: 50% duty cycle, 40Ω load – u_{out}: channel 2, i_L: channel 3 – 5A/div.

The measured overall behaviour of the Half-Bridge Unit confirms the assumption of an ideal half-bridge amplifier in the system modelling section 3.1. It also proves the low-inductive rooting of the layout.

5.4 Auxiliary Voltage Supply

In the input specifications a +5V single supply for the supply of the control circuits is declared. For the most OPA circuits, however, it is necessary to introduce a new reference voltage U_{ref}, to execute the required operations. For instance the PI controller – realised by an OPA, resistors and a capacitor – would count never down if the OPA circuit is referenced to ground, because the input voltage is always equal or higher than ground. This new reference voltage therefore is set nearly to the half supply voltage to have equal positive and negative voltage ranges. U_{ref} is realised by a programmable shunt regulator TL431[30] with a series resistor and capacitor. This part provides an output voltage in the range of 2.44V … 2.55V, depended on the ambient temperature.

In the controller, the exact doubled reference voltage is needed to avoid offset errors. Already a small offset of 10mV – the range of the TL431 – causes an output offset voltage of 2V because of the high DC gain $K = 200$. To avoid this, an additional series voltage regulator, which doubles the TL431 output voltage, is introduced. It is realised by a non-inverting OPA circuit with a transistor to increase the output current. A 5.6V Zener diode limits the output voltage in case of error and a fuse reacts in case of short circuit to protect the other circuit parts. The LED D6 indicates the state of the regulator. Figure 5.11 shows the TL431 and the series voltage regulator circuit. U_{ref} is named there and for all following circuits U2V5.

Figure 5.11 Generation of the reference voltage U2V5 and series voltage regulator for the auxiliary supply voltage U5V.

5.5 Triangular Wave Generator

The Triangular Wave Generator is realised by a frequency determining square wave generator followed by an integrator. Figure 5.12 shows the two parts.
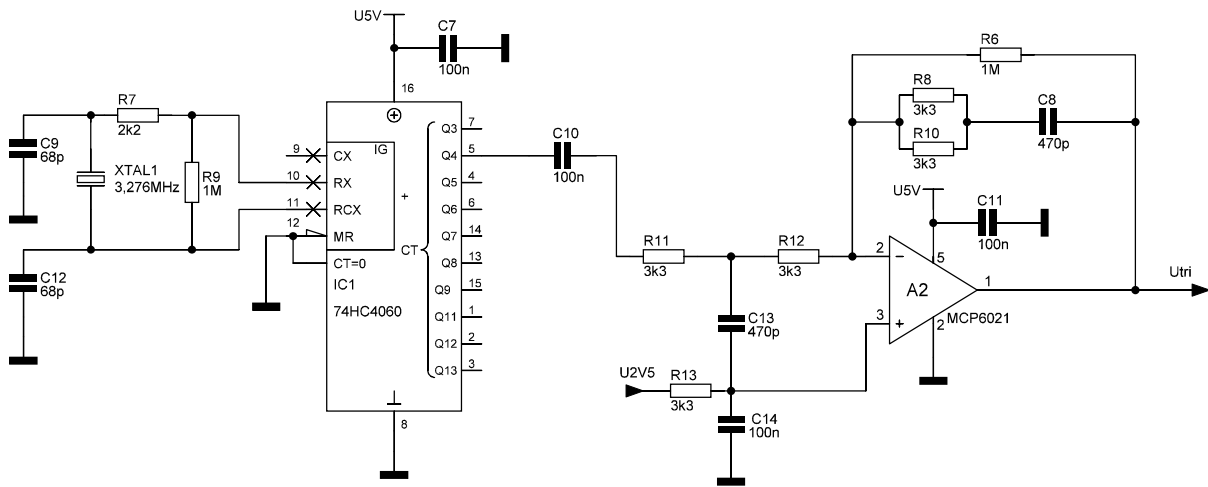
Figure 5.12 Circuit realisation of the Triangular Wave Generator.

The square wage generator is formed by the IC 74HC4060 – a 14-stage asynchronous binary counter and oscillator. In this work, the oscillator configuration is needed. It is only necessary to place few parts – two resistors, two capacitors and the frequency determining crystal oscillator. The configuration bases on the recommendations in the datasheet [31]. The frequency of the crystal oscillator is divided by 32 – the relevant output pin is Q4 – to get approximately the desired 100kHz. Then the square wave has to be transformed into a triangle wave. The obvious approach is to integrate the square wave. Therefore, an integrator, based on a inverting amplifier, is developed, see Figure 5.13.
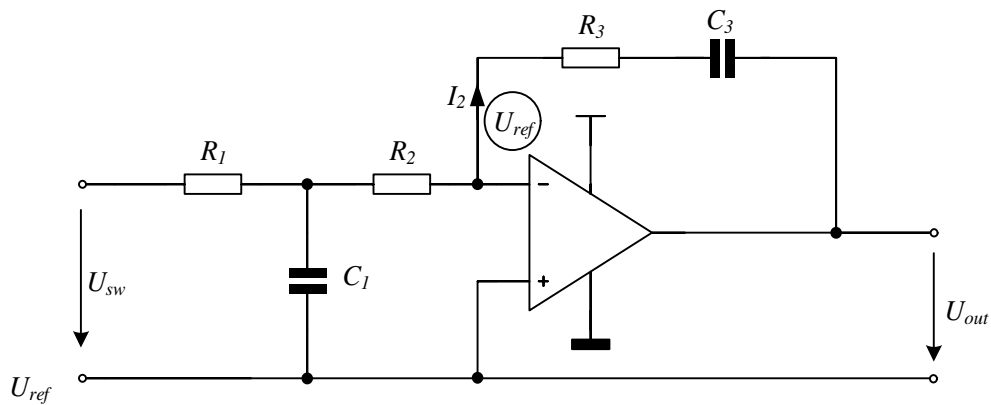
Figure 5.13 Sketch for calculating the integrator transfer function.

The OPA is considered ideally. That means, among others, infinite input resistances – zero input current – and infinite open loop gain. So, the transfer function of the current I_2 is calculated to Equation (5.4).

$$\frac{I_2}{U_{sw}} = \frac{1}{(R_1 + R_2) + s(C_1 R_1 R_2)} \tag{5.4}$$

The output voltage is calculated with $U_{out} = -I_2 \cdot (R_3 \cdot \frac{1}{sC_3})$ and the introduction of V_I to Equation (5.5).

$$\frac{U_{out}}{U_{sw}} = \frac{V_I}{s} \cdot \frac{\frac{1}{V_I} + \frac{C_3 R_3}{V_I}}{C_3(R_1 + R_2) + s(C_1 C_3 R_1 R_2)} \tag{5.5}$$

There the integrator behaviour can be seen in the first fraction $\frac{V_I}{s}$. If the second fraction is made to one with the relationships in Equation (5.6)

$$\frac{1}{V_I} = C_3(R_1 + R_2), \quad \frac{C_3 R_3}{V_I} = C_1 C_3 R_1 R_2 \quad \rightarrow \quad C_1 = C_3; R_1 = R_2 = 2R_3; \tag{5.6}$$

V_I results in Equation (5.7).

$$V_I = \frac{1}{2C_1 R_1} \tag{5.7}$$

This result allows to determine V_I only by setting C_1 and R_1. Then it is only necessary to insert the given frequency and voltages to calculate V_I.

$$V_I = \frac{\hat{U}_{triangle} \cdot 2f}{U_{ref}} = \frac{4\text{V} \cdot 2 \cdot 102.375\text{kHz}}{2.5\text{V}} = 327.6\text{ks}^{-1} \tag{5.8}$$

Then the parameters are selected to $R_1 = 3.3\text{k}\Omega$ and $C_1 = 470\text{pF}$, so that $V_I \approx 322.4\text{ks}^{-1}$. This results in a failure of $\approx 1.5\%$. The functional capability of the circuit was tested in Multisim. There the circuit works well so that this topology is used.

5.6 Controller Circuit

The controller circuit contains all relevant parts of Figure 3.10, except the filter inductors, capacitors and the DC gain K. Therefore, the feedback of the capacitors current sC_1P_1, the feedback of the output voltage divided by K, the PI controller itself and the two summation nodes have to be realised. It is also necessary to adjust the input signal of the waveform generator. In the specifications a input range of $-2\text{V} \dots + 2\text{V}$ is declared. This range itself – 4V – is equal to the voltage range of the triangle signal. Only the offset has to be set to a value of 2.5V.
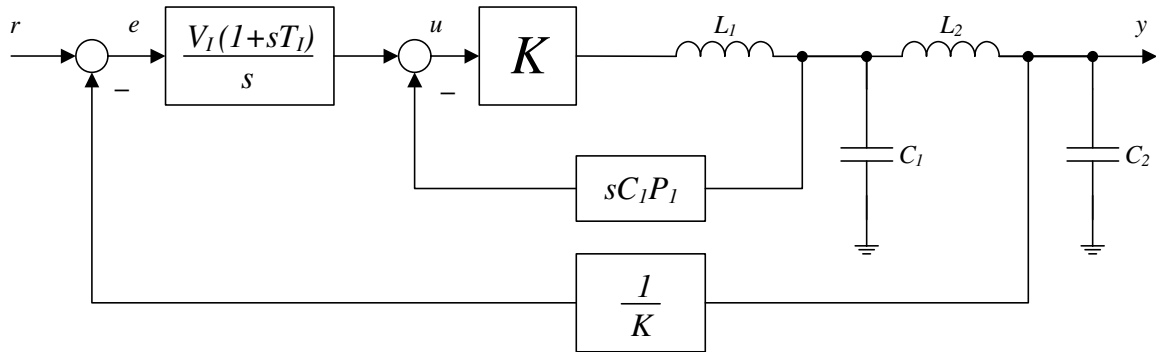
Figure 3.10 Relevant system model, 2nd order Bessel filter approach.

The feedback of the capacitors current is realised by a passive current transformer. This is possible because the capacitors current has no DC part. P_1 is built out of the number of turns of the winding and the resistor R_3, see Equation (5.9).

$$P_1 = \frac{N_1}{N_2} \cdot R_3 \tag{5.9}$$

$N_1 = 1$, $N_2 = 44$ and $R_3 = 3.9\Omega$. These parameters lead to $P_1 = 88.6\text{m}\Omega$.

The feedback of the output voltage is realised by a differential amplifier. The output voltage, however, has to be divided first by a resistor chain. Eight resistors with $100\text{k}\Omega$ for each input of the OPA are used. This is necessary to avoid possible voltage overload due to the small dimension of the used 0805 resistors. The first four resistors are placed on the Power PCB and the second eight on the Controller PCB. Figure 5.14 shows the relevant circuit parts.
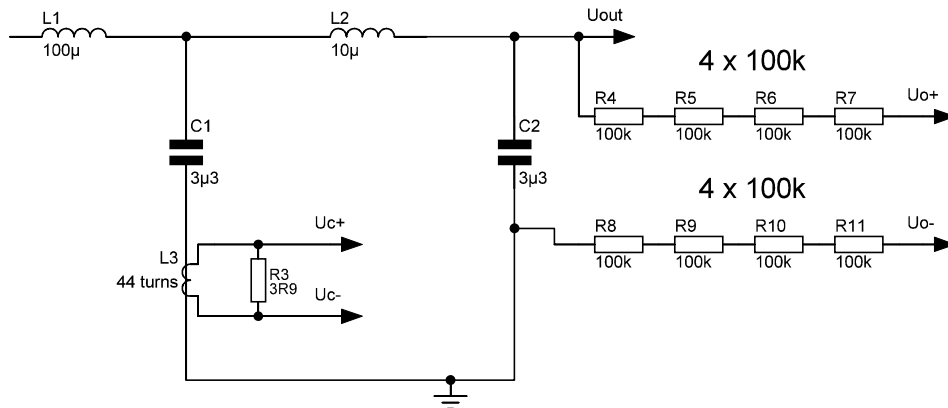
Figure 5.14 Circuit of the Filter Unit with passive current sensing transformer and voltage dividing resistors.

Figure 5.15 shows the first part of the controller circuit. The input signal comes from a waveform generator with 50Ω output resistance. A pull-down resistor is placed to avoid unpredictable input voltages in case of open input. One OPA of the MCP6022 – A3 – adds an offset of 2.5V and inverts the input signal. For this operation, it is necessary to apply the doubled reference voltage.
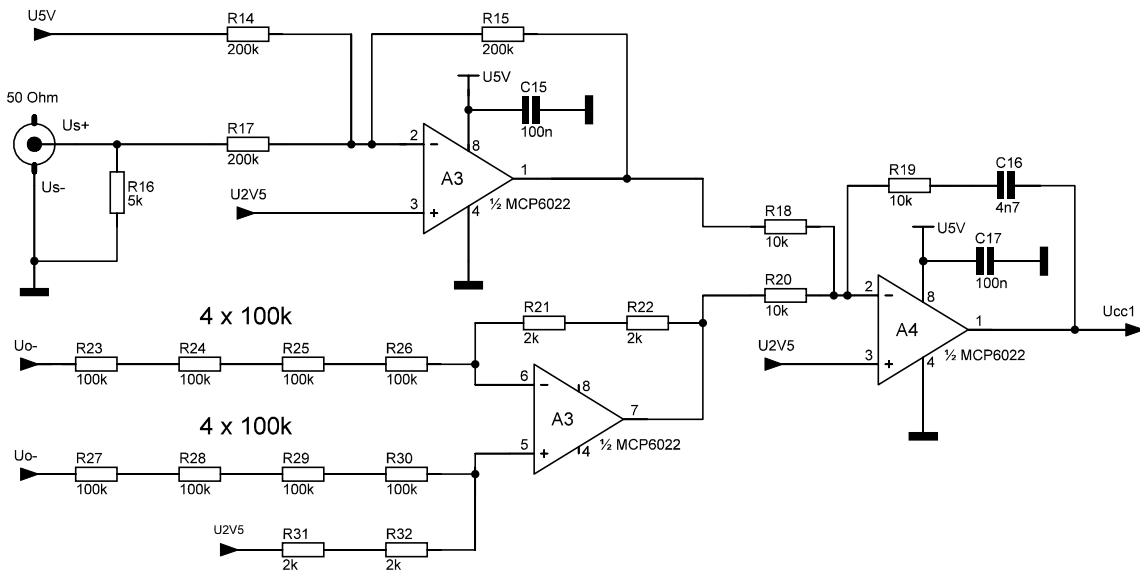
Figure 5.15 Controller part 1: Condidtioning of the input signal, output voltage feedback and PI controller.

The other OPA of A3 is used for dividing the output voltage by $K = 200$. Then the adjusted input signal and the divided output voltage are summed by the resistors R_{18} and R_{20}. This summing signal, however, is polarity reversed than it should be. This property is used in the PI controller. The output signal there becomes also negative because the two times negation gives the correct signal. Thereby, two OPAs can be reduced. The proportional gain $K_P = 1$ is realised by equal values of R_{18}, R_{19} and R_{20}. The V_I parameter of the PI controller is calculated by $V_I = \frac{1}{R_{19} \cdot C_{16}}$. It is not possible to reach the desired value $V_I = 23.73 k\text{s}^{-1}$ with available capacitors. To avoid higher overshoot the next smaller value is selected, $V_I = \frac{1}{10\text{k}\Omega \cdot 4.7\text{nF}} = 21.3\text{ks}^{-1}$.

Figure 5.16 shows the second part of the controller circuit. There, another differential amplifier is used to subtract the capacitor's current feedback voltage from the passive current transformer. Also two RC low-pass elements are introduced to reject high frequency harmonics from the current transformer signal. At last, the PWM generating comparator A5 is placed. The MCP6561 [32] is a comparator with 47ns propagation delay time, which is sufficient for this purposes. There are also other faster comparators available, e.g. the TLV3501, but the MCP6561 worked precise and without faults in the testing phase. At the inputs again RC low-pass filters are placed.
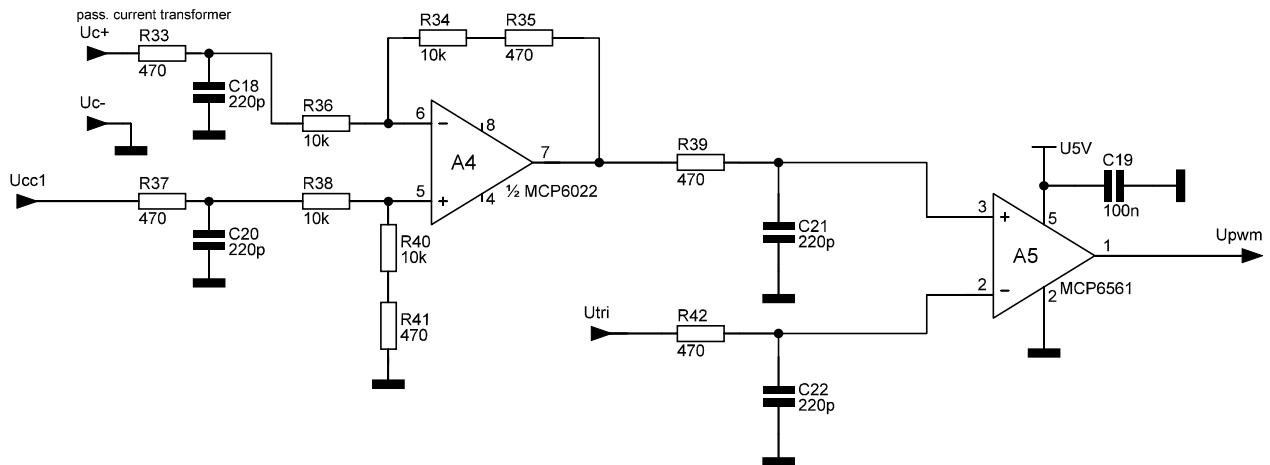
Figure 5.16 Controller part 2: Feedback of the capacitors current and generation of the PWM signal.

5.7 Circuit Protection Unit

The Circuit Protection Unit protects the device against short circuit and overload. The active current transformer LEM's LTS 25-NP and a window comparator detect short circuit. Thermal overload is detected by a temperature depended switch.

Figure 5.17 – on the next page – shows the two error detecting circuits. The LTS 25-NP is placed after L_1 so that the noise caused by the high du/dt -rate of the Half-Bridge Unit's output voltage is minimized. The active current transformer generates a voltage from 0.5 to 4.5V, linear depended on the measured current, see LTS 25-NP datasheet [33]. The resistor chain R_{43}, R_{44} and R_{47} creates the switching levels for the comparators MCP6561. These voltages represent current limits of approximately $\pm 77\text{A}$ in the used input pin configuration of the LTS 25-NP. For overload detection, a temperature depended switch – 67F080 – with a switch point of 80°C and ± 5°C hysteresis is used.
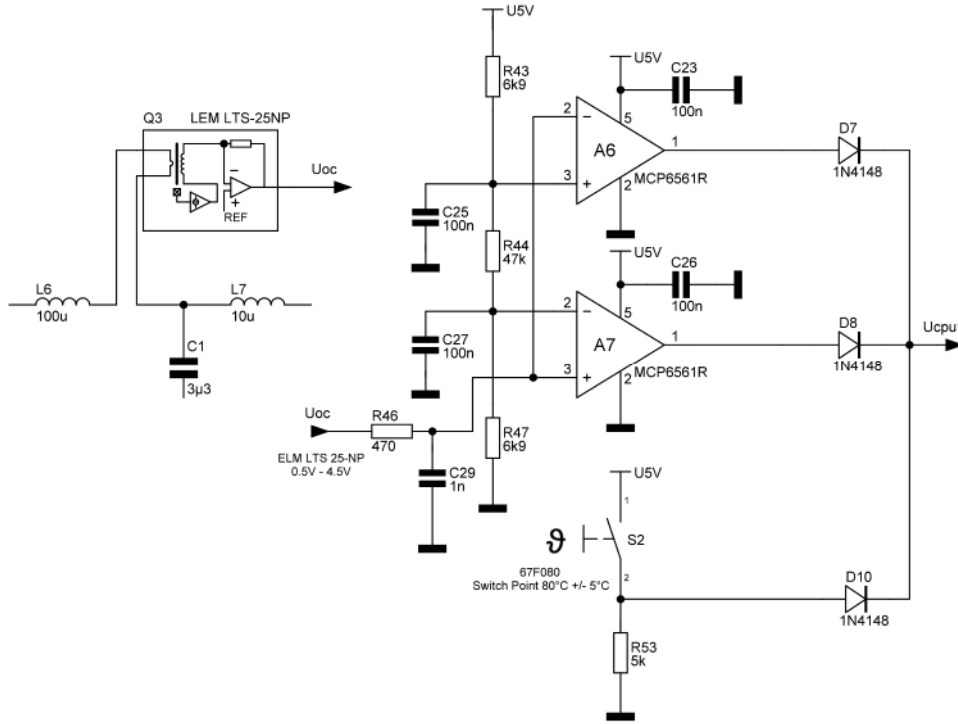
Figure 5.17 Circuit Protection Unit part 1: LEM LTS 25-NP, window comparator and temperature depended switch 67F080.

Figure 5.18 shows the RS-latch with start-up circuit. If an error occurs the input at U_{cpu1} goes HIGH and sets the latch. The reset-button allows resetting the device to normal operation. If the errors still occurs, the latch immediately is set again. In the used latch configuration the initial state – no error – is defined by a start-up circuit. If the plug-in power supply is connected to the grid, the reset input rests HIGH until the capacitor C_{30} is charged to ≈ 0.7V. In this case the transistor BC547 starts conducting and pulls the reset input to LOW. The start-up operation lasts ≈ 330ms. The LED D_9 indicates the error state.
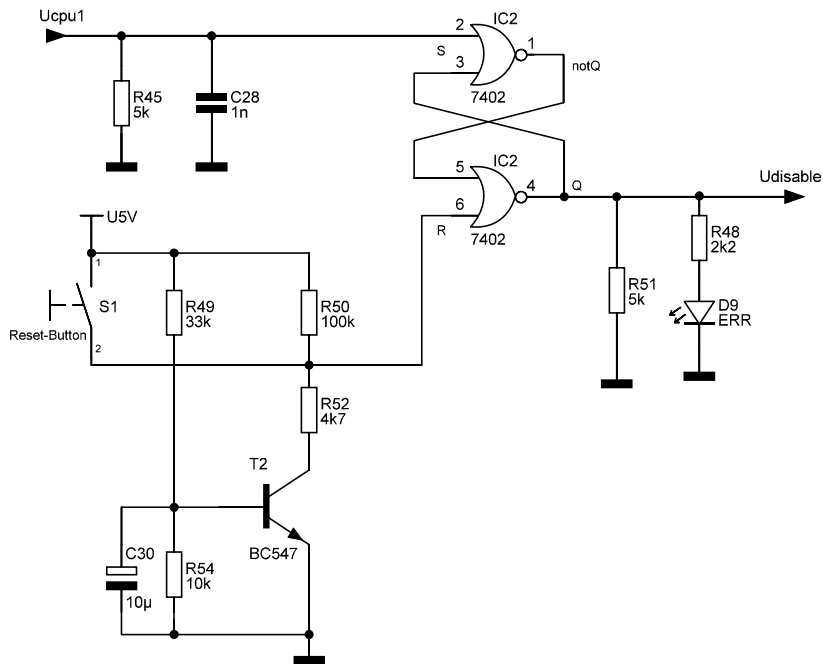
Figure 5.18 Circuit Protection Unit part 2: RS-latch and start-up circuit.

5.8 Test Procedures – Overall Implemented Circuit

After realising the overall system, its functional capability is tested. The test circuit topology is shown in Figure 5.19. Instead of the ± 400V supply voltage, only DC power supplies with ± 300V are available, as described in section 5.3. The filter capacitors have only 3.15μF instead of the 3.3μF rated capacitance – measured with a TEKDMM830 multimeter. The inductance of the self-designed inductor is 99.5μH and also the coilcraft inductors have nearly exact the inductance of 10μH – measured with a HOIKO 3532-50 LCR HiTester.

At the output pin, a resistive load can be switched on or off. The measured parameters are the output voltage u_{out}, the output current i_{out} and the filter input current i_{L_1}.
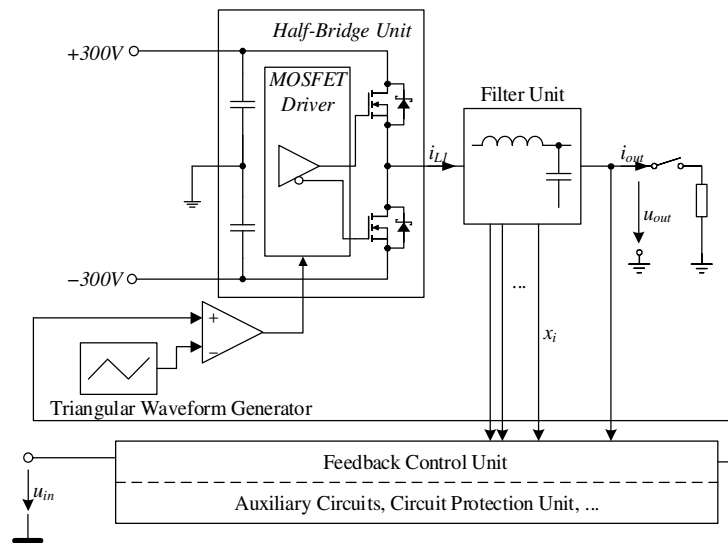
Figure 5.19 Test circuit for the realised system.

The simulation is executed again to consider the changed parameters, especially the ± 300V supply voltage and the smaller capacitors – see Figure 5.20.
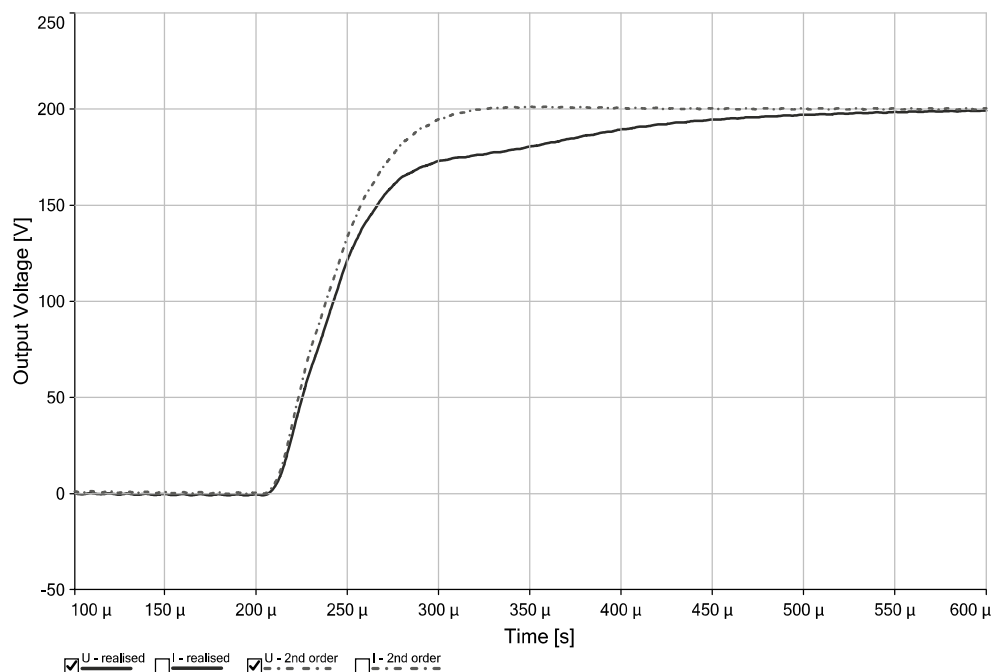
Figure 5.20 Simulated step response of the realised system.

It is evident, that the system with the new parameters lead to a not optimal result. An analysis shows that especially the ±300V supply voltage causes the changed curve shape of the step response. In contrast to the changed supply voltage, the influence of the changed capacitances is small. Therefore, it is necessary to take the variation of the supply voltage into account, if an approved version of this power amplifier is developed.

Nevertheless, for testing the designed feedback control loop the simulation results based on the changed parameters are compared to the measured results. If the simulated and measured results of the realised system coincide, the simulated results for the designed system – ±400V supply voltage, 3.3µF capacitors – can be expected also for a real system with these parameters.

The simulated curve shape, rise time and settling time are compared to the measurements. Figure 5.21 and Figure 5.22 show the related measurement results that look similar to Figure 5.20.
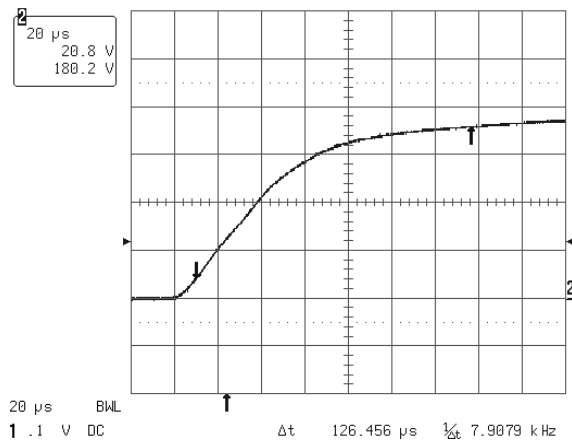
| Figure 5.21 Step response: rise time, u_{out}: channel 2 – 50V/div. | Figure 5.22 Step response: settling time, u_{out}: channel 2 – 50V/div. |
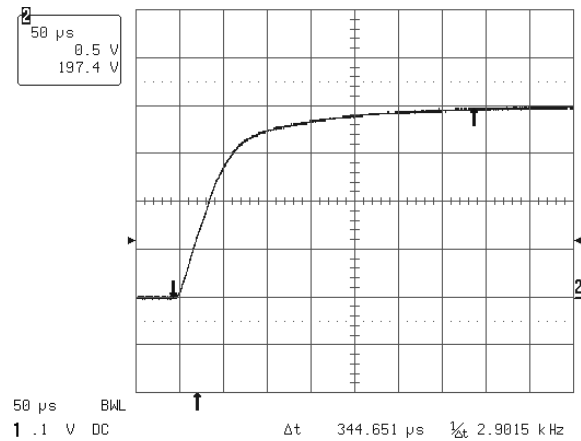
The analysis of the rise time and the settling shows that the error is minimal – in case of the rise time 3.4% and in case of the settling time 2.6%, see Table 5.1. Therefore, the basic function capability of the power amplifier and all related parts is proved – visually and analytically.

Simulated Rise Time [µs]	Measured Rise Time [µs]	Simulated Settling Time [µs]	Measured Settling Time [µs]
131.0	126.5	336.0	344.7

Table 5.1 Step response: Comparison of the measurement and simulation results.

At first, ten pieces of the 10µH coilcraft inductors are used to form L_1=100µH. It occurred, however, the problem of overheated cores. It lasts only 10 to 15 minutes till the cores – especially the first two, three cores near the half-bridge – reach a temperature of over 100°C. Therefore, the 10µH inductors are replaced by the self-designed 100µH inductor. The core of this inductor keeps cool but the two windings reach a temperature of approximately 70°C to 80°C. Therefore, a small fan is installed under the inductor for cooling the two windings.

The simulation results of the self-designed inductor with a winding near the air gap, made in FEMM, are also proved. If one winding is placed near the air gap the temperature rises quickly. Here again, at 100°C the test is stopped. That proves not the predicted values of 7.5W compared to 40W but the overall behaviour.

The next measurement concerns the filter input current, the current flowing through the inductor L_1. Figure 5.23 shows the simulation results.
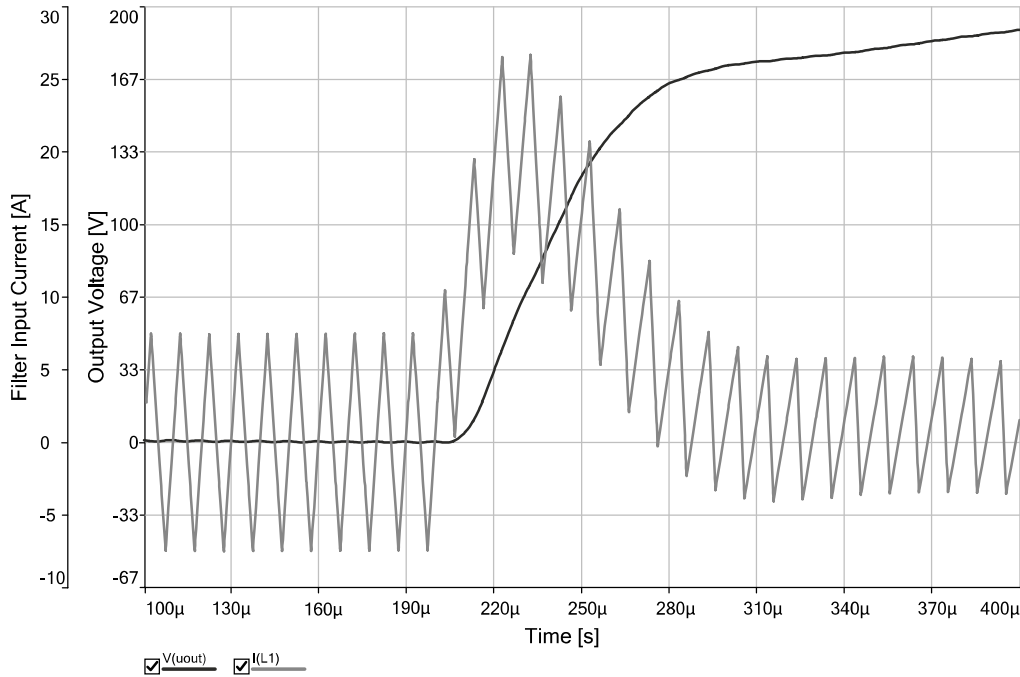
Figure 5.23 Simulated step response with filter input current of the realised system.

The peak value 26.8A of the filter input current occurs at approximately three to four switching periods and determines the highest gradient of the rising output voltage. The measurement of the filter input current shows a peak current of 26.2A, what is nearly the same value compared to the simulation, see Figure 5.24.
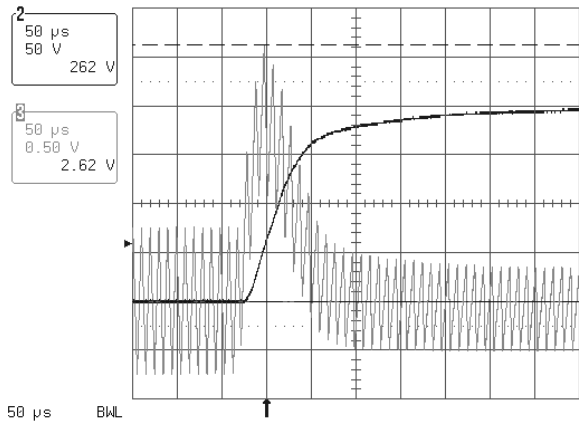
Figure 5.24 Step response: filter input current

u_{out}: channel 2, i_{L_1}: channel 3 – 5A/div.
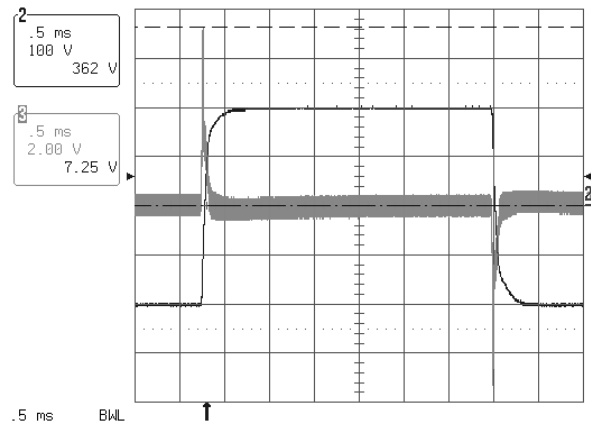
Figure 5.25 Square wave signal: -200V... 200V, filter input current,

u_{out}: channel 2, i_{L_1}: channel 3 – 20A/div.

Figure 5.25 shows a square wave signal with $\pm$200V at the output. The filter input current here has a peak value of 72.5A, what is much more than the simulation result of 53.7A for this case. It has to be mentioned, that the peak value of the measurement is not stable and varies from 60A to 75A, depending on the start time of the rising of the output voltage in relation to the

respective value of the triangle current. Table 5.2 summarizes the simulation and measurement results for the peak value of the filter input current.

Simulated $\hat{i}_{L_1}$ Step Response [A]	Measured $\hat{i}_{L_1}$ Step Response [A]	Simulated $\hat{i}_{L_1}$ Square Wave -200V… 200V [A]	Measured $\hat{i}_{L_1}$ Square Wave -200V… 200V [A]
26.8	26.2	53.7	72.5

Table 5.2 Filter input current: Comparison of the measurement and simulation results.

The attenuation of the switching harmonic is measured at an output voltage $u_{out} = 0\text{V}$. The external waveform generator is able to provide DC voltages. Thereby, it is also possible to identify an offset failure of the controller. It is necessary to set the DC input voltage to -4mV to reach the desired output voltage $u_{out} = 0\text{V}$. Therefore, a circuit that allows adjusting the offset is recommended in further circuit versions. In Figure 5.26 it is zoomed into the output voltage. The signal consists of two relevant parts, a 100kHz sine wave and a high frequency-damped oscillation.
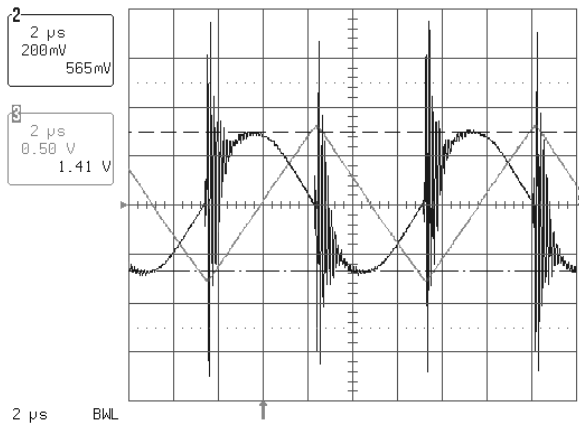
Figure 5.26 Attenuation measurement measured with a common ground line, u_{out}: channel 2, i_{L_1}: channel 3 – 5A/div.
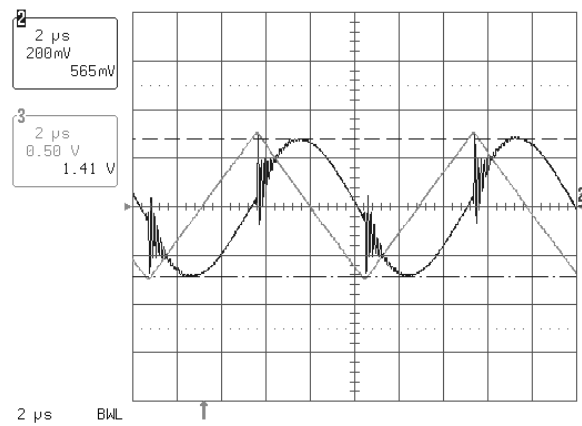
Figure 5.27 Attenuation measurement measured with ground spring, u_{out}: channel 2, i_{L_1}: channel 3 – 5A/div.

The 100kHz sine wave represents the attenuated 100kHz switching harmonic. The amplitude of the sine wave is measured and the attenuation is calculated, see Table 5.3. The theoretic and the measured value are nearly equal. The failure – -0.8dB – is minimal, what proves the theoretical analysis of the system. The simulation result, however, shows a higher attenuation.
Therefore the simulation has to be verified more in detail in case of further analysis.

Simulated Attenuation at f_s [dB]	Theoretic Attenuation at f_s [dB]	Measured Attenuation at f_s[1] [dB]
66.1	63.4	62.6

Table 5.3 Attenuation: Comparison of the measurement and simulation results.

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[1] *Measured. Attenuation at* $f_s = 20 \cdot \log\left(\frac{amplitude\ of\ f_s\ harmonic}{\frac{4}{\pi} \cdot 300V}\right)$

It is assumed that the high frequency-damped oscillation is measured because of the fast switching time of the MOSFETs – results in a high $\frac{\mathrm{d}u}{\mathrm{d}t}$ – in combination with the capacitance of the probe and the inductance of the ground line. The result is a resonant circuit that causes the oscillations. An indication for that assumption is that the oscillation starts always at switching time. Another indicator is that these oscillations are also measured if the probe is near the circuit – not connected to any part of the circuit – and the oscillation amplitude decreases with the distance to the circuit – due to a smaller local $\frac{\mathrm{d}u}{\mathrm{d}t}$. The most important indicator for this assumption is shown in Figure 5.27. There, a ground spring is used instead of the common ground line. Thus, the inductance is decreased what results in significantly lower oscillation amplitudes. The most import issue, however, is that the controller is not affected by these oscillations.

The next measurement concerns the voltage drop in case of a load step. Figure 5.28 shows a load step at the peak of a sine wave and Figure 5.29 shows a load step at a voltage of 100V.
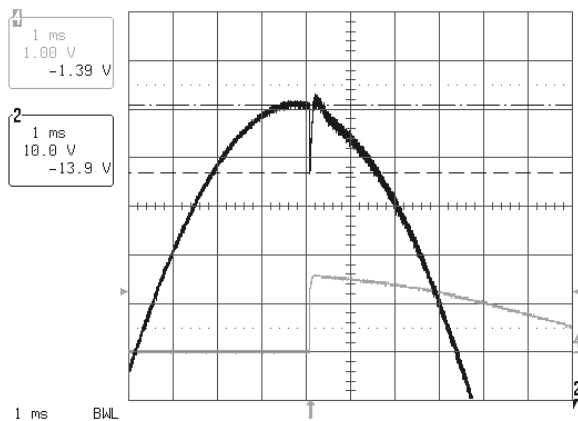
Figure 5.28 Voltage drop measurement, u_{out}: channel 2, i_{out}: channel 4 – 5A/div.
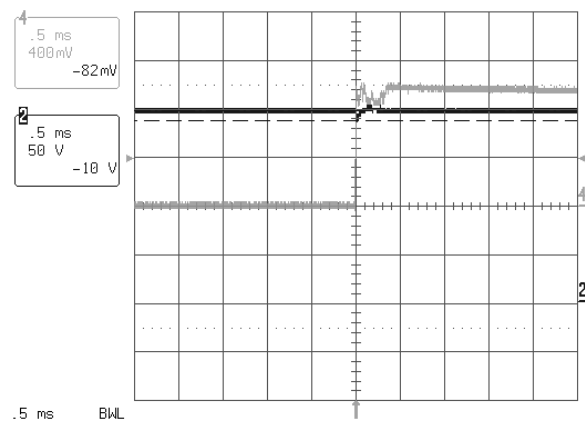
Figure 5.29 Voltage drop measurement, u_{out}: channel 2, i_{out}: channel 4 – 2A/div.

The resulting voltage drops are summarized in Table 5.4 and compared to the simulation results. Also in this case exists only a small difference between the simulation and the real system. A relative voltage drop of $\approx 2\frac{\mathrm{V}}{\mathrm{A}}$ can be determined.

Simulated Voltage Drop 7.5A [V]	Measured Voltage Drop 7.5A [V]	Simulated Voltage Drop 5A [V]	Measured Voltage Drop 5A [V]
14.0	13.9	9.5	10

Table 5.4 Voltage drop: Comparison of the measurement and simulation results.

This measurement, however, shows also the biggest disadvantage of the used circuit topology. At first, a 100V DC voltage was set – without problems. Then the load was switched on. Short time later the over voltage protection of the LS-DC power supply indicated an error. The reason for this error is explained by Figure 5.30. For instance, if a DC voltage of 100V is set and the load is switched on a corresponding DC current flows. If the HS-switch is turned on, there exist no problem. Current flows from the HS-DC power supply through the inductor and the resistance back to power supply. If the HS-switch is turned off and the LS-switch is turned on, the current keep flowing in the same direction because of the inductance. This, however, leads to a charging of the LS capacitor because there is no load, which consumes electric energy besides the balancing

resistor. If the load current is higher, than the balancing current the capacitor is charged every period. At a certain level the over voltage protection of the DC power supply triggers.
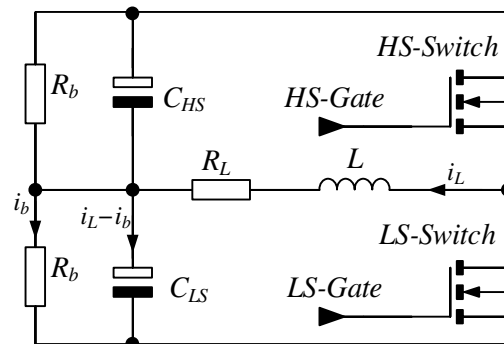
Figure 5.30 Explanation for the tripped over voltage protection of the LS-DC power supply in case of a DC output voltage and a load current.

The last measurement concerns the behaviour of the controller in case of non-linear loads. Therefore, a bridge rectifier with a resistor is used a load. It is also introduced a small inductor before the bridge rectifier for reducing the current peak. The results for a sine wave and a triangle wave are shown in Figure 5.31 and Figure 5.32.
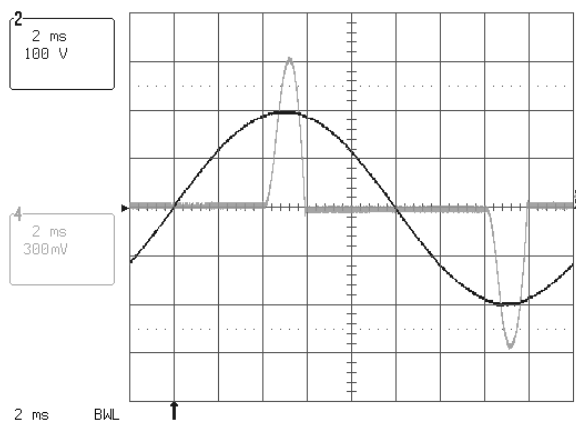
Figure 5.31 Non-linear current – sine, u_{out}: channel 2, i_{out}: channel 4 – 1A/div.
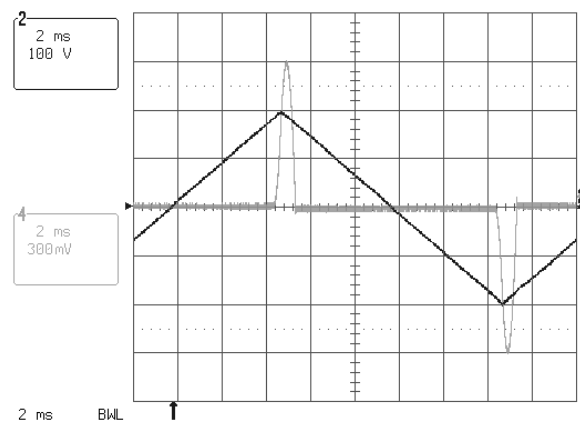
Figure 5.32 Non-linear current – triangle, u_{out}: channel 2, i_{out}: channel 4 – 1A/div.

In both cases, a peak current of 3A is adjusted. These figures show, that the circuit is also able to handle non-linear loads without negative influence to the output voltage.

Figure 5.33 shows a picture of the realised amplifier. The left side contains the DC link capacitors and the SiC MOSFETs with the standing driver PCB. A sheet copper covers the controller PCB. It acts as an electromagnetic shield against the high $\frac{\mathrm{d}B}{\mathrm{d}t}$ from the air gap of the coil. At the right side the capacitors and the second inductor are situated.
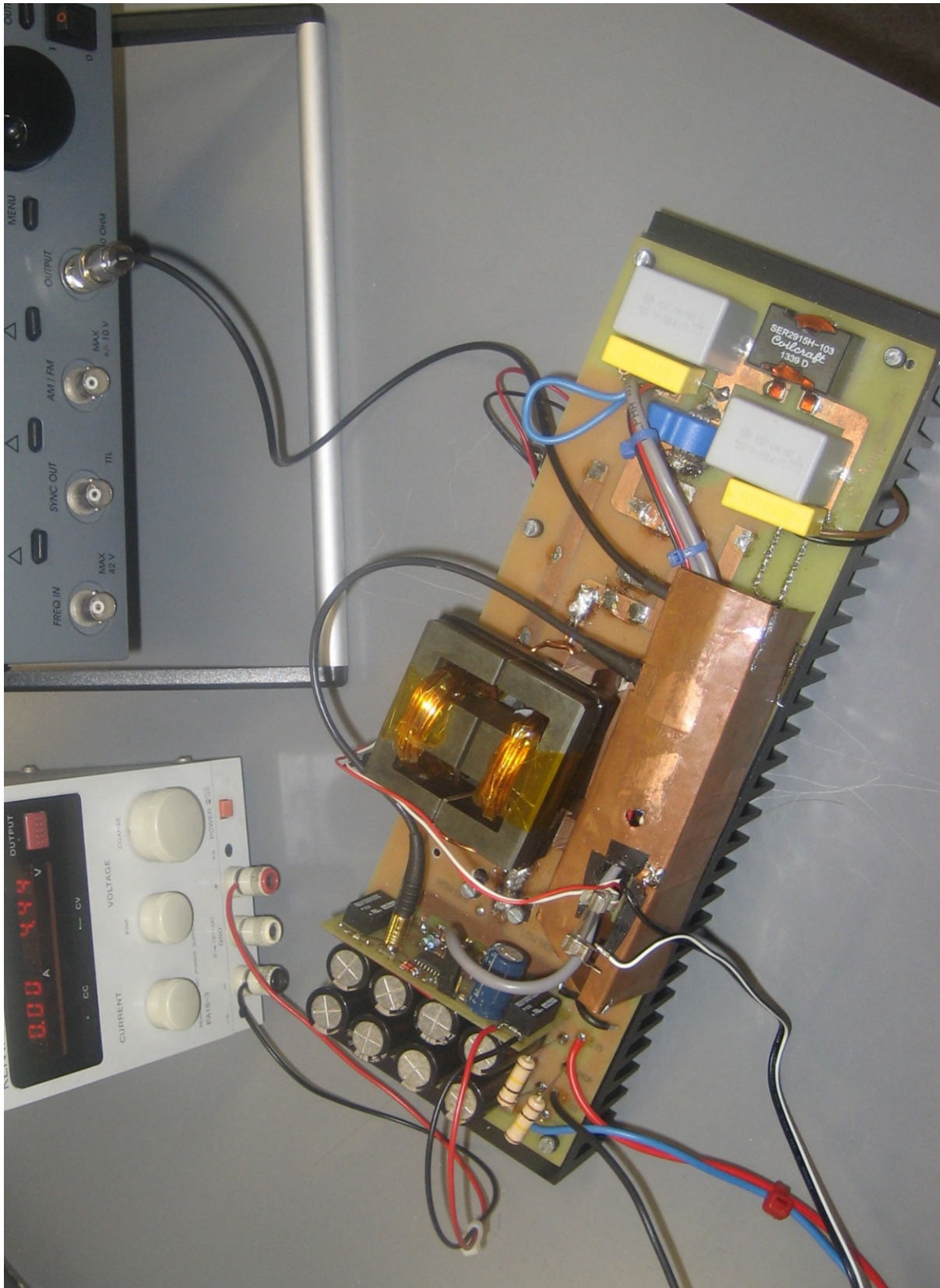
Figure 5.33 Photo of the implemented power amplifier.

6 Outlook and Perspectives

Three main problems occurred in the testing phase of the realised power amplifier. In the list below, the problems and the reasons for them are summarized.

o	High losses in the inductor L_1	A high dB/dt-rate outside the air gap causes air gap stray flux losses in the near winding, due to eddie currents
o	Bad step response curve shape	The controller created transfer function depends on the design-determining DC supply voltage.
o	Unable to drive DC loads	Charging of the DC link capacitors trips the over voltage protection of the DC power supplies

To decrease the losses in the coil, it is possible to increase the switching frequency. This leads, under the condition of the same component values, to a reduced amplitude of the ripple current. In Figure 6.1 the designed 100µH inductor is simulated with $f_s = 200$kHz. The current densities are decreased, shown by the missing dark areas in the winding[1]. The total losses of the inductor are only 2.5W, a small value compared to the realised 7.5W and the first 40W. This is an overall decrease of $\approx 94\%$.
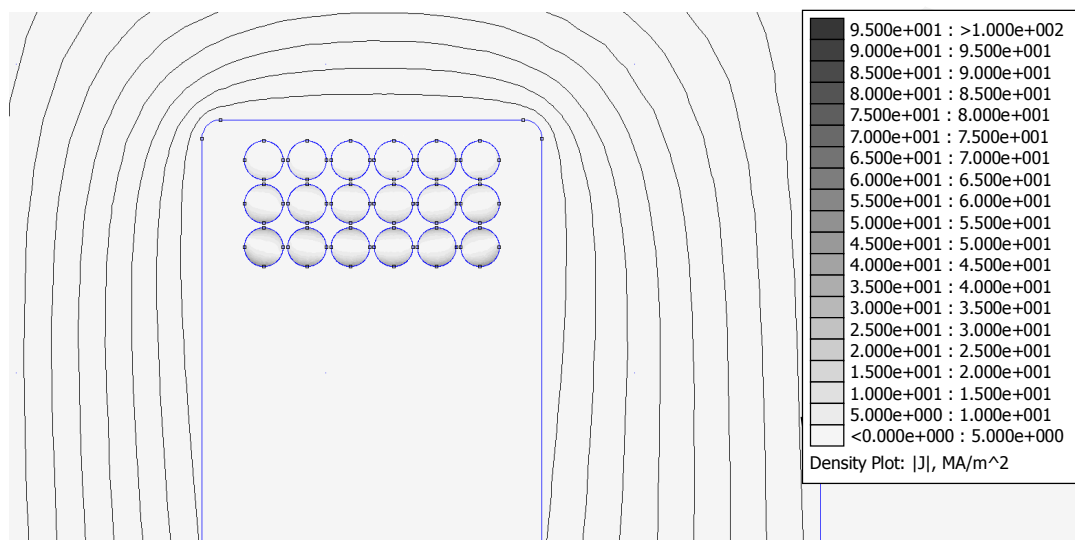
Figure 6.1 100µH inductor with 2x18 turns at $f_s = 200kHz$ – current density plot.

On the other hand, the switching losses of the MOSFETs increase significantly. According to the switching loss diagram in the datasheet [14] the losses assume to 90W at 200kHz. In case of 100kHz – 45W losses – the heat sink temperature raised to 45°C. If the room temperature is subtracted the temperature rise is 20 to 25°C. In the datasheet of the heat sink is given a coefficient of 0.42°C/W. Therefore, 45W losses provoke a temperature rise of 20°C, what is confirmed by the measurement. That means, an increased switching frequency therefore would lead to more overall losses. The question is, if it is valuable if the inductor losses are decreased. The second mentioned drawback in the list concerns the problem with the non-perfect curve shape of the step response in case of ±300V supply voltage instead of the controller parameter determining ±400V supply voltage. The differing supply voltage leads to a differing DC gain in

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[1] All current density plots are plotted with the same legend.

the transfer function, what causes a non-Bessel like step response. It is important to fix the DC gain to a constant value – in this case $K = 200$ – by a supply voltage depended amplitude of the triangle wave from the triangular waveform generator. This would not violate the $\frac{P_1}{L_1} < 1000s^{-1}$ criterion, because the maximum voltage at the inductor $U_{L_1,max}$ is also decreased due to a smaller supply voltage, see Equation (3.8).

$$\frac{P_1}{L_1} < \frac{U_{triangle,p-p} \cdot 2f_s}{U_{L_1,max}} \tag{3.8}$$

The last problem concerns the impossibility to drive DC loads. A method is to introduce resistors beside the balancing resistors to cause a permanent load current. This, however, is connected with additional permanent losses.

A better way is to design a new circuit topology, based on the existing one – a full-bridge amplifier consisting of two half-bridge stages, see Figure 6.2.
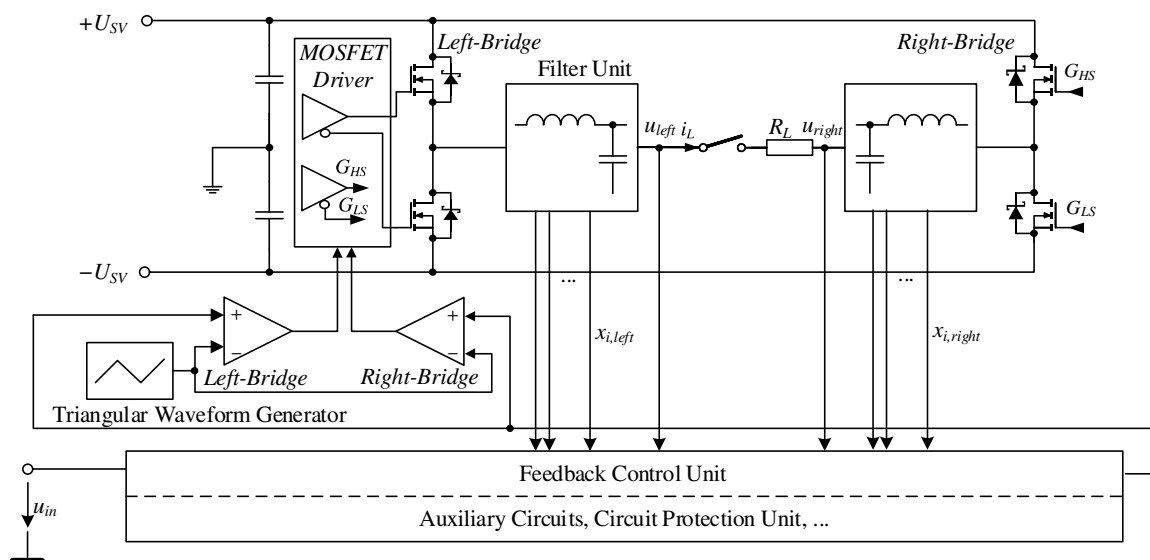
Figure 6.2 Concept for a full-bridge amplifier based on the half-bridge topology.

It is necessary to double the Filter Unit and the MOSFETs. The output voltage is defined as $u_{out} = u_{left} - u_{right}$. It is possible to benefit from a higher output voltage than for a single stage amplifier. For instance, if a DC voltage of $+250V$ is set at the left-bridge and $-250V$ at the right-bridge, the output voltage results in $+500V$ maximum load voltage.

The right-bridge MOSFETs can be switched exactly invers to the left-bridge MOSFETs. The concept bases on the controlled left-bridge, but has an uncontrolled right-bridge. Therefore, the values of the capacitors and inductors of the two bridges must coincide. Otherwise, the step response of the right-bridge differs from the step response of the left-bridge.

The full-bridge combined with the supply voltage depended triangle amplitude would result in a powerful device. Figure 6.3 shows the simulation results[1] of the step response with $\pm300V$ power supply. The bold-black curve represents the output voltage, the plain-grey the supply voltages, the dotted-black curve u_{left} and the dotted-grey u_{right}. The step responses have the designed Bessel-like curve shape, at each supply voltage. A disadvantage of the full-bridge amplifier is the doubled voltage drop because of the two filter units and the doubled switching losses because of

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[1] All full-bridge simulations are executed with GeckoCIRCUITS.

the additional MOSFETs – expected 90W switching losses cause a temperature rise of 40°C in the heat sink.
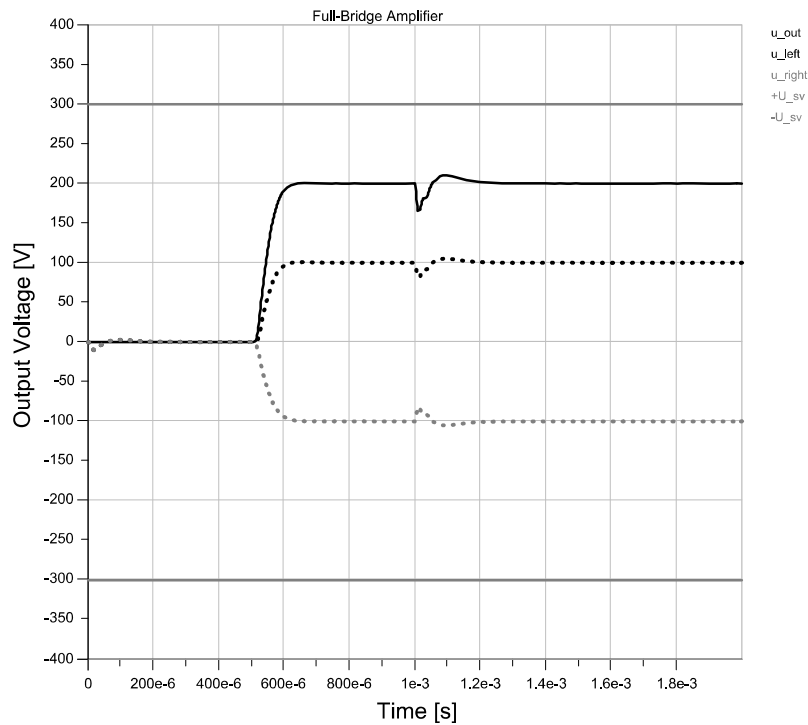
Figure 6.3 Suggested full-bridge amplifier: ±300V supply voltage.

If only the left-bridge is controlled and the right-bridge is switched invers, there occur problems in case of differing filter parameters. Figure 6.4 shows the simulation results for a 10μH higher inductance L_1 and a 300nF smaller capacitance C_1 in the right-bridge. This causes weakly damped oscillations. Therefore, the right-bridge must be controlled separately.
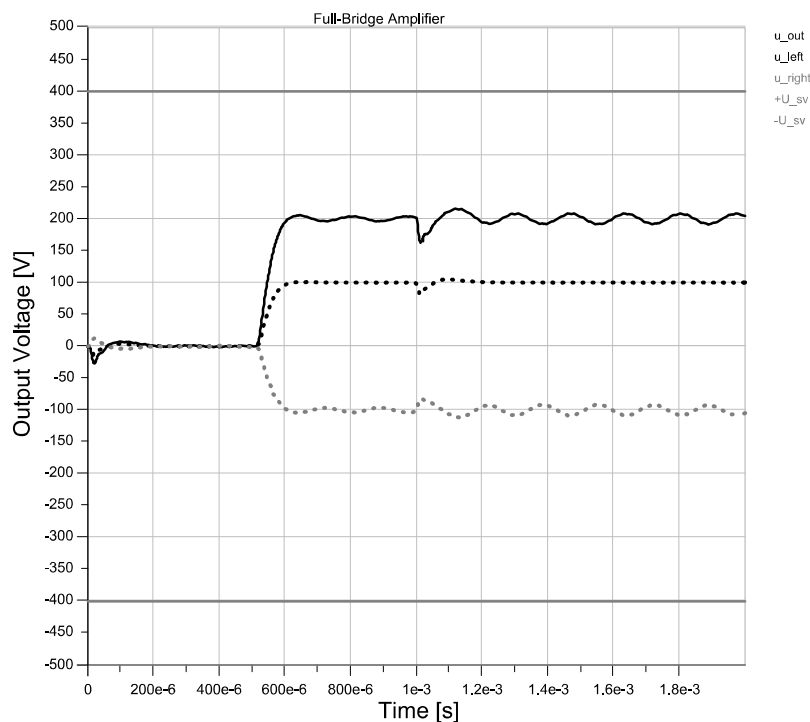
Figure 6.4 Suggested full-bridge amplifier: uncontrolled right-bridge, differing filter parameters.

In the testing phase, it was not possible to generate a 230V (= 325Vpk) sine wave because the upper limit there was one supply voltage ($300V_{DC}$). In the full-bridge case, however, this is possible. Figure 6.5 a 230V sine wave consisting of two 115V sine waves.
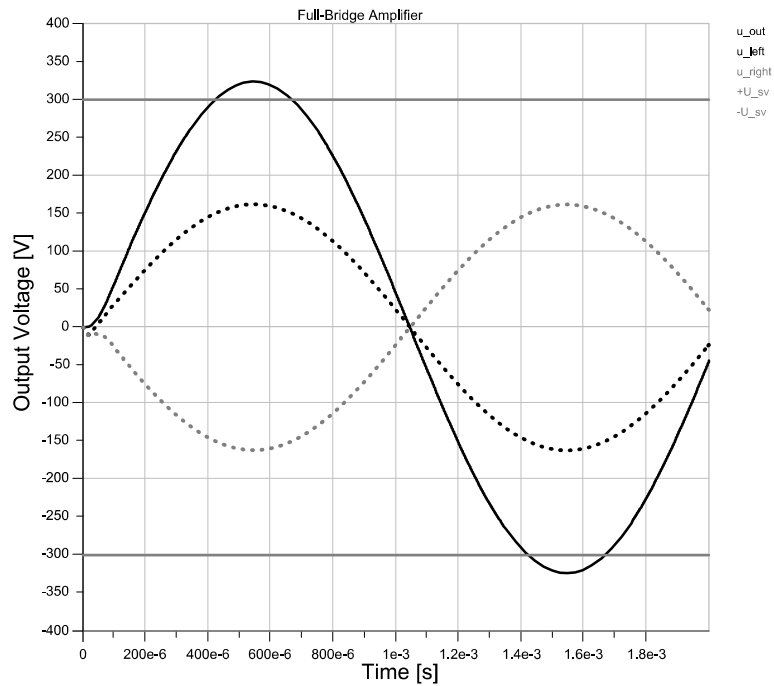
Figure 6.5 Suggested full-bridge amplifier: 230V sine wave with ±300V supply voltage.

Figure 6.6 shows the situation for asymmetric supply voltages. This does not demonstrate a problem because the controller reacts and sets the output voltage to the desired value – noticeable by the short-time positive u_{right}. It is, however, highly recommended to introduce a supply voltage depended offset to the triangle wave – beside the depended amplitude – to avoid this problem.
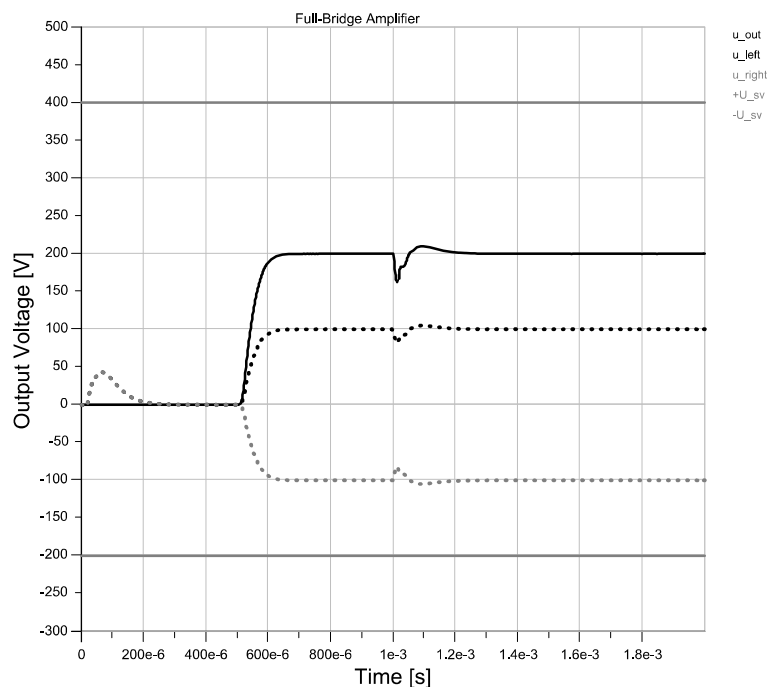
Figure 6.6 Suggested full-bridge amplifier: asymmetric supply voltages.

The amplitude of the switching harmonic of the full-bridge output voltage is significantly lower than for each half-bridge output voltage. Figure 6.7 shows that ripple-reduction effect at switching frequency $f_s = 70$kHz.
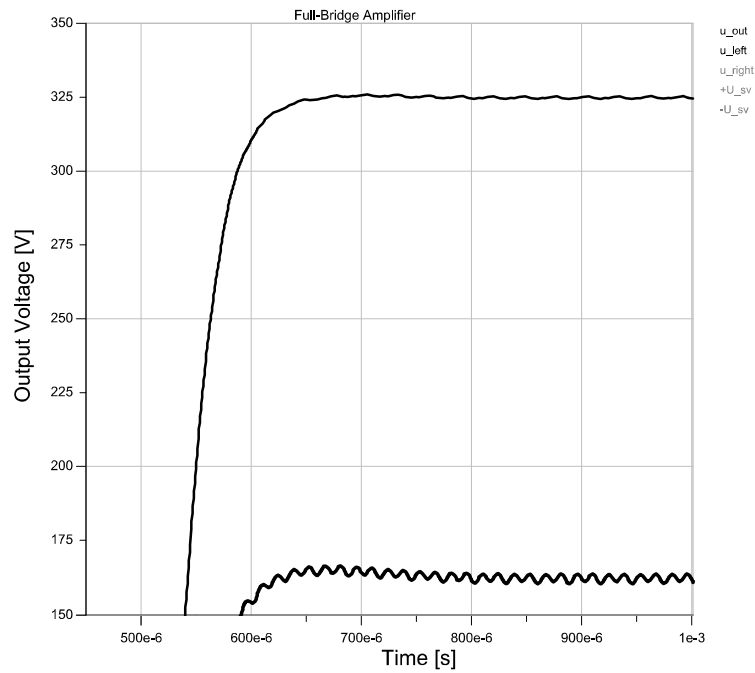
Figure 6.7 Suggested full-bridge amplifier: Superposition of u_{left} and u_{right}, $f_s = 70$kHz.

Therefore, it is possible to reach the specified attenuation also at a lower switching frequency, what concludes in lower switching losses of the MOSFETs.

Thus, the doubled voltage drop rests as only disadvantage. It is strongly recommended to analyse this topology more in detail and to realise – based on this work – the full-bridge amplifier.

7 Conclusion

This work presents the overall process of developing and implementation a silicon carbide power amplifier based on a Class-D amplifier topology.

The specified output voltage range in combination with a high switching frequency requires the utilization of a new semiconductor technology – silicon-carbide semiconductors. The analysis of material specific parameters has shown that silicon-carbide technology provides much lower losses and hence reduced device sizes compared with currently available silicon components. Thus, a realisation of the power amplifier using silicon-carbide power MOSFETs is indicated. The most important differences between the silicon-carbide technology and the state of the art silicon technology are analysed in detail and the advantages of silicon-carbide devices are pointed out.

The high output power range demands a loss-less output filter following the silicon-carbide half-bridge stage what means no resistors or active parts are allowed in the output filter. The proposed LC filter topology, however, basically represents a marginally stable system. Therefore, different feedback control structures are developed to stabilize the system and to achieve transfer functions that results in a high dynamic linear amplifier. The basic idea of various feedback control approaches is described in detail. Each approach results in a possible controller realisation, optimized to have short rise and settling time, no remarkable overshoot, low voltage drop in case of a load step, high attenuation of the switching harmonics and a non-critical current peak in case of a square wave to avoid damages on the semiconductor switches. The proposed configurations are analysed using the National Instruments Multisim 13.0 circuit simulator to analyse the impact of the switching system compared to the theoretic model. The configuration showing the best characteristics – the approximated 2nd order Bessel filter approach – finally is selected for device realisation.

The selection process for the filter related parts is presented. The non-availability of an appropriate 100µH power inductor leads to an inductor self-design, optimized to have low losses in the core and in the winding even in case of the 100kHz 10A peak ripple current. Simulations in FEMM 4.1 show that the major part of the losses in the copper is created due to the high fringe fields near the air gap. Therefore, the winding is split into two parts that are placed as far as possible from the air gap. This arrangement reduces the losses by 80% despite a smaller cross-section of the wire. Nevertheless, this topic requires more attention to improve the losses again.

All circuits and sub-circuits are described in detail. A new MOSFET driver circuit is developed with isolated output drivers – based on a RF transmitter and receiver IC concept instead of using optocouplers – that is able to drive the silicon-carbide MOSFET gates as proposed from the manufacturer. Tests on the realised half-bridge show nearly ideal switching behaviour – no remarkable switching surges as well as low rise and fall times of about 40ns.

The overall circuit is tested extensively. The results of the real system correspond to the theoretic/simulated ones. A drawback represents the non-availability of DC power supplies that are able to provide the design-determining supply voltage (400V). Therefore, it is not possible to show the full potential of the power amplifier. Appearing problems in the test procedures are mentioned, especially the missing possibility of the circuit to adapt to different supply voltages

and the fact that the used topology is unable to drive DC loads. To eliminate these disadvantages, an extended circuit topology is proposed: the full-bridge converter. Is consists of two identic half-bridge stages, either only one or both stages can be controlled. The first solution needs less effort but shows a worse step response – weakly damped oscillations – of the uncontrolled stage in case of differing filter parameters compared to the controlled stage. The second solution – two independently controlled half-bridge stages – nearly would eliminate nearly all drawbacks and provides additional benefits such as a twice as high output voltage range as the supply voltage range. Therefore, it is highly recommended to pursue further researches on this topic.

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List of Figures

List of Tables

List of Acronyms and Abbreviations

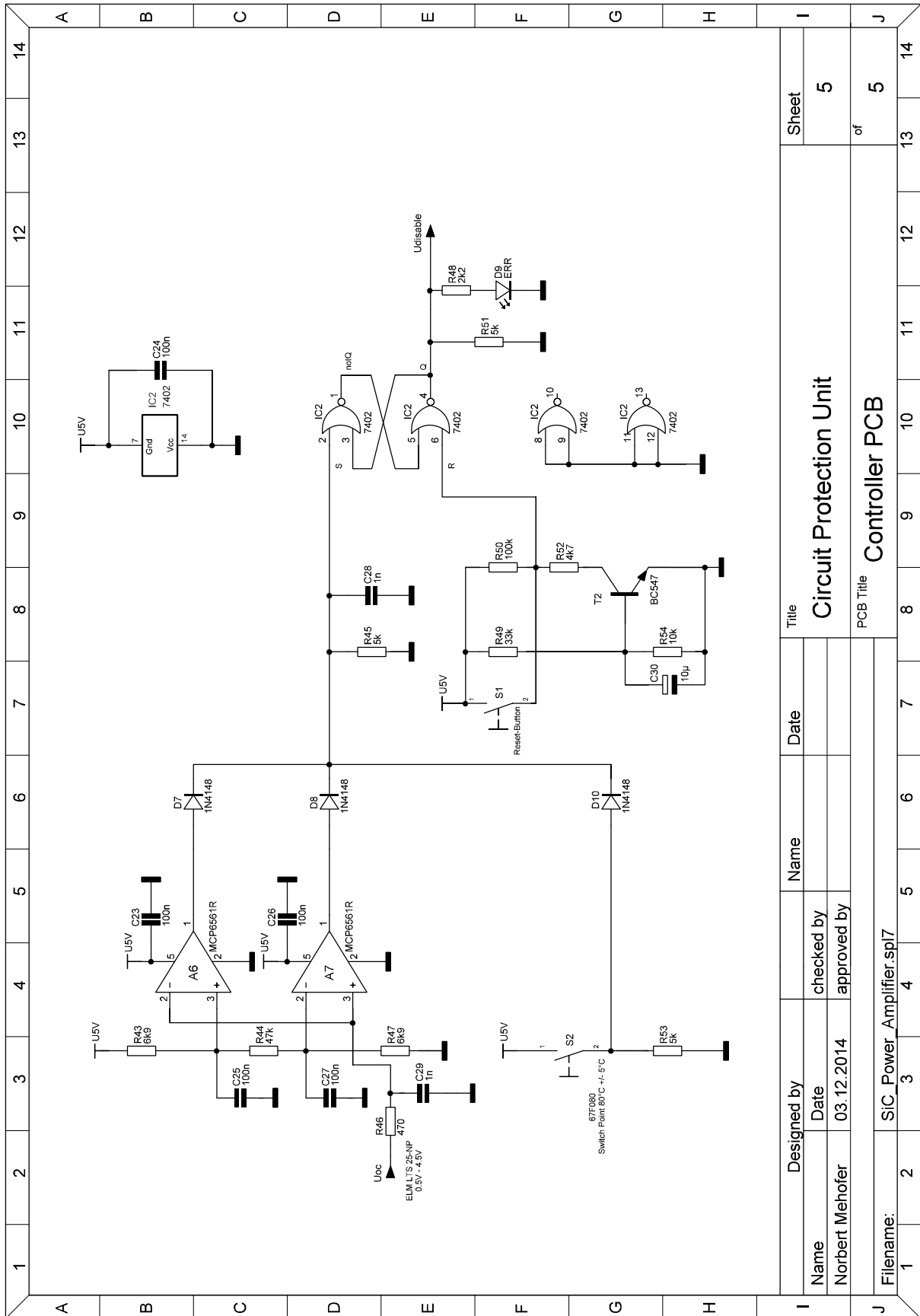|	
SiC	Silicon Carbide
Si	Silicon
PCB	Printed Circuit Board
SBD	Schottky Barrier Diode
HS	High Side
LS	Low Side
IC	Integrated Circuit
UVLO	Undervoltage Lockout Protection
DT	Dead Time
RDT	Dead Time Programmable Resistor
OPA	Operational Amplifier
DCR	Direct Current Resistance
FEMM	Finite Element Method Magnetics
SER	Series Equivalent Resistance

Collection of Circuit Diagrams
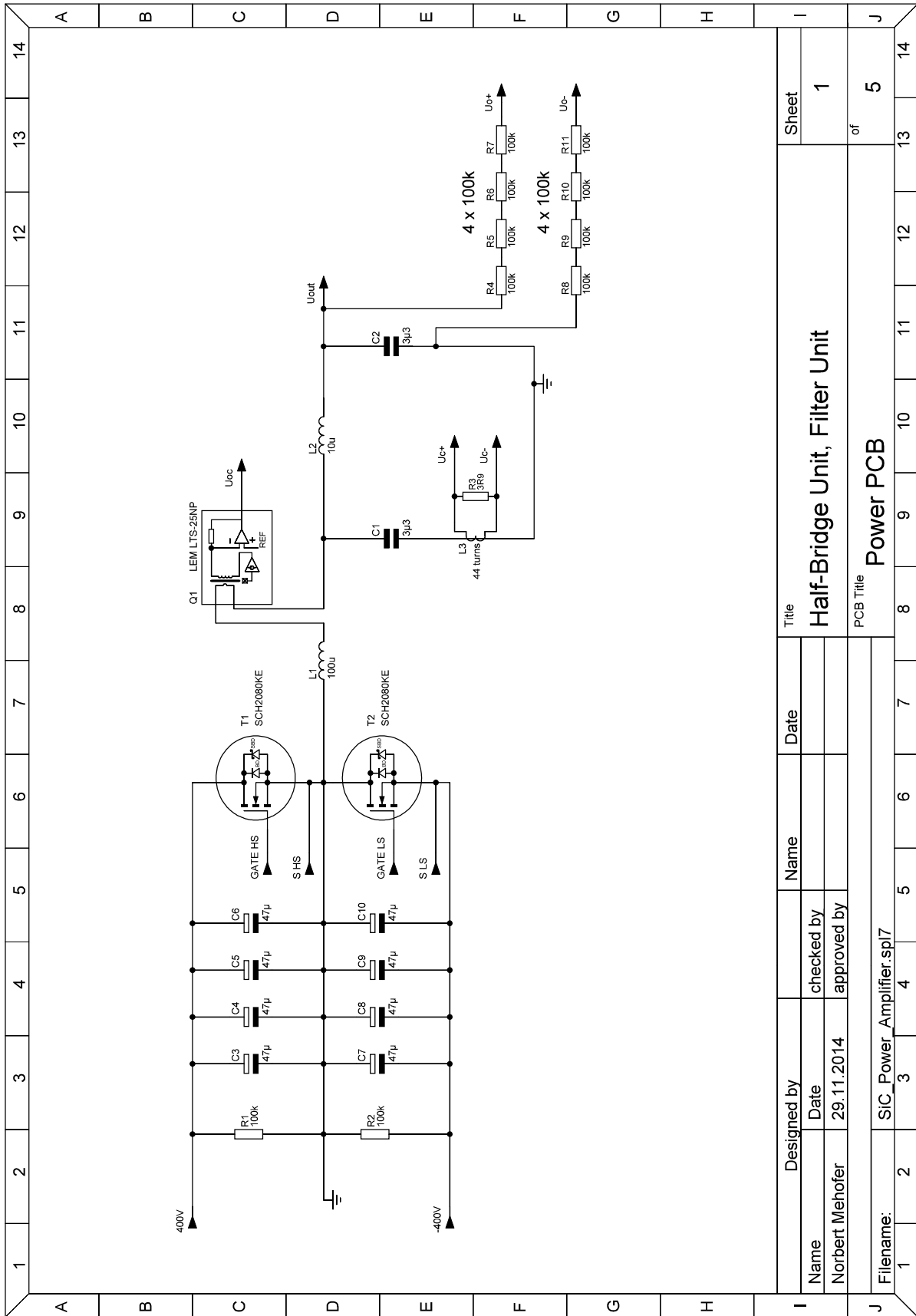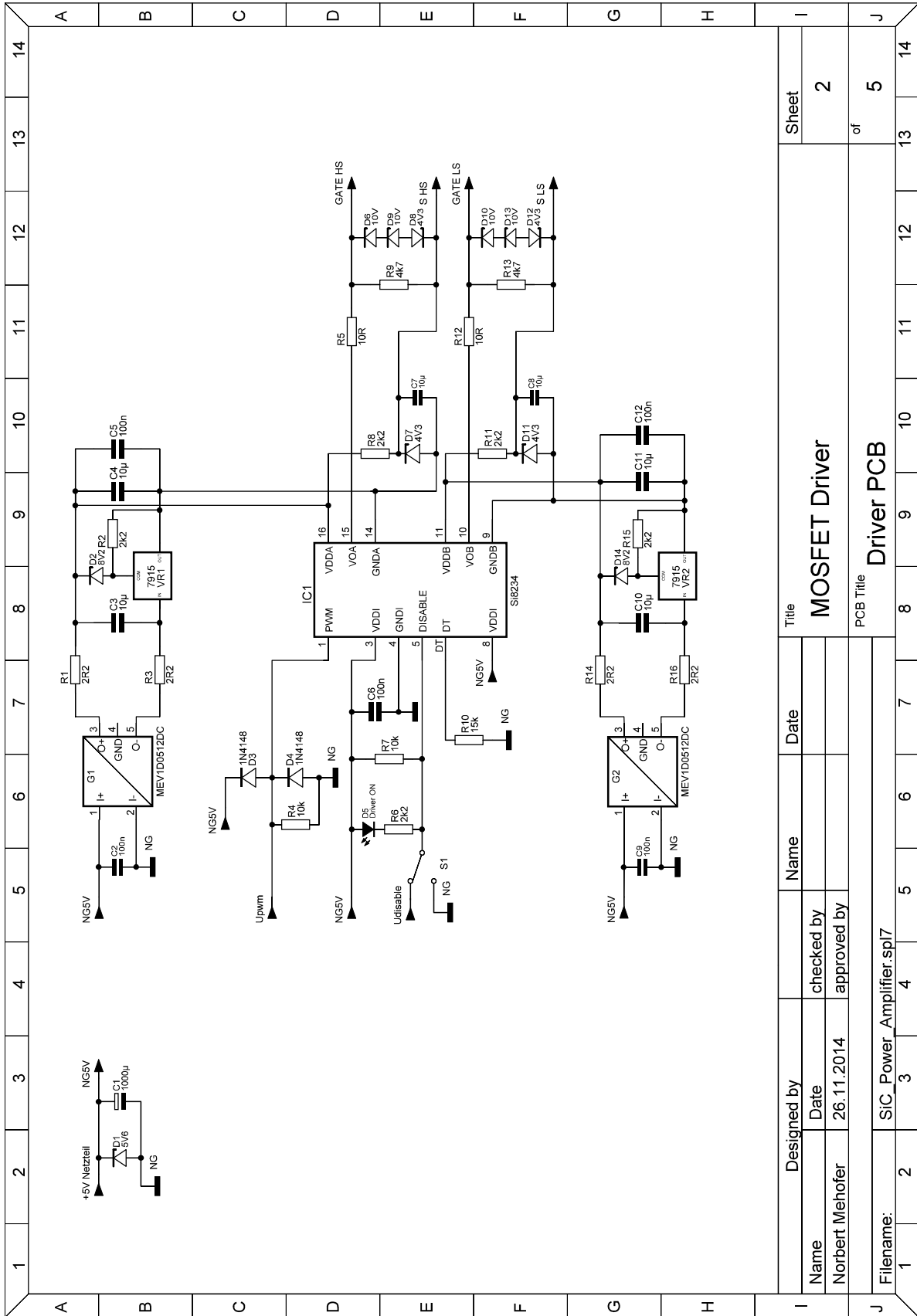
MOSFET Driver

Driver PCB

Aux. Voltage Supply, Triangular Wave Gen.

Controller PCB

| Sheet | 3 |
| of | 5 |

Title

PCB Title

Designed by			Name	Date
Name	Date	checked by		
Norbert Mehofer	26.11.2014	approved by		

Filename: SiC_Power_Amplifier.spl7

Controller Circuit

Controller PCB

Sheet 4 of 5

Designed by

Name | Date
Norbert Mehofer | 26.11.2014

Filename: SiC_Power_Amplifier.spl7

Circuit Protection Unit

Controller PCB

Sheet 5 of 5

Title

PCB Title

Designed by

Name | Date
Norbert Mehofer | 03.12.2014

Name | Date
checked by
approved by

Filename: SiC_Power_Amplifier.spl7