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Synthese und Charakterisierung von Halbleiter-Metall-Halbleiter Nanodraht Heterostrukturen

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unter Anleitung von
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Master's Thesis

Synthesis and Characterization of Semiconductor-Metal-Semiconductor Nanowire Heterostructures

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Abstract

A novel synthesis approach for semiconductor-metal-nanowire (NW) heterostructures is presented and discussed in this thesis. The synthesis employs millisecond flash lamp annealing (FLA) along with several standard techniques of semiconductor manufacturing like sputtering and plasma enhanced chemical vapor deposition (PE-CVD). In the first step the NWs were covered with a thin metal layer using sputter deposition. Then a SiO_2-shell was applied to the NWs using a PE-CVD process. After this the FLA-process was applied with the goal of selectively melting the core material enclosed in the SiO_2-shell, but leaving the shell itself intact. With the proper parameters this resulted in intermixing and finally after resolidification in the synthesis of semiconductor-metal-NW heterostructures. The NWs appeared to be crystalline and were observed to be epitaxial to a large extent in relationship between the metal and semiconductor parts.

It was possible to apply the synthesis method to multiple material systems. The most thoroughly-characterised structures were silicon NWs with gold segments (Si-Au heterostructures) and gallium arsenide NWs with gold segments (GaAs-Au heterostructures). Other material systems like silicon - nickel silicide (Si-NiSi) and silicon-tin (Si-Sn) were also synthesized using the same method. What's special about these structures are the interfaces between the semiconductor and metal parts. It was shown for them to be abrupt in Si-Au, GaAs-Au and Si-NiSi structures. The composition of the synthesized structures was determined using energy dispersive X-Ray spectroscopy (EDX) and electron energy loss spectroscopy (EELS). The phononic properties of the GaAs-Au and Si-Au material systems were investigated using µ-Raman spectroscopy.

The electrical measurements proved troublesome due to high leakage currents and other effects that led to the rejection of most measured data. All electrically measured structures (Si-Au, Si-NiSi and GaAs-Au) displayed only very small to no gating characteristics (factor of 100 max vs. 10^4 for typical Si NWs). The measured mean resistivity of Si-NWs (which were prepared like Si-Au NW heterostructures but didn't display segments) was measured at 5,4 Ωm (σ = 2,6 Ωm). Si-Au NW heterostructures with one segment were measured at 3,1 Ωm (σ = 3,8 Ωm). Si-NiSi NW heterostructures with one segment displayed a mean resistivity of 34,8 Ωm (σ = 47 Ωm). GaAs-NWs (once again prepared the same way as GaAs-Au NW heterostructures) were measured at 570 Ωm (σ = 580 Ωm). GaAs-Au NW heterostructures with one segment displayed a mean resistivity of 2600 Ωm (σ = 3700 Ωm). The single remaining 2-segment GaAs-Au NW structure was measured at 900 Ωm. No definitive statements can be made from these data points.

During the Raman-measurement, Si-Au heterostructures displayed the expected main peak for crystalline Si at 520 cm^{-1}. This peak is the first order longitudinal

optical (LO) mode of Si. Si-Au NW heterostructures displayed a slightly red-shifted LO peak in relation to the other measured structures. As-grown Si-NW displayed a slightly larger full width half maximum and its LO peak falls between the peak of the Si-Au NW heterostructures and the other measured structures.

The most prominent feature of GaAs-Au are its two peaks at 268.5 cm^{-1} (transversal optical, TO) and 289 cm^{-1} (longitudinal optical, LO). The proportion between these peaks changes significantly across different structures, with the proportionally smallest TO peak at a GaAs-Au NW with segments. The TO peak is generated when back-scattering occurs from the (110) surface, the LO peak from backscattering off the (100) surface. Since both peaks would be generated from backscattering off the (111) surface as well, this process is obviously suppressed. In bulk GaAs the LO peak is dominant, in all other measured structures the TO peak is dominant. This indicates that backscattering occurs mostly from (110) surfaces in these structures. (cf. [1])

The Au feature was present in GaAs-Au as well as Si-Au whether segments were present or not, once again with some dynamics of the plateau height when scanning on top of segments or not.

Kurzfassung

Diese Arbeit stellt eine neuartige Synthese-Methode für Halbleiter - Metall - Halbleiter Nanodraht (NW) Heterostrukturen vor und diskutiert diese. Die Methode verwendet Millisekunden flash lamp annealing (FLA) und einige Standard-Verfahren der Halbleiter-Industrie wie Sputtern und plasma-unterstützte chemische Gasphasenabscheidung (PE-CVD). Zuerst wurden die Nanodrähte mittels Sputter Beschichtung mit einer dünnen Schicht Metall überzogen. Anschließend wurde eine Ummantellung aus SiO_2 mit einem PE-CVD Prozess aufgebracht. Darauf folgte der FLA-Prozess mit dem Ziel den Materialkern innerhalb der Ummantelung selektiv zu schmelzen, ohne jedoch den Mantel selbst zu zerstören. Diese Prozessierung erzeugte mit bestimmten Parametern nach der Durchmischung beim Erstarren Halbleiter - Metall Nanodraht Heterostrukturen. Das Metall und der Halbleiter hatten dabei zueinander eine definierte kristalline Ausrichtung.

Es war möglich die Synthesemethode an verschiedenen Materialsystem erfolgreich anzuwenden. Am genauesten wurden Silizium Nanodrähte mit Gold Segmenten (Si-Au NW Heterostrukturen) und Gallium-Arsenid-Nanodrähte mit Gold Segmenten (GaAs-Au NW Heterostrukturen) untersucht. Weitere Kombinationen von Materialien bei denen die Synthese erfolgreich war sind Silizium mit Nickel-Silizid (Si-NiSi) und Silizium mit Zinn (Si-Sn). Das besondere an diesen Strukturen war das Interface zwischen dem Halbleiter- und dem Metallteil der Struktur. Die Interfaces bei Si-Au, GaAs-Au und Si-NiSi sind atomar scharf. Die Zusammensetzung der Strukturen wurde mittels energiedispersiver Röntgenspektroskopie (EDX) sowie Elektronen Energieverlust Spektroskopie (EELS) untersucht. Für GaAs-Au und Si-Au wurden auch die phonischen Eigenschaften mittels µ-Raman-Spektroskopie untersucht.

Bei den elektrischen Messungen konnten aufgrund der hohen Leckströme der Großteil der Messdaten nicht verwendet werden. Die in FETs integrierten Heterostrukturen konnten elektrostatisch nur maximal um den Faktor 100 gesteuert werden. Für Si-NW ohne Segment (aber mit gleicher Prozessierung wie Si-Au NW Heterostrukturen) wurde ein durchschnittlicher spezifischer Widerstand von 5,4 Ωm (σ = 2,6 Ωm) gemessen. Für Si-Au NW Heterostrukturen mit einem Segment wurde ein Wert von 3,1 Ωm (σ = 3,8 Ωm) gemessen. Für Si-NiSi Heterostrukturen mit einem Segment wurden 34,8 Ωm (σ = 47 Ωm) gemessen. GaAs-NWs ohne Segment (aber wiederum mit gleicher Prozessierung wie GaAs-Au NW Heterostrukturen) lagen bei 570 Ωm (σ = 580 Ωm). GaAs-Au NW Heterostrukturen mit einem Segment zeigten einen spezifischen Widerstand von 2600 Ωm (σ = 3700 Ωm). Die einzig sinnvolle 2-Segment Struktur von GaAs-Au NWs, die verblieb, lag bei 900 Ωm. Es können basierend einzig auf diesen Werten keine definitiven Aussagen zu den elektrischen Eigenschaften dieser Strukturen getroffen werden.

Bei den Raman-Spektroskopie Messungen zeigten Si-Au Heterostrukturen wie erwartet einen Hauptpeak bei 520 cm^{-1}. Dieser Peak deutet auf kristallines Si hin und ist der longitudinal optische (LO) peak erster Ordnung. Er war bei Si-Au NW Heterostrukturen etwas zu kleineren Wellenzahlen verschoben (Rotverschiebung). Wie-gewachsene Si-NW zeigten eine etwas größere Halbwertsbreite und der Hauptpeak liegt zwischen dem von Si-Au NW Heterostrukturen und den anderen vermessenen Strukturen.

Das auffälligste Merkmal von GaAs-Au NW Heterostrukturen waren die zwei Peaks bei 268.5 cm^{-1} (transversal optisch, TO) und 289 cm^{-1} (longitudinal optisch, LO). Die Proportionen dieser beiden Peaks verändern sich signifikant von Struktur zu Struktur. Der proportional kleinste TO Peak tritt bei einer GaAs-Au Struktur mit Segmenten auf. Der TO peak tritt auf wenn von (110) Oberflächen gestreut wird, der LO peak bei Streuung von (100) Oberflächen. Bei Streuung von (111) Oberflächen wären beide Peaks stärker ausgeprägt, dieser Prozess ist offenbar unterdrückt. (cf. [1])

Die Flanke und das zugehörige Plateau, das auf Au hindeutet, tritt jeweils bei Si-Au und GaAs-Au auf, egal ob Segmente vorhanden sind oder nicht. Wiederum gibt es eine interessante Dynamik der Plateau-Höhe zu beobachten wenn man über Segmente scannt, verglichen mit Daten ohne Segmente.

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Several measurements that are presented in this thesis were conducted externally. Therefore I would like to acknowledge Michael Stöger-Pollach (TU Wien @USTEM) and Luong Minh-Anh (NEEL Institute, Grenoble) for the incredible TEM measurements of my structures, and to Carsten Ronning from the Institute of Solid State Physics in Jena who provided the tin implanted NWs. This thesis and the pending publication would not be possible without them.

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Contents

Abbreviations

Au	gold
BHF	buffered hydrofloric acid
EDX	energy-dispersive X-ray spectroscopy
FWHM	full width half maximum
FLA	flash lamp annealing
GaAs	gallium-arsenide
GaAs-Au	gallium-arsenide NW with gold segments
HR-TEM	high-resolution transmission electron microscopy
LSPR	localised surface plasmon resonance
MFM	magnetic force microscopy
Ni	nickel
NW	nanowire
RTA	rapid thermal annealing
SEM	scanning electron microscopy
Si	silicon
Si-Au	silicon NW with gold segments
Si-NiSi	silicon NW with nickel-silicide segments
Si-SnAu	silicon NW with tin-gold segments
Sn	tin
TEM	transmission electron microscopy
VLS	vapor liquid solid

Introduction

During the last decades, electronic devices have undergone an enormous scaling process. Starting from room-sized computers and brick-heavy mobile phones in the 1970s and 80s, electronic devices became the foundation of our modern society, becoming ever more ubiquitous. This transformation was largely possible due to the ongoing miniaturization of basic circuit components enabling ultra large scaling integration. This trend towards ever smaller and more efficient electronic systems requires a huge effort both in research and development.

Research into all kinds of new devices, concepts and materials is under way to allow for new and improved devices. Since device dimensions are already nanoscaled in contemporary integrated circuits, new approaches are needed to understand and possibly utilize new functionalities at these dimensions. One of these topics of interest is the fabrication of nanoscaled heterostructures - the topic of the thesis at hand. (cf. [2–4])

NWs represent the principal case for the synthesis of heterostructures due to the so-called strain release mechanism. When two materials are sought to be integrated into a single device, their crystal structure can prevent growing epitaxial layers of these materials on top of each other due to mismatching lattice constants. This prohibits the use of *standard planar epitaxy* methods for the synthesis of such structures. In NWs, however, the mismatches in lattice constants and the resulting strain can be alleviated via the NW surface and therefore enable material combinations which cannot be realized in layers, thereby incorporating these materials' properties into a single device. The mechanisms underlying the strain release process are currently under investigation. However, to the best of our knowledge, combining a semiconductor and metal into such a structure has not been achieved yet. (cf. [5])

The synthesis of the structures presented here was first noticed as a byproduct of experiments synthesizing III-V Si-NW heterostructures by Markus Glaser [6]. During experimentation with a novel annealing method called Flash Lamp Annealing (FLA), molten materials undergo separation when annealed this way during resolidification, resulting in NW heterostructures.

In this thesis we expand this process for the systematic use of the observed separation in the synthesis of semiconductor-metal NW heterostructures. Various semiconductor-metal material combinations were tested, however, with the focus on the prevalent semiconductors in the industry: silicon and GaAs.

Possible applications for such a structure lie for example in the field of plasmonics due to the high carrier density of Au, which supports localised surface plasmon resonance (LSPR). Other possible applications are the photocatalytic conversion of light energy or use of the structures in novel thermoelectric devices with a high thermoelectric figure of merit. (cf. [7–11])

The goals of this thesis were:

- Synthesis of crystalline metal-semiconductor heterostructures in Si and GaAs NW
- Elemental and structural analysis of the synthesized structures

This thesis is structured as follows: Chapter 1 will cover the theoretical background and necessary prerequisites in semiconductor physics, solid state physics and heterostructure formation. Next, in chapter 2, experimental techniques used for the synthesis and characterization of these structures are explained. In the penultimate chapter 3 the results of various experiments and measurements are thoroughly analyzed. The discussion follows in chapter 4 along with the conclusion and an outlook on applications and further research.

Chapter 1

Theory

1.1 Basic Properties of Semiconductors

In the following chapter the basic physics of semiconductors is presented. Considering the vast scale of this topic, only a small portion directly relevant to the topic at hand will be discussed. For a more thorough treatment I refer to the extensive literature available. (cf. [2, 3, 12, 13]).

1.1.1 General Properties of Semiconductors

Semiconductors, as the name suggests, fall 'between' conventional conductors and insulators. The defining property of a semicondutor is its resistivity. Typical values lie between the very low values of conductors (typically $10^{-5}\,\Omega$m) and the very high values of insulators ($\geq 10^{6}\,\Omega$m). In a metal the electrons can move freely. This results in a lower resistance at smaller temperatures. A semiconductor displays infinite resistance at T=0 K and decreasing resistance at higher temperatures due to the band structure (see 1.1.4). The resistivity of semiconductors depends on temperature, with higher conductance at high temperatures and vice versa. Another important property of semiconductors is the possibility of adjusting the resistivity by doping (see section 1.1.5). (cf. [12])

Several parameters of electronic devices are directly related to semiconductor resistivity. Examples include but are not limited to device series resistance, capacitance, threshold voltage, hot carrier degradation of MOS devices and latch-up of CMOS circuits.

With the free electron and hole densities n and p and their respective mobilities μ_n and μ_p, the resistivity can be calculated according to:

$$\rho = \frac{1}{q(n\mu_n + p\mu_p)} \tag{1.1}$$

Experimentally ρ can be determined through a direct or indirect measurement of the carrier densities and mobilities. By measuring the device resistance R and its dimensions, a good estimation for ρ can usually be obtained using the well-known equation 1.2 where A is the cross-sectional area and l is the device length. (cf. [2])

$$\rho = R \cdot \frac{A}{l} \tag{1.2}$$

When considering the non-ideal case, to obtain the resistance of the device on its own, perfect ohmic contact with the semiconductor structure that is being measured would be needed. For this reason it is common to realize a 4-point measurement setup, to get rid of the parasitic contact resistance (cf. [14]). Since the current through the measured structure remains unchanged in this setup, the true unbiased device resistance can be calculated using the potential difference of the inner contacts and the current flowing through the whole structure. A typical I-V and gating characteristic of a MOSFET is presented in Figure 1.

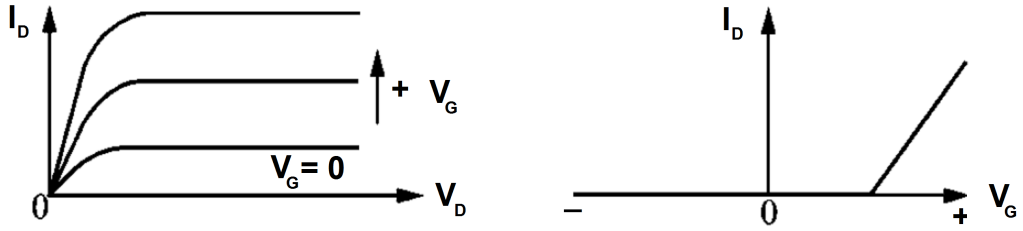


Figure 1. Current-Voltage (I-V) Output and Transfer characteristic of a n-channel MOSFET (adjusted from [3] p.297 Figure 4)

1.1.2 Semiconductors used in Industrial Applications

The arguably most important semiconductors for the industry today are Si and GaAs. This also was the reason for the experimental work in this thesis focusing on these two material systems. Due to the ongoing device miniaturization in the industry, it is expected for Ge to become important in manufacturing within the next couple of years, due to fundamental problems arising in Si at the projected scales. These problems might be contained due to Ge displaying the highest observed hole mobility and a large Bohr radius. Other semiconductors that are being used include the following: indium arsenide, GaN, silicium carbide and related compounds, zinc oxide, aluminium arsenide and many more. These display a wide variety of different properties that make them attractive for different applications like high mobilities, power values, optical properties and so on. (cf. [3, 13])

1.1.3 Crystal Structure of Semiconductors

The diamond and zincblende lattice structure is common among the most common semiconductors used in industry. The arrangement of atoms thereby follows a tetrahedral pattern, where each atom is equidistant to four surrounding atoms, each of which lies in one corner of a tetrahedron. A way to visualize this is to think of two fcc-lattices that penetrate each other. For the diamond crystal structure all atoms are of the same sort. Si and Ge crystallize into the diamond structure, illustrated in

Figure 2. In the zincblende-structure not all atoms are the same. In case of GaAs one fcc lattice is made of gallium atoms, the other fcc lattice of arsenic atoms.

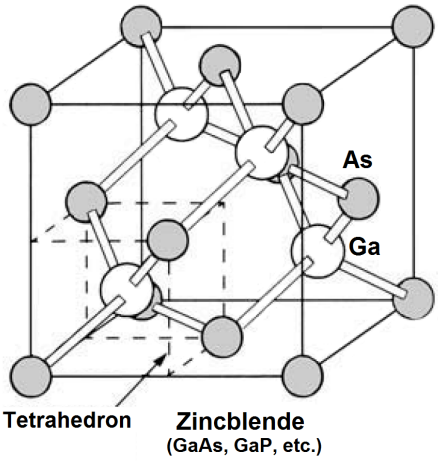


Figure 2. Schematic of the zincblende crystal structure of GaAs (adjusted from [3] Figure 1e) on p.9)

Not all semiconductors crystallize exclusively into a specific structure. An example for this is zinc sulfide, which crystallizes into either a zincblende or a wurtzite structure. The surface of the semiconductor is especially important for use in device manufacturing, since most devices are built near or on a semiconductor surface. For different orientations the mobilities may vary. For example the Si (100)-plane which displays the highest observed mobility. For this reason Miller indices are used as a convenient way to emphasize which crystal orientation is present. The indices are usually labelled with the constants (hkl) used in the description of the crystal using three vectors as a basis. An example for a Miller index would be (111) for a certain crystal plane in crystalline Si. (cf. [3, 13])

1.1.4 Band Structure of Semiconductors

The band structure of a semiconductor - the relationship between energy and the wavevector **k** of the carriers in a lattice - can account for many properties. The material's interaction with photons and phonons as well as the charge carriers' interacting among themselves relates to the concept of the energy band diagram. The effective mass and group velocity are also among the properties which are governed by these interactions. To obtain the sought-after relationship, the Schrödinger-equation needs to be solved for a periodic potential. The wavefunctions that solve this Schrödinger equation are the Bloch-functions of the form:

$$\psi(\mathbf{r}, \mathbf{k}) = exp(j\mathbf{k} \cdot \mathbf{r}) U_b(\mathbf{r}, \mathbf{k}) \tag{1.3}$$

where $\psi(\mathbf{r}, \mathbf{k})$ and $U_b(\mathbf{r}, \mathbf{k})$ are periodic in **r**, b is the band index. Periodicity of $E(\mathbf{k})$ leads to collapse of all wavevectors into one primitive cell, the Brillouin zone. (cf. [3])

The important point in the case of semiconductors is the formation of a forbidden energy range, the energy gap. No allowed states exist inside this region. Any bands above the energy level of the gap are summarised into the *conduction band*, below the gap lies the *valence band*. The bandgap is the name for the energy required to go from the highest valence-band energy to the lowest conductance band energy. It is among the most important parameters of a semiconductor. (cf. [3])

An important property that distinguishes semiconductors from each other with respect to the particular optical properties is the nature of this bandgap. If the lowest point of the conduction band falls exactly to the maximum of the valence band at $k = 0$, the semiconductor is called *direct*, if it doesn't it is called *indirect*. Figure 4 illustrates the difference. A consequence of this property is the conservation of momentum in direct semiconductors and the changed momentum in indirect semiconductors during transfer of carriers from conduction to valence band or vice versa. This has important implications for photon absorbtion and emission cross-sections of the semiconductor, thereby greatly influencing the material's optical properties. (cf. [3])

1.1.5 Doping

The carriers for current in a semiconductor are electrons (n-doped) and holes (p-doped), which basically behave like electrons with an opposite charge. An ideal intrinsic semiconductor displays infinite resistance at T=0 K. At a temperature higher than zero, the occupancy is a given by the Fermi-Dirac distribution function

$$F(E) = \frac{1}{1 + e^{\frac{(E-E_F)}{kT}}} \tag{1.4}$$

where E_F is the Fermi energy. For an intrinsic semiconductor the Fermi energy typically falls almost exactly in the middle of the bandgap. If the bandgap is large, the intrinsic carrier density will thus be small.(cf. [3])

Doping is the technical process that enables control over the resistivity of a semiconductor. Different dopands alter the resistivity in different ways, a unique property compared to metals and insulators. The mechanism that enables doping to alter the electronic properties of a semiconductor is exemplarily illustrated for Si in Figure 3.

Intrinsic Si only has a negligible amount of impurities that could potentially participate in electrical conduction, therefore resistivity is high. Doping Si with phosphorous (coordination number V), which donates one electron to the lattice, results in n-doped Si. Boron on the other hand leaves a hole when bonding with four adjacent Si-atoms thereby contributing a hole for conduction. Both doping strategies result in higher conductivity and therefore less resistivity of the semiconductor.

Through electrostatically biasing a semiconductor device (for example via a back-gate structure), the level and charge-sign of doping can be achieved. Positive bias produces more current in a p-type semiconductor and less current in an n-type semiconductor. The reverse is true for negative bias on the gate. (cf. [3])

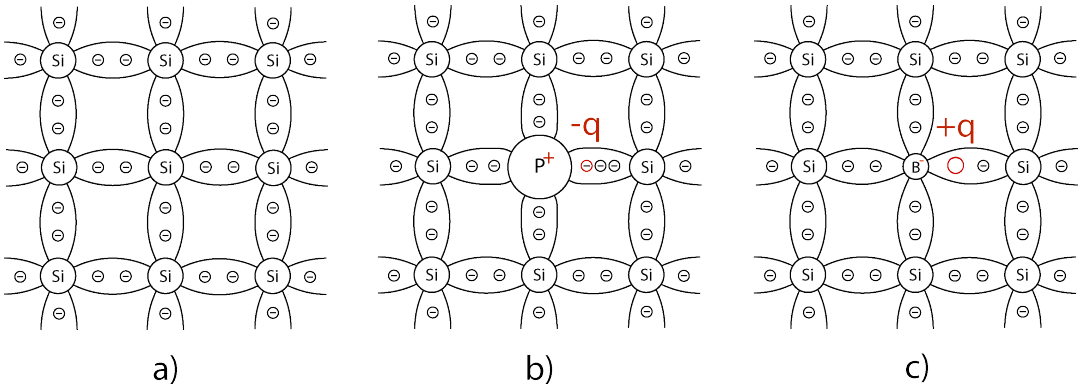


Figure 3. Illustration of the doping mechanism a) intrinsic Si, b) n-type Si with phosphorous as donor, c) p-type Si with boron as acceptor (adjusted from [3] p.16 Fig.7)

In general 3 types of semiconductors can be distinguished in relation to doping:

- nondegenerate semiconductors
- degenerate semiconductors
- intrinsic semiconductors

With *nondegenerate* semiconductors the Fermi Energy is more than several kT below the lowest allowed energy of the conduction band for n-type semiconductors. For p-type semiconductors the reverse holds as a condition for carrier concentration in the valence band, with the Fermi energy being required to be more than a few kT above the energy of the maximum of the valence band.

For *degenerate* semiconductors the Fermi energy is outside the band gap.

At *intrinsic* concentrations only thermal excitation can produce carriers in the conduction band, with an equal number of holes in the valence band. The Fermi level typically lies very close but not exactly in the middle of the energy gap due to differences in the effective mass for electrons and holes. (cf. [3])

Other impurities can also play an important role in device properties. Doping usually produces *shallow impurities*. The resulting energy states are close to the original top/bottom energy of the valence/conduction band and thus help ionization at RT. Since an atom can have many levels though, another type of impurity, a *deep impurity*, is possible. Here the energy states penetrate the energy gap deeply and alter the electronic properties by providing an in-between step for carrier ionization and recombination - thereby effectively lowering the required transition energy between valence and conductance band. The go-to example for such an impurity is Au atoms in a Si lattice. (cf. [3])

Doping semiconductors is achieved by either temperature activated diffusion processes or the more modern approach of ion implantation. Through this technique much shallower and even retrograde dopand profiles with low concentrations are achievable. After the implantation process the crystal structure is usually tempered to activate the dopands and anneal the damage to the crystal structure. The

implanted atoms are included into the crystal's structure, thereby affecting the electronic structure in the desired way. (cf. [4])

1.1.6 Annealing

During ion implantation and possibly other prior processing steps inducing stress in the semiconductor crystal structure, defects can arise. Additionally, the implanted atoms will generally not be electrically active after implantation. These defects and the inactivity of the dopand material need to be adjusted for technical applications. (cf. [4])

The processes for activating the dopand atoms and healing the crystal structure after implantation are linked and dependent on each other. It is desirable, especially for future semiconductor devices at single-digit nanometer scales, for the dopand atoms not to diffuse too far in order to retain the doping profile generated by the implantation process but still guarantee electrical activation in the crystal. This is why rapid thermal annealing techniques are becoming more important nowadays. Temperatures in a RTA system typically range from 400 °C to 1200 °C with heating rates of 100 °C/s, thereby enabling dopand diffusion to active crystal sites as well as crystal structure healing within seconds. For certain applications even this heat rangeing is expected to be too slow. (cf. [4, 15])

In recent years even faster methods for annealing have been introduced. Among the more practical of these methods, due to the possibility of bulk processing, is Flash Lamp Annealing (FLA). In principle the FLA process is similar to a RTA system, as the sample is heated using halogen lamps to the desired temperature. The main difference is the speed and energy levels at which the lamps are discharged. A typical RTA system can reach 1000 °C within a few seconds. A FLA system can achieve similar or higher temperatures within milliseconds. Different FLA systems are in use with different specifications. The system used in our laboratory was built by Dresden Thin Film Technologies. It can pre-heat the sample or wafer up to 700 °C and deliver up to 90 J/cm^2 of energy within 20 ms over a processing area of a 2-inch wafer. The FLA process has been under investigation for a few years now. The formation of ultrashallow junctions in advanced technologies is among the research topics for FLA use. Other advanced applications are also being investigated. (cf. [15, 16])

Process models for the FLA process are currently in development. The reasons for this development are possible problems arising from the process itself, including but not limited to:

- reproducibility
- homogeneity over the process area
- diffusion of heat into the substrate

The emphasis here should be that the FLA process is still an experimental annealing method that hasn't reached full maturity yet. It is very likely for this method

to prevail though, especially considering the goals of the International Technology Roadmap for Semiconductors (cf. [17]). The sought-after dimensions of these new semiconductor devices require the millisecond-anneal times offered by the FLA process. Other methods like laser annealing do not seem suitable for bulk production methods. (cf. [15])

1.1.7 Optical Properties of Semiconductors

Among the most important measurements to obtain information on the band structure of a semiconductor are optical property measurements. Since transitions between bands can occur via emission or absorption of photons, the energy of these photons is characteristic for the bandgap energy. Even within a single band the photon absorption can be a measure for the free carrier absorption. Another related property indirectly measureable through optical means is the phonon spectrum, i.e. lattice vibrations or *phonons*. (cf. [3])

Transitions between bands generally underlie certain conservation rules that effectively split them into allowed and forbidden transitions. *Direct* transitions usually occur between two maxima/minima of the involved bands at the same wavevector k. To conserve momentum in *indirect* semiconductor transitions, phonons are involved in the transitions. Just like the photons themselves, phonons can be absorbed or emitted. They alter the absorption coefficient α, with E_{phonon} of equation 1.5, the phonon energy, and $\pm$ indicating whether absorption or emission takes place. Figure 4 illustrates the different possible transitions - direct and phonon-assisted - in a semiconductor band diagram.

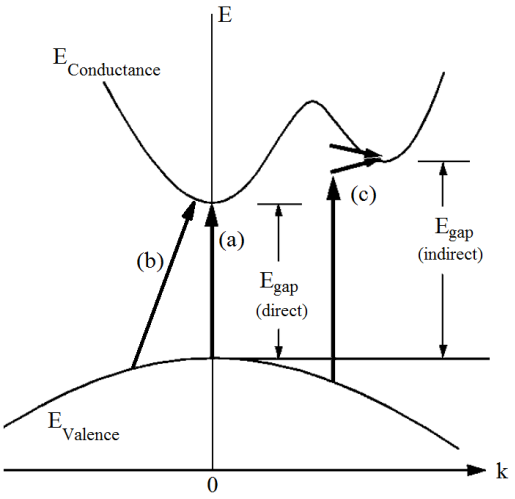


Figure 4. Illustration of the bandstructures of a direct semiconductor and possible transitions in a semiconductor, with a) direct transition at k=0, b) a forbidden direct transition and c) an indirect transition involving phonons (little arrows at the top) (adjusted from [3] p.52 Fig.29)

In a direct semiconductor like GaAs, only direct transitions like a) are allowed. Indirect transitions are only allowed via phonons c) and not with a $\Delta k \neq 0$ as in b). Experimental data for the absorption coefficients of Si and GaAs can be found in

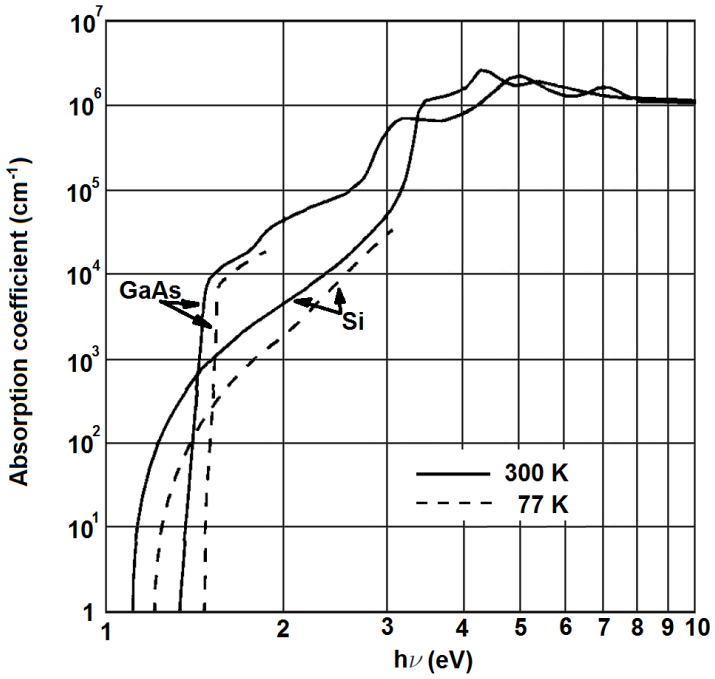


Figure 5. Absorption coefficients at 77 K and 300 K as a function of energy for Si and GaAs (adjusted from [3] p.53 Fig.30)

Figure 5. The behavior of the absorption coefficients is strongly linked to the bandgap and whether it is indirect (like in Si) or direct (like in GaAs). Certain transitions are only activated when a certain energy is reached, resulting in the given diagram. (cf. [3])

$$\alpha \propto (h\nu - E_{\text{gap}} \pm E_{\text{phonon}})^{\gamma} \tag{1.5}$$

Equation 1.6 relates the photon wavelength λ to the absorption coefficient α. An estimate for α close to the absorption edge is given in equation 1.7.

$$\alpha = \frac{4\pi k_e}{\lambda} \tag{1.6}$$

$$\alpha \propto (h\nu - E_{\text{gap}})^{\gamma} \tag{1.7}$$

where γ is a constant, E_{gap} is the bandgap energy and k_e is the imaginary part of the complex refractive index, also called the extinction coefficient, which determines the absorption coefficient.

1.1.8 Properties of Silicon

Si is an elemental semiconductor and the most widely used semiconductor in the industry. Si is the second most common material in the earth's crust. It has a density of $\rho = 2.336\,\text{g/cm}^3$, a melting point of $T_{melt} = 1415\,°\text{C}$. Several electronic properties were crucial for its success in particular electronic applications. Among these are

the bandgap energy of 1.12 eV, enabling a high breakdown voltage of pn-junctions and low leakage current. Its stable oxide also favors it in comparison with Ge, which was used prior to Si when the first transistor was demonstrated. Intrinsic Si has a resistivity of about $2.3 \cdot 10^3\,\Omega$m at room temperature. Through doping the resistivity Si can be lowered by a factor of up to 10^6. (cf. [3, 4, 18])

Crystal Structure of Silicon

Si crystallizes into the diamond crystal structure, where Si-atoms form a tetrahedral 3-dimensional structure. The lattice constant is 543 pm. (cf. [3, 19])

Band Structure of Silicon

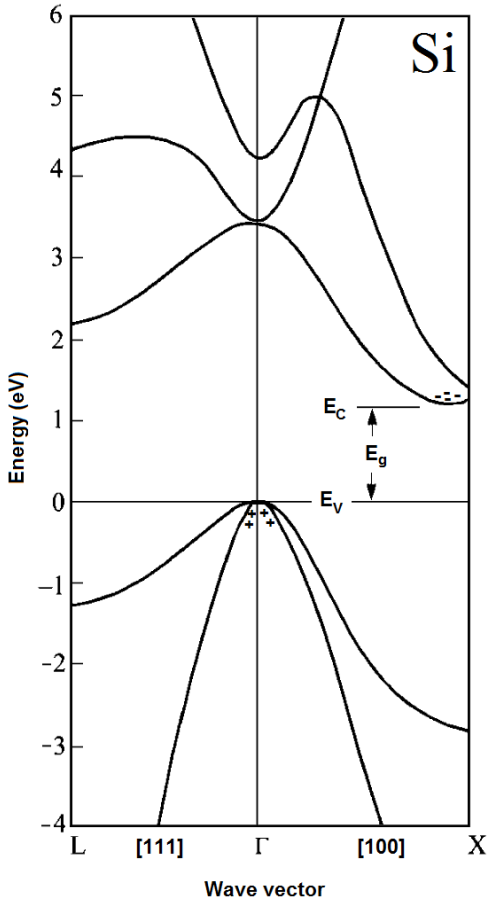


Figure 6. Schmeatic energy band structure for Si, the gap energies are 1.12 eV at the X-poin, 3.4 eV at the Γ-point and 2.2 at the L-point (adjusted from [3] p.14 Fig.4)

Figure 6 shows the energy band structure of Si. It is an indirect semiconductor due to the lowest point of the conduction band being off-center along the (100)-axis as described before in section 1.1.4. The temperature coefficient of the band gap energy $\frac{dE_{\text{gap}}}{dT}$ is negative and decreases with pressure. The gap energy is 1.12 eV at the X-point, at the Γ-point it is 3.4 eV whereas at the L-point E_L the bandgap energy is 2.2 eV. (cf. [3, 12, 13])

The mobility of electrons in Si can be up to $1400\,\mathrm{cm}^2 V^{-1} s^{-1}$, the mobility of holes up to $450\,\mathrm{cm}^2 V^{-1} s^{-1}$. (cf. [20])

1.1.9 Properties of Gallium-Arsenide

GaAs is a so-called III-V semiconductor, consisting of atoms from the third and fifth groups in the periodic table. GaAs has a melting point of $T_{melt} = 1238\,°C$ and a density of $\rho = 5.3\,\mathrm{g/cm}^3$. Although Si is still the most widely used material, GaAs has covered ground in scale manufacturing due to higher mobility which enables high performance devices and effective light emission. Intrinsic Gallium Arsenide displays high resistivity values at $10^6\,\Omega\mathrm{m}$ at room temperature. (cf. [3, 21])

Crystal Structure of GaAs

The compound semiconductor GaAs crystallizes into a zincblende structure as discussed in section 1.1.3. Thereby, depending on the observation point, a gallium atom is surrounded by four arsenic atoms (or vice versa) in a tetragonal way. Usually intrinsic GaAs displays many defects in its crystal structure, depending on material processing and the growth mechanism.

In GaAs, of the low-order planes only the (100), (111) and $(1\bar{1}1)$ planes display polarity. The (110) surface is non-polar. (cf. [3, 22])

Band Structure of GaAs

Figure 7 shows the energy band diagram for GaAs. In contrast to Si, GaAs has a direct bandgap. This fact might enable better use of this compound in optical applications like photon detectors. The bandgap of GaAs at room temperature is 1.42 eV (E_Γ). At the X-point E_X the gap is 1.90 eV and at the L-point E_L is 1.71 eV. As with Si, the temperature coefficient of the band gap energy $\frac{dE_{gap}}{dT}$ is negative in GaAs. Its bandgap increases with added pressure. (cf. [3, 19])

1.2 The Physics of Metals

Metals represent the principal case for solid state physics because they can be easily described. The simplest theory describing the electronic properties of metals is the free-electron model (or *Sommerfeld* model). In this theory the lattice of metal atoms is assumed to be one large potential well for the electrons. Some subsequent calculations reveal many of the basic properties of metals. (cf. [23, 24])

1.2.1 General Properties of Metals

Metals have low resistivity (typically $< 10^{-5}\,\Omega\mathrm{m}$), and good thermal conductivity λ (typically $100\,\mathrm{W/(m{\cdot}K)}$). The law connecting these two properties is the Wiedemann-Franz-law (equation 1.8) with the universal constant $L = 2.45 \cdot 10^{-8}\,\mathrm{W\Omega K}^{-2}$.

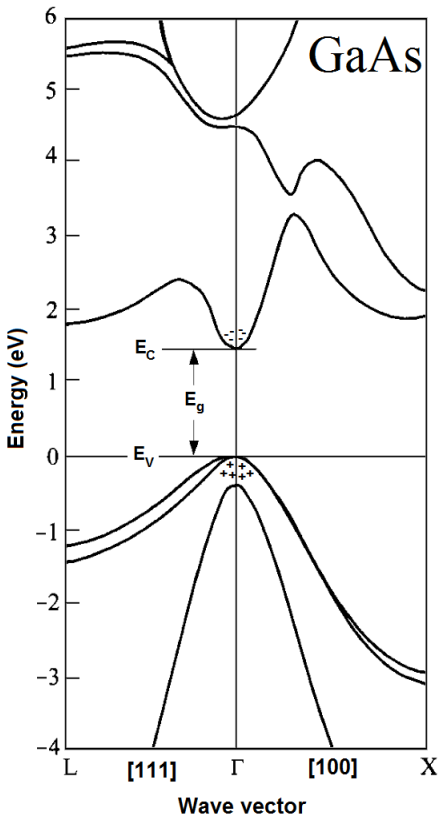


Figure 7. Energy band structure for GaAs, the bandgap energies are 1.42 eV at the Γ-point, 1.90 eV at the X-point and 1.71 eV at the L-point (adjusted from [3] p.14 Fig.4)

$$\frac{\lambda}{\sigma} = LT \tag{1.8}$$

In contrast to semiconductors, the resistivity of metals typically increases with temperature. The reason for this lies in the conduction mechanism in metals as opposed to the mechanism in semiconductors. In a metal the conduction and valence band overlap, so the electrons needs virtually no energy to pass to the conduction band. This is the reason they are referred to as free electrons in the metal crystal lattice. The mobility of the electrons is primarily governed by the thermal movement of the atomic bodies in the crystal lattice. More movement will lead to more scattering of the electrons.

Magnetically, many different configurations are possible, the simplest ones being ferromagnetic, paramagnetic and diagmagnetic. Ferromagnetic materials like Ni (see 1.2.5) can retain a magnetic order in their lattice which can result in the possibility of permanent magnets. A paramagnetic material can be magnetically oriented in an external field, but loses its magnetic order once the external field is turned off. In a diamagnetic material an external magnetic field is dampened. Superconductors are perfect diamagnets, they push any external magnetic field out of its volume. (cf. [23, 24])

1.2.2 Band Structure of Metals

The bonds in a metal lattice are ionic in nature. The ions in the lattice can be positively or negatively charged and are held in place by their mutual attraction. This behaviour is a result of the band structure of metals. In contrast to semiconductors, no bandgap between valence band and conduction band is present in the energy band diagram. Any excitation of electrons in the valence band allows them to enter the conduction band. Once there, the electrons are no longer associated with a certain atom and can roam the crystal lattice freely. The reason for the free electron model to work as well as it does was later explained by introducing the concept of Laundau-quasiparticles. They display the same properties as the electrons save for their mass and therefore their energy. This change is due to their interactions with the crystal lattice. (cf. [23–25])

1.2.3 Crystal Structure of Metals

Metals and alloys come in a wide variety of crystal structures and lattices. Different concentrations of metals in an alloy can lead to differences in crystal structure, often resulting in differences in mechanical or electrical properties. The crystal structure of the metals relevant to this thesis are mentioned in the following sections for Au, Ni and Sn (1.2.4, 1.2.5 and 1.2.6 respectively). (cf. [19, 23, 24])

1.2.4 Gold

Gold (element symbol Au) crystallizes into a face-centered cubic structure. It has a melting point at $T_{melt} = 1064\,°C$ and a density of $\rho = 19.3\,g/cm^3$. It is among the best materials for thermal and electrical conduction with its low resistivity of only $2.4 \cdot 10^{-8}\,\Omega m$ and thermal conductivity of $310\,\frac{W}{mK}$ at room temperature.

Since Au is a noble metal, it is chemically inert and stable faced with most chemicals and etchants. Au etching can be achieved using aqua regia, a mixture of nitric and hydrochloric acid at a ratio of 1:3. Also, it is a diamagnet. (cf. [19])

Plasmonic Properties of Gold

Au is among the materials that support visible light-excitation induced collective oscillations of free charges. When confined in a highly conductive nanocrystal this is refered to as localised surface plasmon resonance (LSPR). This property refers to the large enhancement of the extinction cross-section (sum of absorption and scattering cross-sections) and an associated enhancement of the local electric field upon resonant excitation at the LSPR-wavelength. In order for a material to show LSPR it needs to be able to entain free charge carrier concentrations of up to $10^{21}\,cm^{-3}$. Other materials displaying this property in the visible range are for example silver and copper. The resonant excitation in LSPR can be used to break the diffraction limit and effectively concentrate light into nanoscaled regions. Therefore applications for

Au nanoparticles and -crystals in future optoelectronic devices and detectors might be achievable. (cf. [7])

1.2.5 Nickel

Nickel (Ni), like Au, also crystallizes into a face-centered cubic crystal structure. Pure Ni has a resistivity of $\rho = 7 \cdot 10^{-8}\,\Omega$m and thermal conductivity of 70 $\frac{\text{W}}{\text{mK}}$. It has a density of 8.9 g/cm^3 and a melting point of $T_{melt} = 1455\,°C$. Ni, along with iron, cobalt and gadolinium, is one of the four known materials that are ferromagnetic at room temperature. It is used extensively in the manufacturing of various Ni alloys like constantan. (cf. [19])

1.2.6 Tin

Tin (element symbol Sn) has a density of 5.8 g/cm^3 and a melting point of just $T_{melt} = 232\,°C$. Its resistivity is $\rho = 1.1 \cdot 10^{-7}\,\Omega$m and its thermal conductivity is about 67 $\frac{\text{W}}{\text{mK}}$. It has two polymorphs into which it can crystallize. While white β-Sn has a tetragonal structure, gray α-Sn has a face-centered diamond-cubic one. In electronics, Sn is widely used for soldering, in part due to its low melting point. (cf. [19])

1.3 Nanostructures

Electronic circuits have been scaled down for the last decades, eventually reaching nanoscale dimensions. At these scales due to the confinement effect the functional properties of materials can change drastically. Electronic and optical properties are also determined by quantum effects. The scale where this usually takes place is when the dimensions of the functional elements reaches de-Broglie matter wavelengths. The effect of nanostructuring on the density of states is illustrated in Figure 8.

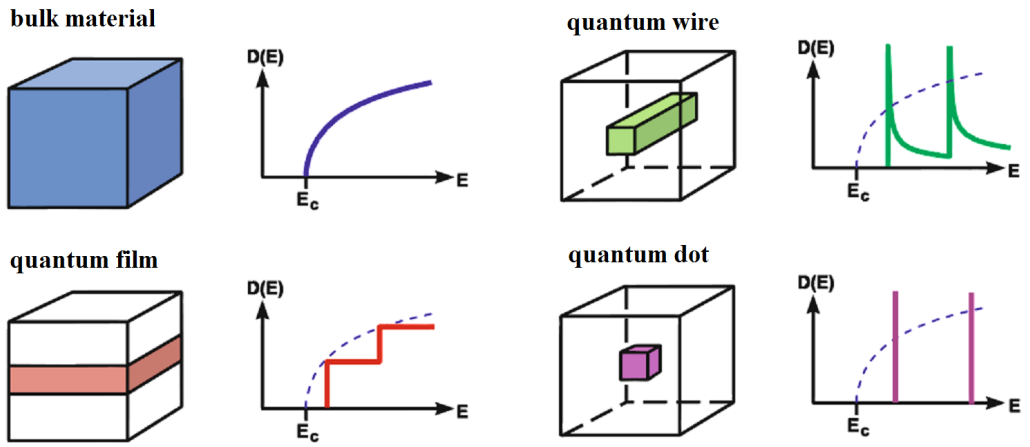


Figure 8. Illustration of quantum effects on the density of states, illustrated through confinement into 0D, 1D, 2D ad 3D nanostructures (adjusted from [13] p.462 Figure 14.1)

The top left image in Figure 8 represents 3-dimensional (bulk) material, which will result in the density of states $D(E)_{3D}$ to be

$$D(E)_{3D} \propto E^{\frac{1}{2}} \tag{1.9}$$

The 2-dimensional case $D(E)_{2D}$ (Figure 8 bottom left) will result in

$$D(E)_{2D} \propto E^0 = \text{const} \tag{1.10}$$

with multiple steps, whereas the 1-dimensional case $D(E)_{1D}$ (Figure 8 upper right) follows

$$D(E)_{1D} \propto E^{-\frac{1}{2}} \tag{1.11}$$

and the 0-dimensional case $D(E)_{0D}$ (Figure 8 bottom right) reveals

$$D(E)_{0D} \propto \delta(E) \tag{1.12}$$

This means that novel electrical and optical properties are attainable by structuring materials at these scales. At the same time it can result in the loss of function of downscaled conventionally-structured devices. This fact is among the most important driving forces for research efforts at the nanoscale. (cf. [13, 17, 26])

1.3.1 Nanowires

The definition of a nanowire (NW) is a bit loose. Quite often the same structures are referred to as NW, nanorods, quantum wires or similar terms. A wide variety of materials have been top-down structured or bottom-up grown into NW. Two of these are the ones used for the research conducted for this thesis: Si and GaAs. (cf. [13])

In the International Technology Roadmap for Semiconductors, NW represent one of the last points in Si technology. With Si-NW, combined with a gate-all-around architecture, the construction of NW field-effect transistors (FETs) at the scales necessary to adhere to the ITRS goals have been demonstrated. NW with diameters as small as 0.5 nm have already been synthesized. This is the main reason for the huge research effort devoted to NW structures and their properties. (cf. [17, 27])

One method for NW synthesis is the vapor-liquid-solid (VLS) method which is presented in the following section.

1.3.2 Nanowire Synthesis: The Vapor-Liquid-Solid Process

The Si-NWs used in this thesis were synthesized using the VLS process as depicted in Figure 9. First, Au is deposited on a Si substrate (Figure 9 (a)). Next, the sample is pumped to $5 \cdot 10^{-2}$ mbar and a constant stream of silane and hydrogen. It is heated above the eutectic temperature. The Si from the gaseous silane gets adsorbed by the Au droplets on the sample. A liquid metal-semiconductor alloy is formed atop the Si wafer (Figure 9 (c)). If the gas flux remains, ever more Si diffuses

into the Au droplets eventually oversaturating them. The excess Si is deposited on the interface between the Si wafer and the Au-Si alloy droplet. Running this process continuously results in the synthesis of NW epitaxially grown on the surface of the Si wafer (Figure 9 (d)). Epitaxial means the crystal orientation of the synthesized NW orients itself along the one of the Si substrate. Depending on the partial pressure of silane, synthesis temperature and the diameter of the catalytic particle, the growth orientation may change from the (111) direction to (110) or (112). A change in the surface energies and line tension at the contact surface between the Au droplet and the NWs may also result in an orientation change. After synthesis, the Au droplet remains on the NWs as a cap.

GaAs can also be synthesized this way using different precursor gases. (cf. [28, 29])

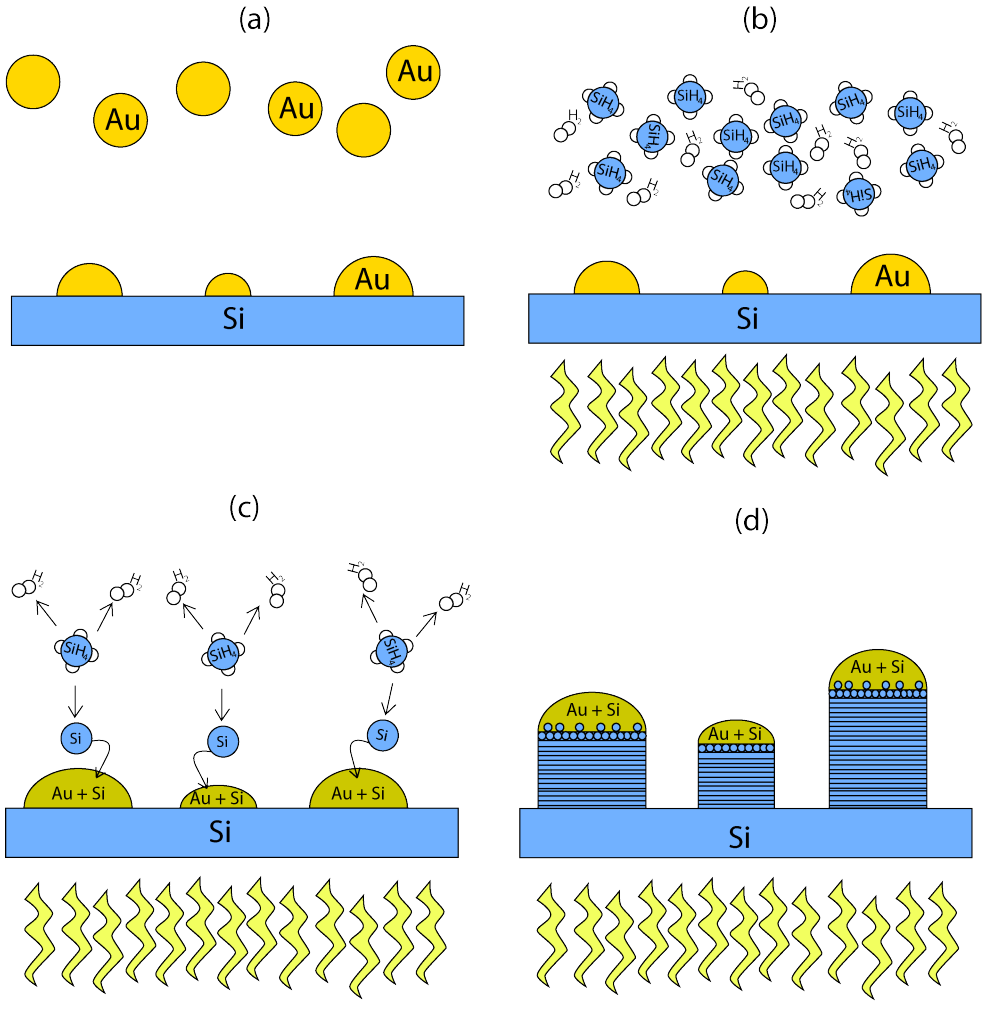


Figure 9. VLS process for NW synthesis, (a) Au deposition, (b) heating to eutectic temperature with stream of SiH_4 and H_2, (c) adsorption and diffusion of Si into the Au droplets and (d) epitaxial growth of NW

The GaAs-NW used for this thesis were synthesized by gallium-assisted self-catalysed molecular beam epitaxy (MBE). With this method a Ga catalyst is used.

It is based on a sputtered layer of SiO_2 on a GaAs wafer which acts as a nucleation site for the NW growth. For details see [30].

1.4 Phase Diagrams and Properties of Material Combinations in Liquids

In the two following sections the usual theory on phase diagrams including the recrystallization process and the surface energy of binary systems is discussed in context for later referral from experimental data. The last section will deal with diffusion in liquids, focusing on diffusion speeds when compared with solid material.

1.4.1 Phase Diagrams & Crystallization Process in General

The interactions of different elements in a liquid and their crystallization into different structures and alloys is governed by their thermodynamic properties. Binary phase diagrams show the possibilities for recrystallization into different components depending on the concentrations of the participating elements when two components are mixed and melted. The thermodynamic theory behind these diagrams relies on the assumption of an equilibrium or at least a high diffusion rate at every point in the diagram, thereby giving the components the necessary time to diffuse and minimize their free energy that way. For a mixture to reach equilibrium long diffusion times have to be taken into account. Especially in solids and at the liquid-solid boundary, diffusion occurs slowly. Therefore phase diagrams should only be used with care, with these limitations in mind, to account for certain features in the experimental data of this thesis. (cf. [15, 24, 31])

Usually, crystallization processes start at a nucleation site and build up solid material of certain concentrations of the two or more participating elements. Along these solid grains, as cooling progresses, more material crystallizes changing the concentrations in the molten mass via uptake of different amounts of the participating elements. The physical and chemical interactions between the elements (which define the lattice energy) will dictate what concentrations are favoured. An important property that some material combinations display is the formation of an eutectic system, where the melting point of the mixture depends on the concentrations of the participating elements and is lower than that of the partcipating elements themselves. Examples for this are Si and Au as well as Si and Ni at certain concentrations. The following sections will cover the material combinations used in the experimental work for this thesis. (cf. [24, 31])

1.4.2 Phase Diagram Si-Au

Figure 10 represents a simple case, with an eutectic phase lowering the melting point of the alloy compared with the melting points of the pure Si or Au. When a mixture between the two participating elements is present at a high temperature and

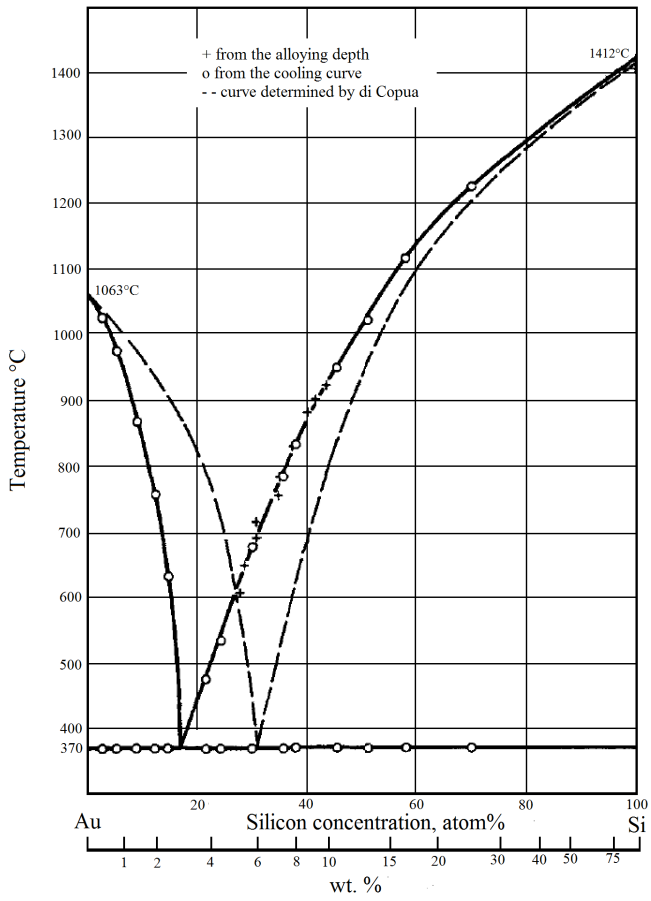


Figure 10. Phase Diagram of Si and Au mixture (adjusted from [32])

it is being cooled, for interpretation the lines of the diagram are the most important part. Take for example a mixture of 40 atom-% Si in Au at a starting temperature of 1500 °C. The recrystallization into a solid form only occurs when the temperature is lowered below about 890 °C. At this stage, 2 phases will separate, one of them pure solid Si and the other the molten mass at an altered mixture concentration. In the diagram the concentration can be determined by measuring the distance of the point you're at (temperature and concentration) and the Si-baseline as well as the distance to the liquid-solid line that eventually leads to the eutectic point. The coefficient between these two distances represents the concentration. When the eutectic point at 370 °C is hit when cooling, the phases will fully separate into Au and Si phases. [31, 32]

1.4.3 Phase Diagram Si-Ni

Figure 11 shows the phase diagram of Si with Ni. Multiple compounds are formed. This is also one of the reasons for this material system's phase diagram to be much more complicated than the simple Si-Au system. Each line that reaches the bottom of the diagram represents a chemical combination of Ni and Si. Therefore, when

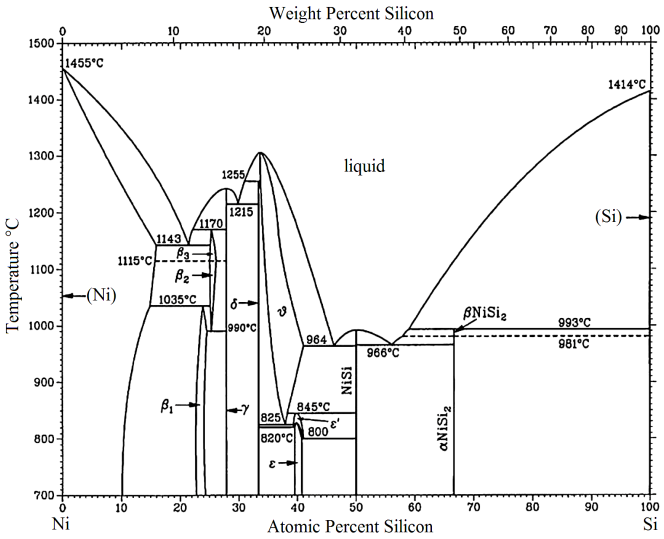


Figure 11. Phase diagram of Si and Ni mixture (adjusted from [33])

some mixture at a high temperature is cooled, these compounds will be the stable final phases of the cooling process. Only to the very right and left of the diagram (meaning either very low Si or very low Ni concentrations) will result in pure Si or Ni crystals. Also, the resulting crystal structure will depend on the concentration in the beginning (greek letters in the diagram). (cf. [31, 33])

NW with 'excellent physical properties' made of NiSi have recently been demonstrated. (cf. [34, 35])

1.4.4 Phase Diagram Si-Sn

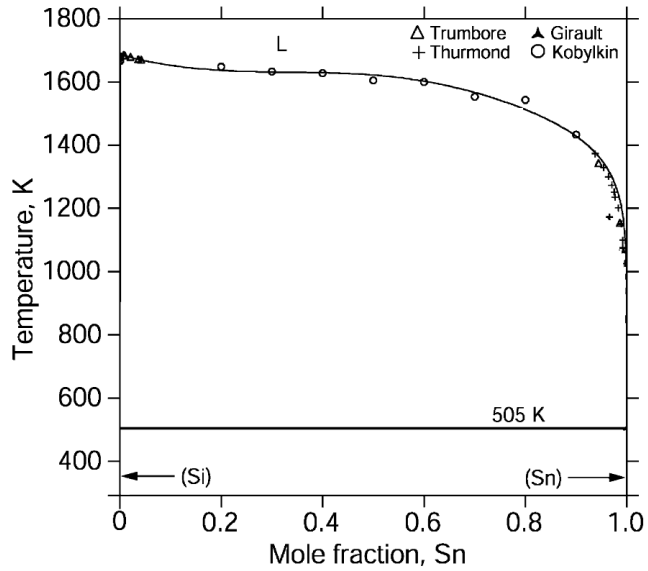


Figure 12. Phase diagram of Si and Sn mixture (adjusted from [36])

Figure 12 shows the phase diagram of Si and Sn. Since no compounds form between Si and Sn and also no eutectic system is formed, the phase diagram is

very simple. Any mixture between the two elements will fully crystallize back into the pure participating elements. (cf. [31, 36])

1.4.5 Phase Diagram GaAs-Au

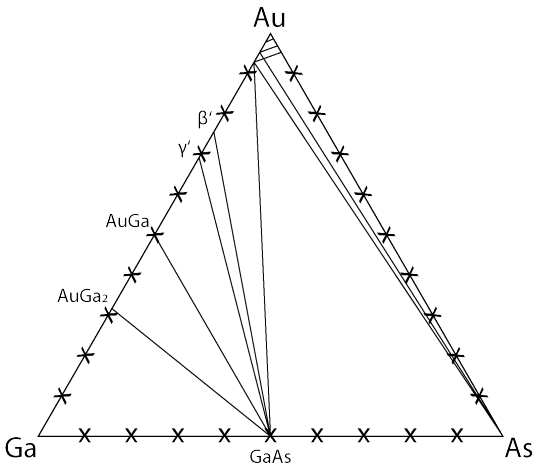


Figure 13. Ternary phase diagram of a mixture with Ga, As and Au (adjusted from [37])

Figure 13 shows the ternary phase diagram of Ga, As and Au. Since it is a ternary system no simple 2-dimensional phase diagram can be drawn due to the three elements involved, making it a ternary system. Shown by Beyers at al [37], GaAs combined with different metals are classified into groups. Au, together with silver and tungsten represent the simplest of 7 cases when combined with gallium arsenide. The paper dubs this case Type-I, when the GaAs is dominant. In this arrangement, the most important feature is the tie-line between the metal (Au) and GaAs, leading to a stable contact between them. Figure 13 shows the actual diagram as determined by Tsai and Williams (cf. [38]). In a perfect Type-I situation, the line would lead straight from GaAs to the metal. For Au this is almost the case, resulting in the expected behaviour of the bond between gallium and arsenide to dominate the system as long as the Au content is not too high. This means that when these materials are mixed, GaAs will be the dominant compound when crystallizing, resulting in a GaAs-phase and a completely separate Au phase. (cf. [37])

1.4.6 Liquid Boundaries: Surface Energy

The surface energies of the involved phases in the recrystallization process can be used to predict the outcome of recrystallization including the interface structure. In a simplified model, two liquids with non-zero surface energies would de-mix prior to recrystallization. Depending on the sign of the surface energy, this would result in a concave or convex interface between them. In NWs it has been observed for interfaces between certain III-V semiconductors to be concave or convex after the recrystallization of the materials into solids. For the structures discussed in this thesis this model is too simple though. There seems to be a surface energy equilibrium

between the two liquids which should result in their mixing since the interface is straight rather than concave or convex. This indicates that the liquid phases do not separate prior to crystallization in this simplified model. To account for the observed behaviour a model incorporating the solid and gaseous phases and their respective contributions to the surface energy is probably needed. Also, this model does not take into account possible interactions with the liquids' container (the SiO_2-shell in the case relevant to this thesis). (cf. [6, 39])

1.4.7 Diffusion

Diffusion is a transport phenomenon, usually describing the transport of a gas or liquid through some obstacle or distance, thereby mixing or de-mixing the participating materials. It is mainly governed by the diffusion constant of the respective materials. The diffusion constant is directly derived from the mean free path Λ and the mean velocity $\bar{v}$ of the involved atoms.

$$D = \frac{\Lambda \cdot \bar{v}}{3} \tag{1.13}$$

This automatically means that diffusion in a solid, which also does occur, will inevitably occur at a much slower rate than in a liquid. Since the position of the atomic nuclei in a crystal lattice is fixed, diffusion can only occur when some process removes them from their fixed position and allows for diffusion. This limits the speed at which diffusion can take place. The diffusion constant displays values of around $10^{-9}\ \frac{m^2}{s}$ for example for ethanol in water, whereas in a solid it will be in the order of magnitude of $10^{-13}\ \frac{m^2}{s}$ for example for Au in Sn. This is a diffusion speed difference of 4 orders of magnitude. Higher temperatures are beneficial for diffusion speeds in solids as well as liquids. (cf. [39, 40])

1.5 Metal-Semiconductor Heterostructures

The general goal of a heterostructure is usually to combine multiple material properties, like two different semiconductors, into a single device that takes advantage of both materials' properties. It can for example be used to alter the band gap and band gap energies (band structure tuning) and even to induce new functionalities not observed in conventional materials. Historically, heterostructures were synthesized with the goal of combining two semiconductors and their properties, although considerable effort has been devoted toward metal-semiconductor heterostructures. An interesting research topic is the integration of plasmonic metals like Au into metal-semiconductor heterostructures. Plasmonics and LSPR are explained in the section about Au (see 1.2.4). Another research area is the use of such a structure for the photocatalytic conversion of light energy.

Modern electronic devices are already heavily reliant on heterostructures, for example diodes, lasers or high electron mobility transistors (HEMT). Charge carriers in layers may display higher mobility and high radiative recombination efficiency. Also

much work has been devoted towards realizing a metal-base transistor, combining the high carrier density of a metal with the band gap property of a semiconductor. (cf. [7, 11, 13, 41])

1.5.1 The Semiconductor-Metal Interface

The following sections will focus on several effects occuring at the interface of a semiconductor and a metal.

Schottky-Contact

The theory correctly describing the formation of a barrier at the semiconductor-metal interface is the thermionic-emission model developed by Bethe in 1942. Historically, Schottky first suggested the model in 1938 though, so the barrier is named after him. Usual names are Schottky diode, Schottky contact or Schottky barrier. The amount of current that can be transfered over the interface is controlled by the height of this potential barrier. The capacitance behavior is also goverened by it. (cf. [3])

Band Structure of the Interface

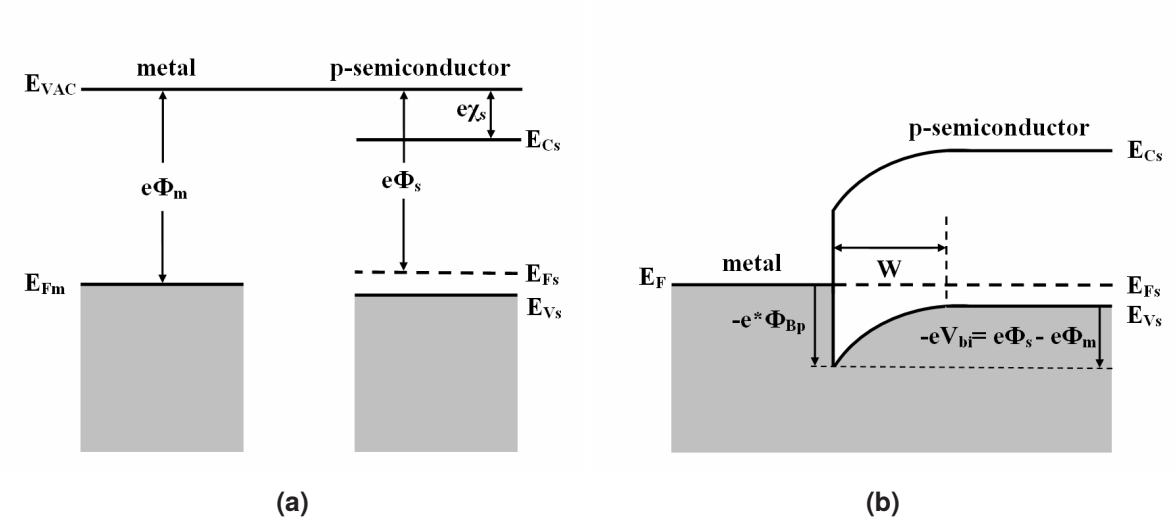


Figure 14. Schematic of an idealized energy band diagram at the interface of a metal and a p-type semiconductor. (a) energy levels of metal and semiconductor, (b) resulting Schottky barrier (cf. [42] p.38 Figure 2.14)

The formation of the Schottky barrier is schematically shown for a p-type semiconductor in Figure 14. E_{Fm} is the Fermi energy of the metal, E_{VAC} the energy of the vacuum level, E_{C_s} and E_{V_s} are the energies of the conductance and valence bands and E_{F_s} the Fermi energy of the semiconductor. ϕ_m is the metal work function and ϕ_s the semiconductor work function, χ_s is the electron affinity of the semiconductor.

In Figure 14 the case when $\phi < \phi_s$, with ϕ_s as the Fermi level of the semiconductor, is illustrated. When contact is established between the semiconductor and the metal, the Fermi levels adjust to coincide. Electrons from the metal flow into the

semiconductor to fill its Fermi level. The electrons are minority carriers in the p-type semiconductor. Therefore the holes of the semiconductor in the interface region will be filled. This leads to the establishment of an electric field at the interface. Depending on the concentration of the acceptor, this depletion region (depletion width W) will be larger or smaller. Since a metal will typically have very high concentration of free electrons no depletion layer will be generated in the metal.

This potential barrier is a result of the difference of the work function of the metal ϕ_m and the electron affinity χ_s of the semiconductor. An idealized model results in the following equation for the barrier energy for holes

$$\phi_{B_p} = \frac{E_g}{q} - (\phi_m - \chi_s) \tag{1.14}$$

where E_g is the bandgap energy of the semiconductor and q is the elementary charge. When holes are transferred from the semiconductor to the metal the opposing barrier height is

$$V_{bi} = \phi_s - \phi_m \tag{1.15}$$

where V_{bi} is the built-in potential of the junction. (cf. [42])

Interface States and Fermi-Level Pinning

In reality, the metal work function and the interface states determine the barrier height of the Schottky contact. Calculation of a general expression for the barrier height relies on assumptions concerning the contact gap width and the density of interface states. If the interface trap density is high (approaching ∞), the Fermi level at the interface is *pinned* above the valence band by the surface states, resulting in the surface properties of the semiconductor determining the barrier height. On the other hand, if there is a negligible amount of interface traps, the barrier height will be as predicted by the ideal Schottky-contact model, where surface-state effects are not taken into account. The Mott-theory is used to describe this situation accurately. (cf. [3, 13])

1.6 Raman Spectroscopy

Raman scattering is a mechanism for light scattering where interactions of rotational, vibrational or phonon modes with electromagnetic radiation are measured. The scattering is inelastic which leads to a change of the energy and therefore frequency of the incident light. This frequency shift is measured. It is most commonly used for nondestructive measurements for the determination of stoichiometry, crystal structure, impurity concentration and strain in solids. The used light source is usually monochromatic (a laser). The photon of energy $h\nu_0$ can be absorbed by a molecule exciting it. If the incident photon does not have enough energy to excite the

molecule, it may be lifted to a virtual state. Since this virtual state is not stable, light emission has to occur for the molecule to relax into the ground state again. (cf. [1])

The main scattering mechanism is *Rayleigh-scattering*, with a probability of approximately 10^{-3}. The molecule is excited into a virtual state and subsequently falls back to the ground state under emission of a photon. Rayleigh scattering is elastic. In *Stokes-Raman scattering* the molecule falls to a higher vibrational state instead of the ground state. The emitted photon displays a smaller energy, in a recorded spectrum a characteristic line appears at higher wavelengths than the Rayleigh peak at 0. *Anti-Stokes-Raman scattering* takes place when a molecule is already excited to a vibrational state. The emitted photon can have a higher energy, thus the spectrum is shifted to smaller wavelengths (negative shift values). The probability for this process is only 10^{-9}. For analysis Stokes-Raman spectrum are most commonly used. The wavenumbers are traditionally given as in equation 1.16 due to the values being very small. (cf. [1])

$$\delta w = (\frac{1}{\lambda_0} - \frac{1}{\lambda_1}) \cdot 10^{-7}[\text{cm}^{-1}] \tag{1.16}$$

CHAPTER 2

Experimental Techniques

In the following chapter the experimental techniques that were used to synthesize and analyze the NW heterostructures of this thesis are presented. The processing steps and parameters for the synthesis of the structures are presented in chapter 2.1. Further processing techniques for analytics follow in section 2.2. The measurement methods follow with section 2.3 dealing with electronic measurement preparations and section 2.4 with phononic measurements.

2.1 Method for NW Heterostructure Formation

In this thesis the synthesis of epitaxial metal-semiconductor heterostructures was achieved employing a bulk method. The Formation process is based on common semiconductor processing techniques like sputtering, chemical vapor deposition and the rather new FLA. In the following section a general overview is given for the synthesis method developed in the course of this thesis. In the subsequent sections the individual processes are explained in detail.

2.1.1 General Overview of the Synthesis Method

The basis material were VLS-grown NWs with diameters of typically 80 to 150 nm and lengths of up to 10 µm. Figure 15 depicts the synthesis method for the heterostructured NWs schematically. Starting off with as-grown NWs (a), the desired material is deposited on the bare NW (b). Next, a layer of SiO_2 is added as a thin shell via a PE-CVD process (c). In the final step, the sample is annealed using the FLA (d). Detailed parameters for the following processes can be found in Appendix A.

2.1.2 VLS Synthesis

The NW synthesis was conducted in a custom-built NW CVD oven. First the oven chamber was vented and the sample placed inside. Next, the chamber was pumped to vacuum conditions. When a pressure below $5 \cdot 10^{-2}$ mbar was reached, heating started and the precursor gases were introduced. The processing parameters were controlled via a computer program. The pressure had to be adjusted to the desired value via a manual valve. For more detailed parameters see Appendix A.1.

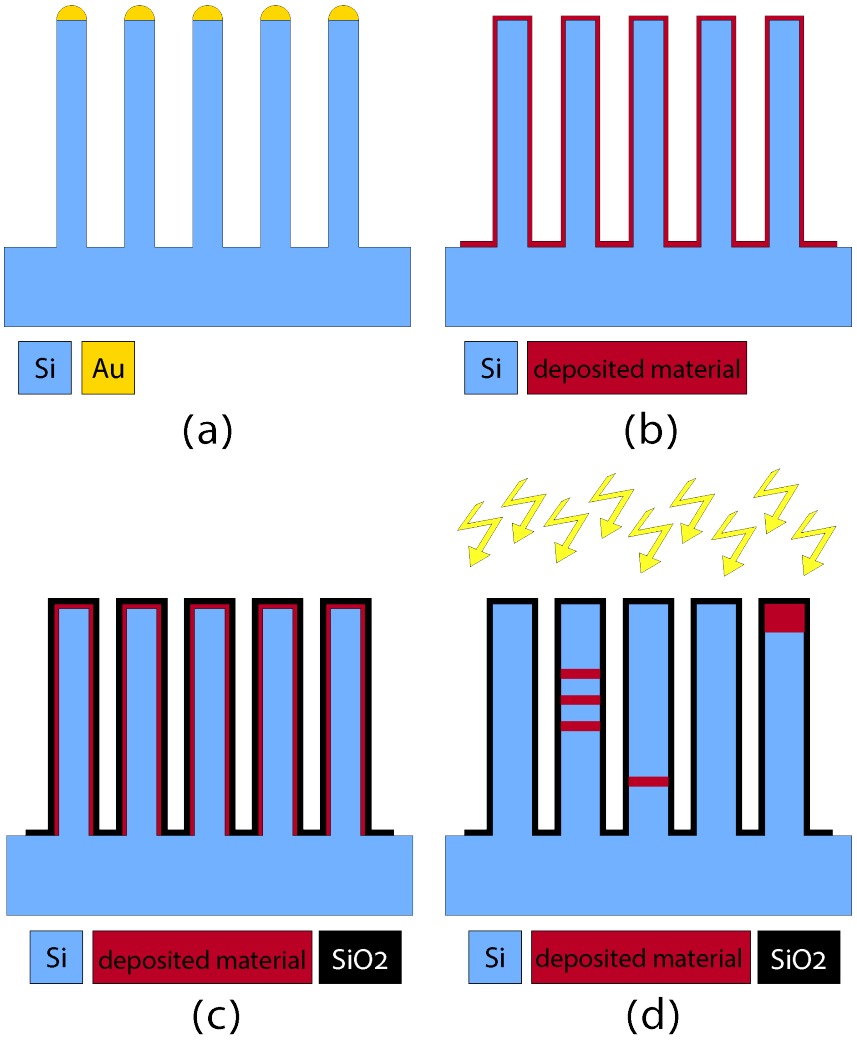


Figure 15. Synthesis of heterostructured NWs, (a) Si-NW synthysized by the VLS method, (b) deposition of desired segment material (VLS Au caps removed prior to this step), (c) SiO_2-shell deposited via PE-CVD and (d) the FLA process yielding the segments

A typical sample with as-grown Si-NWs is shown in Figure 16. Using 80 nm Au colloids resulted in growth of the Si-NW. Due to some subsequent equipment problems, sputtered Au was later used as the growth catalyst instead.

Preparation

Before the VLS process for NW growth, the substrates had to be cleaved into appropriate sample pieces and any surface contaminations with dust or other materials had to be removed. A wafer oriented along a (111) plane breaks into 45 °-angled pieces relative to the indicated direction along the wafer. For sample preparation this can be troublesome and lead to triangle- or rhomboid-formed samples. Preferably a (100)-oriented wafer is used to achieve rectangular wafer pieces. When 100-pieces are used for VLS growth of NW, they will not grow perpendicular though, as the VLS

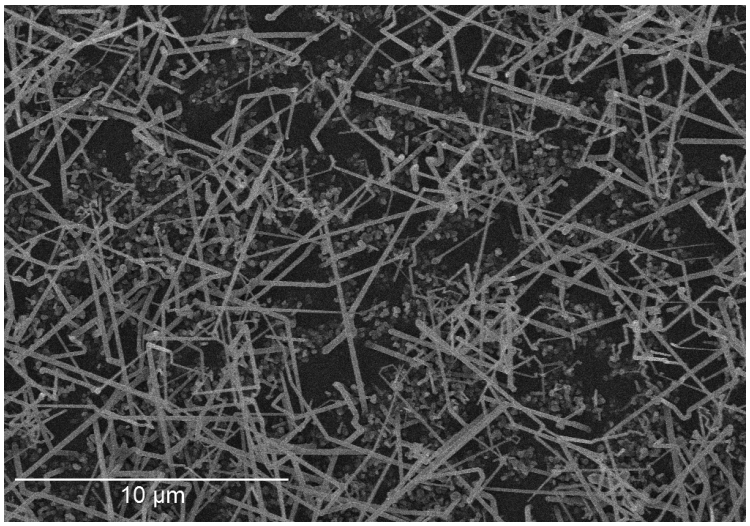


Figure 16. SEM image of typical as-grown Si-NW on a Si substrate wafer

process under the given experimental condition results in epitaxial 111-oriented NW growth.

For cleaning, the sample was rinsed in acetone. An ultrasonic bath removed any surface contaminations. Then the sample was submerged in isopropanol for a few seconds and dried using dry nitrogen.

2.1.3 NW Surface Preparation & Gold Removal

Native oxide was removed via wet-chemical etching. For Si-NWs, buffered hydrofloric acid (BHF, HF buffered with NH_4F) at a concentration of 1:7 was used. For GaAs, diluted hydrochloric acid (HCl) at 1:1 with H_2O was used.

To remove the Au catalyst from the VLS NW synthesis, a Au removal process optimized by Markus Glaser was employed. First, the sample was etched for 10 seconds in BHF, then for 5 minutes in aqua regia. Next, the sample was oxidized in the RTA-system at a temperature of 900 °C. After the oxidation step, the 10 seconds of etching in BHF and the 5 minutes of etching with aqua regia are repeated. The idea is that catalytic etching of SiO_2 around small Au droplets creates small cavities large enough for the aqua regia to enable etching of these very small Au impurities. This results in a completely Au-free sample surface.

Metals can have a catalytic effect on etching which is then called metal assisted etching. An example for this is Au acting as a catalyst when etching Si with HF.

Diluted aqua regia (3 parts 37% HCl : 1 part 70% HNO_3 : 2 parts H_2O displays a remarkably high etch rate when etching Au of about 11 $\frac{nm}{s}$. It does, however, usually not etch SiO_2 at all or, in case of an unannealed PE-CVD oxide, only very slowly at 0.7 $\frac{nm}{min}$. (cf. [43, 44]

2.1.4 Metal Layer Deposition on the NWs

Several materials have been deposited on NWs in order to achieve a segmented structure. Since VLS synthesis of NW leaves the NWs with a Au cap, this cap had to be selectively removed when different materials than Au were deposited. The Au removal process is described in section 2.1.3.

Three different methods were used to deposit material on/in the NWs: sputtering, evaporation and implantation.

In almost every case, the samples were simply sputter coated with the desired material (Au, Ni, ...). Typically, they were covered by a 3 to 5 nm thick layer of the desired metal. The amount of material sputtered onto the sample was varied considerably, as described in the material systems sections 3.2 and following. Any and all layer thickness values should be considered approximate due to limitations in accuracy of the sputtering process. Also, the values mentioned represent sputter rates measured by deposition on flat substrates. 3-dimensional non-flat structures such as NW will result in a different deposition rate on their surface.

Implantation is an exceedingly laborious method for introducing material into NW structures, therefore this method was only used once. The implantation took place at the Institute for Solid State Physics in Jena. In this case about 2% tin was implanted, with the energy optimized for the implanted tin to reach the core of the used Si-NW. Sn was implanted since it oxidises rapidly and cannot be covered with the SiO_2 before all of the deposited Sn is oxidised, which renders it inert in the context of heterostructure synthesis.

Evaporation was also only used once for trial purposes (Sn) to achieve a smooth one-sided covering. For the evaporation to result in a pure layer of the desired material, a pressure of about 10^{-7} mbar is needed. This is achieved by long pumping times and subsequent gettering with titanium.

Detailed parameters for all deposition methods can be found in Appendix A.1.

2.1.5 Formation of SiO_2-Shell

A standard PE-CVD process employing silane and nitrous oxide in low pressure conditions at 400 °C was used to cover the NWs with a 20-25 nm thick shell of SiO_2. The PE-CVD process does not result in a homogeneous shell on the NWs as discussed in the results section 3.6.1. Detailed parameters are once again included in the Appendix, A.3.

2.1.6 Flash Lamp Annealing

A FLA system uses pulses of intensive light to heat up a sample to high temperatures within milliseconds. First, the sample is inserted into the vacuum chamber and the chamber is pumped to approximately $1 \cdot 10^{-5}$ mbar. Then the pre-heating is applied to generate free carriers for effective light absorption. After the heating, the capacitors are charged with the appropriate voltage to match the desired energy output. The

annealing process (or flash) itself can be conducted in a noble gas atmosphere or vacuum. The pre-heating is also applied to achieve higher temperatures in the annealing process.

Depending on the sample, the FLA energy was varied between 10 J/cm^2 and the Dresden Thin Film Technology FLA system's maximum of 90 J/cm^2. With materials displaying a low melting point like GaAs NW, usually the pre-heating was only applied with a temperature of 300 °C and the flash energy was lowered considerably. Si-NW display a higher melting point and were therefore pre-heated up to 700 °C in a trial case. Pre-heating was usually applied for a full 10 minutes. Since the sample was placed on top of a thick silicon carbide piece this long heating time was used to achieve a uniform temperature profile. Previous experience by Markus Glaser suggested that 10 minutes should be more than enough for the temperature of the sample to stabilize.

Multiple flashes were also tested for their effect on heterostructured NW. To achieve this, NWs with already deposited Au and SiO_2 shell were deposited on a Si wafer and subsequently flashed multiple times. Two experiments were conducted, the first employing three, the second five flashes. Of about 20 distinctive NW SEM-pictures were recorded before and after each flash, documenting whether certain NW displayed heterostructures after the FLA process. Also, after the very first flashing process, NWs with segments were identified to guarantee observation of segment evolution under the conditions, in case the previously identified NW wouldn't produce segments. The results of this experiment will be covered in section 3.6.2.

2.2 Sample Preparation for Analytics

After synthesis, the NWs needed to be prepared for further analytics. This meant either directly starting a SEM inspection to check if the synthesis had worked involved further processing to enable better imaging in the SEM, like removal of the SiO_2-shell, and/or deposition on a conductive surface like a highly-doped Si wafer or a specialized membrane for TEM analysis.

2.2.1 Removal of the SiO_2 Shell with Etching

As mentioned in 2.1.3, SiO_2 was etched using BHF. To confidently remove the whole shell from the NWs an etching step of 26 seconds was employed. After etching, the sample was rinsed in deionized water and once again dried with dry nitrogen.

2.2.2 Deposition of NWs on Substrate

To enable analytics like electrical measurements or a TEM-analysis, the NWs needed to be removed from their growth substrate and deposited onto a suitable substrate. This was achieved by putting a small piece of the NW sample into isopropanol and

subjecting it to ultrasound to shake off the NWs. The NWs could then be dropcasted onto samples as needed and the leftover isopropanol dried again.

2.2.3 SEM Inspection

SEM inspection was performed using a Zeiss Neon 40EsB Crossbeam system. The NWs were dropcasted onto a highly doped Si wafer. In some cases it proved to ease viewing the heterostructure when the NWs shell was removed beforehand.

2.2.4 TEM Sample Preparation

To enable TEM inspections, the NWs had to be deposited on a specialized TEM-grid or TEM-membrane. These are small and thin copper plates with holes. For TEM measurements only very thin samples can be imaged. So the holes in the copper plates are covered by membranes or carbon fibres to allow the structures to adhere to the sample at a position where the copper does not interfere with the TEM measurement. This was achieved, as usual, by dropcasting them onto said membrane. In this case we used copper-grids with carbon fibres to which the NWs would stick. A view of such a sample can be seen in Figure 17.

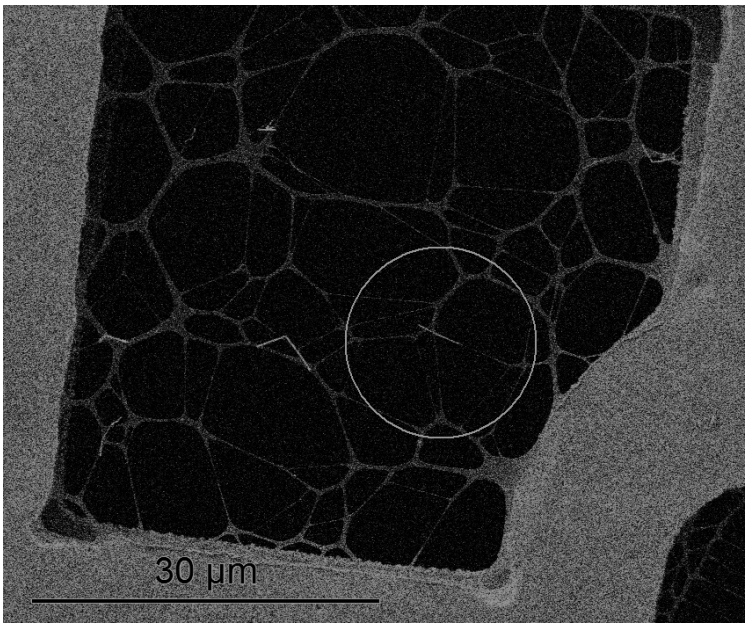


Figure 17. SEM image of a copper TEM-grid with carbon fibres. NW can be seen sticking to the fibres, one of them is indicated by a circle

TEM and related measurements like EDX (energy-dispersive X-ray spectroscopy) and EELS (Electron energy loss spectroscopy) for element analytics and diffractometry for crystallographic analysis were performed at the USTEM at the Technical University Vienna by Prof. Michael Stöger-Pollach and at our partner research group at the NEEL Institute, Grenoble.

2.3 Electrical Characterization of Metal-Semiconductor-Metal NW Heterostructures

Dedicated measurement devices had to be manufactured in order to enable electrical characterization of the NWs heterostructures. Thus mainly 4-point and back-gated FET measurement devices were manufactured to enable characterization.

2.3.1 Fabrication of Electronic Measurement Substrate and Electron Beam Lithography for Structure Contacting

The basic structure for common electrical characterization is based on a highly p-doped substrate with a 100 nm thick layer of SiO_2. Two lithography steps were employed to manufacture measurement devices for the segmented heterostructures. An overview of the testing device structure can be seen in Figure 18.

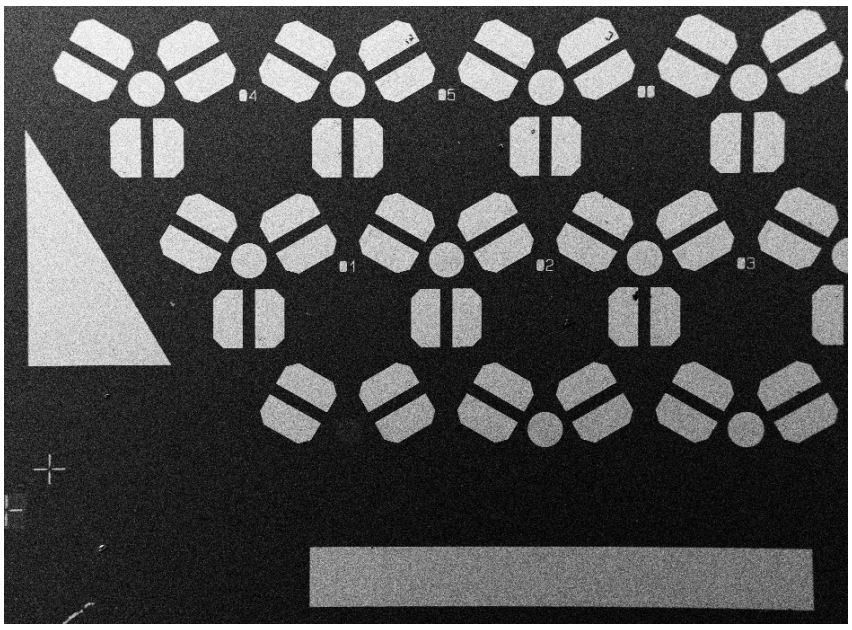


Figure 18. SEM-image of the electronic testing device. The small polygonal pads lie atop the SiO_2 layer, the circular pads directly on the Si allowing back-gated measurements. Around the outside bigger back-gated pads are visible (big triangle & rectangle).

There are a number of metallic pads that either lie on the top layer of the wafer (small polygonal pads) or are etched through to the pure conducting Si substrate below the SiO_2 to allow for back-gated measurements (circular pads). All in all, 19 fields are available in between the final contacts for the NWs to be patterned by electron beam lithography. The metal contact lines were then evaporated and a lift-off process was employed using acetone.

The process for manufacturing a testing device is summarised in Figure 19. First, the Si wafer piece used as a testing substrate has to be cleaved into an appropriate size and cleaned. Then the resist is spinned and dried. Next, in the first optical lithography step, the back-gated contacts are manufactured and etched. Development of

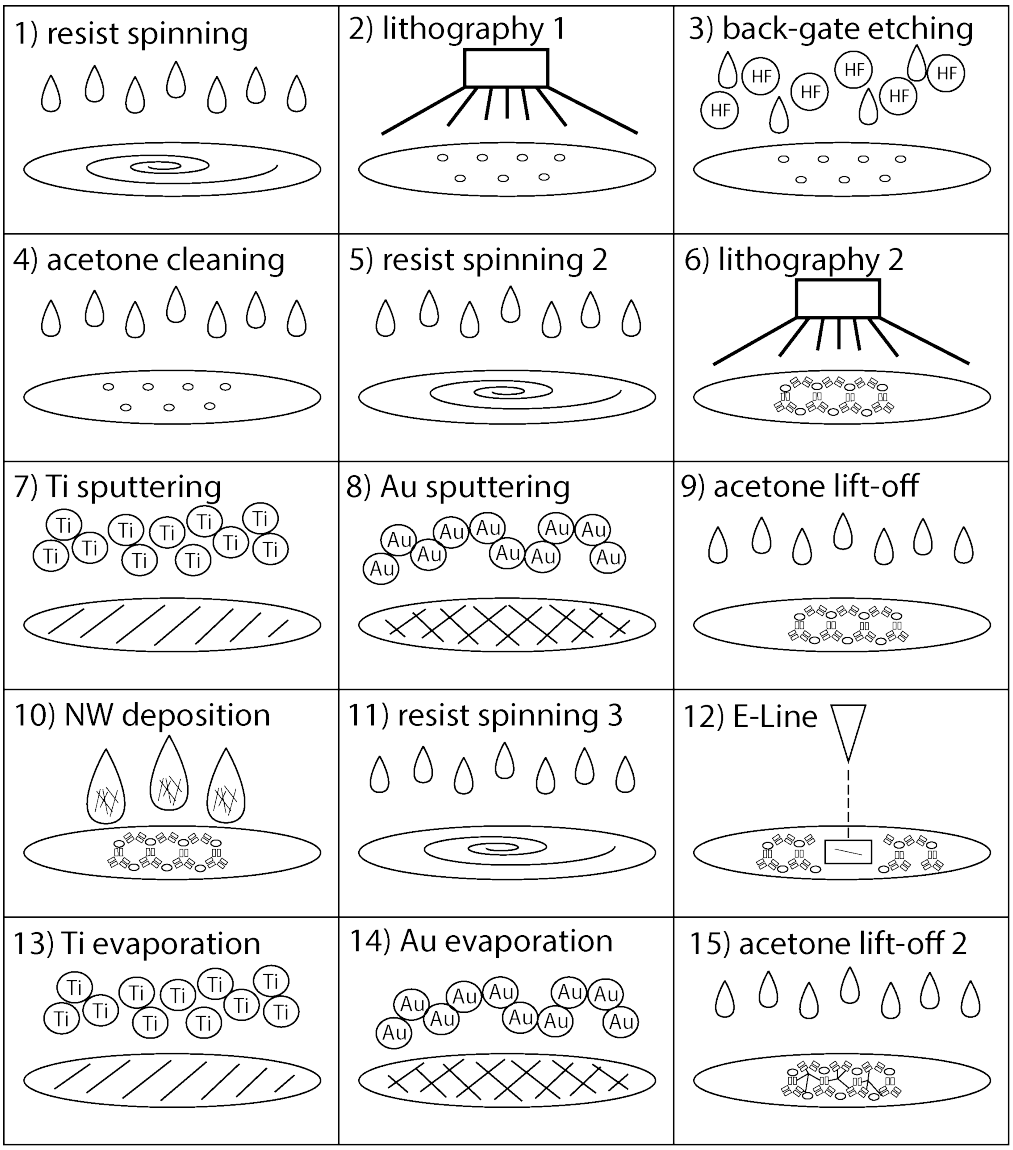


Figure 19. Schematic of the steps necessary to manufacture a electronic testing device for NW heterostructures, from the first lithography step to the last lift-off after electron beam lithography

the resist after lithographic exposure is not shown in the schematic. The resist is then removed with acetone. The second optical lithography step is used to manufacture the top contacts, which lie on top of the SiO_2-layer. Following development, a 5 nm adhesion layer of Ti and a 120 nm layer of Au is sputtered onto the sample. The lift-off is achieved via the use of acetone. Next, the NW are deposited onto the sample via dropcasting. The electron beam lithography resist is spinned onto the sample. Suitable NW for contacting may be located prior to this step via SEM imaging. After resist spinning the NW are contacted via electron beam lithography. The first step in this process is the alignment in the E-Line system, next another 5 nm adhesion layer of Ti is evaporated onto the sample followed by 170 nm of Au. The last step is the second lift-off using acetone.

The reason for the electron lithography contacts to be evaporated instead of sputtered is the size of the lines and contact gaps. Gaps down to 200 nm and line widths down to 300 nm were employed to enable 4-point measurements on the NWs heterostructure. At these dimensions sputtering becomes infeasible due strong adhesion. Typically the acetone-lift-off fails and large junks of Au still cover the NW and its contacts.

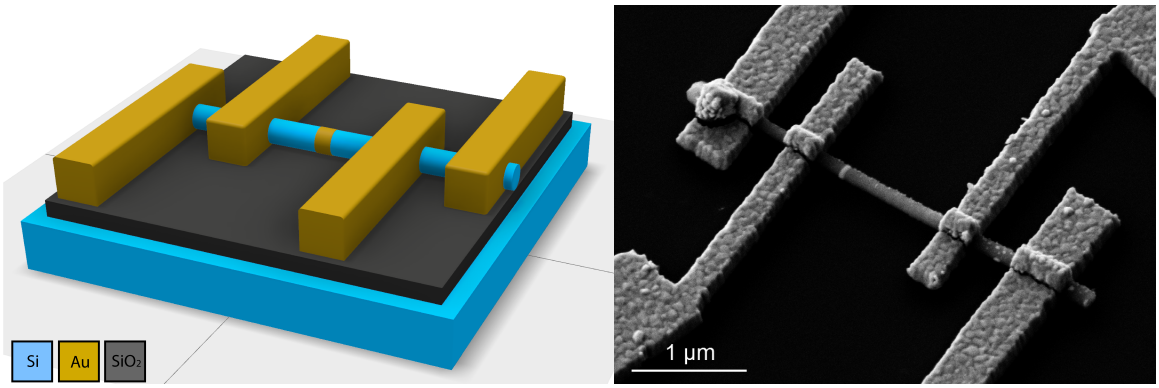
2.3.2 Contact Evaporation

For Si-NW heterostructures (Si-Au or Si-NiSi NW heterostructures) the contacts evaporated after electron lithography were made up of Ti and Au. The first layer was 5 nm thick (Ti), which was used as the bonding agent to make the Au adhere to the substrate. The second layer was pure Au with a thickness in the range of the NW diameters, usually this meant a 170 nm layer of Au.

For the GaAs-NW a different approach was necessary due to the instability of GaAs contacts. A structure consisting of 4 layers was used as suggested by Christoffersen et al [45]. The layers consist of a Ti-Pt-Ti-Au, the Au making up the bulk of the covering. There was only one sample where this approach was employed. The used layer thicknesses were 10-5-10-150 nm respectively.

2.3.3 Four Point Measurements

To enable proper electrical characterization of the NW structure, 4-point-measurement devices were manufactured as detailed in the previous section. Figure 20a shows a schematic and Figure 20b an actual SEM-picture of a contacted NW with a segment.



(a) Schematic of a 4-point measurement device

(b) SEM-picture (at 30 ° tilt) of a Si-Au NW heterostructure integrated into a 4-point measurement device

Figure 20. Schematic (a) and SEM-picture (b) of a 4-point measurement device with integrated Si-Au NW heterostructure

Voltage-Current Characteristic

To measure the voltage-current characteristic in a four-point measurement setup, the inner contacts are set to zero-current-mode and the outer contacts are cycled

through the desired voltages - usually one end at ground, the other varying from -2 V to 2 V. The ratio of current through the outer contacts and the voltage difference between the inner ones accurately reveal device resistance. Resistivity can then be approximated using Equation 1.2. It is expected for the metal segment to have negligible resistivity when compared with the semiconducting NW. Therefore the length of the segment was subtracted from the total measured length that was plugged into equation 1.2.

Transfer Characteristic

The transfer characteristic was measured by using three source voltages (-2 V, 0 V, +2 V) and by varying the gate voltage continuously from -15 V to +15 V. The drain current was then plotted over the gate voltage. The transfer characteristic was recorded in 2-point measurements.

2.4 Raman Measurements

The phononic properties of the heterostructured Si-Au and GaAs-Au NW were measured using Raman spectroscopy. The used system was a confocal µ-Raman setup Alpha300 of the WITec company, with a frequency-doubled Nd:YAG laser emitting linearly polarized light at 532 nm at 100 µW with a spot size of 720 nm. The used object lens for finding the NWs on the sample was a Nikon EPI EPlan 100x objective (NA 0.9, WD 0.23).

2.4.1 Sample Preparation

Raman measurements were performed on two different structures NW heterostructures (Si-Au and GaAs-Au NW heterostructures) as well as their as-grown and no-segment counterparts. For both Si-Au as well as GaAs-Au, the PE-CVD oxide was removed before the Raman measurements via a 26 second BHF-etching step. The Si-NW with Au segments (Si-Au NW) were dropcasted onto a GaAs wafer piece. For GaAs the sample that was also used for electrical characterization was used, where the GaAs-NWs with Au segments (GaAs-Au NW) were dropcasted onto a Si wafer piece.

CHAPTER 3

Results and Discussion

This chapter will start off with an overview of the synthesized heterostructures. Then the individual material systems are covered independently. The Si-Au and GaAs-Au material systems were emphasized, with detailed morphological studies, chemical composition and crystal structures along with electrical and Raman measurements. Si-NiSi was also measured electrically. In case of Si-Sn, the elemental composition and morphology was confirmed. The penultimate chapter will focus on some general observations about the structure synthesis and the last chapter will showcase some trials where other material combinations were tested for viability using the same synthesis method.

3.1 Overview of Synthesized Structures

A variety of materials was experimentally tested for viability using the heterostructure synthesis method described in the previous chapter (see p.29). In Table 3.1 the synthesized NW heterostructures with confirmed composition along with the used deposition method are summarized. Other material combinations were also attempted. In section 3.7 these material combinations are described.

NW material	deposited material	resulting structure
Si	Au (sputtered)	Si with Au-segments
Si	Ni (sputtered)	Si with NiSi-segments
Si	Sn (implanted)	Si with SnAu-segments
GaAs	Au (sputtered)	GaAs with Au-segments

Table 3.1. overview of the material combinations used for the synthesis of NW heterostructures

3.2 Si-Au NW Heterostructures

When synthesizing Si-Au NW heterostructures, the Au catalyst from the VLS process was usually *not* removed. Finding a segmented NW during SEM inspection of a processed sample was usually very easy, with numerous heterostructured NW covering the sample. Judging by the time required after deposition on hexpads to find

suitable structures, probably 5 to 10% and sometimes more NW will be heterostructured after the demonstrated process. More segments are generally less likely, although NW with as much as 10 Au segments have been observed (Figure 21). The deposition method of dropcasting is expected to destroy some heterostructures by breaking them apart at the segment, since NW with segment-shaped material at their ends were frequently observed. Segments appear without a clear preference for position in the NW. They are most often smaller than the NW diameter.

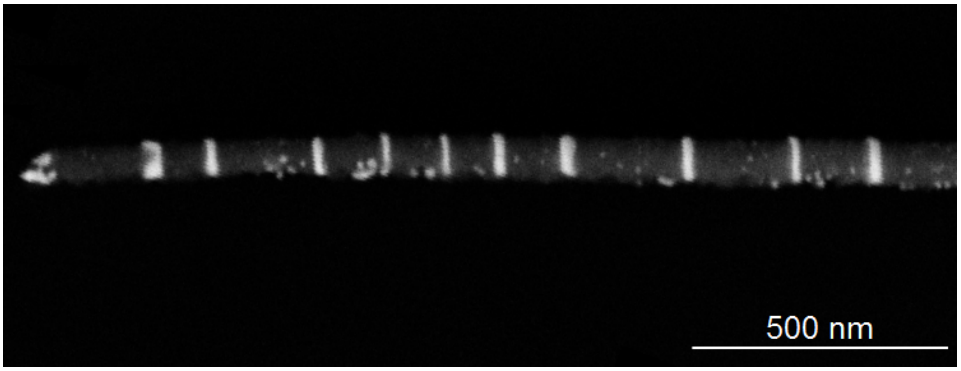
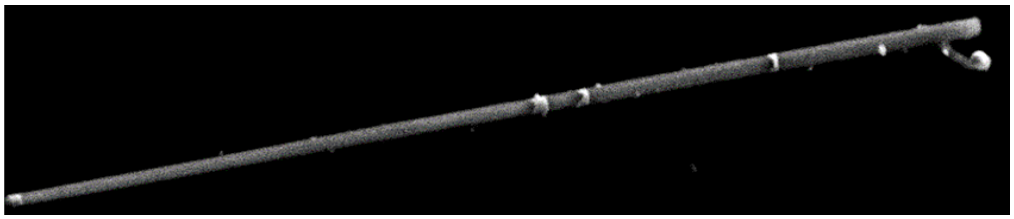


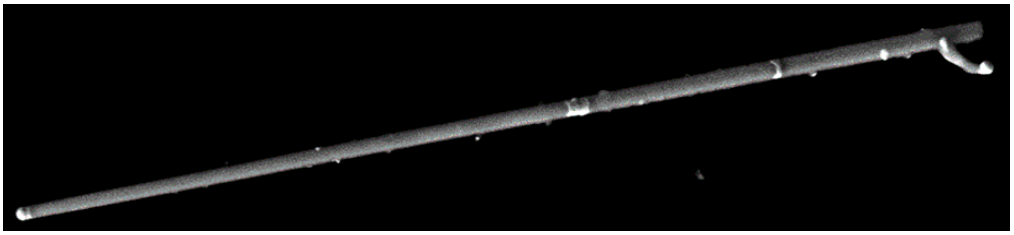
Figure 21. SEM-image of a Si-NW with 10 Au segments on a Si substrate wafer. Some nanoparticles are clearly visible on the NW surface

3.2.1 Mechanism of Heterostructure Synthesis

It is expected that during the FLA process all of the material inside the SiO_2 shell - in case of Si-Au the Si and Au parts - will melt and the shell remain intact. When the temperature starts to decrease again, solid material will build up at some nucleation sites, possibly governed by defects in the SiO_2-shell. The first solid grains are probably made up of Si, since the mixture should have a much larger amount of Si than Au. Therefore the phase diagram predicts for Si to be the first phase to recrystallize into solid form. Only when the eutectic temperature of the Si-Au mixture is reached will the Au crystallize too. This would suggest that the Au segments are already surrounded by solid Si when solidifying. Since there will still be Si in the mixture it is expected for the interface to form at this stage, since Si and Au should separate thoroughly. The reason why the interface is usually straight and perpendicular to the NW surface is not clear up to now. Detailled calculations on the surface energies of the involved phases are required to understand this process in detail. The nanodroplets on the surface of the structure could form by various methods. They might be stabilized by the SiO_2-shell, or there is not enough time during the FLA process for these droplets to agglomerate further than observed. Since a segment requires a significant amount of Au and considering the results of the multiple-FLA processes (next section) this is probably not the case, since diffusion rates in liquids can account for the diffusion distances easily.



(a) Si-Au NW heterostructure after the first FLA process



(b) Si-Au NW heterostructure after the second FLA process

(c) Si-Au NW heterostructure after the third FLA process

Figure 22. Experiment with multiple subsequent FLA processes using Si-Au NW heterostructures. The 3 segments after the first flash (a) merge into two after the second (b) and a single big segment after the third flash(c)

Multiple Flashes

To achieve segments in NW deposited on a flat Si wafer like in this experiment, the flash energy needed to be adjusted. This can be attributed to less scattered light hitting the NW compared with NW on a growth substrate. The NW were damaged rather often when flashed multiple times, resulting in melting, agglomeration into Si blobs or relocation since they couldn't be found at their previous locations on the sample.

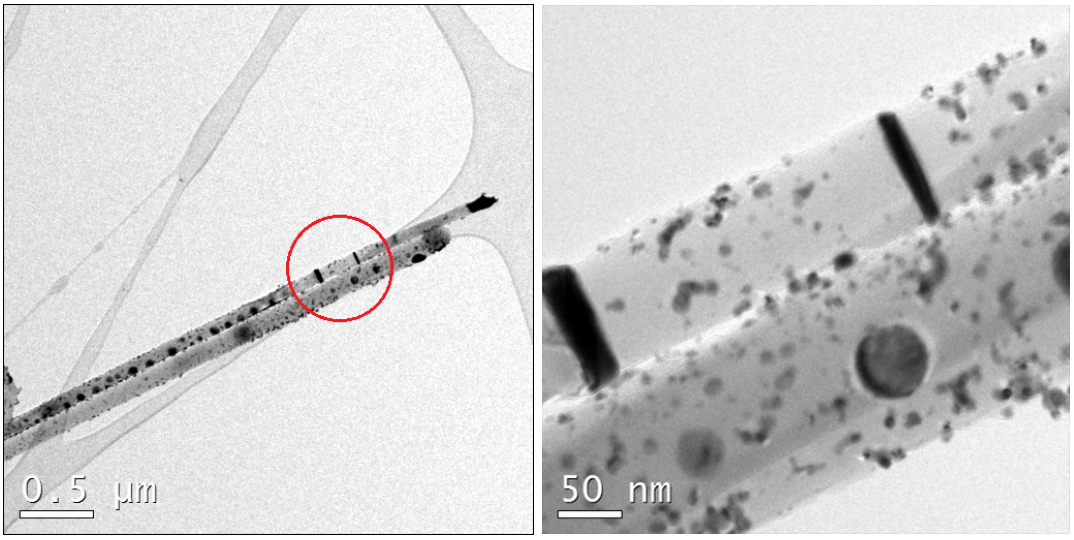
Segments would frequently change their position after a flash. If multiple segments were present at one time, they tended to merge into bigger ones, as demonstrated in Figure 22. This process is called Ostwald ripening, where small droplets of material tend to merge into bigger ones under certain conditions. New segments may appear too after the first flash by way of agglomerating Au from the surface. A splitting of big segments into smaller ones was never observed. It was, however, observed for surface Au on the NW to agglomerate into new segments. (cf. [46])

This experiment demonstrates that the interior of the shell has to melt in order for the observed behaviour to be possible. As previously mentioned, diffusion speeds in solids will generally fall into the range of $10^{-13}\,\frac{m^2}{s}$ or in more practical units for this experiment $10^{-2}\,\frac{\mu m}{100\,ms}$. The flashing process used a 20 ms flash, so the time for the sample to cool again will probably not exceed a second. This would require a much higher diffusion rate for material to be able to move the distances observed in this

experiment. In a liquid the diffusion rates are $10^{-9}\,\frac{m^2}{s}$ or $10^{2}\,\frac{\mu m}{100ms}$ which can easily account for the observed diffusion distance. (cf. [39])

3.2.2 Morphology of Si-Au NW Heterostructures

Figure 23a shows a TEM image of two NWs, one of them with two Au segments with a width of 29 nm and 17 nm respectively. Remarkably, the segments are almost always aligned perpendicular to the NW surface resulting in a perfectly straight and flat metal-semiconductor interface. In the enlarged view in Figure 23b it is obvious that the NW surface is heavily covered in nanodroplets of Au of varying size, some of them only a few nm in diameter.



(a) TEM-image of 2 NW next to each other, location of (b) is indicated by a red circle

(b) TEM view of two Au segments with a width of 29 nm and 17 nm

Figure 23. TEM-images of Si-Au NW heterostructures, (a) overview of the 2 NW, one of them containing two segments, (b) enlarged view of the 2 Au segments (by M. Stöger-Pollach @USTEM)

General Features

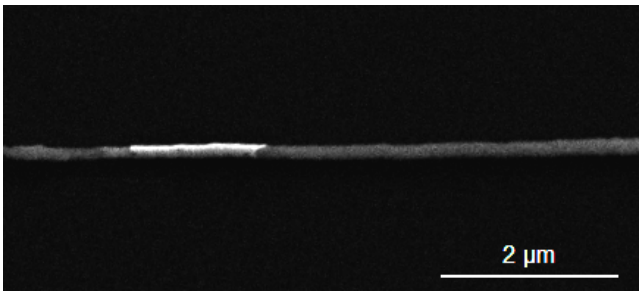
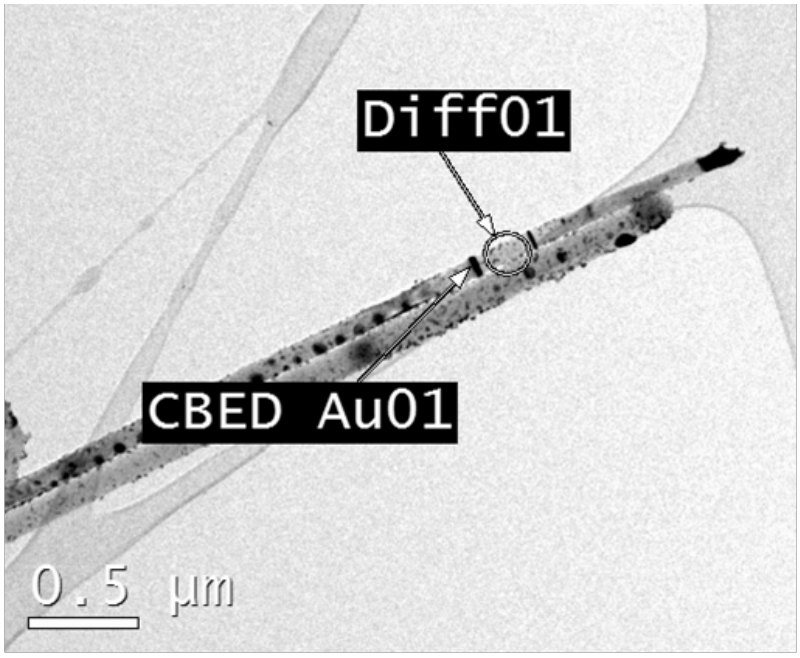


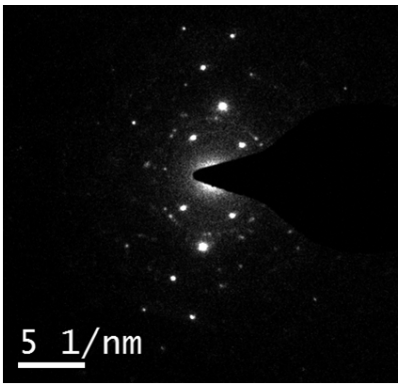
Figure 24. SEM image of a Si-Au structure with a segment length of about 1.5 μm

Segments of all sizes have been observed, the smallest one being just 4,6 nm thick (Figure 27), the largest ranging over a µm (Figure 24). Typical segments were

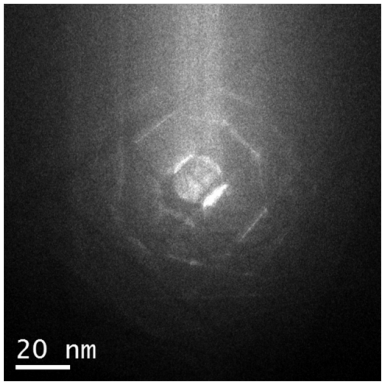
20-100 nm thick for NW with a diameter of 100 nm. It was observed quite often that NW had a Au cap enclosed at their end larger than the expected cap leftover from VLS synthesis. A good example for this is shown in Figure 47 on page 68. The interface at these caps is often not as sharp.



(a) TEM-image of a Si-Au NW with the diffraction spot between the two Au segments indicated, as well as the diffraction spot for on the Au segment (CBED)



(b) Diffraction image of Si between 2 Au segments

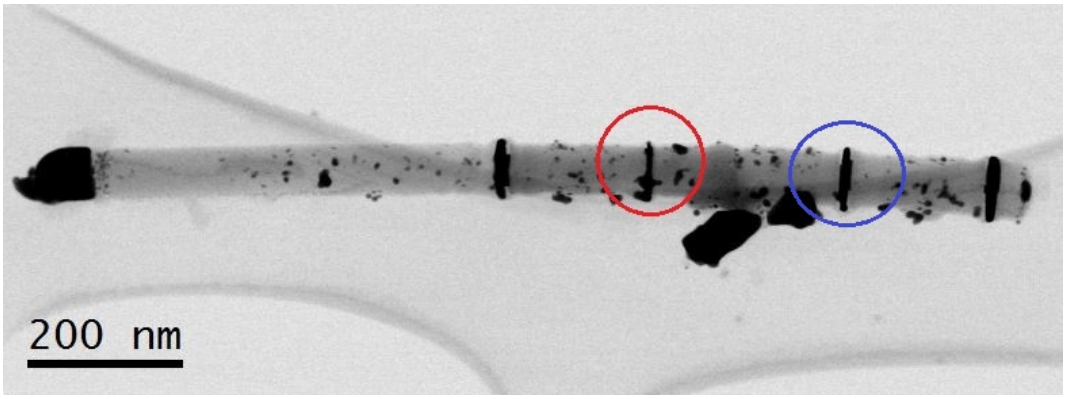


(c) Diffraction image of Au segment

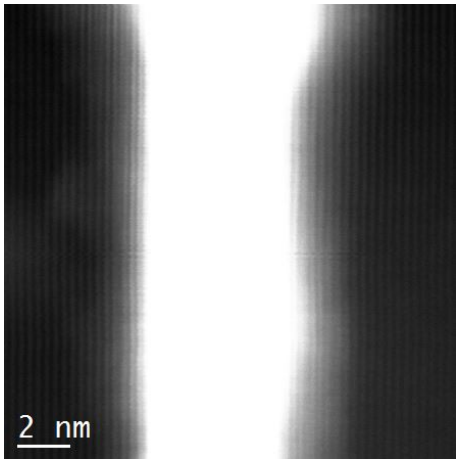
Figure 25. TEM image of Si-Au NW heterostructures with the diffraction spots indicated (a) and diffraction images of Si (b) and Au (d) (by M. Stöger-Pollach @USTEM)

Structure & Element Analysis via TEM

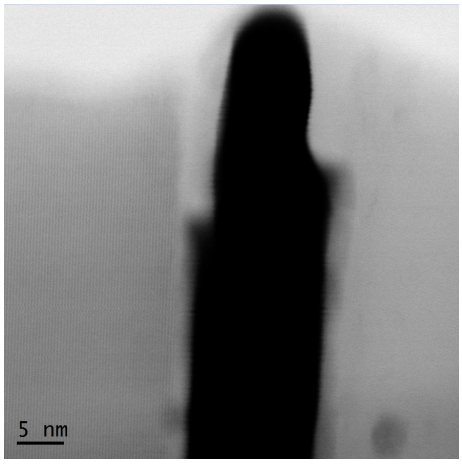
TEM imaging and related analytics revealed several properties of the heterostructure. Figure 23 demonstrates the quality of the Si-Au interface, since it remains looking straight and flat even at the image resolution provided by TEM imaging. Diffraction patterns revealed that the Si and the Au in the segments are crystalline, even when the Si is enclosed between two segments (Figure 25).



(a) TEM of a heterostructured Si-NW with 4 Au Segments, the circles indicate the HR-TEMs in (b) and (c)



(b) HR-TEM red circle, the black part is Si, the white part the Au segment



(c) HR-TEM blue circle, the black part is the Au segment, the white part Si

Figure 26. High resolution TEM images of a Si-Au NW heterostructure. In (a) the position of the other two images indicated by a red (b) and blue (c) circle. (b) and (c) show HR-TEM measurements. (by Luong Minh-Anh, NEEL Institute, Grenoble)

The crystal orientation of the NW is can change across a segment. For example for the NW in Figure 26a, the crystal orientation remains the same across the segment indicated by the red circle (Figure 26b) but changes at the other segment (Figure 26c). The orientation as determined from FFTs of Figure 26b is (111).

The HR-TEM images in Figure 26 show that the interface is not always perfectly sharp and straight. The interface of Figure 26b is quite sharp, possibly down to atomic levels. But the interface of Figure 26c exhibits an in-between layer. The composition of this layer is still unclear, the presence of oxygen and Si points towards amorphous SiO_2. Amorphous Si is also a candidate judging from other measurements at the interface of Si-Au NW.

The surface contaminants often visible under SEM inspection are also clearly visible in the TEM. As expected, these are made up of Au as determined by EELS and can be selectively removed via diluted Aqua Regia wet-chemical etching without removing the segments as well. Though mostly crystalline, the Si sometimes exhibited defects in its crystal structure (Figure 27).

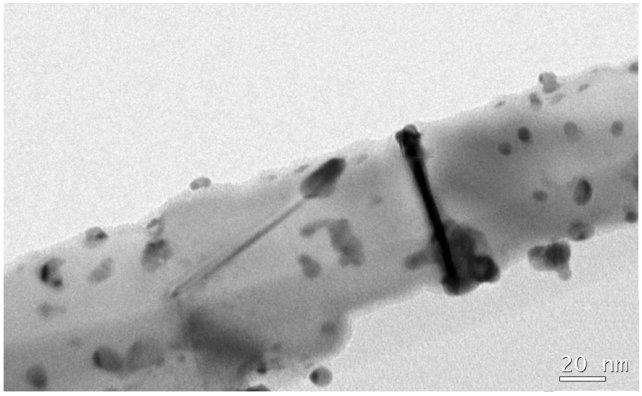


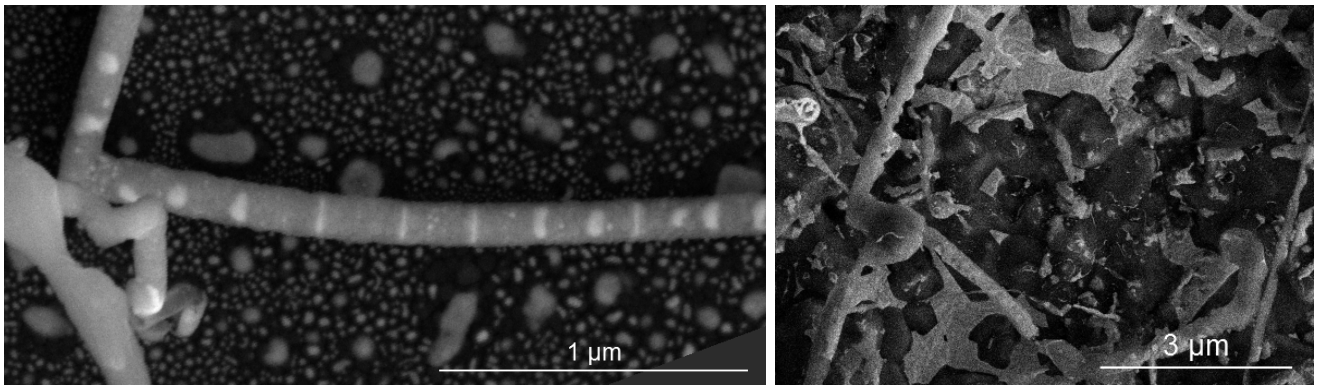
Figure 27. Si-NW with 4,6 nm Au segment, defect in Si is visible next to the segment

Influence of Au Thickness on Heterostructure Yield

The standard Au-thickness used for sputter-coating Au onto Si-NW for Si-Au NW heterostructure synthesis were a Au cover of 3.6 nm. Reducing the layer down to 1.2 nm did not result in any obvious change in gold segment formation as Figure 28a shows. A decrease in the number of segments only became noticeable after removal of the VLS-Au before sputtering and a reduction in layer thickness down to 0.55 nm and 1.65 nm respectively.

A tripling of sputtered material layer thickness of 10.8 nm decreased segment production indirectly since at this and larger Au layer thicknesses, up to 18 nm, the NW were damaged more heavily with increasing Au content, as apparent in Figure 28b. Using a lower flash energy resulted in more Au sticking to the surface of the NW and less segments, though. The melting point of the Si-Au mixture inside the shell would experience a lowering of its melting point when more Au was applied, as obvious from the phase diagram in Figure 10. How this would affect the stability

of the SiO_2 shell is unknown, since the melting point of pure SiO_2 is approximately 1700 °C and should remain unchanged.



(a) NW synthesized with a sputtered Au layer of 1.2 nm **(b)** NW synthesized with a sputtered Au layer of 9 nm

Figure 28. Sputter variations and their influence on segment production in Si-Au NW heterostructures

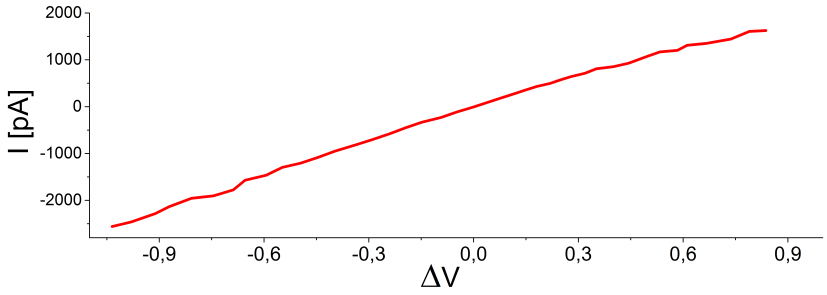
Influence of FLA Energy

The ideal FLA parameters for Si-Au heterostructure synthesis were pre-heating for 10 minutes at 600 °C and a FLA-energy of 64 J/cm^2. Generally, synthesis worked well between 54 J/cm^2 and 84 J/cm^2 with the same pre-heating applied. Even decreasing the flash parameters significantly down to 600 °C / 34 J/cm^2 resulted in the desired segmented structure - although much less segments were found on the sample at these conditions.

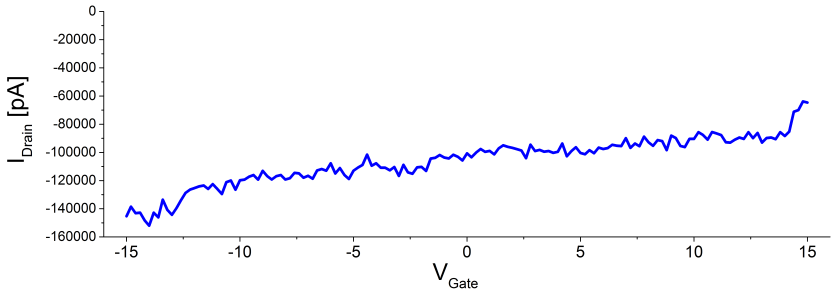
3.2.3 Electrical Properties of Si-Au NW Heterostructures

Several testing devices with heterostructured NW were prepared and characterized electrically. The leakage current to the back-gate ranged from 20 pA to 100 pA. Measurements with currents below 5 pA at 2 V were discarded. Of all fabricated 4-point measurement devices only very few yielded usable data. After rejection of non-sensible datapoints, only two measurements of Si-NW that were prepared the same way as heterostructured Si-Au NW remained, as well as 7 Si-Au NW heterostructures with one Au segment and none with more than one segments. Due to the relatively small number of usable structures and large standard deviations it is hard to make definitive statements on the electronic behaviour of the heterostructures. This should be kept in mind when considering the next paragraph. Two exemplary graphs of measurements are given in Figures 29.

The mean resistivity of Si-NW without Au segments (but processed as the heterostructured Si-Au NWs) was 5,4 Ωm (standard deviation σ = 2,6 Ωm). Si-Au NW heterostructures with 1-segment NW were measured at 3,1 Ωm (σ = 3,8 Ωm). The difference between structures with and without segments is thus negligible. This is unexpected, since a Schottky-barrier should form at each Si-Au interface. In case of a 1-segment heterostructure this would mean two Schottky diodes, one facing



(a) 4-point measurement of voltage-current characteristic of a Si-Au NW heterostructure with 1 segment



(b) 2-point transfer characteristic of a Si-Au NW heterostructure with 1 segment

Figure 29. Exemplary graphs of two measurements on a Si-Au NW heterostructure with 1 segment, (a) 4-point measurement of voltage-current characteristic, (b) 2-point measurement of transfer characteristic

in either direction, one of them always reverse biased when the structure is being measured. The barrier might not form due to the large amount of Au in the semiconductor forming deep impurities at the interface and thereby lowering resistivity of the whole structure. Back-gated measurements revealed almost no gating effect. The maximum observed controllability of the source current was a factor of 10, common values ranged between 2 and 5.

Measurement of as-grown Si-NW were attempted to enable a comparison with Si-Au NW heterostructures. The results, however, did not reflect the expected behaviour of as-grown Si-NW from the literature at all, since the NWs displayed only a small gating characteristic (x100 at the most) and generally only little current passed through the measured NWs.

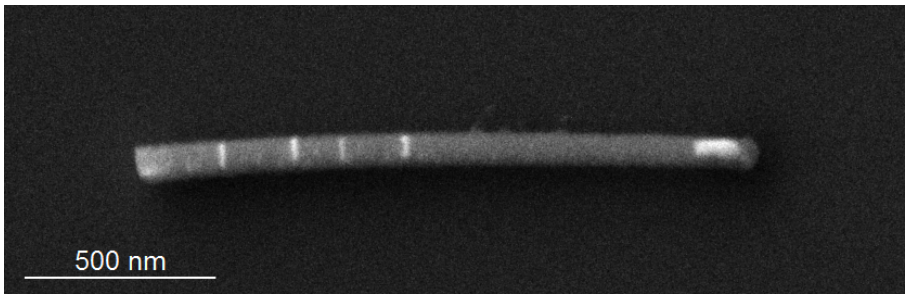
3.2.4 Phononic Properties of Si-Au NW Heterostructures

The phononic properties of Si-Au NW heterostructures, as well as for as-grown Si-NW, Si-NW without segments (but processed like heterostructured Si-Au NW) and bulk Si were measured using Raman spectroscopy. One of the measured Si-Au NW with segments is displayed in Figure 30a. Figure 30b shows the measured raw data. Figure 30c displays the data renormalized to the height of the highest Si-peak at 520 cm^{-1}. It is meant to highlight differences peak position. Figure 30d is renormalized to highlight the Au-edge, with its flank starting at about 150 cm^{-1} and a

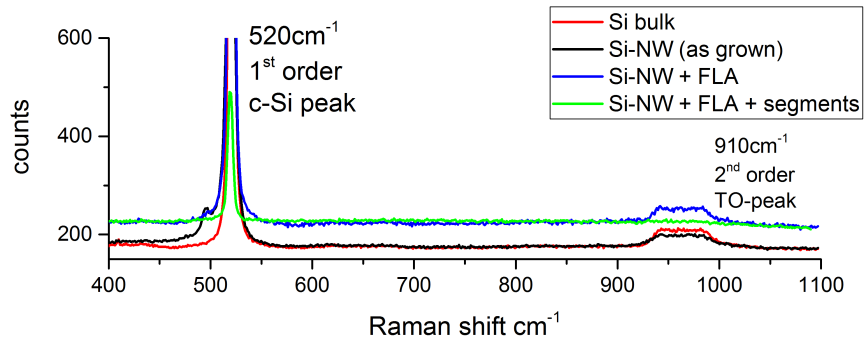
plateau which is reached at roughly 210 cm^{-1}. Not all details that are discussed in the following section can be identified from these Figures alone. Since most data was obtained by performing line scans over the NW, it is not practical to show each and every datapoint separately. The chosen datapoints that are plotted in the Figures are meant to showcase the most prominent features. The GaAs substrate peaks at 268.5 cm^{-1} and 292 cm^{-1} are not shown in these figures.

All measured structures displayed a high crystalline-Si (c-Si) peak at 520 cm^{-1} with usually a full width half maximum (FWHM) between 5 and 6 cm^{-1}. This peak is the first order longitudinal optical (LO) mode of Si. Si-Au NW heterostructures displayed a slightly red-shifted value of this peak in relation to the other measured structures. As-grown Si-NW displayed a slightly larger full width half maximum as well as an even smaller red-shift of the LO peak. Bulk Si of one sample had a FWHM of 11 cm^{-1} though, with a flanked shoulder towards higher values. As mentioned, the as-grown Si-NW display a weak secondary peak at 495.5 cm^{-1}. The feature at roughly 910 cm^{-1} can be identified as the second order transversal optical (TO) Si-peak. It is only present in bulk Si, as-grown Si-NW and at the center of Si-Au NW without segments. At the edges of Si-Au NW without segments this feature disappears, as well as for Si-Au NW with segments. Bulk Si displays a variety of weak peaks, for example at 302 cm^{-1} and 618 cm^{-1}. (cf. [1])

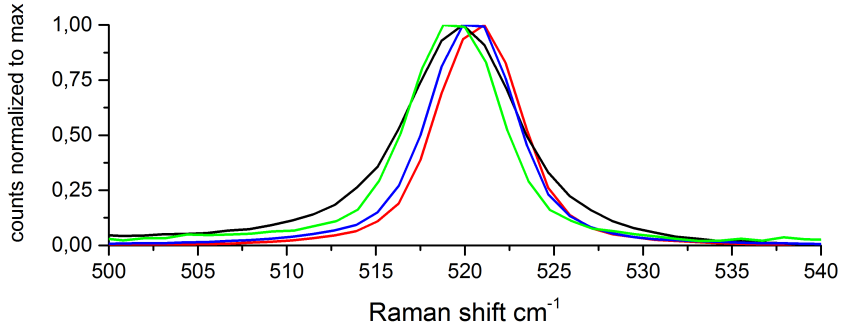
The Au content seems to remain constant along Si-Au NW without segments, since the Au plateau remains rather stable. Along NW with segments, the Au feature is either constant or quite high when on top of the segments. Au end caps like the one visible in Figure 30a do not display equally high Au features, although the measured Au content does increase from the middle of a NW to the end cap. The height of the c-Si peak at 520 cm^{-1} is highest when in-between segments, virtually dwarfing the GaAs substrate peak. In one case the Si peak was especially high at a segment though. When more Au is visible on the surface of the NW, the c-Si peak is significantly smaller. (cf. [47–49])



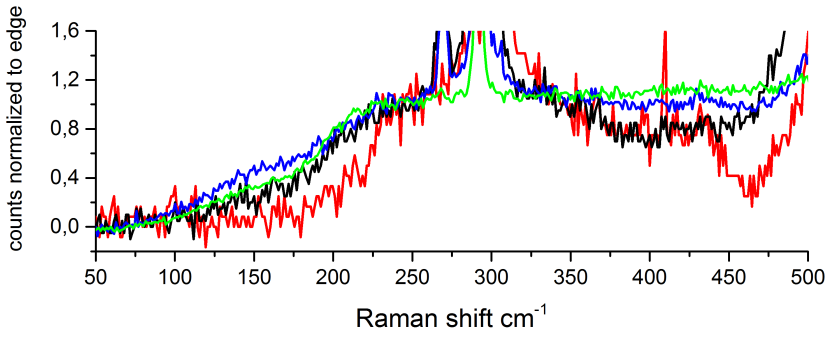
(a) SEM image of Si-Au NW heterostructure used for the Raman measurements



(b) Raman counts, without GaAs substrate



(c) Raman counts normalized to c-Si maximum at 520 cm^{-1} (without substrate)



(d) Raman counts normalized to Au plateau at 250 cm^{-1} (without substrate)

Figure 30. Raman spectroscopy Si-Au NW heterostructures, measured on a GaAs substrate wafer: SEM iamge of measured NW (30a), Raman counts (30b), normalized to maximum value (30c) and normalized to Au-edge value (30d)

3.3 Si-NiSi NW Heterostructures

The material combination of Si with Ni was the only other material system with Si that was thoroughly analysed. Figure 31 showcases a Si-NiSi NW with 7 segments.

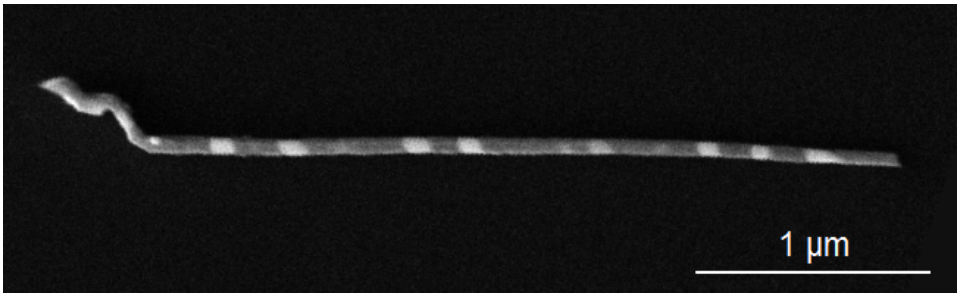


Figure 31. SEM image of a Si-NW with at least 7 NiSi Segments deposited onto a Si substrate wafer

3.3.1 Synthesis of Si-NiSi NW Heterostructures

For Si-NiSi heterostructures, the Au from the VLS synthesis of the Si-NW had to be removed via the process described in 2.1.3 prior to Ni sputter coating. The synthesis properties with respect to the FLA process are similar to the ones described for Si-Au NW. A slightly higher minimum FLA energy was required to produce segments, namely 54 J/cm^2 for NiSi. At 600 °C / 84 J/cm^2 the Si-NiSi NW heterostructures once again displayed melting. As with Si-Au, heterostructured NW are easily found during SEM inspection of a processed Si-NiSi sample. A similar heterostructure production yield of up to 10% is assumed.

Ni Sputtering

For Si-NW with sputtered Ni, reducing the sputtered layer from the 'standard' amount of 2,7 nm to 0,9 nm or lower substantially reduced segment production. At 0,5 nm no segments were found during SEM inspection of the sample. On the other side of the spectrum, when doubling or even tripling the 'standard' amount of sputtered Ni to 5,4 nm and 8,1 nm, no obvious negative influence on segment production was observed.

3.3.2 Morphology of Si-NiSi NW Heterostructures

General Features

Morphologically, NiSi segments appear very similar to Au segments, often with perfectly straight and flat interfaces between the Si and NiSi. Segments also range in size in a similar fashion, although no segments below about 15 nm (Figure 32) have been observed. Again, multi-segmented NW are less likely to occur than single-segmented ones especially when desposited on a substrate. Like with Si-Au, this

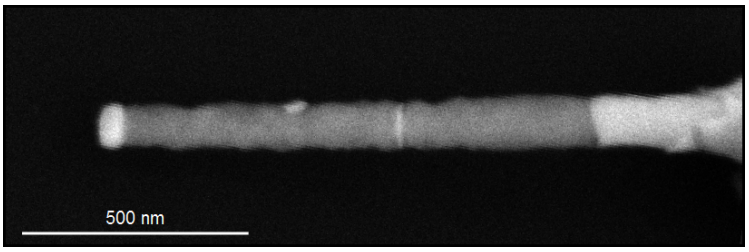


Figure 32. Si-NW with one NiSi segment with a width of about 15 nm (smallest segment observed), deposited on a Si substrate wafer

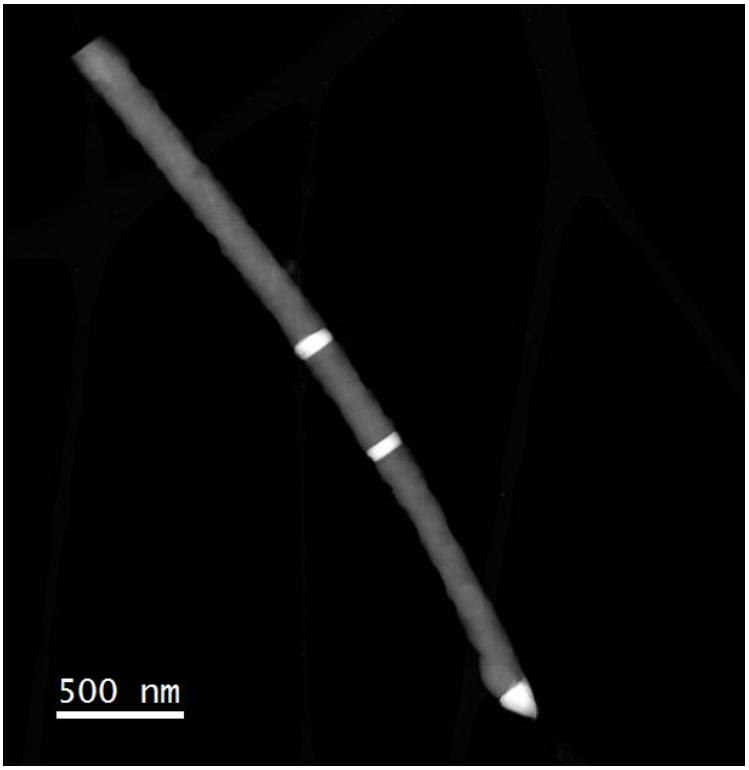


Figure 33. TEM dark field image (DF) of a Si-NW with 2 Ni_xSi_y-alloy segments

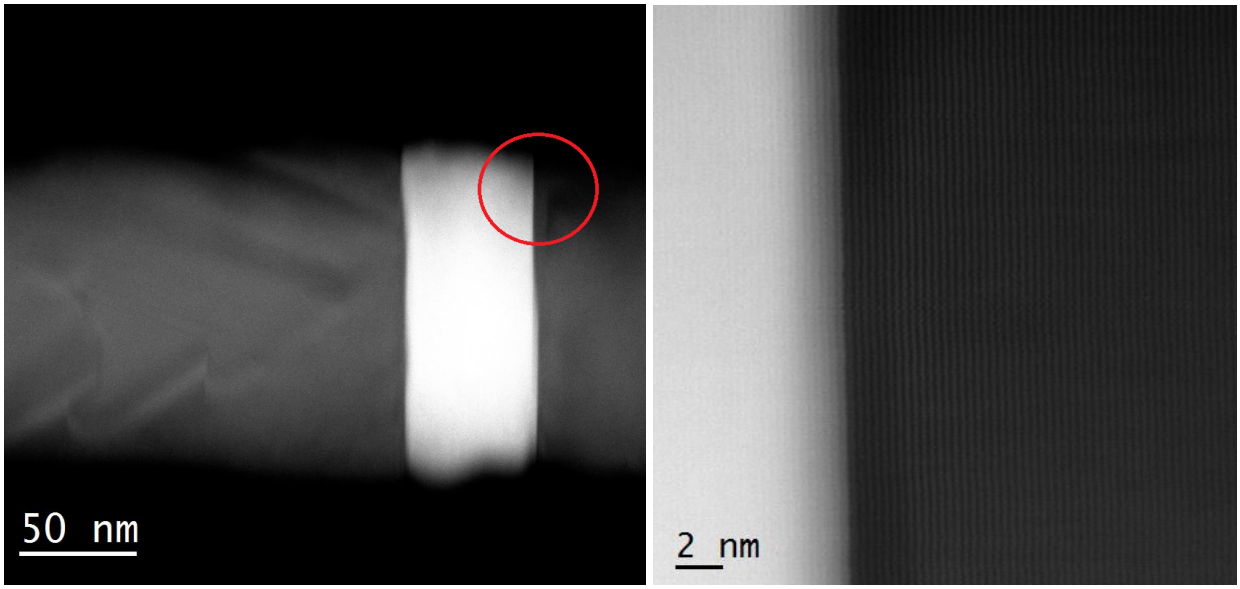
might be due to the deposition method breaking up longer NW with multiple segments.

Structure & Element Analysis via TEM

Element analysis via EDX revealed the segments to be an alloy of Ni and Si, with some Au (around 0.2%) still detectable in the structure. The lattice spacing and EDX analysis points to the segments being made up of the $NiSi_2$-alloy. Since the phase diagram of Si and nickel is very complicated, displaying several potential alloys, it is unlikely that $NiSi_2$ is the only combination present. Similar to Si-Au, caps at the NW endings tended to occur, this time made up of the Si-Ni alloy. One of these caps was specifically analysed and confirmed via EDX to be made of $NiSi_2$. The NW itself remains exclusively made of Si. This is consistent with high concentrations of Si displaying no combinations with nickel in the Si-Ni phase diagram. Between the NiSi-alloy segments, defects may be present in the Si as visible in Figure 34a left

of the segment (the dark shades in the grey Si). The surface of the NW is often covered with droplets of material. These droplets are also made of a Ni-Si-alloy like the segments themselves. An EDX analysis of these surface contaminants show almost equal counts of nickel and Si (Ni:Si at 10:13 so about 56,5% Si in Ni). This matches an eutectic point in their phase diagram indicating an eutectic mixture of the two elements.

The interface between the Si and the alloyed part can be exquisitely sharp. In the HR-TEM image in Figure 34b the atomic planes of Si and the alloy are visibly touching, without any intermediate layer. The atomic planes were measured at 0,32 nm, corresponding to 111-Si. In the HR-TEM image the crystal planes are visibly parallel to the segment and perpendicular to the NW surface. This means the NW is (still) oriented along the 111-plane. A diffraction image on another structure and a different HR-TEM image are in line with this hypothesis, although crystal orientation may change at the defects often present in the NW.



(a) TEM view of a Si-NiSi heterostructure, HR-TEM spot of (b) is indicated, Si is dark, Au is white

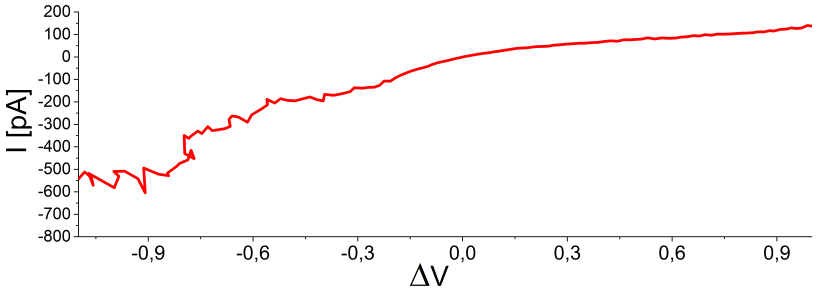
(b) HR-TEM of the interface between Si (right) and the Ni_xSi_y-alloy (left)

Figure 34. TEM image of Si-NiSi NW heterostructures, (a) is a close-up of th lower segment in Figure 33 with the red circle indicating the HR-TEM spot in (b) (by Luong Minh-Anh, NEEL Institute, Grenoble)

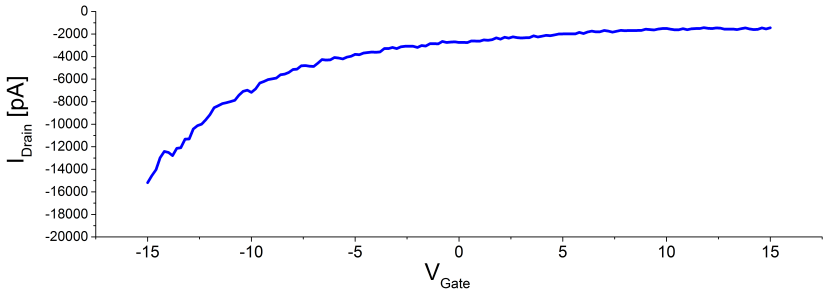
3.3.3 Electrical Properties of Si-NiSi NW

Like for Si-Au, multiple 4-point testing devices were prepared to measure resistivity of Si-NiSi NW heterostructures. The situation for statistics is even worse than for Si-Au structures since only two NW with a single NiSi segment remain after sorting and rejection of datapoints that could not be interpreted sensibly. These two NW demonstrate a mean resistivity value of 34,8 Ωm (σ = 47 Ωm). Exemplary graphs are given in Figure 35. The gating characteristic generally seems to be stronger in Si-NiSi NW heterostructures. Values of up to x1000 have been recorded. This

should be considered with a grain of salt, however, since it is hard to make definitive statements when faced with such data.



(a) 4-point measurement of voltage-current characteristic of a Si-NiSi NW heterostructure with 1 segment



(b) 2-point transfer characteristic of a Si-NiSi NW heterostructure with 1 segment

Figure 35. Exemplary graphs of two measurements on a Si-NiSi NW heterostructure with 1 segment, (a) 4-point measurement of voltage-current characteristic, (b) 2-point measurement of transfer characteristic

3.4 Si-Sn NW Heterostructures

Figure 36 shows a typical Si-Sn heterostructured NW.

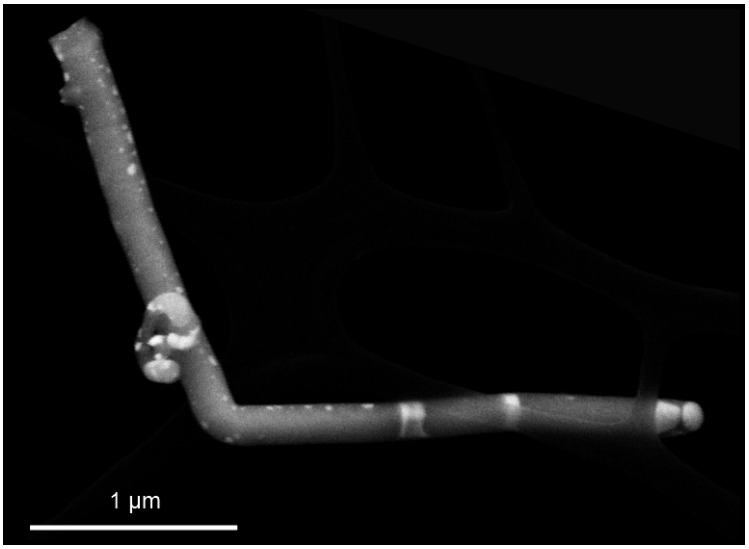


Figure 36. SEM image of a Si-NW with 2 Sn-Au-alloy segments. One segment is obscured by a carbon fibre of the TEM-grid the NW has been deposited onto.

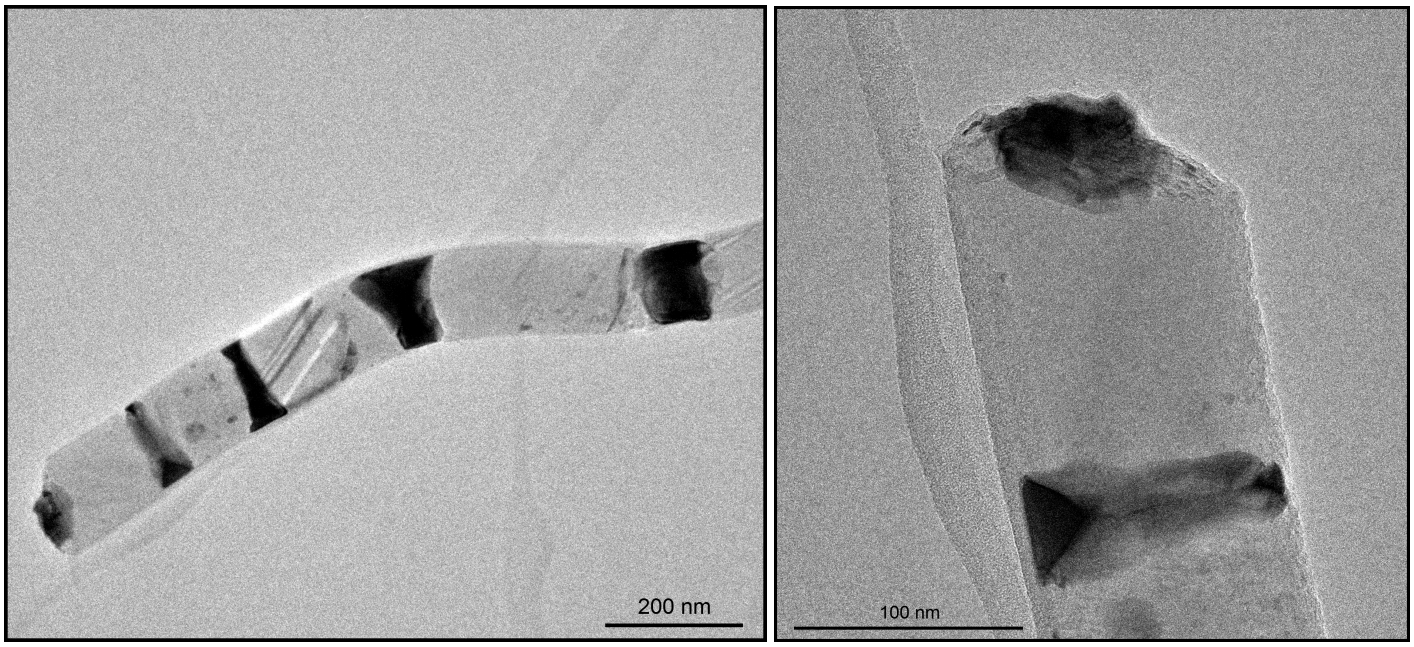
3.4.1 Synthesis of Si-Sn NW Heterostructures

As discussed before, the Sn used for the synthesis of Si-Sn NW heterostructures had to be implanted into the NW to prevent oxidation. The leftover Au was not removed prior to implantation and subsequent processing. Since only one sample was available, this sample was cleaved into two parts and flashed at 600 °C / 84 J/cm^2 and 600 °C / 64 J/cm^2 respectively. 84 J/cm^2 resulted in the melting of all NW structures. This indicates that the stability of the PE-CVD SiO_2-shell depends on the material inside the shell, since with Si-Au the shell was only melted in part at this energy. 64 J/cm^2 resulted in the heterostructured NW.

3.4.2 Morphology of Si-Sn NW Heterostructures

General Features

The interface between the Si part and the Sn segment is not perpendicular to the NW surface as with the other structures, as can be observed in the TEM images in Figure 37. Judging by the TEM images and the Si element mapping in the following section (Figure 38m), the segments do not necessarily go all the way through the wire, the Si in the center of the NW sometimes seems to touch. The interface between the Si and the alloy part remains sharp though, with a confirmed width of under 5 nm. Still, some straight interfaces are present in this structure, not between the Si-NW and the alloy though and this interface cannot be seen under normal SEM or TEM inspection. Only when element mapping comes into play do these interfaces become visible (Figure 38).



(a) TEM view of Si-Sn NW heterostructure **(b)** Enlarged view of the SnAu segments

Figure 37. TEM images of Si-Sn NW heterostructure, (a) overview of a Si-Sn NW with 4 segments, (b) enlarged view of one segment showing the Si possibly touching in the center of the NW (by Luong Minh-Anh, NEEL Institute, Grenoble)

Element Analysis Si-Sn

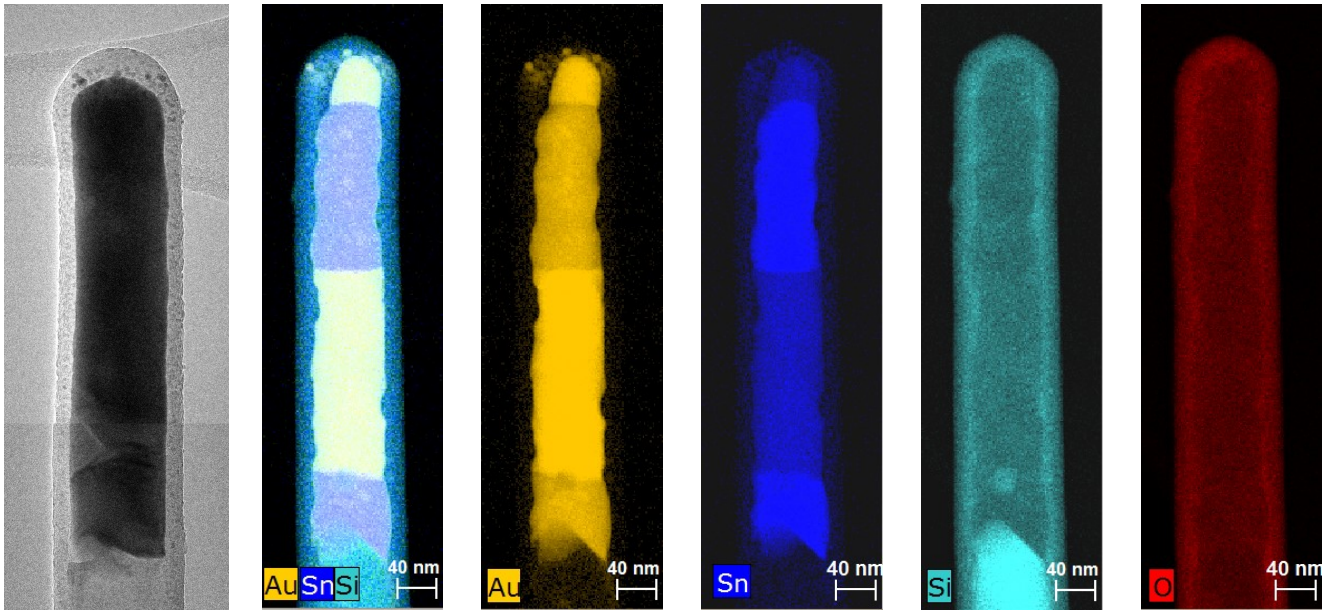
The element maps in Figure 38 reveal interesting properties of the Si-Sn structure. An end cap of a heterostructured NW was thoroughly analysed as well as 3 segments along the same NW. The end cap is made up of two Sn-Au alloys. The maps can be seen in Figures 38a to 38f. In Figure 38g the interface between the two alloys is straight, more so than the interface between the Si-NW and the SnAu-alloy segments in Figures 38h to 38m. Judging by counts, the Au-coloured alloy in Figure 38g is probably the eutectic mixture with 30% Sn in Au while the purple parts are made up of the alloy Sn_2Au with 64% Sn in Au. The interface between the Au-rich and tin-rich regions is also remarkably sharp, with a width smaller than 5 nm.

The segments themselves are probably made of the alloy SnAu, since their EDX counts overlap consistently. The surface of the NW is full of nanoparticles made up of Sn and Au as well. The crystal structure of Si-Sn was not analysed.

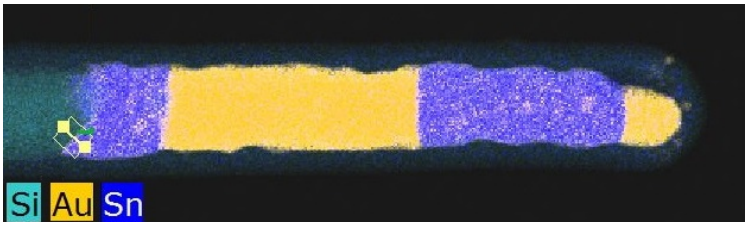
3.5 GaAs-Au NW Heterostructures

3.5.1 Synthesis of GaAs-Au NW Heterostructures

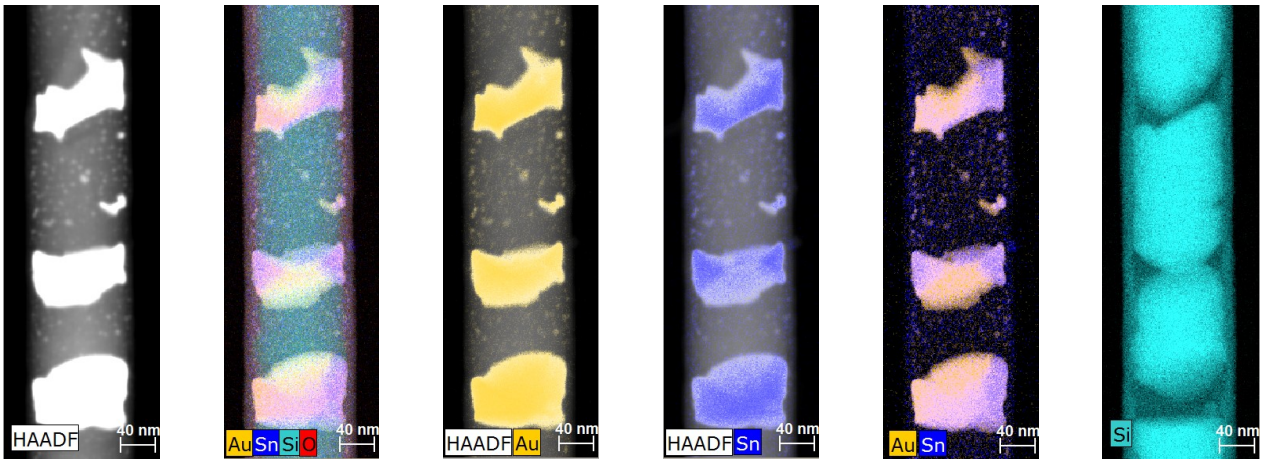
The synthesis of Si-NW heterostructures proved to be remarkably stable when varying the sputtered material. Unless the amounts were altered substantially, normal SEM inspection didn't reveal any significant differences in heterostructure production. Smaller layers of material could lead to less produced segments with both Au and Ni. More material, however, generally did not lead to more or larger segments.



(a) TEM (assembled from 2 images) **(b)** Au, Sn, Si **(c)** Au **(d)** Sn **(e)** Si **(f)** oxygen (O)



(g) enhanced element map of the end cap with (Si,Sn,Au)



(h) TEM darkfield **(i)** Au, Sn, Si, O **(j)** Au **(k)** Sn **(l)** Au, Sn **(m)** Si

Figure 38. EDX element mapping of a Si-Sn NW end cap (top) and three SnAu segments (bottom) (by Luong Minh-Anh, NEEL Institute, Grenoble)

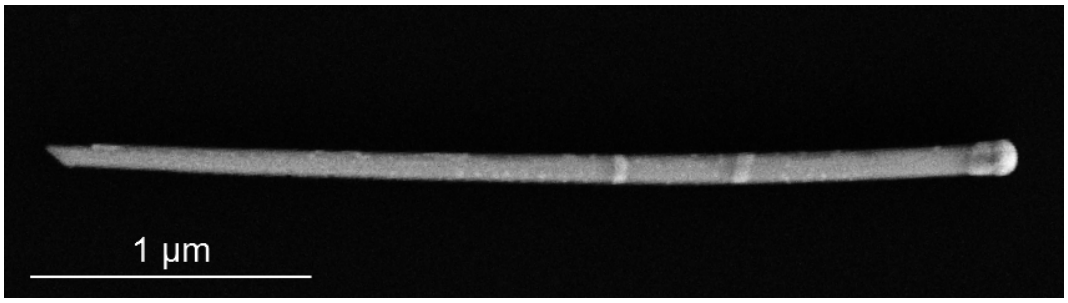
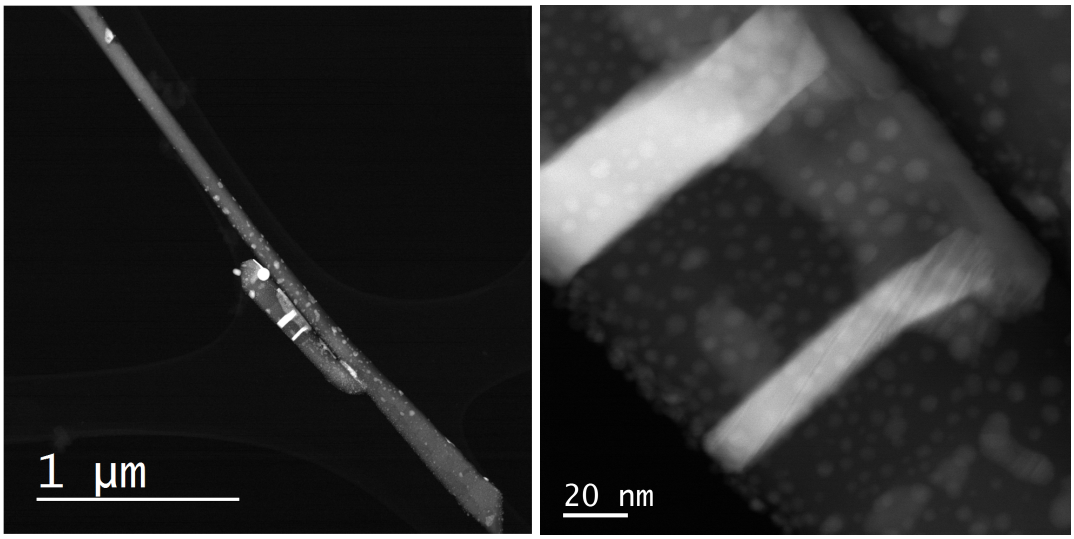


Figure 39. SEM picture of a GaAs with 2 Au-segments deposited onto a Si substrate wafer

When considering the GaAs-Au material system and its phase diagram (Figure 13 on p.23), it seems reasonable to assume that the system would be similarly stable under sputter variations - again unless substantially altering material balances. For this reason the sputter-coated Au layer used for GaAs-Au synthesis was exactly the same as for Si-Au, namely about 3.6 nm. Likewise, the PE-CVD process was also applied using the same parameters as with Si-Au and the other structures, resulting in a 20-25 nm thick SiO_2 shell.

3.5.2 Morphology of GaAs-Au NW Heterostructures



(a) TEM image of two GaAs-NW, one of them containing 2 Au segments

(b) enlarged view of the 2 Au segments of the GaAs-Au NW in (a)

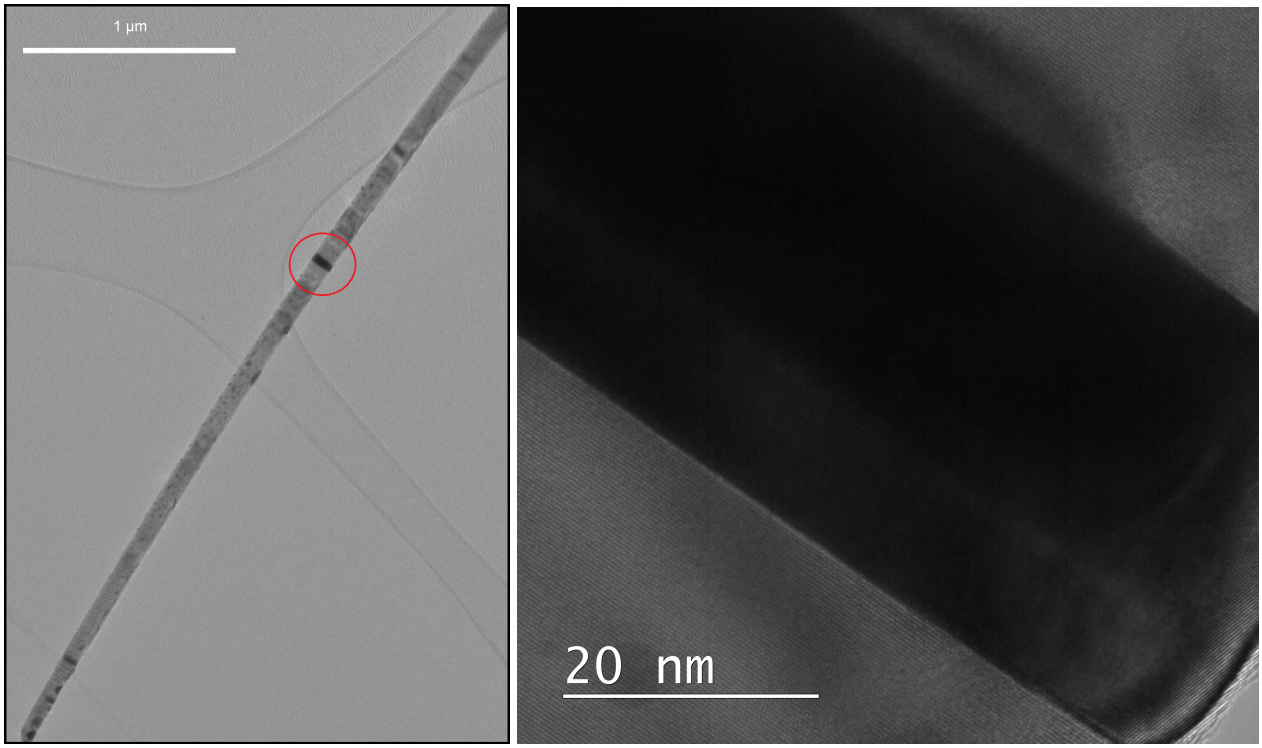
Figure 40. TEM darkfield images of two GaAs-NWs, one of them heterostructured with 2 Au segments (by M. Stöger-Pollach @USTEM)

General Features

The general morphology of the synthesized GaAs-Au heterostructures is very similar to Si-Au and Si-NiSi NW heterostructures. The interface between the NW and the segment is once again straight and perpendicular to the NW surface. The segments

range in size. The smallest one observed (Figure 40b) had a width of 18 nm. No segments bigger than about three times the diameter of the NW were observed. This amounts to about 300 nm in the used NW. Sometimes the segment material forms a cap at the end of the NW, similar to the observed caps in Si-Au, Si-NiSi and Si-Sn. Arguably there is a tendency for the metal component to agglomerate at the end caps even when there is no segment material there in the first place (like with GaAs-Au).

TEM structure analysis of GaAs-Au NW Heterostructures



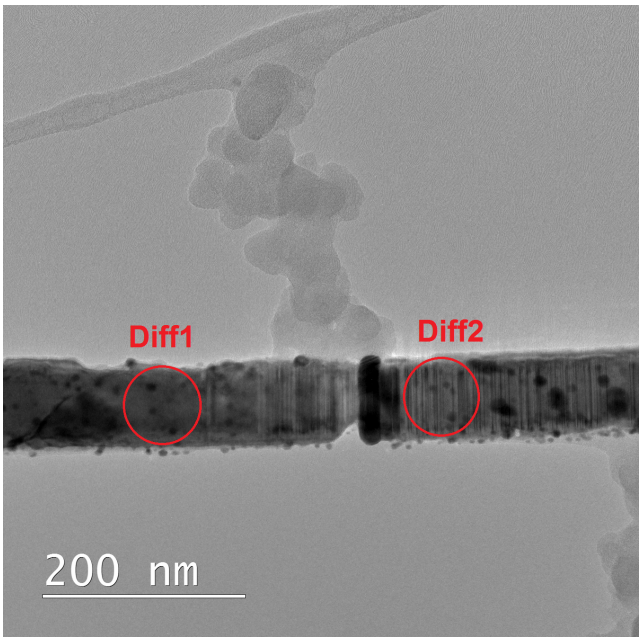
(a) TEM image of GaAs-NWs with a Au segment, HR-TEM spot of (b) is indicated by a red circle

(b) HR-TEM of interface between GaAs (lightly coloured) and Au (dark)

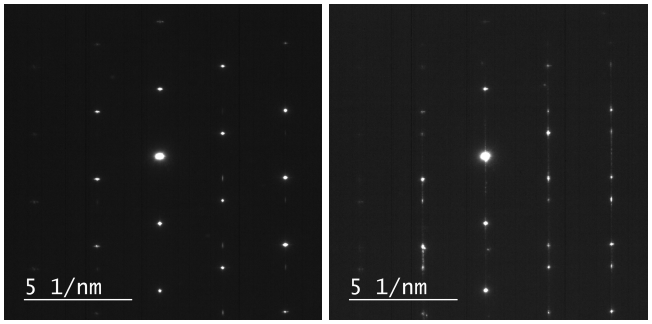
Figure 41. TEM images of GaAs-Au NW heterostructure (by M. Stöger-Pollach @USTEM)

Various structure analysis techniques were used to characterize the GaAs-Au NW heterostructures, chief among them HR-TEM imaging. A HR-TEM image of the interface between GaAs and Au is given in Figure 41b. Once again the atomic planes of GaAs and Au are both clearly visible and touch without any intermediate layer. This is remarkable considering this structure, like the others, forms from a molten mix containing all three participating elements, namely As, Ga and Au.

The GaAs-NW frequently displays twinnings in its crystal structure. Examples are displayed in Figure 43 and Figure 42 on p.62. A diffraction image was recorded at a spot with multiple twinnings, displayed in Figure 42c on p.61. As expected, the image clearly shows a doubling of spots.



(a) TEM overview, diffraction spots are indicated. A small piece of the NW is missing next to the Au segment.



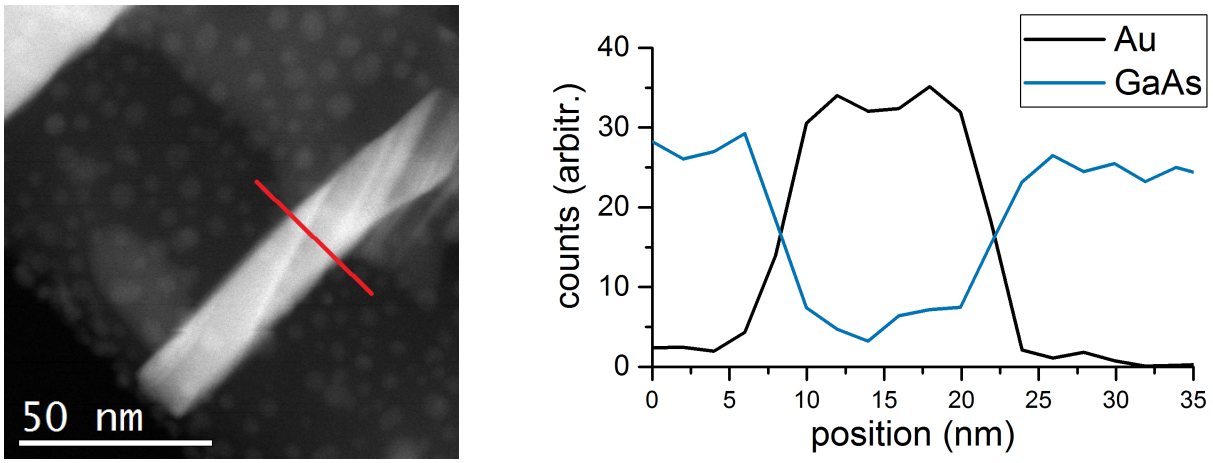
(b) Diff1, no twinnings **(c)** Diff2, with twinnings

Figure 42. Overview and diffraction images of GaAs-Au NW heterostructures (by M. Stöger-Pollach @USTEM)

The crystal structure of the GaAs-Au heterostructure was thoroughly analysed. One example is shown in Figure 42 where two diffraction images were recorded at either side of a Au segment. On both sides the NW is oriented along the (111)-plane. The measurements point to the crystal structure of the NW to be oriented in the (111) direction. Even low-angle grain boundaries which sometimes occur along the GaAs NW are usually twins.

Figure 43. TEM image of two GaAs-NW, the upper with a Au end cap, the other one with a big Au segment. In the upper wire multiple twinnings (small black lines in the NW) are visible (by M. Stöger-Pollach @USTEM)

Element Analysis GaAs-Au NW Heterostructures



(a) TEM image of GaAs-Au NW heterostruc- **(b)** EDX linescan data with the Au and GaAs element mapping
ture used for EDX analysis. An EDX linescan across the measured line
was perfomred, it is indicated by a red line

Figure 44. Element analysis via EDX of GaAs-Au NW heterostructures, (a) TEM image of the used GaAs-Au NW heterostructure, (b) the EDX data with Au and GaAs content (by M. Stöger-Pollach @USTEM)

The element composition of GaAs-Au heterostructures was measured during TEM using EDX. An example of an EDX linescan is given in Figure 44. It confirms that the segment is made of Au and the NW of GaAs. The dark lines in the Au seg-

ment indicate a variation in the Au layer thickness. Like the other synthesized structures, the surface of the NW is covered by small nanodroplets of material. These were also analysed using EDX and confirmed to be Au nanodroplets.

Flash Energy

As expected due to its lower melting point, the required flash energy and pre-heating for the synthesis of GaAs-Au NW heterostructures was significantly lower than for example Si-Au. At a temperature of 300 °C and a flash energy of 30 J/cm^2 the first segments appeared, at 300 °C / 40 J/cm^2 the structures were already clearly melting once again demonstrating that the stability of the SiO_2-shell depends on the NW core material. Below 30 J/cm^2 no segments could be observed.

As with Si-Au, when the proper parameters were applied synthesis of GaAs-Au worked very well. The heterostructure yield is expected to be even higher than for Si-Au, possibly greater than 30%, at least when considering single-segmented structures. Multi-segmented GaAs-Au structures were much less common than for any other of the investigated structures.

3.5.3 Electrical Properties of GaAs-Au NW Heterostructures

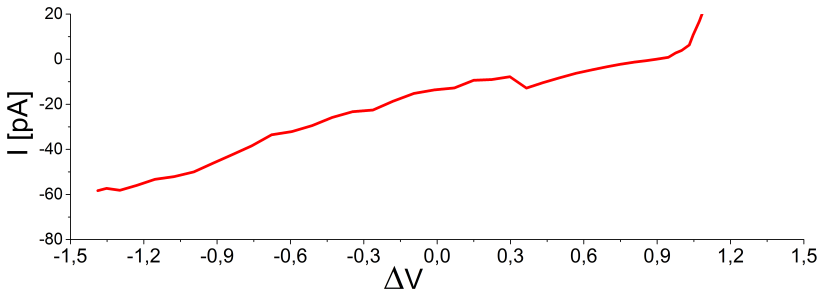


Figure 45. Exemplary graph, 4-point measurement of voltage-current characteristic of a GaAs-Au NW heterostructure with 1 segment

One 4-point testing device with GaAs-Au NW heterostructures was prepared for electrical characterization. Once again the measurements did not yield the desired results as a lot of structures displayed very high gate currents indicating leakage. The measured values would vary rather strongly even if no leakage was detected, making it difficult to give definitive statements on the structure's electronic properties. The remaining number after rejection of all data points that didn't make sense was very small, yielding only 5 GaAs-NW without segments (but prepared like the heterostructured ones). Three GaAs-Au NW heterostructures with 1-segment were left and a single one with 2 segments. The GaAs-NW without segments displayed a mean resistivity of 570 Ωm (σ = 580 Ωm). The single segment structures were measured at a mean resistivity of about 2600 Ωm (σ = 3700 Ωm) and the 2-segment structure at about 900 Ωm. These numbers are far from any values enabling proper characterization.

3.5.4 Phononic Properties of GaAs-Au NW Heterostructures

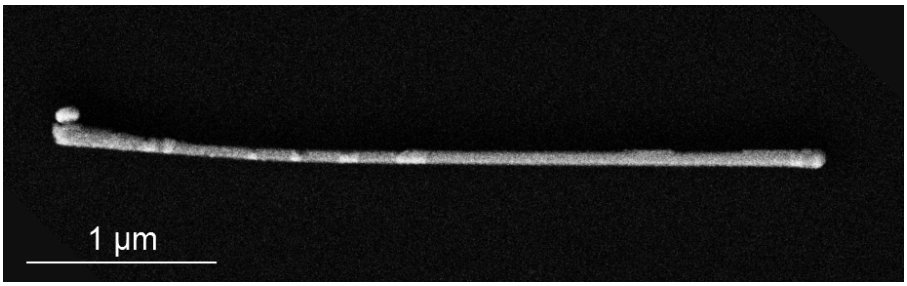
Like for Si-Au, the phononic properties of GaAs-Au heterostructures and, as with Si-Au, of bulk GaAs, as-grown GaAs-NW and GaAs-Au NW without segments, were measured using Raman spectroscopy. Figure 46 once again contains a SEM image of a measured NW along with figures of chosen data points from line scans across multiple sample NW. Figures 46c and 46d again contain the normalized versions of Figure 46b, to a maximum peak or the Au plateau respectively. Since bulk GaAs didn't display a Au plateau it was removed from Figure 46d. As expected, the main Si substrate peak was measured at 520 cm^{-1}. It is not shown in these figures. None of the prominent features in the figures can be attributed to the presence of the Si-substrate.

Bulk GaAs displays two prominent peaks at 268.5 cm^{-1} and 292 cm^{-1} with FWHM of about 6 cm^{-1}. The peak at 268.5 cm^{-1} is the GaAs transveral-optical (TO) peak, the one at 292 cm^{-1} the GaAs longitudinal-optical (LO) peak. The same peaks are present in as-grown GaAs-NW, GaAs-Au NW with and without segments but their intensity proportions are reversed. The proportion of the peaks themselves varies between structures. This is especially obvious in Figure 46c. In GaAs-NW without segments, the TO-peak is proportionally much smaller at the end of the NW. At the same time the LO peak hardly changes. At segments in GaAs-Au NW heterostructures, the same behaviour can be observed. The proportion of the TO to the LO peak is smallest for GaAs-Au NW with segments. For as-grown GaAs-NW, GaAs-Au NWs with and without segments the LO-peak falls to 289 cm^{-1} with a FWHM between 5 and 8 cm^{-1}, more closely resembling the expected behaviour when compared to values from the literature.

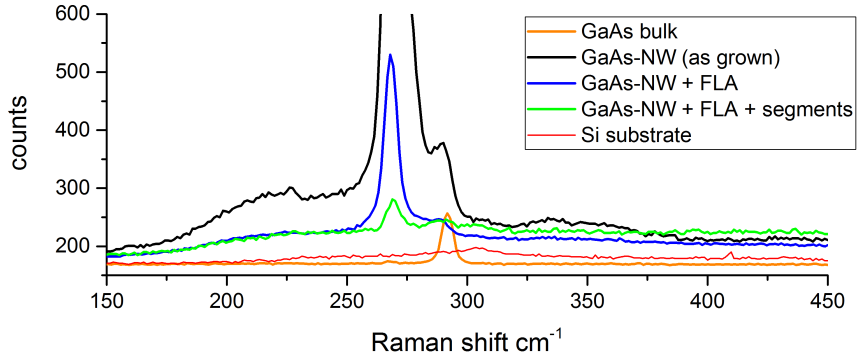
The two GaAs peaks, TO and LO, indicate the polar nature of the GaAs crystal. The TO peak is generated when back-scattering occurs from the (110) and (111) surfaces. The LO peak on the other hand occurs when backscattering from the (100) and (111) surfaces occurs. This means that in bulk GaAs hardly any backscattering occurs from the (110) and (111) surfaces since the TO peak is weak, while at the same time backscattering from the (100) and (111) surfaces is strong. This also means that the (111) surface cannot dominate the peak height because backscattering from this surface would lead to both peaks being more pronounced. In as-grown NW the reverse situation is present, with strong backscattering from the (110) and (111) surfaces. Once again the (110) surface has to dominate here or the (111) surface would result in a higher LO peak. GaAs-Au NW heterostructures display the same properties like as-grown GaAs-NW, although the backscattering from the (110) surfaces are less pronounced. GaAs-NW that were prepared like GaAs-Au NW heterostructures but did not display segments fall in between as-grown GaAs-NW and segmented ones in terms of peak intensity. (cf. [50])

When present, like in GaAs-Au NW with and without segments, the Au plateau feature at $> 210\,cm^{-1}$ is usually constant and doesn't change significantly over the length of the NW. In one measurement, though, it was much more pronounced ex-

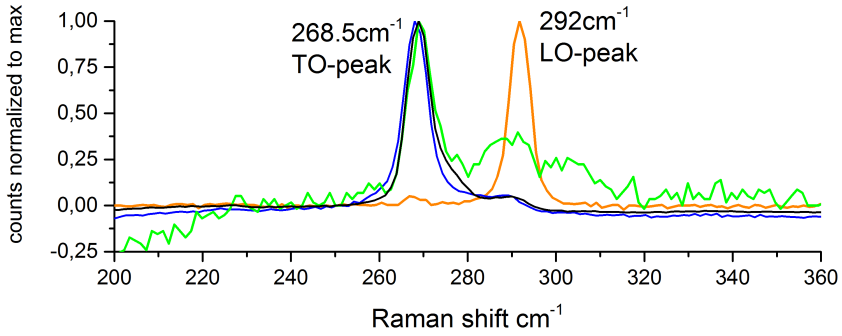
actly at the double-segment structure visible on the left-hand side of Figure 46a. This enhancement was larger than the end-point measurement, where a Au droplet can be seen next to the NW. The relatively large Au segments of this NW are both at about 45 nm, with the NW diameter at 60 nm. The Au content of the end cap together with the Au droplet next to the NW should still contain larger amounts of Au, though, resulting in a bigger Au signal. GaAs-Au NW with segments display a slight increase in the Au plateau at values beyond the GaAs LO and TO peaks. (cf. [51, 52])



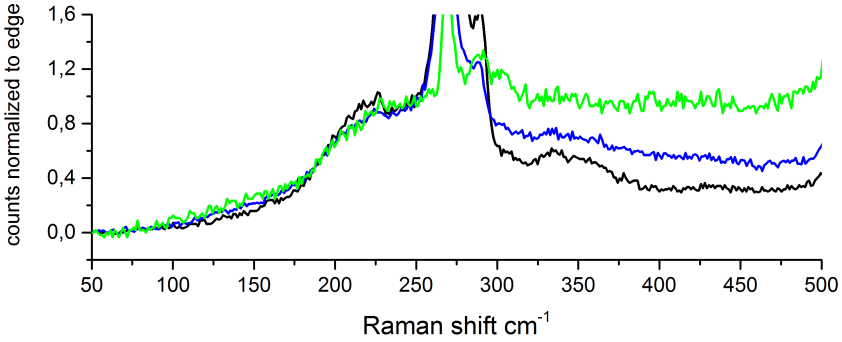
(a) SEM image of GaAs-Au NW heterostructure used for Raman spectroscopy measurement



(b) Raman counts, including Si substrate



(c) Raman counts normalized to maximum (usually at 269 cm^{-1}, for GaAs bulk at 292 cm^{-1} since peak proportions are reversed)



(d) Raman counts normalized to Au plateau at 250 cm^{-1}

Figure 46. Raman spectroscopy GaAs-Au on Si substrate: SEM of measured NW (46a), Raman counts (46b), normalized to maximum value (46c) and normalized to Au-edge value (46d)

3.6 General Observations

In the following short chapter some general results that should be applicable to all structures will be covered, meaning the PE-CVD SiO_2 shell and some observations about the FLA process. All other results were covered in the material-system chapters, starting with chapter 3.2 on p.41.

3.6.1 SiO_2 shell

The SiO_2-shell acts as a stable covering, preventing the NW structure to lose its shape when the NW core material and the deposited metal melt during the FLA process. The PE-CVD process used for the deposition of the SiO_2 shell was previously developed and optimized by Markus Glaser and thus remained unchanged. He suggested the parameters used for the synthesis of the heterostructures of this thesis. (cf. [6])

On a planar surface the same process would result in a layer of about 45 nm thickness. From this it can be reasonably assumed that the mean SiO_2 shell thickness deposited onto the NW should be about half that (22 nm). Measurements of the shell thickness via TEM confirmed the shell to be around 20 nm thick. The PE-CVD process is not always strictly uniform around 3-dimensional structures as can be observed in Figure 47, where it is roughly 4 times the thickness on one side of the NW compared to the other side.

It has to be noted, however, that this picture was taken after the FLA process, where the SiO_2 shell might change shape, meaning it cannot be used as definitive proof of the inhomogeneity of the PE-CVD process when covering micro- or nanostructures.

For unknown reasons, the stability of the SiO_2 shell under FLA conditions was largely dependent on the NW material. With Si-Au, it remained stable up to about 600 °C / 84 J/cm^2 (pre-heating to 600 °C, flash energy at 84 J/cm^2, where the first structures started melting. When the Au content of Si-Au was increased, though, melting already occured at 600 °C / 64 J/cm^2. With GaAs-Au even less energy induces melting. Structures started melting at 300 °C / 40 J/cm^2 already.

3.6.2 Flash Lamp Annealing

The usual FLA parameters, pre-heating temperature and flash energy, were separately adapted for every material system, so this chapter will only focus on one experiment conducted with Si-Au heterostructures, namely multiple FLA flashes. The experimental setup was explained in chapter 2.1.6 on p.32.

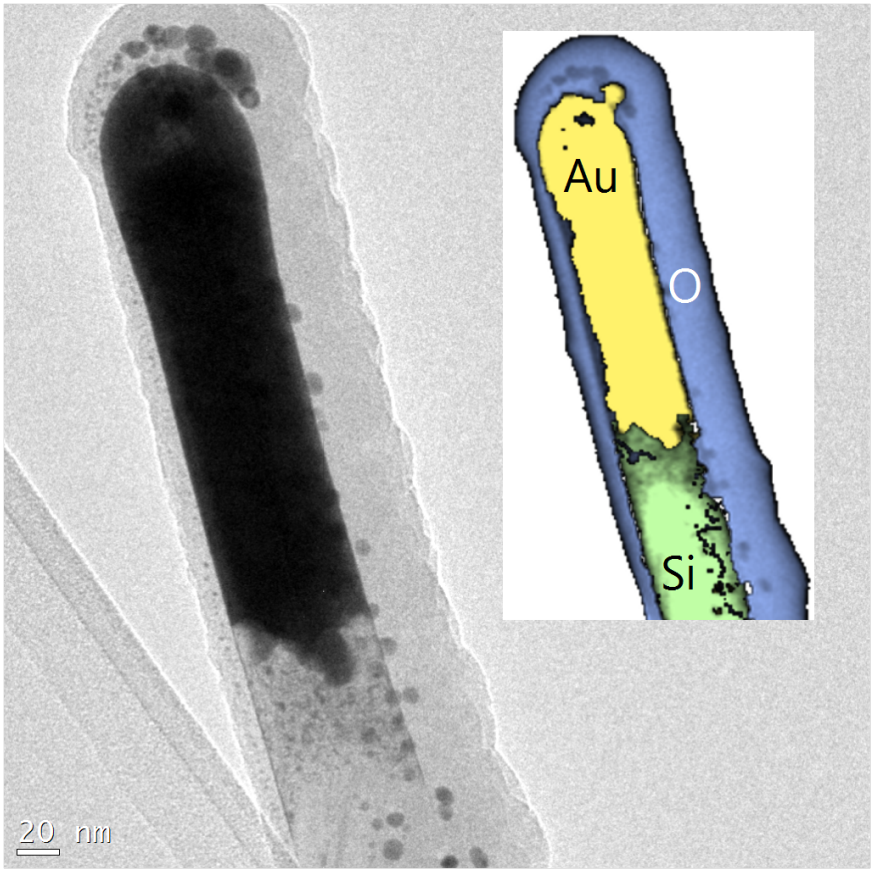


Figure 47. Si-NW with encapsulated Au at the end, TEM-image (left) and EDX element map (right). The Si in the SiO_2 shell is not separately highlighted. (by M. Stöger-Pollach @USTEM)

3.7 Other Tested Material Combinations for Heterostructure Synthesis

NW material	deposited material	status
Si	Al (sputtered)	no segments, oxidation?
Si	Sn (sputtered/evaporated)	no segments, oxidation?
Ag	Si (sputtered)	promising, inconclusive
ZnO	Au (sputtered)	no segments, spiky covering

Table 3.2. other experiments

In Table 3.2 other attempted material combinations for the synthesis of heterostructured NW are summarised. Their structure has either not been confirmed (Ag-Si) or no segmented structure was visible during SEM inspection (the others). The reason for sputtered aluminium and evaporated tin not to form segments like Au or Ni did, might lie in their tendency to oxidise rapidly. Trouble with the aluminium sputter target could also account for the failure of this experiment.

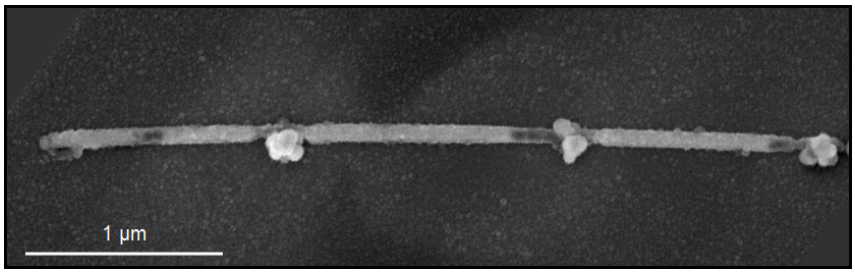
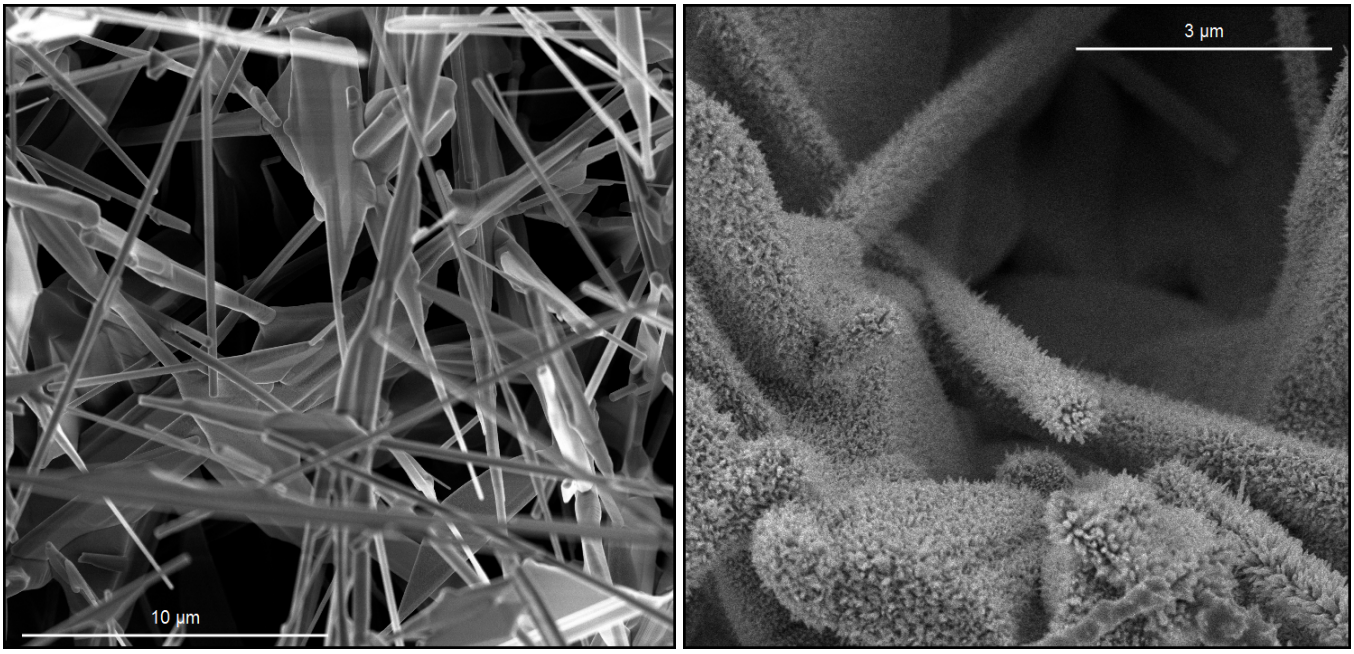


Figure 48. Silver (Ag) NW with possible Si segments, synthesized *after* dropcasting the Ag-NW on a Si substrate wafer

For Ag-Si, silver NW (Ag) were deposited onto a Si wafer with a 100 nm-thick SiO_2-layer. The subsequent synthesis process was the same as with the other structures (Figure 15 on p.30), except for the sputtered material to be a 4 nm layer of Si instead of a metal. The result of a subsequent flash at 600 °C / 64 J/cm^2 can be seen in Figure 48. The NW clearly shows some form of segments, although they are rather large. The NW surface seems much more rough compared with any other NW used in this thesis. Furthermore, just outside the segments there often is material agglomerated on the surface of the NW. Relatively large grains made of silver could potentially explain the surface rougness of the Ag NW. No further analysis was conducted on these structures so it is unknown which elements make up the different features.



(a) ZnO NW sputtered with Au and covered with SiO_2 before flashing **(b)** ZnO sample after the FLA process at 600 °C / 84 J/cm^2

Figure 49. SEM images of the ZnO-NW with Au material combination, (a) before and (b) after the FLA process

For ZnO-NW with sputtered Au something unexpected happened. No segments or segment-like structures were found, possibly since the melting point of ZnO ex-

ceeds that of the SiO_2-shell (roughly 1975 °C vs. the 1700 °C of SiO_2). The used FLA energy was the maximum our system is capable of, namely 700 °C / 90 J/cm^2. For unknown reasons the NW were partly covered in nano-spikes (Figure 49). Their widths were measured at 20 nm and smaller and they covered most of the sample. Since no further analyses were conducted it is unknown what these spikes are made of or how they come to form such a thorough covering. All-in-all 2 flashes were conducted, the first one at the aforementioned 700 °C / 90 J/cm^2, the second one at 600 °C / 84 J/cm^2. Both flashes resulted in the displayed structures, but at 90 J/cm^2 more of the underlying NW were melted and less of the sample was covered in nanospikes.

CHAPTER 4

Discussion, Conclusions & Outlook

4.1 Discussion

In general, the heterostructure synthesis method introduced in section 2.1 works very well with the material systems discussed in the previous sections. The method yields up to 10% (in case of GaAs probably more) heterostructured NWs.

The elemental composition of the synthesized structures turned out largely as expected, with the NW containing only the original NW material (Si or GaAs). With gold as deposited material, the segments were made exclusively of gold. Nickel, as expected, formed several alloys with silicon, among them the eutectic mixture with 56,5% silicon in nickel, $NiSi_2$ and probably NiSi as well. In Si-NW implanted with tin and subsequent synthesis processing, the implanted Sn formed alloys with the leftover Au from the NW VLS-growth. The present alloys were once again an eutectic mixture with 30% Sn in Au and Sn_2Au with 64% Sn in Au. It is very likely that different alloy combinations are also present in these structures when considering the synthesis method relies on complete melting. It is noteworthy to acknowledge the presence of eutectic mixtures in two different material systems. This indicates that these play an important role in the formation of the observed structures.

All synthesized structures displayed contaminants on the surface of the NW, the contaminants made of the same material as the segments (possibly a different alloy though). For Si-Au it was successfully attempted to selectively remove the Au contaminants from the NW surface via wet-chemical etching. Whether this is also possible with the other structures remains to be seen.

Altering the amount of sputtered material did not have a pronounced effect on segment formation in Si-Au and Si-NiSi heterostructures. Synthesis of Si-metal heterostructures also worked rather well when altering the used FLA parameters, although some differences were apparent between different metal/semiconductor combinations. These differences can probably be attributed to the difference in melting points of the pure metals and of their mixtures with the semiconductor. Equally as expected, the required energy for GaAs-Au structure was much less than for Si. It is expected for this difference to be due to the much lower melting point of GaAs.

Interestingly, the stability of the SiO_2 shell under FLA conditions was for unknown reasons largely dependent on the NW material. When the NW material melts, the

shell has to hold its form and weight together with the NW material weight. Since this kind of melting is expected and needed for the synthesis of the presented structures, though, it should not be the reason for the shell to melt at lower energies when a different NW material is present. Another rather weak hypothesis is a modified absorption coefficient of the underlying material, increasing or decreasing the actual temperature. With Si core NWs, the shell remained stable up to 600 °C and a flash lamp power density of 84 J/cm^2. At this energy some of the structures on the sample displayed some melting depending on the position of the NW on the sample. The NW would be melted almost completely when NW density was high at the observed spot or melted only a little or not at all when density was low. This can be explained by the difference in scattered light hitting the NW. When NW density is high, much more scattered light will hit the individual NW increasing the absorption and thus the temperature. The same behaviour was observed when the multiple-flash experiment was conducted. A higher energy than usual (84 J/cm^2 instead of 64 J/cm^2) was required because the NW were deposited onto a clean Si wafer where any scattering would obviously be suppressed.

The synthesized structures display some remarkable properties, chief among them the sharp interface between the metal and semiconductor parts of the Si-Au, Si-NiSi and GaAs-Au material systems. The interfaces are abrupt and sometimes atomically sharp in these structures, a seemingly unusual occurrence when considering the synthesis method relies on melting the NW along with the deposited material inside a container (the SiO_2 shell) and relying on fluid dynamics and phase energies to accomplish the rest. The Si-SnAu is the only characterized structure that did not display straight interfaces perpendicular to the NW surface. The reason for this has to lie in the dynamics of the elements involved. Possibly tin and the occuring tin-gold alloys alter the phase energies to favor a non-flat interface or the dynamics of the alloy with the SiO_2 shell is changed.

The FLA process itself can also be called into question. An experiment was conducted with a Si-Au sample prepared as usual but with an Rapid Thermal Annealing step used for segment synthesis instead of the FLA process. The sample was not nearly heated to the extent the FLA process can achieve and still most of the NW structures were destroyed. At the same time when SEM pictures of the sample were recorded there seemed to be structures resembling segmented NW among the mostly melted structures. Maybe an optimized RTA step can be used to synthesize similar structures. Since diffusion is not limited to millisecond timesframes in an RTA step, it is expected for segments to tend to agglomerate though, like they did when flashed multiple times. Therefore the FLA process should remain superior for synthesis of this kind of heterostructure.

The Raman measurement revealed some interesting and sometimes conflicting features. Si-Au heterostructured NW displayed the expected crystalline Si peak at 520 cm^{-1}, but not the second order transversal optical (TO) Si-peak at 910 cm^{-1}, which is only present in bulk Si, as-grown Si-NW and at the center of Si-Au NW

without segments. The peak at 520 cm^{-1} varies in height, usually with high values when no segments are present, but with one exception with an especially high measured peak exactly when a segment was present within the line scan across the NW. Further interesting dynamics of the Au plateau feature were observed, usually reaffirming the presence of Au on Si-Au NW without segments (as the TEM did as well). GaAs-Au NW heterostructures displayed the standard GaAs double peaks, with the TO peak at 268.5 cm^{-1} and the LO peak at 289 cm^{-1}. Especially interesting in GaAs-Au were the proportions of these two peaks, which changed considerably between structures. GaAs-Au NW heterostructures displaying the proportionally smallest TO peak, and the proportion of the peaks reversed for bulk GaAs with the LO peak dominating the spectrum. This is due to backscattering on different surfaces in the GaAs-NWs when compared with bulk GaAs - (100)-dominant for the LO peak and (110)-dominant backscattering surfaces for the TO peak. The Au plateau feature also displayed some interesting dynamics.

4.2 Conclusions & Outlook

The semiconductor-metal-semiconductor synthesis method presented in this thesis works very well and can yield sharp interfaces between the crystalline metal and semiconductor parts. This kind of interface is advantageous when applications for heterostructures are considered. There are many possible applications for heterostructures which is also the reason why this kind of structure is studied extensively.

Applications for heterostructured materials come in a wide variety. To achieve a high figure of merit in thermoelectric devices the non-linear properties of thermoelectric transmission in a real structure is important. Several approaches are being researched to improve the figure of merit, one of them heterostructured materials. In [10] the transmission function of a NW with multiple metallic segments is calculated. The transmission function largely governs the figure of merit that is achieveable by a structure. With the segmented NW used for the calculation in this paper it would be possible to optimize the transmission function to closely match the ideal case where the thermoelectric figure of merit should increase greatly. Multiple factors that would be difficult to control in an experimental setup are assumed in this theoretical treatment, though. In other papers it is also recognized that NW might be the key to achieve thermoeletric devices with high figures of merit. (cf. [9, 10, 53])

Other possible applications are in the field of plasmonics. Metal-semiconductor heterostructures can be favorable for plasmonic applications. Even suggestions concerning the photocatalytic conversion of light energy were made, employing such structures. (cf. [7, 8, 11])

The FLA process is in of itself a most interesting new tool, offering new possibilities for annealing with limited diffusion and, as demonstrated in this thesis, also the possiblity of synthesizing novel structures. To achieve this, novel process models are needed to predict proper FLA parameters depending on the desired result of the process. (cf. [15, 16])

Further research should be conducted on the electrical properties of the synthesized structures, since some problems with the electronic devices fabricated in the course of this thesis prevented proper characterization of the structures.

Also, not all attempted material systems did result in the expected structures. Especially the spiky covering of the ZnO-NW after the attempted heterostructure synthesis remains mysterious. Other material combinations might be achieveable by the same means that the Si-SnAu heterostructures were synthesized: implantation of the desired segment material. This method does tend to be quite labor-intensive though, since the implantation step can take several days until enough material resides inside the NW.

Since it is unknown why the structures form in the way they do, especially the atomically-sharp interfaces present in Si-Au, Si-NiSi and GaAs-Au, a theory as to how the phase energies and molecular dynamics interact to form these structures would be very interesting indeed. Further research into this is apparently already under way.

We wholeheartedly expect for this synthesis method to open up new roads for the synthesis of new and exciting heterostructures. Especially the use of the FLA process for the synthesis of nanostructures might enable novel devices and manufacturing techniques.

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Appendix A

Process Parameters

A.1 VLS NW Synthesis

The VLS process parameters used for the synthesis of the Si-NW used for this thesis is the following:

- sample inserted into growth chamber
- pumping to approximately $5 \cdot 10^{-2}$ mbar
- cleaning with 100 sccm He gas
- gas flux 110 sccm SiH_4, 10 sccm H_2 (before heating starts, until heating ends)
- 10 minutes at 550 °C and 3 mbar (pressure adjusted manually)
- 80 minutes at 530 °C and 6 mbar (pressure adjusted manually)
- cool-down period, gas flux off
- removal of the sample

A.2 Sputtering

Table A.1 contains all the used parameters for material sputtering. In the thesis text only the approximate layer thickness is mentioned. The respective parameters can be checked here.

An x in the last column indicates that these were the optimal parameters for the synthesis of the respective heterostructure.

A.3 PE-CVD

A PE-CVD Process with 425 sccm SiH_4 and 710 sccm N_2O at 1 Torr and 400 °C substrate temperature for 70 seconds was used. The same parameters were used for all samples. For gold-sputtered samples, the sample plate was pre-heated to the required 400 °C. When the deposited material was known to oxidise easily (like Ni, Al and Sn), the sample plate was not heated until the sample was inside and vacuum conditions were reached.

sputtered material	**power**	**time (s)**	approximate thickness	standard
Au	50 W	3	3,6 nm	x
Au	50 W	1	1,2 nm	
Au	50 W	9	10,8 nm	
Au	50 W	15	18 nm	
Au	25 W	1	0,55 nm	
Au	25 W	3	1,65 nm	
Ni	25 W	30	2,7 nm	x
Ni	25 W	5	0,45 nm	
Ni	25 W	10	0,9 nm	
Ni	25 W	60	5,4 nm	
Ni	25 W	90	8,1 nm	
Al	50 W	5	4,5 nm	
Al	50 W	7	6,3 nm	
Si	50 W	15	4 nm	

Table A.1. List of all the used Sputter-deposition parameters for all materials

A.4 Flash Lamp Annealing

All samples were pre-heated for 10 minutes since a thick Si carbide plate had to be used as the ground plate where samples were deposited onto in the FLA chamber. The reason for this was that the usual substrates, Si wafers, tended to be pulverized during high-energy flashes. All conducted flashes used a flash time of 20 ms. At this timeframe the system's maximum energy of 90 J/cm^2 is available for flashing. No argon flow was used, all flashes were conducted under a pressure of approximately $2 \cdot 10^{-6}$ mbar.

A.5 Hexpad Manufacturing

- sample cleaving, wafer 38 or 39 with 100 nm thermal SiO_2
- cleaning: acetone with 100% power in the ultrasonic bath, isopropanol dip
- drying using dry nitrogen
- spinner: photoresist AZ5214 at 9000 rpm for 35 s with ramp-2
- pre bake: 60 s at 100 °C
- mask alignment, back-gate contacts, exposure for 5,5 s
- developer AZ726MIF for 35 s, then twice 30 s in deionized water
- drying using dry nitrogen
- etching of the back-gated contacts: 130 s BHF-dip
- removal of photoresist in acetone, once again isopropanol dip afterwards and drying using the nitrogen pistol

- spinner again: photoresist AZ5214 at 9000 rpm for 35 s with ramp-2
- post bake: 60 s at 100 °C
- mask alignment, contacting pads, exposure for 4 s
- reverse baking: 60 s at 130 °C
- image reversal exposure: 20 s
- developer AZ726MIF for 30 s, then twice 30 s in deionized water
- drying using dry nitrogen
- sputtering: Ti cleaning at 100 W / 60 s, 10 nm Ti (50 W / 60 s), 100 nm Au (50 W / 60 s twice)
- Lift-off in acetone-bath at 50 °C, afterwards acetone dip, isopropanol dip
- drying using nitrogen

A.6 Electron Lithography

To achieve reliable contact gaps down to 200 nm and contact paths with a width of 5 µm, the line and spot size were kept below 20 nm. The standard E-Line photoresist 679.04 was used, the used spinner configuration was 4000 rpm for 35 seconds at ramp 2 which should result in a 290 nm covering. The photoresist was hardened for 15 minutes at a temperature of 170 °C on a hotplate. After contact evaporation the lift-off was conducted using an acetone bath at a temperature of 50 °C.

A.7 Contact Evaporation

All contact evaporation was conducted at the Leybold-evaporator. The chamber was sealed and pumped for at least 4 hours and subsequently Ti evaporation to getter any leftover particles was used in order to achieve a vacuum of roughly $2 \cdot 10^{-7}$ mbar. The Ti and Au deposition rate was kept low between 0.5 and 1 Å/s. The Au was evaporated onto a thin Ti layer of only 5 nm. The Au layer was usually 160-170 nm thick.

A.8 Etching

For all etching steps involving SiO_2 BHF at a ratio of 1:7 was used. To remove the PE-CVD SiO_2-shell an etching step of 26 s was used. For native-oxide removal 8-10 s of etching was conducted.

The Aqua Regia used for Au etching was mixed directly before application, with 20 ml of hydrochloric acid and 5ml of nitric acid. With the concentrations of hydrochloric and nitric acid of present in our lab (nitric 65%, hydrochloric 32%) this

results in a ratio of 2:1 between them. The standard ratio for Aqua Regia is 3:1. The author didn't check the recipe he was handed and now feels like a fool when he finally did. The actual required amount of hydrochloric acid with 65% is just 3.23 ml when using 20 ml of 32% hydrochloric acid. For surface Au removal, as successfully attempted for Si-Au heterostructures, the 2:1 Aqua Regia mixture was diluted at 1:4 with AquaRegia : deionized water and etched for about 3 s.

Statutory Declaration

I declare that I have authored this thesis independently, that I have not used other than the declared and cited sources, and that I have explicitly marked all material which has been quoted either literally or by content from the used resources.

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Date Signature