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Optimal Card Design for Non-Linear HF RFID Integrated Circuits With Guaranteed Standard-Compliance

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ABSTRACT The state-of-the-art design criteria for *High Frequency* (HF) *Radio Frequency IDentification* (RFID) cards at 13.56 MHz depend on the choice of a resonance frequency and a quality factor of the card. Our investigations show that these values are a result of the *Integrated Circuit* (IC)'s non-linearity and its dynamic range. We describe our accurate method for calculating the IC's circuit model during loaded and unloaded states. The dynamic range is identified where the IC is capable of achieving load modulation for all basic bit rates (106—848 kbit/s). The calculated IC's circuit model is simulated and compared to measurements showing good agreement. We formulate a constrained minimization problem based on the IC's circuit model, its dynamic range, including the entire card's parasitics, as well as loading effects from the reader side. The problem's solution is the optimum inductance for the card's coil that renders a standard-compliant HF RFID card. A prototype card is manufactured based on the optimum inductance and we show that it passes the standardized tests and operates for all basic bit rates within the field intensity range from 1.5 to 7.5 A/m, as specified.

INDEX TERMS HF, RFID, coil, inductive coupling, chip, integrated circuit, optimization, non-linear, load modulation, de-embedding.

I. INTRODUCTION

The *High Frequency* (HF) *Radio Frequency IDentification* (RFID) cards are composed of two components: a coil and an *Integrated Circuit* (IC) containing a microcontroller and the radio interface. The choice of coil type and dimensions is dominated by its inductance value. Established numerical tools exist which allow to compute spiral coil dimensions on the card's body: e.g. ANSYS Electronics [1] (formerly known as HFSS) or FastHenry [2]. The second component is the IC whose nominal equivalent parallel capacitance varies with the choice of IC. Considering a specific IC, a designer seeks the coil's dimensions that optimize the performance of the card. In this context, the optimum performance is determined based on the tests defined in the test standard ISO/IEC 10373-6 [3]. Several tests as specified in [3] need to be passed before any card is considered standard-compliant. One of the main tests that are directly dependent on the coil's design examines the card's responses to the reader's data packets, as specified by ISO/IEC 14443 [4]. According to the standard, Class 1 cards are supposed to fully operate for field intensities between 1.5 A/m and 7.5 A/m [5]. A standard-compliant (ICAO Doc. 9303 compliant) HF RFID card is capable of operating within that field range using all basic bit rates (106, 212, 424 and 848 kbit/s).

HF RFID cards have been utilized in many applications for over 25 years. Many designers have found practical card designs that are standard-compliant. State-of-the-art practical designs of a card's antenna coil depend on the choice of two parameters: the card's resonance frequency and quality factor. IC manufacturers provide a recommendation for the choice of these two parameters to design a fully operational card. However, previously there was no explanation why the recommended choice leads to a standard-compliant card and we are not aware of any previously published systematic method to optimize the card for standard-compliance. Reinhold *et al.* [6] focused on optimizing the energy

transmission to the card considering neither the standardized tests nor the IC's non-linear behavior. In [7] and [8] the condition for the IC's start of operation with respect to the field intensity was considered, however, this condition is not sufficient as shown by the prototype in Section II. Our work utilizes more information from the IC's side in addition to enforcing more conditions to ensure full standard-compliance at all basic bit rates.

To reach a systematic optimization method, we focus on analyzing and modeling the behavior of the IC, since there exists very little publicly available information on its operation and limitations. Based on that analysis, we present our method for providing the actual key parameters for designing a standard-compliant card.

This paper is arranged as follows: In Section II, we analyze the performance of a card designed based on a maximum power transfer criterion. The structure of the IC, as defined by the standard, is briefly explained in Section III. Our method for determining the circuit model of the IC denoted as *De-embedding transformer-based* method is presented in Section IV. This is followed by explanation of the IC's load modulation operation and extending the de-embedding method to characterize the IC during load modulation in Section V. The circuit model of the IC during loaded and unloaded states is verified in Section VI. In Section VII, we present a method to determine the IC's dynamic range for bit rates higher than 106 kbit/s. Based on these analyses, we provide in Section VIII a systematic method for calculating the card's coil inductance that lead to a standard-compliant card. Finally, the algorithm's results are verified in Section IX through a manufactured prototype, which passes the standardized tests.

II. MAXIMUM POWER TRANSFER

We test the performance of a card designed based on a maximum power transfer criterion, which means that the card's resonance frequency is equal to that of the reader (13.56 MHz). For the first glance, this approach seems the most adequate one since this leads to transferring the maximum possible power to the card, which reflects on the card's read range.

We have designed and manufactured the card shown in Fig. 1. This card uses an NXP IC "P5CD081UA/T1AY7996" with nominal capacitance 69 pF and nominal resistance 1850 Ω. The card has a resonance at 13.56 MHz and is denoted as "Card 1". The coil's inductance is 2 μH and its dimensions are available in Table 1 where 'N' indicates the number of turns, 'a' and 'b' are the width and length of the coil, respectively. The track width and height are given by 'w' and 'h', and 'g' is the gap between two adjacent wires.

There exist various tests at the ISO/IEC 10373-6 standard to validate an HF RFID card [3], [9]. The most challenging one with respect to card's design is to test the response of the card over the field intensity sweep from 1.5 up to 7.5 A/m. The test setup uses the *Test Proximity Coupling Device* (PCD) *Assembly*, which is composed of a card placed at 37.5 mm on top of the reference reader antenna (PCD), as specified by the standard [3]. A calibration coil (defined in [3]), composed of one turn and has a high resonance frequency, is used to measure the field intensity of the reader. It is placed at a distance of 37.5 mm below the reader antenna. The field intensity H is calculated from the RMS voltage measured on the calibration coil V_{cal}, using the following equation [10]

$$H = \frac{V_{cal}}{0.32}. \tag{1}$$

For this test, the reader sends several sequences for the card starting by a wake-up signal (Request A), where the card should respond. If the card responds correctly to all the reader's commands, the communication is considered successful, then the reader's power is changed and the test is repeated. For a standard-compliant Class 1 card, it should respond successfully between 1.5 and 7.5 A/m. An overview of the test setup can be watched in the video accompanying this contribution.

The test results for "Card 1" with 106 kbit/s are shown in Fig. 2. The card successfully achieves the lower bound where it is able to communicate starting from nearly 0.5 A/m. On the other hand, the card operates successfully only until 6.2 A/m and then it fails. This behavior is against intuition, since as the field intensity increases, the supplied voltage to the IC increases, thus it should have worked successfully. Such behavior have always been observed by our colleagues in industrial companies, however, its reasons were not determined and were generally related to the non-linearity of the IC without determining a specific reason. This was also one of the reasons that industrial companies did not recommend the use of the 69 pF ICs for HF RFID cards with ID-size 1, as this test becomes even less successful for higher bit rates as depicted in Fig. 2. The behavior of the IC for bit rates higher than 106 kbit/s is analyzed in Section VII.

FIGURE 1. Manufactured "Card 1" with a 69 pF IC.

TABLE 1. Coil's dimensions of "Card 1" (all values are in mm units).

Card 1			
N	3	w	0.3
a	50	g	0.3
b	80	h	0.035

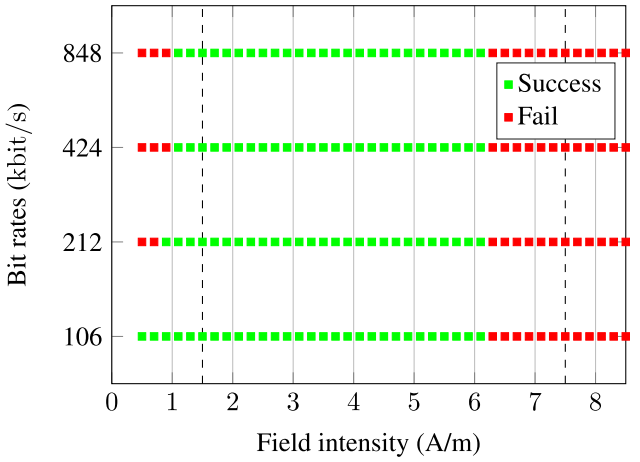

FIGURE 2. Results of the standardized test on "Card 1".

III. IC's STANDARDIZED STRUCTURE

Based on the results of the previous section, it is evident that the optimization method of an HF RFID card has to consider the IC's non-linearity. The IC contains a very complicated structure, as it is composed of many transistors and stages, so it is infeasible to simulate the IC's behavior from a transistor level, either because of the high complexity or because IC manufacturing companies do not share the structure of their ICs, as they are patented and classified. The general structure of the IC is defined within the Reference *Proximity Integrated Circuit Card* (PICC), which is defined in the standard [3]. We have investigated the Reference PICC in details [11], so we present here briefly the general structure of the IC and its operational stages.

The IC is composed of a voltage rectifier and limiter, load emulation and load modulation circuits. The AC voltage induced in the coil on the card is converted into DC inside the IC with the use of the voltage rectifier circuit. Conventionally, it is composed of a full-bridge rectifier [12] and a smoothing capacitor. A zener diode is used as a voltage limiter to avoid a voltage higher than a specific value in the IC. The load emulation circuit is a voltage controlled resistor that varies its resistance value to control the voltage drop on the IC as the power delivered increases.

The data exchange in RFID is achieved through load modulation, which means that the IC alternates its load from high to low values. The reader senses that change in load and maps it to the corresponding zeros and ones. Thus, load modulation circuit is the final stage in the IC, which is responsible for alternating the IC's load.

The IC can be simplified and modeled as a voltage controlled shunt capacitance and resistance circuit [13], [14], where the resistance is denoted as unloaded resistance. This simplified structure is easily verified through reviewing the structure of the Reference PICC [11]. Load modulation is modeled by adding a switch and a parallel low valued resistor denoted as loaded resistor. The values of the loaded resistance, unloaded resistance and capacitance vary with the applied voltage. Load modulation can be implemented by a loaded capacitor instead of resistor [13], but conventionally a resistor is used. The switch is connected to the unloaded resistance by default and when communicating with the reader, the IC switches between unloaded and loaded resistors. The simplified model of the card is given in Fig. 3, where L and R_{L} are the inductance and parasitic resistance of the coil on the card, C is the shunt capacitance of the IC, R_{unloaded} is the unloaded resistance and R_{loaded} is the loaded resistance of the IC during load modulation.

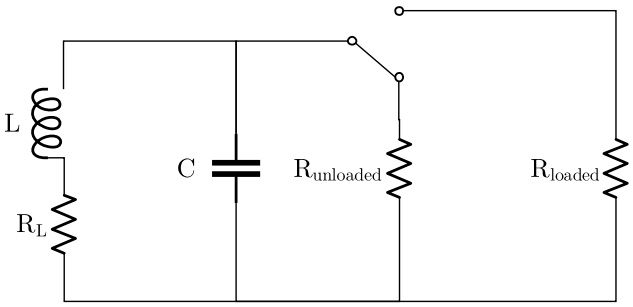

FIGURE 3. Simplified circuit model of an HF RFID card with IC.

To include the IC's non-linearity, we need to calculate the capacitive and resistive values of the IC with respect to the IC's voltage.

IV. DE-EMBEDDING TRANSFORMER-BASED METHOD

A. THE METHOD

The default position for the switch on the RFID IC is connected to the unloaded resistance, so in this section we aim to measure this resistance and the IC's capacitance versus the IC's voltage. A direct measurement of the IC's impedance has been carried out [14]. However, we showed earlier that such measurement technique would easily suffer from inaccuracy [15].

In [14], the resistance of the IC at low power is nearly 10 kΩ, while, at the beginning of IC's operation, it reaches around 2 kΩ. Similar results are also measured in [16] with another NXP IC, which has a different nominal capacitance value. Through analyzing the reflection coefficient Γ_{RC} of a shunt RC circuit, the sources of the inaccuracy are clearly observed. The equivalent impedance for a passive RC load is given by

$$Z_{RC} = \frac{R - j\omega R^2 C}{1 + \omega^2 R^2 C^2}, \tag{2}$$

which can be easily converted to the reflection coefficient (S-parameter). We simulated the effect of changing the value of the resistance and capacitance on the equivalent reflection coefficient. We observe a difference of only 0.3 dB for changing the resistance from 2 to 10 kΩ, as depicted in Fig. 4. Since the measurement equipment (such as a *Vector Network Analyzer* (VNA)) calculates the S-parameters of the IC and based on that we interpret the equivalent resistance and capacitance, this means such measurement has very low

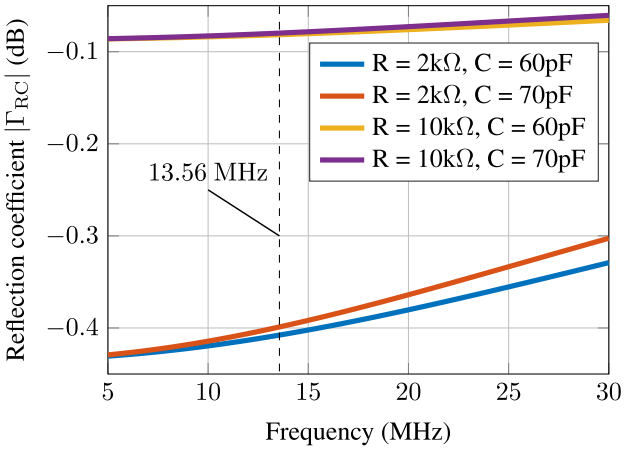

FIGURE 4. Reflection coefficients for 4 variants of an RC shunt circuit.

sensitivity to load variation where the smallest S-parameter's measurement error leads to a high difference in the equivalent values of resistance and capacitance. Furthermore, all variants are highly mismatched, which have a negative impact on the accuracy of the measurement equipment that usually operates with higher precision for matched loads. It is noted that these measurements are not possible to be measured by an impedance analyzer (which is more accurate than a VNA for mismatched loads) because the classical ones do not support high power measurements, which are essential to characterize the IC.

To counteract that problem, we propose the *de-embedding transformer-based method* [15]. Through inserting a proper two port network between the measurement device and the IC, we enhance the matching and more importantly the reflection coefficient's sensitivity to the variations in the RC load of the IC. Our proposed two port network is composed of two strongly coupled coils; one coil connected to the IC and the other to the measurement equipment through an SMA connector, as demonstrated in the circuit in Fig. 5. The first coil is modeled by L_1, R_1, C_1 and R_s represents the substrate's losses [17], while this substrate's resistance is neglected on the second coil, since it is usually much higher than the IC's parallel resistance. The second coil connected to the IC is modeled by L_2, R_2 and C_2. The two coils are conventionally strongly coupled with a mutual inductance M. Finally, we add the 50 Ω resistance, which enhances the circuit's matching with respect to 50 Ω. The voltage V_s represents the input voltage from the measurement equipment to the measurement fixture. Currently, there are several modules [18], [19] containing a coil directly connected to the IC (corresponds to the right half of the circuit in Fig. 5), this was the reason for choosing such circuit structure, as it allows a fast measurement of the IC, by just placing the module wirelessly on top of a coil connected to a 50 Ω, as we did in [15]. However, the prototypes we present here provide higher accuracy as verified in Section VI. Furthermore, this transformer structure provides high sensitivity of the

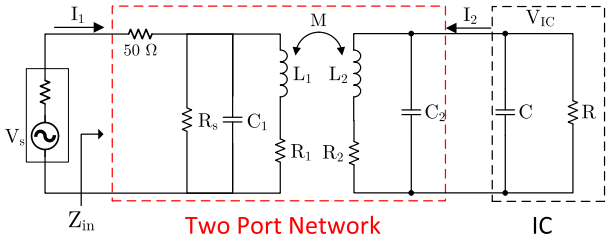

FIGURE 5. Circuit model of the de-embedding transformer-based measurement fixture.

reflection coefficient Γ_{in} (as seen by input source V_s) with respect to changing the resistance's value, as shown in Fig. 7.

A comparison between the simulated reflection coefficients for the proposed measurement fixture with a two port network is shown in Fig. 6. We observe that there is a significant change in the reflection coefficient, with changing the resistance R, similarly with changing the capacitance C. From this curve, it is also clear the choice of the two port network is related to the target load range, where the current circuit would not be suitable for an IC with a significant change in capacitance. However, the de-embedding concept is very general where the designer has to seek a suitable two port network for the target IC to be characterized.

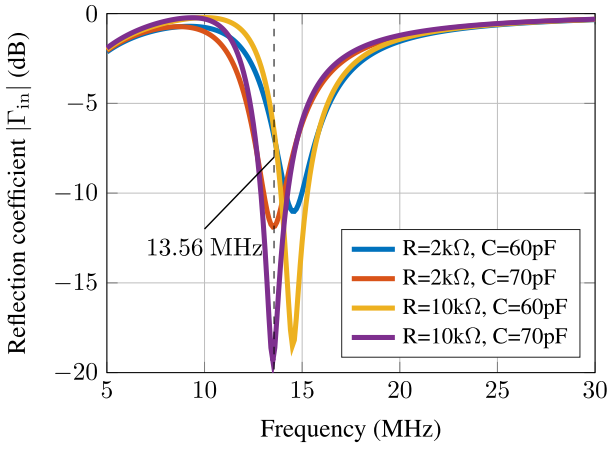

FIGURE 6. Comparing the reflection coefficients of different loads connected to a two port network.

Since we are only interested in the IC's behavior at 13.56 MHz, we compare in Fig. 7 the change in the reflection coefficient versus both the resistance and capacitance using the two port network (solid lines) to the direct method (dashed lines). These results are carried out by ANSYS Electronics (HFSS) simulations for the fixture implemented in Fig. 9. The capacitance value of 70 pF is the center value where we aim for the highest accuracy, since the IC that we measure has a nominal capacitance of 69 pF. At that capacitance value (red solid line), the reflection coefficient is highly sensitive to the change in resistance, so the IC's resistance can be accurately determined based on measuring that reflection coefficient.

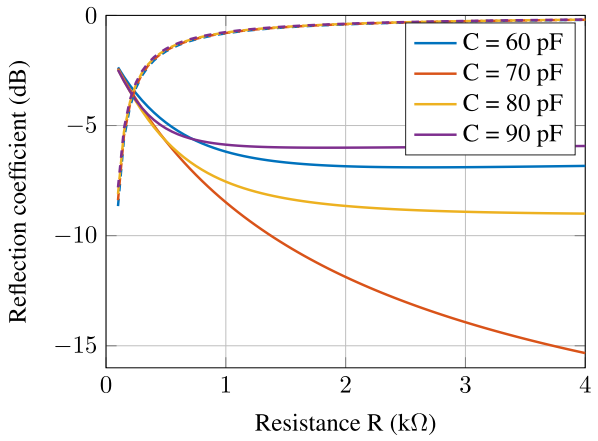

FIGURE 7. Comparing reflection coefficients of different loads with (solid) and without (dashed) a two port network at 13.56 MHz.

Moreover, all the variances of the de-embedding method are much better matched in comparison to the direct method. This is beneficial, since the measurement equipment are more accurate with respect to better reflection coefficient. When the resistance value falls below 200 Ω, the matching of the direct method becomes better. However, the value of matching of the de-embedding method is still good enough for good accuracy. Furthermore, we observe that the direct method is highly insensitive to the capacitance change for all the resistance values, as opposed for the de-embedding method, where there are significant changes in the value of the reflection coefficient at high resistances.

The input impedance Z_{in} of the measurement fixture is measured by a VNA. The impedance of the IC Z_{IC} is calculated using the de-embedding equation as follows

$$Z_{\text{IC}} = \frac{Z_{12}Z_{21}}{Z_{11} - Z_{\text{in}}} - Z_{22}, \tag{3}$$

where Z_{IC} is the equivalent impedance of the IC (R//C) and Z_{11}, $Z_{12} = Z_{21}$ and Z_{22} are the Z-parameters of the two port network.

Equation (3) provides accurate results only if the Z-parameters of the two port network are accurately calculated. To do so, we need to determine the exact values of 8 variables (Fig. 5). We showed earlier the analytical method to calculate these values [15]. The easier method is to perform three measurements on three different known lumped loads before placing the IC, which allows also to account for the different parasitic effects [15]. Using these results, we substitute in (3) and calculate the unknown Z-parameters. Then, with the knowledge of the Z-parameters, the value of the IC's impedance is calculated.

B. TEST SETUP

For accurate results, the reflection coefficient Γ_{in} of the measurement fixture (consequently the input impedance Z_{in}) and corresponding input voltage V_{s} should be accurately measured. This is achieved using a power calibrated VNA (R&S ZVA8). The IC is also tested at high power levels; therefore, we utilize the inputs of the VNA instead of the ports, in addition to using attenuators to protect the inputs of the VNA. The test setup is shown in Fig. 8, where the calibration is carried out as usual in place of the measurement fixture.

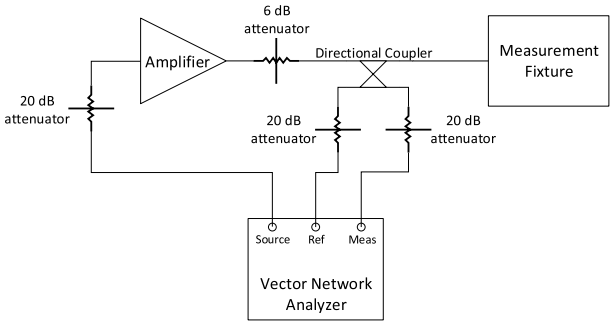

FIGURE 8. Test setup for characterizing the IC.

The "source" input of the VNA provides the input signal to the amplifier. This input signal is attenuated by 20 dB as the VNA provides better signal to noise ratio at higher power levels and on the other hand, the amplifier has a maximum input power. The 6 dB attenuator after the amplifier is placed to better match the amplifier such that it provides constant power regardless of the load's value. A directional coupler is used to connect the measurement fixture and the VNA. The direct path of the directional coupler has nearly no attenuation, while the coupled paths have 20 dB attenuation. Further 20 dB attenuators are placed on the coupled paths before the VNA's inputs, to protect them from high power.

We implement the circuit in Fig. 5 on a *Printed Circuit Board* (PCB), where the two identical coils L_1 and L_2 are placed on top and bottom layers, respectively. This is equivalent to the test fixture that was used in [15], where a PCB and module (IC + small module's coil) were used. However, our approach here provides better accuracy as the location of the two coils is fixed, which is essential, since they are strongly coupled. Furthermore, this allows testing ICs with different packages. Fig. 9 shows the manufactured test fixture. Moreover, using this PCB design we are able to fix an active probe at the IC's location to measure the IC's voltage at each input power level. We utilize an active probe (R&S-ZD30), which has low parasitic capacitance and high resistive value. The dimensions of the two coils L_1 and L_2 are given in Table 2, where both coils are identical. For the 50 Ω, we utilize two parallel 100 Ω resistors with 0.5 W rating such that they can withstand the high input power.

Another approach for calculating the IC's voltage V_{IC} is to derive it based on the source voltage V_{s} measured by the VNA. First, the current at port one is calculated by

$$I_1 = \frac{V_{\text{s}}}{Z_{\text{in}} + 50}, \tag{4}$$

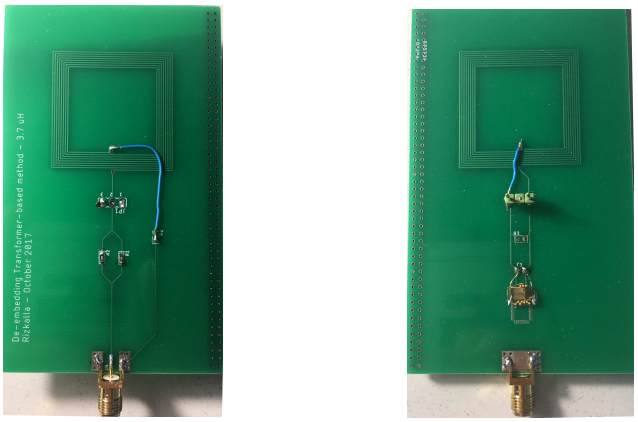

FIGURE 9. Manufactured PCB for characterizing the IC using de-embedding transformer-based method (a) Top (b) Bottom.

TABLE 2. Dimensions of coils L_1 and L_2 for de-embedding method (all values are in mm units).

Coils L_1 and L_2			
N	8	w	0.3
a	33	g	0.3
b	33	h	0.035

where the 50 Ω accounts for the source's impedance. The current of the second port is given by

$$I_2 = -\frac{Z_{21}}{Z_{IC} + Z_{22}} I_1. \tag{5}$$

Then, the IC's voltage is calculated using

$$V_{IC} = -I_2 Z_{IC}. \tag{6}$$

The full implemented test setup is shown in Fig. 10. The three known loads used in the measurements are (3900 Ω, 75 pF), (1800 Ω, 68 pF) and (100 Ω, 62 pF). Through solving equation (3), the Z-parameters of the two port network are calculated, which also accounts for the parasitic effects of the active probe, as the probe is connected during the measurements of the three loads. We recommend splitting this equation into two equations for real and imaginary parts, as this would make solving for the Z-parameters using MATLAB simpler and more accurate. The values of the Z-parameters are calculated at each power level to account for the changes within the measurement equipment themselves.

The measured equivalent IC's load is given in Fig. 11 for an NXP chip model "P5CD081UA/T1AY7996" with a nominal capacitance of 69 pF, where we observe the variation of the resistance with respect to the applied voltage, which is equivalent to the effect of the load emulation circuit in the Reference PICC [3], [11]. The model of the IC measured here provides higher accuracy in comparison to [14] and [16] as per our previous analysis and especially at low power where we measure the resistance value at low power to be around 3.5 kΩ while [14] and [16] shows a value of

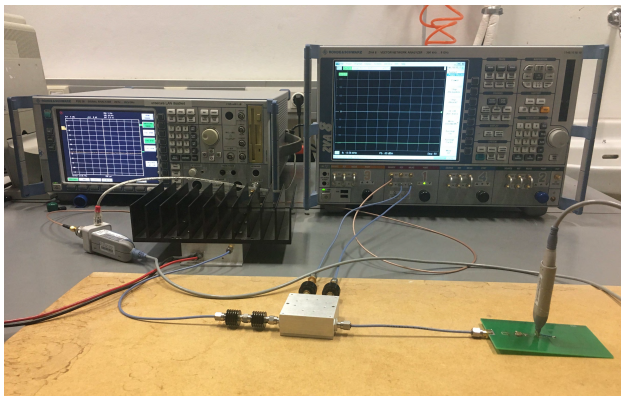

FIGURE 10. Implemented test setup for the de-embedding transformer-based method.

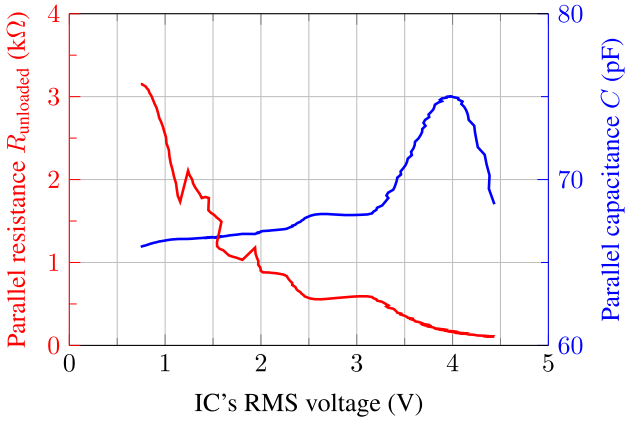

FIGURE 11. Equivalent load of the IC.

nearly 15 kΩ. We present the first verification of our IC's model in Section VI, which shows high accuracy and better results in comparison to our previous model [15].

Through observing the change in IC's load values, two IC's regions of operation are identified. The two spikes between 1.1 V and 1.6 V mark the "Power on reset" mode, where all the blocks of the IC are reset to a predefined state [14]. The following spike corresponds to the "Start of operation" mode, where the CPU of the IC starts operating and after this point (at 2 V) the IC is capable of communicating through load modulation [14]. We have discovered a third operation region, which starts at nearly 3.2 V in which the IC is capable of initiating load modulation at bit rates higher than 106 kbit/s, as shown in Section VII.

V. LOAD MODULATION

A. INTRODUCTION

Load modulation is the method of sending data from the card to the reader. This is achieved within the IC through switching between the loaded and unloaded resistances, as shown in Fig. 3. The unloaded resistance is the one where the IC's switch is connected to it by default. After the IC receives a certain wake-up sequence from the reader, the card responds

by alternating the switch between both resistances. The reader senses that change in resistance, as the card's matching is affected and it maps that into the corresponding zeros and ones.

The standard ISO/IEC 14443-2 specifies the use of a sub-carrier $f_s = 847.5$ kHz to modulate the main carrier $f_c = 13.56$ MHz. Thus, there are two side bands at 12.7125 MHz and 14.4075 MHz, where the card's data are contained only at these side bands [5], [13]. The frequency spectrum is shown in Fig. 12. The blue areas are the transmitted data and they depend on the used bit rate, where the basic bit rates according to the standard are 106, 212, 424 and 848 kbit/s.

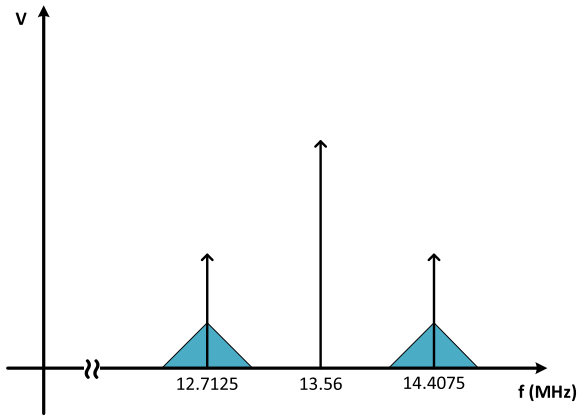

FIGURE 12. Frequency spectrum during load modulation.

B. MEASUREMENT's CHALLENGES

There are several challenges to characterize the IC during load modulation. One cannot directly use the previous de-embedding approach to determine the loaded resistance R_{loaded}, since the IC only switches to this state after receiving the wake-up sequence and then it keeps alternating between loaded and unloaded states for a short period (few milliseconds).

The loaded resistance of an *Ultra High Frequency* (UHF) RFID IC has been previously measured [20], but there are no publications for measuring it for HF RFID ICs. We tried to extend such approach for HF ICs, however, it was not feasible, since a bandwidth of nearly 3 MHz is required to fully capture the modulated signal, as can be seen in the spectrum in Fig. 12. This bandwidth is relatively large for a center frequency of 13.56 MHz and the available VNAs are not able to provide accurate measurements at this bandwidth. Thus, the measurement setup in Fig. 8 has to be modified, as VNA is not suitable for these measurements. The advantages of the VNA is that it provides accurate information on both magnitude and phase of the signal, so when looking for a replacement of the VNA, it needs to provide the same information. Unfortunately, for such bandwidth, we can only measure the magnitude accurately without phase knowledge, which makes the task more complicated. However, we present our work-around through utilizing the information from the unloaded state and through extending the de-embedding method.

We use the same circuit in Fig. 5. A wake-up sequence is transmitted to the IC with a trigger marking the beginning of the IC's response. In [21], we presented an approach to determine the loaded resistance based on the magnitude of the IC's voltage and using the VNA to measure the magnitude and phase of the source voltage V_s. In this work, we use a different approach through simultaneously measuring the current $I_{\text{IC}} = I_2$ and voltage V_{IC} at the IC's terminals, so no need to use a VNA. This approach is simple to determine the loaded resistance of the IC, however, both magnitude and phase information are required. As discussed earlier, due to measurement equipment's capabilities, we are only able to measure the magnitudes of the IC's voltage and current during loaded state. Based on the measured magnitudes at loaded state, the magnitude of the IC's impedance is calculated using (6) where Z_{IC} is the IC's impedance during load modulation (R_{loaded} // C). We derive the following equation based on (2)

$$R_{\text{loaded}}^4 \left(\omega^4 C^4 |Z_{\text{IC}}|^2 - \omega^2 C^2\right) + R_{\text{loaded}}^2 \left(2\omega^2 C^2 |Z_{\text{IC}}|^2 - 1\right) + |Z_{\text{IC}}|^2 = 0, \quad (7)$$

where the capacitance C is dependent on the unloaded IC's voltage. Therefore, we can determine the loaded resistance only if the IC's capacitance with respect to the applied voltage is known, which we calculated in the Section IV. We assume that the IC's capacitance does not change with load modulation, which is an acceptable assumption based on the structure of the load modulation circuit from the standardized Reference PICC [3], [11]. Furthermore, our assumption is verified in Section VI as the measurements are aligned with our extracted model.

C. MEASUREMENTS

We utilize a vector signal generator (R&S SMU 200A) to generate the wake-up sequence for the IC to respond back. This allows also generating a trigger marking the beginning of the IC's response. Our test setup is provided in Fig. 13, where we show the measurement fixture in two parts (two port network + IC) to show where the probes are placed. The current probe (Langer HFI 02) is placed in series to the IC while the active voltage probe (R&S-ZD30) is placed in parallel to the IC to measure its voltage. Since our signal analyzer (R&S FSQ26) has only one input, we use two signal analyzers, one for each probe. The connection of the voltage and current probes to the PCB is shown in Fig. 14.

It is noted that we can also remove the two port network for measuring the loaded resistance, since our measurements are now dependent on the magnitudes of the current and voltage of the IC in addition to the unloaded capacitance of the IC calculated in previous section. However, we keep the two port network in the setup to utilize the same PCB for measurements and also because we reuse the IC's voltage and capacitance extracted in previous section where the

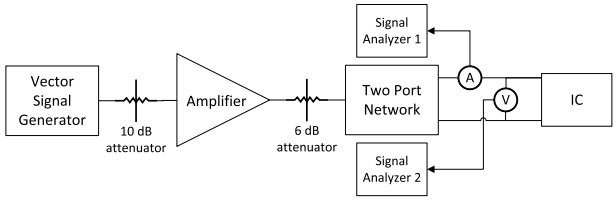

FIGURE 13. Test setup to measure the loaded resistance of an IC.

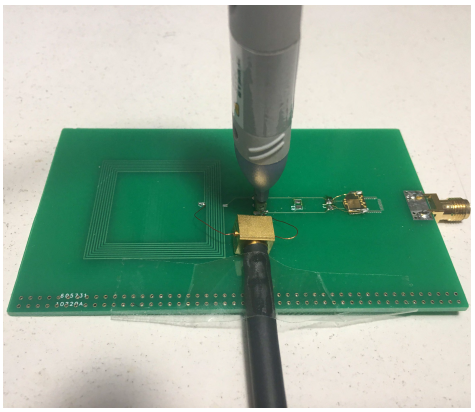

FIGURE 14. Manufactured PCB with current and voltage probes.

parasitic effects of the circuit were accounted for using the three known lumped measurements, so this provides better accuracy.

The vector signal generator sweeps the power between 10 dBm to 32 dBm (power level after the amplifier) and at each point, the loaded and unloaded voltages and currents of the IC are measured. At each step, the measured IC voltage will be as in Fig. 15, if load modulation is carried out successfully. The voltage at the unloaded state (higher voltage) is used to determine the corresponding capacitance value of the IC at this point, through looking into the data in Fig. 11. After that, we substitute in (7) with the capacitance value and the magnitude of the IC's impedance $|Z_{IC}|$, which is calculated by dividing the measured IC's voltage by the IC's current at loaded state (low voltage and current states). Through solving equation (7), the loaded resistance R_{loaded} of the IC is calculated at every power level.

Fig. 16 shows the measured loaded resistance, in addition to the unloaded resistance measured in Section IV. From this figure, we deduce an important information on the IC's operation that there exists a dynamic range in which the IC is capable of achieving load modulation. As already known, the IC is capable of starting load modulation at nearly 2 V [14]. However, there exists also a maximum voltage at which the IC stops load modulation, where it is marked by the small jump around 4.6 V. The difference between the loaded and unloaded resistance just before this point becomes small, which can lead to communication failure as the reader might not be able to differentiate the loaded and unloaded states. Therefore, we conclude that this IC can operate only

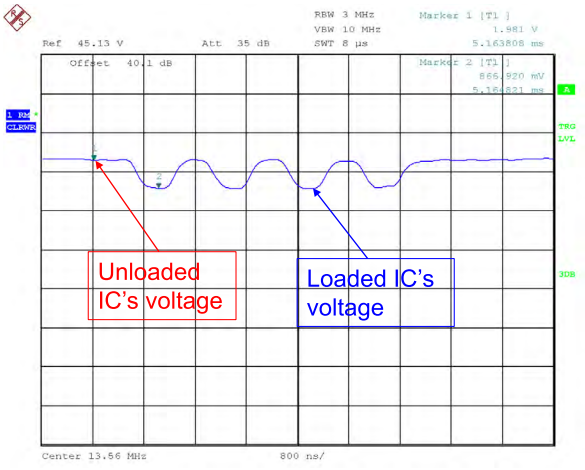

FIGURE 15. Measuring IC's voltage during load modulation using signal analyzer.

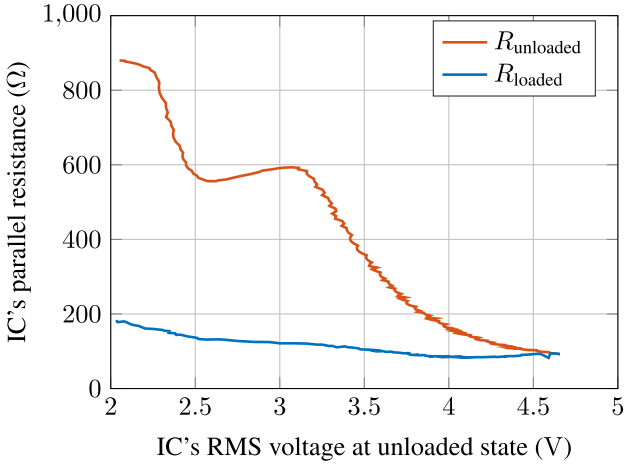

FIGURE 16. The measured unloaded and loaded resistances of the IC.

between 2 – 4.6 V RMS. It is noted that this 4.6 V is different (lower) than the maximum allowable IC voltage after which the IC is burned.

Considering the IC's dynamic range, we can now understand why the card stopped operating at 6.2 A/m, as shown in Fig. 2. At this point, the voltage on the IC reached the peak value, where the values of the unloaded and loaded resistances were equal, so no load modulation was achieved after that. This means that if the card is capable to operate at a very low field intensity, this would directly reduce the value of the maximum possible field intensity. Therefore, a new optimization algorithm must consider the IC's non-linear behavior (change in values of resistance and capacitance), in addition to considering the delivered voltage to the IC. This demonstrates our claim, that the resonance frequency and quality factor are not sufficient parameters for designing a standard-compliant card. Their values are just a result of a certain limitation from the IC.

VI. VERIFICATION

Through the methods proposed in the previous sections, we are able to characterize the IC during loaded and unloaded states. In this section, we aim to verify the accuracy of the derived IC model through simulating the model in ADS circuit simulator and compare that to measurements. For the measurement setup, the characterized IC is connected to a coil on an RFID card. We utilize the same test setup as in Section II, where a reader and the card are placed with a 37.5 mm separation. The reader transmits a wake-up sequence to the card and an active probe (low parasitic effects) is used to measure the voltage on the IC at loaded and unloaded states at 13.56 MHz [10], where the communication bit rate is set to 106 kbit/s. The same setup is simulated with the reader and card using ADS circuit simulator. The reader's circuit is given in ISO 10373-6 [3], while we calculate the card's model and coupling coefficient using HFSS and FastHenry [2].

We model the IC in the simulation as a non-linear voltage controlled RC circuit, where the values of the IC's resistance and capacitance in Fig. 11 and Fig. 16 are used. The IC's voltage is simulated for loaded and unloaded state where the system's circuit model is given in Fig. 17. The circuit on the left hand side is the reference reader antenna's circuit, as defined by the standard [3]. It is composed of a circular coil and a matching circuit to maximize power transfer at the frequency of operation. The right hand circuit is the RFID card. The IC is modeled by the parallel resistance R_{IC} and the capacitance C_{IC}, where their values depend on the applied voltage. The inductor on the coil is represented by the inductor L and small series resistance R_L. The parasitic capacitance of the coil is included in the IC's capacitance. The mutual inductance between the two coils is expressed with M.

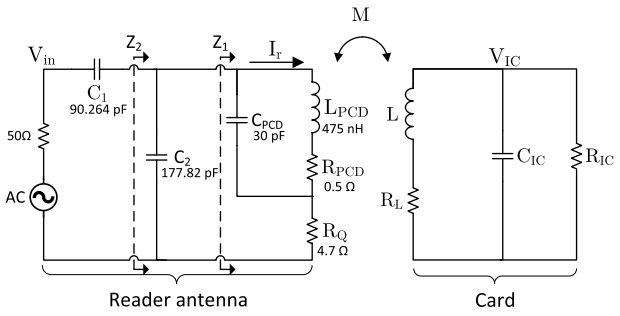

FIGURE 17. Circuits of the reader and card.

Fig. 18 shows the comparison between measurements and simulations of the IC's voltage. The measured IC's voltages are similar to that shown in Fig. 15, where we represent the unloaded and loaded voltages in Fig. 18 through taking the maximum and minimum of the waveform at each reader's power level, respectively. For the unloaded state, the simulated and measured IC voltage shows a very good alignment confirming the accuracy of our de-embedding method for calculating the IC's model. The curves for the loaded state

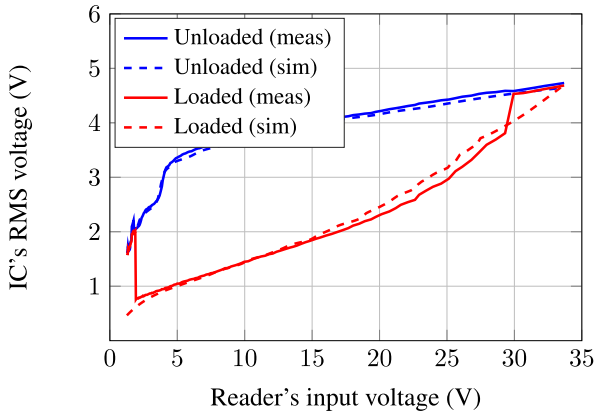

FIGURE 18. Comparison between measurements and simulations of the IC's voltage.

are also aligned well showing the validity of our method and assumptions in calculating the loaded resistance. We also conclude that the parasitic effect of the probes used in calculating the loaded resistance are very low, since the curves are aligned.

The measured loaded voltage (solid red curve) differs from the unloaded one only within the dynamic range of the IC ($2 - 4.6$ V), where load modulation occurs. These limits are not implemented in the simulation, which is why we see difference in comparison to the simulated loaded curve outside the IC's dynamic range.

VII. HIGHER BIT RATES

Before proceeding to the optimization algorithm, we address the different requirements on the IC's operation for bit rates higher than 106 kbit/s. The ISO/IEC 14443-2 standard demands for a Type A communication that the card modulates the information with an *On-Off Keying* (OOK) scheme at 106 kbit/s, while it requires *Binary Phase Shift Keying* (BPSK) modulation of the subcarriers at 12.7125 MHz and 14.4075 MHz with bit rates 212, 424, 848 kbit/s [5]. As observed from Fig. 2, the card's behavior for higher bit rates is different, as load modulation for bit rates higher than 106 kbit/s is initiated at 1.0 A/m in comparison to 0.5 A/m for 106 kbit/s. To identify the source of such behavior, we investigate the IC on its own, without considering the bandwidth limitations enforced by the coil's design. However, the required sequence for an IC to respond at higher bit rate is significantly long that we could not achieve by the vector signal generator (SMU 200A).

For that reason, we utilize an industrial reader (Proxilab) to transmit sequences at high bit rates. According to the standard, the initial communication (Request A, Anti-collision, Select, RATS and PPS) between the reader and card is achieved at 106 kbit/s and after that an "I-Block" is transmitted at the desired bit rate (106, 212, 424 or 848 kbit/s). Thus, the reader needs to sense the IC's response before it can start communicating at high bit rate. Therefore, we utilize the

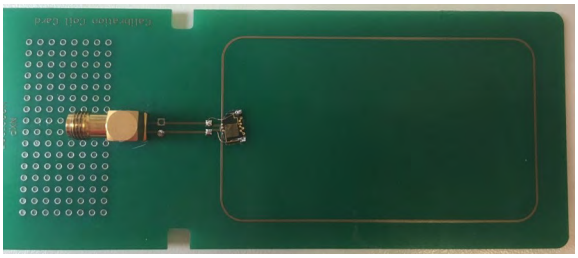

FIGURE 19. A calibration coil with an IC.

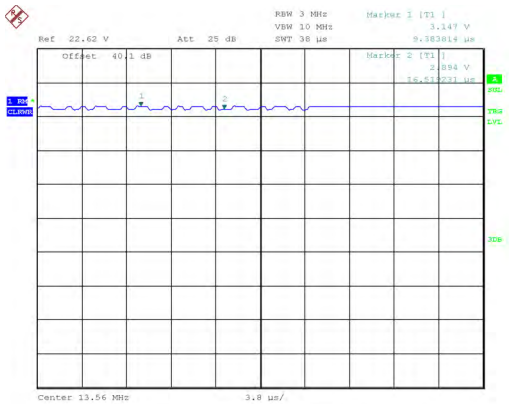

FIGURE 20. The voltage on an IC communicating at 848 kbit/s.

calibration coil [3] by soldering the IC on its terminals and connecting the reader directly to it. There are two advantages for using the calibration coil here; first is that it has a very high resonance frequency (nearly 100 MHz), so it will provide a flat frequency response at the desired frequency of operation (13.56 MHz). This ensures that the conclusions that we draw on the IC are dominated by the IC's behavior and that the coil's dimensions do not affect the performance. The second advantage of using the calibration coil is that by placing the reader's sense coil on top of it, the reader can sense the communication from the IC and initiate the high bit rate communication. The used calibration coil with an IC is shown in Fig. 19.

Through connecting the reader to the SMA connector of the calibration coil, we utilize the active probe (R&S-ZD30) with a signal analyzer to measure the voltage change on the IC. We tested the IC first at 106 kbit/s and the results were as expected, that the IC is capable of starting communication at 2 V. We found out that the IC is only capable to start communication at 3.2 V for higher bit rates. Fig. 20 shows the lowest voltage where load modulation was achieved at 848 kbit/s, where the unloaded IC's voltage is 3.15 V. We observe here that the difference between the loaded and unloaded states is small in comparison to Fig. 15 because in this test the IC is directly connected to the signal source, so the mismatching due to load modulation is not strong.

Therefore, we deduce that for an IC operating at 106 kbit/s, the IC's dynamic range is $2-4.6$ V. While for higher bit rates, the dynamic range is reduced to $3.2-4.6$ V.

VIII. NOVEL OPTIMIZATION ALGORITHM

As per our analysis, the voltage delivered to the IC is essential in determining the operation range of an HF RFID card. To include the IC's voltage, inherently means that the reader's circuit should be included into the analysis also. We aim to use a set of equations in order to formulate an optimization problem to determine the value of the coil's inductance L that leads to a standard-compliant card. The Sections VIII and IX build on and extend our previous work in [22] where, in this contribution, all basic bit rates are investigated, all parasitic elements are included, a better and more practical optimization goal is set, in addition to including further clarifying figures to verify the results.

We utilize the circuit model in Fig. 17 to derive (see Appendix) the following equation

$$\left(\omega^4\, C_{\rm IC}^2 + \frac{\omega^2}{R_{\rm IC}^2}\right) L^2 - (2\omega^2\, C_{\rm IC})L + 1 + \frac{R_L}{R_{\rm IC}} + \frac{R_L^2}{R_{\rm IC}^2} + \omega^2\, R_L^2\, C_{\rm IC}^2 - \left|\frac{j\omega M I_{\rm r}}{V_{\rm IC}}\right|^2 = 0, \quad (8)$$

that relates the reader's current $I_{\rm r}$ with IC's voltage $V_{\rm IC}$ while considering all the components in the system. This is the key equation to deriving an optimization algorithm for HF RFID cards.

Using (8), we formulate a constrained optimization problem to calculate the inductance L that leads to a certain defined voltage at the IC's terminals. Let $V_{\rm IC-1}$ and $V_{\rm IC-2}$ denote the dynamic range of the IC, where $V_{\rm IC-1}$ and $V_{\rm IC-2}$ are the minimum and maximum RMS voltages, respectively, at which the IC is capable of achieving load modulation. Let $R_{\rm IC1}$, $C_{\rm IC1}$, $I_{\rm r1}$ and $R_{\rm IC2}$, $C_{\rm IC2}$, $I_{\rm r2}$ be the IC's unloaded resistance and capacitance and the reader current corresponding to IC voltages of $V_{\rm IC-1}$ and $V_{\rm IC-2}$, respectively. We define the vector $\mathbf{x} = (L, M, |I_{\rm r1}|, |I_{\rm r2}|)^T$ of unknowns, where x_n denotes the nth (between 0 and 3) element in $\mathbf{x}$. Using (8), the function $f(\mathbf{x})$ is defined as,

$$f(\mathbf{x}) = \left(\omega^4 C_{\rm IC1}^2 + \frac{\omega^2}{R_{\rm IC1}^2}\right) x_0^2 - (2\omega^2 C_{\rm IC1}) x_0 + 1 + \frac{2R_L}{R_{\rm IC1}} + \frac{R_L^2}{R_{\rm IC1}^2} + \omega^2 R_L^2 C_{\rm IC1}^2 - \frac{\omega^2 x_1^2 x_2^2}{|V_{IC-1}|^2}, \quad (9)$$

and the constraint vector $\mathbf{g}(\mathbf{x})$ is given by

$$\mathbf{g}(\mathbf{x}) = \begin{bmatrix} ax_0^2 - bx_0 + \left(c - \dfrac{\omega^2\, x_1^2\, x_3^2}{|V_{IC-2}|^2}\right) \\ k\sqrt{x_0\, L_{\rm PCD}} - x_1 \\ |I_{\rm r}(x_0, x_1, R_{\rm IC1}, C_{\rm IC1})| - x_2 \\ |I_{\rm r}(x_0, x_1, R_{\rm IC2}, C_{\rm IC2})| - x_3 \end{bmatrix}, \quad (10)$$

where k is the coupling factor between the reader and card with

$$a = \omega^4 C_{\mathrm{IC2}}^2 + \frac{\omega^2}{R_{\mathrm{IC2}}^2},$$
$$b = 2\omega^2 C_{\mathrm{IC2}},$$
$$c = 1 + \frac{2R_L}{R_{\mathrm{IC2}}} + \frac{R_L^2}{R_{\mathrm{IC2}}^2} + \omega^2 R_L^2 C_{\mathrm{IC2}}^2, \tag{11}$$

and the reader's current I_{r} is calculated by Equation (18).

Using these functions, we formulate the constrained optimization problem

$$\min_{\mathbf{x}} \quad f(\mathbf{x}) \tag{12a}$$
$$\text{subject to} \quad f(\mathbf{x}) \leq 0, \tag{12b}$$
$$\mathbf{g}(\mathbf{x}) = \mathbf{0}, \tag{12c}$$
$$\mathbf{x} \succ \mathbf{0}. \tag{12d}$$

This optimization problem finds the inductance value $x_0 = L$ that leads to a voltage of $V_{\mathrm{IC-2}}$ at field intensity H_2 while reaching at least voltage $V_{\mathrm{IC-1}}$ at H_1. This means that the card works between H_1 and H_2 and it may also work at field intensities below H_1, if the IC's dynamic range allows that. The values of all parameters in (12) are known or calculated in previous sections. The values of the IC's resistance and capacitance are calculated in Section IV.

The objective function is minimized such that it is less than or equal zero, according to (12a) and (12b). These two equations correspond to having an IC voltage of at least $V_{\mathrm{IC-1}}$ at the field intensity H_1. The first equation in the constraint vector $\mathbf{g}(\mathbf{x})$ forces a voltage of $V_{\mathrm{IC-2}}$ on the IC at field intensity H_2. It is noted that the IC's voltage becomes highly sensitive to the resistance value as we approach $V_{\mathrm{IC-2}}$. The value of the mutual inductance is updated in accordance to the inductance value for a certain coupling factor k, as expressed by the second equation in the constraint vector $g_1(\mathbf{x})$.

Finally, the remaining two equations in the constraint vector account for the loading effect (coupling term $\frac{\omega^2 M^2}{Z_{card}}$) by updating the reader's current according to (18), which is dependent on the mutual inductance M and inductance value L. For these two conditions, it is more accurate to consider the actual complex values of the currents rather than the magnitudes. However, solving for the magnitude simplifies the problem and allows it to be solvable through MATLAB. The constraint (12d) ensures that the optimization vector $\mathbf{x}$ is feasible and element-wise positive. The value of mutual inductance $x_1 = M$ can actually be negative in real applications, however, the sign does not make an effect on the performance (it is always squared in the equations) and its sign only reflects the winding direction of the card's coil. Therefore, for simplicity, the whole vector $\mathbf{x}$ is conditioned to be element-wise positive.

The procedure for optimization of L is summarized in Algorithm 1. The algorithm starts by choosing L_0 that leads to maximum power transfer. This means L_0 is calculated such that the card has a resonance frequency at 13.56 MHz. FastHenry [2] is utilized to determine the corresponding mutual inductance M and coupling factor k. After that, the reader currents at 1.5 A/m (H_1 for generality) and 7.5 A/m (H_2) are calculated at the maximum power transfer condition. These values are used as an initial point for solving the optimization problem (12). The algorithm outputs the vector $\mathbf{x}$ where the inductance value is given by x_0.

Algorithm 1: Optimization of L in the RFID Card

1. Initialize $L_0 = \frac{R_{\mathrm{IC1}}^2 C_{\mathrm{IC1}}}{1+\omega^2 R_{\mathrm{IC1}}^2 C_{\mathrm{IC1}}^2}$
2. Calculate coupling factor k and mutual inductance M_0 with FastHenry for L_0
3. Set the power at the reader corresponding to H_1 A/m, calculate the reader current I_1
4. Set the power at the reader corresponding to H_2 A/m, calculate the reader current I_2
5. Set $\mathbf{x}_{\mathrm{initial}} = [L_0, M_0, |I_1|, |I_2|]$
6. Solve the optimization problem (12) with the initial point $\mathbf{x}_{\mathrm{initial}}$

Output: $L = x_0$

IX. PROTOTYPE MEASUREMENTS

To verify our proposed algorithm, we utilize the information of the IC that we measured in previous sections to calculate the inductance value of a standard-compliant HF RFID card. The IC has the following values: $R_{\mathrm{IC1}} = 503\ \Omega$, $C_{\mathrm{IC1}} = 75$ pF and $V_{\mathrm{IC-1}} = 3.3$ V. We consider here the minimum voltage required for communication at the highest basic bit rate (848 kbit/s). The parasitic capacitance of the spiral coil (≈ 7 pF) is included into the IC's capacitance. The IC is capable of communicating through load modulation up to voltage $V_{\mathrm{IC-2}} = 4.6$ V where $R_{\mathrm{IC2}} = 98\ \Omega$ and $C_{\mathrm{IC2}} = 74$ pF. These values, based on results in this contribution, are more accurate in comparison to values extracted from [15].

The value of the coupling coefficient for a card with size ID1 is $k = 0.05$, according to our calculations. The coil's resistance $R_L = 1.4\ \Omega$. The standard specifies the card to operate between 1.5 to 7.5 A/m, however, to allow for some tolerance in the results, we set $H_1 = 1.3$ A/m (corresponds to 26.6 dBm reader's input power) and $H_2 = 7.6$ A/m (corresponds to 42.5 dBm). Substituting all the values into Algorithm 1, the optimum inductance value is $L = 2.16\ \mu$H. The algorithm outputs also the mutual inductance $M = 50.55$ nF, $|I_{\mathrm{r1}}| = 0.318$ A and $|I_{\mathrm{r2}}| = 2.026$ A.

We manufactured an optimized card based on the algorithm's results, where the dimensions of the coil are given in Table 3. Fig. 21 shows the measured voltage on the optimized card, using the same setup as described in Section II. The results show that the voltage on the IC at 7.6 A/m is nearly 4.6 V while at 1.3 A/m the IC's voltage is higher than 3.3 V, which verifies our optimization criterion.

TABLE 3. Coil's dimensions of optimized RFID card (all values are in mm units).

Optimized Card			
N	4	w	0.3
a	38	g	0.7
b	67	h	0.035

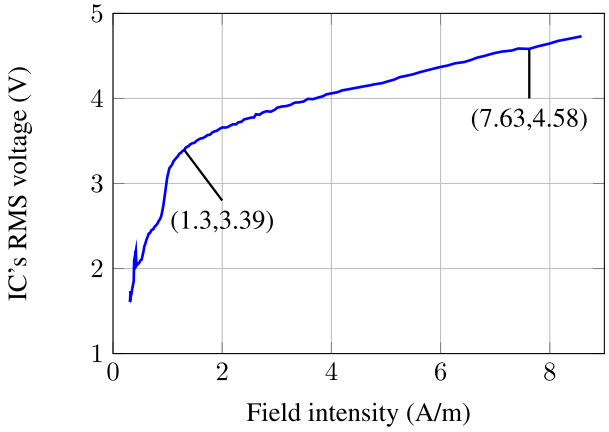

FIGURE 21. Measured IC's voltage of optimized RFID card.

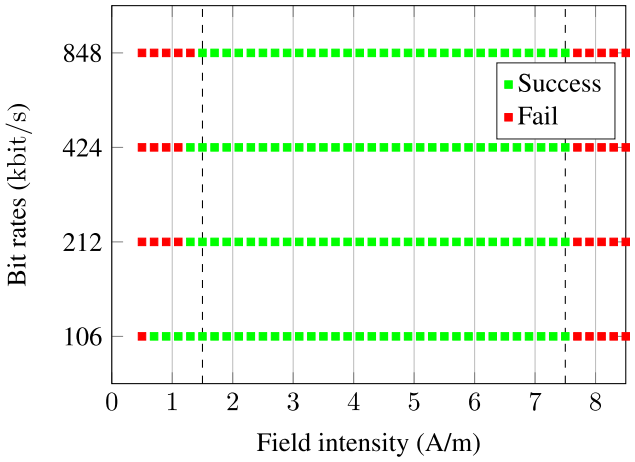

FIGURE 22. Results of standardized test on the optimized card.

Furthermore, the optimized card passes the standardized tests successfully where it operates for all bit rates from 1.4 to 7.6 A/m, as depicted in Fig. 22.

In practical scenarios, a card would not have a constant distance from the reader antenna, it would be rather moving. However, the standard does not define a test for a moving card. It depends rather on the field intensity at the card's level, which is directly related to the movement of the card. This means that the reader's power required to reach 1.5 A/m at a distance of 37.5 mm is higher than that required to reach the same level at 10 mm distance. To illustrate this further, we carry out ADS simulation for our setup, where we include the reader antenna, card and calibration coil. The reader's power is set to 27 dBm and we vary the coupling

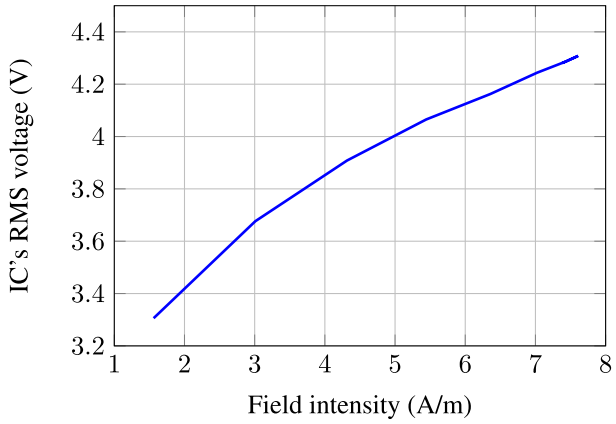

FIGURE 23. Simulated IC's voltage of optimized RFID card at 27 dBm reader's power and varying the coupling factor from 5% to 50%.

factor between the reader and card and that to the calibration coil. This is equivalent to moving the card with respect to the reader antenna while measuring the field intensity at the card's level. Fig. 23 shows the change in IC's voltage versus the field intensity as the coupling factor changes from 5% to 50%. We observe that with increasing the coupling factor, the value of the IC's voltage between 1.5 to 7.5 A/m is still within the IC's dynamic range. This effect is also demonstrated in the video accompanying this contribution.

For the reference reader antenna that we use in our measurements, we calculate that the coupling factor would increase from 5% to 7% (with measurements and simulations) when the card is moved to 9 mm from the reader antenna. Therefore, the change in coupling factor is not very strong. We test the optimized card at 9 mm from the reader antenna for 106 kbit/s and it works for the same field intensity range as shown in Fig. 22.

There exist other reader antenna designs where the coupling factor might have a stronger variation; however, the standard only specifies these tests against the reference reader antenna, which we used. Therefore, the designer should specify an adequate value for the coupling factor (consequently the equivalent reader's input power to reach the needed field intensity) such that the card is operating within the application's range. Usually, the IC's dynamic range is larger than the operational range of the card, as shown in the 106 kbit/s results in Fig. 22 and with another prototype in [22], which can be utilized by the designer. However, we can see in this contribution that for 848 kbit/s the dynamic range is very tight. Thus, flexibility at high bit rates for this type of ICs is limited as its dynamic range is only between 3.2 and 4.6 V.

X. SUMMARY AND CONCLUSION

We have demonstrated that designing HF RFID cards based on a maximum power transfer criterion alone is not suitable, as it does not render a standard-compliant card. We have shown that the main design parameter is the

IC's delivered voltage, which is limited by the IC's non-linear behavior (voltage dependent RC values) in addition to the IC's dynamic range. The state-of-the-art design parameters are the card's resonance frequency and quality factor, and we have shown that these values are only a result of the IC's limitations.

We propose and describe a de-embedding method to accurately determine the IC's equivalent circuit model for loaded and unloaded states and to identify the IC's dynamic range. The IC is capable of initiating load modulation when the voltage on its terminals is between $2-4.6$ V. We also discovered that the IC has a smaller dynamic range ($3.2-4.6$ V) for bit rates higher than 106 kbit/s. The calculated circuit model of the IC was simulated and compared to measurements. The obtained results were in good agreement, which verifies the accuracy of our proposed de-embedding method.

We utilize this information to create an algorithm that calculates systematically the required inductance value for a certain IC to render a standard-compliant card, where we formulated a constrained optimization problem that can be easily solved through MATLAB. The algorithm's results were verified through manufacturing a corresponding prototype and carrying out the standardized tests on this card. The optimized card has successfully passed the standardized test for all the basic bit rates (106 up to 848 kbit/s).

APPENDIX

We consider the circuit in Fig. 17 to derive the key equation for our optimization algorithm. The mutual inductance M between the two coils (L_{PCD} and L) corresponds to having a voltage source series to the card's coil with the value $j\omega MI_{\text{r}}$, where I_{r} is the current passing through the reader coil. Therefore, we need to determine I_{r} in order to calculate the IC's voltage.

First step is to determine the total impedance of the reader circuit where we begin from the reader coil's side. There is an additional term $\frac{\omega^2 M^2}{Z_{\text{card}}}$ placed in series to the reader's inductance L_{PCD} due to coupling, where Z_{card} is the total impedance of the card from the inductive source's point of view. This accounts for the loading effect between the card and the reader. The card's impedance is given by

$$Z_{\text{card}} = R_L + j\omega L + \frac{R_{\text{IC}} - j\omega R_{\text{IC}}^2 C_{\text{IC}}}{1 + \omega^2 R_{\text{IC}}^2 C_{\text{IC}}^2} \tag{13}$$

The impedance Z_1 is calculated as follows

$$Z_1 = \frac{R_{\text{PCD}} + j\omega L_{\text{PCD}} + \frac{\omega^2 M^2}{Z_{\text{card}}}}{(j\omega C_{\text{PCD}})(R_{\text{PCD}} + j\omega L_{\text{PCD}} + \frac{\omega^2 M^2}{Z_{\text{card}}} + \frac{1}{j\omega C_{\text{PCD}}})} + R_Q \tag{14}$$

Adding the parallel capacitor C_2, the impedance becomes

$$Z_2 = \frac{Z_1}{(j\omega C_2)(Z_1 + \frac{1}{j\omega C_2})} \tag{15}$$

The total impedance Z_T at the input of the reader antenna is

$$Z_{\text{T}} = Z_2 + \frac{1}{j\omega C_1} \tag{16}$$

The voltage at Z_2 is

$$V_{Z_2} = V_{\text{in}} \frac{Z_2}{Z_{\text{T}}} \tag{17}$$

where V_{in} is the voltage from the AC source at the reader side.

Therefore, the reader's current I_{r} passing through the coil is calculated by

$$I_{\text{r}}(L, M, R_{\text{IC}}, C_{\text{IC}}) = \frac{V_{Z_2}(Z_1 - R_Q)}{Z_1(R_{\text{PCD}} + j\omega L_{\text{PCD}} + \frac{\omega^2 M^2}{Z_{\text{card}}})}. \tag{18}$$

The IC's voltage is calculated by [23]

$$V_{\text{IC}} = \frac{j\omega MI_{\text{r}}}{1 - \omega^2 LC_{\text{IC}} + \frac{R_L}{R_{\text{IC}}} + j(\frac{\omega L}{R_{\text{IC}}} + \omega R_L C_{\text{IC}})} \tag{19}$$

where we added the effect of R_L into this equation. Since the magnitude of the voltage is the important value, we calculate the squared magnitude of (19) as expressed in (8).

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