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ESD experiments and simulations on RF CMOS switches

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Ao. Univ. Prof. Dr. Dionyz Pogany
Institut für Festkörperelektronik

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Technischen Universität Wien
Fakultät für Elektrotechnik und Informationstechnik

von

Matteo Rigato, M.Sc.

Mat.Nr. 1428669
Peter-Rosegger-Straße 33/13
A-8053 Graz

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1. Gutachter: Prof. Dr. Guido Groeseneken
2. Gutachter: Prof. Dr. Gaudenzio Meneghesso

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Abstract

State-of-the-art bulk silicon RF antenna switches are built by multi-finger nMOSFET transistors connected in stacked configuration, i.e. the transistor blocks are connected in series. Due to the critical location in the RF antenna front-end, an electrostatic-discharge (ESD) self-protection approach is the normal choice to not degrade the RF performance. This fact implies that the stacked devices must be studied in a broad bias operations to detect possible causes of weaknesses, high leakage and low ESD robustness.

In this thesis work, the ESD behavior of stacked multi-finger transistors for RF antenna switch applications for 0.13 μm bulk silicon technology is analyzed by means of a combinations of experiments and simulations. Several measurements technique are exploited for the investigation, like transmission line pulse (TLP) technique, transient interferometric mapping (TIM) technique and emission microscopy (EMMI) technique. Moreover, due to the complexity of the stacked devices, SPICE simulations are used to have deeper understanding of the transient evolution of all transistors belonging to the stacked configuration of CMOS blocks.

The reasons of weak product device performances are investigated on both single transistor device and stacked transistor test structures. Dedicated measurements are presented for creation of accurate models able to cover a wide operation range under ESD conditions and for calibration of TIM measurements. Thanks to all of this, we explain unique TLP waveforms and power dissipation on stacked devices discovering the impact of the interaction of the CMOS blocks via substrate.

Kurzfassung

Modernste Bulk-Silizium-HF-Antennenschalter werden aus Multi-Finger N-Kanal-MOSFET-Transistoren in gestapelter Konfiguration aufgebaut, d.h. die Transistorblöcke sind in Reihe geschaltet. Aufgrund der kritischen Position dieser Schalter im HF-Antennen-Frontend werden Selbstschutzschaltungen gegen elektrostatische Entladungen (ESD) eingesetzt um die HF-Leistung nicht zu reduzieren. Diese Tatsache impliziert, dass die gestapelten Transistoren in einem großen Operationsbereich untersucht werden müssen, um mögliche Ursachen von Schwachstellen wie hohem Leckstrom und niedrige ESD-Robustheit zu erkennen.

In dieser Arbeit wird das ESD-Verhalten von gestapelten Multi-Finger-Transistoren für HF-Antennenschalteranwendungen in 0.13um Bulk-Silizium-Technologie mittels einer Kombination aus Experimenten und Simulationen untersucht. Für diese Untersuchungen werden mehrere Messtechniken eingesetzt, wie die Transmission Line Pulse (TLP)-Technik, das transiente interferometrische Mapping (TIM) und die Emissionsmikroskopie (EMMI). Aufgrund der Komplexität der gestapelten Bauelemente werden SPICE-Simulationen verwendet, um ein tieferes Verständnis der transienten Entwicklung aller Transistoren zu erhalten welche zur gestapelten Konfiguration von CMOS-Blöcken gehören.

Die Ursachen für schwache Leistungsfähigkeit werden sowohl an Einzeltransistoren als auch an der gestapelten Konfiguration untersucht. Spezielle Messungen werden zur Erstellung präziser Modelle präsentiert, die einen großen Arbeitsbereich unter ESD Bedingungen abdecken können und die zur Kalibration von TIM-Messungen dienen. Darauf basierend präsentieren wir Ihnen einzigartige TLP-Wellenformen und den Leistungsverbrauch von gestapelten Transistoren, und leiten den Einfluss und die Interaktion zwischen CMOS Blöcken über deren Substrat her.

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Chapter 1

Introduction

1.1 Motivation

Our history has been shaped by the idea to face and solve common life problems and to satisfy needs in order to have a better and pleasant life. After detecting a problem or a need, we attempt to find possible solutions. These latter must be discussed, designed, implemented, tested and verified before their final usage. The technology has been, is and will be an important part of the human life as the carrier to implement the solutions.

Since the last decades of the past century, the technology progress and the feeling to improve the world assumed a fundamental role: increasing and fastening the communications, opening new possible way to treat diseases, improving and making the life easier in a way not imaginable in the past and unlocking new scenarios in our common daily life.

Among all new technologies, electronics is basic and it is not imaginable a world without. From advent of the first commercial semiconductor devices in the 1954 and the first transistor one year later [37], we have been able to speed up calculations and data processing, communication, data exchange, control, sensing the world surrounding us.

The role of the semiconductor devices as basic components in the communication is fundamental thanks to their reduced sizes, high performances, low cost fabrication and flexible work operations. The technology miniaturization, performance increase, low power consumption, high reliability are the key factors to fulfill new market and safety customer requests. In the last years, the research and the introduction of new materials such as Gallium-Nitride (GaN) or carbides is opening new scenarios on wide range of applications not possible with silicon devices. However, silicon is still paving the way of complementary metal-oxide-semiconductor (CMOS) technology as main semiconductor material thanks to its low cost, high performance and integration easiness. The knowledge about silicon benefits of decades of research and work. Therefore it suits to consumer electronics and several other applications, as also for state-of-the-art mobile communication. On the other hand, the research is still ongoing.

Every communications system has a front-end communication block. In a modern

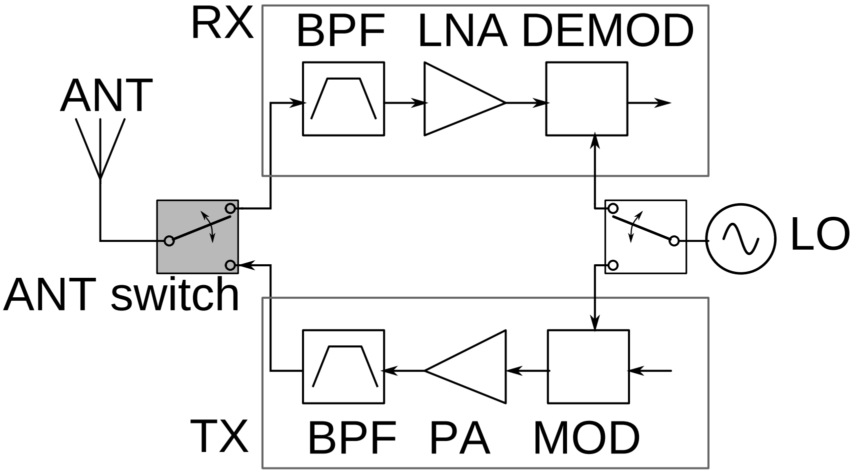

Figure 1.1: Simplified block diagram of an RF front-end. After the antenna (ANT) the ANT switch device select which path is enabled. Two paths are enlightened: the receiver (RX) path and transceiver (TX) path. In the RX path, the block are placed in cascade: the band pass filter (BPF), the low noise amplifier (LNA) and the demodulator (DEMOD). The local oscillator (LO) is connected to the DEMOD and to the modulator (MOD). This latter belongs to the the TX path with the power amplifier (PA) and another BPF.

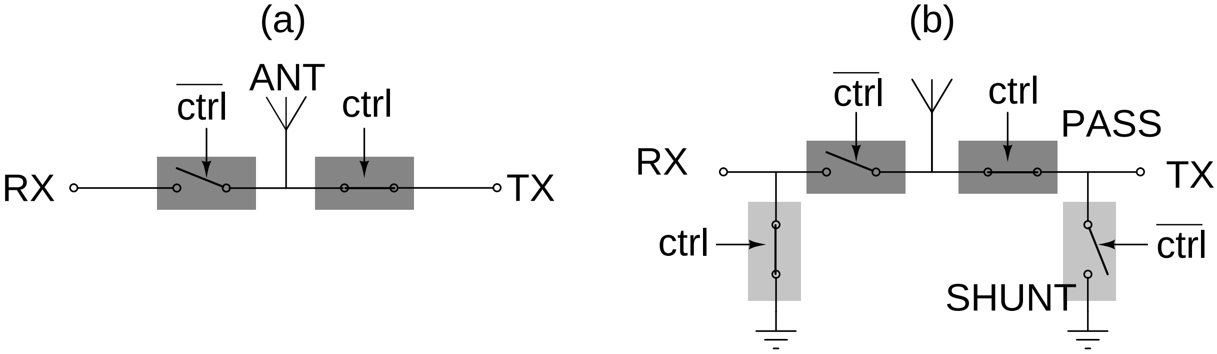

Figure 1.2: Single-pole-double-troughs configuration (SP2T) in (a) for the series configuration given by the pass switch and in (b) by the shunt-pass switch configuration. In (a), the control signal marked “ctrl” enables the transmission path from the transmission terminal (TX) to the antenna (ANT) and it disable the receiver path fron ANT to the receiver terminal (RX). In (b), the “ctrl” enables the PASS branch (corresponding to the transmission path), and it shunts to ground the SHUNT branch (corresponding to the receiver branch).

mobile phone, this is the radio frequency (RF) antenna front-end, see figure 1.1. A key role is played by the antenna switch which allows to receive or transmit data. This latter is the first integrated device from the antenna termination and it carries the RF signal from or to the next blocks. The basic RF antenna switch allowing the transmission and reception of data can be given by the so-called configuration single-pole-double-troughs (SPDT) configuration, where a node can be alternatively connected to a terminal or to the other one, see figure 1.2 where two configuration are depicted in figure 1.2(a) by the

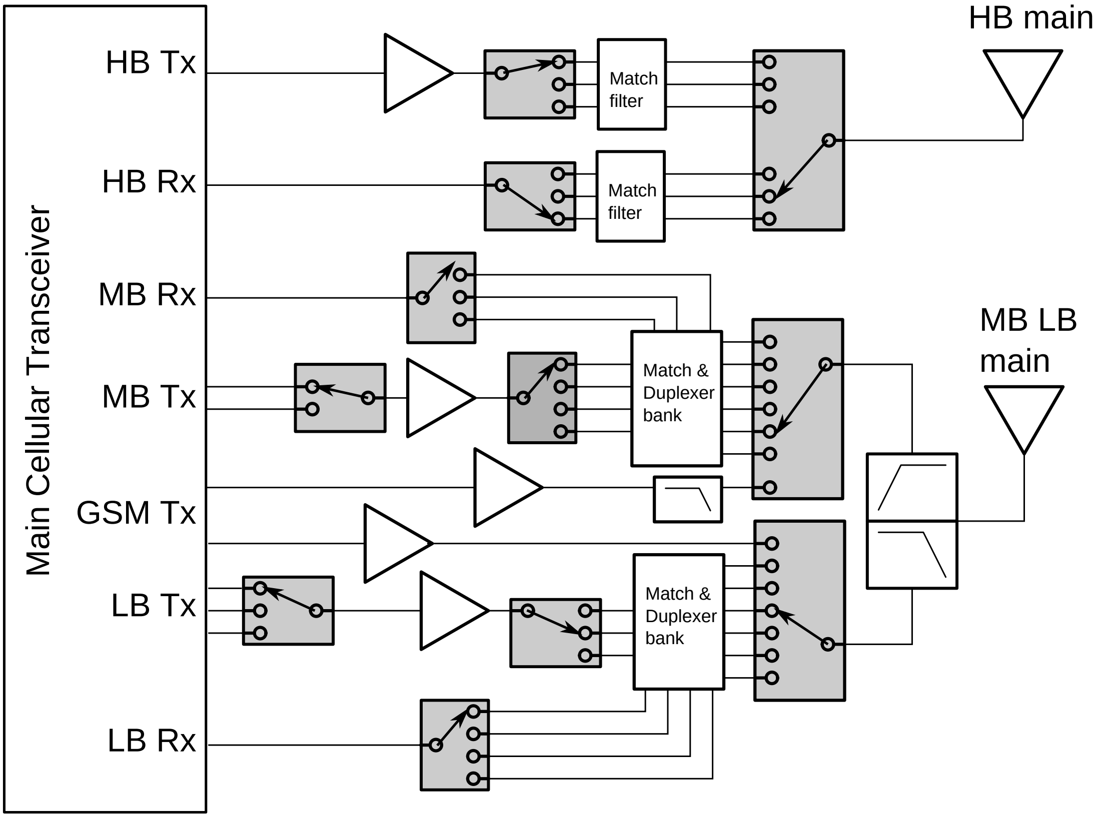

Figure 1.3: Modern mobile phone front end for low band "LB", mid-band "MB" and high band "HB" antennas paths [119]. The single pole multiple through (SPxT) components are gray filled and we note that they are placed close to the antennas but also in the front-end chain before main cellular transceiver.

pass configuration and in (b) by the shunt-pass configuration. Indeed, one of the two paths can be selected by the antenna switch. The paths are named as transmission path (TX) and the receiver path (RX).

The electronics progress with the new consumer needs brought in the middle of 2000s of the so-called smartphone era where multi-mode multi-band mobile phone RF front-end had to be implemented in order to exploit multi-band communication as depicted in figure 1.3. Therefore, the market required a SPxT configuration where the "x" stands for an multiple number of selectable communication bands or channels like for instance Global System for Mobile communications (GSM), Universal Mobile Telecommunications System (UMTS), Enhanced Data rates for GSM Evolution (EDGE). In figure 1.3, we can also note the multitude of SPxT switches employed for every path rising the system complexity.

Although the complexity and the functionality arise, all configurations present the antenna switch device. The state-of-the-art switches are implemented in CMOS substrate by stacked configuration. The choice of bulk substrate in respect to silicon-on-insulator (SOI)substrate cut significantly the production costs and furthermore it shows as high performance for high frequency operations as Gallium-Arsenide (GaAs) solutions. The stacked configuration is necessary in order to provide high radio frequency (RF) power handling due to the intrinsic low silicon breakdown voltage. Due to its critical location in the RF front-end chain, high electro-static discharge (ESD) robustness is required. Additional protection solutions are discouraged because they would lower the RF performance of the device. Therefore, a self-protection approach is required but this solution requires deep investigation to improve the ESD capabilities.

1.2 Scope and outline of the thesis

The scope of this thesis work is the analysis of RF CMOS stacked transistor switches under ESD by means of transmission line pulser technique (TLP) and transient interferometric mapping technique (TIM) at wafer level and at room temperature. Devices were built by a state-of-art 0.13 μm technology designed and produced by Infineon Technologies AG to fulfill the RF requirements for switches used in modern commercial smartphones.

To better explain the measurement results, SPICE-like simulations were carried out developing specific ESD device models. Besides this, accurate measurements were carried out on test structures in order to calibrate the model used during SPICE transient simulations to explain the power dissipation shown by TIM results and peculiar TIM optical response.

The thesis is organized as follows.

In chapter 1, a brief history of RF switches and circuit topologies is given as well as the ESD phenomena are presented. Electrical and optical measurement and simulation methods employed during the investigation are described here.

The beginning of the investigation is presented in chapter 2. The initial results on a devices belonging to a chip product are shown here. We encountered an inhomogeneous power dissipation with a localized hot spot which deserved to be clarified.

Chapter 3 presents the single transistor test structures investigated by means of TLP, DC and TIM measurements. The aim of these measurements was to investigate the drain breakdown phenomena in function of the gate status and bias condition for devices with different gate length and number of gate fingers. Thanks to these measurements, the drain breakdown model was developed to be applied during SPICE simulations for the transient analysis of stacked transistor test structures. A failure discussion for two gate status is also here presented at the end of the chapter.

We validated the developed simulation models in chapter 4, where we have analyzed the transient behavior distribution of a stacked transistor composed by 16 transistors. For the analysis, we used two sets of devices varying the space distance between two consecutive transistors.

In chapter 5, the analysis is reported for stacked transistor test structure devices similar to product with only 6 transistors connected in series. Then an experiment to reproduce the inhomogeneous power dissipation is proposed.

Conclusions and outlook are finally discussed in the chapter 6.

1.3 RF switches for mobile phone and wireless communication

Many kinds of semiconductor switches exist and they can be classified in different manners according to the base material (e.g. silicon, GaN, GaAs) or working principle (solid-state, electro-mechanical) or to the application (e.g. power, RF, digital, ...). However, they have in common the main purpose, that is to enable (ON-state) or disable (OFF-state) an electrical path between their two terminals.

The main function of an RF SPxT switch is to enable the connection of one receiver/transmission path with the antenna disabling the other paths. This is shown in figure 1.4, where the path ANT-RX01 is enabled. The example shows the use of transistors but similar behavior occurs also in presence of other semiconductor devices (e.g. PIN diodes as we will see in the follow). In figure 1.4(a), the path is enabled thanks to the activation of the pass device. In figure 1.4(b) we see the simplified model corresponding to figure 1.4(a). The activated pass device (colored in red) of figure 1.4(a) corresponds to the red R_{ON} resistor in the equivalent circuit of figure 1.4(b)). The shunt transistor from RX01 to ground results to equivalent to an off-state capacitance indicated by C_3 in the equivalent circuit in figure 1.4(b). The other pass branches (i.e. all others transistors laying in the paths ANT-RX0i, where i = 2, 3, 4, ...) result to be off and, in the equivalent circuit of figure 1.4(b), contributing to build the capacitance C_2. Finally, the shunt devices of path RX0i-ground (i.e. all devices connected with one terminal to ground and the other terminal to RX0i where i = 2, 3, 4, ...) contribute to the resistance R_2 in the equivalent circuit of figure 1.4(b).

Even though RF switches are not different than other switches in terms of main functionality, several more critical parameters come into play like switching speed, linearity, isolation and insertion losses [49].

To evaluate the performance of an RF switch, the following parameters are used [113]:

- the ability to provide a linear relation dependence between the RF input power and the RF output power is given by the *linearity*, however the most important parameter is the non-linearity to be checked by the measurements on the second-order intercept point (IP2) and third-order intercept point (IP3);
- the *switching time* is the delay between the the signal at the output port and that at the input port, as we will see in the following, this can be used as starting parameter

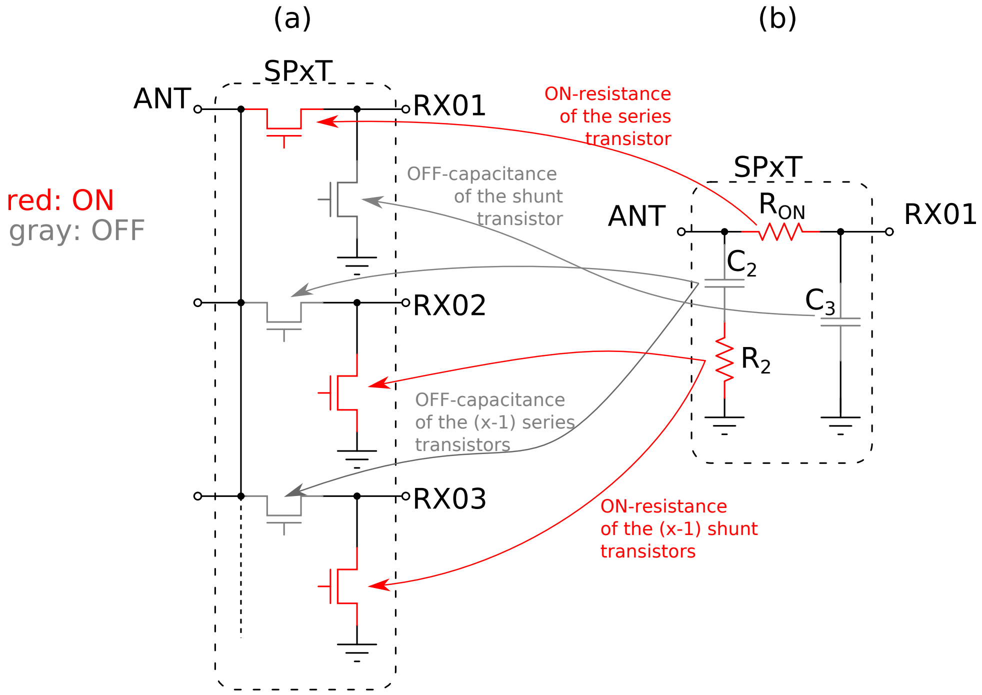

Figure 1.4: (a) single-pole-multiple-troughs (SPxT) configuration and (b) its equivalent RF circuit. The active transistors are colored in red, whereas the inactive ones in gray. Courtesy of W. Simbürger.

to design the switch;

- the *insertion loss* quantifies the signal power losses between the input and output port. Low insertion losses are important since they facilitate the work of LNA in the RX path (see figure 1.3), improving the receiver sensitivity (RX path) [63]. The low insertion loss becomes an important demand for commercial product for improving and saving the output power of power amplifier;

- the RF power leakage between the input port and to all other ports except the output port described by the *isolation*. This parameter is important to fabricate low-power consumption devices.

However, the final choice of the device topology is addressed to power handling capability and topology.

As compared with the series topology, the series-shunt topology improves isolation but increases insertion loss, especially at high frequencies.

1.3.1 RF device solutions to implement a solid-state switch

Since the introduction of PIN diodes in the 80s [44] as RF switches, many solutions were implemented in terms of cost reduction and RF performance and diversity purpose in order to fulfill the new mobile phone and wireless communication standard requirements. The technology improvements and the layout circuit design optimization allow to evolve the mobile phone from an analog communication device into the so-called smart-phone with multi-purpose applications and now the development of the fifth generation (5G) of wireless systems [76, 77]. Besides these aspects, the reliability of these devices was also improved adopting optimized technologies.

In the following several implementation adopted during the years are presented.

RF PIN diodes The first RF switches were implemented by vertical PIN diodes in Gallium-Arsenide (GaAs) [61, 62] and afterwards in silicon technology as in [43]. They showed good small signal performances and linearity [44]. An example of SP2T with PIN diodes is presented in figure 1.5. The two paths, one between the ANT pad and $(RX/TX)_1$ and the other one between the ANT pad and $(RX/TX)_2$, are alternatively enabled by the high signal indicated by bias voltages V_{B1} or V_{B2}, respectively. To enable a path, the high signal on one bias voltage forces the diode in forward bias conduction. At the same time, the other diode is counter polarized, hence disabling the other path. The capacitors are placed in such configuration in order to decoupling DC signal components from the RF path. The inductances avoid to decouple the RF components going towards V_{B1} and V_{B2}. The monolithic configuration proposed in [45] embraced the stacked configuration in order to be able to handle high RF voltage when biased in sub-threshold regime [86]. The stacking configuration, i.e. the series connection of devices is also meant to prevent the switch to work in breakdown already in RF operation to increase the total breakdown handling capability. However, PIN diodes were not enough to reach low power consumption in forward bias operation and also wide integration is not possible due to the dimension of the inductances required and the high intrinsic region to sustain high reverse voltage during the OFF-state operation. For these reasons, integrated solutions using PIN devices were abandoned especially for GSM and UMTS applications.

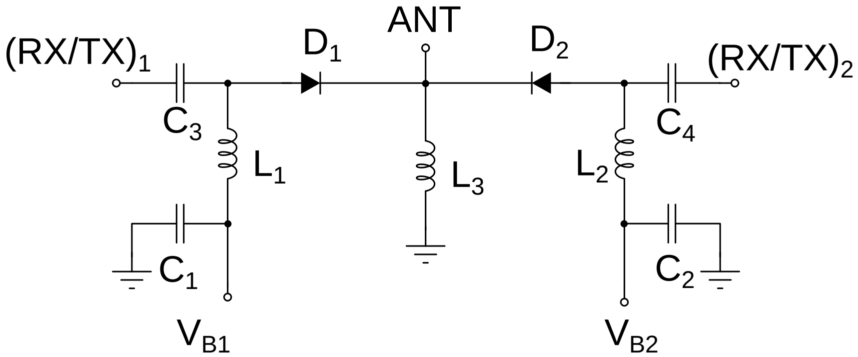

Figure 1.5: Single-pole-double-troughs configuration for a GaAs PIN diodes. The path RX/TX with

GaAs pHEMT A monolithic GaAs metal-semiconductor-field-effect-transistor (MESFET) based SPDT was reported in [61] where each shunt and pass devices were a GaAs transistors. Sometimes they are also called pHEMT standing for pseudomorphic high electron mobility transistor. A GaAs pHMETs is a three terminal transistor where the RF signal passes through the channel between drain and source nodes and the control whether the RF path is enable is given by the gate node. In [61], each pHEMT was connected in series to a 2 $k\Omega$ gate resistor to isolate the RF path from the gate control circuit as drawn in figure 1.6.

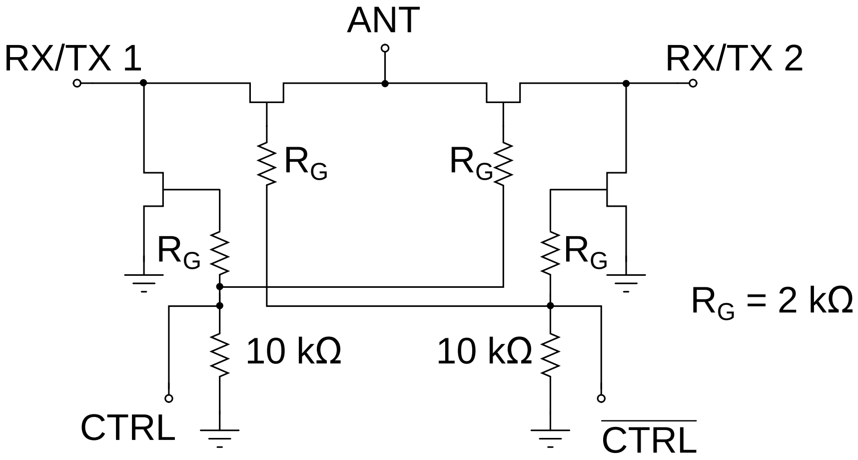

Figure 1.6: Single-pole-double-troughs configuration for a GaAs pHEMT as in [61] with RX/TX using the shunt-series configuration to improve isolation. Every shunt pass and pass devices are given by a GaAs pHEMT with a gate resistor $R_G = 2\ k\Omega$ and a 10 $k\Omega$ resistor connected to ground.

The continuous demand of higher performance devices brought to the definition of the new standards where multiple and higher frequency operations where required. Moreover the available size in the modern mobile phone required to be able to integrate the switch with its logic control (to generate the signal *ctrl* and $\bar{ctrl}$) and level shifter into the same chip. This is not cost-effective in GaAs technology devices like pHMETs and therefore, silicon solutions appeared into the market at the end of 2000s.

CMOS stacked transistors In state-of-the-art antenna switch applications, the bulk substrate metal-oxide-semiconductor-field-effect transistor (MOSFET) device is preferred as component of the switch in respects to others integrated electronics devices thanks to its low power consumption, easy voltage control by the gate terminal and high-frequency switching operation. CMOS stacked transistors employ n-channel transistor due to their higher mobility and therefore lower R_{ON} compared to p-channel transistors. Due to the low breakdown voltage of CMOS transistors, the stacking circuit configuration was introduced to withstand the high RF voltage [68, 69]. These choice resulted beneficial also to reduce the fabrication costs and to increase the integration [39].

The isolation requirement for low power consumption led to different substrate solutions, such silicon-on-sapphire (SOS), silicon-on-insulator (SOI) and high resistive bulk silicon CMOS. The SOS solution was used for instance in [42, 81] at the beginning of 2000s but it was fastly replaced by the SOI solutions as in [60]. In SOI solutions, a buried oxide layer of 1 μm as in [45] is introduced into the silicon substrate in order to isolate the device channel from the substrate. The body of the SOI is let floating [88] to mitigate the short channel effect for high body bias[1].

In RF transistor switches, there are two main sources of insertion loss: the first is the drain-source capacitance C_{DS} (for off-state) and the second are the substrate losses. The series of C_{DS} impacts on the overall C_{OFF}. The C_{DS} can be reduced as suggested in [38] removing the punch-through stopper and p^+ substrate isolation. The C_{DS} is very important in the stacking configuration, since it must be small compared to the C_{OFF}, in order to ensure an even voltage division [42]. However this solution cannot be implemented in device with low L_G as to be $0.13\mu\ m$ due to the high risk of punch-through effect which can result in poor, for example, ESD performances due to early breakdown phenomena.

High resistive substrate stacked transistors Infineon Technologies AG was and is producing RF front-end effective solutions. The studied devices used for RF antenna switches were implemented by C11NP 0.13 μm technology [82–85] on high resistive substrate. The schematic circuit of a stacked transistor used in the shunt branch of a SPxT is depicted in figure 1.7. To each transistor, a series resistor R_G is connected to the gate and a drain resistor R_D to the drain pin of each transistor (the drain pin is the upper pin of each transistor) to ground. The function of R_D is to provide a discharge path for each drain capacitance to ground during the OFF-state operation. This configuration is called *parallel configuration* due to the connection of all R_G. An updated configuration called *star gate configuration* includes the common R_{G2} but this latter is not studied in this work.

In order to reduce the capacitance during operation, the transistors are built onto a high resistive silicon substrate with $\approx 10^{14} cm^{-3}$ doping concentration. Moreover, the bulk contact is placed far away from the stacked transistor to a distance of at least 100 μm depending on the chip. The reason is to avoid inhomogeneous power dissipation during ESD operation due to localized parasitic bipolar action. This substrate solution approach is unique in the world because most of the commercial or in-development solutions are using SOI substrate. The bulk silicon approach leads also to a sensible cost cut due to the cheapest substrate solution.

Design of RF stacked switches Given the technology, the design of such devices is focused on layout parameters as the number of transistors N, the total gate width of each

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[1] However, the floating-body effect is well known in RF literature as in [60]. The accumulation of holes in the substrate can lead to off-state leakages and afterwards also to a parasitic bipolar transistor triggering, resulting in higher current consumption.

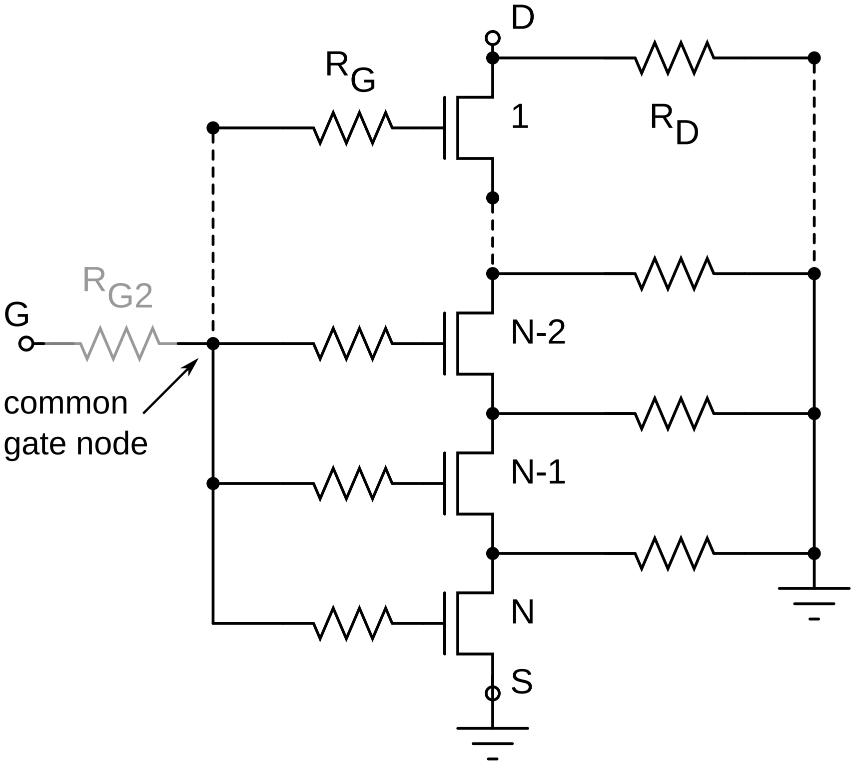

Figure 1.7: Schematic diagram of a stacked transistor used in the shunt branch of a SPxT. For shortness, only last three transistors ($N-2$, $N-1$, N) with their drain resistors R_D and series gate R_{G1} are drawn. The configuration without the resistor R_{G2} is called series gate configuration. Including the common gate resistor R_{G2} it is named gate-star configuration. The studied devices used for this thesis work were not provided with R_{G2}. Therefore the gate pad was directly connected to the common gate node.

multi-finger transistor W_{TOT} and the values of gate resistors. In the studied devices, there is no R_{G2} and the gate pad is directly connected to the common gate node indicated in figure 1.7[2]. Two main requirements are provided: the RF power handling and the turn-on t_{ON} time of the stacked configuration[3]. By the RF power handling $P_{RF,MAX}$, the maximum RF operative voltage $V_{RF,MAX}$ is derived by

$$V_{RF,MAX} = \sqrt{2P_{RF,MAX}Z_L} \tag{1.1}$$

where Z_L is the characteristic impedance (generally 50 Ω). Knowing that the RF breakdown voltage $V_{BD,RF}$ of such technologies is $\approx 1.5\ V$, N is given by

$$N = \frac{V_{RF,MAX}}{V_{BD,RF}}. \tag{1.2}$$

---

[2] State-of-the-art configuration includes R_{G2} in order to uniform the working point of each transistor of the stacked configuration.

[3] According to the requirements, the power handling can be in the range of 10 dBm, whereas the turn-on time can vary in between 500 ns and $1-2$ μs but sometimes higher higher to maximum $4-5$ μs.

The t_{ON} provides the value to design[4] the product $R_G \cdot C_G$ to derive the transistor width by the total gate capacitance C_G [80]. High ohmic resistors are used (in the $\approx 100\ k\Omega$ order of magnitude) in order to effectively decouple the RF gate voltage signal. The R_D value is chosen high enough in order to keep low insertion factor during RF operation. Therefore, it is also in the $\approx 100\ k\Omega$ order of magnitude.

The parallel (or gate star) configuration is not the only choice to implement the stacked configuration. Another stacked configuration using an R_G connected in *series configuration*, i.e. between two consecutive transistors as in [114], can be employed. However, this solution is extremely hard to use whenever high $V_{RF,MAX}$ requirements are provided. The series configuration solution showed a too-long t_{on} proportional to N^2 [115], see also appendix A. In practice, this solution is reasonable only for a small number of transistors and therefore almost never employed for antenna switches.

In the following, the RF working condition is explained for a typical device for C11NP technology.

In ON-state, the device is biased by a positive voltage of $V_G = 1.5\ V$ due to the threshold voltage of $0.3\ V$. The RF signal can travel along the formed gate channel to the load. As said, the high value R_G resistors prevent to have DC power dissipation at the gate and decouples the RF signal due to the presence of the gate-bulk capacitance C_{GB}. The inclusion of high R_D resistors and high R_G resistors together makes the device swinging with the RF signal. In order to prevent the turn-on of the body diodes in case of negative RF signal, the bulk substrate must be high resistive and biased with negative voltage (in our case $-3\ V$) by the charge pump. Thanks to that, the C11NP technology behaves like a RF-SOI CMOS process and the stacking can be used to achieve high RF voltages in OFF mode.

In OFF-state, the gate is biased by $-1.5\ V$[5]. In this situation, the device shows a capacitance given by the series of the gate-source and gate-drain capacitor of each transistor and the body capacitances. In both operation conditions, particular attention on the gate bias voltage should be taken into account by the possible gate oxide (GOX) breakdown and failure. The values depend on the gate oxide thickness t_{ox} which is 2.2 nm for the transistors used in the stacked configuration.

1.4 ESD and methods

Every time that two electrically charged objects at different potentials get in touch, a flow of electrons occurs for a short time. This current flow event is called electrostatic discharge (ESD). ESD events span from the lighting in the sky (thanks to the presence of

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[4] The t_{ON} was derived for several stacked topology circuits and reported in appendix A.

[5] As a comparison, in SOI devices as in [88], high V_G is used for on-state due to the fact that $t_{ox} = 5.2\ nm$ for a 180 nm technology. For the same reason, the off-state requires $-2\ V$.

air as a dielectric mean between the charged cloud and the grounded Earth) to these of somebody walking on a carpet. As example to understand the order of magnitude, this latter action brings to 7.5 kV electrostatic potential (at 55% humidity condition) [52].

Even though they occur in the nanosecond time domain, ESD events occur very often and in an uncontrolled way. These phenomena impact and affect the electronics devices and integrated circuits (ICs) because they can lead to defects, bad-functioning and maybe permanent damage due to the high density of energy dissipated. Despite the improvements during the production, the technology advancement and the experience, a percentage comprised between 30% and 40% is the amount of failure in IC and electronics devices addressed to ESD events [64, 65]. Besides, it might occur also during the fabrication phase, for example when they are handled or moved by one machine. Therefore, ESD models were developed during the years in order to reproduce similar ESD stress conditions on the devices under test (DUT) by a lumped equivalent circuit. From the model, the requirements and the measurements methods to test the devices are defined by the industry community.

For all these reasons and according their function and requirements, electronics devices and ICs should fulfill minimum ESD safety robustness.

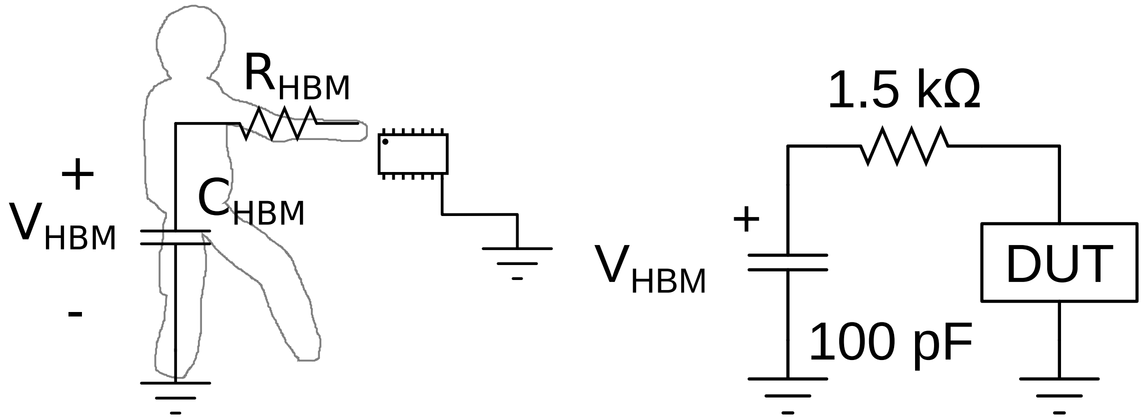
1.4.1 ESD models

Component-level human body model The human body model (HBM) aims to reproduce the discharge of a charged human being touching a DUT with a finger. As enlighten by studies in the 70s in [70], a human being can be charged around $0.6\mu C$ giving rise to several kV voltage peak on the DUT [51]. Nowadays, the HBM requirements are around $1-2$ kV.

The equivalent circuit reproducing this behavior is shown in figure 1.8b consisting of a charged 100 pF capacitor (modeling the capacity of the human body) by V_{HBM} discharging on the DUT by a 1.5 $k\Omega$ resistor (modeling the skin finger resistance, see it in 1.8a). The HBM stress is a slow transient stress in the order of hundred nanoseconds. A simulated current transient example for $V_{HBM} = 1$ kV on 50 Ω resistor is displayed in figure 1.9a. The standards regarding this model can be found in [125]

This investigation method was not used for this work because of the non-flat characteristic of the waveforms. However we employed the TLP method as electrical stress supplier to the DUT. Nevertheless, the TLP method provides an equivalent energy threat to the DUT as the HBM [71], therefore the failure results are related.

Other ESD models Additional ESD models cover the HBM at a system level, like the standard IEC 61000-4-2 as described in [116]. This model is characterized by a strong current peak in the first nanoseconds and high energy as can be seen by simulation in figure 1.9b for a 8 kV stress level on a 50 Ω resistor. An external ESD protection is



(a) Human charged by V_{HBM} inducing an electrostatic discharg on a chip by touch.

(b) HBM equivalent lumped model circuit. The device under test is indicated by DUT. Note that the 100 pF capacitor is charged at V_{HBM} voltage and it discharges to the DUT by a 1.5 $k\Omega$ resistor placed in series.

Figure 1.8: Human body model (HBM).

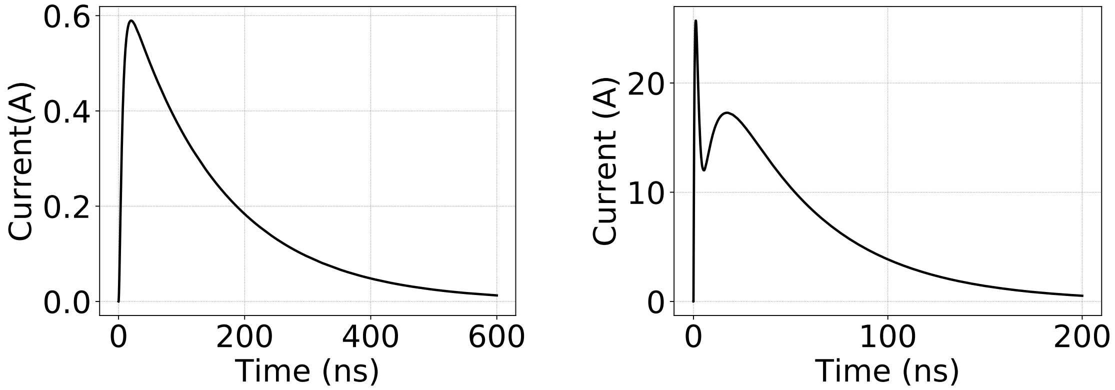
required in this case.

Another example is the charged device model (CDM) aiming to reproduce the situation of a machine/robot handling a component or a wafer, for instance in a semiconductor production site. A simulated example of this model is provided in figure 1.9c for a stress level of 500 V. As one can see from figure 1.9c, such model is characterized by a fast and intensive current variation. The standard JESD22-C101 [126] describes this ESD model.

1.4.2 Investigation methods

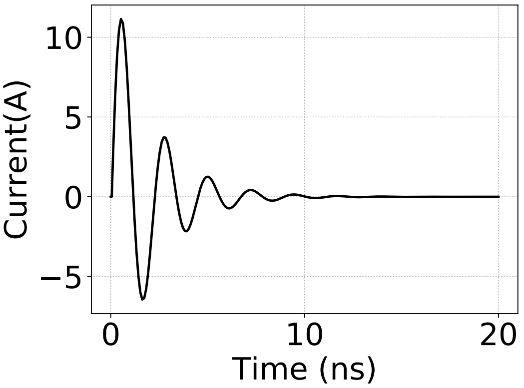
Electrical pulsed characterization by TLP The research requires measurement tools able to reproduce ESD-like pulses with the possibility to vary the pulse length, the rise time and the load line. The reason is to enlighten possible danger or critical behaviors of the DUT in conditions maybe outside of the HBM conditions but still relevant and interesting in the full ESD understanding of the DUTs. Thanks to the TLP method, we could have a wide variety of pulse parameters.

Since its introduction in 1985 by Khurana and Maloney [36], the TLP method has gained more and more importance in the ESD research thanks to its easiness, flexibility and possibility to build the quasi-static characteristic of the device under test (DUT). The main feature of this technique is to be able to supply trapezoidal voltage pulses onto a defined load line generally it is 50 Ω) given by characteristic impedance of the transmission line employed. Thanks to this, high current conditions can be generated on the DUT, and studied in the transient regime applying increasing the amplitude of charging voltage pulses. A TLP measurement consists on a series on increased amplitude voltage pulses until the failure occurring at the current and voltage indicated by I_{t2} and V_{t2}, respectively.



(a) Simulated HBM current waveform for $V_{HBM} = 1\ kV$ on 50 Ω resistor.

(b) Simulated IEC current waveform for $V_{IEC} = 8\ kV$ on 50 Ω resistor.



(c) Simulated CDM current waveform applying $V_{CDM} = 500\ V$ on short circuit load.

Figure 1.9: Simulated ESD current waveforms using different ESD models.

For every TLP pulse, the measured voltage on device under test V_{DUT} and current I_{DUT} are averaged in a certain time window providing the quasi-static TLP-IV characteristic of the device under test [54], see figure 1.10.

The pulse of amplitude V_{CH} is obtained by the discharge of a charged transmission line cable. The transmission line cable length (L) is adjusted according to the required pulse width (PW) by the formula:

$$PW = \frac{2L}{v} \approx \sqrt{\epsilon_r} \cdot \frac{2L}{c} \tag{1.3}$$

where the v is the propagation velocity, ϵ_r is the relative dielectric constant of the inner insulator of the the transmission line (generally Teflon is employed showing a $v \approx 0.2m/ns$ [28]). Exploring the device failure and TLP-IVs for different time stress duration (i.e. TLP PW), one can reconstruct the Wunsch-Bell failure behavior [10, 31] and have precious information about the failure reasons (i.e. thermal versus non-thermal).

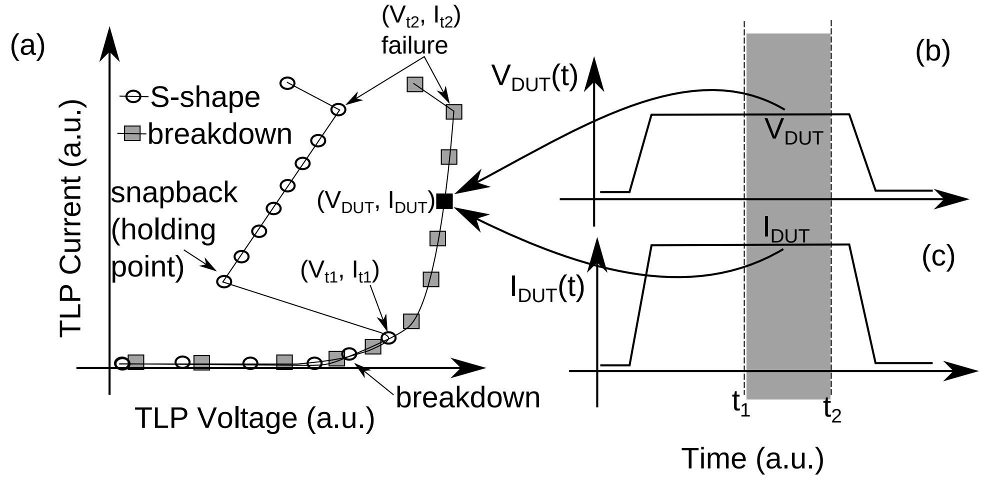


Figure 1.10: (a) TLP-IV plot with two possible behavior: an example of *S-shape* characteristic is reported in dotted line, where we see the snapback point, whereas the squared line represents a device with a simple breakdown characteristic. (b) and (c) plot indicates the device transient current $I_{DUT}(t)$ and voltage $V_{DUT}(t)$. The TLP-IV is obtained by the averaging of voltage and current waveforms in the same time interval (t_1, t_2) getting the point (V_{DUT}, I_{DUT}).

A proper cascade of LC filters, as explained in [50], can tune the rise time (RT) and fall time. The RT variation can give information, for instance, whether the failure might be related to possible dV/dt effects as in [21, 120, 121]. RT values can span from 300 ps to 50 ns. Generally, the falling time is the same as the RT.

Therefore, every TLP pulse is characterized by the following four parameters: V_{CH}, PW, RT and load line. In this thesis work, we mainly use $RT = 1\ ns$ and $PW = 100\ ns$. However, interesting studying are carried out also for $RT = 10\ ns$ or using different PW at $25, 50, 75, 450, 650, 840\ ns$. The reasons will be clarified in the following.

The TLP pulser used for this work is an HPPI TLP pulser [28] with maximum $V_{CH} = \pm 750\ V$ using standard 50 Ω load line.

A TLP measurements is carried out alternating increased amplitude TLP pulses and DC leakage measurements. The TLP pulses are applied to the device, short DC leakage measurements are used to control the status of the device. Amplitude increasing V_{CH} pulses are applied to the DUT with a $0.1 - 1\ s$ time period. DUTs pads are contacted by RF needles. In our setup, we use a signal-ground 50Ω Picoprobe model 10 needle to carry the pulse to the DUT. The I_{DUT} is sensed by the CT-1 current probe [27] when $PW \leq 250\ ns$, otherwise the CT-2 is employed [27]. The voltage is sensed by the 4 point probe configuration method [75] by $5k\ \Omega$ Picoprobe® Model 10 tip as described in [28]. Voltage and current waveforms are collected by digital signal oscilloscope (DSO) set with 50 Ω input impedance.

Transient interferometric mapping technique The transient interferometric mapping (TIM) technique [17] is a backside laser-probing interferometry technique, that measures the local transient variation of the semiconductor refractive index Δn due to temperature variation or free carrier concentration. The temperature variation and free carrier concentration are probed during an electrical well-defined stress pulse, for instance a TLP pulse. The DUT is probed by a laser with wavelength $\lambda = 1.3\ \mu m$ placed in a interferometer setup. Thanks to this choice, the DUT substrate is transparent for the laser beam for all materials showing an energy band gap $E_g > 0.95\ eV$, among all the silicon[6] for low substrate doping. For this reason, the TIM technique is considered a non-invasive optical technique. The investigation can be carried out both at wafer level or bonding the DUT on a printed circuit board (in this thesis work, only wafer level measurements were carried out). Anyway, the wafer or the portion of wafer must be polished from the backside in order to reduce the laser beam scattering due to the roughness of the backside surface. This technique is suited for ESD investigation, since it has 3 *ns* time and 1.5 μm space resolutions [17] making it a unique technique in the world to investigate such phenomena.

The electrical stressing of DUT brings to a local temperature variation ΔT due to heat dissipation and/or local free carrier generation. In [72], the refractive index over the variation of temperature $\partial n/\partial T$ was studied and it was reported to be $1.9 \cdot 10^{-4} K^{-1}$ for $T = 320K$ for silicon. This effect is called thermo-optical effect. On the other side, the plasma-optical effect takes into account the dependence of the refractive index by the free carrier generation from injection [74] of electrons or holes. In our case, the local temperature increase is dominant in respect to the free carrier effect signal. This latter phenomenon can be encountered for instance in silicon-controlled-rectifiers (SCRs) devices as enlighten in [19, 67]. This refractive index variation due to free carrier signal presents a negative dependence. Since the two effects show opposite signs, it allows to easily discriminate them.

The local transient refractive index variation $\Delta n(x, y, z, t)$ in a medium is therefore expressed by the sum:

$$\Delta n(x, y, z, t) = \Delta n_{th}(x, y, z, t) + \Delta n_e(x, y, z, t) + \Delta n_h(x, y, z, t) \tag{1.4}$$

where $n_{th}(x, y, z, t)$ is the contribution due to thermo-optical effect and the two other contributions are associated to the plasma-optical effect for electron and holes, respectively.

The tool to detect the transient refractive index variation is the heterodyne interferometric setup proposed in [66], see the schematic optical setup in figure 1.11a. The measurement principle follows. A scanning path to probe and a stress level for constant TLP charging voltage and TLP parameters are defined. For every defined path position, the same TLP pulse is applied to the DUT and its voltage and current waveforms are collected by a digital oscilloscope as well as the heterodyne signal from the detector. In order to improve the signal to noise ratio, for every point repetitive TLP pulses are applied

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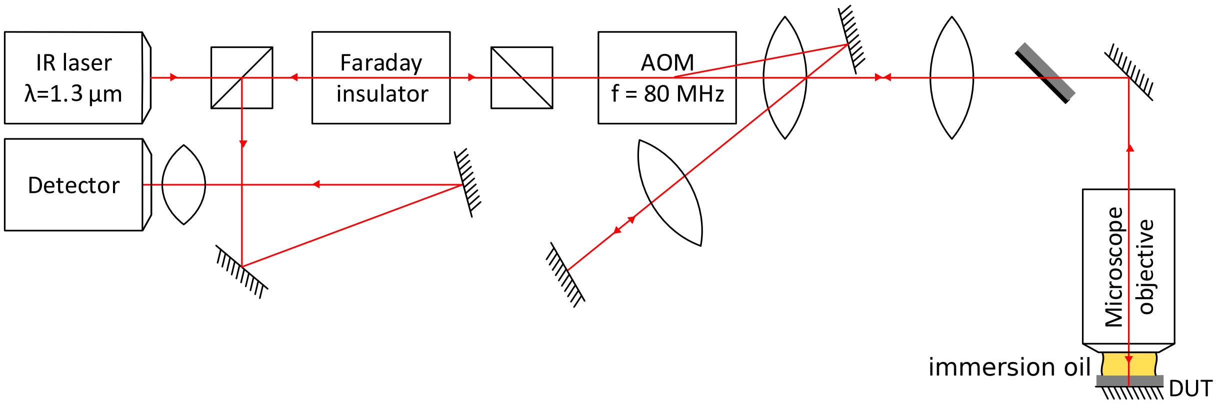
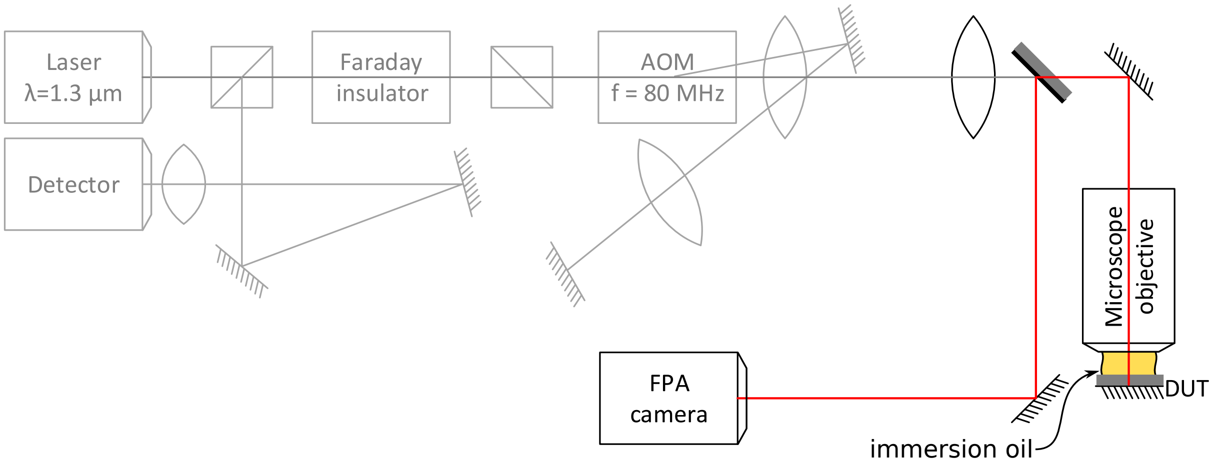
[6] The silicon energy gap $E_{G,silicon} = 1.1\ eV$ [24], hence it is transparent for $\lambda = 1.3\ \mu m$.



(a) Simplified optical TIM setup.



(b) Simplified optical EMMI setup.

Figure 1.11: Schematics of optical investigation setups employed. The activated optical paths are indicated by red lines.

and collected. The collected waveform are then averaged by a Matlab in-house developed program [17]. For this thesis work, at least 15 pulses per positions are collected. Moreover in order to verify the status of the device (e.g. increase or decrease leakage, disconnection, degradation, failure) a short DC IV is measured after every single TLP pulse or, to speed us the measurement, after completing the scan at each scanning position. The drawback of this scanning feature point-per-point is the possible cumulative damage that the DUT can suffer.

The backside laser probing beam is reflected back thanks to the metalizzations above the semiconductor device active region. In this way, the beam travels twice the same path. By this setup the transient spatial phase shift variation $\Delta\phi(x, y, z, t)$ of the probing backside laser beam can be measured and related to the optical path length and in turns to the local transient reflective index variation. Together, they provide [73] the equation:

$$\Delta\phi(x,y,t) = 2 \cdot \frac{2\pi}{\lambda} \int_0^L \Delta n(x,y,z,t)\,dz \tag{1.5}$$

where coefficient 2 takes into account the forward and back travels of the laser beam; λ is the laser probe beam wavelength and the integral is carried out along the z direction parallel to the beam direction between the backside beginning of the wafer ($z = 0$) and the topside end of the wafer ($z = L$). In case of pure thermal contribution Δn_{th}, equation 1.5 can be rewritten and, as derived in [19] from the heat equation, it becomes:

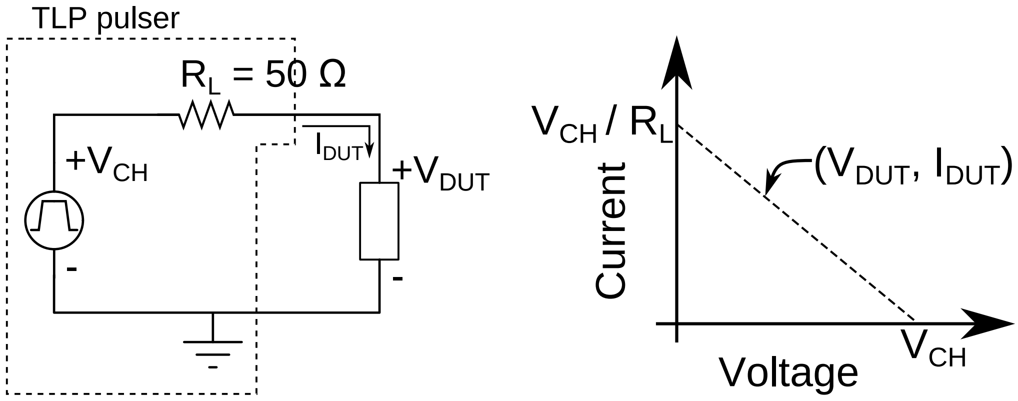
$$\Delta\phi(t) = 2 \cdot \frac{2\pi}{c_V \lambda} \frac{1}{A} \int P(t)\,dt \tag{1.6}$$

where c_V is the silicon volume specific heat coefficient, A is the area of device where the heat takes place and $P(t)$ is the total dissipated power in the active area A. Assuming that $P(t) = V_{DUT}(t) I_{DUT}(t)$ where $V_{DUT}(t)$ is the device transient voltage and $I_{DUT}(t)$ is transient current a relation between $\Delta\phi(t)$ and the device voltage and current waveforms exists.

Pulsed emission microscopy (EMMI) Another useful non-invasive optical technique used in this thesis work is the pulsed emission microscopy (EMMI). It is well-known from literature that CMOS devices working in breakdown emit infrared light where the current flows [78, 122]. The resulted EMMI pattern can be homogeneous in case of homogeneous or inhomogeneous current flow.

The infrared EMMI light is detected by an InGaAs focal plane array (FPA) camera, see the simplified optical EMMI setup in figure 1.11b. The use of pulsed EMMI was very useful thanks to its *quick* and *live* results, since the IR frames collected by the FPA camera are displayed on a TV screen allowing to the user to have answers in real-time. In this thesis work, the pulsed EMMI complements TIM technique to get quick answers as we will see in chapter 5, where precise EMMI pattern can be seen. This fact allows to have fast results to visualize inhomogeneous current flow or to possible failure locations, as in [79] for failure analysis.

SPICE transient simulations SPICE-like transient simulations allow to have insight on electric parameters like internal voltage or current for ESD analysis, as well as to tune certain model parameters in order to know how to modify the physical parameters to fulfill the ESD requirements. As we will see in the following, the complexity of the studied devices requires the use of an electrical circuit simulation tool to have deeper insight of quantities not directly or indirectly measurable by TIM. Advanced Design System from Keysight Technologies fits our needs and moreover, a basic RF model of the multi-finger transistor was already available. This software is one of the most widely simulation software employed in industry and academy to simulate RF devices and circuits.



(a) Equivalent circuit to simulate a TLP pulses in [36] on a device under test. The ideal TLP pulse of V_{CH} amplitude is given by an ideal pulse generator and a load resistor $R_L = 50\ \Omega$ connected in series.

(b) Lumped equivalent model of the TLP tecnique. Given a load line resistor, as indicated in (a), the maximum voltage available to the device under test is given by V_{CH} equivalent to the open circuit condition, whereas the maximum current $I_{DUT} = V_{CH}/R_L$. The (V_{DUT}, I_{DUT}) lays on the line between this two points/conditions.

Figure 1.12: Transmission line pulse (TLP) technique.

In this, work, we will use the transient simulations, to have insights of the parameters that cannot be detected by TIM, like the V_{GS} in a MOSFET with gate non connected to a fixed voltage bias. Therefore, SPICE transient simulations are used as complement of the TIM technique. Furthermore, the relation of the phase shift with the power dissipation [19] from equation 1.6 consents to verify the agreement between measured phase shift extracted from TIM measurements and simulated phase shift.

The TLP pulser was simulated by its equivalent circuit given by the series of an trapezoidal wave voltage pulse source and an ideal 50 Ω load resistor [36], see figure 1.12a. This choice has been done in order to simplify the simulated TLP circuit. The trapezoidal wave voltage pulse source is characterized by its amplitude V_{CH} corresponding to the the TLP charging voltage, its pulse width PW and its rise time RT and falling time FT. The rise time edge was chosen to be sinusoidal and set to be $FT = RT$. The load resistor R_L has been modeled by an ideal 50 Ω resistor. As a matter of fact, we use the same TLP parameter notations for simulations and measurements.

The load resistor limits the possible voltage and current values on the device under test (V_{DUT}, I_{DUT}). The maximum voltage available to the device under test is $V_{DUT} = V_{CH}$ occurring as in an open circuit configuration, whereas the maximum current occurring is $I_{DUT} = V_{CH}/R_L$ as displayed in figure 1.12b.

As further parameter for the simulations, the time incremental step used during simulations has been set to be 0.2 ns. This value is a good compromise to have smooth curves and precise simulations in the *ns* time regime and to keep the simulation time to a couple of seconds.

The simulations were carried out at isothermal conditions.

1.5 Literature overview on ESD on RF stacked switches

Despite the critical location in the RF antenna front-end as first/last device in the RF front-end, few ESD results on RF switches were reported in literature. Results on stacked devices are of interest in order to try to compare different technology and layout solutions. Most of literature deals with devices working on SOI substrate or previous configurations adopting GaAs. Therefore, the uniqueness of choice of the bulk substrate makes the study on bulk substrate very interesting. Furthermore, previous results on SOI devices mainly focused on the RF topics like RF breakdown and maximum linear RF output power. Anyway, his information can be linked to ESD analysis. All these points make the ESD knowledge of RF stacked transistor device limited and necessary to expand.

The off-state RF voltage imbalance is a well-known problem of any stacked configuration [60][7].A voltage imbalance occurs whenever a voltage (in our case we consider each V_{DS} of transistor) is not evenly distributed. The voltage imbalance causes that the breakdown voltage (and the failure) of the stacked devices is no longer linearly proportional to the number of stacked transistors, but rather it presents a sub-linear dependence meaning lower ESD performance [90, 93].

In [88], the uneven V_{DS} distribution during RF operation is studied for devices with 12 stacked transistors. The authors showed that:

- the transistor close to the drain pad (where the signal input is applied) presents highest V_{DS} and
- the V_{DS} of the i^{th} $V_{DS,i}$ gradually decreases towards the last transistors where there is the grounded side .

The authors proposed to connect feed-forward capacitors in correspondence of gate-drain junction of the 1^{st} and 2^{nd} transistors. Thanks to this circuit modification, a 8.5 kV ESD results was reached ensuring also good RF performance. In the solution reported in [91], authors varied each transistor periphery (i.e. layout parameters like the number of fingers or the total gate width) rather than adding external feed-forward capacitors, obtaining a result close to the linear breakdown dependence. However, details of the new geometry were not provided.

Another issue mentioned in [93] is the possible GOX breakdown of the first transistor in the chain due to the high voltage excess. Here, the suggested solution is to add

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[7] The voltage imbalance affects the device linearity quality.

ladder capacitors in the order of $1 - 2\ pF$ in parallel to every drain-gate and gate-source junction to balance the $V_{DS,i}$ along the transistor chain. ESD improvement until 10× was achieved. The price paid is a significant amount of chip area consumed to include the ladder capacitors.

In [89], transient voltage waveforms are reported, but they show only the RF voltage swing.

A part from that, no detailed analysis of ESD in the time domain has been presented in literature for RF stacked devices for antenna switch application. Performance and final final failure level are just provided without any insight on the behavior of each transistor forming the stacked device during ESD operation. Such lack wanted to be filled by this work.

1.6 ESD self-protection approach for RF devices

As previously mentioned, the RF antenna switches cannot be ESD protected by external component. External components are discouraged to use because of the worsening RF performance and also due to the reduced size of the chip. For instance for digital applications, external transient voltage suppressor (TVS) diodes are an effective solution. However, they do not meet the linearity requirements [93] for an RF switch. Anti-parallel stacked diodes and SCRs [93] are other RF solutions used, but not suited to withstand the strict RF requirements at the RF antenna front-end [93]. For these reasons, the ESD self-protection approach at component level is the obvious approach to fulfill ESD requirements[8].

For a self-protection approach, the RF design and ESD design must be taken into account at the same time and therefore a compromise must be reached during the device development. As it will be deeper analyzed in the following chapters, the presence of the R_G connected to ground in a CMOS switch lets the gate internal node floating during ESD stress. Thus, a wide V_{GS} excursion might occur and this can lead to variation of the drain breakdown for instance. The knowledge of the effects of unwanted bias point conditions is also necessary; for instance the studies about the drain breakdown and parasitic bipolar triggering, GOX breakdown and failure, OFF-state leakage.

The working point of a NMOS transistor is mainly defined by gate-source voltage V_{GS} and drain-source voltage V_{DS} and, in a second step and depending on the technology involved, also by the bulk-source voltage V_{BS}.

A pictorial sketch of part of the possible combination of (V_{GS}, V_{DS}) is shown in figure 1.13. The safe operating area (SOA) for an enhanced nMOSFET is limited, and these limits are technology dependent.

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[8] For system level device protection against pulses of more than 200 ns [116] an external shunt inductance is placed at antenna pad to ground.

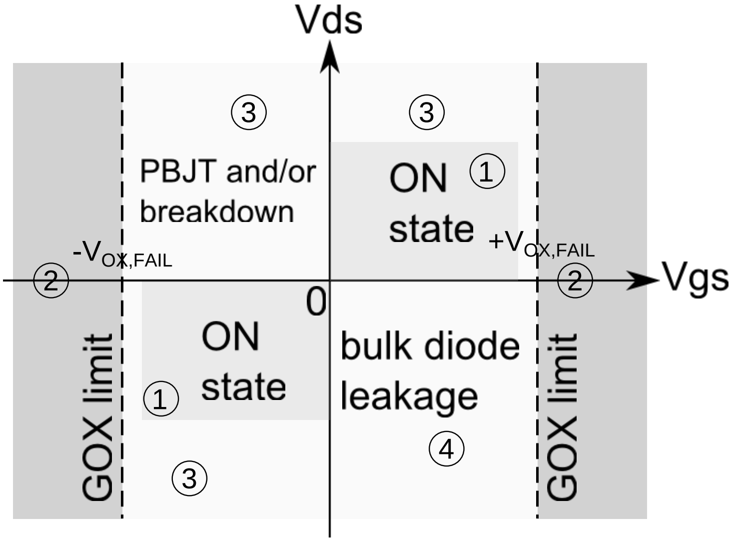
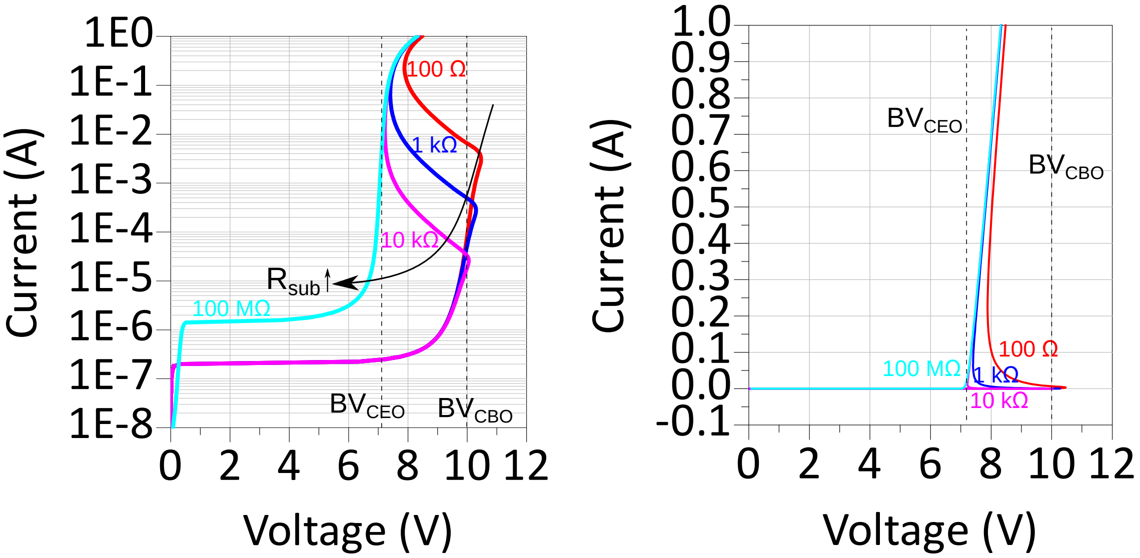


Figure 1.13: Safe operating area (SOA) of a nMOSFET where the GOX limits as well as the parasitic BJT and leakage conditions are indicated. The V_{BS} dependence and possible package limitation are not shown in this pictorial representation. In first approximation, the SOA has been divided into several regions: ① is the common on-state region where the nMOSFET is meant to work; GOX failure is encountered above $\pm V_{OX,FAIL}$ in ②; in ③ multiple phenomena can occur as drain breakdown and parasitic bipolar transistor (PBJT) triggering; in ④ the drain(-bulk) diode leakage occur. The most critical and relevant limits for ESD are regions ② and ③.

Gate limits The V_{GS} excursion is limited by the gate oxide (GOX) $V_{ox,break}$ and failure $V_{ox,fail}$ which are generally directly proportional to the t_{ox}. The regions involved in the SOA plot in figure 1.13 are marked by ②. As the technology advances, the V_{GS} working window shrinks accordingly. This means also that the maximum voltage sustained is also reduced, decreasing the ESD window. By [92], $V_{ox,break}$ for a 2.2 *nm* GOX, is expected to be $\approx 6\ V$. State-of-the-art RF silicon stacked transistors employ 2.2 *nm* or 5.2 *nm*.

Drain limits The V_{DS} limits are related firstly to the drain breakdown and then to the triggering of the parasitic bipolar junction transistor (PBJT) [1, 94]. The PBJT is formed by the source, bulk and drain of the nMOSFET which are respectively emitter, base and collector. The typical device configuration to study such phenomena is grounding gate, source and bulk together and applying (pulsed or DC) reverse bias at drain [51]. The breakdown occurs when the drain-bulk junction reversely biased starts to create electron-hole pairs due to the high electric field. As the stress voltage increases, the kinetic energy of the generated electron-hole pairs is high enough to create new electron-hole pair by impact ionization giving rise to the avalanche condition and avalanche current I_{av}. If generated electrons go towards the drain and recombine there, holes travel towards the bulk recombining at the bulk contact. To holes traveling through the bulk, it is associated a substrate current I_{sub} and assuming a non-negligible bulk resistance R_{sub}, the rise of the bulk potential V_B follows. Thanks to a positive feedback phenomenon as long as the drain potential increases, the forward biased V_{BS} increases and it turns on the PBJT snapping back the drain voltage because an high electric field at drain is no longer necessary to sustain the current. This latter phenomenon is called PBJT triggering and it is the main phenomenon occurring in the ESD anaylsis [51, 52]. The "S-shape" curve in figure 1.10 is an example of classic snapback IV characteristic encountered in the ESD studies.



(a) Y-scale logarithmic plot.

(b) Y-scale linear plot.

Figure 1.14: Simulated IV of a parasitic BJT in function of substrate resistance R_{sub}. The main parameters used for the simulation follows: common-emitter current gain $\beta_F = 0.8$, saturation current $I_S = 10\ nA$, collector saturation current $I_{SC} = 100\ nA$, emitter saturation current $I_{SE} = 1\ pA$

Three main parameters are associated to the PBJT triggering and the resulting TLP-IV shape:

- the substrate resistance R_{SUB},
- the multiplication factor M
- the gain β of the PBJT current (i.e. the drain current after the snapback event) .

Since we cannot have devices with all such combinations, SPICE simulations are very helpful to visualize changes of the TLP-IV [117]. It is of interest for this thesis work to present here SPICE simulation results that we did using a PBJT model varying the R_{sub}, see figure 1.14. We used a BJT model with reasonable typical literature values due to the lack of dedicated test structures. Results are therefore to be interpreted as a didactic instrument to show the concept and the idea. The PBJT breakdown model was taken from [95] and a value of collector-base breakdown voltage $BV_{CBO} = 10\ V$ was chosen. TLP-IV was simulated for four different $R_{sub} = [100, 1k, 10k, 100M]\ \Omega$, i.e from a condition of small substrate resistance towards an infinite substrate resistance. We note that increasing the value of R_{sub}, we span from a S-shaped (snapback) characteristic where the PBJT is activated to the so-called open-base breakdown characteristic seen in the light blue curve with the absence of any snapback called open-base breakdown characteristics characterized by the open-base collector-emitter breakdown voltage BV_{CEO}.

In chapter 3, particular attention on the analysis will be payed to define the GOX limits and drain breakdown in function of negative V_{GS}. The results will be presented by both DC and TLP dedicated measurements.

Chapter 2

ESD on shunt transistor from chip

This work begun with the study of the shunt device (a stacked transistor device) belonging to a single pole 8 troughs (SP8T) product chip (see figure 2.1a and 2.1b) for smartphone antenna front-end switch applications.

2.1 Chip and device description

This chip contained 8 pass transistors (PTs) connected to the common antenna pad (ANT) terminal (see them in figure 2.1b). Every PT was connected in series to its own shunt transistor (ST) to ground through the receiver pad (RX), note them in figures 2.1b and 2.1c. This configuration formed eight paths from ANT to RX pads. The shunt transistor shorts the RX signal to ground and they share three "GND" pads, since they were connected all together by a metal line. Every pass transistors and shunt transistors are driven by their own logic, see in figure 2.1c. The investigation was limited to the shunt transistor, since it showed the weakest ESD ruggedness compared here to the PT (data not compared for shortness). It is important to note that the p^+ implantation for the bulk contact was all around the chip (except one side) and it is marked in blue in figure 2.1a. The minimum distance between the p^+ implantation for bulk contact and the active region of the multi-finger devices is 140 μm.

During ESD test, the shunt transistor is probed applying positive pulses at $RX0x$ pad and the closer GND pad is connected to the GND signal of the TLP pulser for instance.

As one can see in the simplified schematic connection where pads and shunt transistors and pass transistors are indicated by figure 2.1b, possible interaction among neighboring devices and leakage paths cannot be excluded.

Moreover, the common gate terminal (refer to the pad indicated by "G" in figure 1.7 circuit) and the bulk were not accessible directly by pads and therefore they can be assumed at ground potential only at the beginning of the ESD pulse really[1]. As one

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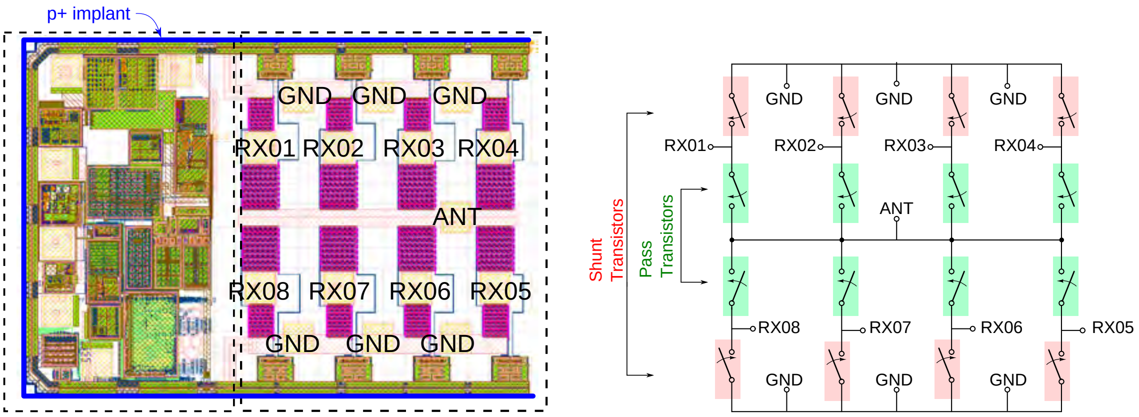
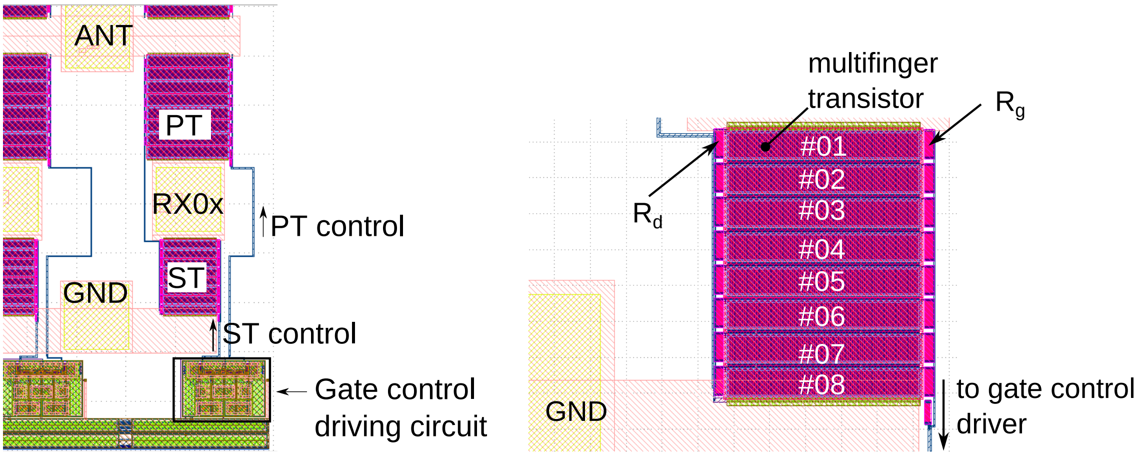
[1] Even though the gate terminal of the shunt transistors and the bulk are not directly accessible by pads, SPICE simulations showed that the common gate terminal of the gate pad might be assumed

can imagine, these lacks of gate and bulk accesses limit a lot the investigation of such chip. Despite this fact, we briefly present in the following the results stressing one shunt transistor of the chip as the beginning of the investigation of this doctoral work. See table 2.1, where the layout parameters of the studied devices are collected.



(a) Chip layout. The chip is divided in two main parts: the logic circuitry on the left side and the SP8T part on the right side. In this latter, the shunt devices, pass devices with their own gate driving controls are placed. The pad names are indicated and they correspond to what drawn in picture in subplot (b).

(b) Simplified circuit of the antenna switch chip SP8T showing pads locations.



(c) Layout of one arm of SP8T chip with pass transistor (PT) and shunt transistor (ST). The gate wires and the location of the gate driving control circuit are also indicated.

(d) Shunt transistors (ST) layout.

Figure 2.1: Antenna switch chip.

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grounded during the overall ESD pulse applied. Such simulations are not displayed in this work. The same is valid for bulk/p^+ implantation ring.

Table 2.1: Main layout and electrical parameters for the shunt device belonging to the SP8T product chip.

Parameter	abbreviation	values
number of blocks	N_B	8
total gate width	W_{TOT}	0.7 mm
multipliers	M	1
gate finger width	W_F	7.3 μm
gate finger length	L_G	0.13 μm
gate oxide thickness	t_{ox}	2.2 nm
gate resistor	R_G	400 $k\Omega$
drain resistor	R_D	400 $k\Omega$
block-to-block distance	D_{B2B}	2.1 μm

2.2 Measurements

TLP-IV In figure 2.2, we see a TLP measurement of the ST carried out for $PW = 100\ ns$ and $RT = 10\ ns$ on a fixed 50 Ω load line. The TLP-IV curve was calculated averaging the current and voltage waveforms in the time window $[70, 90]\ ns$. The ST showed a low $I_{t2} = 300\ mA$ not fulfilling the minimum customer requirement of $V_{HBM} = 1\ kV$. The DC leakage-IV was measured for $V_{leak} = 0.1\ V$. The TLP-IV is characterized by a breakdown voltage of 14 V and a steep increase. No pronounced snapback was visible.

TLP transient waveforms Looking at the TLP waveforms in figure 2.3a (current waveform is indicated by green color and voltage waveform by red color), we noted that current and voltage waveforms were not constant during the TLP pulse. This is not a common behavior in the TLP measurements seen in literature, so far. Therefore, this is interpreted as a sign of possible non-uniform behavior among the transistors composing the stacked device and it suggested to study the transient behavior by TIM to verify whether the transistors are working uniformly showing similar power dissipation distribution, possible free carrier signal or inhomogneous power distribution among the finger of the same block/transistor.

TIM results A TIM measurement was carried out applying the the same charging voltage as of the voltage and current waveforms indicated in figure 2.3a. The TIM path chosen in drawn on top of the layout file corresponding to the ST and reported in figure 2.3b. Three lines (one per transistor) composed the scanned path from the 1^{st} transistor on the R_G side, to the R_D side of the 3^{rd} transistors. Each line scan covered the middle of each multi-finger transistor, probing 19 different points with 3 μm distance one to the other. In order to increase the signal to noise ratio, 15 pulses per position were applied. Thanks to

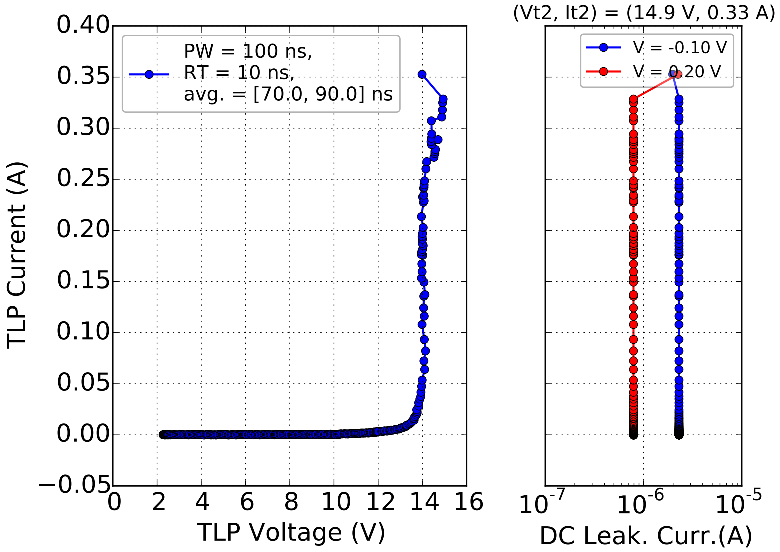
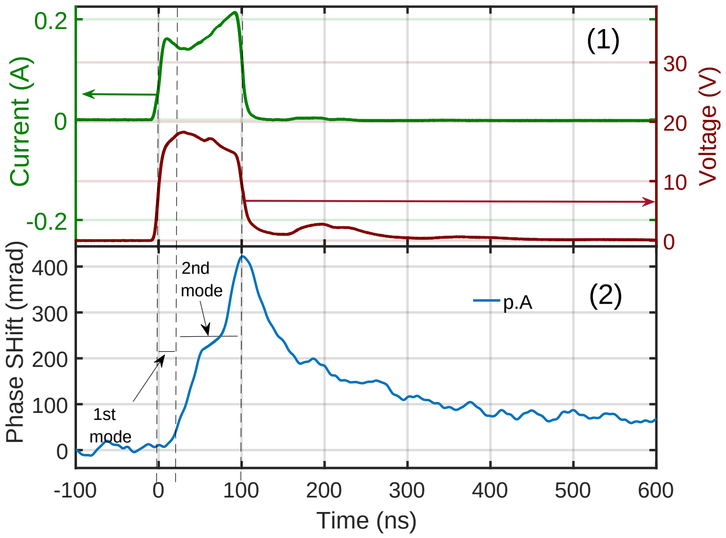


Figure 2.2: TLP-IV (left side plot) and leakage IV (right side plot) for a shunt transistor from a product chip. The TLP-IV parameters are indicate in the TLP-IV plot legend on the top-left corner. The leakage-IVs curves where obtained appling $-0.1\ V$ and $0.2\ V$, see the legend.

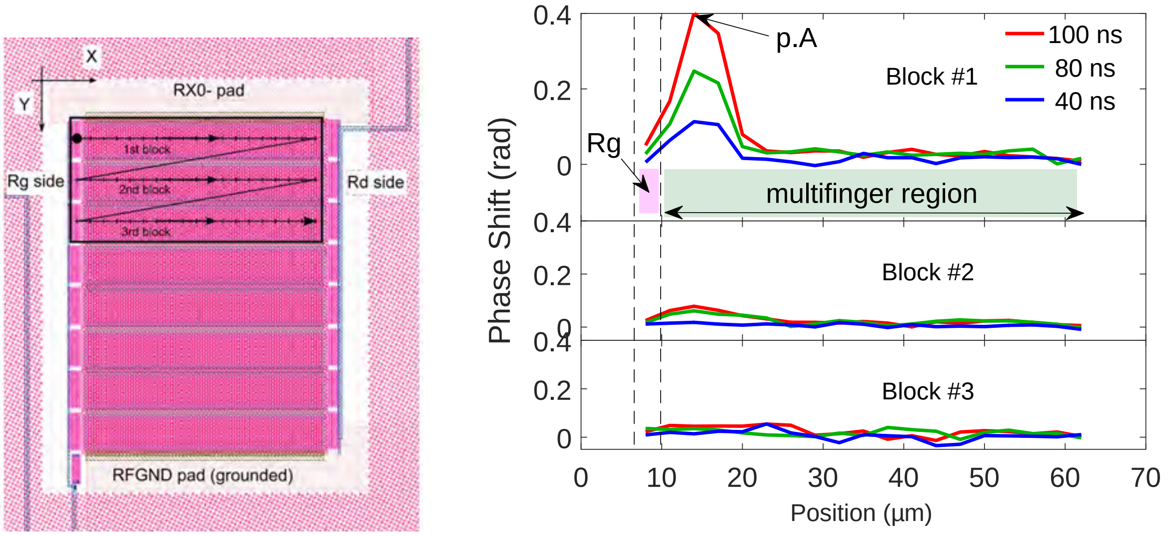
that in the post process phase, we could average all 15 pulses and the averaged phase shift results are displayed in figure 2.3c for three different time instants at $t = [40, 80, 100]\ ns$ and indicated with blue, green and red lines, respectively. Every subplot in figure 2.3c cover a scan of a multi-finger transistor: on the top plot lays the 1^{st} transistor, on the central the 2^{nd} transistor and finally on the bottom plot the 3^{rd} transistor.

The voltage and current waveforms indicated in figure 2.3a show clearly amplitude variations with time. For $t < 30\ ns$, the current decreased and voltage increased; whereas for $t > 30\ ns$ we had the opposite transient behavior. For this behavior, it seemed that the stacked devices worked in two different operation modes.

From the cross-section of the probed transistors in figure 2.3c, we clearly note that a hot spot was appearing from $t = 40\ ns$ in the R_G side of the 1^{st} transistor (top plot). At the next time instant i.e. for $t = 80\ ns$, we saw that also on the 2^{nd} block a localized hot spot in the R_G side arose. The other sides of the device and probed parts presented phase shift at noise level. At the pulse instant i.e. for $t = 100\ ns$, we saw the maximum phase shift peak in the 1^{st} transistor. The phase shift associated to point p.A is time aligned with the transient voltage and current waveforms in figure 2.3a(2). We noted that until 30 ns no phase shift was detected , whereas for $t > 30\ ns$ the phase shift rose. It is interesting to note that the minimum current point in the TLP current transient waveform in figure 2.3a(1) in green curve was associated to the end of the 1^{st} mode in correspondence of the phase shift rise in the subfigure 2.3a(2). Possible minor phase shift variation features in subfigure 2.3a(2) should be interpreted as noise features rather than due to physical power dissipation.



(a) (1) TLP current (green plot), TLP voltage (red plot) and (2) phase shift transient (blue plot) waveforms. The phase shift transient waveforms corresponds to the point "p.A" indicated in subplot (c) for phase shift peak point in block #1.



(b) TIM path indicated on top of shunt transistor layout. The scan consists of three lines, one per block each of them from the R_G side to the R_D side. 19 different points are probed per transistor. For each point, 15 pulses were applied resulting on a total of 285 TLP pulses applied.

(c) Phase shift cross section at three different time instants. The top plot refers to the scan on transistor 01, the center plot to the scan on transistor 02 and the bottom plot to transistor 03. The location of R_g and the multifinger is indicated for shortness only on the top plot since it is the same for the other two scan lines.

Figure 2.3: TIM measurement on shunt transistor at $It2/2$ stress level. The TIM scan is limited to the first three transistor (01, 02, 03) since other blocks show no phase shift.

2.3 Considerations

Besides the presented measurement and results for $PW = 100\ ns$, further measurements were carried out for instance varying TLP PW and RT showing PW dependence for $PW \geq 75\ ns$ but no RT dependence of waveforms nor I_{t2}. We analyzed also the DC-IV before and after the I_{t2} in order to understand the reasons of the failure and comparing all measurements results with SPICE simulations[2].

Despite the huge effort spent in terms of time and amount of measurements, some features limited our investigation and we were forced to stop the analysis of such product device. The first limiting factor was the lack to access the gate. This fact considerably limits the analysis, in particular for the failure root cause analysis since not all junctions can be probed and no gate contact variation studies can be carried out (e.g. study the device with grounded gate versus floating gate). Moreover, the shunt was part of a chip where possible interactions with neighbor devices can take place.

Furthermore, due to the very low I_{t2} and the observed cumulative damage[3], also getting consistent TIM results was really challenging because we could not probe the device for high stress level (i.e. for $I_{DUT} > 0.5 \cdot I_{t2}$) and for multiple stress conditions. Besides, for the maximum TIM stress available the phase shift measured is so low that can be considered at the setup noise level.

For all these reasons, we dropped the investigation and we do not present other results of such product device in this work. Nevertheless, we found similar stacked test structures where a deeper study was finally possible (see them in chapters 4 and 5). These test structures were isolated (i.e. not part of a product chip) with full access to common gate, source, drain and bulk terminals as in figure 1.7. Also in these devices the bulk p^+ implantation was placed far away from the active region of the device. These devices will be presented and analyzed in the following chapters. In appendix C the summary tables of stacked device parameters and main power dissipation distribution findings are reported, respectively in table C.1 and table C.2.

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[2] The model will be presented in chapter 3 and it is valid also for the shunt device of SP8T product

[3] The cumulative damage can be critical for the scanning TIM since, as described before, this technique is based on the repetition of the same TLP pulse for every scanned position of the stressed DUT. With a device showing cumulative damage, one is forced either to change the device after a certain amount of pulses or to reduce the TLP pulse level in order to have homogeneous data collected on the same device.

Chapter 3

Analysis of single transistor and modelling

In this chapter, we explore the technology characteristics and limits on single- and multi-finger transistor test structures for multiple working bias conditions and device configurations, fundamental for an ESD self-protection approach.

The main focus was given to the multi-finger structures because they are the building-blocks of every stacked transistor. However, important information on the breakdown phenomena can be derived from analysis of single finger transistors as well.

TIM measurements were employed to map the thermal power distribution applying TLP pulses in selected stress configurations.

The collected information from the electrical measurements have been used also to improve an existing SPICE MOSFET model of these devices and to develop the drain breakdown model. This model will be applied on TLP transient simulations of stacked transistors and the results will be shown in chapter 4.

Finally a discussion of failure on multi-finger transistor is provided.

Main results of this chapter were published in [22] and [21].

3.1 Device descriptions

Single-finger and multi-finger transistor test structures were available with different total gate width W_{TOT} and gate length L_G. All studied devices had separated drain (D), gate (G), source (S) and bulk (B) pads. We can classify the single transistor test structures in two groups:

1. single finger transistors (i.e. with number of finger $N_F = 1$) characterized by dif-

ferent gate length $L_G = [0.1, 0.11, 0.12, 0.13, 0.14, 0.16, 0.18, 0.25, 0.5, 10]\ \mu m$ (see layout details in table 3.1) and

2. multi-finger transistor test structures with $N_F = [2, 4, 150]$ with the same $L_G = 0.13\ \mu m$, see layout details in table 3.2.

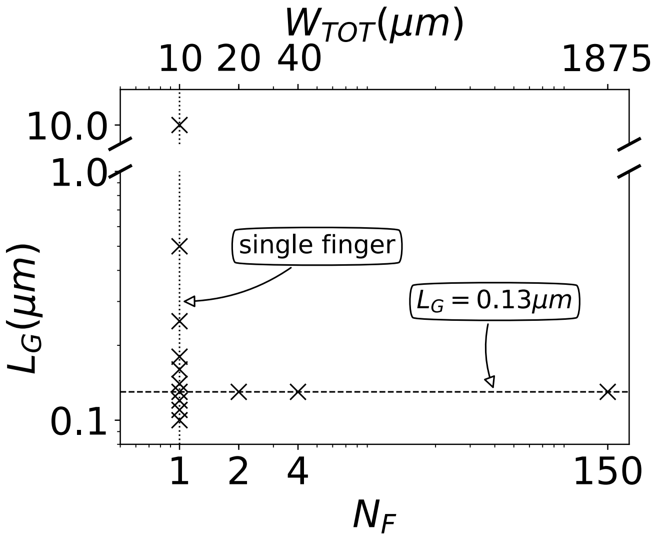


Figure 3.1: Studied single transistor test structures gathered by total gate width W_{TOT}, number of gate finger N_f and gate length L_G. The bottom logarithmic x-axis indicates N_F and its respective W_{TOT} value is reported on the top logarithmic x-axis. On the y-axis, the L_G is indicated in logarithmic scale; note the discontinuity on the y-axis.

A pictorial view of the available two sets of devices is plotted in figure 3.1, where on the bottom logarithmic x-axis N_F is indicated and on the top logarithmic x-axis the respective W_{TOT} values. On the y-axis, the L_G is indicated in logarithmic scale; see the discontinuity on the y-axis.

Table 3.1: Main layout and electrical parameters for single-finger transistor test structures for different gate length L_G.

Parameter	Abbreviation	
number of fingers	N_F	1
gate length	L_G	$[0.1, 0.11, 0.12, 0.13, 0.14, 0.16, 0.18, 0.25, 0.5, 10]\ \mu m$
gate oxide thickness	t_{ox}	2.2 nm
gate width	W_F	10 μm
drain-source pitch		0.56 μm

In figure 3.2a, an IR backside image of a 150 multi-finger transistor is reported. The single fingers cannot be distinguished. The laser beam reflection from the multi-finger active region is visible as white spot.

Table 3.2: Main layout and electrical parameters for multi-finger transistor test structures for the same gate length $L_G = 0.13\ \mu m$. Four devices have been used, every device parameters are listed per column. Note that W_{TOT} is calculated by $W_{TOT} = N_F \cdot W_F$, where W_F is the single finger gate width.

Parameter	Abbreviation				
number of fingers	N_F	1	2	4	150
gate length	L_G	$0.13\ \mu m$	$0.13\ \mu m$	$0.13\ \mu m$	$0.13\ \mu m$
gate width	W_F	$10\ \mu m$	$10\ \mu m$	$10\ \mu m$	$12.5\ \mu m$
total gate width	W_{TOT}	$10\ \mu m$	$20\ \mu m$	$40\ \mu m$	$1875\ \mu m$
gate oxide thickness	t_{ox}	$2.2\ nm$	$2.2\ nm$	$2.2\ nm$	$2.2\ nm$
multipliers	M	1	1	1	1
drain-source pitch		$0.56\ \mu m$	$0.56\ \mu m$	$0.56\ \mu m$	$0.56\ \mu m$
gate resistor	R_G	-	-	-	$400\ k\Omega$

In figure 3.2b, a sketch of the layout of the multi-finger transistor is reported where metal connections are indicated for drain, gate and source. In this chip, the bulk p^+ ring surrounding the chip is placed far from the device active by a minimum distance of $290\mu\ m$.

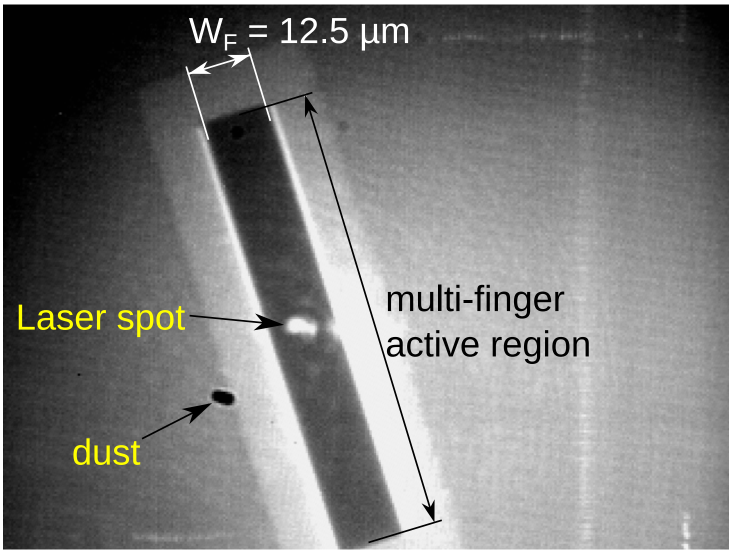
In the following, most of the results will be presented for the device with $L_G = 0.13\ \mu m$ and $N_F = 150$ fingers. We will indicate this particular device as "150 multi-finger transistor".

3.2 DC characterization of multi-finger transistor

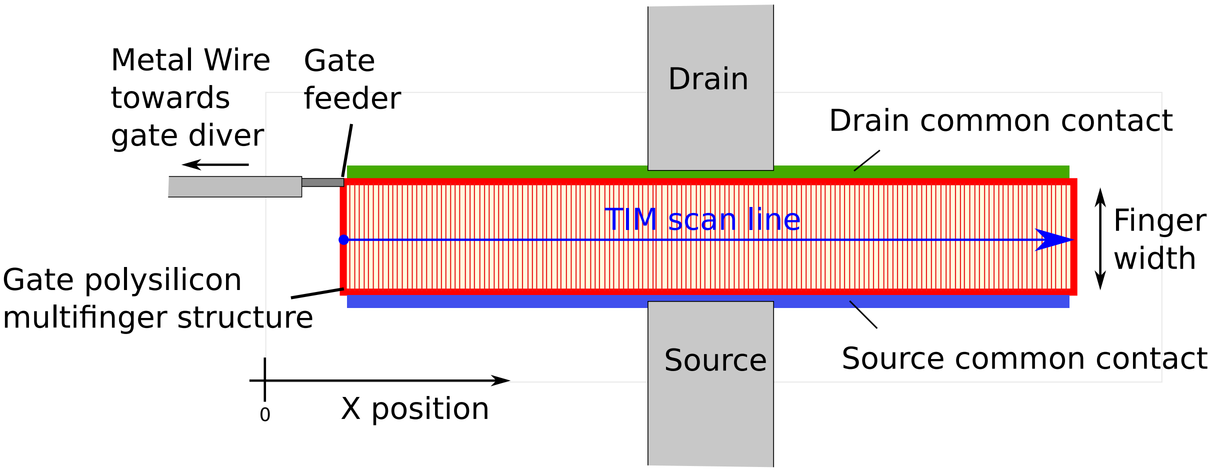
The first characterization of the single 150 multi-finger MOSFET consisted on output characteristic and transfer characteristic. From these two measurements, r_{on} and threshold voltage V_{TH} are extracted. An additional experiment was carried out in order to probe whether a possible V_{TH} shift due to body effect was present.

The DC output characteristic is shown in figure 3.3. The characteristics were limited to $V_{DS} = 1.5\ V$ to avoid drain breakdown (see in the following in this chapter) and device degradation. The output characteristic was recorded for $V_{GS} = [0.2, ..., 1]\ V$. The r_{on} was found to be 2.6Ω for $V_{GS} = 1\ V$ corresponding to a specific $r_{on} = 4.88\ \Omega mm$. The channel modulation effect is also present, see the curve saturation regions.

The measured transfer characteristics for $V_{BS} = 0\ V$ are shown in logarithmic (figure 3.4a) and linear (3.4b) scales. We noted the drain induced barrier lowering effect (DIBL) [24] in the region near the $V_{GS} = 0\ V$. The DIBL is a short-channel effect where a high injection of electron from source are injected into the channel because of the low potential barrier at the source-channel junction [24]. The effect of this phenomenon in the transfer characteristics is a drain current increase in the sub-threshold region (for



(a) Infrared image from the back side of the multi-finger transistor with number of finger $N_F = 150$. We see that in the active region we cannot distinguish the gate, drain and source fingers. We remind that the drain-source pitch distance is 0.56 μm.



(b) Sketch of the layout of the studied devices from the top view. The orientation and the path of the TIM scans relative to figure 3.14 and 3.14 are indicated. The locations of the failure analysis pictures are marked as “F.A. (a)” and “F.A. (b)” relative to figure 3.30a and 3.30b, respectively. Taken from [104].

Figure 3.2: 150 multi-finger transistor test structure.

$V_{GS} = [-0.1, 0.2]\ V$ in figure 3.4a) as the V_{DS} increases.

In this section we do not show drain leakage current for $V_{GS} < -0.5\,V$, since they will be presented in the OFF-state and drain breakdown characterization in the following in section 3.5.

The presence of body effect was investigated since this might be critical for a stacked configuration [105]. The measurement is reported in figure 3.5. For this measurement, the gate voltage was swept for multiple negative V_{BS} bias voltages for $V_{DS} = 1.5\ V$. From

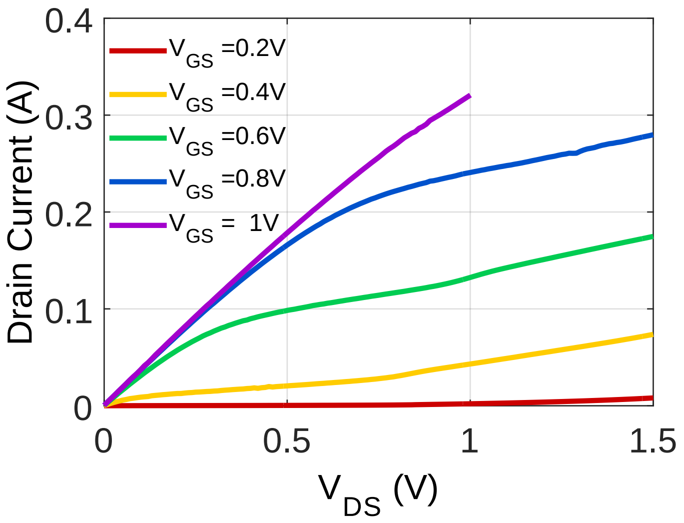


Figure 3.3: Measured DC output characteristic of a multi-finger MOSFET. The $V_{BS} = 0\ V$. The curve for $V_{GS} = 1\ V$ is displayed until $V_{DS} = 1\ V$.

the results, we see that there is no appreciable V_{TH} variation in the region for $V_{GS} \geq 0\,V$. This effect has been investigated also for fixed $V_{DS} = 2\,V$ but not even for this bias there is no V_{TH} variation. For this reason, we exclude the body effect on these devices.

3.2.1 Drain breakdown phenomena in high resistivity substrate

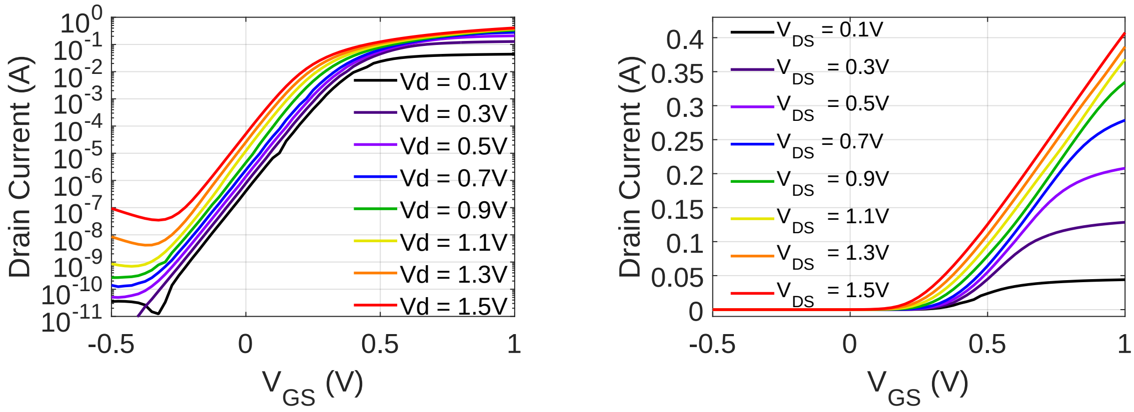
The investigation of the drain breakdown voltage $V_{BD,DS}$ in a self-protected approach is fundamental. This topic is widely studied in literature varying layout parameters or technology parameters to find the optimum performance for the requirements [51, 52].

The first junction probed is the drain-bulk by DC measurement, see the result in figure 3.6 for a 150 multi-finger transistor where drain, gate and source pad where left floating. We noted that the breakdown, a sudden current increase, appeared at 180 V. This value was quite high but we also need to remind the high distance between multi-finger active region and p^+ ring.

The $V_{BD,DS}$ is not changed if also the gate terminal is grounded, thus the measurement is not reported.

In literature, the $V_{BD,DS}$ study is mostly presented in grounded-gate configuration, i.e. when source, bulk and drain are tied all together to ground and the drain of a nMOSFET is biased by positive voltages. A DC sweep was carried out in current control mode for such configuration, see the results in figure 3.7. We noted a weak snapback visible at $V_{DS} = 2.2\ V$ and a drain-source breakdown voltage $V_{BD,DS} = 2.3\ V$ for $I_D = 0.4\ mA$. Secondary, the kink effect [118] was visible at $V_{DS} = 1.1\ V$ by a I_B sudden increase.

Due to the small difference between snapback and $V_{BD,DS}$ voltages, in the following, we will focus on the $V_{BD,DS}$ and its variation to the gate bias.



(a) Measured transfer characteristic for $V_{BS} = 0\ V$ plotted in logaritmic scale.

(b) Measured transfer characteristic for $V_{BS} = 0\ V$ plotted in linear scale.

Figure 3.4: Measured transfer characteristic on a multifinger transistor for $V_{BS} = 0\ V$.

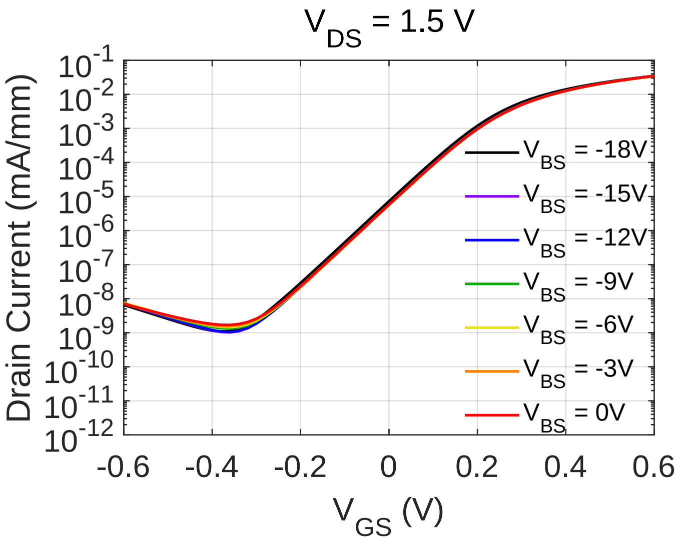


Figure 3.5: $V_{DS} = 1.5\ V$.

3.3 TLP study varying the number of fingers

TLP pulsed IV characteristics on test structures with different finger quantity (N_F) are reported here. Transistors with 1, 2, 4 and 150 fingers were probed in positive Drain versus grounded gate, grounded source and floating bulk configuration using $PW = 100\ ns$ and $RT = 1\ ns$, see the results in figure 3.8. In order to compare devices with different N_F (and therefore different W_{TOT}), the TLP current displayed in the y-axis is shown normalized by W_{TOT}.

From figure 3.8, one can observe that the breakdown voltage V_{BD} tends to decrease and it seems to saturate as the N_F increases. For $N_F = 1$ (blue curve), $V_{BD} = 3.3\ V$, then

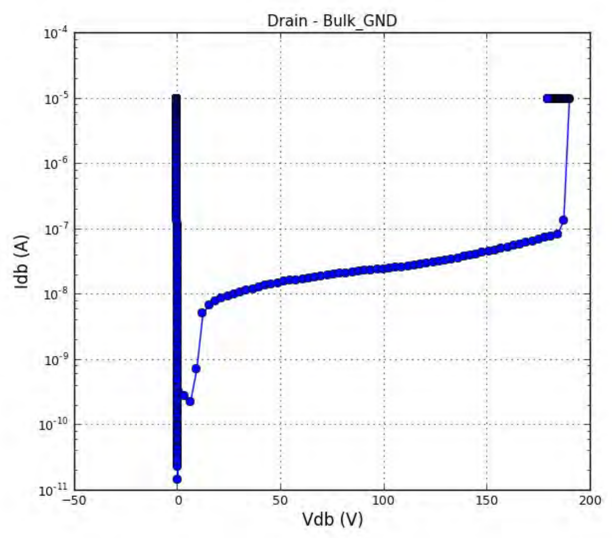


Figure 3.6: Drain-bulk IV characteristic by DC measurements. The gate and source pads are left floating. The instrument compliance was set to 10 μA.

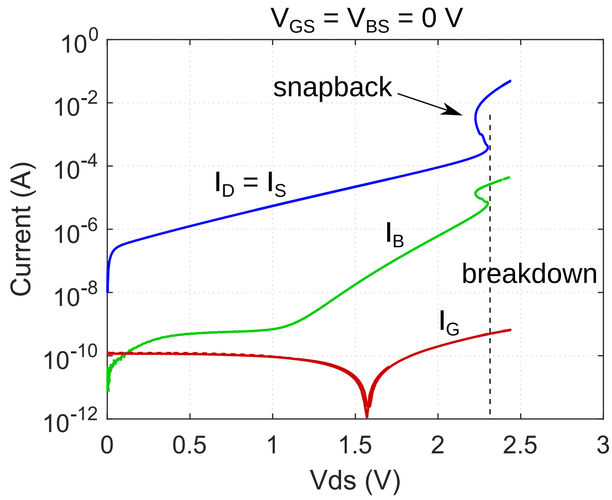


Figure 3.7: DC sweep in current control mode of a 150 multi-finger transistor with $V_{GS} = V_{BS} = 0\ V$. The source current (I_S) coincides basically with the drain current I_D and therefore it is not visible.

it decreases to $\approx 2.7\ V$ for $N_F = [2, 4]$ (green and orange curves, respectively) and finally for $N_F = 150$ it is $2.3\ V$ (red curve). We explain this saturation phenomenon by the finger-to-finger coupling. We attribute this effect to the coupling of the neighbor fingers through the substrate at high injection levels of free carriers under breakdown conditions, as depicted in figure 3.9. The presence of additional fingers significantly affects current distribution and electrical field in the n^{++} - p^{+} wells and then enhances the injection from other fingers. Therefore, avalanche generation starts to be observed at lower potential in multi-finger device in comparison with single finger one. This engineering choice aims to

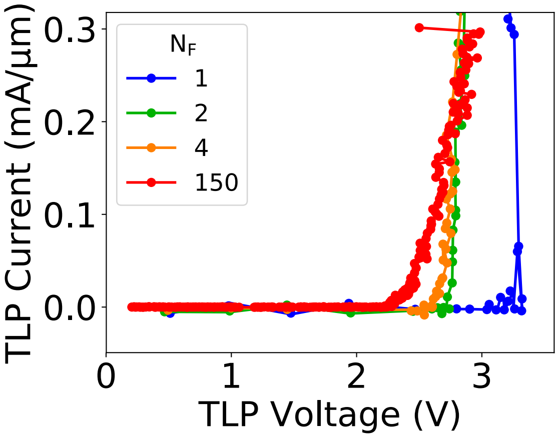


Figure 3.8: Normalized TLP-IVs for N_F variation devices (see it indicated in the legend). The TLP current was normalized by the W_{TOT} of each device. TLP measurements were carried out in configuration positive Drain versus grounded Gate, grounded Source and floating Bulk adopting PW = 100 ns and RT = 1 ns. The time average window is $[70, 90]$ ns.

reduce the finger-to-finger inhomogeneities.

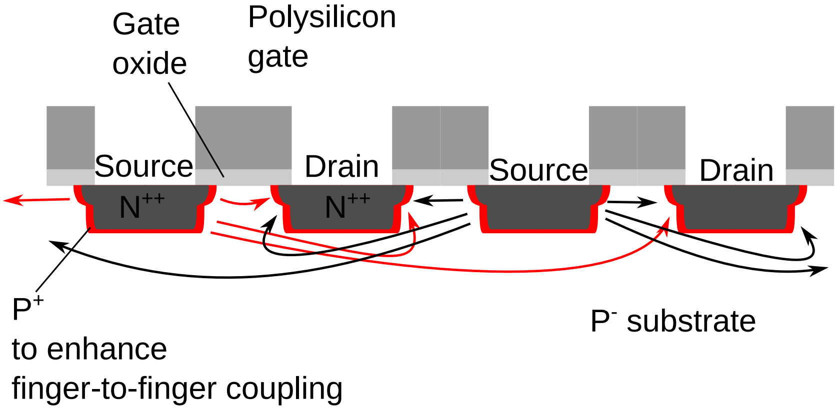


Figure 3.9: Pictorial view of the finger-to-finger coupling on a MOSFET multifinger cross-section. The black or red arrows indicates different injection paths occurring from the breakdown condition. As it can be seen, multiple fingers are involved through the substrate coupling.

The finger-to-finger coupling effect via substrate can also be seen by a TLP-IV comparison for $N_F = 2$ in figure 3.10. In a two gate finger MOSFET, two configuration can be probed one given by Drain-Gate-Source-Gate-Drain (DSD) and another one with Source-Gate-Drain-Gate-Source (SDS), see the two drawings in the inset of figure 3.10. The two configurations show different IV shapes. In particular, only SDS shows a snap-back characteristic with $V_{BD} = 3.45$ V and $V_H = 3.2$ V. The DSD configuration shows a lower $V_{BD} = 2.7$ V since in this configuration electrons injected from the center are all collected at drain. In the other configuration, part of the electron generated from source at the edges does not reach the central drain finger. Therefore to reach the breakdown, higher voltage is required when the sources are at the edges of the structure. Such effect however vanishes for high N_F transistors as for the device with $N_F = 150$.

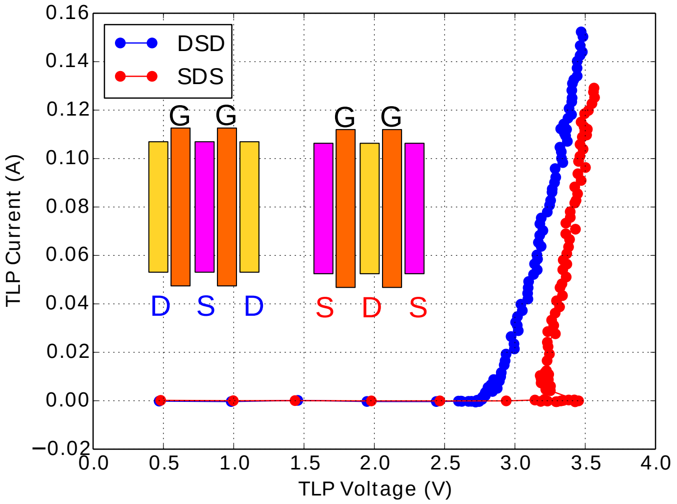


Figure 3.10: TLP-IVs for devices with $N_F = 2$. TLP measurements in configuration positive Drain versus grounded Gate, grounded Source and floating Bulk adopting PW = 100 ns and RT = 1 ns. The time average window is $[70, 90]$ ns. The simplified layout of the two configurations "DSD" and "SDS" is drawn in the inset.

3.4 L_G variation by TLP in single finger transistor

The impact of the gate length (L_G) scaling was already investigated in the past as in [2, 3, 5] to find the optimum parameter for ESD protection devices to choose according to the ESD window. Nevertheless, the L_G variation study on single finger devices here is interpreted in a different manner, considering drain and source two junctions placed at L_G distance.

The devices were stressed for $PW = 100ns$, $RT = 1$ ns in the configuration positive pulses on drain versus grounded gate, grounded source and floating bulk[1].

The results of the breakdown voltage (V_{BD}) and holding voltage (V_H) versus L_G are reported in figure 3.11 for different single finger MOSFETs with $L_G = [0.1, 0.11, ..., 10]$ μm. The definition of V_{BD} and V_H is indicated in the insight where a selection of TLP-IVs is reported.

The V_H and V_{BD} coincided for short channel devices and a snapback clearly appeared only for $L_G \geq 0.12$ μm. For $L_G \geq 0.12$ μm, the difference between V_{BD} and V_H was less than 500 mV. We attributed this behavior to the presence of an intrinsic higher substrate

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[1] Similar configuration but in bulk grounded condition leaded to same results as the ones in figure 3.11. Therefore, it was not reported.

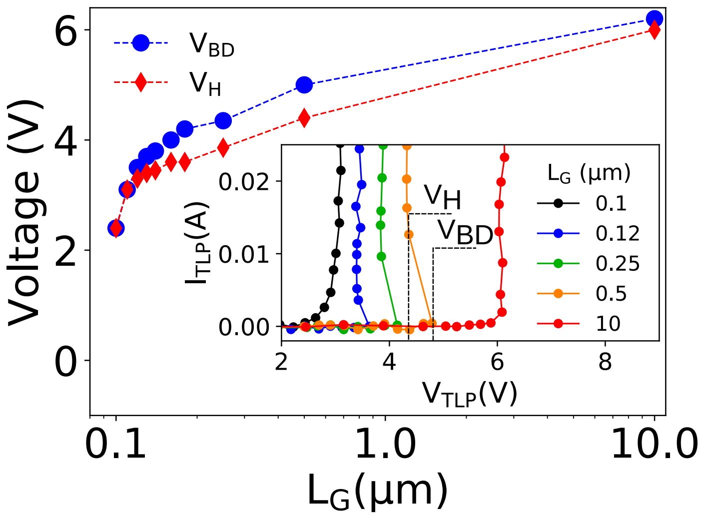


Figure 3.11: Breakdown voltage (V_{BD}) in dotted blue points and V_{t1} in red diamond points versus gate length L_G. The data points were extracted from TLP measurements in configuration positive Drain versus grounded Gate, grounded Source and grounded Bulk adopting PW = 100 ns and RT = 1 ns. Zoom of the selected TLP-IVs are reported in the inset figure. In the inset, an example for V_{BD} and V_H is indicated. The time average window of the TLP-IVs is $[70, 90]$ ns. Taken from [22].

resistance on devices with higher L_G that decreases the current gain of the parasitic BJT [22] as shown from SPICE simulations in figure 1.14.

Furthermore, TLP results on devices with different L_G and N_F showed that the electrical potential configuration of the bulk pad does not influence these devices, since it does not change the device behavior due to it large distance (higher than 290 μm).

3.5 Impact of gate bias on drain breakdown

In order to explore the drain breakdown in the TLP regime, a set of measurements was carried out pulsing the drain versus grounded source and grounded bulk biasing the gate with DC $V_{GS} \leq 0$. However, in a self-protected approach all possible working conditions should be explored to determine the device weaknesses.

After presenting this study by TLP measurements, we propose a DC characterization carried out by a semiconductor parameter analyzer in order to have more information on the current nature for $I_D \leq 1$ mA.

3.5.1 Pulsed characterization

The pulsed characterization was done using the TLP pulser with $(PW, RT) = (100, 10)$ ns pulsing the drain versus grounded bulk and grounded source.

The simplified setup sketch to study the drain breakdown by TLP with DC gate bias is shown in figure 3.12b, whereas the picture of the setup is in figure 3.12a. Previous work like [29] used a bias-tee to decouple the DC path to the biased gate. In our setup, the gate bias was applied through a special Picoprobe Model 10 needle, see figures in 3.12. Generally two configurations of signal-ground needle are used in the Kelvin TLP setup [34, 75]: the first in a 50Ω needle to force the TLP pulse to the DUT and another one provided with $5\ k\Omega$ to sense the voltage [98]. In the TLP setup used for this study, we added a customized needle containing a $5\ k\Omega$ incorporated resistor with a $10\ nF$ capacitor connected to the shield and this ladder. The resistor and the capacitor were placed to protect the source measurement unit (SMU) from the possible incoming pulse reflections and to keep constant the V_{GS} bias, respectively.

Selected results of the measurements are shown in figure 3.13(a) in dotted curves for $V_{GS} = [0, \ldots -4]\ V$ [22] and the drain-source breakdown voltage $V_{BD,DS}$ at 1 mA is shown in figure 3.13(b) by red dotted points in function of V_{GS} for all measurements. We will concentrate on the breakdown variation for $I_D \leq 0.15\ A$, to avoid device degradation.

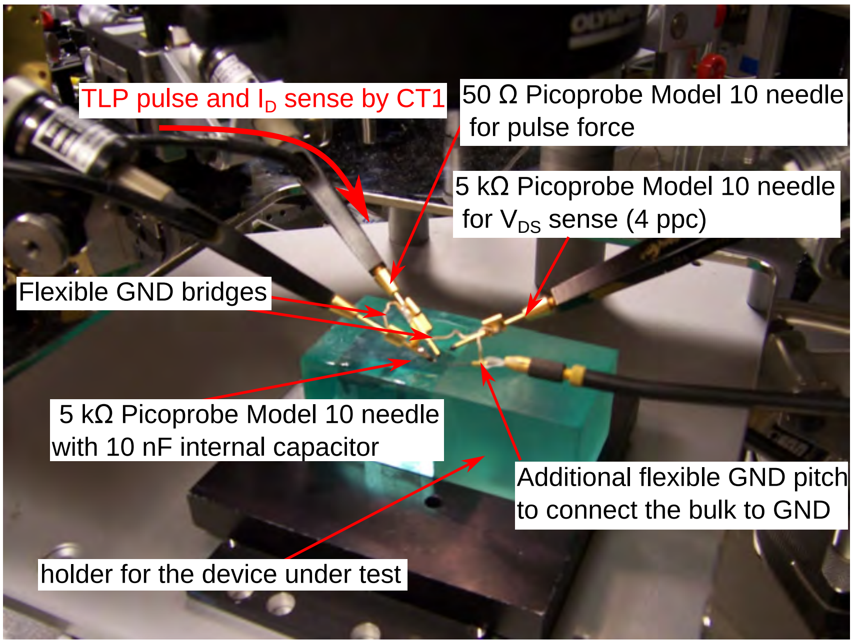
The $V_{BD,DS}$ results are very surprising, since they clearly showed a strong dependence on V_{GS} and moreover for $V_{GS} \leq -1\ V$, the $V_{BD,DS}$ was almost linearly dependent on the V_{GS}, see figure 3.13(b). The reduction of the $V_{BD,DS}$ with V_{GS} is critical if the device is subjected to a negative voltage decrease in ESD operation. We also note that the measurement at $V_{GS} = -0.5\ V$ shows a weak snapback, the other are characterized by a monotonic behavior after the breakdown, similar to an open base breakdown characteristic.

3.5.2 DC characterization

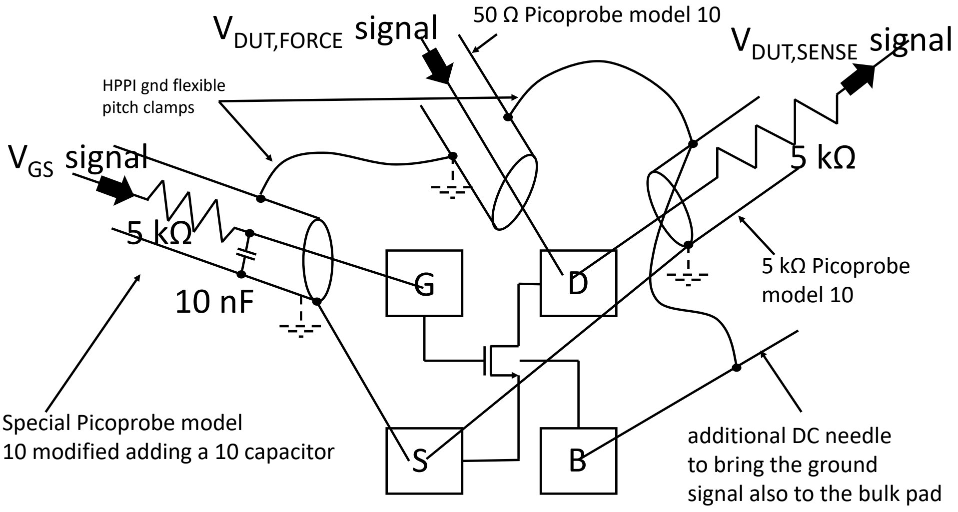
Previous studies by TLP had not enough insight on the origin of such $V_{BD,DS}$ dependence on V_{GS}, for this reason a similar study by DC measurements by a semiconductor parameter analyzer was carried out.

The drain DC current control mode (ccm) measurement for multiple V_{GS} is shown in figure 3.14a for a 150 multi-finger transistor. The choice of a ccm measurement was due to the fact that it was able to measure and resolve possible snapback behavior associated to PBJT triggering and measure low current level than a CT-1 [27]. During the experiment, the bulk was set to ground potential. The drain I_D, gate I_G and bulk I_B currents were directly measured by the parameter analyzer. The source current I_S instead was obtained by applying Kirchoff current law because the parameter analyzer was provided with only three terminal SMUs.

From figure 3.14a, we noted that the drain current and breakdown voltage were strongly dependent on the V_{GS}. The breakdown voltage decreased if V_{GS} decreased to negative values, whereas the drain current increased. We observed that for $V_{GS} \leq -0.5\ V$, the sudden drain current increase at the breakdown condition was stable at $10\ \mu A$. Then,



(a) Picture of the setup used to measure the drain breakdown by TLP with gate bias in 4 point probe configuration (4ppc).



(b) Drawing of the setup used in (a).

Figure 3.12: Setup used to produce measurements in figure 3.13. The complexity of the connections and needles is due to the non-optimal pad positioning, this is the reason why we need to use HPPI ground flexible pitch clamps to share the same ground potential among force, sense and V_{GS} supply needles.

looking at the drain current curves for $V_{GS} \leq -0.5\ V$, we noted also that the overall behavior is very similar. Only curves for $V_{GS} = [0, -0.5]\ V$ showed a small snapback at $1\ mA$. Finally, except the case $V_{GS} \leq -0.5\ V$, the drain current showed three different mechanisms marked by a number from 1 to 3 and separated by a dashed line.

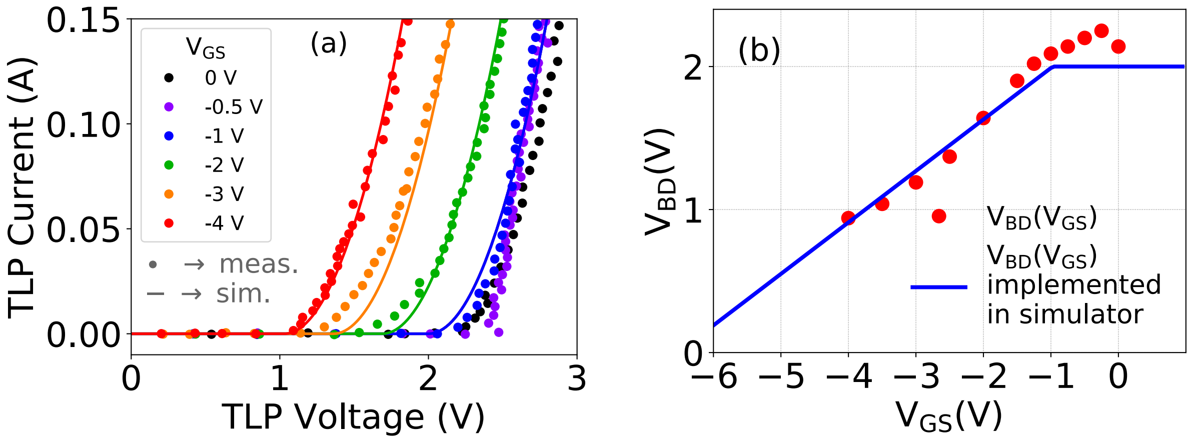
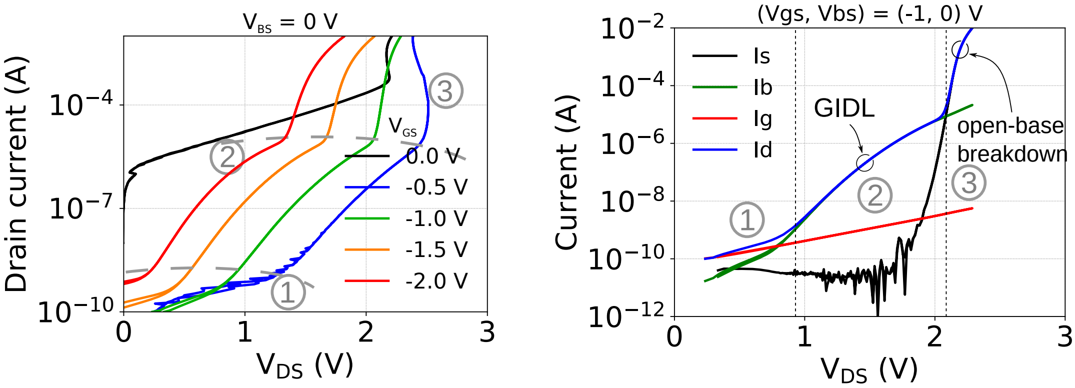


Figure 3.13: (a) Measured (dotted lines) and simulated (solid lines) TLP-IVs for 100 ns pulse width on a single multi-finger transistor (W = 1.95 mm) for different V_{GS} bias. (b) Drain source breakdown voltage (V_{BD}) (red points) extracted from TLP-IVs in (a) at 1 mA. The blue line shows empirical ($V_{BD}(V_{GS})$) function for which the TLP-IV results in (a) fits the best. Taken from [22].



(a) DC drain current control mode sweep measurements for multiple V_{GS}. The V_{BS} is fixed at $0\,V$.

(b) DC drain current control mode sweep measurement for $(V_{GS}, V_{BS}) = (-1, 0)\,V$. The source current I_S has been obtained applying the Kirchoff current law due to the fact that the paramater analyzed was provided with only three SMUs. Taken from [22].

Figure 3.14: DC drain current control mode sweep measurements. The bias conditions are reported in the caption of each subfigure.

A selected measurement for $V_{GS} = -1\ V$ from figure 3.14a is displayed in figure 3.14b, where three main regions appeared. In the first region marked with ①, we note that the drain current coincided with the gate current I_G, this seemed to be related to a gate tunneling current. However in central region ②, the I_D is dominated by the I_B. We explained this, with the gate induced drain leakage (GIDL) current mechanism, typically observed in transistors with thin gate oxides as in [94, 97]. This leakage mechanism is due to the band-to-band tunneling taking place in the overlap region of the gate oxide with the drain n-well for negative gate bias. This mechanism is very critical, since it is a main source of off-state leakage and then, it might trigger the breakdown as observable in region ③, where the device entered into the open-base avalanche breakdown mode.

3.6 Circuit used to simulate one transistor from a stacked device

We present at this point after the breakdown model, the equivalent circuit used to simulate the multi-finger transistor of the stacked devices. The stacked devices are analyzed by measurement and transient simulations in the next chapters.

The base model of the multi-finger MOSFET was developed internally by Infineon Technologies AG. This initial MOSFET model incorporates the gate capacitances, mobility, threshold voltage. Moreover, additional drain-bulk and source-bulk diodes are provided. A BSIM was chosen to model the MOSFET [8]. BSIM is the state-of-the-art model and it widely used both in academic and company environments [106].

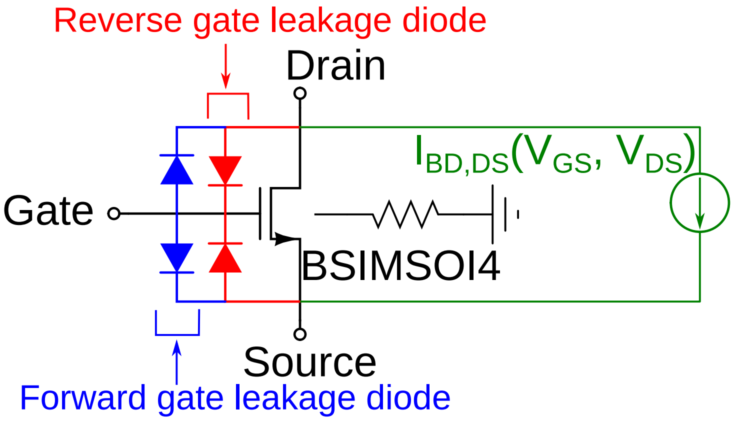


Figure 3.15: Simplified circuit to simulate a multi-finger MOSFET. The core is given by the BSIMSOI4 model MOSFET. Besides the gate leakage diodes for forward (blue) and reverse (red) leakage diodes are indicated.

Such model was meant to fully cover the RF operation conditions, i.e. $V_{DS} \leq 1.5\ V$ and $-1.5\ V \leq V_{GS} \leq 1.5\ V$, thus a confined working bias set. These intervals are not sufficient to cover the wide V_{GS} and V_{DS} excursion occurring during a TLP pulse as we will see in the following chapters. Therefore, the model was extended and refined to fulfill the wide voltage range used during ESD. We extended the gate leakage diodes in order to cover the interval $-3.5\ V \leq V_{GS} \leq 1.5\ V$ thanks to gate voltage sweep in on- and off-state measurements. Hence, forward and reverse diodes were added between gate-source and gate-drain as displayed in figure 3.15. As already presented, we included our breakdown model covering the breakdown for $V_{DS} \leq 2.5\ V$ for the new wide V_{GS}.

Finally, the gate and drain resistors were simulated by ideal resistors.

3.6.1 Drain breakdown model

The development of an accurate drain breakdown component was necessary for ESD SPICE transient simulations. From the previous section, in order to simulate the V_{GS} dependence of the drain breakdown current, it was required a multi-port component able to:

- supply the drain breakdown current $I_{BD,dS}$ depending on V_{GS} and V_{DS} as shown in figure 3.13,
- sense V_{DS},
- sense V_{GS}.

For this reason, a non-linear two port voltage controlled current source component as in figure 3.16 is the best option, since one can choose the dependence of each port voltage and current. In Keysight Advanced Design System, the most suited component is the 2 port "symbolically-defined device" (SDD2P). As indicated in figure 3.16, the port 1 is dedicated to the $V_1 \equiv V_{GS}$ sensing, and for this reason, we set the supplied current value to minimum value allowed i.e. $I_1 = 10^{-30}$. Instead port 2 must sense $V_{DS} \equiv V_2$ and supply the $I_{BD,DS}(V_{DS}, V_{GS}) \equiv I_2$.

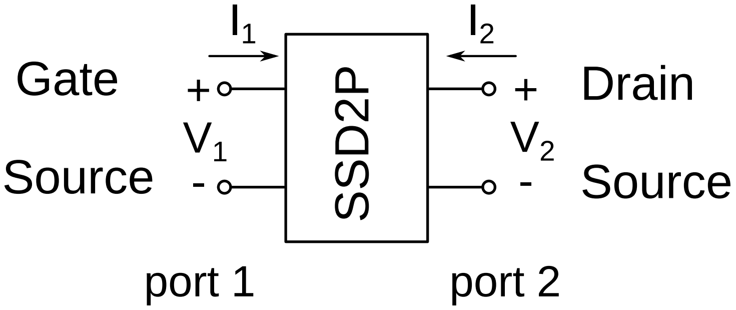


Figure 3.16: 2 port component used in SPICE simulations to supply the breakdown current $I_{BD,DS}$. The port 1 is used for the V_{GS} sensing without absorbing any current, port 2 is employed to sense V_{DS} and to supply $I_{BD,DS}(V_{DS}, V_{GS})$.

In order to efficiently fit the measurement results of figure 3.13(a), the following equations are used [22]:

$$I_{BD,DS}(V_{DS}, V_{GS}) = \begin{cases} 0, & \text{if } V_{DS} < V_{BD,DS}. \\ 0.18A/V^2 \cdot (V_{DS} - V_{BD,DS})^2, & \text{otherwise.} \end{cases} \tag{3.1}$$

where

$$V_{BD,DS}(V_{DS}, V_{GS}) = \begin{cases} 2\ V, & \text{if } V_{GS} > -1\ V. \\ 0.36\, V_{GS} + 2.35\, V, & \text{otherwise.} \end{cases} \tag{3.2}$$

The fitting curves relative to 3.1 are indicated by solid lines in figure 3.13(a), whereas the equation 3.2 was fitted by solid blue line in figure 3.13(b). We used a polynomial fit in equation 3.1 because it did not bring to any convergence issue in the used simulation software. Moreover, the snapback (e.g. for $V_{GS} = -0.5\ V$ in figure 3.13) was neglected, since it is very small.

We want to remark that this model was developed under specific device and bias conditions, i.e. pulsing the drain by TLP on a multi-finger device under constant DC V_{GS} condition, for $V_{GS} \geq -4\ V$, fixed $V_{BS} = 0\ V$ and it is valid in this range of operation[2].

3.7 TIM calibration for ON and OFF states

The continuous semiconductor device reduction size impacts on the testing instrumentation and measurement techniques. This fact involves also TIM technique and the quantification of the phase shift. Previous multi-finger periodic structure investigated by TIM [12] did not report any significant issues because the fingers were well-spaced one to the other. The observed isolated optical effects due to edge scattering were ignored at that time.

As already written at the beginning of the chapter, the devices under test were characterized by drain-source pitch of 0.56 μm with common $L_G = 0.13\ \mu m$. Comparing these sizes with the minimum optical space resolution of TIM of around $1.5\mu m$ [17], we end up that the probing laser beam spot averages the information of at least three fingers: possible finger-to-finger thermal or free-carrier signal variations cannot be resolved.

Another point was also the very low TIM heterodyne signal due to low signal-to-noise ratio encountered if shining the laser spot onto the highly dense multi-finger region, see figure 3.2a. This fact in particular is even worst than previous point. One can see this by the measured heterodyne waveforms shown in figure 3.17. In figure 3.17a, a low heterodyne waveform is collected at laser spot position at the active region of a 150 multi-finger device. We clearly see that in 3.17a, the heterodyne signal is very low and phase extraction might be ambiguous or impossible due to the extremely low heterodyne signal-to-noise ratio. The same device but rotated in respect to its center (i.e. with a different angle) produces an acceptable heterodyne signal as shown in figure 3.17b. On 3.17b the signal amplitude A_{het} is $A_{het} = 0.1\ V \geq 0.04\ V$ which is considered the limit of acceptable signal to be post processed to correctly extract the phase shift.

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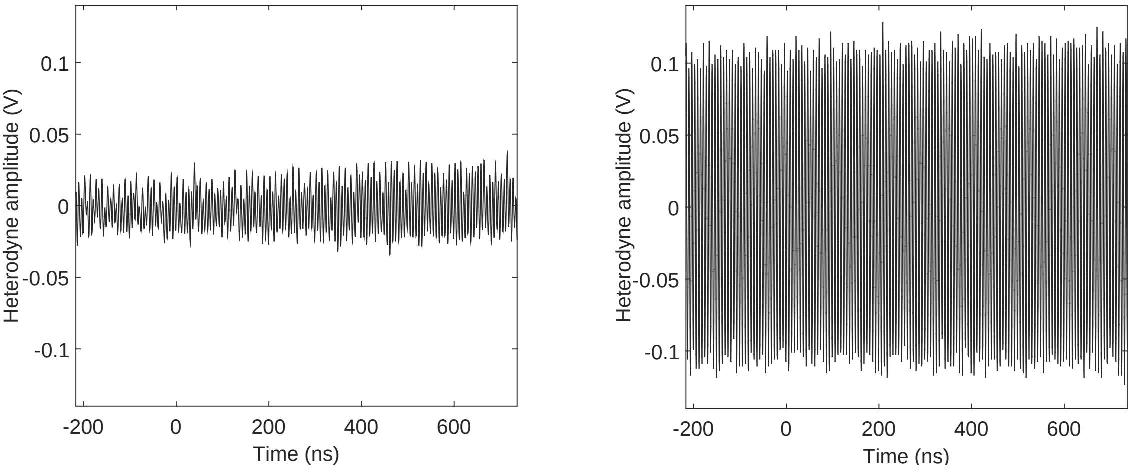
[2] No investigation was done for different V_{BS} condition due to lack of devices.



(a) Example of low heterodyne signal shining the device into the multi-finger active region.

(b) Example of high heterodyne signal shining the device into the multi-finger active region.

Figure 3.17: Heterodyne amplitude comparison on the same device location but with the rotated device in two different locations.

The results in figure 3.17 suggest that we are in presence of a device characterized by optical anisotropic behavior never seen before in any previous studied devices by TIM. Rotating the device, we find that the heterodyne amplitude varies between a maximum heterodyne signal as in figure 3.17b to a minimum heterodyne signal as in 3.17a.

During the preparation of a TIM measurement, a device and the necessary positioners to supply the electrical stress are positioned onto the mechanical stage, see setup picture in figure 3.18. The choice of the location of the positioners is really limited (sometimes even unique) and moreover the lack of space on the stage does not allow to rotate enough the device in order to find the maximum heterodyne signal.

In order to know how to:

- quantitatively interpret the phase shift and
- to have high signal-to-noise ratio,

we introduced a half wave plate (HWP) [22] into the scanning TIM setup of [17], see setup picture in figure 3.18. The HWP introduces a rotation of an angle 2θ to the polarized beam incoming into the device where θ is the angle between the setup main axis and the HWP position (see figure 3.19(a, b) for the setup main axis and the multi-finger parallel axis definitions). Rotating the HWP, we can find the maximum reflectivity signal locations. The HWP is located between the polarizing beam splitter (PBS) and the DUT. The HWP does not impact on the phase shift extraction or alter the working principle of TIM, rather it allows to rotate the linear laser beam traveling to the device.

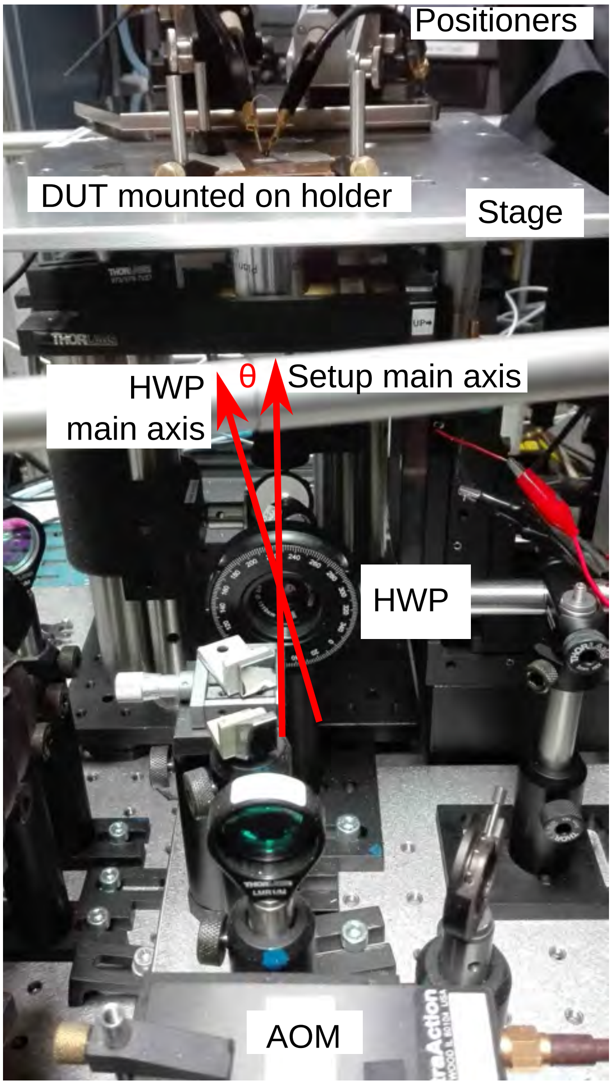


Figure 3.18: Setup picture with the half wave plate in the TIM setup. On the top of the picture, we can also see the device under test positioned on the stage and contacted by two probe needles.

In the first experiment, we wanted to see the effect on the heterodyne amplitude rotating the HWP by a certain angle θ when the laser beam shined the active region. For this reason and to facilitate the comprehension of the results, we defined the difference angle $\theta_{diff} = \theta - \alpha$ where α is the angle between the setup main axis and the multi-finger parallel axis along the fingers (see 3.19(b)). We discovered that rotating the HWP gave rise to a periodic reflectivity of period 90° with local and absolute maximum regions as indicated in figure 3.20. Samples with flat-reflecting-behavior surface would show constant reflectivity. In these devices however, locals maximums at $\theta = 45°$ and at $\theta = 135°$ are shifted of 45° in respect to the absolute maximum peaks at $\theta = 0°$ and $\theta = 90°$. The locations of absolute maximum regions correspond to parallel polarization to fingers and the region of local maximum regions to perpendicular polarization (see 3.19(b)).

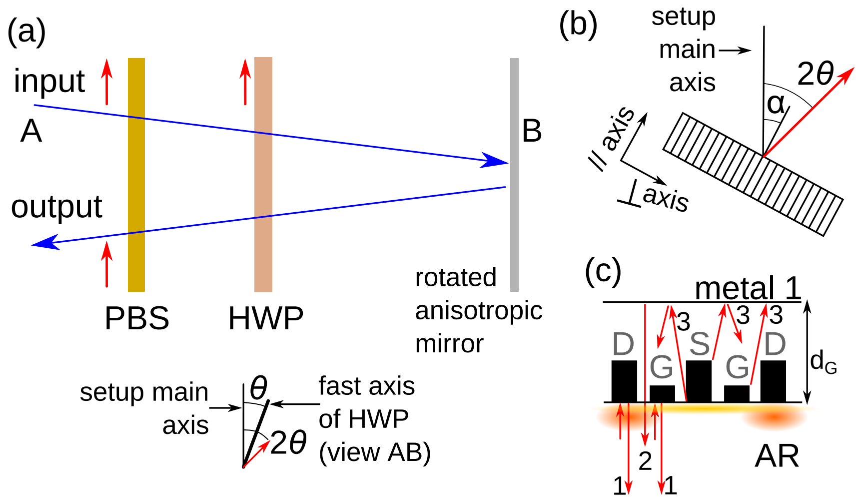


Figure 3.19: (a) Modified TIM setup with possibility of polarization rotation of incident beam: half wave plate (HWP), polarizing beam splitter (PBS), sample (B). The beam polarization is indicated by the red arrow. Elements like e.g. microscope objective are disregarded since they do not affect the polarization. (b) Orientation of the sample (angle α) and beam polarization (angle 2θ) against the main setup axis. (c) Schematic explanation of interference between different parts of the same probing beams; 1-light reflected on drain, source and gate metallizations; 2-light reflected on metal 1; 3-scattered light; AR-active region. Taken from [22].

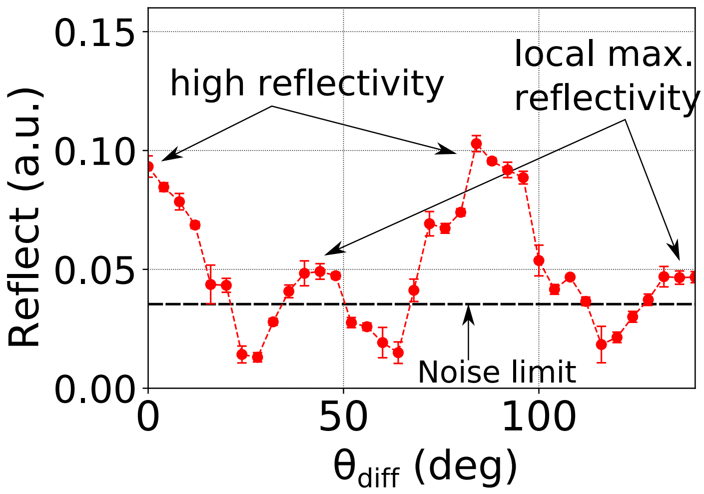


Figure 3.20: Reflectivity cross section in function of the angle θ between the multi-finger parallel direction and the setup main axis.

In the second experiment, the impact of the multi-finger structure onto the extracted phase shift was tested by TIM measurements stressing the device in two configurations:

1. in breakdown condition (OFF-state) for pulsed drain, grounded source, grounded bulk and grounded gate (shortly indicated by DvsGSB configuration) applying a

TLP pulse with $(PW, RT) = (650, 1)\ ns$ with $(V_{DUT}, I_{DUT}) = (3\ V, 0.2\ A)$

2. in normal mode (ON-state, since the device operates in saturation regime) applying a constant DC $V_{GS} = 1.2\ V$ and pulsing the drain versus grounded bulk and grounded source configuration with TLP pulse with $(PW, RT) = (450, 1)\ ns$ with $(V_{DUT}, I_{DUT}) = (2\ V, 0.5\ A)$.

The two configurations were chosen to measure the impact of heat source distribution located at the channel level close to the multi-finger structure (for $V_{GS} = 1.2\ V$) and deeper in the substrate as in DvsGSB condition. The results are shown and compared for $t = 200\ ns$ on figure 3.21a for OFF-state and in figure 3.21b. For each condition, three plots are shown, from the top: (1) reflectivity (the reflectivity used previously in figure 3.20 is the same as in 3.21a(1)), (2) theoretical versus measured phase shift and (3) TIM coefficient k defined by the ratio:

$$k = \frac{\phi_{measured}}{\phi_{theoretical}} \tag{3.3}$$

where $\phi_{theoretical}$ is the theoretical phase shift is obtained from [19] and $\phi_{measured}$ is the measured phase shift extracted from the heterodyne waveform.

We immediately note from plots 3.21a(2) and 3.21a(3) that the phase shift in correspondence of the maximum reflectivity is half of the theoretical $k = k_{BREAK} = 0.5$ with negligible standard deviation for a wide region of the HWP ($\theta_{diff} = [70°, 100°]$). In the region of local maximum heterodyne signal (i.e. for $\theta_{diff} = 45°$) the measured and theoretical phase shifts almost coincided (here $k = k_{BREAK} = 1$) but the standard deviation is higher. At the minimum reflectivity positions, we note a wide standard deviation because of the noise in the experiment.

Similar comments can be derived from the experiment in normal operation mode when gate was biased above the threshold voltage[3]. Here, the phase shift measured is even lower than half of the expected as in breakdown condition; this fact is another sign confirming the fact that also the location of the heat dissipation in the substrate must be taken into account. We see that the average TIM coefficient is $k = k_{NORM} = 0.18$ in the region of max heterodyne signal [22].

One can think that this reduction of measured phase shift might be due to the fact that power is dissipated somewhere else [19]. For instance, power might be dissipated in the metal wires and pads, all of them are not accessible by TIM due to the presence of insulator material and passivation "hiding" the thermal power dissipation due to the poor thermal conductivity. Although we calculated the series resistance at drain and source for this technology, it resulted to have negligible impact on the power dissipation.

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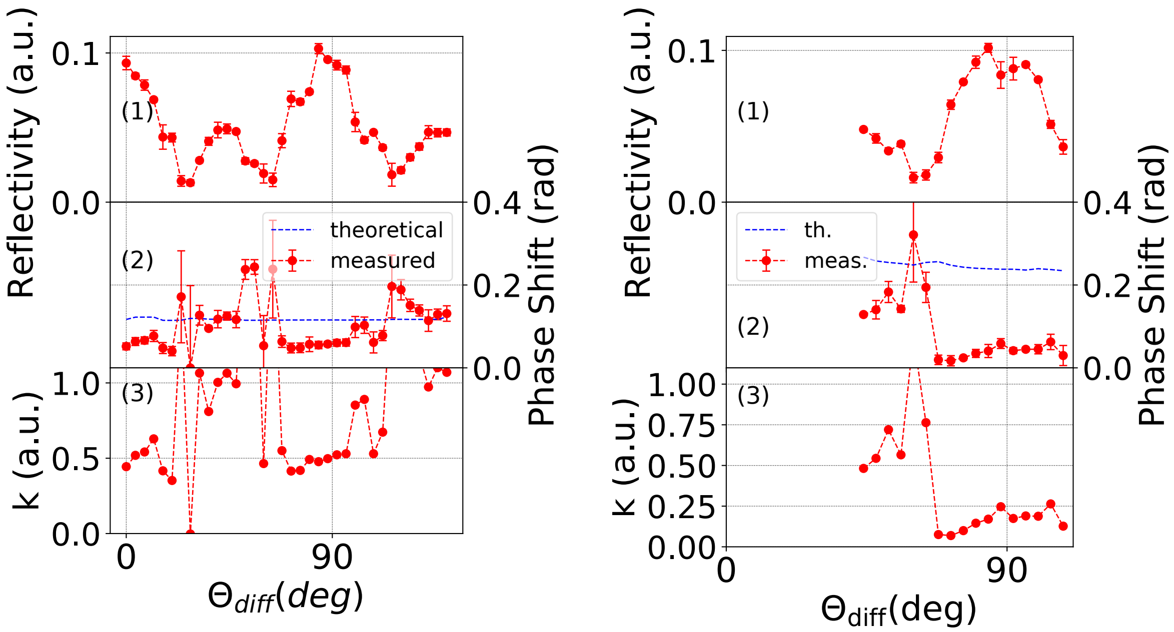
[3] Note that the measurements were carried out only in a limited range of θ_{diff} for less than a period $\theta_{diff} = [50°, 120°]$ thanks to what previously stated about the reflectivity periodicity and its impact on the measured phase shift for breakdown conditions.



(a) Results for OFF-state/breakdown condition in configuration positive TLP pulses at drain versus grounded gate, grounded source and grounded bulk configuration. $(V_{DUT}, I_{DUT}) = (3\ V, 0.2\ A)$. Taken from [22].

(b) Results for ON-state/normal operation mode in configuration positive TLP pulses at drain versus grounded source and grounded bulk configuration. Gate is biased at constant 1.2 V. $(V_{DUT}, I_{DUT}) = (2\ V, 0.5\ A)$.

Figure 3.21: (1) Measured reflectivity, (2) phase shift and (3) TIM coefficient as a function of θ_{diff}, where θ is the HWP angle and α is the sample angle, c.f. 3.19(b). The phase shift was measured in the center of a single multi-finger block (W = 1.95 mm) at time 200 ns.

The summary of the TIM coefficent for normal k_{NORM} and breakdown k_{BREAK} are displayed in 3.3. These values will be used to compare the simulated versus measured phase shift presented in the next chapter on the stacked devices.

Table 3.3: TIM coefficients k.

k	
k_{NORM}	0.18
k_{BREAK}	0.5

We analyze now the reasons of reflectivity and phase shift anisotropy. What is happening to the reflectivity in figures 3.21a and 3.21b seemed to be similar to the effect of a wire polarizer [11]. A wire polarizer consists of many parallel metallic conducting wires which produce a linear polarized beam out of a unpolarized beam. In such component, the parallel beam component to the grids is totally reflected by the metal grids, while the perpendicular component is totally transmitted [11]. In our case, gate, drain and source fingers acted as the wires and can be considered as a grating. The returning beam is generally elliptically polarized and only one polarization component passes through the PBS. This fact explains the the variation of the reflectivity in function of θ_{diff}. Only a part of the incoming beam to the DUT is directly reflected back as depicted in the sketch of figure 3.19(c)by the number (1). Another part indicated by (2) in figure 3.19(c) is associated to the reflected beam from the upper metal levels (in figure only "metal 1" is marked). These two optical effects could also combine together and due to the height of the reflection of (2) marked by d_G could also bring to interference explaining why $k_{ON} < 1$ and $k_{OFF} < 1$. The difference between theoretical and measured phase shifts follows now and it refers to figure 3.19(c). The phenomenon marked by (3) indicates the near field effects such as edge scattering that can occur in the multi-finger active region. Scattering phenomena can be also influenced by the refractive index (and temperature) profiles depending on the device operation (normal mode or breakdown mode). This latter fact also explains why $k_{ON} < k_{OFF}$. Optical simulations reported in appendix B showed that the measurements in figure 3.20 and 3.21 can be reproduced.

In the following, all presented TIM results were carried out at the maximum heterodyne signal in the active region in order to maximize the signal-to-noise ratio, even though this implies a reduction of phase shift response due to scattering effects. Probing the device where local maximum heterodyne signal occur is risky and unsafe: 1) standard deviation is higher due to lower signal-to-noise ratio and 2) this operating region are very small and possible defocusing problem during TIM and mechanical movement of the stage could easily bring to work very close to regions where very low signal-to-noise region occurs (i.e. the minimum heterodyne signal at $\theta = 25°$ and $\theta = 67°$).

The finding of these TIM coefficient needs to be incorporated into the total phase shift $\Delta\phi_{total,i}(t)$ equation from [19] as in [22] to correctly interpret the final measured phase shift:

$$\Delta\phi_{total,i}(t) = 2 \cdot 2\pi/\lambda \cdot dn/dT \cdot [k_{NORM} \cdot E_{DISS,NORM,i}(t) + k_{BREAK} \cdot E_{DISS,BREAK,i}(t)] \tag{3.4}$$

where

$$E_{DISS,NORM,i}(t) = \frac{1}{A}\int_0^t V_{DS,i}(\tau) \cdot I_{NORM,i}(\tau)d\tau \tag{3.5}$$

$$E_{DISS,BREAK,i}(t) = \frac{1}{A}\int_0^t V_{DS,i}(\tau) \cdot I_{BREAK,i}(\tau)d\tau \tag{3.6}$$

with the laser probe wavelength $\lambda = 1.3\ \mu m$, the thermo-optical coefficient for silicon $dn/dT = 1.9 \times 10^{-4}\ K^{-1}$ [19], the thermal energy dissipated in the normal (breakdown) mode of the i^{th} transistor $E_{DISS,NORM,i}$ ($E_{DISS,BREAK,i}$), the V_{DS} of the i^{th} transistor $V_{DS,i}$, the normal (breakdown) current component of the i^{th} transistor $I_{NORM,i}$ ($I_{BREAK,i}$) and the effective area of the block A.

These new TIM correction coefficients and the new equations will be used to compare measured versus simulated phase shift in the next chapter on stacked transistors.

3.8 TLP investigation on grounded gate versus floating gate

So far, we concentrated on the breakdown mechanisms and modeling, without discussing any failure topic. The multi-finger test structure investigation on 150 finger MOSFET is presented here with different conditions of the stress pulse, like RT and PW. TIM results and failure analysis are also presented for two specific configurations.

The devices have been stressed applying positive TLP pulses on drain versus grounded source. Gate and bulk pads were let floating or contacted to ground. The pad configuration abbreviations are shown in table 3.4.

Table 3.4: Pad configuration abbreviation. “gnd” means grounded pad and “float.” stands for floating pad.

Stress option	Drain	Source	Gate	Bulk
DvsS	+	gnd	float.	float.
DvsSB	+	gnd	float.	gnd
DvsGS	+	gnd	gnd	float.
DvsGSB	+	gnd	gnd	gnd
DvsG	+	float.	gnd	float.
DvsGB	+	float.	gnd	gnd

The TLP-IVs for the first four pad configurations and same TLP stress conditions $(PW, RT) = (100, 1)$ ns are reported in figure 3.22. From figure 3.22, we noted that the different pad configuration result into wide I_{t2} variation as well as TLP-IV curves.

If the gate was let floating as in DvsS and DvsSB configurations, we reached high $I_{t2} \approx 8$ A and current starts flowing from low voltage. Letting the gate floating allowed to form the inversion channel thanks to the presence of C_{GS} and C_{GD} and the dV/dt effect during the rise time. A minimum $V_{DS} = 0.6$ $V = 2 \cdot V_{TH}$ was necessary to invert the channel transistor and allow the channel current to flow. This phenomenon is called *gate coupling effect* [9] and it is widely used and exploited in the ESD community to help to turn on MOSFET protection devices by drain channel conduction [9, 99] whenever the gate is not grounded. On the other side, for DvsGSB the $V_{BD,DS}$ voltage increased to 2.4 V without showing any clear presence of snapback behavior (the curve in DvsGSB is also partially shown in figure 3.8 for $N_F = 150$).

The two configurations showing extreme minimum and maximum I_{t2} values, i.e. DvsS and DvsGSB, were chosen to make a PW variation study in order to have more information

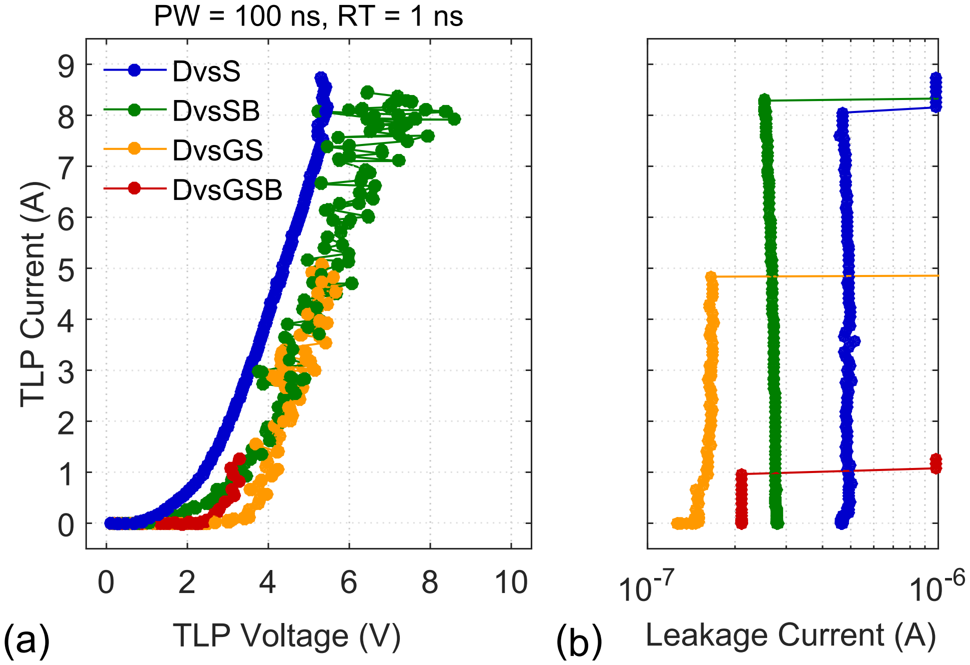


Figure 3.22: (a) Measured TLP-IV at $PW = 100\ ns$, $RT = 1\ ns$ and (b) monitored leakage IVs at 0.1 V for 150 multi-finger transistor. Taken from [21].

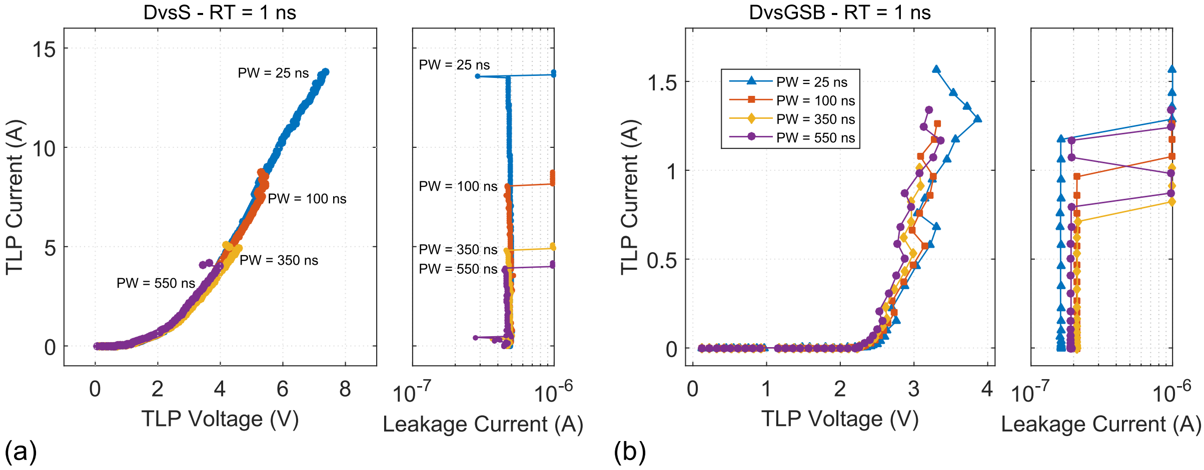


Figure 3.23: PW variation study for constant $RT = 1\ ns$ on 150 multi-finger transistor, for (a) DvsS and (b) DvsGSB configuration. The PW is indicated closed to each curve or in the legend. Taken from [21].

about the nature of the failure. The results are displayed in figure 3.23. In figure 3.23, four TLP-IVs for the two configuration are displayed for $PW = [25, 100, 350, 550]\ ns$. The RT was kept constant to 1 ns for both.

From the results of DvsS configuration, we note very good performance of the multi-finger device, exploiting the gate coupling effect. Furthermore, there is a clear dependence of I_{t2} from the PW for this configuration.

On the other side, when the gate is grounded as in DvsGSB, a constant $I_{t2} \approx 1\ A$ not depending on PW was revealed.

The summary plot of the I_{t2} vs. PW for DvsGSB and DvsS is shown in figure 3.24(a) and in (b) is shown the E_{fail} versus PW. Only for DvsGSB configuration, the same PW dependent study was carried out for $RT = 10\ ns$ (see ther red dots).

The E_{fail} versus PW plot is very important to have information about the failure root cause and it is similar to the Wunsch-Bell plot [10, 31]. The Wunsch-Bell plot shows the normalized failure power P_{fail} on the involved device area over the PW [10]. However, in figure 3.24 we have plotted the E_{fail} but analogous considerations can be done.

Different mechanisms could lead a device to the failure, and they show their time dependence according to different data slopes. Generally, from theory in [25, 26] for very short PW, the failure is adiabatic or P_{fail} is $1/t$ dependent, this means that the failure is not due to overheating or high temperature. An example of non-thermal failure is the gate oxide failure, generally due to voltage overstress. For very long PW, the P_{fail} becomes constant. In the middle, a common thermal failure would show a $1/\sqrt{t}$ dependence on a P_{fail} Wunsch-Bell plot.

We noted that for DvsGSB, the I_{t2} is RT dependent but not PW dependent, observing an $I_{t2} = 4\ A$ for $RT = 10\ ns$ and $I_{t2} = 4\ 1$ for $RT = 1\ ns$. Only the last point at $PW = 550\ ns$ shows a slightly lower I_{t2}. In the E_{fail} plot for DvsGSB configuration, this results into non-thermal E_{fail} dependence [25, 26] but rather flat characteristic because not proportional to $t^{0.5}$. Therefore from the TLP study of I_{t2} and E_{fail} analysis of DvsGSB, the 150 multi-finger transistor seemed to fail due to a non-thermal phenomenon. Due to the configuration, we could hypothesize at this point that the possible non-thermal failure could be due to GOX failure rather than a possible inhomongeneous power dissipation.

On the other side, the configuration DvsS showed the opposite behavior. I_{t2} was decreasing as long as the PW increases and the E_{fail} plot showed a perfect $t^{0.5}$ slope, indicating a typical thermal failure as described in [10, 31] due to high current density and high temperature in silicon. Due to the clarity of the results of DvsS for $RT = 1\ ns$, it was not necessary to carry out a study for $RT = 10\ ns$ for such configuration.

The possible non-thermal failure for DvsGSB configuration suggested to verify what is happening on devices with 1, 2 and 4 fingers used in previous investigations. The results of V_{t2} is shown in figure 3.25 for $(PW, RT) = (100, 1)\ ns$. We clearly note that V_{t2} did not scale with the W_{TOT} or N_F for the configuration DvsGSB but rather it remained bounded to 3.5 V. From this consideration, the hypothesis of GOX failure for DvsGSB became stronger than the inhomogenous power dissipation due to inhomogenous PBJT triggering.

Besides these results and to complete the TLP characterization, the gate oxide failure limit was probed in the configuration DvsG for $PW = 100\ ns$ and $RT = 1\ ns$. The TLP-IV is shown in figure 3.26(1) with the leakage-IV at 0.1 V in 3.26(2). The main outcome is that the V_{t2} is 6.4 V. A TLP in DvsGB showed $V_{t2} = 6.6\,V$. We could therefore state

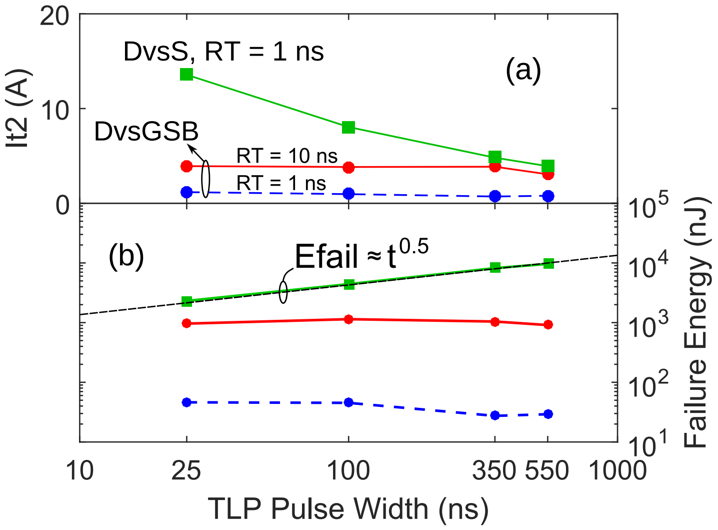


Figure 3.24: (a) I_{t2} and (b) E_{fail} based on the results of figure 3.23 for a 150 multi-finger transistor. The RT, PW and configuration are indicated only on the I_{t2} plot based of the same color curve convention adopted. Taken from [21].

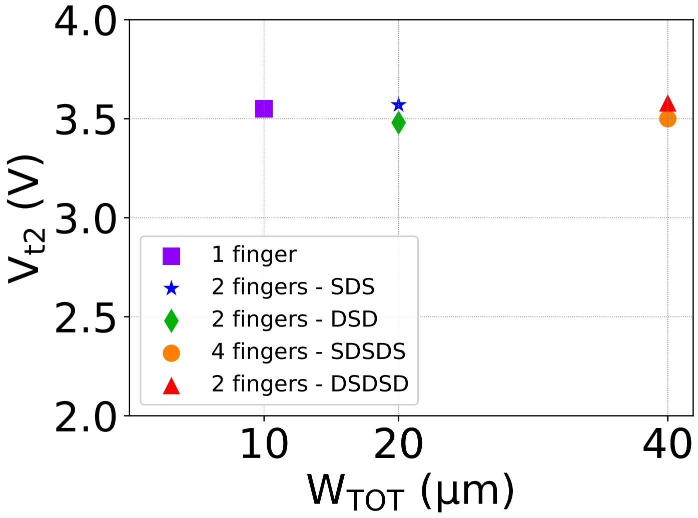


Figure 3.25: V_{t2} extracted for devices with different W_{TOT} for TLP carried out in DvsGSB configurations for $(PW, RT) = (100, 1)$ ns. The number of finger and the configuration of finger probed is indicated in the legend.

that the GOX failure was $\approx 6.5\,V$ for this technology and it gives the operation limit in pulsed mode. The found GOX failure was in line with the values found in literature for similar GOX of 2.2 nm as in [7, 13, 30].

Thus, if for DvsS configuration a typical thermal failure seemed to be the failure root cause for the 150 multi-finger transistor, for the other configuration in DvsGSB, we saw a possible non-thermal failure. A possible reason of non-thermal failure is the GOX failure:

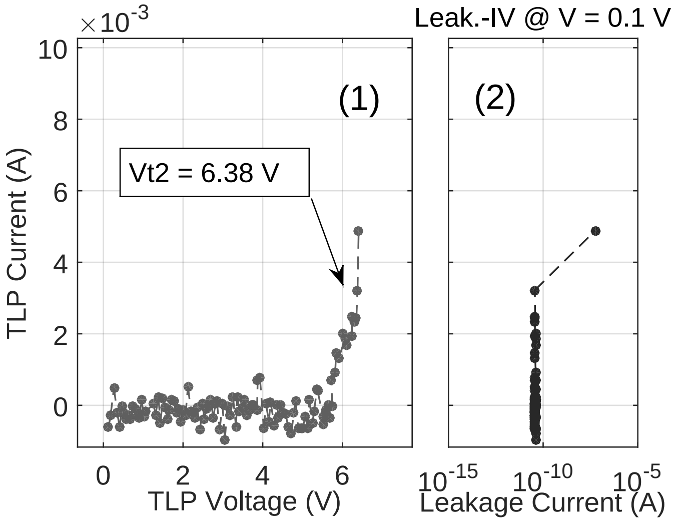


Figure 3.26: (1) TLP-IV on 150 multi-finger transistor in DvsG configuration for PW = 100 ns, RT = 1 ns and avg. window . (2) Leakage IV at 0.1 V.

indication from I_{t2} RT dependence and constant V_{t2} are very important in this sense.

All these considerations led to the TIM study to check if power is dissipated homogeneously during a TLP pulse.

3.8.1 TIM measurements

The two configurations were probed by TIM measurements along the same path indicated in figure 3.2b consisting on a line covering all fingers in the middle.

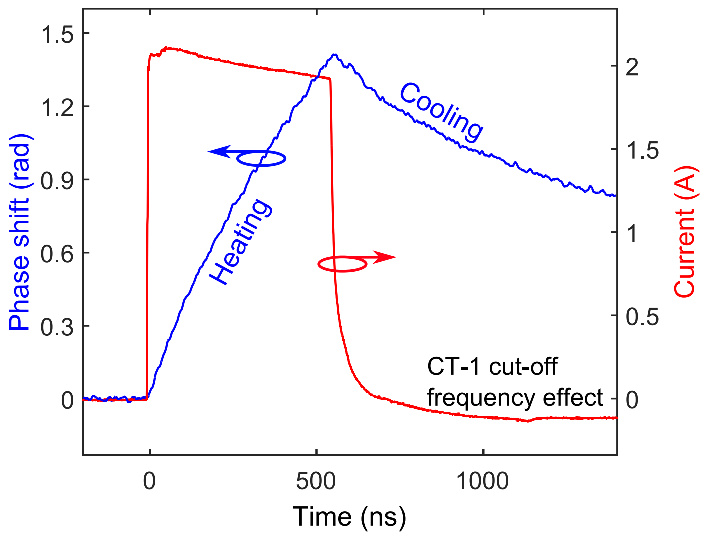
In figure 3.27b, the phase shift cross-section for different time instants from TIM scan result in DvsS configuration for $PW = 550\ ns$ and $RT = 1\ ns$ is displayed. The current pulse time aligned with a phase shift transient waveform are shown in figure 3.27a. The voltage transient waveform is not shown, however the $V_{DUT} = 2.5\ V$. The phase shift transient waveform is associated to the position indicated by a dashed line in figure 3.27b for position $X = 46 \mu m$ located in the middle of the device. From figure 3.27b, we saw that there is no inhomogenous power dissipation in any of the selected time instants. We rather observed a homogenous phase shift throughout the fingers. Then, possible features (in particular visible for $t \geq 350\ ns$) in the phase shift are due to optical artifacts, since they are well below the thermal diffusion length and related to multi-finger device structure.

To probe the device in DvsGSB for $PW = 350\ ns$ and $RT = 10\ ns$. We chose to probe the device at $RT = 10\ ns$ instead of 1 ns because the I_{t2} is four time higher and the failures root causes for $RT = 10\ ns$ and $RT = 1\ ns$ are the same from figure 3.24(b)[4].

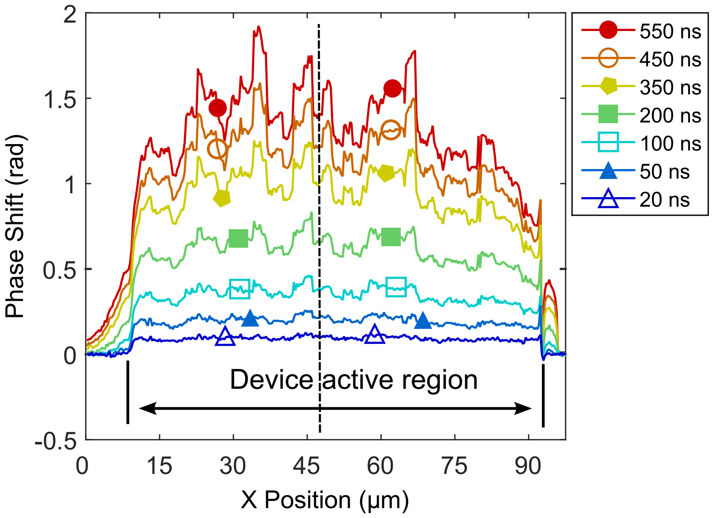
---

[4] The low I_{t2} for $RT = 1\ ns$ limits the phase shift[19]; we tried also several measurements for for $RT = 1\ ns$ but they were unsuccessful because they were at the detection limit due to low signal to noise ratio [21].

We noted that before ($t = 200$ ns) and at the pulse end (350 ns), the phase shift can be considered homogeneous.The two hills on the two sides of the device can be considered at the noise level. Anyway, that seems to strengthen the non-thermal failure hypothesis for DvsGSB configuration excluding once more an inhomogeneous bipolar action.



(a) TLP current pulse employed during the TIM scan in DvsS configuration and transient phase shift waveform relative to position $X = 46$ μm indicated in (a) by a vertical dotted line.



(b) Phase shift cross section of the TIM scan in DvsS configuration at for increasing time instants. The scan path is shown in figure 3.2b.

Figure 3.27: TIM results for configuration DvsGSB for $RT = 1ns$ and $PW = 550$ ns. Both figures are taken from [21].

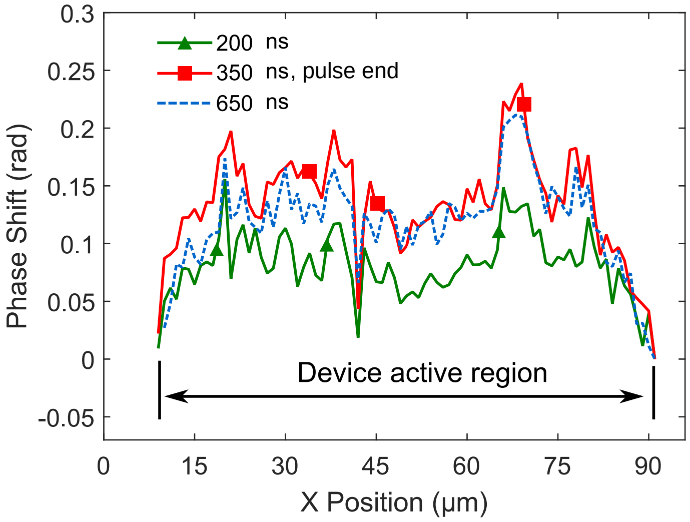


Figure 3.28: Phase shift distribution of the TIM scan in DvsGSB configuration at $RT = 10\ ns$ and $PW = 350\ ns$. The scan path is shown in figure 3.2b. The sharp transitions in the phase below the thermal diffusion length are related to optical artifacts. Taken from [21].

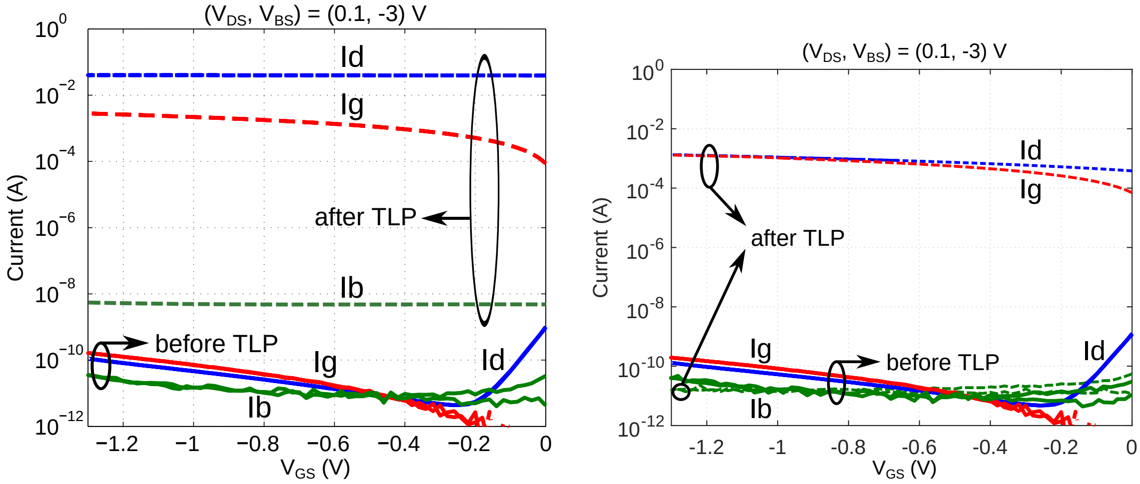
3.8.2 Post-stress analysis and failure mechanism discussion

Finally, the two configurations were probed by OFF-state transfer DC-IV measurements by a semiconductor parameter analyzer to identify the failed junctions (results in figure 3.29) and afterwards a lift-off process to localize the failure regions by scanning electron microscopy (SEM) at the failure analysis laboratory of Infineon Technologies AG was carried out (results in figure 3.30).

The OFF-state transfer characteristics for $(V_{DS}, V_{BS}) = (0.1, -3)\ V$ before (solid lines) and after (dashed lines) TLP are displayed in figure 3.29 in (a) for DvsS after a TLP with $(PW, RT) = (550, 1)\ ns$ and in (b) for DvsGSB after $(PW, RT) = (25, 1)\ ns$ TLP.

From figure 3.29a, we saw that the main leakage path was between drain and source junctions (source current is not shown). The SEM image in 3.29(c) after a TLP for DvsS shows a clear silicon melting in correspondence of the drain and source metal wires due to the extremely high current density.

The electrical leakage failure analysis after DvsGSB shown in 3.29b indicated that the highest leakage path is on the drain-gate, again supporting the hypothesis of GOX damage. The bulk contact seemed to be not affected at the stress because we did not see any appreciable current increase after this kind of stress. An additional measurement with floating bulk and grounded source and drain terminals reported in figure 3.31 confirmed the gate-drain path to be more leaky than the gate-source. Very interesting is the SEM picture in figure 3.30b. This latter was located in the gate wire connection corner with the poly-silicon ring and we see that the poly-silicon gate lines are damaged/disappeared

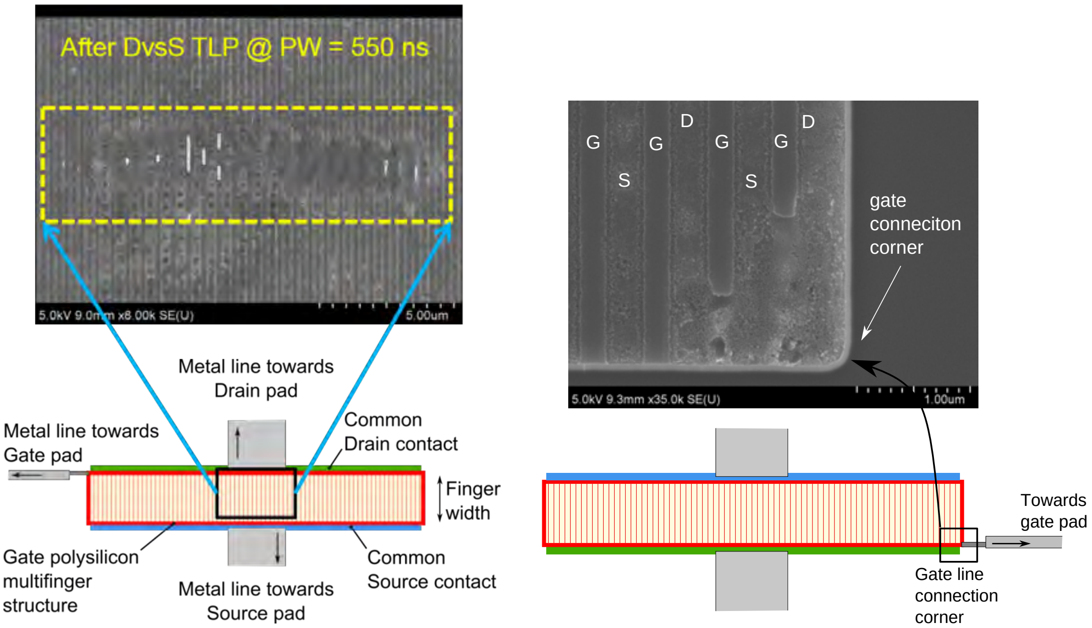


(a) After TLP for DvsS, $(PW, RT) = (550, 1)$ ns.

(b) After TLP for DvsGSB, $(PW, RT) = (25, 1)$ ns.

Figure 3.29: OFF-state DC leakage failure analysis of two devices stressed in the two different configurations. Taken from [21].

and also the first drain finger (see the letter "D" in figure 3.30b). The lack of part of the gate polysilicon fingers indicated that the GOX is the main failure root cause for this configuration. The location and the nature of the failure suggested that the poly-silicon ring and the multi-finger gate structure should be also considered as distributed resistor network, where the local impedance in the multi-finger structures varies (in particular being 0 in the gate connection corner). This network caused the drain voltage division thanks to the presence of C_{GD} and C_{GS} (gate coupling effect) wherever the local impedance can be considered higher than 0. In figure 3.32, a cross-section of one MOSFET finger is drawn in DvsGSB configuration with the gate capacitors (C_{GS}, C_{GD} and C_{GB}) and a poly-silicon resistor $R_{g,poly}(x, y)$ representing the value depending on the position of the finger in respect to the gate connection corner. $R_{g,poly}(x, y)$ would be $\approx 0\Omega$ in the proximity of the gate connection corner where no gate coupling effect might be possible and where there is the maximum dV/dt during the rise time. Far from the corner, the impedance to the corner is higher than the gate coupling (and therefore the voltage division) can always occur. The RT dependent of such configuration is explained by the interaction of all gate capacitors C_{GS}, C_{GD} and C_{GB} (we mention only these for simplicity but there few more involved in this process). As soon as the bulk and gate are grounded, additional short circuit paths at the pulse beginning exist. Therefore, C_{GB} increases the transient voltage built-up. Since this capacitance is non-linear having larger values at low voltages, for short RT (for instance at 1 ns) the short circuit effect due to the dV/dt effects is higher leading to GOX failure.



(a) SEM image of a 150 multi-finger transistor after failure by TLP for DvsGSB, $(PW, RT) = (550, 1)$ ns. The picture corresponds to the region marked in the device layout drawn below. Note the silicon melting in the central region of the figure corresponding to the region where metal wire to pads are located. Courtesy of Werner Simbürger from Infineon Technologies AG.

(b) SEM image of a 150 multi-finger transistor after failure by TLP for DvsGSB, $(PW, RT) = (100, 1)$ ns. The picture corresponds to the region marked in the device layout drawn below. The gate, drain and source finger are indicated by “D”, “G” and “S”, respectively. Note the failure in the gate connection corner. Most of the failure extend in the first drain finger. Courtesy of Werner Simbürger from Infineon Technologies AG.

Figure 3.30: Failure analysis of two devices stressed in the two different configurations. Taken from [21].

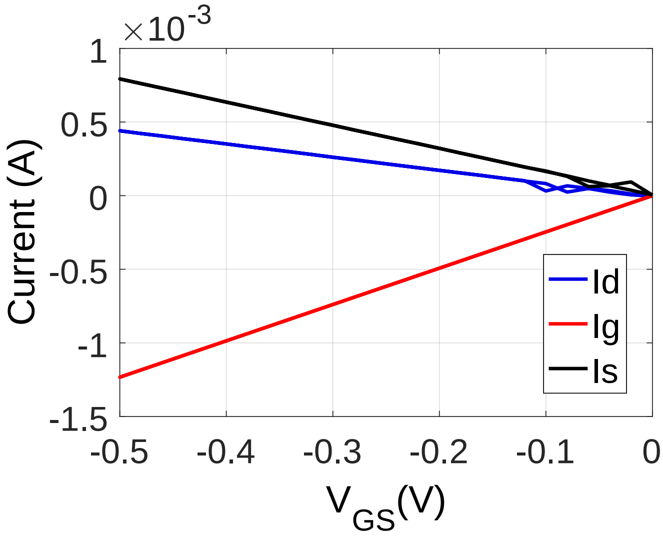


Figure 3.31: DC leakage carried out sweeping the V_G voltage and setting to ground potential both V_S and V_D. The bulk was let floating.

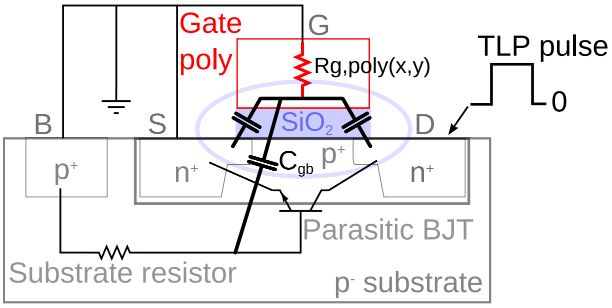


Figure 3.32: Cross-section of one MOSFET finger of the transistor in DvsGSB configuration. The gate polysilicon resistor ($R_{g,poly}(x,y)$) value varies depending on the position of the finger in the device in respect to the gate connection corner. Taken from [21].

3.9 Summary

A wide investigation was carried out on single-finger and multi-finger test structures in order to understand the drain and gate breakdown variations and failure. Thanks to these studies, the device risk bias conditions and failure limits were found. MOreover, these studies are the basis for an ESD self-protection approach for stacked transistors.

Firstly, we investigated the breakdown phenomena varying L_G and N_F and gate status. A strong finger-to-finger coupling via substrate was revealed to trigger open-base breakdown or PBJT. From a detailed investigation of the drain-source breakdown behavior, the strong dependency on gate-source bias emerged. In particular, the drain breakdown voltage decreased as the V_{GS} decreased towards negative values. The cause of this reduction was found to be the gate induced drain leakage mechanism. Then, also the GOX failure limits were measured and found to be similar to literature values for the studied oxide thickness. A pictorial summarizing view of the main founded limits and behavior is reported in figure 3.33. Finally, the existing MOSFET model was extended, developing a wide drain breakdown model dependent on V_{GS} from TLP measurements condition.

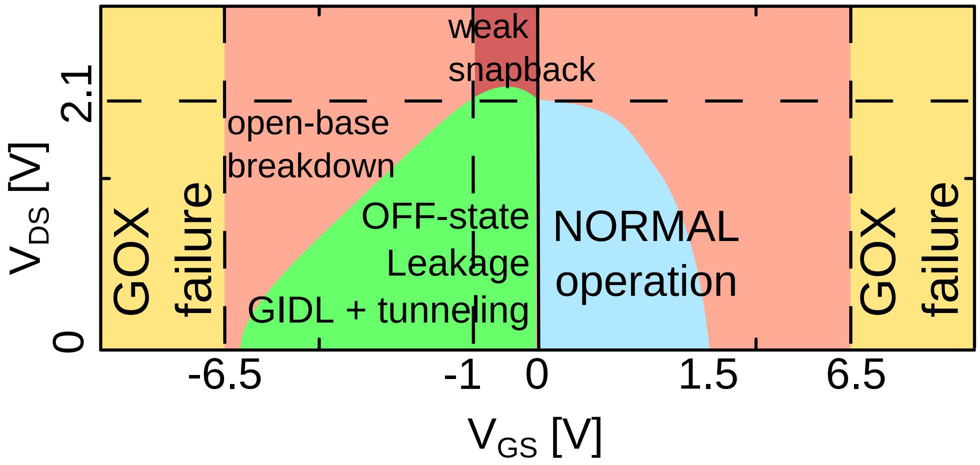


Figure 3.33: Status of multi-finger transistor test structure in the studied configuration varying (V_{GS}, V_{DS}) for $V_{BS} = 0\ V$.

Secondly, we calibrated our TIM measurements for device operations in normal and breakdown modes: the first was carried out above the device threshold voltage, whereas the second for gate grounded condition. We included a half wave plate in the TIM setup to rotate the linear laser polarization of the probed and reflected beams to see the effects on the multi-finger transistor test structures and also to allow more flexibility for setting up a measurement. Including a half-wave plate into the TIM setup in order to vary angle between the linear laser beam polarization and the multi-finger gate structure, we found out that (1) the device showed anisotropy for both heterodyne TIM signal amplitude and phase shift, (2) the measured phase shift was 15% of the theoretical in the normal operation mode and (3) it was 50% of the theoretical in the breakdown condition. Such kind of anisotropic TIM response was never detected before due to the larger layout features of the previously studied devices and not lower that laser beam wavelength. Therefore, we introduced a new TIM coefficient and thus expanded [19] for the case of anisotropic reflection and anisotropic phase.

Finally, we carried out a failure analysis for selected device configurations. Failure investigation in DvsS (floating gate condition) and DvsGSB (grounded gate condition) enlightened the variation of the failure location in respect to the stress, showing thermal failure for the first configuration and athermal failure for the second. For all tested TLP conditions and bias configurations, TIM measurements showed that the devices were always homogeneously working. The reason was addressed to the gate coupling effect for floating gate condition and to the finger-to-finger coupling through the substrate in grounded gate configuration. We discovered that the device limitations were due to GOX failure when the device is stress with grounded gate. On the other side, when the device was stressed in floating gate configuration, the failure reason was themal and due to the high current density and reached temperature for high current stress. Failure analysis and leakage failure analysis confirmed these hypothesis.

Chapter 4

Analysis of 16 stacked transistor test structures

In this chapter, we present the combined ESD analysis by TLP, TIM and transient SPICE simulations on a 16 stacked test structure devices (16STTS) similar to stacked devices present in an antenna switch product analyzed in chapter 2. We analyze devices with same layout and electrical parameters but differing only on the distance between two consecutive blocks D_{B2B}.

The transient analysis aims to explain the device complex TLP waveforms by means of TIM and SPICE simulations based on the models developed in chapter 3. The main focus of the investigation will be given on the device with long block-to-block distance D_{B2B}. The investigation of the failure with its root causes is out of the scope of this chapter.

Throughout the chapter, we refer to *block* or *single transistor* as a multi-finger single transistor (similar to the devices analyzed in the chapter 3) as one transistor of the stacked device.

Part of the material used for this chapter was published in [22].

4.1 Device description

The tested devices were stacked transistor test structures composed by 16 blocks connected in series and provided with gate resistors R_G and drain resistor R_D as indicated in figure 4.1(1, 3). A table with most important layout and electrical parameters and their abbreviation is shown in 4.1.

These devices are studied varying one layout parameter, that is the distance between two consecutive blocks D_{B2B}[1], see figure 4.1(2) where the zoomed simplified layout of the i^{th} transistor "Tr.i" and the $(i+1)^{th}$ transistor are indicated. The figure indicates how the D_{B2B} is measured, i.e. from the upper edge of source (S) or drain (D) or gate (G) fingers

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[1] By the abbreviation "B2B" we indicate simply block-to-block.

of $(i+1)^{th}$ transistor to the bottom edge of the closer finger in the i^{th} transistor. From figure 4.1(2), please note also that for this RF technology the silicon trench insulation (STI) has the same height as the n-well for drain and source fingers. Two devices with different D_{B2B} were studied: the D_{B2B} in short D_{B2B} devices is 1.84 μm and for long D_{B2B} devices is 5.68 μm. The backside IR image of the short D_{B2B} device is indicated in figure 4.2a, and for long D_{B2B} device is reported in figure 4.2b.

Figure 4.1(1) shows the stacked layout indicating the transistors numbering from 1 to 16, where 1 stands for the first/top transistor close to drain pad (D) and 16 for the last/bottom transistor close to source pad (S)[2]. Every transistor/block is implemented by 4 multi-finger sub-blocks, each one surrounded by a poly-silicon gate ring and finally connected in parallel all together, see the layout in figure 4.1(3). The high-ohmic poly-silicon R_G resistors are connected to the gate poly-silicon ring and then to the gate pad (G) as in figure 4.1(3). The R_D resistors are connected to the drain metal line to ground as indicated by 4.1(1). Transistor number 1 is not provided without R_D resistor. As for single 150 multi-finger transistor shown in chapter 3.14, the p^+ implant for bulk contact is placed far away from the device active region (i.e. the multi-finger transistors) of at least 200 μm.

Table 4.1: Main layout and electrical parameters for device used for 16 stacked transistor test structures.

Parameter	abbreviation	values
number of blocks	N_B	16
total gate width	W_{TOT}	6.96 mm
multipliers	M	4
gate finger width	W_F	15.2 μm
gate finger length	L_G	0.13 μm
gate oxide thickness	t_{ox}	2.2 nm
gate resistor	R_G	400 $k\Omega$
drain resistor	R_D	400 $k\Omega$
block-to-block distance	D_{B2B}	1.84 μm and 5.68 μm

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[2] The bulk p^+ ring was placed more than 200 μm far from the device.

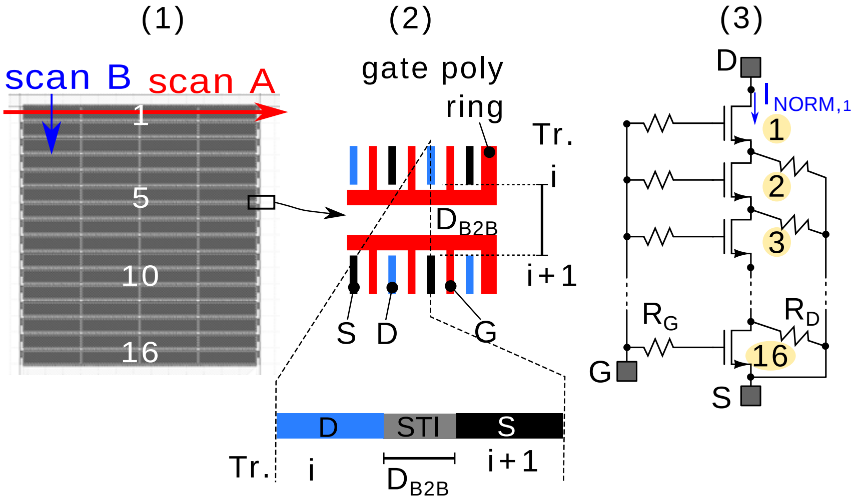
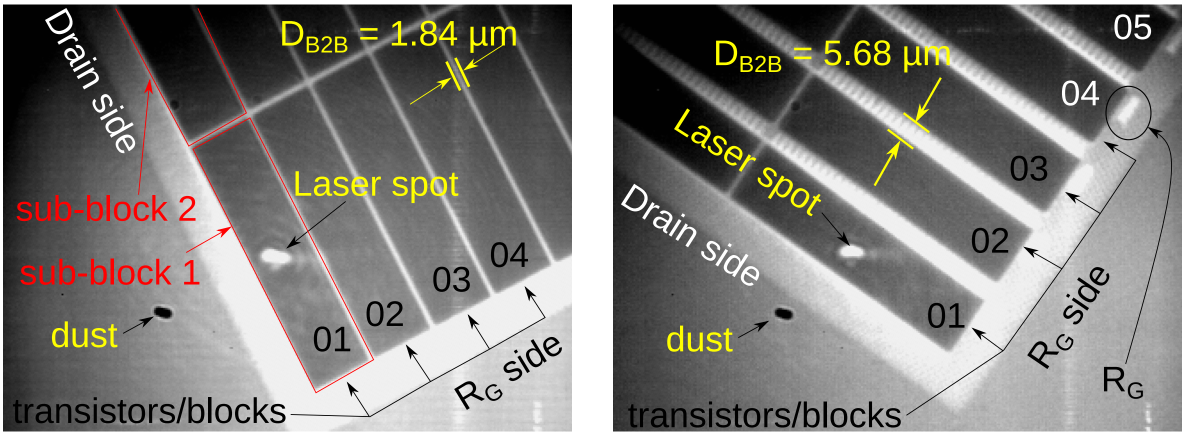


Figure 4.1: (1) Layout of the 16 block device where the TIM scan line A on first transistor (number 1) is indicated. (2) Simplified cropped layout of the region between two consecutive multi-finger blocks; the block-to-block distance (D_{B2B}), gate (G), drain (D), source (S) fingers are indicated. A longitudinal cross- section is also indicated in the bottom part. In the longitudinal cross-section, the silicon trench insulation (STI) region is marked between the drain n-well finger of transistor i and source n-well finger of transistor $i+1$ (for simplicity, metal vias and connections are omitted). Please, note that the height of the STI is the same as the two n-well. (3) Equivalent circuit of a 16 stacked transistor test structure; the reference of the normal current I_{NORM} is given for transistor 1. Taken from [22].



(a) Backside IR image of part of the device with short $D_{B2B} = 1.84\ \mu m$ of 16 stacked transistor test structure (blocks 1-4 are indicated). Note the also the laser spot shining on 1^{st} block in the first sub-block.

(b) Backside IR image of device with long $D_{B2B} = 5.68\ \mu m$ of 16 stacked transistor test structure (blocks 1-5 are indicated). Note the laser spot shining on 1^{st} block in the first sub-block. Only R_G of block 4 can be clearly seen because image was focused mainly to get better resolution on the D_{B2B}.

Figure 4.2: Backside IR images on the devices of 16 stacked transistor test structure available for two different distance block-to-block D_{B2B}.

4.2 PW and D_{B2B} impact by TLP measurements

Both short and long D_{B2B} devices were investigated by fixed 50Ω TLP measurements choosing $RT = 1ns$ and varying the PW in $[100, 450, 650, 840]$ ns range. The devices were tested in the DvsGS and DvsGSB configurations (refer to table 3.4). However, since we did not see any substantial change in terms of TLP-IV and I_{t2}, we will present only results for the configuration DvsGS.

The average I_{t2} results are shown in figure 4.3. We see that the I_{t2} for long D_{B2B} devices is 20% higher than short D_{B2B}. Both devices show $I_{t2} > 10$ A for $PW = 100$ ns resulting in equivalent HBM voltage $V_{HBM} = 1.5k\Omega \cdot I_{t2} > 15$ kV. For $PW \geq 450$ ns instead, it decreases to ≈ 1 A.

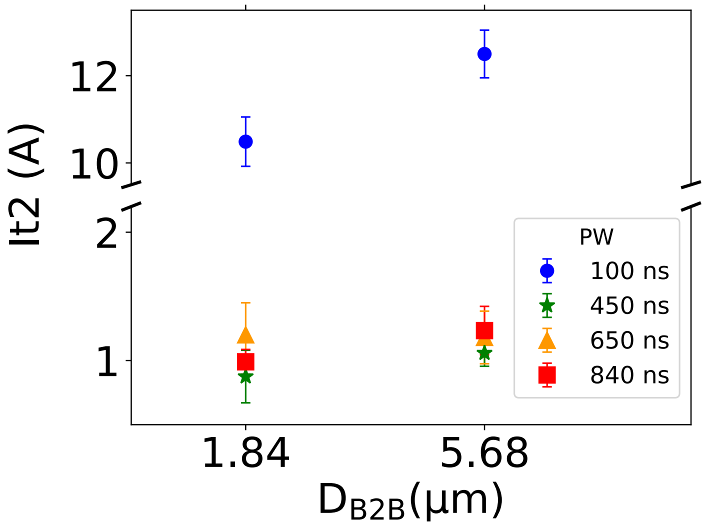


Figure 4.3: Average failure current I_{t2} in the 16 stacked transistor test structure as a function of block-to-block distance (D_{B2B}) for different pulse widths (PW). Notice the vertical scale interruption. Taken from [22].

A TLP measurement comparison for same $PW = 650$ ns is shown in figure 4.4. The device with short D_{B2B} is indicated in red, and the blue color is used for device with long D_{B2B}. In this figure, we show the comparison of (1) the TLP current and in (2) TLP voltage waveforms taken for the same TLP charging voltage $V_{CH} = 30$ V indicated in the TLP-IV in (3). Finally in (4), we report the DC leakage current IV for $V_{DUT} = 1$ V

In most cases, we are used to observe flat-like TLP waveforms for voltage and current. Here, the TLP current and voltage waveforms are non-flat due to the fact that the device changes its impedance during the pulse. We remind that all TLP measurement in this work are all carried out with a 50Ω load line.

In the first part of the TLP waveforms in 4.4(1, 2) i.e. for $t < 200$ ns, the current decreases, the voltage increases and the waveforms of the the two devices are superimposed, this means that the D_{B2B} is not playing a significant role here. For $t \geq 200$ ns, the current is increasing and the voltage is decreasing. Nevertheless, we note here that the current of the device with short D_{B2B} increases faster and reaches higher current value at the pulse end. This also implies that the voltage in the device with short D_{B2B} decreases faster[3].

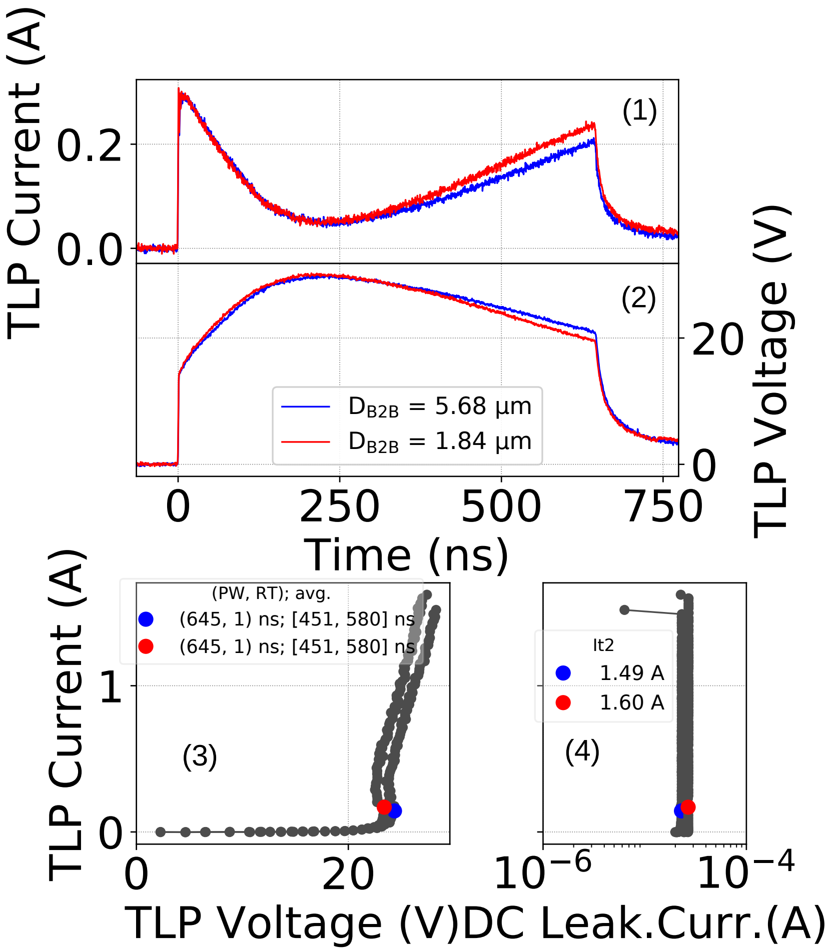


Figure 4.4: Comparison on a device with short ($1.84\mu m$, curves in red) and long ($5.68\mu m$, curves in blue) D_{B2B} of TLP current (1) and TLP voltage (2) for TLP done in DvsGS configuration with $(PW, RT) = (650, 1)$ ns for the same charging voltage 50 V. The location of the waveforms shown in (1, 2) are indicated by colored dots in their respective TLP-IVs in (3) calculated in the time interval $[451, 580]$ ns as indicated in the legend. The red dot is for short D_{B2B}, whereas the blue dot for long D_{B2B}. In (4) the respective DC leakage IVs of the TLP-IVs in (3) are reported. Also in (4), the red dot is for short D_{B2B}, whereas the blue dot for long D_{B2B}. Subfigures (1, 2) are taken from [22].

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[3] We remind once more that all TLP measurements presented in this work were carried out on typical 50 Ω load line, so current and voltage values are related one to the other.

As examples of overall waveform behavior, we selected multiple TLP waveforms depicted in figure 4.5(1, 2) for voltage and current for a device with long D_{B2B}. The location of the waveforms of figures 4.4(1,2) in the TLP-IV is shown in the inset of figrue 4.5(1). The correspondent TLP waveforms for short D_{B2B} are very similar and with the characteristics already shown previously in 4.4(1, 2). Therefore, we decide to not show them.

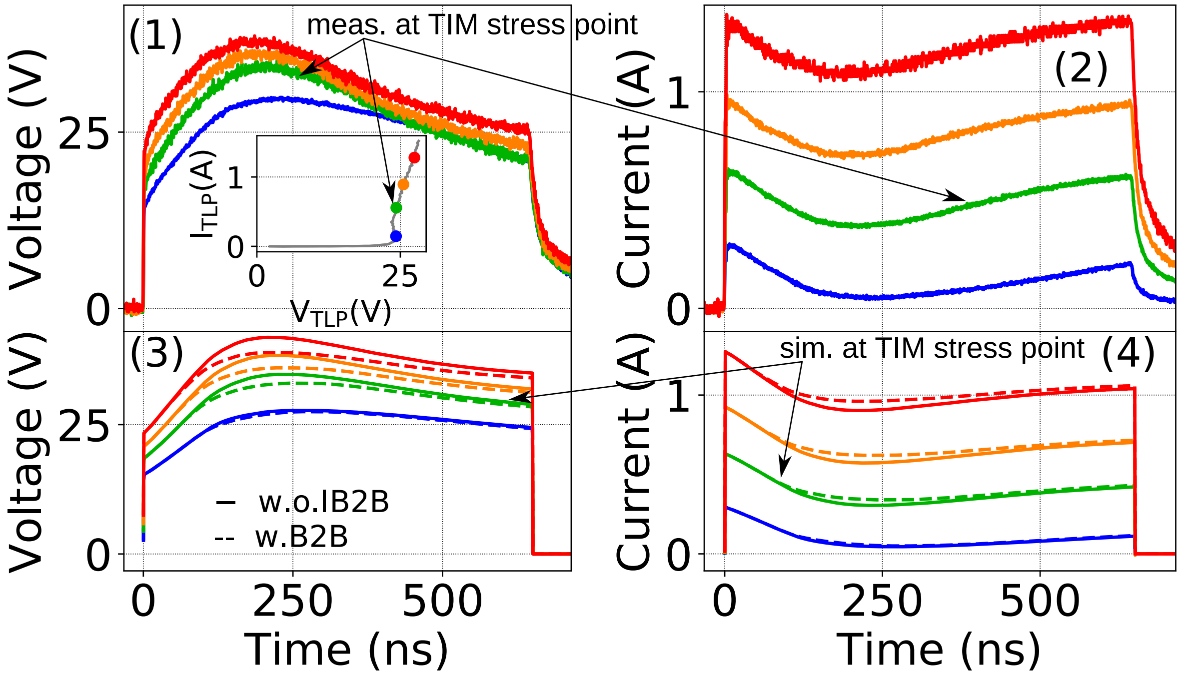


Figure 4.5: Measured (1, 2) and simulated (3, 4) TLP voltage and current waveforms for $PW = 650\ ns$ of the stacked device with long $D_{B2B} = 5.86\ \mu m$ for different increasing charging voltages. The curves marked in green are related to the bias conditions used in TIM experiments in figures 4.7, 4.8 and 4.10a. The TLP-IV curve at 650 ns is shown in the inset of (1). The simulations considering the breakdown source I_{BD} (i.e. without I_{B2B}) are indicated in (3, 4) by solid lines; refer to figure 4.11(1, 2) for the used circuit model that includes the stacked device (figure 4.11(1)) and the I_{BD} current sources (figure 4.11(2)). The dashed curves refer to simulations with additional block-to-block current sources $I_{B2B,(i,i+1)}$ added as indicated in figure 4.11(3) in parallel to stacked device and I_{BD} current sources. The analysis of the transient simulated curves will be provided in section 4.4. Taken from [22].

The waveform variation can be better appreciated showing the TLP-IVs for different averaging time windows, from the pulse begging to the pulse end. See the results in figure 4.6 where solid lines indicate the device with short D_{B2B}, while the dotted lines stand for the long D_{B2B} device. Every curve corresponded to an averaging time interval indicated in the legend. In the first three intervals (black, blue and purple curves), no significant difference between short and long D_{B2B} is encountered. From green interval, we note a sensible lateral shift to lower voltage of the curves with short D_{B2B}.

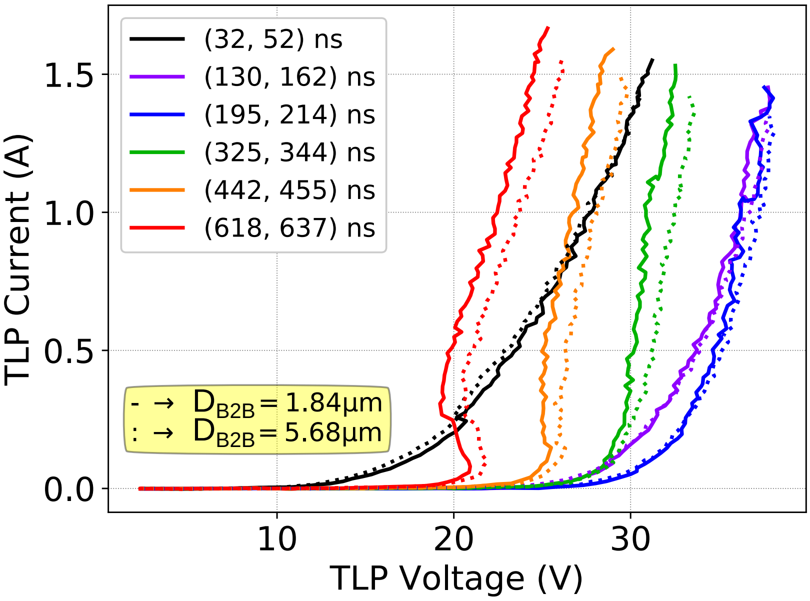


Figure 4.6: Comparison of 50 Ω load-line TLP-IVs calculated for different time interval for devices with short distance block-to-block $D_{B2B} = 1.84\ \mu m$ in solid lines and in dotted lines fro device with long $D_{B2B} = 5.86\ \mu m$. TLP parameters: pulse width $PW = 650\ ns$ and rise time $RT = 1\ ns$. Every color corresponds to a different averaging time interval, for it refer to the legend.

4.3 Analysis of transient behavior by TIM

The peculiarity of TLP waveform shape detected for long PW suggested to have a deeper investigation by TIM to map the power dissipation.

Both devices were probed by TIM for the same charging voltage ($V_{CH} = 50\ V$), $PW = 650\ ns$, $RT = 1\ ns$ and DvsGS device configuration. The TLP waveforms are depicted in figure 4.5(1, 2) by green color assuming the average voltage and current during the pulse to be 27 V and 0.5 A corresponding to $I_{t2}/3$ level.

The phase shift cross-section with one point per block is indicated in figure 4.7 for both devices (red for short D_{B2B} and blue for long D_{B2B}) for two selected time instants at $t = 100\ ns$ (first part of the pulse by dotted points) and at $t = 650\ ns$ (pulse end by triangular points).

The curves at 100 ns were basically flat and at this point we can consider almost superimposed, meaning that the blocks/transistors of both devices were working in similar conditions. If we look back to TLP waveforms presented in figure 4.4(1, 2), the curves at 100 ns are basically superimposed confirming that in this part of the pulse no impact of D_{B2B} is encountered.

On the contrary for $t = 650\ ns$ in figure 4.7, we note that the phase shift is not equally distributed among the blocks, but rather it was concentrated in the first transistors and it decreases going towards last transistor (number 16). This behavior is similar for both configuration, however the short D_{B2B} device shows an overall higher phase shift in respect to the long D_{B2B} in particular in the central blocks.

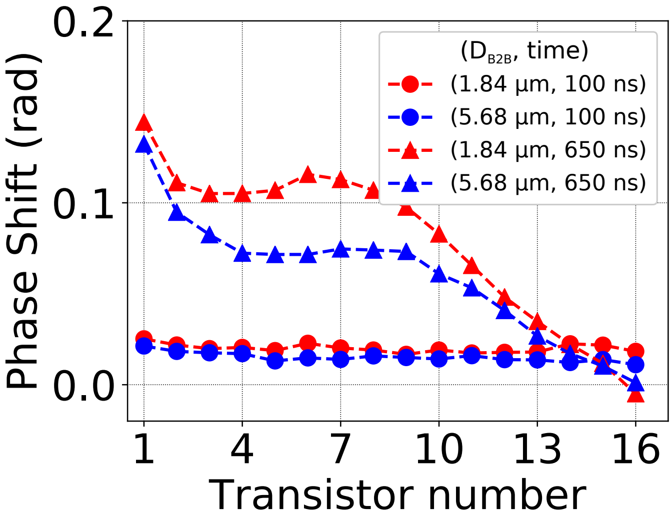


Figure 4.7: Phase shift cross section comparison for three different time instants ($t = 100$ ns and at pulse end for $t = 650$ ns) for both device with long $D_{B2B} =$ 5.68 μm in blue and in red for short $D_{B2B} =$ 1.84 μm device. The TLP stress pulse is indicated in figures 4.5(1, 2). Note the different in the central and first blocks for $t = 650$ ns. Results for $D_{B2B} =$ 5.68 μm are taken from [22].

For the same bias conditions, the devices have been also probed by TIM along the first block as depicted by the red arrow in figure 4.1(1), in order to verify any possible inhomogeneous power dissipation distribution which may occur on the transistor with higher phase shift. The results are illustrated in figure 4.8 for three different time instants (see them indicated in the legend) for a device with long D_{B2B}. The heterodyne amplitude signal corresponding to the same scan displayed in figure 4.8 is reported in figure 4.9, where the points of abrupt change in the heteredyne amplitude and local low amplitude region are indicated. We noted from phase shift cross-section figure 4.8, that in the region close to the edge of each sub-block (note them indicated in bottom part of the figure 4.8) the phase shift is slightly lower than in the center. The blue curve at $t = 100$ ns showed two possible peaks at the edges (one for position 30 μm in the left side and one for 270 μm on the right side of the figure) which they seem to disappear for the other two selected curves at longer time instants. As long as the time increase, a rather more homogeneous power distribution throughout the four sub-blocks can be seen despite the intrinsic presence of noise. Comparing figure 4.8 with figure 4.9, we see that in correspondence of the heterodyne amplitude discontinity points (i.e. t positions 55 μm, 130 μm, 170 μm and 245 μm) a discontinuity phase shift is observable. These should be addressed to optical artifacts. In figure 4.9 a region of local low heterodyne amplitude in the position interval

$(255, 270)$ μm is observable and at this position a possible phase shift peak is detected in figure 4.8. We address the phase shift peak to optical artifact. We can conclude that the overall behavior can be defined rather homogeneous with possible weak inhomogeneity points. Similar TIM scans were done also on second transistor and reported again no sign of strong inhomogeneous power distribution (the result is not shown for shortness). Same conclusions can be done from the short D_{B2B} device TIM scans on its first and second block transistor.

In light of the evidence of what just written, we could state that all fingers belonging to the same block work at the same current density condition because no evident inhomogeneous power distribution inside the same block was found at the probed stress level.

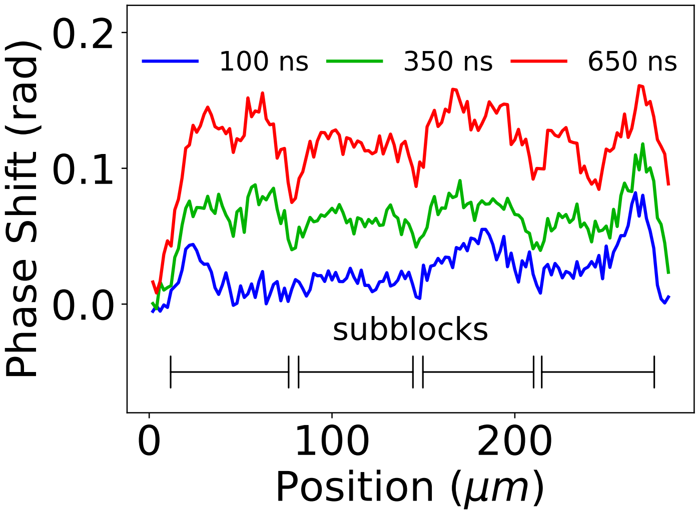


Figure 4.8: Phase shift cross section for three different time instants during the pulse at $t = 100$ ns and $t = 350$ ns and then at the pulse end at $t = 650$ ns for device with long $D_{B2B} = 5.68$ μm. The scan path is indicated in figure 4.1(1) by "scan A" by red arrow. The TLP stress pulse is indicated in figures 4.5(1, 2). Note the lower phase shift located at the edges of each sub-block, sub-blocks location is indicated in the region below. Taken from [22].

The last TIM measurement that we present, it is an accurate TIM scan on the long D_{B2B} device from the region outside the first block to the end of the third as indicated by blue arrow and "scan B" in figure 4.1. The results are depicted in figure 4.10a for selected time instants as indicated in the legend, whereas in figure 4.10b, the corresponding heterodyne amplitude cross-section is reported. The electrical stress is the same as in previous TIM scans in figures 4.7 and 4.8. The peaks visible in figure 4.10a at $X = 9$ μm and $X = 46$ μm are due to optical artifacts (see also figure 4.10b), because the first is located between the multi-finger region and all metal vias until the pad and therefore edge effects occur due to the low heterodyne amplitude. The second peak is due to a low signal-to-noise ratio because it is at the edge of the block.

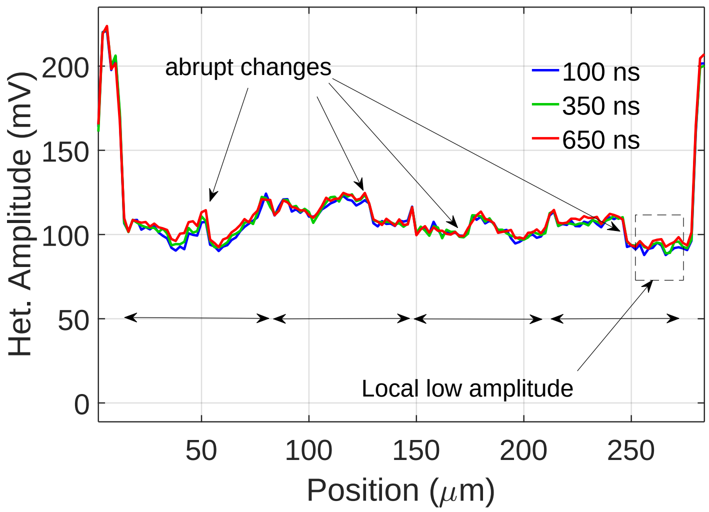
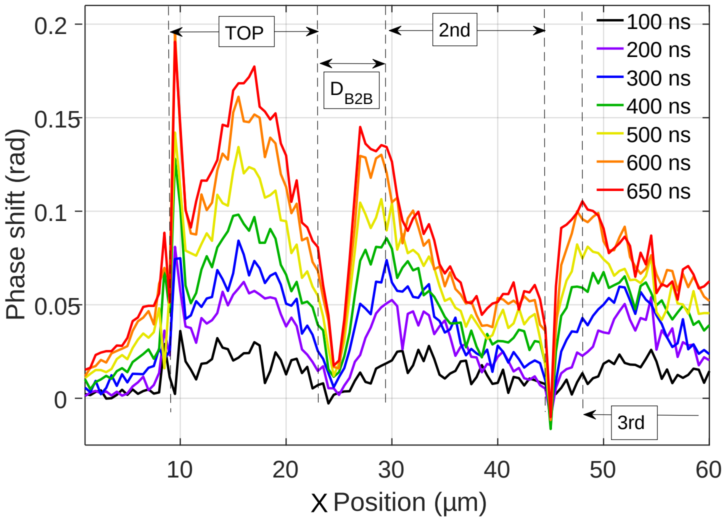


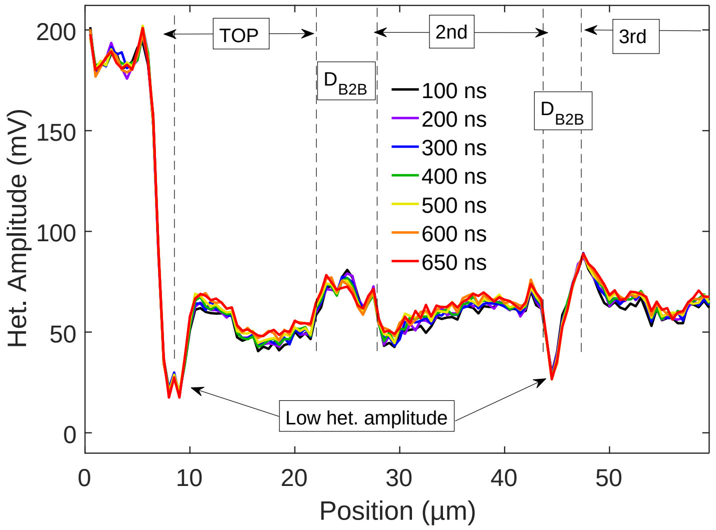
Figure 4.9: Heterodyne amplitude cross-section belonging to the TIM scan on device with long $D_{B2B} = 5.86\ \mu m$ shown in figure 4.8 for the same time instants (i.e. $t = 100\ ns, 350\ nsand\ 650ns$). The heterodyne points with abrupt changes are indicated by arrows at positions 55 μm, 130 μm, 170 μm and 245 μm. Then, the region with local low heterodyne amplitude is also marked. This region corresponds to the region where a possible local peak is detected in figure 4.8.

We noted that in the top/1^{st} transistor the power dissipation was concentrated in the center (at $X = 15\ \mu m$) but this behavior did not occur for second and third block where we saw that the power was dissipated towards the "upper" block, i.e. towards the top for second block and towards the second block for the third block meaning that power was mostly dissipated there. This fact suggested that a possible interaction among the blocks through the substrate should not be excluded even for devices with long D_{B2B}. Looking at the region between top and second block (i.e. where is marked D_{B2B} in figure 4.1(2)), we noted that the phase shift was positive and it appeared since the first time shown ($t = 100\ ns$) meaning that there is a thermal activity also in this region. However, we should be very careful on the quantitative interpretation in such location, since we do not know what is the TIM response in such region with metal lines and vias which could degrade the heterodyne signal and the resulting phase shift (see backside IR image in figure 4.2b).

Summarizing, TIM measurements showed that blocks present increasing high power dissipation towards the first blocks where stress was applied and it was overall higher in device with short D_{B2B}, no strong inhomogeneous power dissipation inside the block was detected and then high positive phase shift in the region in between the blocks for the device with high D_{B2B}.



(a) Phase shift cross section for multiple time instants relative to scan path indicated by "scan B" in figure 4.1(1) by blue arrow. The TLP stress pulse is indicated in figures 4.5(1, 2). Phase shift for positions $X = 11\ \mu m$ and $X = 46\ \mu m$ is due to optical artifacts due to low heterodyne amplitude signal.



(b) Heterodyne amplitude cross-section of the scan for multiple time instants. Please note the regions of low heterodyne amplitude at 9 μm and 45 μm resulting into optical artifacts in the phase shift cross section in the figure above in (a).

Figure 4.10: TIM measurement on long D_{B2B} device along the finger width regarding the 1^{st}/TOP block the D_{B2B} regions and the 2^{nd} block.

4.4 Analysis of transient behavior by SPICE simulations at TIM stress conditions

TIM is a unique technique in the world to map the transient power dissipation distribution and the free carrier distribution in the ESD domain. However, for a complete transient analysis of stacked transistors, TIM was not sufficient to give us information about the status of each transistor[4], i.e. the transient working point (V_{GS}, V_{DS}). To overcome this lack, we chose to use SPICE transient simulations as already presented in section 1.4.2. Thanks to this tool, we had insight on the V_{GS}, a fundamental parameter to explain the TLP waveforms and TIM phase shift distribution in figure 4.7.

This tool is becoming popular in ESD community and in particular for system-level ESD simulations as in [100–102].

The novelty of this work was to use SPICE transient simulations for ESD at circuit level in combination with TIM results. We did not find any publications on accurate transient analysis of the stacked MOSFETs under ESD stress conditions.

The current references are indicated in figure 4.11. I_{NORM1} stands for the normal MOSFET current of the first transistor, $I_{BD,1}$ is the breakdown current. With I_{DUT} and V_{DUT}, we mean the overall current and voltage on the device under test.

We will focus the simulations of the following sections on the device with long D_{B2B} showing firstly the set of simulations with breakdown model (circuit in figure 4.11(1, 2)) and then introducing B2B current sources (i.e. using the whole circuit in figure 4.11(1, 2, 3)).

4.4.1 Simulation with breakdown model

The simulated TLP current and voltage waveforms of figure 4.5(1, 2) for increased V_{CH} are reported in figure 4.5(3, 4) by solid lines (marked with “w.o. B2B” standing for “without B2B model)”. We remind that green curves in figures 4.5(3, 4) refer to the electrical condition for TIM measurements on long D_{B2B} depicted in figures 4.7, 4.8, 4.10a. At a first sight, we already see that the main current and voltage features were well reproduced.

The $V_{GS,i}$ and $V_{DS,i}$ transient waveform corresponding to the solid green curves in 4.5(3, 4) for the TIM results are depicted in figure 4.12(a, b). Each transistor is indicated by a different color from transistor 1 in red, to transistor 16 in dark blue. The normal $I_{NORM,i}$, the breakdown $I_{BD,i}$ and the gate $I_{G,i}$ currents are reported in figure 4.13.

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[4] At the writing time of this work, no test structures provided with pads to probe the V_{GS} voltage of each transistor were available.

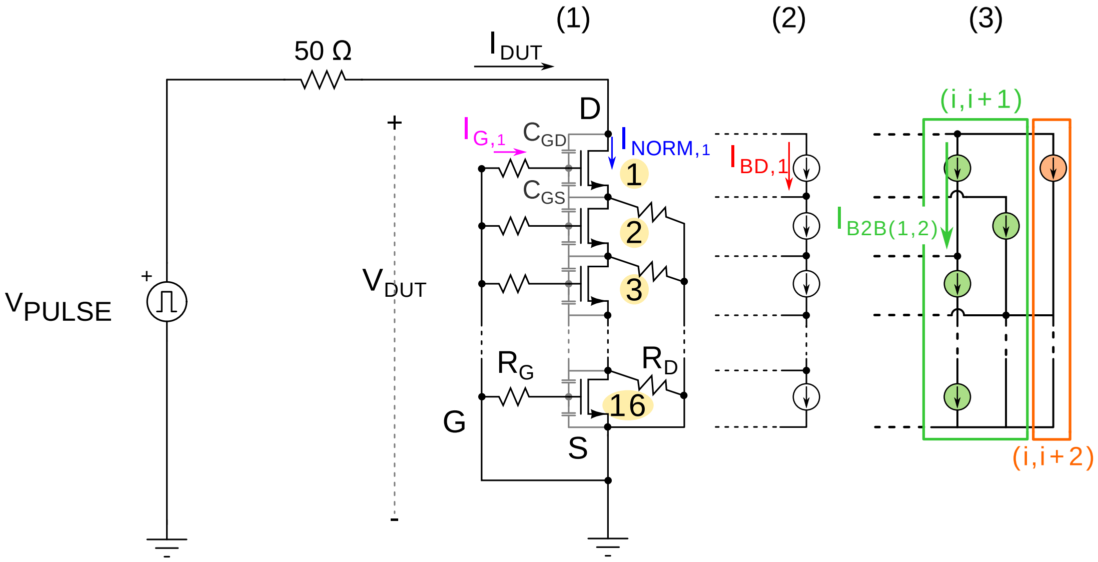


Figure 4.11: (1) the TLP pulser is simulated by a trapezoidal voltage pulse of amplitude V_{PULSE} in series to a 50Ω resistor and the device. The orientation of currents are shown in transistor 1: $I_{G,1}$ for gate current, $I_{NORM,1}$ for the normal current. The total current flowing into the resistor to the device under test (DUT) is indicated by I_{DUT} and the total voltage on the device is indicated by V_{DUT}. (2) Additional breakdown current sources at individual transistors, and (3) parasitic next neighbor coupling (i, i+1) current sources and further coupling among (i, i+2) transistors. Taken from [22].

Rise time interval In the rise time interval and thanks to the dV/dt effect of the rise trapezoidal voltage edge, the gate capacitors C_{GD} and C_{GS} are charged by the gate coupling effect and the presence of R_G resistors enabled the device current to flow when all transistors reached $V_{GS,i} \geq V_{TH}$ working in saturation regime. At the end of the rise time, $V_{GS,i}$ were very similar (see 4.12). In this simulation in particular, $V_{GS,i} = 0.6\ V$ in the simulated TIM conditions. The overall current corresponded to each $I_{NORM,i}$, i.e. $I_{DUT} = I_{NORM,1} = I_{NORM,2} = ... = I_{NORM,16}$.

Gate discharge As the rise of the charging voltage is over, no more gate coupling effect is possible and therefore no more $V_{GS,i}$ increase is possible. This fact brought the MOSFETs gates to start the discharge to ground through their own $R_{G,i}$, see also the negative I_G, i in figure 4.13(1). As the $V_{GS,i}$ currents decreased, the $I_{NORM,i}$ currents decreased and also I_{DUT}. This is in accordance with the measured current for $t < 150\ ns$, figure 4.4(3). On the contrary, the $V_{DS,i}$ voltages increased due to the presence of the constant V_{CH} of the simulated pulser, see figure 4.12(2).

Breakdown current activation The simultaneous $V_{DS,i}$ increased and the $V_{GS,i}$ decrease led to reach the V_{BD} condition from equation 3.2 and the I_{BD} starts to flow. For $t > 150\ ns$, we saw that the I_{DUT} increased because of the progressive activation of the

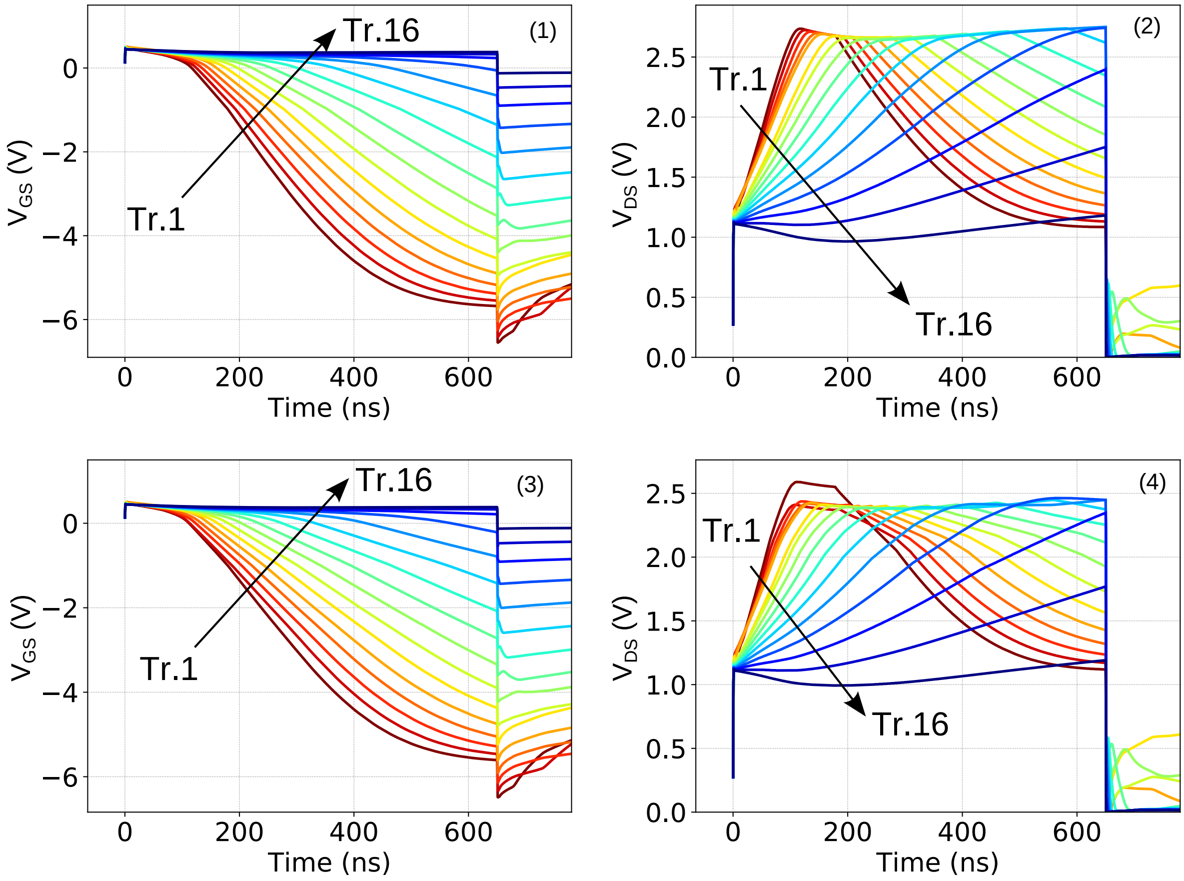
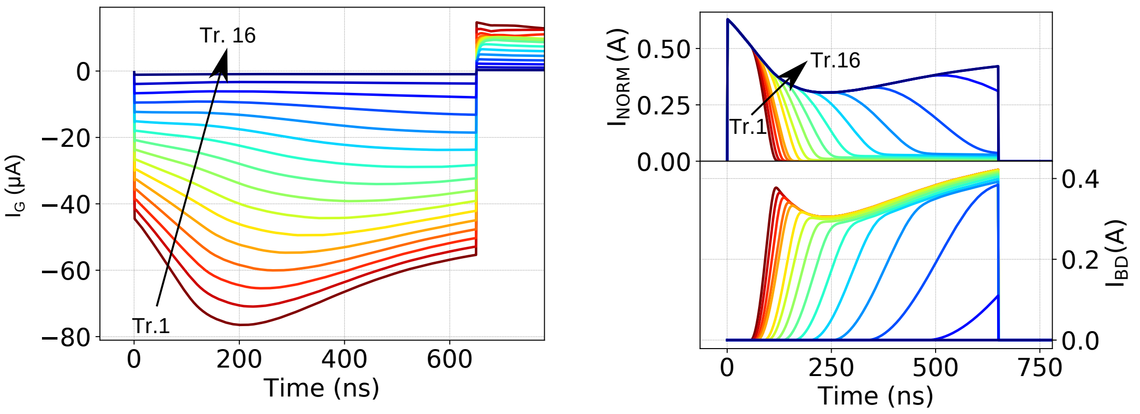


Figure 4.12: Simulated transients of $V_{GS,i}$ (1,3) and $V_{DS,i}$ (2, 4) at transistors 1-16 for the model with the breakdown sources $I_{BD,i}$ (1,2) and for the model with additional block-to-block current sources $I_{B2B,(i,i+1)}$ (3, 4). The bias condition ($V_{PULSE} = 50\ V$) is the same as for the green lines in figure 4.5 (i.e. TIM measurement condition). Taken from [22].

breakdown current source. This is again in accordance with the measured TLP current waveform in 4.5(3). The first device to reach this condition is the first transistor, see the waveforms in figure 4.14(a-c). The $I_{BD,1}$ started to rise at $t = t_1$ since $V_{DS,1} = 2\ V$. Once, the $V_{GS} < V_{TH}$, the $I_{NORM} = 0$ and the current was only due to I_{BD} contribution.

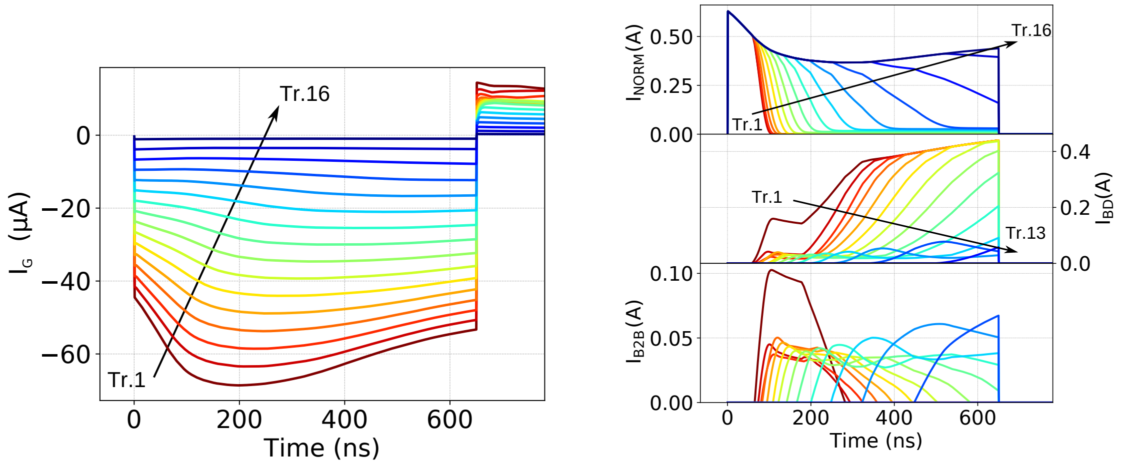
The strong dependence of V_{BD} from V_{GS} and the continuation of V_{GS} decrease bring to the $V_{DS,i}$ decrease when $V_{GS,i} < 0$. In transistor 1 (see the figures in 4.14(a, b, c)), this is shown in the interval $t_1 < t < t_3$, where we have a decrease of $I_{NORM,1}$ and an simultaneous increase of $I_{BD,1}$.

However, we noted the presence of a plateau occurring in the V_{GS} interval for $-1\ V < V_{GS} < 0\ V$. The reason of this plateau is addressed to the implementation of the I_{BD}, since in this interval the V_{BD} is set constant (see figure 3.13(b)). Again, we can appreciate this behavior in the waveforms of the transistor 1 in figure 4.14 in the time interval $t_3 < t < t_4$, where t_3 is the time instant at which $V_{GS} = 0$ and $I_{NORM,1} = 0$ and then t_4 is the time instant when $V_{GS} = -1\ V$. For $t \geq t_4$ the whole current on the first transistor is given



(a) Simulated I_G transient waveform without block-to-block current sources included.

(b) Simulated I_{NORM} (on top plot) and I_{BD} (on the bottom plot) without block-to-block current sources included.



(c) Simulated I_G transient waveform with block-to-block current sources enabled.

(d) Simulated I_{NORM} (in the top plot), I_{BD} (plot in the middle) and I_{B2B} (in the bottom plot) currents including the B2B current sources.

Figure 4.13: Simulated waveforms for long D_{B2B} stacked device at TIM measurement conditions (green current and voltage curves in figures 4.5) shown in figures 4.7, 4.8 and 4.10a. In (a, b) the results are obtained with breakdown current sources but without B2B current sources, whereas in (c, d) both breakdown and B2B current sources were included as indicated in figure 4.11.

only by I_{BD}. Besides these facts, we saw that transistor 14-16 did not reach any breakdown condition because $V_{GS} \geq V_{TH}$ and $V_{DS} \leq V_{BD}$ during the whole pulse. This explains why we found low phase shift on the last blocks in figure 4.7.

Simulated vs. measured phase shift Finally, we discuss the normalized simulated phase shift for $t = 650$ ns from figure 4.15 (blue squared line) using equation 3.4 with the

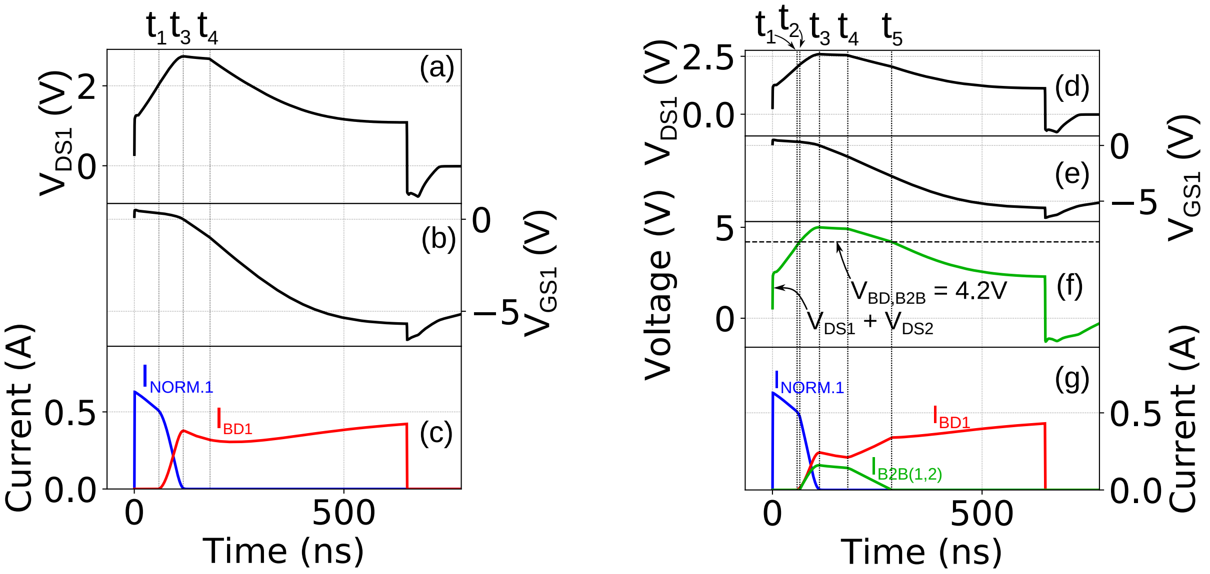


Figure 4.14: Simulated current contributions (I_{NORM1} , I_{BD1} , $I_{B2B(1,2)}$) and voltage transients (V_{DS1} , V_{GS1} , $V_{DS1} + V_{DS2}$) in transistor 1 for the model with breakdown sources $I_{BD,i}$ (a-c) and for the model with additional block-to-block current sources $I_{B2B(i,i+1)}$ (d-g), parameter $K = 0.2\ A/V$. The bias condition ($V_{PULSE} = 50\ V$) is the same as for the green lines in figure 4.5 (i.e. TIM measurement condition). Taken from [22].

measured phase shift in figure 4.7. The simulated phase shift is obtained using $I_{BREAK,i} = I_{BD,i}$ in equation 3.6.

We saw that the normalized phase shift cross section well reproduces the low phase shift on bottom blocks (14-16) and that high phase shift was encountered not in the 1^{st} transistor but rather in the 12^{th}. Therefore, we assumed that the simulated circuit given by the MOSFETs and breakdown current sources (circuit given by figure 4.11(1, 2)) is not taking into account the phenomena involved to reproduce the phase shift distribution. Additional components aiming to consider other phenomena must be included in the circuit. For instance, in the circuit used before there is no components simulating additional parasitic current sources between blocks.

4.4.2 Simulation with additional B2B current sources

From TLP waveforms comparison for short versus long D_{B2B} in figures 4.4 and 4.6, we noted similar behavior but with small differences in current rising slope at $t > 200\ ns$. Then, also TIM phase shift at the pulse end (dashed triangle curves) as shown in figure 4.7 reported similar shape, but clearly higher phase shift in devices for short D_{B2B}. Hence, both TLP and TIM showed some slight but clear differences between short and long D_{B2B} devices. This suggested that B2B coupling through the substrate should not be excluded. Therefore, another breakdown path or parasitic BJT action was included between the blocks of a stacked device.

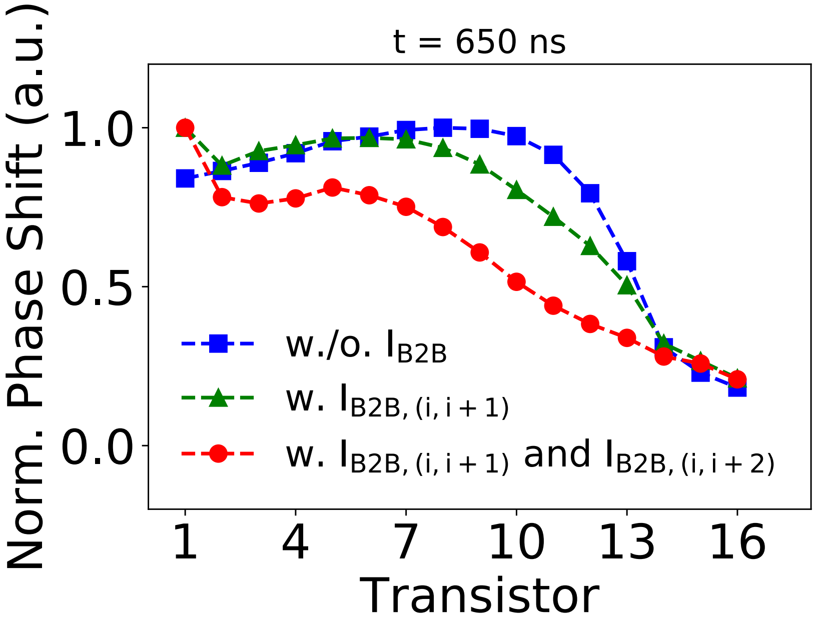


Figure 4.15: Normalized simulated phase shift distribution for comparison along the blocks for the same bias conditions as in 4.7: squares for the model with breakdown sources $I_{BD,i}$, triangles for the model with additional block-to-block current sources $I_{B2B(i,i+1)}$ and dots for the model with additional block-to-block sources $I_{B2B(i,i+2)}$. The phase shift normalization was done dividing the simulated phase shift by the maximum value of each curve. Taken from [22].

From the simplified layout of two consecutive transistors i^{th} and $(i+1)^{th}$ drawn in figure 4.1(2), such parasitic path could exist between every top side of the source finger of the $(i+1)^{th}$ transistor (this would be the collector of the PBJT) and the bottom side of the drain finger of the i^{th} transistor (this would be the emitter of the PBJT). In this region, the total voltage is given by the sum $V_{DS,i} + V_{DS,i+1}$.

Also two results in chapter 3 were interpreted in this way. From the first, i.e. L_G variation experiment displayed in figure 3.11, we saw the snapback parasitic BJT behaviors appearing also for devices with $L_G \leq 10\ \mu m$, i.e. for devices showing $L_G \geq D_{B2B}$. The second was the finger-to-finger coupling, showed in figures 3.8.

The B2B phenomenon was modeled using a voltage controlled current source, sensing the voltage between two (or more) consecutive transistors and supplying a linear current rise with bias overcoming a certain threshold voltage called $V_{BD,B2B(i,j)}$ where i and j stand for the transistor index in the stacked configuration. Examples for $(i, i+1)$ and $(i, i+2)$ are shown in the circuit schematic in figure 4.11(3).

A B2B current source between transistor i and $i+1$ indicated as $I_{B2B(i,i+1)}$ was implemented by the piecewise linear function [22]:

$$I_{B2B,(i,i+1)} = \begin{cases} 0, & \text{if } V_{DS,i} + V_{DS,i+1} < V_{BD,B2B(i,i+1)} \\ K \cdot (V_{DS,i} + V_{DS,i+1} - V_{BD,B2B(i,i+1)}), & \text{if } V_{DS,i} + V_{DS,i+1} \geq V_{BD,B2B(i,i+1)} \end{cases} \tag{4.1}$$

where K is the slope and $i = 1, 2, ..., 16$. Due to a lack of proper test structures available at the time of the writing of this work, the parameter K and $V_{BD,B2B}$ were considered fitting parameters. However, $V_{BD,B2B}$ was taken to be like $V_{BD,B2B} \geq 2 \cdot V_{BD,DS}(V_{GS} = 0)$. For modeling the (i, i+1) B2B effect, we took $V_{DB,B2B(i,i+1)} = 4.2\ V$ and $K = 0.2A/V^2$.

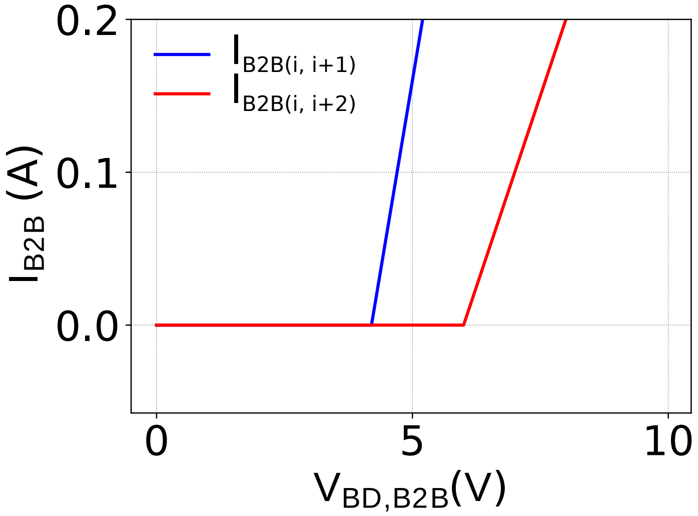


Figure 4.16: Block-to-block current sources $I_{B2B(i,i+1)}$ in function of block-to-block breakdown voltage $V_{BD,B2B}$.

Again and as it was done in the previous section 4.4.1, we simulated the set of $I(t)$ and $V(t)$ curves of figure 4.5(a, b) obtaining the results with dashed lines in figure 4.5(3, 4). The results showed that the impact of additional B2B current sources on the overall waveforms increased the current and decreased the voltage in the second half of the pulse, without affecting the first half. These lasts facts were in agreement with figure 4.4.

The new simulated $V_{DS,i}(t)$ and $V_{GS,i}(t)$ for the TIM bias conditions were reported in figure 4.12(3, 4), respectively; the $I_{G,i}(t)$ currents are shown in 4.13(c) and the other currents $I_{NORM,i}(t)$, $I_{BD,i}(t)$ and $I_{B2B,(i,i+1)}$ in figure 4.13. The most important waveforms on 1^{st} transistor are displayed in figure 4.14(d-g).

The $V_{GS,i}$, $I_{NORM,i}$ and $I_{G,i}$ were not strongly affected by the B2B current sources. However, we noted that $V_{GS,i}$ decreases slightly faster. + On the other side, the $V_{DS,i}$ and $I_{BD,i}$ presented changes just after the activation of the $I_{BD,i}$.

If we observe what is happening in the first transistor (figure 4.14(d-g)), we see that the $I_{B2B(1,2)}$ is flowing in the interval $t_2 < t < t_5$ when $V_{DS,1} + V_{DS,2} > V_{DB,B2B} = 4.2\ V$ i.e. only in the central part of the pulse and it slows the $V_{DS,1}$ decrease.

Simulated phase shift including B2B current sources The $I_{B2B(i,i+1)}$ contributions have been added to $I_{BREAK,i}$ in equation 3.6 taking $I_{BREAK,i} = I_{BD,i} + \sum I_{B2B,(i,i+1)}$ with $\sum I_{B2B,(i,i+1)}$ indicating the summation over nearest neighbors of the i^{th} transistor[5].

The normalized phase shift results adding $I_{B2B(1,2)}$ are indicated by green triangular symbols in figure 4.15 for $t = 650\ ns$. We see now that the simulated phase shift distribution matches better the measured of figure 4.7, because the 1^{st} transistor shows the highest phase shift. Its phase shift peak is due to the fastest decrease of $V_{GS,1}$ in presence of I_{B2B}.

TIM results of figure 4.7 can be now qualitatively explained by the presence of $I_{B2B,(i,i+1)}$ current sources.

A further addition of the second nearest current sources $I_{B2B(i,i+2)}$ (see in circuit of 4.11(3)) led to the results shown in figure 4.15 by dotted red lines (in the legend I_{MB2B} stands for multiple B2B current sources). We noted that the obtained normalized simulated phase shift is very similar to the measured phase shift: the phase shift decreases for first three transistors and then there is a plateau until transistor 7. From the simulated waveform side, the addition of $I_{B2B(i,i+2)}$ components did not lead to any further improvement (results not shown).

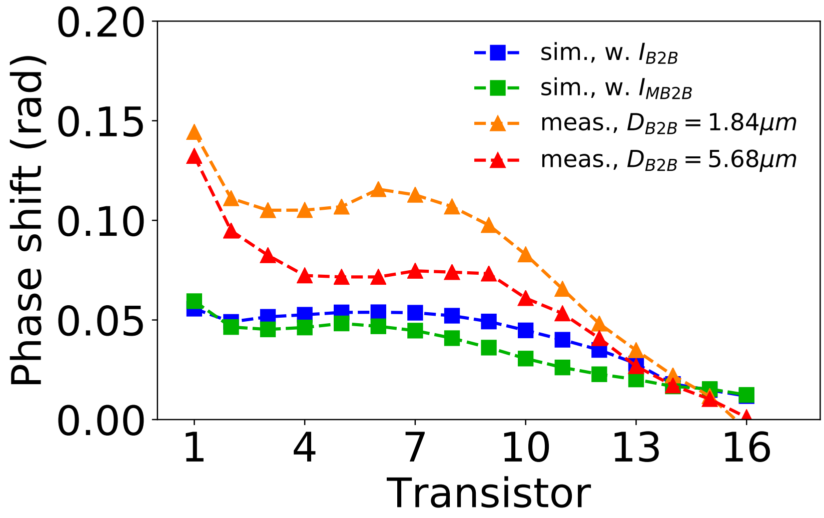


Figure 4.17: Simulated (squared) versus measured (triangle) phase shift cross-sections at the pulse end ($t = 650\ ns$).

The simulated phase shift for long D_{B2B} was also compared quantitatively with the measured. The results is shown in figure 4.17 where measured phase shift for long $D_{B2B} = 5.86\ \mu m$ is indicated by red triangles and for short $D_{B2B} = 1.84\ \mu m$ by orange triangles. The simulated phase shift cross-sections are indicated by blue squares for I_{B2B} and in green squares for I_{MB2B}. We see that the simulated phase shift is more similar to long

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[5] As example for transistor 1 we take $I_{BREAK,i} = I_{BD,i} + I_{B2B,(1,2)}(+I_{B2B,(1,3)} + ...)$.

D_{B2B} condition in particular in the central and bottom blocks.

We attributed this discrepancy to model simplifications, e.g. the use of a stepwise function to model the B2B effect, the neglect of the self-heating effect, the fact that the breakdown model presented in section 3.6.1 is not dependent on the B2B effect and fixed TIM coefficients were extracted for only two gate conditions for one current level.

The definition of proper test structures with D_{B2B} variation would lead to a more accurate B2B model. These test structures could also provide additional information, such as a possible dependence of the drain-source breakdown to the B2B effect. The drain breakdown was also developed under a condition of bulk pad grounded: this condition might not be satisfied during real device operation and could impact shifting V_{BD}.

Besides the test structure definition and their measurements, a TCAD analysis on these breakdown phenomena would be necessary to better understand the complexity of these phenomena.

4.5 Conclusions

A combined study using TIM and SPICE simulations explained the particular TLP transient waveforms occurring in the 16 stacked test structures. These devices were provided with two different D_{B2B} layout parameters.

TLP analysis showed that the transistors belonging to the stacked test structures were not operating at the same bias during a TLP pulse because we measured non-flat time dependent waveforms. At the beginning of the pulse, both short and long 16STTS devices showed the same voltage and current waveforms, whereas in the second half of the pulse (for $t \geq 150\ ns$), a current increase was found more pronounced in devices with short D_{B2B} which also showed 20% less I_{t2}.

The TIM measurements showed that the D_{B2B} impacted also on the power dissipation, showing higher values in the device with short D_{B2B} for the same TLP stress charging voltage used to probe devices with long D_{B2B}. The power dissipation was not constant among the blocks from the second half of the pulse, it was indeed increasing towards the first transistors (highest phase shift on 1^{st} transistor) and very low in the last transistors.

From SPICE transient simulations, we saw that after the gate-coupling effect during the RT, the $V_{GS,i}$ progressively decreased because of the presence of the R_G, resulting in the I_{DUT} decrease (and V_{DUT} increase). The uninterrupted and sequential $V_{GS,i}$ decrease led to the breakdown condition starting from the 1^{st} transistor close to the drain pad. Other transistors followed in sequence and this explained why the current was again increasing in the second part of the pulse, i.e. for $t > 150\ ns$. The inclusion of the breakdown model developed in section 3.6.1 was sufficient to explain the main TLP waveforms. However, it was not enough to reproduce the power dissipation measured by TIM. We found out that introducing B2B sources reshaped the simulated phase shift reaching a good agreement with measured phase shift for devices with long D_{B2B}. The coupling through the substrate, the L_G dependence of the breakdown, TLP waveforms and TIM results on stacked transistors and the I_{t2} dependence on the D_{B2B} for 16STTS were the basis to justify the inclusion of additional B2B current sources.

Chapter 5

Analysis of 6 stacked transistor test structures

In this chapter, we continue the analysis of stacked test structures for antenna switch devices on a new device with different layout parameters from the previous 16STTS devices analyzed in chapter 4. Since these new devices are formed by 6 stacked transistors, they will be named as 6 stacked transistor test structures (6STTS). The layout parameters of 6STTS are very similar to shunt transistor device presented in the antenna front-end product in chapter 2. This fact is the reason why the 6STTS device is widely investigated.

The results are presented in the following way: firstly, the TLP-IVs are studied for two different gate conditions (floating gate versus grounded gate) for the same TLP parameters; then, the power dissipation by TIM and the pulsed emission microscopy (EMMI) are compared for both configurations. At the end, an experiment to reproduce the inhomogenous EMMI in grounded-gate conditions is proposed.

5.1 Device description

The 6STTS devices were similar to 16STTS devices in terms of circuit configuration, resistors positions and they belonged to the same wafers done in the same technology. However, 6STTS differ in terms of certain layout parameters from 16STTS as shown in table 5.1.

Compared to values of 16STTS, the 6STTS devices show:

- reduced W_{TOT},
- reduced W_F,
- reduced N_B,
- only one available $D_{B2B} = 2.1\ \mu m$ (similar to short $D_{B2B} = 1.84\ \mu m$ device of 16STTS).

Table 5.1: Main layout and electrical parameters for 6STTS.

Parameter	abbreviation	values
number of blocks	N_B	6
total gate width	W_{TOT}	0.98 mm
multipliers	M	1
gate finger width	W_F	12.5μ m
gate finger length	L_G	0.13 μm
gate oxide thickness	t_{ox}	2.2 nm
gate resistor	R_G	400 $k\Omega$
drain resistor	R_D	400 $k\Omega$
block-to-block distance	B_{D2B}	2.1 μm

The STI height of this device is as high as the n-well fingers of drain or source fingers, as for 16STTS and represented in 4.1(2).

An IR image of 6STTS from the chip backside is shown in figure 5.1. The transistors are numbered from 01 to 06 in their multi-finger region (the limits of the multi-finger region are highlighted for the 3^{rd} transistor). In this picture, drain side ("drain"), source side ("source"), resistors R_G for 1^{st} transistor and R_D for 2^{nd} transistor are indicated. The R_G resistors are located in the left side of the figure (for this reason, we indicate it as "R_G side"), R_D resistors are placed in the right side.

The investigation presented in the following is limited to the TLP parameters $(PW, RT) = (100, 1)$ ns. However, we will compare the results in two different configurations: DvsGS and DvsS (refer to table 3.4). As for previously studied devices, the bulk pad condition was irrelevant in terms of TLP-IVs. For this reason, TIM results were carried out in floating bulk to reduce the measurement setup complexity.

5.2 TLP measurements for $PW = 100$ ns

The TLP-IVs calculated in the time interval $[70, 90]$ ns were compared in figure 5.2. We noted that for these devices, the gate status brings different TLP-IV shape and failure current. Indeed for DvsS configuration, we saw voltage reduction and higher I_{t2} ($I_{t2} = 1.5$ A for DvsS versus $I_{t2} = 1.2$ A for DvsGS).

The TLP-IVs calculated for different time intervals are reported in figure 5.3a for DvsGS and in figure 5.3b for DvsS. We immediately noted that only configuration DvsS in figure 5.3b shows a smooth TLP-IV throughout the pulse. In DvsGS, we had a smooth behavior at the pulse beginning (blue curve at $[20, 30]$ ns interval) and then the TLP-IV reduced the voltage and steeply increased similarly to what seen in 16STTS devices in figure 4.6 (or to a piecewise linear function).

The most significant TLP waveforms of the two configurations for different current

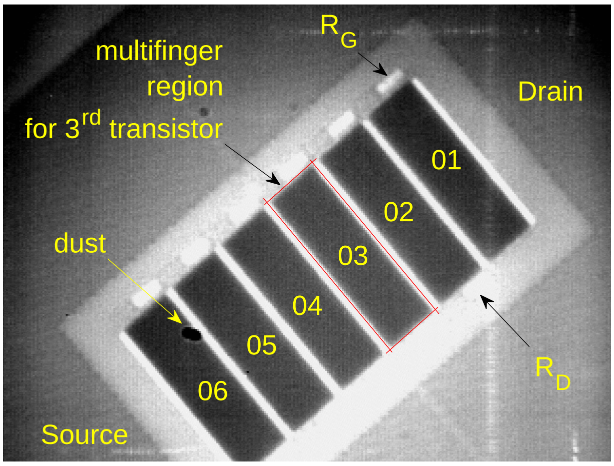


Figure 5.1: Infrared IR image recorded by focal plane array camera of 6STTS device from the back side. Note the location of gate and drain resistors R_G and R_D respectively on the opposite sides of each block (block 3 is indicated as an example).

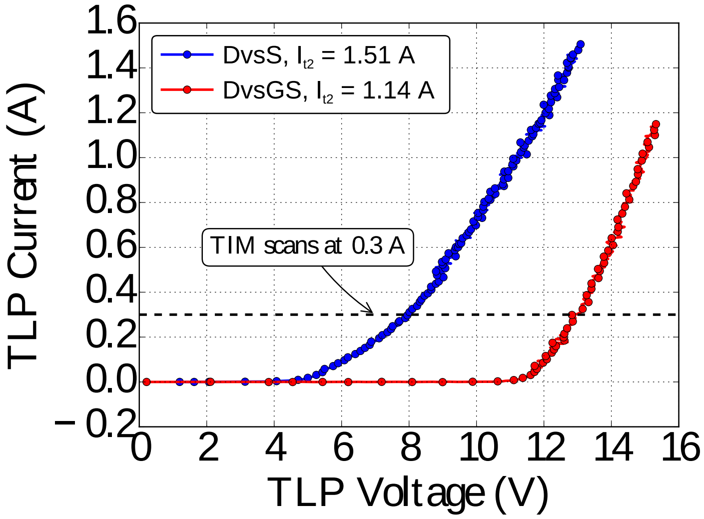
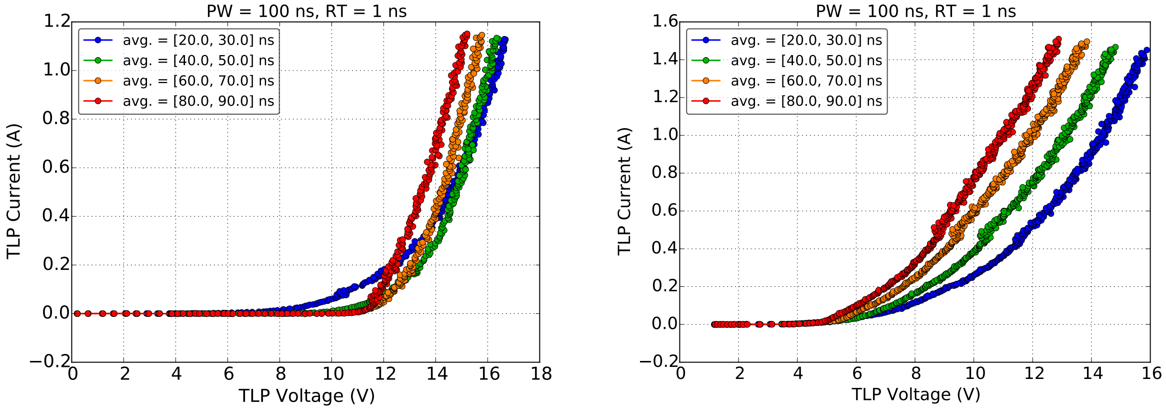


Figure 5.2: TLP-IV comparison for two configuration of 6STTS devices. Common TLP parameters: $(PW, RT) = (100, 1)$ ns, averaged time interval to calculate TLP-IV $[70, 90]$ ns. The horizontal dashed line for 300 mA indicates the current level used to carry out the TIM results in both configurations displayed in figures 5.5 and 5.6.

levels are reported in figure 5.4(a) for DvsGS and in 5.4(b) for DvsS. We note that the waveforms are similar, characterized by current decrease (voltage increase) for $t < 40$ ns and current increase (voltage decrease) in the second part of the interval.

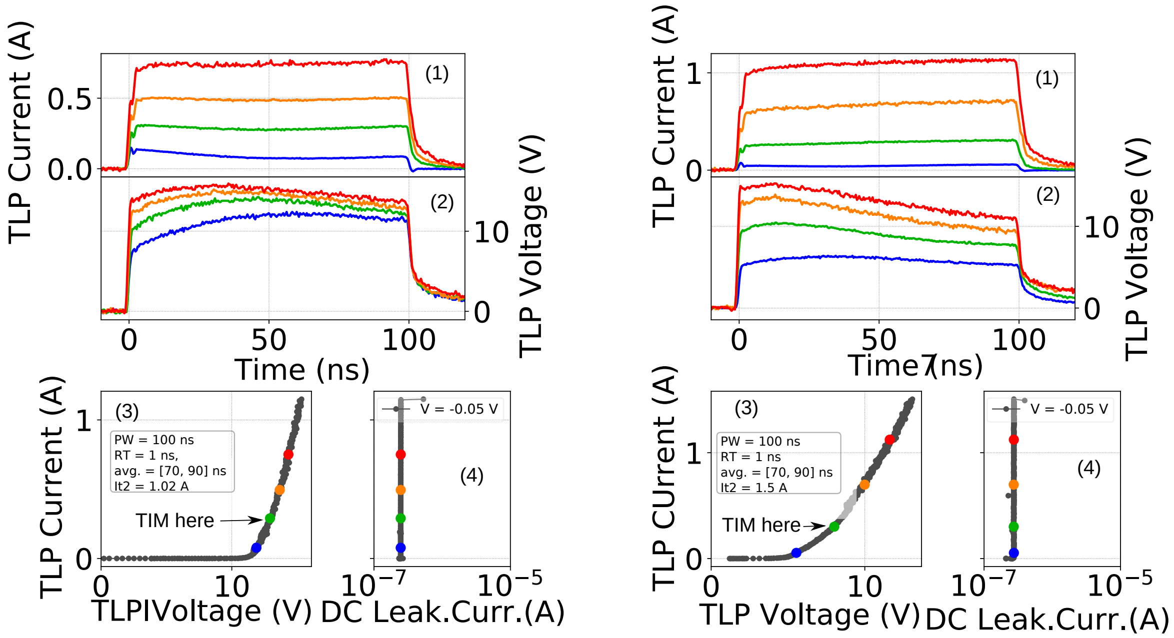
As done for 16STTS devices in chapter 4, we probed the devices by TIM measurements



(a) Configuration DvsGS.

(b) Configuration DvsS

Figure 5.3: TLP-IVs measured at different time intervals on 6STTS device. Time intervals are indicated in the legends. For both figures, $(PW, RT) = (100, 1)\ ns$.



(a) Configuration DvsGS.

(b) Configuration DvsS.

Figure 5.4: For both figures: (1) current waveforms, (2) voltage waveforms, (3) TLP-IV calculated in the interval $[70, 90]$ ns, (4) DC leakage current IV. Waveforms shown in (1) and (2) belongs to TLP-IV colored points in (3) and (4).

in order to map the thermal power dissipation.

5.3 Power dissipation by TIM for $PW = 100$ ns

The device was probed by TIM scans carried out for similar current level of 300 mA as indicated in figure 5.2 for $PW = 100$ ns. Selected TIM measurements are shown in the following for both configurations. The TIM paths for DvsS configuration are indicated in figure 5.5a, whereas for DvsGS configuration in figure 5.6a We scanned the device across multiple paths, in particular it was necessary for the DvsGS configuration.

In the following, we present firstly the results for DvsS configuration and afterwards the results for DvsGS.

Results for DvsS configuration. The chosen TIM paths in DvsS configuration were similar to what shown for 16STTS devices, i.e. a general TIM scan across the blocks in the central region and another across all fingers of the 1^{st} block.

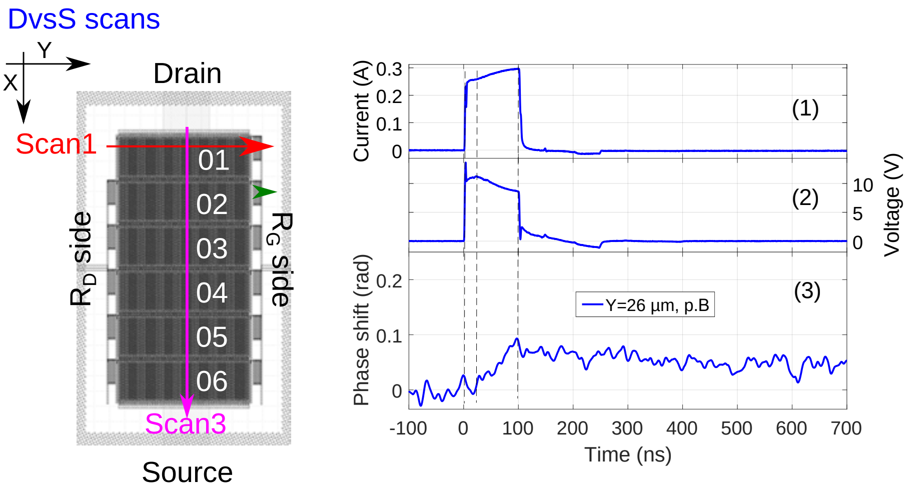
The transient TLP waveforms and a selected phase shift waveform for this case are displayed in figure 5.5b, the TIM scan "scan1" along the 1^{st} block is shown in figure 5.5c and the averaged measured phase shift per transistor is reported in figure 5.5d.

The "scan1" along the 1^{st} block showed rather homogeneous phase shift for all selected time instants during and at the end of the pulse. We saw indeed that the phase from $t = 40$ ns started rising in the whole active region (i.e. the region with the multi-finger transistors), then we observed that the phase shift mostly rose in the central region $Y = [18, 42]$ μm. In the regions outside the multi-finger region (left and right side of the plot), we noted weak phase shift only for curve $t = 100$ ns. Therefore in this configuration, all fingers on the 1^{st} block are subjected to similar power dissipation and electrical stress condition.

The averaged phase shift per transistor (figure 5.5d) per block showed that for $t = 40$ ns, the phase shift is nearly homogeneous among the transistors. It starts rising for $t > 40$ ns in the first transistors. For $t \geq 80$ ns (i.e. orange and red curves), the phase shift increased fastly on the 1^{st} transistor. The 1^{st} transistor has the highest phase shift at the pulse end ($t = 100$ ns, red curve). Other transistors showed progressively decreasing phase shift towards the last blocks. The last transistor (number 6) showed phase shift at the noise level.

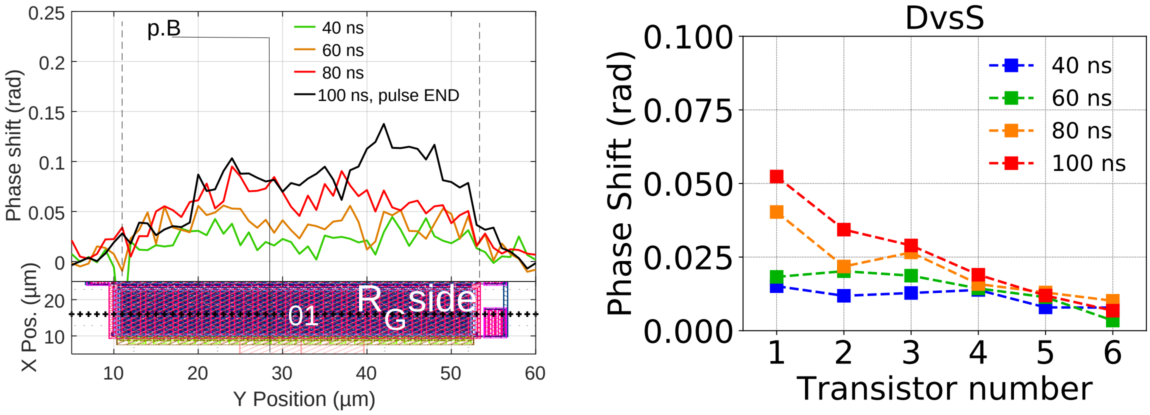
We want to remark that in the R_G side for curve at $t = 100$ ns, the power dissipation is slightly higher than in the rest of the block, it might be the beginning of a possible inhomogneous power dissipation in this part of the block but due to the pulse end we cannot see the evolution.

Additional TIM scans were carried out e.g. along the 2^{nd} block or on the R_G and R_D sides along all blocks. The results are omitted, since they did not provide new information because they did not show any particular sign of inhomogeneous power dissipation along the finger of the same block.



(a) Layout of 6STTS device with TIM paths scan or configuration DvsS indicated by colored arrows.

(b) DvsS. (1) TLP current transient waveform, (2) TLP voltage transient waveform, (3) transient phase shift corresponding to Y position $Y = 28\mu\ m$ indicated in phase shift cross-section in (d) by “p.B”.



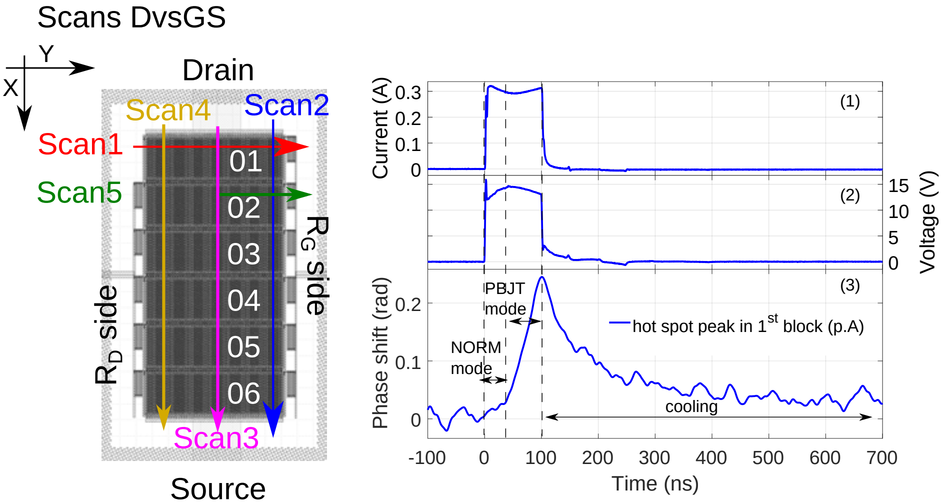
(c) Measured phase shift across the 1^{st} block (refer to path “Scan1” in 5.5a) for the different time instants (see the legend). The vertical dashed lines marked the region with multi-finger transistors. The R_G resistor is on the right side. The location of phase shift transient waveform shown in 5.5b(3) is marked by “p.B”. We observe that the phase shift is concentrated in the center homogenous and it can be considered homogenous.

(d) Measured phase shift per block in the device center (refer to path “Scan3” in 5.5a). We note that the phase shift is higher towards the first block and the first block show the highest value at the pulse end (100 ns).

Figure 5.5: TIM scan paths, TLP waveforms and TIM results on 6STTS device for DvsS configuration.

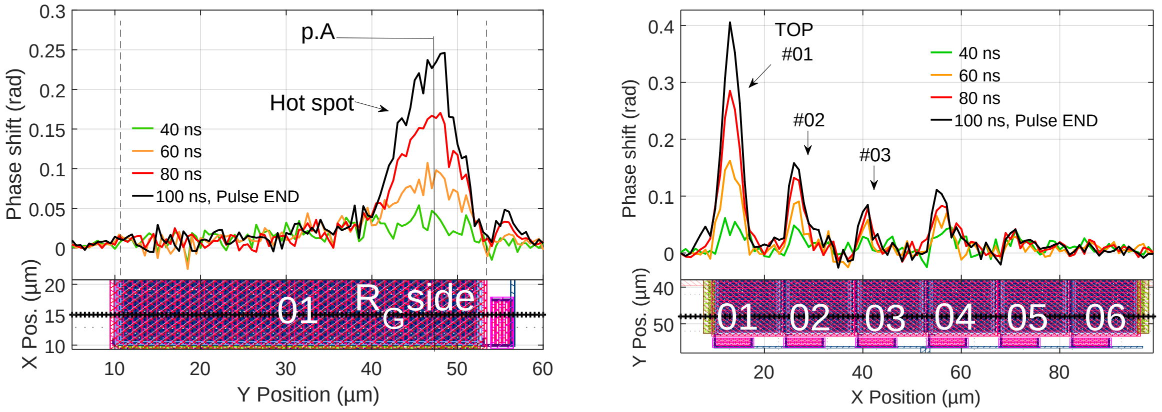
Results for DvsGS configuration. For the chosen TLP stress point for TIM, the TLP waveforms showed an average current of 300 mA and average voltage of 13 V in figure 5.6b(1) and figure 5.6b(2), respectively.

The "scan1" along the fingers of 1^{st} (see path in 5.6a) showed a hot spot visible from curve for $t \geq 60\ ns$ in figure 5.6c. The hot spot size was 10 μm and it was located in the R_G side of the block. We note also that the peak is shifted towards the edge of the multi-finger structure and placed at $Y = 48\ \mu m$.



(a) Layout of device of 6STTS device with TIM paths scan or configuration DvsGS indicated by colored arrows.

(b) DvsGS. (1) TLP current transient waveform, (2) TLP voltage transient waveform, (3) transient phase shift corresponding on the hot spot in 1^{st} transistor.



(c) DvsGS, scan 1 on 1^{st} transistor (refer to path "Scan1" in 5.6a). The R_G side is on the right side of the plot.

(d) DvsGS, scan 2 on on all transistors on R_G side from 1^{st} transistor (left side of the plot) to the last transistor number 6 on the right side of the plot. Refer to path "Scan2" in 5.6a.

Figure 5.6: TLP waveforms and main TIM results in DvsGS configuration for 6STTS device.

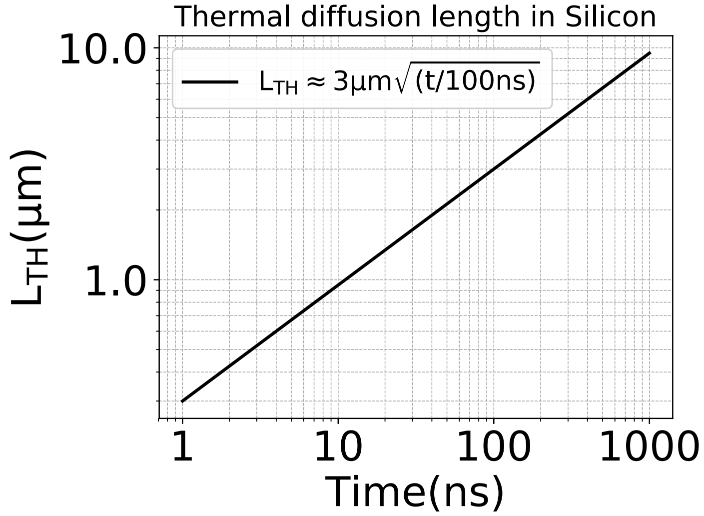


Figure 5.7: Silicon thermal diffusion length L_{TH} as function of time from [16]. The relation between between L_{TH} and diffusion time is reported in the legend. Note that both axis are in logarithmic scales.

We observed also an additional peak in correspondence of the R_G resistor but it was not due power dissipation in the R_G, but rather it originated by the lateral heat diffusion coming from the hot spot inside the 1^{st} transistor. This fact was in accordance with the thermal diffusion length L_{TH} in silicon shown in figure 5.7 where we see that for 80 ns, $L_{TH} > 2$ μm [16] that is the distance between the edge of the multi-finger structure and the high phase shift in correspondence of the R_G. Abrupt change in phase distribution at $y = 54$ μm was due to the low heterodyne signal caused by the edge scattering effects of the multi-finger structure. On the other side of the 1^{st}, we observed no phase shift. Therefore, the localized hot spot in the R_G side seemed to be due to current filament formation due to PBJT activation and related negative differential resistance. From the transient phase shift waveform at the peak value for $Y = 48\mu m$ in figure 5.6b(3), we noted that for $t \leq 40$ ns, the phase slowly rose, but then a steep increases is observed until the pulse end ($t = 100$ ns). Then the phase shift decreases due to the cooling. It is also interesting to point out that the phase shift slope increase occurs at $t = 40$ ns in correspondence of the current increases (follow the vertical dashed lines in figure 5.6b).

Despite the clear hot spot location in one side of the 1^{st} transistor (R_G side) from figure 5.6c we wanted to exclude any possible pulse-to-pulse instability due to finger-to-finger triggering as in [103] analyzing the TIM scatter plot of figure 5.6c for $t = 100$ ns. The result is shown in figure 5.8 by blue circles only for $t = 100$ ns. In this figure, the averaged phase shift is also indicated by red line and it is the same as in figure 5.6b (black line). In the scatter plot, we plotted the phase shift values for each position for each acquired pulse, i.e. 15 values of phase shift per position. The scatter plot did not show any anomalies because all scatter points are quite confined. Therefore, we can consider the hot spot in the 1^{st} block stable, confirming the absence of any pulse-to-pulse instability in the current density.

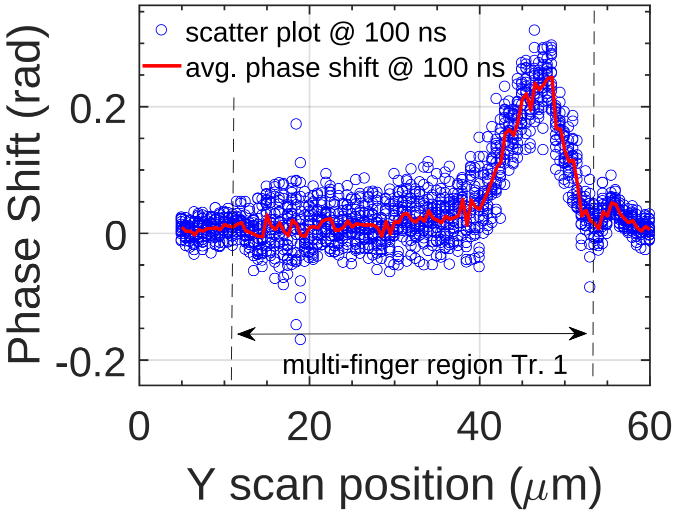
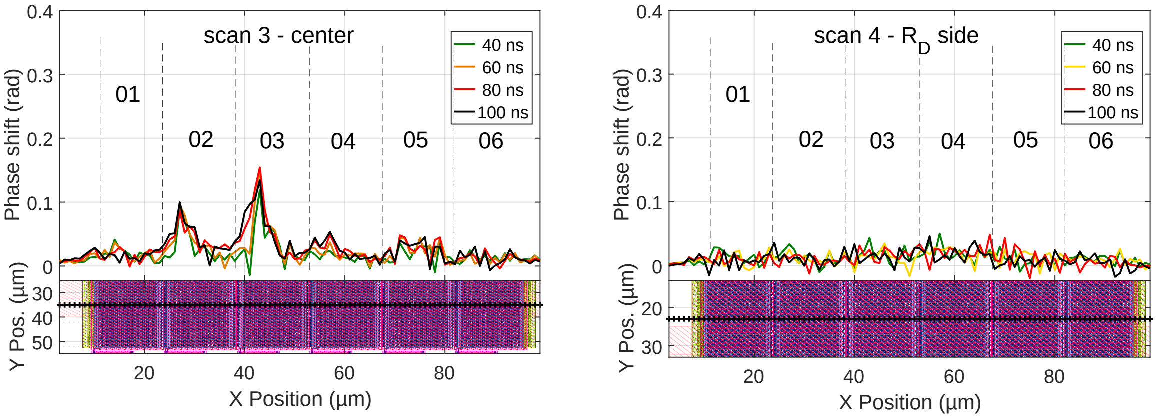


Figure 5.8: In blue circles, the scatter plot refereed of TIM scan "scan1" along the 1^{st} block for $t = 100\ ns$. For every position, 15 points are displayed (one per each acquired waveform). In solid red line, the averaged phase shift. This latter is the same displayed in the black curve at 100 ns in figure 5.6b. The scatter plot excludes any pulse-to-pulse instability in the hot spot of 1^{st} transistor.

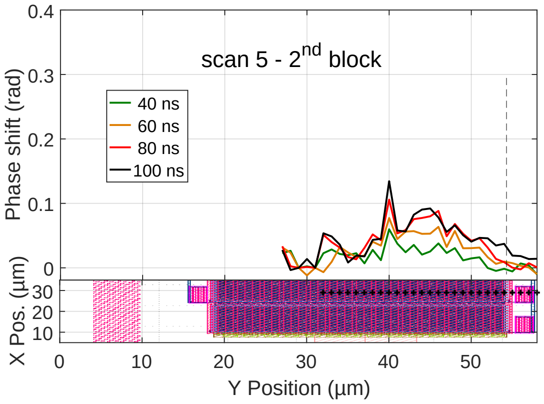
With knowledge of the clear hot spot appearing in the 1^{st} block on the R_G side, we carried out another TIM scan along the path "Scan2" in figure 5.6a along all the blocks in the their R_G side where we found the hot spot inside the 1^{st} transistor. The result for multiple time instants is shown in figure 5.6d. We noted that 1^{st} transistor showed the highest phase shift and this latter decreases towards the last blocks reaching basically the noise level on the last block (number 6). In particular, we saw that also blocks number 2, 3 and 4 can be considered showing relative high power dissipation. The phase shift on block number 5 was really close to the noise level to be certainly considered as a real heat dissipation.

Two additional similar scans along the blocks were also carried out in the center of the multi-finger blocks ("Scan 3" in 5.6a) shown in figure 5.9b and in the R_D side, this latter is named "Scan 4" in 5.6a and it is displayed in figure 5.9a. The "scan 3" showed no phase shift in the first block (because the hot spot is localizedin $Y = [38, 52]\ \mu m$ from figure 5.6c and "scan 3" was carried out for $Y = 35\ \mu m$, i.e. outside the hot spot). On the other side, block 2 and 3 present non-negligible phase shift, sign that the extension of the high power dissipation zone in this block was wider than that in the 1^{st} and it spread beyond the device center (considered to be at $Y = 35\ \mu m$). Block 4 and 5 showed weak power dissipation: the weak hot spot region was vanishing around the center. Block 6 did not show (once more) measurable phase shift and possible features were below the phase shift detectable level.



(a) DvsGS, scan 3 on on all transistors in their center from 1^{st} transistor (left side of the plot) to the last transistor number 6 on the right side of the plot. Refer to path "Scan3" in 5.6a.

(b) DvsGS, scan 4 on on all transistors in their center from 1^{st} transistor (left side of the plot) to the last transistor number 6 on the right side of the plot. Refer to path "Scan4" in 5.6a.



(c) DvsGS, scan 5 on on the R_G side of the 2^{nd} transistor (left side of the plot) to the last transistor number 6 on the right side of the plot. Refer to path "Scan3" in 5.6a.

Figure 5.9: Additional TIM results for DvsGS configuration on device from 6STTS device.

The last TIM scan shown was the 2^{nd} block from the center to the R_G side, see it in figure 5.6a. We observed from the figure that the high power dissipation region extends until $Y \approx 30\mu m$ confirming what seen in "scan 3" in figure 5.9a. We also noted that the high dissipating region can be considered symmetric (in 1^{st} transistor was localized towards the edge and the R_G side of the block, see figure 5.6c).

Comments on TIM measurements TIM scans for the same current level for different gate biasing conditions, resulted in different phase shift distributions. For this TLP pulse width, the gate bias impacted on the TLP-IV and also on the power dissipation distribution.

We tried to carry out additional TIM scans in DvsGS for higher current levels but these resulted into fast and cumulative damage of the device during the scan after few points[1].

On the other side for DvsS, we could carry out TIM measurements also at 500 mA always for $PW = 100\ ns$. Qualitatively, the results were similar to the previous results without any inhomogenous power dissipation in the same block but with the overall power dissipation distribution decreasing from the 1^{st} block to the 6^{th} last block. For these reasons, we will not show these results for 500 mA.

5.4 Transient simulations for $100\ ns$ TLP stress with floating gate (DvsS)

The first results to be shown are in DvsS configuration. The stress level is the same ($V_{CH} = 22\ V$, $I_{DUT} = 300\ mA$) as for TIM measurements at $PW = 100\ ns$ as shown in figure 5.5.

The simulations include both the drain breakdown model and the B2B current sources.

We note qualitatively voltage and current agreement between measured and simulated waveforms in figure 5.10a(1, 2) respectively. The V_{DS} and V_{GS} transient behavior are similar to 16STTS device. However due to the fact of the reduced W_{TOT} and consequently reduced gate time discharge constant of 6STTS device in respect to 16STTS device, the V_{GS} decreases faster in device of 6STTS device, see simulated V_{DS} and V_{GS} in figure 5.10b(1, 2) respectively. The 1^{st} transistor enters into breakdown for $t = 40\ ns$ due to the $V_{DS} \geq 2\ V$ and at the same time the $I_{B2B,(1,2)}$ starts flowing, see plots 5.10c(2, 3). The $I_{BD,2}$ is activated almost at the pulse end, see 5.10c(2).

Then, the normalized simulated phase shift distribution is reported in figure 5.10d for $t = 100\ ns$, i.e. at the pulse end. The simulation are in overall qualitatively agreement with phase shift cross section in figure 5.5. However, we have to point out that the phase shift difference between the 1^{st} and 2^{nd} transistor is quite large compared to measurement results.

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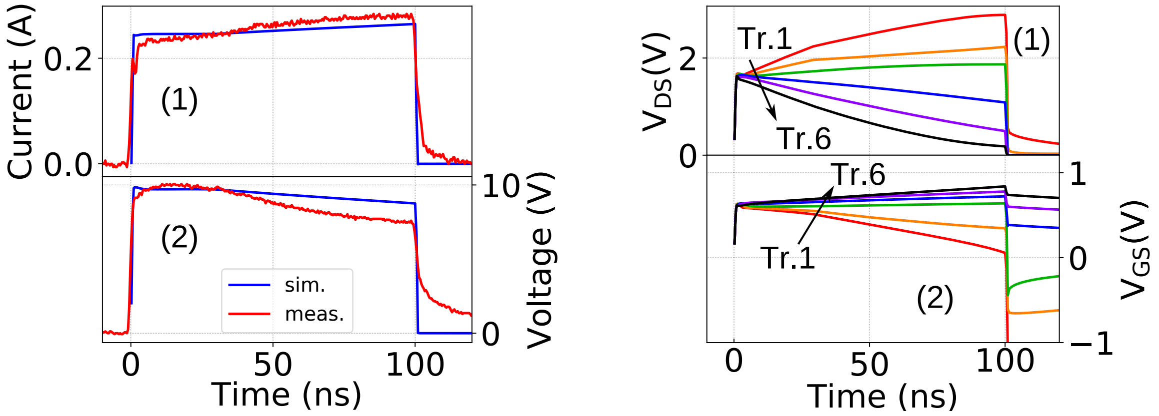
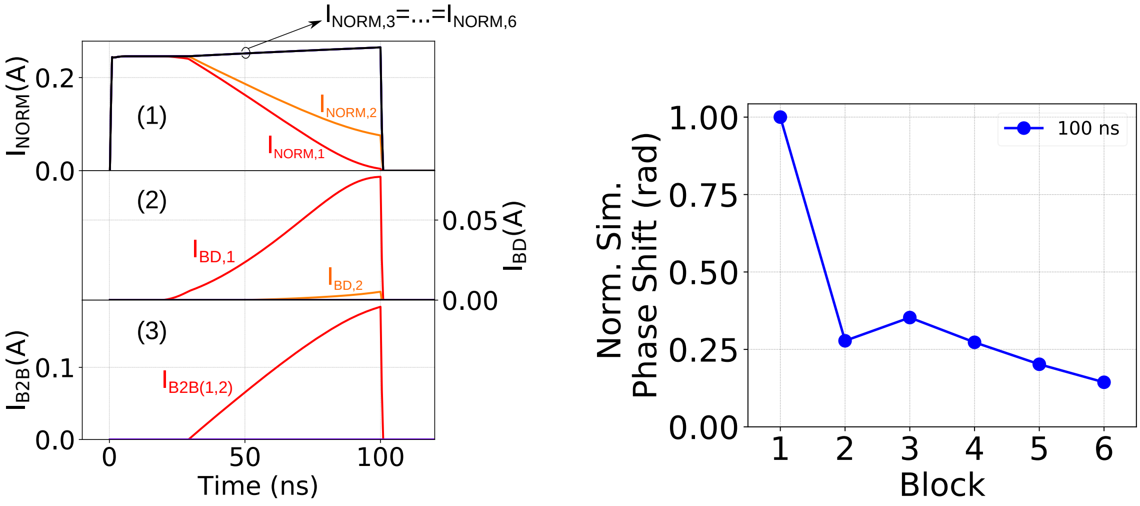
[1] We remind that we must apply at least 15 pulses per scanned position and then average them in order to increase the signal-to-noise ratio on these multi-finger devices.



(a) (1) current and (2) voltage comparison of measurements (in red) versus simulations (in blue).

(b) (1)simulated V_{DS} and V_{GS} transient waveforms. Every curve indicates a transistor.



(c) Simulated transient (1) I_{NORM}, (2) I_{BD} and (3) I_{B2B}. Note that in (1), $I_{NORM,[3-6]}$ coincide.

(d) Simulated phase shift per block. The normalization was done dividing each the simulated phase shift by the maximum phase shift value.

Figure 5.10: DvsS configuration simulations for the TIM bias point shown in figure 5.5.

5.5 Transient simulations for $PW = 100\ ns$ at TIM stress conditions for DvsGS configuration

From TIM measurements in figures 5.6 and 5.9, we saw that this configuration is characterized by inhomogeneous power dissipation in the blocks. In particular, TIM revealed hot spots located in the R_G sides of blocks 1-4 at 300 mA. In order to compare the measured phase shift from TIM and the simulated phase shift from transient simulation as done for 16STTS devices, we had averaged all the phase shift collected per block from previous TIM scans. The result is shown in figure 5.11 only for $t = 100\ ns$ by gray dashed line.

Due to the fact that one multi-finger transistor is simulated by one transistor component, inhomongeous power dissipation could not be simulated by our simplified simulation circuit. The simulations, in this case, should be compared to the averaged phase shift of the fingers.

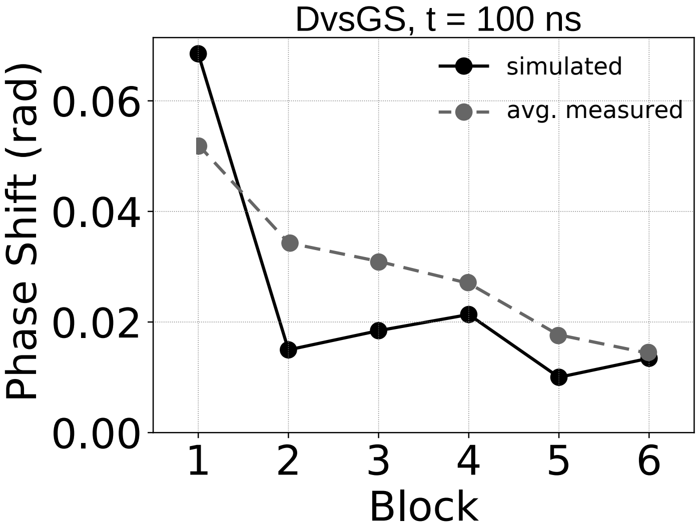
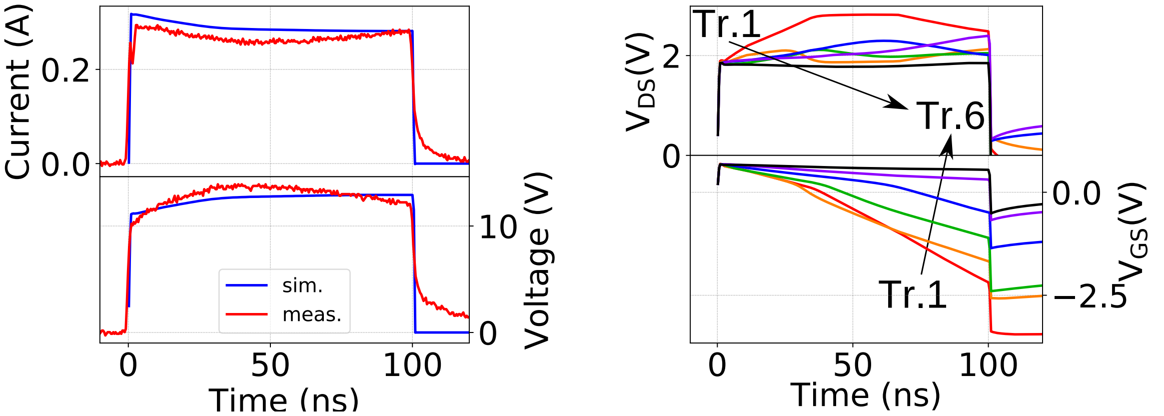


Figure 5.11: Measured averaged (avg.) in dashed gray line per block and in solid black simulated phase shift in configuration DvsGS of 6STTS device. The results are taken at $t = 100$ ns.

The simulated voltage and current waveforms are show in figure 5.12a by blue curves and they report quantitative accordance with measured waveforms in red. From the V_{GS} transient plot, we saw that the red curve corresponding to 1^{st} transistor crosses the 0 V at 40 ns. This is the same time at which the measured phase shift presented a steep rise in figure 5.6b(3).

The simulated phase shift is displayed in figure 5.11 by blue curve and compared with the averaged simulated phase shift for $t = 100$ ns. We saw that the transistors 1-3 showed a different qualitative behavior compared to the measured phase shift: averaged measured phase shift of 1^{st} transistor is lower than the simulated, simulated phase shift on the 2^{nd} and 3^{rd} transistors decrease instead of increasing.

We interpreted this fact as the simplification of our models for these latter conditions. For instance, they do not take into account other possible involved phenomena, e.g. a possible dependence of the drain breakdown from the B2B interaction, inhomogeneous bulk bias condition, self-heating effect, distributed gate resistance network.



(a) (1) current and (2) voltage comparison of measurements (in red) versus simulated (in blue) waveforms.

(b) (1)simulated V_{DS} and V_{GS} transient waveforms. Every curve indicates a transistor.

Figure 5.12: DvsGS configuration simulations for the TIM bias point shown in figure 5.6 and 5.9.

5.6 Further investigation for long PW

The device was investigated for both configurations also for $PW = 450\ ns$ and $RT = 1\ ns$ to see the transient evolution of the hot spot on the 1^{st} transistor detected during the transient TIM analysis in DvsGS configuration for $PW = 100\ ns$ and to verify any inhomogenous power dissipation appearing in DvsS configuration.

The TLP-IVs in DvsGS configuration (in red) and in DvsS configuration (in blue) were calculated in the interval $[0.7 \cdot PW, 0.9 \cdot PW] = [315, 405]\ ns$ and the comparison is shown in figure 5.13. We note that the for $PW = 450\ ns$, the I_{t2} is similar for both configurations and located at $240\ mA$. As also happening for $PW = 100\ ns$, the DvsS configuration showed lower voltage in comparison to DvsGS.

Then, two TIM scan along the 1^{st} transistors from the R_G side to the R_D side for same $100\ mA$ current level were carried out (see them indicated by the arrows in figure 5.13).

TIM measurements for $PW = 450\ ns$ for DvsGS configuration The TLP voltage (in blue and referring to left y-axis) and the TLP current (in red and referring to right y-axis) waveforms for TIM scan in DvsGS are reported in figure 5.14, whereas the phase shift from the TIM scan along the 1^{st} transistor is reported for multiple time instants in figure 5.14b. Please, note that this latter scan was not completed till the end of the multi-finger region due to a disconnection of the sample during the scan at position 52 μm.

The phase shift in figure 5.14b analyzed with the current waveform in figure 5.15a suggested to divide the 1^{st} transistor in three regions of operation named “reg.1” , “reg.2”

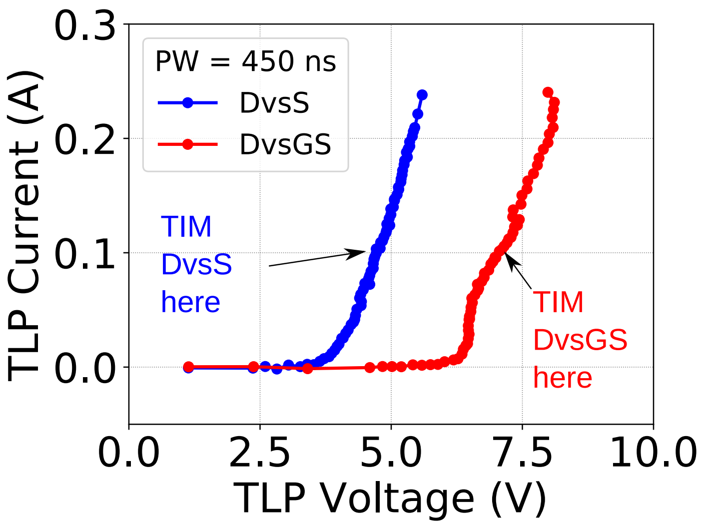


Figure 5.13: TLP-IV comparison of measurement in DvsGS configuration (in red) and in DvsS configuration (in blue) were calculated in the interval $[0.7 \cdot PW, 0.9 \cdot PW] = [315, 405]$ ns. The TIM stress points are indicated for both curves and they are at 100 mA.

and "reg.3". We noted that the hot spot occurs again in the R_G side rising for $t = 50$ ns (purple curve) in figure 5.14b. The curve at the next time instant $t = 100$ ns clearly showed the hot spot in the R_G side of the multi-finger active region from position 13 μm to position 25 μm. The hot spot size resulted to be 10 μm, similar spatial extension and location as found previously for $PW = 100$ ns in figure 5.6c. The "reg.1" corresponded indeed to the hot spot appearing in the 1^{st} transistor detected for $t = 50$ ns and $t = 100$ ns. Regions "reg.1" and "reg.2" showed no phase shift for $t \leq 100$ ns.

New features were however visible from $t \geq 200$ ns in regions "reg.2" and "reg.3": from this time instant (for blue curve $t = 200$ ns), we saw that the phase shift started homogeneously rising also on the other part of the multi-finger active region (i.e. regions "reg.2" and "reg.3") of the 1^{st} transistor.

Besides the phase shift rise in "reg.2" and "reg.3", the hot spot increased (high phase shift) in "reg.1" and also it extends towards the center of the multi-finger region (covering the position until 30 μm). The region "reg.2" was defined as a transition region between the hot spot region ("reg.1") and the region where flat phase shift occurs ("reg.3"). In "reg.2" it was also evident the lateral heat spread[2] coming from "reg.1" (see from green curve, i.e. for $t \geq 300$ ns).

On the other side of "reg.1" i.e. for position ≤ 13 μm, the heat diffusion tail from "reg.1" is also visible.

A way to interpret the results at long PW follows. The fingers in "reg.1" have a negative differential resistance [123] causing a filament behavior and showing high power

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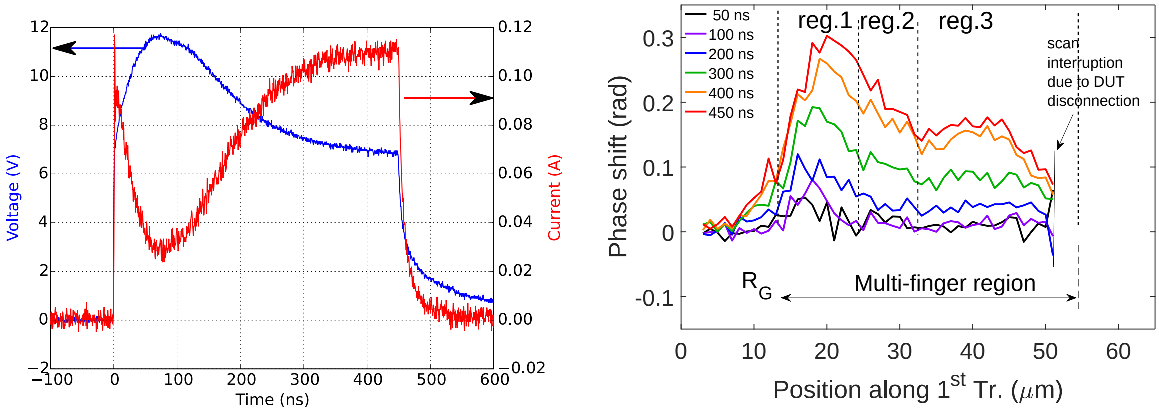
[2] After $200 - 300$ ns, the heat could laterally spread to $4 - 5$ μm, see it from figure 5.7.



(a) TLP voltage (left axis) and current (right axis) waveforms applied for TIM scan along the multi-finger region of the 1^{st} transistor for DvsGS configuration, $PW = 450\ ns$, $RT = 1\ ns$.

(b) TIM scan along the multi-finger region of the 1^{st} transistor for DvsGS configuration, $PW = 450\ ns$, $RT = 1\ ns$. Note the hot spot in the position interval $(13, 25)\ \mu m$. See also the phase shift rise in the other part of the active region for $t \geq 200\ ns$.

Figure 5.14: TLP current and voltage waveforms at the TLP stress level used during the TIM measurement along the 1^{st} transistor for $PW = 450\ ns$ for DvsGS configuration.

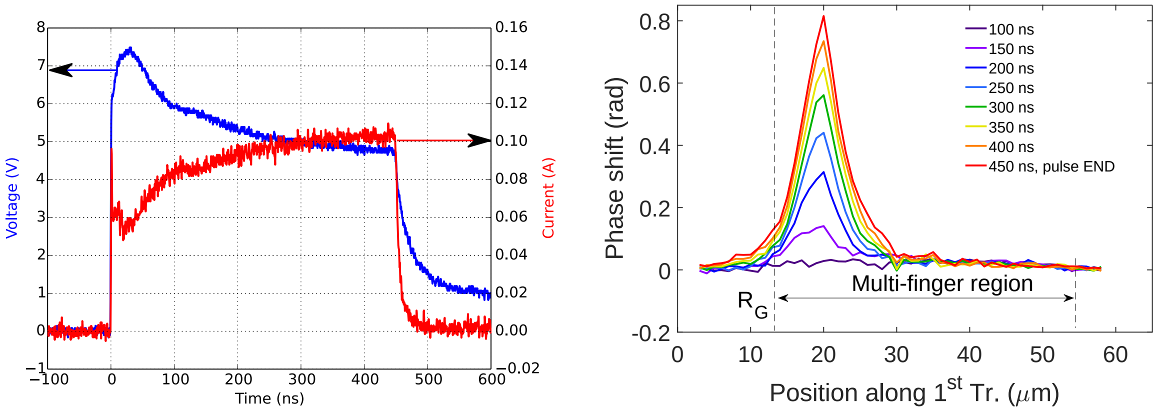
dissipation. Due to the transient decrease of V_{GS}, this region spread towards the other side of the block. The consequent high phase shift appearing in “reg.2” and “reg.3” could be caused by the finger-to-finger coupling effect thanks to the lateral spread of the carriers from the hot spot of “reg.1” causing also here the PBJT triggering seen for $t \geq 200\ ns$ in “reg.2” and “reg.3”. In “reg.2”, we have the superimposition of the effect of the finger-to-finger coupling and the “simple” lateral heat spread from the “reg.1” (this is the reason why we separate “reg.2” from “reg.3”).

However, this is still an hypothesis and it should be verified by accurate TCAD simulations.

TIM measurements for $PW = 450\ ns$ for DvsS configuration The TLP current (in red for right y-axis) and voltage (in blue for left y-axis) used for TIM in this configuration are shown in figure 5.15a. The phase shift cross-section for multiple time instants is displayed in figure 5.15b.

For $t \geq 150\ ns$ this configuration showed a clear hot spot in the R_G side extending until position 30 μm at the pulse end (red curve at $t = 450\ ns$). The hot spot is visible from purple curve for $t = 150\ ns$.

Comparing this results with previous result in the same DvsS configuration for $PW = 100\ ns$ in figure 5.5, we could now say at $PW = 100\ ns$ we saw only the beginning of the inhomogeneous power dissipation concluding that such 6STTS is not immune to inhomogeneous power dissipation no matter of the gate configuration status (floating



(a) TLP voltage (left axis) and current (right axis) waveforms applied for TIM scan along the multi-finger region of the 1^{st} transistor for DvsS configuration, $PW = 450\ ns$, $RT = 1\ ns$.

(b) TIM scan along the multi-finger region of the 1^{st} transistor for DvsS configuration, $PW = 450\ ns$, $RT = 1\ ns$.

Figure 5.15: TLP current and voltage waveforms at the TLP stress level used during the TIM measurement along the 1^{st} transistor for $PW = 450\ ns$ for DvsS configuration.

or grounded). This fact would exclude the gate status as the main root cause of the inohomogeneous power dissipation in the 6STTS. However, the gate bias is involved in the filament width appearing firstly on the 1^{st} block.

A possible hypothesis about the reason of the hot spot might be the B2B effect due to the fact that these devices had similar D_{B2B} as short D_{B2B} devices of chapter 4.

5.7 Pulsed EMMI in DvsGS configuration

The pulsed EMMI setup is presented in figure 1.11b. We used it for DvsGS configuration, in order to see the EMMI light locations and compare it to TIM measurements. The pulsed IV obtained in DvsGS for $PW = 100\ ns$ is displayed in figure 5.16a and it was limited to $0.2\ A$ because the device suffered of cumulative damage. For each charging voltage (i.e. stress level condition), pulses of $PW = 100\ ns$ by an Hewlett Packard 8114A solid state pulser are repeated every $1\ \mu s$ for a $1\ s$ total time[3]. Therefore for each stress condition level, around at least 100000 pulses are applied to the device under test.

The results are shown in the sub-figures of figure 5.16. They display the normalized light intensity collected at the focal plane array camera. In each image, the reader finds the six blocks borders delimited by black lines and marked with numbers from “01” to

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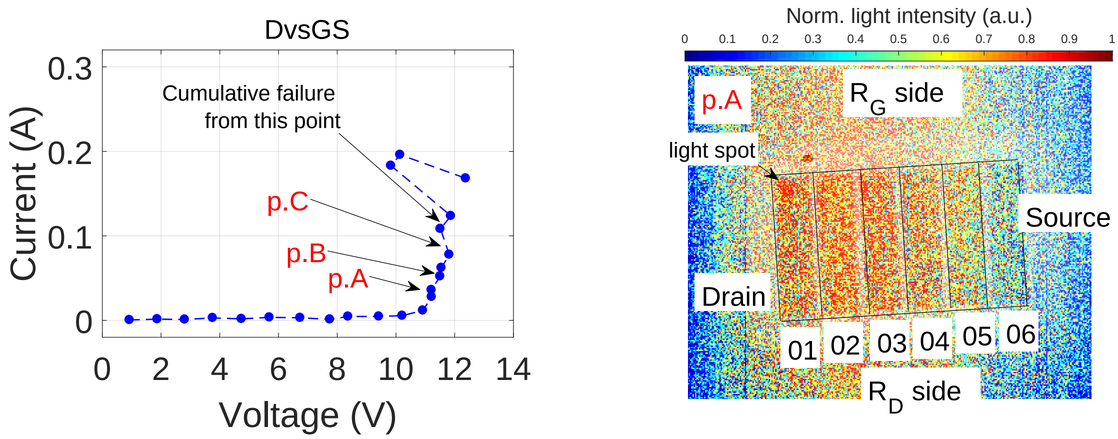
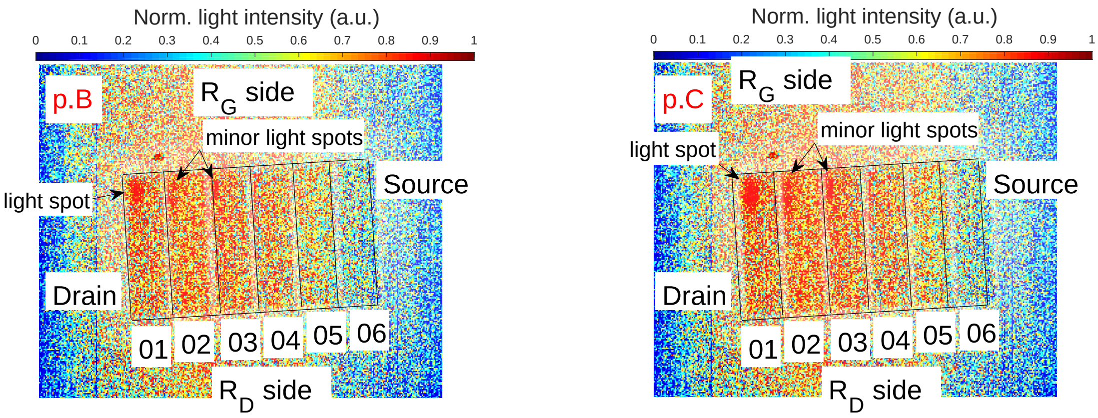
[3] Please, keep in mind that the acquisition time of one IR frame takes $20\ ms$ by the field-plan-array infra-red camera. Therefore, the results are obtained averaging all the frames belonging to the same stress level condition. In order to increase the signal to noise level, multiple frames for the same stress level are necessary.



(a) Pulsed-IV to obtain the EMMI images in DvsGS for PW = 100 ns calculated for (70, 90) ns time interval. The points marked with "p.A", "p.B" and "p.C" refer to other subfigure (b), (c) and (d), respectively. The failure of the device due to cumulative damage is also indicated. No images are shown after the failure.

(b) EMMI image relative to "p.A" indicated in figure 5.16a. See the light spot in the 1^{st} transistor R_G side corner.



(c) EMMI image relative to "p.B" indicated in figure 5.16a. See the light spot in the 1^{st} transistor R_G side corner.

(d) EMMI image relative to "p.C" indicated in figure 5.16a. See the light spot in the 1^{st} transistor R_G side corner.

Figure 5.16: EMMI images on 6STTS device at three different stress levels for $PW = 100\ ns$ in DvsGS configuration indicated in figure 5.16a. Note that the light intensity is normalized in each figure.

"06", where "01" is the label for the closest transistor to drain pad (left side of the image) and "06" is the transistor closest to the source pad (right side of the image). The R_G side (on the top of the figure) and R_D side (on the bottom of the figure) are also indicated.

The first EMMI at point "p.A" corresponding to 50 mA stress level in figure 5.16b reported the appearance of the light spot in the R_G side of the 1^{st} transistor, i.e. in the same position where TIM revealed the hot spot (see it indicated by the arrow and text "light spot"). We interpret the light EMMI spot as the location of the filament due to local parasitic BJT triggering, as observed by TIM measurement in the same configuration.

From EMMI at point "p.B" corresponding to 60 mA stress level, two other small light spots appeared in the R_G side corner of the 2^{nd} and 3^{rd} blocks, respectively (see them indicated by arrows and text "minor light spots"). At this level, the light spot in the 1^{st} block seemed to be brighter than in the condition of point "p.A".

The last EMMI image corresponding to the selected point "p.C" at 80 mA (see the position in the pulsed-IV of figure 5.16a) is shown in figure 5.16d. At this level we saw that the light spot in 1^{st} block and the minor light spots are brighter than point "p.B" and slightly more extended towards each block center. Therefore as the current level stress increases, the parasitic BJT triggering area spreads and this phenomenon progressively involves the blocks starting from 1^{st}.

Unfortunately and as already mentioned, due to cumulative damage in this configuration, we could not perform the EMMI at 300 mA as for TIM results. However, thanks to the analysis presented before, we are confident that for TIM current level also for the 4^{th} block in the R_G side corner should show a light spot, making TIM and EMMI results consistent one to the other. Therefore, (1) EMMI results confirmed the location of inhomogeneous high power dissipation of TIM, (2) provided the 2D distribution figure without scanning[4] and (3) provided an easy and fast tool to investigate these devices.

5.8 Pulsed EMMI in DvsS configuration

Besides the EMMI in DvsGS configuration, a similar analysis in DvsS configuration was carried out with the same EMMI parameters as the previous one: $PW = 100\ ns$, repetition time interval 1 μs and acquisition time per stress level 1 s to confirm also the TIM results of this configuration. The pulsed-IV calculated for $[70, 90]$ ns time interval is reported in figure 5.17a. We selected three points marked as "p.A", "p.B" and "p.C" and shown in figures 5.17b, 5.17c and 5.17d, respectively.

In DvsS configuration, the EMMI signal started to be seen at 220 mA corresponding to point "p.A" in figures 5.17a and 5.17b. We note that the EMMI signal (in red) is homogeneous and localized in the 1^{st} transistor.

Then, from EMMI measurements at "p.B" and "p.C" shown in 5.17c and 5.17d respectively, we saw that the 2^{nd} transistor and the 3^{rd} transistors are emitting. This is the sign that also in DvsS configuration the blocks are triggered one after the other.

Therefore, we confirmed that the locations of high power dissipation detected by TIM coincided with EMMI light regions for DvS configuration.

Hence, we can conclude that EMMI can be used for these devices to have information on the inhomogeneous power dissipation.

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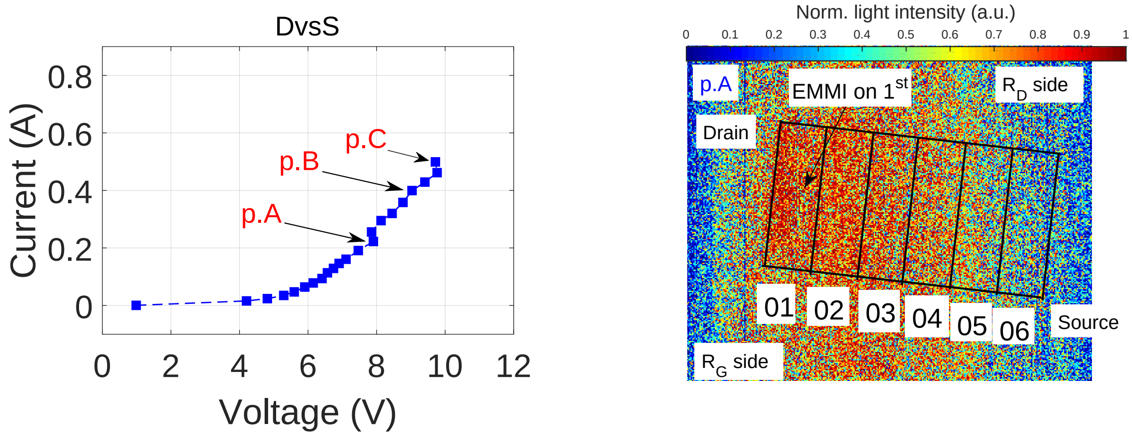
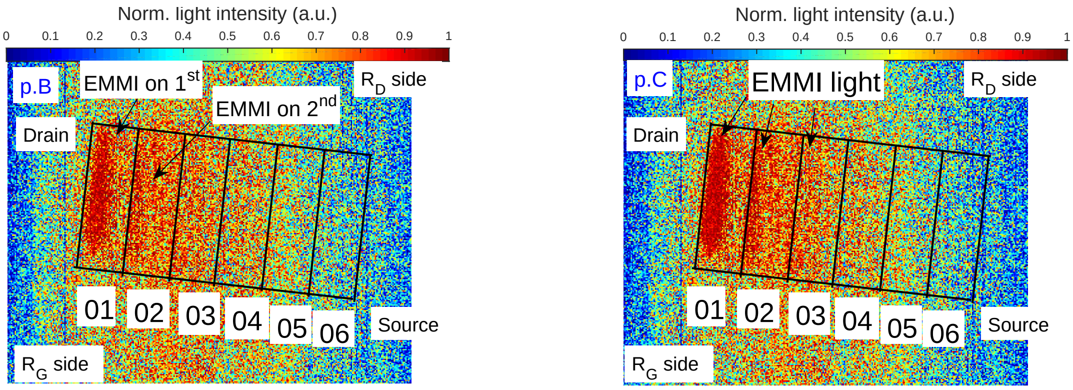
[4] The 2D TIM technique [124] was not suited for these multi-finger devices due to the low sensitivity.



(a) Pulsed-IV to obtain the EMMI images in DvsS for PW = 100 ns calculated for (70, 90) ns time interval. “p.A”, “p.B” and “p.C” indicate the selected points where EMMI results are shown in subfigure (b), (c) and (d). The measurement was interrupted at 500 mA. However, the device was not failed at this stress level and configuration.

(b) EMMI image relative to “p.A” indicated in figure 5.16a. See the weak light spot in the 1^{st} transistor in its center.



(c) EMMI image relative to “p.B” indicated in figure 5.16a. See the light spot in the 1^{st} transistor and a weak light EMMI signal also in the 2^{nd}.

(d) EMMI image relative to “p.C” indicated in figure 5.16a. See the light spot in the 1^{st}, 2^{nd} and also a weak signal in hte 3^{rd} transistors.

Figure 5.17: EMMI images on 6STTS device at three different stress levels for $PW = 100$ ns in DvsS configuration indicated in figure 5.17a. Note that the light intensity is normalized in each figure.

5.9 Experimental attempt to reproduce the inhomogeneous power dissipation on 1^{st} transistor

So far, the TIM results in DvsGS for $PW = 100\ ns$ revealed a hot spot in the R_G side of the 1^{st} transistor interpreted as the local parasitic BJT triggering. Then, TIM results for $PW = 450\ ns$ excluded the gate status as main root cause of the inhomogeneous power dissipation because inhomogeneous power dissipation was detected also in the configuration with gate floating, i.e. DvsS. Besides, the simulation models were not enough precise to explain the origin of the inhomogeneous power dissipation, even though we could have a qualitative overview of the waveforms evolutions. However, EMMI results confirmed the presence of the hot spot (seen as a light spot) in the 1^{st} transistor on the R_G side and the consequent light emission in the 2^{nd} and 3^{rd}.

In order to understand the impact of the B2B phenomenon as a cause of the inhomogeneous power dissipation occurring in the 1^{st} transistor, we decided to go further on the investigation of the DvsGS configuration.

Experiment concept and setup implementation Despite the used simulation model limits, we arise this question:

is there a way to reproduce the hot spot by EMMI on the 1^{st} *transistor block with only a single multi-finger block?* In such condition, no B2B would be possible but only the internal finger-to-finger coupling and proper $V_{GS,1}$ transient condition.

We wanted to realize an experiment that

1. it reproduced similar transient bias conditions on the 1^{st} transistor, in particular the fast negative V_{GS} decrease,
2. by a circuit configuration that is completely isolated the 1^{st} multi-finger transistor, in order to avoid any B2B effects with other transistors/devices.

As single multi-finger transistor, we used the well-known 150 multi-finger test structure used in chapter 3. This device could be also provided with high-ohmic silicon resistor $R_G = 400\ k\Omega$, exactly the same as the R_G of 6STTS device. The challenge was to find a suitable way to reproduce the electrical behavior of other 5 transistors of 6STTS device, i.e. transistors $2^{nd} - 6^{th}$.

The series connection of a single multi-finger transistor (with R_G) and an external device could attempt to mimic the condition of the 1^{st} transistor belonging to a stacked device into a single multi-finger transistor, see figure 5.18.

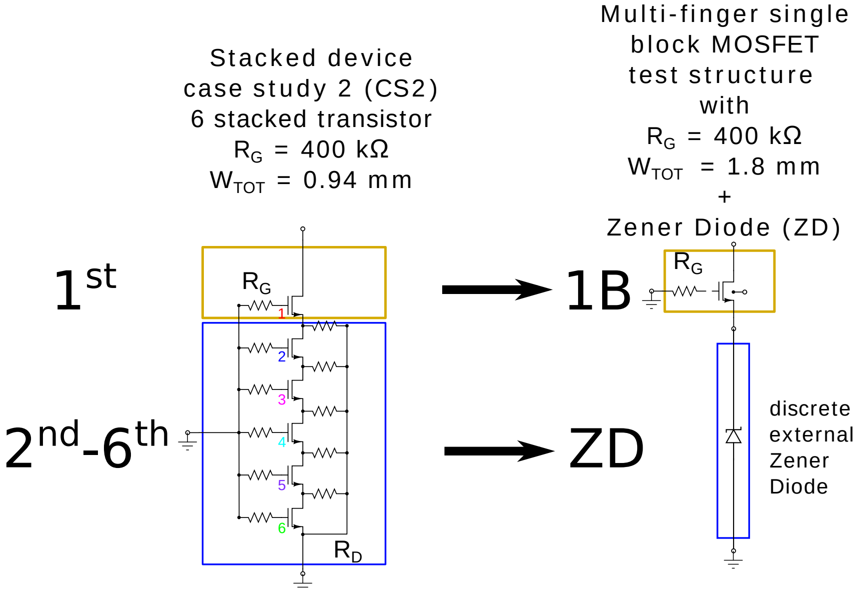


Figure 5.18: Schematic concept to mimic a 6 stacked device of 6STTS device (CS2) by the series of one single multi-finger block transistor with a discrete external Zener diode.

We chose the lowest capacitance external Zener Diode (ZD) with $V_Z = 9.1\ V\ (1\ W)$ [35] found in market as external component. Its capacitance was measured to be 100 pF.

The ZD was tested on the same electrical setup used for pulsed EMMI. Its waveforms are displayed in figure 5.19a. In the test, we stressed the device with 10 ns rise time and $PW = 200\ ns$ (see 5.19a(1, 2)) giving the pulsed IV shown by blue dotted line in figure 5.19a(3).

The setup to reproduce the inhomogeneous light emission included the ZD placed in a flexible pitch metal copper wire (see 5.19b) produced by HPPI [32], [34]. This flexible pitch is generally used to provide an additional ground signal from the shield of the 50Ω GGB Picoprobe model 10 needle probe to the device under test. In this setup, the cathode of the Zener diode was connect to ground (i.e. to the shield of the probe needle) and the anode was connected to the source pad of the multi-finger MOSFET, see the picture 5.19c.

We need to point out that the single block transistor width ($W_{TOT,150finger}$) is different from one block belonging to the stacked test structures ($W_{TOT,6STTS}$) of 6STTS device. As a matter of fact, $W_{TOT,6STTS} = 0.94\ mm$ and $W_{TOT,150finger} = 1.8\ mm$, hence $W_{TOT,150finger}$ is basically the double. The width impacts linearly on the gate discharge due to the $R_G \cdot C_G$ time constant. Hence, we needed to:

1. compare results on stacked transistor for $PW = 100\ ns$ with results on single stack transistor at $PW = 200\ ns$ (the double);
2. properly normalize also current by the respective device widths to be comparable.

The pulsed IV curves are in figure 5.20. Please note the two Y-axis scales. Moreover the IVs are calculated in the same scaled interval since we used $avg. = [0.7 \cdot PW, 0.9 \cdot PW]$, this results to be $[140, 180]$ ns for the series configuration of the multi-finger transistor and the Zener diode and $[70, 90]$ ns for the 6STTS device.

Results In the following, we present the EMMI comparison for the same current density and bias conditions on the 1^{st} block ($I_{DUT}/W = 80\ mA/mm$).

The simulated transient $V_{DS,1}$ and $V_{GS,1}$ are shown in figure 5.21a. Please, note the horizontal axis scale showing the time normalized by the PW used. The transient comparison of $V_{DS,1}$ showed a similar overall behavior. The discrepancies should be addressed to the fact that in the simulations of the 6STTS (blue curve), we employed the B2B. We note immediately in subfigure 5.21a(2), that the $V_{GS,1}$ waveforms are very similar. Both transistors entered into breakdown condition for $time/PW = 0.4$ crossing the $V_{GS,1} = 0\ V$. In particular, we see that at the pulse end both curves reached $-2\ V$. At this value the transistor works already in breakdown condition (see TLP curve in figure 3.13(a) for $V_{GS} = -2\ V$ in green color and the breakdown equation in 3.2).

In figure 5.21, the EMMI results relative to 80 mA/mm condition from figure 5.20 and the transient simulations condition in figure 5.21a are reported. The device orientation is indicated by the location of drain, source and gate with the R_G. We see that for the chosen condition, no inhomogeneous EMMI light spot can bee seen. This result indicated that it is not possible to reproduce the EMMI light spot in the R_G side of the 1^{st} transistor as in figure 5.16.

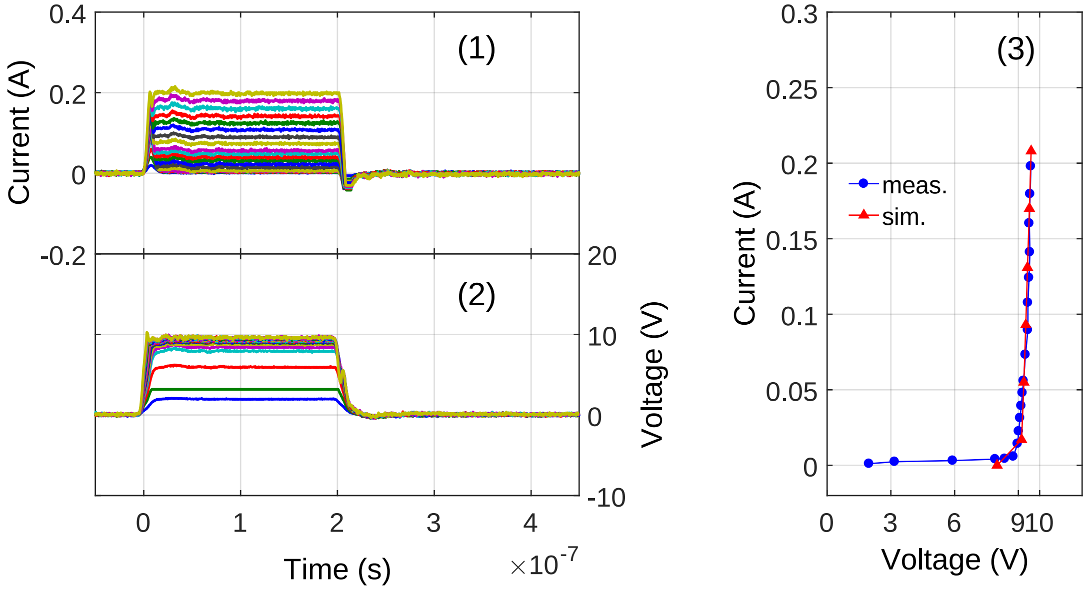
The results at higher currents still showed homogeneous EMMI in the used multi-finger transistor confirming the fact that the configuration given by the series of a 9.1 V Zener diode and multi-finger transistor (with R_G) could not be enough to produce any localized EMMI spot on the R_G side of the MOSFET.

To confirm what previously stated, we continued the investigation increasing the PW to 450 ns ($V_{GS,1}$ would decrease to more negative values) for the series configuration and stressing for very high current like 400 mA. Not even at this extreme conditions for the multi-finger device, we managed to see any localized EMMI spot in the active region.

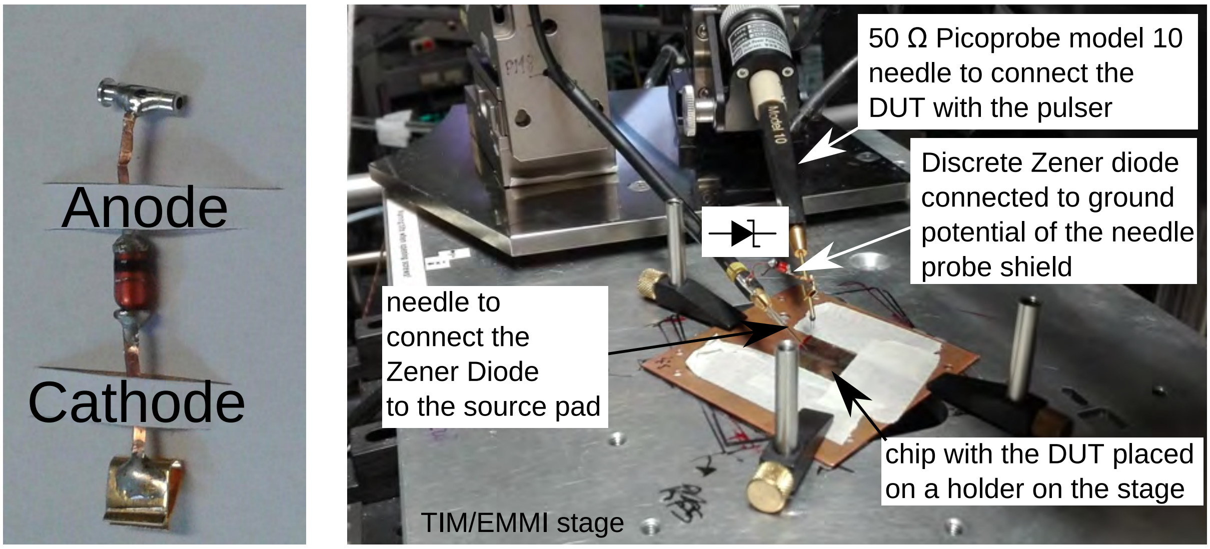
Therefore, the complete isolation of a 150 multi-finger transistor and the use of an external component did not reproduce any localized EMMI light spot. All these facts suggested that B2B phenomena can be the main reason responsible (or at least one very important) of the inhomongeneous power dissipation in ESD conditions.

It would be nice to prove a similar experiment using a test structure formed by the series of two multi-finger transistors (with their own R_G) placed at different D_{B2B} to find at which conditions the inhomongeneous EMMI hot spot appears. Unfortunately, such test structures are not available.

Nevertheless, we point out that we cannot exclude other effects to be the reason of the inhomongeneous power dissipation.



(a) (1) Current (2) voltage waveforms and (3) obtained pulsed IV in dotted blue line for discrete Zener diode for $PW = 200$ ns in the averaged time interval. In (3), the model of the Zener diode is shown by red triangle line.



(b) The discrete Zener diode was soldered into a flexible pitch from HPPI [32], [34] to be easily connected to the source of the multi-finger transistor and the grounded shield of Model 10 Picoprobe® probes.

(c) Picture of the setup to reproduce the inhomogenous power dissipation by the use of an multifinger transistor in the chip connected in series to a discrete Zener diode.

Figure 5.19: Test of the Zener diode with Zener voltage $V_Z = 9.1$ V employed by the experiment to mimic the behavior of 6STTS device.

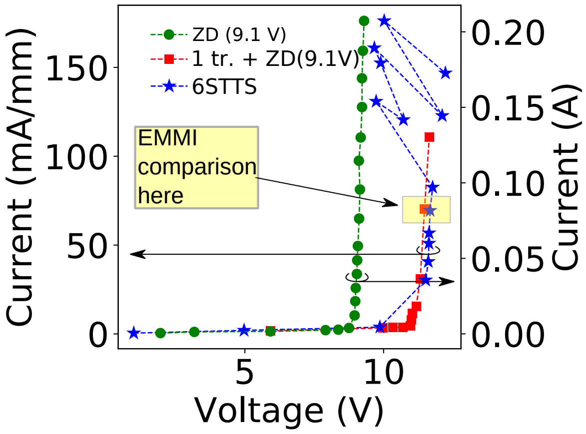
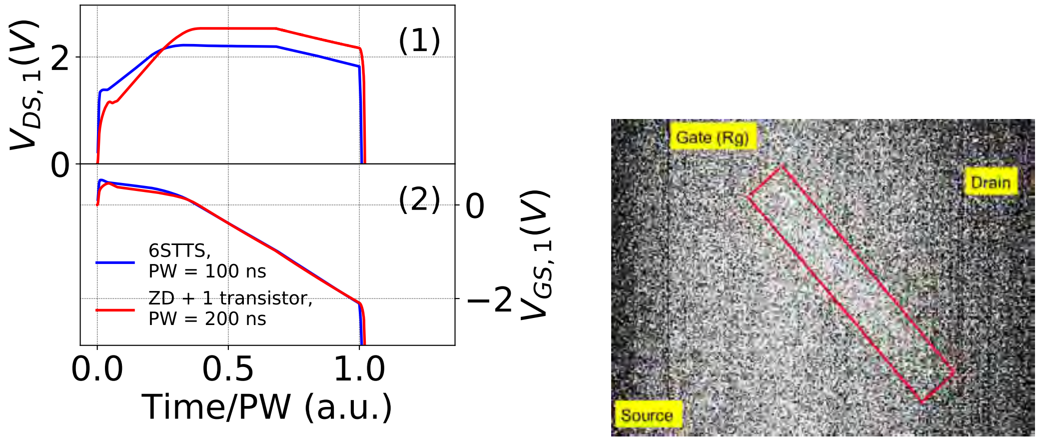


Figure 5.20: Pulsed IV comparisons: green dotted dashed line. Zener diode (Zener voltage $V_Z = 9.1\ V$); in red squared dashed points, the IV of the series configuration given by one multi-finger MOSFET block and the ZD obtained for $PW = 200\ ns$ and average time interval $[140, 180]\ ns$; in blue dashed star points, the IV of the 6STTS device for $PW = 100\ ns$ calculated for in time interval $[70, 90]\ ns$. Note the two different current Y-axis: on the right, for the IV of the Zener diode (ZD) is indicated by absolute current in (A); on the left by normalized current density in (mA/mm), for the other IVs. The stress level related to EMMI results and simulations of figure 5.21 is also indicated.



(a) Simulated (1) $V_{DS,1}$ and (2) $V_{GS,2}$ for the EMMI comparison point at current 80 mA/mm indicated in figure 5.20. In blue, the results relative to the 6STTS device, in red the results corresponding to the series configuration of the 9.1V Zener diode and one multifinger-transistor. Note that, due to different PWs (see in the legend), the time in the horizontal axis has been normalized by the PW.

(b) EMMI image on single multi-finger transistor at the point indicated in figure 5.20 at 80 mA/mm.

Figure 5.21: EMMI and electrical waveform comparisons of 6STTS device (on the left side) versus the series of single block multifinger transistor and 9.1 V discrete external Zener diode (ZD) (on the right side).

5.10 Summary

The analysis of 6STTS device revealed an inhomogeneous power dissipation in ESD operation with similar features as in the product device analyzed in chapter 2.

The investigation focused on the impact of the gate biasing condition (floating versus grounded) carried out for $PW = 100$ ns and 450 ns. This device was characterized by two operation modes visible by its voltage and current waveforms.

Thanks to TIM, we saw that in grounded gate configuration (i.e. DvsGS configuration) the power dissipation on the 1^{st} transistor was inhomogeneous for $PW = 100$ ns. A hot spot appeared on the R_G side during the second half of the pulse. Such hot spot was not clearly visible for floating gate condition (i.e. for DvsS configuration) for $PW = 100$ ns. However, additional measurements increasing the PW to 450 ns revealed that also the DvsS configuration suffered of inhomogeneous power dissipation showing an hot spot in the R_G side of the 1^{st} transistor. We thought that the gate bias condition could not be the only reason for the the observed hot spots. Nevertheless, the gate biasing plays a significant role: (1) it delays the parasitic BJT triggering and (2) it changes the extension of the triggered interested by PBJT triggering.

Besides the TIM investigation, the device was subjected to pulsed EMMI for the same PW used as in TIM ($PW = 100$ ns). EMMI confirmed the features detected by TIM for both probed configurations, in particular confirming that the 1^{st} block/transistor is the first to be interested by PBJT triggering in grounded gate stress configuration.

In order to understand if the B2B coupling was responsible of the inhomogenous power dissipation, we proposed an experiment to avoid any possible B2B effects. Using an external discrete Zener diode connected in series to a single 150 multi-finger MOSFET test structure and included in the TLP setup, we were able to reproduce the TLP-IV of the 6STTS in DvsGS configuration, emulating the electrical conditions occurring in the stacked device. Despite several trials also inducing a more stressful conditions on the multi-finger transistor, we did not obtain the localized EMMI light spot or any sign of inhomogeneous EMMI light patterns on its active multi-finger region as it was in the stacked device probed in grounded gate configuration. Such experiment suggested the B2B coupling to be the main phenomena involved in the inhomogeneous power dissipation in 6STTS.

Chapter 6

Conclusions and outlook

6.1 Conclusions

0.13 μm stacked MOSFET devices used for mobile phone antenna switch product were analyzed by ESD experiments and simulations. The investigation was carried out at wafer level and multiple experimental techniques were combined and employed to reveal complex interaction among the MOSFETs of the stacked device under ESD stress conditions. Several add-on SPICE models (to the standard BSIM model) are proposed to describe breakdown operation of the parasitic bipolar and interaction between MOSFETs in stacked device under ESD conditions.

The main results are summarized as follows:

Breakdown phenomena investigation on multi-finger transistors We investigated the PBJT triggering and drain breakdown phenomena on single MOSFET in function of L_G and number of finger.

A strong electrical coupling was observed among fingers in a MOSFET block. We observed breakdown voltage reduction with increase of the fingers in MOSFET blocks, which was attributed to the coupling effect between fingers. Another factor which affects breakdown voltage value under the transient and DC conditions of stress is the gate bias. A reduction of the breakdown voltage was experimentally observed with lower gate-source biasing. Dependence of the breakdown voltage on the gate bias was attributed to the GIDL effect, which is present in MOSFETs with sub micrometer technology. On the basis of these investigations, a simple empirical SPICE model was proposed for modeling the device behavior under ESD stress in breakdown condition).

Gate impact on power dissipation and failure on multi-finger single transistors We analyzed the failure at I_{t2} and the power dissipation varying the gate status (grounded versus floating). We found out that the device with floating gate undergoes thermally induced failure following the Wunsch-Bell relation for the dependence of the dissipated energy vs time duration. On the other hand, in grounded gate configuration, the GOX failure was limiting factor. It was observed that the failure energy is constant in wide range of the applied TLP pulses ($25-550\ ns$). Moreover, we found that V_{t2} did not change increasing the number of gate fingers for the gate grounded configuration supporting that the GOX is the failure root cause. We point out that none of the two tested configurations presented strong inhomogeneities in any TIM measurements, sign of very good and strong finger-to-finger coupling. Finally, failure analysis showed the junctions involved in the failure and revealed the failure locations: for floating gate, a central silicon melt in the correspondence of the drain and source wires, whereas on the gate connection corner of the multi-finger active region for the configuration in grounded gate.

Improvement of the optical TIM technique We found the multi-finger transistors to be optically anisotropic devices in respect to the TIM heterodyne signal and measured phase shift. Lower phase shift than the expected theoretical phase shift was measured. Proper TIM calibration measurements adding a half-wave plate in the TIM setup quantified the correction TIM coefficient and improved interpretation of the TIM results.. The coefficient was found to be different for ON- and OFF- state operations. Finally, numerical simulations using the Jones' matrix approach explained the reason of the anisotropic behavior encountered on these transistors with dense multi-finger gate structure to be similar to a wire grid polarizer.

Transient analysis of stacked MOSFETs under ESD stress For the first time, a detailed transient analysis of the RF stacked transistors under ESD stress was provided thanks to the combination of multiple investigation methods, such as TLP, EMMI and TIM measurements and SPICE simulations. The complex TLP waveforms revealed to be due to the time dependent behavior of each transistor of the stacked device. After the initial normal operation condition thanks to the gate-coupling effect enabling the channel current flow, the transistors were progressively entering into the breakdown operation one after the other starting from the first transistor where the stress was applied. Thanks to the model developed, the SPICE transient simulations showed that this was due to the sequential gate voltage decrease. The breakdown activation one block after the other led to have an unequal power distribution: highest at the first transistor as detected by TIM.

The study varying D_{B2B} revealed that this parameter affected considerably the measured power distribution thanks to block-to-block interactions via substrate and moreover also the I_{t2}. The devices with shorter D_{B2B} showed worst performance and more critical behavior.

The analysis followed with another device with 6 blocks similar to the product. This latter showed complex waveforms and a main localized hot spot in the first and hottest transistor. From results varying TLP pulse width and gate bias, we saw that this second parameter is involved in the delay of the formation of the hot spot but it cannot be considered the only reason of the critical inohomogeneous power dissipation distribution. Therefore, we analyzed a configuration aiming to emulate the stacked device but avoiding any B2B coupling. Nevertheless, the configuration given by the series of a single transistor and an external Zener diode was not able to produce any hot spot in any stress condition. This was interpreted as the sign that the B2B coupling is involved in the origin of the inhomogeneous power dissipation and the critical transient ESD behavior of bulk stacked transistors.

6.2 Outlook

Thanks to this work, the investigation on high-resistive bulk CMOS stacked devices started. However some points need to be deeper investigated.

The B2B coupling phenomenon in high-resistive substrate technology is really complex, since the multiple possible interactions occurring among fingers and blocks of the stacked devices. The B2B coupling impact on breakdown of a multi-finger transistor can be studied by dedicated single transistor multi-finger test structures placed at different distances, driving a device into breakdown and use the other as sort of collector terminal. This study would provide also ESD layout design guidelines for the next generation devices. The B2B coupling mitigation effect could be fulfilled in two ways: increasing the D_{B2B} or, in case of lack of space in the product chip, improving the isolation among transistors reengineering the silicon trench insulation.

The origin of the inhomogeneous power dissipation in 6 stacked transistor test structure device due to the B2B coupling was investigated by the “transistor + Zener diode” configuration. The experiment aiming to avoid any B2B confirmed that inhomogenous power dissipation on 1^{st} block was not possible to reproduce avoiding this mechanism. This did not exclude other secondary phenomena that might be involved in the complex behavior. This could also explain why the inhomogeneous power dissipation appeared only in the R_G side location and never in the other R_D side. One example could be that the distributed gate resistance network. We saw that this was involved on the failure in gate grounded configuration in section 3.8. This phenomenon can induces the progressive finger gate discharge starting from the finger close to R_G. However this is only an hypothesis and should be deeply investigated by dedicated test structures.

The ESD behavior of the provided test structures was not directly influenced by the bulk pad bias condition: ground or floating condition for the same TLP stress did not result into feature changes (e.g. TLP-IV shape, failure level, power distribution). It would be interesting to be able to probe some key substrate zones of the device without affecting the device behavior. Such investigation could be started designing proper test structures with multiple bulk contacts around the multi-finger active region and, if possible, also inside the active region in particular in the 1^{st} transistor. Such investigation can be complemented and enhanced by TCAD simulations. Additionally, such study could refine the the SPICE model used where one multi-finger transistor was represented by 1 equivalent BSIM transistor but inhomogenous power dissipation could not be reproduced. A distributed device model as in [96] could improve the accuracy of simulations in case of inhomogenous power dissipation as found for the 6STTS and shunt device from product. A complementary and deep investigation can be also carried out about the influence of the substrate voltage on the $V_{BD,DS}$. A wide knowledge of $V_{BD,DS}(V_{DS}, V_{GS}, V_{BS})$ is a must for a robust ESD self-protection approach.

We showed for the first time that TIM measurements were affected by heterodyne signal and phase shift anisotropy. The TIM response on high density multi-finger devices should be deeply investigated. In this work, we started the study for two well defined power conditions for two fixed V_{GS}, it would be interesting to expand this study to cover multiple power levels and for multiple gate conditions (in particular for $V_{GS} << 0\ V$) to find the variation of the introduced TIM coefficient. Additionally, the investigation should also be done varying layout parameters, like the multi-finger pitch above and below the wavelength diffraction limit to have a wider view of the impact of the TIM coefficients. In [107], the initial efforts on the investigation by optical simulations were presented.

Appendix A

Time constants for selected stacked configurations

The turn-on time for selected stacked configurations is reported in the following. As seen in chapter 1, the turn-on time is the starting point to design and choose the component parameters. For this reason, multiple stacked configuration were investigated and the turn-on time constant τ was derived.

The results are reported in table A.1. To derive the turn-on time constant, the stacked device drain and source must be connected to ground applying a step voltage to gate pad from $-1.5\ V$ to $1.5\ V$ with the shortest rise time possible, i.e. from the OFF-state bias condition to the ON-state bias condition. The stacked device can be simplified considering only the gate resistors and the total (OFF-state) gate capacitance C_G. Due to the fact that both drain and source in this turn-on configuration circuit are grounded, the role of the drain-source capacitor C_{DS} can be neglected as well as the drain resistors In this way, the Elmore formula [105] can be applied to the simplified circuit.

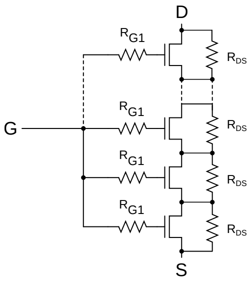
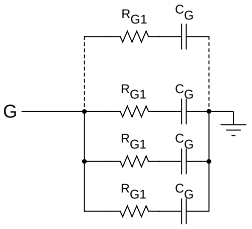
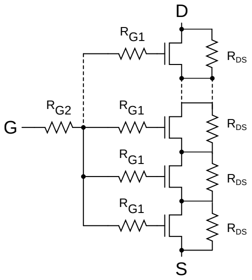
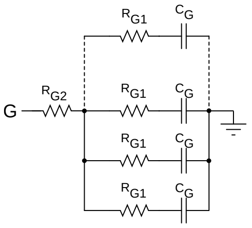
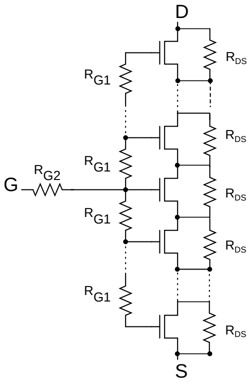
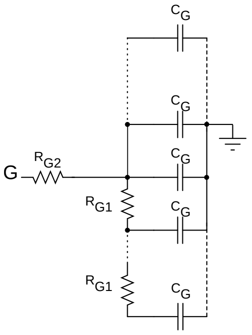
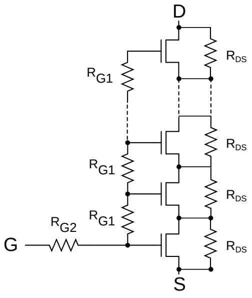
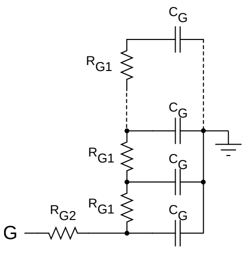
Circuit topology name	Circuit layout	Simplified equivalent circuit	Time constant τ
Parallel-gate			$R_{G1} \cdot C_G$
Star-gate			$(R_{G1} + NR_{G2}) \cdot C_G$
Series-gate central			$(NR_{G2} + \frac{N(N-1)}{2} R_{G1}) \cdot C_G$
Series-gate edge			$(\frac{N}{2} R_{G2} + \frac{(N-1)(N+1)}{2} R_{G1}) \cdot C_G$

Table A.1: Table containing the time constant for each stacked device topology. The column with simplified equivalent circuit refers to the simplified equivalent circuit used to calculate the turn on time using the Elmore formula approach.

Appendix B

Optical simulations of the beam polarization state using Jones matrix approach

The modified TIM setup (figure 3.19(a)) was studied by the Jones matrix theory in order to understand the effect of laser beam polarization on the multi-finger gate structure. By this mathematical approach, we were able to reproduce the reflectivity and phase shift features. The mathematical modeling and simulations are a joint work of Prof. Dionyz Pogany and Dr. Benedikt Schwarz presented in [22] .

The Jones' approach [11] treats the polarized light by a linear vector (Jones vector) and every optical element as 2×2 matrix (Jones matrix). Given an element described by a matrix T and input polarization vector $\mathbf{J_1}$, the resulting output vector $\mathbf{J_2}$ is

$$\mathbf{J_2} = T\mathbf{J_1}. \tag{B.1}$$

We described the linear polarized beam as $(E_0; 0)$ at the input of the polarizing beam splitter thanks to the action of the Faraday insulator (see it in figure 1.11a), where E_0 is the initial electrical field amplitude. During its optical path, the beam passes through the HWP, is reflected back from the sample and then again through the HWP and at the end again through the PBS. The final polarized vector is described to be

$$E_{ret}(\theta) = \widetilde{r}(\theta)E_0.$$

where the complex number containing information on reflectivity and phase is expressed by $\widetilde{r}(\theta)$. The Jones vector at the end of the path is obtained by

$$\begin{pmatrix} E_{ret}(\theta) \\ 0 \end{pmatrix} = S_{pol} \times S_{HWP}(-\theta) \times S_{sample} \times S_{HWP}(\theta) \times \begin{pmatrix} E_0 \\ 0 \end{pmatrix} \tag{B.2}$$

with

$$S_{pol} = \begin{pmatrix} 1 & 0 \\ 0 & 0 \end{pmatrix}$$

$$S_{HWP}(\theta) = \begin{pmatrix} cos(2\theta) & sin(2\theta) \\ sin(2\theta) & -cos(2\theta) \end{pmatrix}$$

and

$$S_{sample} = \begin{pmatrix} r_{\|}\, e^{i(\phi_{\|,0})+\Delta\phi_{\|}} & 0 \\ 0 & -r_{\perp}\, e^{i(\phi_{\perp,0}+\Delta\phi_{\perp})} \end{pmatrix}$$

where S_{pol}, S_{HWP} ans S_{sample} represent the matrices of PBS, HWP and the sample[1], respectively.

The contribution of the sample reflectivity in the S_{sample} matrix are taken into account by the polarization direction parallel and perpendicular to the gate width denoted as $r_{\|}$ and $r_{\perp}$, respectively. The phase shift is indicated by the sum of two terms, both taking into account the anisotropic response of the sample. The intrinsic constant phase shift term is indicated by $\phi_{\|}$ and $\phi_{\perp}$ for parallel and perpendicular contributions, respectively. The second term indicating the phase shift variation term due to thermal contribution is given by $\Delta\phi_{\|}$ (for parallel contribution) and by $\Delta\phi_{\perp}$ (for perpendicular contribution). In equation B.2, the rotation α (see figure 3.19(b)) is not omitted, since it only shifts the θ-axis.

From equation B.2, the total reflectivity r and the total phase response $\Delta\phi$ are obtained by

$$r(\theta) = |\widetilde{r}| \tag{B.3}$$

and

$$\Delta\phi(\theta) = arg[\widetilde{r}(\Delta\phi_{\|}, \Delta\phi_{\perp})] - arg[\widetilde{r}(\Delta\phi_{\|} = 0, \Delta\phi_{\perp} = 0)] \tag{B.4}$$

Note the second term in B.4 representing a reference phase having $\Delta\phi = 0$ for $\Delta\phi_{\|} = \Delta\phi_{\perp} = 0$.

Simulations of reflectivity using equation B.3 and phase shift from equation B.4 are reported in figures B.1(1) and B.1(2) for the case shown in figure 3.21a.

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[1] The minus sign is due to the fact that the DUT acts as mirror reflecting back the signal.

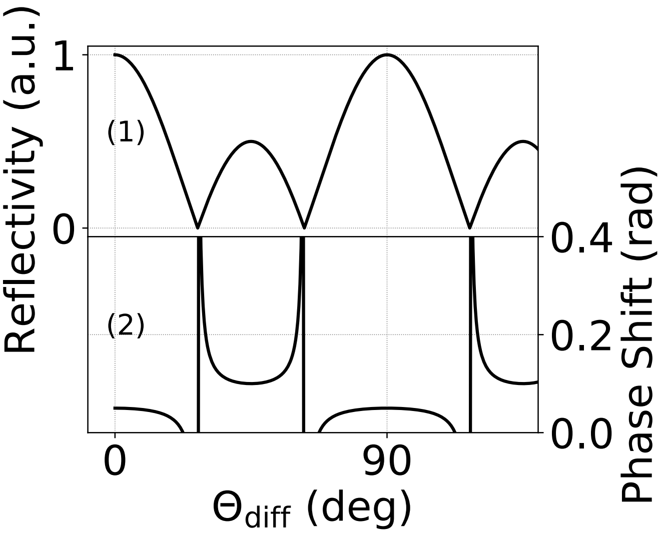


Figure B.1: Simulated (1) reflectivity and (2) phase shift for the condition of figure 3.21a. The parameters taken from experiment used to reproduce the measurements were: $r_{\|} = 1$, $r_{\perp} = 0.5$, $\Delta\phi_{\|} = 0.1\ rad$, $\Delta\phi_{\perp} = 0.05\ rad$. The fitting parameters are instead $\Delta\phi_{\|,0} = 0\ rad$ and $\Delta\phi_{\perp,0} = \pi\ rad$. Taken from [22].

Appendix C

Summary tables

Parameter		ST product	16STTS long D_{B2B}	16STTS short D_{B2B}	6STTS
number of blocks	N_B	8	16	16	6
total gate width	W_{TOT}	0.7 mm	6.96 mm	6.96 mm	0.98 mm
multipliers	M	1	4	4	1
gate finger width	W_F	7.3 μm	15.2 μm	15.2 μm	12.5 μm
gate finger length	L_G	0.13 μm	0.13 μm	0.13 μm	0.13 μm
gate oxide thickness	t_{ox}	2.2 nm	2.2 nm	2.2 nm	2.2 nm
gate resistor	R_G	400 $k\Omega$	400 $k\Omega$	400 $k\Omega$	400 $k\Omega$
drain resistor	R_D	400 $k\Omega$	400 $k\Omega$	400 $k\Omega$	400 $k\Omega$
block-to-block distance	D_{B2B}	2.1 μm	5.68 μm	1.84 μm	2.1 μm

Table C.1: Comparison of the main layout parameters for the investigated stacked devices. The "ST product" indicates the shunt transistor from product device analyzed in chapter 2; the devices named "16STTS long D_{B2B}" and "16STTS short D_{B2B}" are both analyzed and presented in chapter 4; then the device named "6STTS" is analyzed in chapter 5.

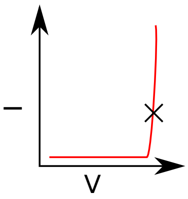
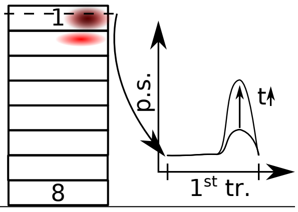
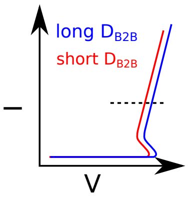
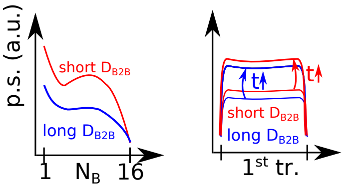
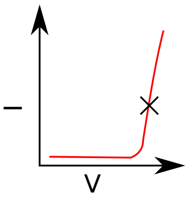
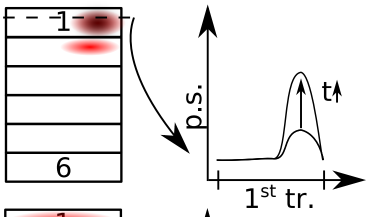
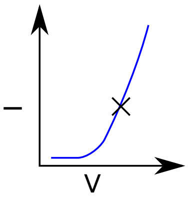
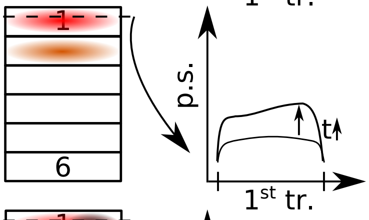
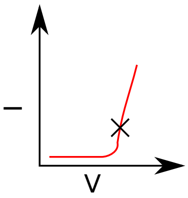
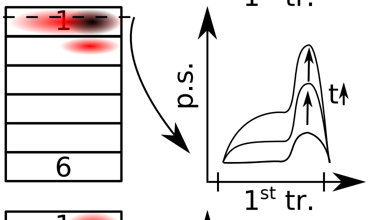
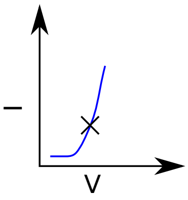
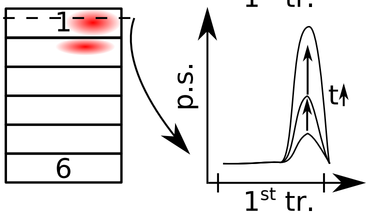
Device name	TLP stress configuration, PW	PW	TLP-IV, TIM location	Phase shift distribution
ST product	DvsGS	100 ns		
16STTS long $D_{B2B} = 5.68\ \mu m$ short $D_{B2B} = 1.84\ \mu m$	DvsGS	650 ns		
6STTS	DvsGS	100 ns		
6STTS	DvsS	100 ns		
6STTS	DvsGS	450 ns		
6STTS	DvsG	450 ns		

Table C.2: Table containing the main results of the studied stacked devices. Used abbreviation: “ST”for shunt transistor device; “16STTS” for 16 stacked test structure; “6STTS” for 6 stacked test structure; “PW”for TLP pulse width; “DvsGS” for TLP stress configuration positive pulses at drain versus gate and source grounded (bulk let floating); “DvsS” for TLP stress configuration positive pulses at drain versus source grounded (gate adn bulk let floating); “p.s.” for phase shift. In the phase shift distribution column, we showed a qualitative 2D phase shift distribution and the phase shift transient evolution for the 1^{st} transistor. However, for 16STTS devices we do not show any 2D power dissipation but rather a phase shift cross section since these devices do not show any inhomogeneous power dissipation inside the same block.

References

[1] A. Amerasekera, M.-C. Chang, C. Duvvury, and S. Ramaswamy. “Modeling MOS snapback and parasitic bipolar action for circuit-level ESD and high-current simulations”. *IEEE Circuits and Devices Magazine* **13** (1997) pp. 7–10. doi: 10.1109/101.583606.

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Curriculum vitae

Personal information

E-mail	matteo.rigato@tuwien.ac.at
Nationality	Italian
Birth	04.08.1987 in Padova, Italy

Education

05.2014–present	**Doctoral programme in Electrical Engineering**, *TU Wien*, Vienna, Austria. Institute of Solid State Electronics, Vienna, Austria
thesis	ESD experiments and simulations on RF CMOS switches
supervisor	AO. Prof. Dr. Dionyz Pogany
04.2014	**Master of Science in Electronic Engineering**, *University of Padua*, Padua, Italy.
03.2011	**Master of Science in Electronic Engineering**, *University of Padua*, Padua, Italy.

Professional career

02.2018–Present	**Test development engineer**, *Infineon Technologies Austria AG*, Graz, Austria. Automotive - Sensor and Control department
05.2014–01.2018	**Project assistant**, *TU Wien*, Wien, Austria. ESD investigation of RF stacked CMOS in collaboration with Infineon Technology AG, Munich, Germany
10.2013–04.2014	**Master's thesis internship**, *Microelectronics group of University of Padua*, Padua, Italy. Electrical characterization of Gallium Nitride (GaN) high electron mobility transistors (HEMTs) for high power switch application. Supervisor: Prof. Dr. Enrico Zanoni
09.2010–02.2011	**Bachelor's thesis internship**, *Luxor Laboratory INFM CNR*, Padua, Italy. Design of an UV plasma lamp to calibrate the spectrometer on board of Bepicolombo ESA space mission Supervisor: Dr. Maria Guglielmina Pelizzo