Diploma Thesis

Digital Correlator in 0.15µm CMOS

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Diplomarbeit

Digitaler Korrelator in 0,15µm CMOS

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von

Alexander Kuttner, BSc

Matr.Nr.: 0926914

unter der Anleitung von

Univ.Prof. Mag.rer.nat. Dr.techn. **Horst Zimmermann**

Dipl.Ing. Dr.techn. **Michael Hofbauer**, BSc

Institute of Electrodynamics, Microwave and Circuit Engineering
Technische Universität Wien
Karlsplatz 13, 1040 Wien, Österreich

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Abstract

This thesis is about the conception and design of a digital correlation circuit used for distance measurement experiments with single photon avalanche diodes (SPADs). SPADs are emerging devices that have an unmatched sensitivity as light detectors. The circuit is designed for a 0.15µm complementary metal oxide semiconductor (CMOS) process provided by LFoundry. In the beginning an overview of the fundamentals of SPAD devices and the different concepts of optical range measurements is given. Following, the functionality of the needed electronic circuit is specified. The fundamental steps and concepts needed, to implement and to simulate the digital circuit featuring that functionality using modern electric design automation (EDA) tools are explained. Subsequently, the design of the needed analog and asynchronous building blocks is discusses and combined with the digital parts to the whole application-specific integrated circuit (ASIC). Finally, results of post-layout simulations of the design are shown, which are used for verification and characterization before the ASIC enters manufacturing.

Kurzfassung

Diese Diplomarbeit beschäftigt sich mit der Konzeption und dem Entwurf einer digitalen Korrelatorschaltung für Entfernungsmessungen mit Einzelphotonen-Lawinendioden (SPADs). SPADs sind moderne Bauteile welche eine sonst unerreichte Empfindlichkeit als Licht Detektoren aufweisen. Die Schaltung ist für einen 0,15µm Komplementärsymmetrischer Metall-Oxid-Halbleiter (CMOS) Prozess von LFoundry entworfen. Zu Beginn wird ein Überblick über die Grundlagen von SPADs und die verschiedenen Konzepte der optischen Distanzmessung gegeben. Anschließend wird die Funktionalität der benötigten Schaltung spezifiziert. Die grundlegenden Schritte und Konzepte die benötigt werden um eine digitale Schaltung eben dieser Funktionalität mittels moderner Entwurfsautomatisierung elektronischer Systeme (EDA) Werkzeuge zu implementieren, werden erklärt. Dem anschließend wird die Entwicklung der benötigten analogen und asynchronen Schaltungsblöcke erklärt und alle Blöcke werden zur kompletten anwendungsspezifischen integrierten Schaltung (ASIC) kombiniert. Am Ende werden Ergebnisse der analogen post-Layout Simulation präsentiert, welche der Verifikation und Charakterisierung des ASICs dienen bevor dieser produziert wird.

Contents

List of Abbreviations

AP afterpulsing

APD avalanche photo diode

ASIC application-specific integrated circuit

CMOS complementary metal-oxide-semiconductor

EDA electronic design automation

EMCE Institute of Electrodynamics, Microwave and Circuit Engineering

ESD electro-static discharge

FPGA field programmable gate array

FSF frequency shifted feedback

HDL hardware description language

LVDS low voltage differential signaling

MOS metal-oxide-semiconductor

NDA non-disclosure agreement

PCB printed circuit board

PDE photon detection efficiency

pin-photodiode positive intrinsic negative diode

PnR place and route

PXI PCI eXtensions for Instrumentation (PCI stands for peripheral component interconnect)

RTL register-transfer level

SDC Synopsys design constraints

SDF standard delay format

SNR signal to noise ratio

SoC system on chip

SPAD single photon avalance diode

STA static timing analysis

STI shallow trench isolation

TCL tool command language

TOF time of flight

VHDL very high speed integrated circuit hardware description language

VLSI very large scale integration

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Chapter 1

Introduction

1.1 Problem - Motivation

The purpose of the research project "Interferometric distance sensing using APDs and SPADs" is to evaluate the usage of avalanche photo diodes (APDs) and single photon avalance diodes for distance measurements with a special, but not exclusive focus on interferometric ones. The reason for this is that interferometric methods of measurements can be as accurate as one thousandth part of the used wavelength. With increasing distances, a rising problem is the reduced intensity of the light that has to be measured. Traditionally used pin-photodiodes (i.e. diodes with an intrinsic layer between p and n regions) suffer from low intensity light levels because of electronic noise. With a decreasing signal level the signal to noise ratio (SNR) rises and limits the measurement range and the accuracy of the measurement. APDs and SPADs have a very high gain and therefore they are suited well to measure even small intensities of light; witch SPADs it is even possible to detect and count single photons which minimizes the impact of electronic noise. SPADs have gained a rising interest in the last years because of their features and ease of implementation in complementary metal-oxide-semiconductor (CMOS) technology. As a part of this project, different types of range measurements will be investigated using digital correlation between a pulsed light source and the reflected and detected light. Part of it is also the comparison between the fully-digital implemented circuit presented in this work and an analog assisted digital correlator developed by Mr. Michael Hauser BSc. Both resulting devices will be compared and evaluated in respect of chip area, accuracy, reliability and repeatability of measurement results. This comparison will not be presented within this thesis. Because the date of the tapeout is in January 2019, this thesis will only include simulation results and the measurement results of the created application-specific integrated circuit (ASIC) will be part of my dissertation and publications. The device will be designed and fabricated in a 1.8 Volt 150nm CMOS process provided by LFoundry. The process

includes digital standard cells, as well as analog metal-oxide-semiconductor (MOS)-devices that are configurable in parameters and up to 6 metal layers used to connect the devices. Since most of the information is provided under non-disclosure agreement (NDA), some figures of merits will be only given as an estimate, this counts especially for propagation delays of digital cells and standard cell layouts.

This chapter will give an overview of how SPADs are working and how they can be used. Additionally, there will be an explanation of the planned experiments for distance measurements and the used laser equipment. In the following, an outline of the digital design flow used for this development will be given. Finally, the steps needed to implement the digital design blocks into the complete ASIC are described.

1.2 SPAD - Single Photon Avalanche Diodes

APDs are highly sensitive optoelectronic devices. They utilize the photoelectric effect to detect light and to convert it to electricity. Their special feature is that they combine this with avalanche multiplication caused by impact ionization to achieve a high gain (up to over 100, there is a gain/bandwidth trade off).

1.2.1 Function

The mechanism used in APDs and SPADs to detect photons is the inner photoelectric effect. It describes that a photon can excite an electron from the valence band to the conduction band, into a bound but transportable state. The photon is required to have a minimum energy, dependent on the band gap of the used material [15, p.351f]. For silicon the minimum energy, and the associated wavelength, can be calculated, using the band-gap energy of 1.12eV (at 300K):

$$E = hf, f = \frac{c_0}{\lambda}$$
$$\lambda = \frac{hc_0}{E} = 1.12\mu m$$

Where E...is the Energy of the photon, h...is the Planck constant, c_0...is the speed of light in vacuum, and λ...the wavelength of the light.

This explains why silicon is transparent for infrared light with a wavelength of more than 1.12μm. For an electron-hole pair to be generated by a photon it needs to be absorbed in the material first. Because of this, the optical absorption constant α is very

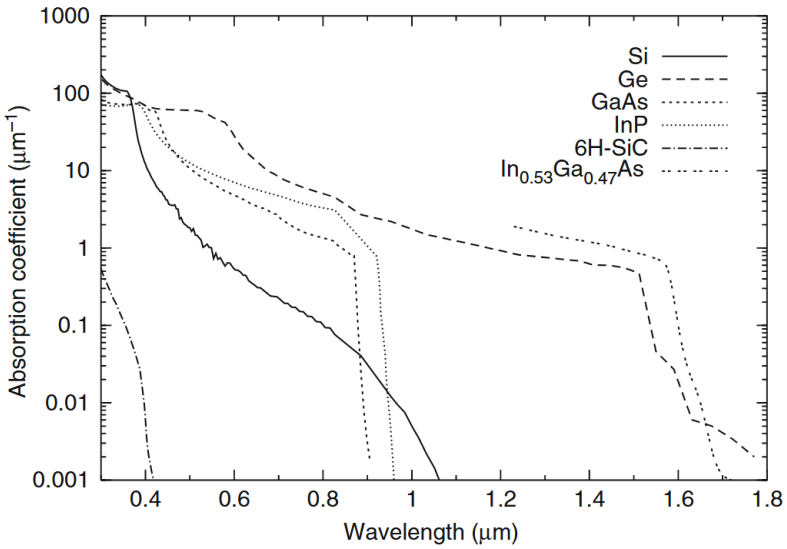


Fig. 1.1: Absorption coefficients of important semiconductor materials. [22, p.15]

important and has to be considered when designing optoelectronic devices, because it defines the penetration depth $\frac{1}{\alpha}$ using Lambert-Beer's law:

$$I(y) = I_0 e^{(-\alpha y)}$$

Where I_0...is the Intensity at the surface, α...is the optical absorption constant, and y...is the depth in the material.
In Figure 1.1 it can be seen that silicon has a worse incline of the absorption when increasing photon energy after the onset, especially for wavelengths longer than 500nm, compared to direct semiconductors like GaAs. Because of the much lower α values of silicon, a thicker absorption zone has to be considered when designing silicon photosensitive devices compared to a similar device using a direct semiconductor material. Nevertheless, it is the material with the most optimized processes and the biggest economic impact and devices operating in the GHz range can be produced [22]. Additional, it is possible to include SPADs in CMOS processes, creating fully integrated circuits containing the photo sensor and needed signal processing circuitry on one die while reducing the size and costs even further.

The second mechanism used in APDs and SPADs is the avalanche breakdown. This phenomenon is a form of electron multiplication that occurs in semiconducting and insulating devices: When a conducting electron is accelerated enough by an electric field so that its speed and therefore kinetic energy is high enough to knock other bound electrons free. By impact ionization it can create more free charge carriers and thereby increasing the current - an avalanche is started. This effect takes place in silicon

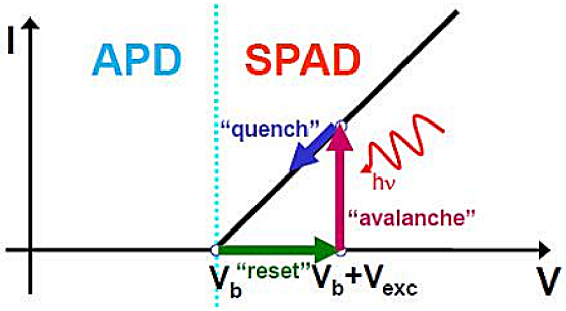


Fig. 1.2: I-V diagram of an SPAD. [2]

pn-diodes that are reverse biased: when a single electron, normally bound, breaks loose due to thermal excitation it gets accelerated and if the bias voltage exceeds a certain voltage, it creates an avalanche, that can only be stopped by reducing the reverse-bias voltage under that voltage. This phenomenon is called a breakdown and the associated bias voltage when this happens is the breakdown voltage.

While APDs are constructed in a way that this avalanche works as a first stage of amplification by having the reverse bias voltage lower than the breakdown voltage, SPADs are designed with a different idea in mind: by applying a reverse-bias voltage above the breakdown voltage, a single electron excited by the photoelectric effect will generate an avalanche in the device. This way of operation is called the Geiger mode. The consequence is that the bias voltage has to be reduced to a value lower than the breakdown voltage, to stop the avalanche and the current flowing (see Figure 1.2). This process is called quenching. There are multiple ways to do this and they will be explained in 1.2.3.

1.2.2 Layout

Figure 1.3 shows the cross-section of a thick SPAD (left) and thin SPAD (right). The thick SPAD features a thick absorption zone created by the p-epitaxy layer (because of this layer a special pin-photodiode-CMOS process is needed for creation) and a separate multiplication zone created by the reverse biased n++/p-well junction. Because of the different doping profiles the electrical field is not constant throughout the whole device and only in the multiplication zone the critical field strength needed for avalanche multiplication is present (higher than 3×10^5 V/cm [14]). The thin SPAD features a combined absorption/multiplication zone and it has no deep absorption layer which enables its manufacturing in a regular CMOS process. Due to the penetration depth of light in silicon (between 0.1μm and 10μm depending on the photon energy, in the typically used wavelength range) it is obvious that a thicker absorption zone can absorb

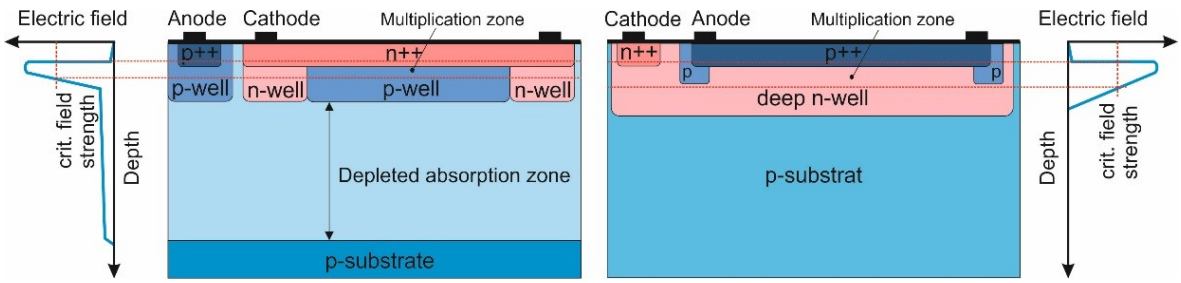


Fig. 1.3: Comparison of thick SPAD (left) and thin SPAD (right). The thin SPAD can be included in any CMOS process while the thick device needs a special process with an epitactic layer. [21, Suppl.Material]

more photons especially in near infrared, resulting in a higher photon detection efficiency (PDE).

While in the thick SPAD a charge carrier created inside the absorption zone has to pass the thick epitaxial layer first, a carrier created inside the p/n junction of the thin device is immediately accelerated by a high electric field, resulting in a faster response. But this only happens if the photon is absorbed in the p/n junction. If it is absorbed in the p-substrate below the junction, the carriers travel only by diffusion because of the negligible electric field there resulting in a much slower performance. In addition the capacitance of the thin SPAD is much higher, resulting in harder to meet requirements for the quenching circuit and making it slower (see section 1.2.3).

1.2.3 Quenching Methods

Passive Quenching

The simplest implementation of a quenching circuit is a passive one. It contains only one resistor that is connected in series to the photodiode (see Figure 1.5). The avalanche current will create a voltage drop on the high ohmic resistor. After the avalanche is quenched, the terminal voltage of the SPAD will again rise to the initial bias level, see Figure 1.4. Because of the capacitance of the device and the series resistor an exponential charging curve can be observed ($\tau = RC$, where τ is the time constant, R is the series resistance and C is the capacitance of the SPAD).

The big drawback of passive quenching is the slow recovery after a photon is detected, the measurements in Figure 1.4 shows a recovery time of 40µs. To use the full potential of SPADs, a better approach is needed: active quenching.

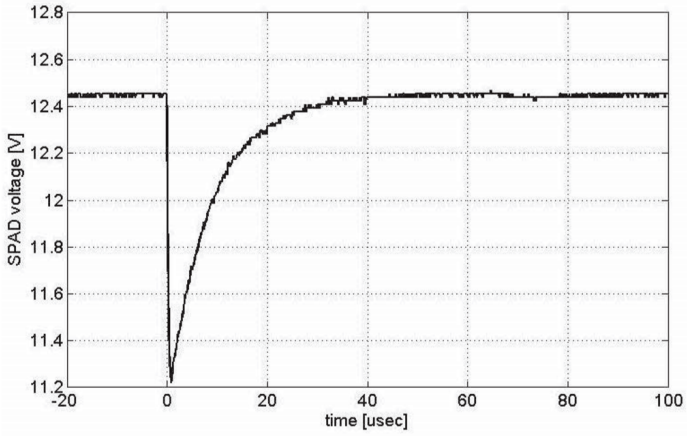


Fig. 1.4: Measurement of passive quenching. [16]

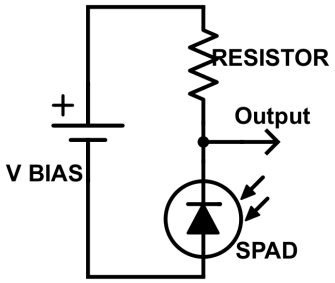


Fig. 1.5: Passive quenching schematic.

Active Quenching

The basic idea of active quenching is to sense the start of an avalanche and immediately react on it by forcing the quenching with a controlled bias source. This can be done for example with the use of a fast discriminator circuit that senses the onset of the avalanche current through a resistor. The discriminator produces a digital output pulse, synchronous with the detected photon and controls the bias source to reduce the bias voltage of the SPAD below breakdown voltage level. Using this technique, the quenching speed can be increased considerably, due to the possibility of higher currents because of the missing resistor. Figure 1.6 shows the typical active quenching operation of a SPAD. When V_{thr}, the threshold voltage of the discriminating circuit, is reached because of an starting avalanche event, the quenching circuit (after its propagation delay τ_{rc}) reduces the bias voltage to a level below the breakdown voltage (V_{BR}) to stop the avalanche. Until the quenching voltage (V_q) is reached deep traps (unwanted energy stated between the conduction and valency band) within the device are filled, this time can be be seen as τ_{trap}. Those trap energy states need to be discharged after the event, because they would result in afterpulsing as described in section 1.2.4. This is done by keeping the

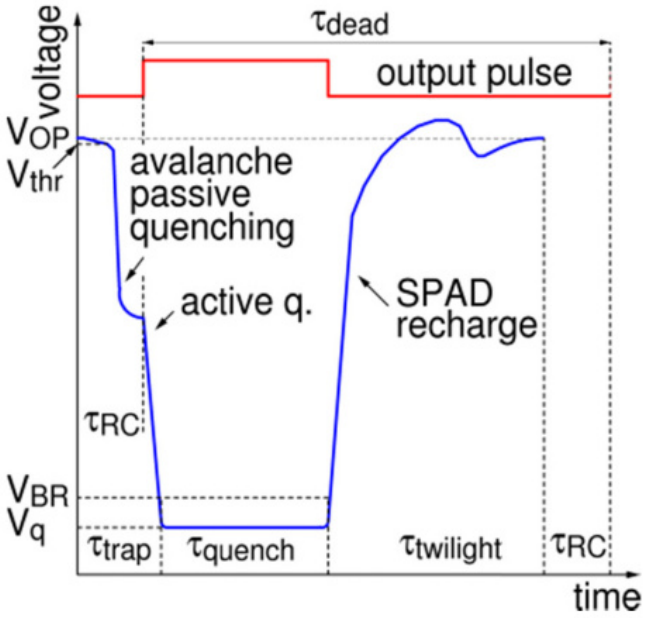


Fig. 1.6: Typical temporal evolution of the voltage across a SPAD during an active avalanche quenching event. [17]

bias voltage at V_q for a certain time. Only then the bias voltage can be brought up to a voltage higher than the breakdown voltage. The whole time needed for this process is commonly referred as the dead-time (τ_{dead}) of the SPAD-quenching circuit combination. With active quenching circuits dead-times of only a few nanoseconds are achievable. But in the nanosecond area, there is already a tradeoff concerning non idealities.

1.2.4 SPAD Characteristics

Photon Counting and Output Characteristics

Due to the high sensitivity of SPADs because of triggering an avalanche after a single photon is detected, they have to be used differently than e.g. pin-photodiodes when used as a sensor. For pin-photodiodes output current is proportional to the detected light. With increasing intensities of light, the avalanche in SPADs will be triggered more often since the photon current increases as well. This is restricted by the quenching speed though. At some point a saturation effect will occur (since quenching always needs some time). Not considering the saturation, the pulse rate at the output of the quenching circuit is proportional to the frequency of the avalanches and therefore to the intensity of light. Because of this, digital counting of the pulses is possible, resulting in a count per time interval proportional to the light intensity.

Non Idealities

Not only photon-generated carriers can trigger an avalanche, thermally-generated carriers can do so as well, even in complete darkness. Output pulses generated by this effect are called "dark counts". Those are one of the major contributors of noise when using the device as photon counter. Their characteristic can easily be measured in the absence of any photons and it is an important key figure of a device.

The second major contributor to noise is afterpulsing (AP). During an avalanche, charge carriers are generated in the pn-junction of the device and trap levels between valence and conduction band are occupied in a much greater density than it is possible due to the thermal-equilibrium distribution. After quenching, there is a probability (which is increased by the preceding avalanche, due to the higher density of those states) that one of those carriers gets enough energy to get released from the trap. Due to the electric field it will get accelerated and most likely trigger another avalanche. Traps are the result of various defects created during the manufacturing of the device, like the presence of unwanted ions (Na^{2+}, K^{+} or Cu^{2+}), lattice defects or interfaces like Si-SiO_2 [1]. In the worst case, one pulse can generate multiple following pulses due to afterpulsing.

The PDE under 100% may also cause noise, especially in low photon counting applications but due to the fact that during range measurements a lot of photons are detected, the effect will neutralize statistically.

Figures of Merits

For commercial available SPAD single photon detectors a study was made concerning the afterpulsing probability (AP) [20]. AP ranges from about 1% to 5% for the investigated detectors with a dead time between 20ns and 50ns. It should be noted that detectors of the same type and production date show a difference by up to one order of magnitude. Figure 1.7 shows the PDEs, dependence on wavelength, and their peak value for commercial available SPAD detectors, see Figure 1.7. Devices created in CMOS processes (light blue line in Figure 1.7) cannot achieve the performance of devices produced in special processes, but they can be easily integrated into a system on chip (SoC). To give an example, the τ-SPAD, featuring a PDE of 75%, is created in a special process, has a power dissipation of 10W during breakdown and a breakdown voltage of up to 500V. CMOS SPADs typically have a breakdown voltage in the range of 10 to 50V. Integration of SPADs in CMOS processes has not only the advantage of decreasing the cost and size of the detector but also puts the SPAD and quenching circuit right next to each other. If they are on separate dies, the bonding wires needed

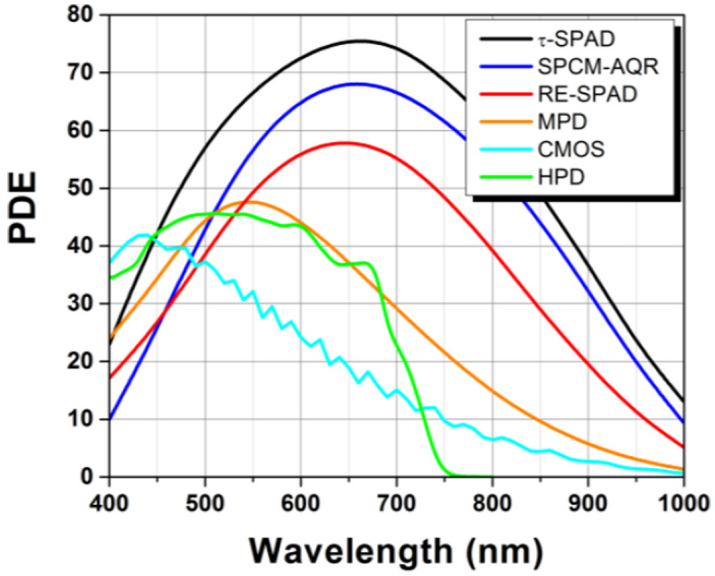


Fig. 1.7: PDE comparison of commercially available SPADs. [18]

Tab. 1.1: Important characteristics of the SPAD used in this project. [21]

Photon detection efficency	22%-36%
Afterpulsing (depending on dead time)	0.02% to 27%
Dark count rate	21k-35k counts s^{-1}@25°C
minimum dead time	7ns

for the interconnect between them add inductance and capacitance and decrease the speed of detector

Thick SPAD by EMCE at TU Wien

A single version of the the thick SPAD created by Institute of Electrodynamics, Microwave and Circuit Engineering (EMCE) that can be seen in Figure 1.8, will be used as detector for this application. In this case, the device is not split into four quadrants resulting in a single SPAD device. Its characteristics can be seen in table 1.1. It has to be noted that the SPADs compared in [20] and [12] were fine tuned to be used as single photon detectors and therefore their dead time is increased to yield better performances in the other characteristics.

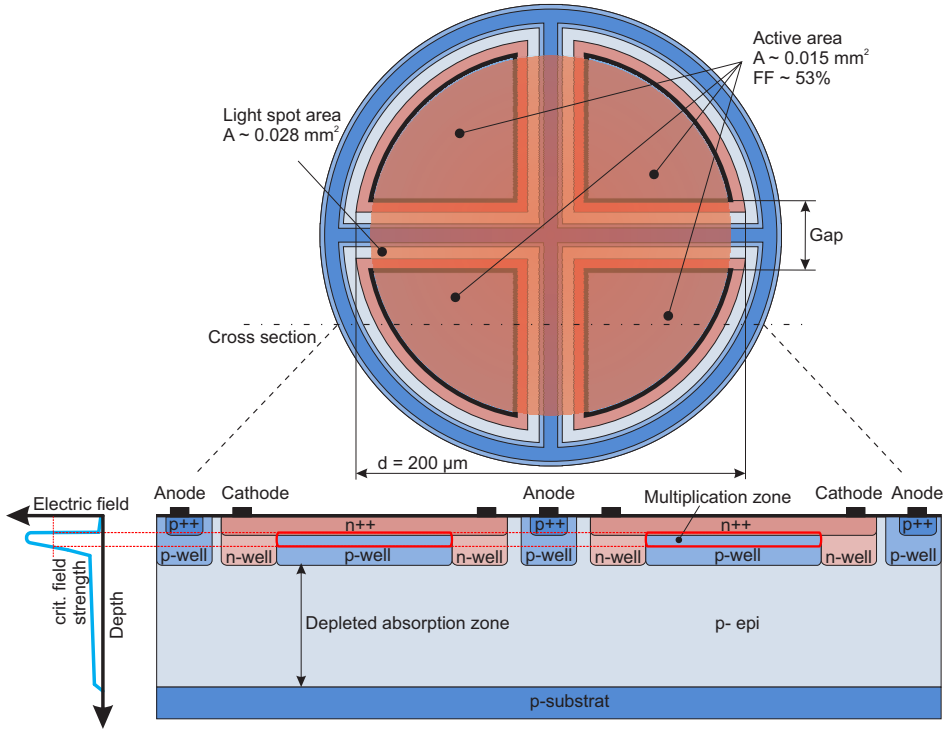


Fig. 1.8: Layout and cross-section through a thick quad-SPAD. A single version (with no intersections between the quarters) will be used for distance measurement experiments. [21]

1.3 Methods of Range Measurement

1.3.1 Time of Flight - TOF

The time of flight (TOF) distance measurement principle uses the measurement of the absolute time that a light pulse needs to travel from a light source to a targeted object and back to a detector to measure the distance of the object. There are two types of TOF light modulation techniques:

- *Pulsed-modulation* measures the time of flight directly. This allows long range measurements, but short distances are hard to measure since the speed of light is 0.3 meters per nanosecond and short distances require very accurate time measurements. This type of modulation requires light pulses with a fast rise-time and high optical power. The distance d can be calculated by $d = \frac{1}{2} * c\tau$(c is the speed of light and τ is the time of flight). Because of this the accuracy is proportional to the accuracy of time measurement (a distance of 1 cm correlates to a time of 67 ps).

- *Continuous-wave-modulation* measures the phase difference between a amplitude modulated sent and received signal. Cross-correlation between sent and received

signals allows a phase measurement. The measured phase difference between the two signals is related directly to the distance, when the frequency of the wave-modulation is known. The relationship between phase shift and time of flight is $\phi = 2\pi f\tau$ (ϕ...measured phase shift, f...modulation frequency, τ...time of flight). The drawback of this method is that the phase shift is periodic, resulting in an unambiguousness range corresponding to phase shift of maximum 2π.

Phase difference calculation through cross-correlation

Since sensing the phase difference between two high frequency signals is very hard if performed in the time domain, it is possible to calculate it using the correlation between two signals. In the following the so-called *4-Bucket method* will be explained:
Emitted signal:

$$e(t) = a * cos(2\pi ft)$$

Received signal:

$$r(t) = A * cos(2\pi f(t - \tau_{timeofflight})) + B$$

Where t...is the time, f...is the frequency of the light modulation, $t - \tau_{timeofflight}$...is the time that a photon needs to travel from the emitter to the measurement object and back to the receiver, a and A are the maximum amplitudes of the emitted respective received signal, and B is the offset caused by ambient light. Continuous-wave-modulation is used here and the amplitude of the emitted (and therefore also the amplitude of the received light) is modulated with a sine wave.
Cross-correlation between the signals is:

$$C(x) = \lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{T/2} e(t)r(t+x)dt$$

The x is a phase shift, introduced by the round trip of the light, the phase modulation.

The solution of the equation is:

$$C(\psi) = \frac{aA}{2} cos(\underbrace{2\pi f\tau}_{\phi} + \underbrace{2\pi fx}_{\psi})$$

Where ϕ is the phase difference,and a and A are the amplitudes of the emitted and received light. To calculate the phase difference, multiple pairs of ψ and C are needed. Figure 1.9 shows the 4-Bucket method. Using four different signals with a phase shift of 90°between them, results in the same number of ψ, C pairs, making it possible to

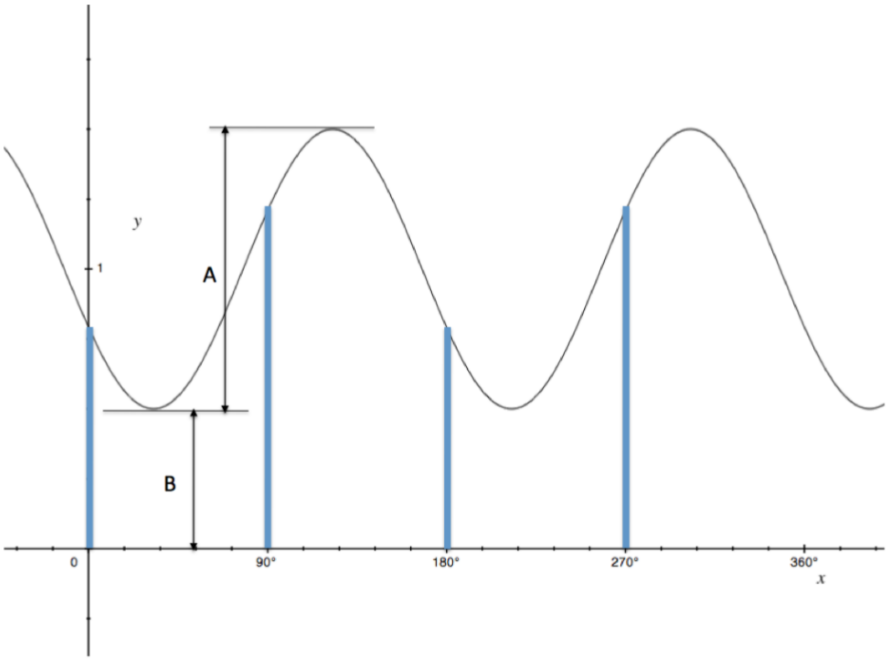


Fig. 1.9: 4-Bucket method for phase difference measurement and calculation through cross-correlation. [6]

calculate the values of A, B and ϕ (it has to be noted that only ϕ is of importance for distance sensing) [6]:

$$\phi = 2\pi f\tau = arctan(\frac{C(270°) - C(90°)}{C(0°) - C(90°)})$$

$$A = \frac{1}{2a}\sqrt{(C(270°) - C(90°))^2 + (C(0°) - C(90°))^2}$$

$$B = \frac{1}{4}(C(0°) + C(90°) + C(180°) + C(270°))$$

Since ϕ can only range between 0 and 2π (this is called phase wrapping) only a limited depth can be measured:

- *Depth*: $d = \frac{1}{2}c\tau = \frac{c}{2f}\frac{\phi}{2\pi}$
- *Minimum depth*: $d_{min} = 0(\phi = 0)$
- *Maximum depth*: $d_{max} = \frac{c}{2f}(\phi = 2\pi)$

For a frequency of $f = 30MHz$ this results in a maximum distance d_{max} of 5 meters. If the object is further away, phase wrapping occurs: a distance measurement of 6m has the same result as a measurement of 1m.

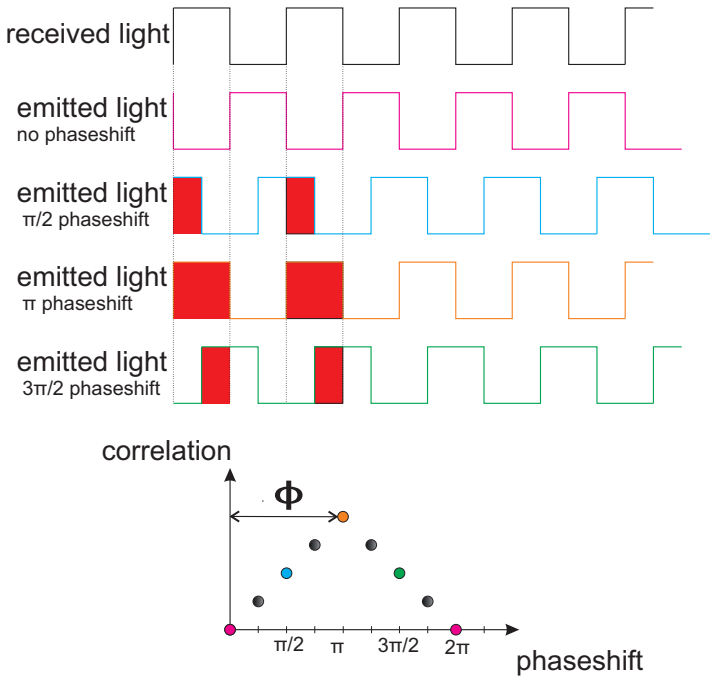


Fig. 1.10: Correlation triangle of two square waves.

Correlation Triangle with x Steps

Another way to calculate the phase difference between the sent and received light is to perform cross-correlation with more phase steps: When correlating the received light with the send modulation signal and stepwise shifting it e.g. 8 time with a phase difference of $\frac{2\pi}{8}$ per step, one of the calculations will yield a maximum correlation. The maximum will be close to the phase at which the traveling light was shifted by the trip. This can be seen in Figure 1.10 where the received light is shown in black. The pink signal is the modulation signal for the light source. It is then phase shifted in 4 steps (for an easier understanding). The colored points in the diagram belong to the signals in the corresponding color. The grey points show the measurement points that would be obtained when performing 8 different correlation measurements. In real measurements the exact phase shift will not be exactly at one of the phase shifts, but it still can be calculated by performing fast fourier transformation on the measurements points. The phase shift of the 0^{th} order wave is very close the phase shift ϕ we are looking for.

Because the sent signal is modulated with a certain frequency, another characteristic of the cross-correlation operation is used to suppress background light: The cross-correlation between signals of different frequency is zero. This feature is also used in an analog lock-in amplifier. This frequency suppressing effect is strong to enough enable measurements in direct sunlight because of the strong damping of unwanted frequency components.

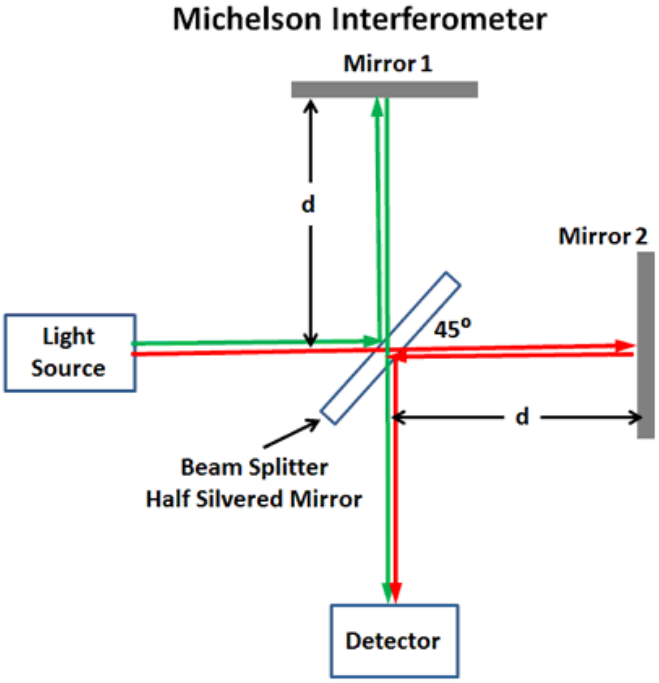


Fig. 1.11: Michelson interferometer: a differences in the distances of the different optical paths results in interference at the detector. [11]

1.3.2 Interferometric Measurements

Interferometers can be used to measure minimal range differences by exploiting the phenomenon of interference. For different length differences between the reference and measurement arm of the device, different interference effects will occur at the detector. Using a static light source the measurement will have a periodic characteristic with a period corresponding to the wavelength λ of the used light, making it impossible to measure an absolute range. This can be achieved by varying the wavelength of the used light: When a length difference is present, altering the wavelength will result in a change of the output signal measured at the detector. With a constant sweep over the wavelength a periodic change between constructive and deconstructive interference will occur at the output. This period depends on the λ change rate and on the measured distance. This can be used to increase the measurement range, especially if the length of the reference arm is increased. A higher coherence length is needed then. Measuring frequencies is often complicated because of the need of large counters running on a high frequency. This can be simplified for this use-case by not altering the laser wavelength automatically, but to alter it stepwise and measure the output of the Interferometer. It is possible to reconstruct the sine waveform that corresponds to these measurement

points by computation and the frequency can be obtained without the need of frequency counters.

1.3.3 Frequency Shifted Feedback Laser

Lasers are optoelectronic devices used to transform electrical energy to light. They are characterized by the fact that they are using optical amplification of photons created by stimulated emission and the coherence of their produced light, meaning that the produced light is able to perform stationary interference. This is especially important for interferometric measurements, because they require interference effects to occur. While regular lasers have modes characteristic for the used laser medium, a frequency shifted feedback (FSF) laser behaves differently: An acousto-optic modulator in the cavity of the laser is used to shift the frequency making it possible to fine tune the wavelength of the light present in it. The acousto-optical mudulator is typically created by a glass such as SiO_2 or TeO_2. By inducing an acoustic wave, the laser light gets diffracted, because the k-vectors that are proportional to the frequencies of the waves, add up. In regular lasers the round trip length of the cavity has to be an integer multiple of the wavelength, resulting in feedback at a discrete frequency. In contrary to that, the light waves in an FSF laser get frequency shifted with each round trip making it not possible to give feedback to itself. Because of this the output spectrum is not discrete but continuously shifting. A FSF laser built by Hofbauer et al. [5] at EMCE from TU Vienna shows a output spectrum sweep of roughly 2nm. Because of this the FSF-laser is perfectly suited for interferometric distance measurements because the output already includes a frequency sweep, yielding a constantly changing interference pattern at the output.

1.4 Design Approach

To create the circuit needed for range measurements, it is planned to use the VLSI design flow (see Figure 3.1), since most functional blocks are digital. The needed steps will be explained in the following chapters. Those functional blocks will be integrated into the full design by hand. First step of the design process is the specification of the device, which will be explained and presented in the next chapter.

Chapter 2

Specification and High Level Design Considerations

2.1 What is a Specification?

At the start of a digital design process a specification is needed. It is very important to have a description of the to be designed device or system because every other step is based upon the preceding one and a flaw early in the design flow cannot be found in the later stages. The specification is defined as *"an explicit set of requirements to be satisfied by a material, product, system, or service."* [9] Every future produced work will be compared to it and has to satisfy it.

2.2 The Project

The goal of this work is to specify and design a digital correlator used for ranged measurements with SPADs. The needed quenching circuit that will be on the same ASIC is designed by Alija Dervic MSc., while the SPAD will be off-chip. The device will be manufactured by LFoundry using a 150nm CMOS process.

2.2.1 SPAD Device

The SPAD that will be used has been developed by EMCE at TU Vienna and has been used and tested in various applications [21]. Its performance characteristics can be seen in section 1.2.4

2.2.2 Functionality

1-bit correlation between the digital output pulses of the SPAD quencher and the supplied correlation signal can be performed using an up/down counter. The output pulses created by the SPAD will trigger the counting, while the signal to which it has to be correlated controls if up or down counting is performed. The SPAD active quencher combination that will be used for measurements, will have a dead time of about 7 ns between output pulses. A better performance should be achieved, because this device should work when using faster SPADs devices as well, since the long dead time is derived from the off-chip diode. When using an on-chip SPAD, the quenching circuit should achieve deadtimes down to 2.5 nanoseconds. The low speed of the SPAD quencher combination results from the fact that the photosensitive device is not on the same die as the quenching circuit: because of the added capacitances (created by bonding pads and wires) a bigger load has to be charged, resulting in a slower operation.

Since longer correlation measurements have a higher accuracy and to be able to investigate the impact of the measurement time for range measurements on the accuracy, a big dynamic range is needed. To enable the circuit to be used for measurement durations up to half a second, with a counting frequency up to 400 Mhz, a depth of 27 bits is needed. Since negative values should be available as well, signed 2-complement arithmetic is used, and therefore an additional bit is necessary, resulting in a depth of 28 bits.

2.2.3 Asynchronous vs. Synchronous Design

Since an asynchronous counter needs less gates, resulting in a smaller layout, careful consideration had to be taken when choosing how the counter should work. The time until the output of an asynchronous counter is stable can be calculated by $t_{stable} = (t_{propagationFlipFlop} + t_{propagationLogic}) * n_{size}$. Since the requirement was a depth of 28 bit, this would result in a settling time of over 10 nanoseconds, with the characteristics of the logic cells taken from the process databook. A synchronous counter would have a settling time of just the propagation delay of the flip flop, which is in the area of 100 to 200 picoseconds.

Timing Considerations

Since the output pulses of the SPAD are asynchronous to the correlation signal an emerging problem is to satisfy setup and hold requirements of the flip flops (since the data input will change when switching from up to down counting). If, in the worst

case, a pulse occurs at roughly the same time as the correlation signal is changing, the behavior of the circuit cannot be known, since setup and hold times of the flip-flops have to be adhered to. A violation of those can result in a metastable state (the state of the flip-flop cannot be known), which has to be avoided at all costs! This settling time would have to be adhered to at every change of the correlation signal. For a correlation frequency of 10 Mhz an asynchrounous counter would have to be stopped for 10% of the measurement time (it has to wait for t_{stable} before a change in counting direction can be performed) resulting in an error of the same size, making it not usable for this device.

For a synchronous design the solution to this would be to stop the counter before changing counting direction. This would result in a complicated operation procedure:

- *UP-counting-state*
- Disable counting
- Change counting state
- Wait for setup time (about 100ps)
- Enter *DOWN-counting-state*

During the disabled state, all pulses created by the SPAD would be lost. Another possibility is to synchronize the asynchronous signals to a known constant clock, which has to be at least twice as fast as the fastest signal. Since the circuit should work up to a speed of 400 MHz, a clock of at least 800 MHz would be needed. This would result in the need of a clock source and would introduce an additional frequency component that would manipulate the measurement.

Because of that, a special counter combination was created, using two parallel counters, one counting pulses during the first half of the correlation period (the UP-counts), the other one counting pulses during the second one (the DOWN-counts). When subtracting the second counter-value from the first, the result can be calculated. To increase the dynamic range of the circuit, a fine/coarse counter structure was introduced. The fine counters work in parallel, while the single coarse counter is responsible for counting the overflows, one positive, the second one negative. The special part of this structure, is that each counter only needs a single input: the clock pulse (additional to the reset of course). However, a circuit to gate the clock-pulses to the correct counter is needed. To get to the final measurement result, the contents off the different counters have to be added together (the DOWN fine counter has to be subtracted).

Fig. 2.1: PXI-System from National Instruments. [8]

2.2.4 Readout

Pads need a big amount of area (65μm $\times$200μm) and having a parallel 28-bit output was no option for this project, since the required chip area would be to much. Because of this, a parallel-serial converter is needed. This can easily be achieved with a shift register, needing only three digital pads: the data output, a clock input and a control input, that controls loading and shifting operation. Since the measurement result is only needed at the end of the measurement, the final value is only calculated when loading the shift register. This results in a smaller required chip area, since the readout can performed at a lower frequency. The ASIC will be interfaced using a National Instruments PCI eXtensions for Instrumentation (PCI stands for peripheral component interconnect) (PXI) high performance measurement system, containing an field programmable gate array (FPGA) and a 1 Ghz, 20 channel digital input/output extension card. The PXI system is a high performance measurement and automatisation system that can be extended using various expansion cards, which are interfaced over the high speed PCI bus. In this use-case a FPGA extension is used together with a digital I/O module that enables high speed, clock precise, control and data aquisition of the designed ASIC. Using Labview software, the system is suitable for high speed data transfer, controlling the laser and the ASIC while being reconfigurable and suitable for different types of range measurements. While the digital IO expansion card features low voltage differential signaling (LVDS) communication channels, the designed ASIC will only need to have single ended inputs and outputs to reduce the required number of pads. The conversion from single ended to differential signaling will be performed on the printed circuit board (PCB) holding the ASIC. Figure 2.2 shows the complete setup for TOF measurements.

Needed Inputs/Outputs

To perform the required function following communication ports are needed:

- SPAD pulse input

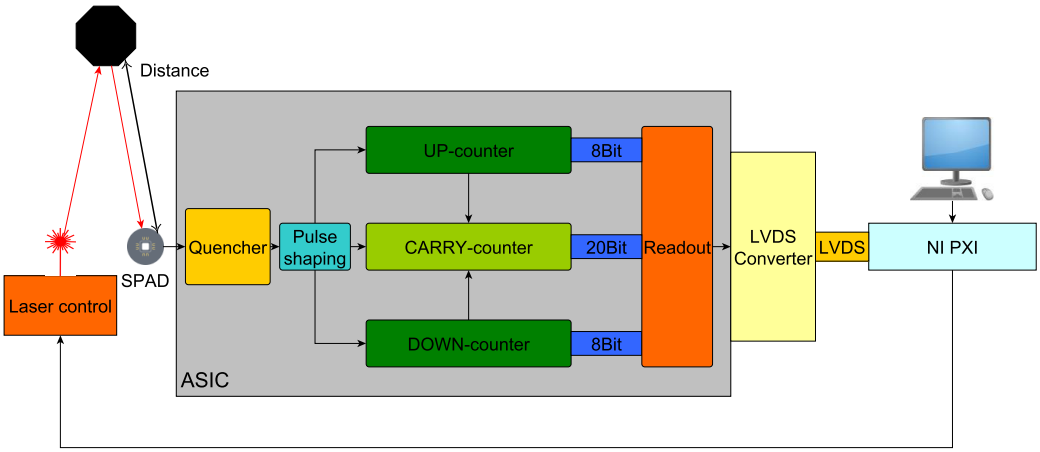


Fig. 2.2: Whole measurement system for time-of-flight experiments including the building blocks of the device.

- Correlation signal
- Enable signal to control counting period
- Reset signal
- Readout of measurement result

Implementation of those ports will be explained in the following chapter.

2.2.5 Specification Document

The finished specification document can be found at the end of this document.

Chapter 3

Digital Design

The digital design flow described in section 1.4 was done using electronic design automation (EDA)-software from Cadence Design systems. Figure 3.1 shows the needed steps and the corresponding software. In this chapter I will explain the different steps in depth.

3.1 Block Design - High Level Design

The first step of the actual design process is about dividing the whole functionality into different functional blocks. Those blocks can be seen in Figure 2.2.

Pulse-shaping

The pulse shaper is used to create the needed clock pulses for the digital blocks. Since it is not created using the VLSI flow, a in-depth explanation can be found in section 4.1.

Fine counters

The 8 bit UP counter and the DOWN counter are created the same way, their different purpose is created by clocking them differently and using their data differently. Both are designed as synchronous 8-bit counters, with a clock and a reset input. Their output is a parallel 8-bit data output and the corresponding carry bit.

Coarse counter

The 20 bit coarse-counter is used to count the overflows occurring in the fine counters: it gets a clock impulse every time when either the UP counter or the DOWN counter get one. When one of the carry-bits is active, the coarse-counter will count in the corresponding direction. When both are active no counting is performed. Care has to be taken when one of the fine counters is stopped while its carry bit is active: if

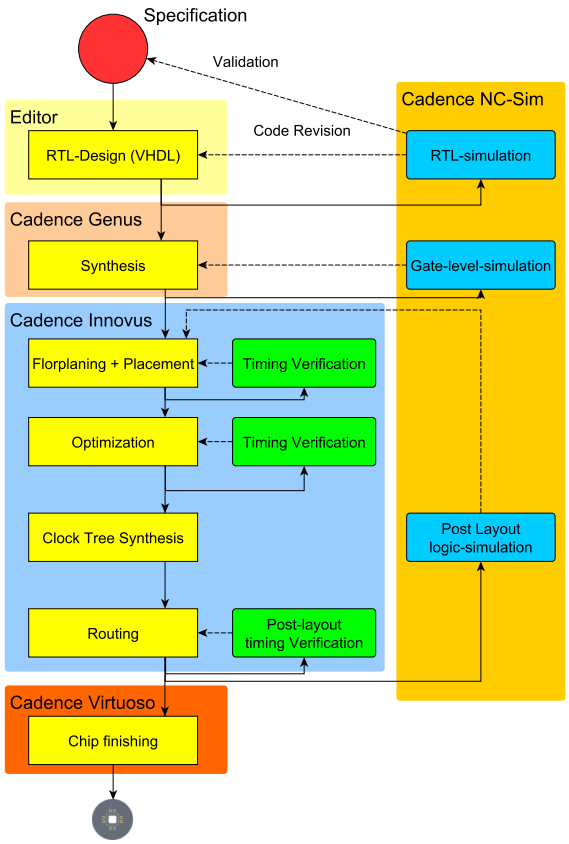


Fig. 3.1: VLSI design flow including the used tools.

the coarse-counter is clocked, it would result in continuous unwanted COARSE counts. Since the fine counters do not get more clock inputs after their counting period, it is impossible to clear the carry bit after one SPAD pulse. Therefore a latch has to be implemented to assure that each overflow only creates one count (see 4.2). The inputs of the coarse counter are a clock, a low active reset and the carry bits of both the UP and DOWN fine counters. Its output is a 20 bit parallel bus. No overflow prevention or signaling is planned because of the big dynamic range.

Readout

When the measurement and counting is finished, the final value has to be calculated by:

$$value = value_{COARSE} * 2^8 (= 256) + value_{UP} - value_{DOWN}$$

The multiplication by 256 is the same as a left shift by 8 bits and is needed because coarse count corresponds to one overflow of the 8 bit fine counters. The result has to be stored inside a shift-register which is used to transfer the result to the PXI system.

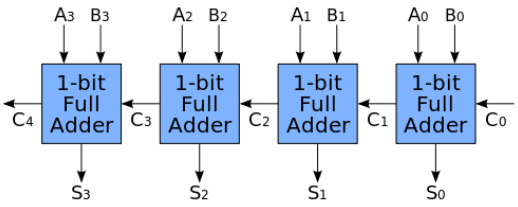


Fig. 3.2: Ripple-carry adder. [18]

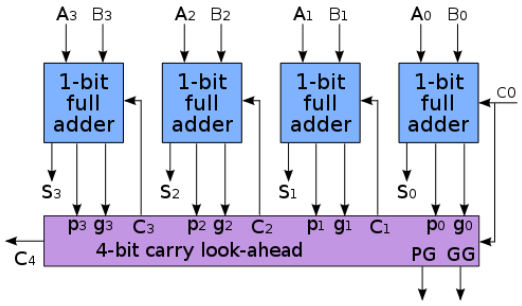


Fig. 3.3: Carry-lookahead adder. [19]

Additional a shift-clock and a control bit (Shifting operation/load) is needed. Since the readout procedure is only performed once every measurement cycle, a ripple-carry adder could be used, but to increase the speed of the design a carry lookahead adder is used. A ripple-carry adder is made out of several full adders corresponding to the number of bits the block has to compute (see Figure 3.2). The carry output of each full adder is connected to the carry input of the next full adder. When calculating the final value, the carry signal has to propagate through all full adders starting with the least significant bit. On the parallel output the final value stabilizes ("ripples") from the least significant bit to the most significant bit. The time needed is $t_{STABLE} = n_{numberofbits} * t_{PropagationDelayFULLADDER}$, resulting in a way longer computational time. The full adder cells from the LFounrdy process have a propagation delay of about 400ps from the carry input to the output, resulting in a computational time of about 12ns. Since the readout shall be performed with 100MHz, the ripple-carry adder is not fast enough.

In comparison a carry lookahead adder has a an additional block of combinational logic that calculates the carry input signal for each full adder(see Figure 3.3). Because of this, the final adder is way faster, but needs more logic cells and chip area. Readout of the 28 bit value will be performed using a shift register because in contrary to a parallel data output this saves a lot of pads and therefore chip area. The drawback is the slower speed, needing 29 clock cycles. This is no disadvantage is this case because a new measurement needs a lot more time than the readout. In sum, the readout block needs the following inputs and one output:

- Input 8 bit UP counter + carry
- Input 8 bit DOWN counter + carry
- Input 20 bit COARSE counter
- Clock input for loading and shifting operation

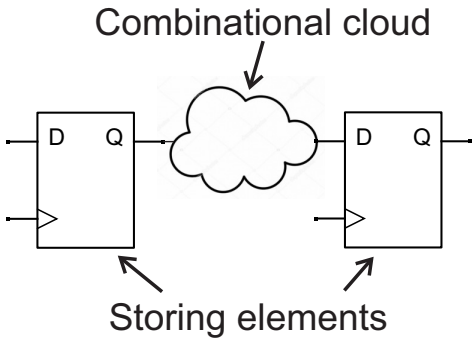


Fig. 3.4: RTL design containing storing elements and combination logic.

- Control bit to switch between shifting and loading
- 1 bit data output

3.2 HDL Design - Low Level Design

A hardware description language (HDL) is a specialized coding language, used to describe the behavior and structure of electronic systems. It enables engineers to create a formal, precise description of an electronic circuit. A subset of this language is synthesizeable, which means, if a module is described by it exclusively, the module can be turned into a specific combination of physical electronic components that behave as described. This is mostly used for clocked digital systems. A big difference to regular programming languages is that HDLs introduce time. This enables simulation of the described systems making verification and validation possible. The time domain is part of the non-synthesizeable set of these languages and is used exclusively for simulation. Today the most used languages are Verilog and very high speed integrated circuit hardware description language (VHDL). Nowadays, digital circuits are mostly implemented by using RTL modeling, which describes storing elements (flip-flops), the data flow between them and logical or arithmetic operations executed on them (often called the "combinational cloud") as depicted in Figure 3.4. Typically this results in storing registers and combinational circuits.

The functionality described for the different blocks was used to create VHDL design entities for each of the blocks. To explain some of the fundamentals of VHDL, the code of the fine counters is shown (the comments, shown in mint color, are not the actual comments, but are used to explain the code):

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;--IEEE library for logic operations
```

```
use IEEE.NUMERIC_STD.ALL;--IEEE library for arithmetic calculations

entity f_counter is --the VHDL entity defines what ports the module has
    Port ( iCLK : in STD_LOGIC; --STD_LOGIC describes logic values
           iRESET : in STD_LOGIC;
           oCARRY : out STD_LOGIC;
           ovDATA8 : out STD_LOGIC_VECTOR (7 downto 0));
           --STD_LOGIC_VECTOR : 8 bits concatenated to a vector
end f_counter;

architecture Behavioral of f_counter is
--the architecture describes the inner workings of the module
signal vuCOUNTERVALUE : unsigned (7 downto 0) := ( others => '0');
--the the signal (a manipulatable variable) is of the type UNSIGNED
--a STD_LOGIC_VECOR cannot be used for calculations
--UNSIGNED can be used

begin
count: process (iRESET, iCLK)
--a process is allways started when one of the signals from the
--sensitivity list is changed (iRESET and iCLK in this case)
begin
    if (iRESET = '0') then --asynchronous Reset, low active
        vuCOUNTERVALUE <= (others => '0');
        oCARRY <= '0';--when a reset is performed the countervalue
        --and the carry are set to '0'
    elsif (rising_edge(iCLK) ) then --trigger on positive clock edge
        if (vuCOUNTERVALUE = 255) then --when the counter is at the
        --maximum value, set it to zero and assign carry bit
            vuCOUNTERVALUE <= (others => '0');
            oCARRY <= '1';
        else
            vuCOUNTERVALUE <= vuCOUNTERVALUE + 1;
            --when the counter is not at the maximum value, add one
            --to it at every positive clock edge
            oCARRY <= '0';
        end if;
    end if;
end process count;
```

```
ovDATA8 <= std_logic_vector(vuCOUNTERVALUE);
--cast UNSIGNED to std_logic_vector output
--the output is connected to the register holding the value
end Behavioral;
```

3.3 Simulation: Verification - Validation

Due to the explicit functional description of a system in a HDL and the inclusion of time, it is possible to simulate the behavior of the system with modeled input parameters. This is needed to perform both verification and validation. Both of those steps are very important and have to be distinguished from each other:

- *"Verification. The evaluation of whether or not a product, service, or system complies with a regulation, requirement, specification, or imposed condition. It is often an internal process."* [7]
- *"Validation. The assurance that a product, service, or system meets the needs of the customer and other identified stakeholders. It often involves acceptance and suitability with external customers."*[7]

Verification proves that a work is of high quality, but doesn't ensure that the object is useful. Validation in contrast, ensures that the piece of work does what it should. In terms of coding, verification ensures that the code has no error and can be run, while validation ensures that the resulting program/system (in case of HDL) fulfills the specification. Therefore verification is an iterative process that is needed in every design step to make sure it is done right and validation is needed after a design step to ensure that the result is still within the specification.

Logic Simulation

With the HDL design done in VHDL it was possible to create a so-called testbench, a program creating the stimuli to test the design. The VHDL blocks can be tested in a functional way, but they will do so without any delay. Those stimuli are created and modified at certain times. In this first stage of simulation the timescale doesn't matter because of the infinite fast response time of the design, but later in the design phase, timing will be included. To validate the design, the testbench creates the stimuli that will happen also at the measurements experiments:

- The SPAD pulses are created.

- The low-active reset is asserted to guarantee that the design is in a known state.
- After the reset is deasserted, the enable is activated, to enable the counting operation.
- UP and DOWN counting is controlled using the UPnDOWN input.
- To end the counting period, the enable is deactivated.
- The LOADnSHIFT signal is used to control the operational modes of the shift register: it is synchronously loaded using the read clock. In this step the calculation of the required value is performed. On the data ouput pin the rightmost bit of the calculated value is asserted.
- The shift register is changed to shifting operation and every further clock edge on the readCLK pin will perform a shift. Since the rightmost bit is connected to the data output the value can be recorded.

Figure 3.5 shows the logic simulation of the readout procedure of the whole digital correlator. The purple signals are input control signals. The orange clock signals are the up and down clock created by the pulse shaper (see section 4.1). The blue clock signal is the readout clock provided by the PXI system. The red signal is the load/shift control bit. It has to be noted that for all simulations a clock with a constant period (2ns) was used to simulate the pulses created by the SPAD. This frequency is much higher than expected. After counting 100 up, 45 down, 150 up and 35 down pulses the readout procedure is started. The control signal myLDnSHIFT (red) is high, meaning the shift register is in loading mode when the first clock edge of myCLKrd (light blue) triggers the output to change. The DEBUG signal is used for the simulation only. It shows the content of the shift register in decimal numbers. The number of 170 as sum of the 250 up and 80 down pulses was taken because its bit representation is *10101010* and this makes the simulation results better readable. After the shift register is loaded with the first clock edge of the myCLKrd, the control signal myLDnSHIFT is changed to '0' to change the register to shifting operation. With every further clock two things can be observed: the content of the shift register is divided by 2, this happens because a right shift by 1 is the same as a division by 2 in binary number representation. Additionally the output bit myDATA changes, because it is connected to the rightmost bit of the shift register. In this case the data transfer is finished after 8 clock cycles. When using the full 28 bit, 28 clock cycles would be needed. Also it can be seen that the counters are reset at 674ns while the readout is active. The readout works independently from the counters.

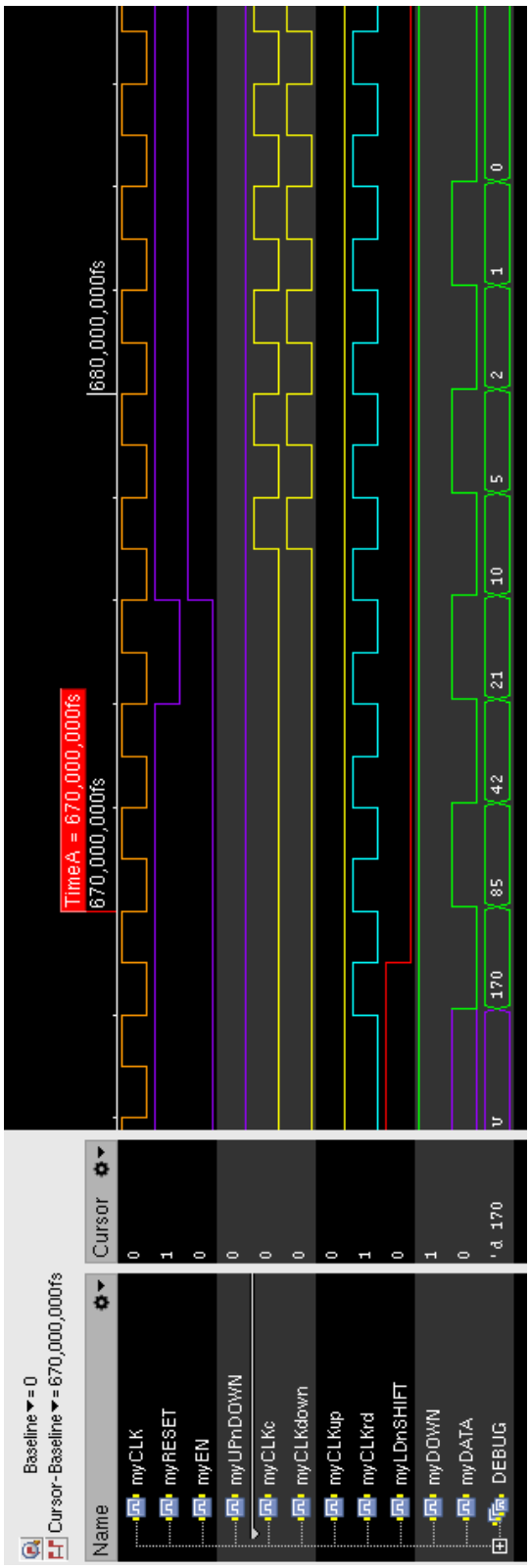


Fig. 3.5: Digital logic simulation of the readout procedure.

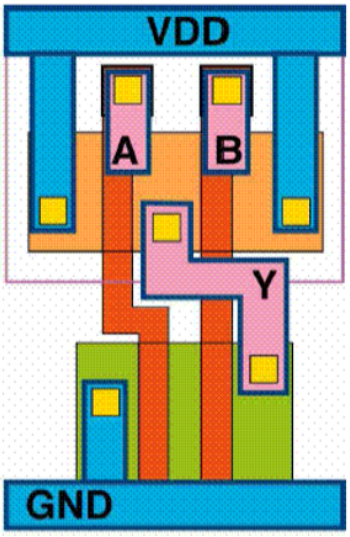


Fig. 3.6: Example of a digital standard cell NAND. [10]

3.4 Synthesis

All steps until now are commonly called the frontend-design (functional design), while the steps after logic synthesis are referred to as the backend-design (process of making the functional design manufacturable). In big ASIC companies those two are normally different departments. Digital synthesis is the step where both departments have to work together. Digital synthesis is the process of transforming HDL-code into a design implementation consisting of logic gates. This step is heavily computerized, because there are a lot of constraints to be considered and calculations to be done. Most ASIC foundries offer digital standard libraries that are composed of a multitude of logic gates. They contain not only the schematic and layout of those gates but also specific timing information that is needed to calculate the timing of a synthesized design. These libraries contain not only typical logical gates like AND, NOR or NOT, but also more complex functions that can reduce the area required by the whole circuit. All standard cells have the same height and VDD and GND connections on the top and bottom (see Figure 3.6). In the first step of the synthesis, the HDL-coded behavior model is analyzed and inferred into logic and state elements. Then technology-independent optimizations are performed (e.g. logic simplification, state assignment). After the logic equations have been minimized, they have to be mapped onto the technology dependent gates. Due to setup and hold time requirements, additional technology dependent optimizations have to be done (e.g. driving strengths of gates are adjusted, so the propagation time of a signal satisfies setup and hold requirements). Timing libraries include information about multiple operational corners:

- **BEST** for the fastest propagation time (low temperature and ideal supply voltage, slighly higher than specified)
- **TYPICAL** for normal operation under expected conditions (temperature 25°C and supply voltage according to databook)
- **WORST** for the slowest propagation time (high temperature and lowered supply voltage)

Digital tools use so-called static timing analysis (STA) because regular (analog) circuits simulations would cause to much computational effort to be done efficiently. Since synchronous digital circuits change their states (= content of their storing elements - flip flops) only at the clock edges, each single path from the output from one flip flop to the input of another has to be analyzed. But this can be done so independently! There are two requirements for every path: *setup* and *hold* time cannot be violated. If they are not complied with, the storing elements cannot operate in a functional way (metastability).

- *Setup time:* defines the amount of time a signal has to be asserted to the data input of a flip flow before a change of state occurs. If this is violated, the output value cannot be known beforehand and the logic circuit does most likely not behave as intended.
- *Hold time:* defines the amount of time a signal has to stay the same after a change of state occurs. As for the setup time, violating this time can cause metastable states.

During synthesis these parameters are observed and optimized with respect to the user provided constraints (e.g. the target clock frequency). A very important key figure is slack. It is defined as difference between actual or achieved time and the desired time for a timing path. For the timing path, slack determines if the design is working at the specified speed or frequency. A negative slack describes that a circuit will not work. The path with the smallest slack is called the critical path, because it determines the maximum clock frequency at which the logic circuit can be run. Figure 3.7 shows the timing diagram of a register-register data path. The blue lines show the minimum required setup and hold times and the green ones show their respective slacks. The clock frequency could be increased until the setup or hold slack is zero while still maintaining functionality.

To use the digital synthesis tool the VHDL-code is not sufficient, because for it to be synthesizable, it cannot include timing information. Those are provided by LFoundry in

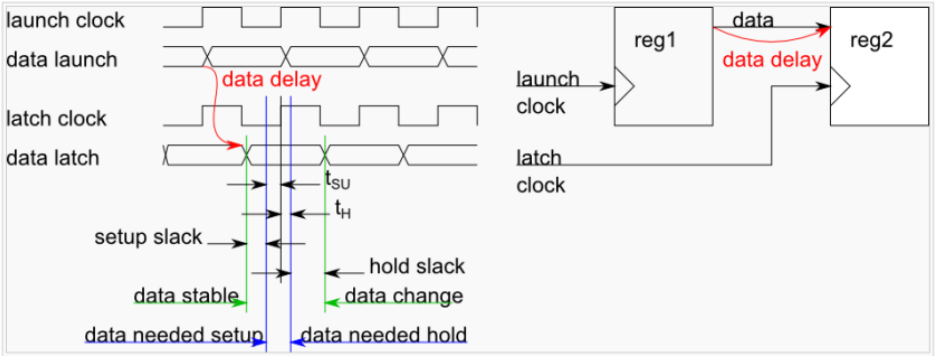


Fig. 3.7: Timing diagram of a data path showing setup and hold slacks. [4]

libraries containing simulated and measured timings for every single available standard cell. In addition, timing constraints are needed to tell the tool which datapaths are valid. This can be done using Synopsys design constraints (SDC), a format used to specify the design intent, including the timing, power and area constraints for a design. SDC is based on tool command language (TCL) and is a standard, accepted by the industry. During synthesis the worst timing library is used because the circuit has to work under any circumstances. The output of synthesis is a technology depended gate level netlist containing only the provided standard cells and their interconnects.

3.4.1 Post-Synthesis Simulation

While the initially used VHDL or verilog design is most likely a RTL design, the output of synthesis is only a combination and wiring of the available standard cells. The propagation time of a signal change is determined by many parameters. Let's analyze the case of two combined sequential NOT gates: When the input of the first gate changes, its output will do so as well, but it only does so after the propagation delay. This is no fixed number because it heavily depends on the capacitive load on the output. The capacitive load is defined by two main components: the capacitance of the connected gate (or even multiple gates) and the interconnect between them. When one output is connected to multiple inputs, the load can become quite high, slowing down the propagation delay of the first gate and therefore the speed with which the circuit can be used. To cope with this, gates with a higher driving strengths can be used. They should only be used when needed, due to their larger area requirements.

During synthesis the propagation times are calculated, without the effect of the interconnect wiring. To be able to check if the design is still working as intended, the synthesis tools will also provide the user with a standard delay format (SDF) file. It

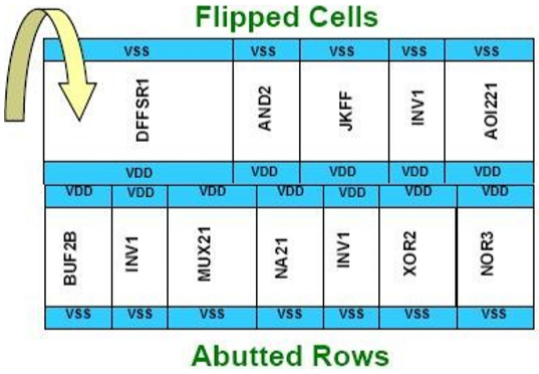


Fig. 3.8: Abbuted (= flipped) placement rows with common supply rails. [10]

contains the propagation delay of every gate used, and makes it possible to include them into the digital simulation.

3.5 Place and Route

During the place and route (PnR) step a corresponding layout for the synthesized netlist is created. This is an iterative process, because the impact of interconnects has not been accounted for yet and will cause additional delays in the circuit.

Floorplaning

During floorplaning the basic size and shape of the layout is set. While a single design chip will take the least area when being a square, a digital design block used within another block can be created in a different way.

The digital cells provided by the chip foundries all have the same height, allowing to place them in so called placement rows. Additional they all have their power connection on the same metal layer and on the same edge (see Figure 3.6). In the beginning of VLSI, between every placement row, there was a routing channel, because there were not enough metal layers available to make the routing on top of the standard cells; nowadays sufficient metal layers are available, saving a lot of area. To reduce the size even further, it is possible to flip every second row, to have common supply connections for two rows, as can be seen in Figure 3.8.

Placement

During the placement of the logic cells, a temporary virtual routing is performed to analyze the resulting timing of the circuit. The lower the slack of a path is, the more

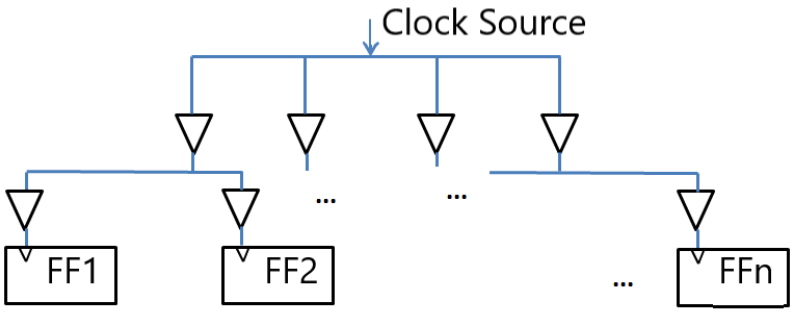


Fig. 3.9: Balanced clock-tree (the path from the clock source to each flip-flop contains equal buffers). [13]

care is taken that the elements of this path are placed near each other to lower the impact of trace length delay. Placement is an iterative process. If the resulting layout doesn't satisfy timing constraints it has to be redone, not as a whole, but the devices that are part of the data paths that do not satisfy the timing. Automated placement needs more area than just the sum of the logic cells; an overhead of about 25% is needed, due to routing cells with a higher drive that need a bigger area and those may be needed. That place has to be accounted for.

Modern synchronous circuits often contain multiple thousands or millions of digital flip-flops. Because of that, the clock and reset net have a high fanout (number of devices a net is connected to). Path length introduces additional delays because of runtime and additional capacitive load. Because of that, multiple buffers have to be added to compensate for the additional load. The process of creating this so-called clock-tree (see 3.9), is called the clock-tree synthesis. The area-overhead introduced in the placement step is used to place those needed buffers, therefore reducing the "wasted" area.

Because this design is rather small with a low clock fanout, no additional buffers where needed to balance the clock-tree. The used EDA tool can display the clock-tree with and shows the time differences between the launch of the clock and the arrival at the different sinks (clock inputs of the flip-flops). For this design the longest delay is 6ps.

Design Rules

Design rules are provided by the semiconductor foundries and enable the engineers to verify manufacturability of the single layers. They include minimum and maximum line widths for e.g. metal layers and minimum distances of those. When they are not complied to, there is no guarantee that the design is working and in most cases the foundry will not be wiling to manufacture the ASIC.

Routing

The virtual routes introduced in the placements step need to be refined and finalized. There are two important constraints: manufacturability (the design rules of the ASIC foundry have to be satisfied) and the timing of the circuit has to be satisfied. First, the routes of the critical timing paths are finished and checked. Afterwards, the non-critical paths are routed. This reduces congestion problems for critical paths. After routing, the timing is again verified by STA. While the STA, which is performed during synthesis, is only done with the worst timing library, it is now done as corner simulation. During corner simulation both the fastest and the slowest timings have to be considered, especially concerning hold times: If a signal is propagated to fast it can violate hold timings.

Filler Cells

After routing the circuit is fully functional but not necessarily manufacturable. This is because of free areas not occupied by standard cells. Therefore there are gaps in the p- and n-wells and diffusion areas that most likely do not satisfy the design rules provided by the foundry. These areas need to be filled with so-called filler cells. There are two types of those filler cells: regular filler cells that are used to fill up the doped areas and CMOS capacitances that are used to stabilize the supply voltage and to reduce current induced voltage drops. After the filler cells are inserted, the layout of the circuit should satisfy design rules and is manufacturable.

3.6 Post-Layout Simulation

From the finished layout it is possible to extract the netlist containing the standard cells and a SDF-file containing the combined timings from the cells and routes (concerning their length and load capacitance). These timings can be used for HDL simulation and to verify functionality of the circuit. Full analog simulation is also possible, but for circuits containing multiple thousands of cells the computational effort is huge. Because of the small size of the design, full analog simulation can also be used to verify circuit functionality. It is the most in-depth possibility to analyze a circuit and it is only limited by computational power and the accuracy of the circuit device models. In this section, the simulations of the fine counter block will be compared.

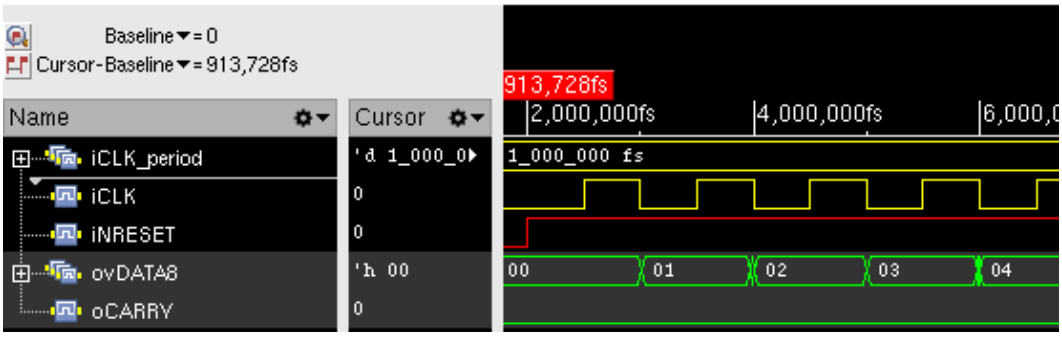


Fig. 3.10: Logic post-layout simulation of fine counter.

3.6.1 Logic Post-Layout Simulation

After the layout is finished in Cadence Innovus, it is possible to extract the resulting verilog netlist that has to match the synthesized netlist and the calculated timing information in form of a SDC file. Using a digital simulato,r capable of including the SDC file to the simulation, it is possible to verify the circuit functionality and to simulate the resulting propagation delays of the digital circuit. The results of the simulation can be seen in Figure 3.10. The yellow clock signal has a period of 1ns, showing that the fine counter is capable of working at a much higher clock rate than needed. The green ovDATA8 signal changes about 450ps after the clock edge triggers the synchronous circuit. The worst case corner was used for this simulation.

Analog Post-Layout Simulation with Extracted Parasitics

Based on finite element models, it is possible to extract the parasitic capacitances between different layers of the ASIC design as well as the resistances introduced by the metal interconnects from the finished layout. This was done after porting the design from Cadence Innovus to Cadence Virtuoso. In Figure 3.11 the analog simulation of the fine counter block can be seen. The red signal is the clock input signal and the teal signal is the reset that has to be done to bring the flip-flops to a defined state. After every positive clock edge the lowermost bit (the blue signal in Figure 3.11) of the counter output changes with a propagation delay of 340 ps. In contrast to digital post-layout simulation there are fixed corners, parameters as temperature and supply voltage can be specified precisely during simulation and not only maximum and minimum corners are possible. While the 340ps delay apply for a temperature of 25°C, increasing the temperature to 150 °C increases the propagation delay of the circuit to roughly 440ps, being quite near the results of the post-layout logic simulation.

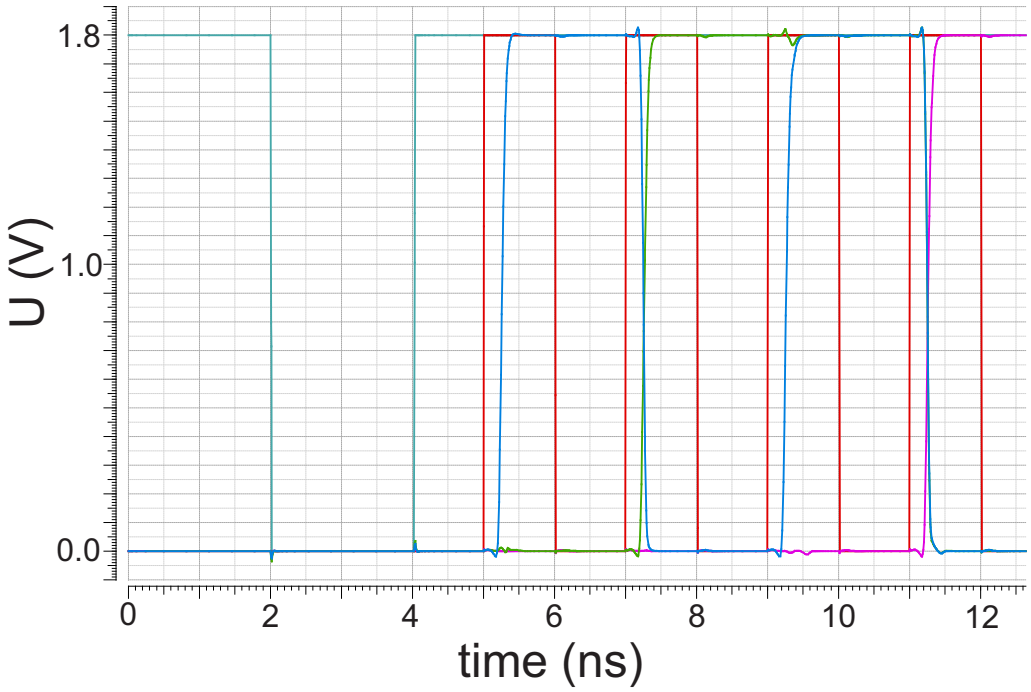


Fig. 3.11: Analog post-layout simulation of fine counter.

3.7 Chip Finishing

Since the digital design will be used as a functional block together with the quenching circuit, no further work is needed and the integration of the created building blocks is described in 4.4.2.

Chapter 4

Analog and Asynchronous Design

4.1 Pulse Shaping and Clock Generation

The digital circuitry needs three different clocking signals:

- **UP-clock** to perform up-counting during the active period of the correlation signal for the UP fine counter.
- **DOWN-clock** to perform up-counting during the inactive period of the correlation signal for the DOWN fine counter.
- **COARSE-clock** to count the overflows of the fine counters.

Those three signals have to be created from the SPAD pulse, the UP/DOWN signal, and the enable signal. Special care has to be taken for the case that the counting direction changes in a timeframe around the SPAD pulse. Because of that, an edge detection circuit is used to create a short pulse that is gated using a combinational logic circuit, creating the pulses for the corresponding clocks. Because these pulses are too short to reliably trigger the clock-input of many flip-flops in parallel, as used in the digital circuit blocks, each pulse is prolonged using an edge-triggered pulse generator.

Edge Detection

The edge detection was created using an AND gate in combination with an inverter and a delay-chain of inverters which can be used to accurately control the output length of the created pulse. The duration of the input pulse doesn't matter as long as the pulse is longer than the output pulse that has to be achieved. The AND gate compares the signal to a delayed, inverted copy of the signal and creates a pulse as long as the propagation delay of the inverter and the delay chain is, as shown in Figure 4.1.

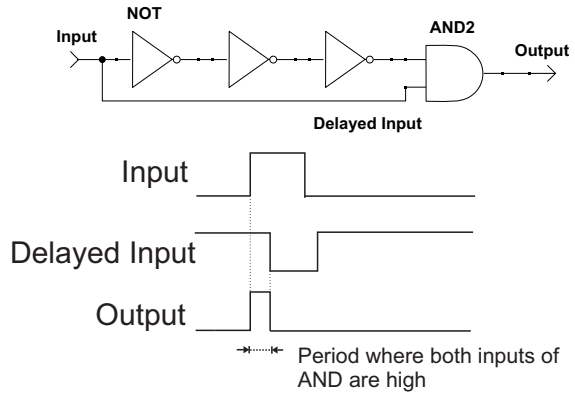


Fig. 4.1: Edge detection circuit functionality

Combinational Logic

When designing the combinational logic, the length of the pulses created by the edge detection had to be considered carefully. Since the pulse cannot be indefinitely short and still trigger the edge detected pulse generator, the outcome of the case in which a counting direction change happens during a shortened pulse has to be thought about. Does the pulse trigger UP or DOWN counting? It is impossible to make this decision perfectly when working with two asynchronous signals and because of that two possible outcomes are preferred:

- *No* counting is performed
- *UP and DOWN* counting is performed

The design choice was to perform both UP and DOWN counting in this case, resulting in no counter change (as would no counting).

Pulse Generator

The pulses that will be used to drive the clock input of the flip-flops used in the digital building blocks are created using a combination of a flip-flop and delay cell. The output from the combinational circuit is fed into the clock input of a flip-flop, resulting in a output transition to 1, since the data input is tied to a logical '1'. While the output Q of the flip-flop is used for the output pulse, the inverted output $\bar{Q}$ is delayed by a delay circuit and is connected to the active low reset of the device. After the propagation delay, Q changes back to zero, $\bar{Q}$ changes to a logic '1' and the reset is deasserted, making it possible to trigger another pulse. This also makes sure that the flip-flop is always in a known state after power up.

The feature of a flip-flop to need a pulse of at least a certain length to trigger an output transition, was exploited to ignore partial pulses created by the combinational logic. This was used by setting the length of the pulses to just over two times the minimum required time, resulting in a time slot of 20 ps in which both counts are performed. With an expected dead-time between rising edges of two pulses of 7ns this results in a maximum error of 0.29% (if the SPAD is saturated). Since this error occurs at random times, it affects down and up counts in the same way, so in average it cancels itself out. A buffer with a strong enough drive is added for each signal, to drive the whole clock nets of the digital blocks.

Results

In Figure 4.2 the results of analog post layout simulation are shown. The orange signal is the simulated pulse created by the quenching circuit. The purple signal is the shortened pulse after the edge detection, whose length has been carefully engineered. The red and blue pulses are the clock pulses created for the digital blocks. Their length is 650ps, which is enough to reliably trigger the flip-flops. A load of 200fF is assumed for the combined gate and net capacitance, resulting in a signal rise time of 100ps. Post-layout simulations of the whole digital correlator show a rise time of 70ps, revealing that the gate capacity of the cells is lower than estimated. When the SPAD is saturated (the deadtime between pulses is 7ns), the pulse shaper has an RMS current consumption of 1 mA and a peak current consumption of 8mA during output pulse generation.

4.2 Carry Latch

To solve the problem that occurs if a fine-counters is stopped with an active carry bit (he coarse-counter would continue counting) a protection register is needed. It has to ensure, that the carry bit can only be active for the one following counting operation of the coarse-counter. Only if during the last cycle the carry was '0' and at the actual carry signal from the fine counter is '1'. This can be achieved by using a flip-flop to always store the state of the carry signals from the previous clock cycle and comparing it to the carry signal.

4.3 Substrate Isolation

Since the digital correlation device will be manufactured on the same chip as the quenching circuit made by Alija Dervic, MSc. additional constraints must be considered.

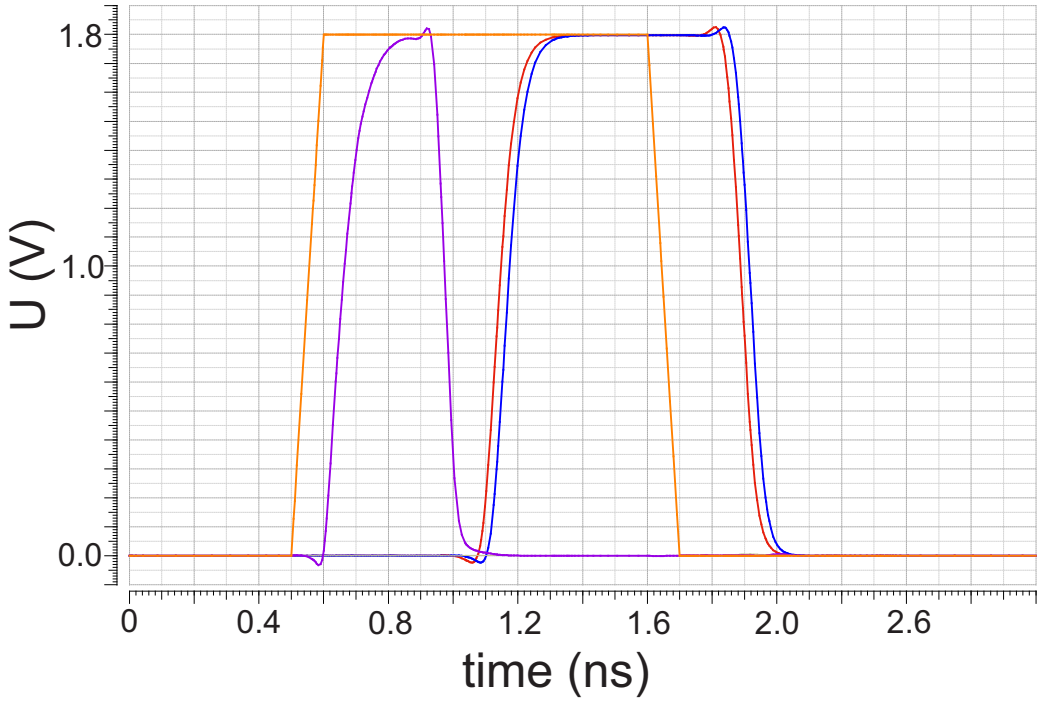


Fig. 4.2: Simulation of pulse shaper.

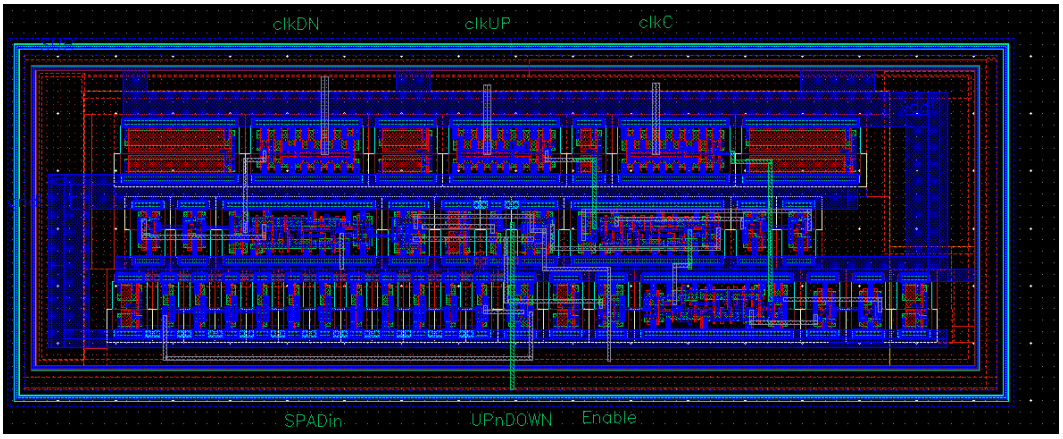
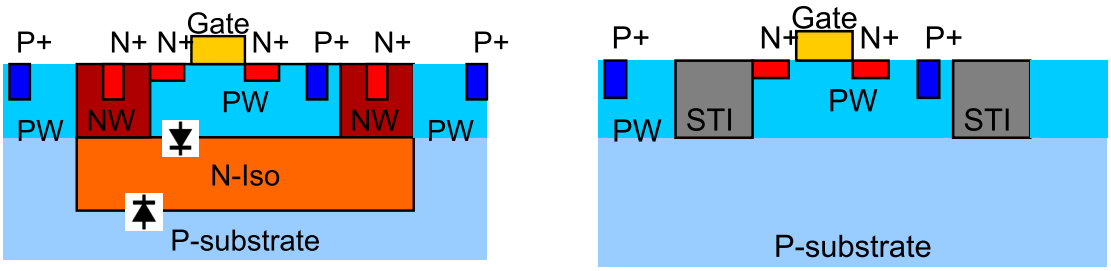


Fig. 4.3: Layout of pulse shaper.



(a) n-channel MOSFET with n-isolation.

(b) Regular n-channel MOSFET.

Fig. 4.4: Comparison of isolated and not isolated MOS devices.

The quenching circuit needs the substrate to be at -5V, while the digital standard cells are designed to work with a grounded substrate. Because of this, an n-isolation layer has to be implemented by hand into all digital blocks. Due to working with placement rows, this is possible without altering the functionality of the design. Especially for the smaller building blocks this is a not insignificant area overhead because of the design rules for the n-well and n-isolation layer.

Figure 4.4b shows an n-channel MOSFET: if the left p+ contact would be connected to a negative voltage, while the right p+ bulk contact of the device is connected to ground, a short would happen. Figure 4.4a shows how the device is isolated from a negative substrate using an n-isolation layer. The n-isolation layer forms two pn-junctions functioning as diodes that are reverse biased: The p-substrate is connected to negative substrate bias (-5V), the n-isolation to VDD (1.8V) and the p-well to ground. The shallow trench isolation (STI) is not shown in Figure 4.4a for a clearer view.

4.4 Padring Design

The final ASIC needs pads to be connected to a package or PCB. While the feature size shrinks more and more, and with it the standard cell size, the pad size cannot be reduced in the same proportion, because bonding machines need a minimum size to be able to bond reliable. The used LFoundry 150nm process provides 65µm and 80µm pads. It has to be noted that the whole pad needs more than just the bonding pad: for outputs additional drivers are needed to drive the load of the bonding wire (some picofarads), the PCB traces and the connected circuits. Inputs also include electro-static discharge (ESD) protection circuits. The outermost area of the ASIC is needed for the seal ring (see 4.5), a structure to enclose the die (the unenclosed

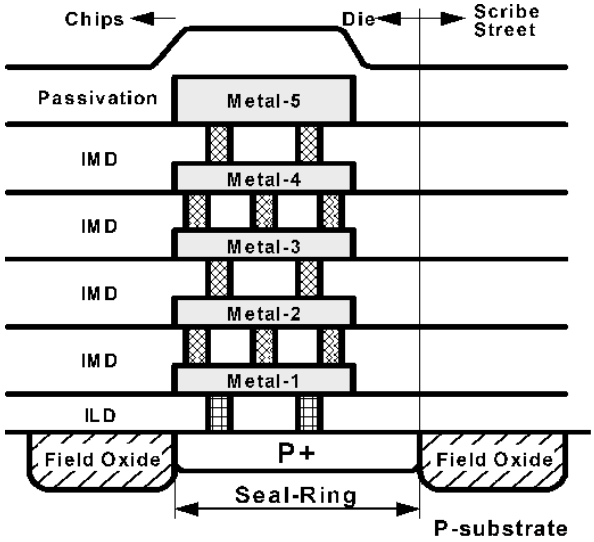


Fig. 4.5: Sealring made out of a full metal stack and multiple vias to provide stability during sawing. [3]

semiconductor chip). It protects the die from moisture and gives it stability for sawing and also contains markings where to saw the die out of the whole wafer.

Due to the negatively biased substrate the regular factory provided input and output pads with their normally used ESD-protection are not usable because they connect the substrate to GND. Not including ESD-protection shouldn't be done for a market ready device, but for a test chip, only handled in the lab it is entirely possible. Input pads do not need a special circuit to work, but output pads have to include a buffering stage to drive the capacitance of the pad, the PCB-traces and the connected devices (about 2 pF in total), since most digital standard cells are only able to drive several fF. Because the output of this device will have a very fast data output and short transitioning times, it is important to take care of the wave impedance to reduce possible reflections of the output signals. Since most measurement equipment uses 50 Ω input impedance, a output buffer that can drive this load is needed.

4.4.1 50Ω Output Buffer

An output buffer for a digital output can be realized using an even numbers of CMOS inverters in series while increasing their width with each step. The output resistance of the last inverter can not be neglected when driving such a low ohmic load. A lower output resistance would need a wider transistors (specially the p-MOS) of the last inverter. As a trade-off between area required and performance a minimum output voltage of 1.4V on the pad was specified, because the needed LVDS converter is available with an input resistance of 50Ω and 1.2V logic level input. This was achievable with a

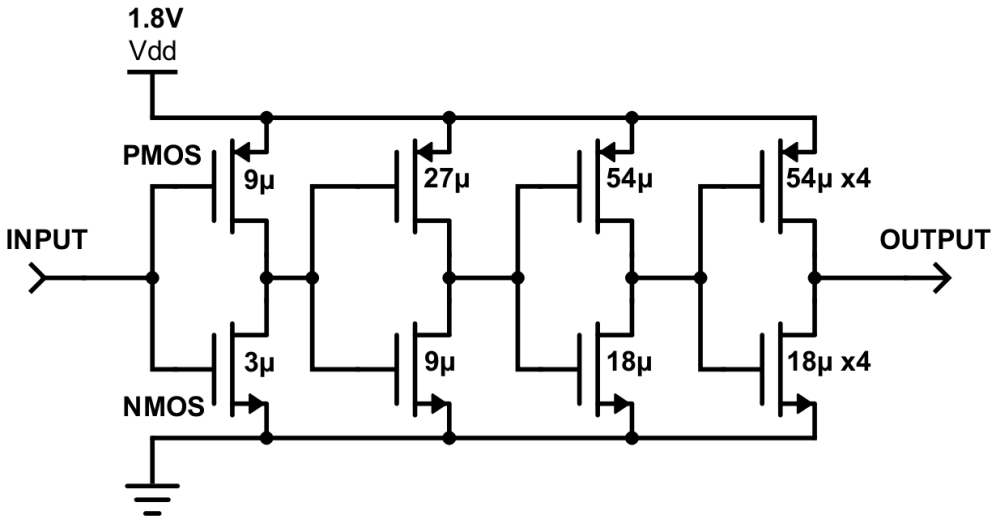


Fig. 4.6: Schematic of 50Ω buffer with transistor widths.

chain of 4 inverters with a width ratio of 1:3:6:24. The absolute widths can be seen in Figure 4.6, the last stage has multiple transistors in parallel. Multiple inverters are needed to drive the rising gate capacitance of the next inverter. The gate length of the devices are set to the minimum of 150nm. This is done to increase their speed and has no negative impact because the short channel effects have only minimal impact on digital circuits. Transistors with multiple fingers are used to fit them better into the layout and to reduce gate resistance. NMOS transistor widths can be smaller than PMOS transistor widths for two reason: first the mobility of carriers (electrons) is higher by a factor of about two to three and the current running through the NMOS transistor of the output stage is just the switching current, while the PMOS has to deliver the current to drive the 50Ω resistor. There is also an enable pin included to make it possible to shut down the driver. When a negative value is output through the shift register, a '1' will remain in it and the circuit would have a permanent high power dissipation that could decrease performance.

To drive a load of 50Ω (R) to a voltage level of 1.8 Volts (U), a current (I) of $I = \frac{U}{R} = \frac{1.8V}{50\Omega} = 36mA$ is needed. Two requirements are given for the buffer to function: the buffer itself has to be able to deliver enough current and the supply needs to be able to. A metal line of 1µm width in the used process will heat up to 80°C when a current of about 3mA is flowing through them. Because of the required 36mA, this means that a supply and output connection of at least 12µm is needed.

The finished layout, see Figure 4.7, has an area requirement of 44µm x 32µm. Figure 4.8, shows the post-layout simulation of the buffer. The blue signal is an input pulse

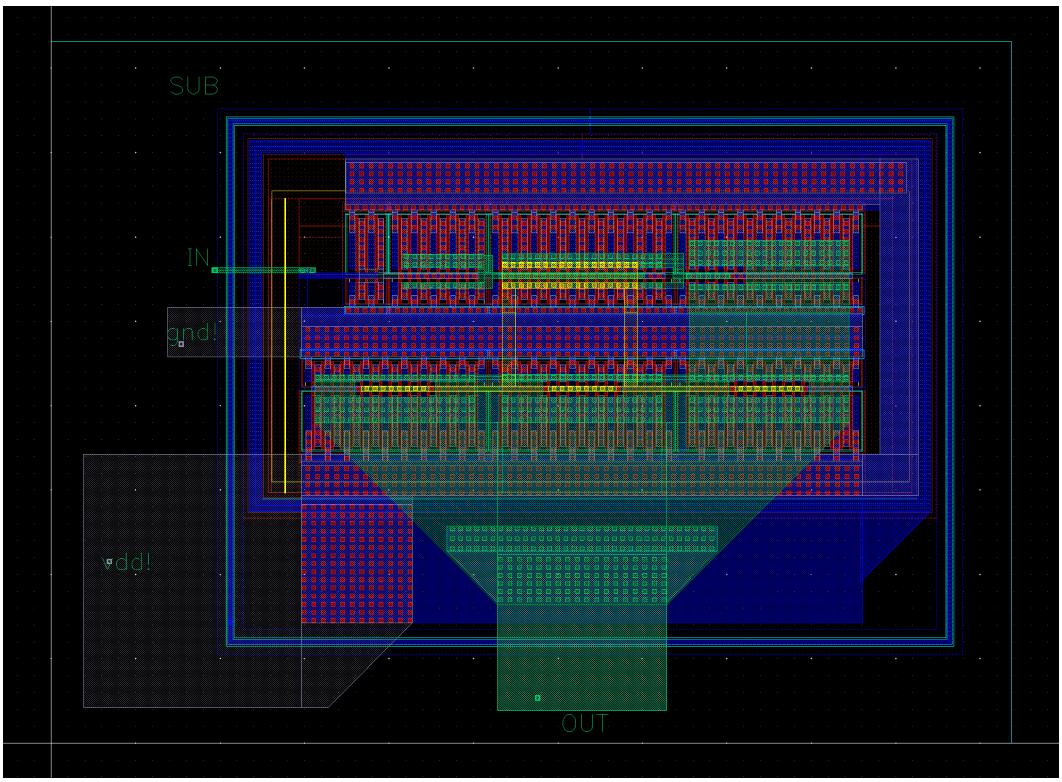


Fig. 4.7: Layout of 50Ω buffer.

and the red is the output. The propagation delay of the buffer is 300ps. This simulation was done with a load of 50Ω with a capacity of 2pf in parallel to take pad and PCB trace capacitances into account. Due to the output resistance of the last inverter, the voltage on the pad is only 1.38V. This is still sufficient for the application. The orange signal is the current consumption of the buffer. During switching the peak current is 42mA and during a logic '1'at the input the current consumption decreases to 28mA.

4.4.2 Block Integration

For the finished device, including the correlation circuit twice, 37 pads are needed, 18 for the Quenching circuit, 15 for the two-phase digital correlator, and 4 for a stand alone correlator used for testing it as a standalone device. This results in a pad-limited design with 750μm $\times$750μm usable area inside the padring. During block integration additional capacitors have to be added to stabilize the supply voltage. All the remaining area inside the padring will be used for this. The LFoundry 150nm process supplies metal in metal capacitors created between the two uppermost metal layers.

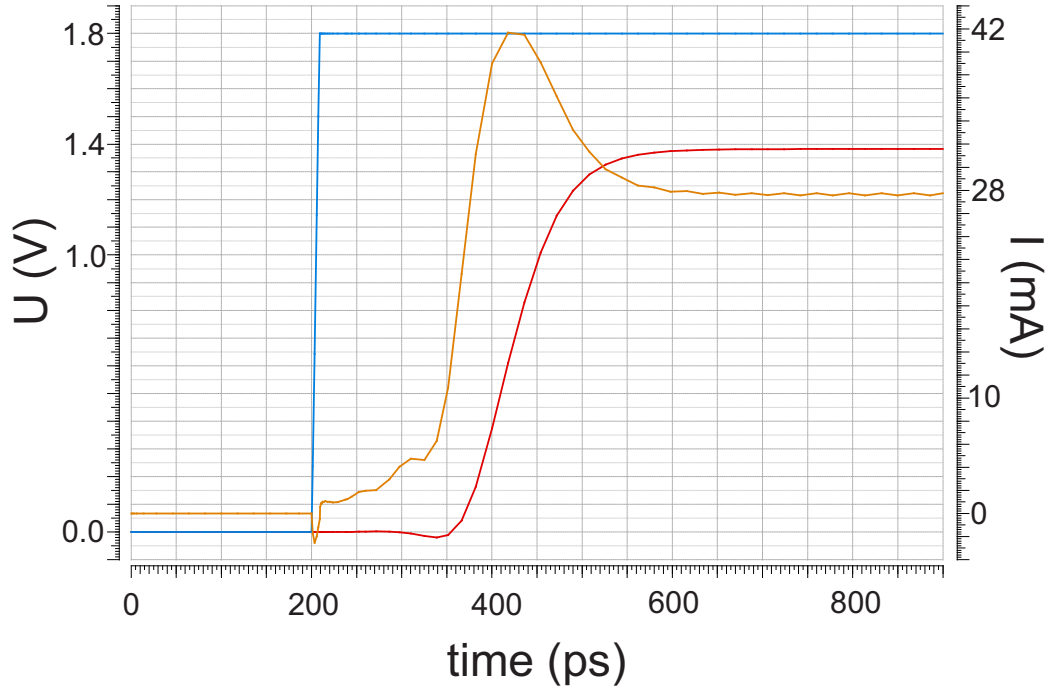


Fig. 4.8: Post-layout simulation of 50Ω buffer.

Chapter 5

Results

In this chapter the final ASIC and some simulation results are presented. Because the final layout of the quenching circuit is not finished yet, a stand alone dual phase digital correlator will be presented that can be connected to any SPAD with quenching circuit to perform distance measurements. The final pins of the ASIC are:

- 2 VDD core pins for 1.8V supply of the digital core circuit
- 2 VSS core pins for core circuit core supply
- SPAD pulse input, the pulses need to be at least 500ps long, both correlators get this input
- Active high enable pin to enable counting
- Active low reset pin to reset counter content
- Up (high) - down (low) control pin for correlator 1
- Up (high) - down (low) control pin for correlator 2
- 2 VDD IO pins for high current 1.8V supply of the 50Ω drivers
- VSS IO pin for ground supply of the 50Ω drivers
- Active high IO enable to enable the drivers only during readout
- Read clock to operate loading and shifting of the 28-bit output shift register
- Load (high) - shift (low) pin for synchronous loading and shifting operation
- Data pin 1 for 50Ohm output of correlator 1
- Data pin 2 for 50Ohm output of correlator 2

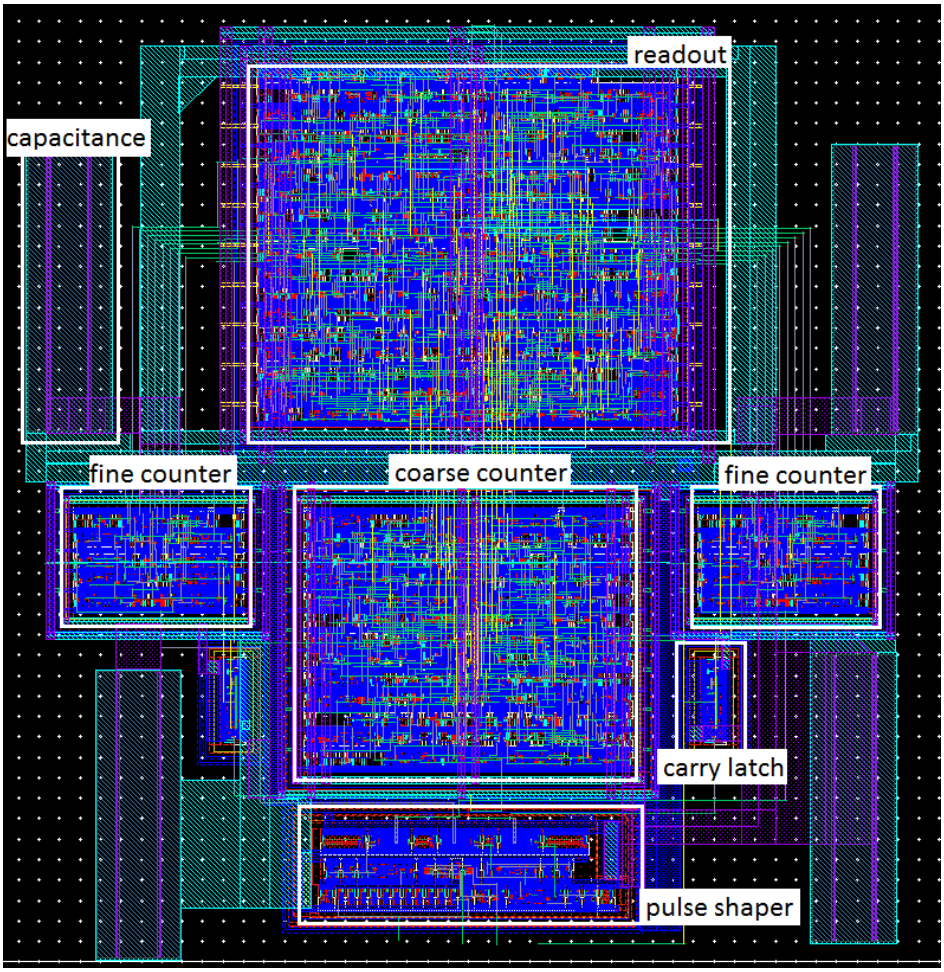


Fig. 5.1: Final layout of digital correlator including 4 metal in metal decoupling capacitors (228µm × 217µm).

5.1 Layout

The area layout of the digital correlator circuit is 228µm × 217µm including metal in metal decoupling capacitors (4 times 1.3 pF) and can be seen in Figure 5.1. The final layout of the ASIC with two digital correlators including pads and sealring is 974µm × 804µm in size and can be seen in Figure 5.2.

5.1.1 Analog Post-Layout Simulation of the ASIC

When simulating the whole ASIC, not only parasitics introduced by the routing have to be taken into account, but the connections of the die to the PCB have to be considered as well. Especially the inductance and resistance of the bonding wires have to be modeled because if the circuit requires a high current for a short time, especially during switching, there will be a drop in supply voltage. The inductance of the wires can be

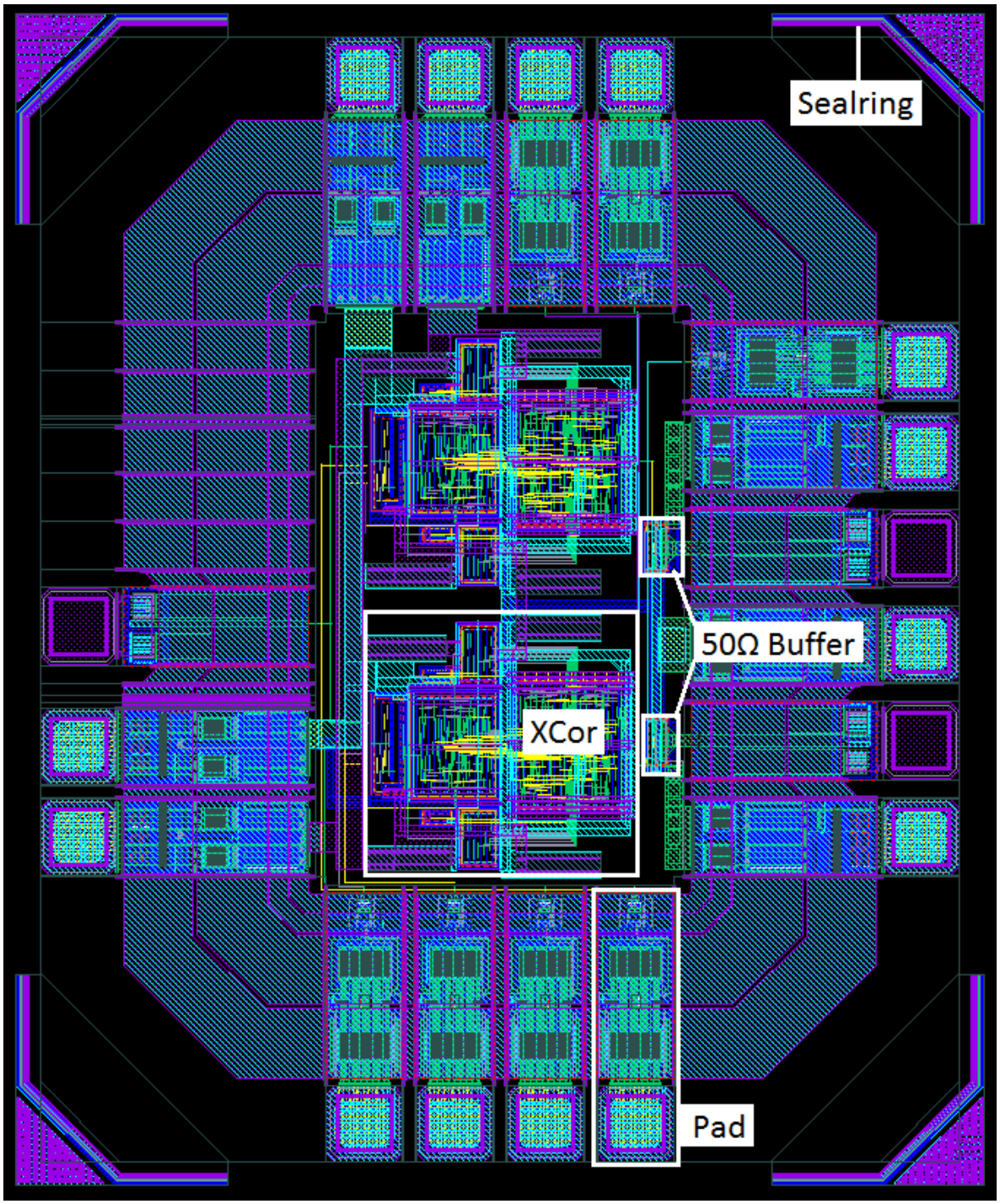


Fig. 5.2: Final ASIC layout of stand alone dual phase correlator including pads and sealring (974µm × 804µm).

assumed as 1nH and their resistance as 100mΩ. It was observed that the inductance of the bonding wires together with the gate capacitance of the logic cells create a serial oscillator that gets stimulated by any change of signal. To dampen this effect, a resistor was added between the pad and the inputs of the corresponding logic cells. The value of the resistor is $R = \frac{400\Omega}{Numberofgatesconnected}$. If there are multiple gates connected in parallel the resistance has to be reduced to not decrease the bandwidth. With this measure the problem was solved.

Results

A maximum pulse rate of 250MHz is possible in all operational corners (supply voltage and temperature). This is equivalent to a dead time of 4ns, while the quencher used for the distance measuring experiments will have a minimum dead time of around 7ns. When ideal operational conditions are satisfied and guaranteed, the pulse rate can be increased even further. Especially the temperature of the device may be concerning during operation of the real device because during readout operations the output buffers are having a high power dissipation. Experiments will show the maximum clock rate, because heating of the substrate due to power dissipation is not supported by the simulation tool. The used temperature corners were 27°C and 150°C.

A timeframe of at least 4ns has to be between end of correlation (disable the counters with the ENABLE signal) and the start of readout operation. The readout itself can be performed with up to 250 Mhz during all operational modes. The delay between a clock edge on the readCLK pin and the change of the data signal is roughly 1ns, this includes the delay introduced by the buffer (300ps).

The digital core draws an RMS current of 4.4mA during the analog simulation. The peak current during counting is 10mA, during loading of the shift register it reaches 27mA, and during shifting operation the circuit consumes a peak current 12mA.

The inclusion of the pads decreased the performance of the 50Ω output buffers a bit: while the output voltage was 1.38V during post-layout simulation of just the buffer, the pad reduces it to 1.35V which is still sufficient for driving 1.2V logic.

Chapter 6

Conclusion and Outlook

Due to their digital output characteristic SPADs are very well suited to be interfaced with digital electronic circuits and together with the fact that they can be included in CMOS processes they are very promising devices promising smaller and integrated sensor solutions such as distance measurements or 3D-imaging.

While the synchronous digital design of the proposed ASIC is rather simple, the asynchronous nature of the SPAD pulses, in relation to the signal to which they are correlated with, provide an obstacle that cannot be overcome easily with regular RTL design. In my opinion the used 3-counter scheme is a good solution for this problem. The use of digital counters also provide a very high dynamic range because it increases exponentially with the bit size of the counters (in this case 29 bit), while the area increases linearly. Other approaches such as charge counting cannot compete in the aspect of high dynamic range, because both the area as well as the dynamic range have a linear relation.

The digital correlator can be used for multiple types of range measurements. While it is especially suited for correlation measurements like continuous-wave-modulation, it can also be used to measure a frequency that occurs when performing interferometric distance measurements with stepwise changed wavelength or a FSF laser. Especially for this second use case the high dynamic range will be helpful, since it will be used as a simple counter. When the needed dynamic range is smaller it is possible to create a far smaller circuit, which will allow to use the digital correlator in pixel arrays.

Both, the stand alone dual-phase correlator and a combination of the quenching circuit and dual phase digital correlator will be produced as ASICs in January 2019 by LFoundry and will be characterized during my planned Ph.D. studies.

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Technical specification of digital correlation circuit 150nm LFoundry

Horst Zimmermann, Alexander Kuttner, Michael Hofbauer, Alija Dervic and Michael Hauser

***Abstract*— This document shall describe the functionality and features of a digital correlation circuit. Based on this, the frontend design will be done in HDL (hardware description language) and will be tested using simulation tools. Once verified, the backend design will be done using cadence software suite (special mention to *GENUS* and *INNOVUS*). This device will be part of an ASIC used for range measurements using a frequency-feedback-shift(FSF)-laser.**

I. Overview

The digital correlation circuit will be used to make range measurements with SPADs (single-photon-avalanche-diodes). The circuit will have to work together with an active quenching circuit designed by Alija Dervic. Two methods of measurement should be performed: TOF (time-of-flight) using frequency measurement based on phase correlation and interferometric measurements using the variance of amplitude depending on varying wavelengths. To increase accuracy of the phase correlation measurement, two instances of this counter will be needed and they have to driven by two 90°shifted signals.

II. Description of circuit features

A. Input clock

Input pules can be as short as 1ns and have to be recognized, this translates into a frequency of 1 GHz. This frequency will not be reached however, since the quenching circuit will have a higher quenching time because of the SPAD being off-chip. It can be assumed that in saturation, one pulse will occur every 5ns. This would translate to a frequency of 200Mhz Since this signal drives the clock of the digital circuit, setup and especially hold times will be critical and careful simulation of timing constraints has to be done. The design will be sped up as much as possible to be able to work with an integrated SPAD in further applications.

B. Counter depth

The counter width has to be enough to not achieve overflow. For a measurement time of 1s and a best-case clock of 500MHz, a counter width of 29 bit is sufficient, since negative values have to be possible since the counter can count up and down. Two's complement representation work very well with digital circuits and will be used. Bit depth is linear proportional to area requirement.

C. Switching between UP and DOWN counting

Since a synchronous counter will be used, switching between counting up and down is possible without harming the counting value. Switching between operational modes while the circuit is in counting operation needs to possible because of the asynchronous nature of the received SPAD pulses.

D. Readout

Readout of the counter value shall be possible using a shift register. After the the counting is finished , the counter value can be stored into a shift register using a second control bit and the shift clock, which has to be supplied off-chip. After the control bit is unset again, the value can be shifted out. Additionally the counting circuit can be used for another measurement simultaneously . It has to be reset beforehand though.

E. Pin description

- *clkC* - counting clock, input from quenching circuit
- *clkEN* - clock enable HIGH active
- *reset* - asynchronous reset, this only resets the counter, not the shift register. LOW active
- *clkSR* - shift register clock used for readout
- *SAVE/SHIFT* - control bit to save counter value to shift register or set shift mode. SAVE works as an synchronous reset and the counter-value is loaded into the shift register
- *DATA* - 1-bit of data used to transmit data from shift register MSB first

III. Design steps

Most of this work will be done using the digital design flow. Only in the final part of the design process analog simulation will be necessary.

A. Specification

This document shall describe the features that the chip implements. Because of the incrementing nature of the design flow, a change in features at a later point will make all work done obsolete.

B. VHDL model and simulation

A VHDL model has to be made and the design has to be verified against the specification using extensive testbench simulation. It is very important that there are no errors, because every further design will be verified against this model.

C. Digital Synthesis

The HDL design has to be synthesized using Cadence GENUS and the standard cell libraries provided by LFoundry. A lot of work has to be put into the synthesis constraints to achieve a design that is usable at various clocking speeds. This is done using static timing analysis. A very important part is the post-synthesis-simulation and -verification. The output of the synthesis is a verilog-netlist.

D. Digital Implementation

Using Cadence INNOVUS the placement and interconnects of standard cells can be simplified. Additionally a clock tree and the power supply has to be build.

E. Post layout simulation

After the layout is designed the design has to be verified against the VHDL model. There may be some difficulties due to impact of trace length, additional delay and load caused by them.

EMCE, TU Vienna

Code of Conduct

Hiermit erkläre ich, dass die vorliegende Arbeit gemäß dem Code of Conduct – Regeln zur Sicherung guter wissenschaftlicher Praxis (in der aktuellen Fassung des jeweiligen Mitteilungsblattes der TU Wien), insbesondere ohne unzulässige Hilfe Dritter und ohne Benutzung anderer als der angegebenen Hilfsmittel, angefertigt wurde. Die aus anderen Quellen direkt oder indirekt übernommenen Daten und Konzepte sind unter Angabe der Quelle gekennzeichnet. Die Arbeit wurde bisher weder im In– noch im Ausland in gleicher oder in ähnlicher Form in anderen Prüfungsverfahren vorgelegt.

Alexander Kuttner
Wien, 13. November 2018