DISSERTATION

Behavior of SiC-MOSFETs under Temperature and Voltage Stress

ausgeführt zum Zwecke der Erlangung des akademischen Grades
eines Doktors der technischen Wissenschaften
unter der Leitung von

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Wien, am 01. September 2018

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I declare that I have authored this thesis independently, that I have not used other than the declared sources / resources, and that I have explicitly marked all material which has been quoted either literally or by content from the used sources.

November 19, 2018

Acknowledgments / Danksagung

- I want to sincerely thank **Tibor Grasser** for the professional guidance of my PhD during the entire three years of my thesis.
- I thank all my colleagues at KAI and IFAT. I especially thank **Josef Fugger** and **Michael Nelhiebel** for the opportunity to join KAI. Furthermore, I thank **Gregor Pobegen** and **Thomas Aichinger** for their important inputs and discussions.
- Zu guter Letzt möchte ich mich noch bei **Betti, Franz, Gisi, Martin und Bernhard** für all die Unterstützung über die letzten Jahre hinweg bedanken! Diese Arbeit wäre ohne euch nicht möglich gewesen!
- This work was funded by the Austrian Research Promotion Agency (FFG, Project No. 860424).

Abstract

Silicon Carbide (SiC), as a wide band gap semiconductor, promises superior performance for power devices. Compared to Silicon-based devices, MOSFETs based on SiC can be operated at higher temperature, higher frequency and higher power density. Furthermore, they provide significantly reduced static and dynamic losses, which allows for shrinking passive components and heatsinks at the system level. All of these benefits make full SiC system solutions more efficient, lighter, compact and even less expensive than their silicon based counterparts.

Despite all of the benefits mentioned above, 4H-SiC-MOSFETs still perform far from their theoretical limits. Especially their low channel mobility and increased threshold voltage variations, which differ substantially from silicon based devices in certain aspects, need to be understood and assessed. Therefore, the main focus of this thesis is the investigation of bias temperature instabilities (BTI), which arise after temperature and voltage stress of the gate oxide. Unlike in Si based MOSFETs, where the major part of BTI originates from trap states within the SiO_2-film, 2 independent components are identified on SiC-based MOSFETs.

The first component is especially visible as a gate voltage hysteresis in the subthreshold regime of the transfer characteristics. This hysteresis may reach several volts and originates from hole capture in traps states at the 4H-SiC/SiO_2 interface. The density of these states depends significantly on the crystal plane of the inversion channel and is approximately one order of magnitude higher on devices with the inversion channel along the *c*-axis. Furthermore, the observed hysteresis scales with the charge pumping signal and is nearly independent of temperature. Unlike in classic BTI in silicon based devices, the observed hysteresis is fully recoverable in normal device operation within micro seconds via a gate voltage above the threshold voltage and does not impact the long-term device reliability. Carbon dangling bonds are suggested as the most promising defect candidate for these states.

The second component is similar to what is observed on silicon based devices and most likely originates from border trap states in the SiO_2, which are energetically located close to the conduction band of 4H-SiC. In the first section of this thesis, similarities in BTI of commercially available SiC-power MOSFETs are presented with the conclusion that all devices available on the market today show a nearly identical drift behavior. As opposed to silicon based devices, even an operation close to the threshold voltage causes a voltage shift in the range of hundreds of millivolts. The second section focuses on various voltage shift measurement techniques. It will be demonstrated that most of the observed voltage shift in 4H-SiC based devices originates from fully reversible and stress-independent components. A new drift evaluation technique using device preconditioning is proposed, which allows for a more comprehensive and nearly measurement delay-time-independent extraction of the permanent voltage shift component.

In the last part of this thesis, the impact of various high-temperature processing steps on the charge state of the SiC/SiO_2 interface was investigated. It will be shown that a high thermal budget results in an significant accumulation of positive charges at the SiC/SiO_2 interface. The build-up of positive charges starts after the deposition of the polycrystalline gate contact, and continues in all additional processing steps, in which the sample is exposed to a high thermal budget with temperatures above 500 °C. Furthermore, the presence of an electric field in the oxide, which likely enables diffusion of the positive charges to the SiC/SiO_2 interface during the high temperature processing steps, is of fundamental importance for the observed mechanism. The atomic origin of the charge build-up is still unknown but likely linked to hydrogen, which is incorporated during the poly-silicon (Si) deposition. An energy barrier of approximately 1.3 eV was extracted from the experimental data.

Kurzfassung

Siliziumcarbid (SiC) verspricht als Halbleiter mit großer Bandlücke (englisch: wide-band-gap, WBG) enorme Vorteile für Leistungshalbleiterbauelemente. Im Vergleich zu auf Silizium basierenden Metall-Oxid-Halbleiter Feldeffekttransistoren (englisch: MOSFETs), erlauben auf Siliziumcarbid basierende MOSFETs einen Betrieb bei höherer Temperatur, höherer Frequenz und höherer Leistungsdichte. Darüber hinaus sind durch die Verwendung von SiC-MOSFETs deutlich reduzierte statische und dynamische Verluste möglich, wodurch passive Bauteile und Kühlkörper auf Systemebene signifikant verkleinert werden können. All diese Vorteile machen auf SiC basierende Systemlösungen weitaus effizienter, leichter, kompakter und auch kostengünstiger als Systeme, welche rein auf Siliziumtechnologie aufgebaut sind.

Trotz all dieser Vorteile bleibt die erreichte Leistung aktueller 4H-SiC-MOSFETs immer noch weit entfernt von den theoretischen Materialgrenzen. Insbesondere die Ursachen der geringen Beweglichkeit der Kanalelektronen und der erhöhten Spannungs- und Temperaturinstabilität der Schwellspannung (englisch: bias temperature instability, BTI), welche sich in manchen Charakteristika grundlegend von siliziumbasierten MOSFETs unterscheidet, müssen verstanden und auf die Langzeitzuverlässigkeit hin bewertet werden.

Aus diesem Grund liegt der Schwerpunkt dieser Arbeit in der Untersuchung der Schwellspannungsinstabilität, welche nach Temperatur- und Spannungsbeanspruchung des Gate-Oxids auftritt. Im Gegensatz zu Si-MOSFETs, bei denen der größte Teil dieser Instabilität aus energetisch breit verteilten Defektstellen innerhalb des Gate Oxides stammt, spielen bei SiC-basierten MOSFETs zwei unterschiedliche Komponenten eine wichtige Rolle.

Die erste Komponente, welche insbesondere als Spannungshysterese in der Transferkennlinie für Gatespannungen unterhalb der Schwellspannung sichtbar ist, kann auf den Einfang von Löchern in Defektstellen direkt am Interface zwischen 4H-SiC und SiO_2 zurückgeführt werden. Die Dichte dieser Defektzustände hängt wesentlich von der Kristallebene des Inversionskanals ab und ist bei MOSFETs mit dem Inversionskanal entlang der c-Achse um etwa eine Größenordnung höher als bei MOSFETs mit dem Inversionskanal parallel zur Waferoberfläche. Im Gegensatz zu BTI in Si-MOSFETs, sind diese Zustände im normalen Betrieb über eine Gatespannung oberhalb der Schwellenspannung vollständig entladbar und zeigen keinerlei Einfluss auf das Langzeitdegradationsverhalten des Bauteils. Offene Kohlenstoffbindungen am Interface gelten als wahrscheinlichster Kandidat für diese Defektstellen.

Die zweite Komponente ist ähnlich zu BTI auf siliziumbasierten MOSFETs und stammt höchstwahrscheinlich von Defektzuständen im SiO_2, welche energetisch nahe am Leitungsband von 4H-SiC liegen. In dieser Arbeit wurden kommerziell erhältliche state-of-the-art SiC-Leistungs-MOSFETs wurden auf ihr BTI Verhalten hin untersucht. Es wird gezeigt, dass alle derzeit auf dem Markt erhältlichen SiC-MOSFETs ein nahezu identisches Einsatzspannungsdriftverhalten zeigen. Im Gegensatz zu siliziumbasierten MOSFETs, führt selbst ein Betrieb nahe der Schwellenspannung zu einer Spannungsverschiebung im Bereich

von mehreren hundert Millivolt. Weiters wurden verschiedene Techniken zur Messung der Spannungsverschiebung untersucht. Insbesondere wird dargestellt, dass in standardisierten Messvorschriften wie dem JEDEC Standard, der Großteil der extrahierten Spannungsverschiebungen aus vollständig reversiblen, schalt- und stressunabhängigen Effekten stammt. Aus diesem Grund wird eine neue Driftauswertungstechnik vorgeschlagen, welche mittels Vorkonditionierung durch einen Akkumulationspuls eine exakte Extraktion der permanenten Komponente der Spannungsverschiebung ermöglicht. Ein weiterer signifikanter Vorteil ist, dass diese Messmethode kaum von der Zeitverzögerung der Messung abhängt.

Im letzten Teil dieser Arbeit werden die Auswirkungen der verschiedenen Hochtemperaturprozesse, welche für die Fertigung der Leistungshalbleiterbauelemente nötig sind, auf den Ladezustand der SiC/SiO2-Grenzfläche untersucht. Es wird gezeigt, dass ein hohes Wärmebudget zu einer signifikanten Anhäufung von positiven Ladungen an der SiC/SiO_2 Schnittstelle führt. Dieser Aufbau von positiven Ladungen beginnt nach der Abscheidung des polykristallinen Gate-Kontakts und setzt sich in allen weiteren Prozessschritten, welche über ein hohes Wärmebudget mit Temperaturen über 500 °C verfügen fort. Der atomare Ursprung der eigebauten Ladungen ist nach wie vor unbekannt. Möglicherweise spielt hier Wasserstoff, welcher durch die Abscheidung des polykristallinen Gate Kontakts in großen Mengen eingebaut wird, eine wichtige Rolle. Durch die Abhängigkeit des Ladungseinbaus vom Temperaturbudget wurde eine Energiebarriere von ca. 1,3 eV aus den experimentellen Daten extrahiert, welche gut zu den theoretischen, auf Wasserstoff basierenden, Defektmechanismen passen würde.

Contents

CHAPTER 1

Introduction

Contents

1.1 Silicon Carbide

1.1.1 Crystal Properties

Silicon carbide (SiC) is a compound semiconductor, with its atomic crystal consisting of 50 % silicon (Si) and 50 % carbon (C) atoms. Each C has exactly four Si neighbors and vice versa, with a very strong C-Si bond strength of approximately 4.6 eV, which leads to impressive material properties as will be discussed below.

Furthermore, silicon carbide is an outstanding example for *polymorphism*, meaning the crystal can grow in a wide range of different crystal structures (the so called *polytypes*), each of which exhibits unique electrical, optical, thermal, and mechanical properties. A certain polytype is defined by the Si-C bilayer stacking sequence along the *c*-axis of the hexagonal close-packed system. On each Si-C bilayer (A), there are two possible stacking sites (B, C) as illustrated in Fig. 1.1. In Ramsdell's notation, each polytype is labeled after the number of Si-C bilayers in the unit cell and the lattice structure, which can be

cubic (C), hexagonal (H), and rhombohedral (R). The structures of the most common SiC polytypes, 3C-SiC, 2H-SiC, 4H-SiC, and 6H-SiC are shown schematically in Fig. 1.2. The respective lattice properties are given in Table 1.1. In Fig. 1.2, Si atoms are indicated in green, whereas C atoms are shown in black.

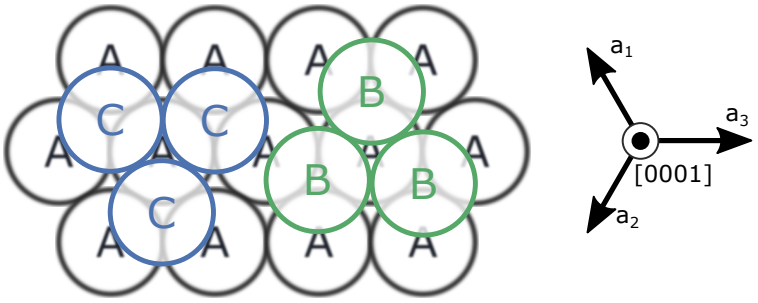


Fig. 1.1 Possible stacking sites of the SiC crystal along the *c*-axis. Each site (A, B, and C) represents a bilayer of Si-C atoms along the *c*-axis of the hexagonal close-packed system. The most common polytypes, 3C-SiC (ABCA), 2H-SiC (ABA), 4H-SiC (ABCBA), and 6H-SiC (ABCACBA) are shown schematically in Fig. 1.2.

Unlike the silicon crystal, the silicon carbide crystal has lattice sites which differ in their structures of nearest neighbors. These lattice sites can either be *hexagonal sites* or *cubic sites*. In Fig. 1.2, those sites are indicated with "h" for a hexagonal or "c" for a cubic lattice site. Cubic and hexagonal sites mainly differ in their position of second-nearest neighbors, which results in different electric fields at the specific site. Therefore, energy levels of impurities, dopants, or point defects depend on the occupied lattice site of the defect/dopant (the so-called *site-effect* [1]). The relative concentration of hexagonal or cubic sites furthermore depends on the polytype: while only cubic sites are present in 3C-SiC, 4H-SiC has one hexagonal and one cubic site, whereas 6H-SiC has one cubic and two hexagonal sites.

Out of the hundreds of available polytypes, 4H-SiC has been almost exclusively employed for power devices. This is mainly due to the following two reasons:

- First, as a result of the high electron mobility μ and critical breakdown field E_B, the Baliga figure of merit (BFOM)

$$\mathrm{BFOM} = \varepsilon_\mathrm{r}^\mathrm{SiC} \varepsilon_0 \mu {E_\mathrm{B}}^3, \tag{1.1}$$

  which defines the material parameters which can be used to minimize the conduction losses in power FET's [2, 3], is significantly higher for 4H-SiC than for most other polytypes, as also indicated in Table 1.1.

- Second, the availability of high-quality, single-crystalline 4H-SiC wafers with large diameters of up to 6 inch (by 2017), allows for higher yields and cost-reduction of commercial devices. Even though other polytypes, like 2H-SiC, might have an even higher mobility than 4H-SiC (as suggested by theoretical calculations [4]), no feasible substrates are available due to the highly complex growth process and polytype control of SiC crystals.

Since all investigated devices in this thesis are based on 4H-SiC, the abbreviation "SiC" refers to the 4H polytype of SiC in all subsequent sections of this work unless otherwise stated.

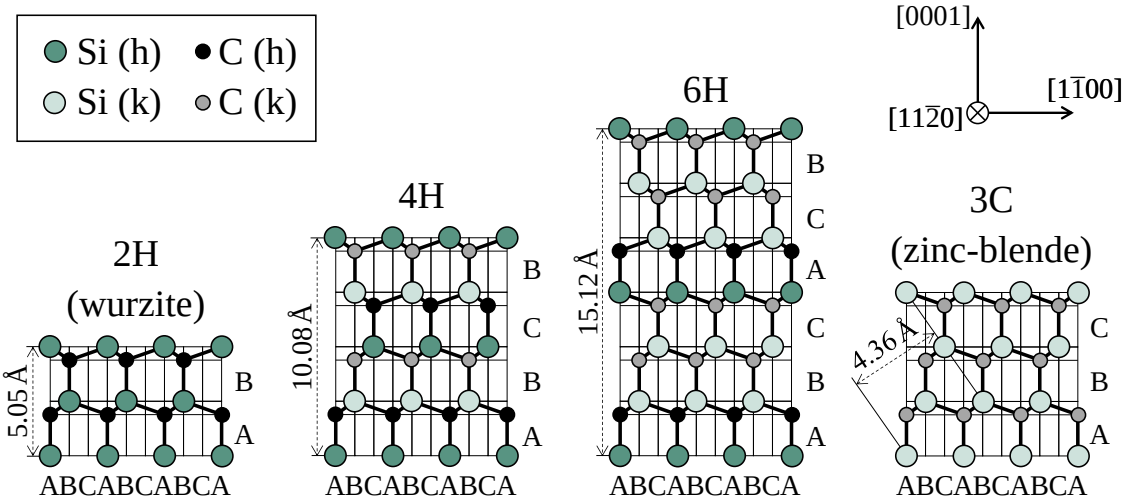


Fig. 1.2 Stacking sequences and inequivalent lattice sites (h and k) of some of the most simple SiC polytypes viewed from the [11$\bar{2}$0] direction) [5].

Table 1.1: Properties of the most simple SiC polytypes at 300 K [4, 6, 7].

Property	2H-SiC	3C-SiC	4H-SiC	6H-SiC
Stacking sequence	AB	ABC	ABCB	ABCACB
Lattice constant c (Å)	5.05	n.a.	10.05	15.12
Lattice constant a (Å)	3.07	4.36	3.07	3.07
Band gap energy (eV)	3.33	2.39	3.26	3.02
Electron mobility $\perp c$ ($cm^2V^{-1}s^{-1}$)	4H+20 %[a]	1000	1020	450
Electron mobility $\parallel c$ ($cm^2V^{-1}s^{-1}$)	4H+45 %[a]	1000	1200	100
Hole mobility ($cm^2V^{-1}s^{-1}$)	-	100	120	100
BFOM (relative to Si)	n.a.	61	626	63

[a] from Monte Carlo simulations [4]

1.1.2 Peculiarities of silicon carbide wafers

Silicon carbide bulk crystals (SiC boules) are usually grown along the [0001] direction from a seed crystal using the *sublimation growth* technique, which was first introduced by Lely in 1955 [8] and later optimized by Tairov and Tsvetkov (modified Lely method) [9, 10]. The growth rate of SiC boules using seeded sublimation growth is around 1 mm h^{-1}. The final length of the SiC boule is usually between 30 mm and 50 mm. Compared to silicon ingots, the complicated growth technique in combination with the slow growth rate and the significantly shorter length of the boules, which is in the range of several meters for silicon and some centimeters for SiC, are the main reasons for the tremendous costs of approximately 1000 $ for one 150 mm high-quality SiC substrate (by 2018).

In general, the process for the production of silicon carbide wafers from the boule crystals is similar to that used for silicon wafers. The main peculiarity of SiC wafers arises from the fact that silicon carbide wafers are sliced off-axis (off-angle) from the cylindrical boules. The whole process is sketched in Fig. 1.3 (left). Fig. 1.3 (right) shows

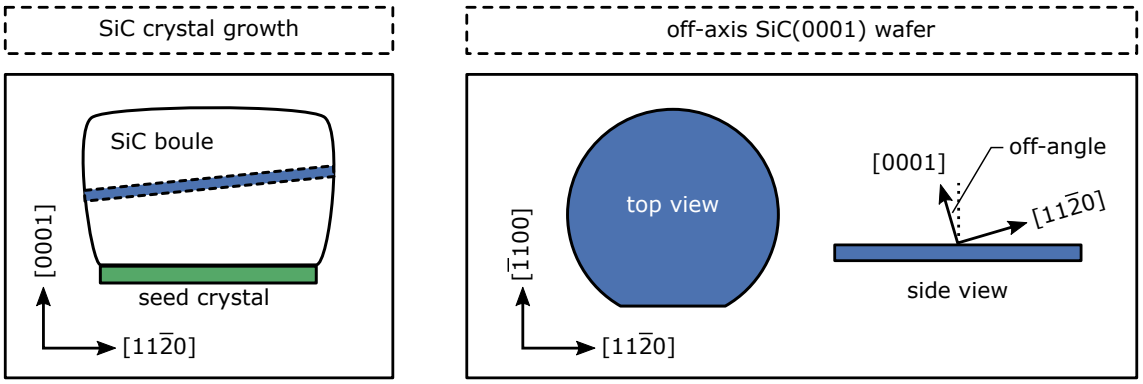


Fig. 1.3 Left: seed crystal (green) and grown boule along the [0001]-direction. To maintain the polytype in the subsequent epitaxial growth, the wafer is cut off-axis (blue). Right: top and side view of an off-axis SiC(0001)-wafer. The off-axis is typically 4° toward [11$\bar{2}$0] [6].

the resulting off-axis 4H-SiC(0001)-wafer, which is usually tilted 4° toward the [11$\bar{2}$0] (or [0001]) direction.

The main reason for the off-axis cut of the SiC wafers is to enable polytype preservation during the high-quality homoepitaxial growth process [6, 11] as indicated in Fig. 1.4. Without an off-axis wafer cut, all stacking information of the polytype is lost and two arrangements, A or B, are possible for the atomic bilayer, which follows C. Due to the step edges, which arise on the surface of an off-axis wafer, only a single possible bond configuration remains (B) [5, 6] because the stacking information is transfered along the crystal growth direction. Fig. 1.5 provides a schematic illustration of the growth modes on an off-axis 4H-SiC wafer during the epitaxial process. The microscopic crystal growth takes place along the step edges, which results in a macroscopic growth along the *c*-axis. Although the off-axis wafer is of fundamental importance for the polytype control, the off-orientation results in an increased surface roughness at the SiC-silicon dioxide (SiO_2) interface (the so-called *step-bunching*), since all step edges are transfered to the surface of the wafer. In the final device, an increased interface roughness along the surface on which the inversion channel forms, might result in a decreased mobility. Therefore several manufacturers try to avoid the step-bunching on the [0001] plane by using trench devices, which also save expensive wafer area, as will be discussed in Section 1.3.2.

1.1.3 Benefits for power devices

As a wide band gap (WBG) semiconductor, 4H-SiC promises superior performance for power device operation due to the 10 times higher breakdown field and 3 times higher thermal conductivity than silicon [12–15]. The higher breakdown field allows for a ten times reduction in the drift layer thickness, which enables a decrease of the on-resistance R_{on} by more than two orders of magnitude. Furthermore, minority carrier charge storage is reduced, allowing for operation at elevated switching frequencies and reduced switching losses. Together with the high thermal conductivity, which enhances heat dissipation and furthermore allows device operation at high temperatures above 400 °C [16–18], SiC is the most promising candidate for high-power electronic semiconductor devices [19].

Another important aspect of SiC is its native oxide SiO_2, which is identical to silicon based devices. Therefore, a high amount of device processing knowledge can be transfered to the processing of SiC based devices. However, several significant differences like the

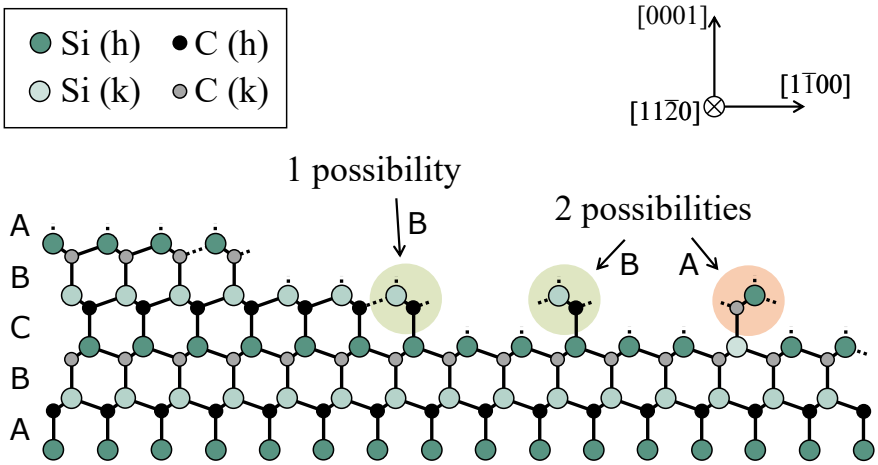


Fig. 1.4 The basic principle of polytype control. Without an off-axis wafer cut, two arrangements (A or B) for the next atomic bilayer are possible after bilayer C since every information about the stacking sequence is lost. Due to the step edges, only a single possible bond configuration remains (B) [5, 6] and the stacking information is available in the crystal growth direction.

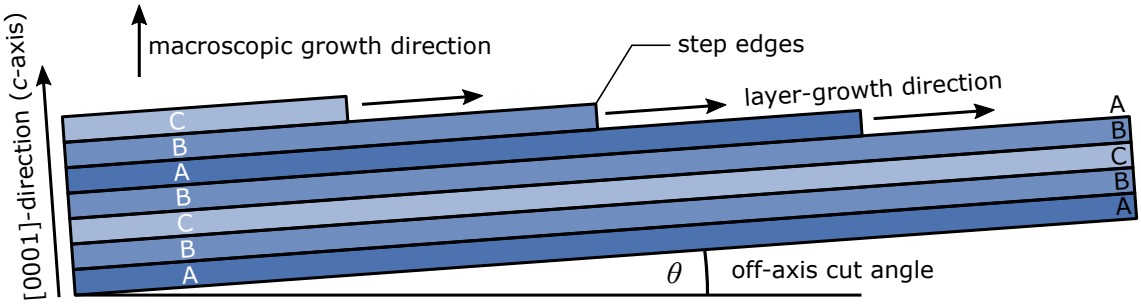


Fig. 1.5 Schematic illustration of the growth modes on an off-axis 4H-SiC wafer. The off-axis cut allows for a preservation of the polytype as indicated in Fig. 1.4 [5, 6].

handling of transparent wafers, necessary high temperature furnaces, low diffusion constants, and novel annealing techniques remain, which is why producing high-quality and reliable SiC devices remains challenging. A comparison of important material parameters for 4H-SiC and other semiconductor materials is provided in Tab. 1.2.

1.2 Detrimental Effects in MOS Devices

Despite all the advantages of SiC, commercially available devices perform far from their theoretical limits. This is mainly due to the fact that the larger band gap of $E_G = 3.23\,\text{eV}$ at 300 K leads to extended interactions of free carriers with interfacial trap states. The energetic positions of these states are within the SiC band gap but outside the silicon band gap and lead to enlarged hysteresis effects [24–29], which are investigated in Chapter 2, and bias temperature instability (BTI), as will be discussed in Chapter 3. Although there have been enormous improvements to the electrical performance within the last years by interface annealing in nitrogen containing atmospheres, like nitrous oxide (N_2O) or nitric

Table 1.2: Material properties of 4H-SiC compared to other semiconductors [2, 6, 20–23].

Property	4H-SiC	Si	GaAs	Diamond	GaN
Band gap energy (eV)	3.26	1.12	1.43	5.45	3.45
Breakdown field ($10^6\,\mathrm{Vcm^{-1}}$)	3.2	0.3	0.4	5.7	3.0
Therm. conductivity $\left(\mathrm{Wcm^{-1}K^{-1}}\right)$	4.9	1.5	0.46	22	1.3
e^- drift velocity ($10^7\,\mathrm{cm\,s^{-1}}$)	2.2	1.0	1.0	2.7	2.2
e^- mobility ($\mathrm{cm^2V^{-1}s^{-1}}$)	1200	1500	8500	2200	1250
Melting point (°C)	2830	1420	1240	4000	2500
BFOM (relative to Si)	626	1	16	27000	650

oxide (NO), SiC-based power MOSFETs still show one to two orders of magnitude higher interface state densities D_{it} as their silicon based counterparts [30–35].

1.2.1 Bias Temperature Instability

Bias temperature instability (BTI), as one of the main topics of interest in countless reliability studies based on 4H-SiC MOSFETs [36–44], is caused by charge trapping at or near the SiC/SiO_2 interface during (high temperature) gate stress, resulting in threshold voltage V_{th} variations, which depend on the polarity of the stress voltage. A positive gate stress results in electron capture leading to V_{th} shifts to more positive gate voltages, whereas a negative gate stress shifts V_{th} to more negative gate voltages. Especially for SiC based power devices, a large positive voltage shift ΔV is undesirable because the voltage overdrive in the on-state is decreased. This is mainly a problem because unlike in silicon based power devices, the contribution of the channel resistance R_{ch} to the total on-resistance R_{on} is significantly higher in SiC devices. Here, R_{ch} accounts for up to 50 % of the total R_{on}. Therefore, a reduction of the overdrive leads to a significant increase in the on-resistance R_{on} and static losses, respectively. A more detailed discussion on the application relevance of BTI for SiC-MOSFETs is given in [43].

Theoretical background

BTI results from charge trapping at or near the semiconductor-insulator interface after the creation of new defects from precursors or charging of preexisting defects [45, 46]. Despite the fact that BTI in silicon based devices has been investigated for more than half a century, the detailed atomic origin is still heavily debated. Several microscopic defect candidates are under intensive investigation, including various interactions with hydrogen (diffusion, hopping, depassivation of silicon dangling bonds etc.) [47, 48], SiO_2 intrinsic electron traps [49, 50], oxygen vacancies [51, 52] or dangling bonds [53, 54]. Although the absolute ΔV is more pronounced in SiC based devices, likely due to the larger band-gap, the BTI characteristics are, at least to some extent, analogous to Si based devices, indicating similar atomic origins. In Section 1.2.2, a more detailed overview on a hydrogen (H) related model (the H release model) is provided, which tries to link the permanent BTI component with H released from the gate-side of the MOSFET and is able to explain many features of BTI.

A often used model for the charge trapping mechanism is shown in Fig. 1.6 (left) assuming a single trap state at the energy level E_{t} within the oxide close to the SiC/SiO_2 interface. At a fixed Fermi-level (e.g during constant bias stress) the classic model is extended by introducing an activation energy E_{A}. Furthermore, the activation energy of

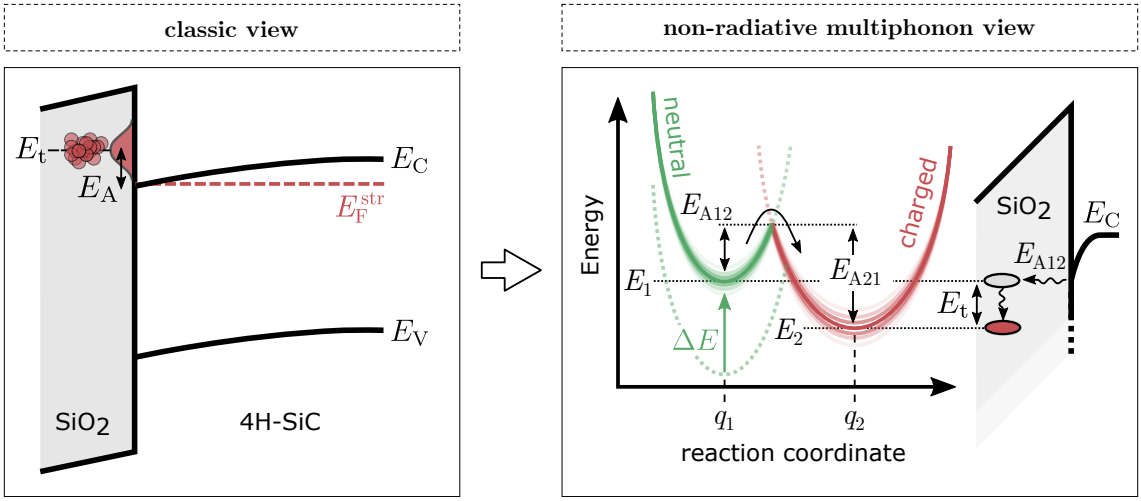


Fig. 1.6 Left: classic view of the trapping mechanism extended with a distributed trap level which results in a distributed activation energy E_A. Right: modern interpretation using non-radiative multiphonon (NMP) theory with distributed activation energies for capture (E_{A12}) and emission (E_{A21}) processes.

the trap state to change its occupancy is assumed to be normally distributed. A more comprehensive explanation of the atomic mechanism is given by the NMP model (Fig. 1.6, right), which also accounts for the atomic deformation of the defect when the charge state is changed and the electric field dependency for both, capture and emission times of the defect [55, 56]. In the NMP model the neutral and charged state of a defect are described as a parabolic function representing the possible energy states (cf. quantum harmonic oscillator) as depicted in Fig. 1.6 (right). Here q_1 and q_2 are the reaction coordinate equilibrium positions with the distributed local ground state energies E_1 and E_2 of the neutral and charged state, respectively.

The required activation energy for a transition of the charge state depends on the ground state energy and the shape of the energy potentials (parabolas). As an example, we start with a neutral precursor described by the green parabola. After providing enough energy E_{A12} through lattice vibrations to change the charge state, the state configuration changes (e.g bond length, equilibrium nuclei position etc.) and is now described by the red parabola. Hence, the activation energy for the reverse transition from the charged (red) to the neutral (green) state is given by E_{A21}, which usually differs from E_{A12}.

Assuming a distributed E_A, the capture/emission process is distributed in time according to the characteristic capture or emission time constant τ

$$\tau = \tau_0 \exp\left(\frac{E_A}{k_B T}\right) \tag{1.2}$$

with the Boltzmann constant k_B, the temperature T and the pre-exponential factor τ_0.

The influence of distributed activation energies on the observed voltage shift ΔV during stress and recovery is shown in Fig. 1.7. For instance, a normally distributed E_A with a mean value $\mu = 1\,\text{eV}$ and standard deviation $\sigma = 0.1\,\text{eV}$ (green, top) will lead to a voltage shift versus stress time behavior with trapping times within $1 \times 10^4\,\text{s}$ and $1 \times 10^{12}\,\text{s}$ (middle, green). Increasing the width of the E_A distribution will lead to a larger stretch out of the stress time dependence as shown in blue ($\mu = 1\,\text{eV}$, $\sigma = 0.2\,\text{eV}$) and red ($\mu = 0.5\,\text{eV}$, $\sigma = 0.3\,\text{eV}$). The bottom picture in Fig. 1.7 represents the discharging behavior for the

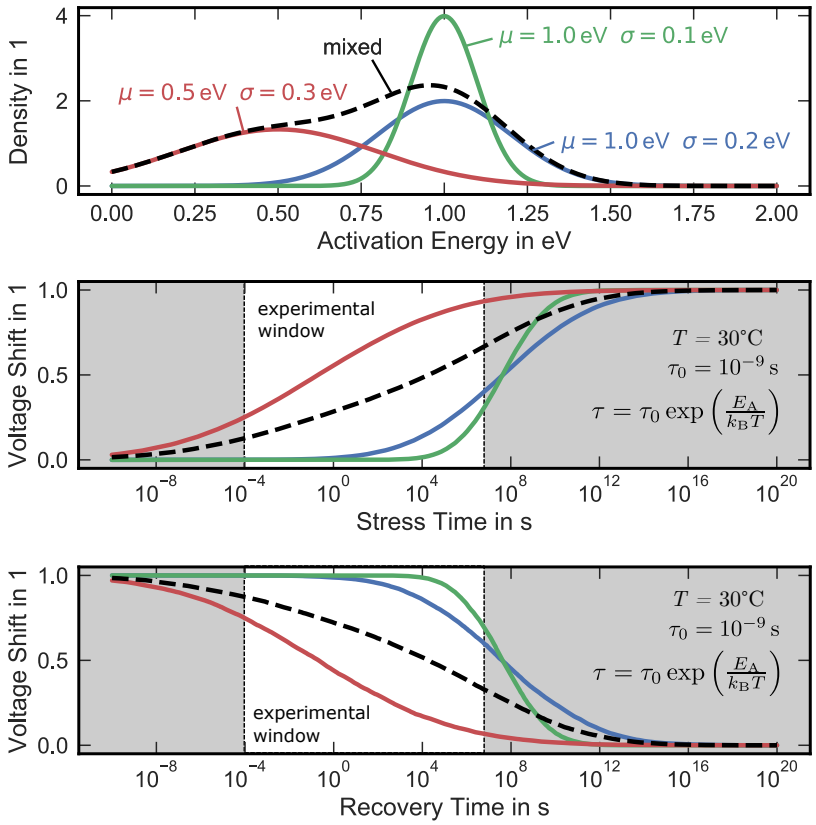


Fig. 1.7 Simulated impact of distributed activation energies (top) on the observed voltage shift during stress (middle) and recovery (bottom) according to (1.4) and (1.6), respectively. The dashed black line represents a mix of the red and blue distributions, which leads to a broad distribution enabling the often used power-law approximation, which is only valid within narrow experimental windows.

same set of activation energies assuming all trapping centers have been filled during the preceding stress. In real devices, a combination of various defects with characteristic energy barriers will contribute, leading to a convolution of the individual voltage shift vs time behaviors [46]. For broadly distributed activation energies, ΔV approaches the often used power-law approximation

$$\Delta V = A \cdot t^k \tag{1.3}$$

with the pre-factor A and the power-law factor k, which is only valid within a narrow time window. An example of a mixture between two individual defects (red and blue) is given in Fig. 1.7 as a dashed black line for stress (middle) and recovery (bottom).

Instead of using (1.3), a physical way to describe the voltage shift ΔV during bias stress is given by [57]

$$\Delta V(t_\mathrm{str}) = \frac{\Delta V^\mathrm{max}}{2} \operatorname{erfc}\left(-\frac{k_\mathrm{B}T \ln(\frac{t_\mathrm{str}}{\tau_0}) - \mu}{\sqrt{2}\sigma}\right) \tag{1.4}$$

with the stress time t_str, the maximum voltage shift ΔV^max as an additional fitting parameter, the parameters of the normal distribution μ and σ, and the complimentary

error function (erfc), which is given by

$$\operatorname{erfc}(x) = 1 - \operatorname{erf}(x) = \frac{2}{\sqrt{\pi}} \int_x^\infty \mathrm{e}^{-a^2}\,\mathrm{d}a. \tag{1.5}$$

In addition to the capture process, the emission process during recovery can be described with a similar equation

$$\Delta V(t_{\mathrm{rec}}) = \frac{\Delta V^{\max}}{2} \operatorname{erfc}\left(\frac{k_{\mathrm{B}}T \ln(\frac{t_{\mathrm{rec}}}{\tau_0}) - \mu}{\sqrt{2}\sigma}\right) \tag{1.6}$$

with the recovery time t_{rec}. Note that the parameters of the normal distribution of the activation energies, μ and σ, for capture and emission processes do not necessarily correlate [46]. As can be seen from (1.4) and (1.6), the time evolution of ΔV scales with the logarithm of the stress or recovery time, resulting in a fundamental dependence of the measurement timing on the extracted ΔV. The strong dependence on the timing parameters of the ΔV measurement will be one of the main topics in Section 3.3.

1.2.2 Hydrogen related defects and the hydrogen release model

Out of all the microscopic defect candidates [49, 50, 53, 54], the interaction of hydrogen with defects or precursors throughout the SiO_2 is able to explain many features of the observed experimental behavior during and after an applied gate stress pulse [48, 58] for semiconductor technology based on a SiO_2 dielectric. In this section, a basic overview on hydrogen related defects in amorphous SiO_2 and their link to bias temperature instability is provided. Most of the information is extracted from the doctoral dissertation of Wimmer [58], where much more detailed information on hydrogen related defects is given.

Possible defect candidates

From the many possibilities of defect candidates in amorphous SiO_2, which are able to explain a considerable amount of BTI features, the 3 most promising are sketched in Fig. 1.8 and described in the following:

- First, the *oxygen vacancy* (V_O) as the best-studied defect in SiO_2 needs to be mentioned (Fig. 1.8, left). The V_O forms when an oxygen (O) atom is missing in the amorphous SiO_2, which causes the two neighboring Si atoms to form a bond resulting in a strong relaxation of the surrounding network. If the oxygen vacancy traps a hole, it is converted to the *E'-center* defect, which has been studied intensively in numerous papers [59–63].

- Second, the *hydrogen bridge* defect (Fig. 1.8, middle), which is similar to the V_O. Here, a H atom is bond to one of the silicon atoms instead of the bridging O atom. The hydrogen bridge forms when an interstitial hydrogen atom is present in the vicinity of a pre-existing V_O. After overcoming a negligible barrier ($E_{\mathrm{B}} < 0.15\,\mathrm{eV}$) [58], the hydrogen is trapped at the position of the oxygen vacancy.

- Third, the *hydroxyl-E' center* as indicated in Fig. 1.8 (right). This defect forms when a H atom interacts with a two-coordinated O atom by breaking one of the Si-O bonds. It is important to note that this particular mechanism requires the presence of a strained Si-O bond, which is the case for approximately 2 % of all the Si atoms in the SiO_2 as calculated by El-Sayed *et al.* [47]. Furthermore, the density

of strained Si-O bonds is likely to increase close to the SiO_2-semiconductor interface, which results in an increased likelihood of hydroxyl E' centers in the vicinity of the SiO_2-semiconductor interface.

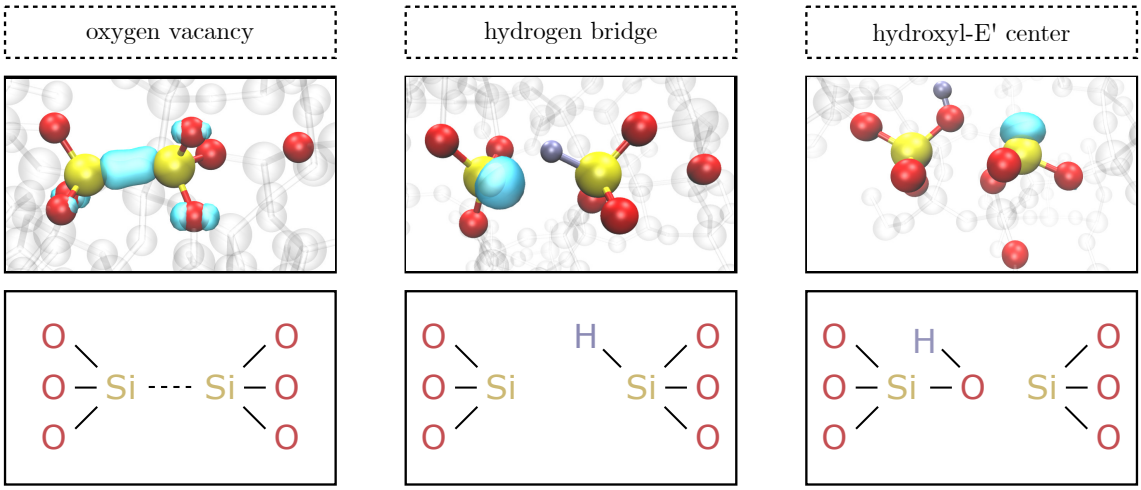


Fig. 1.8 Defect candidates in amorphous SiO_2. Left: the oxygen vacancy V_O. The V_O is able to trap a hole, which converts the V_O into the well-studied E' center. Middle: the hydrogen bridge. The defect is similar to the V_O with a hydrogen atom bound to one of the Si atoms. Right: the hydroxyl E' center. Here a hydrogen atom interacts with one of the bridging oxygen atoms by breaking one of the Si-O bonds, which requires a strained Si-O bond [58].

Hydrogen release model

Out of all atomistic models which have been proposed to explain the outcome of charge capture and emission measurements, the hydrogen release model is one of the most promising. This is mainly due to the fact, that the hydrogen release model is able to explain the recoverable as well as the permanent component, which contribute to the device degradation during BTI [64–68]. Furthermore, the hydrogen release model provides a potential explanation for the accumulation of fixed positive charges at the SiC-SiO_2 interface which occurs during high-temperature processing steps, as will be discussed in Chapter 4.

The hydrogen release model tries to link the permanent component, which arises during long-term gate stress, with the release of additional H from the gate into the oxide. A schematic overview of one of the possible mechanisms, which lead to an increase of the permanent component according to the H-release model is sketched in Fig. 1.9 [69]. First, a trapped proton in the oxide layer close to the gate electrode (A) may become neutralized if a gate potential is applied and the Fermi-level moves below the energy level of the trapped H^+ (B). The neutrally charged hydrogen can now be released from the trapping site by overcoming an energy barrier of approximately 1.5 eV (C). Afterwards, the released hydrogen diffuses through the oxide until it is able to occupy a new trapping site (D). It is important to note that potential trapping sites for the H are available all over the oxide due to the amorphous nature of SiO_2.

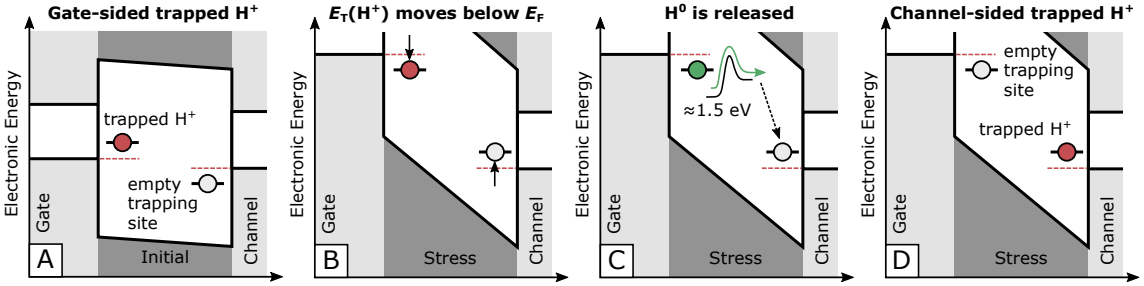


Fig. 1.9 Gate-sided H-release model [69]. A trapped proton in the oxide layer close to the gate (A, left, red) may become neutralized if the energetic position of the trapped proton is shifted below the Fermi-level (B). The neutrally charged H atom can now be released by overcoming an energy barrier of approximately 1.5 eV (C). Subsequently, the neutrally charged, free H atom moves towards the SiC/SiO_2 interface, where it occupies a new trapping site (D).

1.2.3 Hydrogen hopping

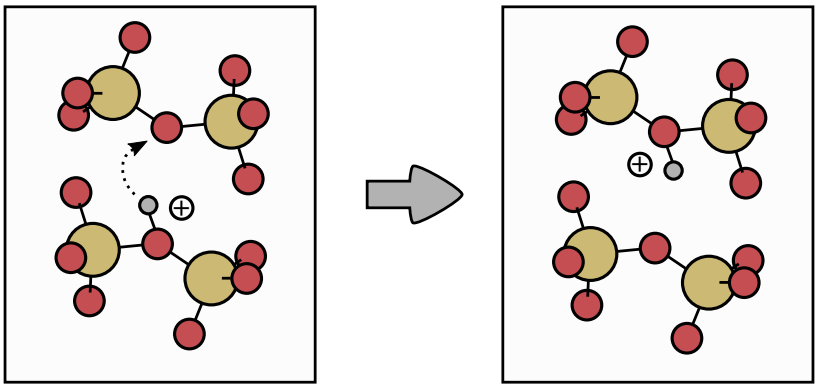


Fig. 1.10 Hopping mechanism for the case of a positively charged hydrogen H^+. Oxygen atoms are indicated in red, whereas silicon atoms are indicated in yellow. The hydrogen atom (grey) moves from one bridging O (initial configuration, left) to a neighboring bridging O atom (final configuration, right). H^+ can stick to nearly all oxygen atoms, whereas the neutrally charged hydrogen, H^0, can only bind to approximately 60 % of bridging O atoms in the SiO_2. The transition barrier for the hopping mechanism of the positive H^+ and neutral H^0 charge state is approximately 1.5 eV [48].

Although the high diffusivity of hydrogen in SiO_2 allows for a very fast exchange of H to a new trapping site and should therefore not limit the rate [70], there are very low barriers for the interstitial neutral H to bind at approximately every third O atom (< 0.1 eV). Therefore, neutral hydrogen would not be able to move efficiently in the SiO_2 system. However, the transport of hydrogen (either in the neutral H^0 or the positive H^+ charge state) is still possible via a so-called *hydrogen hopping* mechanism, meaning the hydrogen moves from one bridging O atom to the next bridging O atom. A sketch of the hopping mechanism for the case of a positively charged hydrogen atom (proton) is given in Fig. 1.10. The positive charged H atom can stick to nearly all bridging oxygen atoms in the system, whereas the neutrally charged hydrogen can only bind to approximately 60 % of the bridging O atoms. However, the activation energies for both transitions are similar and

around 1.5 eV. Due to this, it is not clear which charge state would dominate the transport mechanism [58].

1.3 Methodology

To understand the impact of various trapping centers on the electrical performance and reliability of SiC devices, numerous parameters were extracted using sophisticated measurement techniques. A brief overview on the available experimental setup and on how these electrical parameters were extracted is given in this section.

1.3.1 Measurement system

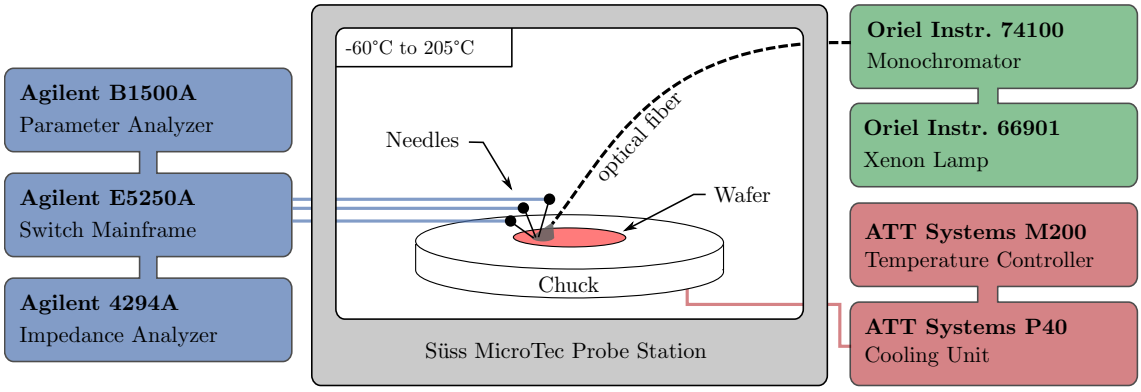


Fig. 1.11 Available instruments and measurement setup.

An overview on the available measurement equipment for all investigations in this thesis is given in Fig. 1.11. All measurements were performed using an Agilent B1500A parameter analyzer, which includes 4 high-resolution source-measurement units (SMUs) and one high-power SMU. All SMUs are connected to an Agilent E5250A switching matrix. For capacitance-voltage measurements an Agilent 4294A impedance analyzer was used, which is also connected to the switching matrix. An Oriel Instruments 66901 300 W xenon lamp in combination with an Oriel Instruments 74100 monochromator was used for measurements which require light at a specific wavelength (see Section 1.3.5). All measurements were performed within an Süss MicroTec probe station, where the temperature is controlled via an ATT Systems M200 temperature controller and an ATT Systems P40 cooling unit.

1.3.2 Layout considerations of SiC-power MOSFETs

Unlike in silicon power-MOSFETs, where the contribution of channel resistance R_{ch} to the total on-resistance R_{on} is negligible, the contribution of R_{ch} to the total R_{on} in SiC-MOSFETs is significant. Here up to approximately 50 % of the total on-resistance originates from the channel resistance due to the higher interface trap density and very low drift layer resistance. This results in the need for an increased die size, which consequently raises the chip costs due to the very expensive base material ($\approx$ 1000 \$ for a 150 mm wafer). Therefore, decreasing R_{ch} using different crystal-planes with higher mobility and shrinking the pitch size is of high importance for SiC based power-MOSFETs.

Typical device layouts used in commercially available SiC power MOSFETs are given in Fig. 1.12 and Fig. 1.13. A typical DMOS design is shown in Fig. 1.12 with the inversion

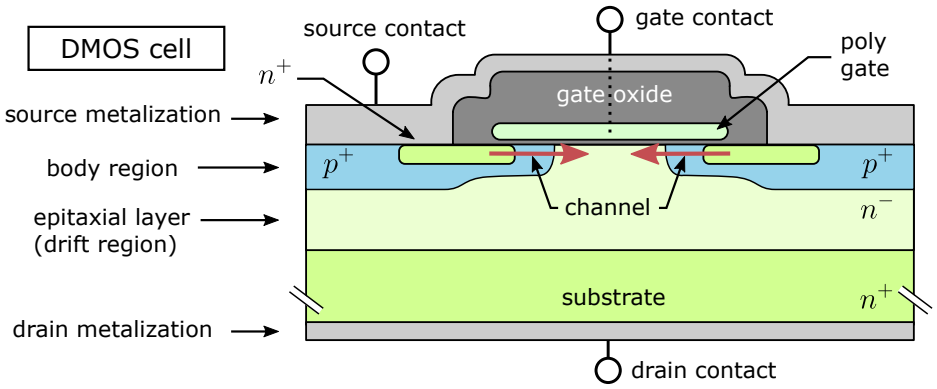


Fig. 1.12 Schematic cross section of a typical DMOS power-MOSFET layout. Here, the inversion channel forms on the (0001)-crystal plane (Si-face) at the surface of the SiC semiconductor.

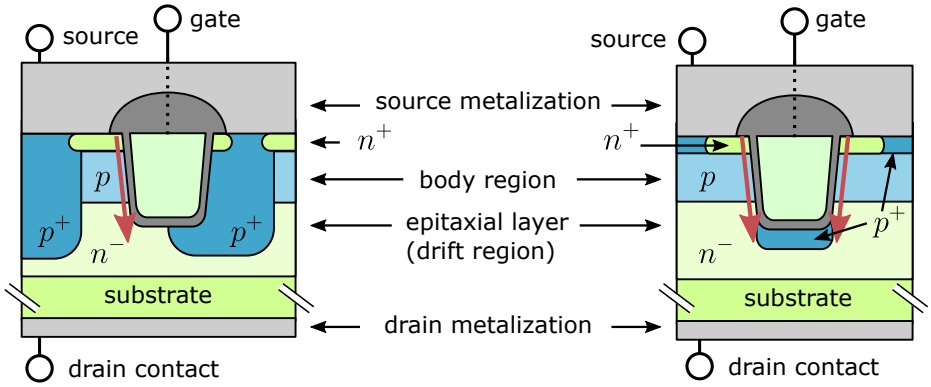


Fig. 1.13 Schematic cross section of two typical power-MOSFET trench layouts on SiC. Here, the inversion channel forms either on the $(11\bar{2}0)$ cyrstal plane (a-face, left) [71, 72], or on various crystal planes (right) [73].

channel (red-arrows) forming on the (0001)-crystal plane (or Si-face). The trench designs (sketched in Fig. 1.13) enable a smaller pitch size, and furthermore take advantage of the higher mobility on the non-polar crystal planes along the *c*-axis of the 4H-SiC crystal [74]. However, these trench devices require a p^+ doped region to shield the insulator at the bottom of the trench from the high electric fields, which arise in the n^- doped epitaxial drift layer in the off-state of the device due to the high drain potential usually applied in power applications [71–73, 75].

As will be shown in Chapter 2, the number of fast interface states with a fully reversible charge state depends strongly on the crystal plane of the inversion layer, and therefore on the device layout.

1.3.3 Transfer Characteristics

The transfer characteristics (I_D-V_Gs) represent the dependence of the drain current I_D on the gate voltage V_G at a fixed drain voltage V_D. Fig. 1.14 shows typical transfer characteristics of a SiC nMOSFET before (blue) and after a high temperature gate stress for several thousand seconds (shifted, green). The threshold voltage V_{th}, as a key parameter of a MOSFET, can be extracted from the I_D-V_Gs in manifold ways [76–81]. In this work,

V_{th} is extracted using either a linear extrapolation (as indicated in Fig. 1.14), or V_{th} is extracted via a defined readout current (e.g. 1 mA) at fixed drain voltage.

As already discussed in Section 1.2.1, a positive/negative bias stress results in a positive/negative threshold voltage shift ΔV_{th}, respectively. Assuming a parallel shift of the transfer characteristics after bias stress, which is usually the case for SiC-nMOSFETs, ΔV_{th} is given by

$$\Delta V_{\mathrm{th}} = V_{\mathrm{th}}^{2} - V_{\mathrm{th}}^{1}, \tag{1.7}$$

and the total number of charges trapped during the stress N_{t} can be easily obtained from the shift of the threshold voltage via

$$N_{\mathrm{t}} = \frac{\Delta V_{\mathrm{th}} C_{\mathrm{OX}}}{q} \tag{1.8}$$

with the oxide capacitance C_{OX}.

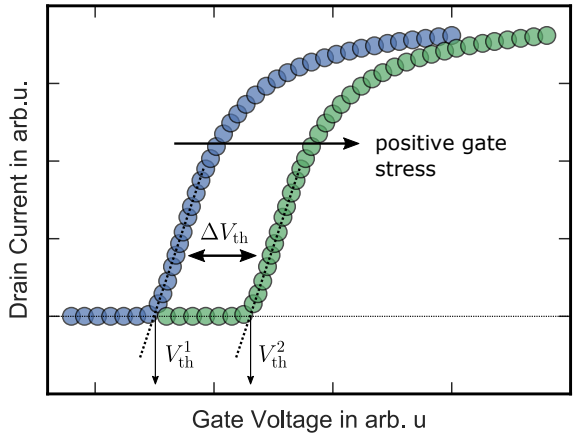


Fig. 1.14 Transfer characteristic of a SiC-nMOSFET.

The transfer characteristics are furthermore used for the evaluation of the low-field mobility μ_0 using the method of Ghibaudo [78]. He derived the linear function

$$\frac{I_{\mathrm{D}}}{\sqrt{g_{\mathrm{m}}}} = \sqrt{\frac{W C_{\mathrm{OX}} \mu_0 V_{\mathrm{D}}}{L}} (V_{\mathrm{th}}^{\mathrm{G}} - V_{\mathrm{th}}) \tag{1.9}$$

with the transconductance g_{m} and Ghibaudo's definition of the threshold voltage $V_{\mathrm{th}}^{\mathrm{G}}$. From (1.9), μ_0 is extracted as a fitting parameter from the slope of the linear function $I_{\mathrm{D}} \big/ \sqrt{g_{\mathrm{m}}}$ as indicated in Fig. 1.15 and Fig. 1.16. Note that in this thesis the term mobility always refers to the low-field mobility μ_0 unless otherwise stated.

1.3.4 Charge Pumping

Charge pumping (CP) is an electrical measurement method which was proposed by Brugler and Jespers in 1969 [82]. The technique is very well suited for the quantitative determination of interface and border states in MOSFETs and was recently demonstrated on SiC based devices [29, 83–86]. The next paragraph will give a short introduction to the measurement technique. More detailed information is given in [82, 87, 88].

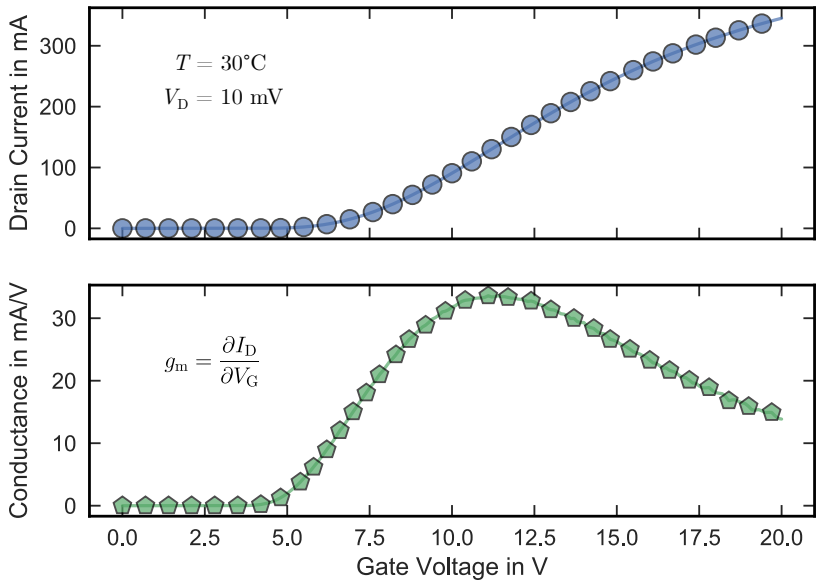


Fig. 1.15 Typical drain current I_D (blue, top) and transconductance g_m (green, bottom) characteristics of a MOSFET.

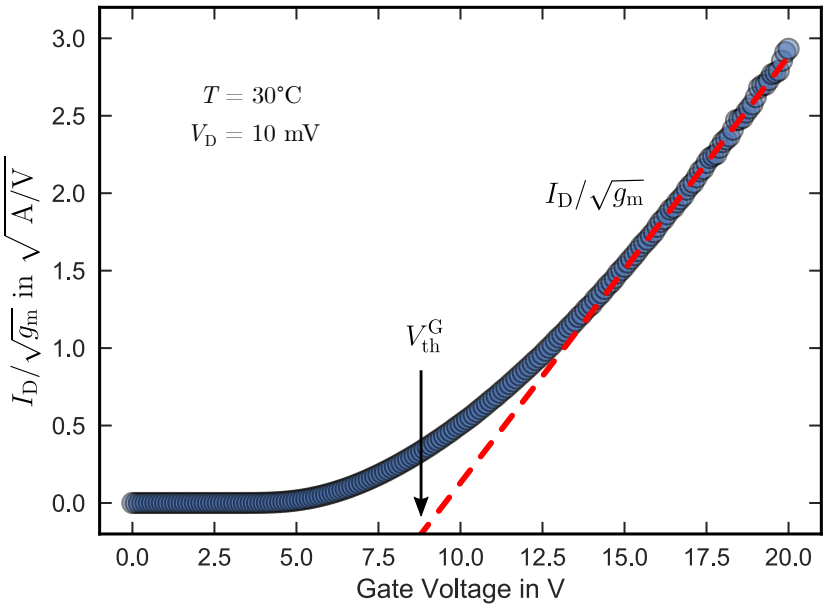


Fig. 1.16 Typical $I_D/\sqrt{g_m}$ characteristic illustrating the parameter extraction via a fit of (1.9) (dashed, red) according to the method of Ghibaudo [78].

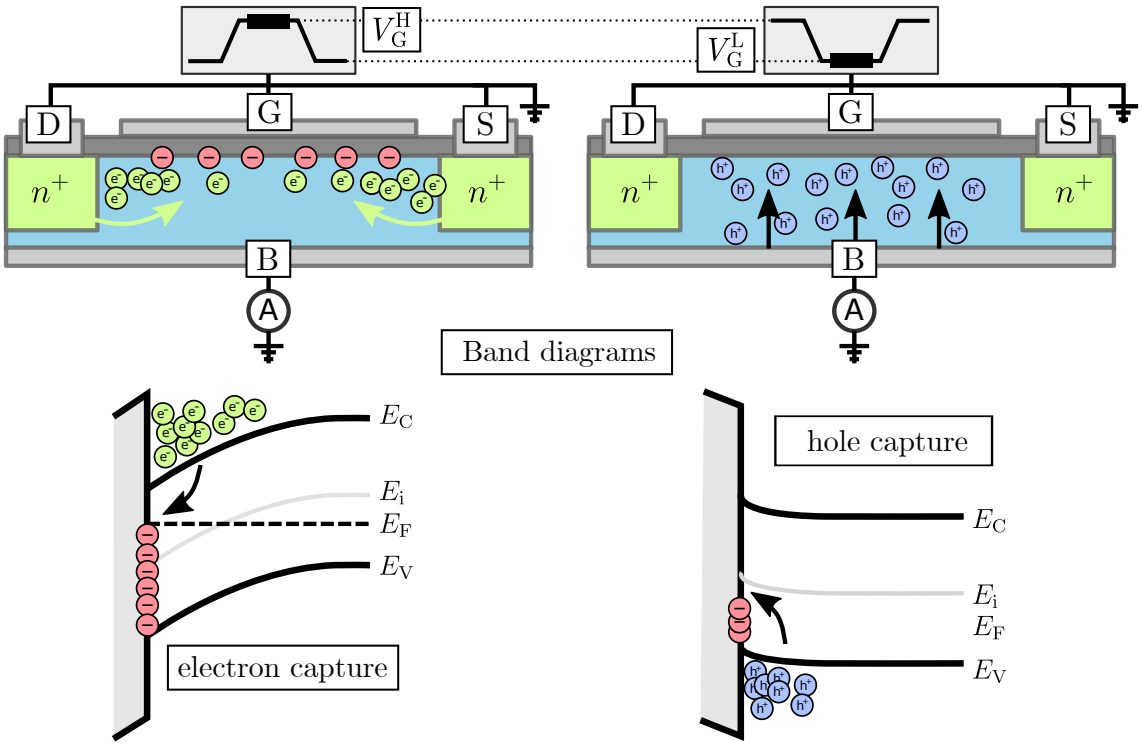


Fig. 1.17 Basic scheme of a CP measurement on a n-channel MOSFET. Left: during the high-level of the gate pulse, an inversion channel forms and minority carriers (electrons) are captured in interface/border states (red). Right: during the low-phase of the gate pulse, these trapped electrons recombine with incoming holes from the substrate resulting in an net current flow (= charge pumping current) from the bulk to the source/drain terminals.

The basic connection scheme of a CP measurement is sketched in Fig. 1.17 for an n-channel MOSFET. While source, drain and bulk terminals are grounded, the gate is pulsed at a frequency of several kHz from accumulation to inversion. During the high-phase of the gate pulse at V_G^H, electrons from source and drain are injected into the channel region of the device. Most of these electrons remain delocalized (free) in the semiconductors conduction band (green), while some get captured in interface or border states (red). As soon as the gate is switched back to accumulation at V_G^L, delocalized electrons flow back to the source or drain regions, while most of the trapped electrons remain captured during the falling edge of the gate pulse. These remaining trapped electrons recombine with incoming holes (blue) during the low-phase of the gate pulse, which results in a net current flow from source/drain to the bulk. In typical charge pumping measurements the gate is pulsed with frequencies ranging from 10 kHz to 1 MHz. Therefore, electrons are repeatedly "pumped" from the conduction band to the valence band via interface/border states resulting in an effective charge pumping current I_{CP} at the bulk terminal. The maximum charge pumping current I_{CP}^{max} is directly proportional to the total number of trapped charges per unit area N_{CP} at the semiconductor-insulator interface according to

$$I_{CP}^{max} = qA_G^{eff} f N_{CP}. \tag{1.10}$$

Here, A_G^{eff} represents the effective gate area, f is the frequency of the gate pulse and q is the elementary charge.

Spectroscopic Charge Pumping

Spectroscopic charge pumping is a tool for the measurement of the energetic distribution of interface traps in MOS systems, which was proposed by Van den Bosch and Groeseneken in 1991 [89]. It is based on the fact that the mean density of interface states $\overline{D_{\mathrm{it}}}$ is always given within a well defined energetic fraction of the band gap according to

$$\overline{D_{\mathrm{it}}} = q\frac{N_{\mathrm{CP}}}{\Delta E_{\mathrm{CP}}}. \tag{1.11}$$

This energetic range within the band gap is called the active energy window ΔE_{CP} given by

$$\Delta E_{\mathrm{CP}} = E_{\mathrm{G}} - 2k_{\mathrm{B}}T\ln\left(\sqrt{\nu_{\mathrm{thn}}\nu_{\mathrm{thp}}}\sqrt{\sigma_{\mathrm{n}}\sigma_{\mathrm{p}}}\sqrt{N_{\mathrm{C}}N_{\mathrm{V}}}\frac{V_{\mathrm{TH}}^{\mathrm{CP}} - V_{\mathrm{FB}}^{\mathrm{CP}}}{\Delta V_{\mathrm{G}}}\sqrt{t_{\mathrm{r}}t_{\mathrm{f}}}\right) \tag{1.12}$$

with the band gap E_{G}, the thermal drift velocity of electrons and holes, ν_{thn} and ν_{thp}, the capture cross section of electrons and holes, σ_{n} and σ_{p}, the charge-pumping threshold and flatband voltages $V_{\mathrm{TH}}^{\mathrm{CP}}$ and $V_{\mathrm{FB}}^{\mathrm{CP}}$, the amplitude of the gate pulse ΔV_{G} and the rise and fall times of the gate pulse, t_{r} and t_{f}.

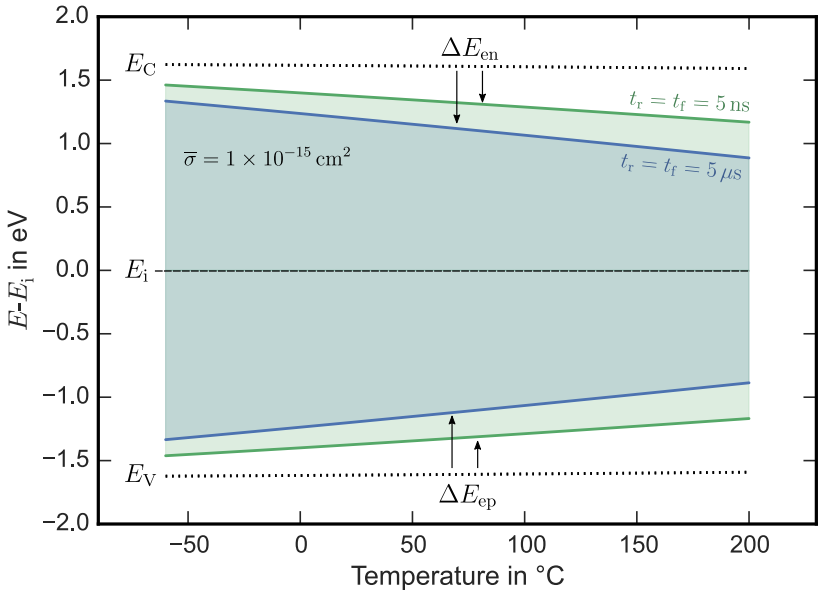


Fig. 1.18 Temperature dependence of the active energy window ΔE_{CP} between −60 °C and 200 °C for 2 different rise and fall times. ΔE_{CP} narrows with increasing temperature and rise/fall times, which furthermore results in a decreasing charge pumping current.

The upper boundary of ΔE_{CP} is given by

$$\Delta E_{\mathrm{en}} = E_{\mathrm{C}} - k_{\mathrm{B}}T\ln\left(\nu_{\mathrm{thn}}\sigma_{\mathrm{n}}N_{\mathrm{C}}\frac{V_{\mathrm{TH}}^{\mathrm{CP}} - V_{\mathrm{FB}}^{\mathrm{CP}}}{\Delta V_{\mathrm{G}}}t_{\mathrm{f}}\right), \tag{1.13}$$

whereas the lower boundary of ΔE_{CP} is given by

$$\Delta E_{\mathrm{ep}} = E_{\mathrm{V}} + k_{\mathrm{B}}T\ln\left(\nu_{\mathrm{thp}}\sigma_{\mathrm{p}}N_{\mathrm{V}}\frac{V_{\mathrm{TH}}^{\mathrm{CP}} - V_{\mathrm{FB}}^{\mathrm{CP}}}{\Delta V_{\mathrm{G}}}t_{\mathrm{r}}\right). \tag{1.14}$$

It is important to note that in (1.13) and (1.14), also the drift velocities $\nu_{\mathrm{th}i}$, the capture cross sections σ_i, and the effective density of states in the conduction band N_C and valence band N_V depend on T. Therefore, the upper and lower boundaries of ΔE_CP can be easily adjusted by changing the temperature or the rise and fall times of the gate pulse. This allows for a spectroscopic scan of the D_it within a certain range of the semiconductors band gap. Fig. 1.18 shows the temperature dependence of ΔE_CP between $-60\,^\circ\mathrm{C}$ and $200\,^\circ\mathrm{C}$ for two fixed pulse slopes of $t_\mathrm{f} = t_\mathrm{r} = 5\,\mathrm{ns}$ and $t_\mathrm{f} = t_\mathrm{r} = 5\,\mu\mathrm{s}$.

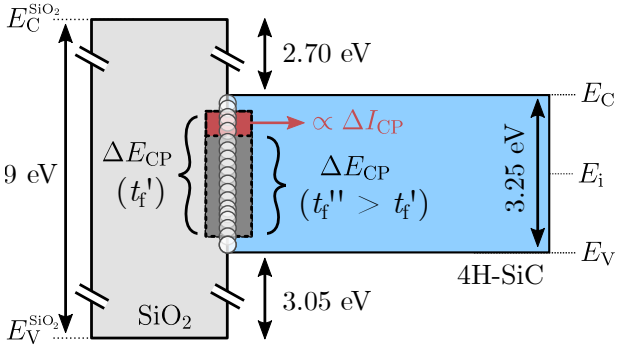


Fig. 1.19 Active energy window for two different gate-pulse fall times t_f' and t_f''. For the slower fall time t_f'' the upper boundary of ΔE_CP moves away from the conduction band edge.

Fig. 1.19 illustrates, how this effect is used in spectroscopic CP to obtain the energetic distribution of the interface/border trap states in the upper half of the band gap. The same formalism holds for the lower part of the band gap by replacing t_f with t_r. At a fixed T and rise time t_r, the charge pumping measurement is performed two times with two different fall times t_f' and t_f'', with t_f' being the faster, and t_f'' the slower one. For t_f', ΔE_CP is given by $\Delta E_\mathrm{CP}(t_\mathrm{f}')$, whereas for the slower fall time t_f'', the upper boundary of the active energy window, ΔE_en, is further away from the SiC conduction band due to (1.13), which results in the narrower active energy window $\Delta E_\mathrm{CP}(t_\mathrm{f}'') < \Delta E_\mathrm{CP}(t_\mathrm{f}')$. Due to this, traps which are located within the energetic range

$$\Delta E = \Delta E_\mathrm{CP}(t_\mathrm{f}') - \Delta E_\mathrm{CP}(t_\mathrm{f}'') = k_\mathrm{B} T \ln\left(\frac{t_\mathrm{f}''}{t_\mathrm{f}'}\right) \tag{1.15}$$

do not contribute to the charge pumping current in the measurement with t_f''. Therefore, the difference between both charge pumping currents

$$\Delta I_\mathrm{CP} = I_\mathrm{CP}(t_\mathrm{f}') - I_\mathrm{CP}(t_\mathrm{f}'') \tag{1.16}$$

is directly proportional to the $\overline{D_\mathrm{it}}$ within ΔE. A spectroscopic scan along a large fraction of the SiC band gap is now easily possible by varying T, which moves the energetic position of ΔE along the band gap. Therefore, the energetic resolution of spectroscopic charge pumping is given by ΔE, which also depends on T but can be reduced by minimizing $|t_\mathrm{f}'' - t_\mathrm{f}'|$ according to (1.15).

1.3.5 Photo-assisted capacitance voltage profiling

Common techniques for the analysis of capacitance-voltage (CV) curves, like the high-frequency Terman method [90], do not work well in wide band gap semiconductors such as

SiC [91]. The Terman technique is based on the assumption that the interface states are not able to follow the small, high frequency AC signal, whereas they follow changes in the overlaying DC bias. For wide band gap semiconductors like SiC, this assumption leads to a significant underestimation of the interface state density because deep states can not follow changes in the DC bias. For a measurement at room temperature and a very slow slew rate of 10 s/V the Terman technique can accurately measure only between 0.2 eV and 0.6 eV above E_V, which is less than 15 % of the 4H-SiC bandgap [91].

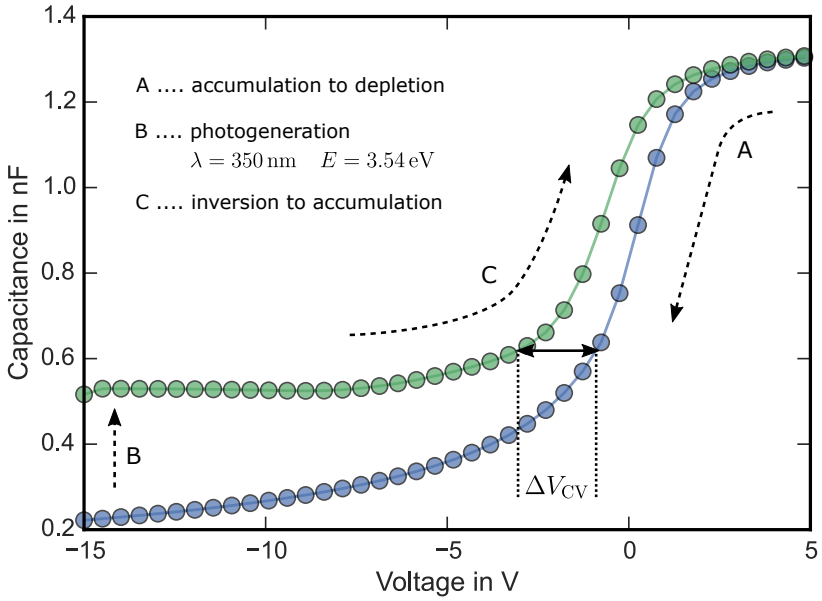


Fig. 1.20 Photo-assisted CV measurement on an n-MOS capacitor. After the sweep from accumulation to depletion in the dark (A), the sample is illuminated with 350 nm light while the bias is kept at −15 V. Due to the generation of minority carriers, and therefore the formation of an inversion layer, the capacitance increases (B). The hysteresis ΔV_{CV}, which occurs in the following sweep back to accumulation in the dark, can be used to estimate the density of interface/border traps.

A more promising and simpler to use method for a quick estimation of the number of interface/border states N_{it} across the band gap at room temperature is the *photo-assisted* CV technique [92–96]. A typical photo-CV curve is illustrated in Fig. 1.20 for a n-type 4H-SiC MOS capacitor. The voltage is swept from accumulation to deep depletion in the dark, which results in the blue curve (A). Due to the low thermal generation rate of minority carriers in wide band gap semiconductors like 4H-SiC, no inversion layer is formed within a reasonable amount of time at room temperature. Therefore, the sample is illuminated with 350 nm (corresponding to 3.54 eV) light to populate the inversion layer via photogeneration while the bias is held at −15 V. The formation of the inversion layer is visible as a rise in the capacitance towards an equilibrium value (B). After the inversion layer is fully formed, the light is turned off and the voltage is swept back to accumulation in the dark, which results in the green curve (C). Here, a voltage shift ΔV_{CV} occurs between both curves, which is caused by minority carriers (in this case holes) trapped in interface states [97, 98]. The number of trapped states N_{it} per cm^2 can be estimated via

$$N_{it} = C_{OX} \frac{\Delta V_{CV}}{q} \ . \tag{1.17}$$

CHAPTER 2

On the first Component: the Subthreshold Hysteresis

Contents

Abstract. MOSFETs based on 4H-SiC show a subthreshold drain current hysteresis between gate voltage sweeps from accumulation to inversion (up-sweep) and gate voltage sweeps from inversion to accumulation (down-sweep). The observed hysteresis between the up- and down-sweep can be expressed as a *subthreshold* voltage shift and may reach several volts. The subthreshold voltage shift is caused by hole capture in fast interface states during accumulation and is directly proportional to the charge pumping signal. To total number of interface states strongly depends on the crystal plane, on which the inversion channel forms. Furthermore, the observed voltage shift is fully recoverable via a gate bias above the threshold voltage and does not impact device reliability even after thousands of charging/discharging cycles. Based on work by Gruber and Cottom, carbon dangling bonds are suggested as a possible defect candidate [5, 99].

2.1 Occurrence of the hysteresis

State of the art power MOSFETs based on SiC show a drain current sweep hysteresis between gate voltage V_G sweeps from accumulation to inversion and vice versa. An example of this phenomenon is given in Fig. 2.1 for a V_G sweep from $-5\,V$ to $5\,V$ (up-sweep, blue) and from $5\,V$ to $-5\,V$ (down-sweep, red) at a fixed drain voltage V_D of $0.1\,V$. The hysteresis is mainly visible in the subthreshold regime where the on-resistance R_{on} of the device is still in the range of several megaohms and becomes less significant as the gate voltage approaches the threshold voltage V_{th}. Above V_{th}, which is approximately at $V_G = 3\,V$ for the tested device, the hysteresis disappears completely (inset).

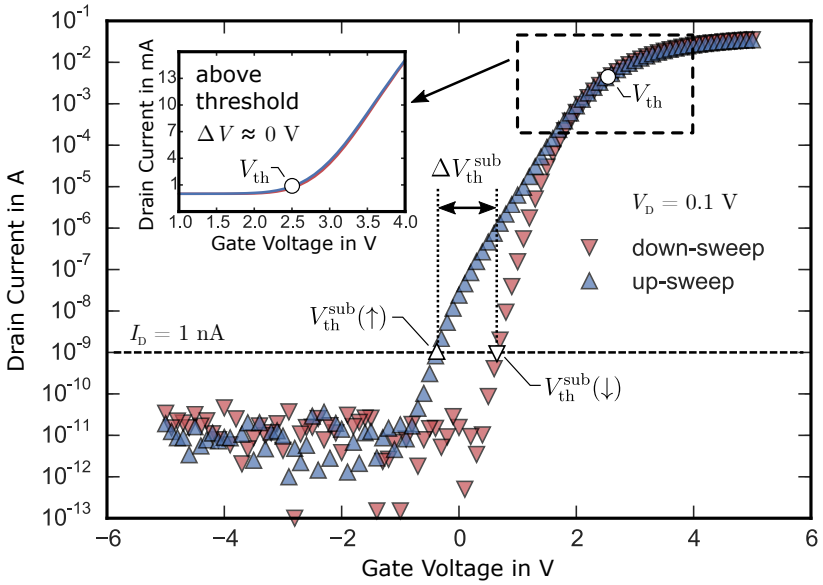


Fig. 2.1 Sweep hysteresis between the up-sweep starting at $-5\,V$ (blue, rectangles up) and the down-sweep starting at $5\,V$ (red, rectangles down). The dashed horizontal line represents the readout current of V_{th}^{sub} at $1\,nA$. The inset shows the input characteristics in linear scale above the threshold voltage where the hysteresis effect vanishes.

In the next sections, we define the gate voltage at which the drain current I_D reaches 1 nA, at a fixed drain voltage of 0.1 V, as subthreshold voltage V_{th}^{sub}

$$V_{th}^{sub} = V_G(I_D = 1\,\text{nA}). \tag{2.1}$$

Note that the difference between V_{th}^{sub} and V_{th} is the extraction current at the drain terminal. V_{th} is extracted at a drain current of 1 µA and represents the "real" threshold voltage of the devices. On the other hand, V_{th}^{sub} is extracted in the subthreshold regime at a drain current of 1 nA. The subthreshold voltage depends on the sweep direction as indicated in Fig. 2.1. A gate sweep in the positive direction from accumulation to inversion (up-sweep, ↑) starting at $V_G = -5\,\text{V}$ results in a $V_{th}^{sub}(\uparrow)$ of −400 mV, whereas a gate sweep in the negative direction from inversion to accumulation (down-sweep, ↓) starting at $V_G = 5\,\text{V}$ leads to a $V_{th}^{sub}(\downarrow)$ of +600 mV. The total hysteresis between the up-sweep (↑) and the down-sweep (↓) is expressed as a subthreshold voltage shift ΔV_{th}^{sub}

$$\Delta V_{th}^{sub} = V_{th}^{sub}(\uparrow) - V_{th}^{sub}(\downarrow). \tag{2.2}$$

In the example given in Fig. 2.1, this corresponds to $\Delta V_{th}^{sub} = -1\,\text{V}$.

Although the presence of ΔV_{th}^{sub} is an outstanding difference between state-of-the-art SiC and Si based MOSFETs, the effect is poorly investigated and little to no literature on this specific topic is available. However, for a comprehensive knowledge on performance and reliability limiting factors of state-of-the-art and future devices, a deeper understanding on the subthreshold hysteresis mechanism is required.

2.2 Investigated devices

All devices produced *in-house* were fabricated on 4H-SiC n-doped substrates using an industrial process. To analyze the impact of the crystal orientation on the electrical properties, MOSFETs with a lateral and trench design were used. A schematic cross section of the devices is shown in Fig. 1.12 and Fig. 1.13. For the DMOS design (Fig. 1.12), the inversion channel forms on the (0001) crystal plane (referred to as Si-face), wheres for the trench design (Fig. 1.13, left) the channel forms on the $(11\bar{2}0)$ crystal plane (referred to as a-face). All devices received a SiO_2 dielectric deposited via chemical vapor deposition (CVD) and an optimized post oxidation anneal (POA) was done in a NO containing atmosphere for all samples.

To make sure the hysteresis phenomenon is not only a peculiar feature of our devices, a comparison with various SiC power MOSFETs available on the market is given in Section 2.8. The investigated devices were purchased from three different manufactures and *randomly* labeled A, B, and C to maintain manufacturer anonymity.

In Section 2.6.2, the density of interface states is extracted using charge pumping measurements [82] by using smaller variants of the in-house devices. Therefore, smaller, but otherwise identical MOSFETs with a distinct bulk pad were produced. Here, the Si-face devices have a gate length L of 6 µm and a gate width W of 100 µm and the a-face devices have a gate length of 0.5 µm and a gate width of 30 µm. All measurements are performed on wafer level using an Agilent B1500A parameter analyzer, an Agilent E5250A switching matrix and an Agilent 4294A impedance analyzer at room temperature unless otherwise stated. Temperature sweeps between −60 °C and 205 °C are performed via an ATT Systems P40 cooling unit. A more detailed description of the measurement system is provided in Section 1.3.1.

2.3 Gate voltage dependence

We start by analyzing the dependence of the subthreshold voltage on the starting gate voltage (low-level) of the sweep from accumulation to inversion (up-sweep, ↑). Fig. 2.2 shows the drain current I_D during a gate voltage sweep starting at varying negative gate bias to $V_G = 4\,V$ (up-sweep, blue) and from $V_G = 4\,V$ back to varying negative bias (down-sweep, red) at a drain voltage V_D of 0.1 V. The measurement pattern is sketched in the inset of Fig. 2.2: the down-sweep was performed with a slope of $-1\,V/100\,ms$ right after the up-sweep with a slope of $0.1\,V/100\,ms$. While monitoring the gate voltage level at which $I_D = 1\,nA$, $V_{th}^{sub}(\uparrow)$, we observe a shift of $V_{th}^{sub}(\uparrow)$ to more negative gate voltages the more negative the up-sweep starting voltage.

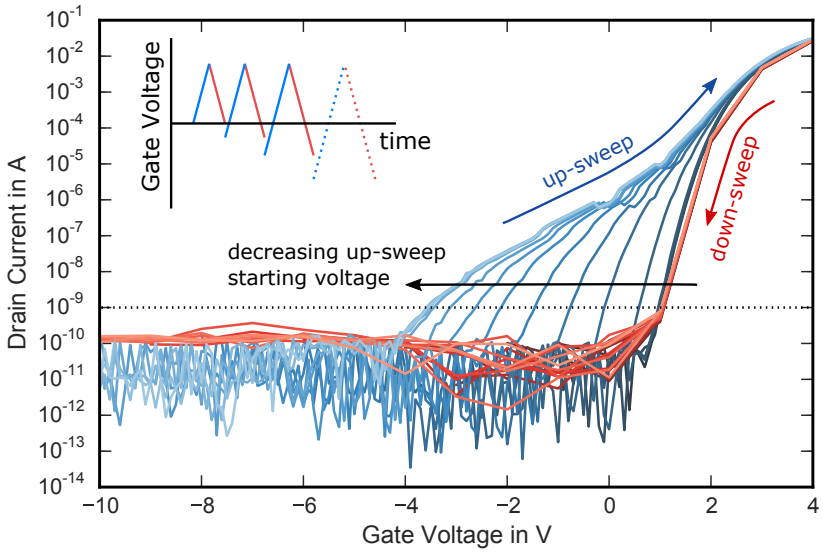


Fig. 2.2 Increase of the sweep hysteresis depending on the starting voltage of the up-sweep from accumulation to inversion (blue). The inset shows the measurement procedure which consists of gate voltage sweeps with varying low level but constant high level. The down sweep from inversion to accumulation is indicated in red. Drain voltage was set to 100 mV.

So far, the effect is consistent with negative bias temperature instability (NBTI), which occurs on all MOS technologies, meaning a negative gate stress results in a negative shift of the threshold voltage. However, there are multiple deviations from the typical NBTI behavior regarding the observed hysteresis effect. One of which is the dependence of the subthreshold voltage shift ΔV_{th}^{sub} on the up-sweep starting voltage as shown in Fig. 2.3. As long as the up-sweep starting voltage is higher or equal to $-3\,V$, no ΔV_{th}^{sub} is observed. Decreasing the up-sweep starting voltage below $-3\,V$ leads to a growth of the hysteresis. From this point on, ΔV_{th}^{sub} grows linearly with decreasing up-sweep starting voltage until it saturates for gate voltages $V_G \leq -12\,V$, meaning any further decrease of the gate voltage does not lead to an increase in ΔV_{th}^{sub}. Furthermore, the hysteresis is independent of the high level of the gate pulse as long as it is above the threshold voltage V_{th}. From the maximum ΔV_{th}^{sub} of approximately $-4.5\,V$ and (1.8), we extract a density of trapped charges of $N_t \approx 1.5 \times 10^{12}\,cm^{-2}$ assuming all charges are captured at the SiC/SiO_2 interface.

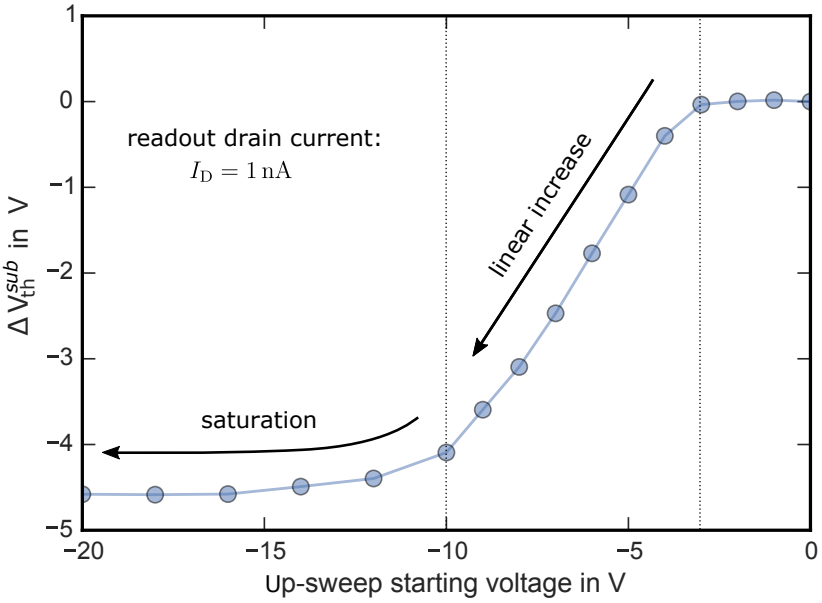


Fig. 2.3 Subthreshold voltage shift extracted from the data in Fig. 2.2 at a drain current of 1 nA (dotted line) as a function of the up-sweep starting voltage. The hysteresis starts to increase linearly with decreasing up-sweep starting voltage as soon as it falls below −3 V and saturates for up-sweep starting voltages below −15 V, where accumulation is reached (see Fig. 2.4). Decreasing the up-sweep starting voltage below −15 V does not lead to any significant increase in the hysteresis.

The mechanism behind the hysteresis growth becomes more clear by analyzing the CV curves. Fig. 2.4 shows a schematic CV curve (red) with an inset of the hysteresis curve (blue). The hysteresis in the up-sweep emerges as soon as the starting voltage falls below the intrinsic Fermi level E_i (in this case $V_G \leq -3\,V$). As a consequence of the further decreasing gate voltage, the density of holes at the SiC/SiO_2 interface becomes larger than the density of electrons at the interface allowing for hole capture in interface and/or border traps. The process becomes increasingly more efficient until strong accumulation is reached at approximately −15 V and the hysteresis saturates. The explanation of the observed hysteresis by hole capture is consistent with the sign of the threshold voltage shift: a positive charge captured at the interface acts like an additional positive gate potential resulting in a negative threshold voltage shift.

2.3.1 The difference to silicon based devices

There are two reasons why the hysteresis is a feature only observed on SiC based MOSFETs:

- The first reason is the much larger interface trap density D_{it} of SiC based devices compared to their silicon based counterparts. For the Si/SiO_2 system typical trap densities are in the range of $10^9\,eV^{-1}\,cm^{-2}$ to $10^{10}\,eV^{-1}\,cm^{-2}$ [30, 65]. This is mainly attributed to the very efficient hydrogen anneal used for the interface passivation in silicon based devices [100–104]. For the SiC/SiO_2 system, on the other hand, the aforementioned hydrogenation is not nearly as effective [105–108]. Although there are other passivation gases like nitric oxide (NO), D_{it} in SiC based devices remains

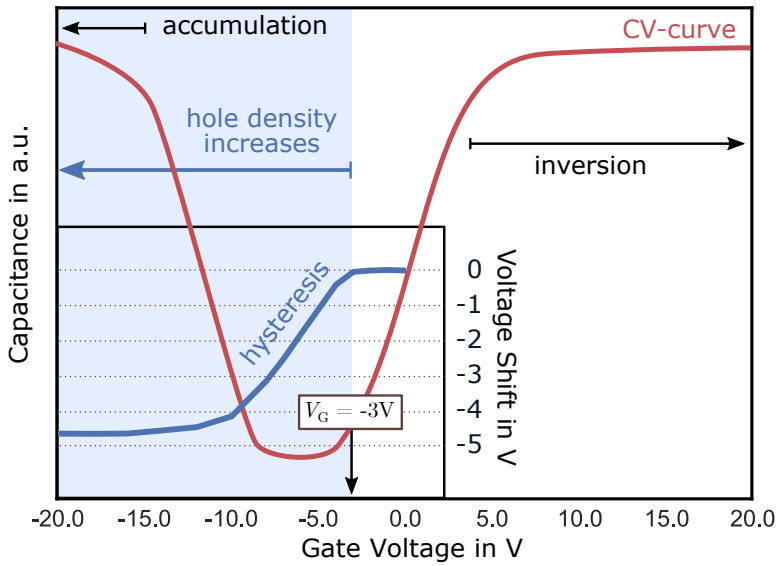


Fig. 2.4 Normalized capacitance voltage CV curve (red) with a inset of the subthreshold voltage shift (blue) as given in Fig. 2.3. The hysteresis starts to grow, as soon as the up-sweep starting voltage falls below $V_G < -3\,V$ and holes become available at the interface. Furthermore, the hysteresis saturates as soon as the system approaches strong accumulation, which is the case for gate voltages below $V_G = -15\,V$.

several orders of magnitude higher and is usually in the range of $10^{11}\,eV^{-1}\,cm^{-2}$ to $10^{12}\,eV^{-1}\,cm^{-2}$ [86, 109–111].

- The second reason is the three times larger bandgap of SiC compared to Si. The expected hysteresis ΔV_{th}^{sub} is connected to the number of trapped charges N_t at the interface by

$$\Delta V_{th}^{sub} = q\frac{N_t}{C_{OX}} = \frac{Q_{it}}{C_{OX}} = q\frac{D_{it}\Delta E_G t_{OX}}{\varepsilon_0 \varepsilon_r^{SiO_2}} \tag{2.3}$$

with the elementary charge q, the vacuum permittivity ε_0, the relative permittivity of SiO_2, $\varepsilon_r^{SiO_2}$, the oxide thickness t_{OX} and the total amount of interface charge Q_{it}, which is given by

$$Q_{it} = qN_t = qD_{it}\Delta E_G \tag{2.4}$$

with the density of interface/border traps D_{it} within the energetic window ΔE_G. The expected hysteresis can be estimated for both technologies by applying (2.3). Assuming an oxide thickness of approximately 70 nm, which is a typical value for power devices, and a band gap of 1.1 eV for Si, one ends up with an expected hysteresis on silicon devices which ranges from 3 mV to 35 mV. For SiC based devices on the other hand, with a band gap of 3.2 eV, the expected hysteresis ranges from 1 V to 11 V. For simplicity, we assumed $\Delta E_G = E_G$ and a uniform trap distribution. In reality, ΔE_G and thereby ΔV_{th}^{sub} depends on multiple parameters like the Fermi level position during the measurement, trap distributions and the time delay of the measurement as will be discussed in the next sections.

2.4 Time and temperature dependence

As shown in Fig. 2.3, biasing the device in accumulation ($V_G = -15\,V$) is sufficient to completely charge the interface states and observe the maximum hysteresis. The positive charging of the interface states at this voltage level happens within several nanoseconds [112], and can therefore not be resolved due to the technical limitations of our measurement setup. Due to this, the next sections focus on the time and temperature dependence of the recovery, assuming the interface is always completely positively charged, which will be the case after an accumulation pulse longer than approximately 500 ns [112].

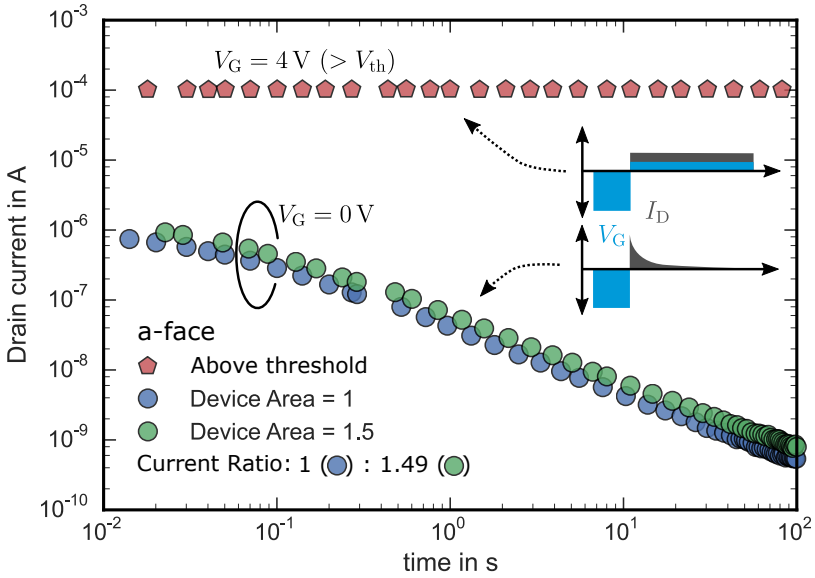


Fig. 2.5 Recovery of the drain current at gate voltages below and above the threshold voltage after a charging pulse at $V_G = -15\,V$ for 1 s on an a-face device. The same trend is observed on Si-face devices. The green data corresponds to a device with a 50 % increased active area. The measurement pattern is depicted in the inset.

To analyze the time dependence of the hysteresis recovery, we start with the worst case scenario: a bias switch from strong accumulation with a completely positively charged interface to (a) the threshold voltage, or (b) 0 V. The outcome is shown in Fig. 2.5. For a bias switch from $V_G = -15\,V$ to $V_G = 4\,V$, which is slightly above the threshold voltage. In this case, I_D is stable over time (red, pentagons) and the hysteresis has already fully recovered before the experimental time window, which starts 20 ms after the bias switch from $V_G = -15\,V$ to $V_G = 4\,V$. On the other hand, switching from $V_G = -15\,V$ to $V_G = 0\,V$ results in measurable drain current transients due to the hysteresis effect (green and blue). Typically I_D should be lower than $1 \times 10^{-10}\,A$ at $V_G = 0\,V$. However, due to the negative shift of $V_{th}^{sub}(\uparrow)$ caused by trapped positive charges, a drain current of approximately 1 µA is detected 20 ms after switching the bias from $V_G = -15\,V$ to $V_G = 0\,V$. The drain current transients are only visible due to the very slow detrapping of charges for Fermi level positions away from the SiC conduction band edge, which is the case for a gate voltage around 0 V.

From Fig. 2.5 it is also clear that the hysteresis does not change with the active device area. This is proven via the green and blue data traces (circles), which represent two a-face devices with different active area but otherwise identical. The drain current scales perfectly

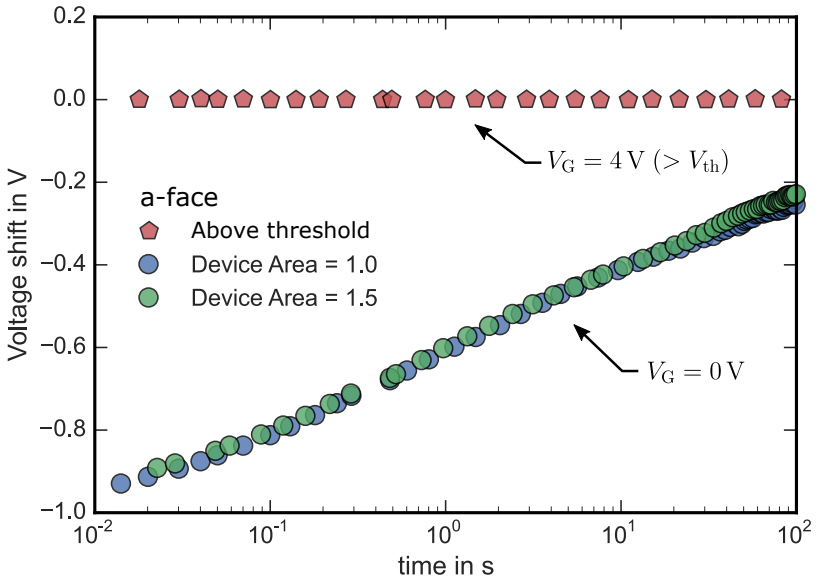


Fig. 2.6 Voltage shift according to the recovery of the drain current in Fig. 2.5. The voltage shift is independent of the active area (circles) and disappears for gate voltages above the threshold voltage (red, pentagons) indicating a uniform distribution of the drain current over the entire active device area.

with device area indicating a uniform distribution of the current over the whole device. The corresponding voltage shift at $V_G = 0\,V$ is shown in Fig. 2.6 and is identical for both devices. This proves that the hysteresis is not due to a local device leakage current caused by localized electric field variations, which might for example occur at the edges of the device, but is uniformly distributed over the entire active device area. The voltage shift at $V_G = 0\,V$ recovers slowly with approximately 175 mV per decade in time. Detrapping until the drain current falls below the measurable window takes at least 1000 s.

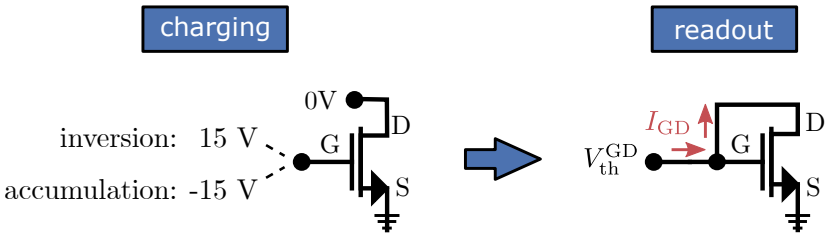


Fig. 2.7 Measurement schematics for the extraction of the hysteresis using a gated diode circuit. The gate is either charged in strong-inversion (15 V) or in accumulation (−15 V) for a charging time of 1 s with grounded source and drain terminals (left). Afterwards, $V_{th}^{GD}(\downarrow)$ or $V_{th}^{GD}(\uparrow)$, respectively, is extracted by forcing various current levels I_{GD} using the gated diode circuit with the drain connected to the gate contact.

2.4.1 Hysteresis after strong inversion

Before we discuss the more complicated hysteresis effect after an accumulation pulse in more detail, we start by analyzing the threshold voltage instability after a positive bias pulse above threshold (inversion). In this case, the gate bias is switched from strong

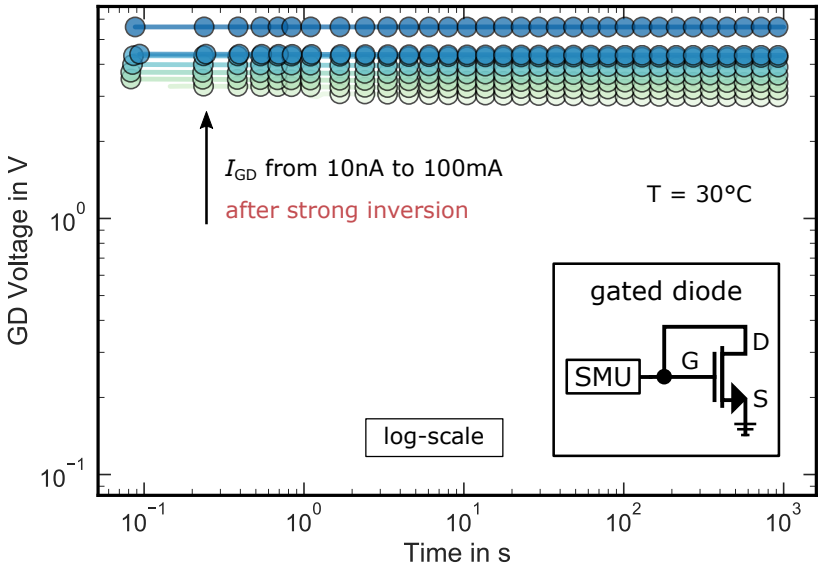


Fig. 2.8 Gated-diode voltage $V_{\mathrm{th}}^{\mathrm{GD}}(\downarrow)$ at various current levels I_{GD} ranging from 10 nA to 100 mA for 1000 s after charging the gate in strong-inversion at 15 V for 1 s. $V_{\mathrm{th}}^{\mathrm{GD}}(\downarrow)$ is nearly stable within the measurement window. All traces have been recorded using a *gated diode* circuit, which shorts the gate and drain contacts of the devices as indicated in the inset.

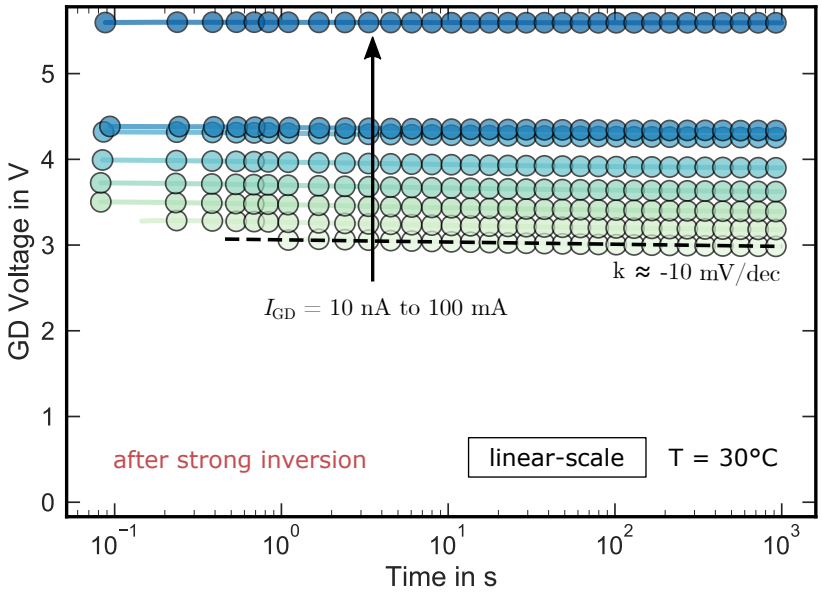


Fig. 2.9 Same as Fig. 2.8 but now with linear y-scale. Only a small remaining recovery slope of approximately $\Delta V_{\mathrm{th}}^{\mathrm{GD}}(\downarrow) \approx -10\,\mathrm{mV/dec}$ is visible due to charge emission form trap states, which captured an electron during the preceding inversion pulse.

inversion to a fixed readout current at which ${V_{\mathrm{th}}}^{\mathrm{GD}}(\downarrow)$ is extracted. Here, the superscript GD indicates that a *gated-diode* circuit is used for the readout of the threshold voltage ${V_{\mathrm{th}}}^{\mathrm{GD}}(\downarrow)$ to keep the inversion carrier density in the channel constant during the readout. The stress/measurement schematics are shown in Fig. 2.7. At first, the interface is charged

in strong inversion at $V_G = 15\,V$ for 1 s while the source and drain terminals are grounded (left). Afterwards, the connection scheme is changed to the gated diode configuration using a switching matrix and a current I_{GD} is forced at the shorted drain/gate terminals while the corresponding voltage at these terminals, $V_{th}^{GD}(\downarrow)$, is monitored. Note that no gate-leakage current flows if a current I_{GD} is forced during the gated-diode configuration. Instead, the potential at the gate terminal rises until the inversion channel forms. From this point on, the forced I_{GD} flows exclusively from drain to source, as indicated by the red arrows in Fig. 2.7.

Fig. 2.8 and Fig. 2.9 shows the $V_{th}^{GD}(\downarrow)$ transients in logarithmic and linear y-scale at various forced current levels I_{GD} ranging from 10 nA to 100 mA for 1000 s. $V_{th}^{GD}(\downarrow)$ is immediately stable within our measurement window. Only a small remaining recovery slope of approximately $\Delta V_{th}^{GD}(\downarrow) \approx -10\,mV/dec$ is visible due to charge emission from border/oxide traps, which captured an electron during the preceding strong inversion pulse. This behavior is the typical voltage recovery, which occurs after positive bias stress as will be discussed in more detail in Chap. 3. A basic overview is provided in Section 3.

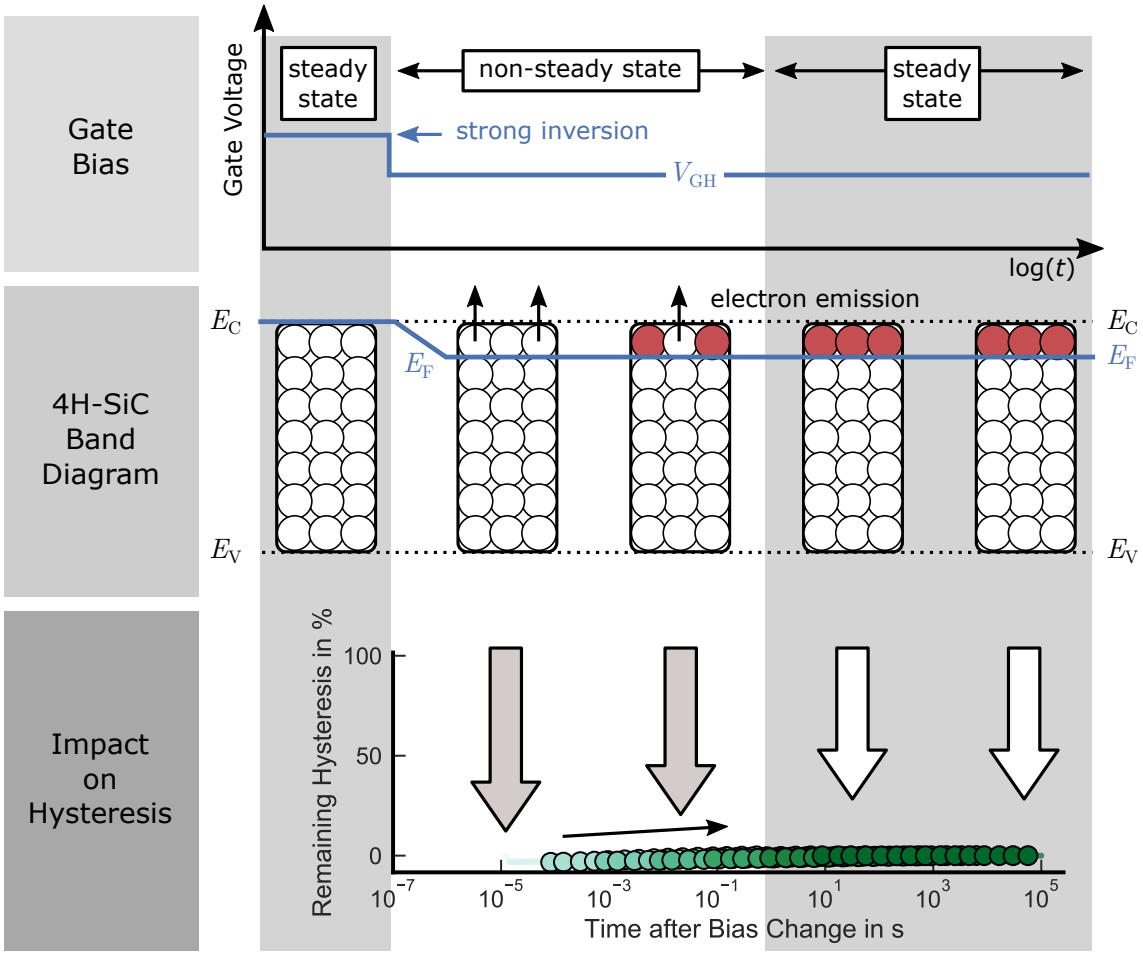


Fig. 2.10 Schematic illustration of the interface charging state after switching the gate bias from strong inversion to inversion. The change in gate voltage is indicated at the top. The observed instability (bottom) is mainly defined by electron emission from trap states close to the conduction band edge (middle).

The interface trap charging state after the bias change from strong inversion to $V_{\mathrm{th}}^{\mathrm{GD}}(\downarrow)$ is sketched in Fig. 2.10. The bias switch is indicated at the top, the interface charge state in the middle and the observed relative hysteresis at the bottom. After the bias switch, the Fermi level changes only slightly and remains close to the conduction band edge. Assuming only interface states, the time constant for electron emission τ_{en} according to Shockley-Read-Hall (SRH) [113, 114] is given by

$$\tau_{\mathrm{en}} = \frac{1}{\nu_{\mathrm{thn}}\sigma_{\mathrm{n}}N_{\mathrm{C}}} \exp\left(\frac{E_{\mathrm{C}} - E_{\mathrm{t}}}{k_{\mathrm{B}}T}\right) \tag{2.5}$$

with the thermal velocity for electrons ν_{thn}, the capture cross section σ_{n} and the effective density of states in the conduction band N_{C}. After the bias switch from strong inversion to inversion, E_{F} remains close to E_{C} and thermal equilibrium is restored almost immediately by electron emission from trap states above the Fermi level to E_{C} (Fig. 2.10, middle) resulting in a stable, hysteresis free, drain current (Fig. 2.10, bottom). Note that no hole capture occurs because the interface remains inverted.

The remaining recovery slope of approximately $\Delta V_{\mathrm{th}}^{\mathrm{GD}}(\downarrow) \approx -10\,\mathrm{mV/dec}$ originates from border trap states with broadly distributed emission time constants, which can be described according to (1.6) (see Section 1.2.1). These states will be intensively investigated in Chap. 3.

2.4.2 Hysteresis after accumulation

In contrast to the behavior after charging the interface in strong inversion, the outcome changes drastically if the device is charged via an accumulation pulse. The switching process is sketched in Fig. 2.11 with the voltage level at the gate contact (top), the interface charging state (middle), and the relative hysteresis (bottom). Starting in accumulation, where the Fermi level is pinned to the valence band, the interface is assumed to be positively charged and in thermal equilibrium. After switching to inversion, where $V_{\mathrm{th}}^{\mathrm{GD}}$ is measured, the Fermi level crossed nearly the entire SiC band gap, which results in a *non-steady* interfacial charge state. Thermal equilibrium is slowly restored by

- electron capture from the SiC conduction band, with time constants according to

$$\tau_{\mathrm{cn}} = \frac{1}{\nu_{\mathrm{thn}}\sigma_{\mathrm{n}}n_{\mathrm{inv}}} \tag{2.6}$$

  with the inversion charge density n_{inv},

- and hole emission to the SiC valence band edge E_{V}, which follows

$$\tau_{\mathrm{ep}} = \frac{1}{\nu_{\mathrm{thp}}\sigma_{\mathrm{p}}N_{\mathrm{V}}} \exp\left(\frac{E_{\mathrm{t}} - E_{\mathrm{V}}}{k_{\mathrm{B}}T}\right) \tag{2.7}$$

  with the thermal velocity ν_{thp} and capture cross section ν_{thp} of holes, and the effective density of states in the valence band N_{V} [113, 114].

Since hole emission is independent of the Fermi level according to (2.7), the main contribution to the restoration of thermal equilibrium originates from electron capture according to (2.6). Therefore, the larger the inversion charge density n_{inv} (and thereby the gate voltage), the faster thermal equilibrium is reached. Fig. 2.12 and Fig. 2.13 show $V_{\mathrm{th}}^{\mathrm{GD}}(\uparrow)$ for various inversion charge densities. As before, the measurement is performed according to the schematics sketched in Fig. 2.8. Instead of a strong-inversion pulse, an

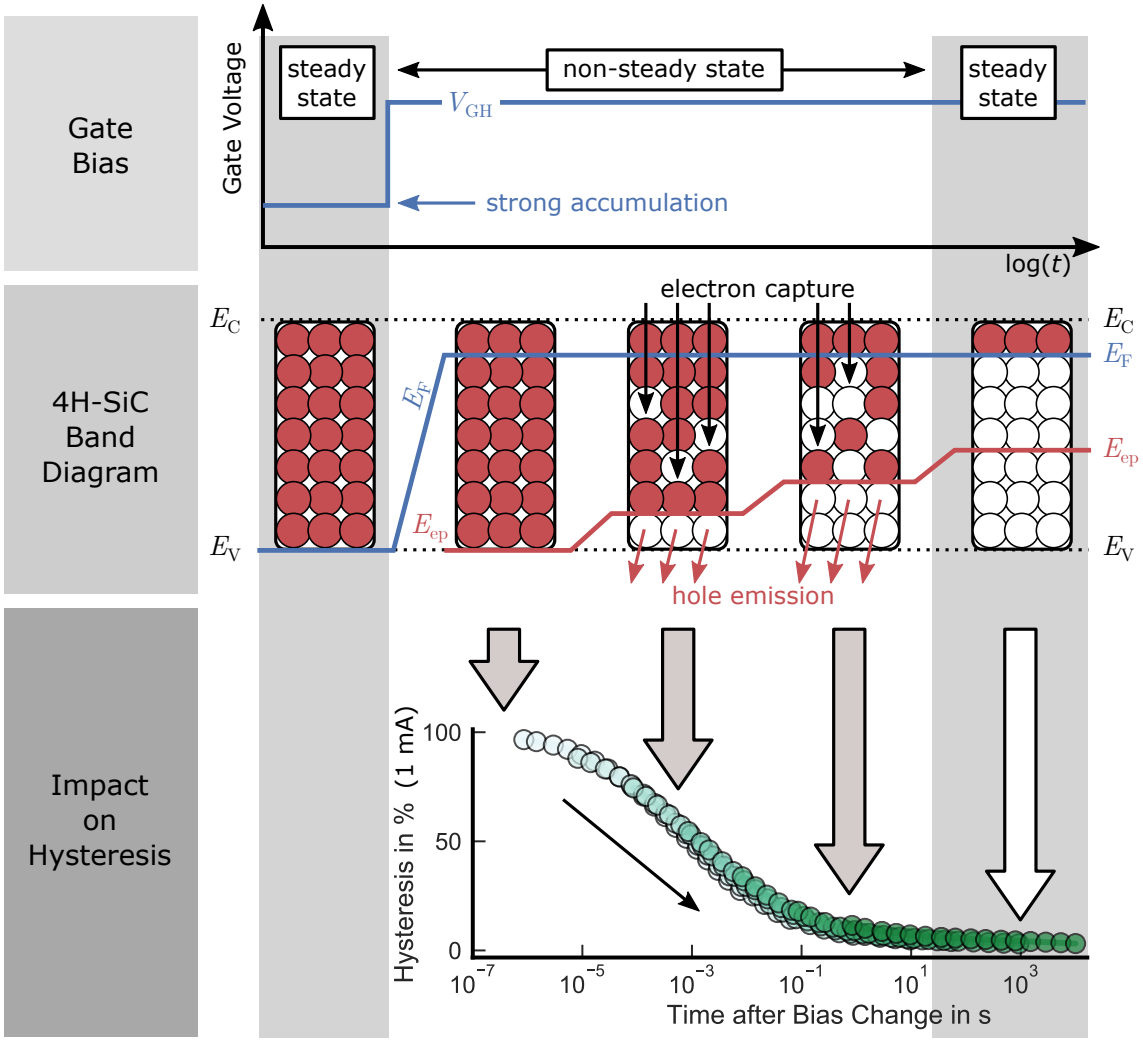


Fig. 2.11 Schematic illustration of the interface charging state after switching the gate bias from accumulation to inversion. Top: timing of the gate voltage. Middle: after the 1 s accumulation pulse, the interface is fully positively charged. Bottom: after switching to inversion, more and more positive charge is lost via hole emission and electron capture leading to a decrease a recovery of the hysteresis.

accumulation pulse at $V_G = -15\,V$ is applied for 1 s. After the charging pulse, I_{GD} ranging 10 nA to 10 mA is forced using the gated diode circuit, while the corresponding gate/drain voltage (labeled as $V_{th}^{GD}(\uparrow)$) is monitored. From (2.6) and the fact that the drain current is to first order a direct measurement for n_{inv} via the textbook formula

$$I_D = \frac{W}{L}\mu_n q n_{inv} V_D, \tag{2.8}$$

it is obvious that the time to restore thermal equilibrium should be indirectly proportional to n_{inv}, if mainly interface states are responsible for the hysteresis. This is in fact the case, as will be shown within the next sections.

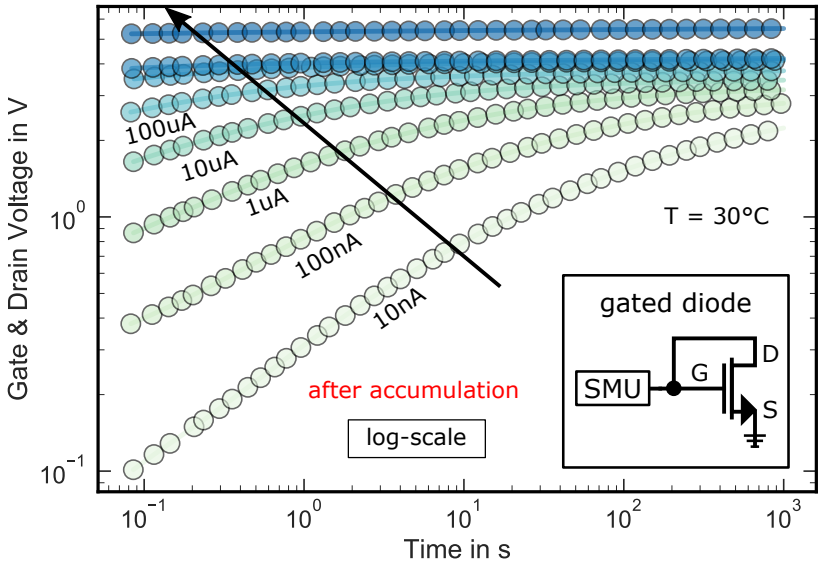


Fig. 2.12 Voltage shift after switching the gate from accumulation to various current densities I_{GD}, ranging from 10 nA to 100 mA. I_{GD} transients are recorded using a gated-diode circuit (inset).

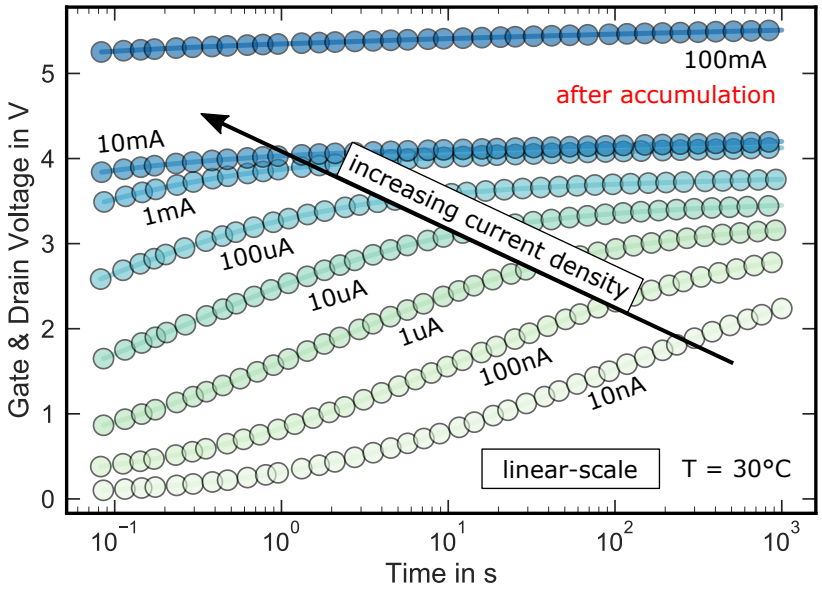


Fig. 2.13 Same as Fig. 2.12 but now with linear y-scale. Recovery of the subthreshold hysteresis scales with current density.

The universal hysteresis recovery curve

If the recovery time constants of the hysteresis mainly scales with the free inversion carrier density n_{inv}, an increase of n_{inv} by a fixed factor should decrease the recovery time constant by exactly the same factor according to (2.6). This is in fact true, since we are able to scale all transients from Fig. 2.12 onto a single *universal* recovery time t_D^u at any given

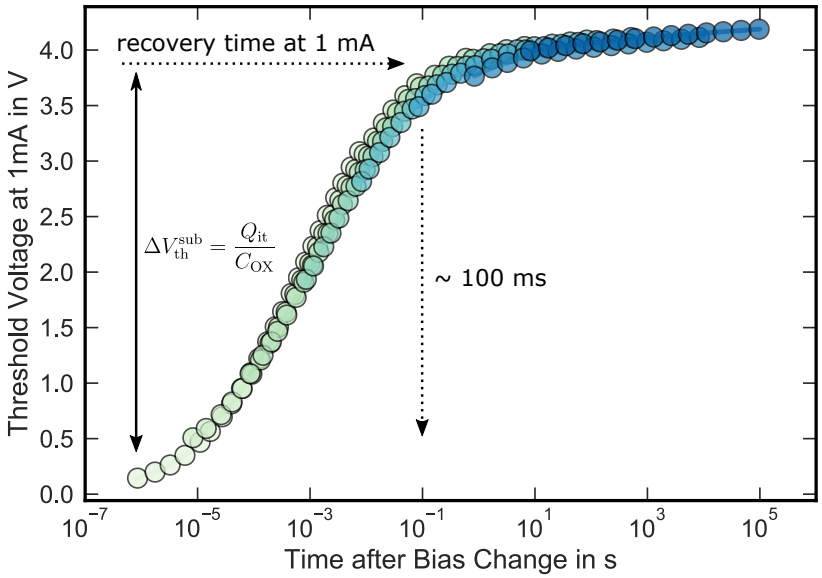


Fig. 2.14 Universal recovery curve for $I_{\mathrm{r}} = 1\,\mathrm{mA}$ obtained by applying (2.9) to the data in Fig. 2.12. At 1 mA the recovery of $\Delta V_{\mathrm{th}}^{\mathrm{sub}}$ takes approximately 100 ms.

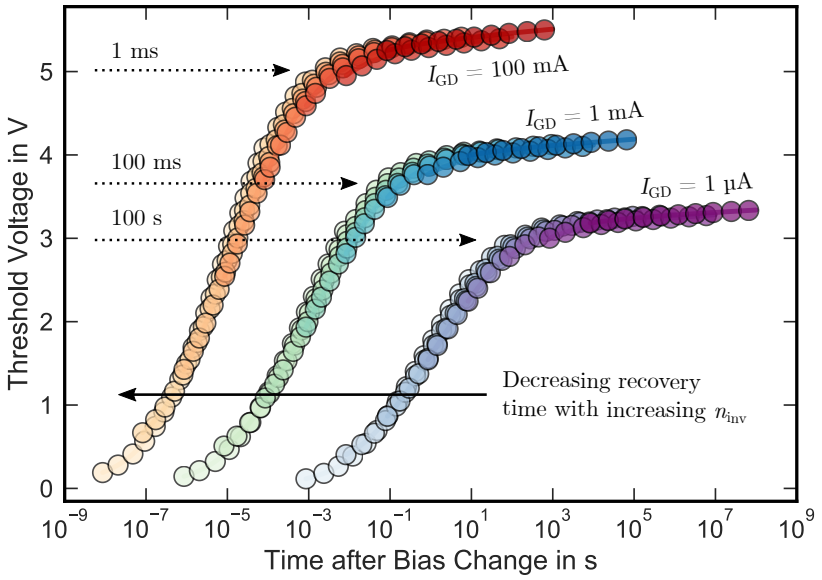


Fig. 2.15 Universal recovery curves for a readout current of 0.1 A (red), 1 mA (green), and 1 µA (purple). The recovery time scales linearly with the inversion carrier density n_{inv}. For $I_{\mathrm{GD}} = 1\,\mathrm{mA}$ (blue), the recovery time is approximately 100 ms, whereas for the 100 times higher current of $I_{\mathrm{GD}} = 100\,\mathrm{mA}$, the recovery time is 100 times shorter and approximately 1 ms (red).

readout current I_{r}, by assuming $t_{\mathrm{D}}^{\mathrm{u}}$ to scale according to

$$t_{\mathrm{D}}^{\mathrm{u}}(I_{\mathrm{r}}) = t_{\mathrm{D}}(I_{\mathrm{D}})\frac{R_{\mathrm{ch}}(I_{\mathrm{r}})}{R_{\mathrm{ch}}(I_{\mathrm{D}})} \approx t_{\mathrm{D}}(I_{\mathrm{D}})\frac{I_{\mathrm{D}}}{I_{\mathrm{r}}}\,. \tag{2.9}$$

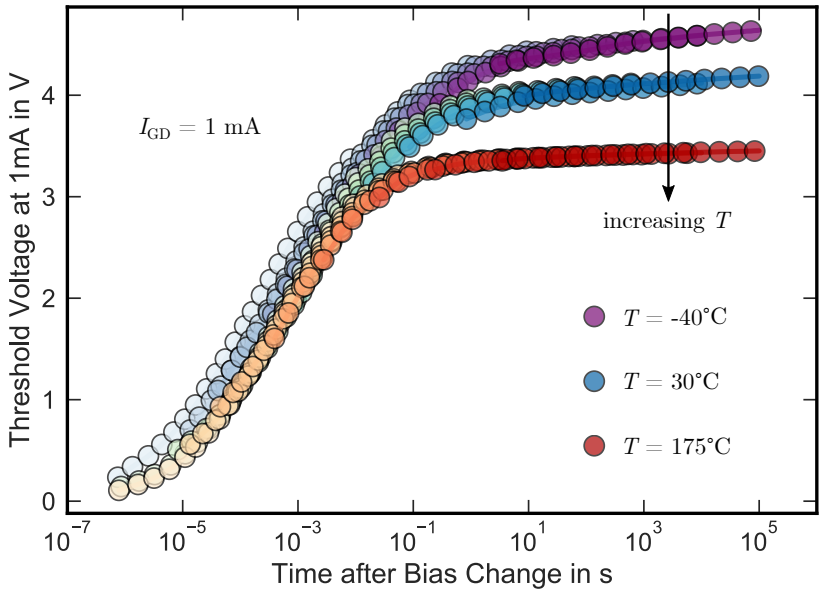


Fig. 2.16 Temperature dependence of the universal recovery curve at 1 mA for $T = -40\,°C$ (purple), $T = 30\,°C$ (blue), and $T = 175\,°C$ (red). The steady state $V_{th}^{GD}(I_{GD})$ decreases from around 4.6 V ($T = -40\,°C$) to approximately 3.4 V ($T = 175\,°C$). At $-40\,°C$ there seems to be ongoing recovery for recovery times >10 s.

Here, $t_D(I_D)$ is the time at the current level I_D, and $R_{ch}(I_r)$ and $R_{ch}(I_D)$ the channel resistance at I_r and I_D, respectively.

Using the data from Fig. 2.12, all distinct transients can be transformed onto one universal recovery curve, which allows to extract the time to reach thermal equilibrium at any given inversion carrier density n_{inv} represented by I_{GD}. Fig. 2.14 shows the universal recovery curve for a drain current of $I_r = 1\,mA$. Coming from strong accumulation, it takes about 100 ms until thermal equilibrium is restored and the corresponding gate voltage of 4 V to be stable. Fig. 2.15 shows the same curve for $I_r = 100\,mA$, 1 mA and 1 µA. Since we are able to describe the time constants solely via the SRH model, the recovery time scales linearly with the drain current, meaning a 100 times higher drain current corresponds to 2 orders of magnitude faster recovery time constants. This is proven in Fig. 2.15: at 1 mA, the time to reach thermal equilibrium is approximately 100 ms, whereas for a 100 times higher drain current of 100 mA thermal equilibrium is reached in 1 ms, which is exactly 100 times faster. The same is true for a 1000 times lower current of 1 µA (purple).

The temperature dependence of the universal recovery at $I_{GD} = 1\,mA$ is shown in Fig. 2.16 for temperatures of $-40\,°C$, $30\,°C$ and $175\,°C$. As can be seen, the steady state $V_{th}^{GD}(1\,mA)$ decreases from 4.8 V to approximately 3.5 V with increasing temperature. Interestingly, there seems to be ongoing recovery at $-40\,°C$ and $30\,°C$ for times > 10 s, as can be seen in the remaining slopes of both curves. In general, one would attribute such a behavior to broadly distributed recovery time constants, which are hard to explain using a SRH based model. However, it will be shown in the next section that the ongoing recovery "tail" can be attributed to broadly distributed NBTI recovery and therefore decoupled from the hysteresis effect.

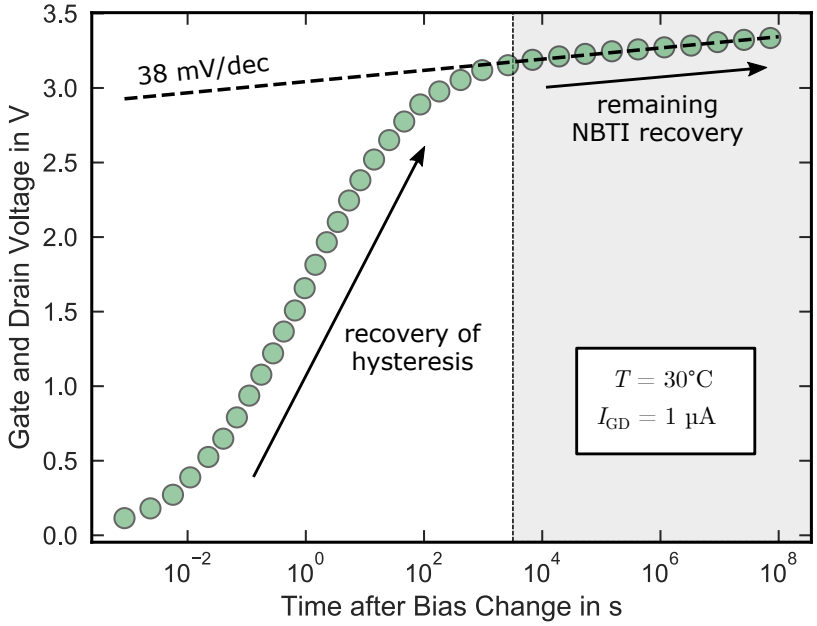


Fig. 2.17 Convolution of the hysteresis recovery curve for a readout current of $I_{GD} = 1\,\mu A$. In addition to the recovery of fast states (white background), a minor contribution originates from border states with broadly distributed time constants (NBTI recovery). The NBTI recovery component becomes dominant after the hysteresis is fully recovered (gray background).

Distribution of recovery times

To extract the recovery time distribution of the interface states responsible for the hysteresis, first one has to disentangle the recovery signal from the convolution of fast states and the broadly distributed NBTI states. Fortunately, this is easily possible due to the broadly distributed emission times of border states after positive and negative bias stress, as was for example shown in Fig. 2.9 after positive bias temperature stress (PBTS) with a constant slope of approximately $k = -10\,\mathrm{mV/dec}$ over the whole measurement window.

The convolution of the hysteresis recovery curve for a readout current of $I_{GD} = 1\,\mu A$ is shown in Fig. 2.17. In addition to the dominant recovery component of the fast interface states responsible for the hysteresis, an additional NBTI recovery component is present, which becomes dominant at approximately $3 \times 10^3\,\mathrm{s}$ after the bias switch. Fortunately, the NBTI component is broadly distributed in time and therefore easy to remove from the hysteresis recovery curve using a constant exponent k (cf. (1.3)), which allows for an explicit extraction of the recovery time distribution.

After the subtraction of the NBTI recovery, the recovery time t_{rec} of the hysteresis can be fitted using a log-normal distribution with the cumulative distribution function (CDF)

$$\mathrm{CDF}(t_{rec}) = \frac{1}{2} + \frac{1}{2}\,\mathrm{erf}\left(\frac{\ln(t_{rec}) - \mu_{ln}}{\sqrt{2}\sigma_{ln}}\right) \tag{2.10}$$

with the error function erf, and the parameters of the log-normal distribution μ_{ln} and σ_{ln} that are, respectively, the mean and standard deviation of the normal distribution of $\log(t_{rec})$. The outcome for the universal recovery curve at $I_{GD} = 1\,\mu A$ and $30\,°C$ is shown in Fig. 2.18 (top). After the NBTI correction, the hysteresis recovery curve shows very

good agreement with the log-normal CDF with $\mu_{\ln} = -0.04$ and $\sigma_{\ln} = 3.27$ (dashed line). The resulting probability density function (PDF) represents the distribution of the recovery time and is shown in the bottom plot in Fig. 2.18.

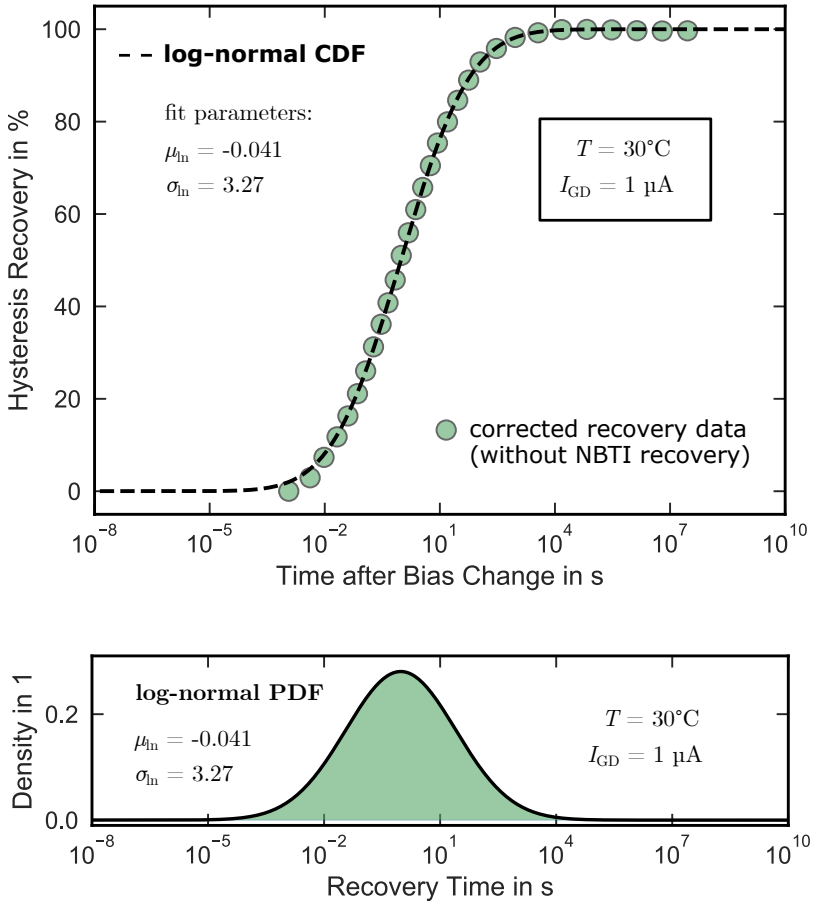


Fig. 2.18 Recovery of the hysteresis at $I_{GD} = 1\,\mu A$ and 30 °C after the removal of the NBTI related component (top, green circles). The recovery shows good agreement with a log-normal CDF with the fitting parameters $\mu_{\ln} = -0.041$ and $\sigma_{\ln} = 3.27$. The representative PDF is indicated in the bottom plot.

Fig. 2.19 shows the log-normal PDFs for $T = -40\,°C$ (blue), $T = 30\,°C$ (green) and $T = 175\,°C$ (red) at a current density of $I_{GD} = 1\,\mu A$. The parameter $\mu_{\ln}$ is independent of the temperature and varies only slightly. Due to this, the recovery mechanism seems not to be temperature activated, or at least has an activation energy which is significantly below 100 meV. On the other hand, the distribution broadens for decreasing temperatures, which results in slightly longer recovery times for lower temperatures. The dependence of the parameters of the log-normal distribution, $\mu_{\ln}$ and $\sigma_{\ln}$, on I_{GD} and T is shown in Fig. 2.20. As already mentioned, $\mu_{\ln}$ is nearly independent of T but scales strongly with the inversion carrier density n_{inv} (see Fig. 2.20, left), which is proportional to I_{GD}. The median of the distribution $\widetilde{t_{rec}}$, which is represented by the parameter $\mu_{\ln}$ according to

$$\widetilde{t_{rec}} = e^{\mu_{\ln}}\,, \tag{2.11}$$

decreases linearly with the logarithm of I_{GD} with a slope of $k_{\mu_{\ln}} = -2.3/\text{dec}$. On the other hand, the standard deviation $\sigma_{\ln}$ is not affected by I_{GD} (not shown), but increases with

decreasing T with a slope of $k_{\sigma_{\ln}} \approx -0.004/°\mathrm{C}$ leading to a stretch out of the recovery time distribution for lower temperatures (Fig. 2.20, right).

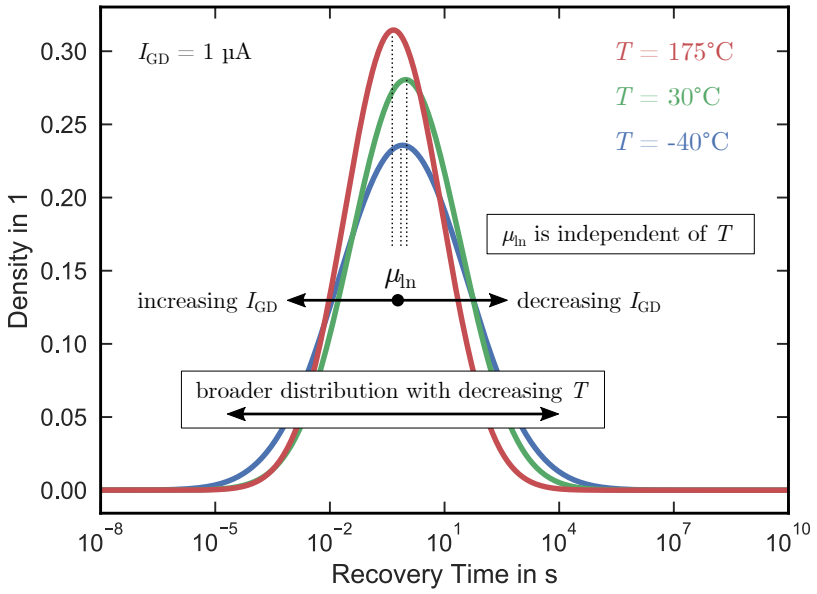


Fig. 2.19 Log-normal PDF for the hysteresis recovery times for $T = -40\,°\mathrm{C}$, $T = 30\,°\mathrm{C}$ and $T = 175\,°\mathrm{C}$ for $I_{GD} = 1\,\mu\mathrm{A}$. If the temperature is decreased, the recovery time distribution broadens ($\sigma_{\ln}$ increases), whereas the parameter $\mu_{\ln}$ is roughly independent of T within the measured temperature range.

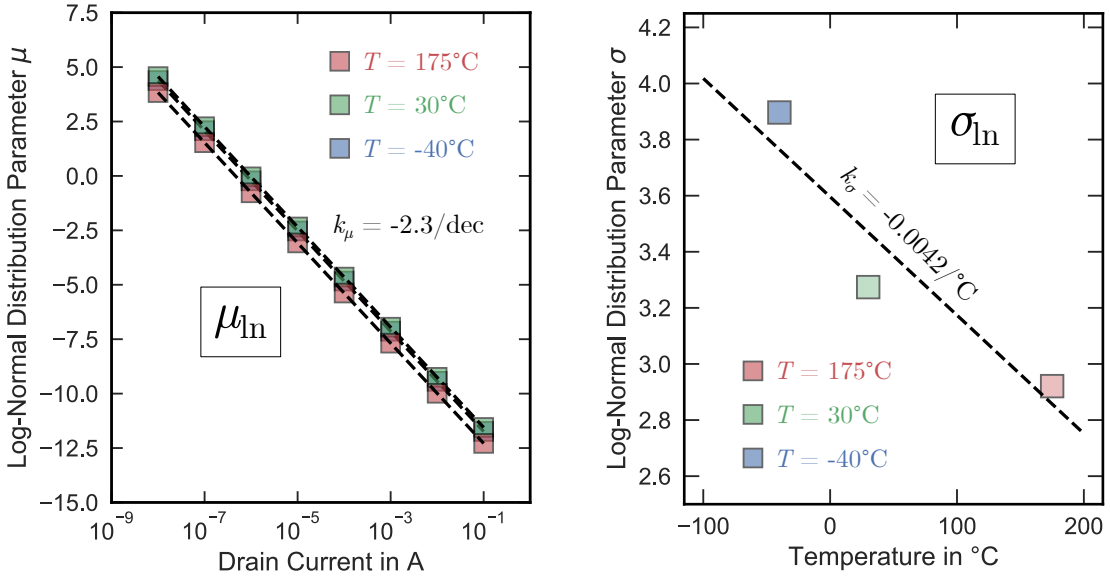


Fig. 2.20 Parameters for the log-normal distribution of the hysteresis recovery times. Left: the parameter $\mu_{\ln}$ seems to be independent of T and scales linearly with $\log(I_{GD})$ with a slope of approximately $k_\mu = -2.3/\mathrm{dec}$. Right: the standard deviation $\sigma_{\ln}$ is independent of I_{GD} but seems to increase with decreasing T, which indicates a broadening of the recovery time distribution for lower temperatures.

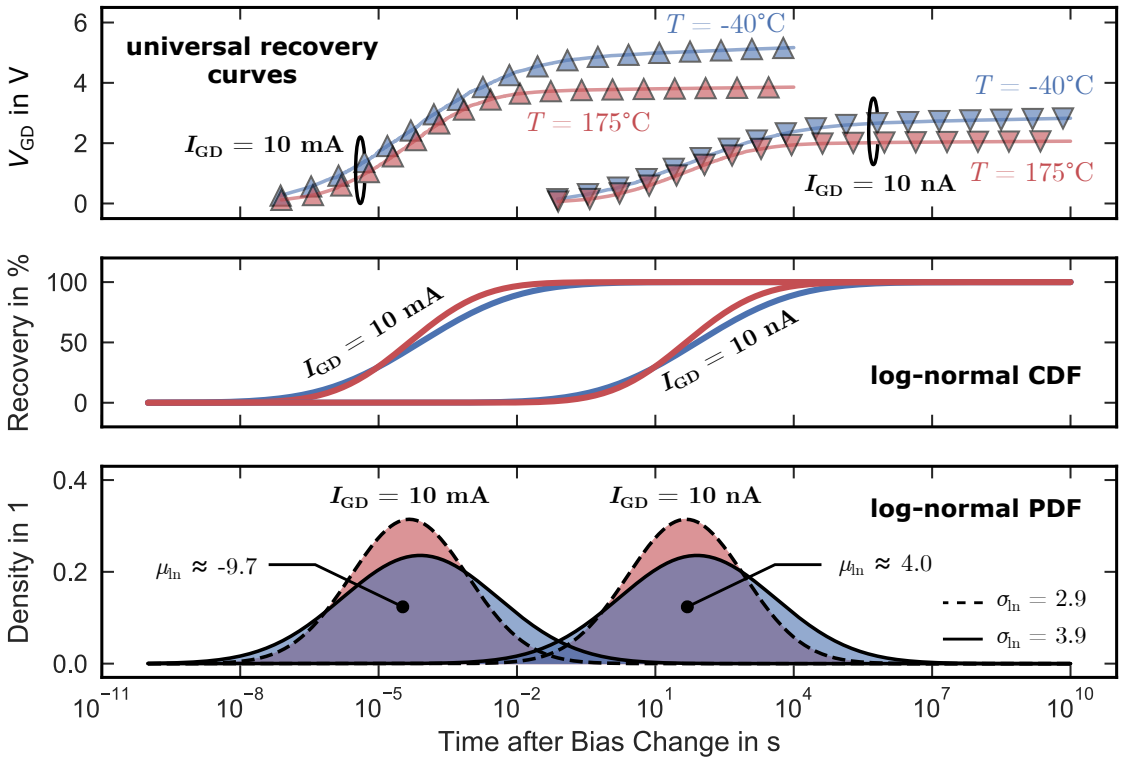


Fig. 2.21 Recovery of the hysteresis as a function of the temperature for $T = -40\,°C$ (blue) and $T = 175\,°C$ (red) for $I_{GD} = 10\,nA$ (right) and a 1 million times higher current density of $I_{GD} = 10\,mA$ (left). Top: universal recovery curves including the NBTI component, which is more pronounced for lower temperatures. Middle: log-normal cumulative distribution functions of the universal hysteresis curves corrected for NBTI recovery. Bottom: probability density functions of the recovery times. For the 10^6 times higher current density (left), parameter μ_{ln} decreases from $\mu_{ln} \approx 4$ to $\mu_{ln} \approx -9.7$ for both temperatures, which represents a 10^6 times faster recovery time. On the other hand, the standard deviation increases from $\sigma_{ln} = 2.9$ at $T = 175\,°C$ to $\sigma_{ln} = 3.9$ at $T = -40\,°C$ with decreasing temperature. This means the recovery time distribution broadens with lower T and full recovery takes slightly longer.

Fig. 2.21 gives a final overview on the recovery of the hysteresis as a function of the temperature for $T = -40\,°C$ (blue) and $T = 175\,°C$ (red) for two different current densities of $I_{GD} = 10\,nA$ (right) and a 1 million times higher current density of $I_{GD} = 10\,mA$ (left). Fig. 2.21, top, shows the universal recovery curves, still including the NBTI component. As stated before, this component is more distinct for lower temperates, as can be seen in the higher slope after the majority of the hysteresis is already recovered. After the NBTI component is removed, the relative amount of recovery can be extracted, which is represented by the CDF (Fig. 2.21, middle). From the CDF, one can extract the recovery time distributions (PDF, Fig. 2.21, bottom). The standard deviation is independent of I_{GD}, but decreases from $\sigma_{ln} = 3.9$ at $T = -40\,°C$ to $\sigma_{ln} = 2.9$ at $T = 175\,°C$ with increasing temperature, which means a broadening of the PDF for lower temperatures. On the other hand, parameter μ_{ln} is nearly independent of T but scales strongly with I_{GD}. For the 10^6 times higher current density (left), μ_{ln} decreases from $\mu_{ln} \approx 4$ to $\mu_{ln} \approx -10$ for both temperatures, which results in an exactly 10^6 times faster recovery.

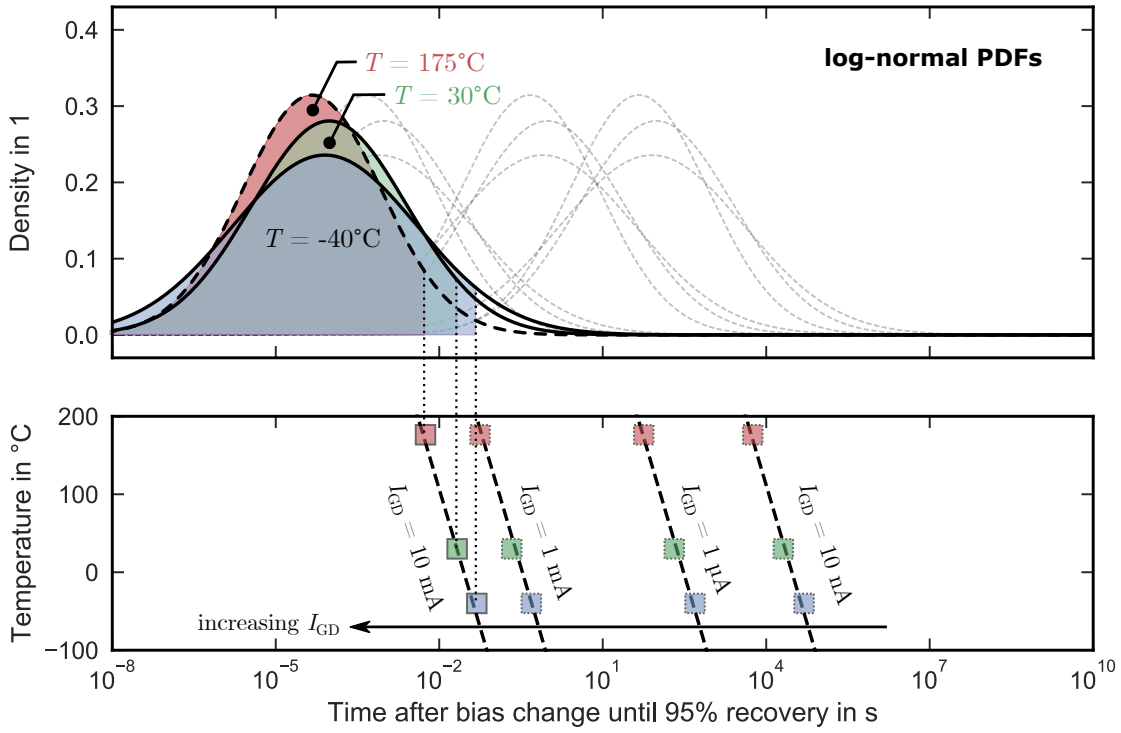


Fig. 2.22 Time after bias change after which 95 % of the hysteresis is recovered for temperatures of $T = -40\,°C$ (blue), $T = 30\,°C$ (green) and $T = 175\,°C$ (red) and current densities ranging from $I_{GD} = 10\,nA$ to $I_{GD} = 10\,mA$. Top: probability density functions. Here the distributions for a current density of $I_{GD} = 10\,mA$ are highlighted, whereas the PDFs for lower current densities are outlined only (dashed). Bottom: recovery time for 95 % recovery as a function of the temperature T for various current densities.

Last but not least, Fig. 2.22 shows the recovery time after which 95 % of the fully-charged hysteresis is recovered for temperatures of $T = -40\,°C$ (blue) and $T = 175\,°C$ (red) with current densities ranging from $I_{GD} = 10\,nA$ to $I_{GD} = 10\,mA$. The top picture shows the representative recovery time distributions for all temperature and I_{GD} combinations. Here, the distributions for $I_{GD} = 10\,mA$ are highlighted do increase readability, whereas the PDFs for lower current densities are outlined only (dashed, gray). The time for 95 % recovery of each I_{GD}-T combination is represented in the bottom plot (squares). As already shown above, the recovery time decreases linearly with increasing current density. At fixed I_{GD}, the main contribution to the recovery time dependence for different temperatures originates from the increasing standard deviation σ_{ln} for lower temperatures and not from a change of μ_{ln}, which roughly remains stable within the investigated temperature range. Therefore, the underlying mechanism seems not to be temperature activated. For $I_{GD} = 10\,mA$, the time to 95 % recovery increases from $t_{rec} \approx 5\,ms$ at 175 °C to $t_{rec} \approx 50\,ms$ at −40 °C.

2.4.3 The hysteresis in the non-radiative multi-phonon picture

In general, the movement of the defect transition is modeled along a reaction path or coordinate using non-radiative multi-phonon transitions (NMP) (see Section 1.2.1). In an NMP transition, the defect state changes without excitation or emission of photons,

meaning the required energies have to be supplied by phonons. A very comprehensive overview on non-radiative multiphonon theory can be found in [58].

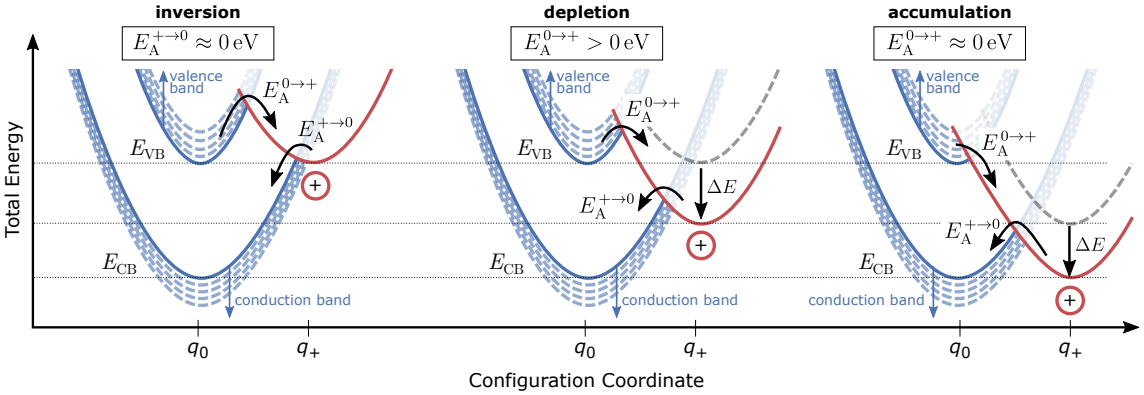


Fig. 2.23 Simplified schematic of the sweep hysteresis using the non-radiative multiphonon view in the hole picture. The valence band (top) and conduction band (bottom) are indicated in blue and represent the neutral charge state of the system. The potential energy surface of the positive charge state (+) is indicated in red. In strong inversion (left), the transition from the positive charge state to the neutral charge state, $+ \to 0$, is nearly barrier-free with ${E_A}^{+\to 0} \approx 0\,eV$. In depletion (middle), the energy of the neutral state is decreased by ΔE, which leads to broadly distributed time constants due to the non-zero and distributed energy barrier ${E_A}^{0\to +}$. In accumulation (right), the energy barrier for the transition of the neutral charge state to the positive states is close to zero, ${E_A}^{0\to +} \approx 0\,eV$, which results in the nearly instantaneous charging times.

An illustration of a simple defect model in the hole picture which describes the hysteresis is given in Fig. 2.23. Each energy state can be approximated by an adiabatic potential energy surface (PES), which usually is approximated by a parabolic form. In strong inversion (left), the energy of the positive charge state (+, red) is close to the valence band edge (blue). Due to the previous observations of very fast recovery times for E_F close to E_C, the transition from $+ \to 0$ has to be nearly barrier-free with ${E_A}^{+\to 0} \approx 0\,eV$. Therefore, all available trap states will be in the neutral configuration in strong inversion.

After changing the gate voltage from inversion to depletion (middle), the energy of the neutral state decreases by ΔE and transitions from the neutral to the positive charge state (+, red) become more and more likely.

In accumulation (right), the transition barrier for charging the positive charge state approaches zero, ${E_A}^{0\to +} \approx 0\,eV$, which results in nearly instantaneous charging times. Furthermore, all available trap states will be in the positive configuration in accumulation. Note that after completely charging the interface in accumulation, a gate bias switch back do depletion will result in the broadly distributed recovery time constants as observed in Section 2.4.2 due to non-zero and distributed energy barriers ${E_A}^{0\to +} > 0$ in depletion (middle).

2.5 Crystal face dependence

All results discussed above are extracted from *in-house* MOSFETs with the active channel on the a-face, $(11\bar{2}0)$-plane. To obtain a complete picture, we also investigated MOSFETs with the channel on the Si-face, (0001)-plane. For these devices, the same trend is observed,

although $\Delta V_{\mathrm{th}}^{\mathrm{sub}}$ is in the range of millivolts and therefore not as pronounced in the I_{D}-V_{G} curves (not shown). This is a surprising outcome if one considers the, in general, much lower mobility for devices with the active channel on the Si-face. Compared to their a-face counterparts, the typical mobility of Si-face MOSFETs, which were subjected to an identical interface passivation, is 2 to 3 times lower. In our case, the extracted low-field mobility of the *in-house* Si-face devices is $\approx 20\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$, whereas the a-face devices show a 3 times higher mobility of $\approx 60\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$, which is consistent with recent studies [115].

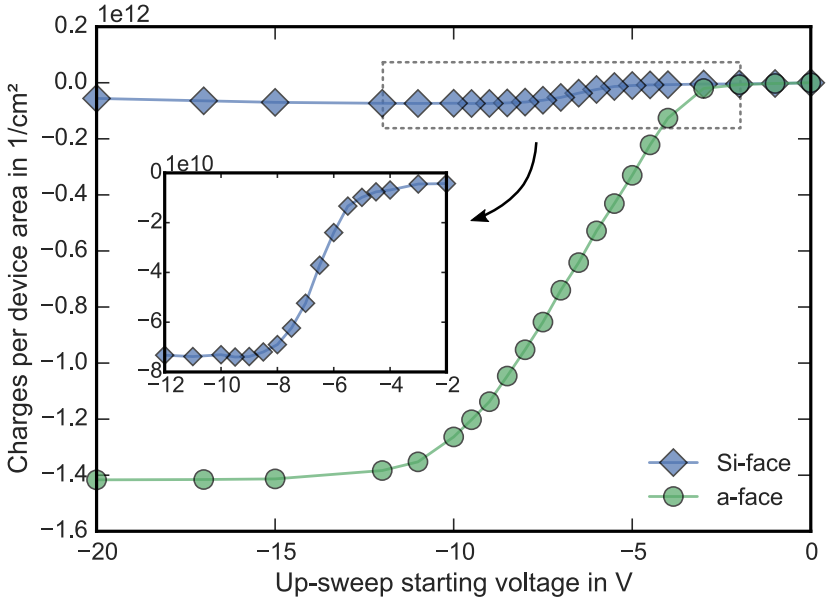


Fig. 2.24 Trapped charges at the interface per device area as a function of the up-sweep starting voltage for a Si-face (diamonds, blue) and an a-face (circles, green) device. The same trend is observed on both crystal faces although the effect is more pronounced on the a-face. The inset provides a closer look on the Si-face curve.

From $V_{\mathrm{th}}^{\mathrm{sub}}$, the number of trapped charges N_{t} per device area A, can be extracted using the the formula of the capacitance and is given by

$$N_{\mathrm{t}} = \frac{\Delta V_{\mathrm{th}}^{\mathrm{sub}} \varepsilon_0 \varepsilon_{\mathrm{r}}}{t_{\mathrm{OX}} q} \tag{2.12}$$

with the relative permittivity of SiO_2, ε_{r}, the vacuum permittivity ε_0, the oxide thickness t_{OX} and the electronic charge q. Fig. 2.24 shows N_{t} extracted from $\Delta V_{\mathrm{th}}^{\mathrm{sub}}$ via (2.12) for both crystal faces as a function of the up-sweep starting voltage. It is important that, despite the lower channel mobility, also the interface trap density calculated from $\Delta V_{\mathrm{th}}^{\mathrm{sub}}$ is about one order of magnitude lower on Si-face (diamonds, blue) devices than on a-face (circles, green) MOSFETs. For both device designs, no permanent component is present in the hysteresis. Even after millions of charging-discharging cycles, which occur during AC-use conditions, N_{t} and therefore the hysteresis remains constant [112].

To summarize the dependence of the *subthreshold* sweep hysteresis on the SiC crystal plane, both Si-face and a-face MOSFETs show the same trend. However, the total amount of trapped charges extracted from the I_{D}-V_{G} curves is smaller on the Si-face, which is in contrast to the lower mobility of these devices. An explanation for the discrepancy between a lower trap density *and* lower mobility is given in the next section.

2.6 Charge pumping

Because of its high sensitivity to interface states, charge pumping (CP) [82] is a suitable technique to investigate the sweep hysteresis and was recently demonstrated on 4H-SiC MOSFETs in various studies [84–86, 116, 117]. An introduction to the charge pumping measurement techniques as performed in this chapter is given in Section 1.3.4.

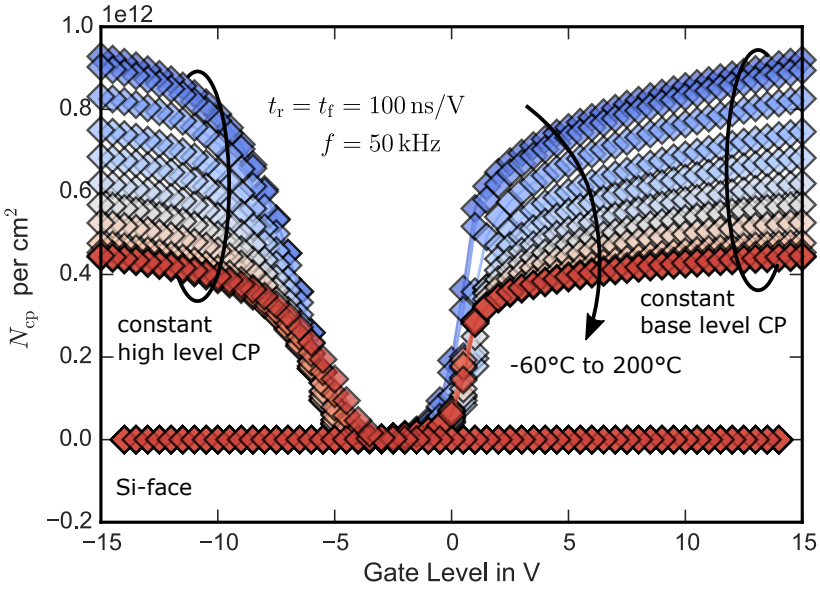


Fig. 2.25 Charges pumped per cycle extracted from constant base level CP (right wing) and constant high level CP (left wing) for the Si-face device. The increase in N_{CP} with decreasing T originates from trap states close to the band edges of 4H-SiC, which do not contribute to I_{CP} at elevated temperatures due to the narrowing of the active energy window, as described in Section 1.3.4.

According to the schematics in Fig. 1.17, *constant high level* and *constant base level* CP measurements at a fixed frequency of 50 kHz and fixed transition rates of $t_r = t_f = 100\,ns\,V^{-1}$ were performed in a wide temperature range between −60 °C and 200 °C. From the charge pumping current I_{CP}, one is able to calculate the number of pumped charges per cycle N_{CP} via

$$N_{CP} = \frac{I_{CP}}{A_G^{eff} q f} \tag{2.13}$$

with the effective gate area A_G^{eff} and the frequency of the gate pulse f. The outcome, which shows temperature dependence of the total number of pumped charges per cycle N_{CP}, is presented in Fig. 2.25 for the Si-face device and in Fig. 2.26 for the a-face device. For the former, N_{CP} ranges between $0.4 \times 10^{12}\,cm^{-2}$ and $0.9 \times 10^{12}\,cm^{-2}$, strongly depending on the device temperature. If the majority of the CP signal originates from trap states with energetic positions close to the band edges, this is an expected outcome due to the narrowing of the active energy window ΔE_{CP} with temperature as described in Section 1.3.4. For the a-face device on the other hand, the total number of pumped charges is approximately 5 times higher ($3.0 \times 10^{12}\,cm^{-2}$) and nearly no temperature dependence is observed. This indicates the major contribution to the signal originates from trap states which are energetically located around the intrinsic Fermi level (mid-gap) of 4H-SiC.

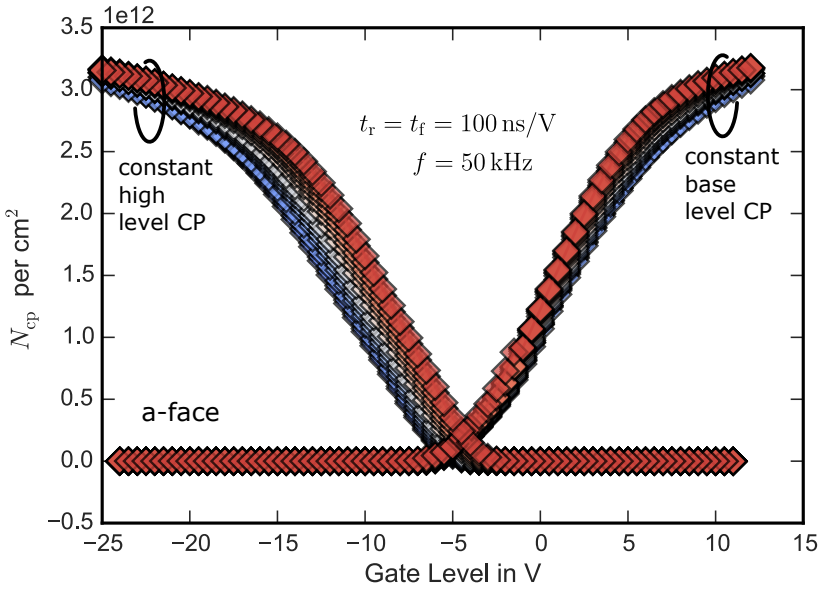


Fig. 2.26 Same as Fig. 2.25 but now for the a-face device. We observe a minor dependence of N_{CP} on the temperature and an overall higher signal, indicating the major contribution to the charge pumping current originates from trap states around midgap.

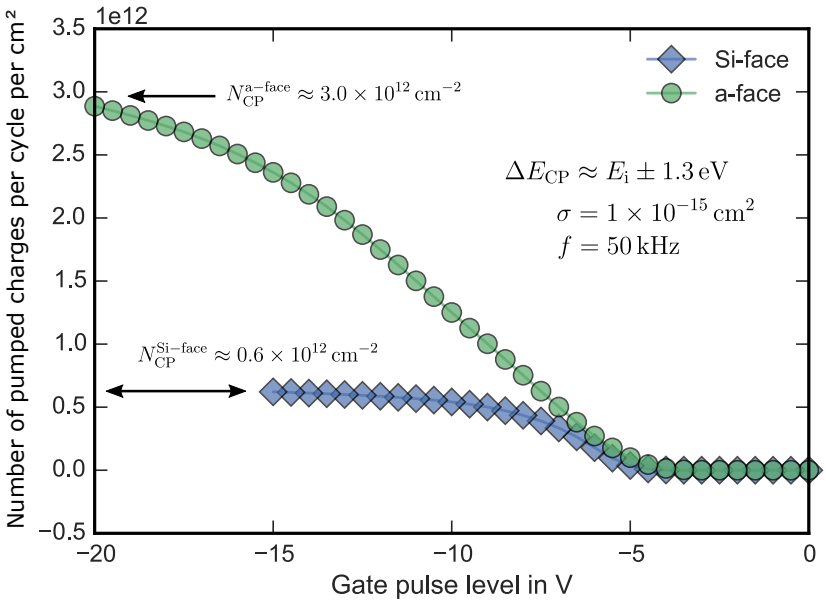


Fig. 2.27 Number of charges pumped during a constant high level charge pumping measurement. Although the a-face devices show better mobility, the interface state density is a factor of 5 higher. The increase is most likely due to defect states close to the intrinsic Fermi level.

A comparison of the trap numbers extracted via charge pumping N_{CP} and the sub-threshold hysteresis N_t is given in Tab. 2.1. Although the absolute numbers of trapped charges at the SiC/SiO_2 interface differs for both measurement techniques (compare with Fig. 2.24), the same trend is observed. The linear correlation between ΔV_{th}^{sub} and the

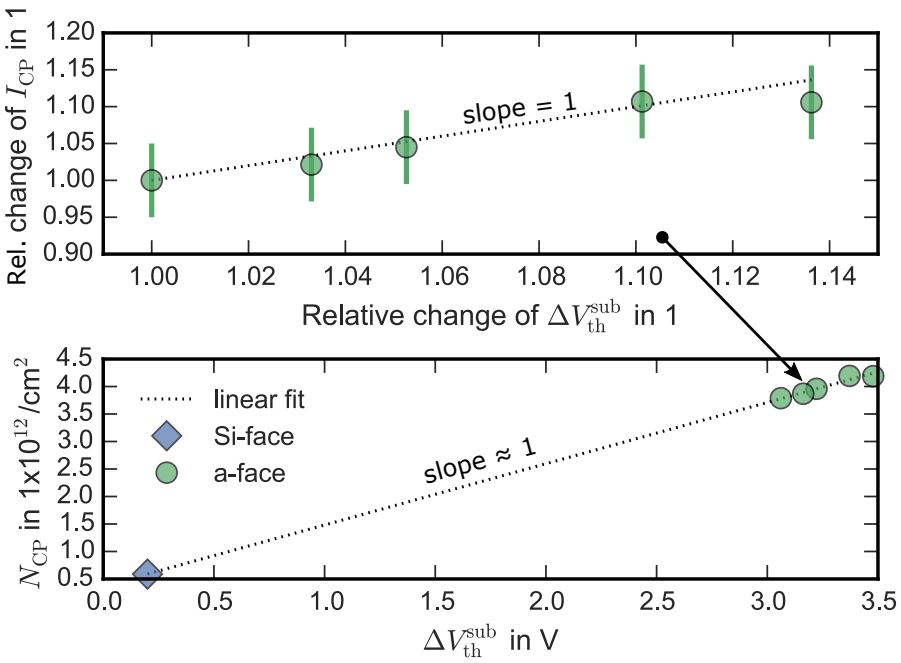


Fig. 2.28 Top: linear increase of the charge pumping current I_{CP} with increasing sweep hysteresis ΔV_{th}^{sub} on a-face devices. Bottom: increase in the number of pumped charges per cycle N_{CP} with increasing hysteresis for the Si-face (diamonds, blue) and a-face (circles, green). Due to the linear dependence of the hysteresis and the charge pumping signal, ΔV_{th}^{sub} likely originates from deep states at the SiC-SiO_2 interface.

charge pumping current I_{CP} for a-face devices is depicted in Fig. 2.28 (top). Here, data is extracted at 30 °C. Devices which show a 5 % increased hysteresis also show a 5 % increased I_{CP}. In the bottom plot of Fig. 2.28 the correlation of N_{CP} and ΔV_{th}^{sub} for both crystal planes is depicted. Again, the result suggests the same origin for the hysteresis and increased charge pumping current on both crystal faces. The reason for the diverging values for both extraction methods is explained in the next section.

Table 2.1: Total number of trapped charges extracted form the input characteristics (from ΔV_{th}^{sub} via (2.12)) and charge pumping measurements (from I_{CP} via (2.13))

Plane	Label	$N_{CP}(I_{CP})$	$N_t(\Delta V_{th}^{sub})$
(0001)	Si-face	$0.6 \times 10^{12}\,cm^{-2}$	$\approx 0.1 \times 10^{12}\,cm^{-2}$
$(11\bar{2}0)$	a-face	$3.0 \times 10^{12}\,cm^{-2}$	$\approx 1.4 \times 10^{12}\,cm^{-2}$

2.6.1 Discrepancies between input characteristics and charge pumping

The discrepancy in the total number of trapped charges extracted via the sweep hysteresis N_t and the charge pumping technique N_{CP} originates from the following facts:

- First, N_t extracted from the sweep hysteresis in our measurements is read out via the drain current at $I_D = 1$ nA. Extracting ΔV_{th}^{sub} at lower drain current, and therefore

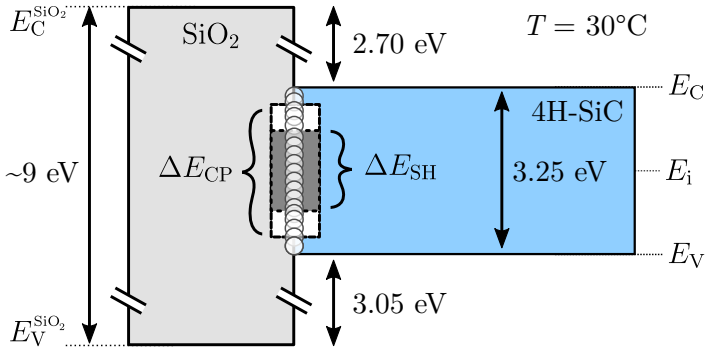


Fig. 2.29 Schematic band diagram of the SiC-SiO$_2$ system to illustrate the difference in the active energy window in the charge pumping ΔE_{CP} and sweep hysteresis ΔE_{SH} measurements. Due to the slower slew rates, ΔE_{SH} is approximately 0.8 eV narrower at 30 °C resulting in a reduced number of interface states, which contribute to the measurement signal.

lower inversion carrier density (see Section 2.3), will result in a higher N_t (compare to Fig. 2.2). Due to this, N_t extracted from the sweep hysteresis gives a lower limit of the total interface trap density. To extract the total number of trapped charges one needs to read out the ΔV_{th}^{sub} at infinitesimal small drain current, which is not possible due to experimental limits of the measurement setup.

- Second, the effective band gap energy window ΔE_{CP} scanned in the CP measurements is a function of the gate voltage rise and fall times and is given by [87]

$$\Delta E_{CP} = 2k_B T \cdot \log\left(\frac{\Delta V_G}{\overline{v_{th}} n_i \overline{\sigma} \sqrt{t_f t_r}(V_{TH}^{CP} - V_{FB}^{CP})}\right) \tag{2.14}$$

with the Boltzmann constant k_B, the temperature T, the mean thermal velocity of holes and electrons $\overline{v_{th}}$, the mean capture cross section of holes and electrons $\overline{\sigma}$, the intrinsic carrier density n_i, the amplitude of the gate pulse ΔV_G, the charge pumping flatband and threshold voltages V_{FB}^{CP} and V_{TH}^{CP} and the rise and fall times of the gate pulse t_r and t_f. In CP measurements, the gate voltage was switched from the high level to the low level within hundreds of nanoseconds compared to the relatively slow gate level slew rate in the range of 1 s/V used in the the sweep measurements. Due to the difference in the slew rate, one has to consider the following two effects:

  (i) According to (2.14), ΔE_{CP} shrinks with decreasing rise time t_r and fall time t_f. Therefore, the energy window scanned in the charge pumping measurements with a switching slope of 100 ns/V corresponds to $\Delta E_{CP} \approx E_i \pm 1.3$ eV whereas the energy window scanned in the sweep hysteresis measurements ΔE_{SH} with a switching slope of 1 s/V corresponds to $\Delta E_{SH} \approx E_i \pm 0.9$ eV at 30 °C. The difference in the active energy window is depicted in Fig. 2.29. The narrower energy range is due to the fast emission of electrons close to the conduction band edge during the down sweep and due to the fast emission of holes close to the valance during the up-sweep. In total, 0.8 eV less than the SiC bandgap is electrically visible in the sweep hysteresis measurement at 30 °C and therefore all trap states within these 0.8 eV do not contribute to the signal.

  (ii) With decreasing t_r, t_f, an increasing number of oxide or near interface traps with longer time constants contribute to the signal. In our case, the effect on

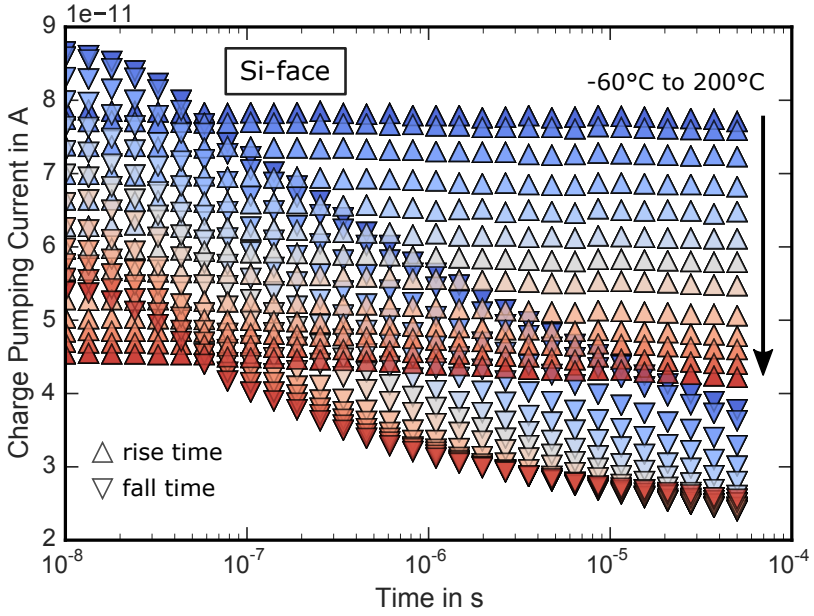


Fig. 2.30 I_{CP} as a function of the temperature and the rise and fall times of the gate pulse for the Si-face device. The strong change in I_{CP} with t_f indicates a high density of states close to the conduction band edge.

the sweep hysteresis in the subthreshold regime is in the range of millivolts and therefore negligible compared to the drift of several volts caused by the high number of fast interface states.

2.6.2 Trap distributions using spectroscopic charge pumping

The discrepancy between mobility and D_{it} is a result of the different energetic distributions of interface/border states for both crystal planes. The energetic distribution of D_{it} was extracted using spectroscopic charge pumping following the approach of van den Bosch [89]. A short introduction to the technique is given in Section 1.3.4. By varying the rise and fall times in addition to the measurement temperature, the active energy window ΔE_{CP} changes according to (2.14). Thereby one is able to scan a large fraction of the SiC band gap and calculate D_{it} from the change in the charge pumping current. Fig. 2.30 shows I_{CP} as a function of the rise time (triangles up) and fall time (triangles down) of the gate pulse in a temperature range between −60 °C (blue) and 200 °C (red) for the Si-face device.

By calculating ΔE_{CP} for every data point using (2.14), one is able to extract the energy distribution of traps, which contribute to the charge pumping signal. The outcome is shown in Fig. 2.31 for both crystal faces. Starting with the Si-face (top), one observes a D_{it} of approximately $0.25 \times 10^{12}\,\mathrm{cm^2\,eV^{-1}}$ around mid-gap, which furthermore increases exponentially close to the conduction band edge of 4H-SiC, resulting in a bad mobility. The a-face device (bottom) shows an approximately 5 times higher D_{it} around mid-gap resulting in a more pronounced *subthreshold* hysteresis, whereas the D_{it} is much lower close to E_C favoring higher mobility. The difference in D_{it} close to the conduction band edge for a-face and Si-face devices annealed in nitric oxide (NO) is supported by the results of Kimoto *et al.* [118] who used the $C - \psi_s$ method, which is based on the theoretical

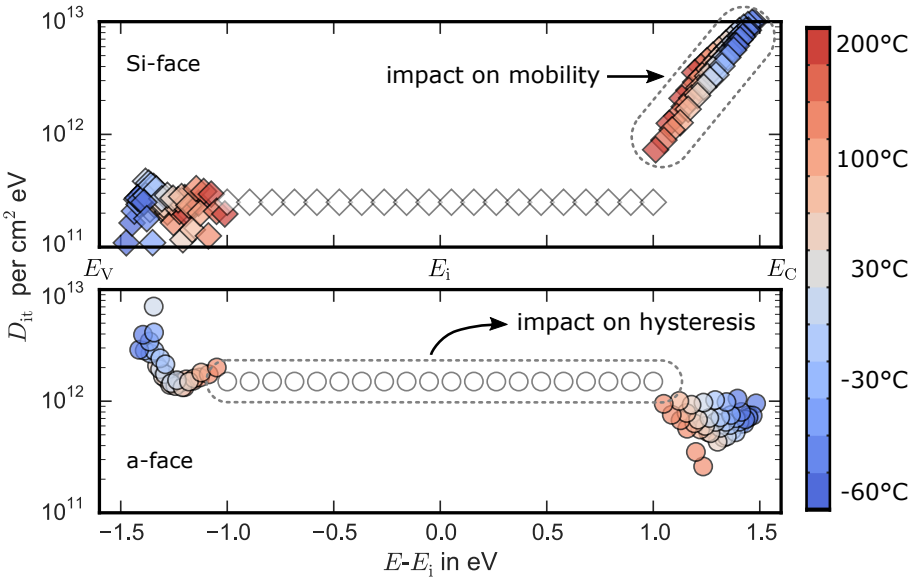


Fig. 2.31 Energetic distribution of interface states for the Si-face (diamonds, top) and a-face (circles, bottom). Although the a-face shows 5 times higher D_{it} around midgap resulting in a more pronounced hysteresis, the D_{it} close to E_C is about one order of magnitude lower resulting in improved mobility. Note that for the a-face device, the points close to E_C do not overlap. This is because most of the charge pumping signal of the a-face device originates from deep states, which results in a very bad signal-to-noise ratio close to the band edges.

capacitance curve of the devices and does not give any information about states deep in the band gap.

2.7 Possible atomic origin

Ion contamination as an origin of the ΔV_{th}^{sub} is excluded by three reasons. First, the capture and emission times are too fast for ion movement. Second, the hysteresis is already observed and nearly unchanged at low temperatures where ion movement is suppressed (e.g. $-60\,°C$). Third, the sign of ΔV_{th}^{sub} caused by typical ion contamination such as K^+ or Na^+ would be inverted (e.g. a negative ΔV_{th} for positive bias stress) [119].

Electrically detected magnetic resonance (EDMR) measurements by Gruber *et al.* in combination with density functional theory (DFT) simulations by Cottom *et al.* demonstrate that the dominant hyperfine EDMR spectrum at the SiC-SiO_2 interface of Si-face MOSFETs (see. Fig. 2.32) can be understood in terms of carbon dangling bonds (P_{bC} centers) [5, 99, 120]. The atomic configuration of this defect is shown schematically in Fig. 2.33. Recent work by Gruber shows an increased P_{bC} signal on a-face devices indicating an increased density of these traps [121]. Due to this, a possible origin of the observed difference in hysteresis could involve the increased carbon density at the surface of the a-face and therefore a higher density of P_{bC} centers at the SiC-SiO_2 interface. These results fit well to the difference in trap density extracted via the sweep hysteresis and charge pumping measurements. Therefore, P_{bC} centers are suggested as the most promising defect candidates for the subthreshold hysteresis effect, although this is still based on limited

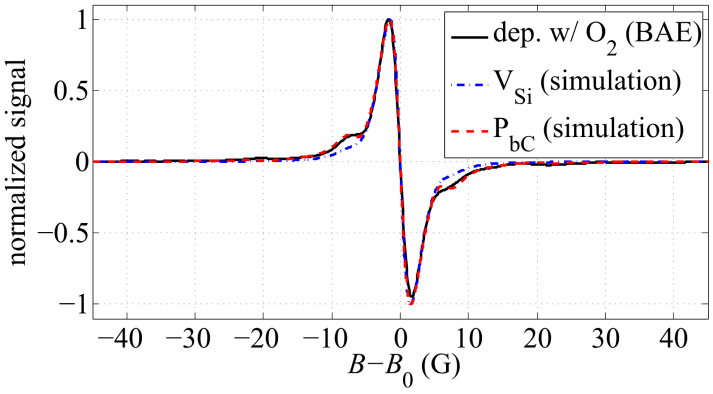


Fig. 2.32 EDMR spectrum of NO annealed Si-face SiC nMOSFETs. The observed signal shows good agreement with a simulated signal of carbon dangling bonds (P_{bC} centers) [120].

literature and further studies on the electrical responses of carbon dangling bonds are needed.

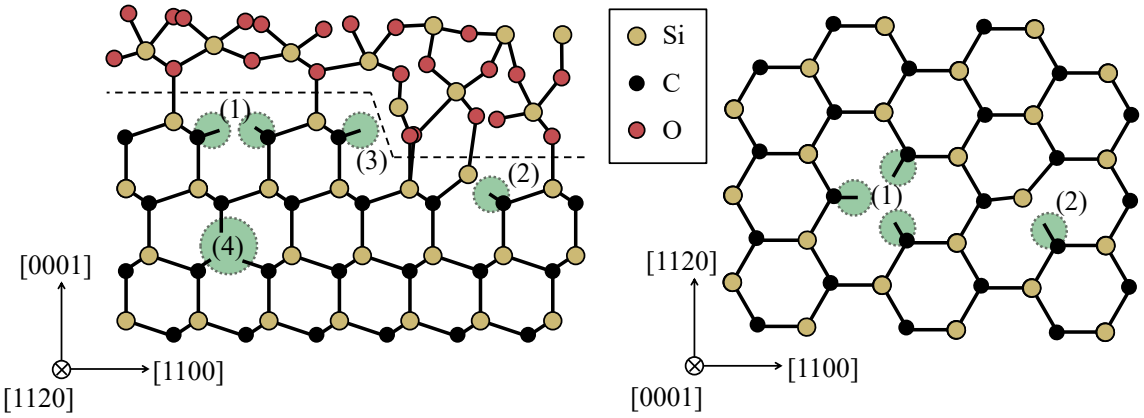


Fig. 2.33 Schematic view of the silicon vacancy (V_{Si}) and the P_{bC} that were considered for comparison with the EDMR measurements [5, 99]. 1) V_{Si} on a terrace, 2) P_{bC} at a terrace, 3) P_{bC} on a step edge, 4) V_{Si} in the layer beneath the interface. Left: view along the [1120]-direction. Right: view along the [0001]-direction [5].

2.8 Hysteresis on devices by various manufacturers

To compare the hysteresis of 4H-SiC MOSFETs produced by different manufacturers, the transfer characteristics have been extracted from devices of the three most important manufacturers. The outcome is shown in Fig. 2.34 for the previous (left column) and current (right column) generation of devices. MOSFETs with a lateral channel design are shown in green, whereas devices with a trench channel design are indicated in blue. Devices are labeled A, B and C to maintain manufacturer anonymity.

Fig. 2.35 shows the number of trapped charges per device area extracted from the input characteristics in Fig. 2.34. The left bar always shows the previous technology generation of each manufacturer, whereas the right one shows the current device generation. As can be immediately seen, the main impact on the sweep hysteresis originates from the crystal

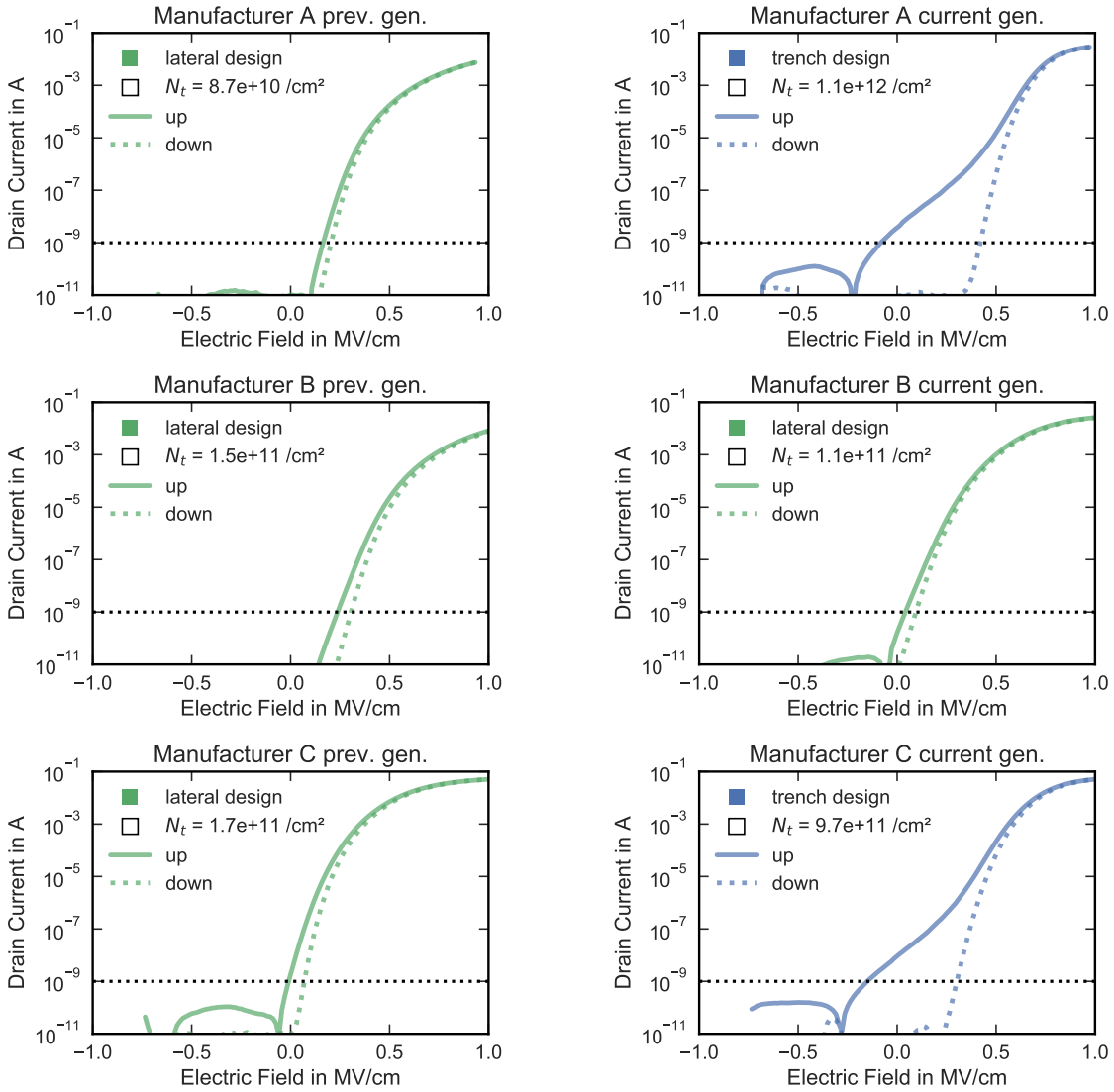


Fig. 2.34 Transfer characteristics from devices of three different manufacturers. The previous device generation is given on the left, whereas the current device generation is given on the right side. Devices with the inversion channel on the [0001]-plane are indicated in green, whereas devices with the inversion channel along the *c*-axis (trench design) are indicated in blue. Trench devices show an increased hysteresis and therefore an increased number of trapped charges by approximately one order of magnitude.

plane of the inversion channel (trench or lateral) and is nearly independent of the device manufacturer. For Si-face devices, N_t is in the range of $0.1 \times 10^{12}\,\mathrm{cm}^{-2}$ to $0.2 \times 10^{12}\,\mathrm{cm}^{-2}$, whereas for trench devices, N_t is in the range of $0.9 \times 10^{12}\,\mathrm{cm}^{-2}$ to $1.1 \times 10^{12}\,\mathrm{cm}^{-2}$.

2.9 Relevance of the hysteresis on normal device operation

The hysteresis effect discussed in this work is an outstanding difference between silicon and silicon carbide based MOSFETs. It is an intrinsic feature of MOSFETs based on wide bandgap semiconductor substrates. The reported hysteresis effect is visible on both

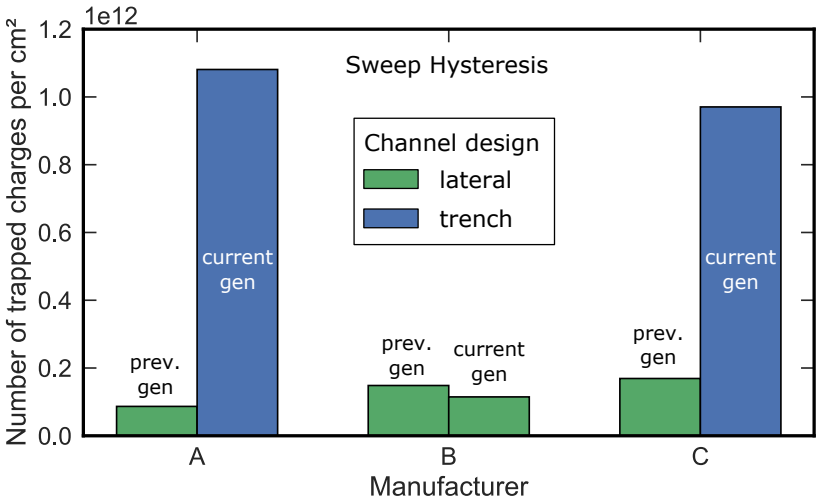


Fig. 2.35 Number of trapped charges extracted from the input characteristics for three different manufacturers. The left bar corresponds to the previous generation of each manufacturer, whereas the right bar shows the performance of the current device generation. As can be seen, the main impact on the sweep hysteresis originates from the crystal plane of the channel and is nearly independent of the device manufacturer.

investigated crystal faces and mainly present in the subthreshold regime, where the on-resistance R_{on} of the device is still in the range of several megaohms. In saturation mode above threshold ($V_{\mathrm{G}} \geq V_{\mathrm{th}}$, see inset in Fig. 2.1) the hysteresis vanishes. Consequently, the reported subthreshold hysteresis does not cause a dynamic change of R_{on} during normal operation on a-face and Si-face devices and its impact on hard switching operation (e.g. switching very fast between accumulation and inversion) is negligible.

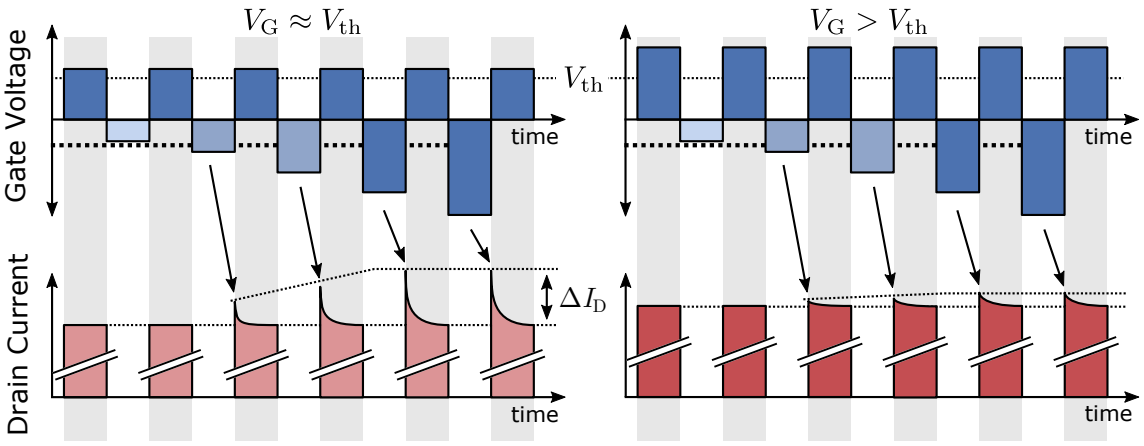


Fig. 2.36 Drain current overshoot due to the hysteresis effect for switching gate bias with the high level close to V_{th} (left) and higher (right). The overshoot of the drain current strongly depends on the minority carrier density in the channel and is therefore less important for typical operating conditions above V_{th} (right).

It is important to emphasize that the reported hysteresis is not identical to classical BTI and cannot be considered as degradation. It is a fully reversible and reproducible

effect which occurs on SiC-based MOSFETs and may have the following effects in the application:

(i) it may reduce switching losses because it actively supports turn-on and turn-off of the transistor due to the lower V_{th} during turn-on and higher V_{th} during turn-off.

(ii) it may cause a drain current overshoot when using fast switching slopes (high $\Delta V/\Delta t$). This overshoot is due to a temporary higher overdrive and a lower channel resistance at the very beginning of the high phase of the gate pulse.

(iii) a short accumulation pulse might lead to a leakage current at 0 V and increases the possibility of a parasitic turn-on due to the negative voltage shift.

According to available literature on the hysteresis [29, 43, 112], it has no negative effect on the performance and on the reliability of SiC MOSFETs. Nevertheless, it needs to be considered and understood in order to include the effect into circuit simulation and to correctly perform and assess threshold voltage measurements and BTI, as will be explained in Chapter 3.

2.10 Conclusions

In this chapter, the drain current hysteresis during up- and down-sweeps of the gate voltage in 4H-SiC MOSFETs with the inversion channel either on the Si-face, (0001)-plane, or the a-face, $(11\bar{2}0)$-plane was investigated. The subthreshold drain current of SiC-MOSFETs at a certain gate voltage strongly depends on the preceding gate voltage. A gate voltage sweep from accumulation to inversion results in lower $V_{\mathrm{th}}^{\mathrm{sub}}$ than a gate voltage sweep from inversion to accumulation.

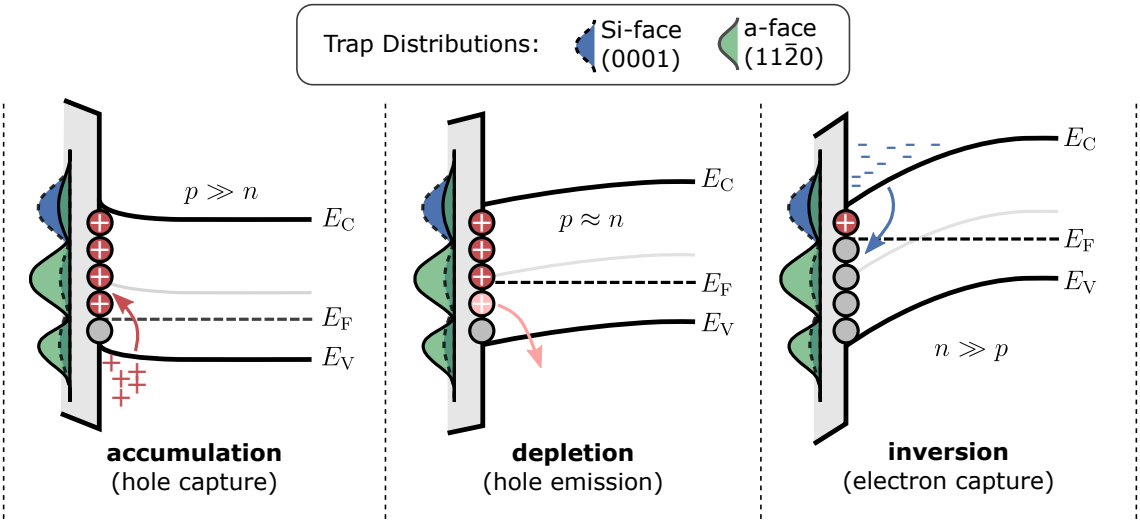


Fig. 2.37 Schematic band diagram of the mechanism causing the sweep hysteresis. Left: hole capture in accumulation (Fermi level close to the valence band). Middle: At a Fermi level position close to mid gap only a few carriers are available resulting in a slow recovery of the trapped holes due to hole emission from deep states. Right: recombination due to very high electron density at the interface for a Fermi level position close to the conduction band (electron capture).

The *subthreshold* voltage $V_{\mathrm{th}}^{\mathrm{sub}}$ (as defined by (2.1)) may fall below 0 V during up-sweeps depending on the up-sweep starting voltage. For the a-face device, we observe *subthreshold* voltage shifts up to $\Delta V_{\mathrm{th}}^{\mathrm{sub}} \approx -4.5\,\mathrm{V}$ after an accumulation pulse which corresponds to about $1.4 \times 10^{12}\,\mathrm{cm}^{-2}$ trapped charges whereas for Si-face devices we observe an approximately 10 times smaller trap density of $0.1 \times 10^{12}\,\mathrm{cm}^{-2}$. Furthermore, it is important to note, that the data-sheet threshold voltage V_{th}, which is (unlike the *subthreshold* voltage $V_{\mathrm{th}}^{\mathrm{sub}}$) typically measured at much higher drain currents of 1 mA to 10 mA where the channel is much stronger inverted, remains always safely above 0 V. Thus, the normally off characteristics of the SiC-MOSFET are maintained in any switching case despite of the reported hysteresis effect in the subthreshold regime.

The *subthreshold* voltage shift scales linearly with the N_{CP} extracted from charge pumping measurements, suggesting that deep level interface traps are responsible for the hysteresis. In general, a-face devices show a more pronounced hysteresis due to a higher interface trap density around mid gap, but also higher mobility due to a lower D_{it} close to the conduction band edge of 4H-SiC. The observed hysteresis is caused by hole capture which occurs for negative gate voltages corresponding to a Fermi level position below the intrinsic Fermi level. Capture and emission times of the holes scale with interface carrier density, which is why hole capture in accumulation and electron capture in inversion occurs within several nanoseconds whereas electron capture in depletion is much slower due to the low free carrier density in the channel at a Fermi level position around midgap. A schematic illustration of the charging/discharging model is provided in Fig. 2.37. Here the interface trap distribution is shown in blue for the Si-face devices and in green for the a-face MOSFETs.

The atomic origin of the sweep hysteresis and the difference in hysteresis for a-face and Si-face 4H-SiC power MOSFETs is suggested to be due to the difference in interface structure and especially the varying density of carbon dangling bonds ($\mathrm{P_{bC}}$-centers) on both crystal planes, which have been suggested as the origin of the dominant hyperfine EDMR spectrum in SiC based n-channel MOSFETs by Gruber *et al.* [5, 120] and Cottom *et al.* [99]. Ion contamination as a cause of the hysteresis is excluded by the sign of the threshold voltage shift, the speed of the capture and emission process and the temperature dependence.

The charging/discharging of the interface during up- and down-sweep does not cause any permanent degradation of the device and also does not show any influence on the reliability. The negative $V_{\mathrm{th}}^{\mathrm{sub}}$ shift caused by an accumulation pulse is fully recoverable via biasing the device subsequently near or above its threshold voltage. Even after several million charging and discharging repetitions, which for example occur during AC-use conditions, no permanent $\Delta V_{\mathrm{th}}^{\mathrm{sub}}$ component is observed suggesting fully reversible trapping and detrapping mechanism.

CHAPTER 3

On the second Component: Bias Temperature Instability

Contents

Abstract. In the first part of this chapter the threshold voltage instability of commercially available SiC power MOSFETs or prototypes from four different manufacturers under positive bias temperature stress is investigated. It is demonstrated that all SiC-MOSFETs from different manufacturers available on the market show nearly identical voltage shift behavior even under a low-bias operation close to the threshold voltage indicating that the observed V_{th} instabilities are likely a fundamental physical property of the SiC/SiO_2 system caused by electron trapping in border states which are energetically located close to the conduction band of 4H-SiC.
In the second part of this chapter it is shown that when using JEDEC-like measurement patterns, MOSFETs based on 4H-SiC show amplified voltage shifts during gate bias stress compared to their silicon based counterparts. The majority of the extracted voltage shift originates from fully-reversible components and strongly relies on stress independent measurement conditions such as the reference point for the calculation of the voltage shift and timing parameters. An enhanced bias temperature instability measurement technique using device preconditioning is presented and compared to standard JEDEC-like measurement patterns developed for BTI evaluation of silicon MOSFETs. The proposed preconditioned measurement allows for accurate and nearly delay and recovery time independent extraction of the permanent component within typical industrial timescales. Therefore, the proposed technique allows for a more accurate lifetime prediction of SiC power devices.

3.1 Investigated Devices

In the first section, commercially available SiC-MOSFETs from four different manufacturers are compared regarding their threshold voltage shift under positive bias temperature stress. The devices are labeled A, B, C and D to preserve manufacturer anonymity. All devices were measured at a drain voltage of $V_{\mathrm{D}} = 0.01\,\mathrm{V}$ in a temperature range between $-60\,^{\circ}\mathrm{C}$ and $150\,^{\circ}\mathrm{C}$.

In Section 3.3, all devices were fabricated *in-house* on 4H-SiC n-doped substrates using an industrial process. A schematic layout of the n-channel $(11\bar{2}0)$-plane (a-face) MOSFETs is given in Fig. 1.13 (left). The SiO_2 gate dielectric was deposited via CVD for all devices. POA was done in an optimized NO containing atmosphere for all samples. A detailed description of the measurement system is given in Section 1.11.

3.2 Similarities in BTI of commercially available SiC-power MOSFETs

Here, we compare the threshold voltage instability of commercially available, application ready SiC-MOSFETs under PBTS. The fact that SiC based MOSFETs show an increased bias temperature instability is well known from countless studies [25, 31, 33, 36–39, 42, 43, 107, 119, 122–127]. However, most of these studies are based on devices which are only optimized for single parameters like mobility or voltage shift characteristics and therefore not ready for application. An application ready device on the other hand, needs to be reliable, meaning *every* device parameter has to stay within a well defined threshold within

the devices lifetime. Furthermore, these MOSFETs have to provide excellent electrical characteristics. Therefore, such a device needs to be optimized with respect to multiple parameters like channel mobility, oxide reliability, and bias temperature instability. Due to this, compromises (trade-offs) are inevitable for certain key-parameters. This results in the fact that commercially available devices usually will not perform as well as devices reported in literature, where (in general) test structures optimized for a single parameter are investigated.

Therefore, this section provides an overview on the BTI of state-of-the-at SiC-MOSFETs, which are already available on the market and optimized for power-electronics and reliability. It will be shown that all of these devices show very similar drift characteristics in the low-bias regime.

3.2.1 Low-field mobility

At first I start by analyzing the low-field channel mobility μ_0 of the devices, which is usually a good indicator for the quality of the SiC/SiO_2 interface. The mobility was extracted via the input characteristics using the method of Ghibaudo [78] (c.f Section 1.3.3) for the devices from manufacturers A, B, and D. Manufacturer C is missing due to unknown channel dimensions of the device. The extracted mobility values are $8\,cm^2\,V^{-1}\,s^{-1}$ for device A, $19\,cm^2\,V^{-1}\,s^{-1}$ for device B and $58\,cm^2\,V^{-1}\,s^{-1}$ for device D. These mobility values are far below the bulk mobility of 4H-SiC, which is around $800\,cm^2\,V^{-1}\,s^{-1}$ [6] and furthermore below the maximum reported mobilities achieved in some recent studies (e.g. up to $100\,cm^2\,V^{-1}\,s^{-1}$ in Ref. [111, 115]). Note that most of these studies are based on lateral MOSFETs, which are not optimized for power electronics and reliability. Therefore, a lower mobility is expected for commercially available SiC-MOSFETs which have to be reliable in high power and high temperature use-conditions.

3.2.2 Measurement pattern

To investigate the threshold voltage instability of the devices under *low-bias*, all MOSFETs were subjected to positive bias stress according to the pattern sketched in Fig. 3.1. The

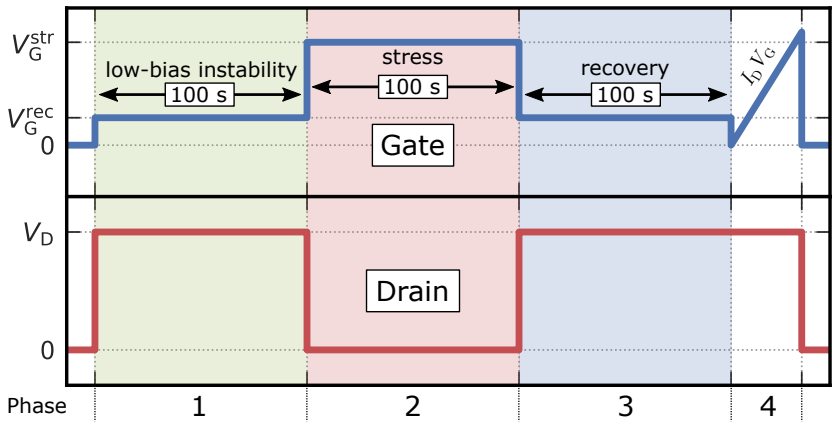


Fig. 3.1 Test pattern for bias temperature stress tests.

measurement sequence consists of 4 different phases starting with a bias switch from $V_G = 0\,V$ to $V_G^{rec} = 5\,V$, which is close to the data-sheet threshold voltage of all devices. Here, the bias is held for 100 s to measure the *low-bias* drain current instability (phase 1).

Afterwards, a stress cycle is performed at a gate voltage of $V_G^{str} = 25\,V$ for a stress time of $t_{str} = 100\,s$ (phase 2). The stress voltage was chosen so that the applied positive bias stress of 25 V is within the allowed maximum gate bias range mentioned in the data sheets of all devices. After the stress phase, another low-bias phase at $V_G^{rec} = 5\,V$ is measured (phase 3) to investigate the time dependent recovery of the threshold voltage shift ΔV_{th} after the 25 V positive bias stress. At the end of the measurement pattern (phase 4), an I_D-V_G curve from $-2\,V$ to 26 V is measured to be able to calculate ΔV_{th} from the change in the drain current during the phases 1 and 3. The whole procedure was repeated at various temperatures between $-60\,°C$ and $150\,°C$ on the same device to also investigate the temperature dependence of the low-bias instability and recovery traces. The drain voltage was set to $V_D = 0.01\,V$ in the phases 1, 3, and 4, whereas V_D was set to 0 V during the stress (phase 2) to suppress self heating, hot carrier degradation and non-uniform electric oxide fields.

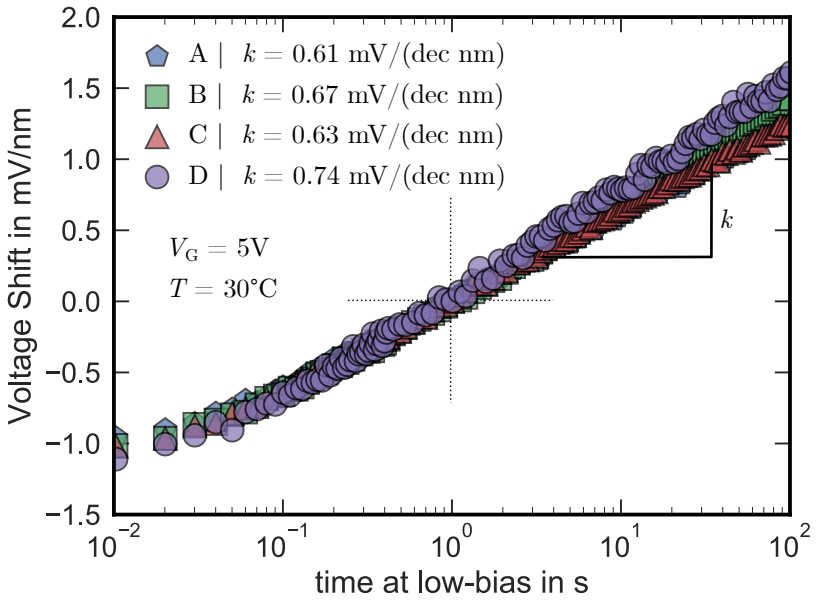


Fig. 3.2 Voltage shift per nanometer oxide thickness after switching from $V_G = 0\,V$ to $V_G^{rec} = 5\,V$, which is slightly above threshold. Although the data is extracted from devices from 4 different manufactures, all show nearly identical behavior with voltage shifts of approximately $0.65\,mV\,nm^{-1}dec^{-1}$.

3.2.3 Low-bias instability

We start by analyzing the drain current I_D transients of the devices under *low-bias* in phase 1. Here, the bias is switched from from $V_G^{rec} = 0\,V$ to $V_G^{rec} = 5\,V$, which is slightly above the threshold voltage V_{th} of all devices (3 V to 4 V). Even at such a low gate bias, drain current transients are observed for all devices. The resulting voltage shift is indicated in Fig. 3.2. All devices show similar drift behavior in the low gate bias regime at $30\,°C$ within the measurement window, which ranges from 10 ms to 100 s. ΔV_{th} follows a logarithmic behavior with slopes around of 0.65 mV per decade per nanometer oxide thickness within our narrow experimental window. Here, ΔV_{th} is normalized to the oxide thickness t_{OX} to account for differences in t_{OX} between the various manufacturers.

Since the input characteristics used for the calculation of ΔV_{th} is shifted to the end of the measurement pattern, the reference value of the threshold voltage of all tested devices originates from the amount of charges captured and emitted during the whole test procedure. Therefore, the *real* point of origin is unkown and all traces in Fig. 3.2 are vertically shifted to a threshold voltage shift ΔV_{th} of 0 V after 1 s (dotted cross) for better comparability. The same holds for all subsequent figures in this section.

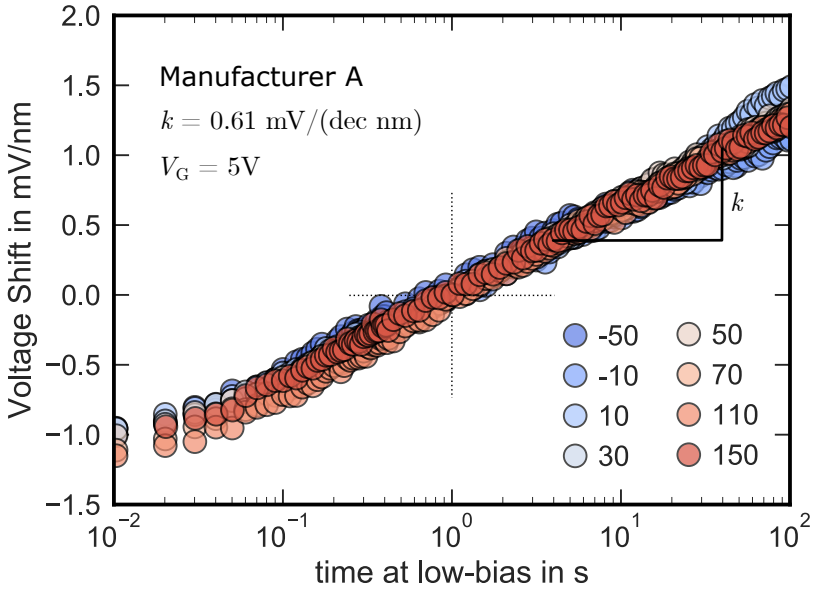


Fig. 3.3 Temperature dependence of the *low-bias* voltage shift per nanometer oxide thickness. Within a temperature range from −50 °C to 150 °C no temperature dependence is visible, which indicates broadly distributed activation energies as described in Section 1.2.1. The picture shows the traces of device A. Devices B, C, and D show the same behavior.

Temperature dependence of the low-bias voltage shift

The temperature dependence of the low-bias threshold voltage instability of device A is shown in Fig. 3.3. Within the measurement range between −50 °C and 150 °C the low-bias instability has a constant value of $\approx 0.6\,\mathrm{mV\,nm^{-1}dec^{-1}}$, which is independent of the device temperature within the investigated temperature range. The same trend is observed for the devices B, C, and D (not shown). Such a temperature independent low-bias ΔV_{th} is most likely observed due to broadly distributed activation energies within the, in this special case, narrow experimental window (c.f Section 1.2.1).

3.2.4 Recovery after high bias stress

The recovery traces of ΔV_{th} at $V_{\mathrm{G}}^{\mathrm{rec}}$ after the 100 s long 25 V stress at 30 °C are shown in Fig. 3.4. Again, we observe a similar behavior for devices A (-1.5 mV/dec/nm), B (-1.1 mV/dec/nm), C (-1.4 mV/dec/nm) and D (-1.5 mV/dec/nm). The temperature dependence of the recovery traces for device A is shown in Fig. 3.5. Devices B, C and D show a similar behavior (not shown). Unlike the low-bias instability, the recovery slope increases with decreasing temperature and furthermore deviate from the power-law behavior observed

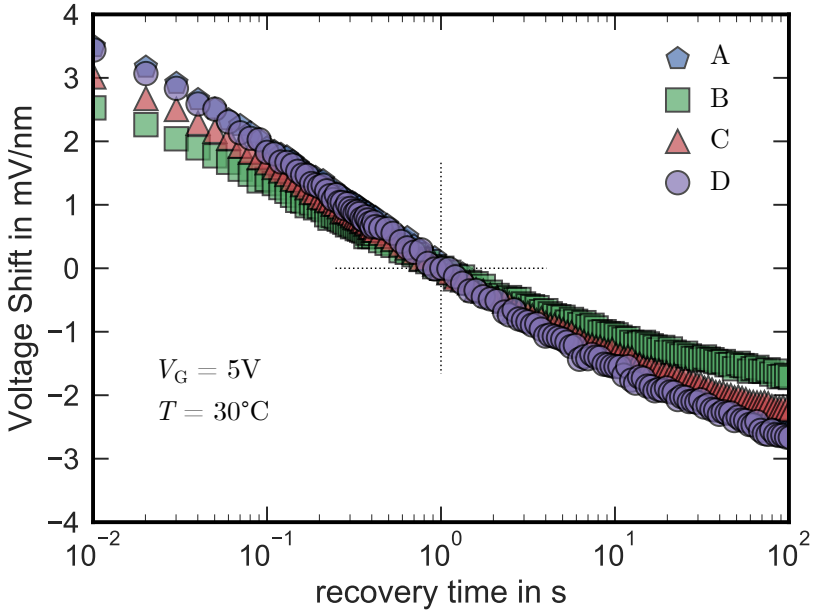


Fig. 3.4 Recovery of the threshold voltage shift divided by the oxide thickness at a positive bias of 5 V after the positive bias stress of 25 V for 100 s. Devices A, B and C show similar recovery rates while device B shows a slower recovery.

withing the narrow experimental window during phase 1. Cold temperatures slow down the emission of trapped carriers. This behavior indicates that, at 30 °C, a considerable amount of recovery takes place outside the experimental window and occurs within the first 10 ms after the bias is applied and thus before the first measurement point. Therefore, only the tail of the ΔV recovery curve is visible, which explains the decreasing recovery slope for high temperatures. The increase in recovery slope is in contrast to silicon based devices, which show a constant recovery slope in a wide temperature range [128].

A comparison of the recovery and low-bias instability slopes of the devices A, C and D is shown in Fig. 3.6 indicating temperature independent low-bias instability and increasing recovery slope with decreasing temperature for all devices. Although the devices from different manufactures differ in the absolute values of the threshold voltage shift, the similar tendencies of all traces indicate that all observed V_{th} instabilities are likely a fundamental physical property of the SiC/SiO_2 system and not related to, e.g. mobile ion contamination, fundamental differences in device processing, chip-package interaction or other issues. It is furthermore important to state that, unlike in silicon devices, most of the ΔV_{th} does not originate from a permanent damage of the interface (e.g. H-bond breakage) and is nearly fully recoverable, as will be shown in Section 3.3.

3.2.5 Summary

All SiC-MOSFET available on the market show nearly identical threshold voltage instabilities caused by trapping and detrapping of charges in oxide or near interface traps. The trapping/detrapping effect appears to be a fundamental property of the SiC/SiO2 system. As opposed to commercially available silicon-based MOSFETs, even an operation at low constant bias close to the threshold voltage causes a threshold voltage shift in the range of tens of millivolts. However, the actual mechanism causing the majority of the voltage

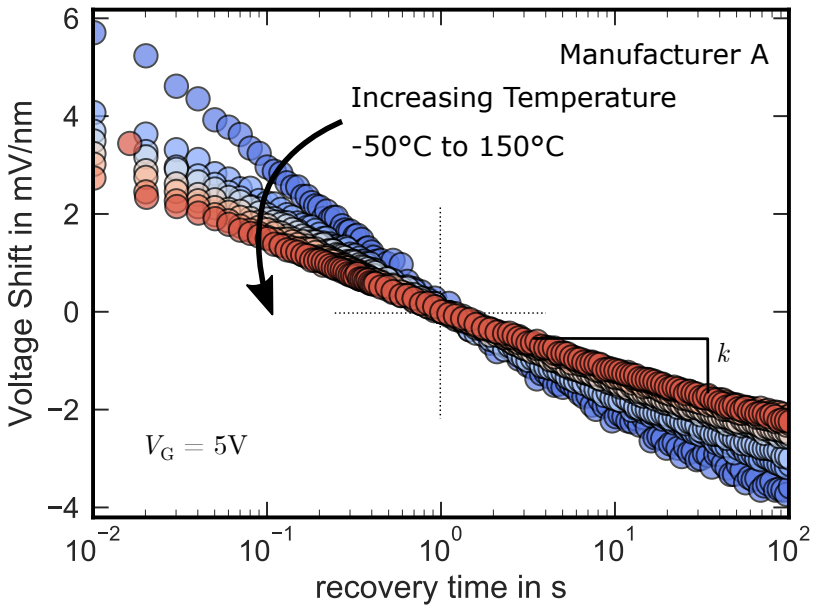


Fig. 3.5 Temperature dependence of the ΔV recovery at V_G^{rec} after the 25 V positive bias stress for 100 s (device A). The recovery slope decreases with increasing temperature. The same trend is observed for all devices. This outcome indicates that most of the recovery already occurs within the first 10 ms after the end of the stress pulse.

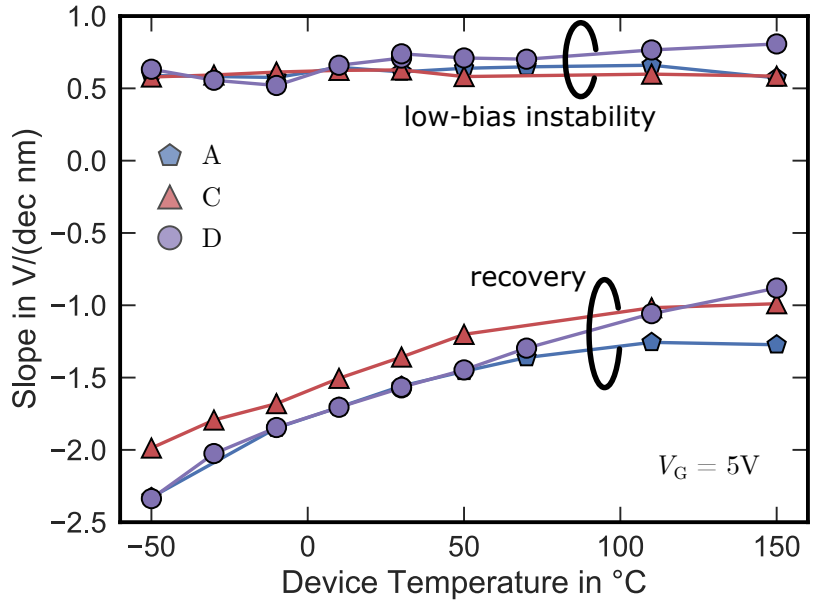


Fig. 3.6 Temperature dependence of devices A, C and D. The slopes of the low-bias instability at 5 V stay nearly constant in the measured temperature range between −50 °C and 150 °C at about 0.65 mV/dec/nm for all devices. The slope of the recovery traces increases with decreasing temperature indicating the majority of carrier detrapping occurs within 10 ms after the end of the stress pulse.

shift in SiC devices differs from silicon and does not cause a permanent damage to the interface. The more pronounced trapping in the SiC/SiO2 system is likely a consequence of the different energetic positions of the 4H-SiC conduction and valence band edges allowing for a wider range of carrier exchange with traps near the SiC/SiO2 interface [37].

3.3 Preconditioned BTI measurements

This section focuses on various ΔV extraction techniques after positive bias stress. It will be demonstrated that most of the voltage shift ΔV typically observed in standardized measurement tests (e.g. JEDEC-like) on 4H-SiC devices results from erroneous extraction techniques including stress independent but fully reversible components, which do not degrade the device performance under regular dynamic operation. A new drift evaluation technique based on *device preconditioning* before each ΔV readout is presented which allows for a more comprehensive and nearly measurement delay- and recovery time independent determination of the permanent voltage shift component $P(t_{\mathrm{str}})$. This component emerges after AC and DC stress and is of fundamental importance from an application perspective.

3.3.1 The impact of thermal non-equilibrium during the reference readout

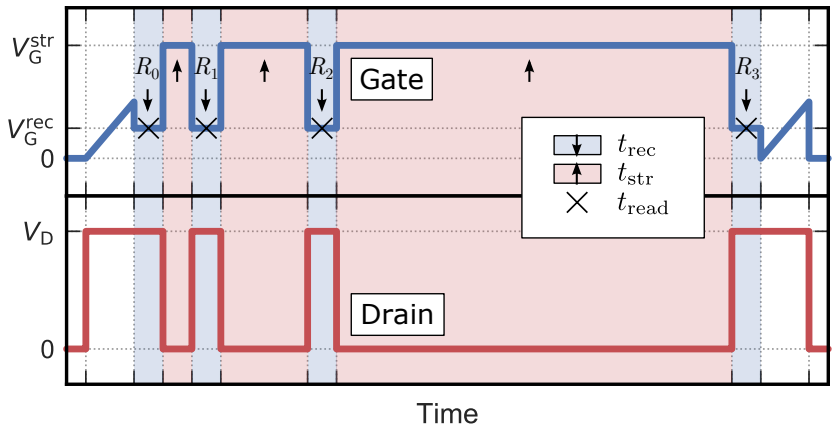


Fig. 3.7 BTI measurement pattern according to JEDEC standard JESD 241 [129].

A BTI measurement test according to JEDEC standard JESD 241 [129] is shown in Fig. 3.7. The measurement pattern consists of a V_{G} sweep from 0 V to the maximum sweep voltage $V_{\mathrm{G}}^{\mathrm{swe}}$ for the calculation of the voltage shift followed by a repeated readout cycle at the recovery voltage $V_{\mathrm{G}}^{\mathrm{rec}}$ in sequence with a stress cycle at the stress voltage $V_{\mathrm{G}}^{\mathrm{str}}$ with logarithmically increasing stress times t_{str}. The drain voltage V_{D} is turned off during every stress cycle to suppress device heating, non-uniform electric oxide fields and hot-carrier degradation. After each stress pulse, the voltage shift ΔV is calculated from the recovery drain current with respect to the reference drain current at the initial readout cycle (marked with R_0). The drain current at each subsequent readout cycle R_i is extracted at $t_{\mathrm{read}} = 100\,\mathrm{ms}$ after the end of the stress pulse. The resulting voltage shift ΔV is shown in Fig. 3.8 (JED, blue) after application of a stress voltage equal to two times the operation voltage $V_{\mathrm{G}}^{\mathrm{op}}$ for stress times up to 1444 s at 30 °C. Using JESD 241, a voltage shift ΔV of 400 mV after 1444 s stress is recorded. A slightly changed but common variation of the JESD 241 standard measurement is shown in Fig. 3.9. The pattern is similar to the pattern

sketched in Fig. 3.7 with one small deviation: we introduce a 10 s delay at $V_G = 0$ V before the reference readout R_0 to represent the influence of the often ill-defined measurement delay. Although at first glance this modification appears to be negligible, the influence on the extracted voltage shift is significant as can be seen in Fig. 3.8 (JED0, green). While the trend over time does not change, an offset of approximately $\Delta V_0 = 200$ mV is introduced which is merely due to changing the bias value prior to the reference readout R_0.

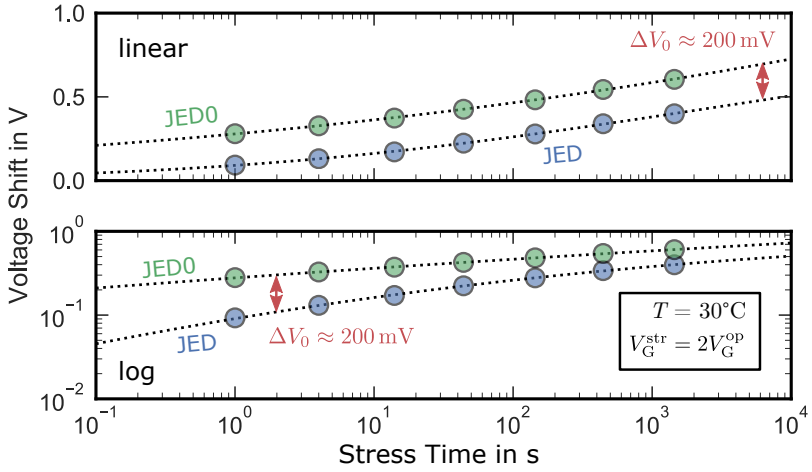


Fig. 3.8 Voltage shift extracted via JEDEC standard (JED) according to Fig. 3.7 in comparison with the delayed JEDEC (JED0) according to Fig. 3.9. V_G was set to 0 V for 10 s before the reference readout. The minor change to the measurement pattern results in a 200 mV offset in ΔV.

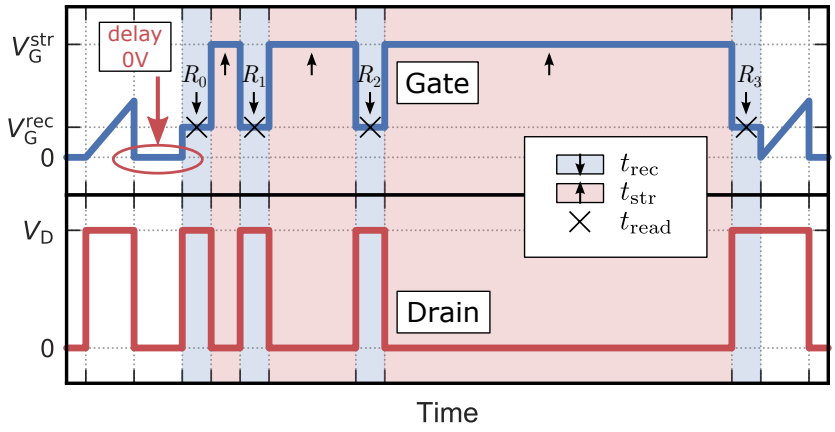


Fig. 3.9 Delayed BTI measurement pattern (JED0) similar to JEDEC JESD 241 (Fig. 3.7), but with a delay at $V_G = 0$ V before the reference readout R_0.

The offset ΔV_0 results from the fact that the reference readout R_0 strongly depends on the device bias history. Fig. 3.10 shows I_D at R_0 ($V_G = V_G^{rec}$) for both measurement patterns. The blue curve represents the measurement pattern according to JEDEC JESD 241 (JED), whereas the green curve represents the same pattern with a 10 s delay at $V_G = 0$ V before R_0 (referenced to as JED0). For JED, we observe increasing drain current after the bias change from the end-of-sweep voltage V_G^{swe} to the readout voltage V_G^{rec}, indicating recovery of trapped electrons, which where captured at $V_G > V_G^{rec}$ during the

preceding voltage sweep. The opposite trend is observed for JED0 (green). At the same readout voltage, JED0 shows a higher and decreasing drain current resulting from carrier trapping in oxide/border traps.

We therefore conclude that the discrepancy in I_D at R_0 is due to the amount of time the system needs to reach thermal equilibrium at a certain gate voltage, meaning every trap state with an energetic position below the Fermi level E_F is filled with electrons and every trap state above E_F is empty. Especially in wide band gap semiconductors like silicon carbide, it may take a long time to reach thermal equilibrium.

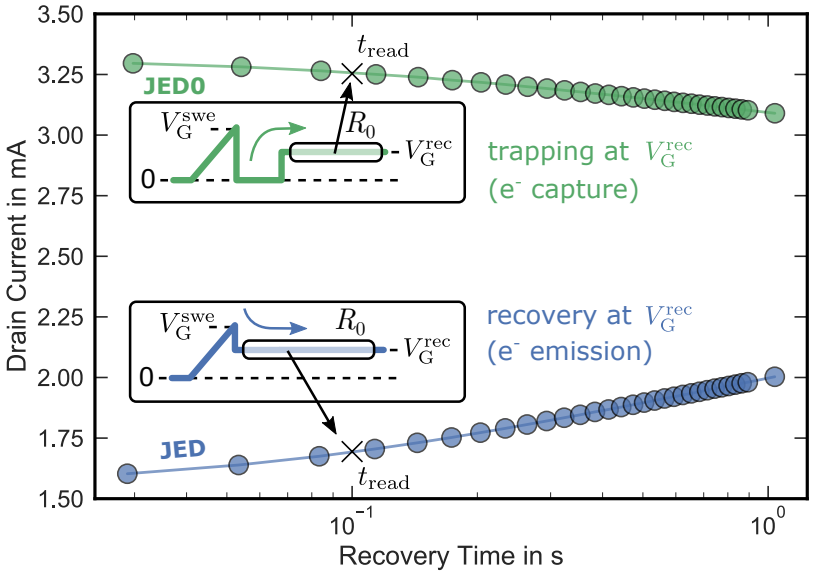


Fig. 3.10 Drain current at the reference readout R_0 for JED (blue, bottom) and JED0 (green, top). Trapping or detrapping behavior depends on the preceding gate bias. After the 0 V phase, I_D is higher and decreases over time (JED0, electron capture), whereas after the switch from V_G^{swe} to V_G^{rec}, the drain current is lower and increases over time (JED, electron emission).

3.3.2 The impact of measurement delay times on ΔV

In addition to a well defined reference readout R_0, the timing of each subsequent ΔV extraction point R_i after the stress cycle is of similar importance. An example for a delayed R_i, JEDEC-like readout is given in Fig. 3.11 (referred to as JEDd). The measurement pattern is similar to the JED pattern in Fig. 3.7, extended with a delay phase at $V_G = 0\,V$ for the delay time d after the stress cycle. Especially in industrial reliability tests, delayed measurements are very common since the stress cycle is usually done in special high temperature furnaces (accelerated BTI stress [130]) where many chips can be stressed in parallel for long times (e.g. 1000 h), whereas the readout is done outside the furnace sequentially for multiple devices at room temperature. The whole procedure of loading and unloading packaged devices naturally introduces a delay time d between the termination of the stress and the extraction point R_i.

The impact of d on ΔV is shown in Fig. 3.12 for multiple devices subjected to identical BTI stress. ΔV is measured according to Fig. 3.11 (JEDd). The delay time d varies from 0 s to 30 s (black, blue). We see a decreasing voltage shift for increasing delay times. An

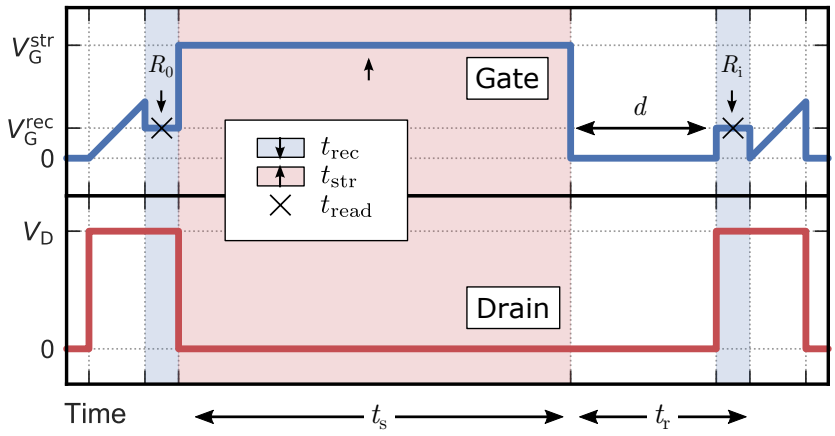


Fig. 3.11 Delayed JEDEC-like measurement (JEDd) similar to JESD 241 [129] extended with variable delay d at $V_G = 0\,V$ after the stress.

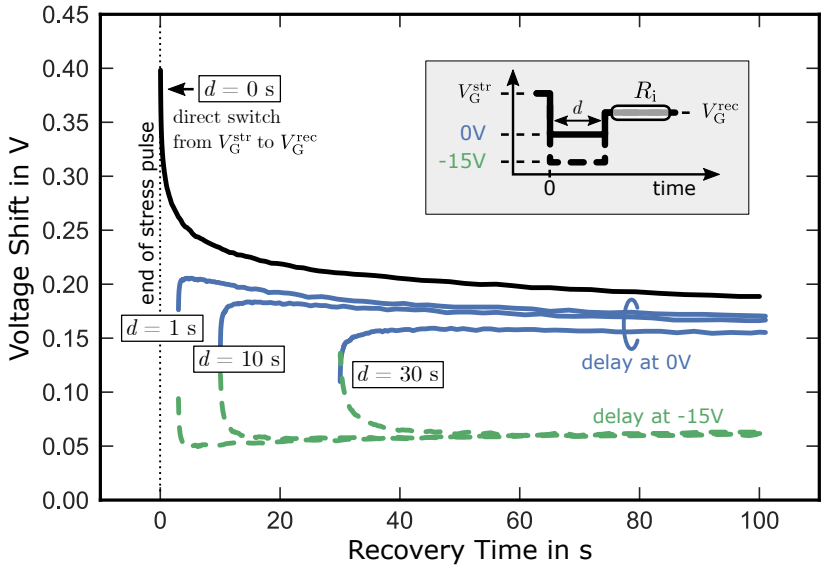


Fig. 3.12 Recovery behavior after identical positive bias stress depending on the delay time d. The black solid line represents ΔV with $d = 0$ (direct switch from V_G^{str} to V_G^{rec}). By introducing a delay phase at $V_G = 0\,V$ between the stress and the recovery phase, ΔV decreases with increasing delay time (blue). The measurement procedure is indicated in the inset.

explanation is given schematically in Fig. 3.13: the change in ΔV is caused by varying Fermi level positions prior to the ΔV extraction. As such, ΔV increases with stress time according to (1.4) (red) during the stress cycle at V_G^{str}. By directly switching to the recovery gate bias V_G^{rec} without any delay ($d = 0\,s$), ΔV follows the black recovery curve according to (1.6). By introducing a delay at $V_G = 0\,V$, E_F moves from a position close to the conduction band ${E_F}^{str}$ to a position around the midgap ${E_F}^{0V}$ leading to emission of trapped charges with energetic positions above ${E_F}^{0V}$, which results in a decrease of ΔV (dashed black). A subsequent bias change back to V_G^{rec} (blue) will lead to a superposition of charge trapping for trap states with energetic positions below ${E_F}^{rec}$ and above ${E_F}^{0V}$ (visible as the rising edge) and the ongoing charge transition of states above ${E_F}^{rec}$ which

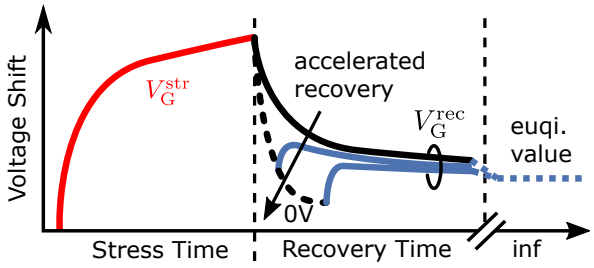


Fig. 3.13 Schematic recovery behavior after identical positive bias stress depending on the delay time d. The increased recovery mechanism is explained via a steeper recovery curve at $V_G = 0\,V$ (dashed, black). This effect is increased by using an accumulation pulse during d, which results in less dependence of ΔV on d as indicated in Fig. 3.12.

have not yet emitted their charge within d. As can be seen, the delayed recovery curve approaches a value smaller than recorded in the non-delayed trace (cf. Fig. 3.12). This effect depends strongly on the delay time and shows that the delay phase at 0 V increases ΔV recovery in comparison to V_G^{rec}. The same trend is observed for a floating gate contact during d (not shown), as would be the case in typical industrial measurements.

A feature that will be exploited in the following is the fact that ΔV is further decreased by using an accumulation pulse instead of 0 V/floating (Fig. 3.12, dashed, green) during the delay phase. In this example an accumulation pulse of $-15\,V$ is used for the same range of delay times resulting in a decrease of ΔV from $> 150\,mV$ to approximately 60 mV after $t_{rec} = 100\,s$.

3.3.3 Preconditioned BTI

As mentioned before, BTI measurements of SiC-MOSFETs are highly sensible to the exact bias and timing conditions of each voltage shift readout (Fig. 3.12). Therefore, no reliable estimation of a permanent component $P(t_{str})$ of ΔV can be given. This is due to two essential facts: first, the extracted voltage shift ΔV depends on the reference readout R_0 timing and gate bias history since thermal equilibrium is not reached within a reasonable period of time, meaning a drain current transient is still noticeable due to ongoing charge capture/emission during R_0. Second, the switching condition of each additional readout R_i usually differs from the switching condition of R_0. For example in the JEDEC JESD 241 standard (Fig. 3.7), R_0 is monitored after the end-of-sweep voltage V_G^{swe}, whereas following readouts R_i are monitored after the stress voltage V_G^{str}. Therefore, the interface charging state differs for each readout, resulting in a stress independent offset in the extracted ΔV.

To overcome timing and bias dependent variations of ΔV, an optimized measurement pattern is proposed which is refer to as *device preconditioning*. The basic scheme is sketched in Fig. 3.14 for a positive bias stress pattern and consists of the following features: first, exactly the same accumulation preconditioning pulse before *each* readout cycle is introduced to ensure a well defined and comparable interface charge state at the instant V_G is switched to V_G^{rec}. By this, one isolates fast interface states (charging state is able to follow the gate signal) from application-relevant border states with slower time constants allowing for an extraction of ΔV nearly independent of the delay time d as will be shown in the next section. Second, voltage sweeps (if needed for the calculation of ΔV), are moved after the readout. Therefore, the bias sweep does not influence the charge state of the trapping centers during the readouts, allowing for a more comparable voltage shift extraction.

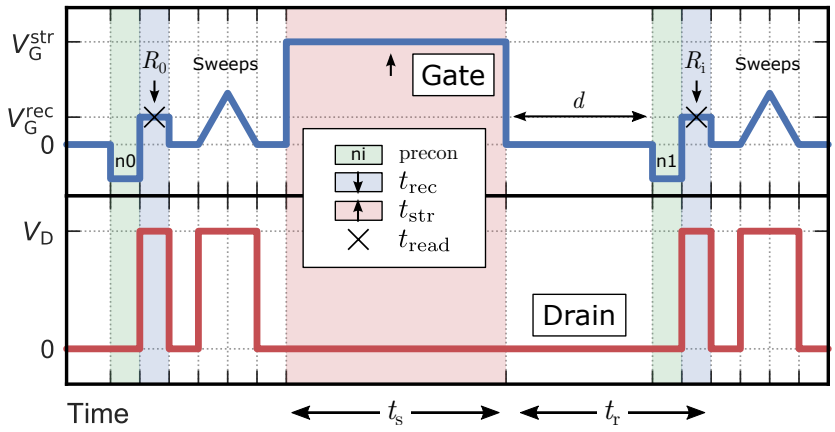


Fig. 3.14 Preconditioned BTI pattern (PRE) with accumulation pulse (n_i, green) before the reference readout R_0 and each subsequent readout R_i to maintain identical switching conditions.

3.3.4 Consequences of preconditioning

For further investigation of the impact of the suggested preconditioning measurement PRE (see Fig. 3.14) on the ΔV extraction, we compare the outcome of various "reference readout" R_0 and "readout after stress" R_i variations on the voltage shift recovery curves. The complete measurement pattern with the various investigated readout patterns, R_0 and R_i, are shown in Fig. 3.15. Here, we start with an I_D-V_G sweep (SWE) for the calculation of ΔV to include its impact on the subsequent readouts. For the reference readout R_0 we either use a bias switch from $V_G = 0\,V$ to V_G^{rec} (JED0, purple) or a preconditioned accumulation pulse readout as shown in Fig. 3.14 with a bias switch from 0 V to −15 V (for the preconditioning time $t_{pre}^{n} = 1\,s$) to V_G^{rec}, which we refer to as n0 (green). After the reference-readout, the device is subjected to a positive bias stress of $5\,MV\,cm^{-1}$ for a stress time of $t_{str} = 1\,ks$ (STR). After the stress pulse STR, ΔV extraction is done according to JEDEC JESD 241 by switching from V_G^{str} to V_G^{rec} (JED1, blue) or via accumulation pulse preconditioning identical to n0, referred to as n1 (green).

The corresponding voltage shift recovery traces are given in Fig. 3.16. Each recovery curve is given relative to one of the reference readouts JED0, n0 or SWE (indicated by the minus sign). At first, we start by analyzing the reference readout JED0, a simple bias change from 0 V to V_G^{rec}. As already discussed before and shown in Fig. 3.10, the drain current I_D at R_{JED0} changes over time and can be converted to a voltage shift ΔV by using the sweep SWE as reference. The outcome is shown in Fig. 3.16 as dotted purple line (JED0-SWE). In the JESD 241 measurement standard and numerous other studies, only a certain point in time t_{read} is used as the reference point for the calculation of ΔV after bias stress. Due to this major drawback of JEDEC-like measurements, ΔV changes drastically in amplitude and time dependence if t_{read} is changed. In our case, t_{read} represents the interface charge state 100 ms after switching to V_G^{rec}.

By using either SWE or JED0(t_{read}) as reference point, we are now able to extract ΔV induced by the stress phase STR as a function of the recovery time t_{rec}. Fig. 3.16 shows the change with respect to SWE (solid, blue) or JED0(t_{read}) (dashed, blue). Both curves only differ by an offset of $\Delta V_0 \approx 200\,mV$, which originates from the voltage shift of JED0 at t_{read}. The same effect was already shown in Fig. 3.8.

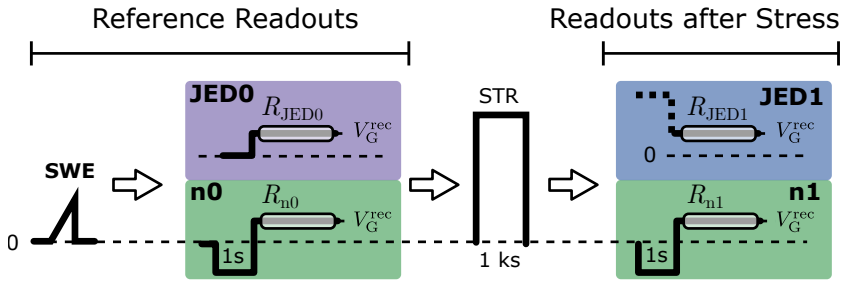


Fig. 3.15 Readout variations for the extraction of the voltage shift. For the reference readouts, we either use the sweep (SWE), a JEDEC-like readout with a bias switch from $V_G = 0\,V$ to V_G^{rec} (JED0, purple) or the preconditioning method with a preconditioning time of 1 s at $-15\,V$ (n0, green). After the stress, ΔV is extracted via a direct bias switch from the stress voltage to the readout voltage (JED1, blue) or via accumulation pulse preconditioning similar to n0 (n1, green).

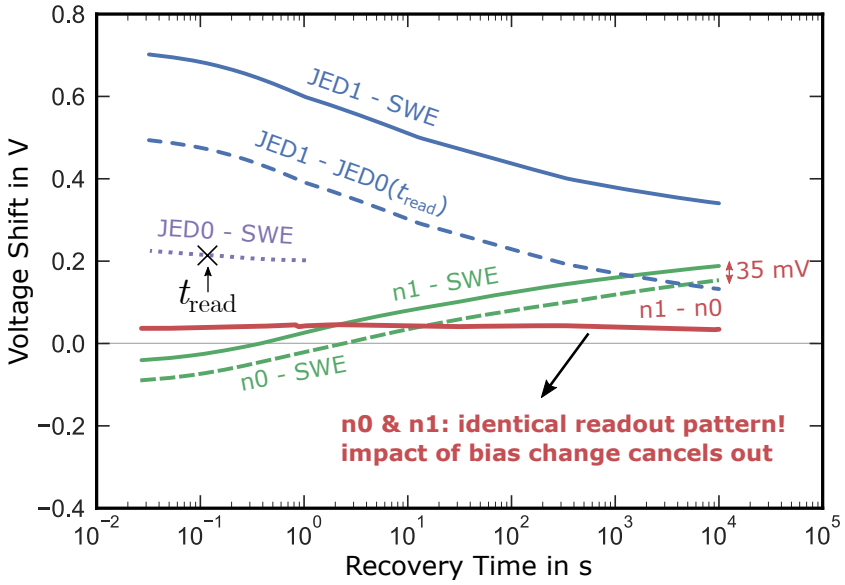


Fig. 3.16 Resulting ΔV as a function of the chosen extraction pattern according to Fig. 3.15. ΔV strongly depends on the recovery time and stress independent switching conditions in measurements without preconditioning (blue). On the other hand, using preconditioned measurements results in less recovery time dependence and a more exact ΔV extraction due to identical and therefore comparable switching conditions before each readout (green and red).

Compared to JED1 recovery curves of the voltage shift (blue), the recovery time dependence of ΔV changes drastically if we switch to the accumulation pulse preconditioned readout and, more importantly, always compare ΔV within identical time frames, meaning t_{read} equals t_{rec}. The solid and dashed green curves represent ΔV at the readouts n0 and n1 with respect to SWE. The difference between n0 and SWE (n0-SWE) shows ΔV before the stress, whereas the difference between n1 and SWE (n1-SWE) shows ΔV after the stress. Since both readouts are performed under identical and well defined switching conditions from accumulation to inversion, n0 and n1 show the same trend over time. This indicates that the form of the recovery curve mainly depends on the switching conditions since STR

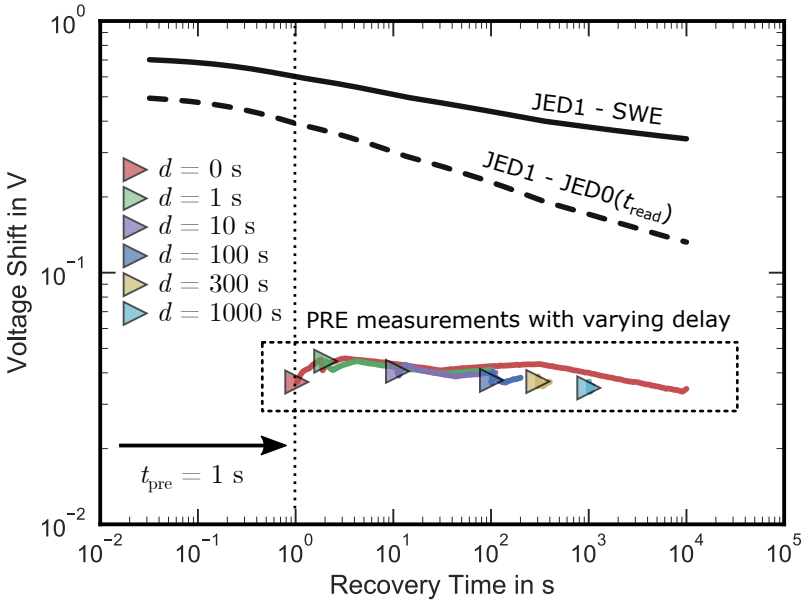


Fig. 3.17 Same as Fig. 3.16 but with delay times ranging from $d = 0\,\mathrm{s}$ (red) to $d = 1000\,\mathrm{s}$ (cyan) at 0 V. ΔV extracted via preconditioned measurements shows only a minor dependence on the delay time. Preconditioning was performed for $t^{\mathrm{n}}_{\mathrm{pre}} = 1\,\mathrm{s}$ (black arrow).

does not result in any noticeable change in the time dependence of the ΔV recovery. The difference between both curves represents the real BTI due to the stress pulse, since any impacts from stress independent switching conditions cancel out. The resulting ΔV is indicated in red and is nearly stable at 35 mV within the measured recovery time of 10 ks, giving a good estimation for the permanent component $P(t_{\mathrm{str}})$. The comparison with the JEDEC-like measurement (given by the difference between JED1 and JED0), which shows a ΔV of $\approx 500\,\mathrm{mV}$ recovering to 140 mV within the same recovery time, proves the importance of comparing pairs of values (ΔV, $t_{\mathrm{rec}} = t_{\mathrm{read}}$) rather than ΔV prior and after the stress for reliable voltage shift measurements. In particular for industrial measurements, it is usually sufficient to extract only one pair of values instead of the complete recovery transient as long as $t_{\mathrm{rec}} = t_{\mathrm{read}}$.

In addition to the accurate determination of ΔV, preconditioned measurements are more robust to delay time variations. Fig. 3.17 shows the data from Fig. 3.16 on a logarithmic y-axis with additional data for delay times between STR and n1 ranging from $d = 0\,\mathrm{s}$ (red) to $d = 1000\,\mathrm{s}$ (cyan). During the delay time, the gate voltage is fixed to 0 V. ΔV depends only slightly on the delay time and stays within 35 mV and 45 mV. A more comprehensive picture on the delay time dependence is given in the next section.

3.3.5 Minimized impact of delay times

Especially in industrial BTI measurements with a large number of devices stressed simultaneously, delay times between the end of the stress pulse and the readout R_i are inevitable. Delay times lead to a large inaccuracy in the extracted ΔV in JEDEC-like measurement due to ongoing recovery, as shown in Fig. 3.12. Preconditioned BTI measurements, on the other hand, show much less dependence of ΔV on the delay time between the end of the stress pulse and the beginning of the readout pulse R_i, allowing for more reliable extraction of application-relevant voltage shift.

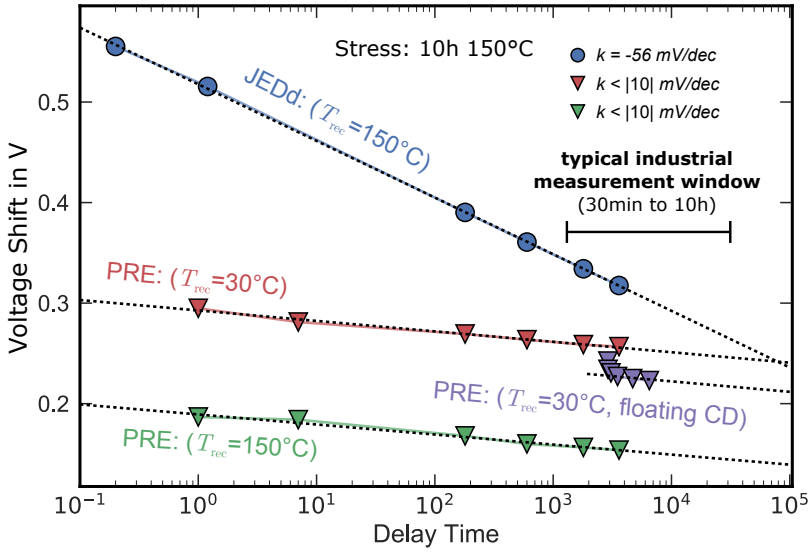


Fig. 3.18 Delay time dependence of ΔV after a 10 h, 5 MV cm^{-1} positive bias stress at 150 °C. Readout was done at either 150 °C or 30 °C. The impact of d on ΔV is reduced by more than a factor of 5 for PRE measurements since fully-recoverable components of ΔV are cleared via the preconditioning pulse.

Fig. 3.18 shows the delay time dependence of ΔV for a 10 h, 5 MV cm^{-1} positive bias stress at 150 °C for delay times up to 1 h, which is in the range of typical industrial delay times. The delayed JEDEC-like measurement JEDd (see Fig. 3.11) is shown in blue circles, whereas the preconditioned measurements (according to Fig. 3.14) are shown with triangles labeled PRE. Readout was done at 150 °C (green and blue) or 30 °C with cooldown under $V_{\mathrm{G}}^{\mathrm{str}}$ (red) or floating (purple). JEDd exhibits a strong dependence of ΔV on d and recovers from 560 mV for $d = 0.2$ s to 320 mV for $d = 1$ h, representing a recovery slope of −56 mV/dec at a recovery temperature of 150 °C. The preconditioned measurement at the same recovery temperature is shown in green triangles and represents ΔV after identical stressing conditions. Since recoverable components, which are irrelevant for application, are eliminated, ΔV shows a 5 times smaller dependence on the delay time and ranges from 190 mV for $d = 1$ s to 155 mV for $d = 1$ h with slopes smaller than 10 mV/dec. The red curve represents PRE with readout performed at 30 °C and cooling down under $V_{\mathrm{G}}^{\mathrm{str}}$ resulting in higher shift and less recovery but identical dependence on the delay time. The purple data represents ΔV after cooling down performed under floating conditions, which results in data points shifted to longer delay times since the time needed to reach 30 °C adds to the delay time.

3.3.6 The impact of the preconditioning time

The impact of the preconditioning time $t_{\mathrm{pre}}^{\mathrm{n}}$ was investigated using the measurement pattern sketched in Fig. 3.19. Here, we compare ΔV after a 100 s positive bias stress and 5 MV cm^{-1} for a measurement without preconditioning (top), and measurements with varying preconditioning times $t_{\mathrm{pre}}^{\mathrm{n}}$ (bottom). For the measurement without preconditioning the recovery of the voltage shift was recorded up to 100 s, allowing for a comparison to measurements with preconditioning times up to $t_{\mathrm{pre}}^{\mathrm{n}} = 100$ s. After the preconditioning pulse, ΔV was recorded for 10 s. For all measurements in this section, the delay time was

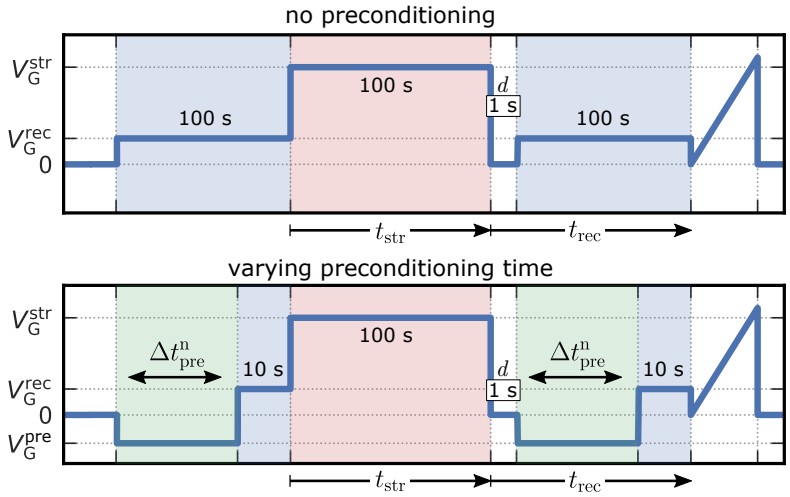


Fig. 3.19 Schematics for the measurement of the impact of the negative preconditioning time $t_{\mathrm{pre}}^{\mathrm{n}}$ on the resulting voltage shift. The measurement pattern without preconditioning is given in the top, whereas the pattern with varying preconditioning time is indicated at the bottom. The delay time for both measurement patterns was set to 1 s.

set to $d = 1\,\mathrm{s}$ at $V_{\mathrm{G}} = 0\,\mathrm{V}$. Preconditioning was performed via an accumulation pulse at $V_{\mathrm{G}} = -15\,\mathrm{V}$ for preconditioning times ranging from 0.1 s to 100 s. Temperature was fixed to 175 °C during the entire process.

Fig. 3.20 shows the impact of $t_{\mathrm{pre}}^{\mathrm{n}}$ on the voltage shift. Here, the solid line represents ΔV without a negative preconditioning pulse. Within two orders of magnitude in recovery time, ΔV decreases from approximately 380 mV (at $t_{\mathrm{rec}} = 1\,\mathrm{s}$) to 250 mV (at $t_{\mathrm{rec}} = 100\,\mathrm{s}$). For the preconditioned measurement on the other hand, even a short $t_{\mathrm{pre}}^{\mathrm{n}}$ decreases the ΔV recovery time compared to the non-preconditioned measurement by several orders of magnitude. For example, the 0.1 s preconditioning pulse (circles, blue) is already sufficient to decrease ΔV to 150 mV (at $t_{\mathrm{rec}} = 1\,\mathrm{s}$), which is 60 % lower than the voltage shift in the measurement without preconditioning after 100 s. Furthermore, ΔV remains nearly constant during the recovery phase, as already discussed in the previous section (c.f. Fig. 3.16, red).

Fig. 3.21 shows the mean value of ΔV extracted from the data in Fig. 3.20 within the first 10 s after the end of the preconditioning pulse for $t_{\mathrm{pre}}^{\mathrm{n}}$ ranging from 0.1 s to 100 s. As for the stress and recovery time, ΔV decreases with the logarithm of the preconditioning time $t_{\mathrm{pre}}^{\mathrm{n}}$. Increasing $t_{\mathrm{pre}}^{\mathrm{n}}$ by one order of magnitude results in 10.6 mV less voltage shift. This proves that the 1 s preconditioning pulse used in this chapter is already a sufficient preconditioning time to decrease the recovery time by several orders of magnitude.

3.3.7 Interface degradation caused by preconditioning

To confirm the correctness of preconditioned measurements, it is necessary to ensure the interface is not damaged by the additional preconditioning pulse itself. Therefore, charge pumping measurements where performed for both extraction patterns as shown in Fig. 3.22. The charge pumping current I_{CP} was extracted at a frequency of 50 kHz before the first readout (virgin) and after the last readout (stressed) for JEDd and PRE using constant base level CP measurements with a low level of the gate pulse of $V_{\mathrm{G}}^{\mathrm{L}} = -25\,\mathrm{V}$ and a high level of $V_{\mathrm{G}}^{\mathrm{H}} = 10\,\mathrm{V}$. The stress field was set to $5\,\mathrm{MV\,cm^{-1}}$ for $t_{\mathrm{str}} = 100\,\mathrm{s}$.

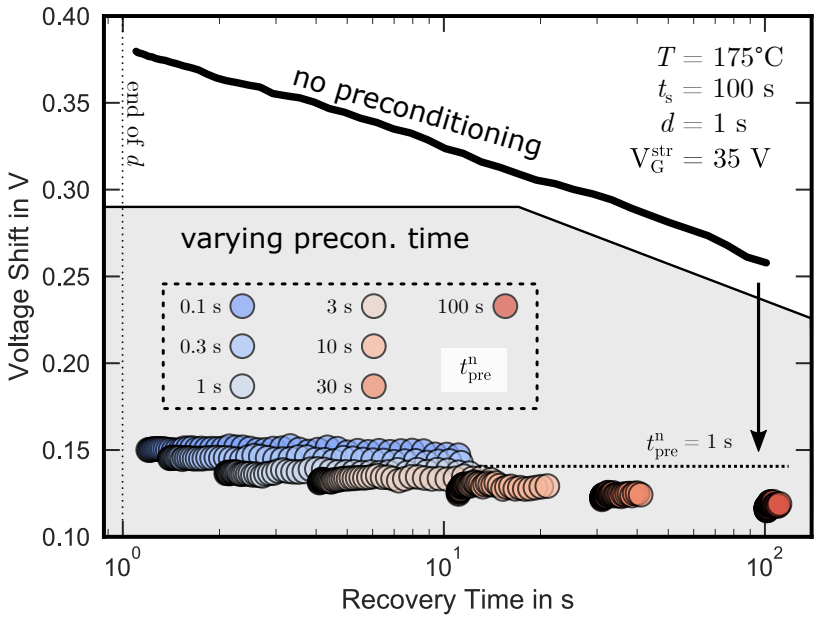


Fig. 3.20 Impact of the preconditioning time $t_{\mathrm{pre}}^{\mathrm{n}}$ varying from 0.1 s (circles, blue) to 100 s (circles, red) on ΔV at 175 °C. The preconditioning was always performed in accumulation at $V_{\mathrm{G}} = -15\,\mathrm{V}$. The solid black line represents the ΔV recovery curve for a measurement without preconditioning. As for the stress and recovery time, ΔV scales with the logarithm of $t_{\mathrm{pre}}^{\mathrm{n}}$. Therefore, even a short $t_{\mathrm{pre}}^{\mathrm{n}}$ decreases the recovery time by several orders of magnitude. Delay time for all measurements was 1 s.

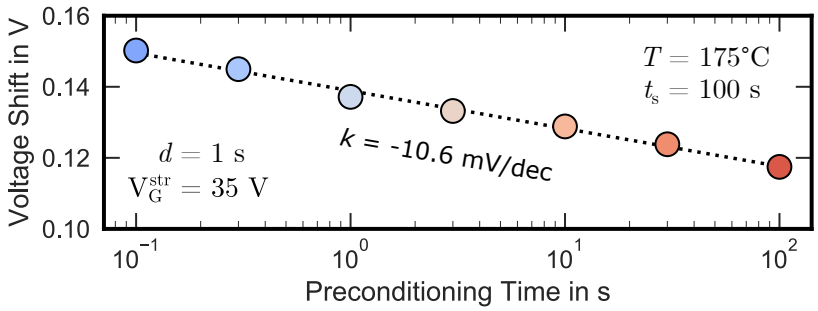


Fig. 3.21 Mean value of ΔV as a function of $t_{\mathrm{pre}}^{\mathrm{n}}$ extracted from the data in Fig. 3.20 for $t_{\mathrm{pre}}^{\mathrm{n}}$ ranging from 0.1 s (blue) to 100 s (red). Increasing $t_{\mathrm{pre}}^{\mathrm{n}}$ by one order of magnitude reduces ΔV by approximately 10.6 mV.

The outcome is shown in Fig. 3.23. As can be seen, both extraction patterns show similar charge pumping signals (left). The additional 1 s accumulation pulse used in PRE does not lead to any additional degradation compared to JEDd. For both readout patterns, I_{CP} increases by approximately 1 % after the 100 s stress at 175 °C.

3.3.8 Hysteresis monitoring

4H-SiC MOSFETs show a hysteresis (SH) between gate voltage up-sweeps from accumulation to inversion and the down-sweeps from inversion to accumulation, which is especially

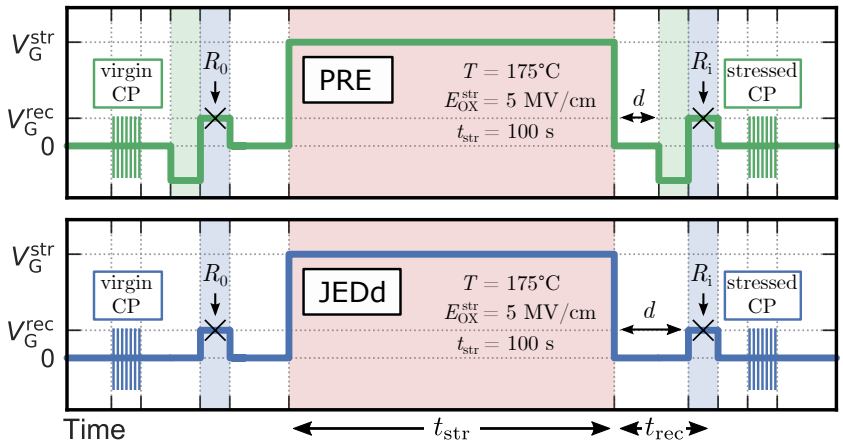


Fig. 3.22 Measurement pattern to investigate if any interface degradation due to the accumulation preconditioning occurs. For both readout patterns, a constant high-level CP measurement was performed before (virgin) and after (stressed) the complete test procedure.

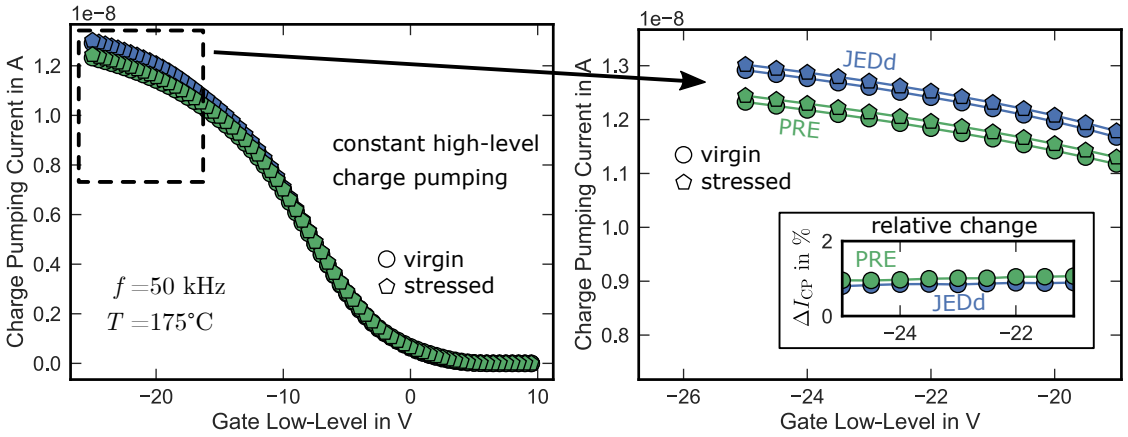
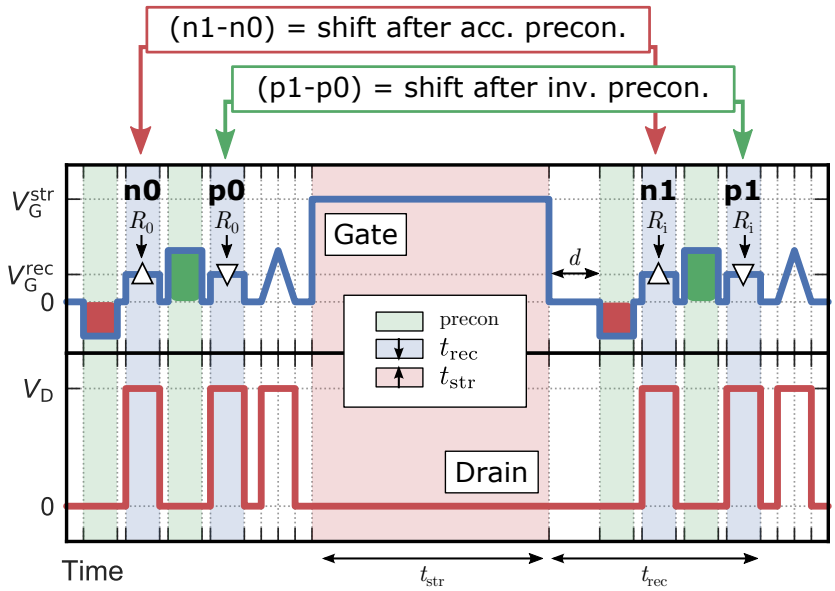


Fig. 3.23 Constant high-level charge pumping measurements for JEDd and PRE. The CP measurement was performed according to Fig. 3.22. I_{CP} increases by approximately 1 % for JEDd and PRE. The additional accumulation pulse for $t_{pre}^{n} = 1$ s does not lead to an additional interface degradation.

visible in the sub-threshold regime. The majority of the hysteresis is caused by charging and discharging of interface states, which is fully recoverable during normal device operation [29, 43, 112]. However, the impact of BTI on the density of interface states D_{it} causing the hysteresis has not been investigated until now. To enable the monitoring of changes in the hysteresis during high temperature gate stress, the accumulation pulse readout n0 is extended via a second inversion preconditioning pulse p0 at use-voltage, resulting in the measurement pattern shown in Fig. 3.24. By using negative and positive preconditioning pulses, AC-use conditions are mimicked. The hysteresis before stress is given by the voltage shift after the positive p0 and negative n0 preconditioning, wheres the hysteresis after the stress is given by the difference between p1 and n1. The change in hysteresis due to BTI is therefore given by $\Delta SH = (p1-n1) - (p0-n0)$. Fig. 3.25 shows a comparison of the JEDEC JESD 241 (circles) and the preconditioned BTI after a 1 s accumulation



monitoring drift in sweep hysteresis (SH):

$$\Delta\mathrm{SH} = \mathrm{SH}(t_{str}) - \mathrm{SH}(t_0) = \text{(p1-n1) - (p0-n0)}$$

Fig. 3.24 Preconditioned BTI measurement pattern with accumulation and inversion pulse preconditioning allowing for additional hysteresis monitoring.

pulse (negative PRE, triangles up) and after a succeeding 1 s inversion pulse (positive PRE, triangles down) for a 44 h, 5 MV cm^{-1} positive stress at 150 °C.

For JEDEC readouts, ΔV is overestimated for given stress times and depends strongly on t_{read} because stress independent components are not excluded. Preconditioned measurements eliminate a large fraction of these components, resulting in an approximately 2.3 times lower and more application-relevant ΔV. The difference in ΔV for negative and positive PRE results from the hysteresis (red squares), which slightly increases during high temperature, high field positive bias stress. The fit (dashed) was done according to (1.4) assuming $\tau_0 = 10^{-9}$ s [130]. Extracted parameters of the normally distributed E_A (σ, μ) are given in the bottom plot. PRE measurements show significantly reduced standard deviation with $\mu = 1.18(5)$ eV.

3.3.9 Conclusions

The impact of various bias temperature instability measurement parameters on the extracted voltage shift of 4H-SiC power MOSFETs was investigated. An accurate BTI procedure should assess exclusive parameter drifts, which degrade the *application-relevant* device performance. However, using JEDEC-like measurements, the majority of ΔV after high bias stress originates from fully-recoverable and stress independent shift components, which strongly depend on the measurement parameters and incorrectly add to the extracted ΔV. ΔV changes drastically by changing the reference point for the shift calculation and strongly depends on recovery and delay times of the measurement. To overcome this issue, a sophisticated bias temperature instability measurement pattern using device preconditioning is demonstrated, which allows for an exact determination of the application-relevant voltage shift ΔV. By using similar and well defined preconditioning pulses before each readout, fully-reversible shift components are eliminated, thereby allowing for a

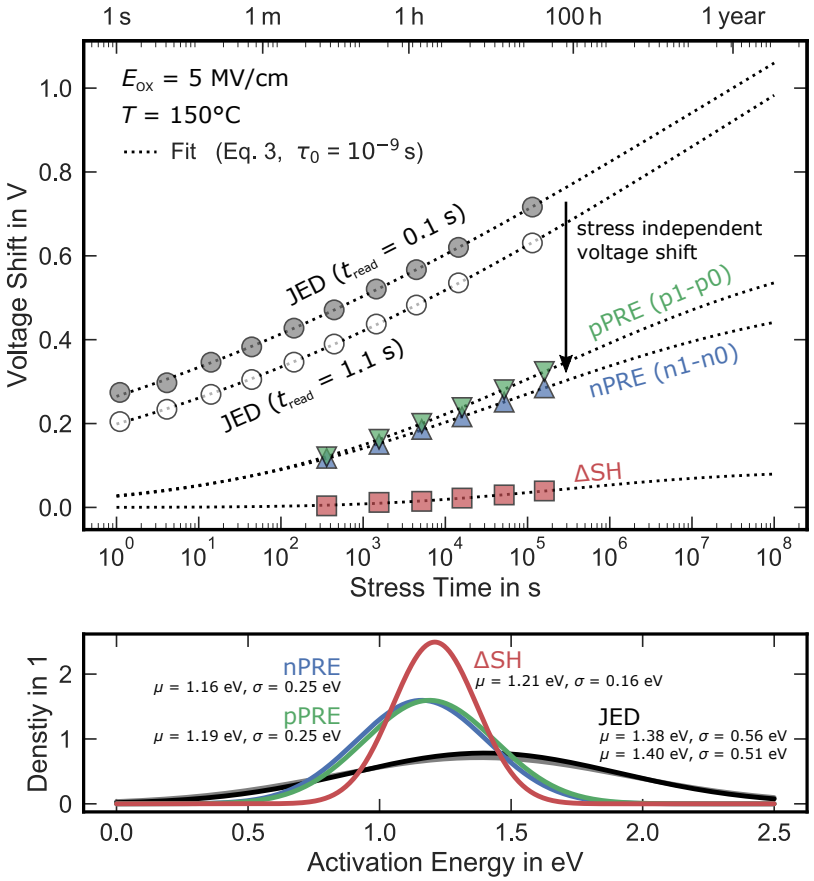


Fig. 3.25 Top: voltage shift for stress times up to approximately 44 h for JEDEC JESD 241 (circles) with two different values for t_{read} and preconditioned BTI according to Fig. 3.24 after negative (nPRE, blue, triangles up) and positive (pPRE, green, triangles down) preconditioning. Although stress conditions are identical, preconditioned measurements show significantly less shift. The difference between pPRE and nPRE represents the change in sweep hysteresis as a function of the stress time (squares, red). Bottom: parameters of the normally distributed E_{A} (σ, μ) are extracted using (1.4) (assuming $\tau_0 = 10^{-9}$ s [130]).

more accurate extraction of the application-relevant permanent component. Voltage shifts extracted via preconditioned BTI are still higher but in the range of silicon based power MOSFETs, less dependent on measurement delay times within industrial timescales, and do not include fully-recoverable hysteresis effects. Therefore, they enable more accurate lifetime prediction of 4H-SiC MOSFETs.

CHAPTER 4

Charge accumulation in high temperature processing steps

Contents

During the processing of SiC MOSFETs, very high temperatures are necessary to manufacture high-quality devices. This is especially the case for the post-oxidation annealing (POA) of the gate oxide, and the metal contact formation, which require temperatures significantly above 1000 °C. The need for such high processing temperatures is an outstanding difference to the manufacturing process of silicon based devices, where usually much lower temperatures are needed. Furthermore, the requirement for such a high thermal budget may be one reason for the overall poorer interface quality of silicon carbide based devices. Although there are several studies which investigate the impact of various processing temperature and time combinations on the electrical behavior of 4H-SiC capacitors [33, 52], no such work is available for the full manufacturing routes of 4H-SiC MOSFETs, which in general require additional high temperature processing steps. The additional thermal budget during MOSFET manufacturing might in the end result in an increased interface state density due to possible defect generation and/or depassivation of previously passivated states at the SiC/SiO_2 interface.

4.1 Devices and high temperature processing steps

To investigate the impact of each high-T processing step on the charge state at the SiC-SiO_2 interface, multiple wafers containing various test structures from an identical processing route were investigated. All wafers were simultaneously subjected to the processing steps

with a high thermal budget. After each of these high-T processing steps, one wafer was removed from the production line and the capacitance voltage CV curves were extracted using the measurement system described in Section 1.3.1. Since it is not feasible to measure a capacitance voltage curve on the MOSFET test structures without a fully-processed source contact, which is usually manufactured in one of the last processing steps, nMOSCAPs test structures with an area A of 2.89 mm^2 and an oxide thickness t_{OX} of approximately 120 nm were investigated. These MOSCAPs are located on the same wafers as the MOSFETs. Therefore all devices are subjected to an identical thermal budget throughout the entire manufacturing process.

An overview on the investigated high-T processing steps is provided in Tab. 4.1 and labeled according to the following scheme:

- process P_1: post oxidation anneal of the gate oxide (POA),
- process P_2: deposition of the polycrystalline silicon gate (Poly),
- process P_3: deposition of the inter-level dielectric (ILD),
- process P_4: annealing of the inter-level dielectric (Anneal),
- process P_{51} to P_{54}: contact formation at various temperatures.

The complete process chain including all high-T steps and the CV measurement is sketched in Fig. 4.1. It is essential to note that the processes P_{51} to P_{54} were done in parallel, whereas P_1 to P_4 are performed in series. Therefore, a sample measured after P_{52} was subjected to P_1 to P_4 and P_{52} but not to P_{51}, as indicated in Fig. 4.1.

Table 4.1: Approximated process temperatures T and times t_{hT} for all investigated manufacturing steps with a high thermal budget.

	P_1	P_2	P_3	P_4	P_{5j}
Process	POA	Poly	ILD	Anneal	Contact variations
T	$> 1000\,^{\circ}\mathrm{C}$	$\approx 500\,^{\circ}\mathrm{C}$	$\approx 500\,^{\circ}\mathrm{C}$	$\approx 800\,^{\circ}\mathrm{C}$	$800\,^{\circ}\mathrm{C}$ to $1100\,^{\circ}\mathrm{C}$
t_{hT}	> 100 min	< 100 min	< 100 min	< 100 min	< 10 min

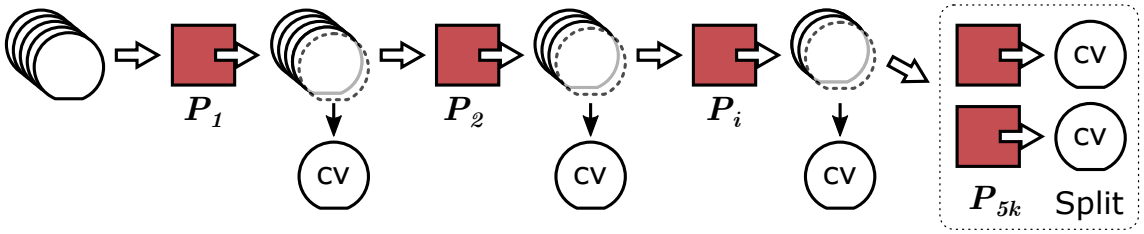


Fig. 4.1 Schematic illustration of the process chain including the extraction of the CV curve after each processing step with a high thermal budget. Note that the processes P_{51} to P_{54} were done in parallel, whereas P_1 to P_4 were performed in series.

It should be pointed out that the post oxidation anneal (POA), which is the first investigated high temperature step (P_1), is the first processing step after oxide deposition. At this point, only a SiO_2 film is present on top of the n-epi layer and no metalization is available for the CV measurement to make contact to the sample. Due to this, the CV measurement after P_1 was performed using a *mercury probe*, which applies mercury contacts

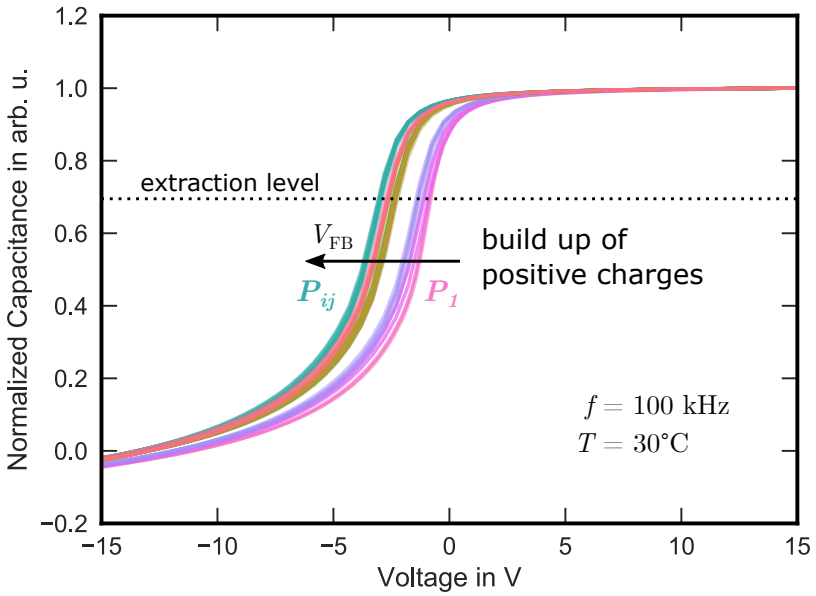


Fig. 4.2 Normalized CV curves extracted from n-MOSCAP test structures at 30 °C and a frequency of 100 kHz after each high-T processing step. For each high-T step from P_1 to P_{54}, the flatband voltage shifts up to $\Delta V_{FB} \approx -2.35$ V to more negative voltages. The extraction level of V_{FB} is indicated as dotted line.

with a well-defined area to the sample using a hollow needle. To allow a comparison of the outcome of this measurement with all subsequent ones, which were performed on the polycrystalline Si (poly-Si) contact, the first CV-measurement is corrected for the area of the mercury droplet, and the difference in the work-function between the polycrystalline silicon and the mercury. This correction results in an offset in the gate potential of approximately 0.4 V.

4.2 Evolution of fixed oxide charges

Fig. 4.2 shows the normalized CV curves after each high temperature processing step given in Tab. 4.1 for 5 n-MOSCAPs from each sample group (wafer). All CV measurement were performed at 30 °C and a frequency of 100 kHz from depletion at −15 V to accumulation at 15 V (up-sweep) and vice versa (down-sweep). With increasing thermal budget, the CV curves shift to more negative voltages. The voltage shift is parallel, which indicates a build-up of fixed positive charges at the SiC/SiO_2 interface. It is important to note that the observed voltage shift is in fact due to the high thermal budget and not caused by the direction of the CV measurement, due to the negligible difference for both sweep directions (not shown).

The flatband voltage V_{FB} extracted from the up- and down- sweep in the data at an extraction level of $0.7 \times C_{max}$ (dotted line) is depicted in Fig. 4.3. Although P_1 is one of the steps with the highest thermal budget ($T > 1000$ °C for $t_{hT} > 100$ min), the CV curve remains close to the theoretical one (as will be shown in Section 4.2.1). The first shift of the CV curve occurs after P_2, which is the deposition of the polysilicon gate. At this point, V_{FB} has already shifted by 300 mV. The voltage shift increases with each additional high-T processing step to a maximum ΔV of approximately 2.35 V after P_{54}. Furthermore,

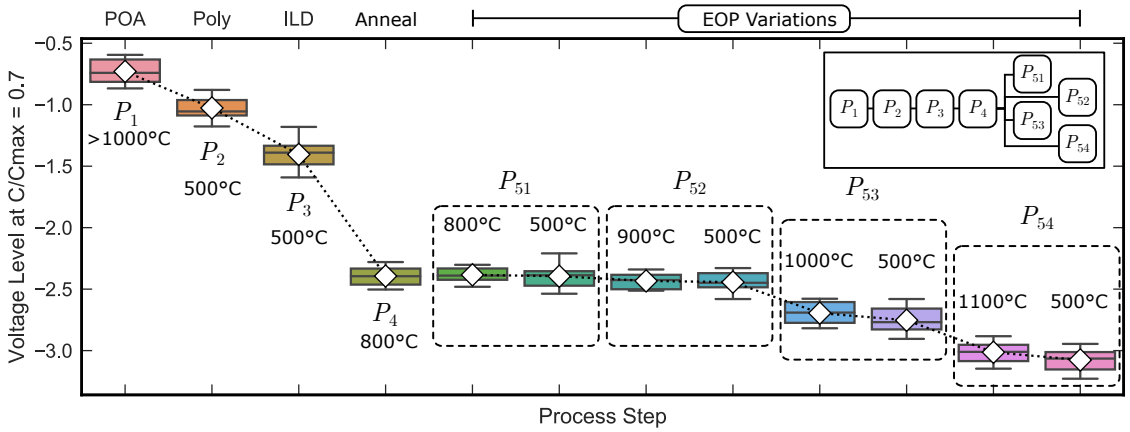


Fig. 4.3 Flatband voltage after all high-temperature processing steps. ΔV_{FB} was extracted at the dashed line in Fig. 4.2. ΔV_{FB} arises after the deposition of the poly-Si gate contact and increases with each additional processing step with a high thermal budget.

it is important to note that the impact of the gate bias on ΔV is negligible ($< 200\,\mathrm{mV}$) compared to the overall voltage shift, which arises due to the thermal budget.

4.2.1 Simulated CV curves

Fig. 4.4 shows a comparison of the measured CV curves after P_1 (blue) and P_{54} (green), which did show the highest shift, with a simulated CV signal (dashed) of the poly-Si/SiO_2/SiC MOS-System. After P_1, the CV curve is very similar to the ideal curve of the system with a total number of oxide traps N_{ot} of approximately $1 \times 10^9\,\mathrm{cm}^{-2}$ (blue). After the last processing step, P_{54}, V_{FB} is shifted to more negative gate voltages due to an increase in trapped positive charges. For the fit, a N_{ot} of approximately $4.5 \times 10^{11}\,\mathrm{cm}^{-2}$ (green) results in a good agreement with the experimental data. Fig. 4.5 shows the values extracted from the fitting parameters for the complete set of high-T processing steps.

4.3 Analysis of minority carrier traps using photo-assisted CV

In a wide band gap semiconductor like SiC, the impact of minority carriers is not visible in the CV curve due to the extremely small intrinsic carrier density. Therefore, the interface charge density D_{it} was extracted using photo-assisted capacitance voltage measurements as described in Section 1.3.5.

Fig. 4.6 shows a photo-assisted CV measurement after processing step P_4. Starting in accumulation at 15 V, the gate voltage is swept to deep-depletion in the dark (cyan). While the bias is held in deep-depletion, the sample is illuminated with 350 nm light to populate the inversion layer, which results in an increase of the capacitance. Minority carriers are generated and move to the interface, where they are trapped in available interface states. Afterwards, the light is turned off and the gate voltage is swept back to accumulation in the dark, which results in the red curve. As can be seen, a voltage shift occurs in the CV curve due to the trapped minority carriers. The dashed lines represent the simulated CV-curves of the MOS system [131]. For the simulation of the illuminated curve (red), N_{ot} remains at the value of the dark-curve and the interface trap density is increased until the

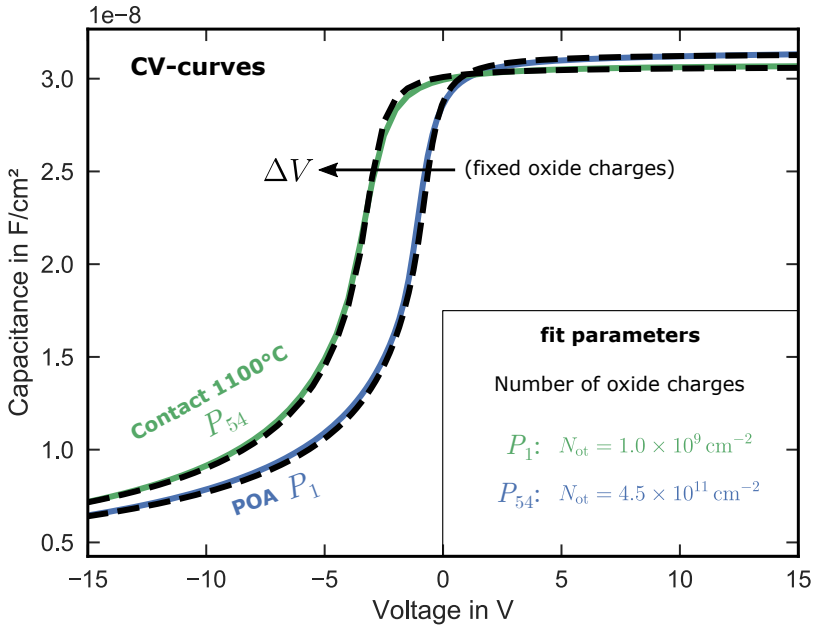


Fig. 4.4 Measured CV-curves after the first (POA, P_1) and the last (Contact 1100 °C, P_{54}) high-T processing step. The CV curve of P_{54} is shifted to more negative gate voltages due to the high thermal budget, which led to a build-up of positive oxide charges. Both curves have been simulated using a total number of oxide charges of $1.0 \times 10^9\,cm^{-2}$ for P_1 and $4.5 \times 10^{11}\,cm^{-2}$ for P_{54}. D_{it} was set to $1.0 \times 10^9\,cm^{-2}\,eV^{-1}$ for both curves.

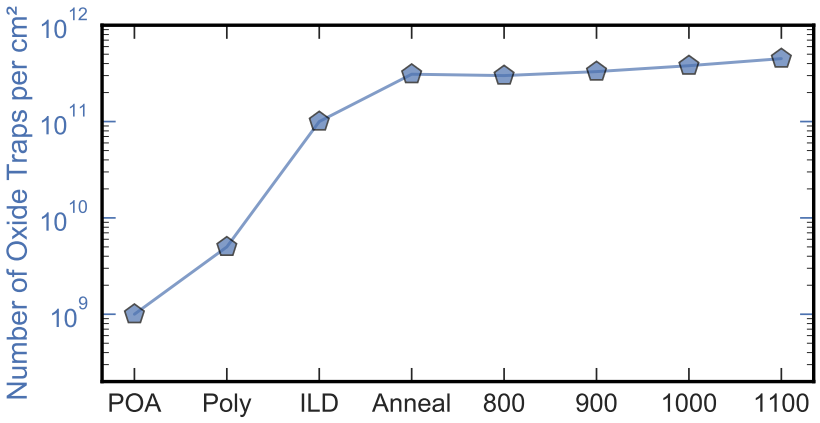


Fig. 4.5 Number of positive oxide charges N_{ot} after each high temperature processing step. After the poly-Si deposition P_2, N_{ot} increases strongly from $1.0 \times 10^9\,cm^{-2}$ up to $4.5 \times 10^{11}\,cm^{-2}$ after P_{45} assuming all charges at the SiC/SiO_2 interface. The high N_{ot} corresponds to a maximum flatband voltage shift of approximately 2.3 V.

simulated and the measured CV curves match. The photo-assisted CV measurements for all high temperature processing steps are shown in Fig. 4.7. For P_1, the photo-assisted data is missing because such a measurement was not possible in combination with the mercury probe. The number of oxide traps N_{ot} and the density of interface states D_{it} extracted from all measurements is given in Fig. 4.8.

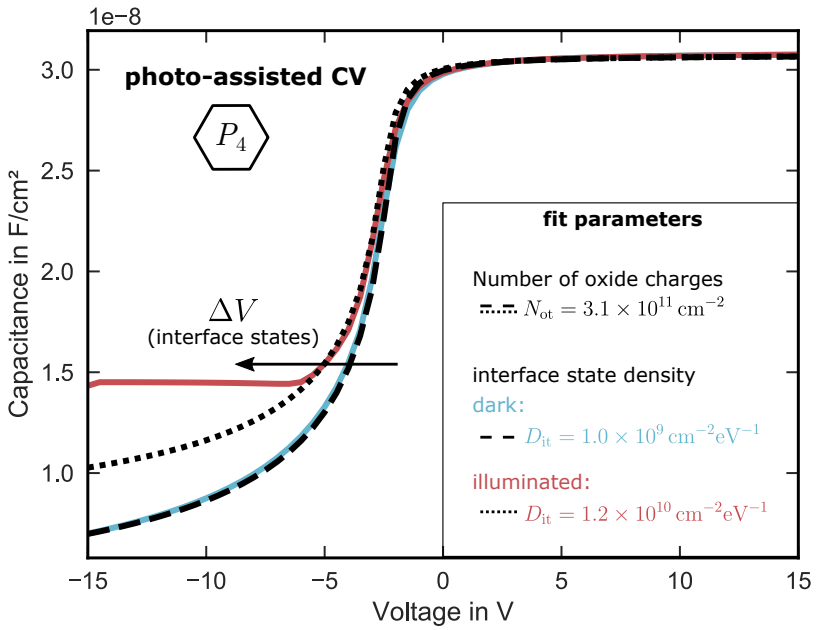


Fig. 4.6 Photo-assisted CV-measurement after high-T processing step P_4. The curve after the sample was illuminated is shown in red. The number of oxide traps remains identical at $3.1 \times 10^{11}\,\mathrm{cm}^{-2}$ for both fits (black). Due to the generation of minority carriers in the photo-assisted measurement, the impact of the D_{it} on the capacitance is visible. The dotted black line shows a simulation of the illuminated curve using an interface state density of $1.2 \times 10^{10}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$.

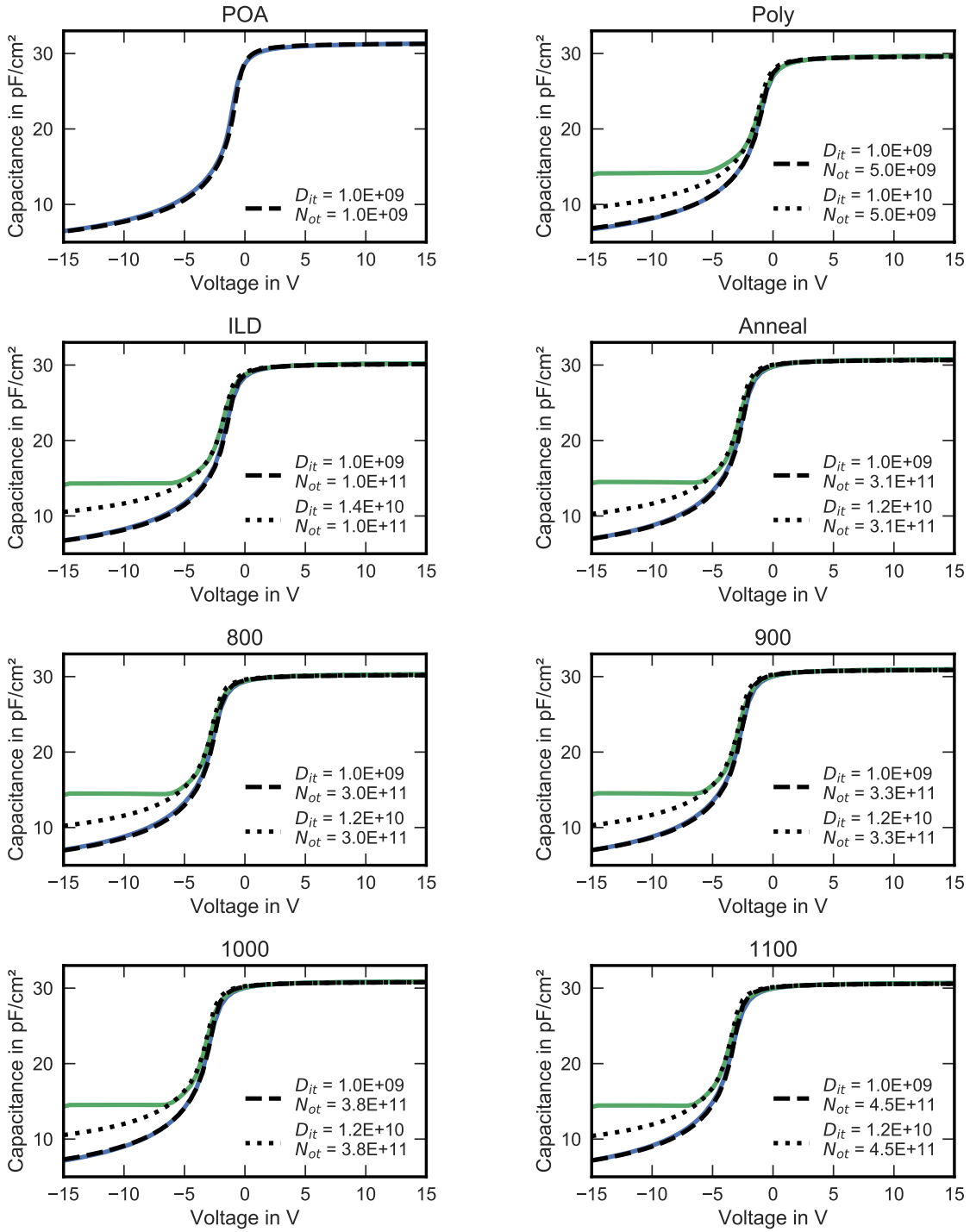


Fig. 4.7 Photo-assisted CV measurement with fitting parameters for processing steps P_2 to P_{54}. For P_1 no photo-assisted CV measurement was possible (mercury probe).

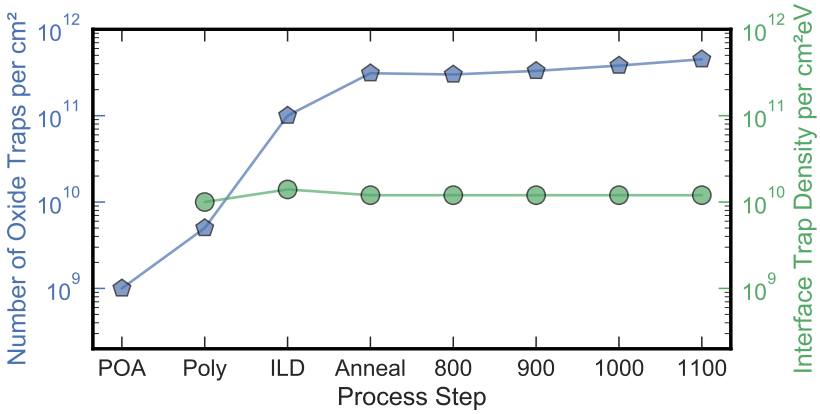


Fig. 4.8 Impact of high-temperature processing steps on the total number of positive oxide charges N_{ot} (left-axis, blue) and the interface trap density D_{it} (right-axis, green). Unlike the N_{ot}, which increases from $N_{\mathrm{ot}}(P_1) = 1 \times 10^9\,\mathrm{cm}^{-2}$ to $N_{\mathrm{ot}}(P_{54}) = 4.5 \times 10^{11}\,\mathrm{cm}^{-2}$, the interface trap density does not change with increasing thermal budget and remains constant at approximately $D_{\mathrm{it}} = 1.2 \times 10^{10}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$ throughout processing.

4.4 Interpretation of the results

Although a change of the interface charging state after high temperature processing steps was expected before the study, the build up of such high amounts of positive fixed charges at the SiC/SiO_2 interface is a surprising outcome. Since the CV-curve after the initial high-T step P_1 is nearly identical to the ideal one, although the thermal budget of P_1 is one of the highest, the deposition of the polycrystalline gate contact P_2 seems of fundamental importance for the involved mechanism.

4.4.1 Charge accumulation via impurity diffusion

A first possibility is that P_2 (poly-deposition) might add impurities, like mobile ions with low diffusion constants at room temperature, to the system. However, these mobile ions could have been present in the system already before P_2. In this case, a voltage shift arises after P_2 due to the deposited gate contact, which introduces an electric field along the oxide layer due to the alignment of the Fermi levels. The mechanism is explained schematically in Fig. 4.9. After P_1, the system is in thermal equilibrium and no electric field is present along the SiO_2 (left). Subsequently to P_2, an oxide field E_{OX} arises due to the Fermi-level alignment. Therefore, positive mobile ions are able to diffuse along the direction of E_{OX} to the SiC/SiO_2 interface due to the very high processing temperatures. In the end, this leads to an accumulation of fixed positive charges at the SiC/SiO_2 interface. It is furthermore important to note that, likely due to diffusion quenching at low temperatures, it was not possible to move these trapped charges away from the interface (recover the CV curve to its ideal position) via a gate stress bias, even at elevated measurement temperatures of up to 200 °C.

4.4.2 Hydrogen related charge accumulation

In addition to the previously discussed mobile ion mechanism, another possible explanation can be given using a hydrogen-based mechanism like the hydrogen-release model, which was

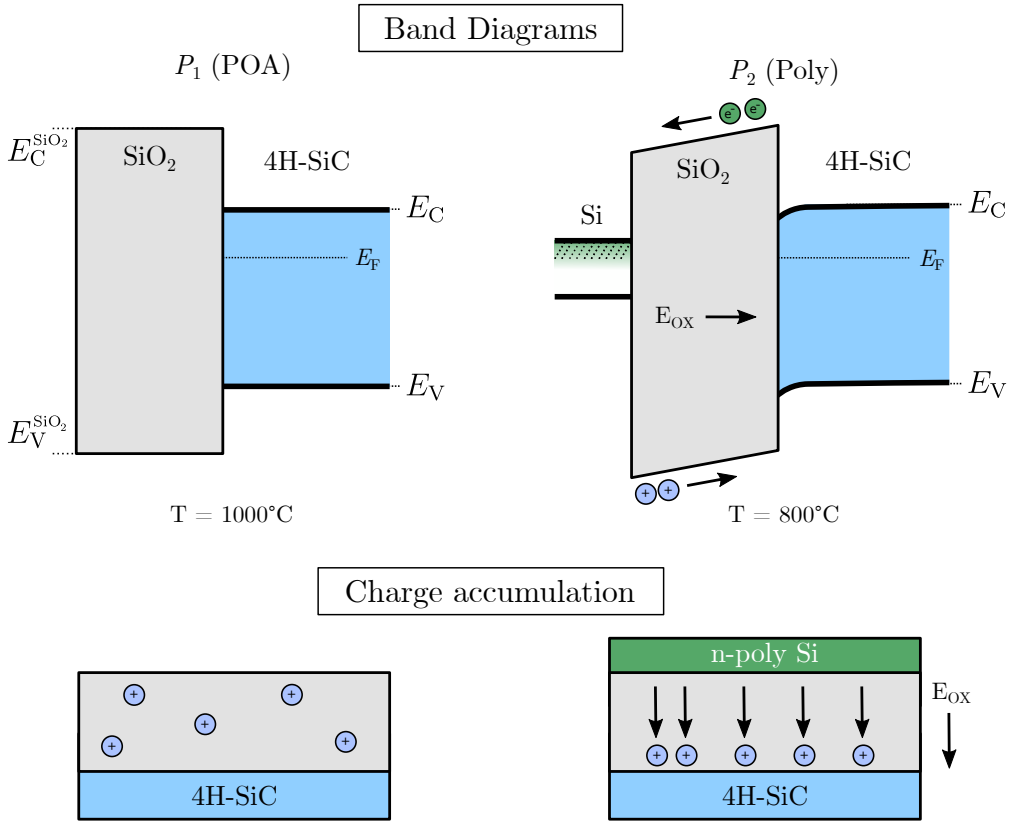
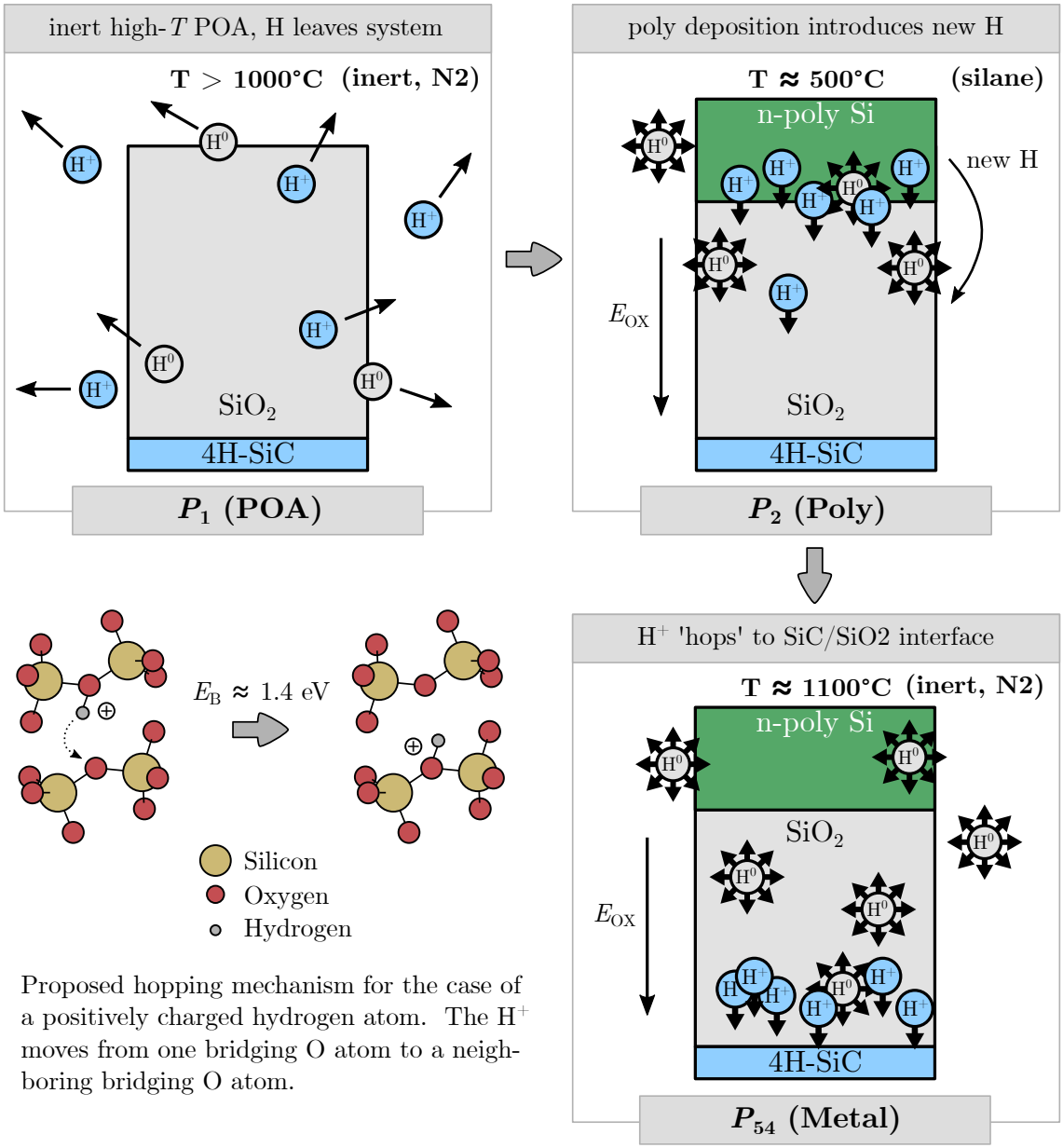


Fig. 4.9 Top: schematic band alignment during a high-temperature processing step. After P_1, the system consists of the semiconductor with the oxide layer on top. Therefore, no electric field E_{OX} is present in the SiO_2 layer (left). In all following processing steps P_2+, the silicon gate contact introduces an electric field in the oxide layer due to the Fermi level alignment (right). In combination with the high temperatures of several hundred Celsius, positive charges are now able to diffuse to the SiC/SiO_2 interface through the oxide layer, which leads to a build-up of positive charges at the interface. Bottom: schematic cross section indicating the accumulation of positive charges at the SiC/SiO_2 interface.

described in Section 1.2.2. A simplified picture of the mechanism, which might lead to the observed charge accumulation, is shown in Fig. 4.10. During P_1, the Tetraethylorthosilicat (TEOS) based SiO_2 film, which was deposited via chemical vapor deposition (CVD), is annealed in an inert dinitrogen (N_2) atmosphere at a temperature above 1000 °C for the time $t_{hT} > 100$ min. Due to the highly elevated temperature and the inert atmosphere, which results in a low H partial pressure in the chamber, trapped and residual hydrogen is likely to be released from the amorphous SiO_2 (Fig. 4.10, top, left). Therefore, no significant deviation of the CV curve from the ideal one should be observed after P_1, which is indeed the case as was shown above using the simulated CV curves. After P_1 (POA), N_{ot} remains at approximately $1 \times 10^9\,cm^{-2}$, which results in a V_{FB} close to the ideal flatband voltage (compare with Fig. 4.8, POA).

The amount of available hydrogen in the system changes drastically after the deposition of the polycrystalline silicon gate in the process step P_2 (Fig. 4.10, top right). Here, the poly-Si gate is grown by chemical decomposition of silane (SiH_4) at a temperature slightly above 500 °C, which releases enormous amounts of hydrogen via pyrolysis. Additionally, also the SiO_2 film is flooded again with neutral H^0 and positively charged protons H^+.



Proposed hopping mechanism for the case of a positively charged hydrogen atom. The H^+ moves from one bridging O atom to a neighboring bridging O atom.

Fig. 4.10 Proposed mechanism of positive charge accumulation at the SiO_2/SiC interface using a hydrogen based model. Top, left: during the post oxidation anneal (P_1), H is removed from the SiO_2/SiC stack due to the high thermal budget and the inert gas composition in the chamber. Top, right: The deposition of the polycrystalline silicon gate introduces high amounts of H into the system. Furthermore, the positively charged hydrogen, H^+, is strongly affected by the oxide field, which results from the difference in work-functions of the poly-Si gate and 4H-SiC. Bottom, right: positively charged H is pushed in the direction of E_{OX}, which leads to a build-up of H^+ at the SiC/SiO_2 interface and a significant shift of V_{FB} to more negative voltages. On the other hand, H^0 does not move in a preferred direction due to the neutral charge state. Bottom, left: possible mechanism of hydrogen hopping. H^+ binds to a bringing oxygen atom and is able to hop to a bringing oxygen atom in the vicinity by overcoming an energy barrier of approximately $E_B \approx 1.4\,eV$ [58] resulting in a drift of bound H^+ to the SiC/SiO_2 interface.

Furthermore, the alignment of the Fermi levels results in an electric field E_{OX} along the oxide layer between the poly-Si metal gate and the semiconductor, which points in the direction of the SiC/SiO_2 interface, as already discussed in the previous section. Due to its neutral charge, H^0 will not be affected by E_{OX}, which results in a random movement of H^0 through the material (indicated via the arrows). On the other hand, the positive charge state, H^+, is strongly affected by E_{OX} resulting in a preferred direction of the hydrogen migration along the electric field, which points in the direction of the SiC/SiO_2 interface. The hydrogen migration process will continue in each additional high temperature manufacturing step, which in the end results in a high amount of positive charges trapped at the SiC/SiO_2 interface (Fig. 4.10, bottom right). In addition to the drift of the positive hydrogen, the neutral hydrogen H^0 may occupy a trapping site close to the channel and capture a hole, thereby creating additional positive charges [58]. The accumulation of H^+ is visible in the CV curves as a significant shift of V_{FB} to more negative voltages.

As discussed in Section 1.10, interstitial hydrogen, either in the positive or neutral configuration, will easily bind to several precursors in the amorphous SiO_2 with a low energy barrier of $E_{\mathrm{B}} < 0.15\,\mathrm{eV}$ [58]. Therefore, hydrogen diffusion in the dielectric seems to be limited. However, H bonded to a bridging oxygen atom is able to "hop" from one bound state to the next bound state by overcoming a barrier of approximately $E_{\mathrm{B}} \approx 1.4\,\mathrm{eV}$ as depicted in Fig. 4.10 (bottom, left), which likely results in an additional specific temperature dependence of the observed charge accumulation mechanism.

In the next section, it will be shown that the extracted activation energy of the observed charge accumulation mechanism during high temperature processing steps is in the range of proposed energy barriers for hydrogen-related models [48, 58, 132].

Barrier extraction

For the extraction of the energy barrier E_{B}, we assume the diffusivity of hydrogen in the the amorphous SiO_2 is not rate limiting [70], and the underlying mechanism is related to hydrogen release (see Section 1.9), which is of course speculative. It is important to note that the knowledge of the exact atomistic mechanism is not necessary for the energy barrier extraction. Therefore, the hydrogen release mechanism is only exemplary. In reality, there might be numberless candidates, which qualify according to the extracted energy barrier.

For a normally distributed E_{B}, the release of H^0 from the bound state to the interstitial state, should also be distributed in time with a specific time constant τ_{H} for each transition event. Here, τ_{H} obeys the Maxwell–Boltzmann statistics according to

$$\tau_{\mathrm{H}} = \tau_0 \exp\left(\frac{E_{\mathrm{B}}}{k_{\mathrm{B}} T}\right) \tag{4.1}$$

with the Boltzmann constant k_{B}, the temperature T and the pre-exponential factor τ_0.

The energy barrier E_{B} which has to be overcome to enable the accumulation of positive charges at the SiC/SiO_2 interface, was extracted by using a fit of the flatband voltage shift ΔV_{FB} as a function of the time t_{hT}, for which the sample was subjected to a high temperature. For a normally distributed E_{B}, ΔV_{FB} has to obey

$$\Delta V_{\mathrm{FB}}\left(t_{\mathrm{hT}}\right) = \frac{\Delta V_{\mathrm{FB}}^{\mathrm{max}}}{2} \operatorname{erfc}\left(-\frac{k_{\mathrm{B}} T \ln(\frac{t_{\mathrm{hT}}}{\tau_0}) - \mu}{\sqrt{2}\sigma}\right) \tag{4.2}$$

with the error function erfc, which is given in (1.5), the mean value, μ, and the standard deviation σ, of the normally distributed E_{B}, and the maximum flatband voltage shift $\Delta V_{\mathrm{FB}}^{\mathrm{max}}$ as an additional fitting parameter.

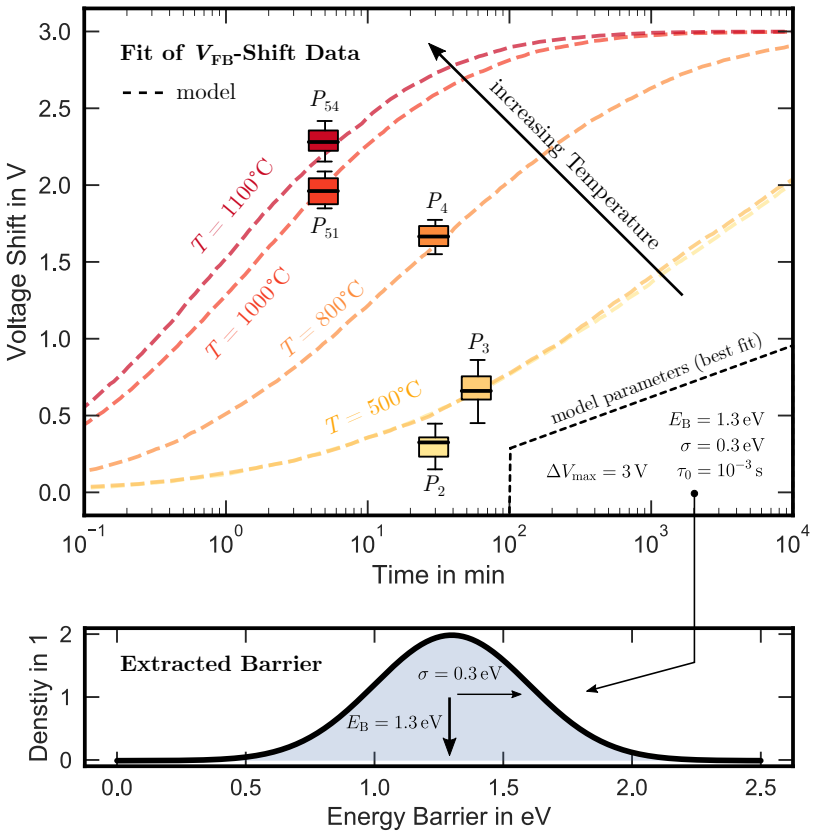


Fig. 4.11 Fit of the flatband voltage shift as a function of the time at a given high temperature processing step. The boxes represent the flat band voltage shift ΔV_{FB} after the processing steps P_2 (Poly), P_3 (ILD), P_4 (Anneal), P_{51} and P_{51} (metal contact). Dashed lines represent a fit according to (4.2), assuming a normally distributed energy barrier E_B. The extracted fitting parameters are given in the inset. The data shows good agreement with an underlying transition mechanism with a mean energy barrier of $E_B = 1.3\,eV$ and a standard deviation of $\sigma_{nd} = 0.3\,eV$. The extracted distribution of the energy barrier is shown in the bottom plot.

Fig. 4.11 shows a fit of the ΔV_{FB} data from Fig. 4.3 for the barrier extraction. The boxes represent the flat band voltage shift ΔV_{FB} after the processing steps P_2 (Poly), P_3 (ILD), P_4 (Anneal), P_{51} and P_{51} (metal contact). The dashed lines represent the fit according to (4.2) for the representative process temperatures ranging from 500 °C for P_2 and P_3 (yellow), to 1100 °C for the metal contact formation P_{54} (red). The fitting parameters are given in the inset. The transition barrier for the mechanism, which results in the observed ΔV_{FB}, is approximately $E_B \approx 1.3\,eV$ (Fig. 4.11, bottom), which is in good agreement with proposed energy barriers for the hydrogen release model [48, 58, 132, 133]. A comparison of energy barriers proposed by DFT simulations for various hydrogen related transition events and E_B extracted in this work from the thermal budget data via the fit in Fig. 4.11 (experimental) is provided in Tab. 4.2.

Table 4.2: Comparison of energy barriers proposed by DFT simulations for various hydrogen related transition events [48, 58, 132, 133] and E_B extracted from the thermal budget data via the fit in Fig. 4.11 (experimental). The extracted energy barrier shows good agreement with hydrogen-related models, which provides a possible explanation for the observed charge accumulation via a build-up of positively charged H at the SiC/SiO_2 interface.

Type	E_B	σ_{nd}
experimental	**1.30**	**0.30**
release of H^0 from bridging O (DFT)	1.50	0.30
hopping of H^0 from bridging O (DFT)	1.55	0.60
hopping of H^+ from bridging O (DFT)	1.40	0.75

4.5 Summary

The impact of various high-temperature processing steps on the charge state of the SiC/SiO_2 interface was investigated using 4H-SiC n-MOSCAPs and CV measurements. By comparing the measured CV curves to an ideal, simulated CV curve, it was shown that during the processing of SiC/SiO_2 based semiconductor structures a significant accumulation of positive charges occurs at the semiconductor-insulator interface. The build-up of positive charges starts after the deposition of the polycrystalline gate contact and continues in all additional processing steps, in which the sample is exposed to a high thermal budget with temperatures above 500 °C. The positive charge accumulation leads to a significant shift of the flatband voltage V_{FB}. The observed flatband voltage shift ΔV_{FB} ranges from $\Delta V_{FB} \approx 0.3\,V$ after the deposition of the poly-Si gate contact at $T \approx 500\,°C$, to approximately $\Delta V_{FB} \approx 2.3\,V$ after the formation of the metal contact at a temperature of approximately $T \approx 1100\,°C$.

The origin of these charges is still unknown. However, two possible candidates have been discussed:

- First, positive impurities (ions) with low diffusion coefficients at room temperature, which are randomly distributed throughout the SiO_2. After subjecting the sample to a high temperature, these ions might be able to diffuse with a preferred direction along the oxide field, which points in the direction of the SiC/SiO_2 interface.
- Second, high amounts of hydrogen are incorporated during the deposition of the polycrystalline gate contact, which can be trapped in various configurations in the amorphous SiO_2. Assuming the diffusivity of hydrogen in the the amorphous SiO_2 is not rate limiting [70], an energy barrier of approximately $E_B \approx 1.3\,eV$ was extracted from the experimental ΔV_{FB} data, which is in good agreement with proposed hydrogen-related trapping mechanisms like the hydrogen release model [48, 58, 132, 133].

To summarize, a significant amount of positive charge accumulates at the SiC/SiO_2 interface during high-T processing steps. The atomic origin of the charge build-up is still unknown but likely linked to hydrogen, which is incorporated during the poly-Si deposition. However, to enable a better understanding, further studies on the observed behavior are mandatory. Here, especially a combination with measurement techniques like secondary ion mass spectrometry (SIMS), which enable the analysis of the exact composition of the specimen, should be advantageous.

CHAPTER 5

Conclusions & Outlook

In the present thesis, the behavior of state-of-the-art 4H-SiC MOSFETs under temperature and voltage stress was assessed with a focus on the impact on the reliability under use-conditions. Numerous devices from multiple manufacturers were characterized using electrical measurements and compared regarding their bias temperature instability. A major achievement in this work was the identification of two independent dominant components which contribute do BTI on 4H-SiC based devices and result in the observed characteristics.

The first component, which is especially visible as a gate voltage hysteresis in the subthreshold regime of the transfer characteristics, originates from hole capture in trap states at the 4H-SiC/SiO_2 interface. Unlike the second component, these states are fully discharged in normal device operation (e.g. AC-use conditions) via an inversion gate pulse above the threshold voltage within nanoseconds. Furthermore, no impact on the long-term device reliability was found even for several million charging/discharging cycles indicating a fully-reversible charging/discharging mechanism which does not cause any permanent damage to the SiC/SiO_2 interface by creating new interface defects. However, the magnitude of the observed voltage shift caused by the first component strongly depends on the crystal plane on which the inversion layer forms. This results in a one order of magnitude higher interface state density for crystal planes which are parallel to the *c*-axis, which was observed on all available SiC-MOSFET by different manufacturers by today. The atomic origin of the defect states, which are responsible for the first component, presumably are carbon dangling bonds on the SiC-side of the SiC/SiO_2 interface.

The second shift component is similar to what is observed on silicon based devices and most likely originates from trap states spatially located at the SiO_2-side of the SiC/SiO_2 interface and energetically located close to the conduction band of 4H-SiC (border states). These states exhibit broadly distributed activation energies for capture and emission. It was demonstrated that all SiC-MOSFETs from different manufacturers available on the market show nearly identical voltage shift behavior even under a low-bias operation close to the threshold voltage. A preconditioned BTI measurement pattern tailored to SiC based devices was demonstrated, which allows for an independent determination of the second component. Furthermore, it was shown that the preconditioned measurement is robust with respect to delay- and readout- timing variations since fully-reversible intrinsics cancel out. Therefore, the preconditioned measurement technique allows for a more accurate lifetime prediction.

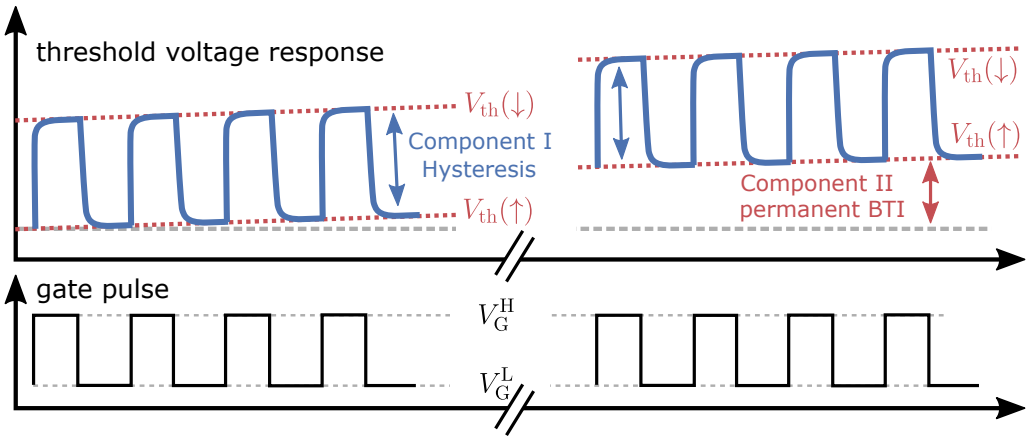


Fig. 5.1 Schematic evolution of the threshold voltage during application (blue). Due to the fully-reversible hysteresis, V_{th} is lower for turn-on $V_{th}(\uparrow)$ and higher for turn-off $V_{th}(\downarrow)$. During long-term operation, border states are increasingly charged leading to a permanent voltage shift (red) [43].

To summarize, both components contribute to the final threshold voltage behavior of the device. A sketch of the evolution of the threshold voltage during application is given in Fig. 5.1 with the gate signal (bottom) and the corresponding threshold voltage (top). Assuming the low level of the gate pulse is in accumulation during V_G^L, interface states (hysteresis, component I) are continuously completely charged and discharge while switching from V_G^L to V_G^H, which results in the fully reversible hysteresis effect (blue), meaning the threshold voltage for turn-on V_{th} ($\uparrow$) will be significantly lower than the threshold voltage for turn-off V_{th} ($\downarrow$). On the other hand, border states are increasingly charged during long-term operation, which in the end leads to device degradation (e.g. a slight increase in the on-resistance), due to the increasing threshold voltage (permanent voltage shift, red).

As a final step, the impact of a high thermal budget on the charging state of the SiC/SiO_2 interface was investigated throughout a series of multiple high temperature manufacturing processes. It was shown that such high temperature processing steps in combination with an electric field result in an accumulation of fixed positive charges at the SiC/SiO_2 interface. The origin of these charges is still unknown. Possibly they originate from ions with low diffusion coefficients at room temperature or are related to hydrogen, which dissociates from precursor states at such high temperatures and is introduced during the deposition of the polycrystalline silicon gate contact. An energy barrier of approximately 1.3 eV was extracted from the experimental data, which is in good agreement with values proposed from theoretical hydrogen related degradation mechanism like the H-release model [48, 58, 132, 133].

Although considerable progress in the understanding of the aforementioned topics could be accomplished in this thesis, several question regarding charge trapping on SiC based devices remain:

- Functioning annealing techniques, which result in an significant decrease of the hysteresis, are still unknown. Although annealing in NO containing atmospheres results in an enormous increase in the electrical device performance, the hysteresis seems to be unaffected. Due to this, different gas compositions like ammonia (NH_3) are intensively investigated and might result in a better passivation of the SiC/SiO_2 interface.

- The origin and microscopic species of the positive charge accumulation during high temperature processing steps remains unknown. Instead of investigating complicated, real devices with complex surface morphology, which furthermore undergo hundreds of processing steps, a simpler approach might be more suited for subsequent research. Here a basic $Si/SiO_2/SiC$ MOS structure, which is stepwise subjected to an increasing thermal budget and measured afterwards, will allow for a much faster and cheaper examination of the topic.

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List of Publications

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List of Figures

Symbols

Symbol	Description	Unit
$A_{\mathrm{G}}^{\mathrm{eff}}$	effective gate area	cm^2
A	effective area	cm^2
C_{OX}	oxide capacitance	F
D_{it}	density of interface traps	$\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$
E_{A}	activation energy	eV
E_{B}	energy barrier	eV
E_{B}	breakdown field	$\mathrm{V\,cm}^{-1}$
E_{C}	energy at the bottom of the conduction band	eV
E_{F}	Fermi energy	eV
E_{G}	band gap energy	eV
E_{OX}	oxide field	$\mathrm{V\,cm}^{-1}$
E_{V}	energy at the top of the valence band	eV
E_{i}	intrinsic Fermi energy	eV
E_{t}	trap energy	eV
$I_{\mathrm{CP}}^{\mathrm{max}}$	maximum charge pumping current	A
I_{CP}	charge pumping current	A
I_{D}	drain current	A
I_{GD}	gate-drain current in gated diode mode	A
I_{r}	readout current	A
N_{CP}	number of pumped charges	cm^{-2}
N_{it}	number of interface states	cm^{-2}
N_{t}	number of trapped charges	cm^{-2}
N_{C}	effective density of states in the conduction band	cm^{-3}
N_{V}	effective density of states in the valence band	cm^{-3}
N_{ot}	number of oxide traps	cm^{-2}
Q_{it}	total trapped interface charge	C
R_0	reference readout for voltage shift calculation	V
R_{ch}	channel resistance	Ω
R_{on}	on-resistance	Ω
R_i	readout for voltage shift calculation	V
T	temperature	K
$V_{\mathrm{th}}^{\mathrm{GD}}$	threshold voltage in gated diode mode	V
$V_{\mathrm{th}}^{\mathrm{G}}$	threshold voltage extracted by the method of Ghibaudo	V
$V_{\mathrm{th}}^{\mathrm{sub}}$	subthreshold voltage: gate voltage at which the drain current reaches 1 nA at a drain voltage of 100 mV	V
V_{th}	threshold voltage	V
V_{D}	drain voltage	V

Symbol	Description	Unit
$V_{\mathrm{FB}}^{\mathrm{CP}}$	charge pumping flat band voltage	V
V_{FB}	flat band voltage	V
$V_{\mathrm{G}}^{\mathrm{H}}$	high level of the gate pulse	V
$V_{\mathrm{G}}^{\mathrm{L}}$	low level of the gate pulse	V
$V_{\mathrm{G}}^{\mathrm{op}}$	operation gate voltage	V
$V_{\mathrm{G}}^{\mathrm{rec}}$	recovery or readout voltage	V
$V_{\mathrm{G}}^{\mathrm{str}}$	stress voltage	V
$V_{\mathrm{G}}^{\mathrm{swe}}$	voltage level at the end a voltage sweep	V
V_{G}	gate voltage	V
$V_{\mathrm{TH}}^{\mathrm{CP}}$	charge pumping threshold voltage	V
ΔE_{CP}	active charge pumping energy window	eV
ΔE_{G}	band gap energy window	eV
ΔE_{en}	upper emission boundary of the active energy window	eV
ΔE_{ep}	lower emission boundary of the active energy window	eV
$\Delta V^{\max}$	voltage shift	V
$\Delta V_{\mathrm{th}}^{\mathrm{sub}}$	subthreshold voltage shift	V
ΔV_0	initial voltage shift between varying measurements	V
ΔV_{CV}	capacitance voltage shift	V
$\Delta V_{\mathrm{FB}}^{\max}$	maximum flat band voltage shift	V
ΔV_{FB}	flat band voltage shift	V
ΔV_{G}	total amplitude of the gate pulse	V
ΔV_{th}	threshold voltage shift	V
ΔV	voltage shift	V
μ_0	low field mobility	$\mathrm{cm^2\,V^{-1}\,s^{-1}}$
μ_{ln}	parameter of the log-normal distribution	
μ_{n}	electron mobility	$\mathrm{cm^2\,V^{-1}\,s^{-1}}$
μ	mobility	$\mathrm{cm^2\,V^{-1}\,s^{-1}}$
ν_{thn}	thermal drift velocity of electrons	$\mathrm{cm\,s^{-1}}$
ν_{thp}	thermal drift velocity of holes	$\mathrm{cm\,s^{-1}}$
σ_{ln}	standard deviation of the log-normal distribution	
σ_{nd}	standard deviation of the normal distribution	eV
σ_{n}	capture cross section of electrons	$\mathrm{cm^{-2}}$
σ_{p}	capture cross section of holes	$\mathrm{cm^{-2}}$
σ	capture cross section	$\mathrm{cm^{-2}}$
τ_0	phonon frequency	s
τ_{H}	transition time constant for each H hopping event	s
τ_{cn}	time constant for electron capture in SRH theory	s
τ_{en}	time constant for electron emission in SRH theory	s
τ_{ep}	time constant for hole emission in SRH theory	s
τ	transition time constant	s
ε_0	vacuum permittivity ($8.854\,187\,817 \times 10^{-14}$)	$\mathrm{F\,cm^{-1}}$
$\varepsilon_{\mathrm{r}}^{\mathrm{SiC}}$	relative permittivity of SiC (≈ 10)	1
$\varepsilon_{\mathrm{r}}^{\mathrm{SiO_2}}$	relative permittivity of SiO_2 (3.9)	1
f	frequency	Hz
g_{m}	transconductance	$\mathrm{A\,V^{-1}}$
k_{B}	Bolzmann constant ($8.617\,332\,478 \times 10^{-5}$)	$\mathrm{eV\,K^{-1}}$
n_{inv}	carrier density in the inversion channel	$\mathrm{cm^{-2}}$
n_{i}	intrinsic carrier density	$\mathrm{cm^{-3}}$

Symbol	Description	Unit
q	elementary charge ($1.602\,176\,565\,35 \times 10^{-19}$)	C
$t_{\mathrm{pre}}^{\mathrm{n}}$	accumulation preconditioning time	s
t_{rec}	recovery time	s
t_{str}	stress time	s
t_{OX}	oxide thickness	cm
t_{f}	fall time of the gate pulse	s
t_{hT}	time the sample is subjected to a high thermal budget	s
t_{read}	time extraction point for voltage shift calculation	s
t_{r}	rise time of the gate pulse	s

Acronyms

$I_{\mathbf{D}}$-$V_{\mathbf{G}}$ transfer characteristic.

$\mathbf{V_O}$ oxygen vacancy.

BFOM Baliga figure of merit.

BTI bias temperature instability.

C carbon.

CDF cumulative distribution function.

CP charge pumping.

CV capacitance-voltage.

CVD chemical vapor deposition.

DFT density functional theory.

EDMR electrically detected magnetic resonance.

erfc complimentary error function.

H hydrogen.

MOSCAP metal oxide semiconductor capacitor.

MOSFET metal oxide semiconductor field effect transistor.

$\mathbf{N_2}$ dinitrogen.

$\mathbf{N_2O}$ nitrous oxide.

NBTI negative bias temperature instability.

$\mathbf{NH_3}$ ammonia.

NMP non-radiative multiphonon.

NO nitric oxide.

O oxygen.

P_{bC} carbon dangling bond.

PBS positive bias stress.

PBTS positive bias temperature stress.

PDF probability density function.

PES adiabatic potential energy surface.

POA post oxidation anneal.

Si silicon.

SiC silicon carbide.

SiH_4 silane.

SIMS secondary ion mass spectrometry.

SiO_2 silicon dioxide.

SMU source-measurement unit.

SRH Shockley-Read-Hall.

TEOS Tetraethylorthosilicat.

V_{Si} silicon vacancy.

WBG wide band gap.

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Experiences

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Computer skills

Basic	C
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Driving license	Cars, motorcycles and agricultural vehicles: Austrian category A, B and F.
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Klagenfurt, June 7, 2018