Die approbierte Originalversion dieser Dissertation ist in der Hauptbibliothek der Technischen Universität Wien aufgestellt und zugänglich.
http://www.ub.tuwien.ac.at

The approved original version of this thesis is available at the main library of the Vienna University of Technology.

http://www.ub.tuwien.ac.at/eng

PhD thesis

Physics and Characterization of the Gate Stack in Gallium Nitride based MIS-HEMTs

Ausgeführt am

Institut für Festkörperelektronik
der Technischen Universität Wien

in Kooperation mit der

Infineon Technologies Austria AG

unter der Anleitung von
Ao.Univ.Prof. Dipl.-Ing. Dr.techn. Dionyz Pogany
und
Dr. Clemens Ostermaier

durch

Dipl.-Ing. Peter Willibald Lagger

Kleinegg 3
9701 Rothenthurn

Matrikelnummer 0625122
Studienkennzahl 786 710

Datum	Unterschrift

Dwarfs standing on the shoulders of giants.
Nanos gigantum humeris insidentes.

Bernard of Chartres

Kurzfassung

Die Bedeutung von Elektrizität für Wirtschaft und Gesellschaft nimmt zu und damit auch die Rolle von Halbleiterbauelementen für die elektrische Leistungswandlung. Galliumnitrid und verwandte Verbundmaterialien bieten überragende Materialeigenschaften die eine weitere signifikante Verbesserung der elektrischen Eigenschaften dieser Bauelemente ermöglichen. Das in diesem Zusammenhang favorisierte Bauelementekonzept basiert auf einem Aluminumgalliumnitrid/Galliumnitrid Heterostrukturübergang. Ein auf der Aluminiumgalliumnitrid-Barriere abgeschiedenes Dielektrikum wird überlicherweise verwendet um Gate-Leckströme zu minimieren. Dabei ist allerdings die Dichte an elektrischen Defekten an der Grenzfläche zur Barriere so hoch, dass dies zu extremen Driften der Einsatzspannung führt.

In dieser Arbeit wird eine Methode zur zeitaufgelösten Messung der Relaxation der Einsatzspannungsdrift nach positiven Spannungs-Stresspulsen mit varrierender positiver Stressspanung und Stresszeit am Gate-Kontakt entwickelt. Dieses ermöglicht einen quantitativen Vergleich verschiedener Gate-Strukturen. Im Gegensatz dazu, haben sich die meisten etablierten Methoden zur Charakterisierung der Grenzflächendefektdichte als ungeeignet zum Vergleich verschiedene Prozess- und Designvariationen herausgestellt. Die Verfügbarkeit einer solchen Methode ist der Schlüssel zur technologischen Optimierung der Grenzflächeneigenschaften. Dabei werden systematisch die Einsatzspannungsdriften nach Stresspulsen mit einer Länge von 100 ns bis 10 ks für Relaxationszeiten im Bereich von 1 μs bis zu 1 Ms gemessen. Die typischen Stressspannungen sind dabei im Bereich bis 10 V. Das getestete Material umfasst verschiedene Dielektrika mit variierender Schichtdicke des Dielektrikums und der Aluminiumgalliumnitrid-Barriere. Darüberhinaus wird auch der Einfluss von repetitivem Stress untersucht.

Die experimentellen Daten zeigen eine logatrithmische Verteilung von charakteristischen Zeitkonstanten. Die Einsatzspannungsdrift skaliert dabei mit der angelegten Stressspannung. Es wird dargelegt, warum die Defektprozesse sich nicht mit dem einfachen Modell diskreter Energieniveaus beschreiben lassen. Des Weiteren wird für kurze Stresszeiten und kleine Stressspannungen ein limitierender Effekt der Barrie für die Höhe der Einsatzspannungsdrift angenommen. Darüberhinaus wird gezeigt, dass die dielektrische Konstante einen starken Einfluss auf das Driftverhalten hat, wobei die extrahierten Defektdichten direkt mit der dielektrischen Kapazität skalieren, wenn die Gate-Spannung größer als die kritischen Spannung zur Akkumulation von Elektronen am dielektrischen Interface ist. Daraus wird die Schlussfolgerung gezogen, dass die eigentliche Defektdichte viel höher sein muss und die Messung durch die dielektrische Durchbruchsfestigkeit begrenzt wird.

Abstract

The importance of electricity for our economy and society is increasing and hence the role of power semiconductor devices for improving the efficiency of electrical power conversion systems. Gallium nitride and its compounds offer superior material properties for a further significant improvement of these devices. The favored device structure is based on an aluminum gallium nitride/gallium nitride heterojunction. An insulated gate contact on top of the aluminum gallium nitride barrier layer would be much desired to suppress parasitic gate leakage currents. But the high density of interface states between the barrier and the deposited dielectric causes tremendous threshold voltage drifts.

In this work, a measurement setup for a time-resolved measurement of the recovery curves of the threshold voltage drift after forward gate bias stress pulses of varying magnitude and duration is developed. This setup enables a quantitative comparison of different test samples, whereas most of the established interface characterization methods are not suitable for this purpose. The availability of such a method is of key importance for the technological improvement of the interface quality. This setup is used to perform a systematic study of threshold voltage drift dependency on gate stress bias and time with stress times ranging from 100 ns to 10 ks and recovery times ranging from 1 μs and 1 Ms. The typical stress biases are below 10 V. Different test samples with different dielectric materials, varying dielectric layer thickness and barrier layer thickness are compared. Moreover, the impact of repetitive stress pulses is investigated.

The experimental data show a broad distribution of characteristic stress/recovery time constants of threshold voltage drift ΔV_{th}, as well as an increase with the stress bias. It is concluded that the observed stress/recovery behavior cannot be explained by first-order defect kinetics. Furthermore, a Coulomb charging of the interface is proposed. In these experiments no saturation of ΔV_{th} with increasing stress bias and time is found. For small stress bias and short stress times the barrier layer is proposed to be a rate limiter for electron capture processes at the dielectric/III-N interface. Moreover, it is suggested that under spill-over conditions, i.e. accumulation of a second electron channel at the dielectric/III-N interface, the density of trapped electrons under stress scales with the dielectric capacitance. It is argued that the number of defect states at the interface is larger than what can be electrically measured.

Contents

1 Introduction **2**
- 1.1 Motivation 2
- 1.2 Objective of this work 4
- 1.3 Power Semiconductor Devices 4
- 1.4 Outline of the Thesis 7

2 Fundamentals of Gallium Nitride Based MIS-HEMTs **8**
- 2.1 III-N Semiconductors 8
  - 2.1.1 Crystal Structure and Polarization 8
  - 2.1.2 The AlGaN/GaN Heterostructure 13
  - 2.1.3 The Surface Donor State Model 14
- 2.2 III-N Based MIS-HEMT Devices 16
- 2.3 Gate Dielectrics for III-N Based Devices 18
  - 2.3.1 Review of the SiO_2/Si System 19
  - 2.3.2 Dielectrics On III-N Layers 20

3 Methodology **23**
- 3.1 General Approach 23
- 3.2 Time-Resolved ΔV_{th} Measurements 24

4 Scientific Articles **29**
- 4.1 Summary of the Scientific Articles 29
- 4.2 Other Scientific Contributions 32
- 4.3 Towards understanding the Origin of Threshold Voltage Instability of AlGaN/GaN MIS-HEMTs 34
- 4.4 New Insights on Forward Gate Bias Induced Threshold Voltage Instabilities of GaN-Based MIS-HEMTs 39
- 4.5 Very Fast Dynamics of Threshold Voltage Drifts in GaN based MIS-HEMTs 42
- 4.6 Comprehensive Study of the Complex Dynamics of Forward Bias Induced Threshold Voltage Drifts in GaN Based MIS-HEMTs by Stress/Recovery Experiments 46
- 4.7 Enhancement of V_{th} Drift for Repetitive Gate Stress Pulses due to Charge Feedback Effect in GaN MIS-HEMTs 55
- 4.8 Understanding the Fundamental Limitations for the Improvement of Forward Gate Bias Induced $\mathrm{V_{th}}$ Drift Stability of GaN Based MIS-HEMTs 62

4.9 Role of the Dielectric for the Charging Dynamics of the Dielectric/Barrier Interface in AlGaN/GaN based Metal-Insulator-Seminconductor Structures under Forward Gate Bias Stress 65

5 Conclusion and Outlook 76

List of Figures

1.1 Consecutive transfer characteristics with increasing maximum gate bias $V_{\mathrm{G,max}}$ shows the forward gate bias induced threshold voltage drift. For this test a HEMT structure with a 25 nm $\mathrm{Al_{25}Ga_{75}N}$ barrier layer with a 3 nm GaN cap, on which a 20 nm $\mathrm{Al_2O_3}$ is deposited by an ALD-process, is used. . . . 3
1.2 Frequency, current, voltage domain of the most important power devices [Wik06]. 6
1.3 Theoretical limits of the specific on-resistance $R^{\mathrm{sp}}_{\mathrm{DS,on}}$ versus breakdown voltage V_{br}. The symbols mark results achieved by state-of-the-art devices for different device concepts implemented on different materials [HPE10]. . . . 7

2.1 The ideal wurzite crystal structure consists of two interlaced hcp lattices. In III-N crystals, one lattice is occupied by a metal ion and the other by a N-ion [AMM+02]. 9
2.2 Hexagonal lattice with lattice constants a and c. 9
2.3 Crystal structure of AlN with lattice constants a and c and the cell internal parameter u, i.e. a parameter for the bonding length between Al and $\mathrm{N_{c1}}$. Ideally the bonding lengths $\mathrm{N_{c1}}$ and $\mathrm{N_{b1}}$ are equivalent. In the real crystal it yields that $\mathrm{N_{c1}} > \mathrm{N_{b1}}$. Thus the bond in [001] direction is streched compared to the other three bonds. The same also holds for GaN and AlGaN [AMM+02]. 11
2.4 Miller indices in the hexagonal lattice. III-N compounds show spontanous polarization in the [001] direction. The (001) plan is also called c-plane [Fas05, 08]. 11
2.5 Schematics showing the induction of the piezoelectric polarization in a strained pseudomorphic AlGaN layer on top of a GaN buffer layer [AMM+02, 08]. . . 11
2.6 Spontanous and piezoelectric polarization charges induced in a pseudomorphic AlGaN-layer on top of a relaxed GaN-layer [AMM+02]. 12
2.7 Illustration of the formation of surface dipoles in a free-standing GaN material (top) and the formation of a surface dipole and a 2DEG channel in a heterojunction, e.g. AlGaN on top of GaN (bottom). The build-in field defines a critical thickness for the formation of surface dipoles (top) and a 2DEG channel (bottom). [08]. 13
2.8 Comparison of a high density surface donor state at a single energy level (left) and low density surface donor states distributed in energy (right). The former leads to a fixed surface barrier height Φ_B independent of the layer thickness, while the latter leads to an increasing surface barrier height Φ_B for increasing thickness of the barrier [GMC+10]. 14

2.9 Schematics of the conduction band minimum of a AlGaN/GaN structure showing the various charge contributions [IFN+00]. 15
2.10 Epitaxial structure of a GaN-on-Substrate wafer, which is used for the fabrication of GaN based devices. 17
2.11 Bandgap and band offsets of AlGaN as a function of x varied between GaN ($x = 0$) and AlN ($x = 1$). The valence band maximum of GaN is taken as reference level [AMM+02]. 18
2.12 Schematics of a normally-on MIS-HEMT device build on top of a GaN-on-Si wafer. 18
2.13 Schematics of the near interfacial regions at the SiO_2/Si interface [HP94]. . 20
2.14 Band alignment of various oxides to GaN [RF06]. 22

3.1 Overview of a typical learning cycle. The stress/recovery experiments are based on time-resolved measurements of the ΔV_{th} recovery after forward gate bias stress pulses. 24
3.2 Top: Gate and drain bias signals during the measurement of the transfer-characteristics. Bottom: the transfer characterisitics is measured at discrete gate bias levels, where each drain current point is integrated over a certain integration time. 25
3.3 Drift of the threshold voltage after forward gate bias stress for logarithmically increasing stress time at a constant stress bias of 5 V. The transfer characterisitics is recorded at a drain bias of 1V, initially before stress and then after each stress pulse. 26
3.4 Schematics of the ΔV_{th} measurement used in this work. The drain current is monitored at a constant gate bias $V_{\mathrm{G}} = V_{\mathrm{G,meas}}$. Due to the parallel shift of the transfer characteristics, it is possible to map the transient I_{D} signal to the initial transfer curve to calculate the according ΔV_{th} signal. 26
3.5 Schematics of the field distribution in a GaN MIS-HEMT device during forward gate bias stress. The intrinsic 2DEG channel acts as counter-elecrode to the gate electrode and hence the field is homogenously distributed between gate electrode and 2DEG channel. 27
3.6 Signal pattern of a stress-recovery cycle. The gate is biased at $V_{\mathrm{G}} = V_{\mathrm{G,stress}} > 0$ for a certain stress time t_{s}. After the stress pulse, the gate signal is switched to $V_{\mathrm{G}} = V_{\mathrm{G,meas}}$ and the drain current is measured. In between the measurement points, the device is switched to recovery conditions, where all device terminals are grounded. 27
3.7 Comparison of ΔV_{th} for constant stress bias and logarithmically increased stress time. The coloured lines are recorded on a single device, whereas the black lines are each recorded on a virgin device. The tests are performed on devices with a 30 nm SiO_2 dielectric on top of a barrier layer with a 3 nm GaN cap and 25 nm $Al_{25}Ga_{75}N$ layer. 28

5.1 Schematics of the test device with on-wafer integrated heater resistors. . . . 77

5.2 Recovery of V_{th} drift after a forward gate bias stress at a stress bias $V_{\mathrm{G,stress}} =$ 2 V for a stress time t_{s} of 10 s for varying heater power of 0 to 3 W. The heater is switched of after 7 s of electrical stress to ensure cool-down until the end of the electrical stress pulse. This test is performed on a wafer with a 20 nm $\mathrm{Al_{20}Ga_{80}}$ barrier layer, on which a 25 nm $\mathrm{Si_3N_4}$ is deposited as gate dielectric. 78
5.3 Dummy measurement, i.e. the ΔV_{th} recovery is measured without preceeding stress pulse. The influence of the measurement itself is within ±20 mV for recovery times up to 10^5 s. This test is performed on a HEMT structure with a 25 nm $\mathrm{Al_{25}Ga_{75}N}$ barrier layer with a 3 nm GaN cap, on which a 20 nm $\mathrm{Al_2O_3}$ is deposited by an ALD-process. 80
5.4 Schematic of the oscilloscope-pulse generator based setup. The value of the series resistance $R_{\mathrm{S}} = 50\ \Omega$. 80
5.5 Schematics of the $I_{\mathrm{D}}(V_{\mathrm{D}})$-characteristics for different values of V_{G}. The load-line is defined by the series resistance R_{S} (cf. Fig. 5.4). 81
5.6 Transconductance of the initial transfer characteristics shown in Fig. 3.3. . 81

List of Tables

1.1 Electrical material parameters and figure of merits (FoMs) for selected semiconductor materials at room temperature (300 K) [Wit98, LRS99, KH12, RS]. 6

2.1 Comparison of material properties of substrates used for the expitaxial growth of GaN [RR96, MKAS03, KH12]. 16

Symbols

Symbol	Unit	Meaning
q	[C]	elementary charge
ϵ_0	[As/(Vm)]	vacuum dielectric constant
ϵ_r	[1]	relative dielectric constant
$\mathcal{E}$	[V/m]	electric field strength
E	[eV]	energy
E_F [eV]	Fermi-level	
P	[C/m^2]	polarization
v_sat	[m/s]	saturation velocity
φ	[V]	electrostatic potential
V	[V]	potential difference, i.e. bias
V_th	[V]	threshold voltage
ΔV_th	[V]	threshold voltage drift
Q_it	[C/cm^2]	interface charge density
ΔQ_it	[C/cm^2]	change of the interface charge density, e.g. due to gate stress
N_it	[cm^{-2}]	interface defect density, i.e. Q_it/q
ΔN_it	[cm^{-2}]	change of interface defect density, i.e. $\Delta Q_\mathrm{it}/q$
$P_\mathrm{GaN}^\mathrm{sp}$	[C/cm^2]	spontanous polarization of GaN
$P_\mathrm{AlGaN}^\mathrm{sp}$	[C/cm^2]	spontanous polarization of AlGaN
$P_\mathrm{GaN}^\mathrm{pz}$	[C/cm^2]	piezoelectric polarization of AlGaN
Q_GaN	[C/cm^2]	surface polarization charge density for GaN, i.e. $Q_\mathrm{GaN} = \lvert P_\mathrm{GaN}^\mathrm{sp}\rvert$
Q_AlGaN	[C/cm^2]	surface polarization charge density for a pseudomorphic AlGaN layer grown on GaN, i.e. $Q_\mathrm{AlGaN} = \lvert P_\mathrm{AlGaN}^\mathrm{sp}\rvert + \lvert P_\mathrm{GaN}^\mathrm{pz}\rvert$
$V_\mathrm{G,stress}$	[V]	gate stress bias, usually $V_\mathrm{G,stress} > 0\mathrm{V}$
t_s	[s]	stress time
t_r	[s]	recovery time
C_D	[F]	dielectric capacitance
C_B	[F]	barrier capacitance
τ_emission	[s]	emission time constant
τ_capture	[s]	capture time constant
n	[cm^{-3}]	electron density
p	[cm^{-3}]	hole density
n_S	[cm^{-2}]	sheet electron density in the 2DEG channel

Symbol	Unit	Meaning
σ	[cm^2]	capture cross section
Q_{sh}	[C/cm^2]	sheet charge density
μ_{n}	[cm$^2/Vs$]	electron mobility
E_{C}	[eV]	conduction band minimum
$R^m_{\mathrm{DS,on}}tsp$	[Ω]	specific on-resistance
$I_{\mathrm{DS,max}}$	[A]	maximum drain current of a power device
$R_{\mathrm{DS,on}}$	[Ω]	on-resistance of a power device
V_{br}	[V]	breakdown voltage
f	[Hz]	frequency
E_{G}	[eV]	band gap
κ	[W/m K]	heat conductivity
g_{m}	[S]	transconductance
x	[%]	Al-content in AlGaN

Acronyms

Acronym	Meaning
GaN	gallium nitride
AlGaN	aluminum gallium nitride
AlN	aluminum nitride
Ga	gallium
N	nitrogen
hcp	hexagonal close package
Al	aluminum
MIS	metal-insulator-semiconductor
HEMT	high electron mobility transistor
MIS-HEMTs	metal-insulator-semiconductor high electron mobility transistors
Si	silicon
SiO_2	silicon oxide
Al_2O_2	aluminum oxide
Si_3N_4	silicon nitride
SiC	silicon carbide
2DEG	two dimensional electron gas
UID	unintentional doped
CV	capacitance voltage
CNL	charge neutrality level
MIS	metal-insulator-seminconductor
GaN-on-Si	substrate with epitaxial gallium nitride layers grown on a silicon wafer
HVDC	high voltage direct current
AC	alternating current
DC	direct current
MOSFET	metal-oxide semiconductor field effect transistor
IGBT	insulated gate bipolar transistor
GTO-thyristor	gate turn-off thyristor
ESR	electron spin resonance
H	hydrogen
BTI	bias temperature instability
SMU	source-measurement-unit
ALD	atomic layer deposition

Acknowledgement

This page is dedicated to all those who supported me during the great time of my PhD thesis at Infineon Technologies in Villach. Despite, I take care that this list is complete, I cannot exclude that somebody is missing. Thus, my first thanks go to everybody I forget to mention.

My true thanks go to Clemens Ostermaier, who guided me through the ups and downs during this challeging time. I am very thankful that he gave me the oppurtunity to grow. I am thankful for all our discussions and for his manifold inputs and inspirations. I appreciate his free-spirited way of thinking and working and his exceptional creativity.

My true thanks go to Prof. Dionyz Pogany for his excellent support and help. I am very grateful that he often challenged my ideas and gave me extremly valueable inputs. I am thankful for the great time I could spend in Vienna during the first time of my PhD work and to the numerous discussion we had during the last three years. I am greatly indebted to his patience during correcting my publications and for the great guidance through the interesing process of learning.

I am greatly indebted to Maria Reiner for being a good friend. I owe gratitude to our several discussions. She was a great colleague during the last three years.

I am greatly indebted to Helmut Angerer, who greatly supported me. I am thankful for his strong commitment to my work and my personal developement.

I owe my gratitude to Oliver Häberlen, for his open-minded way of thinking and for his great support regarding the publication of my scientific work.

My true thanks go to Gregor Pobegen, for being a great mentor, especially during the first time of my PhD. I thank him for the great discussions and the inputs he had on my work.

I owe my gratitude to Katrin Lenhart for her initiative to connect people in the PhD network.

I am greatly indebted to Ingrid Rotar and Christina Katefidis, for their cooperativeness regarding all my business trips.

I like to thank Michael Nelhiebel, for connecting me with other students in the group of interface specialists, this helped me a lot.

I am very grateful to Josef Mohamed for his interest and great support during the design process of the heater device. I am indebted to Gerhard Prechtl for great discussions and for helping me to get resources to implement the heater device.

I am indebted to Hiroshi Narahashi, Martin Sporn and Stefan Krivec. They helped me during various process experiments.

I am thankful to Heinz Mösslacher for his input on metal layer reliability.

I am very greatful to Michael Stadtmüller, for the numerous discussions on semiconductor physics and for the very valuable inputs on dielectric layer processing. My great thanks go to Günter Denifl, who helped me performing important process experiments.

My thanks go to Patrick Steinschifter and Elisabeth Greil for their great support.

My great thanks to the GaN team, especially Bernhard Brunner, Gianmauro Pozzovivo, Simone Lavanga, Marco Silvestri and Arno Zechmann.

My great thanks to Wolgang Tscharre for being interested in my questions and for his great help during numerous device analyis.

My thanks go to Gottfried Strasser, who gave me the oppurtunity to work at the Institute of Solid State Electronics at the Vienna university of technology during the first months of my PhD work.

I am thankful to all interns, which I had the chance to supervise. My great thanks go to Alexander Schiffmann, for his highly motivated way of working and for his fundamental inputs for fast time-resolved measurements of the threshold voltage drift. My thanks go to Lukas Briesch for challenging my knowledge on semiconductor physics. I am thankful to Bernhard Fritz for his great work. My great thanks go to Stefan Donsa and Philipp Spreitzer for there great interest and for there self-motivated way of working.

My thanks go to Alexander Grill for the inspiring discussions we had during the time he spent in Villach.

I am much obliged to my parents. They always supported my ideas and objectives and gave me the time and freedom to grow. Their contribution is essential.

Last but not least, many thanks to my sister and my brother and all the other members of my family. They are an important part of my life.

Chapter 1

Introduction

The world's energy consumption was increased by more than 90 % within a period of 38 years, from 54.4 PWh in 1973 to 103.7 PWh in 2011. In the same time, the share of electricity raises from 9.4 % (5.1 PWh) to 17.7 (18.4 PWh), where the total increase of electricity was approximately 260 % [IEA]. This clearly demonstrates the raising significance of electricity in the past four decades.

The energy value chain describes the supply of consumers with electricity, which includes generation, transmission and consumption. Electrical energy is not directly available itself, but has to be generated out of some other form of available energy. The process of generation includes the conversion of a primary energy source (e.g. oil, coal, natural gasoline, nuclear energy, solar energy, hydro power, wind power, biomass, etc.) into electrical power. Eletrical power is determined by its voltage, current and frequency. The transmission of electrical power from the generator to the consumer includes the conversion of electrical power to different voltage, current and frequency levels. Finally, the electrical power is converted into the desired form for the end-use consumption (e.g. mechanical power in a electric motor, light in a light bulb, heat in a stove, etc.). All this conversion processes require power semiconductor devices, which are lossy. Hence it is desired to improvement their efficiency [IFX08].

Although gallium nitride is considered as base material for future power device technologies, which enhance the efficiency of power conversion processes, there are several issues to solve prior to a broad market introduction and acceptance. Especially the reliability of such devices is still of major concern. In this work, the focus is on the understanding of dielectrics for gallium nitride based devices, which would enable a attractive device concept with an insulated gate contact.

The first chapter includes a section about the motivation of this work and its objectives, which is followed by general introduction to power devices and an outline of the thesis.

1.1 Motivation

Gallium Nitride (GaN) is a compound seminconductor, which has drawn a lot of attention in the last years. It is a wide bandgap semiconductor, which offers beneficial material properties for power semiconductor devices (e.g. high breakdown voltage, high channel mobility, high channel electron density, etc.). Therefore, it is considered to, at least partly, replace silicon (Si) as the dominant base material for these devices. An intrinsic two dimen-

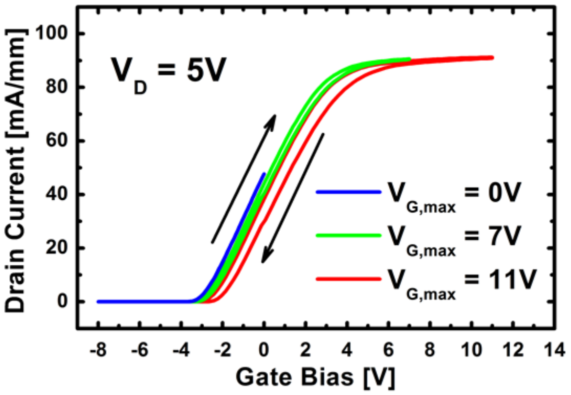


Figure 1.1: Consecutive transfer characteristics with increasing maximum gate bias $V_{\mathrm{G,max}}$ shows the forward gate bias induced threshold voltage drift. For this test a HEMT structure with a 25 nm $Al_{25}Ga_{75}N$ barrier layer with a 3 nm GaN cap, on which a 20 nm Al_2O_3 is deposited by an ALD-process, is used.

sional electron gas (2DEG) channel can be induced in GaN by growing an epitaxial barrier layer, e.g an aluminum gallium nitride (AlGaN) layer, with a higher bandgap on top of the underlying GaN substrate without intentional doping of the active channel region. The intrinsic 2DEG channel is the starting point for a so-called high electron mobility transistor (HEMT). This is a lateral field-effect transistor, where the gate contact, in the simplest case, is a Schottky contact, where a metal is directly deposited on top of the barrier layer. The 2DEG channel is connected by ohmic contacts, i.e. source and drain [KBKO93]. Due to the intrinsic 2DEG channel the region below the gate contact has to be actively depleted by a negative gate bias, hence a HEMT is a normally-on device. Since the barrier has insufficient insulation properties, an additional insulating layer is deposited on top of the barrier layer to minimize parasitic gate leakage currents. A device with such an insulating layer is called metal insulator semiconductor (MIS) HEMT [KSY$^+$03]. The word insulator is used instead of oxide, because it is the more general term and often also nitrides are used as gate insulators for GaN MIS-HEMTs. Although, the problem of gate leakage currents can be solved by a MIS-gate stack, the physical and technological properties of the insulator/barrier interface are poorly understood. Defect states at these interface are identified as the root cause of tremendous forward gate bias induced threshold voltage drifts (ΔV_{th}), which are observed in these devices. The V_{th} drifts are due to electron trapping at interface defect states [IMKK11, HYRC12, WMZ$^+$13, CRJ$^+$13]. An example of V_{th} drifts under positive gate bias stress is given in Fig. 1.1. In general, there is still a lack of knowledge about the suitable characterization of interface defect states in GaN based MIS-HEMTs, where a suitable methodology is presented in this work.

A comparison of different interface characterization methods, on a simpler test structures without barrier layer, including frequency dependent CV, UV assisted CV and admittance spectroscopy reveals huge discrepancies of the observed values of the extracted interface defect state density [MTLC12]. It is mentioned that these methods are well-established for SiO_2/Si technology [NB03]. But the barrier layer in a MIS gate stack of a GaN HEMT adds additional modeling complexity due to the additional barrier layer. Nevertheless, these small-signal based measurement techniques are widely deployed to study the density of defect states at the dielectric/III-N interface, including UV-assisted CV [IMKK11, YSM12], quasi-static CV [HYRC12] and conduction spectroscopy techniques [SKS12, CRJ$^+$13]. The interpretation of the measurement results of small-signal based characterization methods is not straightforward. The measurement itself provides two independent informations, i.e. amplitude and phase. In general, an equivalent circuit model is necessary to calculate the parameters of interest [NB03]. Furthermore, assumptions have to be made for models with more than two parameters. In many cases the existing models, originally developed for the characterization of the SiO_2/Si interface, are used to characterize the dielectric barrier gate stack without challeging if the model and the corresponding assumptions are suitable or not [SKS12]. Another issue is that the small-signal measurements, in the positive bias regime, are influenced by large-signal V_{th} drifts, i.e. no quasi-equilibrium state can be established during the measurement [LSP$^+$13b].

The difficulties and issues related with small-signal based methods can be easily overcome by using a much simpler method, which is based on the extraction of ΔV_{th} after forward gate bias stress from transfer characterisitic measurements [IMKK11, HYRC12, WMZ$^+$13, CRJ$^+$13]. The advantage is that measurements of the transfer characteristics are simple to implement and that they allow a straightforward interpretation of the measurement result. Moreover, the measurement results for different samples can be directly compared. In addition, this method serves a basis for the time-resolved measurement of the V_{th} drift, which is also well-established for SiO_2/Si technologies [KGR$^+$08]. The methodology used throughout this work is based on stress-recovery cycles, where after defined forward gate bias stress pulses with a magnitude of $V_{\mathrm{G,stress}}$ and a stress duration of t_{s} a time-resolved measurement of the ΔV_{th}-recovery is performed. This methodology forms the foundation of this thesis. Time-resolved measurements of ΔV_{th}-recovery enables a quantitive comparison of different samples, which is a key requirement for the development of a proper gate stack. They are a suitable tool for technology development and quality engineering.

1.2 Objective of this work

The objective of this work is to understand the behavior and physics of V_{th} drifts in GaN based MIS-HEMTs and to further evaluate, understand and model which parameters influence this behavior. This includes an investigation of the influence of layer thicknesses, layer structures, dielectric constants, as well as an assessment of different dielectric materials. Moreover, the influence of process parameters, cleaning sequences prior to deposition and post-deposition annealings is to be assest. In addition, the location and nature of defects, which cause the V_{th} drifts is to be investigated.

1.3 Power Semiconductor Devices

Power semiconductor devices are used to control the flow of electrical power through an electrical load. They are typically operated in two different conditions, i.e. on-state and off-state. The ideal power switch conducts any current without losses during on-state and blocks any bias up to the breakdown voltage of the device without any leakage current during off-state, while it does not consume any energy for the switching from off- to on-state [Bal08]. Therefore, no power is consumed by the ideal device itself. For real devices, the intention is to minimize all loss contributions as far as possible to further improve the efficiency of the device operation in power applications.

By switching from on-state to off-state, power semiconductor devices enable the conversion of electrical power between different current, voltage and frequency levels. They are used in a broad range of applications with different power levels and frequency. These applications are ranging from a few watts (e.g. AC adapter for mobile phones) to gigawatts (e.g. HVDC transmission systems), where different device concepts are used for different power levels. Typical devices are MOSFETs, IGBTs, GTOs and Thyristors. Each concept is suitable for applications at different power levels. In general, there is a trend that with increasing switching frequency, the maximum achievable power level is decreasing, cf. Fig. 1.2. From the application point of view a high switching frequency is much desired, because it enables to shrink the passive components in a power electronic system and hence enables to increase the power density of the system, i.e. the power rating of a system per unit volume [KBW$^+$10]. The main parameters of a power device can be summarized as

- breakdown voltage V_{br},
- current rating,
- switching capacitance,
- on-resistance $R_{\mathrm{DS,on}}$.

Moreover, the breakdown voltage V_{br} and the on-resistance $R_{\mathrm{DS,on}}$ are connected. In the simplest case of a unipolar power device in a 1D field configuration, the specific on-resistance per unit area $R^{\mathrm{sp}}_{\mathrm{DS,on}}$ is given by [Bal82, SN07, Bal08]

$$R^{\mathrm{sp}}_{\mathrm{DS,on}} = \frac{4V^2_{\mathrm{br}}}{\epsilon_{\mathrm{S}}\mu_n E^3_{\mathrm{C}}}[\Omega\mathrm{cm}^2], \tag{1.1}$$

where ϵ_{S} is the dielectric constant of the semiconductor, μ_{n} the electron mobility and E_{C} the critical electric field strength for breakdown of the material. The denominator of (1.1) is commonly refeered to as Baliga's figure of merit for power devices (BFoM). It was originally formulated in 1982 by Baliga [Bal82, Bal08] and it combines the key material parameters for the minimization of the conduction losses in power devices in a single figure of merit. It is often used as a benchmark for the suitability of semiconductor materials for the developement and fabrication of power semiconductor devices. The electrical properties of a semiconductor material define the fundamental physical limitations for the electrical performance of a power semidonductor device based on this material. Another important FoM was formulated in 1965 by Johnson [Joh65]. The so-called Johnson Figure of Merit (JFoM) defines the power-frequency product and is important for high frequency power devices in high frequency power amplifiers, like e.g. in mobile communication base stations. It is defined by

$$\mathrm{JFoM} = \frac{E_{\mathrm{C}}v_{\mathrm{sat}}}{2\pi}, \tag{1.2}$$

where v_{sat} is the electron saturation velocity of the material. In Table 1.1 an overview of the most important material parameters for selected materials is given. The theoretical prediction of BFoM and JFoM classifies GaN as a material with superior properties for the use as base material for power semiconductor devices. Fig. 1.3 shows achieved $R^{\mathrm{sp}}_{\mathrm{DS,on}}$ of

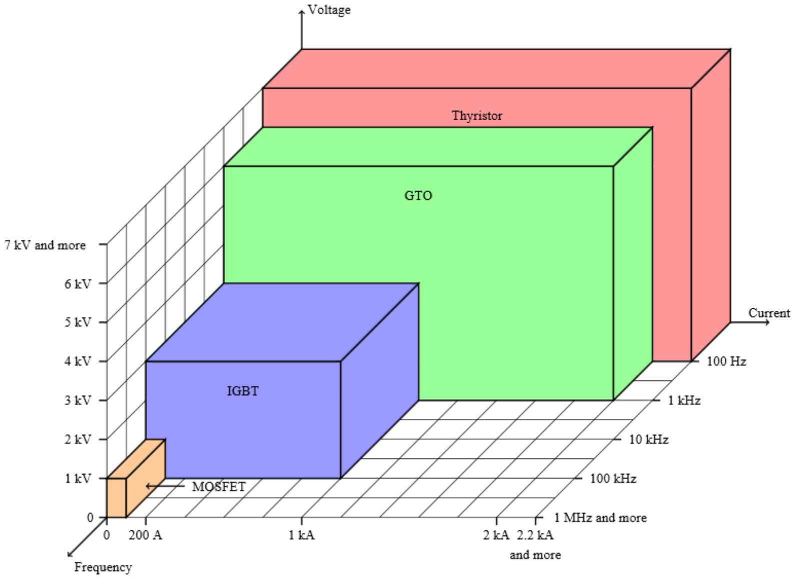


Figure 1.2: Frequency, current, voltage domain of the most important power devices [Wik06].

state-of-the-art devices in comparison to the theoretically predicted limitations for Si, SiC and GaN according to Baliga's figure of merit [HPE10]. Since the prediction is limited to the one dimensional case of a unipolar device, the theoretical proposed limits are exceeded using advanced device concepts, like superjunction MOSFETs or IGBTs [Bal08]. Beyond that, an alternative approach for the improvement of $R_{\mathrm{DS,on}}^{\mathrm{sp}}$ is using new materials with better material properties, like e.g. GaN and SiC.

In the following, the focus is on GaN based MIS-HEMTs [KSY+03], where an intrinsic 2DEG channel with an electron concentration in the order of 10^{13} cm^{-2} [ASS+99] is induced in an AlGaN/GaN heterostructure, directly below the AlGaN barrier. The main advantage is that the GaN channel region is undoped and hence high channel mobilities in the order of 2000 cm^2/Vs are achieved [FMUM+11].

	unit	Si	GaAs	4H-SiC	6H-SiC	GaN (wurzite)	Diamond
ϵ_{r}		11.9	10.9	9.7	9.7	8.9	5.7
μ_{n}	[cm^2/Vs]	1400	8500	900	400	2000 (AlGaN/GaN)	2200
E_{C}	[MV/cm]	0.3	0.55	3	3	3.3 - 5	5.6
E_{G}	[eV]	1.12	1.4	3.3	3	3.4	5.5
κ	[W/cm K]	1.3	0.55	4.9	4.9	4.1 (bulk GaN)	20
v_{sat}	[cm/s]	10^7	$1.2 \cdot 10^7$	$2 \cdot 10^7$	$2 \cdot 10^7$	$2.7 \cdot 10^7$ (ideal)	$2.7 \cdot 10^7$
BFoM		1	34	524	233	4946	4896
JFoM		1	2	20	20	45	50

Table 1.1: Electrical material parameters and figure of merits (FoMs) for selected semiconductor materials at room temperature (300 K) [Wit98, LRS99, KH12, RS].

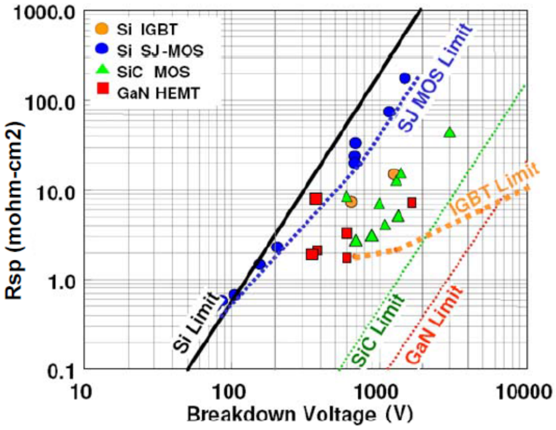


Figure 1.3: Theoretical limits of the specific on-resistance $R^{\mathrm{sp}}_{\mathrm{DS,on}}$ versus breakdown voltage V_{br}. The symbols mark results achieved by state-of-the-art devices for different device concepts implemented on different materials [HPE10].

1.4 Outline of the Thesis

In Chapter 1 a general introduction of the work and an short overview to power devices is given. Subsequently, in Chapter 2, the basics of III-N material physics are introduced and the advantages of III-N based power devices are discussed. This is followed by a review of the state-of-the-art knowledge and challenges regarding MIS gate contacts for such devices. In the next chapter (Chapter 3), the methodology of time-resolved ΔV_{th}-measurements is described. The final chapter summarizes the findings of this works and give an outlook regarding the open topics and questions. Chapter 4 contains all the scientific articles that have been published out of this thesis work. An summary of the thesis and an outlook is given in Chapter 5.

Chapter 2

Fundamentals of Gallium Nitride Based MIS-HEMTs

This work is about the characterization and modeling of the gate stack in GaN based metal-insulator-semiconductor (MIS) high electron mobility transitors (HEMTs) [KSY$^+$03]. In contrast to a standard MOS gate structure, where a dielectric is grown on top of a bulk Si wafer, the gate stack in these devices consists of a heterojunction, e.g. an AlGaN layer on top of a GaN substrate, on which a dielectric is deposited. A further difference to standard MOS devices is that these devices are normally-on, i.e. their threshold voltage is negative and they have to be actively switched off by applying a negative gate bias. Unfortunately, these devices are very sensitive to positive gate bias signals, which causes immediate drifts of their threshold voltage.

This chapter starts with some general considerations about the importance of electricity and the role of power devices to control the flow of electrical power. Subsequently, the advantages of GaN based power devices are motivated and the basic material properties of III-N semiconductors are reviewed. Furthermore, the basics of of III-N based MIS-HEMTs, with a focus on the MIS gate stack, are introduced and the challenges of depositing a dielectric on top of III-N materials are discussed.

2.1 III-N Semiconductors

In this section, the material properties of GaN, AlN and their alloy AlGaN are reviewed to give a basic understanding of these materials. Detailled information about material properties can be found in [RS, LRS99]. A comprehensive discussion of the polarization effects is given in [BFV97, AMM$^+$02, 08].

2.1.1 Crystal Structure and Polarization

Group III-N compound semiconductors are formed by a group-III metal-ion (e.g. Ga, Al or In) and the group-V element N. The focus is on the wurzite crystal structure (Fig. 2.1), which consists of two interlaced hcp lattices (Fig. 2.2) with a stacking sequence of AaBb [Fas05, ASS$^+$99, AMM$^+$02, 08]. Upper and lower case corresponds to the first and second hcp lattice, respectively. In group III-N compound semiconductors, one hcp lattice is occupied by the metal-ion and the other one by the N ion, forming a metal-face or a N-face crystal

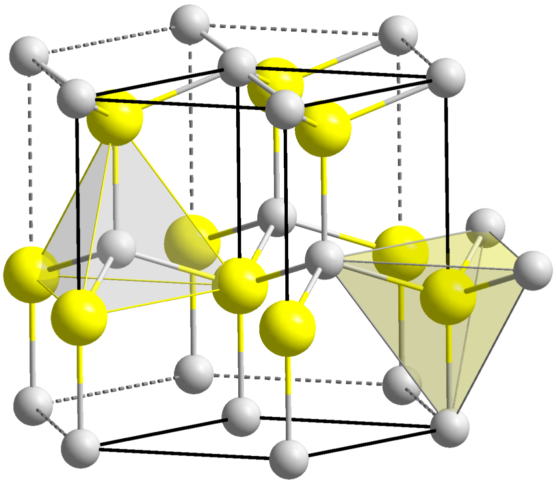


Figure 2.1: The ideal wurzite crystal structure consists of two interlaced hcp lattices. In III-N crystals, one lattice is occupied by a metal ion and the other by a N-ion [AMM+02].

[ASS+99, AMM+02, 08]. Here the focus is on AlN and GaN and its alloy AlGaN. The latter is is a ternary compound with a stochastic distribution of Ga and Al. The Al-content x is commonly declared with the notation $Al_xGa_{1-x}N$.

In Fig. 2.3, the tetrahedal bonding configuration between Al and N in Al-face AlN is shown. The tetrahedal bonding configuration is due to formation of sp^3 hybrid orbitals between Al and N [Fas05]. In N-face AlN, Al and N change their places in the wurzite crystal structure. In the following, the focus is on metal-face crystals. The Al metal-ion has a partial positive charge, while the N ion has a partial negative charge, which is due to the difference in electronegativity [Fas05]. This induces a dipole moment between each pair of Al and N atoms. The same considerations can also be applied to GaN and AlGaN.

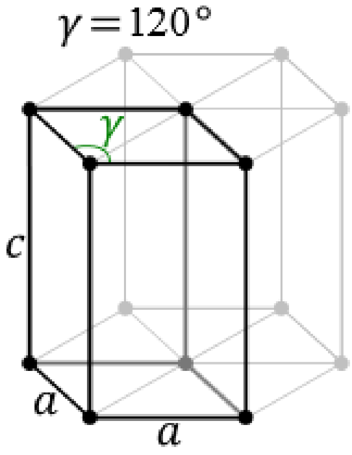


Figure 2.2: Hexagonal lattice with lattice constants a and c.

In the ideal wurzite structure all bonding lengths are equivalent and the vectorial sum over all dipole moments is zero. However, in III-N crystals a macroscopic polarization of the material in [001]-direction (Fig. 2.4) is induced by the difference in bonding length between the metal-ion and N in [001]-direction compared to the bonding length to the three other N atoms, cf. Fig. 2.3. In this case, the vectorial sum of all dipole moments adds up and the material shows a macroscopic spontanous polarization in [001]-direction [08]. It is to mention that the alternative notation [0001] is often found in literature instead of [001]. The spontanous polarization [ASS+99, 08] induces sheet charges of opposite sign at the {001}-surfaces of the material of magnitude

$$Q_{\mathrm{pol}} = P_{\mathrm{sp}}, \tag{2.1}$$

where Q_{pol} is the polarization induced sheet charge density and P_{sp} is the spontanous polarization of the material in [001]-direction. In a HEMT structure (see section 2.2), an AlGaN layer is pseudomorphically grown, i.e. with the same lattice constant a (cf. Fig. 2.2), on top of a relaxed GaN buffer layer. In this case, an additional piezoelectric polarization is induced in the AlGaN layer due to strain, which is schematically explained in Fig. 2.5. The lattice constants vary between GaN and AlN from a = 0.31986 nm and c = 0.52262 nm to a = 0.31095 nm and c = 0.49939 nm [AMM+02]. The values for the spontanous and piezoelectric polarization for a pseudomorphic AlGaN layer on top of a relaxed GaN layer as function of the aluminum content x are shown in Fig. 2.6. The higher spontanous polarization of AlN is due to a larger difference in electronegativity between Al and N in comparison to Ga and N [Fas05, 08]. The piezoelectric component is due to the smaller lattice constant a of AlGaN compared to the GaN substrate. In the case of AlGaN, the magnitude of the dipoles is randomly distributed, where the dipole moment at Al-sites is higher compared to the Ga-sites. Consequently, the magnitude of resulting spontanous polarization of AlGaN varies between the value for GaN and AlN. Moreover, the random distribution of Al and Ga is a source of scattering for electrons in the 2DEG channel (i.e. alloy scattering) and hence reduces the mobility [Sin03, 08].

In an idealized picture, where only the polarization induced sheet charges are considered, the electric field strength in the free standing material is given by

$$\mathcal{E}_{\mathrm{pol}} = \frac{Q_{\mathrm{pol}}}{\epsilon_0 \epsilon_r}, \tag{2.2}$$

where ϵ_0 is the vaccum permittivity and ϵ_{r} is the relative dielectric constant of the layer. The build-in potential V_{bi} follows as

$$V_{\mathrm{bi}} = \mathcal{E}_{\mathrm{pol}} t, \tag{2.3}$$

where t is the layer thickness. For a GaN layer, the polarization-induced electric field strength according to (2.2) is $\mathcal{E}_{\mathrm{pol}} \approx 3.64$ MV/cm $= 0.364$ V/nm [AMM+02]. This is in the order of the critical electric field strength for breakdown of the material, which is according to literature between 3.3 MV/cm [KH12] and 5 MV/cm [RS] depending on the material quality. Another example of an AlGaN/GaN heterostructure is given, because of the relevance of this structure for GaN based HEMTs. In a strained $\mathrm{Al}_{0.20}\mathrm{Ga}_{0.80}\mathrm{N}$ on top of a relaxed GaN buffer layer, the polarization induced electric field strength is $\mathcal{E}_{\mathrm{pol}} \approx 6$ MV/cm = 0.6 V/nm. Hence, the build-in potential according to (2.3) for a 20 nm thick layer is $V_{\mathrm{bi}} = 12$ V [AMM+02]. This is totally unrealistic, because the build-in

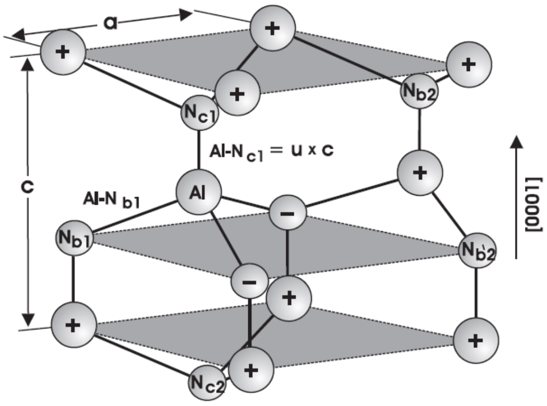

a
c
$Al-N_{c1} = u \times c$
$Al-N_{b1}$
Al
N_{c1}
N_{b1}
N_{b2}
N_{b2}
N_{c2}
[001]

Figure 2.3: Crystal structure of AlN with lattice constants a and c and the cell internal parameter u, i.e. a parameter for the bonding length between Al and N_{c1}. Ideally the bonding lengths N_{c1} and N_{b1} are equivalent. In the real crystal it yields that $N_{c1} > N_{b1}$. Thus the bond in [001] direction is streched compared to the other three bonds. The same also holds for GaN and AlGaN [AMM+02].

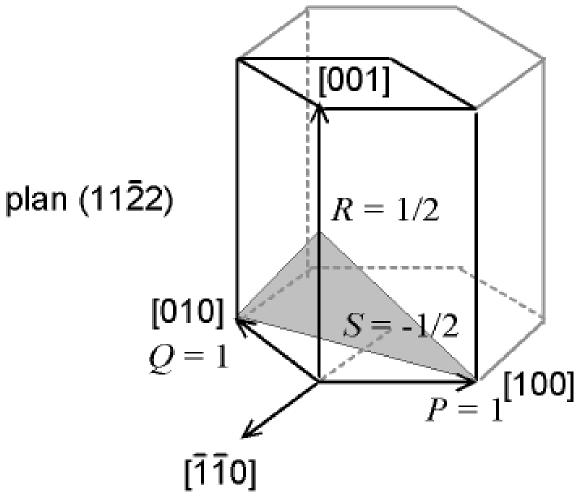

[001]
plan $(11\bar{2}2)$
$R = 1/2$
[010]
$Q = 1$
$S = -1/2$
[100]
$P = 1$
$[\bar{1}\bar{1}0]$

Figure 2.4: Miller indices in the hexagonal lattice. III-N compounds show spontanous polarization in the [001] direction. The (001) plan is also called c-plane [Fas05, 08].

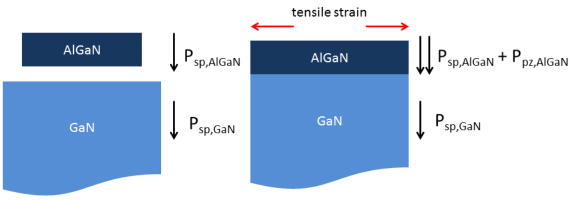

AlGaN
$P_{sp,AlGaN}$
GaN
$P_{sp,GaN}$
tensile strain
AlGaN
$P_{sp,AlGaN} + P_{pz,AlGaN}$
GaN
$P_{sp,GaN}$

Figure 2.5: Schematics showing the induction of the piezoelectric polarization in a strained pseudomorphic AlGaN layer on top of a GaN buffer layer [AMM+02, 08].

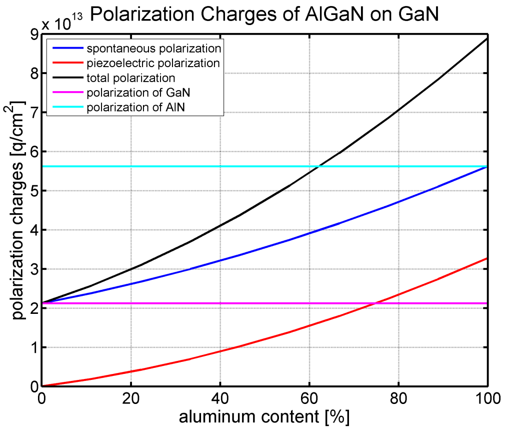


Figure 2.6: Spontanous and piezoelectric polarization charges induced in a pseudomorphic AlGaN-layer on top of a relaxed GaN-layer [AMM$^+$02].

potentential exceeds the bandgap of the material. Nevertheless, the energy E stored in a layer of a polarized material is given by

$$E = \frac{Q_{\mathrm{pol}}^2 A}{2\epsilon_0 \epsilon_r} t, \tag{2.4}$$

where t is the thickness of the layer and A is the area. Hence, the energy per unit area scales linearly with the thickness t. This equation suggests that in order to minimize the energy, which is stored in the system, it is beneficial to locally compensate the polarization charge Q_{pol}. The local compensation mechanism of the polarization charges is reviewed with a thought experiment [08]: The bandgap of GaN sets a limit to the thickness of a spontanous polarized layer (i.e. critical thickness) beyond which the polarization charges are neutralized. Considering the bandgap of GaN to be 3.4 eV, the upper limit for the critical thickness of a GaN layer beyond which the polarization charges are compensated is $\approx$ 10 nm. This is an upper limit, because in a real structure there are surface states in the bandgap of the material. Fig. 2.7 sketches the formation of surface dipoles for a free standing GaN layer and for a pseudomorphic AlGaN layer on top of a GaN buffer. In thermal equilibrium a common Fermi-level E_{F} is established [WHS89] and consequently, the valence band maximum of the GaN layer exceeds the Fermi-level E_{F} for a certain critical thickness. Since no surface states are considered in this idealized picture, the polarization charges are compensated by the formation of a hole channel at the surface. The principle of charge neutrality requires that an electron channel on the bottom side of the layer has to be formed (Fig. 2.7). In this case free charge carriers are locally compensating the polarization charges. In a more realistic consideration one has also to consider surface states and donor states in the bulk of the material [EYN13]. According to (2.4), the local compensation of the polarization charges also reduces the energy, which is stored in the system.

A further implication of the local charge compensation is that in a GaN buffer layer with a typical thickness of some micrometers, the polarization charges $\pm Q_{\mathrm{GaN}}$ are supposed to be compensated locally (i.e. separately on the top and on the bottom of the layer). For the further discussion, the charge balance of the gate stack is of interest. The gate stack is build on-top of a GaN buffer layer, where only the local polarization charges of the GaN layer have to be considered (i.e. the polarization on top of the layer). The polarization

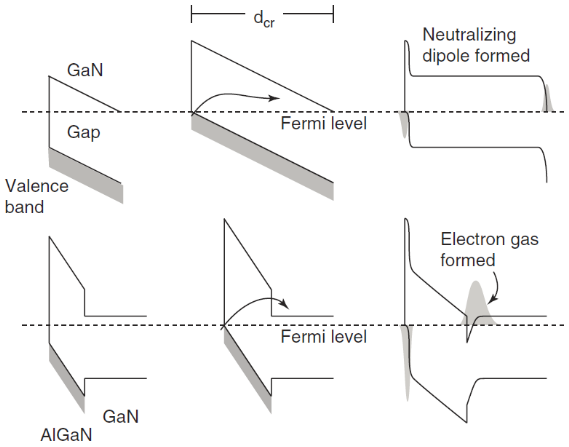


Figure 2.7: Illustration of the formation of surface dipoles in a free-standing GaN material (top) and the formation of a surface dipole and a 2DEG channel in a heterojunction, e.g. AlGaN on top of GaN (bottom). The build-in field defines a critical thickness for the formation of surface dipoles (top) and a 2DEG channel (bottom). [08].

charges on the GaN buffer side are supposed to be of no relevance for charge balance the gate stack. In section 2.1.3, the formation of the 2DEG channel in a AlGaN/GaN structure is discussed, where the positive charges are ascribed to ionized surface donor state instead of holes.

2.1.2 The AlGaN/GaN Heterostructure

The AlGaN/GaN heterostructure is a core building block of GaN based HEMT devices, as already mentioned before. This is due to formation of an intrinsic 2DEG channel in the GaN buffer directly below a thin pseudomorphic AlGaN barrier layer, which is used as electron channel in those devices. The 2DEG conductivity of the AlGaN/GaN structure was first observed in 1991 by Khan et al. [KHKO91], where an increase of the 2DEG mobility by more than a factor of ten in comparison to the bulk mobility was found. In the following, the source of the 2DEG electrons was under debate, where several possibilities were considered. In principle, also other alloys can serve as barrier layer, usually this includes alloys of AlN, InN and GaN. Here the focus is on AlGaN solely, because of its importance for GaN based power devices.

In 2000, Ibbetson et al. [IFN+00] identified surface states as the source of 2DEG electrons and proposed a dominant surface donor state at an energy level of 1.65 eV below the AlGaN conduction band minimum in a $Al_{0.34}Ga_{0.66}N$/GaN structure. Since then it is widely accepted that the 2DEG electrons are originating from surface states, while their microphysical nature is still under debate. In literature either fixed surface barrier heights [IFN+00, SCM+01, HKW+03] or varying surface barrier heights [KS05, GMC+10, HCM+10] for varying barrier thicknesses are reported. The former observations corresponds to a high density of states at a single dominant trap energy level, while the latter one suggests a distribution of low density surface states over a wide range of the bandgap. In Fig. 2.8 both cases are schematically depicted.

In [HCSM10] a correlation between oxidation of the surface and behavior of the barrier

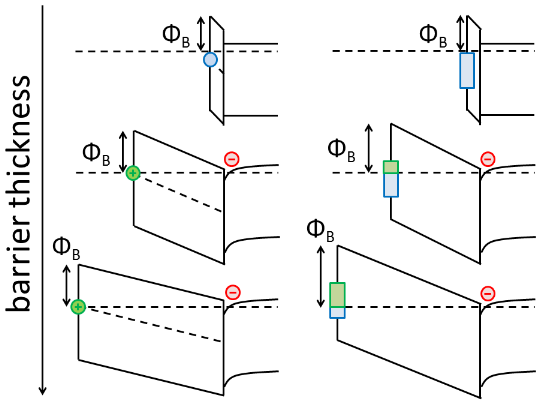


Figure 2.8: Comparison of a high density surface donor state at a single energy level (left) and low density surface donor states distributed in energy (right). The former leads to a fixed surface barrier height Φ_B independent of the layer thickness, while the latter leads to an increasing surface barrier height Φ_B for increasing thickness of the barrier [GMC+10].

height with increasing layer thickness is demonstrated. This suggests a correlation between oxidation and the electronic structure of the surface. Nevertheless, the GaN (001) surface is well known to oxidize in ambient atmosphere, where a native Ga_2O_3 is formed [Ber96, WWG99, DFN06a, DFN06b]. A possible relation between oxidation and the origin of the 2DEG is disussed in [DFN06a, KRL+02]. Further, dangling bonds on the GaN (001) surface are considered to be the source of 2DEG electrons [GMC+10]. A very detailled investigation based on density functional theory about surface reconstructions on (001) GaN and AlN surfaces and there oxidation is made in [MWdW10], where the fixed and variable surface barrier heights are attributed to different densities of surface donors. This could be related to different growth, surface preparation, processing and annealing conditions. Further it is indicated that there is also a difference in the nature of the surface states and not only their density.

However, while the exact nature of the surface donor states is still under debate, their importance for 2DEG creation is widely accepted.

2.1.3 The Surface Donor State Model

The surface donor state model was originally proposed by [IFN+00] and is reviewed in the following. It is a phenomenological model, where no detailled information about the surface states is included. In the following, the arguments for the surface states to be the origin of the 2DEG electrons are summarized. In [IFN+00], the following charge contributions in a AlGaN/GaN stack (Fig. 2.9) are identified:

- polarization induced surface charges on top of the AlGaN layer: $-Q_{\mathrm{AlGaN}}$
- polarization induced interface charges at the AlGaN/GaN interface: $Q_{\mathrm{AlGaN}} - Q_{\mathrm{GaN}}$
- negative sheet charge due to the 2DEG: $-qn_{\mathrm{S}}$

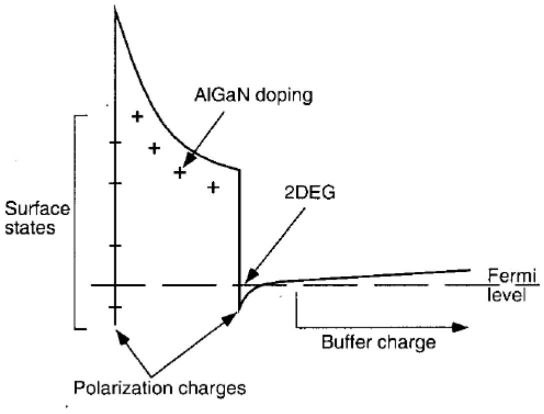


Figure 2.9: Schematics of the conduction band minimum of a AlGaN/GaN structure showing the various charge contributions [IFN+00].

- equivalent sheet charge density due to positive charges from ionized donors in the barrier layer: Q_{D}
- equivalent sheet charge density due to buffer charges: $-Q_{\mathrm{buffer}}$
- donor charges from surface states: Q_{surface}

The positive polarization sheet charge of the GaN buffer layer $+Q_{\mathrm{GaN}}$ is assumed to be compensated locally according to the arguments given in section 2.1.1 and hence do not contribute to the charge distribution within the gate stack. Further, the spatial confinement of the 2DEG in the GaN channel layer directly below the AlGaN barrier excludes that the positive countercharge Q_{GaN} influences this region, because otherwise the electrons would not be confined [IFN+00]. But the confinement of the 2DEG is an experimentally well known fact, proven by CV concentration profiles [ASS+99]. However, the assumption of charge neutrality within the gate stack yields that

$$0 = -Q_{\mathrm{AlGaN}} + Q_{\mathrm{AlGaN}} - Q_{\mathrm{GaN}} - qn_{\mathrm{S}} + Q_{\mathrm{D}} - Q_{\mathrm{buffer}} + Q_{\mathrm{surface}}. \tag{2.5}$$

The polarization charge contributions of the AlGaN layer cancel out, while the contribution of the GaN layer remains. This contribution was not included in the original work of [IFN+00], but should be included in the opinion of the author. The 2DEG could be influenced by negative space charge in the buffer layer, but for the sake of clarity this component is neglected. A positive space charge contribution from the buffer layer can be excluded due to the confinement of the 2DEG. The barrier is not intentially doped and thus it is assumed that $Q_{\mathrm{D}} = 0$. To explain a 2DEG with a typical density in the order of 10^{13} cm^{-2} a doping density in the order of 10^{19} cm^{-3} would be required for typical barrier thicknesses of 10 to 20 nm. Such a high doping density would degrade the channel mobility and can thus be excluded [Sin03].

In summary, the charge balance equation (2.5) simplifies to

$$Q_{\mathrm{surface}} = Q_{\mathrm{GaN}} + qn_{\mathrm{S}}. \tag{2.6}$$

This equation requires that $Q_{\text{surface}} > Q_{\text{GaN}}$, because the other remaining components are all negative. In principle, surface states can be either donor-like or acceptor-like [WHS89, Sch06], where

$$Q_{\text{surface}} = Q_{\text{donor-like}} - Q_{\text{acceptor-like}} > 0 \rightarrow Q_{\text{donor-like}} > Q_{\text{acceptor-like}}. \tag{2.7}$$

Conclusively, the surface states have to be dominantly donor-like in order to compensate the negative polarization charges and the 2DEG [IFN+00]. The formation of the 2DEG is not explained by the polarization itself, but by their local compensation with ionized surface donor states. In the ideal case of a defect free surface, the formation of the 2DEG could only be explained by the formation of a hole channel at the top of the AlGaN-layer, cf. also dicussion in 2.1.1.

2.2 III-N Based MIS-HEMT Devices

The fabrication of semiconductor devices rely on the availability of suitable semiconductor substrates (wafers). The availability of bulk GaN substrates is still limited and their costs are not competitive in comparison to other available substrate materials. Alternatively, pseudo-substrates were developed to overcome this issue [KH12,Sin03]. The most promising pseudo-substrate in terms of costs is the GaN-on-Si system [KH12]. GaN-on-Si wafers are available since the 1990s [KSZ+95] and the first devices based on GaN-on-Si wafers were implemented in the early 2000s [BBP+02]. Further, also other pseudo-substrates are available, e.g. based on SiC and sapphire [RR96, MKAS03]. An overview of material properties of common substrate materials is given in Table 2.1.

		GaN	Al_2O_3	SiC	Si (111)
lattice constant a	[nm]	3.19	4.75	3.08	5.43
lattice mismatch	[%]	0	49	-3.5	70
thermal expansion coefficient	[10^{-6} K^{-1}]	5.6	7.5	4.46	3.59
thermal mismatch	[%]	0	33.9	-20.3	-35.8
thermal conductivity	[W/cm K]	1.3	0.5	5	1.5
costs	[EUR/cm^2]	100	1	10	0.1
available wafer size	[inch]	2-3	8	4-6	12

Table 2.1: Comparison of material properties of substrates used for the expitaxial growth of GaN [RR96, MKAS03, KH12].

In Fig. 2.10 the schematics of a GaN heterostructure wafer on a supporting substrate is shown. The expitaxy of the (Al)GaN layers starts with a nucleation layer, followed by the growth of the buffer. For the design of the buffer, several conditions has to be considered, e.g. thermal and lattice mismatch, cf. Table 2.1. Moreover, the electrically active part of the device is located in the GaN buffer, directly below the AlGaN barrier. It has to be considered that the buffer has to sustain all applied biases in different operating conditions [BTEH+10, WBTB+11, IGBT+11]. The barrier layer, which is grown on top of the buffer, is used to induce the intrinsic 2DEG channel. This structure provides a crystallographic interface for the 2DEG. The pseudo-substrate provides the starting point for the device fabrication.

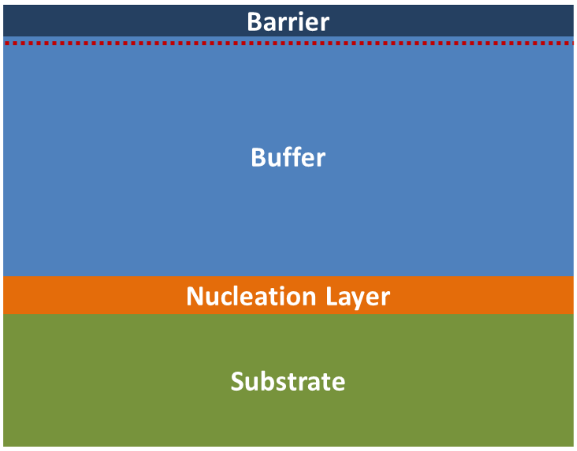


Figure 2.10: Epitaxial structure of a GaN-on-Substrate wafer, which is used for the fabrication of GaN based devices.

The schematics of a GaN based normally-on device is shown in Fig. 2.12. The AlGaN/-GaN heterostructure provides an intrinsic 2DEG transistor channel, offering high electron densities in the order of 10^{13} cm^{-2} [ASS+99] and mobilities in the order of 2000 cm^2/Vs at the same time (Table 2.1). Hence, the sheet resistance of the channel is in the order of 300 Ω/square. The channel region is unintentional doped (UID). The ohmic contacts, i.e. source and drain, are connecting the 2DEG to the outside. This structure is in contrast to the most Si-based power device concepts, where the active region of the device is vertically spanned between the top and bottom of the wafer. The gate contact is used to control the current flow between the ohmic contacts. The first GaN HEMTs were build using a Schottky gate [KBKO93], while the same group developed later also the first MIS-based HEMTs. They demonstrate variants with SiO_2 and Si_3N_4 as gate dielectric [KSY+03]. A passivation layer is used to suppress the charging of defect states at the AlGaN surface, which helps to prevent parasitic current collapse effects [VZKM01]. Usually, the transfer characterisitics of these devices show hysteresis and drift effects, if the gate bias exceeds to positive voltages [IMKK11, LOPP12, HYRC12, WMZ+13]. Intrinsically, these devices are normally-on, i.e. their threshold voltage V_{th} is negative. Despite solely normally-on devices are studied throughout this thesis, the experimental findings are also of importance for MIS-based normally-off devices, i.e. devices with a positive threshold voltage. The MIS-gate stack of a normally-on HEMT serves as vehicle to evaluate dielectrics for normally-off devices based on the same MIS-gate structure. This includes devices with recessed barrier layer [ON08, PSC+06, STK+06, IMKK11, CCC+11a, CCC+11b] and with fluorine implanted barrier [CZCL05]. Similar drifts, compared to normally-on MIS-HEMTs, are also found on devices with a fully-recessed barrier [CRJ+13]. The use of normally-on devices for our studies has the advantage that one does not have to deal with the additional processing complexity due to the barrier modifications. An alternative normally-off concept is based on p-n-junction gate contacts [UHU+07, IUTU13, Ued13], for which the results are not of relevance.

A design parameter of the barrier layer is the Al-content. The bandgap and band offsets for the $Al_xGa_{1-x}N$ system for varying Al-content from GaN to AlN are shown in Fig. 2.11 [AMM+02]. It can be seen that the bandgap increases from 3.4 eV to 6.1 eV with

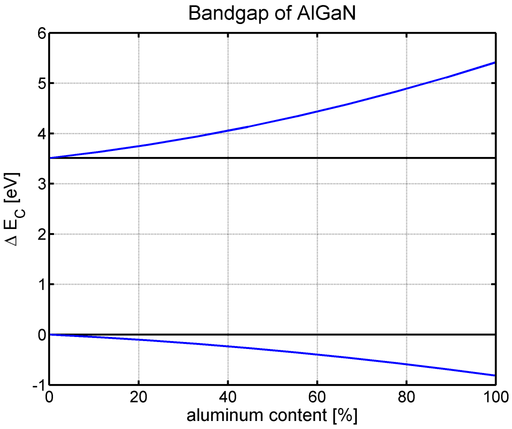


Figure 2.11: Bandgap and band offsets of AlGaN as a function of x varied between GaN ($x = 0$) and AlN ($x = 1$). The valence band maximum of GaN is taken as reference level [AMM+02].

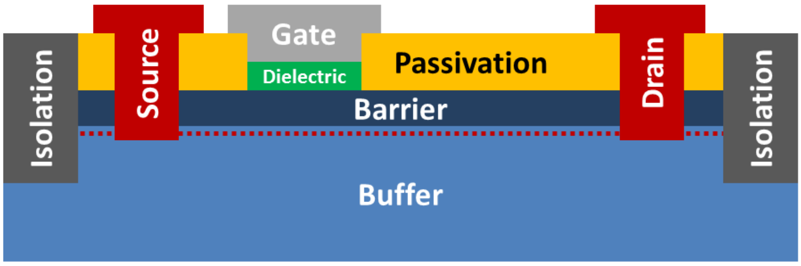


Figure 2.12: Schematics of a normally-on MIS-HEMT device build on top of a GaN-on-Si wafer.

increasing Al-content x. Although, up to now only simple barrier structures formed by a single AlGaN layer are considered, the barrier structure can be also more complex. An AlN liner is often grown on top of the buffer below the AlGaN layer to improve the channel mobility. Optionally, the AlGaN layer can be terminated by an additional GaN or AlN cap layer [SCM+01]. The cap layer has an influence on the surface structure and on the oxidation of the surface, as well as on the interface to the dielectric layer [MWdW10]. A dielectric on top of the barrier is used to significantly reduce the gate leakage current [KSY+03]. It enables a high impedance gate contact, which simplifies the design of the gate driver circuitry [Bal08]. More details about dielectrics on III-N layers are found in section 2.3.2.

2.3 Gate Dielectrics for III-N Based Devices

This thesis deals with the characterization of the gate stack of GaN based MIS-HEMTs, with a focus on the dielectric/III-N barrier interface. This section starts with a review of the work done on the SiO_2/Si interface over the last five decades, because it is intended to serve as a role model for dielectric/semiconductor interfaces in general. A lot of effort was made on the processing and the characterization of SiO_2 dielectrics on top of Si. In the following, a discussion about the current understanding of the dielectric/III-N interface including a literature review is made.

2.3.1 Review of the SiO_2/Si System

In this section, the historically evolvement of the SiO_2 is taken as role-model to understand the prerequisites for the processing of a high quality dielectric on top of a semiconductor. The first working MOSFET was invented in 1960 by Kahng and Atalla [KA60]. The gate contact included a thermally grown SiO_2 on top of a Si substrate as insulating layer [Jae01]. The MOSFET enabled in the following the triumpf of highly integrated circuit technologies. Since the 1970s, MOSFETs also gained interest for power switching applications [Bal08] and are in the meantime the dominating device concept for low to medium voltage applications. Moreover, the SiO_2/Si interface is also a key element of the IGBT, which was invented in the 1980s [Bal08], and therefore is nowadays also an important building block of devices for high power switching applications. Nevertheless, the dominance of Si in the semiconductor business is owed to the possibility of processing a high-quality dielectric on top of Si, where the interface has a low density of electrically active interface states. The origin of these states is clearified in the following.

The lattice mismatch between crystalline Si and amorphous SiO_2 causes unsaturated Si-bonds at the interface between this two materials [HP94]. The upper limit for the density of interface states, i.e. dangling Si bonds, is the density of Si surface atoms, which is given by 6.78 10^{14} cm^{-2} and 11.76 10^{14} cm^{-2} for for Si (100) and (111) surfaces, respectively [KAWUM02, Lig61]. ESR studies revealed an actual interface state density in the order of 10^{13} cm^{-2}, which is about two decades smaller than the upper limit [SNA98, Ste93]. This means that every 100th Si surface atom is not bound to the overlying SiO_2. These dangling Si bonds can be effectively passivated in a H atmosphere at temperatures between 400 °C and 600 °C [KKP$^+$00]. Under optimized process condictions in a forming gas atmosphere (mixture of N and H), the number of interface defects can be further reduced down to 10^9 cm^{-2}, which is four order of magnitude compared to the ESR measured values of 10^{13} cm^{-2} [PC1]. This means that 99.99% of all dangling bonds can be passivated by optimized annealing conditions, or in other words every 10^6 Si atom is not bound to an atom of the dielectric in this case.

The proper cleaning of the Si surface prior to oxide grow is an further critical step, which ideally removes all foreign species and contaminations from the surface leaving a clean surface behind. It is well known that the native oxide layer on top of a Si substrate can be removed by a HF solution [KP70, Ker90, IKMO93]. A similar cleaning procedure is not yet established for the cleaning of III-N surfaces.

However, the SiO_2/Si interface is the best investigated interface between a dielectric and a semiconductor. Fig. 2.13 sketches the current understanding of the interfacial region in SiO_2/Si [HP94]. Three different regions can be identified. In the near-interface Si region the Si atoms show a significant perturbation from their expected positions in the bulk region. This region is followed by a transition region of non-stoichiometry, which extends over 0.2-0.3 nm. Also in the stoichiometric near-interface SiO_2 region, the properties of the SiO_2 are different from the bulk region. Especially the non-stochiometric SiO_x region is in the focus of interest. Defects in this region are controversely discussed as root cause for the bias temperature instabiliy (BTI) of SiO_2/Si based devices [Gra12]. BTI is triggered by the application of positive or negative voltage at the gate with respect to all other terminals of a MOSFET at elevated temperatures in the range of 50 °Cto 200 °C. The mechanism is temperature activated, where the magnitude of the degradation is increasing with temperature. It leads to a shift of the threshold voltage and a reduction of the channel

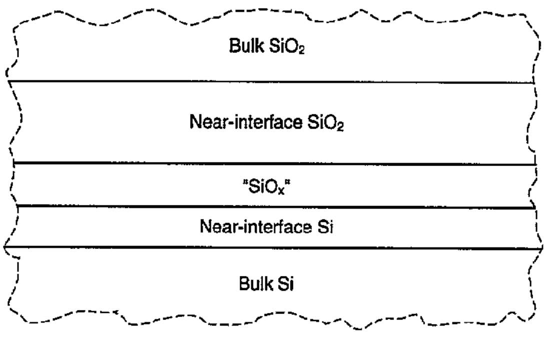


Figure 2.13: Schematics of the near interfacial regions at the SiO_2/Si interface [HP94].

mobility [GN66, MM66]. This is mentioned, because V_{th} drifts in GaN based MIS-HEMTs show some similarities to BTI in Si based MOSFETs [LRPO14].

Beside a low interface state density, a gate dielectric must have sufficient band offsets with regard to the semiconductor conduction and valence band in order to confine charge carrieres (i.e. electrons and holes) in the channel and to enable a low gate leakage current level [SN07]. In addition, the dielectric have to sustain the applied electric field strengths without dielectric breakdown within the targeted lifetime of the device [McP10].

In conclusion, the knowledge on producing high quality dielectrics and dielectric/semiconductor interfaces is of key importance for the entire semiconductor industry. But the fabrication of dielectrics on materials other than Si is still challeging [RFG$^+$12, RFG$^+$14].

2.3.2 Dielectrics On III-N Layers

In this section, the state-of-the-art of dielectrics on III-N barrier layers is reviewed. Further, the oxidation of (Al)GaN surfaces and their preparation are discussed. Despite an insulated gate contact would be strongly desired [KSY$^+$03], a main problem of the AlGaN/GaN MIS-HEMT devices is still that these devices show significant threshold voltage drift effects when the gate contact is forward biased. This is assigned to a high number of defect states at the dielectric/III-N interface [IMKK11, HYRC12, WMZ$^+$13, CRJ$^+$13].

The density of (001) surface atoms of GaN and AlN gives an upper boundary for the density of interface defect states, which is 1.13 10^{15} cm^{-2} and 1.19 10^{15} cm^{-2}, respectively [AMM$^+$02]. The interface donor state density is in the order of 10^{13} cm^{-2}, which is in the order of dangling bonds observed in SiO_2/Si. Nevertheless, a high number of defect states at the dielectric/III-N interface is considered for the creation of the 2DEG channel [IFN$^+$00, GMC$^+$10, MWdW10]. The question is, if this states are also related to the observed V_{th}-drifts. In principle, the V_{th} drifts can also be due to acceptor-like interface states energetically located above the donor-like states [SN07, Sch06, WHS89] or border traps in the dielectric [FSW$^+$95, FWRR98, Sch09, Gra12]. The situation differs for normally-off structures, where no 2DEG is induced below the gate. But also on barrier-less normally-off structures tremendous V_{th} drifts are reported [CRJ$^+$13], which indicates that the surface donor states and the V_{th} drifts might not be correlated. In [GVL$^+$11] the number of donor states at the Al_2O_3/AlN interface is estimated to be as high as 6 10^{13} cm^2.

Thermally grown oxides are not considered as gate dielectrics for III-N based devices. The reasons are discussed in the following. It is well known that the (Al)GaN surface is prone to oxidation [Ber96,WWG99,DFN06a,DFN06b] and a native Ga_2O_3 is formed on top of a GaN layer, while the native oxide on an AlN layer is Al_2O_3 [MWdW10]. In the case of a AlGaN surface, the native oxide is expected to be a mixture of Al_2O_3 and Ga_2O_3. Although, the thermal oxidation of the GaN surface was demonstrated [WMH+05], its suitability as gate oxide is very questionable. In [DFN06a, DFN06b] it is stated that the oxidized GaN surface have a bandgap similar to bulk GaN with a good band alignment. However, the bandgap of bulk Ga_2O_3 is reported to be in the range of 4.4 - 4.8, with a conduction bandoffset of 0.5 eV to on GaN [RF06, DFN06a]. This might be not sufficient in order to suppress gate leakage currents. Therefore thermally grown Ga_2O_3 is most probably not a proper candidate for a gate dielectric. A further drawback might be that the oxidation is not uniform, but a preferential oxidation of threading dislocations is observed [WMH+05]. A thermal oxidation process always consumes part of the oxidized material. While in Si the bulk material is usually oxidized, which allows the growth of oxides of practically any thickness, the thickness of the barrier layer in a III-N heterostructure is limited due to build-in stress. This is especially of concern for AlN top layers, which could in principle be thermally oxidized. A solution would be to create a proper interface layer of thermally oxidized AlN and a deposited dielectric. However, a feasible solution is not yet reported.

An alternative to thermally grown oxides are deposited dielectric layers. This include the deposition of several different kind of oxides and nitrides. Practically, dielectrics for GaN based MIS-HEMTs are always deposited. Nevertheless, the surface has to be prepared prior to deposition, e.g. native oxides has to be removed to get a clean surface. The complete removal of oxygen contaminants from GaN surfaces is quite challeging from point of view of cleaning processes. Furthermore, also the detection of oxygen impurities is challenging, where an incomplete removal of oxygen from the surface results in an unintential interlayer of Ga_2O_3 between the III-N surface and the deposited dielectric [GUKM09]. However, there is still a lack of knowledge about the physical and chemical properties of the dielectric/III-N interface and the improvement of cleaning sequences prior to deposition is an unsolved issue.

In contrast to Si, in GaN there is currently no possibility to get a thermally grown oxide with a low density of electrically active interface defect states. This opens up a wide range of dielectrics, which can be deposited on top of the III-N barrier layer. Devices with HfO2 [FPTB+12], Al2O3 [CCC+11a,CCC+11b,YTW+13,LLH+13,CRJ+13] and SiO2 [LSP+13a, LRPO14, LPO14] as gate oxide are reported in literature. Moreover, also AlN [RFG+14, SKS12] and Si_3N_4 [CRJ+13] are used as gate dielectrics. In Fig. 2.14 the band offsets for a selection of high-k oxides is shown. For Si_3N_4 a conduction band offset to GaN of 1.3 eV is reported [RF06]. In conclusion, several development steps were necessary to establish a stable and reliable process for the SiO_2/Si interface, i.e. cleaning of the surface and annealing of dangling bonds at the interface. For GaN based devices, this two issues are not yet solved and further the choice of the dielectric material itself gives an additional degree of freedom.

In fact, the reported D_{it} values are in the range of 10^{12} cm^{-2} to 10^{13} cm^{-2}, which is similar to the defect density in non-annelead SiO_2/Si samples [SNA98, Ste93]. In addition, defects at this interface do not degrade the mobility as observed in SiO_2/Si devices [KGR+08], which is further indicated by the pure parallel shift of the transfer characteristic [LOPP12].

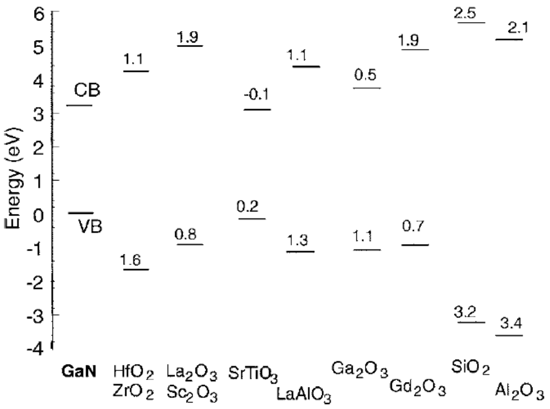


Figure 2.14: Band alignment of various oxides to GaN [RF06].

Chapter 3

Methodology

In this chapter, the general approach of this thesis work is reviewed. To put it in the nutshell, this work focus on understanding the physics and limitations of insulated gate contacts for GaN based HEMTs, where the magnitude of ΔV_{th} over device lifetime is limited to an acceptable value. In this context, ΔV_{th} is the critical parameter and hence a direct time-resolved measurement of ΔV_{th} recovery after forward gate bias stress is choosen as a measurement tool. Moreover, the correlations between ΔV_{th} and the sample parameters (e.g. thickness of the dielectric and barrier layer, dielectric material, etc.) are of interest.

3.1 General Approach

The time-resolved measurement of ΔV_{th} allows a direct comparison of the measurement data between different test samples, because V_{th} is independent of the lateral device dimensions, i.e. gate length and gate width. It depends on the layer thicknesses of the dielectric and the barrier and on the density of positively charged interface states [GVL$^+$11]. Details about time-resolved ΔV_{th} measurements are found in Section 3.2. In this section, the general approach of this thesis is discussed. An overview of a typical learning cycle is shown in Fig. 3.1, where the typical steps are summarized as follows:

- fabrication of test samples (variation of sample parameters)
- stress/reocvery experiments for a systematic scan of the dependency of ΔV_{th} on $V_{\mathrm{G,stress}}$ and t_{s} (i.e. the test parameters)
- collection and preparation of the measurement data
- interpretation and modeling (find relation between ΔV_{th} (output parameter) and the input parameters(sample parameters and stress parameters)

The learning of one cycle is used as input for the subsequent cycle. One distinguishes between sample (layer thicknesses, dielectric materials, etc.) and test parameters (stress bias, stress time, etc.). The output parameter is always the V_{th} drift. The first studies (cf. Chapter 4.3) are performed by varying only the test parameters ($V_{\mathrm{G,stress}}$ and t_{s}) on a single test sample. The parameter space is later extended by variations of sample parameters to study the relations between ΔV_{th}, sample parameters and stress parameters (cf. Chapter 4.9). An outlook on extending the test parameter space towards variation of

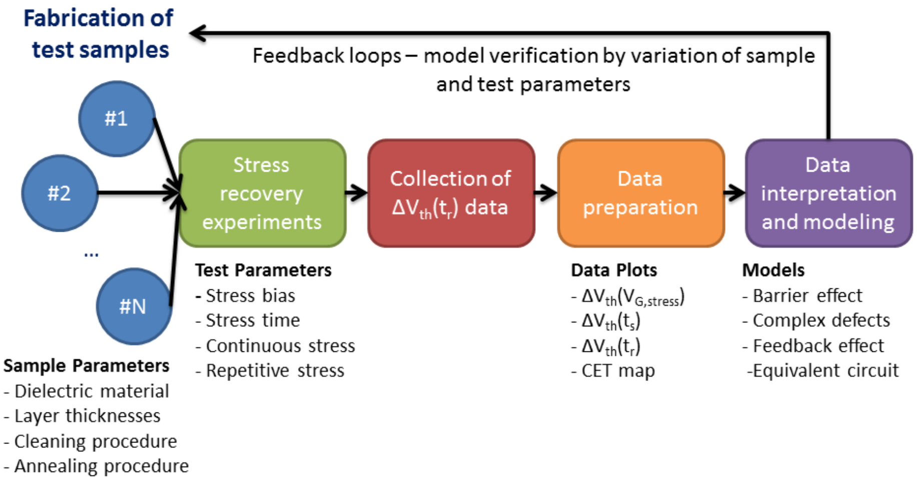

Fabrication of test samples
Feedback loops – model verification by variation of sample and test parameters
#1
#2
...
#N
Stress recovery experiments
Collection of ΔV_th(t_r) data
Data preparation
Data interpretation and modeling
Test Parameters
- Stress bias
- Stress time
- Continuous stress
- Repetitive stress
Data Plots
- ΔV_th(V_G,stress)
- ΔV_th(t_s)
- ΔV_th(t_r)
- CET map
Models
- Barrier effect
- Complex defects
- Feedback effect
-Equivalent circuit
Sample Parameters
- Dielectric material
- Layer thicknesses
- Cleaning procedure
- Annealing procedure

Figure 3.1: Overview of a typical learning cycle. The stress/recovery experiments are based on time-resolved measurements of the ΔV_{th} recovery after forward gate bias stress pulses.

T is given in Chapter 5. The interpretation and modeling is founded on existing knowledge of state-of-the art BTI research on Si based devices (cf. Chapter 4.6).

3.2 Time-Resolved ΔV_{th} Measurements

The measurement of the V_{th} drift induced by forward gate bias stress [IMKK11, HYRC12, WMZ^{+}13, CRJ^{+}13] is a direct way to examine the impact of gate stress bias and stress time on the V_{th}, which is a critical device parameter. The direct measurement of V_{th} drift offers an easy and straightforward interpretation of the measurement results. Further it has the advantage that it can be easily implemented on standard measurement equipment. Details about the implementation of such measurements are given in Appendix A.

The most basic way to determine ΔV_{th} is to measure the transfer characterisitc $I_{\mathrm{D}}(V_{\mathrm{G}})$ before and after a certain forward gate bias stress pulse, which is applied for a certain stress time, and extract the ΔV_{th} out of the measured $I_{\mathrm{D}}(V_{\mathrm{G}})$-curves before and after stress. In principle, this can be extended to a time resolved-measurent of ΔV_{th} recovery by repetitive measurement of the $I_{\mathrm{D}}(V_{\mathrm{G}})$ characteristics after the stress pulse for a certain recovery time. This method has the disadvantage that the minimum delay time between the end of the stress pulse and the acquisition of the first measurement point t_{delay} is in the range of several seconds. It is advantageous to minimize t_{delay}, because the information for recovery times $t_{\mathrm{r}} < t_{\mathrm{delay}}$ is lost.

The idea is to take the measurement of the transfer characteristic $I_{\mathrm{D}}(V_{\mathrm{G}})$ as a starting point. An $I_{\mathrm{D}}(V_{\mathrm{G}})$-measurement is performed at a constant drain bias V_{D}, while the gate bias V_{G} is sweeped in discrete steps, cf. Fig. 3.2. The measurement time is defined by the number of sweep points and by the integration time per sweep point. Hence a straightforward way to minimize the measurement time is to minimize the number of sweep points and to reduce the integration time per point. The most minimalistic way, of measuring $I_{\mathrm{D}}(V_{\mathrm{G}})$, is to measure I_{D} at one single measurement point $V_{\mathrm{G,meas}}$, which offers the minimal possible delay time t_{delay}. Since a parallel drift of the transfer characteristics $I_{\mathrm{D}}(V_{\mathrm{G}})$ after forward gate bias

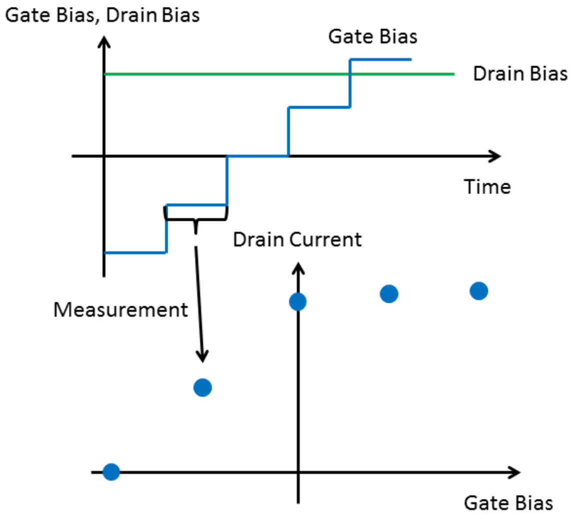


Figure 3.2: Top: Gate and drain bias signals during the measurement of the transfer-characteristics. Bottom: the transfer characterisitics is measured at discrete gate bias levels, where each drain current point is integrated over a certain integration time.

stress is observed (Fig. 3.3), this is feasible to speed up the measurement. Moreover, this method is already well-established to study V_{th} drifts in $\mathrm{SiO_2}$/Si based devices [KGR$^+$08]. In Fig. 3.4, the basic schematics of the time-resolved ΔV_{th}-measurement is shown. The parallel drift of the transfer characterisitics is monitored at a single bias point $V_{\mathrm{G}} = V_{\mathrm{G,meas}}$, where the transient drain current signal $I_{\mathrm{D}}(t)$ is recorded. In a post-processing step, the transient drain current signal $I_{\mathrm{D}}(t)$ is transformed to a transient $\Delta V_{\mathrm{th}}(t)$ signal by simple mapping to the initial $I_{\mathrm{D}}(V_{\mathrm{G}})$-characteristics, which is recored before stress. In Fig. 3.4, the extraction of ΔV_{th} from the transient drain current signal is sketched. An advantage of GaN based MIS-HEMTs is that the do not suffer from mobility degradation after forward gate bias stress [LOPP12, LRPO14], which is in contrast to $\mathrm{SiO_2}$/Si based MOS devices.

In this thesis, all investigation are done on normally-on devices. They have the advantage that during $V_{\mathrm{G}} > 0$ stress, the 2DEG acts as a counterelectrode to the gate electrode as illustrated in Fig. 3.5. During stress the field distribution is totally homogenous, because drain and source electrodes are grounded. The recovery of ΔV_{th} is studied after pulses of varying stress bias and time as shown in Fig. 3.6. The $I_{\mathrm{D}}(t)$ signal is monitored after forward gate bias stress at a single bias point, which enables a fast measurement response, i.e. a short delay time t_{delay}. The $I_{\mathrm{D}}(t)$ signal is directly mapped to a $\Delta V_{\mathrm{th}}(t)$ signal, which enabels a time-resolved measurement of ΔV_{th} after forward gate bias stress pulses with magnitude $V_{\mathrm{G,stress}}$ and duration t_{s}. This method is simple but powerful, because it offers the possibility to study the impact of $V_{\mathrm{G,stress}}$ and t_{s} in a very systematic way. Further, it offers a straightforward interpretation of the measurement result and it gives directly the change of a critical device parameter. Therefore it is close to operating conditions of the device. A further advantage is that the measurement itself does not need time-consuming preparation or complex test conditions and hence offers a fast response as soon as test material is available. It enables the screening of a huge number of wafers. Moreover, the method is sensitiv to changes of the charge state of interface defect states, since ΔV_{th} can be correlated to the

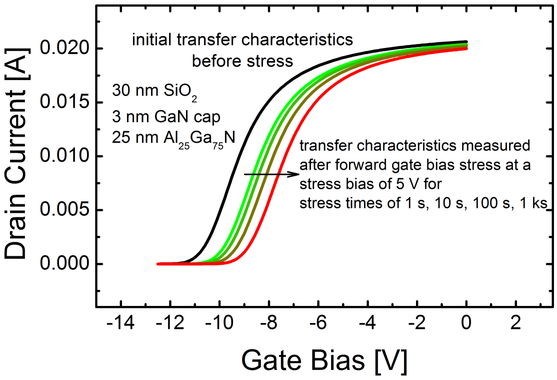


Figure 3.3: Drift of the threshold voltage after forward gate bias stress for logarithmically increasing stress time at a constant stress bias of 5 V. The transfer characterisitics is recorded at a drain bias of 1V, initially before stress and then after each stress pulse.

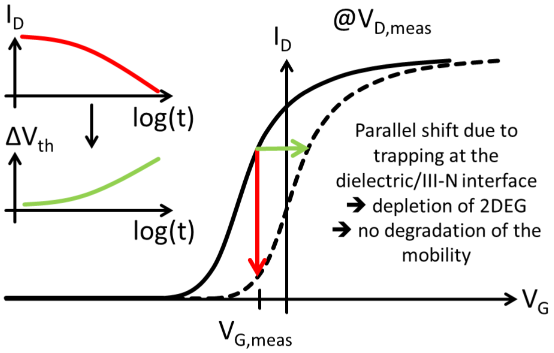

I_D
log(t)
ΔV_{th}
log(t)
I_D
@$V_{D,meas}$
Parallel shift due to trapping at the dielectric/III-N interface
➔ depletion of 2DEG
➔ no degradation of the mobility
V_G
$V_{G,meas}$

Figure 3.4: Schematics of the ΔV_{th} measurement used in this work. The drain current is monitored at a constant gate bias $V_{\mathrm{G}} = V_{\mathrm{G,meas}}$. Due to the parallel shift of the transfer characteristics, it is possible to map the transient I_{D} signal to the initial transfer curve to calculate the according ΔV_{th} signal.

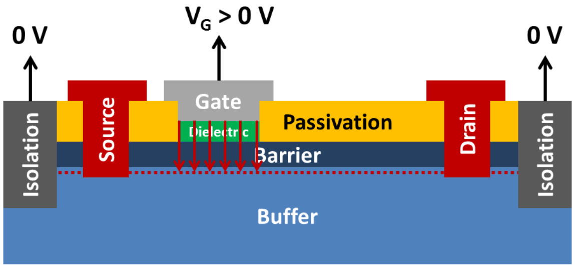


Figure 3.5: Schematics of the field distribution in a GaN MIS-HEMT device during forward gate bias stress. The intrinsic 2DEG channel acts as counter-elecrode to the gate electrode and hence the field is homogenously distributed between gate electrode and 2DEG channel.

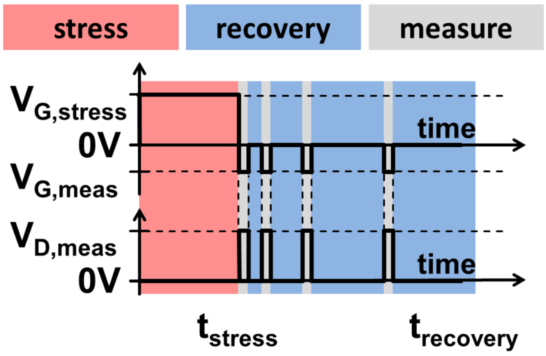


Figure 3.6: Signal pattern of a stress-recovery cycle. The gate is biased at $V_{\mathrm{G}} = V_{\mathrm{G,stress}} > 0$ for a certain stress time t_{s}. After the stress pulse, the gate signal is switched to $V_{\mathrm{G}} = V_{\mathrm{G,meas}}$ and the drain current is measured. In between the measurement points, the device is switched to recovery conditions, where all device terminals are grounded.

density of trapped charges ΔN_{it} via the dielectric capacitance [LOPP12, LSR+14].

Since in general, the V_{th} drift does not fully recovery within the measurement time. A new device for each combination of stress bias $V_{\mathrm{G,stress}}$ and stress time t_{s} can be used to ensure defined initial conditions. Fortunately, it is possible to use a new device per stress bias $V_{\mathrm{G,stress}}$ under the condition of logarithmically increasing stress time t_{s}. An comparison is given in Fig. 3.7.

The advantages of time-resolved ΔV_{th} measurements are summarized as follows:

- fast measurement execution with a low experimental effort
- automated measurements possible
- reliable, comparable and reproducable
- scalable, because the stress conditions can be easily increased ($V_{\mathrm{G,stress}}$ and t_{s})
- directy sensing of a device parameter (easy interpretation of the measurement result)

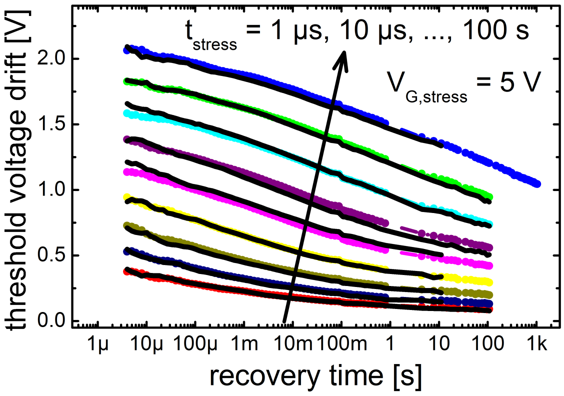


Figure 3.7: Comparison of ΔV_{th} for constant stress bias and logarithmically increased stress time. The coloured lines are recorded on a single device, whereas the black lines are each recorded on a virgin device. The tests are performed on devices with a 30 nm SiO_2 dielectric on top of a barrier layer with a 3 nm GaN cap and 25 nm $Al_{25}Ga_{75}N$ layer.

- sensitive to changes of the charge state of interface states

Chapter 4

Scientific Articles

4.1 Summary of the Scientific Articles

This section gives a summary of all first-author scientific contributions.

Towards understanding the Origin of Threshold Voltage Instability of AlGaN/-GaN MIS-HEMTs

Authors	P. Lagger, C. Ostermaier, G. Pobegen and D. Pogany
Published In	Proceedings of the IEEE International Electron Device Meeting
Year	2012
Pages	13.1.1 - 13.1.4
Conference Location	San Francisco, California, United States of America
Presentation	Oral Presentation

This work includes the first systematic study on forward gate bias induced V_{th} drifts (ΔV_{th}) of GaN based MIS-HEMTs based on the time-resolved measurement of ΔV_{th} recovery after stress pulses with stress biases up to 6 V and stress times ranging from 100 ms up to 1 ks. A broad distribution of stress and recovery time constants is found, as well as a scaling of ΔV_{th} with the applied stress bias. The observed recovery time constant range from 20 ms to 1 Ms. The data is analyzed using the approach of capture emssion time (CET) maps known from bias temperature instability (BTI) reasearch in Si based MOS-devices. It is found that capture and emission from independent defect states can occur at the same time. This first study was done on devices with a Al_2O_3 gate dielectrics.

New Insights on Forward Gate Bias Induced Threshold Voltage Instabilities of GaN-Based MIS-HEMTs

Authors	P. Lagger, A. Schiffmann, G. Pobegen, D. Pogany and C. Ostermaier
Published In	Proceedings of the Workshop on Compound Seminconductor Devices and Integrated Circuits
Year	2013
Pages	161 - 162
Conference Location	Warenemünde, Germany
Presentation	Oral Presentation

In this abstract, a broad distribution of stress and recovery time constants on devices with a SiO_2 gate dielectrics, similar than before for Al_2O_3 based devices, is reported. The concept of active energy region is introduced and the role of the barrier for the overall capture dynamics is discussed.

Very Fast Dynamics of Threshold Voltage Drifts in GaN based MIS-HEMTs

Authors	P. Lagger, A. Schiffmann, G. Pobegen, D. Pogany and C. Ostermaier
Published In	IEEE Electron Device Letters
Year	2013
Volume	34
Issue	9
Pages	1112-1114

In this paper, an improved measurement setup based on an oscilloscope and a pulse-generator is presented. It enables the application of very short stress times (100 ns). Furthermore, the delay time between the measurement of the transient signal of ΔV_{th} after the forward gate bias stress pulse is improved by approximately four orders of magnitude. The broad distribution of recovery time constants in Al_2O_3 based devices is found to span from below 1 μs up to 1 Ms. A first study on repetitive stress with a series of repetitive stress pulses with a stress time of 100 ns and a recovery time of 100 μs in between each pulse is performed. Already under these conditions, a significant V_{th} drift with increasing number of stress pulses is observed. The findings clearly indicate that high frequency capacitance voltage measurements (HF-CV) for positive biases are influenced by V_{th} drifts, which means that during forward gate bias stress there is no quasi-equilibrium between 2DEG channel and dielectric/III-N interface established. But this would be required for a HF-CV measurement. These findings are further of relevance for normally-on devices, which are usually operated only up to gate biases of 0 V, where no V_{th} drifts are observed. Nevertheless, repetitive positive gate voltage spikes can occur in these devices during switchting the device from off-state to on-state.

Comprehensive Study of the Complex Dynamics of Forward Bias Induced Threshold Voltage Drifts in GaN Based MIS-HEMTs by Stress/Recovery Experiments

Authors	P. Lagger, M. Reiner, D. Pogany and C. Ostermaier
Published In	IEEE Transaction on Electron Devices
Year	2014
Volume	61
Issue	4
Pages	1022-1030

A comprehensive study on the stress bias and stress time dependency of ΔV_{th} is made in this journal contribution. It is revealed that the curvature of the recovery curves changes independently of the stress bias from concave to convex for increasing stress time. Moreover, a first experimental evidence for the contribution of the barrier layer to the overall capture time is found. Further, significant negative entries in the CET map are observed, which indicates that the observed data cannot be explained by simple first-order defect kinetics. A comprehensive discussion of physical defect processes, including tunneling to border states, lattice relaxation effects and trapping at multi-state defects, is made and a feedback mechanism due to Coulomb charging is proposed.

Enhancement of V_{th} Drift for Repetitive Gate Stress Pulses due to Charge Feedback Effect in GaN MIS-HEMTs

Authors	P. Lagger, D. Pogany and C. Ostermaier
Published In	Proceedings of the IEEE International Reliability Physics Symposium
Year	2014
Pages	6C.3.1 - 6C.3.6
Conference Location	Waikoloa, Hawaii, United States of America
Presentation	Oral Presentation

This abstract includes a systematic investigation of the impact of repetitive stress on forward gate bias induced V_{th} drifts. It is found that ΔV_{th} after repetitive stress pulses is enhanced compared to a single stress pulse with the same total stress time. A dependency of this behavior on the intermediate recovery time in between the individual repetitive stress pulses is observed. The behavior is related to a charge feedback effect during $V_{\mathrm{G}} > 0$.

Understanding the Fundamental Limitations for the Improvement of Forward Gate Bias Induced V_{th} Drift Stability of GaN Based MIS-HEMTs

Authors	P. Lagger, M. Reiner, G. Denifl, M. Stadtmüller, D. Pogany and C. Ostermaier
Presented At	International Workshop on Nitride Semiconductors
Year	2014
Conference Location	Wroclaw, Poland
Presentation	Oral Presentation

A first report on the influence of layer thicknesses and dielectric constant on ΔV_{th} is given in this abstract, where a strong influence of ΔV_{th} on the layer thicknesses is found. Moreover, it is reported that the extracted density of trapped charges scales with the dielectric constant for the same stress-recovery conditions.

Role of the Dielectric for the Charging Dynamics of the Dielectric/Barrier Interface in AlGaN/GaN based Metal-Insulator-Seminconductor Structures under Forward Gate Bias Stress

Authors	P. Lagger, P. Steinschifter, M. Reiner, M. Stadtmüller, G. Denifl, A. Naumann, J. Müller, L. Wilde, D. Pogany and C. Ostermaier
Published In	Applied Physics Letters
Year	2014
Volume	105
Issue	3
Pages	033512-1 - 033512-5

In this journal paper, a comprehensive study on different dielectric materials, as well as varying dielectric thickness t_{D} and barrier thickness t_{B} is performed using capacitance-voltage analysis. It is revealed that the density of trapped electrons, ΔN_{it}, scales with the dielectric capacitance under spill-over conditions, i.e. the accumulation of a second electron channel at the dielectric/AlGaN barrier interface. Hence, the maximum density of trapped electrons is defined by the charging of the dielectric capacitance. The scaling behavior of ΔN_{it} is explained universally by the density of accumulated electrons at the dielectric/III-N interface under spill-over conditions. It is proposed that the spill-over voltage, i.e. the gate bias at which a carrier accumulation at the interface occurs, is defined by the barrier height for electron transport from the 2DEG channel to the diectric/III-N interface and the capacitive voltage divider given by the dielectric and barrier capacitance. We conclude that the overall density of interface defects is higher than what can be electrically measured, due to limits set by dielectric breakdown.

4.2 Other Scientific Contributions

- K. Rupp, P. Lagger, T. Grasser, and A. Jüngel, "Inclusion of carrier-carrier-scattering into arbitrary-order spherical harmonics expansion of the Boltzmann transport equation", Proceedings of the IEEE International Workshop on Computational Electronics, 2012, p. 1-4
- C. Ostermaier, P. Lagger, M. Alomari, P. Herfurth, D. Maier, A. Alexewicz, M.-A. di Forte-Poisson, S. L. Delage, G. Strasser, D. Pogany, E. Kohn, "Reliability investigation of the degradation of the surface passivation of InAlN/GaN HEMTs using a dual gate structure", Microelctronics Reliability, 2012, Vol. 52, p. 1812-1815
- C. Ostermaier, P. Lagger, M. Reiner, G. Pobegen, D. Pogany, "Is PBTI at the

dielectric/III-N interface limited by interface traps?", Talk at the Workshop on Compound Semiconductor Materials and Devices 2014

- M. Cappriotti, P. Lagger, C. Fleury, R. Stradiotto, M. Oposich, C. Ostermaier, G. Strasser, D. Pogany, "Effect of III-N Barrier Resistance on CV Characteristic in GaN-based MOSHEMTs in Spill-Over Regime", Proceedings of the International Workshop on Nitride Semiconductors, 2014

4.3 Towards understanding the Origin of Threshold Voltage Instability of AlGaN/GaN MIS-HEMTs

Authors	P. Lagger, C. Ostermaier, G. Pobegen and D. Pogany
Published In	Proceedings of the IEEE International Electron Device Meeting
Year	2012
Pages	13.1.1 - 13.1.4
Conference Location	San Francisco, California, United States of America
Presentation	Oral Presentation

Student Paper

Towards Understanding the Origin of Threshold Voltage Instability of AlGaN/GaN MIS-HEMTs

Peter Lagger[1,*], Clemens Ostermaier[1], Gregor Pobegen[2], Dionyz Pogany[3]

[1]Infineon Technologies Austria AG, Siemensstraße 2, A-9500 Villach, Austria [2]KAI GmbH, Europastraße 8, A-9524 Villach, Austria [3]Institute for Solid State Electronics, Vienna University of Technology, Floragasse 7, A-1040 Vienna, Austria

Abstract

GaN-power HEMTs with insulated gate structure suffer from threshold voltage drifts (ΔV_{th}) under forward gate bias stress. We present a systematical approach to characterize the phenomenon and understand the dominant physical mechanisms causing this effect. We found out that ΔV_{th} is caused by traps with a broad distribution of trapping and emission time constants. This distribution is analyzed using so called Capture Emission Time (CET) maps known from the study of bias temperature instability (BTI) in CMOS devices. Physical models, which could explain the broad distribution of time constants, are discussed.

Introduction

High efficient GaN-based high electron mobility transistors (HEMTs) for power applications require an insulated gate structure in order to suppress parasitic gate leakage currents. In such MIS-HEMTs, in contrast to Schottky devices, a drift of the threshold voltage under forward gate bias is an often observed but rarely investigated phenomenon and usually related to trapping at the dielectric/III-N interface [1]. Previous investigations of this interface based on photoassisted CV-measurements [2], admittance measurements [3] or DTLS-like measurements [4] are mainly focusing on determining the interface trap density. We present a detailed physical analysis of the trapping and detrapping phenomena at the dielectric/III-N interface responsible for threshold voltage instabilities of GaN MIS-HEMTs. The investigation of threshold voltage transients over five decades of time and analysis of its bias and temperature dependency suggests a broad distribution of trap time constants with similar tendencies as known from the bias temperature instability (BTI) phenomena on silicon MOS devices [5,6]. Our results reveal the dominant mechanism responsible for threshold voltage drift offering a tool for a systematical improvement of the gate bias overdrive stability.

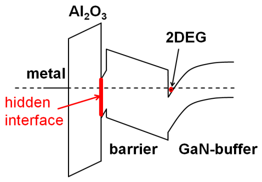


Fig 1. Band diagram showing the spatial separation of channel electrons from the “hidden” interface between gate oxide and GaN cap on top of the AlGaN barrier.

Devices & Experiments

Devices were fabricated on 4 inch GaN-on-SiC substrates with a gate length of 2 µm and a gate width of 200 µm. The barrier layer of the HEMT structure consisted of a 3 nm GaN cap and a 25 nm $Al_{0.25}Ga_{0.75}N$ layer (Fig. 1). The gate dielectric was provided using a 20 nm ALD-deposited aluminum oxide with an additional annealing step at 650°C. All characterizations have been carried out on an automated Keithley SCS 4200 system using consecutive stress and recovery sequences (Fig. 2a). Monitoring of the device threshold voltage drift ΔV_{th} is done at a single bias point ($V_{g,meas}$, $V_{d,meas}$) in the linear region of the transfer characteristic, where the drain current degradation and the threshold voltage shift can be correlated. This enables to measure also fast transient responses of ΔV_{th} (Fig. 2b). The threshold voltage drift is monitored during both, stress and recovery sequences. There is a delay of about 20ms between the end of the stress pulse and the first measured value of ΔV_{th}. During this delay there is already a recovery, which cannot be measured. Forward bias stress is applied to the gate contact, while drain and source are grounded. In

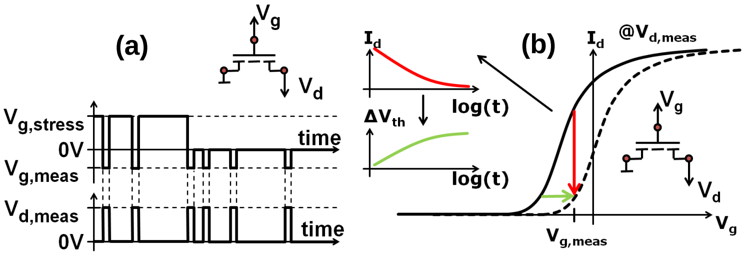


Fig 2 (a) Measurement scheme of a single stress-recovery sequence used to monitor ΔV_{th}. (b) Correlation between drain current degradation and ΔV_{th}. The bias point ($V_{g,meas}$,$V_{d,meas}$ = 5 V) is in the linear region of the transfer characteristic.

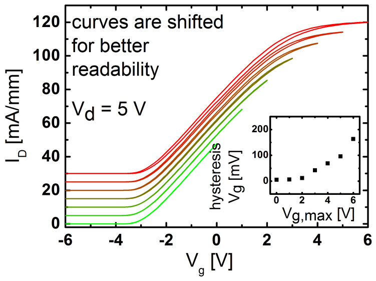


Fig 3. Consecutive transfer characteristics with increasing maximum gate bias $V_{g,max}$. The observed hysteresis starts at around 2 V and increases with $V_{g,max}$ (inset).

*corresponding author: E-mail: peter.lagger@infineon.com, Phone: +43 5 1777 6520, Fax: +43 5 1777 3212

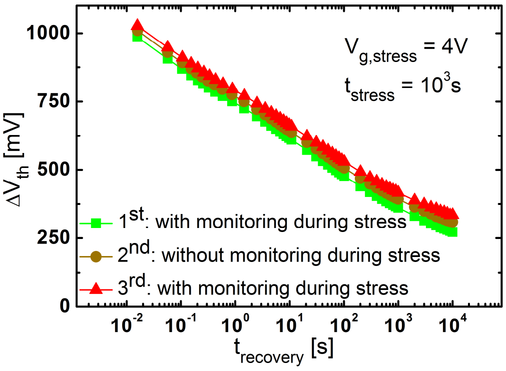


Fig 4 Recovery traces of ΔV_{th} from three consecutive stress-recovery sequences (stress not shown), where the first and the third stress sequence have been interrupted by monitoring measurements but not the second. The parallel shift of the consecutive traces is caused by traps with an emission time larger than the recovery time of 10^4 s. The reproducibility of the results further indicates no creation of additional traps during the measurement.

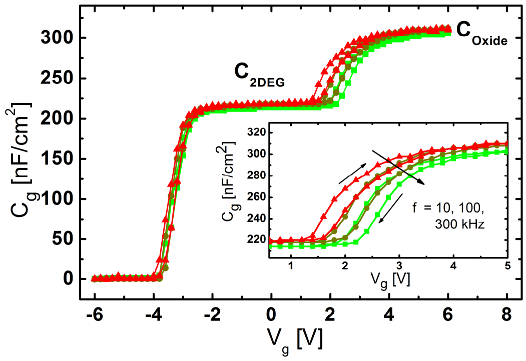
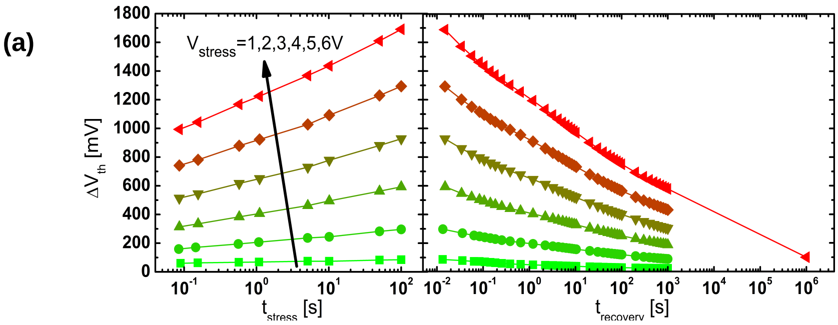


Fig 5. CV analysis: The increase of the capacitance at forward bias > 2 V suggests charge accumulation at the dielectric/III-N interface. The second capacitance plateau is consistent with the gate oxide capacitance. The hysteresis between forward and backwards sweeps for CV curves at different frequencies indicates trapping of charges with different time constants.

this case the intrinsic 2DEG acts as a counter electrode to the gate contact and a nearly homogenous electrical field distribution over the barrier is achieved. During recovery all contacts are grounded. In contrast to silicon MOS structures the V_{th} shift is not accompanied by a degradation of the transconductance (Fig. 3), because of remote trapping at the dielectric/III-N interface spatially away from the active channel (2DEG) which is therefore referred as “hidden” interface (Fig. 1). Thus the drain current degradation directly correlates with ΔV_{th} following the trend of the transfer characteristic. Comparing repeated stress-recovery sequences with and without monitoring at room temperature suggests that monitoring during stress has no significant influence and also no new traps are created during consecutive stressing sequences (Fig. 4). Further, dummy measurements without any stress between the monitoring measurements show an overall V_{th} drift stability of about 15 mV up to 10^5 s.

Experimental Results

In consistency with other authors [7], measurements of the transfer characteristic on our devices (Fig. 3) show no clear hysteresis up to 2 V maximum gate bias. The capacitance-voltage (CV) measurements exhibit a hysteresis around the second plateau, which is a hint on charge trapping (Fig. 5). Measurements of the threshold voltage drift over stress-recovery sequences show a quasi-linear characteristic on a logarithmic time scale, indicating a broad distribution of time constants for stress and recovery. Also a clear dependency on the gate bias is observed (Fig. 6). Due to this characteristic an extraction of time constants using conventional multiexponential fitting analysis is ambiguous (Fig. 7). A method to analyze such a broad distribution of characteristic time constants has been developed by Reisinger et al. [5] using so called capture emission time (CET) maps, which are extracted out of the recovery traces like that shown in Fig. 8a. The difference between two recovery traces of different stress times equals the threshold



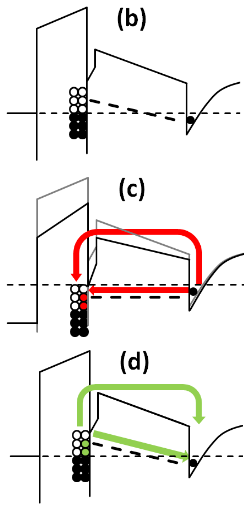


Fig 6 (a) Stress-recovery sequences over different gate bias show a quasi-linear behavior on a semi-logarithmic scale indicating uniformly distributed time constants. The slope of the stress/recovery curves increases/decreases with increasing gate voltage indicating a large amount of traps involved. Nearly full recovery is observed after a recovery time of 10^6 s. The conduction band together with the occupation of oxide traps is shown (b) under thermal equilibrium, where all electrons below the Fermi level are filled, (c) during stress, and (d) during recovery. Additionally a leakage path (potentially formed by a dislocation band) through the barrier is shown (dashed line). Open and filled circles indicate empty and filled traps, respectively.

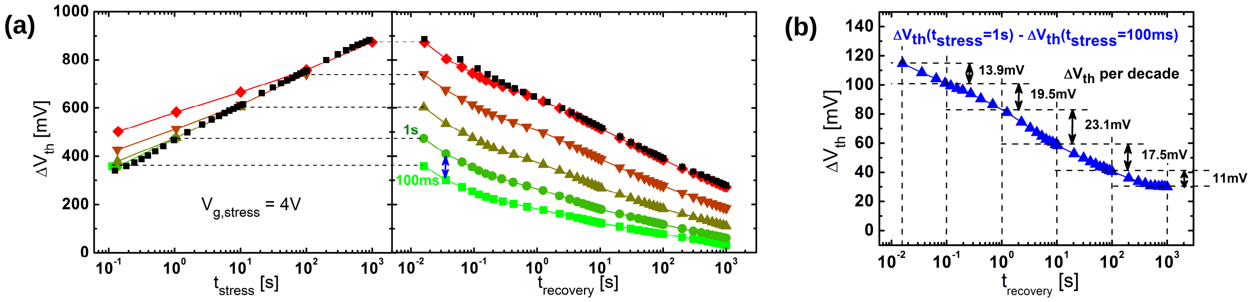


Fig 8 (a) Stress-recovery sequences with logarithmically increased stress times starting from 10^{-1} s to 10^{3} s at a fixed gate bias $V_{g,stress} = 4$ V. The decreased trapping slope and the increased drift offset of the later stress sequences (colored curves) can be explained by traps with larger emission time constants than the recovery duration of 10^{3} s. Due to logarithmically increased stress time the recovery sequences follow the same trend as a single stress-recovery sequence (black dots). The recovery traces appear rather parallel in contrast to figure 6 indicating similar densities of traps with same emission time constants. (b) Difference between the recovery traces for stress times of 100ms and 1s.

voltage drift caused by traps with characteristic capture time constants within the corresponding stress decade. From the recovery trace of such a stress decade the portion of ΔV_{th} for each recovery decade is extracted, which is caused by traps with characteristic emission times within each recovery decade (Fig. 8b). The ΔV_{th} value can easily be translated into an interface trap density using the oxide capacitance. The procedure is repeated for every neighboring pair of logarithmically distributed recovery curves of Fig. 8a to extract the whole CET map (Fig. 9). Such CET maps typically show a broad distribution of emission time constants for each decade of capture time constants (equivalent to the rows in the CET map). It means that a certain stress pulse fills up a huge number of traps with logarithmically distributed emission time constants, which are magnitudes larger than the stress time. Further, the stress curves in Fig. 8a justify the use of logarithmically distributed stress times, because all stress curves follow the same trend after one decade of additional stress and thus pre-stress effects can be excluded for the recovery curves. Analyzing devices during stress sequences with additional pre-stress at relatively higher gate bias reveals parallel capture and emission to and from traps located at different energetic and/or local positions (Fig. 10). The result suggests parallel emission and capture of independent traps being activated under different gate bias conditions. Further it indicates again that the gate bias determines the overall number of accessible traps. Analysis of the temperature activation reveals a small increase of the V_{th} shift per decade during stress and recovery with increased temperature (Fig. 11). However, the real influence of the temperature could be shaded by the experiment, because of parallel acceleration of stress and recovery dynamics [5,6]. There seems to be a strong correlation between trap density and oxide quality as indicated by the comparison of the threshold voltage drift dependency on the gate bias stress

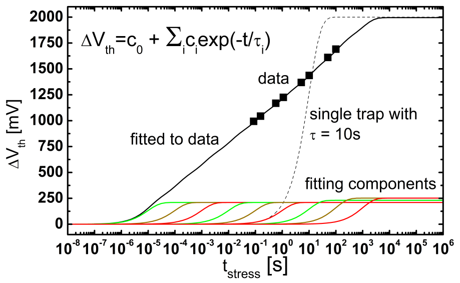
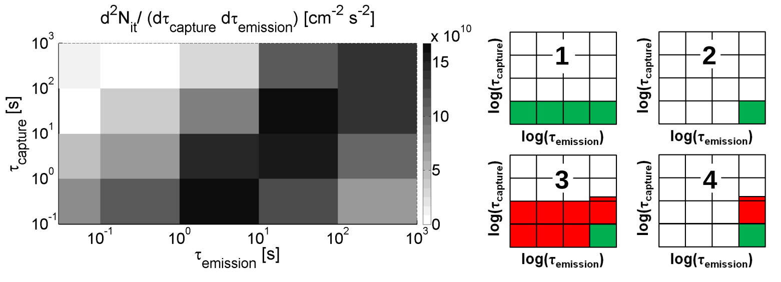


Fig 7 The stress curve at $V_{g,stress} = 6$V from Fig. 6 is fitted to the sum of an arbitrary number of logarithmically equally distributed exponential functions. The obtained amplitudes c_i are nearly the same proving that the experimentally observed semilogarithmic charging is only explainable through a very large and logarithmically uniform distribution of time constants. Hence the measurement does not allow extracting individual trap densities or time constants.



(a)

(b)

Fig 9 (a) CET map extracted out of the measurement from Fig. 8. The formula used to calculate N_{it} is given in the inset of Fig. 12. The result points out the strong correlation between capture and emission time constants with a relatively slower emission from traps. (b) Demonstration of the filling of the CET map: In the first stress recovery sequence all traps with a capture time constant smaller than the stress time are filled (1). After a certain recovery time all traps with a larger recovery time constant stay filled, all others are emptied (2). The remaining filled traps explain the initial stress offset visible in Fig. 8. A second stress recovery cycle with a ten times longer stress time (3) fills up the next decade in the CET map leading to an relatively increased filling level for emission time constants longer than the recovery time. (4) depicts the situation after another stress-recovery sequence.

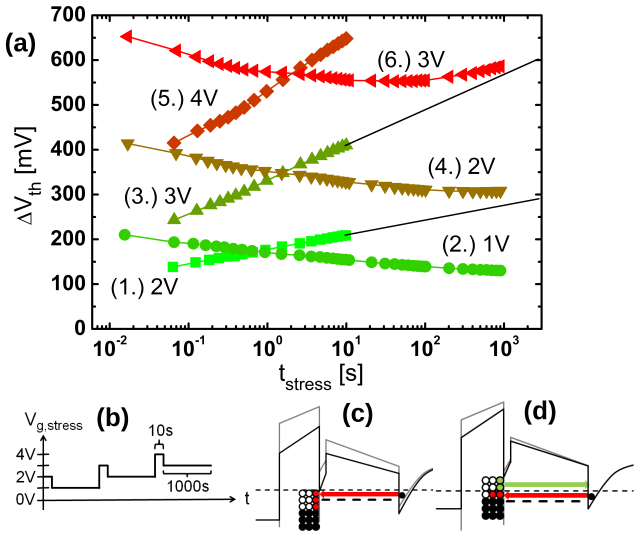


Fig 10 (a) Consecutive stress-stress sequences, where the first stress lasts for 10 s at a higher forward gate bias before the second stress with 1000 s duration, compare with (b). The 1000s stresses initially shows a recovery, followed by a quasi-saturation which starts to increase again continuing the stress characteristic from the prior 10 s stress at the same bias (dashed lines). In (c), capture of electrons during the 10s stress is shown. (d) sketches a parallel emission and capture process after stress shown in (c).

for annealed (densified) and not annealed gate oxides (Fig. 12).

Discussion & Conclusion

Although the microscopic nature of the defect states at the “hidden” interface cannot be clearly determined from our measurement, the behavior shows a strong similarity to bias temperature instability (BTI) in Si devices. Similar to BTI we found a broad distribution of time constants, which are represented by the CET map (Fig. 9). The CET map can be used to calculate device behavior under different stress/recovery conditions offering a tool for lifetime predictions [5,6]. However, the almost linear behavior of ΔV_{th} over V_g (Fig. 12) stands in contrast to silicon BTI results typically following a power law with an exponential coefficient of about three [5]. In addition, we present hypotheses which can explain the broad distribution of time constants: (1) a distribution of capture cross sections due to the disordered nature of oxide states at or near the “hidden” interface, (2) a distribution of tunneling distances between the interface and border traps [8,9], (3) spatially distributed leakage paths (dislocations bands) in the GaN/AlGaN barrier structure with varying magnitude of leakage current [10], which connect the 2DEG channel and traps at/near the “hidden” interface, (4) additional lateral trapping at the dielectric/III-N interface plane due to carrier hopping and thus a transport mechanism between the interface/border states. Mechanisms (2)-(4) can act as a common rate limiting process, which could explain the observed correlation between capture and emission processes (Fig. 9). In addition to the trap related behavior of our findings, we have to consider that even in an ideal dielectric bilayer charge is accumulated at the interface in order to maintain a constant steady-state current density. This is due to the different conductivities of each layer and is known as Maxwell-Wagner instability [11]. In summary, our characterization approach, using the concept of CET maps, has demonstrated its suitability for the investigation of the threshold voltage instability of gate insulated GaN HEMTs and provides a useful tool for their development.

Acknowledgement: We are very grateful to Fouad Benkhelifa, Stefan Mueller, Michael Mikulla, and Oliver Ambacher from the Fraunhofer Institute for Applied Solid State Physics IAF for wafer preparation and processing.

References

[1] T. Imada et al, IRW 2011 IEEE International, p. 38,
[2] R. Yeluri et al, J. of Appl. Phys., 2012, 111, 043718
[3] X. Liu et al, IEEE Tr. on Electr. Dev., 2011, 58, 95 -102
[4] A. R. Arehart et al, Phys. Status Solidi C, 2011, 8, 2242–2244
[5] H. Reisinger et al, IRPS, 2010, 7 -15
[6] T. Grasser et al, IEDM, 2011, 27.4.1 -27.4.4
[7] A.Fontserè et al, Proc. of the Int. Symp. on Power Sem. Dev. and ICs, 2012, p37
[8] D. M. Fleetwood, J. of Appl. Phys., 1998, 84, 6141-6148
[9] O. Engström, Semicond. Sci. Technol. 4 (1989) 11 06-1 11 5
[10] H. Zhang et al., J. Appl. Phys. 99, 023703 (2006)
[11] J. R. Jameson et al., IEEE Tr. on Electr. D., 2006, 53, 1858ff

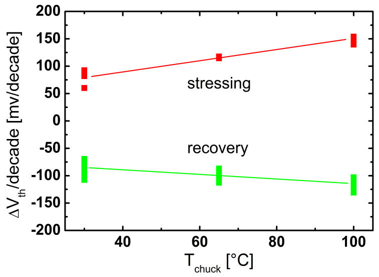


Fig 11 Slopes of stressing and recovery curves at increased temperatures showing weak temperature activation. The gate bias during stress was 3 V. The connecting lines are only a guide for the eyes.

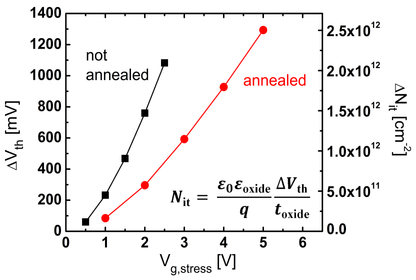


Fig 12 The threshold voltage drift over gate bias measured after 100s of stress shows a nearly linear relation. The two curves reflect a comparison between the standard process (i.e. annealed) and another wafer without the additional annealing step at 650°C after the ALD deposition.

4.4 New Insights on Forward Gate Bias Induced Threshold Voltage Instabilities of GaN-Based MIS-HEMTs

Authors	P. Lagger, A. Schiffmann, G. Pobegen, D. Pogany and C. Ostermaier
Published In	Proceedings of the Workshop on Compound Seminconductor Devices and Integrated Circuits
Year	2013
Pages	161 - 162
Conference Location	Warenemünde, Germany
Presentation	Oral Presentation

NEW INSIGHTS ON FORWARD GATE BIAS INDUCED THRESHOLD VOLTAGE INSTABILITIES OF GAN-BASED MIS-HEMTS

P. W. Lagger[1,4*], A. Schiffmann[2], G. Pobegen[3,4], D. Pogany[4], C. Ostermaier[1]

[1] Infineon Technologies Austria AG, Siemensstraße 2, 9500 Villach, Austria
[2] TU Graz, Rechbauerstraße 12, 8010 Graz, Austria
[3] K.A.I. GmbH, Technologiepark Villach Europastraße 8, 9524 Villach, Austria
[4] TU Wien, Floragasse 7, 1040 Wien, Austria
[*] E-mail: Peter.Lagger@infineon.com

ABSTRACT

GaN based MIS-HEMTs suffer from threshold voltage drifts (ΔV_{th}) caused by forward gate bias stress. We present a systematical approach to characterize the phenomenon based on the measurement of the transient behavior of ΔV_{th}. We found out that ΔV_{th} is caused by traps with a broad distribution of trapping and emission time constants, which was related to defect states in oxides.

1. INTRODUCTION

Power devices based on AlGaN/GaN heterojunctions are promising building blocks for future power electronic systems due to their superior figure of merits [1]. It is widely accepted that the two dimensional electron gas (2DEG), which is induced below the III-N barrier, is originating from donor like states at the surface of the barrier [2]. In order to reduce the parasitic gate leakage currents apparent in Schottky gate devices an additional gate dielectric is required, which also passivates these donor like surface states [3]. The transfer characteristic of such MIS-HEMT devices suffers from hysteresis and drift effects in forward gate bias direction [4, 5]. In difference to the oxide/semiconductor interface states in silicon MOSFET devices, these states cannot directly exchange charge with the channel, but only via the barrier (Fig. 1). The density of these interface states is usually investigated using photo assisted CV [6], conductance [7], or DLTS like measurement methods [8], which are measuring the response of charges to a small-signal AC bias excitation and an additional large-signal DC bias. These methods depend on the frequency of the AC signal and are ignoring apparently existing large-signal drift phenomena. In our work a more general approach to study the observed phenomena is presented based on the measurement of the transient recovery traces of the threshold voltage drift ΔV_{th}.

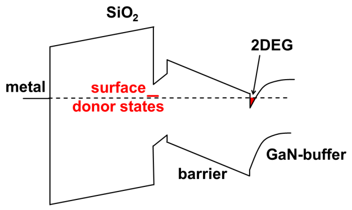


Fig 1. Sketch of the bandstructure of a typical gate stack used for normally-on AlGaN/GaN based HEMT structures. The barrier consists of a thick AlGaN layer with a GaN cap layer. The oxide is provided on top of the GaN cap layer. At the interface between the barrier and the buffer, a two dimensional electron gas is induced.

2. EXPERIMENTAL SETUP

All measurements were carried out on an optimized setup, which is capable of measuring the transient response of the recovery traces of ΔV_{th} with a delay of 10µs, using consecutive stress and recovery sequences [5]. The devices were processed on wafers with a standard epitaxial HEMT stack with a 30 nm thick SiO$_2$-layer as gate oxide.

3. EXPERIMENTAL RESULTS

Measurements of the recovery traces of the threshold voltage drift after stress at constant forward gate bias reveal a broad and dense distribution of characteristic emission time constants over several orders of magnitude of recovery time for logarithmically distributed stress times (Fig. 2). Due to this behavior the extraction of time constants using conventional multi-exponential fitting analysis is ambiguous. There is no unique correlation between the energetic position of the traps and the observed characteristic time constants [5, 9]. The positive threshold voltage drift ΔV_{th} indicates a net negative charging of the interface region with a density of interface states ΔN_{it} in the order of 10^{12} cm^{-2}. Fig. 2 reveals a fundamental problem of determining the total interface state density. All traps with a recovery time faster than the minimum delay time of the measurement setup are not included in this analysis and the onset of recovery is unknown. However, there has to be a lower boundary for the emission time constant of the traps which defines the onset of the recovery phenomenon. This value is yet unknown because we have not been able to observe a plateau in the onset of the recovery, but it is smaller than 10^{-7} s. As such the calcu-

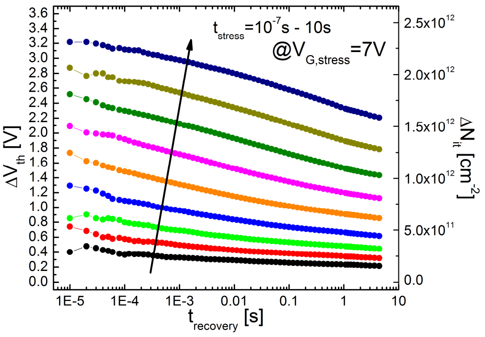


Fig. 2. Recovery traces after stress pulses with a gate stress bias of 7V and logarithmically distributed stress times ranging from 100 ns up to 10 s. The continuous decrease of ΔV_{th} with recovery time can be explained by several individual emission processes of defects with a very broad distribution of time constants.

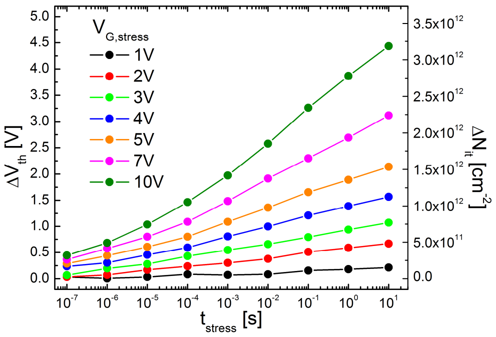


Fig. 3 Stress curves extracted from recovery traces of the threshold voltage drift ΔV_{th}, which were recorded after stress pulses with varying gate stress biases and stress times after a recovery time of 100 µs.

lated density of interface trap values can provide only an estimate and the total drift value will in general be higher. Fig. 3 shows stress curves, which are extracted from recovery traces after a fixed recovery time. It can be seen that ΔV_{th} varies with the stress time and the stress bias. The stress bias determines the number of accessible traps. The higher the stress bias, the more traps are charged within the same period of time. During a stress pulse all accessible traps with capture time constants within the stress time are activated.

4. DISCUSSION AND CONCLUSION

Although the microscopic nature of the defect states causing the observed behavior cannot be clearly determined from our measurement method, it gives us important information about their properties. The channel acts as a reservoir for electrons, which are trapped at the oxide/III-N interface. These electrons have to be provided via the barrier (Fig. 4). This could be either via the conduction band of the barrier or via leakage paths in the barrier. Both processes could be supported by trap assisted tunneling via bulk traps in the barrier [10]. At the interfacial region electrons can be trapped by interface states or by near interface defect states in the oxide. The degradation of the interfacial region between the bulk material and the oxide is also of concern for mature silicon based technologies. There the effect is known as bias temperature instability (BTI), which shows identical signatures than the degradation of the oxide/III-N interface. Such a broad distribution of characteristic trapping time constants is typical for defect states in oxide materials [9, 11, 12]. The most obvious difference to silicon based devices is the barrier of the MIS-HEMT, which influence is not fully understood yet. We speculate that the barrier gives an additional contribution to the time constant of the trapping process, but the major characteristic is determined by oxide traps. The forward stress bias dependency of the threshold voltage drift ΔV_{th} can be explained by simple electrostatic considerations. In Fig. 5a it is shown that in thermal equilibrium all traps below the Fermi level are filled. Under forward bias conditions the Fermi level of the gate metal contact and the 2DEG channel are separated. This opens up an “energetic volume”, i.e. the region in the bandgap of the oxide and the barrier, which was above the Fermi level under equilibrium conditions and is now below the Fermi level of the channel (Fig. 5b). The barrier has a lever effect, because it widens the energetic volume in the oxide in comparison to standard MOS-structures [11]. In summary, our characterization approach has demonstrated its suitability for the investigation of the threshold voltage instability of gate insulated GaN HEMTs and provides a useful tool for their development.

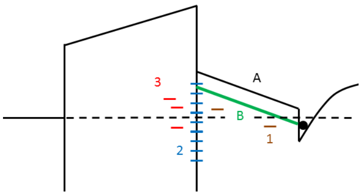


Fig. 4 Conduction band of the gate stack showing possible conduction paths and trap sites. The channel acts as a reservoir for electrons, which can get trapped at these sites during forward bias stress. The electrons are either provided via the barrier conduction band (A) or via spatially distributed leakage paths in the barrier (B). Both processes could be assisted by bulk traps in the barrier (1). Electrons can be trapped at interface states at the oxide/III-N interface (2) and at bulk oxide traps near this interface (3).

REFERENCES

[1] Kaminski et al, Proc. CIPS (2012), p. 1-11
[2] Ibbetson et al, Appl. Phys. Lett. 77 (2000), 250
[3] R. Vetury et al, Tr. ED 48 (2001), 560-566
[4] T. Imada et al, IRW (2011), p. 38
[5] P. Lagger et al, IEDM (2012), p. 13.1.1-13.1.4
[6] R. Yeluri et al, J. of Appl. Phys. 111 (2012), 043718
[7] X. Liu et al, IEEE Tr. on Electr. Dev. 58 (2011), 95 -102
[8] A. R. Arehart et al, Phys. Stat. Sol. C 8 (2011), 2242–2244
[9] H. Reisinger et al, IRPS (2010), 7 -15
[10] H. Zhang et al., J. Appl. Phys. 99 (2006), 023703
[11] T. Grasser, Microelectr. Rel. 52 (2012), 39-70
[12] D. K. Schroder, Microelectr. Rel. 47 (2007), 841-852

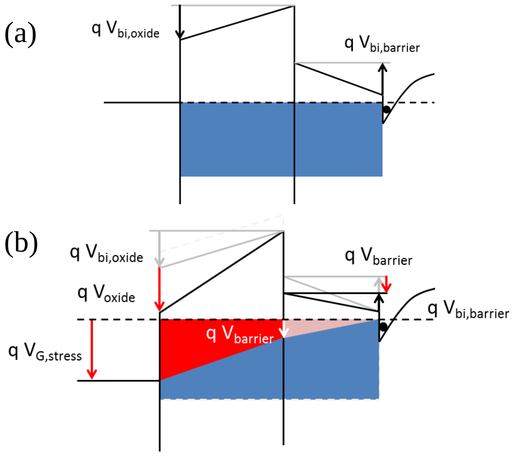


Fig. 5 In thermal equilibrium all trap states below the Fermi level are occupied (a). The build in potentials $V_{bi,oxide}$ and $V_{bi,barrier}$ are induced by the polarization charges and by charges at the oxide/III-N interface. During forward bias stress the applied voltage $V_{G,stress}$ is distributed over the oxide layer V_{oxide} and the barrier layer $V_{barrier}$, if it is assumed that the potential drop in the buffer is not affected. The red area marks the energy region (volume), which is additionally dipped below the equilibrium Fermi level. In this energy region (volume) all traps where unoccupied during equilibrium and can potentially be occupied during stress. It is obvious that the higher the stress bias the larger the volume which can be potentially charged [12].

4.5 Very Fast Dynamics of Threshold Voltage Drifts in GaN based MIS-HEMTs

Authors	P. Lagger, A. Schiffmann, G. Pobegen, D. Pogany and C. Ostermaier
Published In	IEEE Electron Device Letters
Year	2013
Volume	34
Issue	9
Pages	1112-1114

Very Fast Dynamics of Threshold Voltage Drifts in GaN based MIS-HEMTs

P. Lagger, *member, IEEE,* A. Schiffmann, G. Pobegen, D. Pogany, and C. Ostermaier

***Abstract*—The very fast dynamics of threshold voltage drift (ΔV_{th}) of GaN based MIS-HEMTs induced by forward gate bias stress is investigated with a simple oscilloscope based setup. We show that the logarithmic recovery time dependence of ΔV_{th}, previously found for recovery times ranging from 10 ms up to 1 Ms, extend even to the µs regime. Further, we observed an accumulation of ΔV_{th} due to repetitive stress pulses of 100 ns. Consequences for device operation and reliability are discussed.**

***Index Terms*—forward gate bias stress, HEMT, AlGaN/GaN, MIS, MOS, reliability, threshold voltage drift, trapping**

I. INTRODUCTION

In GaN based high electron mobility transistors (HEMTs) a thin barrier layer is used to induce a two dimensional electron gas (2DEG) in the GaN channel, directly below the barrier layer. The insulating properties of this barrier layer are insufficient. Particularly for power applications, the use of a gate dielectric is needed to suppress parasitic gate leakage currents [1]. However, threshold voltage instabilities limit the stability and reliability of these devices [2, 3, 4, 5]. Therefore the properties of the interface between the dielectric and the III-N barrier layer have to be understood. The observed ΔV_{th} instabilities (i.e. drifts and hysteresis in IV and CV curves) are usually associated with defect states at this particular interface and their density is mostly investigated using photo assisted CV [6], admittance [7,8], or DLTS like measurement methods [9], which are measuring the response of charges to a small-signal AC bias excitation under fixed DC bias. These methods do not link the fast AC response with apparently existing large signal drift phenomena within one methodic framework. Further, they are mostly based on simplifying assumptions, as e.g., that the relaxation processes in MIS-HEMTs are governed only by capture/emission processes where the trap energy levels and the characteristic time constants (e.g. due to carrier emission) are directly linked [10]. Recently, based on the measurement of the transients of the threshold voltage drift ΔV_{th} in response to positive gate bias stress pulses we have shown that ΔV_{th} in GaN based MIS HEMTs is caused by a broad distribution of characteristic relaxation time constants over several decades of stress and recovery [5]. The methodology is similar to that known from well-established bias-temperature-instability (BTI) stress-recovery analysis in CMOS devices [11]. In contrast to many other studies we do not rely on any assumptions about the relaxation processes and the measurement data can be evaluated in a straightforward manner. The threshold voltage drift strongly depends on the applied positive gate stress bias and time, where the time dependence of ΔV_{th} recovery is to first order logarithmic. This means that the amount of recovery of ΔV_{th} per decade is constant. It has been shown that this is valid for recovery times in the range of 10 ms to 1 Ms [5]. The logarithmic distribution of time constants suggests that even larger ΔV_{th} may exist for shorter recovery times, but it requires an experimental prove. It is apparent that these instabilities are a major limitation for normally-off devices. But up to now it was unclear if they are also relevant for the stability and reliability of normally-on devices, where positive voltage overshoot spikes can occur during switching the devices to the on-state depending on the parasitic components in a certain application, e.g. resistances and inductances. In this work we show that the broad distribution of recovery time constants is extended even to the µs regime by using a simple measurement setup based on an oscilloscope. This allows us to measure the recovery of ΔV_{th} with a delay of 1 µs using stress pulses with 100 ns duration. The characterization of such fast relaxation processes is usually a subject of the AC-bias based analysis methods mentioned above. We demonstrate that ΔV_{th} accumulates under short repetitive stress spikes with 100 ns duration. The dynamics of ΔV_{th} on this time scale is thus relevant in respect to AC-bias based analysis methods mentioned before as the cycle period is of the same order of magnitude or larger.

II. EXPERIMENTAL SETUP

The sample devices are fabricated on a GaN-on-Si substrate using state of the art processing technologies. The barrier layer of the HEMT structure consists of a 18 nm $Al_{0.20}Ga_{0.80}N$ layer. The gate dielectric is a 15 nm silicon oxide, which is not specifically optimized for threshold voltage drift stability. The nominal threshold voltage is -3.5V. The measurement setup is schematically depicted in Fig. 1a. In Fig. 1b the waveform of a 100 ns stress pulse is shown. A digital storage oscilloscope (DSO) is used to capture the transient responses. The device under test (DUT) is connected with a DC bias source in series with a resistor R_S. The voltage drop across the resistor is proportional to the drain current I_D. A pulse generator is used to modulate the drain current I_D by the gate input bias V_G along the load line defined by the resistor R_S, where the drain bias V_D is directly correlated with the drain current I_D. In Fig. 2, an example of a full stress-recovery cycle is depicted: 1) The $V_D(V_G)$ characteristic of the DUT is measured by applying a saw tooth voltage signal at the gate to bias the device from off-state ($V_{G,off}$) to on-state ($V_{G,on}$). 2) A gate bias point $V_{G,meas}$ in the linear region of the $V_D(V_G)$ characteristic is chosen and in a post-processing sequence the drain voltage signal $V_D(t)$ is directly converted to the equivalent threshold voltage drift ΔV_{th}

This paper was submitted to review on 17.05.2013.

P. Lagger is a PhD-student of Vienna University of Technology and he is with Infineon Technologies Austria, Siemensstraße 2, 9500 Villach Austria (Peter.Lagger@infineon.com)

C. Ostermaier and A. Schiffmann are with Infineon Technologies Austria.

G. Pobegen is with K.A.I GmbH, Europastraße 8, 9524 Villach Austria

D. Pogany is with Vienna Univ. of Techn., Florag. 7, 1040 Wien Austria

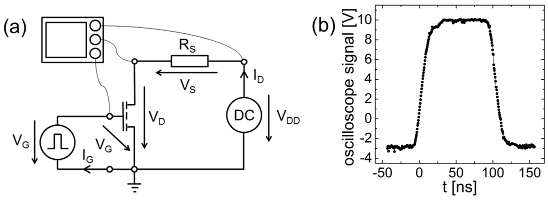


Fig. 1. (a) The experimental setup consists of a pulse generator, an oscilloscope, a DC bias source and a resistor R_S = 10 Ω. The input impedance of the DSO is 1 MΩ. (b) A 100 ns stress pulse switched from a certain $V_{G,meas}$ to the maximum applicable stress bias of the setup.

[5]. 3) A dummy measurement without stress ($V_{D,DUMMY}$) is performed to ensure the stability of the setup and the device during measurement conditions ($V_G = V_{G,meas}$) and to exclude parasitic effects (e.g. self-heating). 4) A stress pulse with a stress bias $V_{G,stress}$ and pulse length t_{stress} (e.g. 3 V, 100 µs in Fig. 2b) is applied and the transients of $V_D(t)$ are recorded at $V_{G,meas}$. The stress voltage is chosen well below the onset of measurable increase of the gate leakage current. Due to impedance mismatch, the recovery traces stabilize at around 1 µs after the stress pulse, which limits the minimum measurement delay. We state that we selectively investigate traps at the dielectric/III-N interface underneath the gate electrode due to the following reasons: These traps affect solely the threshold voltage and are charged via the barrier during forward gate bias stress with a homogenous electrical field distribution. However, traps at the dielectric/III/N interface do not significantly degrade the mobility due to the spatial separation from the active channel region (typically 20 nm distance) [12]. Further, the 2DEG screens the buffer potential and thus it is very unlikely that there is a contribution of buffer traps to the drift. This is further supported by the observation of a pure parallel shift of the transfer characteristics following forward bias stress [5].

III. EXPERIMENTAL RESULTS AND DISCUSSION

In Fig. 3 the recovery traces of ΔV_{th} after stress pulses with a fixed stress bias $V_{G,stress}$ of 3 V and logarithmically distributed stress times t_{stress} from 100 ns to 100 s are depicted. The maximum detectable ΔV_{th} is limited to 0.6 V due to the finite width of the transition region between off- and on-state of the device (cf. Fig. 2). The recovery traces give insights into the relaxation dynamic in the sub-ms regime and reveal a logarithmic dependence in time indicating a broad distribution of characteristic relaxation time constants, in accordance with previous observations for larger stress/recovery times [5]. The result suggests that in the whole range from µs to Ms the same class of defect states is activated. We speculate that the stress-recovery processes are governed by capture and emission processes at the oxide/III-N interface, as the observed signature is similar to the BTI phenomenon known from Si based MOS devices [11, 13, 14]. Further hypotheses are given in [5]. Newest studies on BTI state that configurational changes of oxide multistable defects [15] with no direct link between the trap energy level and the relaxation processes have to be taken into account for a proper description of the phenomenon [13]. A detailed discussion will be made in [16]. Furthermore, our results do not show any sign of an onset of the recovery which would give the total number of charges activated by a certain stress pulse. The curves still tends to rise towards smaller recovery times not showing a turning point. We remark that standard measurements clearly underestimate ΔV_{th} due to a long measurement delay. It is also important to notice that even for the 100 ns long stress pulses used in this example a significant drift of the device threshold voltage is observed. Every data segment in the curves in Fig. 3 is recorded using different devices and sampling rates, which indicates that the device to device variation is negligible and that the behavior is universal. Only the recovery traces for 100 ns stress time (i.e. three segments) are recorded consecutively on a single device after full recovery of the drift ΔV_{th}. This indicates that there are no additional traps created during consecutive stress-recovery cycles, but the same traps are filled and emptied during each cycle. It can be speculated whether the traps are created during the first cycle or whether they are due to pre-existing states.

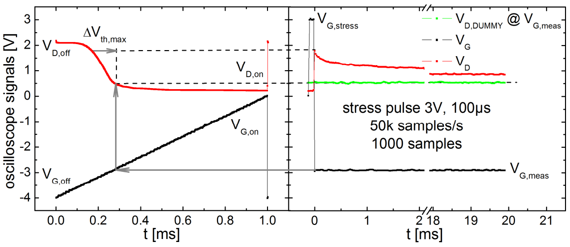


Fig. 2. Example for a typical stress-recovery cycle with (a) $V_D(V_G)$ and (b) pulsed $V_G(t)$ and $V_D(t)$ characteristic.

Further, we present a study of ΔV_{th} drift due to the cumulative effect [5, 11, 13] of repetitive stress pulses (spikes). In Fig. 4 such a scenario is emulated for a frequency of 10 kHz. In this case the time between the consecutive pulses is not sufficient for a full recovery of the threshold voltage. The frequency used for the experiment is lower than for typical applications, which means that for typical operating frequencies the effect is expected to be even stronger, because of reduced recovery time between the pulses. The observed threshold voltage degradation is in the order of some 100 mV already after a few milliseconds, with a logarithmic trend of the envelope of the ΔV_{th} curve (see inset of Fig. 5 for the pulse envelope definition). The difference between the two trend lines is also about 100 mV (sampling rate 100 kSa/s). This value is of concern for the short-term stability of the device, while the overall accumulation is of concern for the long-term reliability. Further, the observed ΔV_{th} recovery traces are on a time-scale comparable to the oscillation time of HF-CV measurements. Taking into account the accumulation due to repetitive spikes together with recovery effects in the µs regime, this clearly indicates that a HF-CV measurement is influenced by a combination of drift effects due to the applied DC bias during the integration time of each single measurement point and fast relaxation processes (e.g. trapping) following the superimposed AC-signal. To our understanding this makes it difficult to interpret the result of such a measurement. This is in a clear contrast to our method, where we are able to investigate the underlying relaxation processes on a very broad time scale in a systematic manner within one methodic framework. Our method offers an accurate control of all bias and timing parameters, while for example in a HF-CV setup the integration time cannot be controlled arbitrarily.

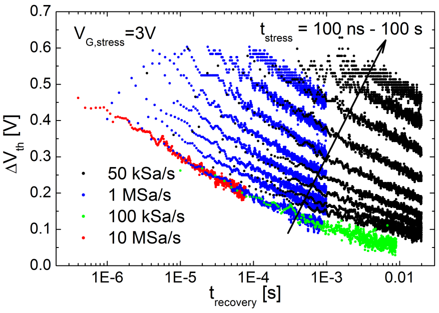


Fig. 3. Recovery of ΔV_{th} over a logarithmic time scale for a stress bias $V_{G,stress}$ of 3 V and logarithmically distributed stress times from 100 ns to 100 s. The measurements were performed on different devices using different sampling rates. Data segments are distinguished by color.

IV. CONCLUSION

We have shown that the logarithmic time dependence of V_{th} stress and recovery is extended even to the µs regime by using a simple oscilloscope based setup. Taking into account our previous findings [5], this shows that the relaxation time constants related to the oxide/III-N system are broadly distributed in the µs to Ms range. Significant V_{th} changes are observed even for gate bias pulses as short as 100 ns. Further we have studied the cumulative ΔV_{th} degradation induced by repetitive 100 ns stress pulses (spikes). In conclusion, our work gives well improved estimates on the reliability limiting degradation mechanism due to stress spikes and sets a profound basis for further investigations towards this topic.

REFERENCES

[1] M. A. Khan, G. Simin, J. Yang, J. Zhang, A. Koudymov, M. S. Shur, R. Gaska, X. Hu, A. Tarakji, “Insulating gate III-N heterostructure field-effect transistors for high-power microwave and switching applications”, IEEE Tr. on Microw. Th. a. Techn., 51, 624-632, 2003.

[2] A. Fontserè et al, Proc. Int. Symp. on Pow. Sem. Dev. & ICs, 2012, p37

[3] S. Huang, S. Yang, J. Roberts, K.J. Chen, “Characterization of Vth-instability in Al2O3/GaN/AlGaN/GaN MIS-HEMTs by quasi-static C-V measurement”, Physica Status Solidi C, 9(3-4):923-926, 2012.

[4] T. Wu, D. Marcon, M. Zahid, M. Van Hove, S. Decoutere, G. Groeseneken, “Comprehensive Investigation of On-state Stress on D-mode AlGaN/GaN MIS-HEMTs”, IRPS, 2013

[5] P. Lagger, C. Ostermaier, G. Pobegen, D. Pogany, “Towards understanding the origin of threshold voltage instability of AlGaN/GaN MIS-HEMTs”, IEDM, 2012, pp.13.1.1-13.1.4

[6] R. Yeluri, B. Swenson, U. Mishra, “Interface states at the SiN/AlGaN interface on GaN heterojunctions for Ga and N-polar material”, Journal of Applied Physics, 2012, 111, 043718

[7] X. Liu, H. Chin, L. Tan, Y. Yeo, “In situ Surface Passivation of Gallium Nitride for Metal Organic Chemical Vapor Deposition of High-Permittivity Gate Dielectric”, IEEE Tr. on El. Dev., 2011, 58, 95 -102

[8] X. Sun, O. I. Saadat, K. S. Chang-Liao, T. Palacios, S. Cui, T. P. Ma, “Study of gate oxide traps in HfO2/AlGaN/GaN metal-oxide-semiconductor high-electron-mobility transistors by use of ac transconductance method”, Appl. Phy. Lett., 102:103504/1-4, 2013.

[9] A. Arehart, A. Malonis, C. Poblenz, Y. Pei, J. Speck, U. Mishra, S. Ringel, “Next generation defect characterization in nitride HEMTs”, Phys. Status Solidi C, 2011, 8, 2242–2244

[10] M. Miczek, C. Mizue, T. Hashizume, B. Adamowicz, “Effects of interface states and temperature on the C-V behavior of metal/insulator/AlGaN/GaN heterostructure capacitors”, J. Appl. Phys, 103:104510/1-11, 2008.

[11] H. Reisinger, T. Grasser, W. Gustin, C. Schlünder, “The statistical analysis of individual defects constituting NBTI and its implications for modeling DC- and AC-stress”, IRPS, 2010, 7 -15

[12] S. Sze, K. Ng, “Physics of Semiconductor Devices”, Wiley, 2006

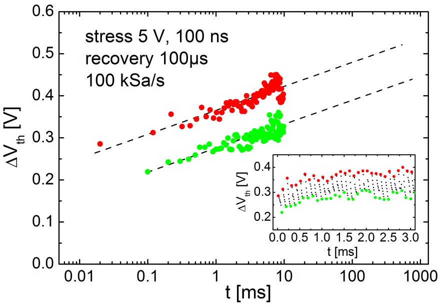


Fig. 4. Envelope of the threshold voltage drift ΔV_{th} induced by periodically repeated stress spikes (5 V, 100 ns). The inset shows the recovery traces of V_{th}, which are recorded after each spike for a duration of 100 µs. The first and last measurement point are marked with a red and green dot, respectively. The fluctuations are due to aliasing and due to coupling effects with the 50 Hz power line.

[13] T. Grasser, “Stochastic charge trapping in oxides: From random telegraph noise to bias temperature instabilities”, Microelectronics Reliability 52, 2012, 39-70

[14] D. M. Fleetwood, “Bulk oxide traps and border traps in metal-oxide-semiconductor capacitors”, J. of Appl. Phys., 1998, 84, 6141-6148

[15] M. Kirton, M. Uren, “Noise in solid-state microstructures: A new perspective on individual defects, interface states and low-frequency (I/f) noise”, Advances in Physics, 1989, 38, 367-468

[16] P. Lagger, to be submitted to Trans. on Electr. Dev., 2013

4.6 Comprehensive Study of the Complex Dynamics of Forward Bias Induced Threshold Voltage Drifts in GaN Based MIS-HEMTs by Stress/Recovery Experiments

Authors	P. Lagger, M. Reiner, D. Pogany and C. Ostermaier
Published In	IEEE Transaction on Electron Devices
Year	2014
Volume	61
Issue	4
Pages	1022-1030

Comprehensive Study of the Complex Dynamics of Forward Bias Induced Threshold Voltage Drifts in GaN Based MIS-HEMTs by Stress/Recovery Experiments

P. Lagger, *Member, IEEE*, M. Reiner, D. Pogany, and C. Ostermaier

***Abstract*— The transient recovery characteristics of the threshold voltage drift (ΔV_{th}) of GaN based HEMTs with a SiO_2 gate dielectric induced by forward gate bias stress are systematically and comprehensively investigated for stress times from 100 ns to 10 ks, recovery times from 4 µs to 10 ks, and stress biases from 1 V to 7 V. The measured recovery data are analyzed using the concept of capture emission time (CET) maps. It is shown that the observed data cannot be explained by simple first-order defect kinetics. It is revealed that the recovery curves for constant stress times scale with the stress bias. Further, the shape of the recovery curves changes from concave to convex with increasing stress time, independent of the stress bias. For short stress times and low stress bias a dominant rate limiting effect of the III/N barrier layer is proposed. Defect-related physical processes with a broad distribution of characteristic time constants are discussed to explain the logarithmic time dependency of ΔV_{th} stress and recovery, at which the role of Coulomb feedback effect, complex defects and spatially distributed defects is considered.**

***Index Terms*— power switching applications, forward gate bias stress, defect models, HEMT, AlGaN/GaN, MIS, MOS, reliability, threshold voltage drift, trapping, multistate defects, interface states**

I. INTRODUCTION

Gallium Nitride (GaN) offers superior material properties over silicon (Si) in terms of Baliga's figure of merits for electronic power devices [1]. It enables the implementation of high electron mobility transistors (HEMTs) with high breakdown capability, low on-state resistance and fast switching dynamics [2]. Due to the polar nature of III-N compounds, a two dimensional electron gas (2DEG) can be induced by a thin barrier layer (e.g. AlGaN) on top of a GaN channel layer. A gate dielectric is an effective measure to eliminate parasitic gate leakage currents in HEMT structures [3]. Further it offers an attractive basic framework for the implementation of normally-off devices [4]. However, state-of-the art metal insulator semiconductor (MIS-)HEMTs still suffer from hysteresis and threshold voltage drift effects induced by forward gate bias [5, 6, 7, 8]. This limits the stability and reliability of these devices, hence, the understanding and proper characterization of the dielectric/III-N interface is crucial. The observed ΔV_{th} drifts are mostly associated with interface defects at the dielectric/III-N interface [8, 9, 10]. In contrast to interface states in SiO_2/Si MOSFETs, those states in III-N MIS-HEMTs cannot exchange charge directly with the channel, but only via the III-N barrier. Traditionally, AC based measurement methods are used for the characterization of these states [11, 12, 13]. However, they are not able to treat the frequency dispersion and long term drifts of ΔV_{th} in a single methodic framework [7]. We have used a methodology known from well-established bias temperature instability (BTI) stress-recovery (S-R) analysis of CMOS devices [14, 15] to investigate the threshold voltage drift ΔV_{th} dynamics in GaN MIS-HEMTs [6]. A logarithmic time dependency of ΔV_{th} has been observed over a broad range of S-R times [5, 6, 7]. While Ref. [6] focused on S-R dynamics in the ms to hour range, in Ref. [7] the ns to ms dynamics has been evaluated. The logarithmic dynamics have been related to capture/emission processes of individual defects with a broad distribution of characteristic time constants. The recovery data were analyzed using the concept of CET maps [6, 14]. This concept does not rely on the relation of emission time constants to trap energy levels. For example, even in the simple and often encountered case of a thermally activated defect capture cross section (i.e. effect of lattice relaxation and multi-phonon capture/emission processes

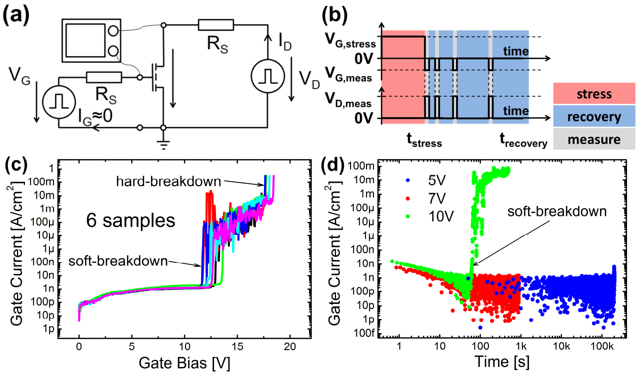


Fig. 1. (a) The experimental setup consists of a double pulse generator with an internal resistance of R_S = 50 Ω, and an oscilloscope. The input impedance of the DSO is 1 MΩ. (b) Pulse pattern of $V_{G,pulse}$ and $V_{D,pulse}$ during a stress-recovery cycle. To measure the transient response of V_D, the input biases are pulsed to $V_G = V_{G,meas}$ and $V_D = V_{D,meas}$. (c) Breakdown characteristics $I_G(V_G)$ shows low leakage levels up to a region above V_G = 10 V, where soft breakdown occurs (70 mV/s sweep rate). (d) I_G on logarithmic time scale is decreasing with time, indicating defect-related charging processes. Time-dependent breakdown can clearly be seen for V_G = 10 V.

This paper was submitted to review on 28.11.2013.

P. Lagger is a PhD-student of Vienna University of Technology and he is with Infineon Technologies Austria AG, Siemensstraße 2, 9500 Villach Austria (Peter.Lagger@infineon.com)

C. Ostermaier and M. Reiner are with Infineon Technologies Austria AG

D. Pogany is with Vienna Univ. of Techn., Florag. 7, 1040 Wien Austria

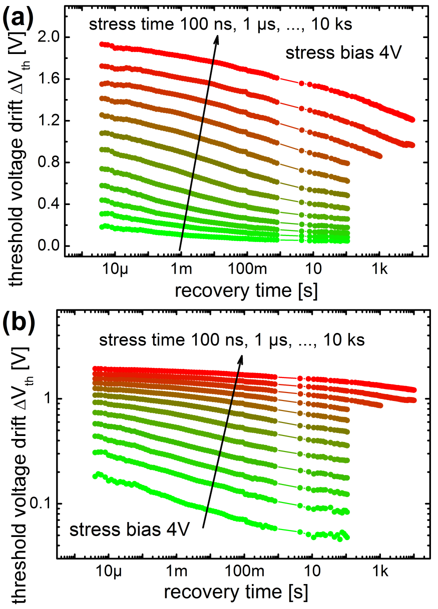


Fig. 2. Recovery curves of ΔV_{th} for a constant stress bias of 4 V after logarimically distributed stress times from 100 ns up to 10 ks in (a) linear scale and (b) logarithmic scale.

[16]), the trap energy level cannot be determined from transient measurements without any knowledge of the activation energy of the capture cross section [16, 17]. In Ref. [6] a uniform shape of the recovery curves has been observed in the limited S-R time (100 ms-1 ks stress, 15 ms-1 ks recovery) window, indicating first order relaxation dynamics (i.e. simple capture emission processes), resulting in positive entries in the CET map.

In this work, we provide a comprehensive study of the S-R dynamics of ΔV_{th} of AlGaN/GaN MIS-HEMTs in an expanded S-R time window. We analyze the scaling behavior of the recovery curves as a function of stress time and bias. The shape of the recovery curves changes from concave to convex for increasing stress times, which gives rise to negative entries in the CET map. This indicates more complex relaxation dynamics and will be discussed in terms of Coulomb effect, defect-to-defect interaction, and multistate defects [15, 18]. The paper is organized as follows: The experimental setup is presented in part II, the S-R results are shown in part III and the data evaluation using the concept of CET map with basic CET explanations is treated in part IV. The concept of active energy region, the role of the Coulomb effect and the GaN/AlGaN barrier, as well as various physical processes related to simple and complex defects, that are involved in the relaxation processes, are discussed in part V, followed by a conclusion.

II. EXPERIMENTAL SETUP

The sample devices are fabricated on a GaN-on-Si substrate using state of the art processing technologies. The barrier layer of the HEMT structure consists of a 3 nm GaN cap and a 25 nm $Al_{0.25}G_{0.75}N$ layer. The gate dielectric is a 30 nm SiO_2, which is not particularly optimized for threshold voltage drift stability. The wafer surface is cleaned with a HF dip before the dielectric is deposited by a low-pressure chemical vapor deposition process, followed by a post-annealing step at 1000 °C for 1 min under N_2 atmosphere. The nominal threshold voltage is -7.5 V. The test devices have a gate length of 1.3 µm and a gate width of 480 µm. For the measurement of the ΔV_{th} dynamics an oscilloscope based setup is used [7], cf. Fig. 1a. The transient response of the drain bias V_D is measured after forward gate bias stress pulses with a magnitude of $V_{G,stress}$ and stress time t_s according to the bias pattern as

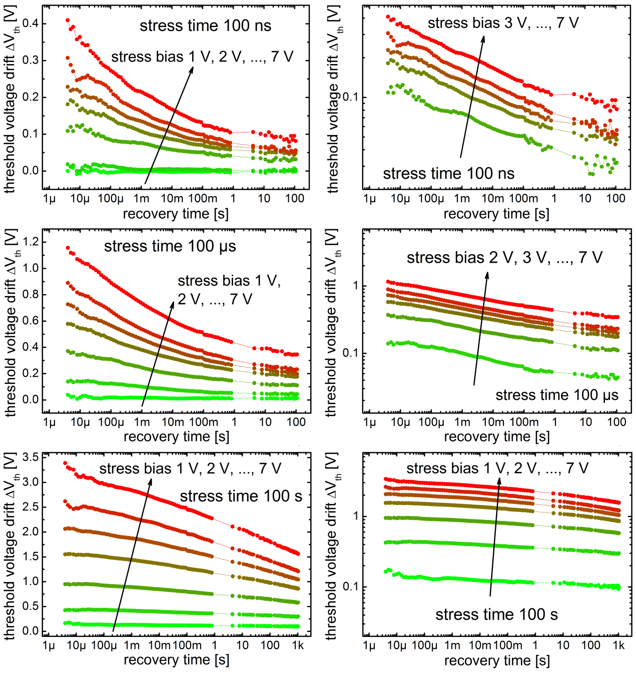


Fig. 3. Recovery curves for constant stress times of 100 ns, 100 µs, 100 ms and 100 s for varying stress bias from 1 V to 7 V.

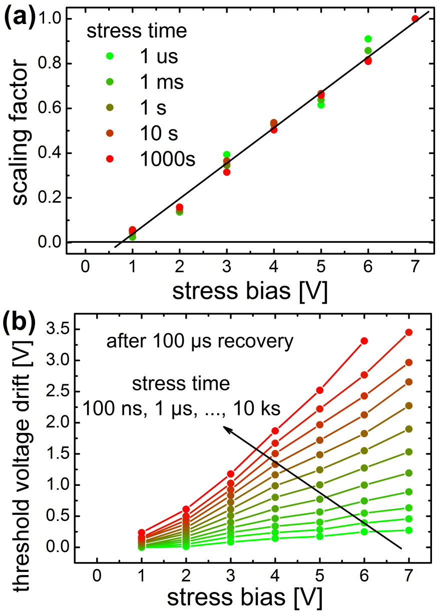


Fig. 4. (a) Scaling Factors of ΔV_{th} recovery as a function of the stress bias for different stress times. The black lines are only a guide for the eyes. (b) Stress bias dependency of ΔV_{th} as a function of the stress bias for varying stress times.

depicted in Fig. 1b. In a post-processing step the transient response of V_D is related to ΔV_{th} [7]. The delay time of the measurement setup is 4 µs. Transient recovery processes, which are faster than 4 µs, are not detected. The V_{th} recovery curves have a gap between 1 s and 5 s recovery time due to a change from continuous recording of V_{th} recovery directly after the stress pulse to pulsed recording (averaged over 100 ms) for longer recovery times (cf. Fig. 1a). All contacts are grounded during the recovery (i.e. between the recording pulses). Measurements are performed in sequences of constant $V_{G,stress}$ and logarithmically increased t_s. For each $V_{G,stress}$ a virgin device is used to ensure defined initial test conditions. The error caused by the logarithmically increased t_s on the same device is negligible in comparison of using a virgin device for each t_s sequence. The dielectric strength is sufficient for all performed measurement sequences, i.e. no dielectric breakdown occur (cf. Fig. 1c, d).

III. EXPERIMENTAL RESULTS

In Fig. 2 the recovery of ΔV_{th} is shown over logarithmic recovery time for logarithmically distributed stress times ranging from 100 ns to 10 ks for $V_{G,stress}$ = 4 V. The V_{th} drift continuously decreases over recovery time in the range of 4 µs up to 10 ks. The V_{th} drift increases for increasing t_s and the curvature of the ΔV_{th} recovery curves change from concave to convex.

An overview of recovery curves for constant t_s and varying $V_{G,stress}$ from 1 V to 7 V is given in Fig. 3. The logarithmic plots (see right panel) shows that the curves for a constant t_s are scaled by a constant factor, except the curves for 1 V up to 10 ms and for 2 V up to 1 µs. These curves show a negligible drift (cf. Fig. 5a). Furthermore, it can be seen that the change of the curvature from concave to convex for increasing t_s is independent of $V_{G,stress}$. The scaling factors (i.e. $\Delta V_{th}(t_s,V_G = V_{G,stress})/\Delta V_{th}(t_s,V_G = 7\text{ V})$ for t_r = 4 µs-100 s, or t_r = 4 µs - 1 ks respectively) of the recovery curves are summarized in Fig. 4a as a function of the stress bias for different stress times. The recovery curves scale nearly linear with the stress bias independent of the stress time.

The V_{th} drift, as seen in Fig. 4b, is extracted from recovery curves at t_r = 100 µs as a function of $V_{G,stress}$ for logarithmically distributed t_s (stress curves). The curves show the cumulative effect of all drift processes with t_r longer than the extraction time of 100 µs. In Fig. 5 the same data are plotted over stress time. The stress curves for different stress biases are parallel on a logarithmic scale (Fig. 5b), except the curves for stress biases of 1 and 2 V, which show a deviation from this scaling for short stress times (cf. Fig. 5b).

If we assume that the defects are located at the SiO_2/III-N interface, the correlation between ΔV_{th} and the density of defects ΔN_{it} is given, in a sheet charge approximation, by

$$\Delta N_{it} = - C_{ox} \cdot \Delta V_{th} / q, \tag{1}$$

where C_{ox} is oxide capacitance per unit area and q is the elementary charge. A positive ΔV_{th} corresponds to a net negative charging of the SiO_2/III-N interface. According to the measured values of ΔV_{th}, the overall density of apparent trapped electrons (under the maximum applied stress conditions) is in the order of $2\text{-}3\cdot10^{12}$ cm^{-2} (cf. Fig. 5). The stress curves show no saturation up to 10 ks of stress, but still a rising tendency. Although, this indicates that the total density of defects states is even higher than the observed values (cf. Eq. 1), an upper limit of ΔV_{th} cannot be observed due to the limitations set by the time-dependent dielectric breakdown phenomenon (cf. Fig. 1d).

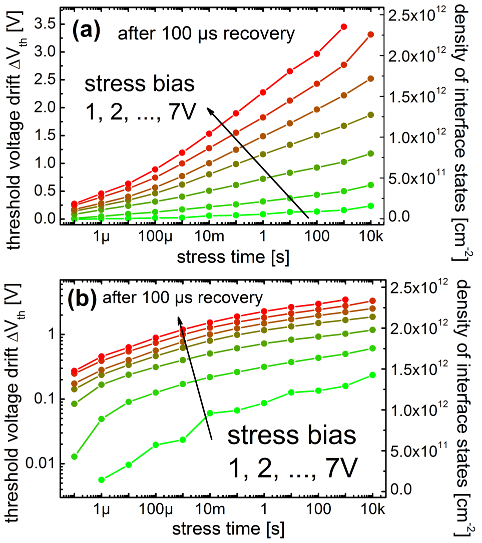


Fig. 5. Threshold voltage drift for varying stress time and bias after a constant recovery time of 100 µs in linear scale (a) and logarithmic scale (b).

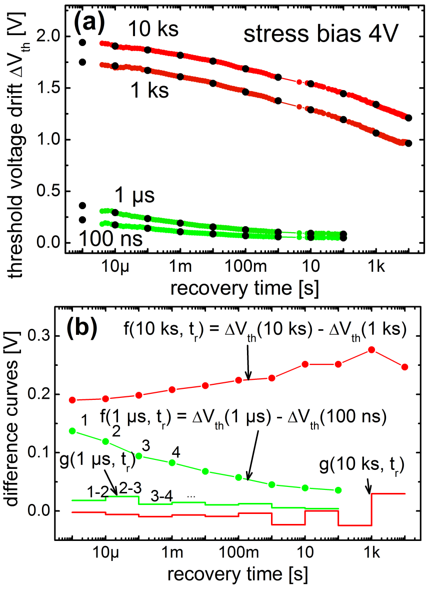


Fig. 6. (a) Recovery curves from Fig. 2 for two pairs of neighboring stress times, showing extraction points per decade of recovery time. (b) Difference of the recovery curves shown in (a). This curves are used to extract the CET map.

IV. CAPTURE EMISSION TIME MAP

For the readers convenience we briefly recall the main concept of the CET map for the representation of S-R data [14]. The continuous recovery of ΔV_{th} over several orders of magnitude of t_r can be explained by a huge number of parallel stochastic emission processes from individual defect states with a broad distribution of characteristic emission time constants [14] (cf. Fig. 2 and Fig. 3). Considering a simple defect with two states (occupied and empty) and first order capture/emission kinetics (i.e. no-coupling between the trap charge density and trap occupancy, see part V.D1), the occupation probability of the i-th defect during recovery is given by [14]:

$$P_i(t_r) = P_i(t_r{=}0) \cdot \exp(-t_r/\tau_{e,i}), \qquad (2)$$

where i is the index of the defect, t_r is the recovery time and $\tau_{e,i}$ is the characteristic emission time constant of the defect. The V_{th} drift is due to the cumulative contributions of an ensemble of individual defects acting in parallel given by

$$\Delta V_{th}(t_r) = \sum \Delta V_{th,i}\, P_i(t_r), \qquad (3)$$

where $\Delta V_{th,i}$ is the threshold voltage drift caused by the i-th defect [19]. A multi-exponential fitting analysis of the measured recovery data is ambiguous, because the single fitting components cannot be clearly distinguished [6]. The recovery data can be represented using a CET map, in which the density of threshold voltage drift $g(t_s,t_r)$ is plotted as a function of t_s and t_r (for the first-order kinetics, t_s and t_r is thus directly linked to capture and emission times, respectively [20]) Function g is defined as [14]:

$$g(t_s,t_r) = -\,\partial^2 \Delta V_{th}/(\partial t_s\, \partial t_r), \qquad (4)$$

From Eq. (4) it directly follows that

$$\Delta V_{th}(t_s,t_r) = \int_{-\infty}^{ts} \int_{tr}^{+\infty} g(t_s,t_r)\, dt_s\, dt_r. \qquad (5)$$

The assumption of first-order capture/emission kinetics of simple defects, obeying Eq. (2) and (3), yields that $g(t_s,t_r) \geq 0$. Fig. 6 explains the extraction process of the CET map using the experimental data of Fig. 2 is explained. In practice $g(t_s,t_r)$ is calculated using a discrete form of Eq. (4) where t_s and t_r are quantized by a decade:

$$f(t_s,t_r) = \Delta V_{th}(t_s, t_r) - \Delta V_{th}(t_s/10, t_r), \qquad (6a)$$
$$g(t_s,t_r) = f(t_s,t_r) - f(t_s, t_r/10). \qquad (6b)$$

An example for $f(t_s,t_r)$ and $g(t_s,t_r)$ is given in Fig. 6b. The recovery curves of Fig. 2, which have been used for this example, are highlighted in Fig. 6a. The resulting CET-map is shown in Fig. 7. Every row corresponds to a decade of t_s and every column corresponds to a decade of t_r. During each decade of stress, defects with τ_e's distributed over several decades of recovery are occupied. Moreover, the maximum of $g(t_s,t_r)$ for increasing t_s is shifted to longer t_r. This directly corresponds to the curvature change of the recovery curves from concave to convex for increasing t_s (cf. Fig. 3). In the region $\tau_c > \tau_e$ the CET consequently has negative entries, which indicates that the relaxation processes are not of first-order kinetics governed by Eq. (2) and (3). We further note that the scaling of the recovery curves with $V_{G,stress}$ directly implies the $V_{G,stress}$-scaling of the g-function in the CET map (not shown here).

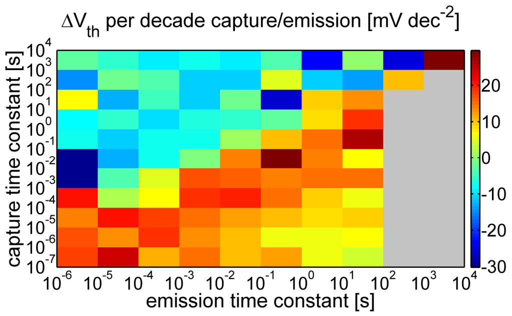


Fig.7. CET map extracted out of the recovery curves shown in Fig. 2.

V. Discussion of the Experimental Results

During forward gate bias stress ($V_G > 0$, $V_S = V_D = 0$) the 2DEG acts as a counter-electrode to the gate electrode and the electric field distribution over the gate stack is homogenous. The modulation of the occupancy of buffer defects under these conditions can be excluded and the position of the defects can be confined to the GaN/AlGaN barrier and the SiO_2. In Fig. 8a an overview of possible defect centers causing V_{th} drift is given, including bulk barrier defects, defects at the SiO_2/III-N interface and bulk oxide defects. We do not expect that defects at the interfaces between the III-N layers significantly contribute to V_{th} drift [21]. Forward bias induced V_{th} drifts are a consequence of charge transfer from the 2DEG to the defects listed above (e.g. via thermionic emission, trap assisted tunneling, etc.). In addition, the GaN cap is a quantum well, which can also play a role for the electron-exchange between GaN channel and defects.

The following discussion is structured according to the experimental observations.

A. *Bias Scaling of the Recovery Curves*

We suggest that the stress bias determines the number of accessible defects, due to bias scaling of ΔV_{th} recovery for constant t_s (cf. Fig. 3). This behavior is consistent with the active energy region (AER) model [15]. The AER is defined as the region between the Fermi-level $E_{F,S}$ at the channel, the equilibrium Fermi level at the SiO_2/III-N interface $E_{F,I}$ and the Fermi level at the gate electrode $E_{F,M}$ (Fig. 9a). The channel acts as an electron reservoir from which all states below $E_{F,S}$ can be filled with electrons, which are not filled at $V_G = 0$ V. The size of the AER scales with $V_G > 0$ and consequently also the number of potentially accessible defects, although the AER does not state about the actual defect locations. In addition, the contribution of defects to V_{th} drift depends also on their position within the gate stack, cf. Eq. 1.

B. *The Role of the Barrier Layer as a Leaky Dielectric*

We propose that the stress bias and time dependent onset of V_{th} drifts (cf. Fig. 5a) is related to the decrease of the barrier potential Φ_B, i.e. the potential difference between the Fermi level at the 2DEG channel $E_{F,C}$ and the conduction band minimum of the GaN cap at the SiO_2/III-N interface, with increasing V_G (cf. Fig. 9b). In thermal equilibrium $\Phi_B = \Phi_{B0}$. For $V_G > 0$ ($\Phi_B < \Phi_{B0}$) a net electron flux from the channel towards the SiO_2/III-N interface is induced. We introduce the equivalent circuit model, as shown in Fig. 9c, where the SiO_2 is assumed to be an ideal insulator with capacitance C_D (no leakage current) and the barrier is modeled by a capacitor C_B in parallel to a nonlinear resistance R_B (leaky dielectric). The barrier resistance R_B is expected to be strongly dependent on the barrier potential Φ_B. The bias and time dependent onset for V_{th} drift (for 1 V up to 10 ms, for 2 V up to 1 µs, cf. Fig. 5a) suggests two regimes: 1) the stress dynamics is governed by individual stochastic capture processes on interface or oxide defects, and 2) the stress dynamics is dominated by the rate limiting properties of the barrier layer. The role of the barrier acting as a rate limiter is discussed in detail in C5.

C. Broad Distribution of Capture/Emission Time Constants

In this section, defect models are reviewed to explain the broad distribution of time constants. It is organized according to the complexity of the models.

1) Distribution of Capture Cross Sections and Trap Energy Levels of Individual Defects

The Shockley-Read-Hall (SRH) [22] model describes the capture/emission rates of a single defect interacting with an electron reservoir by the following set of equations:

$$1/\tau_{c,i} = n\ \sigma_i\ v_{th}, \qquad (9a)$$
$$1/\tau_{e,i} = N_C\ \sigma_i\ v_{th}\ \exp(-\Delta E_{T,i}/kT), \qquad (9b)$$

with the capture rate $1/\tau_{c,i}$, the emission rate $1/\tau_{e,i}$, the defect's capture cross section σ_i, the trap level ionization energy $\Delta E_{T,i} = E_C - E_{T,i}$, the trap energy level of the i-th defect $E_{T,i}$, the thermal velocity v_{th}, the density of electrons in the conduction band n (i.e. here at the SiO_2/III-N interface), the conduction band edge E_C, the effective density of states in the conduction band N_C, and the thermal energy kT. In the framework of the SRH model, the broad distribution of observed capture/emission time constants can thus be explained by a broad and nearly homogenous distribution of E_T and log(σ) of individual defects at the SiO_2/III-N interface [23].

2) Distribution of Border Traps in the Silicon Dioxide

In addition, a spatial distribution of defects in the SiO_2 (border traps [23]) can be considered. We expect that the defect density is higher for a deposited SiO_2 (used here) compared to a thermally grown SiO_2. The tunneling process from the SiO_2/III-N interface to individual bulk oxide defects adds an additional contribution to the defect capture/emission time constants of Eq. (9) according to

$$\tau_{tunneling} = \tau_0\ \exp(x/\lambda), \qquad (10)$$

with the tunneling time constant $\tau_{tunneling}$, the depth in the oxide x (tunneling distance), and τ_0 and λ material and bias dependent parameters [24], which can, in general, be different for stress and recovery conditions [15]. In this context, the broad distribution of time constants can be explained by a nearly uniform distribution of tunneling distances to individual oxide defects, which leads to a logarithmic distribution of $\tau_{tunneling}$ [25]. This also fits to the concept of AER. Further, the defect energy level $\Delta E_{T,eff}(x)$ for border traps (Fig. 8b) depends on the depth x of the defect in the SiO_2 given by [18]

$$\Delta E_{T,eff}(x) = \Delta E_T - q\ x\cdot\varepsilon_{D0}, \qquad (11)$$

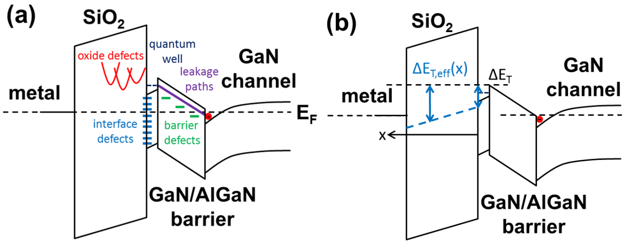


Fig.8 (a) Overview of potential defect centers in the SiO_2/barrier gate stack of a GaN based HEMT device. (b) Bias effect on defect energy position of bulk oxide defects as a function of the depth x.

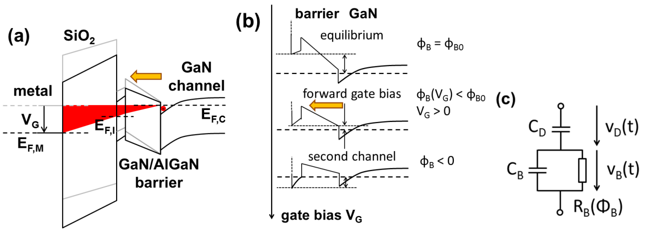


Fig. 9. (a) Bandstructure of a SiO_2/AlGaN-barrier/GaN-buffer stack. The red area is spanned by the applied forward gate bias and marks the energetic region, where defects can be filled due to forward gate bias. (b) Section of the barrier/buffer region showing the evolution of the conduction band with increasing gate bias from equilibrium to spill-over. (c) Equivalent circuit model of the gate stack for forward gate bias conditions.

where ΔE_T is the trap energy level at the SiO_2/III-N interface, and ε_{D0} is the electric field strength in the SiO_2 for $V_G = 0$ for recovery conditions ($V_G = 0$) (cf. Fig. 8b.). According to Eq. 9b this leads to an x dependent broadening of the characteristic emission time constant of oxide defects with a single energy level ΔE_T.

3) Distribution of Activation Energies due to Lattice Relaxation Effects

In general, the capture cross section σ (cf. Eq. 9a and 9b) can be thermally activated due to lattice relaxation effects given by [16, 17]

$$\sigma_i(T) = \sigma_{0,i}\ \exp(-E_{A,i}/kT), \qquad (12)$$

where $\sigma_{0,i}$ is a constant factor and $E_{A,i}$ is the activation energy. In Fig. 10, a so-called configuration-coordinate diagram, representing the sum of electronic and vibrational energy of a defect, is depicted. The sketched parabolas are the lowest-order approximations of a lattice displacement potential (i.e. harmonic oscillator). The energy barrier for electron capture is $E_{A,i}$ and for emission it is $\Delta E_{T,i} + E_{A,i}$. The transitions between the defects states are governed by non-radiative multi-phonon (NMP) processes [16]. $E_{A,i}$ depends generally on defect properties such as bonding length and bonding angle. In a disordered material (like amorphous SiO_2) these properties are distributed and therefore also the activation energy $E_{A,i}$ and the corresponding capture/emission time constants [15, 26]. In the next section this model will be generalized to multi-state defects.

4) Multi-State Defects

The defect models considered in C1-C3 describe defects with two defect states (occupied and empty). Random telegraph noise [18, 27] and time dependent defect spectroscopy [13] studies on SiO_2/Si devices revealed the existence of such defects with more than two defect states. The transitions between the states are governed by NMP processes, similar as described in the previous section [15]. These defects can be represented by a multi-well configuration-coordinate diagram. For example in Fig. 12a there are two possible states 2) and 3) for the occupied state, being separated by energy barriers E_{B3} and E_{B4}. The respective electron capture and emission processes have rates k_{12} and k_{21} and the configuration rates of the occupied defect are k_{23} and k_{32}. Therefore, such a defect cannot be modeled with a SRH model. The energy barriers for state transitions of these defects are statistically distributed due to statistically distributed defect properties in the amorphous network of atomic bonds in SiO_2 [13, 22]. Additionally, the defect energy levels E_{Ti} change with the electric field strength ε_D and position x of the defect in the SiO_2 according to Eq. 11. E_{T1} is the energy level at the electron reservoir, i.e. the channel Fermi-level $E_{F,C}$. The different defect states are due to different bonding configurations at the defect site and arise from a complex interaction between the electronic and the vibrational system [13]. Multi-state defects can naturally explain negative CET map entries $g(t_s,t_r)$ as further discussed in D2.

5) *Rate Limiting Properties of the Barrier Layer*

The model in Fig. 9c suggests that the barrier acts as rate limiter and the effective capture time constant is modified according to

$$\tau_{c,eff,i} = \tau_{c,i} + \tau_{barrier}, \tag{13}$$

where $\tau_{barrier} = R_B(\Phi_B)\cdot(C_B+C_D)$ is the barrier potential-dependent time constant of the GaN/AlGaN barrier layer [24]. Some studies report the existence of discrete leakage paths in AlGaN barrier layers [28]. The resistance (and thus $\tau_{barrier}$) of such localized leakage paths can be distributed, leading to a broadening of capture time constants according to Eq. 13. Moreover, a resulting non-uniform potential distribution over the SiO_2/III-N interface plane (Fig. 11a) will cause a non-uniform defect occupancy, which can additionally lead to a broadening of recovery time constants.

6) *Coulomb Charging*

The accumulation of electrons at the SiO_2/III-N interface during stress ($V_G > 0$) increases the barrier potential Φ_B proportional to the density of accumulated charges (Fig. 9b), which in turn also increases the barrier resistance R_B. We think that the transient decrease of I_G is due to this charge accumulation (Fig. 1d). The more charges are accumulated during stress, the more the barrier potential and the barrier resistance are increased, until steady state is reached and a constant leakage current over the whole structure is maintained [29]. We propose that this feedback effect can also lead to a broadening of capture time constants according to Eq. 13 and emission time constants according to Eq. 11 (see also part D below). In the case of discrete leakage paths as described in C5 a non-uniform feedback dynamics is expected due to spatially distributed leakage paths, which cause a non-uniform distribution of the barrier resistance, cf. Fig. 11a.

D. *Negative Entries in the CET Map*

Interestingly, the CET map in Fig. 7 reveals negative entries, which contradicts first-order capture/emission kinetics. The related change of the shape of recovery curves from concave to convex for increasing t_s indicates that the contribution to ΔV_{th} from recovery processes with relatively shorter emission time constants decreases as t_s increases. We propose three hypotheses, which do not necessarily exclude each other, to explain this observation. Electrostatic feedback effect (D1) and dynamics of complex defects (D2-D3) are considered:

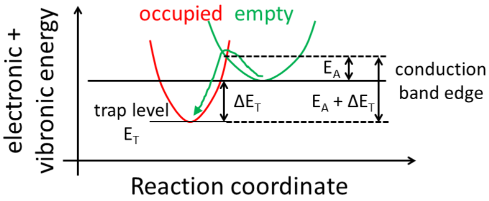


Fig. 10 Configuration-coordinate diagram showing the dependency of the total energy (electronic and vibrational) of a defect state as a function of an abstract reaction coordinate along the reaction path from the occupied state to the empty one.

1) *Coulomb Charging*

Coulomb charging as described in C6 causes a dynamical change of the barrier potential Φ_B during forward gate bias stress that is proportional to the change of the interface charge density, which leads in turn to a dynamical change of the AER. This change causes parts of the AER to be lifted above the channel Fermi level $E_{F,C}$ and thus in this region the emission of electrons is possible (cf. Fig. 11b). This can explain the observed negative CET map entries. The electrons, which are emitted from the lifted parts of the AER during stress ($V_G > 0$), would be emitted during recovery ($V_G = 0$) without Coulomb charging. The more the AER is lifted, the more the potential barrier for the emission of electrons is increased and hence, to first-order, also the corresponding emission time constants. Electrons with “shorter” emission time constants tend to be more likely emitted during stress than those with “longer” emission time constant. The electrons emitted during stress are therefore missing during recovery (negative CET map entries). One can expect a correlation between t_s and t_r up to which electrons are emitted during stress. This might explain that the negative entries in the CET map are arranged in the region $t_s > t_r$. On the other side, further studies have to be carried out whether the scaling of recovery with $V_{G,stress}$ (Fig. 3) is consistent with this explanation, because the shape of the recovery curves is independent of $V_{G,stress}$ and hence also of ΔV_{th}, ΔN_{it}, and Φ_B. However, a higher Φ_B implies a higher energy barrier for the electron emission while the same shape of V_{th} recovery curves means that the distribution of the according emission time constants is scaled rather than arbitrarily changed.

2) *Multi-State Defects*

The explanation of $g < 0$ in the CET map in the case of a single multi-state defect (cf. Fig. 12a) is given in the following: For a short stress time t_{s1} the defect is in state 2. During the recovery, the defect emits the electron (i.e. transition to state 1) and the defect acts as a simple trap. The corresponding recovery curve is given in Fig. 12b. As we consider a single defect it is a discrete step-function [15, 19]. For a longer stress time t_{s2}, the defect can also reach state 3 and the recovery occurs via state 2 with a longer recovery time leading to a recovery curve shown in Fig. 12c. Importantly, the short recovery process related to transition from state 2 to

1 is thus missing in the recovery curve. The difference of ΔV_{th2} - ΔV_{th1} shown in Fig. 12d gives hence a negative value leading to $g < 0$ in the resulting CET map (cf. Fig. 12e).

3) Defect-to-Defect Interaction

Defect-to-defect interaction [18] may be possible for a high density of interface states N_{it}. For example a N_{it} of 10^{13} cm^{-2}, which is of the same order as the surface donor density [30, 31], corresponds to a mean defect distance of about 3.2 nm. Thus it allows an electron hopping to neighboring defects, where an electron captured initially on a defect with a relatively short τ_c can be transferred to a defect with a longer τ_e during stress. At recovery, short recovery time constants will consequently be missing in the recovery processes, leading to $g < 0$ as in the previous part. In the above two cases of complex defects, the effect on the CET map is the same as for the Coulomb charging, but the underlying physics is totally different.

In this part, we have discussed a variety of plausible defect models in addition to the influence of the barrier to explain the experimental data. Based on this ideas, we see no direct way to translate the measured S-R time constants into physical quantities like trap energy levels E_T, tunneling distances (e.g. border traps), etc., which is often suggested in literature [11, 12, 13]. Further we want to recall that the observed transients of ΔV_{th} are on a time-scale of the ac signal period used in small-signal measurements (e.g. HF-CV, admittance, etc.), which are frequently used for interface characterization [7]. Moreover, the barrier has to be taken into account for the extraction of defect properties [32], cf. Fig. 9c. Nevertheless, a small-signal measurement is always accompanied by the large-signal V_{th} drift and thus can only scan a fraction of the total defect density. Therefore, without detailed knowledge about the underlying physical mechanism, we have to stick on the general description of S/R time constants.

We want to explicitly point out that no dominant capture/emission time constants can be identified in our ΔV_{th} data and therefore a multi-exponential fitting analysis, like described in [33], is ambiguous [6]. In difference to our study, the work of [33] focuses on the investigation of bulk traps in the barrier and the buffer of Schottky devices under on-state and $V_G < 0$ stress conditions.

VI. CONCLUSIONS

Our systematic and comprehensive study of V_{th} drifts in GaN based MIS-HEMTs can be summarized as follows:

1. The nearly logarithmic time evolution of ΔV_{th} indicates a broad distribution of corresponding stress and recovery time constants. Defect models and related effects including simple and complex defects, tunneling to border traps and the effect of the double capacitive gate stack of a dielectric and the III-N barrier have been discussed.
2. V_{th} recovery curves scale with stress bias. This can be explained in terms of the active energy region model.
3. For short stress times, the shape of the recovery curve is concave and with increasing stress times the shape changes to convex, which indicates more complex dynamical processes.

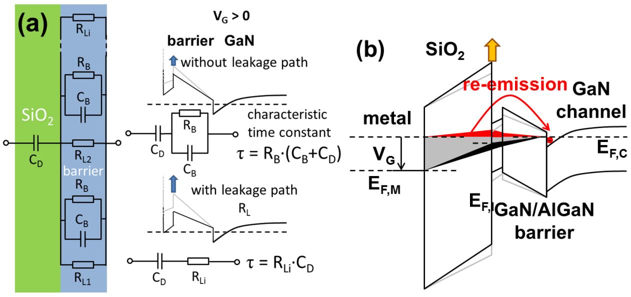


Fig. 11 (a) Extended equivalent circuit model of the gate stack for $V_G > 0$ including distributed parallel resistances R_{Li}, which represents distributed discrete leakage paths in the barrier (left side). The band structure diagrams indicate different voltage distribution between dielectric and barrier with/without leakage path with the equivalent circuits and characteristic time constants for both cases (right side). (b) Change of the active energy region due to change of the barrier potential Φ_B proportional to the accumulation of electrons at the SiO_2/III-N interface during forward gate bias stress. The longer the stress time, the more Φ_B is increased (indicated by the change of the band structure from gray contours to black contours). The black area shows the initial AER, directly after the stress pulse is applied (no electrons accumulated). It is overlapped by the gray area, which shows the AER due to Coulomb charging of the dielectric/III-N interface. The red area shows the part of the AER, which are lifted above the channel Fermi level $E_{F,C}$ and thus defects in this region can in principle re-emit afore trapped electrons.

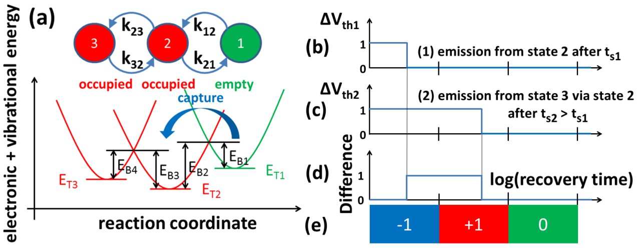


Fig. 12 (a) Defect potentials for a three-state defect in the SiO_2 (two occupied states) for zero electric field (bottom part) with corresponding state transition diagram (upper part). The defect energy levels E_{Ti} are marked with a line. The energy barriers for the state transitions are E_{Bi}. (b) and (c) shows recovery traces of ΔV_{th} after different stress times. (d) The difference between (1) and (2) explains why $g(t_s,t_r)$ can be negative. (e) Corresponding row of the CET map.

4. The observed negative fields in the CET maps have been attributed to the Coulomb effect and to complex dynamics of multistate defects and defect-to-defect interactions.
5. The onset of the V_{th} drift has a stress bias and stress time dependent onset, for which an III-N barrier transport limiting effect is accounted.

The features 1) and 2) are also observed for other dielectric materials, e.g. Al_2O_3 [6] and SiN_x [34, 35]. We believe that these observations might be found for a broad class of dielectrics. This assumption is further supported by the profound work on bias temperature instability (BTI) found in the dielectric/Si system. BTI is observed for a broad range of dielectric materials [36], including SiO_2, SiON, HfSiO, HfSiON, etc. It also shows a broad distribution of characteristic S/R time constants similar to our observations, although the magnitude of ΔV_{th} is significantly smaller. The features 3) and 4) are not described previously in GaN literature and should be further clarified. Further studies to clarify this question are necessary. Moreover, we expect that feature 5) is also observed for other dielectric materials, since we ascribe it to the III-N barrier.

Although, a comprehensive overview of plausible models is given, a final assessment of the dominant physical root cause needs additional investigations and further modeling. Nevertheless, important knowledge about the characteristics of V_{th} drifts is gained. Furthermore, we demonstrate that the transient measurement of ΔV_{th} offers a very powerful tool to investigate, characterize and qualify GaN based MIS devices.

REFERENCES

[1] B. J. Baliga, “Fundamental of Power Semiconductor Devices”, Springer, 2008

[2] N. Kaminski, O. Hilt, “SiC and GaN Devices – Competition or Coexistance?”, CIPS, 2012, p. 1-11

[3] M. A. Khan, G. Simin, J. Yang, J. Zhang, A. Koudymov, M. S. Shur, R. Gaska, X. Hu, A. Tarakji, “Insulating gate III-N heterostructure field-effect transistors for high-power microwave and switching applications”, IEEE Tr. on Microw. Th. a. Techn., 51, 624-632, 2003.

[4] T. Imada, M. Kanamura, T. Kikkawa, “Enhancement-Mode GaN MIS-HEMTs for Power Supplies”, Int. Pow. Electr. Conf. , 2010, 1027-1033

[5] T. Wu, D. Marcon, M. Zahid, M. Van Hove, S. Decoutere, G. Groeseneken, “Comprehensive Investigation of On-state Stress on D-mode AlGaN/GaN MIS-HEMTs”, IRPS, 2013

[6] P. Lagger, C. Ostermaier, G. Pobegen, D. Pogany, “Towards understanding the origin of threshold voltage instability of AlGaN/GaN MIS-HEMTs”, IEDM, 2012, pp.13.1.1-13.1.4

[7] P. Lagger, A. Schiffmann, G. Pobegen, D. Pogany, C. Ostermaier, „Very Fast Dynamics of Threshold Voltage Drifts in GaN-Based MIS-HEMTs“, IEEE Electron Device Letters, Vol. 34, No. 9, 2013

[8] T. Imada, K Motoyoshi, M. Kanamura, T. Kikkawa, “Reliability Analysis of Enhancement-Mode GaN MIS-HEMT with Gate-Recess Structure for Power Supplies”, IIRW 2011, p. 38-41

[9] X. Liu, H. Chin, L. Tan, Y. Yeo, “In situ Surface Passivation of Gallium Nitride for Metal Organic Chemical Vapor Deposition of High-Permittivity Gate Dielectric”, IEEE Tr. on El. Dev., 2011, 58, 95 -102

[10] H.-Y. Liu, C.-S. Lee, W.-C. Hsu, L.Y. Tseng, B.-Y. Chou, C.-S. Ho, C.-L. Wu, “ Investigation of AlGaN/AlN/GaN MOS-HEMTs on Si Substrate by Ozone Water Oxidation Method”, Transaction on Electron Devices, Vol. 60, No. 7, 2013

[11] R. Yeluri, B. Swenson, U. Mishra, “Interface states at the SiN/AlGaN interface on GaN heterojunctions for Ga and N-polar material”, Journal of Applied Physics, 2012, 111, 043718

[12] S. Huang, S. Yang, J. Roberts, K.J. Chen, “Characterization of Vth-instability in Al2O3/GaN/AlGaN/GaN MIS-HEMTs by quasi-static C-V measurement”, Physica Status Solidi C, 9(3-4):923-926, 2012.

[13] X. Sun, O. I. Saadat, K. S. Chang-Liao, T. Palacios, S. Cui, T. P. Ma, “Study of gate oxide traps in HfO2/AlGaN/GaN metal-oxide-semiconductor high-electron-mobility transistors by use of ac transconductance method”, Appl. Phy. Lett., 102:103504/1-4, 2013.

[14] H. Reisinger, T. Grasser, W. Gustin, C. Schlünder, “The statistical analysis of individual defects constituting NBTI and its implications for modeling DC- and AC-stress”, IRPS, 2010, 7 -15

[15] T. Grasser, “Stochastic charge trapping in oxides: From random telegraph noise to bias temperature instabilities”, Microelectronics Reliability 52, 2012, 39-70

[16] C. H. Henry, D. V. Lang, “Nonradiative capture and recombination by multiphonon emission in GaAs and GaP”, Physical Review B, Vol. 15, No. 2, 1977

[17] O. Engström, H. G. Grimmeiss, “Vibronic states of silicon-silicon dioxide interface traps”, Semicond. Sci. Technol., 4, p. 1106-1115, 1989

[18] M. Kirton, M. Uren, “Noise in solid-state microstructures: A new perspective on individual defects, interface states and low-frequency (1/f) noise”, Advances in Physics, 1989, 38, 367-468

[19] T. Grasser, H. Reisinger, P.-J. Wagner, F. Schanovsky, W. Goes, B. Kaczer, „The Time Dependent Defect Spectroscopy (TDDS) for the Characterization of the Bias Temperature Instability“, IRPS 2010, p 2A.2.1-2A.2.10

[20] In general, a more appropriate name of the CET map would be “stress-recovery time map”, but we keep the historical notation of [14]

[21] M. Silvestri, M. J. Uren, M. Kuball, “Dynamic Transconductance Dispersion Characterization of Channel Hot-Carrier Stressed 0.25-µm AlGaN/GaN HEMTs”, IEEE Electron Device Letter, Vol. 33, No. 11, 2012

[22] R. L-Y. Sah, R. N. Noyce, W. Shockley, „Carrier Generation and Recombination in P-N Junctions and P-N Junction Characteristics“, IRE, Vol. 45, Issue 9, 1957

[23] D. M. Fleetwood, “Bulk oxide traps and border traps in metal-oxide-semiconductor capacitors”, J. of Appl. Phys., 1998, 84, 6141-6148

[24] D. K. Schroder, “Electrical Characterization of Defects in Gate Dielectrics”, CRC Press, Taylor & Francis Group, Boca Raton, 2009

[25] A. L. McWorther, “1/f noise and germanium surface properties”, Semicond. Surface Phys., 1957, p 207-228

[26] T. Grasser, P.-J. Wagner, H. Reisinger, Th. Aichinger, G. Pobegen, M. Nelhiebel, B. Kaczer, „Analytic Modeling of the Bias Temperature Instability Using Capture/Emission Time Maps“, IEDM 2011, p. 27.4.1-27.4.4

[27] K. R. Farmer, R. A. Buhrman, “Defect dynamics and wear-out in thin silicon oxides”, Semicond. Sci. Technol. 4, 1989, p 1084-1105

[28] A. Fontserè, A. Pérez-Tomás, M. Placidi, J. Llobet, N. Baron et al., “Gate current analysis of AlGaN/GaN on silicon heterojunction transistors at the nanoscale”, Appl. Physics Letter, 101, 0935505, 2012

[29] J. R. Jameson, P. B. Griffin, J. D. Plummer, Y. Nishi, “Charge Trapping in High-k Gate Stacks Due to the Bilayer Structure Itself”, IEEE Tr. on Electron Dev., Vol. 53, No. 8, 2006

[30] J. P. Ibbetson, P. T. Fini, K. D. Ness, S. P. DenBaars, J. S. Speck, U. K. Mishra, “Polarization effects, surface states, and the source of electrons in AlGaN/GaN heterostructure field effect transistors”, Applied Physics Letter, Vol. 77, No. 2, 2000

[31] S. Ganguly, J. Verma, G. Li, T. Zimmermann, H. Xing, D. Jena, „Presence and origin of interface charges at atomic-layer deposited Al2O3/III-nitride heterojunctions“, Appl. Phys. Lett., 2011, 99, 193504

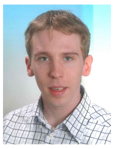
[32] S. Yang, Z. Tang, K-Y. Wong, Y.-S. Lin, Y. Lu, S. Huang, K. J. Chen, “Mapping of Interface Traps in High-Performance Al2O3/AlGaN/GaN MIS-Heterostructures Using Frequency- and Temperature-Dependent C-V Techniques, Proc. of the IEDM, 2013, pp. 6.3.1-6.3.4

[33] J. Joh, J. del Alamo, “Current-Transient Methodology for Trap Analysis for GaN High Electron Mobility Transistors Electron Devices”, IEEE Transactions on, 2011, 58, 132 -140

[34] W. Choi, H. Ryu, N. Jeon, M. Lee, H.-Y. Cha, K.-S. Seo, “Improvement of Vth Instability in Normally-Off GaN MIS-HEMTs Employing PEALD-SiNx as an Interfacial Layer”, IEEE Electron Device Letters, Vol. 35, No. 1, 2014

[35] P. Lagger, C. Ostermaier, (measurement report), unpublished results

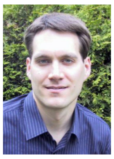
[36] T. Grasser, P.-J. Wagner, H. Reisinger, T. Aichinger, G. Pobegen, M. Nelhiebel, B. Kaczer, “Analytic modeling of the bias temperature instability using capture/emission time maps”, Electron Devices Meeting (IEDM), 2011 IEEE International, 2011, 27.4.1 -27.4.4



Peter Lagger received his master’s degree in electrical engineering from Vienna University of Technology in 2011. He is currently working towards his Ph.D. degree at Vienna University of Technology in cooperation with Infineon Technologies Austria AG. His main research interests include characterization and technology of GaN based power devices.

Maria Reiner received her master’s degree in chemistry after graduating from the University of Graz in 2011. Since 2012 she is working towards her Ph.D. degree in surface chemistry and analysis at the University of Kassel in cooperation with Infineon Technologies Austria AG. Her central topic is the understanding and modification of the surface and interface of group-III-nitrides.

Dionyz Pogany received the Dipl.-Ing. degree in solid state engineering from the Slovak Technical University in Bratislava, Slovakia in 1987, and the Ph.D. degree from INSA de Lyon, France in 1994. Since 1995 he is with the Vienna University of Technology (Assoc. Prof. since 2003) where he works mostly on device characterization.



Clemens Ostermaier has received his master’s degrees from Vienna University of Technology and Kyungpook National University, South Korea, in microelectronics and semiconductor engineering in 2008. In 2011 he received his Ph.D. in electrical engineering from Vienna University of Technology. His main interests have been around the technology and device design of GaN devices including reliability aspects. He is currently working at Infineon Technologies Austria AG in the field of GaN technology development.

4.7 Enhancement of V_{th} Drift for Repetitive Gate Stress Pulses due to Charge Feedback Effect in GaN MIS-HEMTs

Authors	P. Lagger, D. Pogany and C. Ostermaier
Published In	Proceedings of the IEEE International Reliability Physics Symposium
Year	2014
Pages	6C.3.1 - 6C.3.6
Conference Location	Waikoloa, Hawaii, United States of America
Presentation	Oral Presentation

Enhancement of V_{th} Drift for Repetitive Gate Stress Pulses due to Charge Feedback Effect in GaN MIS-HEMTs

P. Lagger, C. Ostermaier
Infineon Technologies Austria AG
Siemensstraße 2
9500 Villach, Austria
peter.lagger@infineon.com

D. Pogany
Vienna University of Technology
Floragasse 7
1040 Wien, Austria
dionyz.pogany@tuwien.ac.at

***Abstract*—An unexpected enhancement of V_{th} drift (ΔV_{th}) in GaN MIS-HEMTs induced by repetitive forward gate bias stress pulses in contrast to single pulses is found. Further, it is revealed that the slope of ΔV_{th} recovery curves decreases for increasing intermediate-recovery time t_i, i.e. the recovery time in between individual stress pulses. The observed behavior is explained by the interaction of the 2DEG channel with the dielectric/III-N interface via the III-N barrier during (repetitive) stress, for which a charge feedback mechanism plays a crucial role.**

Keywords – repetitive stress pulses; forward gate bias stress; threshold voltage drift; AlGaN, GaN; MIS-HEMT; bilayer gate stack, Coulomb charging, charge feedback mechanism, capture emission time map

I. INTRODUCTION

Threshold voltage drifts induced by forward gate bias stress are a severe problem for GaN MIS-HEMTs [1, 2, 3, 4, 5]. A broad distribution of characteristic stress/recovery time constants over many decades was found recently [3, 4, 5]. These studies focus mostly on the degradation induced by single stress pulses. Although normally-on GaN-HEMTs are usually operated at gate biases $V_G < 0$, stress pulses with $V_G > 0$ can occur during switching the device to on-state (e.g. due to overshoot) [4]. The investigation of repetitive stress is thus of major concern for the reliability of these devices.

In this work, we investigate V_{th} drifts due to repetive stress with varying stress bias $V_{G,stress}$, stress time of each individual stress pulse t_s and intermediate-recovery time t_i. It is found that the slope of ΔV_{th} recovery curves (i.e. $|dV_{th}/d\log(t_r)|$) after repetive stress pulses is decreasing with the number of pulses N, i.e. the V_{th} drift gets more permanent. This result is discussed by means of the so-called capture-emission time (CET) map [3, 5, 6, 7, 8, 9] and in addition a link to previously reported observations of higher-order capture/emission kinetics in these devices is made [5]. Moreover, a changing slope of the recovery curves after repetitive stress pulses in dependency of t_i is found. Further an enhancement of ΔV_{th} due to repetitive stress ($V_G > 0$) compared to continous stress with a stress time of $N \cdot t_s$ can be observed under certain stress conditions. Thus the V_{th} drift due to repetitive stress, as one would expect in an application, cannot be directly estimated from a continuous stress test. The observations are ascribed to an electrostatic feedback mechanims in the double layer gate stack composed of III-N barrier and dielectric.

	V_G	V_D
Stress	$V_{G,stress} > 0$	0
Intermediate-Recovery	0	0
Recovery	0	0
ΔV_{th}-measurement	$V_{G,meas} < 0$	$V_{D,meas} > 0$

Tab. 1 Overview of gate bias V_G and drain bias V_D for the different phases of electrical stress tests. The source bias V_S is always 0 V (ground potential).

II. EXPERIMENTAL SETUP

The test devices are fabricated on GaN-on-Si wafers. The gate stack consists of a 30 nm SiO_2, a 3 nm GaN cap, and a 25 nm $Al_{25}Ga_{75}N$ barrier. The test devices have a gate length and width of 1.3 µm and 480 µm, respectively. The wafer surface is cleaned with a HF dip prior to dielectric deposition. The

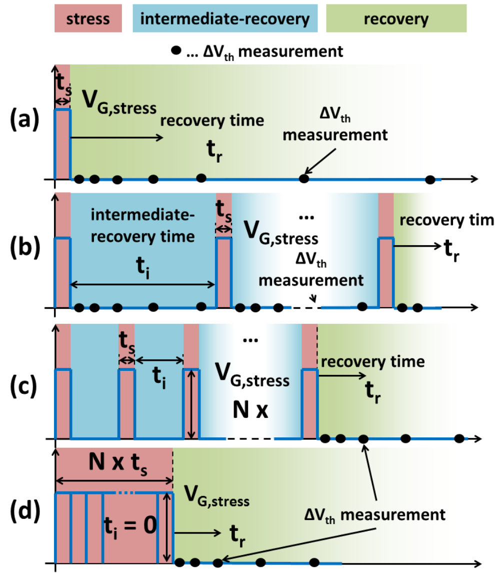


Fig. 1. Schematic of the pulse pattern used for different stress modes: (a) continuous stress, (b) repetitive stress with ΔV_{th} monitoring during intermediate-recovery, (c) repetitive stress without monitoring and (d) equivalent continuous stress. The stress parameters are forward gate bias $V_{G,stress}$, number of stress pulses N, duration of an individual stress pulse t_s, intermediate-recovery time in between each individual stress pulses t_i.

dielectric is deposited by a low-pressure chemical vapor deposition process. This is followed by a post-annealing at 1000 °C under N_2 atmosphere for 1 min. The nominal threshold voltage of the devices is -12 V.

The electrical stress tests are divided into three different phases: 1) stress, 2) recovery, and 3) ΔV_{th} measurement, cf Tab. 1. During stress, a forward gate stress bias $V_{G,stress}$ is applied for a stress time t_s, while the drain and source contacts are grounded. The recovery is performed with all device contacts grounded. The same holds for intermediate-recovery, i.e. recovery in between consecutive stress pulses (Fig 1b, c). The transient of ΔV_{th} is recorded at measurement bias conditions $V_{G,meas}$ and $V_{D,meas}$. Details can be found in [4]. These three phases are combined to different stress modes, cf. Fig. 1. The simplest form is continuous stress, where the V_{th} drift is recorded after a single stress pulse (Fig. 1a). A comprehensive study about continuous stress is made in [5]. For repetitive stress, we distinguish between repetitive stress with (Fig. 1b) and without monitoring (Fig. 1c) of ΔV_{th} during intermediate-recovery. The reason for this is that monitoring is limited by the minimum measurement delay of 4 µs. For each stress test a virgin device is used to ensure defined initial conditions. In Fig. 2 a sample record of the gate signal for repetitive stress (cf. Fig. 1c) is given.

III. EXPERIMENTS

A. *Repetitive Stress with Monitored Intermediate-Recovery*

In Fig. 3a the recovery of V_{th} is shown for repetitive stress, where the V_{th} recovery is recorded after each consecutive stress pulse (see stress sequence in Fig. 1b). The V_{th} drift increases with the number of stress pulses N, while the slope of the recovery curves slightly decreases. This means that with increasing N, the degradation is more permanent, i.e. less recovery within the same intermediate-recovery time t_i. In addition, the difference between consecutive curves gets smaller. In Fig. 3b, the extraction of the V_{th} drift at two fixed recovery times t_{r1} and t_{r2} is plotted over the logarithm of N. This reveals a logarithmic increase with N for the overall V_{th} drift for both extraction times. Moreover, it is remarkable that the slope of the curve extracted at $t_r = t_{r2}$ is steeper than those of the curve extracted at $t_r = t_{r1}$. Hence, the difference of the two curves shows a declining trend, i.e. the total value of V_{th} recovery between t_{r1} and t_{r2} declines with increasing N.

B. *Repetitive Stress with Varying Intermediate-Recovery*

From the application point of view, the repetitive stress test can be used to mimic the appearance of positive overshoot pulses [4]. These can occur due to parasitic elements in the switching circuit. The intermediate-recovery time t_i is a measure for the repetition frequency of these pulses. The influence of a varying intermediate-recovery time t_i (i.e. varying repetitive frequency) is investigated in this section. In order to ensure identical test conditions for all tests, the monitoring of intermediate-recovery is not applied in this section (see stress sequence in Fig. 1c).

A comprehensive overview of ΔV_{th} recovery after repetitive stress under various stress conditions is given in Fig. 4. The intermediate-recovery time t_i is varied from 100 ns up to 100 s. The number of stress pulses is kept constant at N = 100. Stress biases $V_{G,stress}$ of 2, 3 and 4 V and stress times t_s of 1µs, 1 ms and 1 s are chosen. The recovery curves for continuous stress with stress times t_s and $N \cdot t_s$ are given for comparison. Since under repetitive stress conditions the V_{th} drift is recovered in between each stress pulse, one could expect that ΔV_{th} induced by continuous stress for a total stress time of $N \cdot t_s$ (Fig. 1d) gives an upper limit for ΔV_{th} induced by repetitive stress [8, 9].

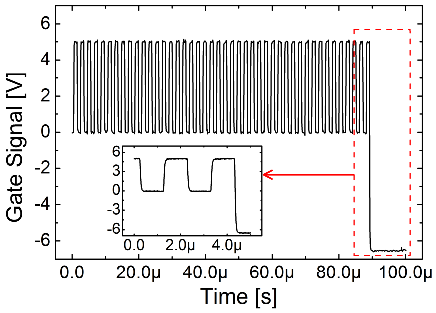


Fig. 2 Oscilloscope record of the pulse pattern for stress parameters $V_{Gstress}$ = 5 V, t_s = 1 µs, and t_i = 1 µs. The sampling rate of the oscilloscope is 10 MSa/s (250 MSa/s in the inset). No spikes occur during switching, which might hypothetically explain the enhancement of ΔV_{th} after repetitive stress. After the stress pulses, the bias is directly switched to measurement conditions [4].

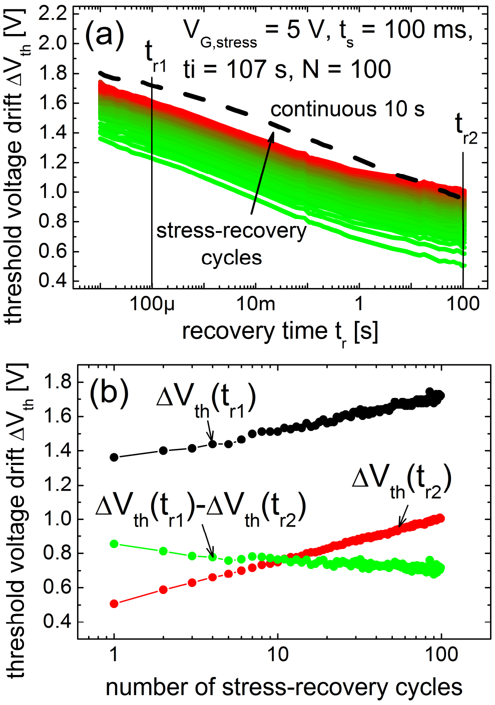


Fig. 3 (a) Recovery curves for repetitive stress according to Fig. 1b, with N = 100, $V_{G,stress}$ = 5 V, t_s = 100 ms, t_i = 107 s. The dashed black line shows a ΔV_{th} curve for continuous stress with a stress time of $N \cdot t_s$ = 10 s for comparison. Note that the notation recovery time t_r in this example is used also for the intermediate-recovery time t_i for simplicity, cf. Fig. 1b. (b) Extraction of ΔV_{th} at two different t_{r1} = 100 µs and t_{r2} = 100 s for the data in (a).

Fig. 4 reveals an enhancement of V_{th} drift for short t_i induced by repetitive stress over a wide range of t_r against continuous stress with a stress time of $N \cdot t_s$. In particular, for a $V_{G,stress}$ of 3 V the effect is most pronounced (Fig. 4d-f). For a $V_{G,stress}$ of 2 and 4 V a significant enhancement is only observed for a t_s of 1 s (Fig. 4c and Fig. 4j). Further, the slope of ΔV_{th} recovery curves decreases with increasing t_i, i.e. more recovery processes with longer recovery time constants in relation to shorter ones are activated. It is remarkable that the recovery curves for $t_i \leq t_s$ are practically identical, while for further increasing t_i, ΔV_{th} for short t_r tends to decrease and for longer t_r it tends to increase, cf. e.g. Fig. 4d. Another interesting observation is that for a $V_{G,stress}$ of 2 V for all t_s and for 3 V up to t_s = 1 ms, the overall V_{th} drift increases for a t_i of 100 s in comparison to shorter t_i (Fig. 4a-e). In addition, it is found that V_{th} drift due to continuous stress with a stress time of t_s is a lower limit for V_{th} drift after pulsed stress.

A change of the curvature of ΔV_{th} curves in Fig. 4 from concave to convex for continuous stress with increasing t_s is found, which is in accordance to the observations in [5].

IV. DISCUSSION

The discussion is organized according to the experimental results in Part III. In section IV.A, the observation that the slope of recovery curves tends to decrease with increasing N (cf. Fig. 3) is discussed using the concept of CET maps. In section IV.B a model of the double-layer gate stack is presented, which is connected to the following observations in Fig. 4: 1) Enhancement of V_{th} drift in comparison to continuous stress, and 2) V_{th} drift tends to be more permanent for increasing t_i. The observation that the enhancement is particularly pronounced for a $V_{G,stress}$ of 3 V (cf. Fig. 4d-f) is linked to rate limiting properties of the barrier occurring at low $V_{G,stress}$ and to formation of an second channel for higher $V_{G,stress}$, which was previously reported in [5].

A. *Capture Emission Time Map*

The V_{th} drift is explained in terms of capture and emission of electrons at the dielectric/III-N interface (shortly called interface in the following) and at border states in the dielectric [3, 5]. The density of interface trapped charges Q_{it} increases during stress and decreases during recovery ($V_G = 0$). After a stress pulse with a magnitude of $V_{G,stress}$ and a duration of t_s, in a first-order approximation, all defects with a capture time constant $\tau_c \leq t_s$ are occupied. In Fig 5a the occupied area of the so-called capture-emission time (CET)-map for this scenario is sketched. In general a CET-map depicts the density of ΔV_{th} in the capture-emission time (τ_c, τ_e) space for a certain $V_{G,stress}$ [5, 6, 7, 8, 9]. The overall V_{th} drift for a certain combination of t_s and t_r is directly obtained by integrating over the corresponding area of the CET map according to

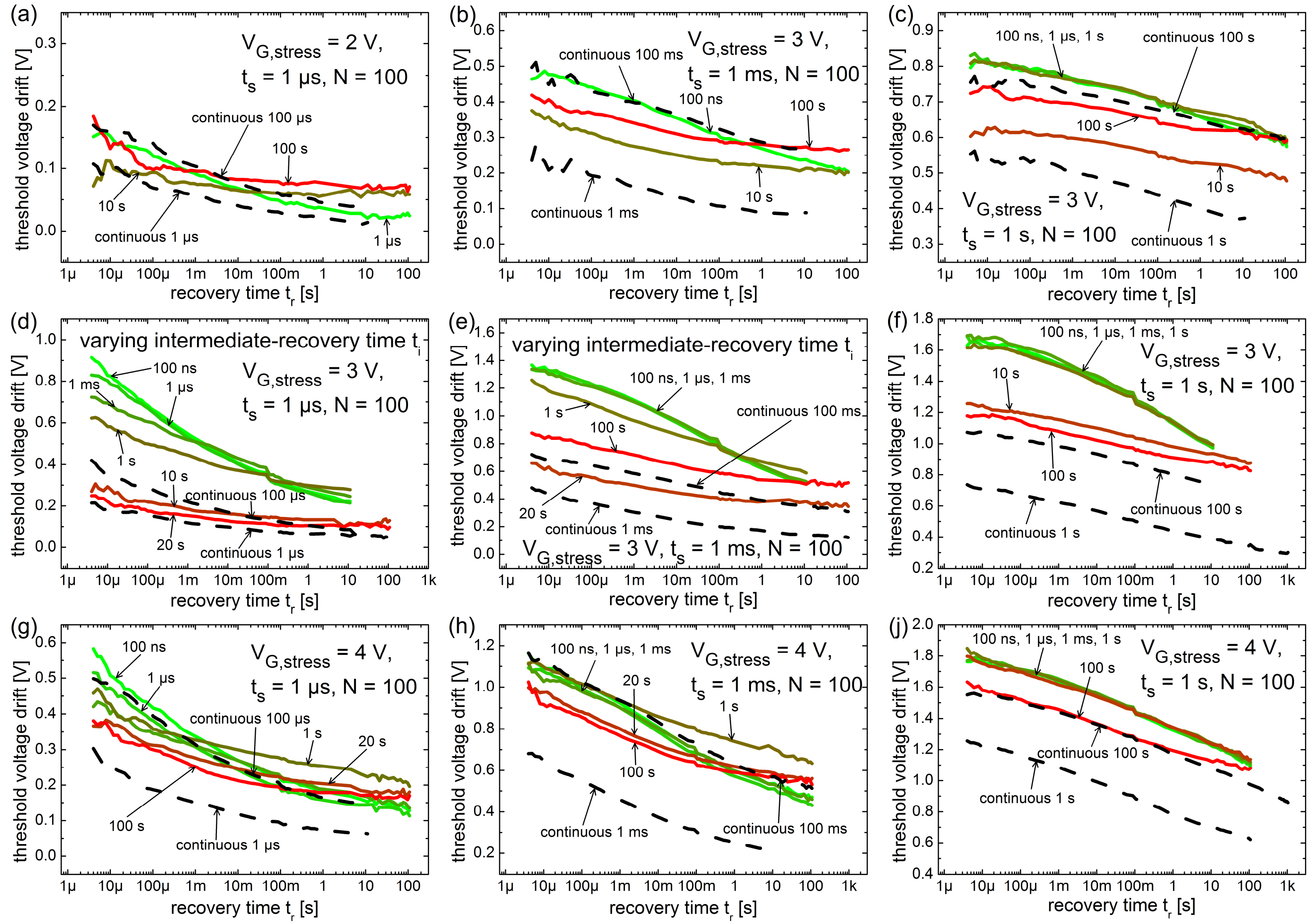


Fig. 4. Recovery curves of ΔV_{th} after repetitive stress according to Fig. 1c, with varying t_i from 100 ns up to 100 s, $V_{G,stress}$ from 2 to 4 V, and N = 100 for (a) t_s = 1 µs, (b) t_s = 1 ms and (c) t_s = 1s. The dashed curve corresponds to continuous stress (cf. Fig. 1a) with stress time of t_s and $N \cdot t_s$.

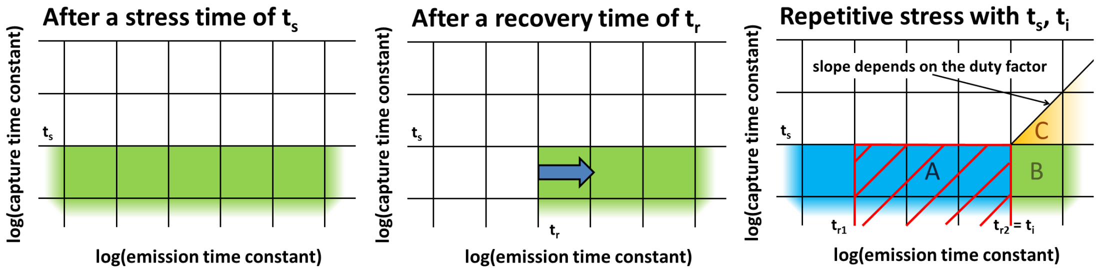

After a stress time of t_s
After a recovery time of t_r
Repetitive stress with t_s, t_i
log(capture time constant)
log(emission time constant)
t_s
t_r
slope depends on the duty factor
A
B
C
t_{r1}
$t_{r2} = t_i$

Fig. 5. In (a) the occupancy of the CET-map after a stress pulse with stress time t_s is shown. All defects up to a capture time constant of the stress time are filled. During recovery, defects with emission time constants smaller than the recovery time are emptied (b). In (c) the occupancy of the CET-map for repetitive stress is shown. Three different regions are identified: Region A is repetitively filled and emptied during each stress-recovery cycle. Region B is filled during the first pulse and is not affected by consecutive stress-recovery cycles. In region C, a pile-up due to consecutive stress-recovery cycles is observed. The slope of the region C depends on the duty factor between t_s and t_i, details can be found in [9].

$$\Delta V_{th}(t_s,t_r) = \int_{-\infty}^{ts} \int_{tr}^{+\infty} g(\tau_c,\tau_e)\, d\tau_c\, d\tau_e, \qquad (1)$$

where $g(\tau_c,\tau_e)$ is the density of ΔV_{th}. The integration area is equal to the occupied area of the CET-map. For first-order capture/emission kinetics it is shown that $g(\tau_c,\tau_e)$ is not changing for repetitive stress [8, 9]. During subsequent recovery after the stress pulse, all defects with an emission time constant $\tau_e \leq t_r$ are emptied, cf. Fig. 5b.

The situation for repetitive stress [8, 9] is described in Fig. 5c, where three different regions can be identified: Region A is charged and discharged during each consecutive stress-recovery cycle. Region B is filled during the first stress pulse and does not emit during intermediate-recovery, whereas region C is build up during repetitive stress-recovery cycles [8, 9]. In Fig. 5c the region between t_{r1} and t_{r2} is marked. The integral over this region is equal to $\Delta V_{th}(t_{r1})$ - $\Delta V_{th}(t_{r2})$, cf. Fig. 3b. However, the observation of declining $\Delta V_{th}(t_s,t_{r1})$ - $\Delta V_{th}(t_s,t_{r2})$ means that $g(\tau_c,\tau_e)$ is decreasing in this region with increasing number of stress pulses and thus also the number of emitted electrons. This could be due to 1) the number of defects, which are filled during stress in region A is declining in the sense that they are not accessible during stress anymore, or 2) the emission time constant of these defects is changed with time, i.e. the disappear in region A (Fig. 5c). However, $g(\tau_c,\tau_e)$ changes with N, indicating a higher-order defect kinetics. For a time-invariant $g(\tau_c,\tau_e)$, i.e. first-order capture/emission kinetics, a parallel shift of recovery curves for repetitive stress would be observed. The behavior is further consistent with the observation of the decreasing slope of ΔV_{th} recovery curves for increasing stress time t_s [5]. In [5] a $g(\tau_c,\tau_e) < 0$ is reported as a sign of higher-order defect kinetics, which is explained by complex defect dynamics, e.g. defect-to-defect interactions, multi-state defects, feedback effects, etc. We speculate that this is directly connected to the observation of decreasing $g(\tau_c,\tau_e)$ for increasing N.

The overall build-up of V_{th} drift with increasing number of repetitive stress pulses (Fig. 3a) can be explained by the charging of defects in region B and C, where $\tau_e > t_i$ (Fig. 5c).

B. Gate Stack Model

In this section, a model is presented, which explains the experimental observations by a charge feedback mechanism during stress ($V_G > 0$). The change of Q_{it} for a constant V_G changes accordingly the barrier potential Φ_B, i.e. the potential of the conduction band minimum at the interface, and therefore also the bias distribution between dielectric $v_D(t)$ and barrier $v_B(t)$. In Fig. 6, the change of Φ_B for increasing V_G is sketched. The equivalent circuit model (Fig. 7a) from [10] is used to explain our results. There, the non-linear barrier resistance R_B mimics the net current i_B of electrons between the 2DEG channel and the interface states via the barrier. In a transient situation, after the application of $V_G > 0$, the barrier resistance R_B reaches finite values. The net current flux i_B increases with decreasing Φ_B [11]. The distribution of v_D and v_B for a step function (transition from 0 V to V_G at t = 0) are given explicitly for time t = 0:

$$v_D(t = 0) = V_D(V_G) = V_G\,[C_B/(C_B+C_D)], \qquad (2a)$$
$$v_B(t = 0) = V_B(V_G) = V_G\,[C_D/(C_B+C_D)], \qquad (2b)$$
$$v_D(t) = V_D + \Delta\Phi_B(\Delta Q_{it}), \qquad (2c)$$
$$v_B(t) = V_B - \Delta\Phi_B(\Delta Q_{it}). \qquad (2d)$$

with capacitances C_B and C_D of the barrier and the dielectric. The interface is charged with electrons provided by the 2DEG channel via the barrier during constant $V_{G,stress} > 0$. Moreover, we assume that the potential in the channel is fixed due to strong electron accumulation. Hence, the change of the barrier

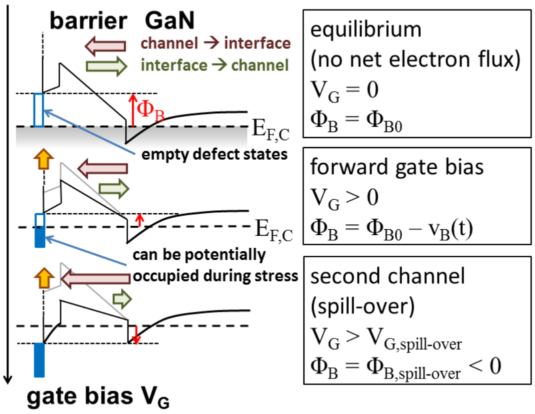


Fig. 6. Decrease of the barrier potential Φ_B for increasing V_G. The red and green arrows show the electron flux from the channel to defect states located at the interface and vice versa. The bottom sketch shows an accumulation of electrons in a second channel at the interface. The yellow arrow indicates the change of Φ_B due to the charge feedback effect. For a defect free interface there is no feedback, because $\Delta Q_{it} = 0$ and so also $i_B \rightarrow 0$. For the case of spill-over ($i_B \rightarrow 0$ and $R_B \rightarrow \infty$).

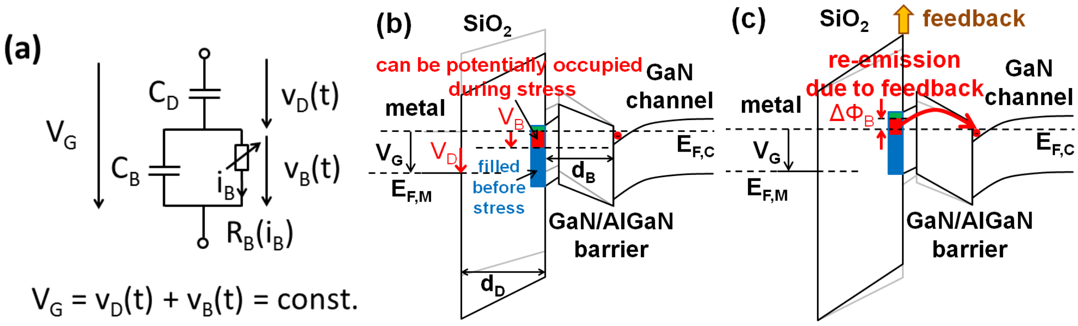

(a)
V_G
C_D
$v_D(t)$
C_B
i_B
$v_B(t)$
$R_B(i_B)$
$V_G = v_D(t) + v_B(t) = \text{const.}$
(b)
SiO_2
can be potentially occupied during stress
GaN channel
metal
V_B
V_G
V_D
filled before stress
$E_{F,M}$
d_B
$E_{F,C}$
GaN/AlGaN barrier
d_D
(c)
SiO_2
feedback
re-emission due to feedback
GaN channel
metal
$\Delta\Phi_B$
V_G
$E_{F,C}$
$E_{F,M}$
GaN/AlGaN barrier

Fig. 7. (a) Equivalent large signal circuit model of the gate stack for $V_G > 0$. The transport mechanism of electrons from the channel to interface defects is assumed to be e.g a combination of thermionic emission and defect assisted tunneling, which is enhanced with decreasing Φ_B. (b) Bandstructure of the gate stack in thermal equilibrium (gray) and for $V_G > 0$ (black). For $V_G > 0$, the barrier potential is lowered from its thermal equilibrium value Φ_{B0} to Φ_B, cf. Fig. 3. Under these conditions, the channel acts as an electron reservoir, which provides electrons to interface and border defect states in the region below the channel Fermi level $E_{F,C}$. (c) Charging of the interface increases Φ_B and consequently electrons can be re-emitted from the region lifted above $E_{F,C}$.

potential Φ_B during stress, i.e. $\Delta\Phi_B$, is governed by the parallel circuit of C_D and C_B (cf. Fig. 7a):

$$\Delta\Phi_B(\Delta Q_{it}) = \Delta v_B(t) = -\Delta v_D(t) = -\Delta Q_{it} / (C_B + C_D). \qquad (3)$$

$\Delta\Phi_B$ is further related to ΔV_{th} via $\Delta Q_{it} = C_D \cdot \Delta V_{th}$. For the structure investigated in this paper, the following values are estimated from this model with the simplification that the dielectric constant of the AlGaN barrier and the GaN cap are equal: $V_D/V_G = 0.73$, $V_B/V_G = 0.27$, $\Delta\Phi_B/\Delta V_{th} = 0.27$ and $\Delta N_{it}/\Delta V_{th} = 7.2 \cdot 10^{11}\ \text{cm}^{-2}/\text{V}$.

Under $V_G > 0$ conditions, the charging process continues until a steady-state is established ($d\Delta Q_{it}/dt = 0$). In this case $i_B \rightarrow 0$ and $R_B \rightarrow \infty$. However, there is no indication for such behavior, because ΔV_{th} is increasing on a logarithmic time-scale for stress times of at least 10 ks, without indicating saturation [3, 5].

The barrier voltage drop V_B defines the region at the interface which is drawn below the channel Fermi-level $E_{F,C}$ (called active energy region (AER) in the following) and therefore the number of potentially accessible defect states [7], cf. Fig. 7b. The evolution of the barrier potential during continuous and repetitive stress is depicted in Fig. 8. During stress electrons are trapped in defect states at the interface and hence $\Delta\Phi_B$ is increasing, which also lifts parts of the AER above $E_{F,C}$ according to ΔQ_{it}, cf. Fig. 7c. During intermediate-recovery $\Delta\Phi_B$ is decreasing, due to recovery processes faster than t_i. The longer t_i, the more electrons are emitted and the smaller the remaining $\Delta\Phi_B$ at the beginning of the next stress pulse. In contrast, Φ_B is continuously increasing during continuous stress (dotted line in Fig. 8). The initial voltage drop V_B at the beginning of each consecutive stress pulse is independent of $\Delta\Phi_B$ (Eq. 2a, b), but the higher the remaining $\Delta\Phi_B$ due to previous stress pulses, the smaller the size of the AER and the lower the probability for electrons to overcome the barrier. In addition, it means that the barrier potential is increased for each consecutive stress pulse $\Phi_{B,n+1} > \Phi_{B,n}$, where n is the index of consecutive stress pulses. Hence the trap energy levels in reference to the Fermi-level E_F at the interface are shifted accordingly [5].

Moreover, also re-emission during stress from the lifted parts is possible. This might explain the decrease of fast recovery components with increasing t_s (cf. decreasing slope of ΔV_{th} curves for continuous stress in Fig. 4).

The decrease of ΔV_{th} with increasing t_i for short t_r can be explained by "decoupling" of repetitive pulses due to emission of electrons during intermediate recovery (i.e. for $t_i \rightarrow \infty$ the

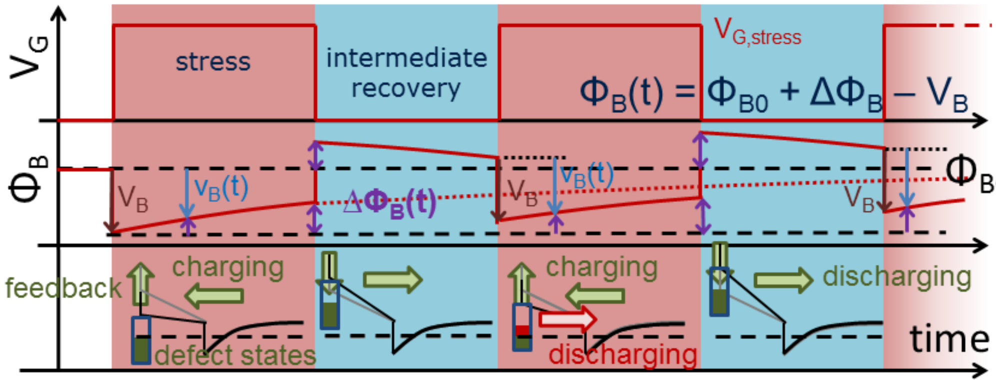

V_G
stress
intermediate recovery
$V_{G,stress}$
$\Phi_B(t) = \Phi_{B0} + \Delta\Phi_B - V_B$
Φ_B
V_B
$v_B(t)$
$\Delta\Phi_B(t)$
V_B
$v_B(t)$
V_B
Φ_{B0}
feedback
charging
defect states
charging
discharging
discharging
time

Fig. 8. Change of the barrier potential during repetitive stress. Directly after V_G is applied, Φ_B drops by V_B. In the following a net current towards the interface is induced. The overall change of Φ_B due to change of Q_{it} is given by $\Delta\Phi_B$. During intermediate recovery $\Delta\Phi_B$ is decreased due to emission of trapped electrons. The barrier potential Φ_B is changed by the same amount V_B at the beginning of each stress pulse. Further, the relation of Φ_B and V_G is time-variant and consequently also $R_B(V_G)$. The evolution of Φ_B for continuous stress is shown by the dotted line for comparison.

pulsed stress equals continuous stress with stress time t_s, under the assumption of full-recovery after each pulse).

The increase of ΔV_{th} for longer t_r with increasing t_i (see e.g. curves for t_i = 1 µs up to 1 s in Fig. 4d) might be explained by the enhanced relaxation of $\Delta\Phi_B$ during intermediate recovery, which causes an increased electron transfer to the interface at the beginning of the consecutive pulse due to effective lower Φ_B compared to continuous stress or shorter t_i. The increase of ΔV_{th} for short t_i could be due to fast increase of Φ_B, which is caused by defects with capture/emission time constants in the sub-µs regime. This would limit charging most efficiently for continuous stress.

If we assume that Φ_B is in the order of 1 eV, the spill-over voltage is estimated to be in the order of 4 V. In [5], a V_{th} drift-limiting barrier effect (i.e. the onset in strong ΔV_{th} increase) for small $V_{G,stress}$ and short t_s is observed. We speculate that for $V_{G,stress}$ = 2 V this limiting effect is still significant and that for $V_{G,stress}$ = 4 V already a second channel at the interface is formed (spill-over), which might be connected to the fact that the ΔV_{th} enhancement is especially pronounced for $V_{G,stress}$ = 3 V.

V. CONCLUSION

The investigations of the threshold voltage drift of GaN based MIS-HEMTs under repetitive stress can be summarized as follows:

1. The V_{th} drift for repetitive stress is enhanced in comparison to continuous stress under certain conditions.
2. The V_{th} drift gets more permanent for increasing intermediate-recovery time.
3. The V_{th} drift is increasing on a logarithmic scale with the number of stress pulses.
4. The slope of recovery curves after each consecutive stress pulse decreases, i.e. the drift gets more permanent with every additional pulse.
5. The experimental data is qualitatively explained by a charge feedback mechanism in the double-capacitive gate structure.

In the SiO_2/Si system the ΔV_{th} enhancement for repetitive over continuous stress is not observed [8, 9]. This is, in contrast to our structure, due to the direct exchange of charge carriers between defects and MOS-channel and related first order stress/recovery kinetics.

For a life-time estimation of maximum ΔV_{th} for normally-on MIS-HEMTs, a continuous stress test, as standardly used in CMOS, might underestimate the V_{th} drift induced by repetitive stress and hence a repetitive stress test is unavoidable.

REFERENCES

[1] T. Wu, D. Marcon, M. Zahid, M. Van Hove, S. Decoutere, G. Groeseneken, “Comprehensive Investigation of On-state Stress on D-mode AlGaN/GaN MIS-HEMTs”, IRPS, 2013

[2] T. Imada, M. Kanamura, T. Kikkawa, “Enhancement-Mode GaN MIS-HEMTs for Power Supplies”, Int. Pow. Electr. Conf. , 2010, 1027-1033

[3] P. Lagger, C. Ostermaier, G. Pobegen, D. Pogany, “Towards understanding the origin of threshold voltage instability of AlGaN/GaN MIS-HEMTs”, IEDM, 2012, pp.13.1.1-13.1.4

[4] P. Lagger, A. Schiffmann, G. Pobegen, D. Pogany, C. Ostermaier, „Very Fast Dynamics of Threshold Voltage Drifts in GaN-Based MIS-HEMTs“, IEEE Electron Device Letters, Vol. 34, No. 9, 2013

[5] P. Lagger, M. Reiner, D. Pogany, C. Ostermaier, „Comprehensive Study of the Complex Dynamics of Forward Bias-Induced Threshold Voltage Drifts in GaN Based MIS-HEMTs by Stress/Recovery Experiments“, IEEE Tr. on Electron Dev., online, 2014

[6] T. Grasser, P.-J. Wagner, H. Reisinger, T. Aichinger, G. Pobegen, M. Nelhiebel, B. Kaczer, “Analytic modeling of the bias temperature instability using capture/emission time maps”, Electron Devices Meeting (IEDM), 2011 IEEE International, 2011, 27.4.1 -27.4.4

[7] T. Grasser, “Stochastic charge trapping in oxides: From random telegraph noise to bias temperature instabilities”, Microelectronics Reliability 52, 2012, 39-70

[8] H. Reisinger, T. Grasser, W. Gustin, C. Schlünder, “The statistical analysis of individual defects constituting NBTI and its implications for modeling DC- and AC-stress”, IRPS, 2010, 7-15

[9] H. Reisinger, T. Grasser, K. Ermisch, H. Nielen, W. Gustin, C. Schlünder, “Understanding and modeling AC BTI”, IRPS, 2011, 6A.1.1-6A.a.8

[10] J. R. Jameson, P. B. Griffin, J. D. Plummer, Y. Nishi, “Charge Trapping in High-k Gate Stacks Due to the Bilayer Structure Itself”, IEEE Tr. on Electron Dev., Vol. 53, No. 8, 2006

[11] S. Sze and K. Ng, *Physics of Semiconductor Devices*. New York, USA, Wiley 2006

4.8 Understanding the Fundamental Limitations for the Improvement of Forward Gate Bias Induced V_{th} Drift Stability of GaN Based MIS-HEMTs

Authors	P. Lagger, M. Reiner, G. Denifl, M. Stadtmüller, D. Pogany and C. Ostermaier
Presented At	International Workshop on Nitride Semiconductors
Year	2014
Conference Location	Wroclaw, Poland
Presentation	Oral Presentation

Understanding the Fundamental Limitations for the Improvement of Forward Gate Bias Induced V_{th} Drift Stability of GaN based MIS-HEMTs

P. Lagger[1,2], M. Reiner[1], G. Denifl[1], M. Stadtmüller[1], D. Pogany[2] and C. Ostermaier[1]

[1] *Infineon Technologies Austria AG, Siemensstraße 2, 9500 Villach, Austria*
[2] *TU Wien, Institute of Solid-State Electronics, Floragasse 7, 1040 Wien, Austria*

Motivation The high number of defect states at the dielectric/III-N interface (shortly interface) in GaN based MIS-HEMTs causes tremendous V_{th} drifts (ΔV_{th}) and is the most severe challenge for the development of normally-off MIS-HEMT devices. Recent studies revealed a broad distribution of stress/recovery time constants for different dielectric materials [1, 2, 3]. In this work, we show that the magnitude and dynamics of ΔV_{th} is mostly determined by the electrostatic properties of the gate stack and the measurement conditions itself. Subsequently, we conclude that the density of interface states is much larger than what can be measured electrically. Therefore, the interface quality has only a minor influence on ΔV_{th}. We reveal that the measured ΔN_{it} values, i.e. the number of trapped electrons at the interface per unit area due to $V_G > 0$ stress, vary over more than two orders of magnitude by solely varying the layer thicknesses on wafers sharing the same interface quality. The major role of electrostatics is further proved by the scaling of ΔN_{it} with the dielectric constant k.

Experiments The measurement is based on the monitoring of the transient recovery of ΔV_{th} after stress pulses with a magnitude of $V_G = V_{G,stress}$ and a duration of t_s [2, 3]. Wafers with varying dielectric and III-N barrier thickness, t_D and t_B respectively, are compared, cf. Tab. 1. For all wafers the same deposition process for the SiN_x dielectric is used and hence the interface quality is equivalent. The test devices have a gate length and width of 1.3 µm and 480 µm, respectively. Fig. 1 reveals a strong increase of ΔV_{th} and ΔNit for increasing t_B under the same stress conditions. The connection between ΔV_{th} and ΔN_{it} is given by (1). In Fig. 2, ΔV_{th} and ΔN_{it} are compared for wafers with varying t_D, showing an opposite trend compared to the t_B variation. Fig. 3 shows a nearly constant ΔV_{th} for different dielectric materials, i.e. varying dielectric constant k, for the same stress conditions, while ΔN_{it} increases with k.

Discussion The large-signal equivalent circuit model of the gate stack [3, 4] is used to explain the experimental results, cf. Fig. 4a. Fig. 4b shows the bandstructure of the gate stack for $V_G > 0$, where the barrier potential Φ_B is decreased by V_B. Values for V_B/V_G according to (2) are given in Tab. 1. Fig. 5 shows the ΔV_{th} data of Fig. 1-2, where the V_G-axis is scaled by V_B/V_G. This clearly demonstrates the role of the barrier (V_B) for the charging of the interface. Fig. 5b shows that ΔN_{it} for wafers 1-3 is very similar, while the ΔN_{it} of wafer 5 is significantly lower and wafer 4 shows a transition from low to high ΔN_{it}. The deviation of wafer 4-5 could be due to the down-scaling of the dielectric electrical field strength E_D with increasing t_D, which might influence the trapping behavior at the interface. Interestingly, the increase in ΔN_{it} with k in Fig. 3b is compensated by the decreasing $\Delta N_{it}/\Delta V_{th}$ (cf. Tab. 1) and ΔV_{th} is nearly constant Fig. 3a. This is explained by the increase of V_B/V_G with k, cf. (2).

Conclusion Our results indicate that ΔV_{th} is mainly influenced by the change of the barrier potential V_B, because the interface density is still too high to have a significant impact. In [1], a ΔN_{it} improvement by a factor of 2 for different deposition processes is observed, while we demonstrate that simple t_D variations change ΔN_{it} by more than two decades. The V_{th} drift increases with V_G and t_s, which further suggests that the upper limit for ΔV_{th} is set by the stress and measurement conditions itself [2, 3]. A fundamental limit of the electrical measurement is given by $(k \cdot E_{crit})/q < \Delta N_{it,max}$, where E_{crit} is the critical electric field strength for the dielectric breakdown [3]. Moreover, the model in Fig. 4a implies that $\Delta V_{th} \leq V_{G,stress}$, because the distribution of V_G is distributed to the dielectric with ongoing stress [3]. The observations described in this paper are crucial for the interpretation of ΔV_{th} and ΔN_{it} data.

[1] W. Choi et al., IEEE EDL, Vol. 35, No. 1, 2014
[2] P. Lagger et al., Proc. of the IRPS 2014
[3] P. Lagger et al., IEEE Tr. on Electron Dev., online, 2014
[4] J. R. Jameson et al., IEEE TED, Vol. 53, No. 8, 2006

Wafer	t_D [nm]	t_B [nm]	V_B/V_G	$\Delta N_{it}/\Delta V_{th}$ [$cm^{-2}\ V^{-1}$]
1	25	21	0.40	$1.55 \cdot 10^{12}$
2	10	10	0.44	$3.87 \cdot 10^{12}$
3	25	10	0.24	$1.55 \cdot 10^{12}$
4	40	10	0.16	$9.67 \cdot 10^{11}$
5	75	10	0.09	$5.16 \cdot 10^{11}$

Tab. 1. Overview of wafers with a SiN_x dielectric (k = 7) used for the experiments with varying dielectric thickness t_D and barrier thickness t_B. In addition, the change of the barrier potential V_B normed to the applied gate bias V_G and $\Delta N_{it}/\Delta V_{th}$ are given. $\Delta N_{it}/\Delta V_{th}$ is used for the translation of the measured ΔV_{th} values to equivalent ΔN_{it}. It is a measure for the sensitivity of the gate stack to changes of the interface charge density $q \cdot \Delta N_{it}$. The values are calculated using (1) and (2). All samples have an AlGaN barrier with an Al-content of 20%. All wafers have the same buffer structure. Further, the wafers 2-5 have the same barrier structure. All wafers share the same process for SiN_x deposition.

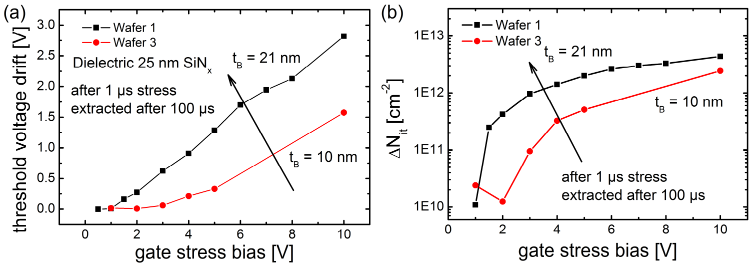


Fig. 1. Threshold voltage drift ΔV_{th} (a) and the according number of interface trapped charges ΔN_{it} (b) are compared for different barrier thickness t_B of 10 nm (wafer 3) and 21 nm (wafer 1) for varying gate stress bias $V_{G,stress}$ and constant stress time t_s = 1 µs.

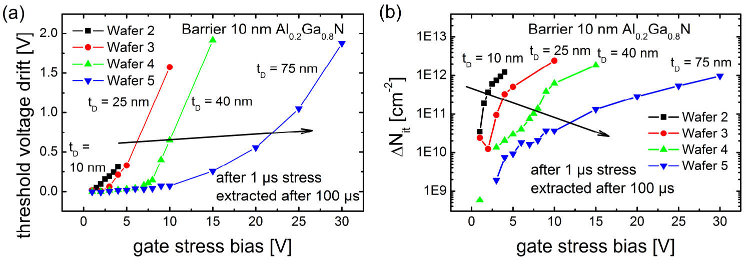


Fig. 2. Impact of the dielectric thickness t_D on ΔV_{th} (a) and ΔN_{it} (b) for wafers 2-5 for varying gate stress bias $V_{G,stress}$ and constant stress time t_s = 1 µs.

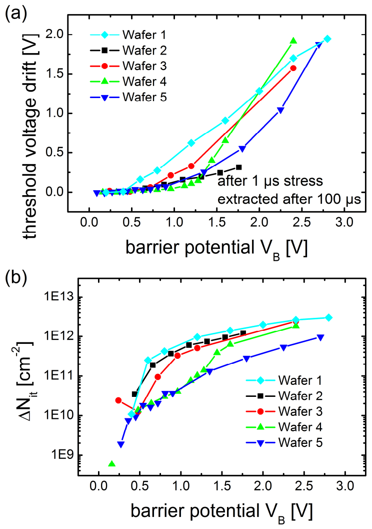


Fig. 5. ΔV_{th} (a) and ΔN_{it} (b) data from Fig. 1 and Fig. 2 plotted as a function of the barrier potential V_B, cf (2).

$$(1)\ \Delta V_{th} = q \cdot \Delta N_{it}/C_D$$
$$(2)\ V_B/V_G = C_D/(C_D+C_B)$$

Formulas: ΔV_{th} is the threshold voltage drift, q is the elementary charge, ΔN_{it} is density of electrons trapped during electrical stress with a gate bias $V_G > 0$, C_D and C_B are the dielectric and barrier capacitances, V_B is the change of the barrier potential for $V_G > 0$.

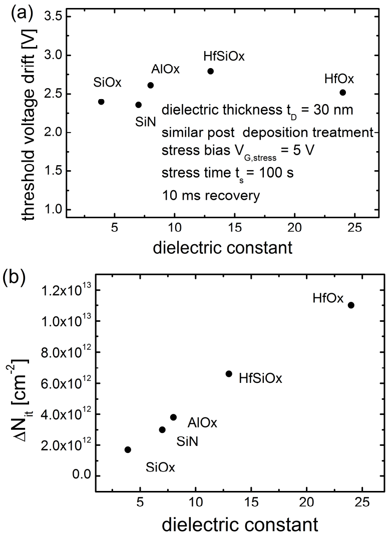


Fig. 3. Influence of the dielectric constant k on ΔV_{th} (a) and ΔN_{it} (b) under the same stress conditions for comparable wafers. The thickness of the dielectric is 30 nm.

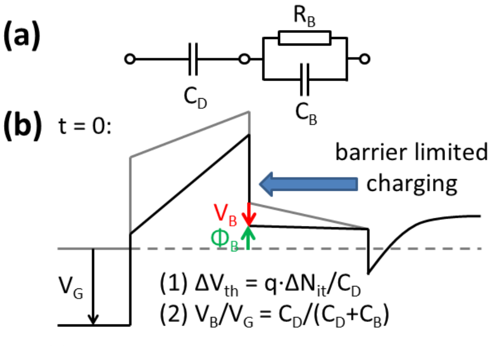

(a)
R$_B$
C$_D$
C$_B$
(b)
t = 0:
barrier limited charging
V$_B$
Φ$_B$
V$_G$
(1) ΔV$_{th}$ = q·ΔN$_{it}$/C$_D$
(2) V$_B$/V$_G$ = C$_D$/(C$_D$+C$_B$)

Fig. 4. (a) Equivalent circuit model of the gate stack, where C_D and C_B are the dielectric and barrier capacitances and R_B is the barrier resistance. R_B models the transport of electrons from the 2DEG channel to the interface [2, 4]. R_B decreases with increasing V_B, due to e.g. thermionic emission. (b) Distribution of the applied gate bias $V_G > 0$ to the dielectric and the barrier according to this model. The barrier potential Φ_B, i.e. the conduction band minimum of the barrier at the interface with respect to the Fermi-level, is changed by V_B due to the applied gate bias V_G. Although the model gives a first-order qualitative understanding, further effects may play a role, like e.g. pinning of the barrier potential due to a dominant defect level or due to spill-over (accumulation of a second channel at the interface). In addition, also the field in the dielectric may play a role for the stress/recovery dynamics.

4.9 Role of the Dielectric for the Charging Dynamics of the Dielectric/Barrier Interface in AlGaN/GaN based Metal-Insulator-Seminconductor Structures under Forward Gate Bias Stress

Authors	P. Lagger, P. Steinschifter, M. Reiner, M. Stadtmüller, G. Denifl, A. Naumann, J. Müller, L. Wilde, D. Pogany and C. Ostermaier
Published In	Applied Physics Letters
Year	2014
Volume	105
Issue	3
Pages	033512-1 - 033512-5

Role of the Dielectric for the Charging Dynamics of the Dielectric/Barrier Interface in AlGaN/GaN based Metal-Insulator-Semiconductor Structures under Forward Gate Bias Stress

P. Lagger[1,3,a)], P. Steinschifter[1)], M. Reiner[1)], M. Stadtmüller[1)], G. Denifl[1)], A. Naumann[2)], J. Müller[2)], L. Wilde[2)], J. Sundqvist[2)], D. Pogany[3)], and C. Ostermaier[1)]

[1]*Infineon Technologies Austria AG, Siemensstraße 2, 9500 Villach, Austria*

[2]*Fraunhofer IPMS-CNT, Königsbrücker Straße 178, 01099 Dresden, Germany*

[3]*Institute of Solid State Electronics, Vienna University of Technology, Floragasse 7, 1040 Wien, Austria*

The high density of defect states at the dielectric/III-N interface in GaN based metal-insulator-semiconductor structures causes tremendous threshold voltage drifts, ΔV_{th}, under forward gate bias conditions. A comprehensive study on different dielectric materials, as well as varying dielectric thickness t_D and barrier thickness t_B is performed using capacitance-voltage analysis. It is revealed that the density of trapped electrons, ΔN_{it}, scales with the dielectric capacitance under spill-over conditions, i.e. the accumulation of a second electron channel at the dielectric/AlGaN barrier interface. Hence, the density of trapped electrons is defined by the charging of the dielectric capacitance. The scaling behavior of ΔN_{it} is explained universally by the density of accumulated electrons at the dielectric/III-N interface under spill-over conditions. We conclude that the overall density of interface defects is higher than what can be electrically measured, due to limits set by dielectric breakdown. These findings have a significant impact on the correct interpretation of threshold voltage drift data and are of relevance for the development of normally-off and normally-on III-N/GaN high electron mobility transistors with gate insulation.

Gallium Nitride (GaN) based metal-insulator-semiconductor high electron mobility transistors (MIS-HEMTs) are highly desired for power switching applications[1]. However, even state-of-the-art devices suffer from stress bias and stress time dependent V_{th} drifts (ΔV_{th}) induced by forward gate bias stress $V_G > 0$ V, which limits their stability and reliability. The V_{th} drifts are ascribed to electron trapping in defect states at the dielectric/III-N interface (here shortly the interface), where the electrons are provided by the two-dimensional electron gas (2DEG) channel via the III-N barrier layer[2-5]. A broad distribution of stress and recovery time constants extracted from V_{th} recovery curves after $V_G > 0$ V stress was observed recently[6-8]. It was mainly attributed to a broad distribution of defect properties of interface or near interface defect states in the dielectric. Furthermore, the III-N barrier is supposed to be a rate limiter for electron transport to defect states at the interface below the spill-over voltage $V_{G,spill\text{-}over}$, i.e. the gate bias at which a carrier accumulation at the interface occurs[8]. Although, a reduction of interface defect states density after special surface treatment and post-deposition annealing was reported[4-6], the observed V_{th} drifts are still a blocking point for the implementation of MIS-based normally-off devices and are even of concern for normally-on devices[7].

In this work, it is shown that the overall V_{th} drift depends strongly on the layer thicknesses of the dielectric and the barrier, and the dielectric constant. It is found that the density of trapped electrons at the interface ΔN_{it} is determined by the dielectric capacitance under spill-over conditions. Further, it is revealed that the thickness of the AlGaN barrier layer influences the spill-over voltage $V_{G,spill\text{-}over}$. An universal scaling behavior between the trapped interface state density and the "overdrive" gate bias V_G - $V_{G,spill\text{-}over}$ is found, which gives insight into the physics of the interface charging. The gate stack design (i.e. its electrostatics) has to be considered for the correct comparison of the measurement results. This is in clear contrast to previous works, where the focus is on the investigation of the interface properties itself and the apparent influence of the electrostatic properties is ignored. We reveal that the change of ΔN_{it} for varying gate stack design is higher than the influence of ΔN_{it} reduction due to process improvements, which are reported so far[5,6]. We conclude that ΔN_{it} is even higher than what can be electrically measured.

---

[a] Corresponding author, E-mail: peter.lagger@infineon.com

The sample devices are fabricated on GaN-on-Si substrates, see TABLE I. The III-N barrier consists of an $Al_{0.2}Ga_{0.8}N$ layer of varying thickness t_B for all the samples. The following dielectrics, with a varying layer thickness t_D, were deposited by various techniques on the AlGaN barrier layer: low pressure chemical vapor deposition (LPCVD)-SiO_2, LPCVD-Si_3N_4, atomic layer deposition (ALD)-HfO_2, ALD-$HfSiO_2$ 1:1 (ratio between Hf and Si precursor pulses), ALD-$HfSiO_2$ 10:1 and ALD-Al_2O_3. Circular MIS-diodes with a diameter of 100 µm are used as test devices, where a new device is taken for each test to ensure defined initial conditions. The threshold voltage drift ΔV_{th} is extracted from capacitance voltage (CV)-curves swept from gate biases V_G = -10 to 0 V (100 kHz, 1V/s), which are measured directly before and after forward gate bias stress at different $V_G > 0$ V. The spill-over voltage $V_{G,spill\text{-}over}$ is extracted from CV measurements at $V_G > 0$. Even though, it is not proven that the small-signal response from a high frequency CV measurement is directly linked to the actual spill-over event of electrons, it is the best known reference to monitor this effect. Since it is intended to study the maximum ΔN_{it} for a given stress bias and ΔV_{th} is stress bias and stress time dependent, the stress time is intended to be as long as possible. Practically, a stress time of 10 s is chosen as a compromise between a sufficiently high ΔV_{th} magnitude and the required measurement time[8].

The influence of the dielectric thickness t_D and barrier thickness t_B on ΔV_{th} is studied on samples with a Si_3N_4 dielectric, which is deposited under the comparable process conditions for all samples. The V_{th} scales linearly with t_D (TABLE I), which indicates that the density of positive donor charges at the dielectric/III-N interface for $V_G = V_{th,}$ which compensate the surface polarization charges, is the same for all the wafers[9-11]. The V_{th} drifts for varying gate stress bias V_{G} are summarized in FIG. 1a. The corresponding change in number of trapped electron density at the interface, ΔN_{it}, is calculated from the measured ΔV_{th} values as

$$\Delta N_{\mathrm{it}} = (C_{\mathrm{D}}\, \Delta V_{\mathrm{th}}) \,/\, q = (\varepsilon_0\, \varepsilon_D\, \Delta V_{\mathrm{th}}) \,/\, (q\, t_{\mathrm{D}}), \tag{1}$$

where C_{D} is the dielectric capacitance, q the unit charge, ε_0 the vacuum permittivity and ε_{D} the dielectric constant. The overall ΔN_{it} scales, according to (1), with the dielectric capacitance C_{D} for a constant ΔV_{th}. Hence, for higher C_{D}, more electrons have to be trapped at the interface to achieve the same V_{th} drift. In FIG. 1a, it can be seen that for an increasing t_{D}, the overall ΔV_{th} is decreased. The opposite trend is observed for increasing t_{B}, where the influence of t_{B} is not explained by (1). In FIG. 1b the according $\Delta \mathrm{N}_{\mathrm{it}}$ values for the data in FIG. 1a are plotted using (1).

A comparison of the ΔV_{th} and ΔN_{it} for different dielectric materials is given in FIG. 2a. The V_{th} drift is shown for varying $\mathrm{V_G}$. Interestingly, structures with all dielectrics, except SiO_2 and Al_2O_3, exhibit nearly the same overall trend in $\Delta \mathrm{V_{th}}$ degradation. Moreover, the slope of all curves is very similar except for SiO_2. The ΔN_{it} scales, according to (1), linearly with the dielectric constant ε_{D}, i.e. the higher ε_{D}, the more electrons have to be trapped to achieve the same overall ΔV_{th}. FIG. 2b reveals that $\Delta \mathrm{N}_{\mathrm{it}}$ shows an overall increasing trend with increasing dielectric constant ε_{D}, which means that the tendency for the accumulation of charges at the interface scales with ε_{D}.

The strong dependence of forward gate bias induced ΔV_{th} and ΔN_{it} on the layer thicknesses and the dielectric constant suggests that ΔV_{th} dynamics, i.e. interface charging, is influenced by the layer capacitances, cf. FIG. 1-2. Choi et al.[5] showed an ΔN_{it} improvement by a factor of two for different SiN_x deposition processes, while we demonstrate that simple C_{D} variations change ΔN_{it} by nearly two decades. In the following, it is demonstrated that ΔN_{it} scales with the dielectric capacitance C_{D} for above spill-over conditions $V_{\mathrm{G}} > V_{\mathrm{G,spill\text{-}over}}$. For $V_{\mathrm{G}} < V_{\mathrm{G,spill\text{-}over}}$, the barrier potential Φ_{B0} (Fig. 3) is supposed to be a rate limiter for electron trapping at the interface[8].

Under equilibrium conditions (FIG 3a), a common Fermi-level is established and the probability for an electron transfer from the channel to the interface and vice versa is the same, i.e. there is no net current flux[8,12]. For $V_{\mathrm{G}} > 0$, we distinguish between two different bias regimes. For $V_{\mathrm{G}} < V_{\mathrm{G,spill\text{-}over}}$, the gate bias is distributed between dielectric and barrier according to

$$V_{\mathrm{G}} = V_{\mathrm{D}} + V_{\mathrm{B}}, \tag{2a}$$

$$V_{\mathrm{B}}/V_{\mathrm{G}} = C_{\mathrm{D}} \,/\, (C_{\mathrm{D}} + C_{\mathrm{B}}), \tag{2b}$$

where V_D and V_B is the voltage drop on the dielectric and the barrier, respectively, and C_B is the barrier capacitance. Under these conditions, we expect a net electron flux from the 2DEG channel to the interface, which is induced by the voltage drop on the barrier V_B (FIG 3b). Forward gate bias stress leads to a positive V_{th} drift and to a net negative charging of the interface. The barrier height Φ_{B0} decreases with increasing V_G and more electrons can be transferred from the 2DEG channel to the interface (see FIG. 3b), where V_B/V_G is a measure for the relative change in Φ_{B0}. We propose that $V_{G,\text{spill-over}}$ is defined by the barrier height Φ_{B0} and V_B/V_G, which is supported by the trend of decreasing $V_{G,\text{spill-over}}$ with increasing V_B/V_G (TABLE I). Deviations from this trend are explained by variations in Φ_{B0} between different samples. Thermionic emission or trap assisted tunneling[12-15] mechanism can be considered as electron transport process. A detailed model of the electron transport for this bias regime has still to be developed, where variations of Φ_{B0} and transport rates with V_G has to be taken into account.

For $V_G > V_{G,\text{spill-over}}$, a second electron channel at the dielectric/AlGaN interface is formed and the III-N barrier can be considered as transparent (i.e. the C_B capacitor in FIG. 3a-inset is virtually short circuit). The maximum charge, which could be available for trapping at the interface in this regime, is theoretically given by

$$Q_D = C_D V_G. \tag{3}$$

FIG. 4a shows the data of ΔN_{it} from FIG. 2b with Q_D/q in the horizontal axis. It can be seen that the extracted ΔN_{it} values are below the theoretical limit of $\Delta N_{it,max} = Q_D/q$. This is due to the fact that the stress kinetics of ΔV_{th} is logarithmic with time, due to broadly distributed capture time constants[8]. For a stress time of 10 s, the density of trapped charged ΔN_{it} is still below the theoretical limit Q_D/q. For $V_G < V_{G,\text{spill-over}}$ the data show a big spreading, where for higher V_G the data points tend to align parallel to the theoretical limit, i.e. $\Delta N_{it} \sim Q_D/q$. We expect that the curves converge to the theoretical limit for stress times much larger than 10 s or recovery times shorter than in this measurement[7]. Under spill-over, a second channel is formed at the interface and the bias distribution is given as (see FIG. 3c)

$$V_G = V_{D,\text{spill-over}} + V_{B,\text{spill-over}} + \Delta V_D = V_{G,\text{spill-over}} + \Delta V_D, \tag{4}$$

where $V_{D,\text{spill-over}}$ and $V_{B,\text{spill-over}}$ is the voltage drop on the dielectric and barrier at $V_G = V_{G,\text{spill-over}}$, respectively, and ΔV_D is the voltage overdrive in the dielectrics above $V_{G,\text{spill-over}}$. The potential at the interface is fixed for $V_G > V_{G,\text{spill-over}}$ and the voltage drop $V_{D,\text{spill-over}}$ and $V_{B,\text{spill-over}}$ do not change for increasing V_G. The additionally applied gate bias, ΔV_D, is dropped at the dielectric solely. In this case, the electrons for trapping at interface states are provided directly by the second channel. The related charge at the interface induced by the applied overdrive voltage ΔV_D is:

$$\Delta Q_D = C_D (V_G - V_{G,\text{spill-over}}) = C_D \cdot \Delta V_D, \tag{5}$$

which is limited to the regime where $V_\mathrm{G} > V_\mathrm{G,spill\text{-}over}$. At the time immediately after the stress pulse, ΔQ_D is the charge of free electrons which are formed at the interface. At later times, these free electron charge can be captured at interface states, which leads to a Coulomb charging effect, i.e. the lifting of the conduction band at the interface, as described in[8], see also FIG. 3d.

The data of ΔN_it from FIG. 4a are re-plotted as function of ΔQ_D in FIG. 4b, where it is demonstrated that (5) describes correctly the correlation between ΔN_it and C_D. Interestingly, ΔN_it depends linearly on ΔQ_D, which demonstrates that the free electron charge in the second channel at the interface are responsible for the increase in ΔN_it. Consequently, the higher the dielectric capacitance, the more charges are accumulated under the same stress conditions. The scaling law given by (5) compensates the effect that with higher ε_D more ΔN_it is needed to achieve the same overall ΔV_th as stated by (1).

The influence of the barrier thickness t_B is reflected in the change of the spill-over voltage $V_\mathrm{G,spill\text{-}over}$ between the samples with varying t_B, cf. TABLE I. Further, also an dependency of $V_\mathrm{G,spill\text{-}over}$ on the dielectric material is observed, which might be due to different structure of interface defect states and hence different barrier potential Φ_B0 for different dielectric materials.

The absence of saturation of ΔN_it with increasing Q_D/q for all of the investigated samples, observed in this work and in ref.[8], indicates that there are more interface traps available than those which can be achieved by an electrical measurement. The upper limit for ΔV_th, and hence also ΔN_it, is given by the stress magnitude V_G (see (4)). We suggest that the maximum measureable ΔN_it is limited by the breakdown strength of the dielectric, where an upper limit for the electrical measurement is set by

$$(\varepsilon_0\ \varepsilon_\mathrm{D}\ E_\mathrm{crit})/q\ <\ \Delta N_\mathrm{it,limit}, \tag{6}$$

where E_crit is the critical electric field strength for dielectric breakdown. For a E_crit for oxides in the range of 10 MV/cm[16] and a relative permittivity of the dielectrics in the range of 3.9-19.1[17], the maximum measureable ΔN_it is in the range of $2.16\ 10^{13}$-$1.06\ 10^{14}$ cm^{-2}. This represents a problem in the determination of the correct maximum concentration of available interface states, which may exist at the dielectric/III-N barrier interface[18] by electrical means. Moreover, the $\Delta N_\mathrm{it,limit}$ determined by electrical measurements can be even lower due to time-dependent dielectric breakdown effects[3,8,19], so (6) represents just a lower estimate of the overall density of interface defect states.

In conclusion, a comprehensive study of threshold voltage drift on AlGaN/GaN MIS-heterostructures with different dielectric materials is performed. We found that $V_\mathrm{G,spill\text{-}over}$ tends to decrease with increasing $V_\mathrm{B}/V_\mathrm{G}$, which explains the impact of the barrier capacitance C_B. Further we show that for $V_\mathrm{G} < V_\mathrm{G,spill\text{-}over}$, the III-N barrier height acts as a rate-limiter. In the voltage regime above the spill-over voltage the extracted ΔN_it scales with the amount of free electrons at the dielectric/barrier interface, where a theoretical limit for ΔN_{it} is given by the dielectric charge Q_D/q. This is related to the fact that the density of defect states is much higher than the density of available electrons at the interface. We suggest that the upper limit of the electrically measureable interface state density is set by the breakdown strength of the dielectric material. This suggests that the density of interface states for any kind of dielectric is practically high enough to completely deplete the 2DEG channel with a typical electron density in the order of 10^{13} cm^{-2}. According to this model, a relative improvement of ΔV_{th} can be either assigned to an increase in the barrier height Φ_{B0}, and hence also $V_{G,\text{spill-over}}$, or to a partial reduction of interface states, which are able to respond within the timeframe of the measurement. It appears therefore as a fundamental limitation for the stability of normally-off MIS devices.

VI. FIGURES

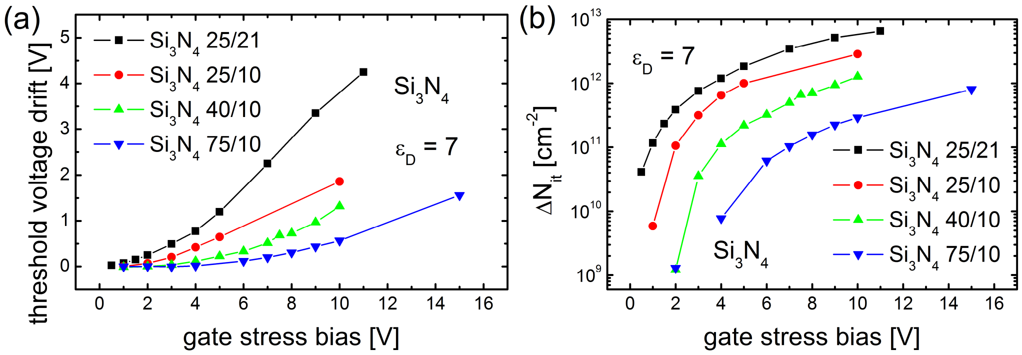


FIG. 1. (a) Comparison of GaN MIS-HEMTs with a Si_3N_4 dielectric and $Al_{20}Ga_{80}N$ barrier with varying dielectric and barrier thicknesses in terms of ΔV_{th} drift. (b) Calculated ΔN_{it} values. Detailed information about the samples can be found in TABLE 1.

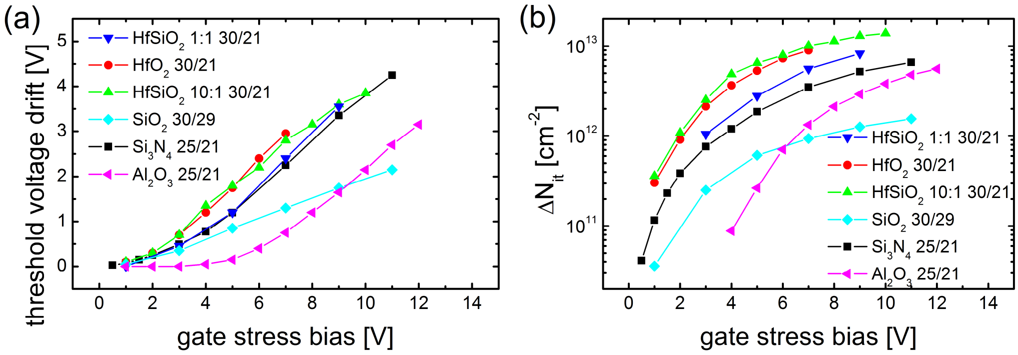


FIG. 2. (a) Comparison of V_{th} drift of GaN MIS-HEMTs with different dielectrics for different gate stress bias. (b) According ΔN_{it} values, where an overall trend of increasing ΔN_{it} for increasing dielectric constant ε_D is observed. Detailed information about the samples can be found in TABLE 1. For simplicity, we consider a potential pinning in the GaN channel.

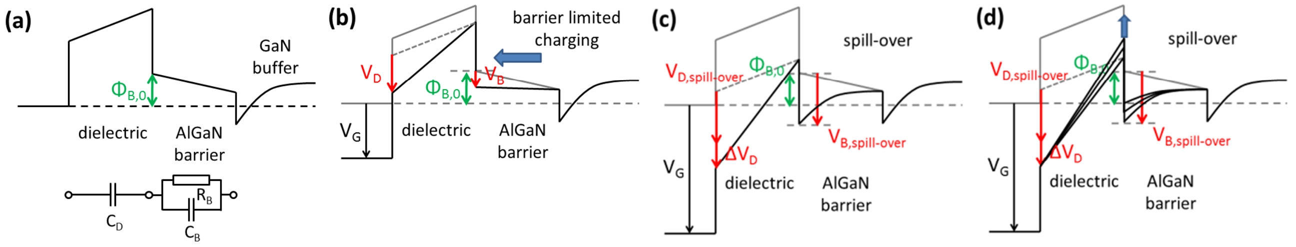

(a)
ΦB,0
GaN
buffer
dielectric
AlGaN
barrier
CD
RB
CB
(b)
barrier limited
charging
VD
ΦB,0
VB
VG
dielectric
AlGaN
barrier
(c)
spill-over
VD,spill-over
ΦB,0
VB,spill-over
ΔVD
VG
dielectric
AlGaN
barrier
(d)
spill-over
VD,spill-over
ΦB
VB,spill-over
ΔVD
VG
dielectric
AlGaN
barrier

FIG. 3. (a) Conduction band edge of the gate stack in a GaN based MIS-HEMT in thermal equilibrium. There is no net electron flow between the channel and the interface. The inset shows an equivalent circuit model of the gate stack. (b) The initial barrier potential Φ_{B0} is changed by V_B under $V_G > 0$ V stress, which induces a net electron flow via the barrier towards the III-N interface. (c) In the spill-over case a second channel at the dielectric interface is accumulated and electrons are directly provided from this second channel to interface defect states. (d) Change of the conduction band potential at the interface due to Coulomb charging.

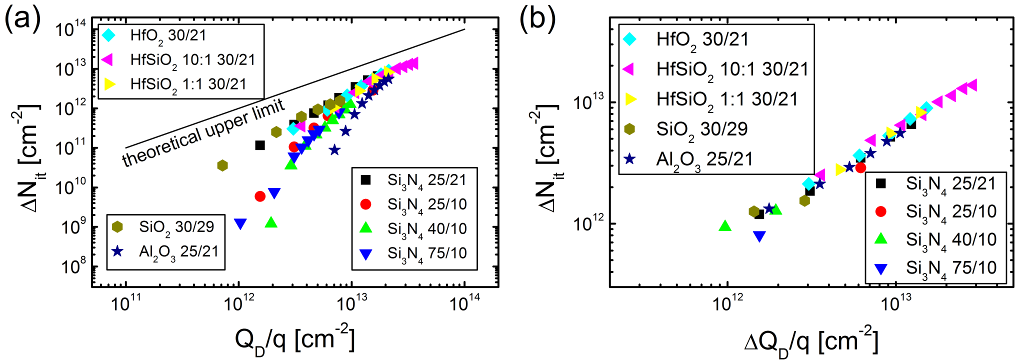


FIG. 4. (a) ΔN_{it} shows an increase with the dielectric charge Q_D/q. The deviation between the different samples can be explained by the varying spill-over voltage $V_{G,spill\text{-}over}$. (b) Linear scaling of ΔN_{it} with the applied overdrive voltage ΔV_D in the spill-over regime. Detailed information about the samples can be found in TABLE 1.

VII. TABLES

TABLE I. Overview of samples.

ID	Material	t_D[1]	ε_D[2]	t_B[3]	V_{th}[4]	$\Delta N_{it}/\Delta V_{th}$[5]	V_B/V_G[6]	$V_{G,spill\text{-}over}$[7]
		nm		nm	V	cm^{-2} V^{-1}		V
Si_3N_4 25/21	Si_3N_4	25	7.0	21	-6.6	1.55 10^{12}	0.37	3
Si_3N_4 25/10	Si_3N_4	25	7.0	10	-5.7	1.55 10^{12}	0.22	6
Si_3N_4 40/10	Si_3N_4	40	7.0	10	-8.8	9.67 10^{11}	0.15	8
Si_3N_4 75/10	Si_3N_4	75	7.0	10	-16.4	5.16 10^{11}	0.09	12
HfO_2 30/21	HfO_2	30	16.7	21	-6.8	3.04 10^{12}	0.54	2
$HfSiO_2$ 10:1 30/21	$HfSiO_2$	30	19.1	21	-6.7	3.60 10^{12}	0.58	2
$HfSiO_2$ 1:1 30/21	$HfSiO_2$	30	13.6	21	-8.0	2.32 10^{12}	0.47	3
SiO_2 30/29	SiO_2	30	3.9	29	-10.1	7.18 10^{11}	0.27	7
Al_2O_3 25/21	Al_2O_3	25	8.0	21	-8.2	1.77 10^{12}	0.40	6

[1] thickness of the dielectric layer

[2] dielectric constant

[3] thickness of the barrier layer

[4] threshold voltage

[5] density of trapped electrons per threshold voltage drift according to (1)

[6] voltage drop on the barrier VB per 1 V applied gate bias VG according to (2b)

[7] spill-over voltage extracted from capacitance voltage measurements

REFERENCES

[1] M. A. Khan, G. Simin, J. Yang, J. Zhang, A. Koudymov, M. Shur, R. Gaska, R.; X. Hu and A. Tarakji, IEEE Transaction on Microwave Theory and Techniques, 2003, Vol. 51, p. 624

[2] T. Imada, K. Motoyoshi, M. Kanamura and T. Kikkawa, Proceedings of the IIRW, 2011, p. 38-41

[3] T.-L. Wu, D. Marcon, M. Zahid, M. V. Hove, S. Decoutere and G. Groeseneken, Proceedings of the IRPS, 2013

[4] S. Yang, Z. Tang, K.-Y. Wong, Y.-S. Lin, Y. Lu, S. Huang and K. J. Chen, Proceedings of the IEDM, 2013

[5] W. Choi, H. Ryu, N. Jeon, M. Lee, H.-Y. Cha and K.-S. Seo, IEEE Electron Device Letters, 2013

[6] P. Lagger, C. Ostermaier, G. Pobegen and D. Pogany, Proceedings of the IEDM, 2012

[7] P. Lagger, A. Schiffmann, G. Pobegen, D. Pogany and C. Ostermaier, IEEE Electron Device Letters, 2013, Vol. 34, p. 1112-1114

[8] P. Lagger, M. Reiner, D. Pogany and C. Ostermaier, IEEE Transactions on Electron Devices, 2014, Vol. 61, p. 1022-1030

[9] S. Ganguly, J. Verma, G. Li, T. Zimmermann, H. Xing and D. Jena, Applied Physics Letters, 2011, Vol. 99, 193504

[10] M. Esposto, S. Krishnamoorthy, D.N. Nath, S. Bajaj, T.-H. Hung, S. Rajan, Appl. Phys. Lett. 99 (2011)133503.

[11] A. Alexewicz, C. Ostermaier, C. Henkel, O. Bethge, J.-F. Carlin, L. Lugani, N. Grandjean, E. Bertagnolli, D. Pogany and G. Strasser, Thin Solid Films, 2012, Vol. 520, p. 6230-6232

[12] S. M. Sze and K. K. Ng, “Physics of Semiconductor Devices”, Wiley and Sons, 2007

[13] H. Zhang, E.J. Miller, and E.T. Yu, J. Appl. Phys. 99 (2006) 023703

[14] E.J. Miller, E.T. Yu, P. Waltereit, J.S. Speck, Appl. Phys. Lett. 84 (2004) 535

[15] D. J Yan, H. Lu, D. Cao, D. Chen, R. Zhang, Y. Zheng, Appl. Phys. Lett 97 (2010) 153503

[16] J. McPherson, J.-Y. Kim, A. Shanware, H. Mogul, Applied Physics Letters, Vol. 82, 2003, p. 2121-2123

[17] O. Engström, B. Raeissi, S. Hall, O. Buiu, M.C. Lemme, H.D.B. Gottlob, P.K. Hurley, K. Cherkaoui, Solid State Electronics, 2007, Vol. 51, p. 622-626

[18] M. S. Mio, J. R. Weber, and C. G. V. de Walle, Journal of Applied Physics, 2010, Vol. 107, 123713

[19] R. Degraeve, B. Kaczer, G. Groeseneken, Microelectronics Reliability, 1999, Vol. 39, p. 1445-1460

Chapter 5

Conclusion and Outlook

In this thesis, a systematic study of the impact of design parameters (layer thicknesses, dielectric material, influence of process parameters, etc.) and electrical stress parameters (gate stress bias and stress time) and conditions (pulsed vs. continuous) on forward gate bias induced V_{th} drifts is performed. The key findings of this work are summarized as follows:

- A measurement setup for a fast transient characterization of the recovery curves of V_{th} drift is developed. The measurement delay time between the end of the stress pulse and the recovery measurement is 1 μs, cf. Chapter 4.5.
- Small-signal measurements are not suitable for interface characterization in GaN based MIS-HEMTs, because no quasi-equilibrium situation during $V_{\mathrm{G}} > 0V$ can be established [LSP+13b], cf. Chapter 4.5.
- It is found that ΔV_{th} is bias and time dependent, where no maximum of ΔV_{th} is found. The amount of ΔV_{th} is limited by dielectric breakdown [LOPP12, LRPO14, LSR+14], cf. Chapter 4.3, Chapter 4.6 and Chapter 4.9.
- The observed defects show a broad distribution of stress and recovery time constants and a complex defect kinetics. [LRPO14], cf. Chapter 4.6.
- The charging of the bilayer gate capacitance causes an increase of the barrier potential proportional to the density of trapped electrons (feedback effect) [LRPO14, LPO14, LSR+14], cf. Chapter 4.6, Chapter 4.7.
- The overall ΔV_{th} is limited by $V_{\mathrm{G,stress}}$ because the maximum charge, which could be available for trapping at the interface is theoretically given by the dielectric charge $Q_{\mathrm{D}} = C_{\mathrm{D}} V_{\mathrm{G}}$, where C_{D} is the dielectric capacitance and V_{G} is the applied gate bias [LRPO14, LPO14, LSR+14], cf. Chapter 4.6, Chapter 4.7, Chapter 4.9.
- The stress dynamics is supposed to be influenced by the barrier potential below spill-over, where the barrier layer acts as a rate limiter for electron trapping at the interface [LRPO14, LSR+14], cf. Chapter 4.6 and Chapter 4.9.
- The ΔN_{it} follows a common trend for several dielectric materials above spill-over and hence the density of defect states at the interface between dielectric and III-N barrier is higher than what can be electrically measured [LSR+14], cf. Chapter 4.9.

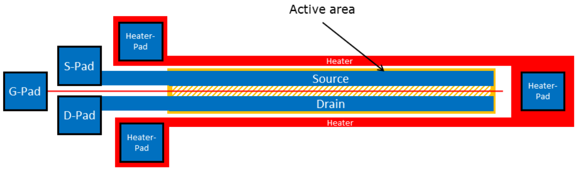


Figure 5.1: Schematics of the test device with on-wafer integrated heater resistors.

The probably most important finding is the last one. The charging dynamics of interface defect states, of whatever nature, is finally determined by the capacitance of the dielectric on top of the III-N barrier. A common charging trend for several dielectric materials in the spill-over regime, following the dielectric capacitance, is found. This entails that the density of interface defects is higher than what can be electrically charged. The differences in V_{th} drift between different materials are explained by differences in barrier potential Φ_{B0}.

Although, the influence of gate stress bias and stress time, as well as the impact of layer thickesses and dielectric material is comprehensively investigated throughout this work, the influence of the temperature on ΔV_{th} is still unknown. The study of the impact of temperature is subjected to future work. Nevertheless, within this work the ground for systematic temperature investigations is layed. For this purpose a special test structure is developed, which integrates a heater directly on wafer level, cf. Fig. 5.1. This structure enables fast switches of the local device temperature, i.e. fast heating and fast cooling. Similar test structures already exist for standard Si technologies [PNdFG14], where the heater resistor is formed with poly silicon. The adaption of this structure for GaN includes the investigation of a proper material for the heater resistor, where finally a 2DEG heater resistor is implemented.

The big advantage of integrated heaters is that one can decouple the temperature during stress and recovery. First tests show that the cool-down of the local temperature can be realized within $1s$. Although, a calibration of the temperature as a function of the heater power is outstanding, first preliminary results indicate a positive temperature activation of ΔV_{th} (Fig. 5.2).

The suitability of time-resolved ΔV_{th}-measurements for the characterization of the dielectric/III-N interface is succesfully demonstrated in this work. This study shows that there are still fundamental issues to solve to realize electrically stable and reliable interfaces between dielectrics and III-N surfaces. The microphysical structure of the interface is still quite a mystery. Many fundamental issues are yet to be solved. However, a proper characterization tool is a prerequisite for the further development.

A comparison with historical development of SiO_2/Si technology shows that the problem of optimizing the dielectric interface for GaN devices is by far more complex. First of all, different surfaces exist (e.g. AlN, GaN, AlGaN, ...). Furthermore, the number of possible dielectric materials is huge, where no clear favorite is yet nominated. Although, at the moment no solution for a MIS-structure, which is stable in forward gate bias direction, exists, there is no proof that it is not possible to fabricate such a structure at all. In the end, the feasibility can only be proven by a proper implementation of such a structure.

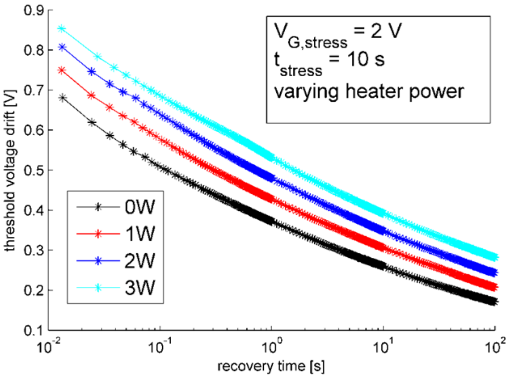


Figure 5.2: Recovery of V_{th} drift after a forward gate bias stress at a stress bias $V_{\mathrm{G,stress}} =$ 2 V for a stress time t_{s} of 10 s for varying heater power of 0 to 3 W. The heater is switched of after 7 s of electrical stress to ensure cool-down until the end of the electrical stress pulse. This test is performed on a wafer with a 20 nm $\mathrm{Al_{20}Ga_{80}}$ barrier layer, on which a 25 nm $\mathrm{Si_3N_4}$ is deposited as gate dielectric.

Appendix A - Measurement Setups

SMU-based Setup

The stress-recovery pattern of Fig. 3.6 can be directly implemented on a standard SMU-based measurement setup [KGR+08]. This has the advantage of a high measurement accuracy, because of the high accuray of the current measurement itself, cf. (5.3). The disadvantage is that the minimum delay time t_{delay} after switchting from stress to measurement bias is limited to some 10 ms and the minimum achievable stress times are in the range of 100 ms. In Fig. 5.3, the ΔV_{th}-curve without a preceeding stress pulse, i.e. a so-called dummy measurement [LSP+13b], is shown. The purpose of this measurement is to test the influence of the measurement conditions on the device. The result shown in Fig. 3.6 clearly demonstrates that the measurement itself has a negligible influence on the device.

Oscilloscope/Pulse Generator based Setup

Since forward gate bias stress induced ΔV_{th} recovers quickly after switching from stress to measurement conditions [LSP+13b,LRPO14], it is advantageous to minimize the delay time t_{delay} between end of the stress pulse and the first measurement point. For this purpose a setup based on an oscilloscope and a pulse generator is developed. A schematics of this setup is shown in Fig. 5.4. The stress-recovery pattern (Fig. 3.6) is implemented in the same way as on a standard SMU-based measurement setup, but with the difference that $V_{\mathrm{D,meas}}$ is applied to the series connection of the resistor and the actual device under test. While the drain bias is kept constant in the SMU-based setup, the drain bias V_{D} changes with the applied gate bias V_{G} in this setup according to

$$V_{\mathrm{D}} = V_{\mathrm{DD}} - R_{\mathrm{S}} I_{\mathrm{D}}(V_{\mathrm{G}}), \tag{5.1}$$

where V_{DD} is the externally applied bias, V_{D} the actual drain bias of the device, R_{S} the resistance value of the series resistor in the load-line configuration and $I_{\mathrm{D}}(V_{\mathrm{G}})$ is the drain current of the device for a certain gate bias V_{G}. This means that, in the load-line configuration (Fig. 5.5), the drain signal V_{D} as a function of the gate bias V_{G} is directly proportional to the transfer characterisitics $I_{\mathrm{D}}(V_{\mathrm{G}})$. This enables a direct sense of V_{D} instead of measuring I_{D}, which is advantageous since an oscilloscope can only probe voltages. Hence it is not necessary to probe the current via the series resistor, which would add additional noise due to the subtraction of two bias signals. The advantages of this setup are a improvement of the minimum stress time (100 ns) and a reduction of the mimimum delay time t_{delay} of the setup, which is in der order of some μs. Unfortunately, the overall accuracy of this

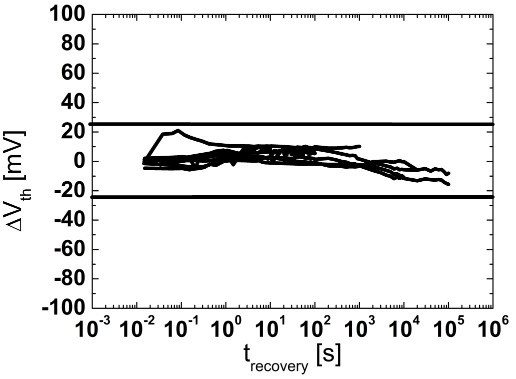


Figure 5.3: Dummy measurement, i.e. the ΔV_{th} recovery is measured without preceeding stress pulse. The influence of the measurement itself is within ±20 mV for recovery times up to 10^5 s. This test is performed on a HEMT structure with a 25 nm $\mathrm{Al_{25}Ga_{75}N}$ barrier layer with a 3 nm GaN cap, on which a 20 nm $\mathrm{Al_2O_3}$ is deposited by an ALD-process.

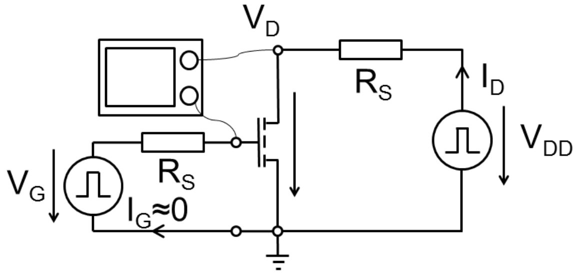


Figure 5.4: Schematic of the oscilloscope-pulse generator based setup. The value of the series resistance $R_{\mathrm{S}} = 50\ \Omega$.

setup is worse in comparison to the SMU-based setup, because the voltage measurement resolution of an oscilloscope is worse than the current resolution of a SMU. Due to the large magnitude of the measured ΔV_{th} signals this is not a major problem.

Resolution of the Measurement

The upper limit for the accuracy of the ΔV_{th} measurement is determined by the transconductance of the device (cf. Fig. 5.6) which is defined as

$$g_{\mathrm{m}} = \frac{\mathrm{d}I_{\mathrm{D}}}{\mathrm{d}V_{\mathrm{G}}}. \tag{5.2}$$

Since the ΔV_{th} is examined by simple mapping of $I_{\mathrm{D}}(t)$ to the initial $I_{\mathrm{D}}(V_{\mathrm{G}})$, the transconductance is a measure for the maximum achievable resolution of the ΔV_{th}-measurement. The uncertainty in ΔV_{th} directly yields to

$$\Delta(\Delta V_{\mathrm{th}}) = \frac{\Delta I_{\mathrm{D}}}{g_{\mathrm{m}}}, \tag{5.3}$$

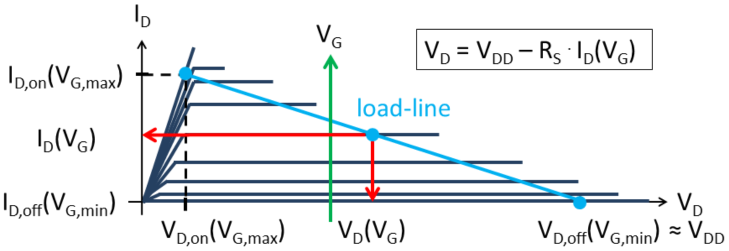


Figure 5.5: Schematics of the $I_{\mathrm{D}}(V_{\mathrm{D}})$-characteristics for different values of V_{G}. The load-line is defined by the series resistance R_{S} (cf. Fig. 5.4).

where $\Delta(\Delta V_{\mathrm{th}})$ is the uncertainty in ΔV_{th} and ΔI_{D} is the uncertainty of the current measurement. The proper choice of the monitoring bias $V_{\mathrm{G}} = V_{\mathrm{G,meas}}$ is usually done close to the maximum of the transconductance g_{m}.

The sensitivity is given by

$$\Delta(\Delta N_{\mathrm{it}}) = -C_{\mathrm{D}}\frac{\Delta(\Delta V_{\mathrm{th}})}{q}, \tag{5.4}$$

with $\Delta(\Delta N_{\mathrm{it}})$ is the density of trapped electrons, C_{D} the dielectric capacitance and q the elementary charge. The typical sensitivity of the setup is in the range of $\Delta N_{\mathrm{it}} > 10^{10}\mathrm{cm}^{-2}$ for typical resolutions of the measurement setup of some 10 mV for typical a dielectric thickness of 30 nm [LSR$^+$14].

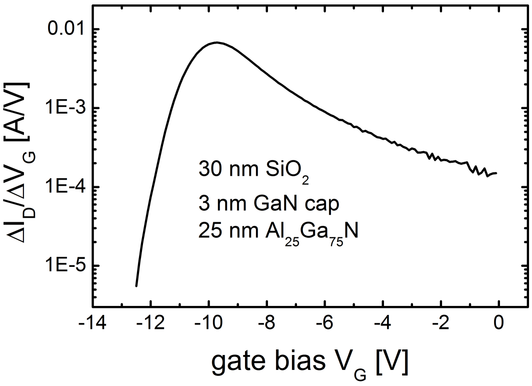


Figure 5.6: Transconductance of the initial transfer characteristics shown in Fig. 3.3.

Bibliography

[08] *Polarization Effects in Semiconductors - From Ab Initio Theory to Device Applications*. Springer, 2008.

[AMM$^+$02] O Ambacher, J Majewski, C Miskys, A Link, M Hermann, M Eickhoff, M Stutzmann, F Bernardini, V Fiorentini, V Tilak, B Schaff, and L F Eastman. Pyroelectric properties of al(in)gan/gan hetero- and quantum well structures. *Journal of Physics: Condensed Matter*, 14(13):3399, 2002.

[ASS$^+$99] O. Ambacher, J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Murphy, W. J. Schaff, L. F. Eastman, R. Dimitrov, L. Wittmer, M. Stutzmann, W. Rieger, and J. Hilsenbeck. Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in n- and ga-face algan/-gan heterostructures. *Journal of Applied Physics*, 85(6):3222–3233, 1999.

[Bal82] B. J. Baliga. Semiconductors for high-voltage, vertical channel fet's. *Journal of Applied Physics*, 53:1759–1764, 1982.

[Bal08] B. J. Baliga. *Fundamentals of Power Semiconductor Devices*. Springer-Verlag, New York, 2008.

[BBP$^+$02] J. D. Brown, R. Borges, E. Piner, A. Vescan, S. Singhal, and R. Therrien. Algan/gan hfets fabricated on 100-mm gan on silicon (111) substrate. *Solid State Electronics*, 46:1535–1539, 2002.

[Ber96] V. M. Bermudez. Study of oxygen chemisorption on the gan(0001)(1x1) surface. *Journal of Applied Physics*, 80:1190, 1996.

[BFV97] F. Bernardini, V. Fiorentini, and D. Vanderbilt. Spontaneous polarization and piezoelectric constants of iii-v nitrides. *PHYSICAL REVIEW B*, 56:24–27, 1997.

[BTEH$^+$10] Bahat-Treidel, E., Hilt, O., Brunner, F., V. Sidorov, J. Würfl, and G. Tränkle. Algan/gan/algan dh-hemts breakdown voltage enhancement using multiple grating field plates (mgfps). *Electron Devices, IEEE Transactions on*, 57(6):1208 –1216, june 2010.

[CCC$^+$11a] Rongming Chu, A. Corrion, M. Chen, Ray Li, D. Wong, D. Zehnder, B. Hughes, and K. Boutros. 1200-v normally off gan-on-si field-effect transistors with low dynamic on -resistance. *Electron Device Letters, IEEE*, 32(5):632 –634, may 2011.

[CCC+11b] A. L. Corrion, M. Chen, R. Chu, S. D. Burnham, S. Khalil, D. Zehnder, B. Hughes, and K. Boutros. Normally-off gate-recessed algan/gan-on-si hybrid mos-hfet with al2o3 gate dielectric. In *Device Research Conferenc*, 2011.

[CRJ+13] Woojin Choi, H. Ryu, N. Jeon, M. Lee, H.-Y. Cha, and K.-S. Seo. Improvement of vth instability in normally-off gan mis-hemts employing peald-sinx as an interfacial layer. *IEEE Electron Device Letters*, 2013.

[CZCL05] Yong Cai, Yugang Zhou, K.J. Chen, and K.M. Lau. High-performance enhancement-mode algan/gan hemts using fluoride-based plasma treatment. *Electron Device Letters, IEEE*, 26(7):435 – 437, july 2005.

[DFN06a] Y. Dong, R. M. Feenstra, and J. E. Northrup. Electronic states of oxidized gan(0001) surfaces. *Applied Physics Letters*, 89:171920, 2006.

[DFN06b] Y. Dong, R. M. Feenstra, and J. E. Northrup. Oxidized gan(0001) surfaces studied by scanning tunneling microscopy and spectroscopy and by first-principles theory. *Journal of Vacuum Science & Technology B*, 24:2080, 2006.

[EYN13] B. S. Eller, J. Yang, and R. J. Nemanich. Electronic surface and dielectric interface states on gan and algan. *Journal of Vacuum Science & Technology, A: Vacuum, Surfaces, and Films*, 31:050807, 2013.

[Fas05] Gerhard Fasching. *Werkstoffe für die Elektrotechnik*. SpringerWienNewYork, 2005.

[FMUM+11] T.B. Fehlberg, J.S. Milne, G.A. Umana-Membreno, S. Keller, U.K. Mishra, B.D. Nener, and G. Parish. Transport studies of algan/gan heterostructures of different al mole fractions with variable passivation stress. *Electron Devices, IEEE Transactions on*, 58(8):2589 –2596, aug. 2011.

[FPTB+12] A. Fontserè, A. Pérez-Tomás, V. Banu, P. Godignon, and J. Millán. A hfo2 based 800v/300°c au-free algan/gan-on-si hemt technology. In *Proceedings of the 2012 24th International Symposium on Power Semiconductor Devices and ICs*, 2012.

[FSW+95] D.M. FLEETWOOD, M.R. SHANEYFELT, W.L. WARREN, J.R. SCHWANK, T.L. MEISENHEIMER, and P.S. WlNOKUR. Border traps: Issues for mos radiation response and long-term reliability. *Microelectronics Reliability*, 35:403–428, 1995.

[FWRR98] D. M. Fleetwood, P. S. Winokur, L. C. Riewe, and R. A. Reber. Bulk oxide traps and border traps in metal-oxide-semiconductor capacitors. *Journal of Applied Physics*, 84(11):6141–6148, 1998.

[GMC+10] Luke Gordon, Mao-Sheng Miao, Srabanti Chowdhury, Masataka Higashiwaki, Umesh K Mishra, and Chris G Van de Walle. Distributed surface donor states and the two-dimensional electron gas at algan/gan heterojunctions. *Journal of Physics D: Applied Physics*, 43(50):505501, 2010.

[GN66] A. Goetzberger and H. E. Nigh. Surface charge after annealing of al-sio2-si structures under bias. In *Proceedings of the IEEE 54.10*, page 1454, 1966.

[Gra12] Tibor Grasser. Stochastic charge trapping in oxides: From random telegraph noise to bias temperature instabilities. *Microelectronics Reliability*, 52:39–70, 2012.

[GUKM09] L. C. Grabow, J. J. Uhlrich, T. F. Kuech, and M. Mavrikakis. Effectiveness of in situ nh3 annealing treatments for the removal of oxygen from gan surfaces. *Surface Science*, 603:387–399, 2009.

[GVL⁺11] Satyaki Ganguly, Jai Verma, Guowang Li, Tom Zimmermann, Huili Xing, and Debdeep Jena. Presence and origin of interface charges at atomic-layer deposited al[sub 2]o[sub 3]/iii-nitride heterojunctions. *Applied Physics Letters*, 99(19):193504, 2011.

[HCM⁺10] Masataka Higashiwaki, Srabanti Chowdhury, Mao-Sheng Miao, Brian L. Swenson, Chris G. Van de Walle, and Umesh K. Mishra. Distribution of donor states on etched surface of algan/gan heterostructures. *Journal of Applied Physics*, 108(6):063719, 2010.

[HCSM10] Masataka Higashiwaki, Srabanti Chowdhury, Brian L. Swenson, and Umesh K. Mishra. Effects of oxidation on surface chemical states and barrier height of algan/gan heterostructures. *Applied Physics Letters*, 97(22):222104, 2010.

[HKW⁺03] S. Heikman, S. Keller, Y. Wu, J. S. Speck, S. P. DenBaars, and U. K. Mishra. Polarization effects in algan/gan and gan/algan/gan heterostructures. *Journal of Applied Physics*, 93:10114, 2003.

[HP94] C. R. Helms and E. H. Poindexter. The silicon-silicon-dioxide system: its microstructure and imperfections. *Rep. Prog. Phys.*, 57:791, 1994.

[HPE10] P. Hower, S. Pendharkar, and T. Efland. Current status and future trends in silicon power devices. In *Proceedings of the International Electron Device Meeting*, pages 13.1.1–13.1.4, 2010.

[HYRC12] Sen Huang, Shu Yang, John Roberts, and Kevin Chen. Characterization of vth-instabilities in al2o3/gan/algan/gan mis-hemts by quasi-static c-v measurement. *Physica Status Solidi*, 0:0, 2012.

[IEA] IEA. International energy agency - key world energy statistics 2013.

[IFN⁺00] J. P. Ibbetson, P. T. Fini, K. D. Ness, S. P. DenBaars, J. S. Speck, and U. K. Mishra. Polarization effects, surface states, and the source of electrons in algan/gan heterostructure field effect transistors. *Applied Physics Letters*, 77(2):250–252, 2000.

[IFX08] Saving energy - through innovation and technology, 2008.

[IGBT⁺11] P. Ivo, A. Glowacki, E. Bahat-Treidel, R. Lossy, J. Würfl, C. Boit, and G. Tränkle. Comparative study of algan/gan hemts robustness versus buffer design variations by applying electroluminescence and electrical measurements. *Microelectronics Reliability*, 51:217–223, 2011.

[IKMO93] M. Itano, F. W. Kern, M. Miyashita, and T. Ohmi. Particle removal from silicon wafer surface in wet cleaning process. *IEEE Transactions on Semiconductor Manufacturing*, 6(3):258ff, 1993.

[IMKK11] T. Imada, K. Motoyoshi, M. Kanamura, and T. Kikkawa. Reliability analysis of enhancement-mode gan mis-hemt with gate-recess structure for power supplies. In *Integrated Reliability Workshop Final Report (IRW), 2011 IEEE International*, pages 38 –41, oct. 2011.

[IUTU13] M. Ishida, T. Ueda, T. Tanaka, and D. Ueda. Gan on si and technologies for and power switching and devices. *IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 60, NO. 10, OCTOBER*, 60(10):3053–3059, 2013.

[Jae01] R. C. Jaeger. *Thermal Oxidation of Silicon - Introduction to Microelectronic Fabrication.* Prentice Hall, 2001.

[Joh65] E. O. Johnson. Physical limitations on frequency and power parameters of transistors. *RCA Review*, pages 163–177, 1965.

[KA60] D. Khang and M. M. Atalla. -. In *IRE-AIEE Solid-State Device Research Conference Pittsburg*, 1960.

[KAWUM02] K. Kushida-Abdelghafar, K. Watanabe, J. Ushio, and E. Murakami. Effect of nitrogen at sio 2 / si interface on reliability issues - negative-bias-temperature-instability and fowler-nordheim-stress degradation. *Applied Physics Letters*, 81:4362, 2002.

[KBKO93] M. A. Khan, A. Bhattarai, J. N. Kuznia, and D. T. Olson. High electron mobility transistor based on ganalxga1-xn heterojunction. *Applied Physics Letters*, 63:1214ff, 1993.

[KBW$^+$10] J. W. Kolar, J. Biela, S. Waffler, T. Friedli, and U. Badstuebner. Performance trends and limitations of power electronic systems. In *CIPS*, 2010.

[Ker90] W. Kern. The evolution of silicon wafer cleaning technology. *Journal of the Electrochemical Society*, 137:1887–1892, 1990.

[KGR$^+$08] B. Kaczer, T. Grasser, P.J. Roussel, J. Martin-Martinez, R. O'Connor, B.J. O'Sullivan, and G. Groeseneken. Ubiquitous relaxation in bti stressing - new evaluation and insights. In *Reliability Physics Symposium, 2008. IRPS 2008. IEEE International*, pages 20 –27, 27 2008-may 1 2008.

[KH12] N. Kaminski and O. Hilt. Sic and gan devices - competition or coexistence? In *CIPS*, 2012.

[KHKO91] M. A. Khan, J. M. Van Hove, J. N. Kuznia, and D. T. Olson. High electron mobility gan/al x ga1x n heterostructures grown by lowpressure metalorganic chemical vapor deposition. *Applied Physics Letters*, 58:2408, 1991.

[KKP$^+$00] S. P. Karna, H. A. Kurtz, A. C. Pineda, W. M. Shedd, and R. D. Pugh. Point defects in si-sio2 systems: current understanding. *Defects in SiO2 and related dielectrics: science and technology*, pages 599–615, 2000.

[KP70] W. Kern and D. A. Puotinen. Cleaning solutions based on hydrogen peroxide for use in silicon semiconductor technology. *RCA Review*, 31:187–206, 1970.

[KRL$^+$02] M. Kocan, A. Rizzi, H. Lüth, S. Keller, and U. K. Mishra. Surface potential at as-grown gan(0001) mbe layers. *Phys. Status Solidi B*, 234:773–777, 2002.

[KS05] G. Koley and M. G. Spencer. On the origin of the two-dimensional electron gas at the algan/gan heterostructure interface. *Applied Physics Letters*, 86(4):042107, 2005.

[KSY$^+$03] M. A. Khan, G. Simin, J. Yang, J. Zhang, A. Koudymov, M. Shur, R. Gaska, X. Hu, and A. Tarakji. Insulating gate iii-n heterostructure field-effect transistors for high-power microwave and switching applications. *IEEE Transactions on Microwave Theory and Techniques*, 51(2):624, 2003.

[KSZ$^+$95] P. Kung, A. Saxler, X. Zhang, D. Walker, T. C. Wang, I. Ferguson, and M. Razeghi. High quality aln and gan epilayers gown on (001) sapphire, (100), and (111) silicon substrates. *Applied Physics Letters*, 66:2958, 1995.

[Lig61] J. R. Ligenza. Effect of crystal orientation on oxidation rates of silicon in high pressure steam. *Journal of Physical Chemistry*, 65.11:2011–2014, 1961.

[LLH$^+$13] H.-Y. Liu, C.-S. Lee, W.-C. Hsu, L.-Y. Tseng, B.-Y. Chou, C.-S. Ho, and C.-L. Wu. Investigations of algan/aln/gan and mos-hemts on and si substrate and by ozone and water oxidation and method. *IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 60, NO. 7, JULY*, 60(7):2231–2237, 2013.

[LOPP12] P. Lagger, C. Ostermaier, G. Pobegen, and D. Pogany. Towards understanding the origin of threshold voltage instability of algan/gan mis-hemts. In *Proceedings of the IEEE Internation Electron Device Meeting*, 2012.

[LPO14] P. Lagger, D. Pogany, and C. Ostermaier. Enhancement of vth drift for repetitive gate stress pulses due to charge feedback effect in gan mis-hemts. In *Proceedings of the International Reliability Physics Symposium*, 2014.

[LRPO14] P. Lagger, M. Reiner, D. Pogany, and C. Ostermaier. Comprehensive study of the complex dynamics of forward bias-induced threshold voltage drifts in gan based mis-hemts by stress/recovery experiments. *IEEE Transactions on Electron Devices*, 2014.

[LRS99] M. Levinstein, S. Rumyantsev, and M. Shur, editors. *Handbook Series on Semiconductor Parameters.* World Scientific, London, 1999.

[LSP$^+$13a] P. W. Lagger, A. Schiffmann, G. Pobegen, D. Pogany, and C. Ostermaier. New insights on forward gate bias induced threshold voltage instabilities of gan-based mis-hemts. In *Proceedings of the WOCSDICE*, 2013.

[LSP$^+$13b] Peter Lagger, Alexander Schiffmann, Gregor Pobegen, Dionyz Pogany, and Clemens Ostermaier. Very fast dynamics of threshold voltage drifts in gan-based mis-hemts. *IEEE ELECTRON DEVICE LETTERS*, 34(9):1112–1114, 2013.

[LSR$^+$14] P. Lagger, P. Steinschifter, M. Reiner, M. Stadtmüller, G. Denifl, A. Naumann, J. Mueller, L. Wilde, D. Pogany, and C. Ostermaier. Role of the dielectric for the charging dynamics of the dielectric/barrier interface in algan/gan based metal-insulator-semiconductor structures under forward gate bias stress. *Applied Physics Letters*, tbd:tbd, 2014.

[McP10] J. W. McPherson. *Reliability Physics and Engineering.* Springer, 2010.

[MKAS03] C. R. Miskys, M. K. Kelly, O. Ambacher, and M. Stutzmann. Freestanding gan-substrates and devices. *Phys. Status Solidi C*, 0:1627–1650, 2003.

[MM66] Y. Miura and Y. Matukura. Investigation of silicon-silicon dioxide interface using mos structure. *Japanese Journal of Applied Physics*, 5.2:180, 1966.

[MTLC12] T. Marron, S. Takashima, Z. Li, and T. P. Chow. Impact of annealing on ald al2o3 gate dielectric for gan mos devices. *Phys. Status Solidi C*, 9:907–910, 2012.

[MWdW10] M. S. Miao, J. R. Weber, and C. G. Van de Walle. Oxidation and the origin of the two-dimensional electron gas in algan/gan heterostructures. *Journal of Applied Physics*, 107:123713, 2010.

[NB03] E. H. Nicollian and J. R. Brews. *MOS (Metal Oxide Semiconductor Physics and Technology).* Wiley Interscience, 2003.

[ON08] T. Oka and T. Nozawa. Algan/gan recessed mis-gate hfet with high-threshold-voltage normally-off operation for power electronics applications. *Electron Device Letters, IEEE*, 29(7):668 –670, july 2008.

[PC1]

[PNdFG14] G. Pobegen, M. Nelhiebel, S. de Filippis, and T. Grasser. Accurate high temperature measurements using local polysilicon heater structures. *IEEE Transactions on Device and Materials Reliability*, 14:169–176, 2014.

[PSC$^+$06] T. Palacios, C.-S. Suh, A. Chakraborty, S. Keller, S.P. DenBaars, and U.K. Mishra. High-performance e-mode algan/gan hemts. *Electron Device Letters, IEEE*, 27(6):428 – 430, june 2006.

[RF06] J. Robertson and B. Falabretti. Band offsets of high k gate oxides on iii-v semiconductors. *Journal of Applied Physics*, 100(1):014111, 2006.

[RFG$^+$12] F. Roccaforte, A. Frazzetto, G. Greco, F. Giannazzo, P. Fiorenza, R. L. Nigro, M. Saggio, M. Leszczynski, P. Pristawko, and V. Raineri. Critical issues for interfaces to p-type sic and gan in power devices. *Applied Surface Science*, 258:8324–8333, 2012.

[RFG$^+$14] F. Roccaforte, P. Fiorenza, G. Greco, M. Vivona, R. L. Nigro, F. Giannazzo, A. Patti, and M. Saggio. Recent advances on dielectrics technology for sic and gan power devices. *Applied Surface Science*, in press:in press, 2014.

[RR96] M. Razeghi and A. Rogalski. Semiconductor ultraviolet detectors. *Journal of Applied Physics*, 79:7433, 1996.

[RS] SERGEY L. RUMYANTSEV and MICHAEL. S. SHUR. *MATERIALS PROPERTIES OF NITRIDES. SUMMARY.*

[Sch06] D. K. Schroder. *Semiconductor Material and Device Characterization.* Wiley Interscience, third edition edition, 2006.

[Sch09] D. K. Schroder. Electrical characterization of defects in gate dielectrics. *CRC Press*, 2009.

[SCM$^+$01] I. P. Smorchkova, L. Chen, T. Mates, L. Shen, S. Heikman, B. Moran, S. Keller, S. P. DenBaars, J. S. Speck, and U. K. Mishra. Aln/gan and (al,ga)n/aln/gan two-dimensional electron gas structures grown by plasma-assisted molecular-beam epitaxy. *Journal of Applied Physics*, 90(10):5196–5201, 2001.

[Sin03] J. Singh. *Electronic and Optoelectronic Properties of Semiconductor Structures.* Cambridge University Press, 2003.

[SKS12] H.-A. Shih, M. Kudo, and T.-K. Suzuki. Analysis of aln/algan/gan metal-insulator-semiconductor structure by using capacitance-frequency-temperature mapping. *Applied Physics Letters*, 101:101ff, 2012.

[SN07] S. M. Sze and Kwok K. Ng. *Physics of Semiconductor Devices.* Wiley & Sons, 2007.

[SNA98] A. Stesmans, B. Nouwen, and V. V. Afanasev. Pb1 interface defect in thermal (100)si-sio2:si29 hyperfine interaction. *Physical Review B*, 58:15801–15809, 1998.

[Ste93] A. Stesmans. Structural relaxation of pb defects at the (111)si/sio2 interface as a function of oxidation temperature: the pb-generation-stress relationship. *Physical Review B*, 48:2418–2435, 1993.

[STK$^+$06] W. Saito, Y. Takada, M. Kuraguchi, K. Tsuda, and I. Omura. Recessed-gate structure approach toward normally off high-voltage algan/gan hemt for power electronics applications. *Electron Devices, IEEE Transactions on*, 53(2):356 – 362, feb. 2006.

[Ued13] Daisuke Ueda. Status quo and trends of gan power devices. In *IRPS*, 2013.

[UHU$^+$07] Y. Uemoto, M. Hikita, H. Ueno, H. Matsuo, H. Ishida, M. Yanagihara, T. Ueda, T. Tanaka, and D. Ueda. Gate injection transistor (git) - a normally-off algan/gan power transistor using conductivity modulation. *Electron Devices, IEEE Transactions on*, 54(12):3393 –3399, dec. 2007.

[VZKM01] R. Vetury, N.Q. Zhang, S. Keller, and U.K. Mishra. The impact of surface states on the dc and rf characteristics of algan/gan hfets. *Electron Devices, IEEE Transactions on*, 48(3):560 –566, mar 2001.

[WBTB$^+$11] J. Wuerfl, E. Bahat-Treidel, F. Brunner, E. Cho, O. Hilt, P. Ivo, A. Knauer, P. Kurpas, R. Lossy, M. Schulz, S. Singwald, M. Weyers, and R. Zhytnytska. Reliability issues of gan based high voltage power devices. *Microelectronics Reliability*, 51:1710–1716, 2011.

[WHS89] C. M. Wolfe, N. Holonyak, and G. E. Stillman. *Physical Properties of Semiconductors.* Prentice Hall, 1989.

[Wik06] Wikipedia, 2006.

[Wit98] A. Witek. -. *Diamond Related Materials*, 7:962–694, 1998.

[WMH$^+$05] O. Weidemann, E. Monroy, E. Hahn, M. Stutzmann, and M. Eickhoff. Influence of thermal oxidation on the electronic properties of pt schottky contacts on gan grown by molecular-beam epitaxy. *Applied Physics Letters*, 86:083507, 2005.

[WMZ$^+$13] T.-L. Wu, D. Marcon, M. B. Zahid, M. Van Hove, S. Decoutere, and Guido Groeseneken. Comprehensive investigation of on-state stress on d-mode algan/gan mis-hemts. In *Proceedings of the International Reliability Physics Symposium*, 2013.

[WWG99] N. J. Watkins, G. W. Wicks, and Y. Gao. Oxidation study of gan using x-ray photoemission spectroscopy. *Applied Physics Letters*, 75:2602, 1999.

[YSM12] Ramya Yeluri, Brian L. Swenson, and Umesh K. Mishra. Interface states at the sin/algan interface on gan heterojunctions for ga and n-polar material. *Journal of Applied Physics*, 111(4):043718, 2012.

[YTW$^+$13] Shu Yang, Zhikai Tang, King-Yuen Wong, Yu-Syuan Lin, Yunyou Lu, Sen Huang, and Kevn J. Chen. Mapping of interface traps in high-performance al2o3/algan/gan mis-heterostructures using frequency- and temperature-dependent c-v techniques. In *Proceedings of IEEE International Electron Device Meeting*, 2013.