

Stacked Layers of Different Porosity in 4H SiC Substrates Applying a Photoelectrochemical Approach

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Porous 4H-SiC layers were prepared from monocrystalline samples applying photo-electrochemical etching in hydrofluoric acid. The influence of both current and voltage controlled mode during photo-electrochemical porosification was investigated. It was found that the resulting degree of porosity, the homogeneity in porosity as well as the pore morphology mainly depend on the applied voltage, whereas the current level has an almost negligible impact on these important parameters. Based on these results, it is proposed that the formation of porous SiC during photo-electrochemical etching can be described by fractal growth. Finally the gathered knowledge allowed to detach the porous 4H-SiC layers, which comprised several sub-layers of alternating degree of porosity, from the 4H-SiC substrate. Such layers of tailored porosity are key components for several advanced device concepts such as optical filters or membranes for biological applications.

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Manuscript received July 13, 2017. Published August 24, 2017.

A common method to prepare porous Si is electrochemical etching in HF based solutions.¹ There are numerous application scenarios of porous Si, such as electrode material in super-capacitors, 2 as sacri-ficial layer in the production of MEMS devices^{[3](#page-10-2)} or as optical filters in bio- or vapor-sensors.[4](#page-10-3)[,5](#page-10-4) In the last application scenario, a stacked layer of porous silicon is electrochemically etched into a silicon wafer. The individual porous layers of the stack show alternating degrees of porosity and thus have a different index of refraction. This results in a wavelength selective reflection of optical light.⁶ Undoubtedly, porous Si is a well-established material for future micro- or nanomachined device architectures, but it shows a poor chemical stability when ex-posed to e.g. air at higher temperatures or alkaline electrolytes.^{[7,](#page-10-6)[8](#page-10-7)} Therefore it has to be covered with a dense protective layer when operation in harsh or biological environments is targeted.[9](#page-10-8) This drawback encourages research devoted to other porous materials that can be used instead of porous Si without a surface protection. A promising candidate is porous SiC prepared from single crystalline wafers because it shows a higher chemical stability than silicon.¹⁰ In contrast to electrochemical etching of Si, photo-electrochemical etching (PECE) of SiC in HF based etching solutions is a comparably challenging task and hence, only a limited number of publications exist[.11](#page-10-10)[,12](#page-10-11) Some authors report a skin layer on top of the porous structure, which exhibits only a few pores with diameters in the nm range.^{[13,](#page-10-12)[14](#page-10-13)} This skin layer is followed by a cap layer which shows an irregular porous structure.^{[15](#page-10-14)} This problem has been addressed recently by a combination of metal assisted photochemical etching with PECE[.16](#page-10-15) Metal assisted photochemical etching (MAPCE) can be utilized to generate a layer in the μm range prior to PECE. The pore tips of this porous layer provide initiation sites for PECE. Thus, neither a skin nor a cap layer are observed.

Furthermore some authors report about an increased porosity at the bottom of the porous layer, despite constant current conditions were applied during etching.^{[17](#page-10-16)} Porous layers prepared with constant voltage conditions showed a decreasing porosity with depth.^{[11](#page-10-10)} These observations are cumbersome when a constant degree of porosity is required, such as in the preparation of optical filters^{[18](#page-10-17)} or membranes for biological applications.^{[19](#page-10-18)}

This work aims to create a process serving as technological basis for the preparation of porous SiC layers that can be used within e.g. optical Bragg filters. In particular this requires the capability to produce individual porous layers with alternating degree of porosity, while the porosity within each sub layer is constant. To achieve this goal the above mentioned drawbacks of PECE have to be overcome.

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Beside these technological issues this work also intends to contribute to the fundamental knowledge of PECE of SiC which is necessary for the implementation as a reliable processing technology.

Experimental

For this study square-shaped samples cut from a single crystalline n-doped 4H-SiC wafer with side lengths of 2.5 cm were used. The samples had a bulk resistivity of 0.02 and 0.106 Ω cm, respectively. First, all samples were consecutively soaked for 5 minutes in acetone, isopropanol and ethanol. After this cleaning process a porous layer with an approximate thickness of 1 μm was generated with MAPCE.²⁰ MAPCE does not require an external electric field, thus samples are just immersed in an etching solution, containing HF and oxidizing agent as is shown in Figure [1.](#page-0-1) A noble metal deposited at

the samples surface acts as local cathode where the oxidizing agent is reduced. Simultaneously the bare SiC surface is oxidized, while the formed oxide is dissolved with HF. This leads to the formation of a porous SiC layer. During the whole process UV light irradiation is required to generate the necessary minority charge carriers (i.e. holes) for the etching reaction. Furthermore a decreased contact resistance at the noble metal/SiC junction enhances the etching performance, as electrons are transferred across this interface during the etching reaction to preserve charge neutrality.²⁰ Therefore samples with a bulk resistivity larger than 0.02Ω cm were surface near doped with a phosphoric acid/ethanol solution under high temperatures of 1100◦C (Figure [1](#page-0-1) ii). The experimental details of the doping process can be found elsewhere.¹⁶

Samples with a bulk resistivity of $0.02 \Omega \cdot cm$ were not doped but cleaned with an inverse sputter etching process for 120 s at 500 W, prior to sputter deposition of Pt (see Figure $1 - step$ $1 - step$ i). Afterwards, an array of 300 nm thin, circular Pt pads was realized in the center of each sample using sputter deposition and standard photolithography (see Figure 1 – step iii). The diameter of each pad was 1 mm and the total area of the pads was 50 cm^2 . For sputter deposition and sputter cleaning, a LS730S Von Ardenne sputter equipment was used. After sputter deposition of Pt, the samples were annealed in a Nabertherm L9/11/SKM oven under Argon flow of 40 L/h, starting at 800◦C with a subsequent 30 minute ramp up to 1100◦C. This temperature was held for 5 minutes. This was done to further decrease the contact resistance between the 4H-SiC substrate and the Pt pads which served as cathode during MAPCE.

Then the samples were immersed in an etching solution containing 0.04 mol/L $Na₂S₂O₈$ and 1.31 mol/L HF—under UV light irradiation. At the blank 4H-SiC surface, not covered with Pt pads, oxidation takes place according to Equations $1-3$. During this process the necessary holes $h⁺$ are generated with UV light illumination. The formed oxide is then dissolved with HF, as is shown in Equation [4.](#page-1-2) To restore charge balance the oxidation reaction described in Equation [1](#page-1-0) has to be counterbalanced with a reduction reaction. This is realized at the etching solution/Pt interface by the reduction of $S_2O_8^{2-}$ ions (see Equation [5\)](#page-1-3).

$$
SiC + 4H_2O + 8h^+ \to SiO_2 + 8H^+ + CO_2
$$
 [1]

$$
SiC + 2H2O + 4h+ \rightarrow SiO + 4H+ + CO
$$
 [2]

$$
\text{SiC} + 3\text{H}_2\text{O} + 6\text{h}^+ \rightarrow \text{SiO}_2 + 6\text{H}^+ + \text{CO} \tag{3}
$$

$$
SiO2 + 6HF \rightarrow H2SiF6 + 2H2O
$$
 [4]

$$
4S_2O_8^{2-} + 8e^- \to 8SO_4^{2-} \tag{5}
$$

As UV source a 250 Watt ES280LL mercury arc lamp at full spectrum was used. The distance between the UV source and the sample was approximately 3 cm and all MAPCE experiments lasted for 120 minutes. During etching, the samples were mounted in a standard electro-chemical cell for the porosification of silicon purchased from AMMT GmbH and the effective volume of etching solution was approximately 150 mL.

The experimental parameters were systematically modified to improve the preparation process and to minimize the use of HF containing solutions. This was the case for all experiments were alternating voltage conditions were applied (see section Voltage controlled experiments). In particular, Pt was sputter deposited at the edges of the sample covering a total area of 1.0 cm^2 . Furthermore 10 mL of an etching solution containing 0.15 mol/L Na₂S₂O₈ and 1.31 mol/L HF were used for MAPCE while a custom built 18 W UV source (254 nm peak intensity) was utilized. The etching time was 2 hours while the old etching solution was replaced every 30 minutes with fresh one. The distance between the UV source and the sample was here approximately one cm.

After MAPCE, photo-electrochemical etching (PECE) was performed. The experiments were performed with the porous silicon

Figure 2. Schematic depiction of PECE.^{[16](#page-10-15)}

etching chamber from AMMT mentioned above while the 250 Watt mercury lamp was used as UV source. A schematic illustration of PECE with the given equipment is shown in Figure [2.](#page-1-4) In contrast to MAPCE, PECE utilizes an external power source (CPX400DP Dual 420 watt power supply from Aim-TTi - Thurlby Thandar Instruments Limited) to initiate etching. For the experiments an etching solution containing 5.52 mol/L HF and 1.7 mol/L ethanol was used. In the given experimental configuration the sample is mounted between two fluidically isolated compartments filled with etching solution. Voltage is applied and the side of the sample close to the negative potential is illuminated with UV light. At this side, a porous layer forms due to the chemical reactions described in Equations [1–](#page-1-0)[4.](#page-1-2) Simultaneously electrons need to leave the semiconductor at the not UV irradiated side (see Figure [2\)](#page-1-4) according to Equation [6.](#page-1-5)

$$
2H_3O^+ + 2e^- \to H_2 + H_2O \tag{6}
$$

The total area etched in each experiment was approximately 3.14 cm2. After etching, the samples were investigated with a Hitachi SU8030 scanning electron microscope (SEM) using acceleration voltages between 1 and 5 kV. All etching experiments were performed on the Si face of the sample. Fourier transform infrared spectroscopty (FT-IR) measurements were performed in attenuated total reflection (ATR) and transmission mode. For both a different Bruker Tensor FT-IR spectrometer was used. Reflectance spectra were recorded with a Filmetrics F20 layer thickness measurement device.

TOF SIMS depth profiles were acquired using a TOF-SIMS5 (IonTof GmbH, Münster, Germany). A 25 keV Bi^+ primary ion beam was used for analysis (high current bunched mode²¹). For sputtering a 2 keV Cs⁺ beam was used. The analysis area was set to $50 \times 50 \,\mu$ m with a pixel resolution of 128×128 and the crater size to 400×400 μm. The measurements were carried out in negative ion mode using the interlaced mode with a cycle time of 100 μs. Low energy electron flooding (21 V) was used.

Results and Discussion

*Current controlled experiments.—*To generate a stack of layers with alternating degrees of porosity, while the porosity within each sub layer had to be constant, the effect of changing electrical conditions during PECE is investigated in the first part of this paper. This means that the power source was programmed to carry out a sequence of changing current densities. The applied sequence with the corresponding time intervals is given in Table [I.](#page-2-0)

The first sample that was subjected to the described sequence of current densities had a resistivity of $0.02 \Omega \cdot$ cm. The corresponding voltage and current density characteristics during the PECE experiment are illustrated in Figure [3.](#page-2-1) One can see that the programmed current density could be maintained throughout the whole experiment, except at the beginning of period 5 where the current density

was lower than the targeted value for a short period. Simultaneously to this decreased current density, a sharp increase to the maximum possible voltage of 60 V could be observed. At all the other steps the voltage increased at the beginning until a relatively constant value was reached.

After etching the sample was cracked for scanning electron microscope (SEM) analysis. During cracking an approximately 20 μm thick, porous film detached from the bulk sample (the principle of thin film detachment is illustrated in Figure [13](#page-6-0) while an example of a detached film is shown in Figure [17\)](#page-7-0). A cross sectional SEM micrograph of this film is shown in Figure [4.](#page-2-2) In this micrograph several layers having a different microstructures can be identified. On top there is a porous layer which was generated during the MAPCE process. This layer is followed by 4 other layers which can be assigned to the first four current density periods in Figure [3.](#page-2-1) The expected 4 remaining layers from the current density periods 5–8 could be found in the cross-sectional analysis of the bulk sample.

Figure 3. Voltage and current density characteristics during current controlled PECE of a 4H-SiC sample with a bulk resistivity of $0.02 \Omega \cdot cm$.

Figure 4. Detached porous 4H-SiC film after PECE of a sample with a bulk resistivity of $0.02 \Omega \cdot cm$.

An examination of the bottom of the detached film and the top of the porous substrate material showed that lines of breakage had been created on the detached film. This is illustrated in Figure [5.](#page-2-3) In Figure [5a](#page-2-3) it can be seen that there is a first line of breakage after the fourth porous PECE layer. This line of breakage is followed by a thin porous layer and a second line of breakage at which separation took place during cracking of the sample. The lines of breakage can be assigned to specific events in the current density and voltage characteristics, shown in Figure [3.](#page-2-1) The first line of breakage can be assigned to the very beginning of the fifth period where the current density shows a single peak (marked with a). Then a region with decreased current density follows which caused the very bottom layer in Figure [5a.](#page-2-3) Finally the line of breakage which caused separation can be assigned to peak b in the current density evolution.

Figure 5. Cross-sectional view on a) the bottom region of a detached porous 4H-SiC film and b) the corresponding top region of the bulk material from which the film was separated. The bulk resistivity of the sample was 0.02 $\Omega \cdot \text{cm}$.

Figure 6. SEM micrographs of a 4H-SiC sample with a bulk resistivity of 0.02Ω cm after PECE with corresponding black and white images obtained with image processing. a) Transition from period 1 to 2. b) Transition from period 7 to 8.

The porous region generated after the current density peak b could be identified at the top of the bulk sample which is illustrated in Figure [5b.](#page-2-3) At its end a third line of separation (indicated by yellow arrows) started to form. A corresponding peak (marked with c in Figure [3\)](#page-2-1) is observed in the voltage evolution during etching, while

the current density stayed relatively constant. So far the presented findings showed that the transition from a low to a high current density mode caused the formation of lines of breakage in the porous material. These lines of breakage could be assigned to either peaks in the current density (see Figure 3 ; peaks a and b) or to the voltage characteristics (Figure [3,](#page-2-1) peak c).

To further analyze this behavior, the remaining porous layers generated during the current density periods 1–4 and 6–8 were investigated. Therefore the porosity of the porous layers was estimated with image processing. Denoising and adaptive Gaussian image thresholding were performed by using the OpenCV library²² interfaced with the Python programming language.[16](#page-10-15) Typical results are shown in Figure [6,](#page-3-0) where the original SEM micrographs and the black and white images are presented to illustrate the trend in porosity. In particular, the porous regions resulting from the current density period transitions $1 \rightarrow 2$ and $7 \rightarrow 8$ are displayed. Basically, the porosity decreases at the beginning of a new current density period until it becomes relatively constant. This is similar to the voltage characterisitics during each period of constant current density (see Figure 3 – voltage characteristics). For a direct comparison of the voltage characteristics and the resulting porosity both quantities were plotted in Figure [7.](#page-3-1) The degree of porosity was determined with the black and white images obtained from image processing. Each number in Figure [7](#page-3-1) represents a current density period as defined in Table [I.](#page-2-0)

Independent of the current density level, the porosity and the voltage drop at the onset of a new current density period. Afterwards both quantities increase and in most cases they show a saturation behavior.

To investigate whether this behavior is also true for samples with higher bulk resistivities, a similar experiment was performed with a

Figure 7. Estimated porosity (blue) and voltage (red) characteristics during each current density step. The numbers correspond to the current density periods shown in Figure [3.](#page-2-1)

Table II. Programmed sequence of changing current densities during PECE of a 4H-SiC sample with a bulk resistivity of 0.106 $\Omega \cdot \text{cm}$.

Period	Duration [min]	Targeted current density [mA/cm ²]
		50.9
		33.7
3		25.5
4		9.5
5		25.5
6		9.5
		25.5
8		9.5

sample having a bulk resistivity of $0.106 \Omega \cdot cm$. The programmed current density periods for this experiment are shown in Table [II.](#page-4-0) The periods 5 to 8 were programmed with a lower current density to avoid the formation of lines of separation and subsequent separation of a porous film like in the previous experiment. The corresponding current density and voltage characteristics are illustrated in Figure [8.](#page-4-1) The different current periods (see Table [II\)](#page-4-0) are indicated by red numbers. At the beginning of the periods 1 to 4 the voltage tends to increase. During the periods 3 and 4 the voltage becomes rather constant like it was in the case for the sample with a bulk resistivity of $0.02 \Omega \cdot$ cm. This indicates that the etching process turned into a steady state condition. During the periods 1 and 2 the voltage still increased at the end of the period or the maximum possible voltage had been reached. Here a steady state condition could not be reached because of the higher desired current density and the maximum possible voltage of 60 V.

Figure 8. Voltage and current density characteristics during current controlled PECE of a 4H-SiC sample with a bulk resistivity of $0.106 \Omega \cdot cm$.

During the periods 5 and 7 the desired current density could not be maintained by the power supply. This is accompanied by a voltage increase to the maximum possible value.

To estimate the impact on the degree of porosity the porosity and the voltage characteristics were plotted as done for the sample with a bulk resistivity of $0.02 \Omega \cdot \text{cm}$ (see Figure [9\)](#page-5-0).

Basically, the porosity shows a similar trend as the voltage. This is essentially the same result as has been obtained for the sample with a bulk resistivity of $0.02 \Omega \cdot$ cm. One difference, however, can be seen at the current density period transitions $4 \rightarrow 5$ and $6 \rightarrow 7$, respectively. Here the current density stayed relatively constant while the voltage raised to the maximum possible value. This instantaneous change in voltage was accompanied by a sudden increase in the resulting porosity, at an almost constant current density. The corresponding SEM micrographs together with their black and white images are given in Figure [10.](#page-5-1) In both cases the pore morphology as well as the degree of porosity changes instantaneously.

The collected data in current controlled mode showed that the resulting porosity as well as the pore morphology are predominantly determined by the applied voltage and not by the current density. In most cases the voltage and the resulting porosity increase in one period of constant current density until they become almost constant. This indicates that a period of constant current density starts with a transition phase until a steady state condition is reached. Later in the paper possible factors that determine this behavior are given (see chapter Discussion). On the other hand, when the voltage increased at a relatively constant current density the resulting porosity also increased instantaneously. This shows that changes in the pore morphology as well as the degree of porosity are determined by the applied voltage and do not necessarily require a change in current density. For the sample with a bulk resistivity of $0.02 \Omega \cdot cm$, the increase in porosity was so high that even the separation of a porous 4H-SiC film could be observed. This separation process is somewhat different from the other observations, since the second line of breakage was not accompanied with a voltage peak. This case is discussed in more detail in the chapter Discussion of the results. These initial results showed that a current controlled PECE process is not suitable for the preparation of a porous SiC stack of layers that can be utilized as e.g. optical Bragg filter, since the degree of porosity needs to be constant throughout every sub layer of the stack. 6

*Voltage controlled experiments.—*The experimental observations so far showed that the degree of porosity and etching rate strongly depend on the applied voltage. Thus a sample with a bulk resistivity of $0.02 \Omega \cdot$ cm was etched under voltage controlled conditions. The performed sequence of voltage steps is shown in Table [III.](#page-5-2) The values of the voltages were chosen such that they were similar to the observed voltage values during the first current controlled experiment, before lines of separation occurred (see Figure [3\)](#page-2-1).

The evolution of the voltage and the current density as well as the resulting porosity can be seen in Figure [11.](#page-6-1) The current density tends to decrease in every period of constant voltage. The porous layer generated during the first voltage period showed a decreasing tendency in porosity with depth. The porous layers generated during the voltage periods 2, 3 and 4 showed a slightly increasing porosity, despite a simultaneously decreasing current density. In contrast to the experiments in current controlled mode, the degree of porosity is relatively constant with depth. This is exemplary illustrated in Figure [12,](#page-6-2) where the transition from the third to the fourth porous layer is shown. In addition, the porosity drops only slightly at the beginning of a new voltage period.

These findings confirm that the resulting degree of porosity as well as the trend of the porosity with depth crucially depend on the applied voltage and not the current density. From a practical point of view this means that voltage controlled experiments are preferred for the preparation of porous SiC layers with homogeneous porosity as requested for e.g. optical filters.

To demonstrate an alternating degree of porosity in subsequent layers further experiments were conducted with alternating voltages

Figure 9. Estimated porosity (blue) and voltage (red) characteristics during each current density step. The numbers correspond to the current density periods shown in Figure [8.](#page-4-1)

Figure 10. SEM micrographs of a 4H-SiC sample with a bulk resistivity of $0.106 \Omega \cdot$ cm after PECE with corresponding black and white images obtained with image processing. a) Transition from period 4 to 5. b) Transition from period 6 to 7. The $7th$ layer was generated during the current density periods 7 and 8 (see Figure [8\)](#page-4-1).

of 11.5 V and 8.5 V based upon the previous experiment. Furthermore it was aimed to separate the porous layers from the bulk material after etching with the formation of a line of breakage as it had been observed during current controlled experiments. Therefore the experimental parameters for MAPCE were modified (see Experimental parameters section) such that the Pt was sputter deposited at the corners of the sample. Figure [13](#page-6-0) shows the principle of the desired preparation process. When the Pt is sputter deposited at the edges of the sample, MAPCE can be performed again after the separation of the porous layer. Doing so, the sample can be re-used several times for porous film preparation.

The first experiment was performed with alternating voltages of 11.5 V and 8.5 V while the duration of each period was one minute (see Supplementary material S1). It was found, that the thickness of

Figure 11. Voltage and current density characterisitics during voltage controlled PECE of a 4H-SiC sample with a bulk resistivity of $0.02 \Omega \cdot cm$.

Figure 12. Cross-sectional SEM micrograph of a 4H-SiC sample with a bulk resistivity of 0.02Ω cm after voltage controlled PECE with a corresponding black and white image obtained with image processing.

the porous sub-layers decreases with etching time. To counterbalance this effect the durations of the periods were increased with increasing etching time, according to a rough calculation presented in the Supplementary material S1.

The individual time intervals obtained for each period are illustrated in Table [IV.](#page-6-3) The first period represents a starting period analogous to the experiment with fixed time intervals while the last period had the purpose to separate the porous layer from the substrate (see Supplementary material S1 for details). The values for both, the porous

Figure 13. Principle of porous layer separation.

Table IV. Programmed sequence of alternating voltages during PECE of a 4H-SiC sample with a bulk resistivity of $0.02 \Omega \cdot cm$. **Alternating etching periods with adjusted time intervals and a starting period of 0.05 minutes.**

layer thickness and the transported charges are also shown in the same table. Their relationship is discussed in the section Discussion of the results. The goal was to generate the same thicknesses for periods of the same voltage. This has been partially fulfilled up to period 8. In the following layers, however, the resulting thickness values diverge.

The corresponding current and voltage characteristics are shown in Figure [14.](#page-6-4) The etching periods according to Table [IV](#page-6-3) are indicated in the current density plot. It can be seen that the current density decreases throughout the whole sequence until the voltage raises at the end, implemented to separate the porous layer from the bulk sample.

Figure 14. Voltage and current density characteristics comprising alternating etching periods with adjusted time intervals and a starting period of 0.05 minutes during voltage controlled PECE of a 4H-SiC sample with a bulk resistivity of $0.02 \Omega \cdot$ cm. At the end of the experiment the voltage is increased to separate the porous layer from the substrate.

Figure 15. Porosity versus etching depth for a voltage controlled PECE of a 4H-SiC sample with a bulk resistivity of 0.02Ω cm, based on alternating etching periods with adjusted time intervals and a starting period of 0.05 minutes.

The resulting porosity is shown in Figure [15.](#page-7-1) Despite the decreasing current density throughout PECE, the porosity stayed relatively constant for a given voltage and changes instantaneously when the voltage is switched between 11.5 V and 8.5 V as can also be seen in Figure [16.](#page-7-2) There the porous sub-layers corresponding to the etching periods 3, 4 and 5 are illustrated.

Finally, also the separation process during period 12 succeeded. After removing the sample from the etching chamber, the etched porous layer easily detached from the bulk sample during cleaning with deionized water. Both, the sample and the detached porous layer are shown in Figure [17.](#page-7-0)

Beside these findings, it can also be seen that the etching rate was significantly higher during the first period (compare with Supplementary material S1). This phenomenon is discussed in the section Discussion.

The resulting degree of porosity can be properly adjusted by a constant voltage during etching, relatively independent of the current density. Also sharp borders between the porous sub-layers can be formed by utilizing voltage controlled PECE. Furthermore the porous layer can be separated from the sample by a steep increase of the voltage.

Discussion

Basically, the degree of porosity as well as the pore morphology are crucially influenced by the voltage while the current density shows no correlation with these properties. This observation indicates that the etching process can be described in a similar manner as fractal structures in solids obtained from dielectric breakdown.²³ In such processes, growth takes place along the pore tips where the electric field strength is higher compared to the surrounding regions. This argumentation is supported by a study published previously where it was shown that a porous layer generated with MAPCE prior to PECE

Figure 16. Cross sectional SEM micrograph of a 4H-SiC sample after voltage controlled PECE comprising alternating etching periods with adjusted time intervals and a starting period of 0.05 minutes. The sample had a bulk resistivity of $0.02 \Omega \cdot \text{cm}$.

Figure 17. Detached porous layer of 4H-SiC after PECE and the corresponding 4H-SiC sample.

enhances the uniformity of the porous layer.^{[4](#page-10-3)} There it was found that the first pores that are formed with PECE initiate at the pore tips of the previously formed porous layer.

To further confirm the similarity between dielectric breakdown and PECE, an experiment with alternating voltages (10 V and 5 V; 1 minute durations, see Supplementary material S6 for a current and voltage plot) was performed. The intention was to decrease the porosity and thus the amount of pore tips during the periods of low voltage. Indeed, the result differed strongly from all the previously performed experiments as can be seen in Figure [18.](#page-7-3) First, the etching fronts are not parallel to the sample's surface. Such a behavior had not been observed for the samples prepared so far. This shows that for a uniform etching pattern the pore tip density is not allowed to drop below a certain value. This can also be seen by so-called Lichtenberg Figures (see black arrow in Figure [18\)](#page-7-3). The presence of such patterns is typical when dielectric breakdown has occured, where the direction of the growth follows the regions of highest electric field strength.²⁴

From the experimental data it is reasonable to assume that at an increased voltage the active area at the pore tip is increased such that a higher porosity results. Figure [19](#page-8-0) shows the thickness of the porous sub-layers versus the transferred charge obtained from the last PECE experiment performed in the section Voltage controlled experiments (see Table [IV\)](#page-6-3) with adjusted time intervals.

It can be seen that a higher amount of transferred charge as well as a higher voltage lead to a decreased thickness of a single porous

Figure 18. Cross section SEM micrograph of a sample etched with alternating voltages of 10 V and 5 V. The samples bulk resistivity was $0.02 \Omega \cdot cm$. Etching periods had a constant time interval of 1 minute.

Figure 19. Transferred charge versus the porous layer thickness obtained from voltage controlled PECE. The transferred charge values are those given in Table [IV.](#page-6-3)

sub-layer. This confirms the statement that with increased voltage the active area at the pore tip is increased as well. Furthermore data points of constant voltage tend to be at the same position in Figure [19.](#page-8-0) The two data points corresponding to the highest and lowest transferred charge do not fit into this pattern. This can be explained as follows. The 11.5 V data point that groups with the 8.5 V data points represents the initial porous layer (period 1 in Table [IV\)](#page-6-3). The initial porous layers always showed an increased etching speed, which may be due to different starting conditions. The initiation sites for the first layer are the pore tips from the MAPCE layer and they are larger than the pores from PECE. This effect has not been studied in more detail, but explains why the data point corresponding to the lowest amount of transferred charge does not group with the other 11.5 V data points. The other data point that does not fit into the described pattern is the 8.5 V data point corresponding to a transferred charge of 15.4 C. Here the etching time (and transferred charge) was significantly larger than for the other 8.5 V data points.

Finally the chemical etching mechanism is discussed. During PECE, holes h^+ are consumed as is described in Equations [1–](#page-1-0)[3.](#page-1-1) There it is stated, that 4, 6 or 8 holes are required to oxidize one formula unit of SiC. The data presented so far, allows the estimation of the amount of holes h ⁺ that are needed to dissolve one formula unit of SiC during the porosification processes (see Supplementary material S2). This is exemplarily illustrated in Figure [20.](#page-8-1) The amount of holes needed is shown for the voltage controlled PECE experiment with adjusted times and alternating voltages (the corresponding experimental data is shown in Table [IV](#page-6-3) and Figure [14\)](#page-6-4). It can be seen that the amount of holes changes with voltage as well as with increasing etching time.

Figure 20. Average amount of holes needed to dissolve a formula unit of SiC during an etching period. The corresponding experimental data are illustrated in Table [IV.](#page-6-3) The sample bulk resistivity is $0.02 \Omega \cdot cm$.

Figure 21. Amount of holes that are needed to dissolve a formula unit of SiC und current controlled conditions. The sample bulk resistivity is 0.02Ω cm. The corresponding current density and voltage characteristics are shown in Figure [3.](#page-2-1)

The former is reasonable because the electrochemical oxidation of SiC can be realized via several reaction paths, $15,25$ $15,25$ each with a different activation energy and different amount of holes needed. When the voltage is modified, the weighting of each reaction path contributing to the overall oxidation process changes. In particular, it can be seen that the generation of porous sub-layers with a higher degree of porosity requires a higher amount of holes to dissolve SiC (compare Figure [20](#page-8-1) with Figure [15\)](#page-7-1).

The overall increase of the amount of holes with etching time is attributed to diffusion, as explained as follows: all experiments showed on average an increasing amount of holes needed with enhanced etching time (see Figures in the Supplementary material S3). The only exception was the first current controlled PECE experiment. Figure [21](#page-8-2) shows a plot of the holes needed corresponding to the first performed current controlled PECE experiment (see Figure [3](#page-2-1) for the current and voltage characteristics). At the beginning of period 5 the porous film detached from the bulk sample (shown in Figure [4\)](#page-2-2). Thus it is reasoned that the supply with fresh etching solution was improved during the following periods, which caused a decrease of the amount of holes needed for dissolution of a formula unit of SiC.

These observations show that the applied voltage as well diffusion through the porous layer are the dominating factors. But, the amount of required holes is larger than those reported in literature. This may be due to an underestimation of the porosity because image thresholding provides only an approximation of this parameter. Furthermore the error in the calculation of the holes is larger when n_{avg} is substantially higher than 8 as can be seen in Figure [21](#page-8-2) (for details see Supplementary Material S2).

In most of the experiments, a transient phase of the voltage and the porosity could be observed at the beginning of a new period of constant current density (see Figures [7](#page-3-1) and [9\)](#page-5-0). This means that the electrolyte/semiconductor interfacial resistance (ESIR) increases with time until it becomes constant. This is at first counterintuitive because an increasing porosity (and thus an increased area for charge transport) should lower the resistance for charge transport. A chemical interpretation of the transient behavior, however, provides an adequate explanation. As stated in literature, the dissolution of SiC is a two-step process, involving the oxidation of SiC and subsequent dissolution of the oxide with $HF¹¹$ $HF¹¹$ $HF¹¹$ It has been shown that the electrolytic oxidation of SiC generates an amorphous oxide layer on its surface, which is permeable for electrolyte solutions.²⁶ An amorphous layer has also been found on the surface of porous SiC prepared with PECE.¹⁵ When the dissolution rate of the oxide is slower than its formation rate, the ESIR increases. In this case the voltage increases, which leads to a higher porosity and actively etched area. This, in turn, decreases the formation rate of the oxide layer per unit area because the same amount of charge can pass through a larger area. At some point, a

Figure 22. SIMS depth profile of a porous SiC sample with alternating layers of low and high porosity. The bulk resistivity of the sample is $0.02 \Omega \cdot cm$.

steady state condition is reached. The presence of an oxide layer on the surface of porous SiC is proved by Fourier transform infrared (FT-IR) spectroscopy and secondary ion mass spectrometry (SIMS) depth profiling.

Figure [22](#page-9-0) shows the SIMS depth profile of a sample that was etched with alternating voltages of 11.5 V and 8.5 V. O−, F[−] as well as C_xH^- and CN^- fragments were identified in the mass spectrum. Oxygen and fluoride are present due to the etching process while the nitrogen is due to the n-doping of the sample. The variation in the measured intensities in the depth profile is due to the porosity profile of the sample. The Si[−] and C[−] signals exceeded the limits of the detector, thus $30\,\text{Si}^-$ and C_2H^- are plotted respectively. Elemental information gained by the SIMS measurement can be used for interpretation of the IR spectra shown in Figure [25.](#page-9-1) The porous thin film for SIMS profiling was etched under charge controlled conditions. This means that the voltage was switched after a specific amount of charge (11.5 V phase: 0.6 C; 8.5 V phase: 0.12 C) had been transferred during each sub-layer formation. This was already done with regard to the preparation of optical filters where thin sublayers in the 50 nm dimension are required. The charge controlled mode was chosen as there is a correlation between transferred charge and porous layer thickness (see Figure [19\)](#page-8-0).The corresponding cross sectional SEM micrograph is shown in Figure [23.](#page-9-2) Reflection measurements at the bottom of the porous thin film showed that visible light is selectively reflected (see Figure [24\)](#page-9-3). This is a first proof of principle that PECE is a suitable method for producing porous SiC optical filters.

The IR spectra were acquired in attenuated total reflection (ATR) and transmission mode. One can see three different spectra obtained

Figure 23. Cross sectional SEM micrograph of a porous 4H-SiC film prepared on the dense 4H-SiC substrate with alternating voltages. The bulk resistivity of the sample is $0.02 \Omega \cdot cm$.

Figure 24. Reflection curves of a porous SiC film prepared with alternating voltages under charge controlled conditions. The bulk resistivity of the sample is $0.02 \Omega \cdot \text{cm}$.

from two samples. A porous, 4H-SiC film was detached from a bulk sample and measured in ATR and transmission mode while a not etched bulk sample was only measured in ATR mode. The experimental details of the detached film preparation can be found in the Supplementary material S4. First the porous film is compared with a bulk sample of 4H-SiC. Secondly the ATR measurement of the porous film is compared with a measurement in transmission mode. All samples had a bulk resistivity of $0.02 \Omega \cdot cm$.

There is a significant difference between the ATR-IR spectra of a detached porous SiC film and the original bulk SiC (Figure [25a\)](#page-9-1).

Figure 25. FT-IR spectra of a porous 4H-SiC sample detached from the substrate, measured in ATR mode and in transmission mode. a) Comparison of etched and not etched sample with ATR method. b) Comparison of an etched sample in transmission and ATR mode. All samples had a bulk resistivity of $0.02 \Omega \cdot \text{cm}$.

The spectrum of the latter sample shows two characteristic peaks of SiC at 800 cm⁻¹ (TO phonon) and 975 cm⁻¹ (LO phonon).^{27,[28](#page-10-27)} The etched sample also shows these peaks together with a main peak at 1030 cm⁻¹ which is attributed to Si-O-Si stretching vibrations.²⁹ The minor peak at 975 cm⁻¹ can be assigned to Si-F₂ vibrations.^{30,[31](#page-10-30)} According to literature and in agreement with the SIMS results it is also possible that C-F vibrations contribute to this peak (C-F bending at 1100 cm−1)[.32](#page-10-31) Several peaks also appear at higher wavenumbers, which are due to functional groups attached during PECE. The peak at 1460 cm⁻¹ can be assigned to C-H bending,^{[33](#page-10-32)} while the two peaks at higher wavenumbers are probably due to N-H vibrations.^{[33](#page-10-32)} The detached film had only a thickness of about $4 \mu m$, so a measurement in transmission mode was also possible. The corresponding spectrum (see Figure [25b\)](#page-9-1) shows two main peaks which can be attributed to SiC vibrations at 800 cm⁻¹ (TO phonon) and 890 cm⁻¹ (Si-C stretching),³⁴ but no peaks from an Si-O-Si stretching vibration or other functional groups at higher wavenumbers are detected. The small peaks at 1545 cm⁻¹ and 1625 cm⁻¹ are due to phonon overtones of SiC.^{27,[28](#page-10-27)} So, the measurement in transmission mode shows that the detached porous film still consists mainly of SiC. This is in accordance with the SIMS measurement where the C- and Si-signals exceeded the limits of the detector. The surface sensitive ATR measurement implies that the porous film is covered with an oxide layer and other functional groups.

Finally the first layer separation process during current controlled PECE is discussed. The corresponding current and voltage evolution is shown in Figure [3.](#page-2-1) The peak "a" in the current density is also accompanied by a steep voltage increase and thus a line of separation occurred in the porous layer. The following decrease in current density (and thus ESIR) can be explained with a decrease in the amount of pore tips, which are required for further etching. Such a phenomenon is also observed when no MAPCE is done prior to PECE.^{14[,16](#page-10-15)}

Conclusions

In this study basic investigations are presented for a micromachining process which can be used to prepare stacked layers of porous SiC having a highly different degree of porosity. The porosity should be constant within each sub-layer to a maximum degree so that the films could be used as e.g. optical Bragg filters. For this purpose photoelectrochemical etching (PECE) was utilized. The first samples were etched under current controlled conditions like it is done for the preparation of porous silicon optical filters. This approach proved to be inappropriate for porous SiC because the resulting degree of porosity turned out to be almost independent of the current density. In contrast, the degree of porosity shows similar trends as the voltage during experiments, both exhibiting a transient phase at the beginning of an etching step.

Therefore PECE was performed with constant voltages. This proofed to be an appropriate approach for preparing porous layers with sub-layers having a constant degree of porosity. The experimental results could be interpreted in terms of fractal growth like it is the case for dielectric breakdown in solids. The applied voltage determines the active region at the pore tips during etching and thus the resulting degree of porosity. It has also been shown that the etched porous layers can be detached from the bulk sample and by controlling the sub-layer thickness by the amount of transferred charge, porous SiC optical filters can be prepared. This makes the presented results also economically interesting because costly SiC substrates can be re-used several times for porous layer preparation.

Furthermore, the average amount of holes needed to dissolve a formula unit of SiC is influenced by the applied voltage as well as by diffusion of fresh reactants into the porous layer. The transient phase during current controlled PECE is explained by the oxide growth counteracted by its dissolution rate due to the presence of HF.

In summary it could be shown that both, the degree of porosity and the homogeneity are controllable in a wide range in 4H-SiC when applying a photo-electrochemical approach. This paves the way for the realization of numerous novel MEMS or even NEMS device concepts exceeding the limitations given by standard silicon-based solutions.

Acknowledgments

This project has been supported by the COMET K1 centre ASSIC Austrian Smart Systems Integration Research Center. The COMET – Competence Centers for Excellent Technologies - Programme is supported by BMVIT, BMWFW and the federal provinces of Carinthia and Styria. The authors acknowledge the TU Wien University Library for financial support through its Open Access Funding Program.

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