TECHNISCHE UNIVERSITÄT WIEN

HEPHY Institute of High Energy Physics

DIPLOMARBEIT

# Development of a DAQ System for Depleted Monolithic Active Pixel Sensors

zur Erlangung des akademischen Grades

**Diplom-Ingenieur**

im Rahmen des Studiums

**Technische Physik**

eingereicht von

**Klemens Flöckner, BSc**
Matrikelnummer 01527009

ausgeführt am Institut für Hochenergiephysik der Akademie der Wissenschaften und am Atominstitut der Technischen Universität Wien

Betreuung: Assistant Prof. Dipl.-Ing Dr. Albert Hirtl
Mitwirkung: Dipl.-Ing Dr. Thomas Bergauer
Dipl.-Ing Christian Irmler

Wien, 15. August 2022

Klemens Flöckner | Albert Hirtl

# Acknowledgements

At the beginning I would like to thank my two supervisors Thomas Bergauer and Albert Hirtl, who made it possible for me to conduct the master thesis in such an exciting field of physics and who supported me on every step of the way.

I would also like to thank Patrick Sieberer, who always stood by me with a helping hand and with whom I spent countless hours at the beam experiments at MedAustron. Furthermore, I would like to thank the HEPHY team, especially Helmut Steininger, Christian Irmler, Felix Ulrich-Pur and Klaus-Dieter Fischer, who supported me during the process of my thesis. A special thanks also goes to Simon Spannagel from CERN, who always brought me back on the right track when problems arose.

Last but not least, I would like to thank my girlfriend Stefanie, who always showed great understanding for my numerous hours in the HEPHY lab, and my parents Elfriede und Sebastian, whose support enabled me to pursue my physics studies.

# Kurzfassung

Siliziumsensoren werden heute in fast allen Experimenten der Teilchenphysik eingesetzt. Da sie mit standardisierten Photolithographietechniken leicht segmentiert werden können, erreichen sie eine ausgezeichnete Ortsauflösung und spielen eine Schlüsselrolle bei der Messung von primären und sekundären Vertices und dem Tracking von geladenen Teilchen.
Bislang wurden die Sensoren von entsprechenden Front-End-Elektronikchips ausgelesen, die über Bump- oder Wire-Bonding Techniken miteinander verbunden waren, was ihre Performance aufgrund eines recht hohen Materialbudgets und komplizierter und teurer Montageverfahren einschränkt.
Nach jahrelanger Forschung und Entwicklung ermöglichen *Depleted Monolithic Active Pixel Sensors* (DMAPS), produziert mittels *Complementary Metal-Oxide-Semiconductor* (CMOS) Technologien, die Vereinigung des ladungsempfindlichen Volumens und der aktiven Ausleseelektronik in einem Bauelement.
Diese Technologie eignet sich besonders für Anwendungen, die ein geringes Materialbudget und eine hervorragende Positionsauflösung erfordern, wie sie für Leptonbeschleuniger bei zukünftigen Upgrades des Belle II-Experiments oder dem *Future Circular Collider*-ee (FCC-ee) benötigt werden. Um den Anforderungen von Hadronenbeschleunigerexperimenten wie dem high luminosity *Large Hadron Collider* (LHC) oder dem FCC-hh gerecht zu werden, sind jedoch weitere signifikante Verbesserungen bezüglich der Strahlenhärte erforderlich.
Um die Technologie in diesem vielversprechenden Bereich weiter voranzutreiben, werden DMAPS im Rahmen der RD50-Kollaboration unter Verwendung des LFoundry 150 nm CMOS-Prozesses am Institut für Hochenergiephysik entwickelt. Im Rahmen dieser Arbeit habe ich den zweiten Prototyp RD50-MPW2 charakterisiert und analysiert. Die aktive Matrix dieses Chips besteht aus 8×8 Pixeln, die jedoch aufgrund des analogen Frontends nur nacheinander ausgelesen werden können. Ich habe die *Data Acquisition* (DAQ) für den Betrieb und das Auslesen dieses Detektors realisiert, indem ich den Chip in ein Hardware- und ein Software-Framework, namens *Control and Readout Inner Tracking Board* (CaRIBOu) bzw. Peary, eingebettet habe. Das CaRIBOu-Framework wird im Stand-alone-Betrieb mit einer radioaktiven $^{90}$Sr Quelle im Labor und auch in einem Protonenstrahl am MedAustron-Synchrotron, eingebettet in eine EUDAQ2-Umgebung, verwendet und getestet. Im Rahmen dieser Messungen habe ich die allgemeine Performance des Chips bestimmt und einen unbestrahlten Chip mit Chips verglichen, die bis zu einer 1 MeV Neutronen-äquivalenten Fluenz von $10^{14}$ $n_{\mathrm{eq}}/\mathrm{cm}^2$ bestrahlt wurden.

# Abstract

Silicon sensors are used today in almost all experiments in particle physics. Since they can be easily segmented using standard photo-lithographic techniques, they can achieve excellent position resolution and play a key role in measuring primary and secondary vertices and tracking of charged particles.
Up to now, the sensors were read out by dedicated front-end electronic chips connected via bump- or wire-bonding techniques, which is limiting their performance because of a rather high material budget and complicated and expensive assembling procedures.
After years of research and development, *Depleted Monolithic Active Pixel Sensors* (DMAPS) manufactured by *Complementary Metal-Oxide-Semiconductor* (CMOS) technologies now allow a combination of the charge-sensitive volume and the active readout electronics into one device.
This technology is particularly suitable for applications that require low material budget and excellent position resolution, such as those required for electron machines such as Belle II upgrades or the *Future Circular Collider*-ee (FCC-ee). However, more significant improvements in their radiation tolerance are needed to meet the needs of hadron accelerator experiments such as the high luminosity *Large Hadron Collider* (LHC) or the FCC-hh.
In order to further push the technology in this promising field, DMAPS are being developed within the RD50 collaboration using the LFoundry 150 nm CMOS process. Within this thesis I characterized and studied the second prototype RD50-MPW2. The active matrix of this chip consists of 8×8 pixels, but the pixels can only be read out one after another due to the analog front end. I established the *Data Acquisition* (DAQ) system to operate and read out this detector by embedding the chip in a hardware and software framework, called *Control and Readout Inner Tracking Board* (CaRIBOu) and Peary, respectively. The CaRIBOu framework is used and tested in stand-alone operation with a radioactive $^{90}$Sr source in the laboratory and also in a proton beam at the MedAustron synchrotron embedded into an EUDAQ2 environment. Within these measurements, I determined the general performance of the chip and compared an unirradiated chip with chips irradiated up to a 1 MeV neutron-equivalent fluence of $10^{14}$ $n_{\mathrm{eq}}/\mathrm{cm}^2$.

# Contents

CHAPTER 1

# Introduction

Currently, hybrid pixel detectors (figure 1.1) are state-of-the-art in *High Energy Physics* (HEP) experiments. They consist of multiple pixel sensors, each connected with a technique called bump-bonding to an electric read-out layer. Due to the high complexity, the technology is potentially error-prone and thus expensive to keep the yield at an acceptable high level, as there is virtually no possibility of reworking failed bumps. The two required layers also result in a high material budget which has a negative impact on the tracking performance [1].

A promising alternative are *Depleted Monolithic Active Pixel Sensors* (DMAPS), realized

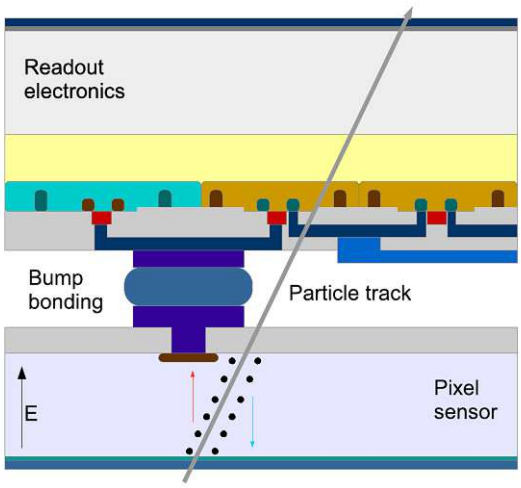



Figure 1.1: Cross-section of a hybrid-pixel detector with a pixel sensor layer connected via bump bonding with the readout electronic layer [1].

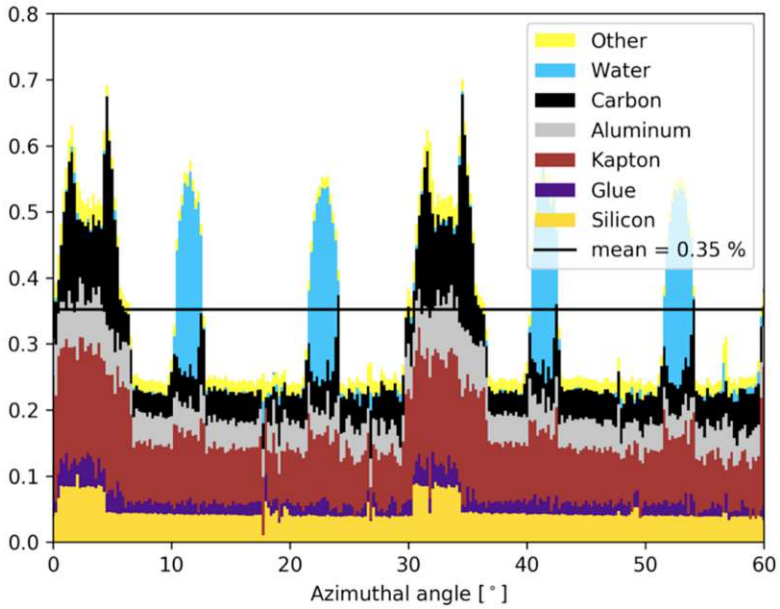



Figure 1.2: Angular distribution of the material budget of the ITS 2 [3].

with *High-Voltage* (HV) CMOS and/or *High Resistivity* (HR) CMOS processes. With this technology, particle detection and signal processing is performed in the same silicon substrate, which results in a lower material budget. For example at the FCC-ee, for the innermost vertex layers a material budget of about 0.2 % $X_0$ is aimed for [2]. This should be feasible when looking at the material budget of the *Inner Tracking System* 2 (ITS2) realized with another DMAPS named *ALice PIxel DEtector* (ALPIDE) in *A Large Ion Collider Experiment* (ALICE) experiment (figure 1.2). By thinning, a detector thickness of 50 µm is achieved, resulting in a material budget for the silicon of about 0.05 % $X_0$. The remaining material budget results from additional support structure. In the future ITS3 update the detector thickness should be further reduced to 20-40 µm [3].

Since CMOS technology is used in the commercial chip industry, this results in faster and more cost-efficient production. DMAPS offer the possibility to be operated by HV and to be used with HR to increase the radiation hardness required for fluences expected at future applications like the FCC [1].

This kind of detector is being developed within the RD50 collaboration [4]. A first prototype RD50-MPW1 was developed, but it had problems with high leakage current and with the readout of the chip via a digital front end [1]. To get the problems under control, a second prototype RD50-MPW2 (figure 1.3) was developed, where the digital readout part was omitted and the full concentration was put on the analog readout. Regarding the large leakage current, the layout design was adapted. The RD50-MPW2 chip [5] has an active pixel matrix with $8 \times 8$ pixels, where the pixels can only be read

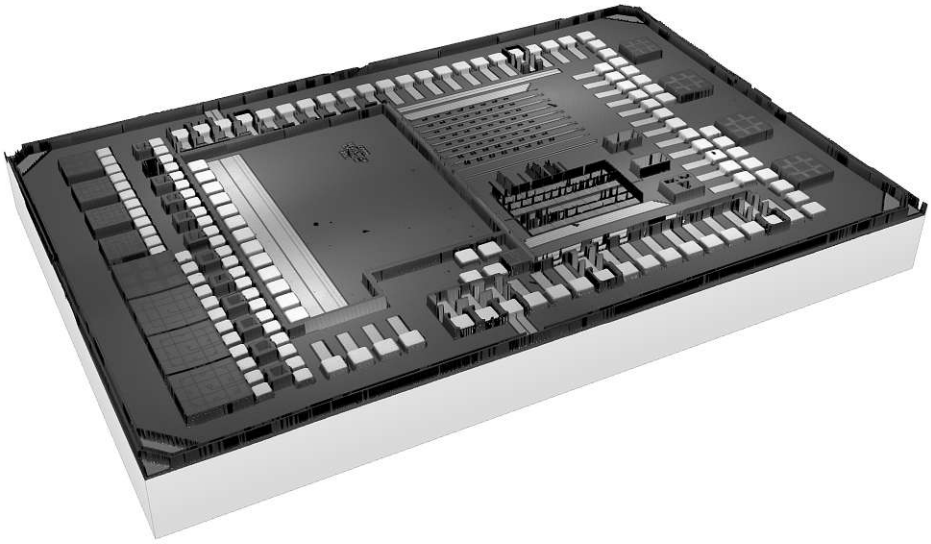


Figure 1.3: 3D representation of the MPW2 chip

out one after the other. The chip also contains further test structures, which are not analyzed in the course of this thesis.

With conventional *Data Acquisition* (DAQ) systems, the implementation of a new detector has always been associated with significant effort of cost and time. Therefore, the modular hardware and software DAQ framework called CaRIBOu will be used to control the RD50-MPW2 chip. The CaRIBOu hardware of the DAQ framework consists of an evaluation board, a *Control and Readout* (CaR) board, and a chipboard on which the chip under analysis is mounted. The CaRIBOu software Peary allows a fast, standardized implementation of the detector and can be used in combination with a superior DAQ system like EUDAQ2.

With the help of this system, the chip will be tested and characterized in the laboratory and in a proton beam at the MedAustron particle accelerator. Before that, however, the theoretical basics of particle detection and of DAQ systems will be presented.

CHAPTER 2

# Silicon Particle Detector Principle

Silicon detectors play a major role in *High Energy Physics* (HEP)-experiments. Thanks to the high granularity of silicon detectors, they can be operated at high particle rates even with a thin design, which has a positive effect on the material budget. Also the semiconductor industry has a lot of experience in this field due to microchip technology, which has a favorable effect on quality and price performance for silicon detectors. In this chapter, the basic concept of energy loss of particles when interacting with matter is described. Then, semiconductor physics for the detection of particles on the basis of silicon is explained and finally how a signal is generated.

## 2.1 Particle Interaction

Any radiation detection depends on the interaction between radiation and matter. Particles entering the medium exchange energy. Basically, there are three types of particles: photons, charged particles and uncharged particles. Since only charged particles and photons will appear in this work, the latter will not be discussed in this chapter.

### 2.1.1 Interaction of Charged Particles with Matter

Charged particles traversing through matter lead to kinetic loss of energy. If the energy is high enough the process takes place through the ionization of the atom. At lower energies, excitation of the bound electrons is more probable. This leads to low-energy photons, which help in the detection of the particle. The charged particles can also penetrate through the electron hull and interact with the nucleus which leads to Bremstrahlung.

#### Energy Loss through Ionization

The ionization of an atom is more likely for heavy charged particles (protons, $\mu^{\pm}$, $\pi^{\pm}$, $\alpha$-particles, ...). Classically the mean energy loss per distance was already described

| | | | |
|---|---|---|---|
| $N_A$ | Avogadro's number | $v$ | speed of projectile |
| $r_e$ | classic electron radius | $\beta = \frac{v}{c}$ | relativistic speed of projectile |
| $m_e$ | electron mass | $\gamma = \frac{1}{\sqrt{1-\beta^2}}$ | Lorentz factor radius |
| $c$ | speed of light | $\delta(\beta\gamma)$ | density effect correction |
| $z$ | charge number of projectiles | $W_{max}$ | maximum energy transfer |
| $Z$ | atomic number of absorber | $I$ | mean excitation potential |
| $A$ | mass number of absorber | | |

Table 2.1: Variables used in the Bethe-Bloch equation (2.1).

by Bohr in 1913. Bethe and Bloch provided a quantum mechanic solution, leading to the Bethe-Bloch equation, describing the mean energy loss per unit path length by moderately relativistic heavy particles [6]

$$\left\langle -\frac{dE}{dx} \right\rangle = 4\pi N_A r_e^2 m_e c^2 z^2 \frac{Z}{A}\frac{1}{\beta^2}\left[\frac{1}{2}\ln\left(\frac{2m_e c^2\beta^2\gamma^2 W_{max}}{I^2}\right) - \beta^2 - \frac{\delta(\beta\gamma)}{2}\right], \tag{2.1}$$

valid in the energy range of $0.1 \lesssim \beta\gamma \lesssim 1000$ and absorber materials with intermediate Z-values. The variables used in this equation are listed in the following table (2.1). The unit of the stopping power $\langle -dE/dx \rangle$ is $\mathrm{MeVg^{-1}cm^2}$. $W_{max}$ describes the maximum energy transfer at a head-on single collision and $I$ is the mean ionization excitation potential of the absorber.
Figure 2.1 shows the energy dependence of $\langle -dE/dx \rangle$ of an incoming particle ($\pi^{\pm}$). At low energies, the $\ln(\beta\gamma)$ term is negligible, so the stopping power is proportional to $1/\beta^2$. At high energies, the $\ln(\beta\gamma)$ term is dominant instead. In this range, the density correction flattens the curve which originates from the polarization shield effects caused by the charged particles. For energies $\beta\gamma > 1000$, radioactive losses dominate the stopping power and for energies $\beta\gamma < 0.1$, shell corrections and other mechanisms must be taken into account.
For $\beta\gamma \approx 3-4$ ($\beta \approx 0.95$) a minimum is reached. Particles in this region are called *minimum ionizing particles* (MIP) [7]. For silicon, the energy loss of MIPs is $1.66\,\mathrm{MeVg^{-1}cm^2}$ / $3.87\,\mathrm{MeVcm^{-1}}$ [8].

### Energy Loss through Bremsstrahlung

Lighter charged particles ($e^+$, $e^-$) have a greater probability to penetrate through the hull to reach the nuclear range. When the particles are decelerated in the Coulomb field of the nucleus, photons are emitted, which is called Bremstrahlung. The energy loss by radiation for $e^{\pm}$ given as follows

$$-\frac{dE}{dx} \approx 4\alpha N_A \frac{Z^2}{A} r_e^2 E \ln\left(\frac{183}{Z^{1/3}}\right), \tag{2.2}$$

is only valid if $E \gg m_e c^2/\alpha Z^{1/3}$. $\alpha = \frac{e^2}{4\pi\epsilon_0\hbar c}$ is the fine-structure constant and $r_e$ the radius of the $e^{\pm}$. The other variables can be found in the table 2.1. With this equation

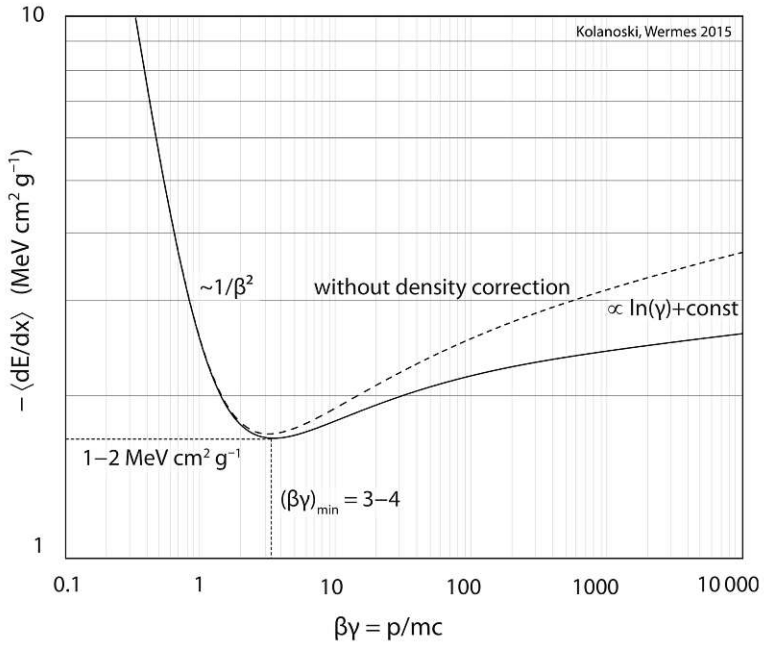



Figure 2.1: Mean energy loss of pions by ionization in silicon as a function of $\beta\gamma = p/mc$ with and without density correction [7].

(2.2) the radiation length $X_0$ can be defined as follows

$$-\frac{dE}{dx} = \frac{E}{X_0} \rightarrow X_0 = \frac{A}{4\alpha N_\mathrm{A} Z^2 r_\mathrm{e}^2 \ln(183 Z^{-1/3})}. \tag{2.3}$$

$X_0$ is the distance, where the energy of the $e^-$ is reduced by a factor of $1/e$, compared to its original energy [8].
The total energy loss of $e^\pm$ is composed of two parts

$$\left(\frac{dE}{dx}\right)_\mathrm{tot} = \left(\frac{dE}{dx}\right)_\mathrm{rad} + \left(\frac{dE}{dx}\right)_\mathrm{coll}. \tag{2.4}$$

The critical energy $E_\mathrm{c}$ can be defined where energy loss through ionization and radiation are in balance: (figure 2.2)

$$E_\mathrm{c} = \left(\frac{dE}{dx}\right)_\mathrm{rad} = \left(\frac{dE}{dx}\right)_\mathrm{coll} \tag{2.5}$$

For electrons in silicon, $E_\mathrm{c} = 40.19\,\mathrm{MeV}$. At lower energies, ionization dominates, while at energies higher than $E_\mathrm{c}$, radiation takes over [7].

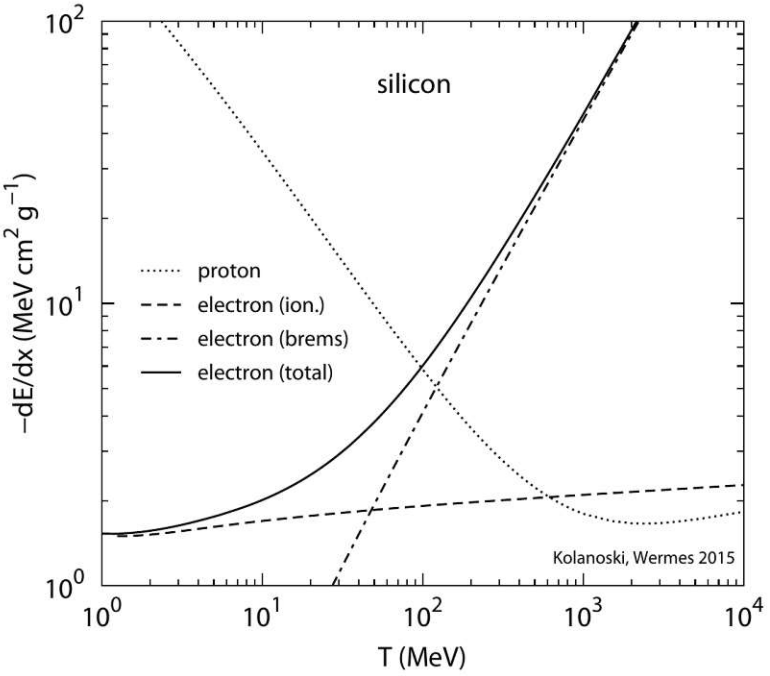



Figure 2.2: Energy loss of electrons in silicon by ionization and by radiation as a function of the kinetic energy. The intersection where the the energy loss by ionization and by radiation are the same is specified as critical energy $E_c$ [7].

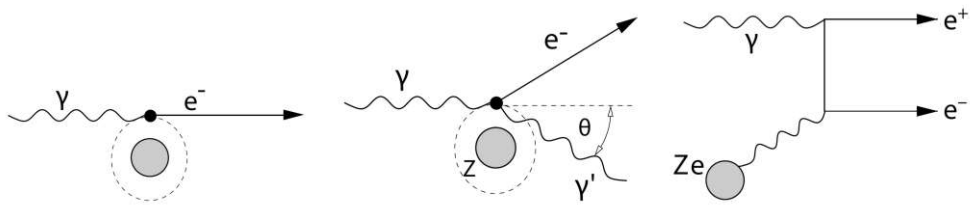
### 2.1.2 Interaction of Photons with Matter

The interaction of photons with matter is completely different to the interaction of charged particles. The energy is not emitted continuously, but the photon is either completely absorbed or scattered by a large angle.

#### Interaction Mechanisms

The probability of an interaction between an projectile and an absorber is proportional to the cross-section of the interaction. For the detection of photons, three processes are of crucial importance.

- Photoelectric effect (*absorption*)
  The energy of the photon is completely absorbed by the atom, which in return emits an inner shell electron with the energy $E_{e^-} = h\nu - E_b$, where $h$ is the Planck's constant, $\nu$ the frequency of the photon and $E_b$ the binding energy of the photon. (figure 2.3a) The photoelectric effect is predominant in the lower energy range ($100\,\text{keV} \geq E_\gamma \geq E_{ion}$).
- Compton effect (*scattering*)
  The photon is deflected by an outer shell electron, changes the direction by angle $\theta$




(a) Photoelectric effect (b) Compton effect (c) Pair production

Figure 2.3: Three fundamental interaction mechanisms of photons with matter [7].

and loses energy. The energy of the deflected photon depends on the scattering angle $\theta$. This effect occurs mainly in the medium energy range $E_\gamma \approx 1\,\text{MeV}$.

- Pair production (*absorption*)
  If the energy is high enough, the photon interacts with the Coulomb field of the nucleus and it is converted into an electron-positron pair. This requires at least twice the rest energy of an electron $E_\gamma > 1.022\,\text{MeV}$. Therefore, this effect is only present at high energies ($E_\gamma \gg 1\,\text{MeV}$).

Thus, depending on the energy, a different mechanism is dominant, as can be seen in figure 2.4a. At the border between photoelectric effect and Compton scattering as well as between Compton scattering and pair formation the respective cross-sections are exactly equal. ($\sigma_{\text{photo}} = \sigma_{\text{compt}}$ and $\sigma_{\text{compt}} = \sigma_{\text{pair}}$) In addition, there is a strong dependence on the atomic number. With increasing Z, the photoelectric effect and pair production dominate in comparison to Compton scattering [8]. In figure 2.4b, the total absorption coefficient and the division among the respective mechanisms for a silicon layer are shown. With a higher atomic number (see *Total CdTe*), the overall probability of absorption also increases, which is desirable at particle detection.

### Photon Attenuation

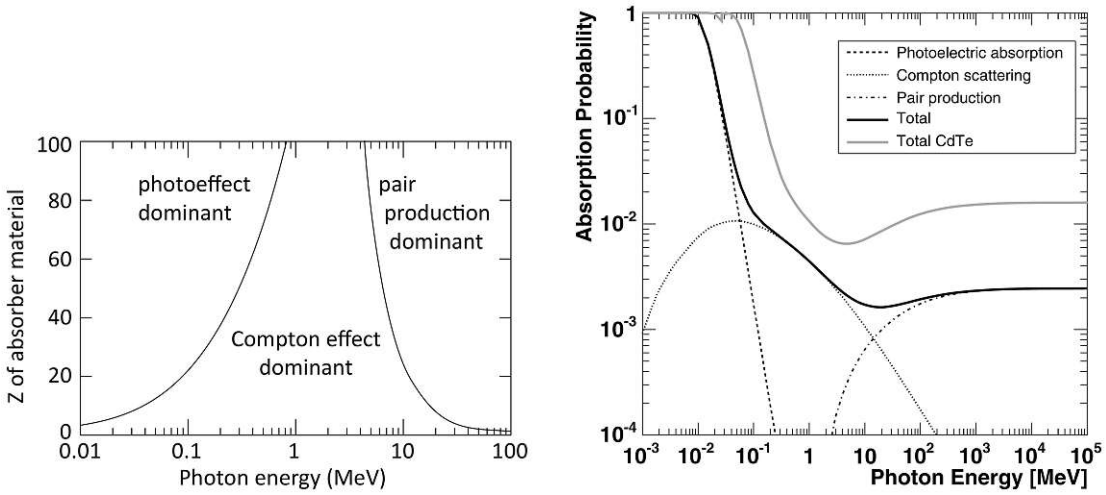
The interaction of photons with the absorber (*absorption* and *scattering*) is a statistical process. The attenuation of the initial photon beam $I_0$ takes place exponentially

$$I = I_0 \mathrm{e}^{-\mu x}, \tag{2.6}$$

where $\mu$ is the *mass attenuation coefficient* with the unit $\text{cm}^2/\text{g}$. It is directly related to the cross-section as follows

$$\mu = \frac{N_\text{A}}{A} \sum_i \sigma_i, \tag{2.7}$$

with $\sigma_i$ representing the different cross-sections of the photon mechanisms (2.1.2), Avogadro's number $N_\text{A}$ and atomic weight $A$. So there is a strong dependence of the *mass attenuation coefficient* on the energy [8].




(a) Regions of different cross-sections as a function of the atomic number $Z$ of the absorber material and the photon energy [7].

(b) Absorption probability for the different photon interaction mechanisms for 300 $\mu$m silicon as a function of the photon energy [9].

Figure 2.4: Behavior of cross-section for the three photon interaction mechanisms in dependence of the photon energy $E_\gamma$

## 2.2 Semiconductor Physics

For the detection of particles, the semiconductor silicon is particularly suitable. The high density causes a large energy loss within a short distance of the semiconductor material. In addition, silicon has a low ionization energy compared to other detection methods.

### 2.2.1 Bond Model of Semiconductors

In the solid state, silicon forms a diamond lattice structure. Since it is located in the 4th main group of the periodic table, the outer shell electrons build covalent bonds with the 4 closest neighbors. The dense, periodic alignment of the semiconductor atoms leads to discrete energy levels. When these levels are energetically densely packed, they form a continuum, a so-called *energy band*. The energy band with the highest energy forms the *Valence Band* (VB), separated by a *band gap* $E_g = E_c - E_v$ with the next higher energy, the *Conduction Band* (CB). Depending on the occupation of the *energy bands*, which depends on the position of the energy level, charge carriers can be more or less mobile. The following 3 cases can be distinguished [7]:

- Insulators:
  The VB is completely packed, while the CB is not filled at all. A typical energy gap of an insulator is $E_g \approx 9\,\text{eV}$. The transition of electrons from the VB to the CB is very rare, so there is no current flow (figure 2.5a).

- Semiconductor:
  Weaker bonds between atoms lead to a smaller band gap, e.g. for silicon $E_g = 1.12\,\text{eV}$. This allows the transition of electrons from the VB to the CB with the help of thermal excitation or an external electric field. The remaining free holes in the VB and the free electrons in the CB can be treated as free particles and therefore contribute to the current flow under the influence of an electric field (figure 2.5b).

- Conductors:
  The CB is either only partially filled or the VB and the CB overlap. In both cases, the charge carriers are free to move. Thus, current flow occurs with minimal energy input (figure 2.5c & figure 2.5d).

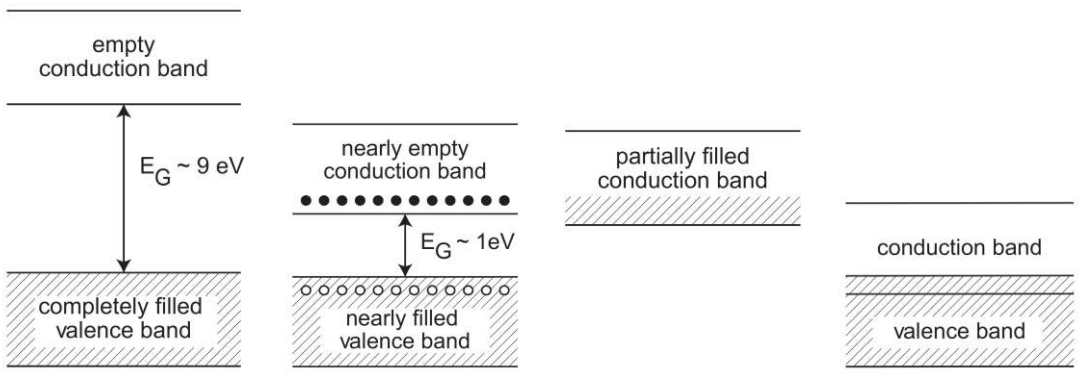
In the following, the intrinsic *charge carrier concentration* $n(E)$ in thermal equilibrium is derived according to the reference [7]. The charge carrier concentration in an infinitesimally small energy range

$$n(E)dE = Z(E)f(E)dE, \tag{2.8}$$

depends on the density of states $Z(E)$ and its occupation probability $f(E)$.
$Z(E)$ is the number of electrons and holes that can be occupied in the respective band. Normalizing and applying the non-relativistic energy-momentum relation $E = p^2/(2m)$ provides the following term

$$Z(E)dE = 4\pi \left(\frac{2m^*}{h^2}\right)^{3/2} \sqrt{E}\, dE, \tag{2.9}$$

where $m^*$ is the effective mass and $h$ the Planck's constant. Considering the regions where no energy levels are present, the following density of states is obtained for the VB




(a) Insulator (b) Semiconductor (c) Conductors: partially filled CB (d) Conductors: overlap of VB and CB.

Figure 2.5: Different types of energy band structures [7].

and the CB

$$Z(E)dE = 4\pi \left(\frac{2m_{\mathrm{e}}^*}{h^2}\right)^{3/2} \sqrt{E - E_{\mathrm{c}}}\, \Theta(E - E_{\mathrm{c}})\, dE \tag{2.10}$$

$$Z(E)dE = 4\pi \left(\frac{2m_{\mathrm{h}}^*}{h^2}\right)^{3/2} \sqrt{E_{\mathrm{v}} - E}\, \Theta(E_{\mathrm{v}} - E)\, dE, \tag{2.11}$$

where $m_{\mathrm{e}}^*$ and $m_{\mathrm{h}}^*$ is the effective mass of the electron and the hole. $E_{\mathrm{v}}$ is the upper band edge of the VB and $E_{\mathrm{c}}$ is the lower band edge of the CB.
The occupation probability for the electrons $f_{\mathrm{e}}(E)$ and the holes $f_{\mathrm{h}}(E)$ is described by the Fermi-Dirac distribution

$$f_{\mathrm{e}}(E) = \frac{1}{\mathrm{e}^{\frac{E-E_{\mathrm{f}}}{k_{\mathrm{B}}T}} + 1} \tag{2.12}$$

$$f_{\mathrm{h}}(E) = \frac{1}{\mathrm{e}^{\frac{E_{\mathrm{f}}-E}{k_{\mathrm{B}}T}} + 1}, \tag{2.13}$$

where $k_{\mathrm{B}}$ is the Boltzmann constant, $T$ is the absolute temperature and $E_{\mathrm{f}}$ is the Fermi energy. The Fermi energy is approximately in the middle of the band gap for undoped semiconductors resulting in $E_{\mathrm{f}} \approx \frac{E_{\mathrm{c}}-E_{\mathrm{v}}}{2}$. Assuming that $(E - E_{\mathrm{f}}) \gg k_{\mathrm{B}}T$ and $f_{\mathrm{e}}(E) + f_{\mathrm{h}}(E)$ the following approximation can be made

$$f_{\mathrm{e}}(E) \approx \mathrm{e}^{-\frac{E-E_{\mathrm{f}}}{k_{\mathrm{B}}T}} \tag{2.14}$$

$$f_{\mathrm{h}}(E) \approx \mathrm{e}^{-\frac{E_{\mathrm{f}}-E}{k_{\mathrm{B}}T}} \tag{2.15}$$

Multiplying the occupation probabilities from equation (2.14) and equation (2.15) with the density of states from equation (2.10) and equation (2.11) according to equation (2.8) and integrating over the energy provides the respective charge carrier densities

$$n_{\mathrm{e}} = 2\left(\frac{2m_{\mathrm{e}}^* k_{\mathrm{B}}T}{2\pi\hbar^2}\right)^{3/2} \mathrm{e}^{-\frac{E-E_{\mathrm{f}}}{k_{\mathrm{B}}T}} = N_{\mathrm{c}}\, \mathrm{e}^{-\frac{E-E_{\mathrm{f}}}{k_{\mathrm{B}}T}} \tag{2.16}$$

$$n_{\mathrm{h}} = 2\left(\frac{2m_{\mathrm{h}}^* k_{\mathrm{B}}T}{2\pi\hbar^2}\right)^{3/2} \mathrm{e}^{-\frac{E_{\mathrm{f}}-E}{k_{\mathrm{B}}T}} = N_{\mathrm{v}}\, \mathrm{e}^{-\frac{E_{\mathrm{f}}-E}{k_{\mathrm{B}}T}} \tag{2.17}$$

with the effective densities $N_{\mathrm{c}} = 2\left(\frac{2m_{\mathrm{e}}^* k_{\mathrm{B}}T}{2\pi\hbar^2}\right)^{3/2}$ and $N_{\mathrm{v}} = 2\left(\frac{2m_{\mathrm{h}} p^* k_{\mathrm{B}}T}{2\pi\hbar^2}\right)^{3/2}$.
Multiplying the two densities results in the final charge carrier concentration

$$n_i^2 = n_{\mathrm{e}}\, n_{\mathrm{h}} = N_{\mathrm{c}}\, N_{\mathrm{v}}\, \mathrm{e}^{-\frac{E_{\mathrm{c}}-E_{\mathrm{v}}}{k_{\mathrm{B}}T}} = N_{\mathrm{c}}\, N_{\mathrm{v}}\, \mathrm{e}^{-\frac{E_{\mathrm{g}}}{k_{\mathrm{B}}T}}, \tag{2.18}$$

which strongly depends on the temperature

$$n_i \propto T^{3/2} \mathrm{e}^{-\frac{E_{\mathrm{g}}}{k_{\mathrm{B}}T}}. \tag{2.19}$$

For silicon, an intrinsic charge carrier density of $n_i|_{\text{silicon}} \approx 1.01 \cdot 10^{10}\,\text{cm}^{-3}$ is obtained [7].
A measure of the purity of silicon is the *specific resistivity* [8]

$$\rho = \frac{1}{e(n_\text{e}\mu_\text{e} + n_\text{h}\mu_\text{h})}. \tag{2.20}$$

With electron mobility $\mu_\text{e}|_{\text{silicon}} = 1450\,\text{cm}^2\text{s}^{-1}\text{V}^{-1}$, hole mobility $\mu_\text{h}|_{\text{silicon}} = 500\,\text{cm}^2\text{s}^{-1}\text{V}^{-1}$, elementary charge $e = 1.602 \cdot 10^{-19}\,\text{C}$ and $n_\text{e} = n_\text{h} \approx n_i|_{\text{silicon}}$ a specific resistivity of $\rho \approx 320\,\text{k}\Omega\,\text{cm}$ is obtained [7].

**Small estimation for detector construction:**
The average ionization energy for the generation of an e/h pair is $I_0 = 3.65\,\text{eV}$ [7]. The average energy loss per path length for silicon is $dE/dx = 3.87\,\text{MeVcm}^{-1}$ (see section 2.1.1). A detector is assumed with the typical area of $A = 1\,\text{cm}^2$ and a thickness of $d = 300\,\mu\text{m}$.
The number of $e^-h^+$-pairs created through a *minimum ionizing particle* in such an environment

$$\frac{dE/dx \cdot d}{I_0} \approx 3.2 \cdot 10^4 \tag{2.21}$$

representing the signal, is much lower than the number of intrinsic charge carriers in the same volume

$$n_i\, A\, d \approx 3.03 \cdot 10^8 \tag{2.22}$$

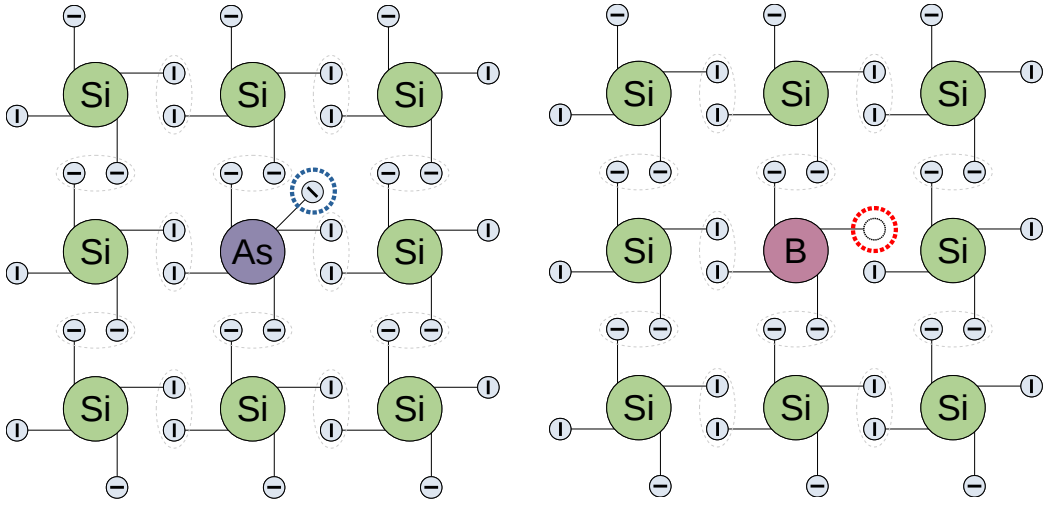
representing the noise in the detector. To improve the *Signal-to-Noise-Ratio* (SNR), either the signal must become larger, or the noise smaller. Since there is only a limited number of ionizing particles, the number of intrinsic carriers has to be decreased. This can be accomplished by a reverse biased pn-junction establishing a depletion zone, which will be explained in the next section.

### 2.2.2 PN-Junction

The insertion of atoms with a slightly different number of valence electrons than the initial substrate (*doping*), changes the conduction property of the semiconductor.

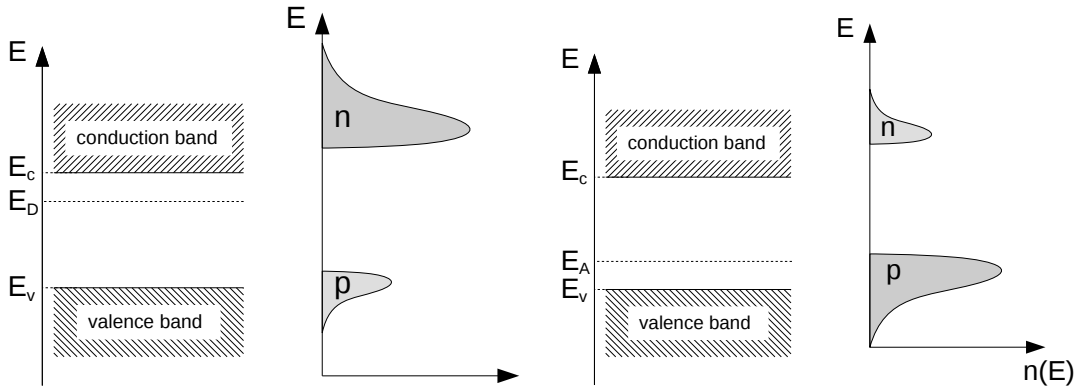
**n-Doping**:
Introducing pentavalent arsenic (figure 2.6a) with one more valence electron than silicon (*donors*) leads to an additional energy band $E_\text{d}$, just below the CB. (figure 2.7a) The donors can now enter the CB without a large barrier, which increases the occupation probability of the electrons (*majority carriers*) in the CB. (figure 2.7b) This way, also the Fermi-Energy is shifted towards the CB.

**p-Doping**:
Incorporation of trivalent boron (2.6b) with one less valence electron than silicon (*acceptors*) results in an additional energy band $E_\text{a}$ just above the VB. (figure 2.7c) The




(a) n-doped silicon (b) p-doped silicon

Figure 2.6: Representation of the electron bonds in doped silicon.

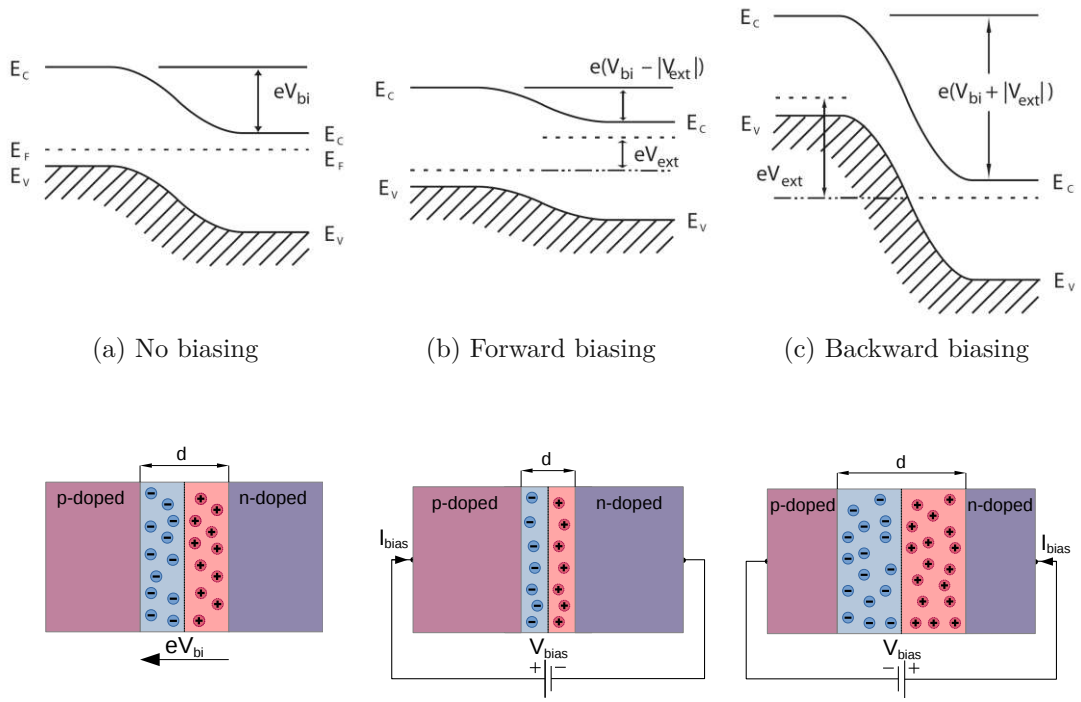



(a) Energy band with additional donor-level (b) Distribution of the electrons in the CB and holes in the VB (c) Energy band with additional acceptor-level (d) Distribution of the electrons in the CB and holes in the VB

Figure 2.7: Influence of n-doping (figure a & b) and p-doping (figure c & d) on the band-model.

acceptors can easily switch to the VB, enhancing the occupation probability of the holes (*majority carriers*) in the VB. (figure 2.7d). Therefore, the Fermi-Energy moves near the VB.

By joining together these two regions a pn-junction is formed. The gradient of electrons and holes leads to a diffusion current $I_{\text{diff}}$ in which the majority carriers of the given




(a) No biasing (b) Forward biasing (c) Backward biasing

(d) No biasing (e) Forward biasing (f) Backward biasing

Figure 2.8: Band model (a - c) [7] and visualization of the space charge region (d - e) of a pn-junction with a different kind of biasing.

doped material diffuse into the respective other material and recombine there. This creates a zone that is free of charge carriers (*depletion zone*). The donors and acceptors at the border of the zone generate an intrinsic electric field that prevents the diffusion of further majority carriers. The electric field generates a current $I_{\text{drift}}$, which flows in the opposite direction of $I_{\text{diff}}$. While the Fermi energy remains the same, the energy levels $E_{\text{C}}$ and $E_{\text{V}}$ are shifted downward during the transition from p- to n-doped part. (figure 2.8a) The electric field is described by the *built-in voltage*

$$V_{\text{bi}} = \frac{k_{\text{B}}T}{e} \ln\left(\frac{N_{\text{A}}N_{\text{D}}}{n_i^2}\right) \tag{2.23}$$

, where $N_{\text{A}}$ is the doping concentration of the acceptors in the p-doped material and $N_{\text{D}}$ the doping concentration of the donors in the n-doped part. For silicon, this is about 0.4 - 0.8 V.

By applying an external voltage $V_{\text{ext}}$, the width of the depletion zone can be modified. At *forward biasing* (figure 2.8b & 2.8e) the electric field is reduced by $V_{\text{ext}}$ and therefore also the depletion zone becomes narrower. With *backward biasing* (figure 2.8c & 2.8f), the electric field is increased and with this also the depleted area becomes larger. A semiconductor detector is operated this way to get a depletion zone as large as possible.

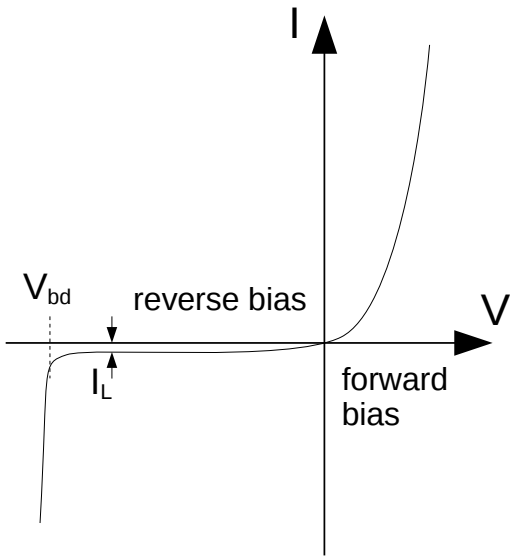



Figure 2.9: I-V curve of a pn-junction (diode) in forward and reverse biasing. $I_{\mathrm{L}}$ is the leakage current and $V_{\mathrm{bd}}$ specifies the breakdown voltage.

The width of the depletion zone (figure 2.8d & 2.8e & 2.8f) for the respective doped material (donors/acceptors) is given by

$$d_{\mathrm{D/A}} \approx \sqrt{\frac{2\epsilon_0\epsilon_{\mathrm{r}}}{eN_{\mathrm{D/A}}}\left(V_{\mathrm{bi}}+V_{\mathrm{ext}}\right)} = \sqrt{2\epsilon_0\epsilon_{\mathrm{r}}\mu_{\mathrm{e/h}}\rho\left(V_{\mathrm{bi}}+V_{\mathrm{ext}}\right)}. \tag{2.24}$$

where $\epsilon_0$ is the vacuum permittivity, $\epsilon_{\mathrm{r}}$ the relative permittivity and $\rho \simeq 1/(e\,\mu_{\mathrm{e/h}}N_{\mathrm{D/A}})$ is the resistivity of the wafer. Here it was assumed that one doping concentration is much higher than the other one ($N_{\mathrm{A}} \gg N_{\mathrm{D}}$ or $N_{\mathrm{D}} \gg N_{\mathrm{A}}$), which is usually the case [7].

**Current-voltage characteristics**:
In forward biasing the current exponentially depends on the external voltage applied

$$I = I_{\mathrm{S}}\left(\mathrm{e}^{\frac{eV_{\mathrm{ext}}}{k_{\mathrm{B}}T}} - 1\right), \tag{2.25}$$

with the reverse saturation current $I_{\mathrm{S}}$. This current caused by the diffusion of free carriers is also present in the *leakage current* $I_{\mathrm{L}}$ (figure 2.9), occurring at a reverse biased pn-junction. However, the thermal generation of electron-hole pairs in the depletion zone accounts for the majority of the leakage current.

The generation current is

$$I_{\mathrm{gen}} = eAd\frac{n_i}{\tau_{\mathrm{g}}}, \tag{2.26}$$

where $A$ is the cross-sectional area of the pn-junction, $d$ the width of the depletion zone (2.24) and $\tau_g$ the charge carrier generation lifetime. The temperature dependence

$$I_{gen} \propto T^2 e^{-\frac{E_a}{2k_B T}} \tag{2.27}$$

of the leakage current arises from the charge density concentration $n \propto T^2$ from equation (2.19) and $\tau_g \propto T^{-1/2}$. $E_a$ is the activation energy [7]. With increasing reverse voltage, the leakage current remains more or less the same, until the the breakdown voltage $V_{bd}$ is reached where the depletion zone collapses and a higher current begins to flow due to the avalanche breakdown [9].
Since charge only generated in depleted regions can be detected, it is desirable to deplete the detector over the whole thickness. This point is reached with the *full depletion voltage* $V_{depl}$. This voltage could be determined by measuring the I-V curve, since after complete depletion the current $I_{gen}$ of the full volume no longer increases. However, this transition is difficult to measure, which is why $V_{depl}$ is determined via a CV-measurement. The capacity, depending on the voltage is given as follows

$$C(V) = \frac{\epsilon_0 \epsilon_r}{d_{D/A}(V)} \begin{cases} \sqrt{\frac{\epsilon_0 \epsilon_r}{2\mu_{e/h}\rho V}} \cdot A & for\ V < V_{depl}, \\ \frac{\epsilon_0 \epsilon_r}{d_{max}} \cdot A & for\ V > V_{depl}, \end{cases} \tag{2.28}$$

where the thickness $d_{D/A}(V)$ from equation (2.24) is taken with the assumption that $V_{ext} \gg V_{bi}$ and $d_{max}$ is the width of the fully depleted detector.
$V_{depl}$ can be determined effectively by plotting $1/C^2(V)$ (figure 2.10) This requires a linear line to be drawn for $V < V_{depl}$ and $V > V_{depl}$. The point of intersection gives exactly the full depletion voltage [9].

### 2.2.3 Signal Generation

Part of the energy lost by a charged particle or a photon (see section 2.1) in the bulk of a semiconductor detector (figure 2.11) is used to produce an electron-hole pair. As soon as the incoming particle enters the medium, the carriers drift towards the respective electrodes due to the electric field $E$ present between the two plates. The drift velocity [7]

$$v = \mu(E)E \tag{2.29}$$

depends on the magnitude of the electric field $E$ and the mobility $\mu$ of the respective charge carrier, which itself depends on the energy. The drift velocity for electrons is much higher than for holes because of the different mobilities (see section 2.2.1). The movement of a charge e (electron or hole) with the velocity $\vec{v}$ in an electric *weighting field* $\vec{E}_w$ induces an instantaneous current

$$i = e\vec{E}_w\vec{v} \tag{2.30}$$

on the respective electrode of the detector. The weighting field differs from the field causing the drift of the carriers in the first place. To obtain $\vec{E}_w$ the electrode to which

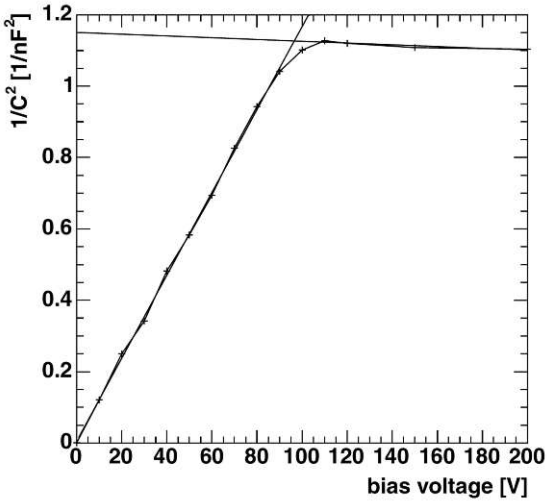



Figure 2.10: C-V curve of a pn-junction for detection of $V_{\text{depl}}$, which is located at the intersection of the linear fits [9].

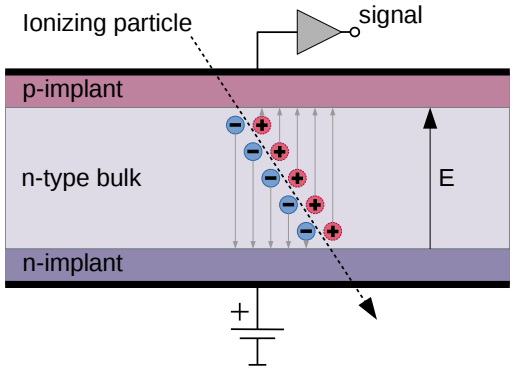



Figure 2.11: A traversing particle at a simple single pad semiconductor detector creating electron-hole pairs.

the particles drift must be set to unit potential and all others to zero potential. The charge induced to the electrode is obtained by integrating the current over time resulting in

$$Q = \int_{t_1}^{t_2} i(t)\, dt = e\, [\phi_{\text{w}}(\vec{x}_1) - \phi_{\text{w}}(\vec{x}_2)], \tag{2.31}$$

where $\phi_{\text{w}}(\vec{x}_1)$ and $\phi_{\text{w}}(\vec{x}_2)$ is the *weighting potential* at the start and end point of the carrier trajectory. This potential can be obtained with the same conditions as described before by solving the Poisson equation [9].

CHAPTER 3

# Silicon Pixel Detectors

The most simple silicon sensor is a *single pad detector* as described in section 2.2.3. It is often used at prototypes to test the basic behavior of the detector. Since there is no information about the location of the incoming particle, this is not very useful in actual applications. Adding one dimension leads to the *strip detector*. Every strip needs its readout electronic which is placed at the edge of the strip. So for $N$-strips, $N$-readout channels are required. To obtain a 2-dimensional spatial resolution, two strip detectors are placed on top of each other, with one rotated relative to the other one, called *Double Sided Strip Detector* (DSSD). Drawbacks of this type of detectors are ghost hits, which occur when two particles hit the detector at the same time or shortly after each other. Since 4 strips are activated at the same time, it is no longer possible to clearly distinguish where exactly the particles arrived. So another, more elegant way of getting 2-dimensional spatial information are *pixel detectors*. Here the semiconductor is subdivided into multiple smaller implant areas. Each pixel needs its own readout channel resulting in $N^2$ channels which is significantly higher than for strip detectors with $2N$ channels for 2-dimensional spatial resolution.

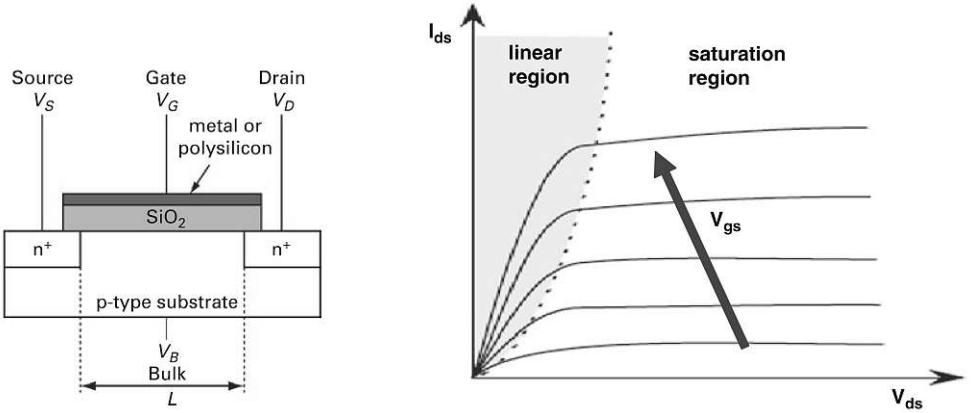
To cope with this bulk of electronics, hybrid pixel detectors are currently used. The hybrid pixel detector consists of a readout-electronics layer, connected via bump-bonding to the single pixels (figure 1.1). Thus, the two substrates are decoupled from each other, which prevents them from influencing each other and allows an independent development of the individual layers. The drawback of this technology is, that due to the complexity the bump-bonding yield is low, which makes this process quite expensive. Furthermore, this technology requires a high material budget resulting in multiple Coulomb scattering, which has a negative impact on the tracking performance [1].

The high-voltage CMOS-technology offers a different approach, *depleted monolithic active pixel sensors* (DMAPS). The front-end readout electronic and the sensor diode are both implemented on the same wafer. This way, the cost-intensive bump-bonding process is obsolete and less material is needed. Since the CMOS technology is used in the

commercial chip industry, the production is cheaper and faster and it also leads to the reduction of the *Minimum Feature Size* (MFS) resulting in overall smaller chips, making this technology possible in the first place. There are still unsatisfying issues like the radiation tolerance and the timing resolution [10].

## 3.1 CMOS-Logic

Since the readout electronic of DMAPS is highly dependent on CMOS logic, this section will deliver some fundamental information about this topic. *Complementary Metal-Oxide-Semiconductor* (CMOS) is an integrated circuits fabrication process combining *p-type Metal-Oxide Semiconductor* field-effect transistors (PMOS field-effect transistors) and *n-type Metal-Oxide Semiconductor* field-effect transistors (NMOS field-effect transistors). So the use of the Complementary *Metal-Oxide-Semiconductor field-effect transistors* (MOSFETs) enables an efficient process of designing digital circuit functions but is also helpful in analog circuits such as image sensors [13].
The MOSFET provides three terminals, as can be seen in figure 3.1a for an NMOS transistors. The *source* delivers the charge carriers, which in turn are collected by the *drain*. The amount of charge carriers that reach the drain from the source is determined by the *gate*. For gate-source voltages $V_{GS}$ below a threshold voltage $V_{th}$, the electron charge is around zero, so the bulk between source and drain acts as an insulator. As $V_{GS}$ rises above $V_{th}$ and $V_{DS} < V_{GS} - V_{th}$ also the drain-source current $I_{DS}$ (electron charge) increases linearly, as can be seen in figure 3.1b. This happens due to an inversion channel of electrons built underneath the electrode resulting in a conductive connection between source and drain. For $V_{GS} > V_{th}$ but $V_{DS} > V_{GS} - V_{th}$, the source drain current $I_{DS}$ saturates, being only weakly dependent on $V_{DS}$ [11].




(a) Cross-section of an NMOS transistor with the respective terminals [11].

(b) Drain current $I_{DS}$ in dependence of source to drain voltage $V_{DS}$ for rising gate to source voltages [12].

Figure 3.1: Cross-section and IV characteristics of a MOSFET.

## 3.2 Monolithic Active Pixel Sensors

In the field of monolithic pixel detectors, two types can be distinguished. First, *Charge-Coupled Detectors* (CCD) were developed, which are based on the fact that the charge is transferred from pixel to pixel leading to the output sense node at the side of the array. This limits the amount of readout electronics required and also results in a large fill factor. In addition, the sensitivity is quite high and the noise of the output amplifier is very low, due to the low capacitance of the output sensing node. However, this technology is quite dependent on radiation damage, since only a single defect in silicon can trap electrons, leading to a reduction of the *Charge Transfer Efficiency* (CTE). Since the CTE must be almost perfect in order to operate the detector adequately, the maximum size of the array and the maximum readout rate are limited [14].

At monolithic *active* pixel sensors, *low voltage* p- and n-channel transistors are directly integrated into the pixel. To enable high and low voltage on the same substrate, a so-called floating logic is required. In a p-substrate process, this floating zone appears as a lowly doped *deep n-well* embedded in a predominant *p-substrate* (figure 3.2). This *deep n-well* contains the different transistors for the pixel electronics. The PMOS transistors are directly located in the *deep n-well* (blue region), while for the NMOS transistors there is an additional *p-well* structure within the *deep n-well* (red region).
The *deep n-well* acts as an insulator between the inherent low-voltage logic and the *High Voltage* (HV) occurring in the *p-substrate*. This enables applying of an HV with respect to the p-substrate, without damaging the transistors in the floating logic [15]. The HV forms a depletion zone in the *p-structure* next to the *deep n-well* and allows particle detection, due to the current implied by the separation of the charge carriers by the electric field (see section 2.2.3).
So the floating logic structure enables complex CMOS readout circuits inside the *deep n-well*. This way, pixel readout selection, amplification and buffering is possible directly

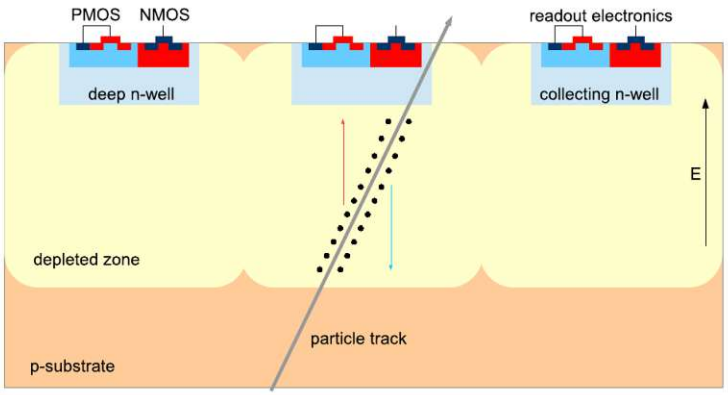



Figure 3.2: Cross-section of an depleted HV-CMOS-DMAPS with an traversing particle [1].

on site like in the hybrid detector [15].

## 3.3 RD50 Second prototype DMAPS chip

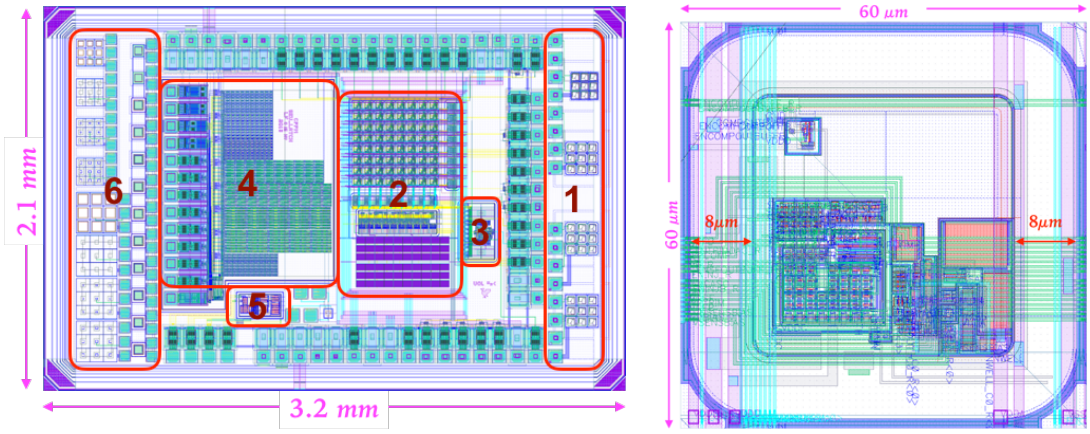
For the purpose of this project, the sensor prototype RD50-MPW2 (figure 1.3) was used. It is a follow-up chip to the first prototype RD50-MPW1. This chip was developed to get a feeling for the workflow of designing and fabricating a detector. However, it caused problems with a high leakage current and also a too low breakdown voltage. Also, the digital readout part was not working properly, due to cross-talking [1]. All these issues should be taken care of with the new developed RD50-MPW2 chip. For the readout of the newly developed chip the digital part was omitted and the full concentration was put on the analog front end part. This means that only one pixel can be read out at a time. Another significant change is the enlargement of the pixel size from 50 µm × 50 µm to 60 µm × 60 µm.

### 3.3.1 General Structure

It is based on the monolithic CMOS technology discussed in section 3.1, developed using the 150 nm HV CMOS technology LFoundry process and manufactured in February 2020. The chip size is 2120 µm × 3211.66 µm. The wafers are fabricated with the resistivities 10 Ω · cm, 200-500 Ω · cm, 1.9 kΩ · cm and 3 kΩ · cm. Per resistivity two wafers are produced with a thickness of 280 µm resulting in 80 chips per resistivity. The floorplan of the whole chip shows the different structures present on the RD50-MPW2 chip (figure 3.3a). (1) represents passive test structures for I-V measurements and edge transient-current technique measurements of single pixels. (2) is the active matrix with 8 × 8 pixels. (3) is the analog buffer for the analog readout and (4) is the Single Event Upset tolerant memory array. (5) delivers the band gap reference voltage and (6) is a test structure with single photon avalanche diodes [5].

### 3.3.2 Active Pixel Matrix

Figure 3.3b shows the floorplan of a single pixel with dimensions of 60 µm × 60 µm. The cross-section of the pixel (figure 3.4) is very similar to the cross-section of the RD50-MPW1 and consists mainly of the p-substrate for a sufficiently large depleted sensing volume, biased with a high negative voltage HV. The deep n-well (DNWELL) acting as the collecting electrode is biased with the power supply voltage $V_{\mathrm{DN}}$ through a combination of an n-well and a NISO layer. NISO is an n-type layer used to isolate the low voltage p-wells from the high voltage p-substrate. So the p-substrate and the deep n-well build the pn-junction used for the detection of the particles. The deep p-well (PSUB) isolates the in-pixel n-wells (NWELL) from the deep n-well so that in each pixel CMOS electronic circuits can be established. The overlap between the deep p-well and the neighbor p-wells avoids punch-through between the n-well and the deep n-well [16].




(a) Whole RD50-MPW2 chip (b) Single pixel

Figure 3.3: Floorplans of the RD50-MPW2 chip [5].

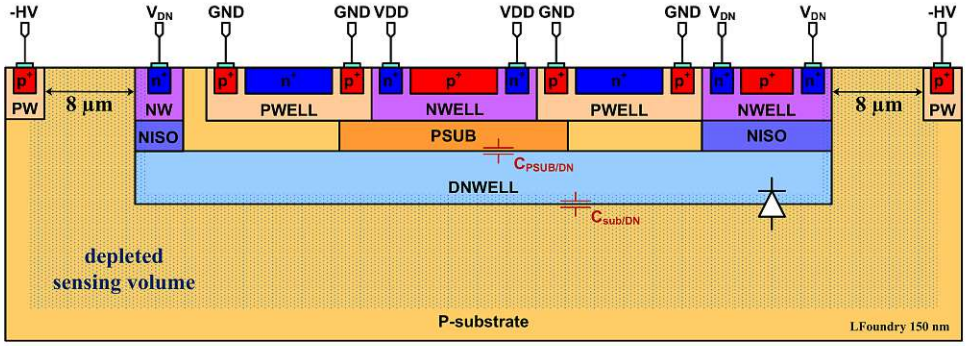



Figure 3.4: Cross-section of the RD50-MPW2 detector with the differently doped regions [5].

### 3.3.3 Analog Readout Process

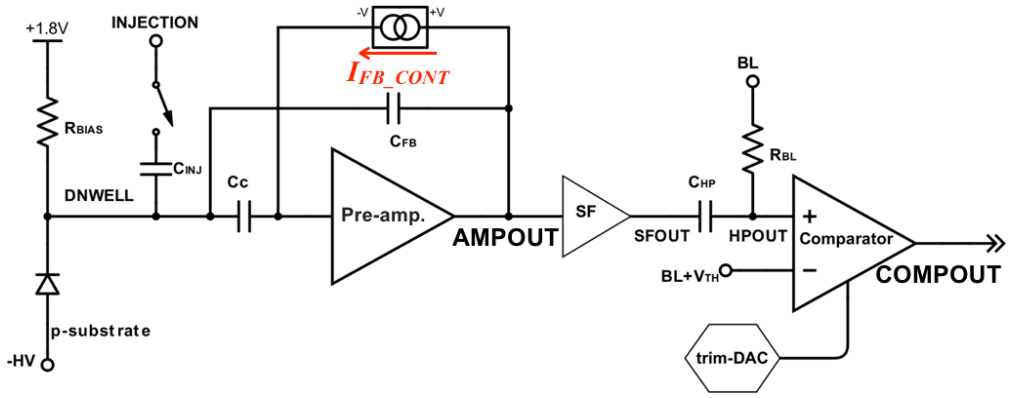
The whole matrix consists of two different pixel flavors according to the analog readout type (figure 3.5). Column 0-3 consists of *Continuous Reset*-pixels (CR-pixels) and column 4-7 of *Switched Reset-pixels* (SR-pixels).
The charge of an incoming particle present in the depleted p-substrate will be collected by the DNWELL. For testing reasons, it is also possible to simulate a particle by an injection pulse. The detected or produced signal is now amplified by using a *Charge-Sensitive Amplifier* (CSA), resulting in the AMPOUT-Signal (available with a pad) for the feedback and the input of the source follower used as a buffer amplifier. The analog SFOUT (available with a pad) will be shifted to BL-level with an RC high-pass, to be able to compare it with a threshold voltage composed of the baseline (BL) and $V_{\text{th}}$. $V_{\text{th}}$ can be varied with a *trimmable Digital-Analog Converter* (TRIMDAC), adjusting the sensitivity

of the pixel. The digitized output of the comparator COMPOUT (available with a pad) can then be used for further purposes. The dead time of a pixel, i.e. the time in which the pixel is again ready to detect a new particle without pile-ups, is composed of the rising and falling edge duration ($t_{\text{rise}}$ & $t_{\text{fall}}$). The smaller the dead time, the higher the response rate.

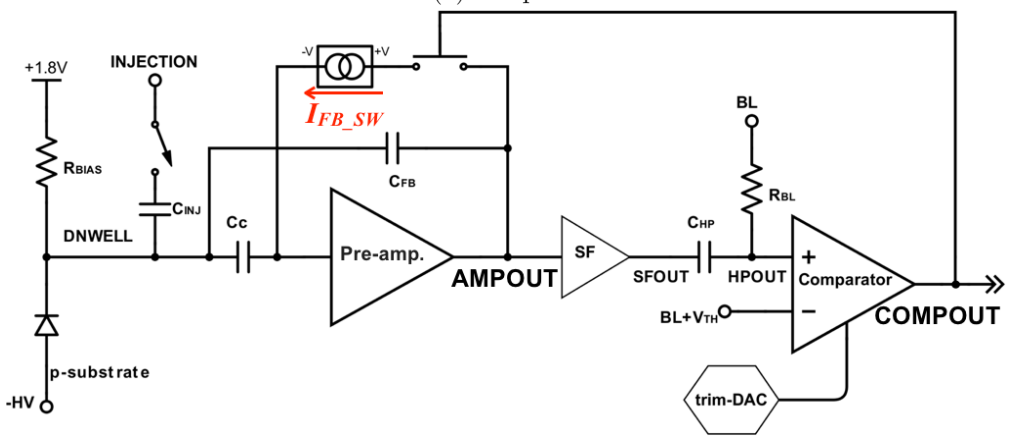
$t_{\text{rise}}$ is proportional to $C_{\text{d}}/g_{\text{m}}$, where $C_{\text{d}}$ is the detector capacitance mainly composed of $C_{\text{sub/DN}}$ and $C_{\text{PSUB/DN}}$ (see figure 3.4) and $g_{\text{m}}$ the transconductance, depending on the input transistor of the CSA. Since $g_{\text{m}} \propto I_{\text{out}}$, with a high drain current of the input transistor and a low overall capacitance of the detector, we get a desirable small rising time.

$t_{\text{fall}}$ is inversely proportional to the feedback current $I_{\text{FB}}$ responsible for returning the pixel to its original state. This pixel reset can be realized in two different ways.

At CR-pixel (figure 3.5a) the respective feedback current $I_{\text{FB\_CONT}}$ is constant, so the charge $Q$ of the feedback capacitor $C_{\text{FB}}$ is linearly discharged. $t_{\text{fall}}$ is therefore proportional to the input charge enabling the *Time over Threshold*-measurement (ToT-




(a) CR-pixel



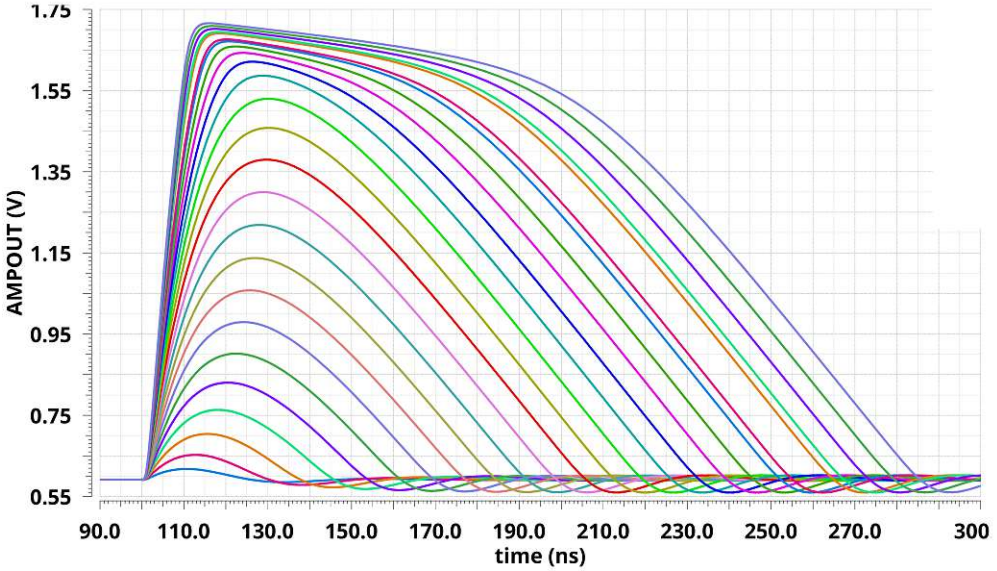

(b) SR-pixel

Figure 3.5: Schematics for different types of pixel-reset methods [5].

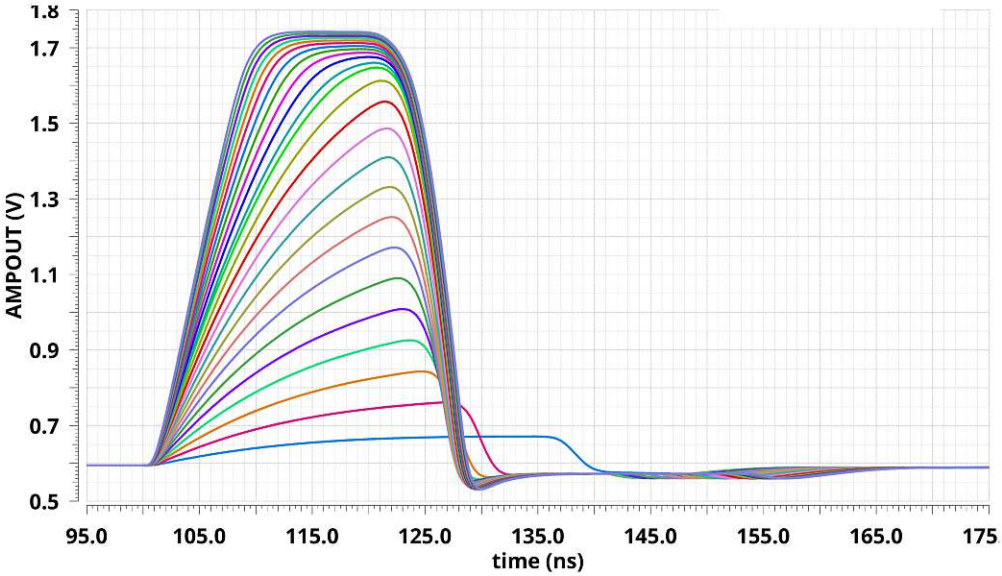
measurement). $I_{\text{FB\_CONT}}$ has an upper limit, due to a resulting increase in noise and a lower charge-to-voltage gain. The simulated signal AMPOUT of a CR-pixel can be seen in figure 3.6a.
At the switch reset pixel (figure 3.5b) $C_{\text{FB}}$ is discharged asynchronously. The feedback circuit is normally open, so no current $I_{\text{FB\_SW}}$ flows. Only when the comparator output COMPOUT jumps to high, the switch is closed after a 15 ns delay. Within 5 ns the pixel is reset, whereby COMPOUT jumps to low and the feedback loop is interrupted again. Since the capacitor is not discharged until the reset, the current $I_{\text{FB\_SW}}$ can be quite high without influencing the noise level and the charge sensitivity, which makes the discharge process way faster. This is also visible in the simulation of AMPOUT (figure 3.6b) and in figure 3.7, the monitoring outputs via the analog buffer are visible. However, now that the charge is not proportional to $t_{\text{fall}}$, it is no longer possible to determine the charge from the ToT [5].

### 3.3.4 Chip Configuration

A bias block generates the required voltages for the analog circuit, which then supplies the transistors with voltages at the desired operating points. To set these biases, as well as other row and column-specific settings there are configuration registers, which can be set by shifting a long chain of bits into the chip. The previously set configuration chain is pushed out again for control purposes. For monitoring reasons, it is possible to route the source follower output (SFOUT) or the comparator output (COMPOUT) of a specific pixel to an output pad. For each pixel individually, the injection signal can be enabled and the respective TRIMDAC value can be set.

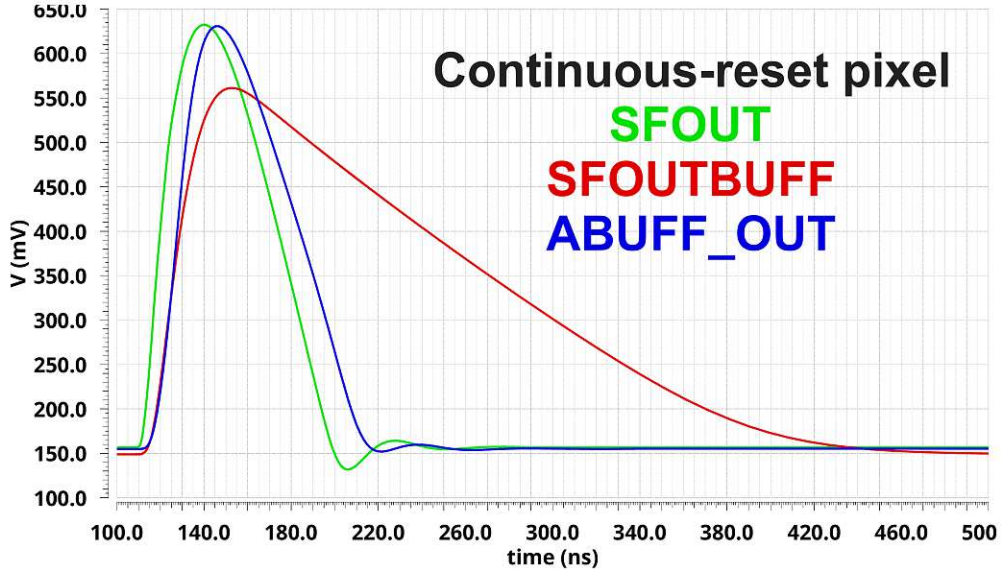



(a) CR-pixel

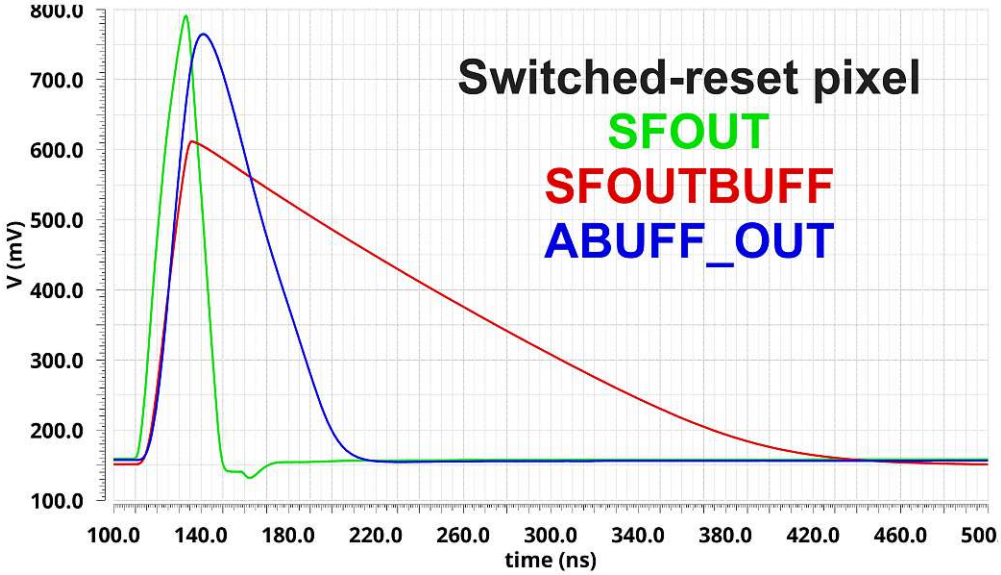



(b) SR-pixel

Figure 3.6: Simulation of AMPOUT for the different kind of pixel-reset methods with injection voltages equivalent to energies from 1k$e^-$ to 1k$e^-$ and with HV=−60V [17].




(a) CR-pixel




(b) SR-pixel

Figure 3.7: Simulation of SFOUT, SFOUTBUFF, ABUFF_OUT for the different kind of pixel-reset methods for an injection pulse with 1 V [17].

CHAPTER 4

# Data Acquisition

The definition of *Data Acquisition* (DAQ System) is given as follows *"Data acquisition is the process by which physical phenomena from the real world are transformed into electrical signals that are measured and converted into a digital format for processing, analysis, and storage by a computer"* [18]. In this work, radiation represents the physical phenomenon that is converted into an electrical signal using an HV-CMOS DMAPS detector, as already described in the previous chapters.

## 4.1 Data Acquisition Process

The DAQ is composed of 4 different activities:

- acquisition
- processing
- integration
- analysis

First, the physical quantity is sensed and converted into an electrical. The conversion can happen *directly* by ionization or indirectly, where different energy conversions are taking place before receiving the final electrical signal. The direct detection has already been discussed in detail in section 2.2, so only the indirect detection will be shortly explained. An often used indirect detection is done by the use of scintillators. Ionizing radiation penetrating a scintillator material leads to exhibition of luminescence. The absorbed energy from the incoming radiation is converted into near visible light. This light is then detected by a *Photo Multiplier* (PM) and converted into an electrical signal.
After the signal has been detected, it is processed in the so-called *front-end* electronic,

which is located very close to the detector. Here the signal is amplified and by applying a shaper, it can be manipulated (e.g. pulse stretching, spreading techniques) to simplify the further processing of the signal (pile-up cancellation, timing measurements, ...). Before the signal is further processed using more sophisticated methods, it must be digitized using an *Analog-Digital Converter* (ADC). This step can also be performed in the back-end electronic.
By means of a suitable data bus system, the data is passed on to the back-end electronics. With high-performance processors different processing algorithms can be applied. These algorithms may contain digital filtering, pulse shape analysis, pile-up deconvolution and timing measurements [19].

## 4.2 Triggering and Data Flow

The DAQ process can be operated in two different ways. At *triggerless* DAQ, the detector pushes data at its speed and the DAQ must handle all the incoming data. When using a *trigger*, only the interesting events are selected, while all the other events are rejected. There are two essential connections to enable a trigger-based DAQ (figure 4.1). The trigger path transmits the required information from one or more detectors to reach a decision in the trigger logic. Only at a positive trigger decision, the acquired data is transferred to the storage unit. In contrast to the previous fast control, for non-time-critical applications like temperature control, supply voltages and configuration settings there is an additional slow control connection.

Since the DAQ system used for this work, relies on a trigger pulse, the workflow of a triggered acquisition process is described (figure 4.2). The data generated by the detectors is gathered in the readout section. This data is then formed into an event, with an associated trigger assigned. A high-level trigger enables to feed other trigger levels. The built event will then be moved to the storage unit [20].

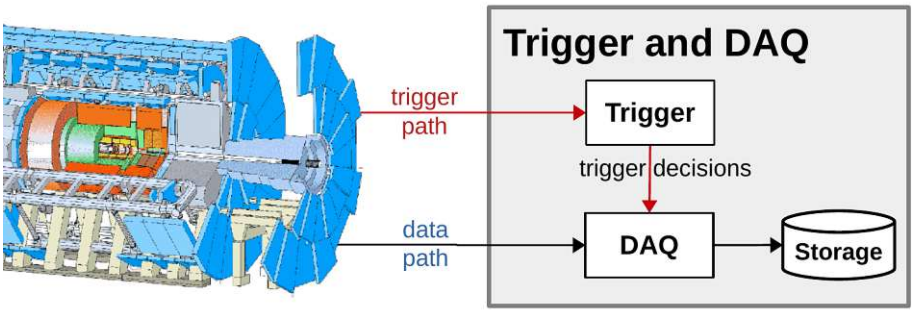



Figure 4.1: Illustration of trigger and datapath in the example of the ATLAS detector [20].

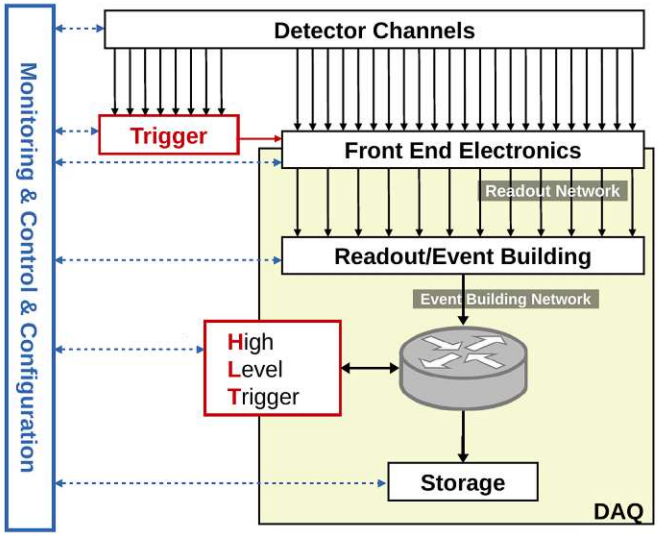



Figure 4.2: Data flow, data manipulation and operation of a triggered DAQ process [20].

## 4.3 Data Acquisition Software

A DAQ software enables the communication between the DAQ-hardware, the PC and the user. The software can be implemented in multiple programming languages and runs with the help of a *Central Processing Unit* (CPU). It can be established as a full *Graphical User Interface* (GUI), as an input/output control program, as a data logger or a combination of the respective components. In addition, monitoring functionalities can be built in, which ensure that everything runs smoothly during the measurement. Using the software, the user is able to send commands and set up specific parameters for the measurement. The incoming data can be manipulated before it is saved in the desired format [18]. The DAQ software used in the course of this thesis will be explained in detail in section 5.2.2.

## 4.4 EUDAQ2 Framework

Implementing several hardware (detector under device, telescope, ...) and software (run control, data collector, ...) components into one DAQ system is a complicated task to do. The modular, DAQ framework EUDAQ2[1] simplifies this integration process. It is used to perform continuous measurements. This open-source framework is written in C++ and is independent of the *Operating System* (OS). All components of the EUDAQ2-DAQ must be in the same network. With the console interface or even a GUI, the user can easily interact with the superior DAQ [21].

[1] https://github.com/eudaq/eudaq

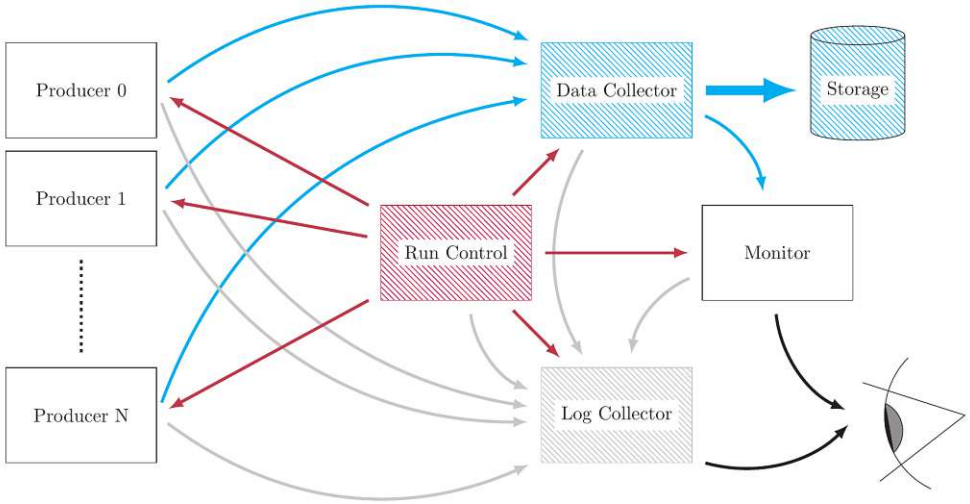



Figure 4.3: Schematic of EUDAQ2 architecture with command-, data-, and log flow between the respective components [21].

### 4.4.1 Architecture of EUDAQ2

The central component of the EUDAQ2 architecture (figure 4.3) is the *run control* communicating with all the other components connected to it via a TCP/IP-based protocol. Within the framework there are three different information channels. The command channel (red), the data channel (blue) and the log channel (grey). The communication within the hardware is based on a trigger-busy communication protocol. The architecture is composed of the following components [21, 22]:

- The *run control* is the user interface for controlling the DAQ. All the command channels originate from here and are received from the other components via a standardized command receiver. This way, it is able to start a measurement *RUN*, which is divided into several *events*, representing all the data from the measurement. Also, other standardized commands can be sent via the run control. It also monitors all the different processes and determines the global state of the whole DAQ-system.

- The *producer* is any device that creates data, for example the *Device Under Test* (DUT) or the telescope detector. When receiving a trigger, the producer should create one event and send it to the data collector. The serialized data sent with the producer contains a header with the run number, the trigger number and the actual unprocessed raw data from the detector.

- The *log collector* gathers all the logs from all the other components via the log channel, to inform the user of the current state or an unexpected behavior of a specific component. The three different log-levels for the messages sent to the log

collector are INFO, WARNING or ERROR. For the chronological reconstruction of the events, associated *timestamps* (TSs) are appended.

- The *data collector* arranges, synchronizes and then combines all the incoming data originating from the producers into a single stream and writes it to a storage disk.

- The *monitor* receives data from the *data collector* to create plots for online monitoring of the whole measurement with the help of ROOT[2].

### 4.4.2 Finite State Machine

For EUDAQ2, the *Finite State Machine* (FSM) in figure 4.4 is used to control the DAQ process. An FSM is characterized by being in only one state, of a finite number of states, at any given time. The state machine is always in the state of the connected components with the lowest priority. A change of the current state is only possible via predefined transitions, as can be seen in figure 4.4. This avoids unpredictable situations like deadlocks or executing the steps in the wrong order. For EUDAQ2 the possible states are given in ascending order of priority as follows [22, 23]:

- ERROR: Any component can throw an error at any state and change to the ERROR state, in case there is an unpredictable event. With the *Reset* command, the FSM can switch to the UNINITIALIZED state.

- UNINITIALIZED: This is the state after the connection with the run control. The component is waiting for the *Initialize* command.

- UNCONFIGURED: The initialization has been performed and the component is ready for the *Configure* command. When a connection is added, the FSM jumps back to the UNINITIALIZED state.

- CONFIGURED: The component is now configured. When the configuration parameters have changed, it is possible to execute the *Configure* command again. Otherwise, the component is waiting for the *StartRun* command to begin the DAQ.

- RUNNING: The RUN has now been started. With the *StopRun* command the DAQ is ended and the FSM switches to the CONFIGURED state.

In addition to the commands already mentioned, there is the *terminate* command which exits the FSM. This command can be called from any state except RUNNING. The standardized commands responsible for the transition from pre-state to a state of success can be found in table 4.1.

[2]ROOT is an object-oriented software developed at CERN which is used for the analysis of data in the field of particle physics.

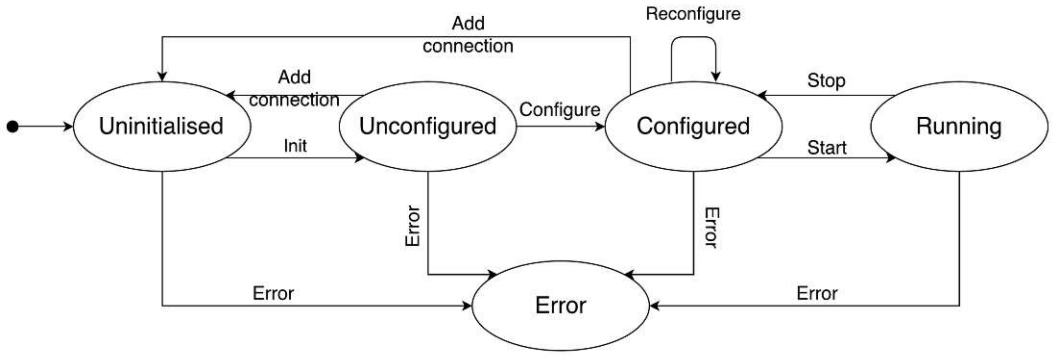



Figure 4.4: Block diagram of an FSM from EUDAQ2 with the different states and the respective transitions [22].

| Command | Pre-state | State of success |
|---|---|---|
| Reset | ERROR | UNINITIALIZED |
| Initialize | UNINITIALIZED | CONFIGURED |
| Configure | UNCONFIGURED, CONFIGURED | CONFIGURED |
| StartRun | CONFIGURED | RUNNING |
| StopRun | RUNNING | CONFIGURED |
| Terminate | any except running | - |

Table 4.1: List of standardized EUDAQ2 commands for a transition from one state to another [23].

## 4.5 FPGA

*Field Programmable Gate Arrays* (FPGAs) are widely used to cope with the huge and computationally intensive amount of data. The FPGA consists of multiple inputs and outputs which can be programmed individually to implement arbitrary combinational logic. *Hardware Description Language* (HDL) is used to program the electronic circuits of FPGAs. The most common high-level languages of HDL are are VHDL and VERILOG [24].

### 4.5.1 Architecture

FPGAs consist of two-dimensional arrays of logic blocks which are surrounded by programmable I/O blocks (figure 4.5). These blocks are interspersed with reconfigurable interconnections (electrical switches), allowing the blocks to be connected in different combinations. This is the main difference to custom *Integrated Circuits* (ICs), where the logic blocks are interconnected with permanent metal connections. The functionality of the blocks themselves can also be configured as desired. The complexity of a block ranges

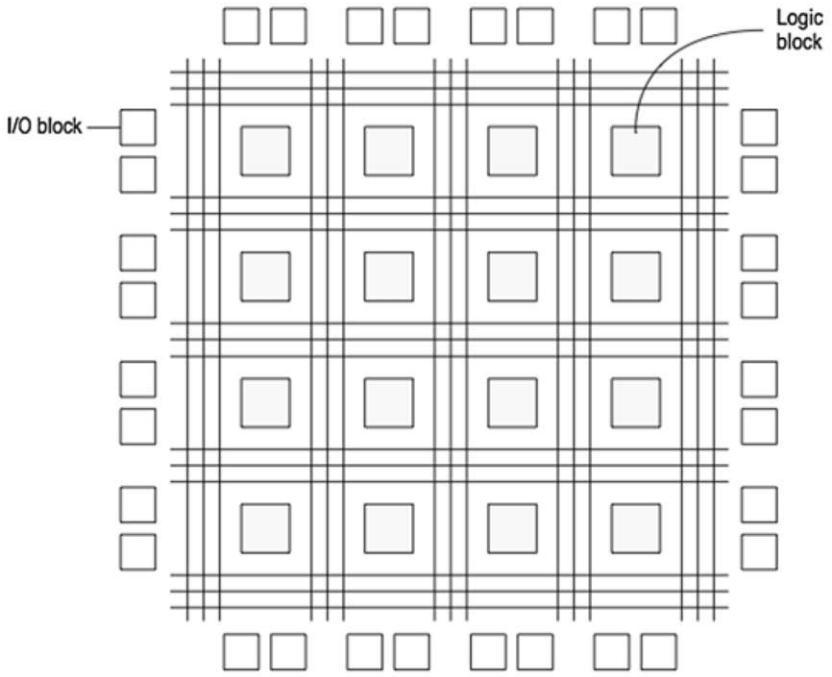



Figure 4.5: General structure of the architecture of an FPGA [25].

from the functionality of simple transistor circuits (logic AND, OR and XOR gates) to an entire microprocessor based on the logic gates. Logic blocks also contain memory elements formed by simple flip-flops or more complete blocks of memory [25, 24].

### 4.5.2 Performance and Application

FPGAs allow the user to realize an entire *System-on-a-Chip* (SoC), as an alternative to the *Application-Specific Integrated Circuits* (ASICs), which are considerably more expensive when the number of pieces is small. Also, if the use case changes slightly, or something does not work properly, it is not necessary to design a new circuit using an ASIC, but the circuit can simply be reprogrammed using FPGAs. Due to the parallel nature of FPGAs, a huge computational throughput is possible. Time consuming tasks, normally taken care of by the software, can be outsourced to the FPGA. The field of application includes data processing and storage, digital signal processing as well as instrumentation and telecommunications [24].
For the purpose of the DAQ system for this thesis, the FPGA houses on an evaluation board to control the sensor and process the incoming data.

## 4.6 Evaluation Board

An evaluation board is a *Printed Circuit Board* (PCB) designed to provide a variety of settings and options. It can be easily configured for specific applications and takes up as much space as it requires. Since the evaluation board is always sold in a combination with a specific microprocessor, it is often provided by the microprocessor manufacturer itself. The *Central Processing Unit* (CPU) allows running a SoC on the evaluation board, which is usually supplemented with an FPGA. This represents the logical core of the DAQ. This allows the evaluation board to run the DAQ software or even a whole operating system OS that contains the DAQ software. An SD-slot allows inserting a card, which contains for example the operating system. In addition, the board includes a memory to run the SoC. A serial link or an Ethernet Port is used to communicate with the board from the PC. Multiple I/O-devices provided connections to required devices [26]. A widely used standard connector is the *FPGA Mezzanine Card* (FMC) which works intimately with an FPGA [27].

CHAPTER 5

# CaRIBOu DAQ-System

The *Control and Readout Inner Tracking Board* (CaRIBOu) system (figure 5.1) forms a stand-alone DAQ framework used for new detector prototypes. So far, developing a DAQ system (hardware as software) for a new detector has always taken a considerable amount of work. The generic framework for hardware and software minimizes the effort to implement new detector devices into the DAQ. Due to its high-performance and flexibility, the CaRIBOu system can be used in stand-alone operation in the laboratory but also in test-beam facilities. Its modular nature allows it to be used together with multiple other detectors, altogether within a superior DAQ. Since the CaRIBOu system is set up as an open-source project, all design files regarding hardware, software and firmware are provided in a repository [28].

## 5.1 Hardware

The hardware of CaRIBOu (figure 5.1 from right to left & figure 5.2) consists of

1. the commercially available *System-on-a-Chip* board ZC706 (*evaluation board*),
2. the self-developed *Control and Readout* board (*CaR-board*),
3. the self-developed *breakout board* above the CaR-board,
4. and the detector-specific custom designed *chipboard* to fit the sensor/chip ASIC (RD50-MPW2).

The detector chipboard sits directly on the CaR-board. To access different inputs and outputs (FPGA, chip, ...) there is an additional breakout board. The connection between the CaR-board and the evaluation board can be established directly or with an according FMC cable for a remote operation [30]. All the mentioned boards are mounted on the

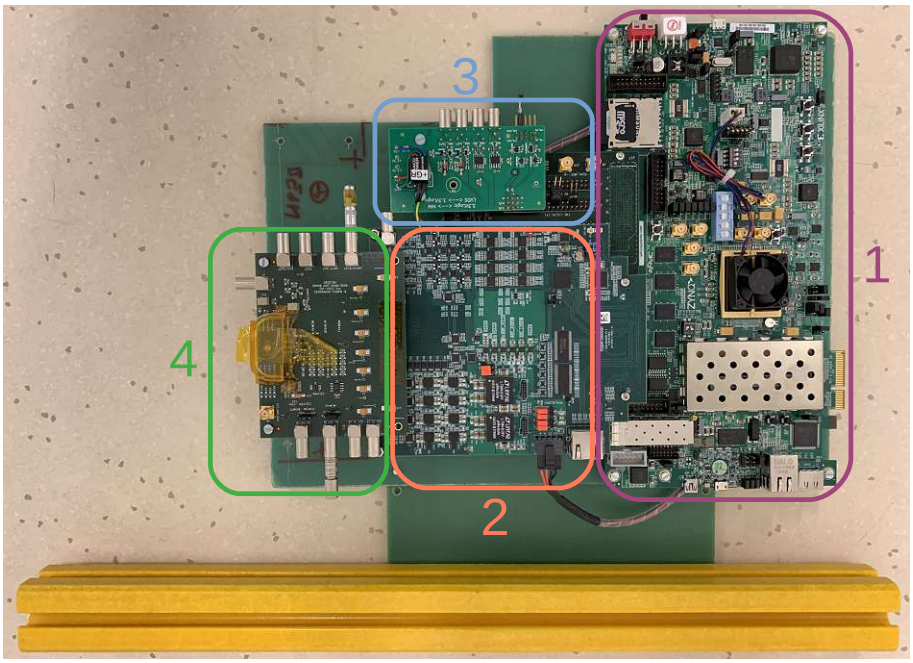



Figure 5.1: Hardware architecture of the CaRIBOu-setup, with the associated mounting fixation.

green Vetronit plate, which in turn is attached to the yellow rail. This is used to mount the setup in the test-beam facility.

### 5.1.1 RD50-MPW2 Chipboard

To keep the costs of the chip to a minimum, it only provides essential functionalities. The chipboard contains an HV-CMOS detector, a 12-bit ADC to digitize the different voltages from the chip and a thermometer. These devices are connected with the pin-connector for power supply, biases, data connection, slow-control via $I^2C$ clock and direct connections to the FPGA. With LEMO coaxial connectors, the following inputs and outputs are established: HV-input, injection-input, two ADC-inputs, ABUFF-output, CMPBUFF-output, SFOUTBUFF-output and SOUT-output. Test pins are available to check the set voltages.

### 5.1.2 CaR-Board

Since the hardware on the chipboard is limited, the CaR-board[1] offers a wide range hardware environment for various detector chips. The CaR-board contains power supply voltages, biases, current outputs, clock generators and injection pulser. It is also equipped

[1] detailed specifications available in [31]

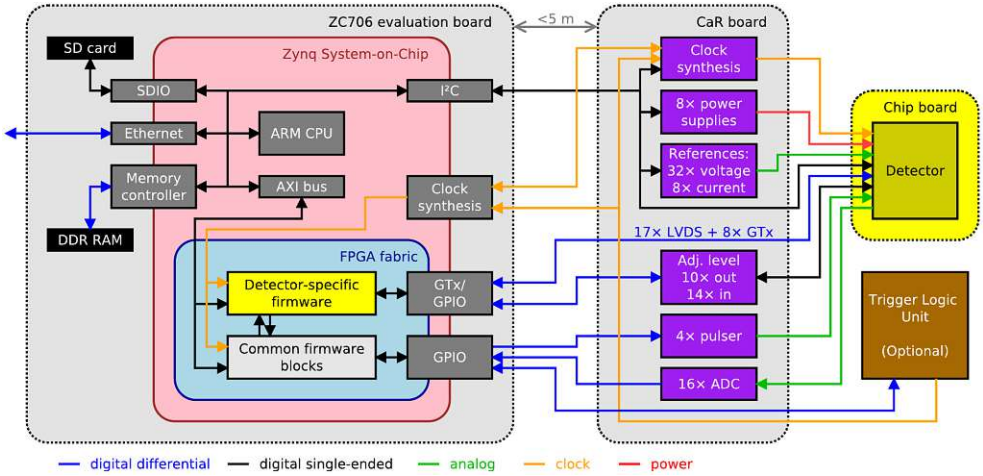



Figure 5.2: Schematics of the complete CaRIBOu hardware architecture and the connections between the different boards/components [29].

with multiple communication standards ($I^2C$, ...) and a set of ADCs, to enable monitoring of the DAQ-process. Due to direct connections from the chip to the CaR-board via the pin-connector, it is possible to operate these features close to the chip. The devices can be controlled by an $I^2C$-bus leading from the evaluation board to the devices on the CaR-board. Direct routing from the evaluation board connector to the chipboard connector leads to fast communication between the detector and the FPGA. The CaR-board also offers an HV-input via the LEMO coaxial connector directly routed to the chipboard [30]. More specifications are provided in [31].

### 5.1.3 Evaluation Board

The Zynq-7000 SoC ZC706 evaluation board from Xilinx [2] with the SoC consisting of the dual-core ARM Cortex-A9 processor and the Kintex-7 FPGA is the logic core of the DAQ. A Linux distribution is operated by an ARM processor located on the SD-card in the according SD-slot. The DAQ software is running on this distribution [30]. The sensor-specific firmware is running on the FPGA fabric. Via the AXI4 bus, the FPGA registers are connected to the CPU and mapped to a memory space of the processor. This allows direct writing and reading of the FPGA registers with the respective memory addresses [29]. To access and control the evaluation board, an *Universal Asynchronous Receiver Transmitter* (UART) or a *Secure Shell* (SSH) connection can be used. An RJ45 connector provides high-speed data transfer (1Gbps) and remote control with a superior DAQ system. Since the board is commercially available, it is easily available and a cost-effective solution for small-scale production [30].

[2] detailed specifications available in [32]

## 5.2 DAQ Software and Firmware

The non-hardware part of the CaRIBOu-system consists (figure 5.3) of

- the custom Linux distribution (*meta-CaRIBOu*)
- the software DAQ framework (*Peary*),
- and the FPGA processing image containing the compiled VHDL code (*Peary-firmware*).

The meta-CaRIBOu distribution already contains the DAQ *Peary* software and is hosted on the SD-card, running with the ARM processor of the evaluation board. The chip-specific *Peary-firmware* is hosted on the FPGA.

The *Hardware Abstraction Layer* (HAL) in *Peary* provides an unified access to physical hardware components. This is done by translating commands from the software into Linux driver calls which address the hardware components of the board. The AXI4 interface is the central communication system on the board, enabling communication between the FPGA, the periphery components and Peary within *meta-CaRIBOu*. Data from the chipboard will be forwarded to the main memory via the FPGA. The processor can now forward the data directly to the periphery or make it available to Peary [30].

a

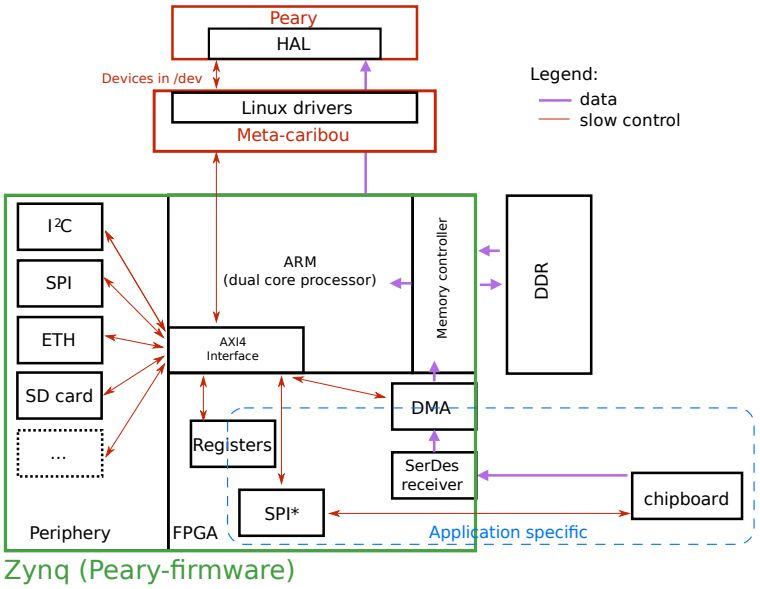



Figure 5.3: Software architecture of the CaRIBOu-DAQ. (figure adapted from figure 2 in [30])

### 5.2.1 Meta-CaRIBOu

Since the hardware of the evaluation board is specialized for certain applications but is cut down in other aspects, it requires a specially adapted OS, the *meta-CaRIBOu* distribution[3]. This specialized distribution is formed of a reference Linux distribution (Poky) modified with special functionalities for the Xilinx evaluation board ZC706 and the CaR-board using the so-called Yocto project. This is an open-source project for creating custom, hardware-specific, specialized Linux-based distributions [33].

#### Building Workflow

Figure 5.4 shows the different layers representing the workflow to build a custom Linux image. First, the developer must provide configuration scripts, packages, kernel patches and other custom functionalities. All these instructions are packed in so-called recipes, which are located in the different layers (meta-...). The base for the custom CaRIBOu distribution is built of the core reference distribution (Poky), the Xilinx layers (for ZC706 evaluation board) and several other layers, all fetched from the repository. Additionally to the base layers, there is a meta-CaRIBOu layer including all the CaRIBOu-specific recipes is needed. This layer also contains the DAQ *Peary* and the detector-specific *Peary-firmware*.
With the help of the bitbake build engine, all the different layers are fetched, patched and cross-compiled[4] regarding the respective recipes leading to a final boot image. The bitbake build engine also enables to cross-compile and build only single layers [34]. For example, this allows only the DAQ-Peary layer to be re-cross-compiled, making it easier

[3] `https://gitlab.cern.ch/Caribou/meta-caribou/`

[4] The compilation of a code is performed on the host environment, but the compiled software eventually runs on a different operating environment.

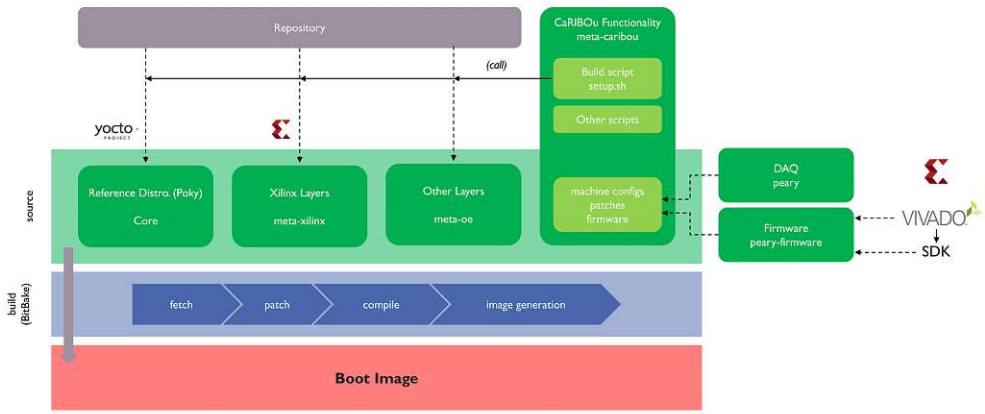



Figure 5.4: Workflow of the build process with the required layers for the custom meta-CaRIBOu distribution. (figure adapted from figure 2 in [34])

to develop the software. This compiled software can then be deployed directly on the meta-caribou distribution running on the evaluation board via SSH transfer. Generally, the distribution is controlled remotely via UART or SSH. With the help of a script provided by the meta-caribou layer, the image can be sent to the SD-card [29].

#### Distribution Features

The final custom CaRIBOu distribution exists of a console-only Linux image to provide computing power resources for other applications on the SoC. For the same reason, only essential special packages like python and SSH are installed on this distribution. A *Secondary Program Loader* (SPL) is required to load the bitfile of the Peary-firmware into the FPGA and sets the ARM CPU in the right state, while booting the OS. In the distribution also a device tree with the corresponding configuration of CaR-board hardware is set up. The patched kernel already provides $I^2C$ and SPI modules [30].

### 5.2.2 Peary

The DAQ software framework of the CaRIBOu-project is called Peary[5] and is already contained in the meta-CaRIBOu distribution. The software is written in C++. With its inherit HAL it simplifies the correct configuration of the DAQ environment for the chip, as well as the actual DAQ through suitable interfaces.

Peary enables the user to control and communicate with the CaR-Board and the devices on the chipboard. A device can be added with a single command. Also, setting the required power supply voltages and biases as well as the configuration of the device happens with unified commands. Settings required for initialization can be passed to Peary with a configuration file. The device manager of the software is able to handle several devices at the same time. There is a comparatively small effort in code writing to add a new device because of the user-friendly HAL and templates for creating device-specific functions [29]˙ The standardized commands (same as in table 4.1) and common modules like the logging engine are very useful for communication with a superior DAQ Client such as EUDAQ2.

#### Architecture of Peary

Figure 5.5 shows the architecture of the Peary framework. The HAL enables the developer to handle the hardware peripherals as simple C++ objects, which allows them to be standardized and uniformly integrated into the software. The chips, the modular parts of the DAQ are handled as *devices*. So if a new detector is added, a new device must be created. The rest of the software remains untouched. Adding a new device is a comparatively small effort in code writing because of the user-friendly HAL and templates for creating device-specific functions. The Device Manager allows multiple

[5] https://gitlab.cern.ch/Caribou/peary

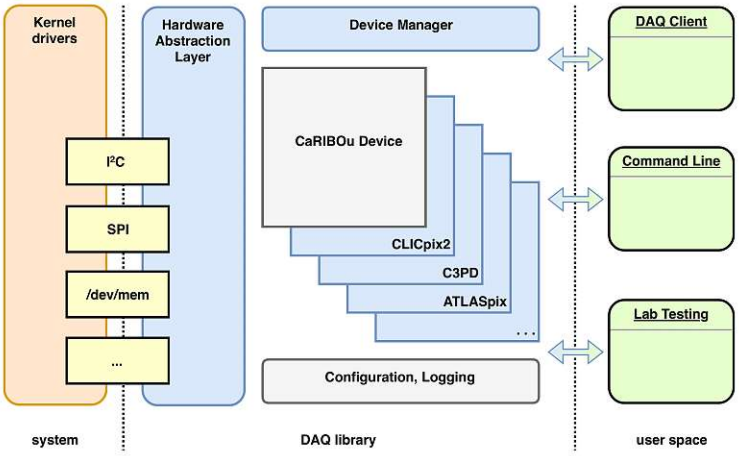



Figure 5.5: Architecture of the DAQ-Peary Software [29].

devices to be operated side by side at the same time. The configuration and logging procedures are standardized. Peary can be executed directly on the distribution using a *Command Line Interface* (CLI) but also by a superior DAQ Client such as EUDAQ2 with the help of an *Application Interface* (API) [29].

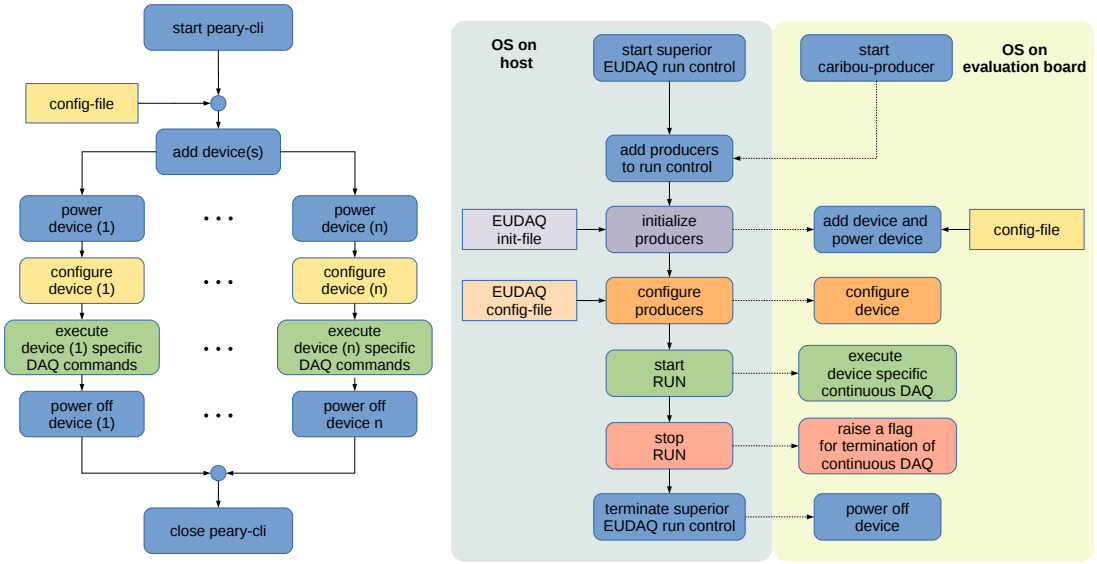
### Peary Device

So to implement a new detector into Peary, an individual new *device* has to be written, in form of a C++ class. It is used to set the required voltages and biases for the detector via the slow-control and to perform the actual DAQ by communicating with the chip over the FPGA.
It generally can be structured into the following three parts:

- In the *default header*, default values for the voltages, maximum currents and addresses of the CaR-board are set. It also contains the used registers of the FPGA and if available, also from the chip.

- The *device header* contains the definitions of the class functions with the respective access rights.

- In the *device main program*, device-specific CLI-commands, the registers of the FPGA and the chip, according to the default header, are added to the device. Also, the defined voltages and biases are used to set up the periphery. It also contains the basic functions required for every device, as well as device-specific functions.




(a) Workflow in laboratory operation with the peary-cli

(b) Workflow within a superior DAQ with the caribou-producer and EUDAQ2

Figure 5.6: Different measurement workflows for operation of the DAQ-Peary software.

### Operation of Peary

For the operation of Peary, two different modes are possible. For lab measurements the standalone operation using a CLI and for operation in a superior DAQ-environment (EUDAQ2) with the help of a caribou-producer. Before starting the measurement, the detector must be implemented into the Peary software and also the detector-specific firmware must be available in the CaRIBOu distribution.

- *Laboratory operation* (figure 5.6a) In this mode, a connection with the OS running on the evaluation board can be established via SSH or UART. The CLI is globally available and can be started with a configuration file. With the configuration file, set default values can be replaced with desired other values, for example voltages or biases. After launching Peary, one or more devices can be added and for each device a unique ID number is assigned. With this ID number, commands can be sent to the respective device. First, the devices need to be powered to establish the desired voltages for the chip. The configuration brings the chip into a state ready for measurement. In the MPW2, for example, a bitstream is inserted into the chip, which determines the internal voltages and contains additional settings for the pixels (see section 3.3.4). Now device-specific DAQ-commands, representing finite measurements, can be executed. These commands can be added additionally to the standard commands available in Peary. After the measurement, the voltage must be switched off. This is automatically done for all devices, when closing Peary-CLI

- *Superior DAQ operation* (figure 5.6b): For running Peary in combination with EUDAQ2, the evaluation board must be in the same network as the host machine. After starting the run control of EUDAQ2 on the host machine, the caribou-producer must be started on the OS running on the evaluation board. The caribou-producer and other devices will be added to the run control. If now in the run control of EUDAQ2 commands are executed, at the same time the associated standardized commands are called on the evaluation board in Peary. For EUDAQ2, there are separate initialization and configuration files available. The files contain device-specific sections with the respective measurement parameters. These parameters can be transferred to Peary. However, transferring the parameters must be implemented in the software code of the caribou-producer on the evaluation board. At the initialization with the run control, at Peary one or more devices according to the initialization file are added and powered. The configuration file for Peary is still taken from the environment of the evaluation board. At configuration, all the standardized configuration commands for the devices are called. In contrast to the laboratory operation, the DAQ measurement must also be executed in a standardized command. The continuous measurement must be started with the help of a thread to keep the run control responsive. When stopping the measurement, a flag will be raised to ensure a secure termination of the continuous measurement. When the run control is reset or closed, all the devices are securely switched off.

### 5.2.3 Peary-Firmware

The Peary-firmware houses on the FPGA and combines custom CaRIBOu modules as well as commercial Xilinx *Software Development Kits* (*Intellectual Property Cores* (IPs)), containing Linux device drivers. The firmware is also responsible for the SoC-configuration (clock frequencies, address spaces and processor periphery settings). The registers of the FPGA are mapped into the CPU memory space (/dev/mem). The firmware acts as an interface between the CPU (software) and the detector (hardware). Since the hardware changes with the used sensor, also the firmware must be adapted to the respective detector. For the design of the firmware, an external Xilinx Vivado tool is used, resulting in a bitstream and a hardware definition. The device tree is built by the *Software Development Kit* tool (SDK-tool). The base firmware is located in a repository[6] and will be fetched from the meta-CaRIBOu layer with the help of a recipe during the build process [30, 34].

[6] https://gitlab.cern.ch/Caribou/meta-caribou

# CHAPTER 6

# Lab Measurements

Since the RD50-MPW2 detector is still a prototype, it was tested in the laboratory, before using it in an actual testbeam environment. Therefore, only the active pixel matrix was used, the passive test structure remained untouched. First, the basic functionality of the readout electronic was checked by means of the injection pulse measurement. Then TRIMDAC values were adjusted to obtain the maximum sensitivity for the pixel matrix. Finally, an open shutter measurement was performed using a radioactive source to test the functionality of the charged particle detection.

## 6.1 Setup

The hardware setup for the laboratory measurements is visible in figure 6.1. The pixel matrix sits on the RD50-MPW2 chip (figure 6.1 - 1), which in turn is located on the chipboard. This board is operated by using the CaRIBOu hardware-setup (figure 6.1 -

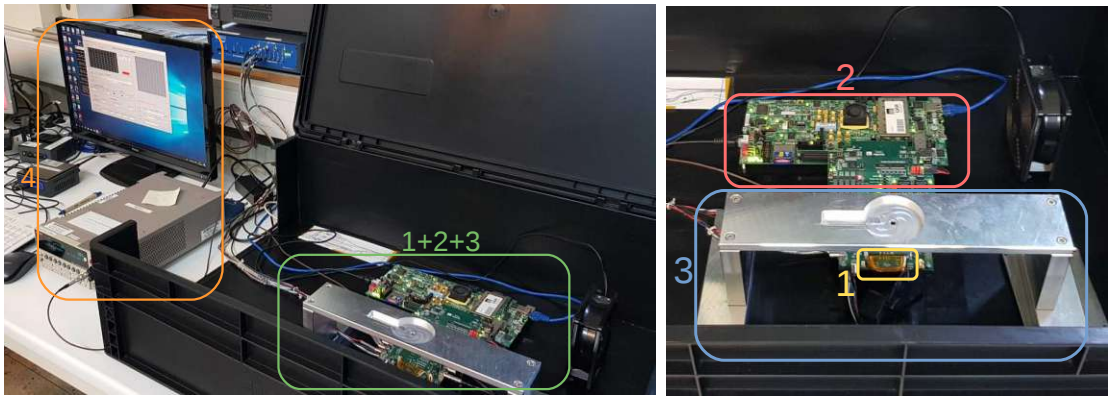



Figure 6.1: Hardware-setup for the laboratory measurements.

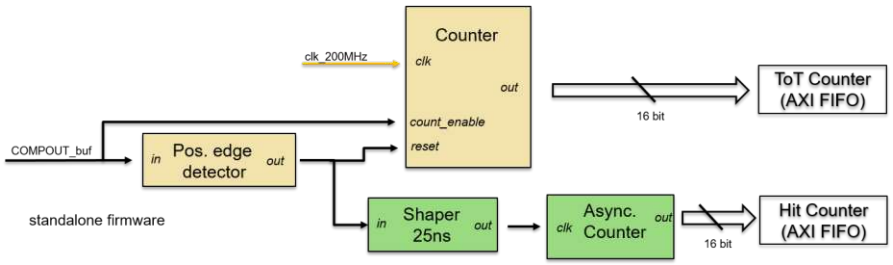



Figure 6.2: Firmware for standalone operation of the RD50-MPW2 chip [35].

2), which has already been described in section 5.1. For the open shutter measurements, there is an aluminum holder (figure 6.1 - 3) for the radioactive source to guarantee consistent, stable measuring conditions. All these components were placed together in a black box to avoid any influence on the measurement by light. The chip was supplied by the HV coming from the Source Measure Unit[1] (figure 6.1 - 4), which can be controlled remotely using a PC.
To read out the single pixels, an analog buffer in combination with a multiplexer is used to switch through the pixels individually. This means that only one pixel at a time can be read out. This pixel is determined by the configuration stream for the detector.
The injection pulse is generated with the CaR-board using the Peary software and is inserted right before the amplifier with the feedback loop, as can be seen in figure 3.5. With the help of the capacitor $C_{\text{inj}}$, the charge of an incoming particle is simulated. The pulse generated with actual particles originates from the diode consisting of the DNWELL and the p-substrate.

## 6.2 Measurement Process

For all the measurements, the two different pixel flavors were distinguished, as they have different kind of pixel-reset mechanisms, as described in 3.3.3. The outputs used for the laboratory measurements are the analog source follower output SFOUT and the digital comparator output COMPOUT. The threshold for the comparator is adapted with an *trimmable Digital-Analog Converter* (TRIMDAC), also using the configuration stream of the detector. For all the measurements, a comparator baseline (BL) of 900 mV was used. The buffered COMPOUT output is fed into the standalone firmware housing in the FPGA (figure 6.2). To detect the ToT-value, a 200 MHz counter is started by the rising edge and reset by the falling edge. To get the overall number of hits the edges are shaped and then counted by an asynchronous counter. The 16-bit ToT counter value and the hit counter value are written into an AXI *First In - First Out* (AXI FIFO), contained by the AXI-bus of the Xilinx evaluation board [35]. These two buffers are then read out by the DAQ software Peary and written into a file on the local memory space of the evaluation board.

[1] Keithley 2410 SMU

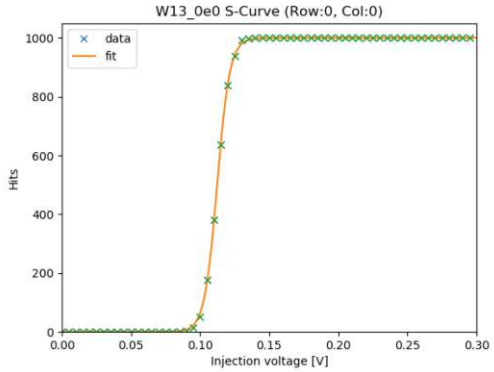



Figure 6.3: S-curve for a single pixel with 1000 injections per voltage step (10 mV), fitted with a sigmoid function.

## 6.3 Injection Pulse Measurement for Pixel Sensitivity

For this measurement, the injection for the respective pixel must be activated by the configuration stream. Then a certain amount of voltage pulses is injected by the CaR-board via the Peary software and afterwards, the counted number of hits is read out. This is done discretely for a specific voltage range. Above the threshold of the comparator, all sent injections are detected, but as the injection voltage gets lower, fewer hits[2] are registered, until no hits are registered at all. This leads to an S-like curve, which can be fitted with a sigmoid function[3], as can be seen in figure 6.3.

### 6.3.1 S-Curve Measurement for All Pixels

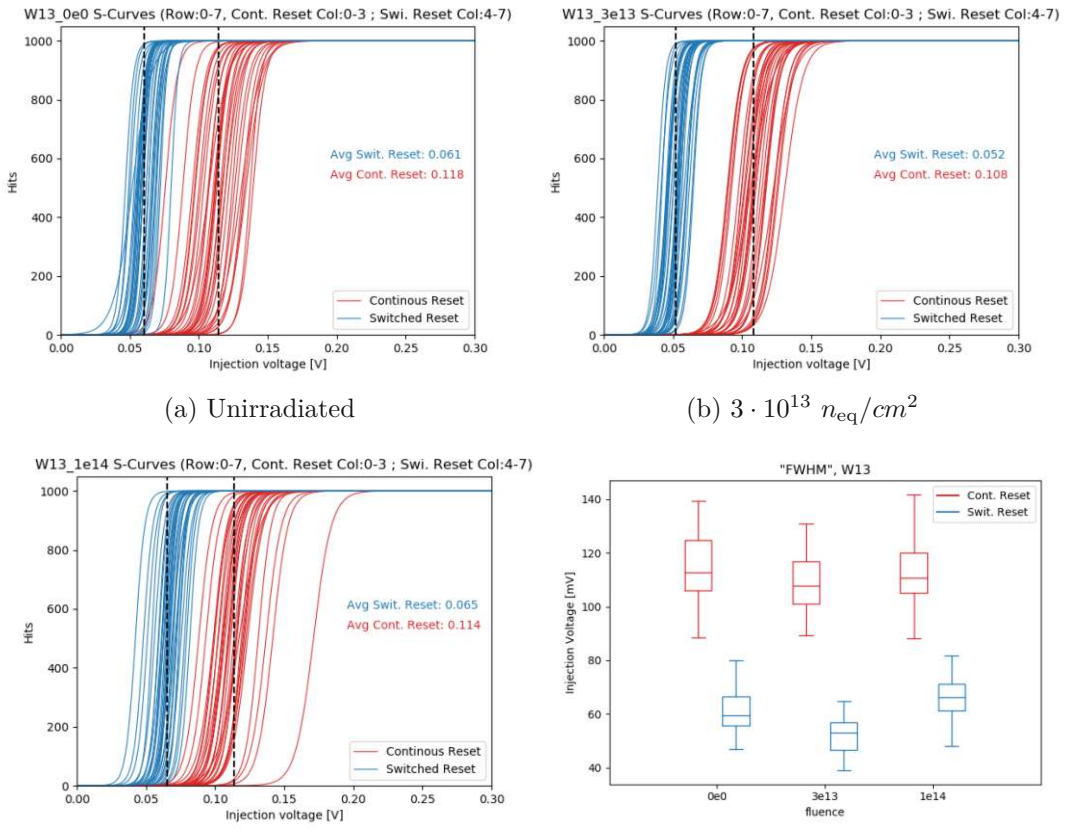
This S-Curve measurement was done with three separate chips from the wafer 13 ($> 2.2\,\mathrm{k\Omega \cdot cm}$), which has the highest resistivity from all produced chips. Two of the chips were irradiated in advance, to investigate the effect of radiation damage.[4] For this measurement, no HV was applied at all. Per voltage step (10 mv) 1000 pulses were injected, ranging from 0 mV to 30 mV. All 64 pixels were measured with the maximum TRIMDAC value to avoid possible noise.
Looking at the S-curves of the unirradiated chip (figure 6.4a), there is a clear difference between *Switched Reset*-pixel (SR-pixel), plotted in blue and *Continuous Reset*-pixel (CR-pixel), plotted in red. The mean value of the threshold, indicated by the vertical dashed line, is higher for the CR-pixel than for the SR-pixel. This implies that the SR-pixels are more sensitive than the CR-pixels, since the SR-pixels detect hits already at lower injection voltages. This observation is also true for the irradiated chips (figure

[2] "hits" might be a bit misleading, since no actual hits, but injections are detected. However, to facilitate the flow of reading, hits are treated equally to injections.

[3] $f(x) = \frac{1}{1+e^{-x}}$

[4] The irradiation is given equivalent to the effects of a 1 MeV neutron-equivalent fluence per /cm$^2$. Within this work, this is indicated with the unit $n_{\mathrm{eq}}/\mathrm{cm}^2$.

6.4b & 6.4c). Furthermore, it is noticeable that there are considerable variations within a pixel flavor.
To get a better understanding of this, the same data is visualized using a box plot. The voltage where 500 out of 1000 hits are detected, so basically a horizontal cut along the 500 hits border, called *Full Width Half Maximum* (FWHM), is plotted for each fluence (figure 6.4d). The spread of the curves within a pixel flavor equals the respective length of the bar. The box ranges from the first quartile to the third quartile and the horizontal line within the box indicates the mean injection voltage value. The observation made from this plot is, that for the threshold there is no clear trend visible. The threshold seems more dependent on the sample variation than on the fluence. Also, the spread of the curves is quite high but noticeably smaller for the SR-pixels. In general, there is no real trend visible regarding different fluences. To draw better conclusions, more statistics would be needed.



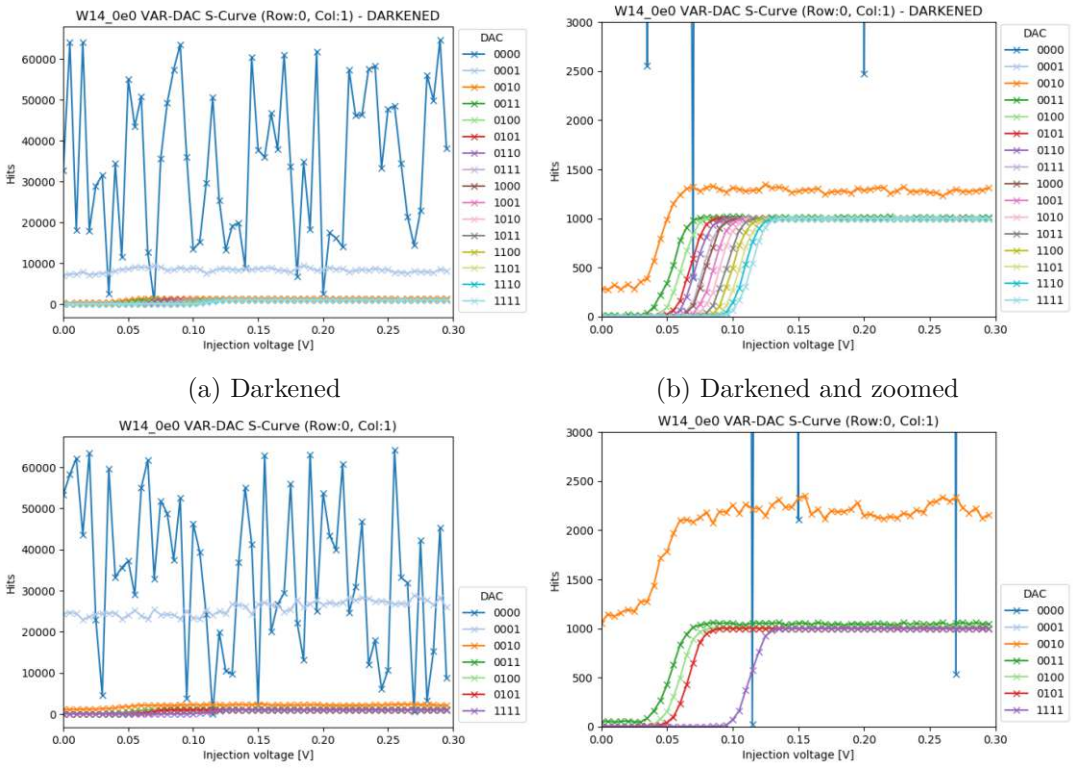

(a) Unirradiated

(b) $3 \cdot 10^{13}$ $n_{\mathrm{eq}}/cm^2$

(c) $1 \cdot 10^{14}$ $n_{\mathrm{eq}}/cm^2$

(d) Full width at half maximum

Figure 6.4: S-curves (a-c) and FWHM (d) for all pixels from unirradiated and irradiated chips from wafer 13, separated by the different pixel-reset method.




(a) Darkened

(b) Darkened and zoomed

(c) Not darkened

(d) Not darkened but zoomed

Figure 6.5: S-curves for variable DAC values for unirradiated chip from wafer 13.

## 6.4 TRIMDAC Adjustment

The threshold voltage $V_{\text{th}}$, that is put on top of the baseline voltage BL, can be varied for each pixel individually using a 5-bit TRIMDAC as can be seen at the analog pixel readout schematic in figure 3.5. This results in fine adjustments for the overall threshold $(BL + V_{\text{th}})$ of the comparator. Up to now, the TRIMDAC value was always set to the maximum. To optimize the pixel according to sensitivity, the TRIMDAC values have to be adopted.

### 6.4.1 S-Curve Measurement with Variable DAC Values for Single Pixel

To get a feeling for the influence of the different TRIMDAC values on the S-curves, they were varied over the whole 5-bit range for a single pixel. This measurement was performed with an unirradiated chip from the wafer 13 ($> 2.2\,\text{k}\Omega \cdot \text{cm}$). To determine the influence of light on the sensitivity of the sensor, one measurement was darkened with the help of the black box and the other was not.
Looking at figure 6.5a and 6.5b, the threshold is below the noise level for the three lowest

TRIMDAC values. Only with the next TRIMDAC value (green), the S-curve settles at the expected level. With this TRIMDAC-setting, the detector should be operated to provide the highest possible sensitivity because with increasing TRIMDAC values, also the S-curves shift more and more to the right, until the highest TRIMDAC value is reached. So incoming particles with an energy equivalent to a voltage below the threshold are not detected anymore. The S-curve with the highest TRIMDAC setting starts at around 100 mV which leads to a total variable range of about 50 mV. When comparing the darkened S-curves with the not darkened S-curves (6.5c & 6.5d), an influence of the light is visible but only for the three lowest TRIMDAC values, due to the increase of noise. S-curves with higher TRIMDAC values seem not to be affected by the light.

### 6.4.2 Automatic TRIMDAC Adjustment

To operate the pixels at the maximum sensitivity, an automatic TRIMDAC adjustment was implemented. The highest possible reasonable sensitivity is given, when the comparator threshold is just slightly above the noise level. This automatic adjustment was implemented in Peary, with the following workflow for a single pixel (figure 6.6). At first, *dac* is set to 7, the half of all the possible TRIMDAC values. The auxiliary variables *finished* and *over_zero* are set to 0. Now in the loop, the pixel is configured with the current *dac* value. The shutter is opened for 2 s and the detected hits are read out. Now multiple queries are performed. The combination of loop runs and queries can be described as follows:

1. The *dac* values are decreased until hits are detected. Then *over_zero* is set to 1.
2. Now the *dac* value is increased until no hits are detected anymore.
3. If two periods in a row no hits are detected, *finished* is increased to 2 and the adjustment for the pixel is done. The current *dac* value will be decreased by 1 before leaving the loop, to get a few hits. This is done because it results in a better sensitivity than with the *dac* value with zero hits.
4. If the upper or the lower border is reached before (0 or 15), the respective value is assigned.

This is now the adjusted *dac* value for the current pixel. This procedure is performed for every pixel in the matrix in parallel, until every pixel has an adjusted TRIMDAC value.

### 6.4.3 S-Curve Measurement with Adopted DAC Values for All Pixels

With these adjusted TRIMDAC values, the measurement from section 6.3.1 was repeated but only for the unirradiated chip from the wafer 13 ($> 2.2\,\mathrm{k\Omega \cdot cm}$).
Compared to the S-curves with the untrimmed DACs from figure 6.4a, the S-curves with the trimmed DACs (figure 6.7a) move to the left. Also, in figure 6.7b the boxes move to lower injection voltage. What can also be observed is that the voltage drop for the

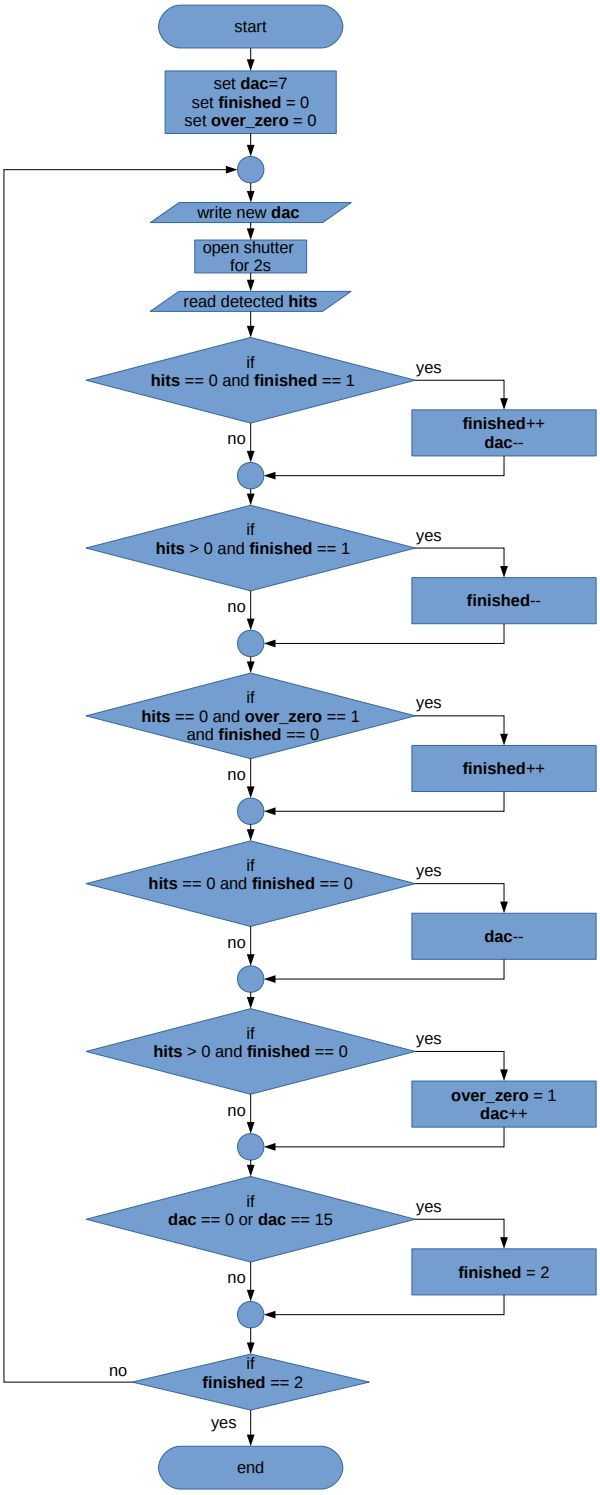
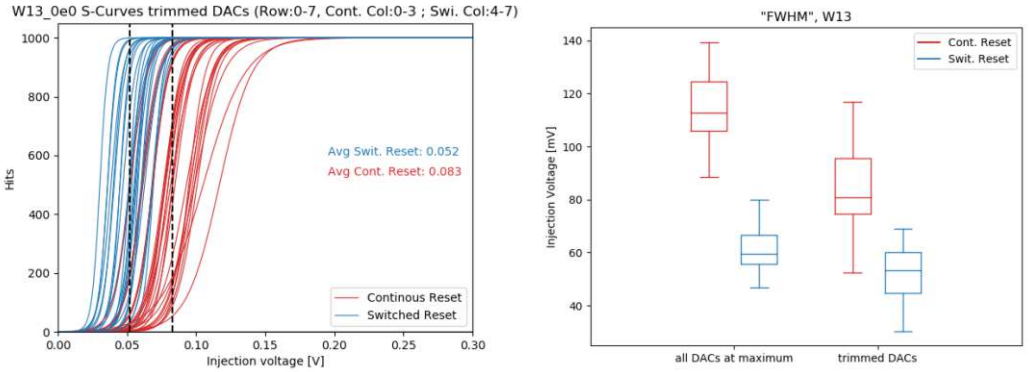



Figure 6.6: Workflow for automatic TRIMDAC adjustment for a single pixel.




(a) S-curves

(b) FWHM comparison between untrimmed and trimmed DACs

Figure 6.7: S-curve measurement with adopted TRIMDAC values with unirradiated chip from wafer 13 and comparison with S-curve measurement from unadopted chip.

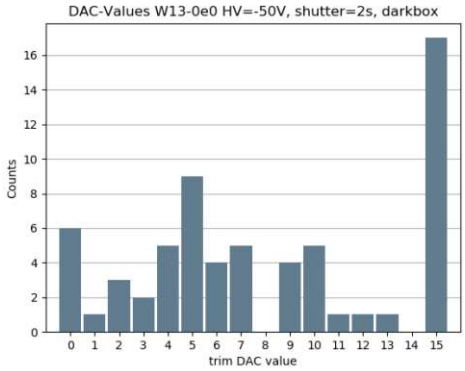
CR-pixel is significantly higher than for the CR-pixel. The spread of the S-curves with the trimmed DACs even slightly increases.

## 6.5 Open Shutter Measurement

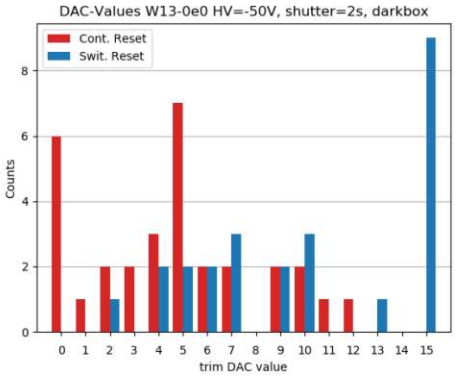
Now that the basic functionality of the analog pixel readout electronic has been confirmed, the entire circuit was tested with real particles. For this, a radioactive strontium-90 source ($^{90}$Sr) with 10 mCi / 370 MBq (figure 6.8) was used, which was placed on the


Figure 6.8: $^{90}$Sr source with 10 mCi / 370 MBq used for open shutter measurements.

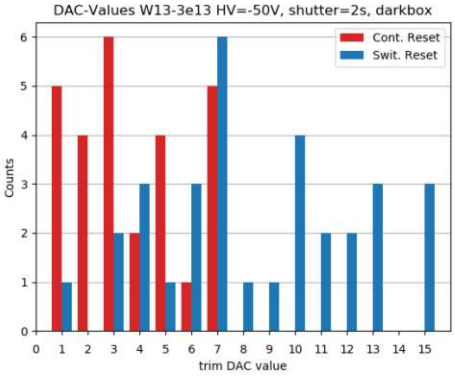
foreseen holder ((3) in figure 6.1). The detector was just below the hole of the source holder. This way, the source was about 2 cm above the chip, with an additional acrylic glass in between. For the measurement, the shutter of the chip is opened for a specific time. After that, the buffer of the detected hits is read out.
Since the signal is coming from the depleted p-substrate of the detector, the switch for the injections must be open (figure 3.5). For this measurement, again three separate chips from the wafer 13 ($> 2.2\,\mathrm{k\Omega \cdot cm}$) were used. One of them was irradiated, the other two were not. To deplete the substrate, an HV of $-50\,\mathrm{V}$ was applied.



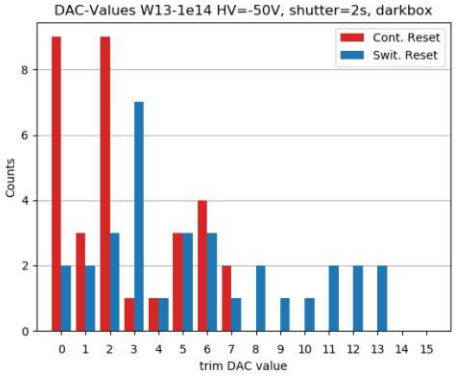

(a) Unirradiated (pixel flavor not distinguished and containing noisy pixel)




(b) Unirradiated




(c) $3 \cdot 10^{13}\ n_{\mathrm{eq}}/cm^2$




(d) $1 \cdot 10^{14}\ n_{\mathrm{eq}}/cm^2$

Figure 6.9: Adjusted TRIMDAC values for all pixels from the unirradiated (a-b) chip and the irradiated chips (c-d) from wafer 13, with a shutter time of 2 s and an HV of $-50\,\mathrm{V}$.

### 6.5.1 Trimdac Adjustment

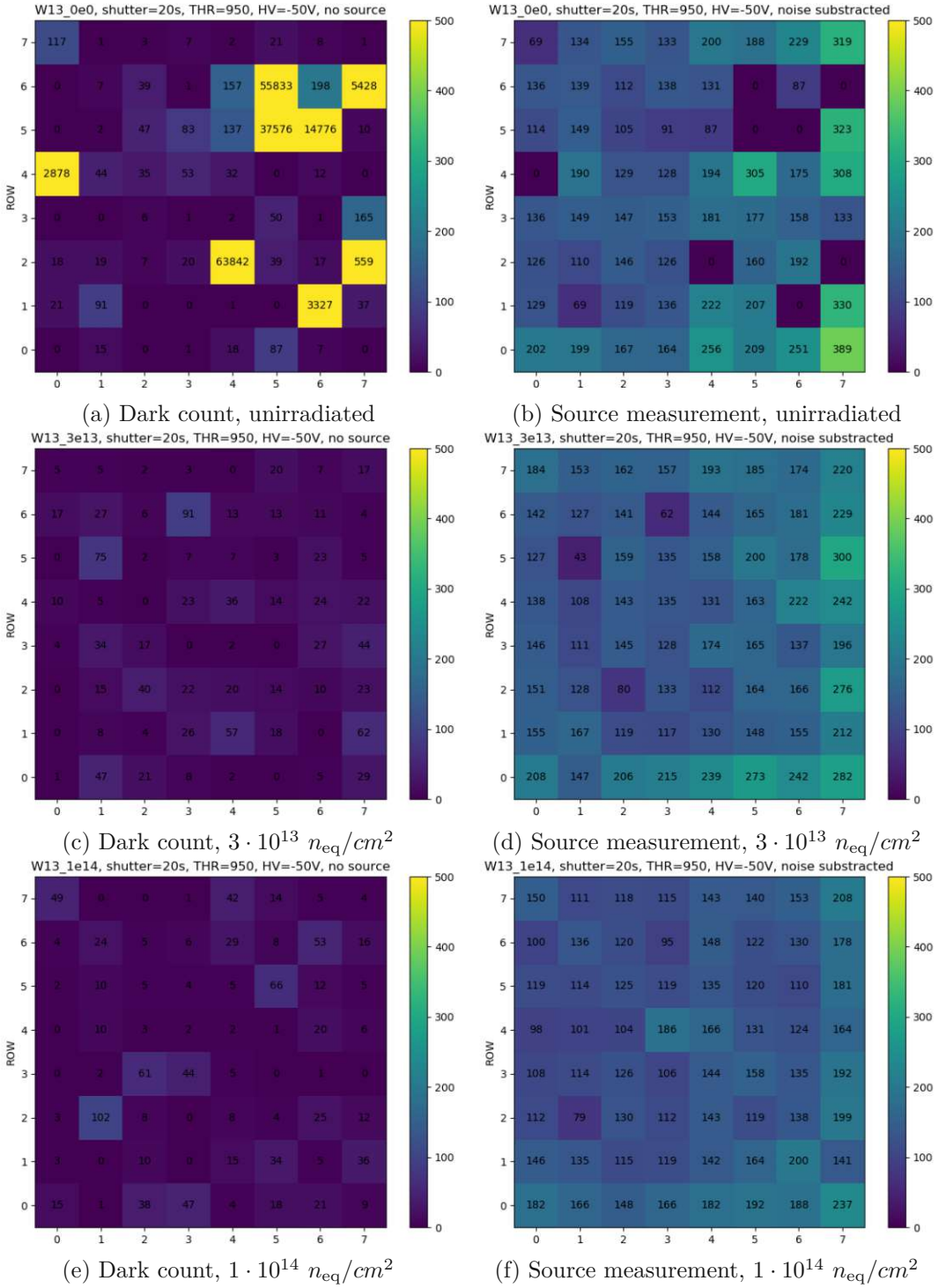
Before starting with the measurement, the TRIMDAC values of the chip were adopted with the automatic TRIMDAC adjustment, already introduced in section 6.4.2. The shutter was open for 2 s. As can be seen in figure 6.9a, a high peak occurs at the highest TRIMDAC setting. This can be traced back to the noisy pixels (figure 6.10a), which still generate countless hits even at the highest possible threshold. Therefore, these pixels are masked in the further plots and measurements. In addition, also CR- and SR-pixels are distinguished, since the pixel behave quite differently depending on the used reset-technology. Looking at the TRIMDAC settings of the unirradiated (figure 6.9b and irradiated (6.9c & 6.9d) chips, the values for the CR-pixels are smaller than for the SR-pixels. The remaining large peak at the highest TRIMDAC setting results from moderately noisy pixels. The expectation that irradiated chips have a higher noise, which would lead to higher TRIMDAC values, is not confirmed. The explanation for this could be the sample variation of the different chips. Also, the distribution within a pixel-reset type should be Gaussian-shaped, which is probably not evident because of the low statistics.

### 6.5.2 Dark Count Measurement

Another thing to do, before getting started with the actual source measurements is the dark count measurement, without a radioactive source. Since the automatic TRIMDAC adjustment is performed in such a way that a few noise hits are detected (for better sensitivity), this noise had be determined for the planned shutter time of 20 s. The dark counts were subtracted from the source measurements to account for the noisy pixels.
For the unirradiated chip, there are multiple noisy pixels (figure 6.10a) that were masked in the following measurements. Other than that, there is no significant difference between the unirradiated chips and the irradiated chips (6.10c & 6.10e).

### 6.5.3 Radioactive Source Measurement

The actual open shutter measurement was conducted with the radioactive source ($^{90}$Sr, 10 mCi) on top of the sensor. The shutter time was 20 s, as in the dark count measurement before. The noise of the dark count measurements was subtracted. The maximum of the scale for the hitmaps of dark count measurements as well as the source measurements is 500, to make the plots comparable with each other.
In the hitmap of the source measurement with the unirradiated chip (6.10b), the noisy pixels are masked. For all hitmaps, there is an increase of hits towards the right and the bottom border visible, like a mirrored L-shape. These more sensitive regions may come from layout effects of the detector. With increasing the fluence (figure 6.10d & 6.10f), the hitmaps are getting darker and darker, which means fewer hits are detected. This behavior is expected and will become even clearer with the following measurement resulting in figure 6.11.
For multiple HVs (10 to 100 V) the average number of hits for one half of the matrix




(a) Dark count, unirradiated

(b) Source measurement, unirradiated

(c) Dark count, $3 \cdot 10^{13}$ $n_{\mathrm{eq}}/cm^2$

(d) Source measurement, $3 \cdot 10^{13}$ $n_{\mathrm{eq}}/cm^2$

(e) Dark count, $1 \cdot 10^{14}$ $n_{\mathrm{eq}}/cm^2$

(f) Source measurement, $1 \cdot 10^{14}$ $n_{\mathrm{eq}}/cm^2$

Figure 6.10: Hitmaps of dark count measurement (a, c and e) and hitmaps of source measurement (b, d, f) for unirradiated and irradiated chips from wafer 13, with a shutter time of 20 s and an HV of −50 V.


Figure 6.11: Average number of hits per HV, distinguished by pixel flavor for unirradiated and irradiated chips from wafer 13, with a shutter time of 20 s.

(SR- and CR-pixel) was measured and plotted for chips irradiated with different fluences. For this measurement, no noise was subtracted since it doubles the measurement time but results only in a small correction effect.
As expected, higher voltages result in more hits for all detectors and pixel reset types. In general, there are more hits for SR-pixels than for CR-pixels due to the lower threshold, already visible in section 6.3.1. For both pixel reset types, fewer hits for higher fluences are visible. In addition, it appears that CR-pixels are less affected by fluence than SR-pixels. However, this is not certain, since there are many masked noisy pixels in the unirradiated SR-pixels. More statistics would be needed to confirm this statement.

CHAPTER 7

# Proton Beam Measurements

Now that the basic functionalities have already been successfully confirmed in the laboratory, further tests were carried out using a proton beam at MedAustron [36]. This is a medical particle accelerator close to Vienna. In the first testbeam, the linearity of the detector was checked and a relative efficiency was measured. In the second test beam and attempt was made to integrate the detector into a higher-level DAQ system with a telescope and thus track individual particles. In addition, the energy of the particles were determined by means of a ToT measurement.

## 7.1 Linearity Measurement

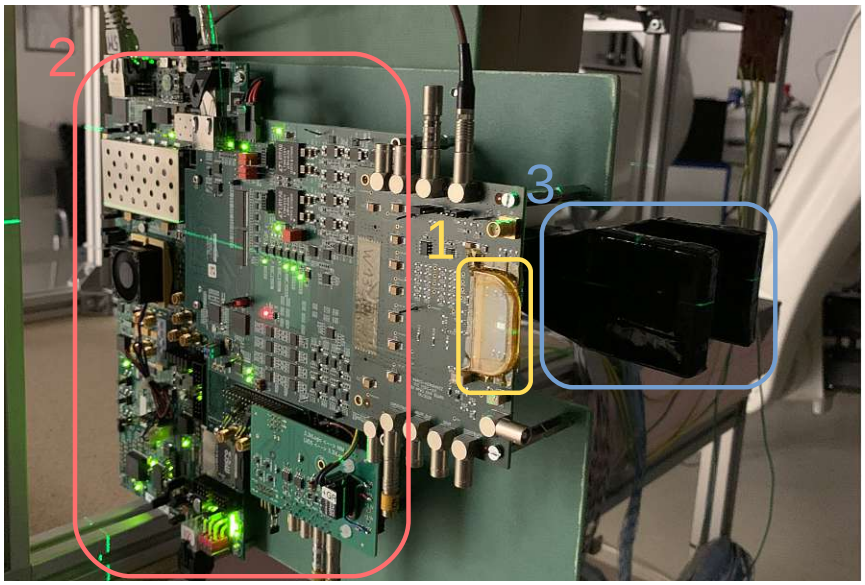
In the first testeam, the relative efficiency was determined by measuring the hits of a single pixel of the MPW2 and additionally the total number of hits by means of two scintillators. The scintillators detect most of the particles of the beam, whereas the MPW2 with its small dimensions ($60\,\mu m \times 60\,\mu m$) detects only a fraction of them. For this measurement, a chip from the wafer 13 ($> 2.2\,k\Omega \cdot cm$) was used.

### 7.1.1 Setup for First Testbeam

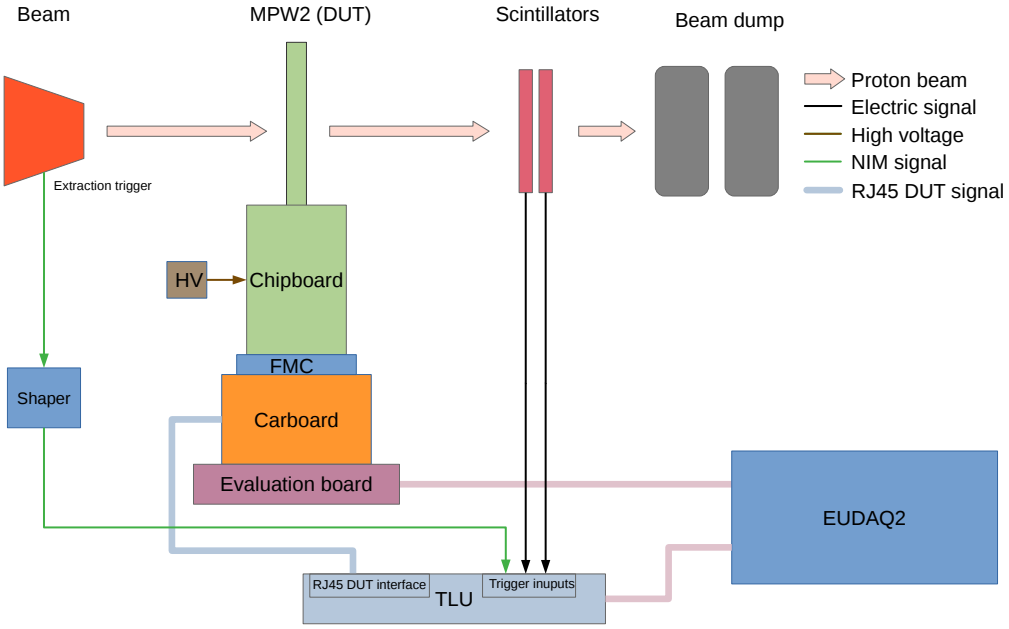
The hardware setup for the first testbeam is visible in figure 7.1a. The MPW2 chip (1) together with the two scintillators (3) is aligned along the beam with the help of the green laser. The MPW2 chip sits on the chipboard, which is operated by the CaRIBOu hardware-setup (2). To get a better understanding of the whole setup, there is a block diagram of the whole setup in figure 7.1b.

### 7.1.2 Measurement Process

$4\,\mu s$ before the spill of the beam arrives at the setup, a start extraction trigger is sent by the accelerator. This trigger is shaped and then captured by the *Trigger Logic Unit*




(a) Setup for the first testbeam with the CaRIBOu setup and additional scintillators in the back




(b) Block diagram of the setup for the first testbeam with the respective connections between the single components

Figure 7.1: Setup for the first testbeam.

(TLU) and passed on to the firmware on the FPGA over the CaR board. With this signal, the shutter of the MPW2 is opened for 5 s, which is approximately the length of the spill. When the shutter closes, the falling edge of the signal is detected by Peary. The detected hits during the current spill are read out the same way as in section 6.2 with the firmware for the standalone operation (figure 6.2). The detected spills are stored one after the other with the corresponding TS, spill number, pixel information (row/column) with the configured TRIMDAC value and the number of detected hits. In parallel, the number of total hits resulting from coincidences of the two scintillators in the TLU are detected for each spill. Using EUDAQ2, the hits per spill together with the corresponding TS are also stored in a file on the host computer where EUDAQ2 is running. The run control of EUDAQ2 is handling the whole DAQ-process with the caribou-producer on the evaluation board, as well as with the control of the TLU.
Regarding the used beam, this measurement was performed with two different "low flux"-settings. One setting with a rate of 2.2 MHz, the other with 400 kHz. For both settings, the energy was 252.7 MeV with a spot size around 7 mm.

### 7.1.3 Trimdac Adjustment

Before starting with the measurement, the TRIMDAC values had to be adjusted to the new condition at the test beam facility. This was again performed as described in section 6.4.2. The shutter time of 5 s had the same as the length of the spill. The substrate was depleted with an HV of −80 V. As expected, the TRIMDAC values for CR-pixels are smaller than for software-reset pixels (figure 7.2). For the TRIMDAC values of the CR-pixels, there is a peak at the lower border of the scale, so for these pixels in the 5 s

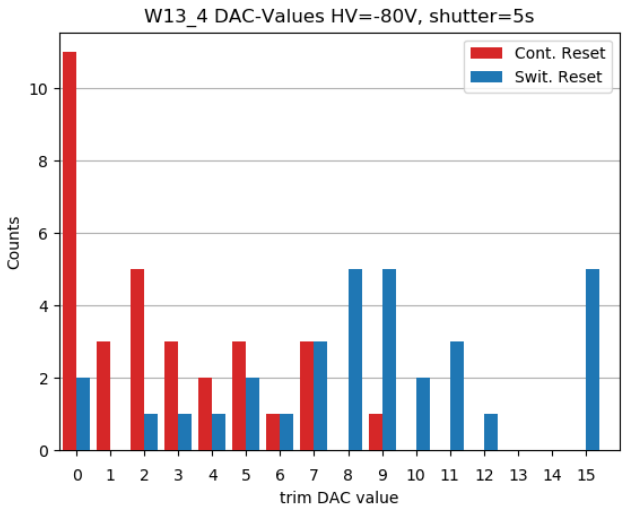
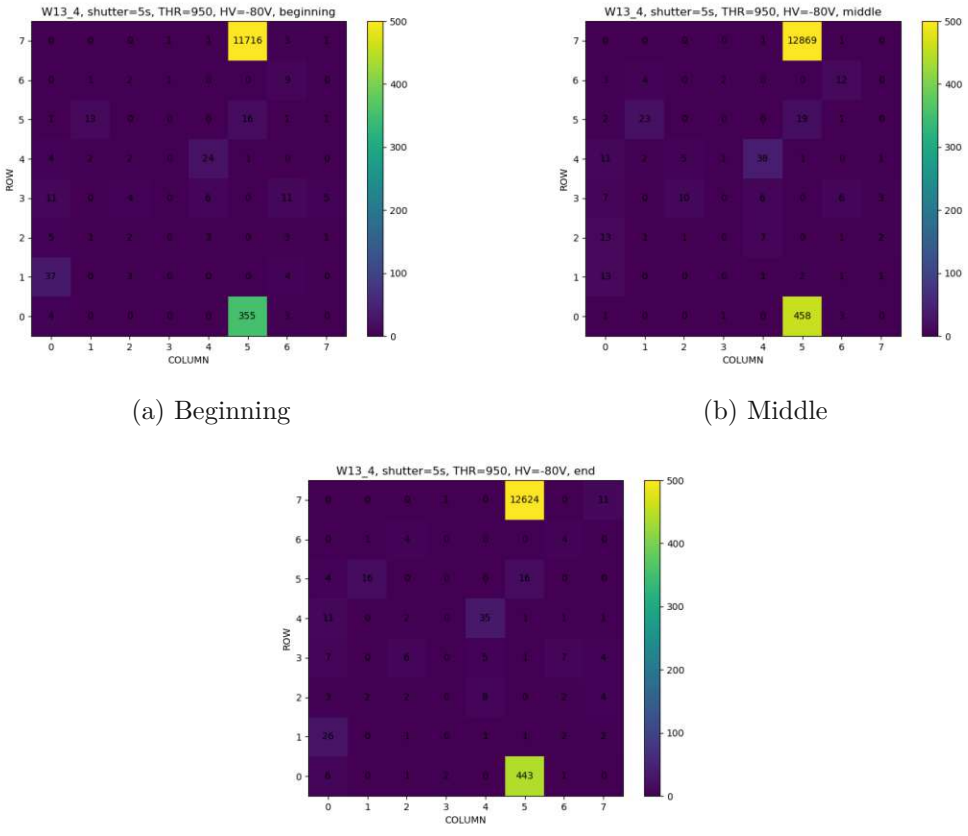



Figure 7.2: Adjusted TRIMDAC values of all pixels for the linearity measurement with an unirradiated chip from wafer 13, with a shutter time of 5 s and an HV of −80 V.

no noise hits were detected at all. With a wider range of TRIMDAC values, sensitivity could be increased for these pixels.

### 7.1.4 Dark Count Measurement

Before the measurement is started, the noise accumulated in the 5 s is determined. This measurement is also performed with an HV of −80 V. To get a feeling for the influence of the irradiation with protons on the noise of the sensor, the dark count measurement was repeated in the middle and at the end of the test beam. The collected plots can be found in figure 7.5. In the course of the test beam, the noise remains pretty much the same. At the half of the SR-pixels, two noisy pixels are detected, which have to be considered in the further course of the measurement.




(a) Beginning

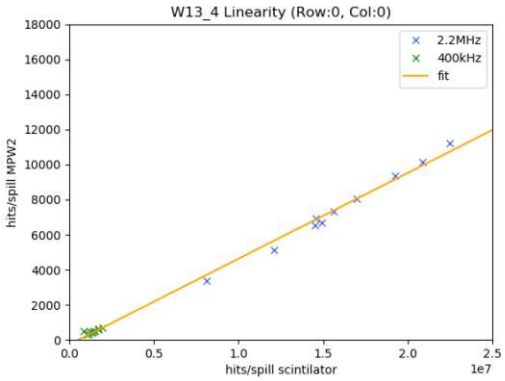
(b) Middle

(c) End

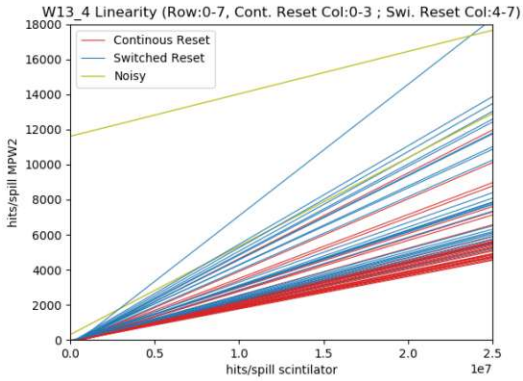
Figure 7.3: Hitmaps of the dark count measurement in the course the testbeam, with a shutter time of 5 s and an HV of −80 V.

### 7.1.5 Linearity Measurement with Different Particle Rates for All Pixels

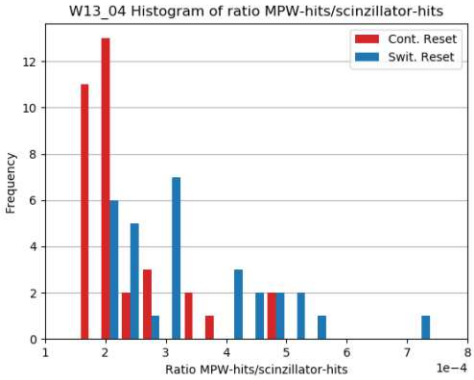
For the actual linearity measurement, the substrate of the detector was depleted with an HV of −80 V. For every single pixel, 20 spills with a length of about 5 s were measured. 10 spills were measured with the 400 kHz beam setting and 10 spills with the 2.2 MHz beam setting. All the hits from one spill are accumulated with the MPW2 and the scintillator.
The hits per spill detected by a single pixel of the MPW2 are plotted as a function of the hits per spill on the scintillators, as can be seen in figure 7.4a. As expected, much fewer hits are detected with the MPW2 than with the scintillator, but the ratio always remains the same at different rates. This confirms the linear behavior of the MPW2 detector. The




(a) Hits per spill from MPW2 vs. hits/spill from scintillator and an associated fit for a single pixel




(b) Linear fits for hits per spill from MPW2 vs. hits/spill from scintillator for all pixels



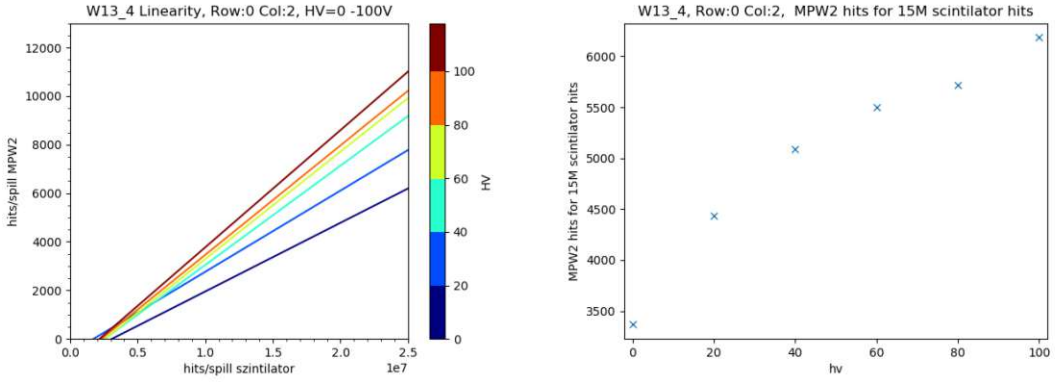

(c) Histogram of the ratio MPW-hits/scintillator-hits

Figure 7.4: Linearity measurement with two different beam rates for unirradiated chip from wafer 13, with an HV of −80 V.

two rate settings can be easily distinguished, with the measurement points of the lower rate collected in the lower range. The measurement points of the 2.2 MHz setting are widely scattered, indicating a high standard deviation of the rate. In normal operation, this is not desirable, but for the linearity measurement, this is beneficial because several points in different regions are available for the linear fit.
In figure 7.4b, the linear fits for all pixels are plotted, distinguished by the flavor of the pixel. The two noisy pixels are also included but marked as such.
The information of the plot can now be displayed more clearly by putting the slope of the curves, i.e. the ratio of MPW-hits/spill per scintillator-hits/spill, into a histogram (figure 7.4c). The more sensitive the pixels, the further to the right they are located in the plot. The CR-pixels detect fewer hits than the SR-pixels and are therefore less sensitive. This confirms the statement already made in the source measurements (6.5.3).

### 7.1.6 High Voltage-Scan

This measurement was used to determine the influence of different HVs on the sensitivity of a single pixel. For this purpose, the HV was ramped from 0V to 100V in 20V steps. At each step, the linearity measurement was performed using the two different beam settings.
In figure 7.5a, the MPW2 hits/spill in dependence of the scintillator hits/spill are visualized again. With increasing HV, the linear curves become steeper and thus the sensitivity of the pixel improves. This behavior is expected due to the increased depletion of the substrate.
To get a better understanding of the increasing sensitivity, in figure 7.5b the number of MPW2 hits is plotted, which is needed to get 15 M scintillator hits, depending on the HV. The curve looks basically fine, but there is no satisfying explanation for the dip at




(a) Linear fits of hits per spill from the MPW2 vs. hits/spill from the scintillator

(b) Acquired MPW2 hits for 15 M scintillator hits for a single pixel, as a function of the HV

Figure 7.5: Linearity measurement depending on various applied HVs for unirradiated chip from wafer 13.

80 V. If the number of hits at 100 V would be at around the same level as at 80 V, this could indicate the complete depletion of the substrate. However, this is not the case.

## 7.2 Waveform and Tracking Measurement

In the second testbeam, tracking of incoming protons was performed with the help of 4 *Double Sided Strip Detectors* (DSSDs) and a customized trigger setup. In addition, the waveforms of incoming protons were detected. This was realized with an external picoscope, as well as with the internal CaR-board ADC. In addition, the ToT was measured with an internal FPGA and compared with the measured curves. This testbeam was performed with a chip from wafer 13 ($> 2.2\,\mathrm{k\Omega \cdot cm}$).

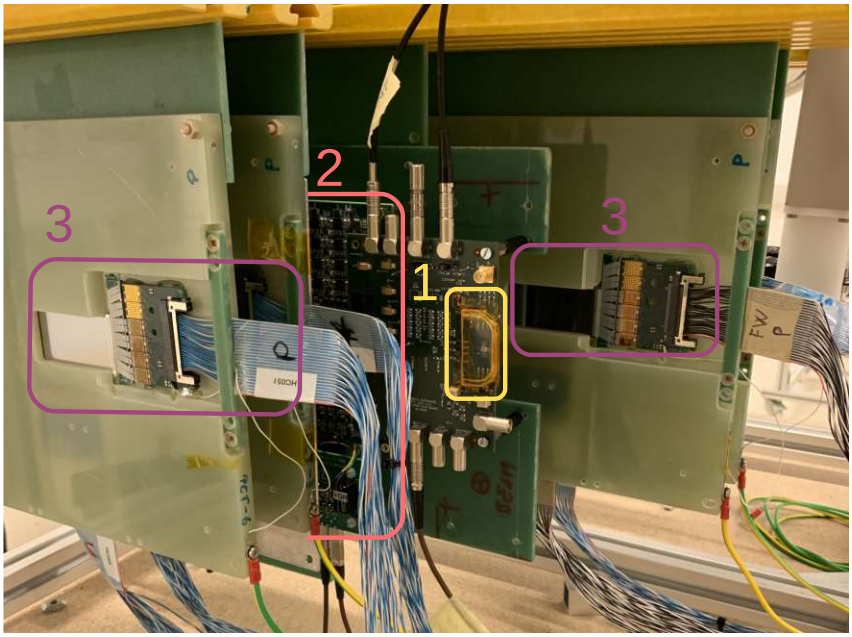
### 7.2.1 Setup for Second Testbeam

In figure **??**, the physical setup for the second testbeam is visible. The MPW2 (1) sits on the chipboard, which in turn is connected to the partially visible CaRIBOu hardware-setup (2). For the tracker planes (3), *Double Sided Strip Detectors* (DSSDs) are used. The orthogonally aligned strips of the DSSD on the n-side have a pitch of 100 µm, on the p-side a pitch of 50 µm. The two strip detectors together cover an area of 2.56 cm × 5.12 cm and are 300 µm thick. The strip detectors are read out on both sides with the help of 4 APV25 chips and an associated *Versa Module Eurocard*-based (VME-based) flash ADC (FADC) system. More information about the tracker setup can be found in [37]. Two DSSDs are placed upstream and two DSSDs are placed downstream of the MPW2 (DUT). In this image, they are not yet aligned together with the MPW2 along the beam. In the back (not visible) there are additionally two scintillators. To get a better idea of the setup, you can find a block diagram in figure 7.6b. In addition to the setup of the first testbeam, desired *Nuclear Instrumentation Standard* (NIM) signals can be fed in and out via LEMO connections using a breakout board.

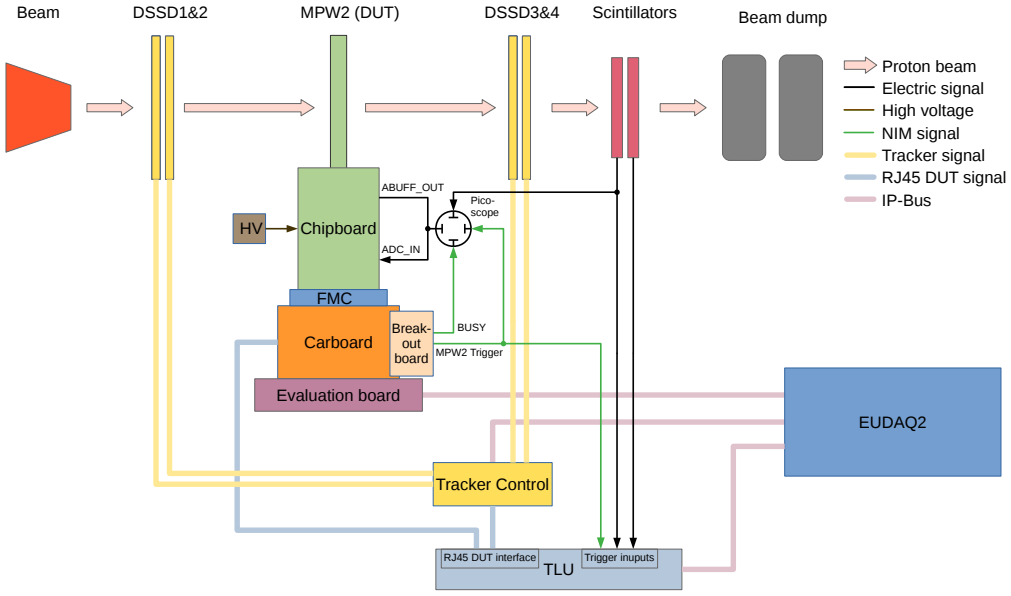
### 7.2.2 Measurement Process

The MPW2 detects a particle hit via an edge detection in the firmware of the FPGA. This generates a 5 ns long NIM signal (MPW2 trigger) which is sent from the breakout board to a trigger input of the TLU. The signal is also fed into the picoscope. Also, the trigger signals from the two scintillators are connected to the trigger input of the TLU. Here a superior trigger decision is made, either a *2-way coincidence* only with the scintillators or a *3-way coincidence* additionally with the MPW2. The tracker planes are not included into the trigger decision. The trigger decision, together with the trigger number and the clock signal, is then forwarded to the tracker control and the CaR-board via the RJ45 DUT signal.

Within the tracker control the hits of the triggering particles are detected at the 4 DSSD boards and stored in a file with the respective configuration file on a hard disk.




(a) Setup for the second testbeam with the CaRIBOu setup between 2 pairs of DSSD tracker planes.




(b) Block diagram of the setup for the second testbeam with the respective connections between the single components

Figure 7.6: Setup for the second testbeam.

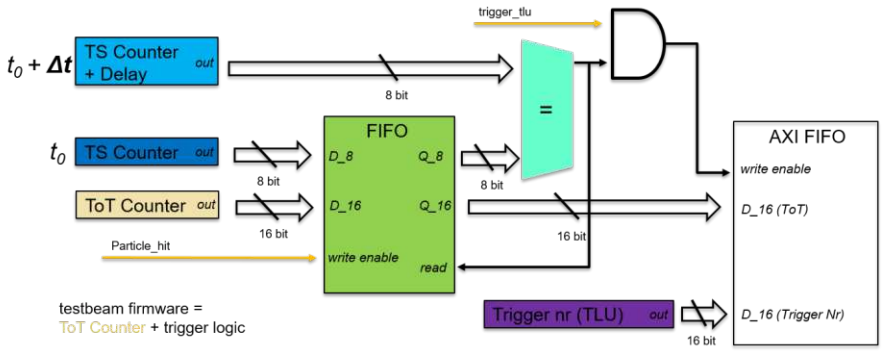
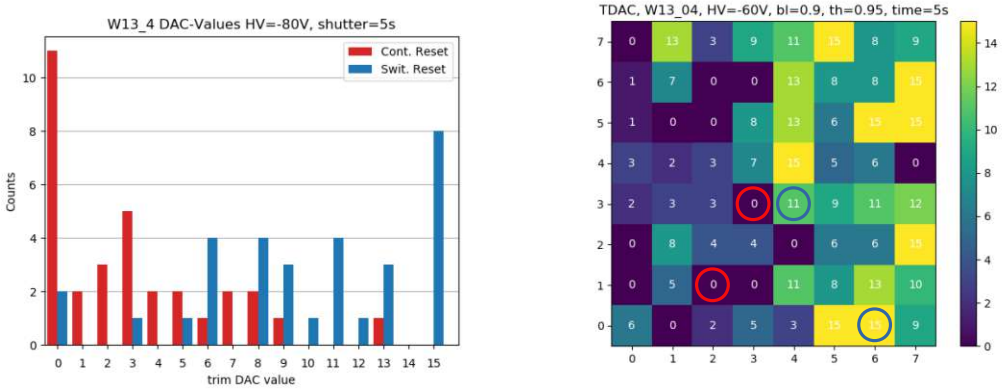



Figure 7.7: Firmware for testbeam operation of the RD50-MPW2 chip [35].

At the MPW2 the handshake is performed using a busy line. The FPGA raises this busy line until the trigger number is stored. The busy line connected to the picoscope via the breakout board is used to trigger the waveform measurement. To capture the waveform with the picoscope, the ABUFF-output is monitored with the picoscope and fed back into the ADC-input. This input is routed over the FMC-connector to an ADC sitting on the CaR-board. There are two ways of operating this setup, depending on the kind of the superior triggering.

- When using the *3-way coincidence*, the MPW2-Trigger can easily be assigned to the overall trigger of the TLU by the FPGA, since it is part of the trigger decision itself. So the particle that triggered the scintillators also went through the MPW2.
- With the *2-way coincidence*, only the two scintillators are used for the trigger decision. Thus, also all particles are detected, which did not pass the MPW2 pixel. Now it must be determined whether at time $\Delta t$ earlier, a particle was detected with the MPW2 or not. If yes, a superior trigger number of the TLU can be assigned to this particle.

This process is made clearer by the functionality of the firmware for testbeam operation (figure 7.7). If a particle is detected with the MPW2 pixel, the ToT value which originates from the standalone firmware is written into a FIFO. In addition, the TS of an internal counter is forwarded and compared with a second counter delayed by $\Delta t$. So after a time $\Delta t$ these counters match exactly and the 16-bit TOT value is passed to the AXI fifo. However, this value is only really read into the FIFO if a superior trigger of the TLU is also detected within a certain time window, realized with an AND Gate. If this is the case, the corresponding superior trigger number is also read into the AXI FIFO. This buffer is read out by the DAQ software Peary and written into a file. The entire process is handled by the run control of EUDAQ2 connected with the caribou-producer on the evaluation board, the TLU and the tracker control.
Regarding the used beam, this measurement was performed with a "low flux"-settings with a rate around 3.5 MHz with a spot size of 3 cm. The energy of the beam was




(a) Histogram with TRIMDAC values

(b) Color map with TRIMDAC values and marking of measured pixels

Figure 7.8: Adjusted TRIMDAC values for the waveform- and the tracking measurement with chips from wafer 13, with a shutter time of 5 s and an HV of −80 V.

ranged between 60 MeV and 800 MeV for the waveform measurement. For the tracking measurement an energy of 250 MeV was used. More information about the beam structure can be found in [38].

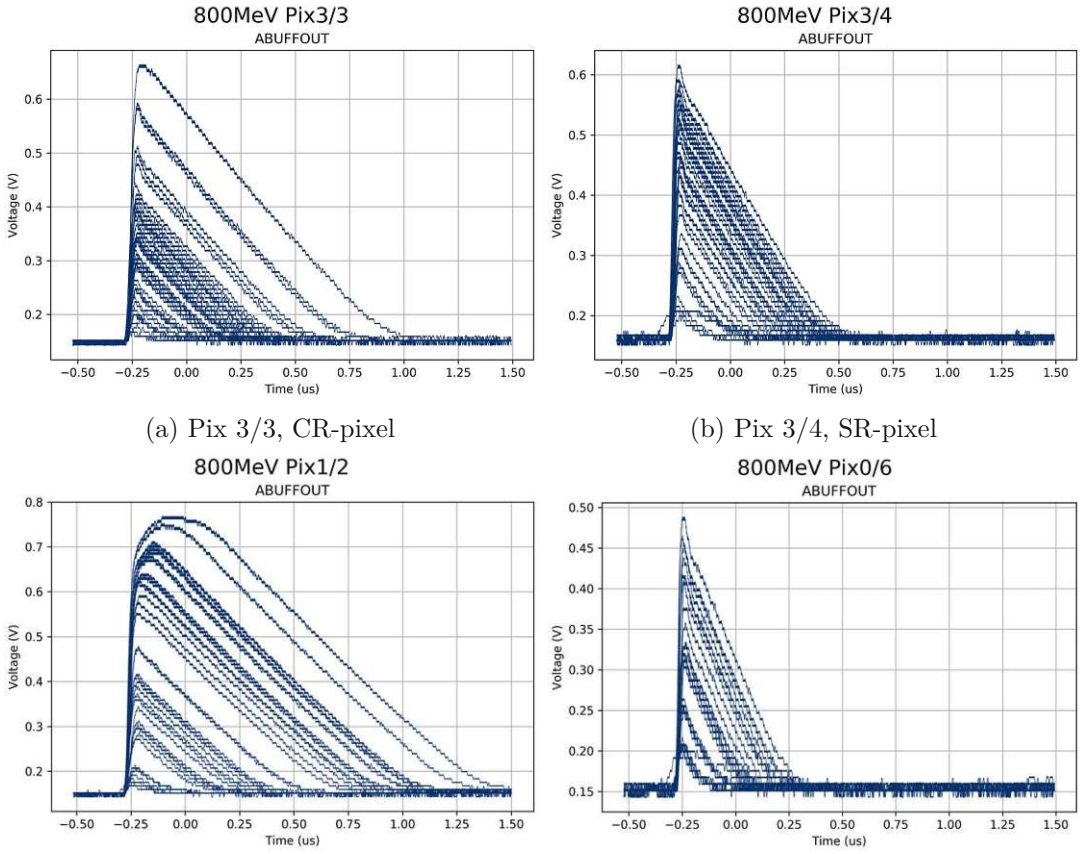
### 7.2.3 Trimdac Adjustment

Before starting with the measurement, the TRIMDAC values were adjusted to gain the maximum sensitivity of the chip. This was again performed with the automatic TRIMDAC adjustment already explained in section 6.4.2. The substrate was depleted with HV=−60 V to make the measurement comparable with the simulation for which the same HV was used.
As expected, the smaller TRIMDAC values are obtained for the CR-pixels and the larger ones for the SR-pixels (figure 7.8a). Since the pixel position and the corresponding TRIMDAC value are important for this measurement, the corresponding TRIMDAC values are plotted in a color map in figure 7.8b. The pixels used in later on measurements are marked with circles. The difference between the two pixel flavors is also clearly visible here (left half with CR-pixels, right half with SR-pixels).

### 7.2.4 Measurement with Picoscope and CaR-Board ADC

The measurement was used to obtain the waveform of the incoming particles (ABUFF_OUT) and also measure the energy by determining the ToT. The waveforms were captured with two different devices, the picoscope and the CaR-board ADC. The picoscope has the advantage of capturing the whole amplitude, which is not possible with the ADC on the CaR board. However, because of the high measurement rate, the CaR-board ADC can record many curves in a short time. As in the simulation, −60 V was used as HV.

In the first measurement (figure 7.9), the picoscope detected around 20 waveforms per measurement for different pixels with different flavors. When comparing the waveforms of the CR-pixels (7.9a & 7.9c) with those of the SR-pixels (7.9b & 7.9d), a clear difference becomes evident. In the SR-pixels, the discharge of the capacitor with the higher current is visible by the abrupt and steep descent of the curve. For the CR-pixels, a smooth transition into the discharge process is evident. This is also consistent with the simulations shown in figure 3.7. When comparing 7.9a with 7.9c and 7.9b with 7.9d, there is quite some variation in the length of the Pulse (ToT) within a pixel flavor. The difference between pixel 3/4 and pixel 0/6 could be explained by the different TRIMDAC values (11 and 15), but for pixel 3/3 and pixel 1/2 they are the same (0 and 0). The expectation that the curves would concentrate at a certain energy, and thus have a similarly equal ToT, within a pixel did not turn out to be true. On the contrary, the curves are quite continuously distributed over a certain energy range.
This could possibly be explained by the fact that the particles do not penetrate straight



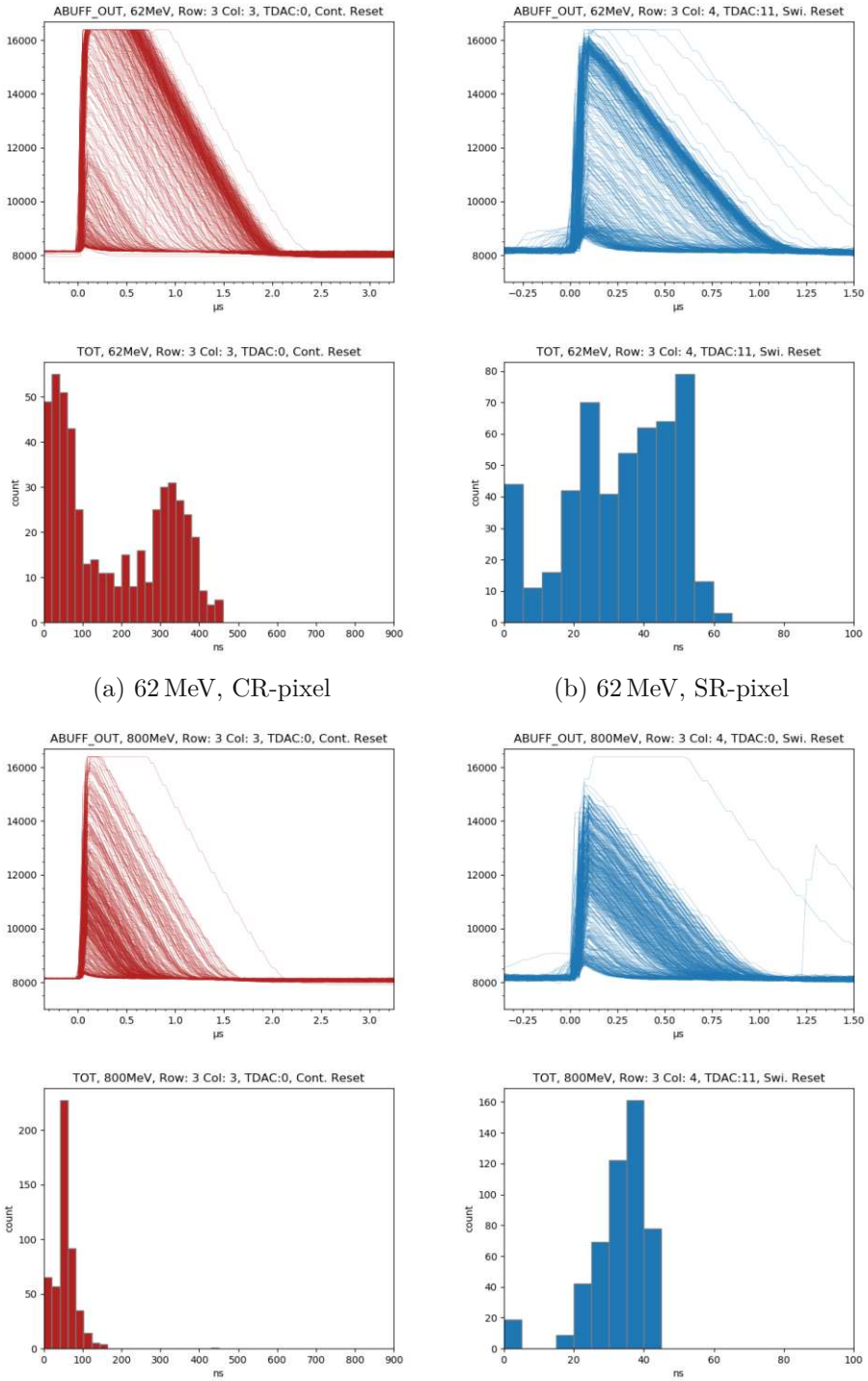

(a) Pix 3/3, CR-pixel

(b) Pix 3/4, SR-pixel

(c) Pix 1/2, CR-pixel

(d) Pix 0/6, SR-pixel

Figure 7.9: Waveform measurement of $\sim$ 20 waves with energy of 800 MeV for different pixels with chips from wafer 13, with an HV of $-80$ V.




(a) 62 MeV, CR-pixel (b) 62 MeV, SR-pixel

(c) 800 MeV, CR-pixel (d) 800 MeV, SR-pixel

Figure 7.10: Waveform and ToT measurement of 500 waves for 62 MeV and 800 MeV for every pixel flavor with chips from wafer 13, with an HV of −80 V.

through the depletion zone, but at an angle to the detector surface and thus emit a different energy contribution. But since the energy is quite high, the angles are small and therefore the effect should be negligible. Another explanation could be the landau energy loss distribution occurring at thin absorbers, where the energy is not equally distributed [39].
In the second measurement, 500 waveforms per energy were recorded for one pixel per flavor using the ADC on the CaR board. In addition, the internal ToT of COMPOUT_BUF was also measured for each recorded waveform, as already described in section 6.2. The energy was varied between 62 MeV and 800 MeV.
When looking at figure 7.10, it is evident that the measured internal ToT is shorter than the ToT of the recorded curves coming from the ABUFF_OUT. This is expected and can be explained by the parasitic capacitance, which is added for the ABUFF_OUT, which is also the case in figure 3.7. So the length of the curves measured with ABUFF_OUT have only a qualitative and no quantitative value.

Apart from this factor, however, the histogram seems to match the curves regarding the distribution of the ToT values. For 62 MeV, at the maximum ToT value ($\sim 2\,\mu s$ for CR-pixel and $\sim 1.1\,\mu s$ for SR-pixel), the curves appear to densify. For the higher energy, the densest region of curves is not at the maximum anymore. When comparing the peak of the internal ToT distribution of the 800 MeV SR-pixel histogram (ToT$\approx 35ns$) with the ToT value from the simulation from figure 3.6b (ToT$\approx 30ns$), the values agree reasonably well. Measurements with energies between those already shown, can be found in the appendix A.1.

### 7.2.5 Tracking Measurement

Since the MPW2 can only read one pixel at a time, the tracking measurement was only performed for a single pixel (row=3, column=4). The detector was again depleted with an HV of $-60$ V. To perform the tracking analysis, 3 different measurements were conducted:

- In the first *alignment run* (500 M events), the DUT (MPW2 detector) was not included in the beam. Only the coincidence of the 2 scintillators was used for the trigger decision in the TLU. This data was used for the alignment of the tracker planes in the x- and y-direction.

- In the second *window run* (10 k events), the MPW2 was set up as shown in figure 7.6b between 2 DSSD planes along the beam. In this measurement, the data is acquired using a *3-way coincidence*, as already described in section 7.2.2. This data was used for the alignment of the DUT and for the later window scan.

- In the final *tracking run* (8 k events), the DUT was placed the same way as in the window run. Only this time, during the measurement, the data was recorded using the *2-way coincidence*. This data was used to attempt real tracking.

The analysis of the data was conducted with the reconstruction software tool corryvreckan [40]. The data from the *alignment run* and the geometry data of the setup, consisting of y-distances between the detectors along the beam, was used to perform the prealignment and alignment of the telescope. This alignment looks reasonable. The alignment of the DUT by means of the *window run* data is unfortunately not satisfying, since probably too few data was recorded. The following analysis was performed anyway.
With the *window run* data as well as with the *tracking run* data, an attempt was made to perform an efficiency analysis. Unfortunately, the analysis did only work out for the *window run* data. This way, no real efficiency analysis is possible, because all particles have inevitably passed through the MPW2 and thus the efficiency is always 100 %. However, the efficiency measurement of the *window run* data could be modified in such a way, that a useable output could still be obtained.

In figure 7.11, the result of the *window scan* can be seen. During the entire measurement, always the hits of the same, fixed pixel (row=3 column=4, bordered in red) were measured. In a single analysis only the tracks are counted, which occur in a certain 3×3 *Region of Interest* (ROI) (e. g. green rectangle) and thereby trigger a hit in the pixel R3 C4. The number of the determined tracks is then entered into the middle pixel (green circle) of the ROI. Now this analysis is executed for all pixels. For the edge pixels, the area is reduced to a 2×3 ROI and in the corner only a 2×2 ROI is evaluated.
When looking at the plot, the measured pixel R3 C4 contains the maximum number of hits. The further away the ROI was set, the fewer hits were detected in the measured pixel. However, a clear difference is evident at the boundary (dashed orange line) of the

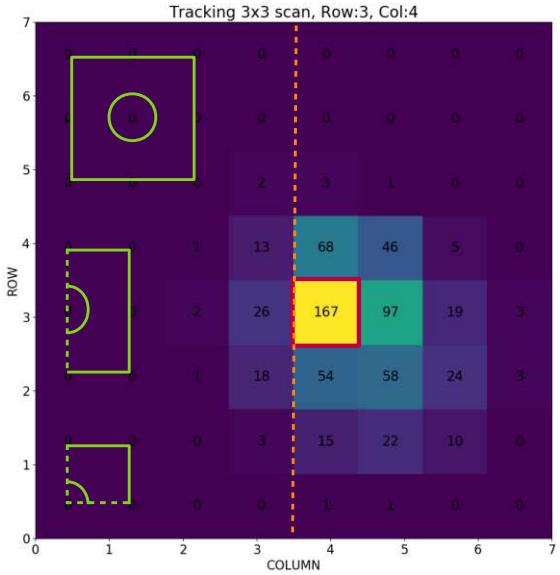



Figure 7.11: 3×3 Window scan for pixel row=3 and column=4.

two pixel flavors[1]. The CR-pixels appear to have significantly less charge sharing than the SR-pixels. In addition, the increased hits towards the right and bottom boundaries may be related to the mirrored L-shape artefact that occurred already during the radioactive source measurement in section 6.5.3.

[1] Column 0-3 → Continuous Reset; Row 4-7 → Switched Reset

CHAPTER 8

# Summary & Conclusion

In the course of this work, the sensor prototype RD50-MPW2 was integrated into the CaRIBOu DAQ system. For this purpose, a device was included in the DAQ software Peary and also a detector-specific firmware was realized. Since the reference distribution Poky was updated to a new branch during the project, the corresponding Peary software was also updated. In order to be able to use the device with the latest version of Peary, it has to be adapted to it. This system works in stand-alone mode in the lab and by integrating it into the higher level EUDAQ2 environment, it can also be used in a test beam environment in combination with multiple detectors.

By using a radioactive $^{90}$Sr source, the detector was tested using real particles. Here, as expected, a slightly reduced sensitivity was found for higher irradiated chips. However, CR-pixels seemed to be less affected by radiation than SR-pixels. To verify this claim, however, more statistics would be needed. In general, increased sensitivity was found at higher applied voltages. At the right and the lower edge of the chip an increased sensitivity was observed, which may be explained by layout effects of the sensor. This can be taken into account in the development of a further detector.

At MedAustron, the chip and two reference scintillators were exposed to a proton beam. This demonstrated the linear behavior of the chip. As in the laboratory measurements, the SR-pixels were more sensitive than the CR-pixels. Also, the higher sensitivity at higher applied HVs was evident, but at $\sim$80 V a small dip occurred which cannot be explained properly. This would need further investigation by measuring other pixels. In the course of the testbeam of 8 h, there was no noticeable deviation from the basic noise.

At the second testbeam, the waveforms of incoming protons were captured via the analog buffer output by an external picoscope and the internal CaR-board ADC. The ToT of the internal waveform signal was measured with the firmware. The setup was established together with a telescope consisting of two pairs of DSSDs to enable tracking. Looking at the waveforms, an apparent difference between SR-pixel and CR-pixel was found

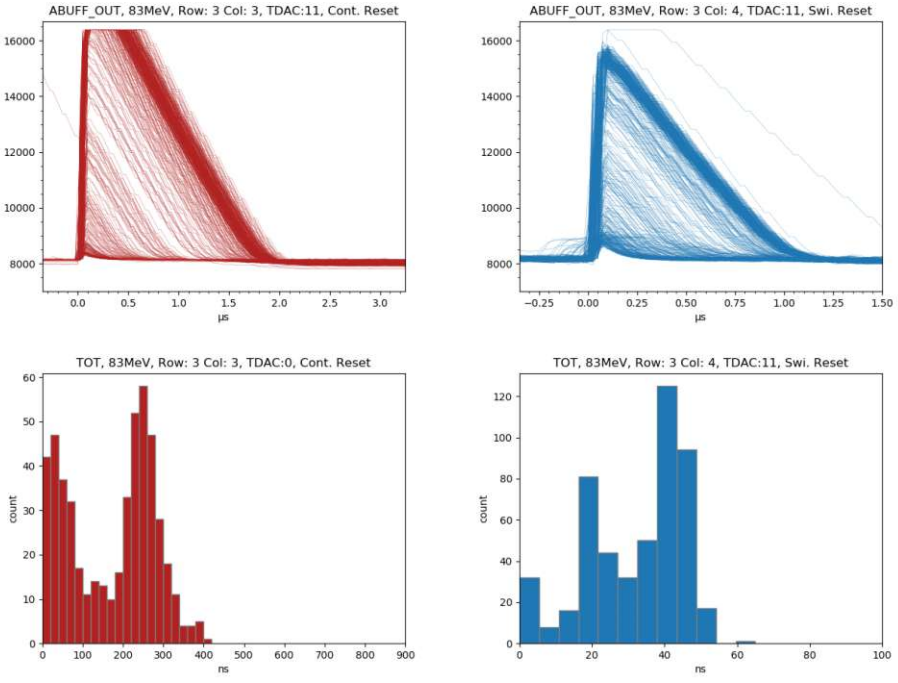
and the waveforms also matched the corresponding simulations. Within a pixel flavor, considerable changes in ToT were observed. The ToT for the waveforms from the external analog buffer output was considerably longer than for the ToT determined internally using the firmware. This was, however, expected due to the parasitic capacitance caused by the chipboard. In the development of another detector, this effect could be reduced by a modified design.

In this testbeam also tracking data was obtained by using appropriate acquisition methods of the firmware and the tracker control of the telescope. The data was analyzed with the corryvreckan framework. The alignment for the tracker planes seemed reasonable, but the alignment for the MPW2 was not satisfying. Here a larger data set would have been necessary and also additional measured pixels would have improved the results. Due to the poor alignment, the efficiency analysis could not be performed with actual tracking data but only with data from the window run. By adapting the measurement, a so-called window scan could be performed, whereby the different charge sharing of the two pixel reset types became visible. The charge sharing of the CR-pixels appeared to be lower than of the SR-pixels.

All aspects and findings of this work on the MPW2 led to the development of a successor chip, the MPW3, which is currently in production and will be available later this year.

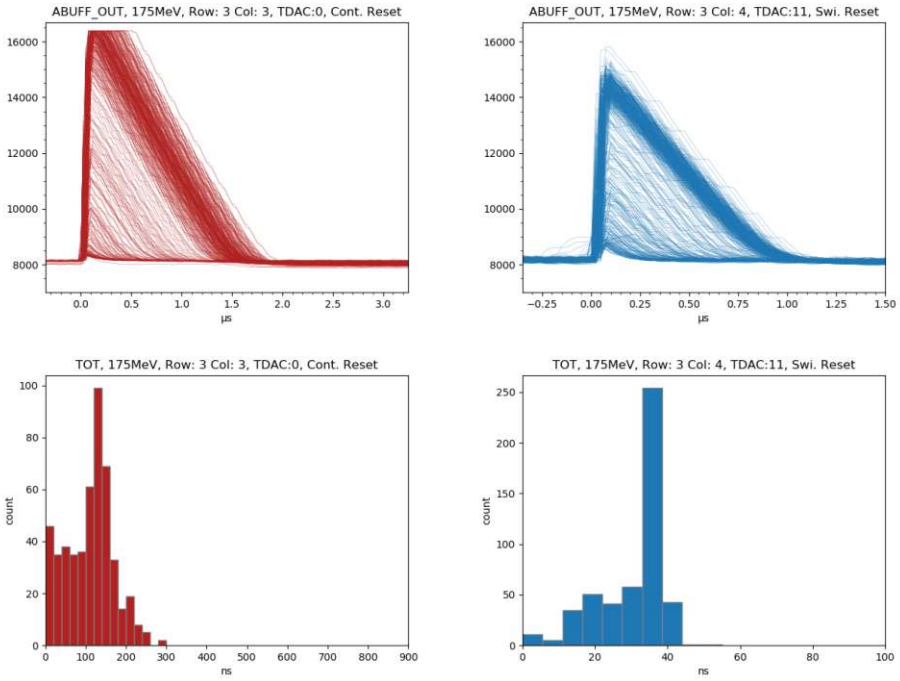
# Appendix A

## A.1 Waveform Measurements

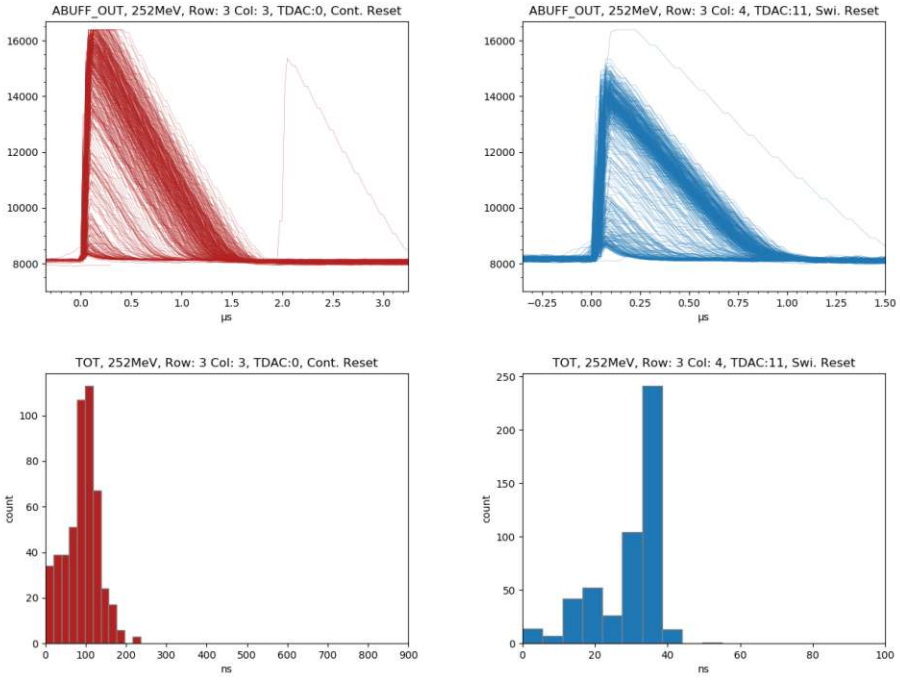



(a) 83 MeV, CR-pixel (b) 83 MeV, SR-pixel

Figure A.1: Waveform and ToT measurement for 83 MeV for every pixel flavor with chips from wafer 13.




(a) 175 MeV, CR-pixel (b) 175 MeV, SR-pixel




(c) 252 MeV, CR-pixel (d) 252 MeV, SR-pixel

Figure A.2: Waveform and ToT measurement for 175 MeV and 252 MeV for every pixel flavor with chips from wafer 13.

# List of Figures

# List of Tables

# Acronyms

**ADC** Analog-Digital Converter. 30, 38, 39, 65, 67, 68, 71, 75, 86

**ALICE** A Large Ion Collider Experiment. 2

**ALPIDE** ALice PIxel DEtector. 2

**API** Application Interface. 43

**ASIC** Application-Specific Integrated Circuits. 35, 37

**CaR** Control and Readout. 3, 37–39, 41–43, 48, 49, 61, 65, 67, 68, 71, 75

**CaRIBOu** Control and Readout Inner Tracking Board. v, vii, 3, 37–42, 44, 45, 47, 59, 60, 65, 66, 75, 80

**CB** Conduction Band. 10–14

**CCD** Charge-Coupled Detectors. 21

**CLI** Command Line Interface. 43, 44

**CMOS** Complementary Metal-Oxide-Semiconductor. v, vii, 2, 19–22, 29, 38, 79

**CPU** Central Processing Unit. 31, 36, 39, 42, 45

**CR** Continuous Reset. 23–27, 49, 54, 56, 58, 61, 64, 68–71, 73, 75–78

**CSA** Charge-Sensitive Amplifier. 23, 24

**CTE** Charge Transfer Efficiency. 21

**DAC** Digital-Analog Converter. 51, 52, 54, 80, 87

**DAQ** Data Acquisition. v, vii, 3, 29–33, 35–37, 39–45, 48, 59, 61, 67, 75, 79, 80

**DMAPS** Depleted monolithic Active Pixel Sensor. v, vii, 1, 2, 19–21, 29, 79

**DSSD** Double Sided Strip Detector. 19, 65, 66, 71, 75

**DUT** Device Under Test. 32, 65, 71, 72

**FADC** Flash ADC. 65

**FCC** Future Circular Collider. v, vii, 2

**FIFO** First In - First Out. 48, 67

**FMC** FPGA Mezzanine Card. 36, 37, 67

**FPGA** Field Programmable Gate Arrays. 34–40, 42, 43, 45, 48, 61, 65, 67, 80, 86

**FSM** Finite State Machine. 33, 34, 80

**FWHM** Full Width Half Maximum. 50, 54, 80

**GUI** Graphical User Interface. 31

**HAL** Hardware Abstraction Layer. 40, 42

**HDL** Hardware Description Language. 34

**HEP** High Energy Physics. 1, 5

**HR** High Resistivity. 2

**HV** High Voltage. 2, 21, 22, 26, 29, 38, 39, 48, 49, 55–58, 61–64, 68–71, 75, 79, 80

**IC** Integrated Circuit. 34

**IP** Intellectual Property Core. 45

**ITS** Inner Tracking System. 2

**LHC** Large Hadron Collider. v, vii

**MFS** Minimum Feature Size. 20

**MIP** minimum ionizing particle. 6, 13

**MOSFET** Metal-Oxide-Semiconductor Field-Effect Transistors. 20, 79

**NIM** Nuclear Instrumentation Standard. 65

**NMOS** n-type Metal-Oxide Semiconductor. 20, 21

**OS** Operation System. 31, 36, 41, 42, 44, 45

**PCB** Printed Circuit Board. 36

**PM** Photo Multiplier. 29

**PMOS** p-type Metal-Oxide Semiconductor. 20, 21

**ROI** Region of Interest. 72

**SDK** Software Development Kit. 45

**SNR** Signal-to-Noise-Ratio. 13

**SoC** System-on-a-Chip. 35, 36, 39, 42, 45

**SPL** Secondary Program Loader. 42

**SR** Switched Reset. 23, 24, 26, 27, 49, 50, 56, 58, 62, 64, 68–71, 73, 75–78

**SSH** Secure Shell. 39, 42, 44

**TLU** Trigger Logic Unit. 61, 65, 67, 71

**ToT** Time over Threshold. 24, 25, 48, 59, 65, 67–71, 75–78, 80, 81

**TRIMDAC** trimmable DAC. 23, 25, 47–49, 51–56, 61, 62, 68, 69, 80

**TS** Timestamp. 33, 61, 67

**UART** Universal Asynchronous Receiver Transmitter. 39, 42, 44

**VB** Valence Band. 10–14

**VME** Versa Module Eurocard. 65

# Bibliography


[1] Ricardo Marco-Hernández. "Overview of CMOS Sensors for Future Tracking Detectors". In: *Instruments* 4.4 (2020), p. 36. DOI: 10.3390/instruments4040036. arXiv: 1910.07284 [physics.ins-det].

[2] Nicola Barchetta, Paula Collins, and Petra Riedler. "Tracking and vertex detectors at FCC-ee". In: *Eur. Phys. J. Plus* 137.2 (2022), p. 231. DOI: 10.1140/epjp/s13360-021-02323-w. arXiv: 2112.13019 [physics.ins-det].

[3] Domenico Colella. "Upgrade of the ALICE experiment beyond LHC Run 3". In: *10th International Conference on New Frontiers in Physics*. June 2022. arXiv: 2206.13247 [hep-ex].

[4] E. Vilella. "Development of high voltage-CMOS sensors within the CERN-RD50 collaboration". In: *Nucl. Instrum. Meth. A* 1034 (2022), p. 166826. DOI: 10.1016/j.nima.2022.166826.

[5] Chenfan Zhang et al. "Development of RD50-MPW2: a high-speed monolithic HV-CMOS prototype chip within the CERN-RD50 collaboration". In: *PoS* TWEPP2019 (2020), p. 045. DOI: 10.22323/1.370.0045.

[6] K. A. Olive et al. "Review of Particle Physics". In: *Chin. Phys. C* 38 (2014), p. 090001. DOI: 10.1088/1674-1137/38/9/090001.

[7] H. Kolanoski and N. Wermes. *Particle Detectors: Fundamentals and Applications*. Oxford University Press, 2020. ISBN: 9780198858362.

[8] C. Grupen and B. Shwartz. *Particle Detectors*. Cambridge Monographs on Particle Physics, Nuclear Physics and Cosmology. Cambridge University Press, 2008. ISBN: 9780521840064.

[9] L. Rossi et al. *Pixel Detectors: From Fundamentals to Applications*. Particle Acceleration and Detection. Springer, 2006. ISBN: 9783540283324.

[10] R. Turchetta et al. "CMOS Monolithic Active Pixel Sensors (MAPS): New eyes for science". In: *Nucl. Instrum. Meth. A* 560 (2006). Ed. by M. Caccia and B. Mikulec, pp. 139–142. DOI: 10.1016/j.nima.2005.11.241.

[11] M.C. Schneider and C. Galup-Montoro. *CMOS Analog Design Using All-Region MOSFET Modeling*. Cambridge University Press, 2010. ISBN: 9780521110365.

[12] J. Korec. *Low Voltage Power MOSFETs: Design, Performance and Applications*. SpringerBriefs in Applied Sciences and Technology. Springer New York, 2011. ISBN: 9781441993205.

[13] Erik Bruun. *CMOS Analog IC Design: Fundamentals*. English. 2nd edition. bookboon, 2019. ISBN: 9788740330045.

[14] Eric R. Fossum. "Active pixel sensors: are CCDs dinosaurs?" In: *Charge-Coupled Devices and Solid State Optical Sensors III*. Ed. by Morley M. Blouke. Vol. 1900. International Society for Optics and Photonics. SPIE, 1993, pp. 2–14. DOI: 10.1117/12.148585. URL: https://doi.org/10.1117/12.148585.

[15] Ivan Peric. "A novel monolithic pixelated particle detector implemented in high-voltage CMOS technology". In: *Nucl. Instrum. Meth. A* 582 (2007). Ed. by Giovanni Ambrosi et al., pp. 876–885. DOI: 10.1016/j.nima.2007.07.115.

[16] E. Vilella et al. "Report on recent activities in HV-CMOS detectors for Mu3e, ATLAS and RD50". In: *JINST* 13.07 (2018), p. C07002. DOI: 10.1088/1748-0221/13/07/C07002.

[17] Zhang C. *RD50-MPW2 Documentation*. version 1.2 29/04/2019. RD50 HVCMOS group. 2019.

[18] J. Park, ASD John Park, and S. Mackay. *Practical Data Acquisition for Instrumentation and Control Systems*. Electronics & Electrical. Elsevier Science, 2003. ISBN: 9780750657969.

[19] Z. Karakehayov. *Data Acquisition Applications*. IntechOpen, 2012. ISBN: 9789535107132.

[20] Andrea Negri. *Introduction to Data AcQuisition*. Jan. 2020. URL: https://indico.cern.ch/event/828931/contributions/3469971/attachments/1863381/3272510/isotdaq20.Negri.DaqIntro.pdf.

[21] P. Ahlburg et al. "EUDAQ-a data acquisition software framework for common beam telescopes". In: *JINST* 15.01 (2020), P01038. DOI: 10.1088/1748-0221/15/01/P01038. arXiv: 1909.13725 [physics.ins-det].

[22] Darya Shirokova. "Software Development for a common DAQ at test beams". In: *DESY summer student project* (2016).

[23] Yi Liu. *EUDAQ2 User Manual*. Tech. rep. 2017.

[24] P. Zhang. *Advanced Industrial Control Technology*. William Andrew/Elsevier, 2010. ISBN: 9781437778076.

[25] Maurizio Di Paolo Emilio. *Embedded Systems Design for High-Speed Data Acquisition and Control*. Springer Publishing Company, Incorporated, 2014. ISBN: 3319068644.

[26] W. Wolf. *Computers as Components: Principles of Embedded Computing System Design*. ISSN. Elsevier Science, 2008. ISBN: 9780080886213.

[27] Dave Barker. *Introducing the FPGA Mezzanine Card: Emerging VITA 57 (FMC) standard brings modularity to FPGA designs*. Apr. 2008. URL: http://vita.mil-embedded.com/articles/introducing-fpga-brings-modularity-fpga-designs/.

[28] *Open Source CaRIBOu project*. URL: https://gitlab.cern.ch/Caribou.

[29] Tomas Vanat. "Caribou – A versatile data acquisition system". In: *PoS* TWEPP2019 (2020), p. 100. DOI: 10.22323/1.370.0100.

[30] Adrian Fiergolski. "A Multi-chip Data Acquisition System Based on a Heterogeneous System-on-Chip Platform". In: *Springer Proc. Phys.* 212 (2018). Ed. by Zhen-An Liu, pp. 303–308. DOI: 10.1007/978-981-13-1313-4_57.

[31] *CaR-board specifications*. URL: https://gitlab.cern.ch/Caribou/hardware/carboard/-/blob/master/README.md.

[32] *Xilinx ZC706 Evaluation Board for the Zynq-7000 XC7Z045 SoC*. URL: https://www.xilinx.com/products/boards-and-kits/ek-z7-zc706-g.html#documentation.

[33] *Manual of Yocto Project*. URL: https://docs.yoctoproject.org/ref-manual/index.html.

[34] Reyhan Ramadhan. "OS Update and Board Upgrade of CaRIBOu DAQ System. OS: operating system". In: (Aug. 2019). URL: https://cds.cern.ch/record/2686217.

[35] Patrick Sieberer et al. "Readout system and testbeam results of the RD50-MPW2 HV-CMOS pixel chip". In: (Jan. 2022). arXiv: 2201.08585 [physics.ins-det].

[36] Michael Benedikt and Albin Wrulich. "MedAustron—Project overview and status". In: *The European Physical Journal Plus* 126.7 (2011), pp. 1–11. DOI: https://doi.org/10.1140/epjp/i2011-11069-9.

[37] F. Ulrich-Pur et al. "Imaging with protons at MedAustron". In: *Nucl. Instrum. Meth. A* 978 (2020), p. 164407. DOI: 10.1016/j.nima.2020.164407. arXiv: 2003.00115 [physics.ins-det].

[38] Felix Ulrich-Pur et al. "Commissioning of low particle flux for proton beams at MedAustron". In: *Nucl. Instrum. Meth. A* 1010 (2021), p. 165570. DOI: 10.1016/j.nima.2021.165570. arXiv: 2102.06240 [physics.acc-ph].

[39] S. Meroli, D. Passeri, and L. Servoli. "Energy loss measurement for charged particles in very thin silicon layers". In: *JINST* 6 (2011), P06013. DOI: 10.1088/1748-0221/6/06/P06013.

[40] Morag Williams et al. *Corryvreckan - A Modular 4D Track Reconstruction and Analysis Software for Test Beam Data*. Version 2.0.0. Dec. 2020. DOI: 10.5281/zenodo.4384186. URL: https://doi.org/10.5281/zenodo.4384186.