Masterthesis

Characterization of printed copper layers on power chips

submitted in fulfilment of the requirements for the degree of Diplomingenieur under supervision of

Associate Prof. Dipl.-Ing. Dr.techn. Christian Gierl-Mayer

at the Institute of Chemical Technologies and Analytics on TU Wien

by

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Wien, May 2022

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Diplomarbeit

Charakterisierung von gedruckten Kupferschichten auf Leistungschips

ausgeführt zum Zwecke der Erlangung des akademischen Grades Diplomingenieur unter der Leitung von

Associate Prof. Dipl.-Ing. Dr.techn. Christian Gierl-Mayer

am Institut für Chemische Technologien und Analytik der Technischen Universität Wien

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Abstract

Recent developments among the semiconductor industry like a trend to replace conventional silicon semiconductors with wide bandgap materials such as silicon carbide but also new fields of application call for new interconnecting technologies with adapted properties.

Especially in the field of power semiconductors conventional interconnecting technologies like lead-based solders are limiting the exploitation of the full potential of the new materials due to their low operating temperature. Sintered porous copper interconnects can operate at much higher temperatures, come with outstanding performance in terms of electrical and thermal conductivity. A possible way of realizing such porous interconnects is by sintering of printed sinter pastes.

During this work first samples of sintered porous copper layers were investigated with classical powder metallurgical techniques like scanning electron microscopy SEM and helium pycnometry. A special focus was thereby given to the microstructure and porosity. The topography of the layer was further analysed with light optical microscopy via "z-stacking" and finally the elemental composition investigated by energy dispersive x-ray EDX analysis as well as infrared spectroscopy.

Based on the results found, a good first impression about the nature of the layer as well as its porosity, pore size distribution and elemental composition was gained. By comparison of different production parameters it was possible to investigate the influence of pressure sintering to the porosity and microstructure.

As this thesis is part of an ongoing developing process, a final assessment is not possible yet. The results found however will be implemented in the production process to eliminate existing problems and further improve the product.

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Zusammenfassung

Aktuelle Entwicklungen in der Halbleiter Industrie wie der Trend konventionelle Silizium Halbleiter mit „wide bandgap“ Materialien wie Siliziumcarbid zu ersetzen aber auch sich ändernde Einsatzbereiche benötigen neue Verbindungstechnologien mit angepassten Eigenschaften.

Speziell im Bereich der Leistungshalbleiter gängige Verbindungstechnologien wie Blei basierte Lote limitieren diese neuen Bauteile wegen ihrer niedrigen möglichen Einsatztemperaturen. Gesinterte poröse Kupfer Schichten können bei deutlich höheren Temperaturen eingesetzt werden und zeichnen sich durch exzellente thermische und elektrische Leitfähigkeiten aus. Eine mögliche Form der Realisierung solcher Schichten ist das Sintern von gedruckten Sinterpasten.

Im Zuge dieser Arbeit konnten erste Proben mit gesinterten porösen Kupferschichten mit Methoden der klassischen Pulvermetallurgie wie Rasterelektronenmikroskopie REM oder Helium Pyknometrie. Dabei wurde besonderes Augenmerk auf die Mikrostruktur und Porosität gelegt. Die Topographie wurde in weiterer Folge mit optischer Lichtmikroskopie durch „z-stacking“ untersucht und schlussendlich die elementare Zusammensetzung durch energiedispersive Röntgenanalyse EDX und Infrarotspektroskopie aufgeklärt.

Basierend auf den erhaltenen Ergebnissen konnte ein guter erster Eindruck über die Beschaffenheit der Schicht wie auch über deren Porosität, Porengrößenverteilung und elementarer Zusammensetzung gewonnen werden. Durch einen Vergleich von unterschiedlichen Produktionsparametern konnte der Einfluss von Drucksintern auf die Porosität und Mikrostruktur untersucht werden.

Da die vorliegende Arbeit Teil eines Entwicklungsprozesses ist, ist eine abschließende Beurteilung zum aktuellen Zeitpunkt noch nicht möglich. Die Ergebnisse werden in den Produktionsprozess eingebunden um vorhandene Probleme zu eliminieren und das Verfahren weiter zu optimieren.

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1 INTRODUCTION

1.1 Background & Motivation

1.1.1 Background

The present thesis originated from a project by the Austrian Research Promotion Agency (Österreichische Forschungsförderungsgesellschaft, FFG) called *"Produktionstechnische Umsetzung von nano-porösen Kupfer-Verbindungstechnologien in der Leistungselektronik"* with project number 883905. While the general project aims for a production-related implementation of nano-porous copper interconnect technologies in power electronics, the main focus of the work described here will be the characterization of first prototype power chips coated with nano-porous copper. The practical work was performed at TU Wien in Assoc. Prof. Dr. Christian Gierl-Mayer's working group for powder metallurgy.

The samples used for this thesis were produced by Infineon Technologies Austria AG – a brief overview on the production will be given in *section 2.1*.

1.1.2 Motivation

As the global market is subject to constant change and requirements continuously evolve, the semiconductor industry has to adapt likewise. In recent years a trend towards miniaturization of devices demanded higher efficiency and better performance as well as higher energy densities and a reduction of losses in semiconductors.

The addition of new fields of application and different operating conditions come with new challenges. Also, a rising awareness on climate change and environmental compatibility comes with restrictions regarding production materials.

To meet these new requirements a lot of research effort has been put into finding and developing new semiconductor materials. Thus, the power semiconductor industry for example is continuously moving from conventional silicon semiconductors to so called wide bandgap WBG semiconductor materials and devices because of their higher efficiency.

While the new materials for WBG applications are already well known and established, the corresponding interconnection technologies are still in development. For reasons of miniaturization, thermal stability and heat management as well as concerns about toxicity the widely used lead-based solders are replaced by new interconnection methods.

This thesis focuses on the research and characterization of sintered porous copper metallization for the formation of all copper interconnects in power semiconductors.

1.2 Fundamentals of power semiconductors

Power semiconductors are a key element in power electronics systems to convert energy [1], and are further used in a wide range of applications from (renewable) energy systems [2, 3] via industrial equipment to hybrid and electric vehicles [4, 5]. In simple words power semiconductors in electrical power converters can be described as switches.

The most common devices used are metal oxide semiconductor field-effect transistor (MOSFET) and insulated-gate bipolar transistor (IGBT). For both devices, high efficiency and high-power density are key characteristics. Thereby from a constructional point of view the reduction of switching and conduction losses, but also temperature management are important design parameters.

For the integration of power semiconductors in electrical devices they have to be electrically connected. The two main terms to consider in this regard are interconnection technology and metallization. While the interconnection technology describes the way how the semiconductor is connected, the term metallization refers to the area where the connection happens.

1.2.1 Pad metallization

In recent years the copper replaced aluminium as the state-of-the-art metallization material. Copper clearly outperforms aluminium in terms of electrical and thermal conductivity as shown in *Table 1*. Further there are several advantages during the production process that are making copper a desirable metallization material.

Table 1 – relevant material properties of copper, silver, aluminium, and silicon [6, 7]

	Copper	Silver	Aluminium	Silicon
electrical conductivity (MS/m)	59.6	63	34	
thermal conductivity (W/mK)	401	429	237	
CTE (ppm)	16.5	19	23.1	2.6

While aluminium must be deposited in a sputtering process and for this reason requires vacuum, copper can be deposited electrochemically or as sinter paste and is thereby a less cost intensive way for pad metallization in terms of investment costs as well as process costs.

Despite all the advantages, the usage of copper as metallization cannot overcome all difficulties known for the pad metallization. While the coefficient of thermal extension CTE in the case of copper fits better to silicon-based semiconductors (mismatch 13.9 ppm) compared to aluminium (mismatch 20.5 ppm) a difference still remains – *Table 1*.

As the device generates heat upon operation the varying CTE’s cause mechanical stress that can lead to wafer bow and in the worst case to a complete mechanical failure. Thereby the simple change of the metallization material alone is not enough.

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Further copper is reactive towards silicon and forms intermetallic phases which can also cause failure of the semiconductor device. In *Figure 1* the phase diagram of the system silicon – copper is shown. One can clearly see, that even at relatively low temperatures of around 400 °C copper can solve up to about 5 wt% of silicon. Also, several stable intermetallic phases and line compounds like the η'' (Cu_3Si), ε and γ exist at these temperatures [8].

In combination with a very fast diffusion of copper in doped silicon devices [9] it is reported, that the contamination of silicon devices with copper can cause several failure modes like short cuts and leakage currents up to mechanical failure as a result of the formation of intermetallic phases [10].

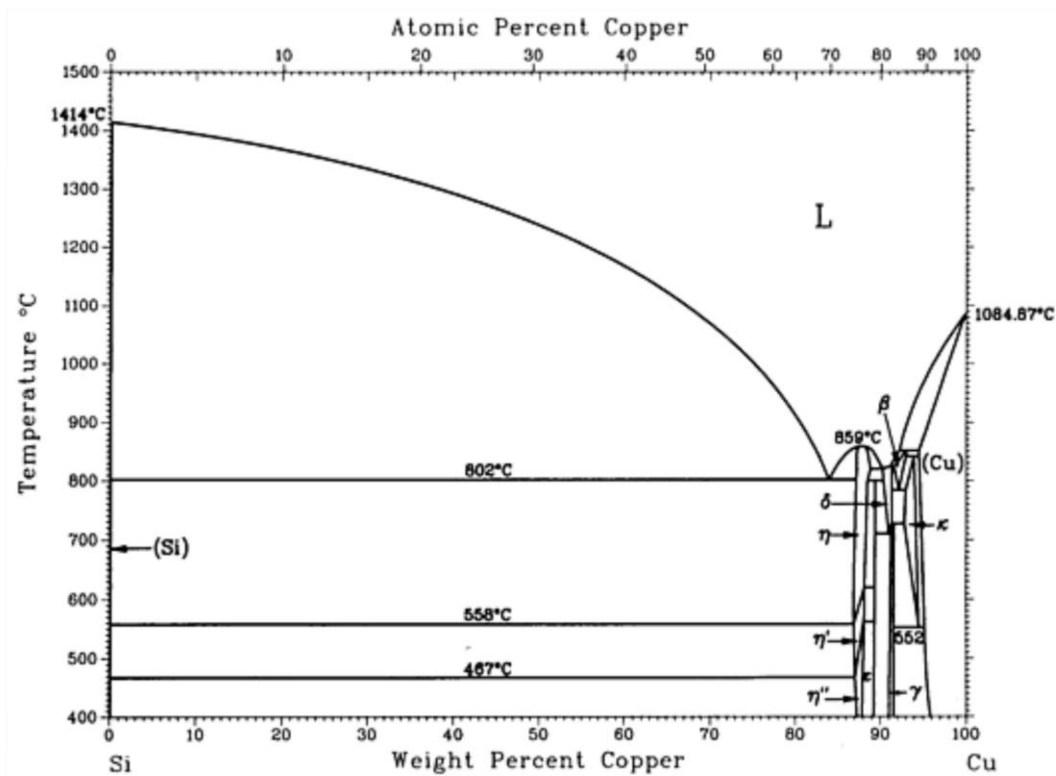

Figure 1 – binary phase diagram of the system silicon/copper [8]

Aluminium in contrast faces none of these challenges – *Figure 2*. While at temperatures of around 500 °C a very low solubility for silicon in aluminium exists, there are no intermetallic phases formed in between these metals at any given temperature [8].

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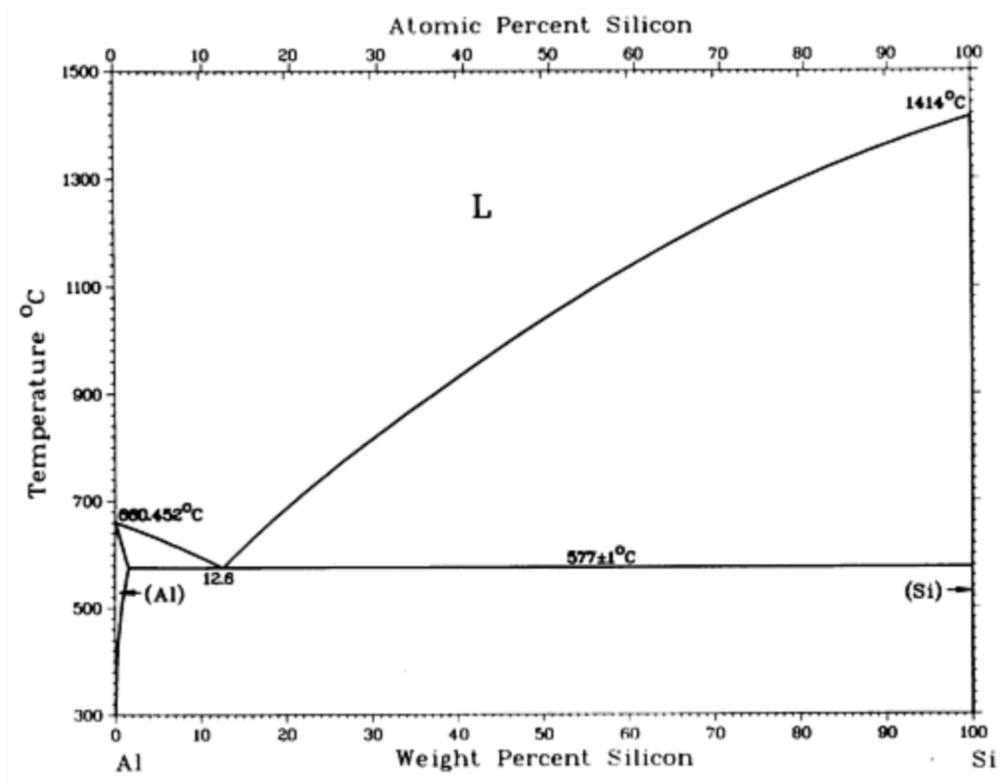

Figure 2 – binary phase diagram of the system aluminium/silicon [8]

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1.2.2 Interconnect technologies

As power electronic devices usually consist of more than one semiconductor, interconnecting technologies are of enormous importance for the functionality of respective devices. Another reason for their huge importance is their influence on the reliability upon operation. In general interconnects must perform well in three different categories[11]:

- **Electrical properties:** The goal of an interconnect is to provide high transmission speed and signal integrity at low power. Thereby, to reduce losses, the electrical resistance as well as the capacitance and the inductance of the interconnect shall be held at a minimum. Further the amount of current that possibly can pass through should be maximized. In order to fulfil the above-mentioned requirements, the choice of material, but also the geometry of the interconnection are main design parameters.

- **Thermal properties:** Every semiconductor device generates heat during operation. From Joule heating to switching losses, there are several mechanisms that cannot be fully prevented. Thereby the heat management especially the dissipation of heat is a major issue to be addressed to avoid temperature induced failure of devices.
  In this regard the key characteristic for the interconnect is a high thermal conductivity. The coefficient of thermal extension (CTE) is also important to be considered, as a mismatch in CTE between interconnect and substrate leads to thermal induced stress at the interface. Upon operation of the device one has to keep in mind, that due to the amount of switching operations the change of temperature is no longer a single event, but a permanent process. Thereby the mechanical load intensifies as to the now dynamic nature of the load.

- **Mechanical properties:** The mechanical behaviour of interconnects during operation is an important factor, as mechanical failure most likely leads to electrical failure and possibly to failure of the whole device. This is in particular of very high concern, as power semiconductors are used in many parts of everyday life and failure in worst case scenarios endangers human lives. To prevent thermomechanical fatigue the yield strength should be rather high to avoid plastic deformation. In contrast to that the drop performance improves with lower modulus, making the choice of material dependent on the field of application.

Besides the main design requirements listed above, there are several methods to realize an interconnection. A brief overview on some of the most common interconnection technologies will be given:

- **Soldering:** Solder interconnects come in a wide range of compositions. While solders originally were based on tin-lead compounds nowadays lead-free solders are used due to the high toxicity of lead. Generally speaking, lead-free solders slightly fall short in terms of thermomechanical properties and have an increased melting point compared to their lead containing equivalents. Nonetheless they are today a widely used interconnection technology. To enable a miniaturization of devices, the size of the interconnects needs to be reduced as well as the amount of solder used due to possible failure because of solder bridging. Despite all their advantages, solders are limited regarding their operating temperature because of their low melting points.

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- **Solid-Liquid interdiffusion (SLID) bonding:** SLID bonding is a technique to create an interconnection based on a two-metal system which forms an intermetallic compound [12]. In general, one of the metals comes with a high melting point while the other one comes with low melting point. During assembly the temperature exceeds the melting point of the lower melting metal and an intermetallic compound is formed by interdiffusion. The intermetallic phases melting point is higher than the assembly temperature making SLID bonded interconnects a viable alternative for solders especially for high temperature applications [13]. A common example for SLID bonding is the system Cu-Sn which forms the intermetallic compound Cu_3Sn and thereby rises the melting point from ~230 °C (melting point Sn) to ~650 °C (melting point Cu_3Sn) [13].

- **Direct wire bonding:** Wire bonding is one of the most important interconnect technologies in the semiconductor industry. While gold was originally the most common wire material, nowadays copper is mainly used [14]. In comparison to the above mentioned solder based methods, direct bonding faces several challenges like slow kinetics, oxidation and high bonding forces [11, 15]. To overcome these issues the material is often activated by elevated temperatures and ultrasonic energy [11, 16]. Further the bonding process should be carried out in inert or reducing atmosphere.

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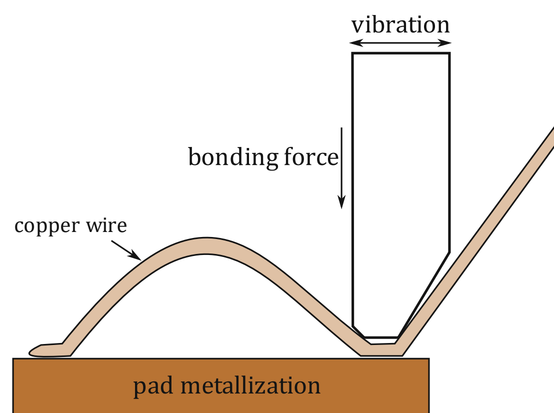

Figure 3 – scheme of ultrasonic wire bonding [17]

- **Sintered porous interconnects:** As described above, in recent years semiconductor devices more and more switched from all silicon devices to wide bandgap (WBG) materials such as SiC or GaN. However, the performance of WBG devices is at the moment limited by the interconnection technologies, as conventional methods are not optimized for them [18]. Thereby especially for high temperatures which originate from the enhanced performance of respective devices new interconnecting technologies are needed [18, 19]. Porous metal interconnects in this context have been heavily researched as they have excellent electric and thermal conductivities and stable performance at higher temperatures.
  There are several methods to synthesize porous metal interconnects from which metal sinter pastes [20, 21] and chemical dealloying [18, 20] are the most common. Further methods like electrochemical deposition [22] and oblique angle deposition [23] have been reported.

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1.3 Highly porous copper sinter pastes - state of the art

1.3.1 Porous materials

The International Union of Pure and Applied Chemistry (IUPAC) defines porous solids as:

"a solid with pores, i.e. cavities, channels or interstices, which are deeper than they are wide"[24]

Further depending on the pore size one can categorize pores as follows[24, 25]:

- **macropores:** pores with width exceeding 50 nm
- **mesopores:** pores with width between 2 nm and 50 nm
- **micropores:** pores with width below 2 nm

At this point it has to be mentioned, that the term "nanopore" which is commonly used in literature and industry is according to CEN ISO/TS 80004-11:2020 defined as pore with at least one dimension in the range between 1 – 100 nm and thereby embraces all three categories mentioned above with the exception of an upper limit of 100 nm [26].

In terms of the pores availability to the open, they can be divided into closed, and open pores [24]. Further one can distinguish between isolated pores and interconnected pores.

For the determination of porosity several methods have been developed and are commonly used:

- gravimetric methods, e.g. Archimedes method
- gas absorption, e.g. BET [27]
- gas volume measurements, e.g. He-pycnometry [28]
- pore infiltration, e.g. Hg-porosimetry [29]
- optical image analysis [30]

Of course, all these methods come with their own limits and constraints which have to be kept in mind to gain precise and accurate results. In case of the present thesis the limiting factor was the number of samples available which excluded BET and Hg-porosimetry from usage as they required more absolute surface or pore volume.

The introduction of porosity to a material naturally changes the material properties. Mechanical properties like Young's modulus or Yield strength for example show a significant decrease for increasing porosity [31] – *Figure 4 and Figure 5*.

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In *Figure* 5 one can see a linear correlation between the porosity and the yield strength. It is also apparent, that smaller particle sizes result in overall higher yield strengths.

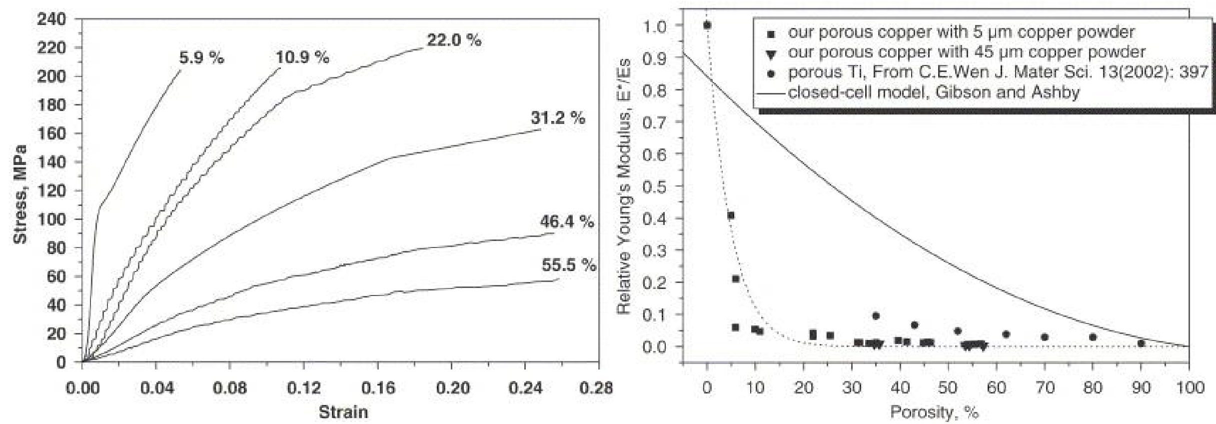

Figure 4 – stress - strain diagrams of porous copper samples with porosities between 5.9 % and 55.5 % (left) and relative Young's modulus vs. porosity (right) [31]

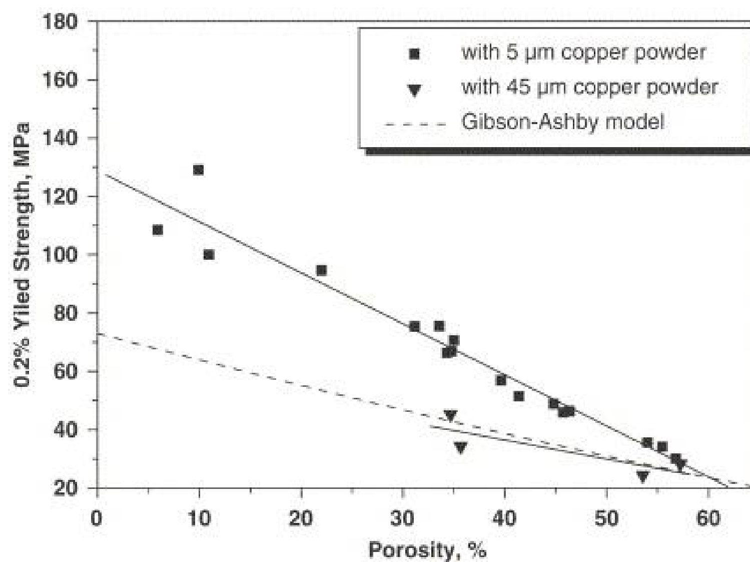

Figure 5 – compressive yield strength vs porosity for different particle size copper powders [31]

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Not only mechanical properties but also thermal and electrical conductivity are strongly affected by the introduction of porosity [31-34]. In *Figure 6* it is shown that the thermal conductivity decreases with in increasing porosity.

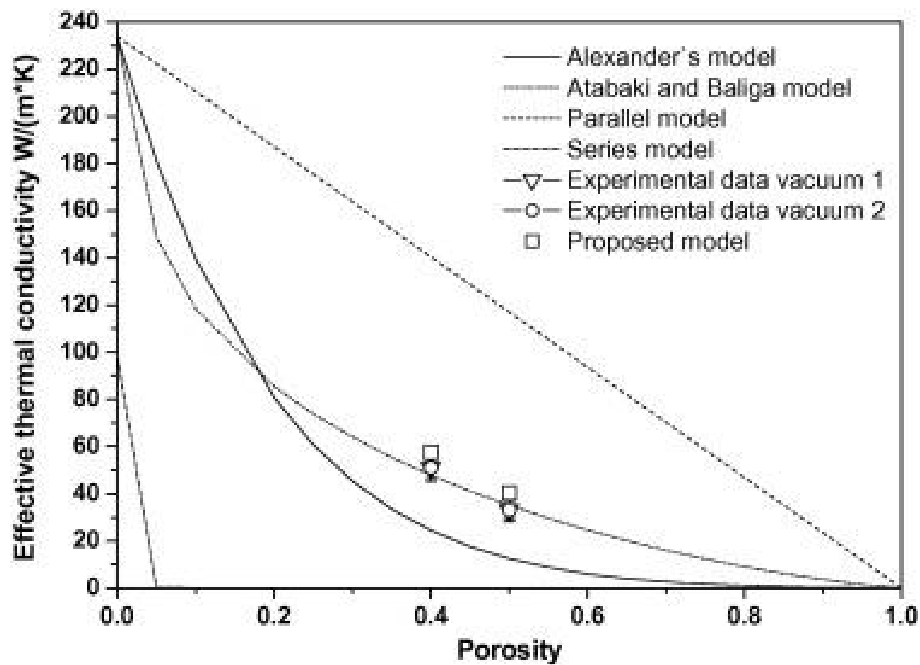

Figure 6 – Effective thermal conductivity vs. porosity measured under vacuum for experimental data and calculations from literature models [33]

A similar behaviour can be seen in *Figure 7*. It is apparent, that the electrical conductivity decreases with higher porosities.

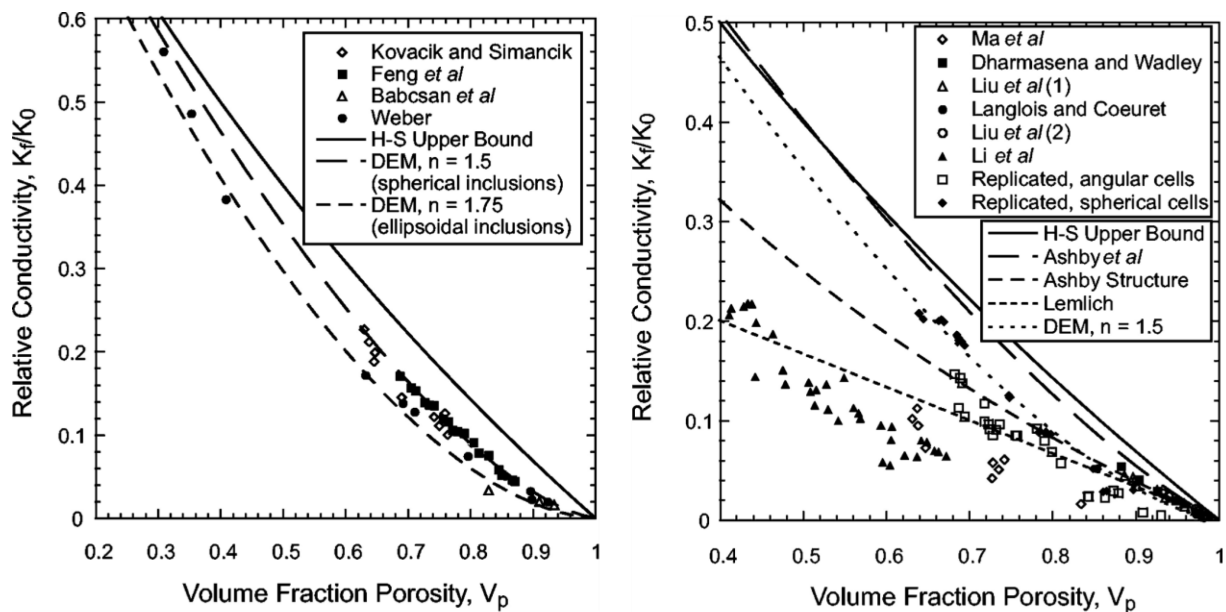

Figure 7 – literature data on the realtive electrical conductivity vs the volume fraction porosity for closed cell (left) and open cell (right) metallic foams [35]

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1.3.2 Sintering process

In general, the term sintering refers to a heat treatment of (powder) particles which leads to its consolidation [36]. It further describes all physical and chemical processes that lead to a filling of the pore volume [37]. While for single metal compacts the sintering temperature is below the melting point of the respective component, in mixed metal systems the sinter temperature can exceed the melting temperature of the lower melting component [36, 37].

As for most chemical and physical systems the main driving force for sinter processes is the reduction and minimisation of the systems total free energy. To achieve this, the system undergoes change in terms of inner and outer surface reduction. For a single-phase system this can be described by the Laplace equation – *see equation (1)[36]*.

$$\boldsymbol{\sigma = \gamma\left(\frac{1}{r_1} + \frac{1}{r_2}\right)} \tag{1}$$

The stress σ causes a gradient in the chemical potential and thereby in the free energy – *equation* (*2*) *[36].* The gradient is proportional with the atomic volume Ω.

$$\boldsymbol{\Delta\mu = \sigma\Omega} \tag{2}$$

From *equation (1)* one can not only see the relation between stress σ and surface tension γ, but also the dependency on the particle size as r_1 and r_2 represent the radii of the surfaces curvature and thereby directly correlate to the particle size. Based on this correlation one can state, that finer powders come with a higher sinter activity.

Thus, to equalise the chemical potential material is transported. Several mechanisms have been reported to be involved in the material transport – *Figure 8*. The most common mechanism is diffusion followed by evaporation and condensation [38]. To provide sufficient mobility and diffusion rates the sinter process runs at elevated temperatures but below the melting point of the main component. Typical sinter temperatures for single-metal powders are around 2/3 to 3/4 of the melting temperature of the individual material.

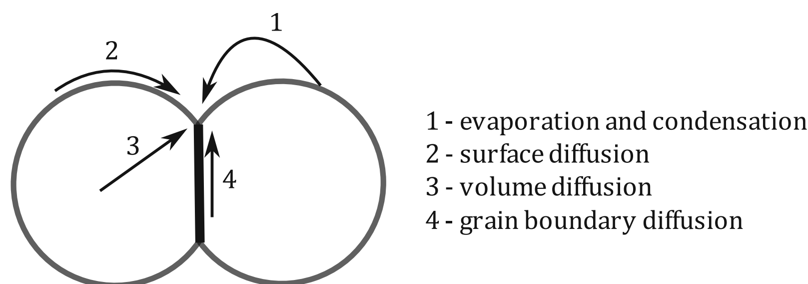

Figure 8 – scheme of sintering particles illustrating different transport mechanisms

A typical sinter processes consist of several steps beginning with the formation of sinter necks via the reduction of pore volume and pore rounding to a growth of grains. Although these steps in general follow the given order, there are no strict separation in between them, and they can thereby overlap.

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1.3.3 Sinter pastes

While the power semiconductor industry more and more replaces conventional silicon power devices with wide bandgap materials like silicon carbide SiC [39] and the operating conditions also trend towards higher operating temperatures conventional interconnection technologies face their limits as conventional solders for example cannot operate at temperatures above 200 °C.

New high temperature interconnects are thereby needed. Sintered porous interconnects can not only operate at temperatures above 200 °C without problems, but also come with outstanding thermal and electrical properties[21].

The need for a low temperature sintering process due to the low junction temperatures of semiconductors compared to conventional sintering temperatures lead to the introduction of metal sinterpastes. Due to the so-called size effect the conventional sinter temperature - *see section 1.3.2* can be significantly lowered by reduction of particle size [39-41]. Submicron and nano scale sinter pastes can thereby be sintered at temperatures between 180 °C and 270 °C [18, 42]

As copper comes with lower material costs than silver while showing similar performance copper sinter pastes are a highly researched topic at the moment. A further advantage of copper over e.g. silver is the lower CTE mismatch between copper and silicon (13.9 ppm) compared to the combination of silver and silicon (16.4 ppm) [6, 7] – *see Table 1*. By adjusting the porosity a “sweet spot” between the – still existing – CTE mismatch and preferably high conductivity can be found [43].

However, the high reactivity of copper and silicon demands the implementation of diffusion barriers between the coating and the semiconductor [9, 44].

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2 MATERIALS & METHODS

2.1 Sample production & pre-treatment

The production of the samples was performed by Infineon Technologies Austria AG. In general, the production included three main steps: a printing step, a curing step, and a pressure sintering step.

As the present thesis mainly focuses on the characterization of the printed copper layers, the individual production steps will not be described in detail. Nonetheless a brief overview about the production parameters is necessary, because a big part of the characterisation was to determine the influence of respective production parameters. The exact production parameters for each sample can be found in *Table 2*.

In general, the samples can be divided in two different groups. The first group included samples which were produced with a bimodular copper sinter paste. This bimodular paste was a combination of a micro sized and a nano sized copper powder. For the second group only nano sized powder was used.

The production of the copper layer started by printing the copper sinter paste via stencil printing on a chip. For all samples the same IGBT chip was used. A scheme of the chip can be found in *Figure 9*. During the printing step the printing thickness as well as the viscosity of the sinter paste was variated.

After printing the samples were cured and sintered under pressureless conditions. Until 100 °C the sintering atmosphere for this step was nitrogen which was replaced by an nitrogen atmosphere containing 3.3 wt% formic acid at temperatures exceeding 100 °C.

To obtain a denser structure which is expected to result in favourable thermal and electrical features an additional third production step – pressure sintering – was conducted with some samples. This sintering step combines sintering with the additional application of mechanical pressure. The force applied, as well as the sinter temperature and the sintering atmosphere, were variated and can be found in *Table 2.*

As Infineon Technologies Austria AG already had a prioritization of the samples, the number of samples for each group varied.

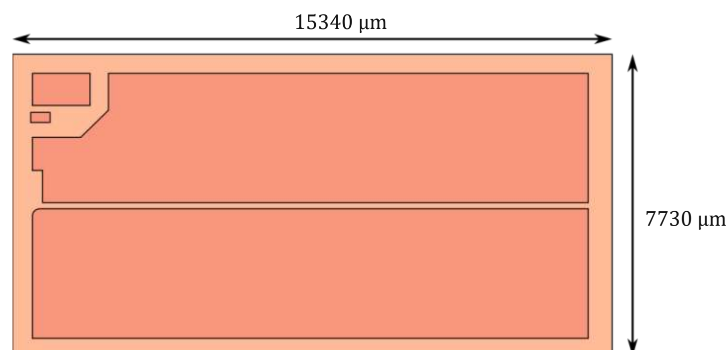

Figure 9 – scheme of the IGBT chip used

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Table 2 – production parameters of samples provided by Infineon Technologies Austria AG

	sample	printing		curing/sintering		pressure sintering		
		thickness (µm)	viscosity (Pa*s)	atmosphere	temperature (°C)	pressure (kN)	temperature (°C)	atmosphere
mixed sinter paste	VE041888 #3	60	80	N_2/formic acid	400			
	VE043977 #8	120	80					
	VE043977 #22	60	30					
	Group 1	60	80	N_2/formic acid	400	330	270	N_2H_2
	Group 4	60	80			450	285	N_2H_2
	Group 7	60	80			450	285	formic acid
nano sinter paste	Group 1	60		N_2/formic acid	230	330	275	N_2H_2
	Group 2	60			230	450	310	formic acid
	Group 3	60			300	450	310	formic acid
	Group 4	60			300	330	275	N_2H_2

Table 3 – grinding and polishing parameters

	disc	grit/suspension	force (N)	sample rotation speed (rpm)	table rotation speed (rpm)	time (min)	operating mode
grinding	Piano	200/water	30	300	150	5	co rotation
polishing	Largo	DiaDuo 9 µm	30	150	150	10	co rotation
	Dac	DiaDuo 3 µm	25	150	150	18	co rotation
	Nap	DiaDuo 1 µm	15	150	150	5	counter rotation

2.2 Structural analysis

2.2.1 Surface analysis

In order to gain a general overview on the nature of the porous copper layer, the samples were first investigated with a scanning electron microscope – SEM. The "mixed" sinter paste samples were analysed in a *JEOL JCM-6000 Benchtop SEM.* For the "nano" sinter paste samples a higher magnification was needed and thereby a *Quanta-200 SEM* was used.

2.2.2 Metallography and microstructure

The microstructure of the sintered copper layers was analysed by optical microscopy and SEM. To do so, metallographic crosscuts and angled cuts were made – *Figure 10*. The metallographic grinding and polishing were performed on a *Struers Tegramin-30* preparation system.

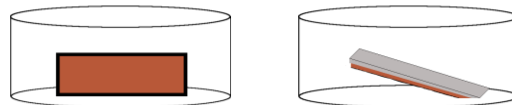

Figure 10 - scheme of embedment direction for metallographic crosscut (left) and angled cut (right)

For both types of cuts, the samples were cold embedded in epoxy resin with a *Struers EpoFix Kit*. As the main goal of this procedure was to present the porosity and pore structure, it was essential to infiltrate the pores with epoxy resin to preserve its original shapes. The infiltration of the pores was performed by putting the embedding moulds in a vacuum chamber and evacuating three times – to 100 mbar, 80 mbar and 60 mbar. After the infiltration, the epoxy was hardened overnight.

The embedded samples were then grinded and polished to prepare a smooth surface for the analysis. All samples were prepared with the same parameters which can be found in *Table 3.* Between each preparation step the specimens were submerged in isopropanol and put into an ultrasonic bath.

Before finally analysing the embedded samples with SEM, a thin gold layer was sputtered on the surface to avoid charging effects.

2.2.3 Topographical analysis

From the microstructural analysis of the samples not only information on the porosity and pore size distribution was gained, but also information on the layer thickness. However, as this information was not representative for the entire copper layer, a closer look at the distribution of the layer thickness was taken.

This analysis was performed on a KEYENCE VHX 5000 optical microscope, by combining height information from z-stacking with areal information via panorama pictures. The pictures were

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taken with x500 magnification and finally merged to a heatmap representing the layer thickness across the entire wafer.

The main challenge with this method was the huge amount of data that had to be processed. For this reason, it was not possible to picture the whole wafer in one panorama at once. Thereby to obtain a complete heatmap representing the entire layer two pictures had to be combined.

2.3 Porosity analysis

The porosity of the samples was analysed by two different methods: Archimedes-principle and He pycnometry. In case of the cured but not pressure sintered samples, uncoated wafers were available. For the pressure sintered samples this was not the case, as the wafers were sintered on a direct bonded copper (DBC) substrate – *Figure 11 (l)*. To be able to perform all the measurements described below, this substrate had to be cut. Thereby each pressure sintered sample had an individual amount of the DBC substrate attached making it impossible to compare results to not coated single wafers. As a workaround, after the first measurement of the cut sample, the copper layer was removed with concentrated nitric acid – *Figure 11 (r).* The resulting wafer was then measured again and used as reference to determine the mass and density of the single copper layer. As a third method image analysis was used to conclude to the porosity.

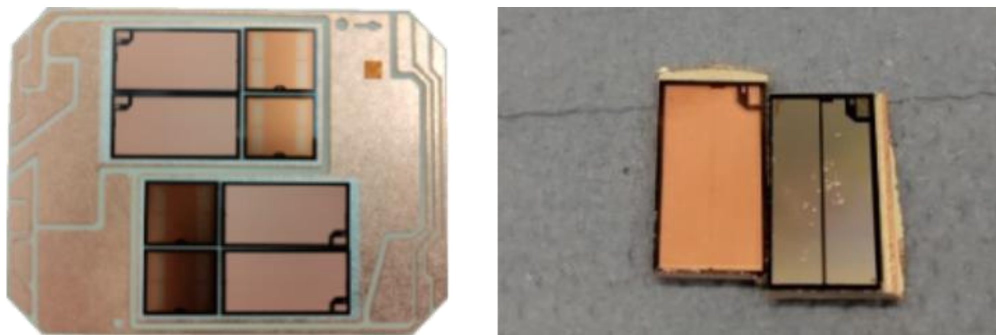

Figure 11 – pressure sintered sample on DCB plate (l) and cut pressure sintered samples before and after etching (r)

2.3.1 Archimedes Method

For the density measurement according to the Archimedes-principle the mass of the sample was measured on air (m_a) and when submerged into a fluid (m_f). DIN ISO 2738 describes the exact procedure. In order to measure the apparent density, it had to be assured that the submerging fluent did not penetrate the open pores. Thereby the samples surface was coated with a thin layer of paraffin, by immersing the samples for a few seconds into a bath of cyclohexane with 3 wt% of paraffin. The measurements were performed on a *METTLER TOLEDO XS204 DeltaRange®* and a respective density kit. In all experiments described here distilled water was used as submerging fluid. With *equation (3)* the density of the sample was calculated. The mass of the copper layer was determined by subtracting the mass of an uncoated wafer from the mass of the actual sample. This procedure was repeated for the mass submerged in water.

$$\rho_{(sample)} = \frac{m_a * \rho_{(fluid)}}{m_a - m_f} \tag{3}$$

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2.3.2 Helium pycnometry

The principle of pycnometry is based on Boyle's law which is used to calculate the volume of the sample by measuring the gas pressure [28]. Theoretically every gas can be used, but according to the almost ideal gas behaviour and its negligible adsorption tendency helium is preferably used [28]. The measurements were performed on a *Quantachrome Ultrapycnometer 1000* with a custom-made sample chamber designed for optimized space filling by the samples – *Figure 12*. In this chamber between 5 (coated wafers) and 7 (uncoated wafers) were able to be measured at once. *Figure 13* shows a control diagram of the helium pycnometer.

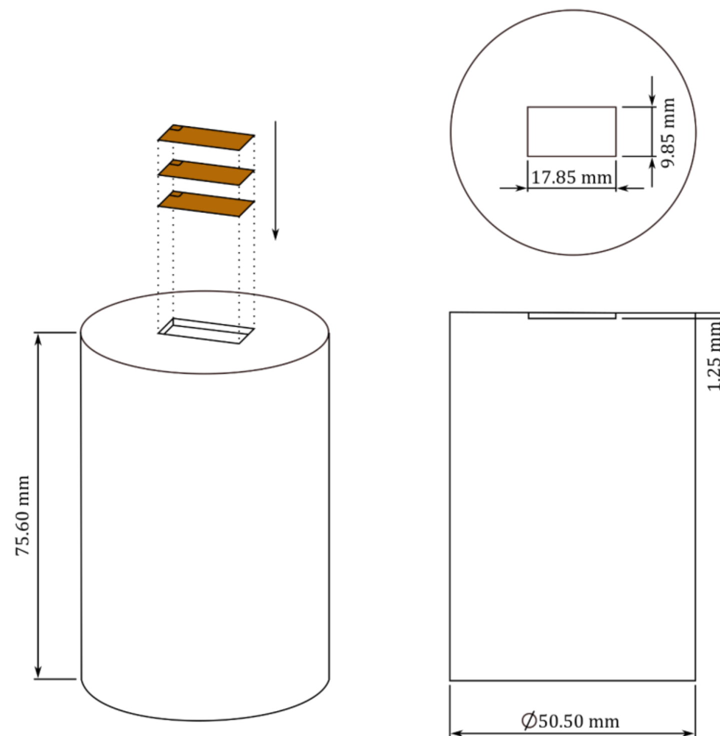

Figure 12 – scheme of custom-made sample cell for a Quantachrome Ultrapycnometer 1000

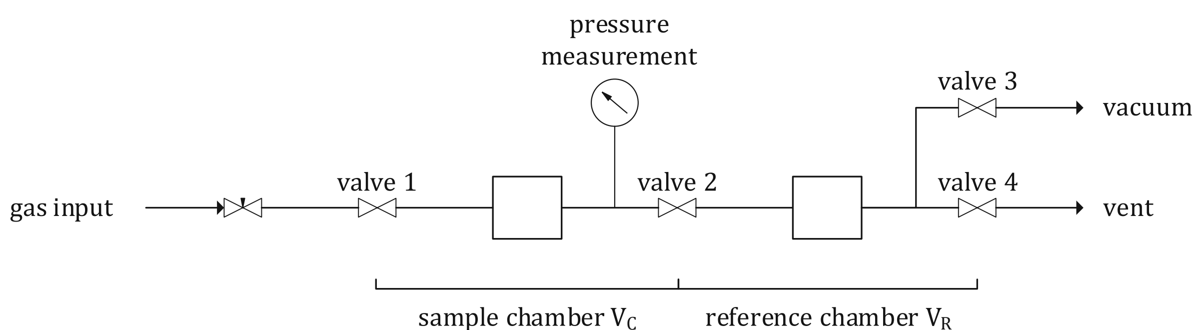

Figure 13 - flow diagram of a helium pycnometer

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The measurement itself consisted of 3 steps:

1. The sample is put in the respective chamber. Depending on the operation mode, both chambers are either evacuated first and then purged with helium (vacuum mode) or directly purged several times with helium (purge mode).
2. Both chambers are separated (*valve 2* was closed). The sample chamber is then pressurized with helium to pressure p_2.
3. *Valves 1 - 4* are closed. Now *Valve 2* is opened and the chambers are connected again. The pressure decades to p_3.

As helium behaves almost like an ideal gas, its state can be described with de general gas equation – *equation* (*4*).

$$\boldsymbol{p} * \boldsymbol{V} = \boldsymbol{n} * \boldsymbol{R} * \boldsymbol{T} \tag{4}$$

Starting with *equation* (*4*), knowing the volumes of the chambers of the pycnometer and measuring the pressures of the gas as described above, one can calculate the samples volume by *equation* (*5*).

$$\boldsymbol{V_S} = \boldsymbol{V_C} + \frac{\boldsymbol{V_R}}{\mathbf{1} - (\boldsymbol{p_2}/\boldsymbol{p_3})} \tag{5}$$

In contrast to the previously mentioned Archimedes method, helium pycnometry analyses only the closed porosity. This is because the helium gas penetrates the open pores and thereby their volume is not considered for the analysis of the sample.

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2.3.3 Image analysis

The image analysis was executed with the software ImageJ. For the determination of the porosity via image analysis SEM pictures were used. In a first step the images were converted into an 8-bit greyscale version. Further a threshold was set and used to create a binary picture with the pores set to the colour black and all surroundings to white. While the software offers several methods for thresholding it was found that the automated thresholding procedure pictured the pore structure very well. This procedure is based on an algorithm, that sets an initial threshold and calculates the average values of pixels above and below the threshold. Then it increments the threshold and repeats the procedure until the threshold exceeds the composite average which is defined as shown in *equation (6)*.

$$\boldsymbol{composite\ average} = \frac{\boldsymbol{av.\,below\ TH + av.\,above\ TH}}{\mathbf{2}} \tag{6}$$

The porosity was then calculated by comparing the black and white pixel. *Figure 14* demonstrates the conversion of the pictures.

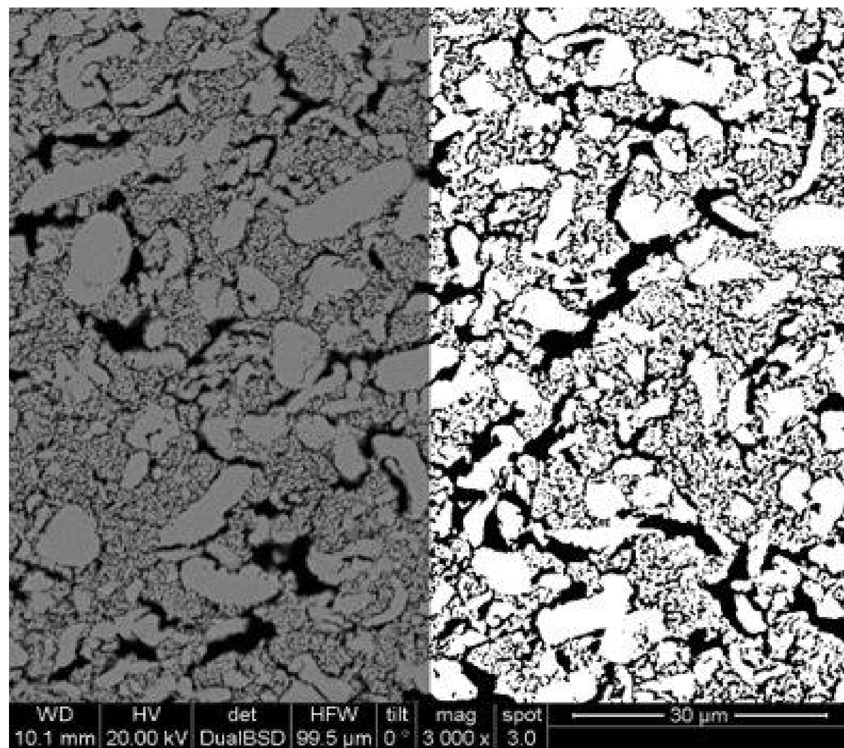

Figure 14 - exemplary picture showing the conversion of the original image (left) to the binary version (right).

For the analysis of the pore size distribution a simplification was necessary, as one can clearly see that especially the large pores have no particular symmetrical shape. Under the assumption of a similar behaviour in all directions, the pore size distribution was thereby approximated by the analysis of the pore areas visible in the images.

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2.4 Chemical analysis

2.4.1 X-ray analysis

For the elemental analysis of the copper layer as well as the seed layer and diffusion barrier coatings energy dispersive x-ray (EDX) analysis was used. Especially for the interface between wafer and coating layer angled cuts – *see section 2.2.2* – were used. The analysis was performed on a *Quanta-200 SEM* with respective detector for EDX analysis.

2.4.2 Infrared analysis

As difficulties with the wire bonding process occurred frequently, the copper layer was analysed regarding oxidation and carbon contamination. The analysis was performed by infrared spectroscopy on a *LECO CS230* for measuring the carbon content and on a *LECO TC400* for the oxygen content.

Oxygen analysis: The analysis of oxygen content is based on the absorption of infrared radiation by carbon monoxide (CO). To convert oxygen entirely to CO, samples are put in carbon crucibles which are then electrically heated. The degassing CO is directed by helium as carrier gas to the IR cell, where the absorption is measured.

For this analysis the whole wafer was used. First a blank was measured by using an uncoated wafer in a graphite crucible. The analysis of the copper layer was performed in the same way differing only in the wafer used.

Carbon analysis: As the edges of the IGBT wafer were coated with imides and thereby to avoid potential corruption of the measurement, the copper layer had to be separated from the rest of the wafer. This was achieved by mechanically separating the porous layer via scratching. From a single chip an average of a few milligrams porous copper could be obtained by scratching which was not sufficient for reliable results. To overcome this problem, for a single carbon analysis 15 to 20 wafers were used to gain an adequate amount of copper.

For the analysis itself, the sample was burned under oxygen atmosphere converting all existing carbon to carbon dioxide (CO_2) which can be detected very well by an infrared detector.

The carbon content of the samples was expected to be very low making it obligatory to remove potential adsorbed carbon containing gases from the crucibles. To do so, the crucibles were heated to 1100 °C, held at this temperature for 3 hours and then stored in a closed environment.

After an evaluation of the first results, an additional step was included to the sample preparation procedure. During this step, the copper scratches were treated with moistened hydrogen at 600 °C for 30 minutes. The moistening of the hydrogen was performed with a gas washing flask.

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3 RESULTS & DISCUSSION

3.1 Structural analysis

3.1.1 Surface analysis

As the connection and thereby the integration of the device covered by the printed copper layer via wire bonding is a desired goal, the investigation of the surface is a natural first step to gain an idea of the composition of the layer.

The surface of the "mixed" sinter paste samples – *Figure 15 (a - b)* – reflects the initial powder composition. One can clearly see the two different particle sizes represented on the surface, starting with big dense particles sitting in between or being embedded in porous areas of sintered copper representing the fine powder share of the mixture. A similar context can be found in regards of porosity. Areas of fine porosity in the submicron region are alternating with micro scale crack shaped pores. By comparing the surface of sintered samples *Figure 15 (a – b)* with pressure sintered samples *Figure 15 (c – d)* it is interesting to see, that the additional pressure sintering step seems to have no influence on the surface at all.

In terms of the "nano" sinter paste samples one can clearly see a much more homogeneous surface structure compared to the "mixed" sinter paste samples – *Figure 15 (e)*. The porosity of this layer also represents the mono sized powder from which it originates and thereby comes with a very consistent pore size distribution. Also the "nano" scale is represented as a much higher magnification was needed to resolve the surface.

By taking a closer look on *Figure 15 (f)* one can see single sinter necks between powder particles and it becomes apparent, that this porous layer is not a cluster of independent pores but a system of interconnected pores.

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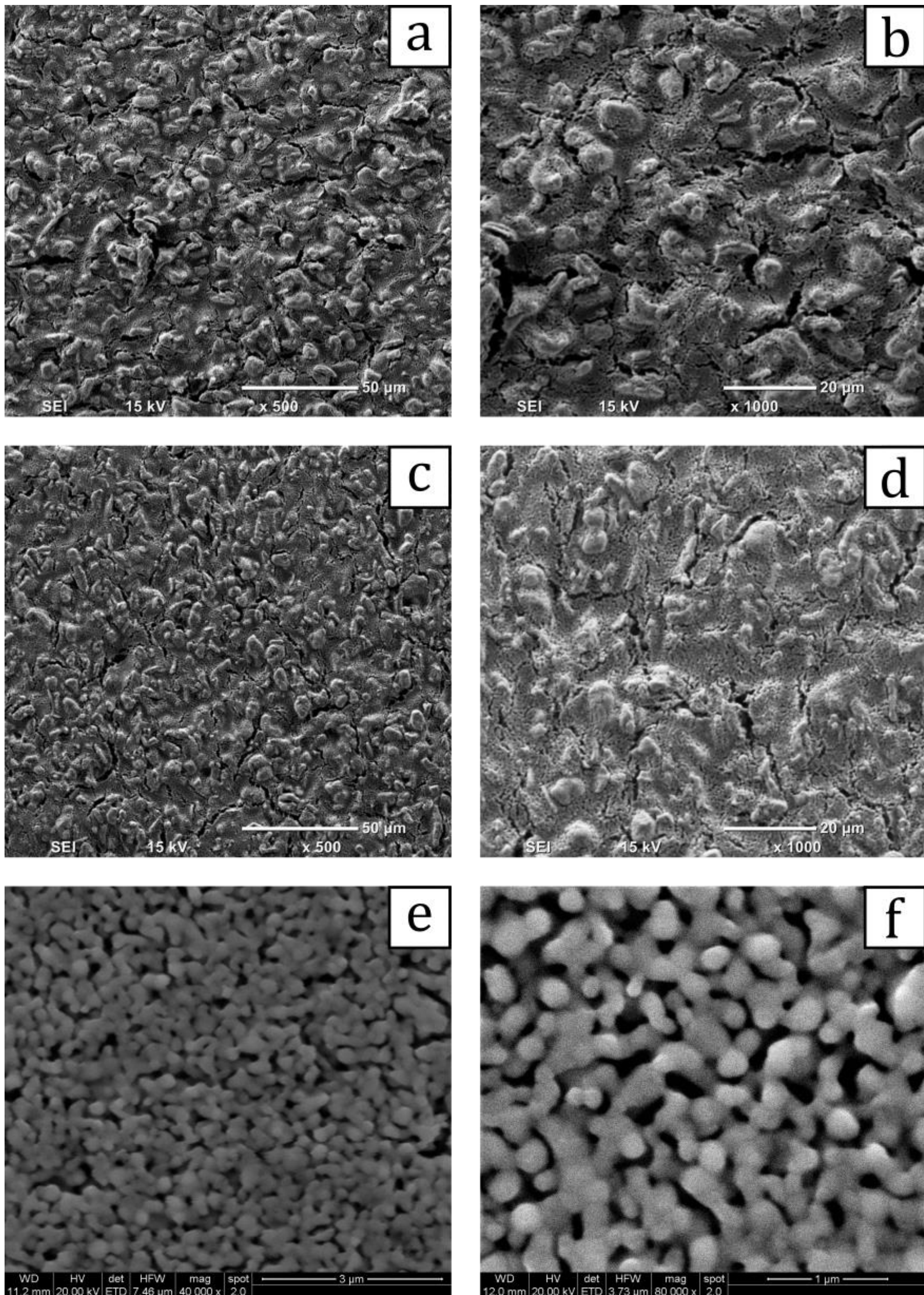

Figure 15 – SEM images of the surface of the copper layer: (a - b) sintered "mixed" paste samples, (c - d) pressure sintered "mixed" paste samples, (e - f) pressure sintered "nano paste samples

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3.1.2 Metallography and microstructure

The metallography of the samples did not only enable a close investigation of the microstructure of the copper layer but also of the interface between diffusion barrier and the printed copper layer.

Based on a first investigation of the angled cut samples the diffusion barrier coating and the copper seed layer was analysed regarding their basic structure and thickness. The chemical analysis of this layers can be found in *section 3.4.1*. Even without knowing the exact elemental composition of the interface, the backscattered electron detector – BSD – clearly reveals the existence of at least four layers consisting of different elements. In *Figure 16* the diffusion barrier coating as well as the copper seed layer is shown from an angled cut. Enclosed in the second and fourth layer as well as in the silicon waver one can see square shaped structures. The structures in the second layer seem to also contain porous material.

As a direct connection of these structures to the porous copper layer was not found, and they do not appear in the cross cuts, they were not further investigated.

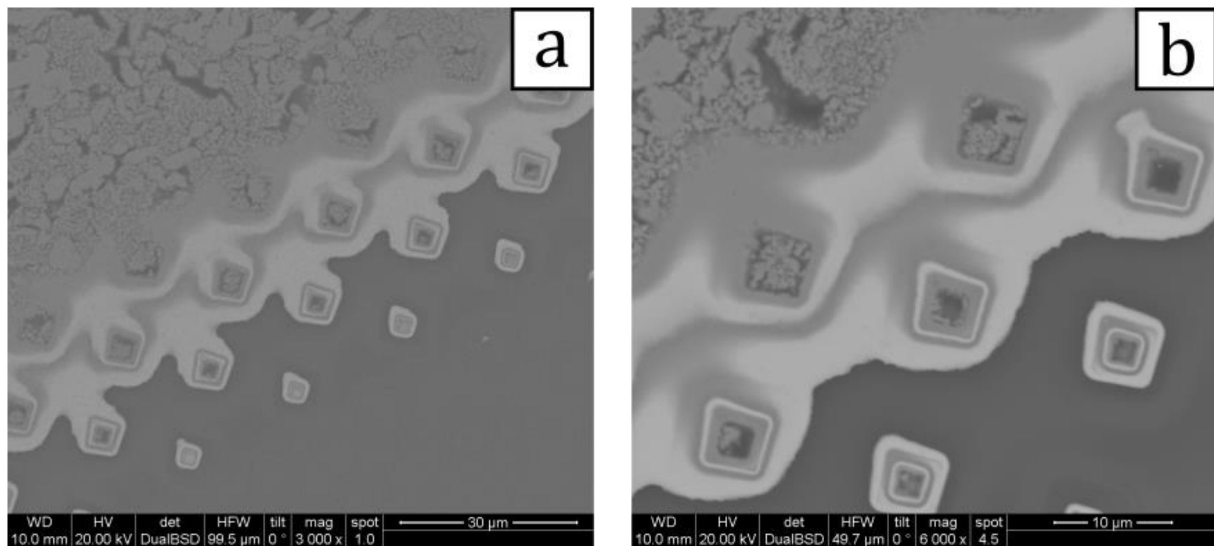

Figure 16 – SEM images of an angled cut showing the diffusion barrier coating and thereby the interface between copper layer and wafer

Table 4 – thicknesses of diffusion barrier layers

Layer 1 (µm)	Layer 2 (µm)	Layer 3 (µm)	Layer 4 (µm)
0.62 ± 0.09	0.30 ± 0.03	0.51 ± 0.09	0.61 ± 0.04
Layer 1 is the seed layer – the top layer of the diffusion barrier			

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By studying the microstructure of the “mixed” paste samples – *Figure 17 & Figure 18* – one can clearly see the bimodal nature of the paste. Even at lower magnification it is possible to determine between dense areas originating from micro scale powder particles, large microscale pores and “nanoporous” areas. An overview on where to find the microstructure of each individual sample is given in *Table 5*

The analysis of the interface of these samples showed a very good connection between diffusion barrier and printed copper. *Figure 17* shows that the sintered samples, as well as the pressure sintered samples, formed numerous sinter contacts with the top layer of the diffusion barrier and have established a stable connection to the wafer.

By comparing the microstructure of the sintered samples with the microstructure of the pressure sintered samples, there seems to be no differences.

However, by taking a closer look on the top end of the copper layer, which represents the surface, a difference between the sintered and the pressure sintered samples can be seen. These findings are contrary to the results of the direct surface analysis from – *section 3.1.1*. Especially in the LOM images in *Figure 18* one can see, that the surface flattened compared to the surface in *Figure 17* which comes with a rougher nature.

Table 5 – assignment of individual samples to images

		Sample	**Figure**
"mixed" paste	sintered	VE041888 #3	Figure 17 a - b
		VE043977 #8	Figure 17 c - d
		VE043977 #22	Figure 17 e - f
	pressure sintered	Group 1	Figure 18 a- b
		Group 4	Figure 18 c - d
		Group 7	Figure 18 e - f
"nano" paste	pressure sintered	Group 1	Figure 19 a - b
		Group 2	Figure 19 c - d
		Group 3	Figure 20 a - b
		Group 4	Figure 20 c - d

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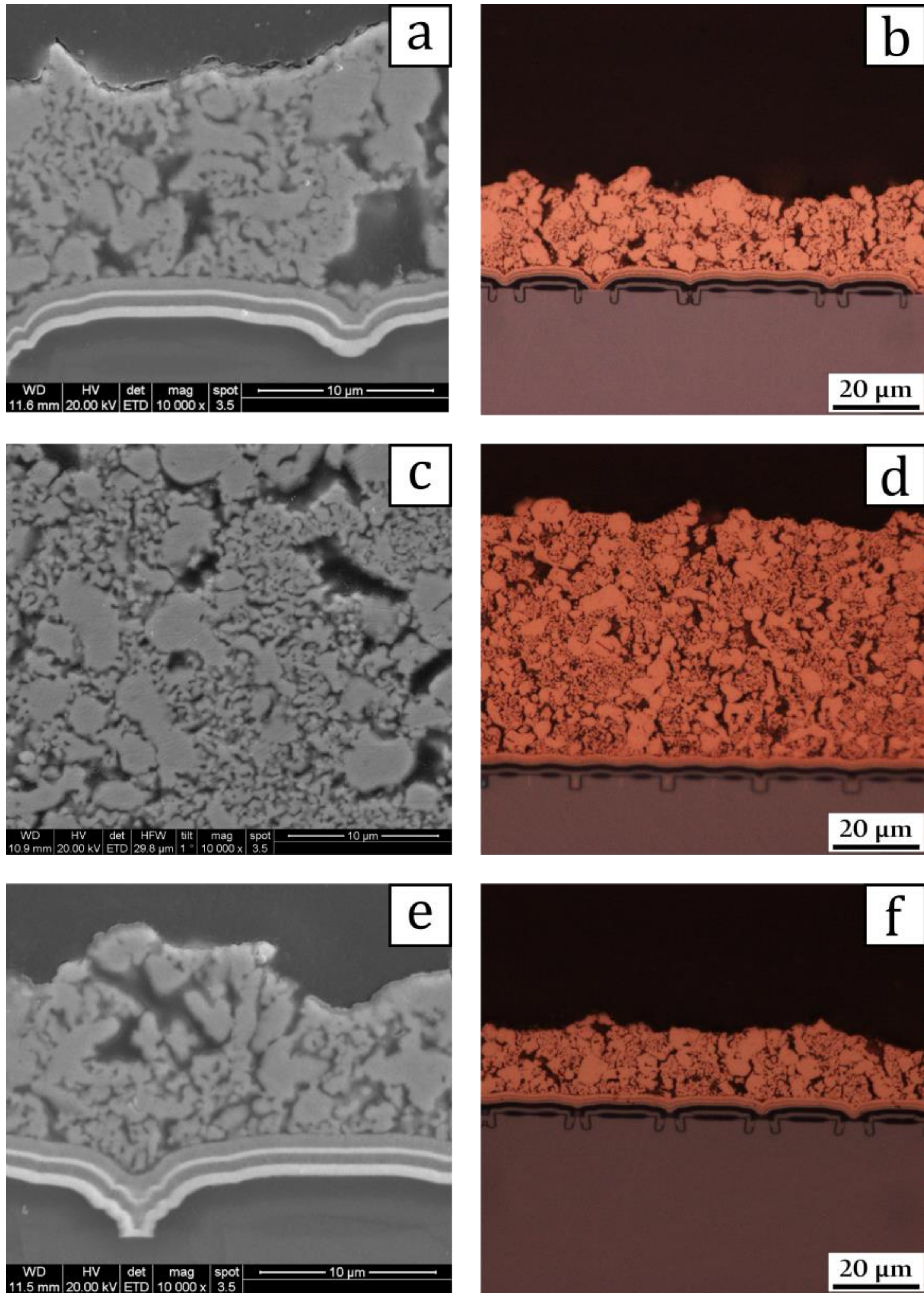

Figure 17 – SEM and LOM images of metallographic cross cuts of sintered "mixed" paste samples: (a & b) VE041888 #3, (c & d) VE043977 #8, (e & f) VE043977 #22

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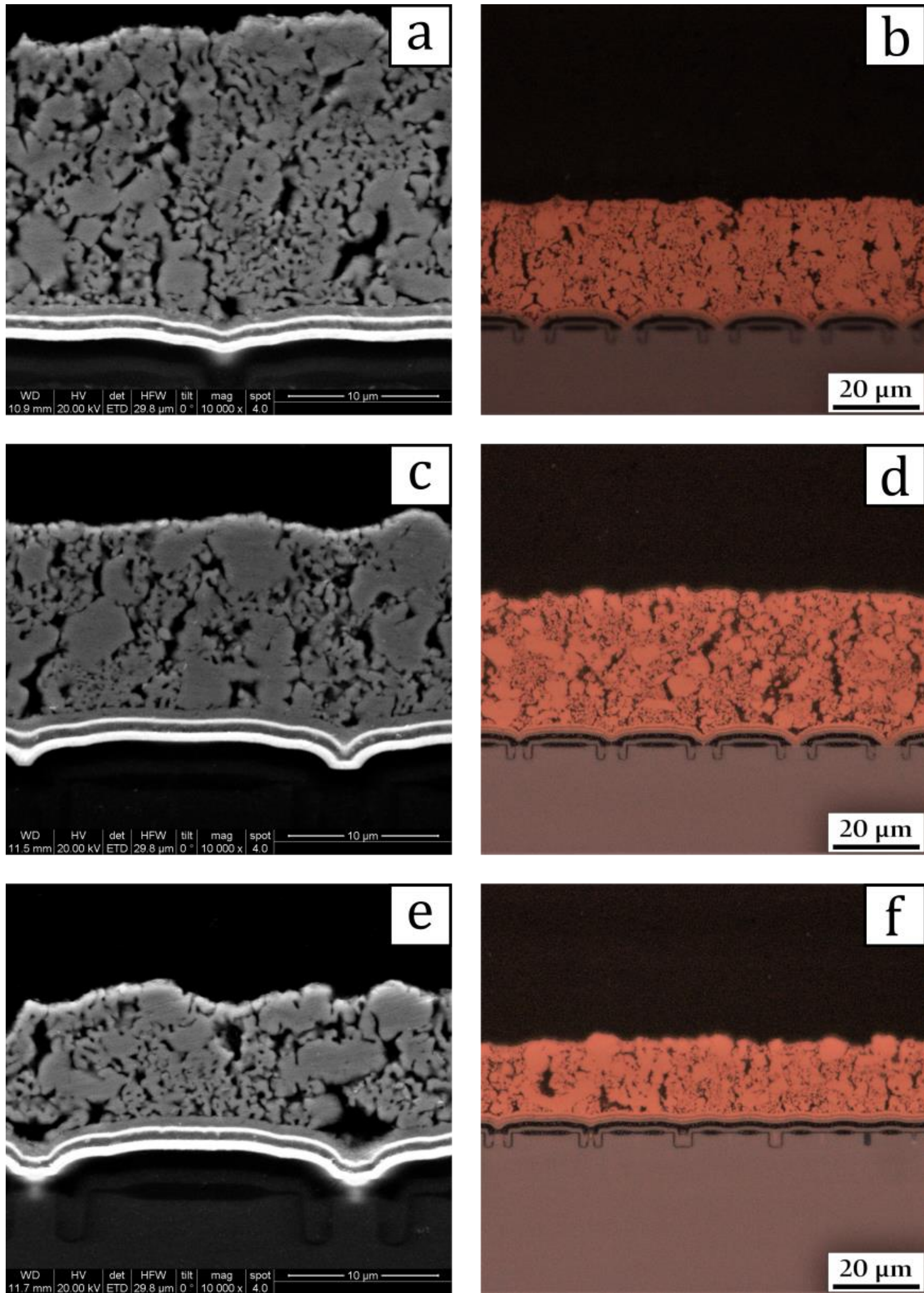

Figure 18 – SEM and LOM images of metallographic cross cuts of pressure sintered "mixed" paste samples: (a & b) Group 1, (c & d) Group 4, (e & f) Group 7

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The “nano” paste samples had a very homogenous microstructure – *see Figure 19* and *Figure 20* . This perfectly represents the unimodal particle size distribution of the “nano” paste. During the metallographic analysis of these samples, however, several issues were identified, demanding a closer investigation.

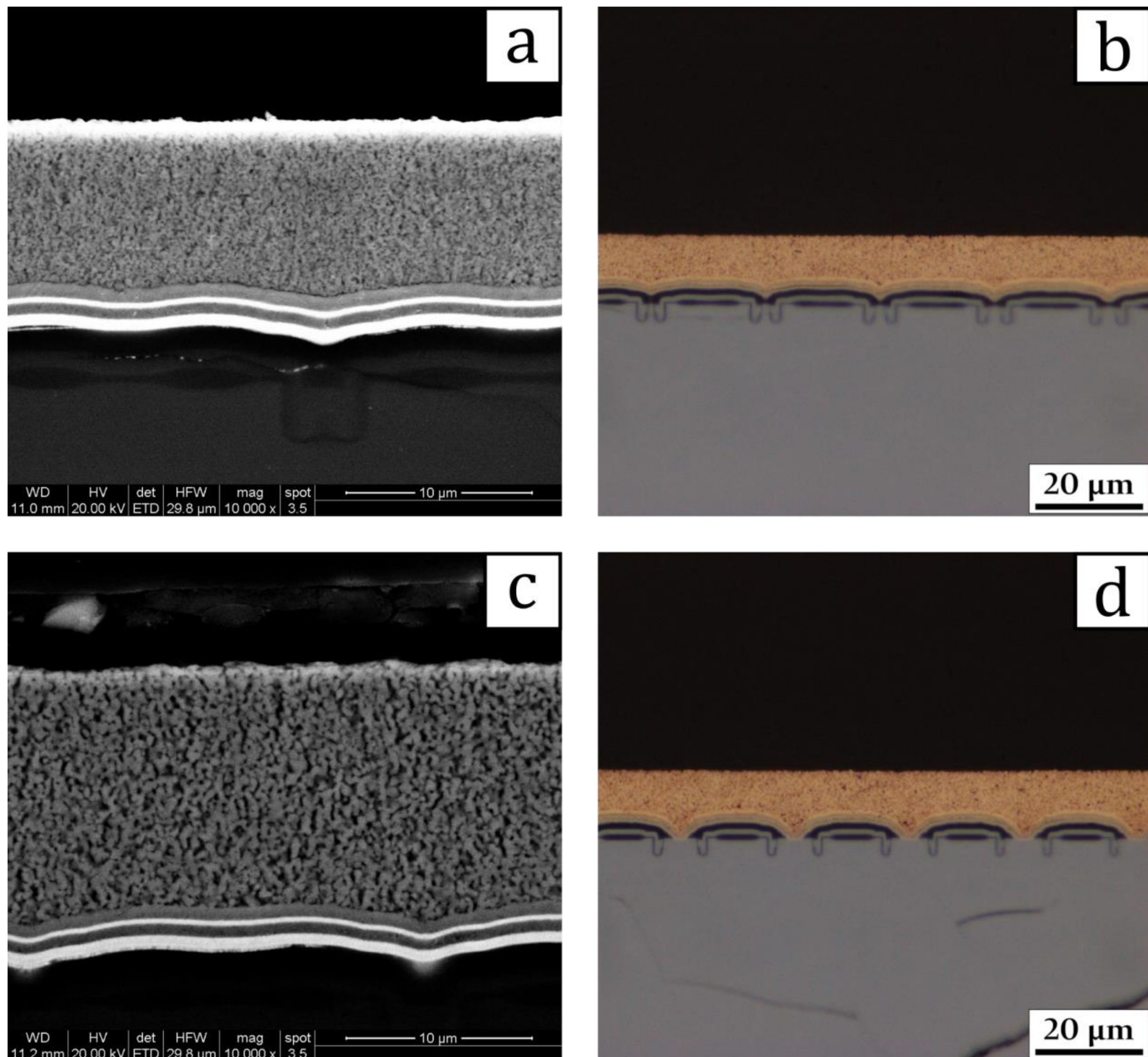

Figure 19 – SEM and LOM images showing the microstructure resulting from the "nano" paste samples: (a – b) Group 1; (c – d) Group 2

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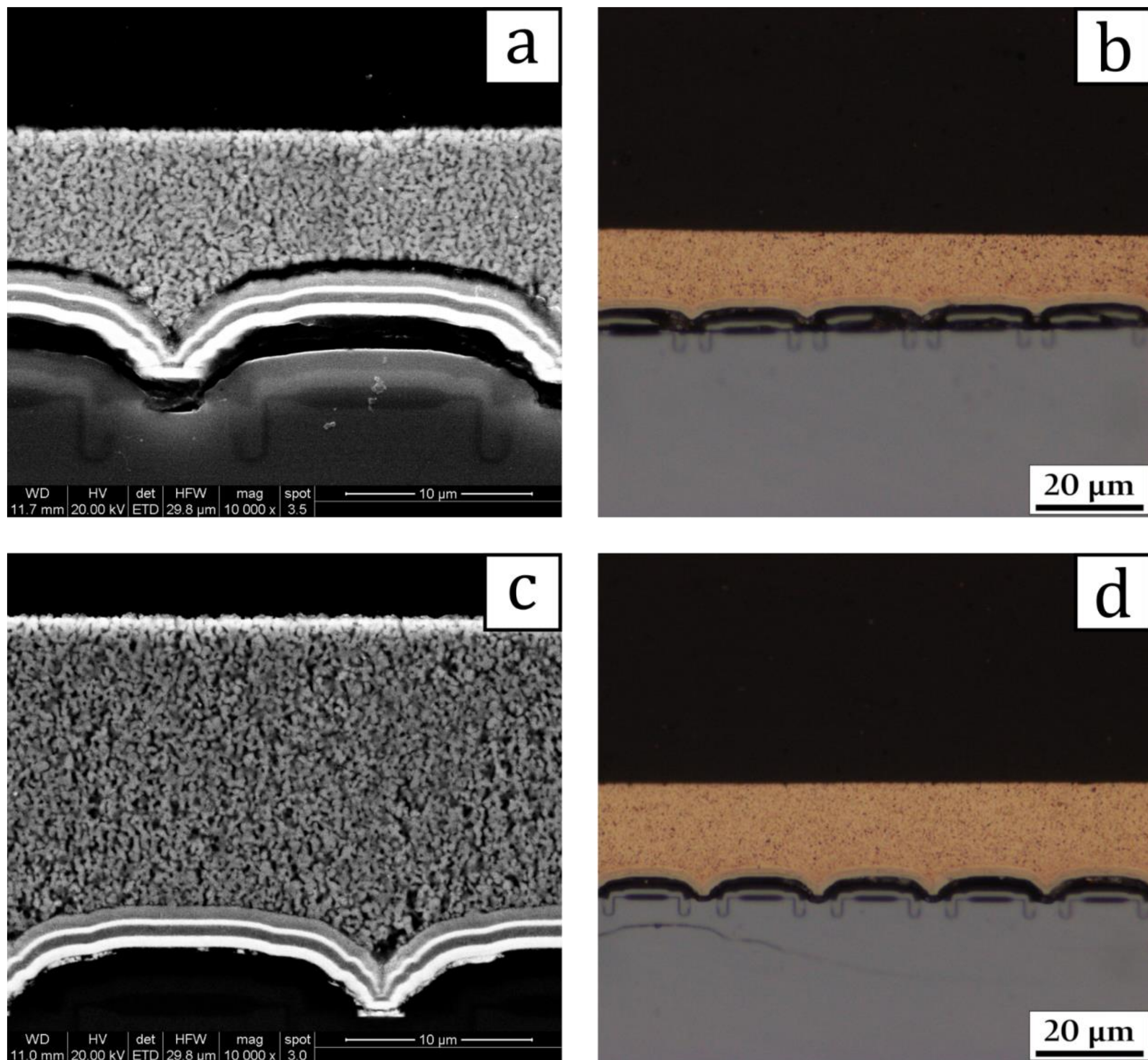

Figure 20 – SEM and LOM images showing the microstructure resulting from the "nano" paste samples: (a – b) Group 3; (c – d) Group 4

Over wide areas of the metallographic cross cuts the printed copper layers showed almost no contact to the diffusion barrier below – *see Figure 21 (a - b)*. However, despite no contact the layer appears to mimic the shape of the surface below. Reasons for this behaviour are yet to be determined. The absence of sinter contacts over wide areas, and more important, no fracture signs of sintered contacts, indicate a problem in the sample production before or while sintering. In *Figure 21 (c – d)* one can see that in constricted areas on the wafer below the delamination is sometimes interrupted. Further it can be seen that the void spaces between copper layer and wafer are in some cases partially filled with porous copper, which seems to have formed sinter contacts to the diffusion barrier coating – *Figure 21 (c)*. None the less, there appears to be no connection between the copper layer and these "filled areas" as the shape of the void spaces can still be seen.

A possible explanation for this behaviour might be given by the fact that the sinter activity of the powder particles should exceed the one of the seed layer by far due to their small size. This would however not explain why the copper layer in some cases forms sinter contacts with the seed layer as shown in *Figure 21 (d).* Those contacts might have formed as a result of the pressure sintering step, as the mechanical load could have helped enabling sinter contacts to the seed layer. Still the filling of the void spaces as shown in *Figure 21 (c)* cannot be explained by this theory.

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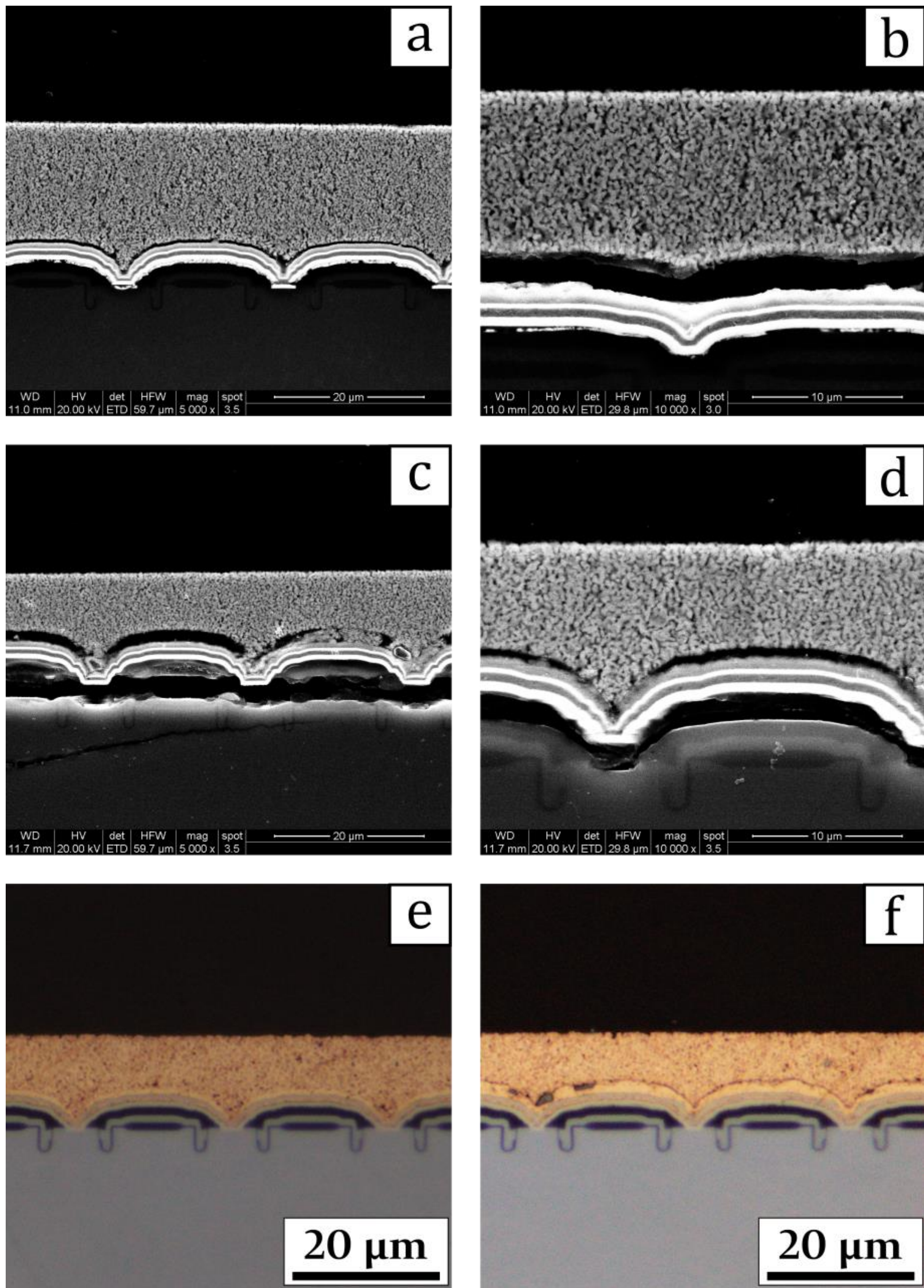

Figure 21 – SEM images of "nano" paste samples showing almost complete delamination of the copper layer (a & b), partial filling of the resulting void spaces (c), interruption of the delamination in constricted areas of the wafer (d), and optical microscope images comparing differences in the seed layer

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In this regard it is worth discussing *Figure 21 (e – f)*. The dense copper layer on top of the diffusion barrier in the optical microscope is clearly variating in its thickness. The first impression is that a parameter during the sputtering process was changed, which resulted in a thicker layer. A more likely explanation could be, that the dense layer was mistaken as seed layer, and following appears to be a complete filling of the void space between porous copper layer and diffusion barrier coating. In this case it is not clear why or how the filling material in *Figure 21 (f)* appears to be dense and not porous like in *Figure 21 (c).*

In *Table 6* screens the results of the analysis of this thicker seed layer/dense filling regarding its thickness as well as the deviation from the regular seed layer.

Table 6 – analysis of the seed layer in Figure 21 f

thickness layer (µm)	deviation from regular seed layer (%)
1.56 ± 0.25	39.74 ± 20.6

On the other hand, the additional pressure sintering step might also have caused some sort of “spring back” effect when the mechanical load was removed after sintering. This could explain the mirroring shapes of the copper layer and the wafer below.

Further a possible amplifying effect for these failures in the layer might be the mechanical stress upon preparation of the samples. Beneath the diffusion barrier coating one can see fractions in the silicon waver which are most likely a direct result of this mechanical load.

In context of mechanical stress, another phenomenon, which only occurred in “nano” paste samples has to be mentioned. During the sample preparation, some areas of the copper layer broke out of the embedded specimen. The possibility that the mechanical stress during the sample preparation caused the breakout cannot be neglected, nevertheless it is worth to investigate as none of “mixed” paste samples faced the same problems. *Figure 22* shows an example of such a breakout area.

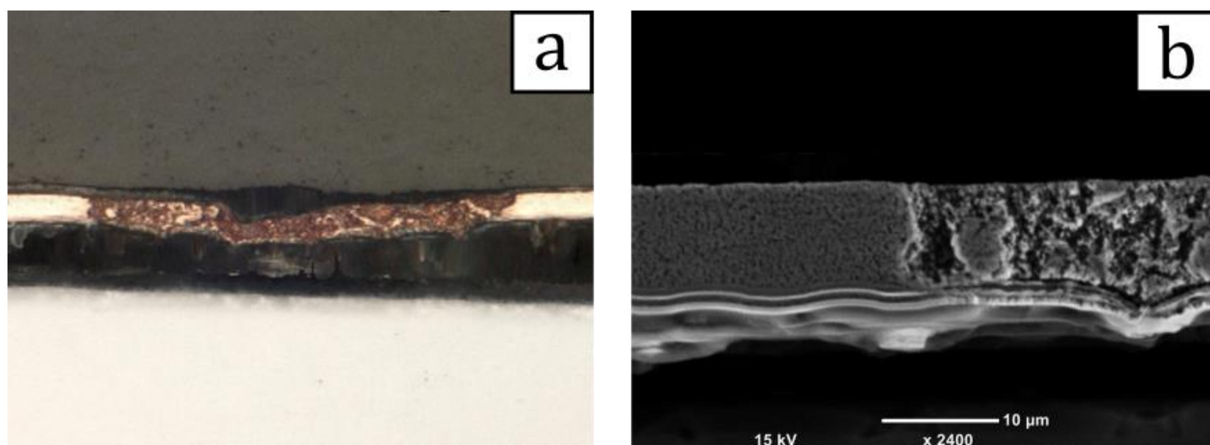

Figure 22 – 3D stack optical microscopy (a) and SEM image (b) of broken area in the copper layer*

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3.1.3 Topographical analysis

During the metallographic analysis of the crosscuts a strong fluctuation in the layer thickness was found. In order to gain reliable information of the layer thickness throughout the entire wafer topographical analyses were performed. Because the enormous amount of data needed for this kind of analysis, the wafer was separated into two sections which were analysed separately. The resulting images were then combined.

The first results – *see Figure 23 (a)* – indicated that the printed copper layer reaches its maximum thickness in the middle of the respective wafer. These results were not expected, as they fundamentally contradict the results of the metallographic analysis of the layer thickness.

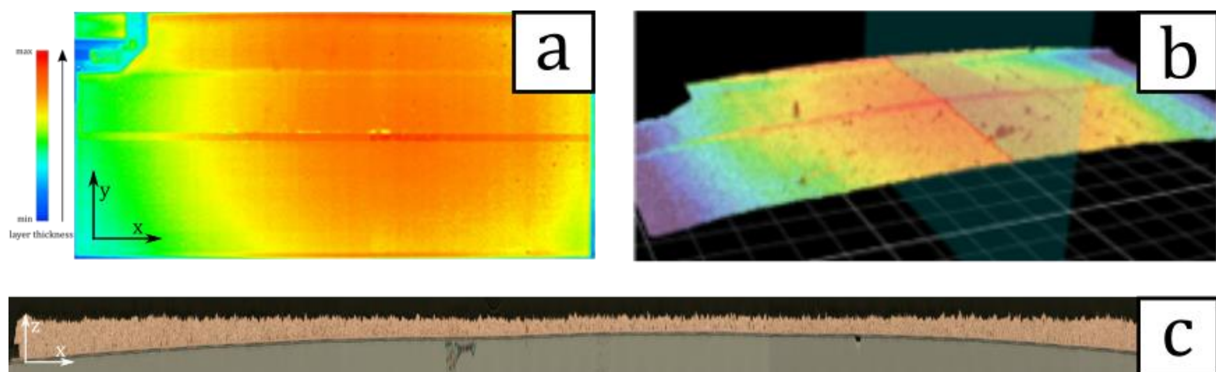

Figure 23 - Topographical heatmap of a sintered sample (a) 3D scan of uncoated wafer showing convex curving (b) and metallographic crosscut along y-axis with contradictory results regarding layer thickness (c)

To explain these contradictory measurements, the shape of uncoated wafer was investigated. The results of this investigation found that they were curved in a convex way – *see Figure 23 (b – c)*.

As a result of these findings, a tilt correction was applied to the measured topographical heatmaps. Further to verify the resulting heatmaps, metallographic crosscuts of every scanned wafer were prepared, polished and panorama pictures taken. Furthermore, these images were not only used for a qualitative verification of the heatmaps but also for a quantitative investigation of the actual layer thicknesses. In *Figure 24* the tilt corrected heatmap and the corresponding metallographic crosscuts of a sintered "mixed" paste sample are shown. It must be mentioned that the panorama pictures are stretched in hight by a factor of 10 to be able to show the entire cross section while keeping the copper layer visible. *Table 7* sums up the layer thicknesses and the respective minimum and maximum values of each sample.

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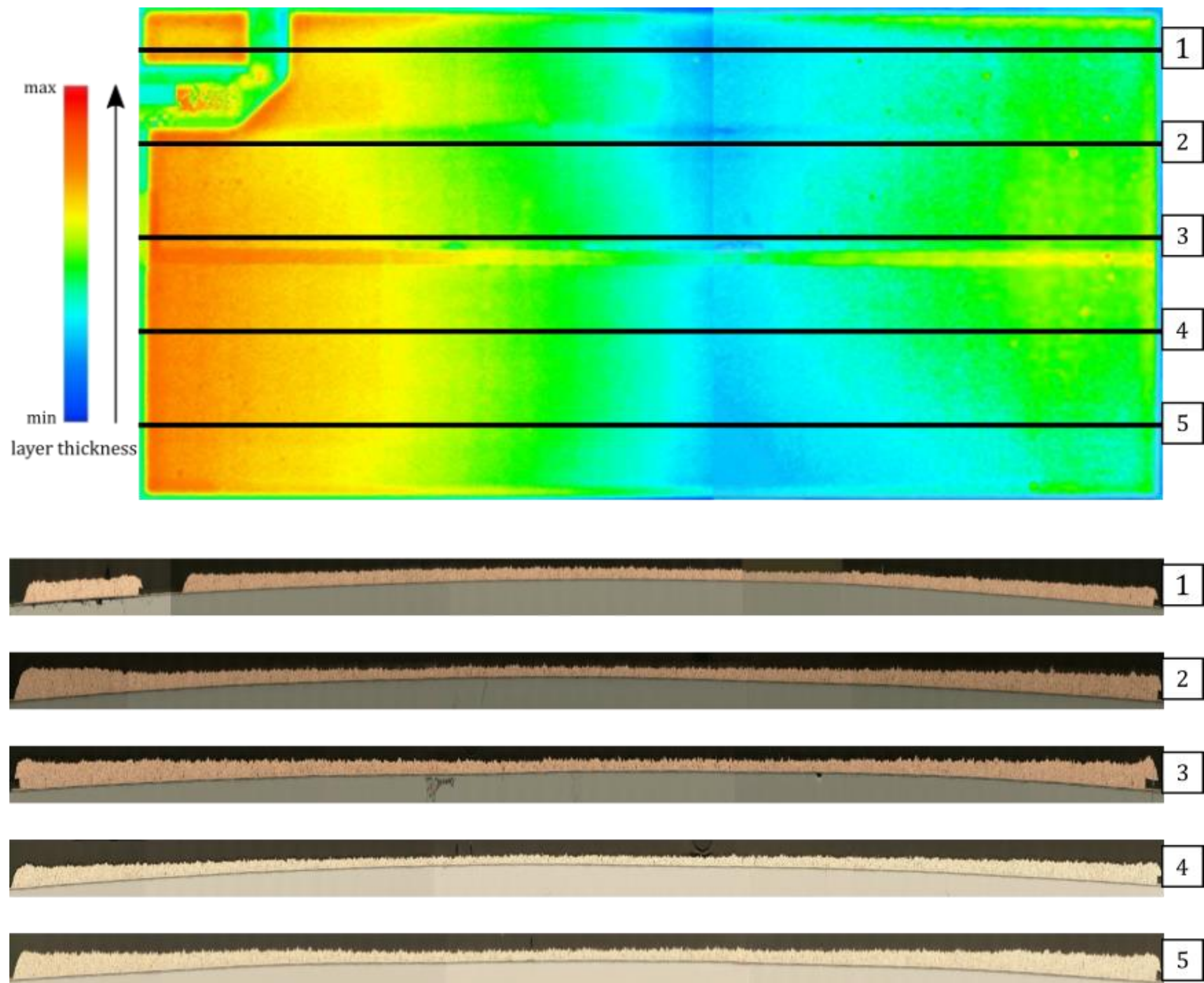

Figure 24 – tilt corrected heatmap and respective metallographic cross cut panorama pictures of sample VE041888 #3

Both the metallographic cross cuts as well as the corrected heatmap clearly point out, that the layer thickness strongly variates and reaches its minimum in the middle of the waver, while the maximum is located at the left edge. This information is of special interest, as wire bonding also takes place in the middle of the waver and Infineon Technologies Austria AG repeatedly reported difficulties with this interconnecting technology throughout the project.

To investigate a possible connection between the reduced layer thickness in the bonding area and the failure of the wire bonds, Infineon Technologies Austria AG provided SEM images [45] of previous successful wire bond interconnects for comparison. In *Figure 25 (a)[45]* a wafer after successful bonding as well as the respective cross cuts are shown. The wafer was produced under similar parameters than the sintered "mixed" paste samples. *Figure 25 (b)* shows sample VE043977 #8 – *see Table 2* – and the layer thickness is equal to the one used in *Figure 25 (a)*. In *Figure 25 (c)* a pressure sintered sample is shown which, according to Infineon Technologies Austria AG, showed difficulties with wire bonding.

It is clearly visible, that the pressure sintered sample comes with a thinner copper coating than previous samples which are reported to have no problems with wire bonding.

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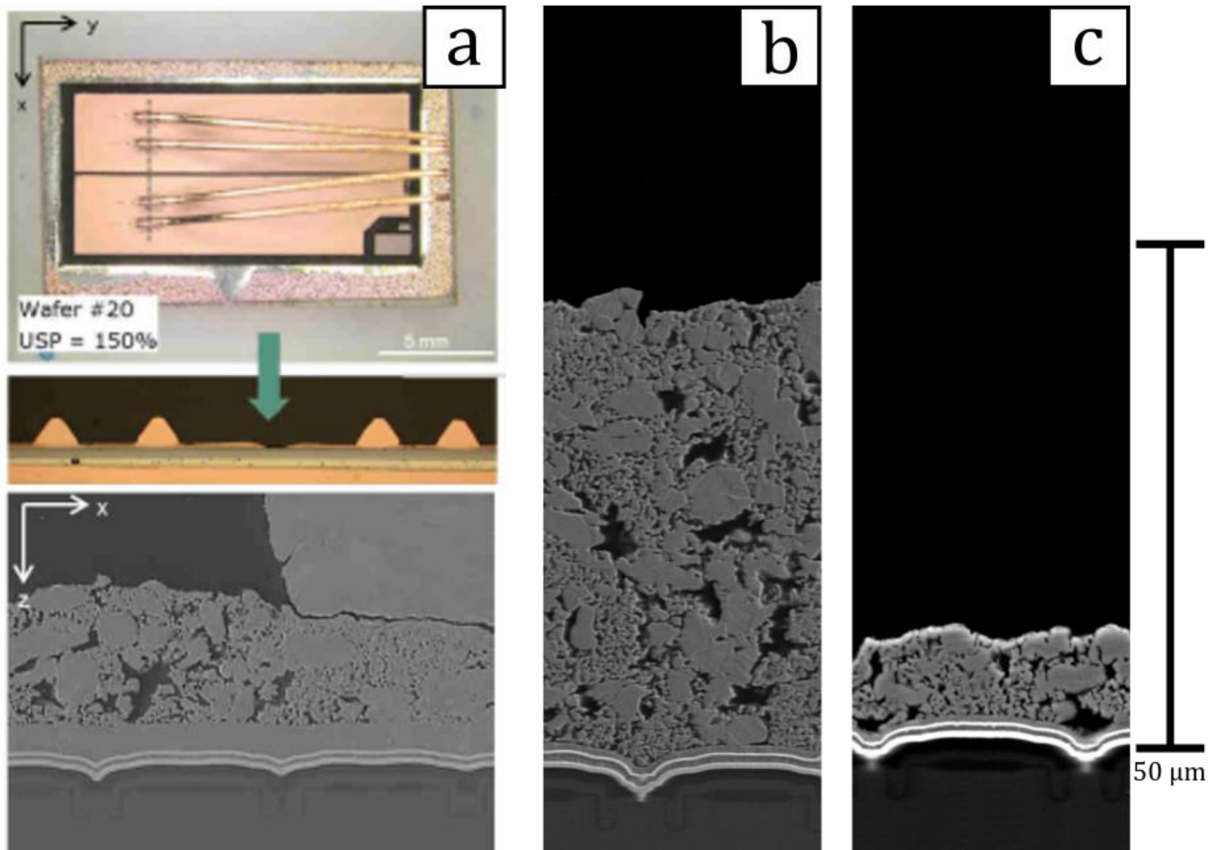

Figure 25 – wire bonded wafer and respective metallographic cross cuts (a)[45], cross cut of sintered "mixed" paste sample with similar layer thickness (b) and cross cut of a pressure sintered "mixed" paste sample (c)

With the finding of the convex nature of the silicon wafers – *Figure 23* – it seems possible that the force applied to the copper layer during pressure sintering is not equally distributed across the wafer. This could in theory lead to a higher densification of the copper layer in the middle of the wafer where the curvature reaches its maximum. A closer look on this issue will be taken in *section 3.3*.

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Table 7 – layer thicknesses of the printed copper layers

	sample	mean thickness (µm)	max. thickness (µm)	min. thickness (µm)
"mixed" sinter paste	VE041888 #3	24.68 ± 9.35	39.25	12.96
	VE043977 #8	58.85 ± 10.15	72.85	45.75
	VE043977 #22	16.69 ± 5.30	29.26	6.91
	Group 1	16.69 ± 6.61	29.26	6.91
	Group 4	20.44 ± 6.94	35.74	12.17
	Group 7	23.07 ± 7.33	31.22	7.27
"nano" sinter paste	Group 1	8.02 ± 1.35	10.3	4.35
	Group 2	10.87 ± 2.33	14.65	7.44
	Group 3	10.32 ± 3.76	16.73	3.87
	Group 4	13.80 ± 2.56	19.05	8.46

Considering the printing parameters, with a special focus on the printing thickness – *see Table 2* – and further comparing it to the measured mean layer thicknesses in *Table 7,* one can identify a clear difference between the "mixed" sinter paste and the "nano" sinter paste in the pressure sintered state. Even though both sample sets were printed in a thickness of 60 µm, the "nano" paste samples show a significantly lower layer thickness after sintering. Vice versa this means that in order to reach a similar layer thickness compared to the "mixed" sinter paste, one needs to increase the printing thickness.

This is most likely due to the much finer powder in the "nano" sinter paste, as finer particles are known for showing increased sinter activity and thereby also can show higher shrinkage upon sintering – *see section 1.3.3*.

Further one can also partly confirm the impression from *section 3.1.1* that the "nano" paste samples come with a more homogeneous surface as the respective standard deviation of the mean layer thickness for these samples is also lower compared to "mixed" paste samples.

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3.2 Porosity analysis

As described in *section 2.3* for the determination of the porosity of the copper layer, the share of the respective wafer had to be subtracted. For this reason, the density of the blank uncoated wafer was analysed with Archimedes method and helium pycnometry. The results can be found in *Table 8*.

Table 8 – density of uncoated wafer determined by Archimedes method and helium pycnometry

Archimedes method		helium pycnometry	
density (g/cm^3)	**std. deviation (g/cm^3)**	**density (g/cm^3)**	**std. deviation (g/cm^3)**
2.728	0.23	2.303	0.09

Based on these results the density of the copper layer was measured/calculated. In *Table* 9 the measured densities and the resulting calculated porosities are shown.

Table 9 – densities and corresponding porosities of sintered samples

	Archimedes method		helium pycnometry	
sample	**density (g/cm^3)**	**porosity (%)**	**density (g/cm^3)**	**porosity (%)**
VE041888 #3	4.76 ± 0.17	46.88 ± 1.87	6.12 ± 0.31	31.82 ± 3.54
VE043977 #8	5.53 ± 0.22	38.33 ± 2.47	5.91 ± 0.30	34.02 ± 3.35
VE043977 #22	4.35 ± 0.21	48.99 ± 2.38	4.83 ± 0.25	46.11 ± 2.84

The analysis of the pressure sintered samples showed strongly deviating results – *Table 10* . In some cases, the calculated porosity showed values smaller than zero, which would imply that the porous layer must consist of a material with higher density than copper. A more likely explanation for these results is the influence of the porous copper layer on the total mass of the sample. As described in *section 2.1* the samples were sintered to a DCB plate during the pressure sintering step. The fraction of the DCB plate remaining directly under the wafer heavily increased the total mass of the sample and at the same time reduced the share of the porous copper on the total mass.

The copper layer of the pressure sintered samples amounted for only ~1 % of the total mass. For this reason, the error of the measurements was strongly increased.

Further, the removal of the copper layer by etching increased the error, as the top layer of the diffusion barrier coating also consisted of copper and was thereby also removed by the acid.

In case of the helium pycnometry the measurements were complicated by the increased volume of the pressure sintered samples due to the DCB plate. For this reason, only one sample could be fit into the sample chamber of the pycnometer at a time resulting in low space filling. All these circumstances combined led to highly scattering values which were not reproduceable and made the determination of the layer porosity impossible.

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Table 10 – densities and corresponding porosities of pressure sintered samples

sample	Archimedes method density (g/cm³)	Archimedes method porosity (%)	helium pycnometry density (g/cm³)	helium pycnometry porosity (%)
Group 1	5.20 ± 1.24	41.96 ± 13.83		
Group 4	7.37 ± 3.79	17.76 ± 42.27		
Group 7	7.88 ± 1.39	12.06 ± 15.53		

Finally, as a complementary analysis the embedded samples from the metallography were used to gain information about the porosity by image analysis – *see 2.3.3 and 3.1.2*. This is also the only method which was found to produce reliable results for the "nano" paste samples. In *Table 11* the results of the image analysis can be found.

Table 11 – densities and corresponding porosities calculated by image analysis

		sample	density (g/cm³)	porosity (%)
"mixed" paste	sintered	VE041888 #3	6.47 ± 0.30	27.74 ± 3.35
"mixed" paste	sintered	VE043977 #8	5.89 ± 0.21	34.25 ± 2.31
"mixed" paste	sintered	VE043977 #22	6.33 ± 0.32	29.36 ± 3.55
"mixed" paste	pressure sintered	Group 1	7.03 ± 0.22	21.53 ± 2.43
"mixed" paste	pressure sintered	Group 4	6.89 ± 0.10	23.12 ± 1.16
"mixed" paste	pressure sintered	Group 7	7.09 ± 0.07	20.90 ± 0.76
"nano" paste	pressure sintered	Group 1	6.52 ± 0.53	27.26 ± 5.96
"nano" paste	pressure sintered	Group 2	6.97 ± 0.44	22.22 ± 4.94
"nano" paste	pressure sintered	Group 3	6.73 ± 0.39	24.41 ± 5.61
"nano" paste	pressure sintered	Group 4	6.83 ± 0.66	25.72 ± 7.23

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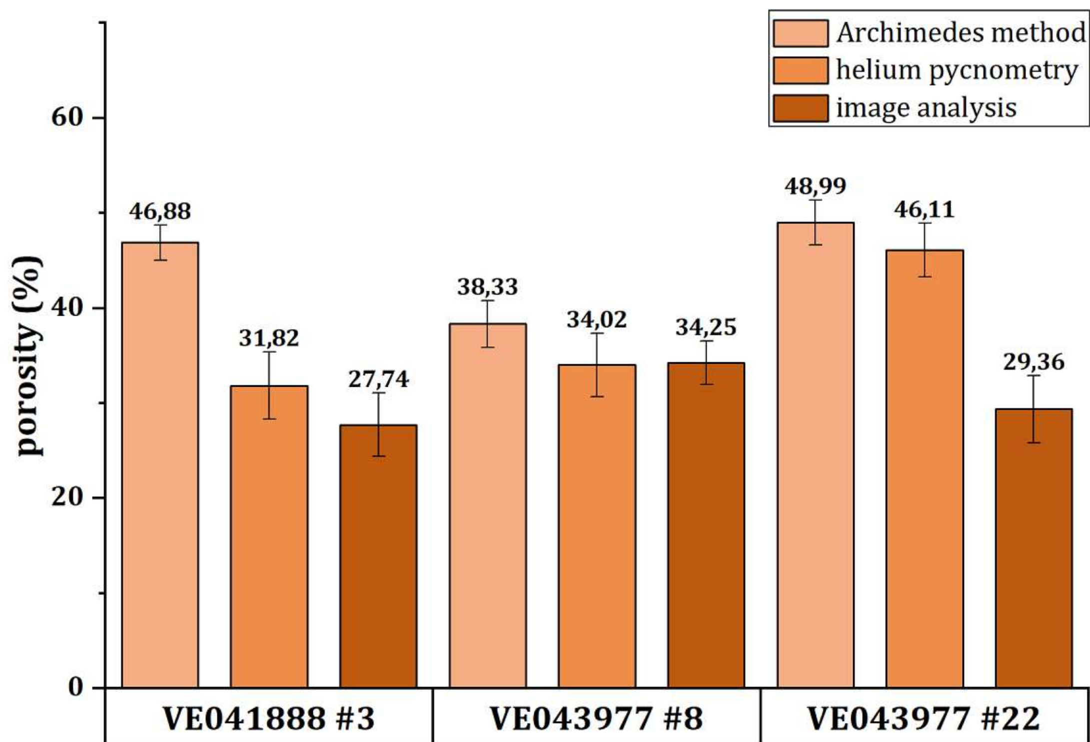

Figure 26 – comparison measured densities by different methods of sintered "mixed" paste samples

By comparing the results of the Archimedes method and the helium pycnometry one can see, that the samples appear to be denser in the helium pycnometry – *see Figure 26*. Per definition the fluid must not penetrate the pores for the Archimedes method – *see 2.3.1*, measuring the open porosity as part of the sample and thereby resulting in a lower density. In contrast to that the helium is especially chosen to penetrate the open porosity. The comparison of these two methods enables the differentiation between open and closed porosity.

It is also apparent, that the image analysis measures distinctly lower values for the porosity. For these results it has to be kept in mind, that the SEM images are not necessarily representative for the entire sample and further this method concludes from a two-dimensional image to a three-dimensional structure. Thereby the results have to be treated under the assumption of an isotropic distribution of pores and porosity across the entire sample. Under this point of view the error for the “mixed” paste samples definitively exceeds the one of the “nano” paste samples as they come with a much more homogenous microstructure and surface – *see also 3.1*.

To quantify the homogeneity of the layer, their pore size distribution was analysed. These measurements are also based on the same images used for the porosity analysis. For better comparability the relative frequency was plotted against the pore size. As mentioned in *section 2.3.3*, the pore size distribution was approximated by the use of the pore area visible in the cross section images. As clearly shown in *Figure 27, Figure 28* and *Figure 29* most pores come with a cross section below 1 μm^2. At this point it must be mentioned that there are pores with a bigger cross section than 2 μm^2. However, considering their very low relative frequency compared to the submicron pores, and thereby for the better readability of the graphs these pores are not displayed, but were considered for all calculations. In terms of relative frequency, the submicron

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pores clearly dominate. In contrast to that the bigger pores account for a much higher amount of the total pore area – *see Table 12 & Table 13*.

In case of the “nano” paste samples, it is shown, that almost no pores bigger than 1 µm² exist, and further the do hardly contribute to the total pore area – *Table 14*.

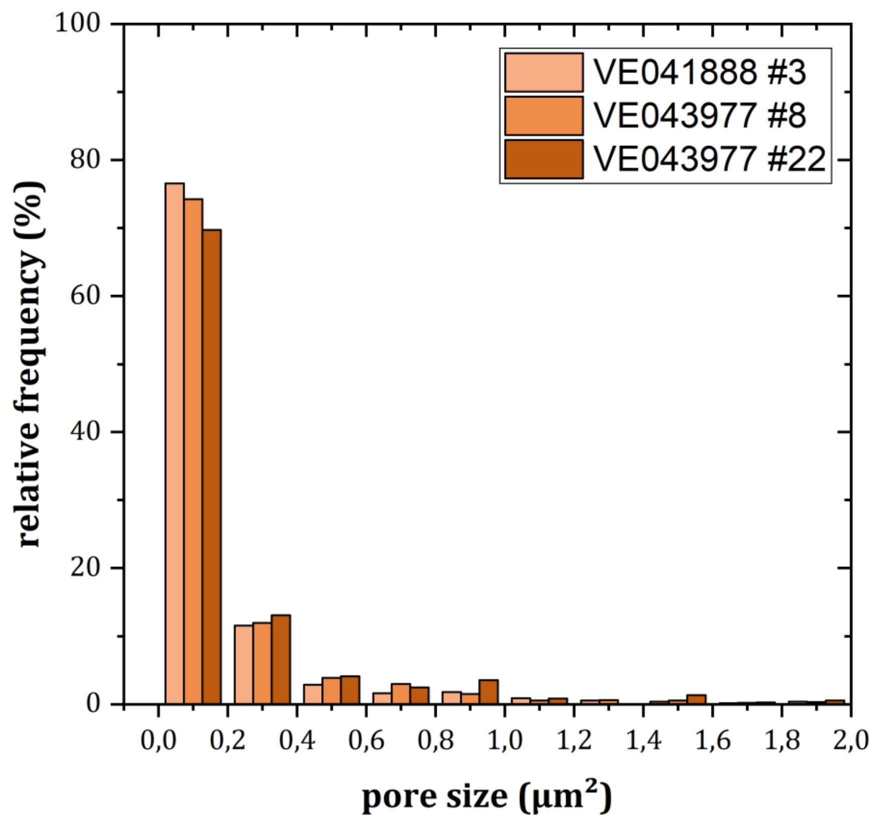

Figure 27 – pore size distribution of sintered "mixed" paste samples

Table 12 – share of pores on total pore area and relative frequency for sintered “mixed” paste samples

	pore size (µm²)	share of total pore area (%)	relative frequency (%)
VE041888 #3	<1	31.56	93.17
	>1	68.44	6.83
VE043977 #8	<1	36.34	93.65
	>1	63.66	6.35
VE043977 #22	<1	35.54	96.21
	>1	64.46	3.79

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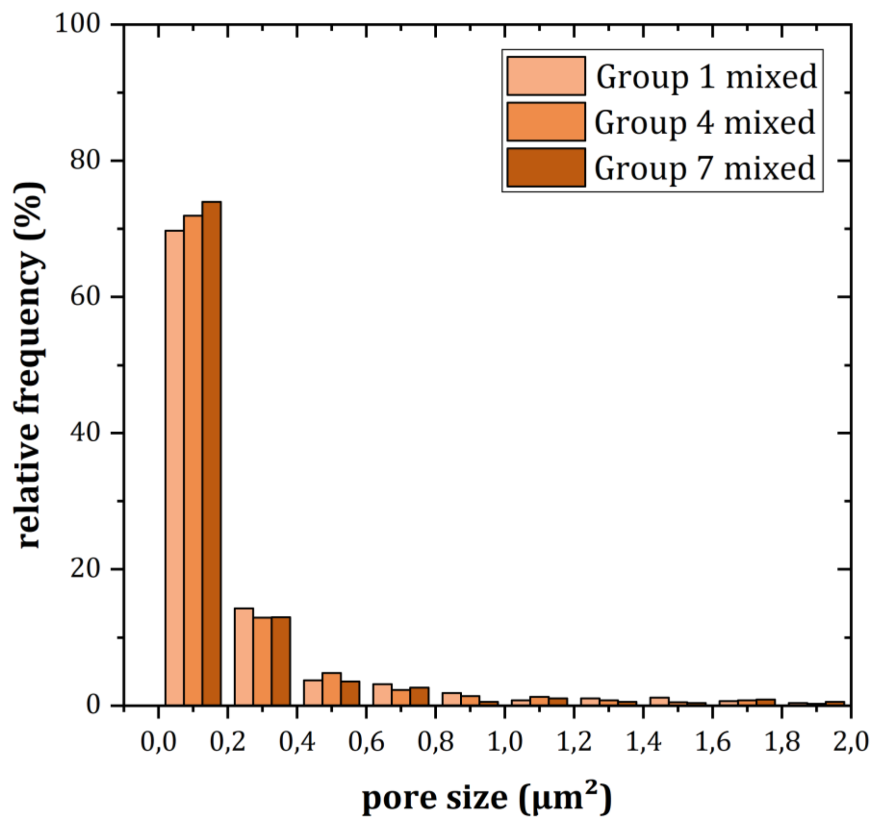

Figure 28 – pore size distribution of pressure sintered "mixed" paste samples

Table 13 – share of pores on total pore area and relative frequency for pressure sintered "mixed" paste samples

	pore size (μm^2)	share of total pore area (%)	relative frequency (%)
Group 1	<1	34.54	92.88
	>1	65.46	7.12
Group 4	<1	43.23	95.30
	>1	56.77	4.70
Group 7	<1	39.99	92.41
	>1	60.01	7.59

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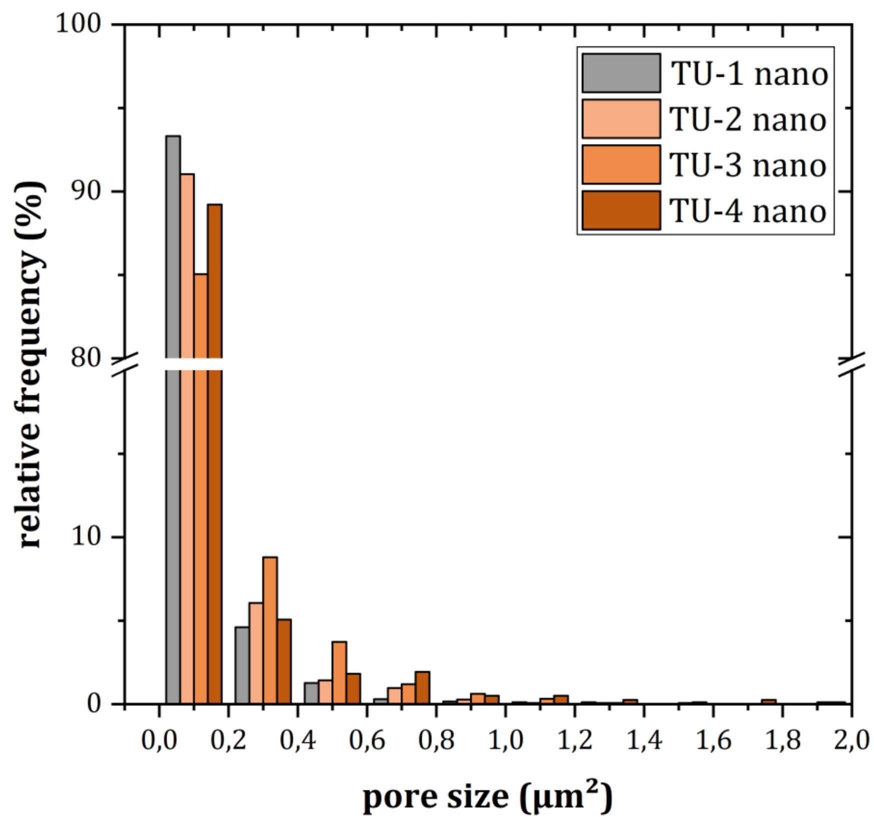

Figure 29 – pore size distribution of pressure sintered "nano" paste samples

Table 14 – share of pores on total pore area and relative frequency for pressure sintered "nano" paste samples

	pore size (μm^2)	share of total pore area (%)	relative frequency (%)
Group 1	<1	92.42	99.67
	>1	7.58	0.33
Group 2	<1	93.79	99.75
	>1	6.21	0.25
Group 3	<1	93.17	99.43
	>1	6.83	0.57
Group 4	<1	75.40	98.32
	>1	24.60	1.68

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3.3 Investigation of the influence of additional pressure sintering on printed copper layers

3.3.1 Influence of additional pressure sintering on the porosity

The contradictory requirements to the copper layer in terms of increasing electrical and thermal conductivity while reducing thermal induced mechanical stress on the interface has been described in *section 1.2* and *1.3*. In order to approach a denser copper layer while obtain a porous structure on the interface the additional pressure sintering step was introduced – *see 2.1*.

The effect of this pressure sintering step on the porosity was investigated by the comparison of the results from the porosity analysis – *see 3.2*. To exclude all other parameters but the pressure sintering step. only samples with the same production parameters – *see Table 2* – were considered. A graphical comparison is shown in *Figure 30.* As only for the "mixed" sinter paste samples both sintered and pressure sintered samples were available. the following analysis is limited to those samples.

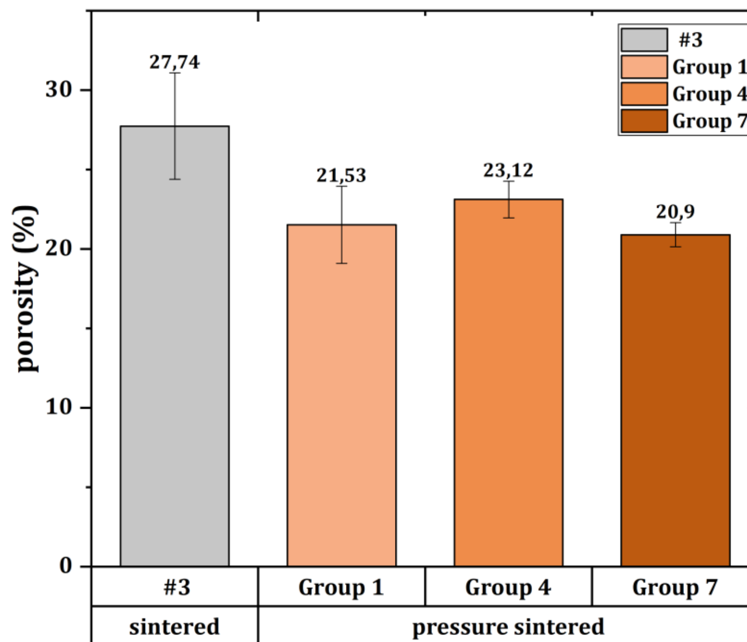

Figure 30 – influence of the pressure sintering step on the porosity

In *Figure 30* it can clearly be seen that the pressure sintering step has a certain densifying effect on the samples. Considering the results from the image analysis – *Table 11* – the densification lies between 4.6 and 6.8 %.

Table 15 – densification of pressure sintered "mixed" paste samples

	porosity (%)	densification (%)
VE041888 #3	27.74	
Group 1	21.53	6.21
Group 4	23.12	4.62
Group 7	20.9	6.84

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By taking a closer look on the pressure sintering parameters – *Table 2* – it is interesting to see. that a rising the force/pressure (compare *Group 1* with *Group 4*) seems to have no significant additional densifying effect considering the statistical deviation. The same behaviour can be seen by raising the temperature or changing the sinter atmosphere.

The influence of the densifying effect on the pore size distribution was further investigated. In *Figure 31* and *Table 16* the pore size distributions are compared.

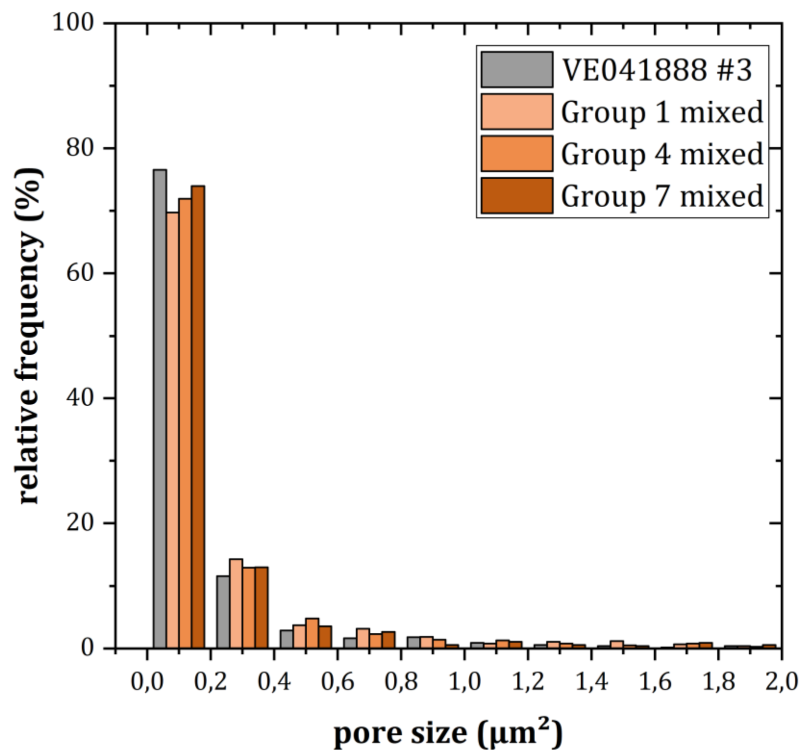

Figure 31 – comparison of pore size distribution of sintered and pressure sintered "mixed" paste samples

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Table 16 – share of pores on total pore area and relative frequency for sintered and pressure sintered "mixed" paste samples

	pore size(μm^2)	share of total pore area (%)	relative frequency (%)
VE041888 #3	<1	31.56	93.17
	>1	68.44	6.83
Group 1	<1	34.54	92.88
	>1	65.46	7.12
Group 4	<1	43.23	95.30
	>1	56.77	4.70
Group 7	<1	39.99	92.41
	>1	60.01	7.59

Based on the comparison one can see no significant influence of the pressure sintering on the pore size distribution. Thereby one could argue that the measured densification is a direct result of the mechanical force and not a result of a sintering process. as during sintering the ratio between small pores and big pores should change. However. as the densification seems to stay constant even with higher force – *see Figure 30 and Table 2* – this results are contrary and a final assessment of the influence of pressure sintering on the porosity cannot be given.

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3.3.2 Influence of pressure sintering on the layer thickness

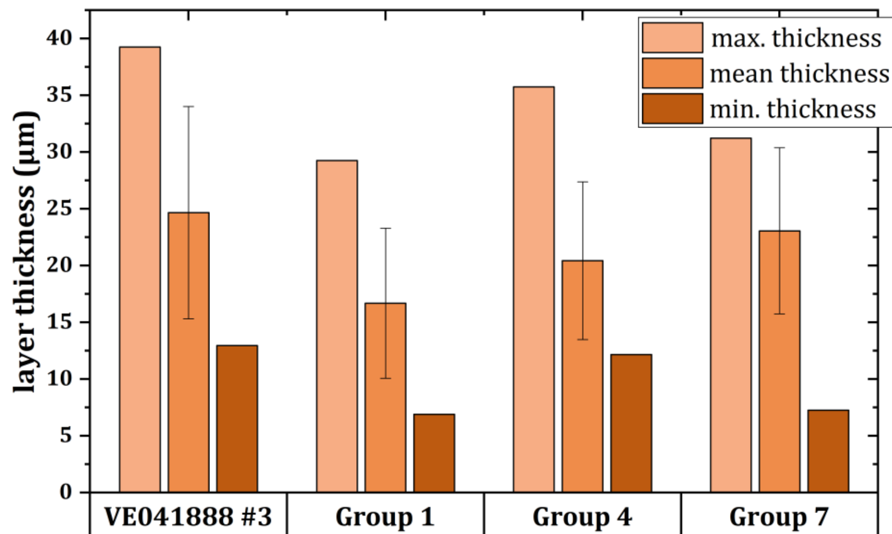

Figure 32 – influence of pressure sintering on the layer thickness

As shown in the previous *section 3.3.1* the pressure sintering step has a densifying effect on the copper layer. By comparing the mean layer thickness before and after pressure sintering in theory similar shrinkage like measured for the porosity should be observed. In *Table 17* the shrinkage of the mean layer thickness is calculated. With respect to the difficulties during wire bonding the change in the minimum values of the layer thickness was investigated due to the positioning of the bond wire – *see section 3.1.3*. The results are also shown in *Table 17*.

Table 17 – shrinkage of copper the copper layer during pressure sintering

	mean thickness (µm)	shrinkage (%)	min. thickness (µm)	shrinkage (%)
VE041888 #3	24.68		12.96	
Group 1	16.69	32.37	6.91	46.68
Group 4	20.44	17.18	12.17	6.10
Group 7	23.07	6.52	7.27	43.90

Based on the calculation of the shrinkage one can say. that for Group 1 and Group 7 the minimum layer thickness shows a higher shrinkage than the average layer thickness. This goes well together with the convex curvature of the wafer and the nature of the pressure application during the pressure sintering step. The results of Group 4 however show contrary results as in this case the average layer thickness shrinks stronger than the minimum values. Several reasons for these results could apply. The most likely explanation is since this analysis is based on image analysis of the cross cuts. This means one concludes from the discrete values of the images to the entire wafer. In theory Group 4 could show the same behaviour as Group 1 and Group 7 but simply the images were taken on different spots. so the minimum did not show the same behaviour. As for the sample prioritization – *see section 2.1*– more samples of Group 7 were available to be investigated and the measurements to be used for the image analysis. Thereby one can conclude that the findings of Group 7 not only seem to be likely because they can be explained by the production process. but also because the results are statistically more reliable.

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3.4 Chemical analysis

3.4.1 EDX analysis

The EDX analysis was used to determine the elemental composition of the diffusion barrier coating. In *Figure 33* an exemplary backscattered electron SEM picture *(a)* and representative EDX point spectra *(b - c).* The appearing gold peak is a result of the sample preparation for the SEM analysis. as the crosscut samples produced a lot of charging and drifting effects.

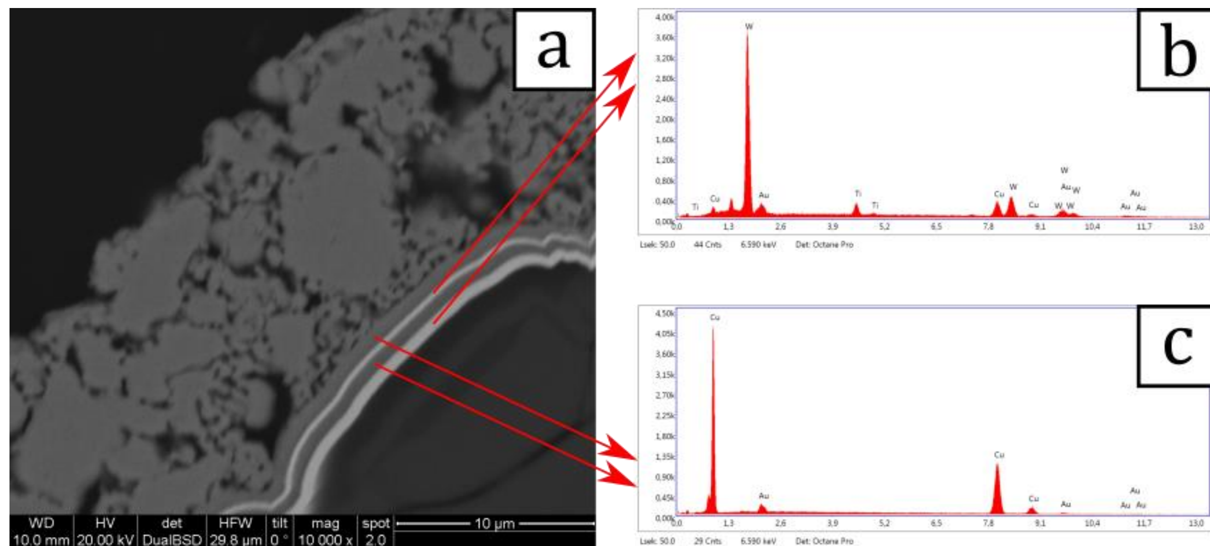

Figure 33 - BSD SEM image (a) of the diffusion barrier coating and respective EDX spectra (b) & (c)

The elemental analysis in combination with the structural information from the SEM images – *see section 3.1.2* – gave a good impression of the structure of the diffusion barrier coating.

One can clearly see that the barrier consists of four layers. Two of them are pure sputtered copper layers with the top one acting as the seed layer for the printed copper layer as well. The remaining two layers consist of tungsten and titanium which is a common coating to prevent diffusion of foreign elements – *see section 1.3.3*.

3.4.2 Carbon analysis

The results of the carbon content analysis can be found in *Table 18* and *Table 19*. The first measurements showed a carbon content of about 0.23 wt%. Taking into consideration. that the copper layer should be free of any carbon and further carbon comes with a significantly lower atomic mass compared to copper these results were very high.

Two different sources were suspected to be responsible for the contamination: adsorbed carbon containing gases from the atmosphere and organic residues from the sinter paste.

In order to investigate the strength of the bond between copper and carbon, and in an attempt to remove the carbon contamination, a second experiment was executed. For this purpose, the scratched copper particles were treated with wet hydrogen at 600 °C for 30 minutes. After this treatment the carbon contend was measured. The results of this analysis can be found in *Table 19*.

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Table 18 – results of the carbon content analysis

	sample weight (g)	carbon content (wt%)	mean (wt%)	std. deviation (wt%)
#3_1	0.0108	0.246		
#3_2	0.0332	0.221	0.232	0.013
#3_3	0.0242	0.229		
calibration standard: LECO 502-873				

Table 19 – results of carbon analysis after treatment with wettened hydrogen

	sample weight (g)	carbon content (wt%)	mean (wt%)	std. deviation (wt%)
#3_1 H_2	0.0094	0.101		
#3_2 H_2	0.0062	0.097	0.113	0.024
#3_3 H_2	0.0042	0.141		
calibration standard: LECO 502-916				

With a carbon content of about 0.11 wt% the second measurement showed a significantly lower result than the first measurement. By comparing the two measurements. one can conclude. that the treatment with wetted hydrogen reduced the carbon content by more than 50 %. This also means, that the resulting carbon content origins from sources that cannot be removed by the treatment mentioned above.

With carbides, high molecular weight organic residues from the copper paste or traces of the sinter imide coating being the most likely candidates. The sources of the remaining carbon are still subject for further investigation. The removal of carbon contamination however is an important issue to address, as it comes with a reduction of properties like e.g. electrical conductivity [46].

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3.4.3 Oxygen analysis

Oxidation is a very common phenomena when dealing with metals. Although the samples were produced under protective or reducing atmospheres – *see Table 2*. the results of the oxygen content analysis showed a considerable amount of 0.39 wt% oxygen in the sample – *see Table 20*.

Table 20 – results of the oxygen content analysis

	sample weight (g)	oxygen content (wt%)	mean (wt%)	std. deviation (wt%)
#3_1	0.0256	0.322	0.391	0.097
#3_2	0.0334	0.349		
#3_3	0.0586	0.501		
calibration standard: LECO 501-149				

As the samples were produced and pressure sintered at two different facilities of Infineon Technologies Austria AG before being sent to TU Wien for the analysis. and being stored without protective atmosphere in between each step. it is very likely that the surface and the open pores simply oxidised over time.

With that in mind and considering the highly porous nature of the sample the oxygen content of 0.39 wt% is of no concern.

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4 CONCLUSION

Based on the results found, one can state, that a characterization of porous copper layers on silicon wafers with classical powder metallurgical methods is possible. For the porosity analysis a combination of density measurements by Archimedes method and classical metallography with following scanning electron microscopy seems to produce the most reliable results. While He-pycnometry works excellent with sintered samples, it struggles with pressure sintered samples due to the attached DCB plate.

Regarding the sinter pastes, the metallography of the copper layers from both “mixed” and “nano” samples showed advantages in different areas. For the “mixed” paste samples one can clearly say. that the sintering as well as the pressure sintering shows the desired effect and the paste forms numerous sinter contacts to the wafer below. The surface and the microstructure however come with a more inconsistent appearance originating in the bimodular nature of the sinter paste.

Vice versa, the “nano” paste samples come with a very homogeneous surface and microstructure but show a lot of different difficulties forming contacts to the diffusion barrier coating. Based on the results found, one can say that one or possibly more than one problem during the production procedure causes the “nano” paste to form hardly any contacts or to delaminate from the diffusion barrier coating. To isolate the problem a possible further analysis should compare sintered with pressure sintered samples.

During the investigation of the impact of additional pressure sintering on the structure and porosity several important findings were made. Firstly. the results clearly show that a densification can be achieved by the applied procedure and the copper layer can thereby be densified for 4 – 7 % Nonetheless the results also show that the effect of the pressure sintering is not distributed equally across the entire copper layer. as the shrinkage analysis combined with the topographical analysis clearly indicate a stronger impact of the pressure sintering in the middle of the wafer. Based on these findings it is very likely that the densification is also subject to the same fluctuations. Further the mechanism of the densification could not be uncovered as contrary results were found.

With all these results combined it is not only very well apparent, that the specifications of the copper layer vary throughout the wafer, but also clearly indicate the enormous importance of topographical analysis for the investigation of several specifications like layer thickness and densifying effects.

The chemical analysis of the carbon content revealed a considerable amount of carbon in the samples. It is very likely that the source for the contamination are organic residues from the sinter paste which were not removed during the sinter process. As the fine powders sinter already at lower temperatures the carbon removal might be counteracted by the beginning sinter process. For reasons of reliability further investigation on the carbon contamination is necessary.

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LIST OF ABBREVIATIONS

BET	Brunauer–Emmett–Teller theory for surface area determination
BSD	backscattered electron detector
CTE	coefficient of thermal expansion
EDX	energy dispersive x-ray analysis
FFG	Austrian Research Promotion Agency
GaN	gallium nitride
IGBT	insulated-gate bipolar transistor
IUPAC	International Union of Pure and Applied Chemistry
IR spectroscopy	infrared spectroscopy
MOSFET	metal oxide semiconductor field-effect transistor
SEM	scanning electron microscopy
SiC	silicon carbide
SLID	solid liquid interdiffusion
WBG	wide bandgap

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