DISSERTATION

Design Space Evaluation for Standby Power Supplies in Smart Appliances

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Kurzfassung

Diese Arbeit präsentiert und untersucht verschiedene Konzepte für die Versorgung von kabellosen Sensor- und Kontrollknoten, direkt von der Netzspannung. Das Hauptaugenmerk liegt dabei auf Energie- und Kosteneffizienz, als auch auf guten Integrationsmöglichkeiten. Die beiden Konzepte, die in die engere Auswahl kommen und deshalb genauer untersucht werden, sind das kapazitive Netzteil und nicht isolierte Schaltreglertopologien.

Die wesentlichen Neuerungen in dieser Arbeit sind :

- Das kapazitive Netzteilkonzept wird genauestens beleuchtet und vor allem auf die Verwendbarkeit im gegenständlichen Anwendungsbereich untersucht. Ein speziell entwickeltes zweistufiges Konverterkonzept, als auch eine leicht integrierbare Version werden vorgestellt. Das Ergebnis dieser Untersuchungen dient als Grundlage für den automatisierten Entwurf kapazitiver Netzteile für Smart Appliances und legt damit den Grundstein für zukünftige Arbeiten in diese Richtung.
- Es wird ein neuer Ansatz eines nicht isolierten Schaltreglers untersucht, bei dem die Form der Netzeingangsspannung verwendet wird um die Spannung zu einem nachfolgenden Regler zu begrenzen. Dieses Konzept verspricht eine Kostenreduktion durch kleinere Bauweise, bei guter Effizienz. Das Ergebnis ist ein funktionsfähiger Hardwaredemonstrator, der das neue Konzept implementiert. Zusätzlich wurde für dieses Konzept eine spezielle Schaltreglertopologie entworfen, in der zwei Konverterstufen mit nur einer Spule auskommen, um die Integration zu erleichtern.

Abstract

This work presents and evaluates different concepts of ultra low power supplies for wireless sensor and control nodes. The main focus lies on power and cost efficiency as well as good integration capabilities. The two concepts that are investigated in greater detail are the capacitive power supply and the non-isolated SMPS converter.

The essential contributions of this work are :

- The capacitive supply is analyzed in great detail especially for the utilization in wireless sensor and control nodes. A specialized two stage concept is presented as well as a possible integrated topology. The result of this design space exploration is the basis for the automated design of capacitive ultra low power supplies for smart appliances and lays the foundation of future work in this direction.
- A new SMPS based approach is investigated that utilizes the slope of the input voltage sine wave to limit the converter input voltage. This concept promises to reduce costs through smaller components and easy integration while maintaining good efficiency. A functional hardware demonstrator was built to verify the functionality of this concept. Additionally a special power feedback SMPS topology is presented that uses only a single inductor for two supply stages to decrease integration costs.

Vorwort/Preface

Earlier, complex electronic circuits were only used when it was absolutely necessary for the primary function of the device mainly because they were much bigger and also more expensive. When integration density increased and the device costs decreased more and more devices were equipped with electronics thereby adding secondary functionality such as remote control capabilities, simple push button control or advanced displays. Nowadays nearly every modern device is equipped with advanced electronic circuitry. The trend goes into adding complex communication capabilities to the devices and hereby establishing a network including as many devices as possible. The purpose of these great number of interconnected intelligent devices is to support the user imperceptibly wherever possible. This is commonly referred to as "Internet of things".

Because of this development the requirements of the power supplies are changing too. Earlier a lot of appliances didn't need a dedicated power supply as they were operated directly from the mains. The number of dedicated power supplies was small and the power supplies itself were typically designed for a relative high output power. As the control and communication circuits that are nowadays added to all kinds of devices need a dedicated supply the number of power supplies increased dramatically.

Additionally, the actual power requirements for control and communication are typically very small. As the typical power supplies were designed for a high power output they are bigger then necessary and less efficient at low power output. Therefore new power supply concepts are necessary that are both energy and cost efficient. This work picks up on capacitive power supply concepts, investigates their usability for this purpose and presents some enhancements. Additionally a new SMPS based concept is discussed that utilizes the slope of the input voltage sine wave. Both concepts are non-isolated and powered directly from the mains supply. As the trend is to equip more and more appliances with low power electronics and also independent low power devices are gaining ground, this research area will become more important.

"The greatest pleasure in life is doing what other people say you cannot do."
[Walter Bagehot]

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1 General introduction

In the past decades state of the art of most electronic devices has shifted to smaller form factors with a simultaneous increase of performance. That led to a wide spread of electronic devices of all kind in everyday life. While earlier only few electronic devices were present in a household and these devices consumed a considerable amount of power, nowadays the number of devices is much higher and the average power consumption per device is much lower.

Nowadays a typical household appliance remains connected to the mains and either doesn't have a hard power switch or the switch is in "on" position most of the time. This is done to offer the user a high comfort level by enabling remote control functionality or memory retention for the clock or operation settings. The operation state where the equipment is not performing the task for which it is built but standing by and waiting for user input is called standby mode. When the device is completely powered down by disconnecting it from the mains, it usually takes more time to start its designated operation because it may have to be reconfigured first. Also the remote control obviously doesn't work in this state. Unfortunately the device has to consume some power to stay in standby mode.

During the 90s the standby power consumption has gained attention and was subject to several studies all over the world [Sid13]. A standby power consumption of about 10 W was not uncommon for a typical appliance. A large part of the power losses was caused by inefficient power supply stages at light loads. As the effected appliances grew in numbers, efforts were made to reduce the standby power consumption of that devices. As part of these efforts the Energy Star label [Ene13] was created to define rules to produce energy efficient products. Appliances should not only have a maximum power consumption depending on their function but also a maximum standby consumption and a maximum on-time without user interaction, depending on the device.

In 2008 another study [BSBKV08] researched the standby consumption of appliances available in stores in two eastern European cities. The results show that the average standby consumption is well under 5 W and strongly dependent on the device. A large number of additional new device types was investigated that did not draw any standby power in the past. This clearly illustrates the trend to integrate more electronics in home appliances to improve user comfort by creating smart appliances. Now a growing number of appliances is equipped with a microcontroller to control its primary function or to assist the user. Additionally, a hard power switch is becoming less important because the controller has to be supplied all the time to enable user interaction, communication or memory retention.

The trend to add complex communication capabilities to a variety of former simple devices is also clearly visible. The newly established network of these interconnected smart appliances is called "Internet of things". These smart appliances shown in figure 1.1, can communicate with each other, form a network and optionally communicate with the user over a smartphone or a notebook. There is a great variety of network structures and communication protocols available for this purpose. To go into details on this topic would go

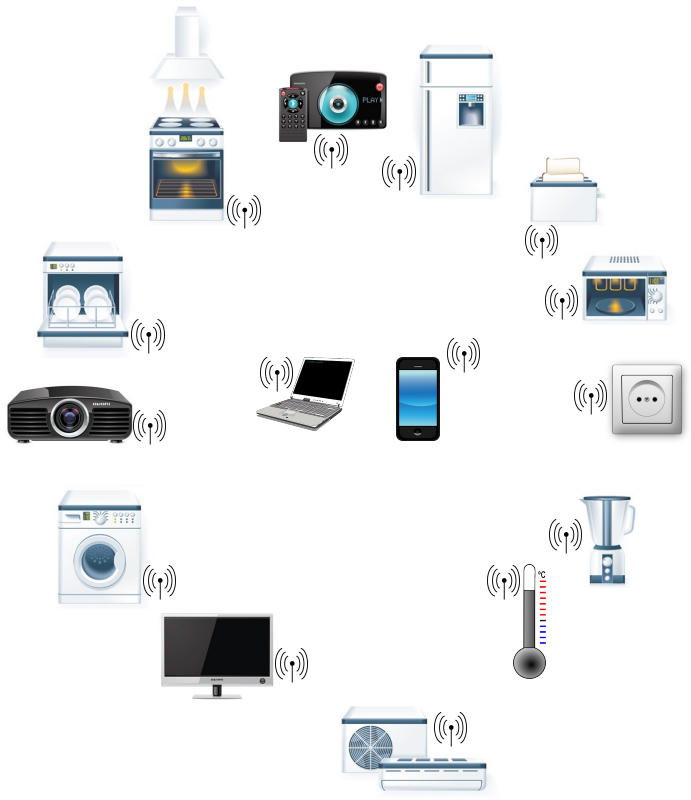

Figure 1.1: Smart appliances with advanced communication capabilities can communicate with each other or with the user through a smartphone or a notebook.

beyond the scope of this work, although ZigBee has to be mentioned as a typical set of communication protocols for personal area networks. ZigBee is based on the IEEE 802.15.4 standard [IEE] and is typically used with low power transceivers. Although the range of a single communication node is very limited depending on the used low power transceiver and the environment, data can be transmitted over greater distances through the utilization of a meshed network where the message is running over numerous adjacent nodes.

What all these network topologies have in common is that they require a specific amount of power. Although there are efforts to minimize power consumption, in the end each node will need some power all the time even when it's not active in order to receive messages and interact with the user. With a growing number on appliances that draw a small amount of power all the time as standby consumption, this topic becomes more and more important. In 1999 the International Energy Agency (IEA) released the One Watt Initiative [MB99] that led to several national and international regulations. Besides the energy star label [Ene13] the EU regulation 1275/2008 [Eur] has to be mentioned in particular out of a set of EU eco design regulations. When it was first implemented in 2008 the maximum energy consumption of an appliance in standby mode was limited to 1 W for appliances without displays and to 2 W for appliances that can display information to the user. In 2013 these limits were tightened to 0.5 W and 1 W for appliances with a display.

With state-of-the-art technology it is possible to get the standby power consumption of a typical appliance well within these limits. But the additional network capabilities necessary for smart appliances require additional power. In order to keep additional power losses small, the International Energy Agency released voluntary guiding principles for energy efficiency in networked products [IEA] in 2007. Although there are no hard limits mentioned this guideline addresses principles to reduce power consumption in networked devices including network management.

In order to still meet all requirements the power supply of a smart appliance has to be very efficient as it has to cover not only simple standby but additional communication capabilities. Depending on the actual appliance the main power supply usually is inapplicable to reach that goal because the supply is typically designed to power much bigger loads and is therefore very inefficient for light loads. An efficient second standby power supply that is optimized for light load is therefore often used to power the device during standby mode even if it's communicating with other devices. This work covers the design and selection of these ultra low power supplies.

Figure 1.2 shows a block diagram of a state-of-the-art dual supply. Because this represents a complete independent low power supply the costs are higher than utilizing only the main supply. A key is therefore not only to create an energy efficient supply for light loads but also to create a cost efficient supply solution.

Certainly it's not enough to focus only on the power supply when reducing the standby power consumption of a device. The circuit technology surrounding the microcontroller, the microcontroller itself and even its software are integral parts to reach a low standby power consumption. With the utilization of the right parts and the right techniques it should be possible to reach a standby power consumption of less than 100 mW for most devices. The lower the standby power consumption of the appliance, the more significant is the actual standby power supply circuit.

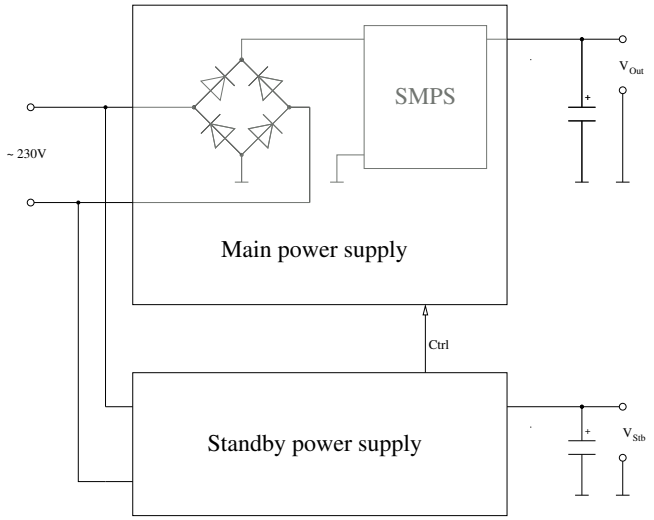

Figure 1.2: An additional high efficient dedicated standby power supply is used to power an appliance in standby mode to decrease standby power consumption.

With the trend to smart appliances, power supplies are needed in devices to power their electronics that didn't require a dedicated supply in the past to fulfill their main purpose. A good example for this are white goods. In this case a single low power supply may be enough as the main functional parts of the appliance are powered directly from the mains. In principal in most of these cases the device electronic has to measure some basic parameters, perform simple processing tasks and control some actors based on the results. Additionally communication with the outside world may be performed utilizing a simple remote control or more sophisticated using a wireless transceiver. In this scenario every properly equipped appliance can communicate with each other smart appliance or the user, thus forming a communication network. These smart communication nodes can even exist without a dedicated host appliance. These independent nodes can be used to measure temperature, light intensity, or the power output of a power socket. Additionally such nodes can be used as independent routers for the whole network.

This offers great opportunities in the field of home automation including lighting control applications which leads to a point where even a light switch is equipped with a wireless transceiver to communicate with the lamps as can be seen in figure 1.3. This network may even be connected to the internet in order to enable user access even when the user is not at home. That gives the user great flexibility and a high level of comfort but all the devices have to be powered in order to stay connected to the network. As the smart devices grow in numbers the total cost of a single device as well as its power consumption gain importance. Hence a cost and energy efficient power supply is almost mandatory.

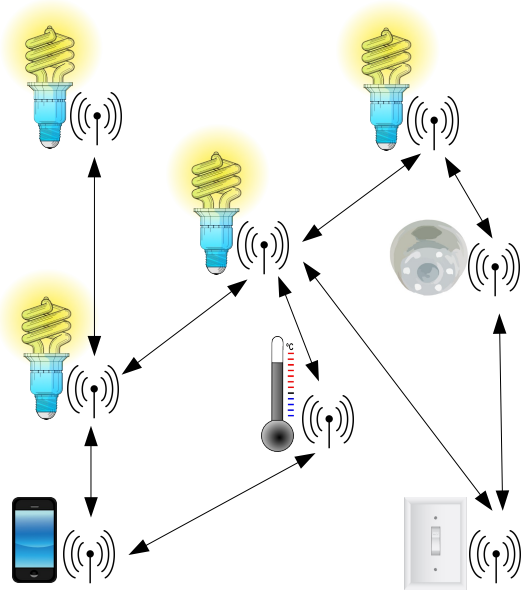

Figure 1.3: Example topology for a lighting system using a meshed network.

1.1 Motivation

As the number of household devices with standby capabilities rises, the standby power consumption becomes more and more an issue. Dedicated standby power supplies are used to ensure reasonable efficiency that cannot be provided by the mains supply at light load. Additionally, there is a growing number of sensor and actuator nodes that have the same power requirements as household appliances in standby mode and therefore need a similar power supply type. While mains driven power supplies are a wide research field, this work focuses mainly on standby power supplies for smart appliances utilizing a wireless transceiver and dedicated power supplies for wireless sensor and control nodes. As the user has no direct contact to the secondary supply side and optional data is transfered wirelessly the supply can be built non-isolated to decrease the costs. On the other hand this decision implies that this supply type can not be utilized when a tethered data connection to another appliance is required or the user may have direct contact to the secondary side of the standby power supply. While wireless sensor and control nodes can be found in various household appliances as control nodes for actual device operation, they can be also used independent of an appliance to perform various tasks as measuring temperature or movement. The acquired data is then transfered through a wireless network to a destination node that can trigger various actions (e.g. switch on a light). The power requirement of the node lies somewhere around 100 mW at a relatively low output voltage of about 3.3 V [KKWK10]. This power requirements are also typical for standby operation of smart appliances utilizing a wireless transceiver. The main motivation for this thesis therefore is, to find and evaluate concepts to realize a cost and energy efficient standby power supply design for the next generation of smart appliances.

1.2 Design problem and focus of this work

In the past the main focus of research has been at the main power supply ranging from a few watts up to a few hundred watts. Additional power factor correction (PFC) circuits have become necessary for these supply types as a result of their high power rating, in order to fulfill applicable standards. These main power supplies (e.g. typical PC power supplies) have become very sophisticated in terms of efficiency and power factor, while their main disadvantages are their high price, their size and their typically poor efficiency at very light loads.

Nowadays a lot of new device types are emerging that don't have high power demands. These devices can be individual wireless nodes as part of a bigger network, or they can be the result of the effort to add standby capabilities to an appliance that didn't need a dedicated power supply before. This leads to a new type of power supply in the ultra low power range that is not only energy efficient but also cost efficient. As these new devices are small and inexpensive (e.g. , a light switch node or a temperature sensor node) the power supply can easily become the most expensive part of the device. This leads to the conclusion that cost efficiency is one of the most important characteristics of these power supplies.

The main challenges of a standby power supply for smart appliances are :

- Cost efficiency
- Low weight
- Low component count
- Low component costs
- Easy to integrate
- Reasonable efficiency
- Small form factor

The main design problem is therefore to find a supply topology which brings the best tradeoff mainly between cost efficiency and energy efficiency. Transformer based isolated topologies have been left out as the necessary transformer would generate high costs. Simple single-resistor linear supplies also have been left out as the energy efficiency would be too poor. The main focus of this work therefore lies on two promising concepts of non-isolated supplies. One is capacitor based and the other is based on a non-isolated SMPS design. When the actual topology for a power supply is selected the actual dimensioning remains. When building a standby power supply for a smart appliance a lot of different parameters have to be considered that completely can change the cost and energy efficiency. Therefore another design problem is to find the right structure and dimensioning for the selected supply concept. This is another focus of this work as the chosen topologies are analyzed in detail to provide the future designer or an automated design tool with data to dimension a proper supply.

1.3 Structure of this thesis

After the general introduction an introduction into the field of standby power supplies for smart appliances is given. Therefore first the possible operation states of the appliances with their different power requirements are classified. Several concepts to minimize power consumption in the appliance itself are introduced to minimize the power requirements of the necessary supply. Then different power supply concepts are shown and their advantages and disadvantages are explained which finally leads to the non-isolated ultra low power mains power supplies that are further investigated within this thesis. A non-isolated capacitive supply and a non-isolated SMPS-based concept are the two most promising concepts.

The third section deals with the state of the art of these two concepts. First the two basic structures of the capacitive supply are explained. Then the dimensioning of the introduced topologies is explained in great detail. The required properties of the main components are outlined so the safety of the supply is ensured and it is compliant with the corresponding standards.

At last previous work is introduced that brings several enhancements to the basic supply topology. As a second part the basic SMPS topologies that are necessary to understand the rest of the work are explained. Different operation modes and control algorithms are also introduced for this matter.

The fourth section deals with the design space evaluation of the selected supply concepts. This means that the selected supply concepts are investigated on their usability in the desired field of standby power supplies for smart appliances and the possible and optimal dimensioning parameters are outlined according to the design goals defined in section 1.2. Therefore, first the capacitive based supply is analyzed in great detail leading to a extensive loss and efficiency analysis. Then possible enhancements for the utilization in the desired application field are introduced based on the results of the analysis. In the second part of this section the SMPS-based concept is analyzed. Therefore, first the sources of possible losses in the suitable operation modes are investigated. Then a detailed loss-analysis based on the switching frequency the inductance and the actual losses is performed to outline the optimum operation area for the desired application field.

The fifth section deals with a new SMPS-based supply concept that builds up on the analysis of the fourth section. Therefore first the underlying key parameters are explained and then the basic operation principle of the new concept is introduced. Then different operation modes are compared and their advantages and disadvantages shown. The utilized sub-circuits are explained in greater detail as they are crucial to ensure efficient supply operation.

The sixth section deals with the integration possibilities of the introduced supply concepts. An integrated version of the capacitive supply is introduced and first simulation results are presented. For the new SMPS-based supply introduced in section 5, a special and more complex integrated solution is presented as it promises to reduce integration costs dramatically. The operation principle is explained and first simulation results are presented.

The seventh section evaluates the prototype of the capacitive supply solution during a field test and presents an experimental functional demonstrator for the new SMPS-based concept. The capacitive approach was used as power supply for wireless sensor nodes during an extensive field test over several weeks. Its results are presented within this section. Additionally, a functional demonstrator of the new SMPS-based concept was built and evaluated. Although the good efficiency and the full extent of the integrated version could only be demonstrated in early simulations, this demonstrator could verify the principal of operation. The measuring results are provided within this chapter.

The eight section concludes on the utilization of the introduced power supply concepts in standby power supplies for smart appliances.

1.4 Contributions

The central contributions of this work are the detailed design space exploration of the capacitive supply concept as well as the investigation of a new SMPS-based converter concept.

Although the basic capacitive power supply and some variants as described in section 3.1 are well known, the literature is lacking a detailed design space exploration for the field of wireless sensor and control nodes. This is not unusual as a few hundred milliwatts or even more losses and a relative high reactive input power did not state a problem in the past. When it comes to smart appliances, especially a small form factor as well as low cost and low reactive input power combined with good efficiency is of most importance. This is comprehensible as these supplies will come in greater numbers and will strain the mains accordingly.

This work contributes the loss analysis and design space evaluation for capacitive supply solutions for smart appliances in section 4.1. This exploration then leads to the preferred two stage concept of section 4.1.6 and its analysis. The analysis without the two stage concept has been rudimentarily published in [GHW+12] for slightly different parameters. The selection sheets in section 3.1.4 used to dimension the two basic capacitive supply topologies for standby power supplies in the investigated power and voltage range have not been published yet although similar graphics have been published in [GHW+12] by the author. The integrated two stage capacitive supply variant from section 6.1 has been published in [Luk11] and [GHW+12].

Lots of literature exists on SMPS-based supply concepts as it is an ongoing research topic. Most literature deals with the maximization of efficiency for medium or heavy loads. A few work on supplies up to a few watts. Section 3.2 gives an overview over existing SMPS-based topologies that can be utilized for smart appliances as well as related work. The problems when using a typical SMPS-based supply design in smart appliances are the size of the supply, the high number of high voltage parts that make integration harder and the bad efficiency at ultra light loads.

This work gives a design space evaluation for the SMPS-based approach to standby power supplies for smart appliances including the analysis in section 4.3 as a minor contribution. The new phase controlled converter concept of section 5 is a major contribution. Its main principle has been published in [Luk11] and [GHW+12] although this section provides much more details. The power feedback SMPS from section 6.2.1 as part of the integrated variant from section 5 is also a major contribution and has not yet been published. The functional HW demonstrator and its evaluation in section 7.2 has also not yet been published.

2 Introduction into power supplies for smart appliances

When it comes to power supplies for smart appliances a lot of issues have to be considered. Before a proper supply can be designed, the power requirements that change with the operation state of the device have to be analyzed very carefully. Therefore a proper classification scheme has to be found and the possible operation states of the appliance have to be specified. Through careful design of the appliance the power requirements especially at standby or other low power states can be minimized. Then a proper power source has to be selected depending on various parameters. As the main focus of this work is on non-isolated mains driven ultra low power supplies these concepts will be investigated in greater detail. As explained previously the power supply then consists typically of two independent stages. The primary stage supplies the appliance during normal operation and is high efficient at the operating power of the appliance. The standby stage supplies the appliance during low power states and is therefore operating most of the time.

2.1 Classification

[DMG+11] introduced a device classification for appliances based on their function, available parameters and energy management options. Looking at this topic from the side of actual power consumption, each device class may have different power requirements depending on its actual operation state. While some devices get along with a simple plug or an on/off switch, other devices may require a more sophisticated approach. A simple classification scheme is summarized in figure 2.1.

Rarely any device comes without a power switch and can be switched off only by disconnecting the power source. However, disconnecting the power source is a save way to prevent any power consumption. Some devices are equipped with a hard power switch which means that a switch can physically disconnect the power source. This hard power switch is another safe way to prevent power consumption. In most cases where the user is required to operate the appliance manually, a hard power switch brings no substantial downsides. On the contrary it can add additional safety (e.g. drilling machine, stove). Additionally a hard power switch can often be found in older appliances (e.g. TV, PC) while it disappeared from lots of newer consumer products. When it is still included it is often located on the back of the device and not easily accessible to the user.

Nowadays a button is often used to switch a device on or off. Unlike a hard switch that disconnects the device physically from the mains, a button is part of a control electronic that needs to be supplied in order to work. Therefore a soft switched device always draws a certain amount of power. This can be a problem when a battery powered device is in “off” mode for a longer time because the battery is still stressed by the control electronics. Hence it is a good idea to remove the battery if possible when a device is not used for a longer time. How much power the control circuit actually needs is depending on its design but can be very low for higher quality circuits. If a device is in “off” mode there is no substantial advantage to a device which is disconnected from the supply. In standby mode an appliance

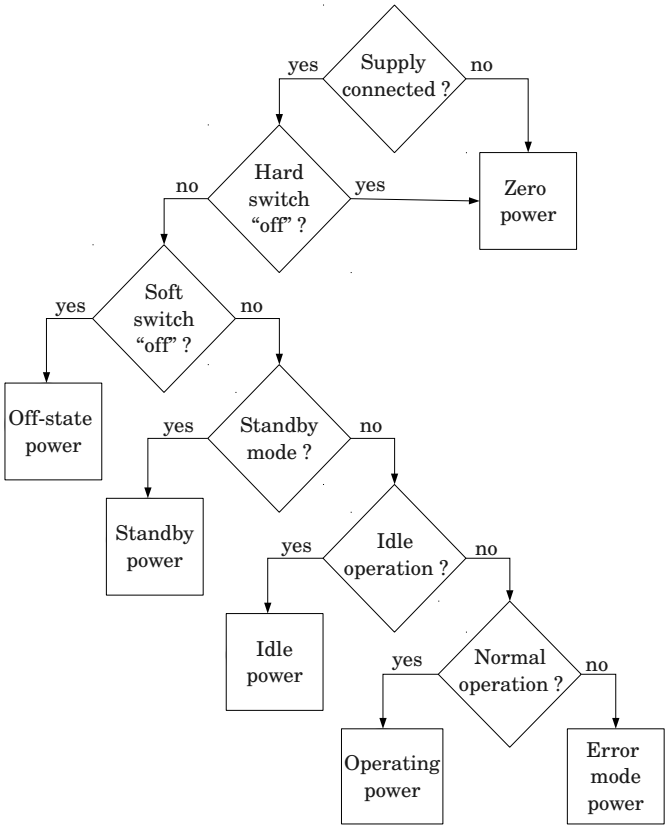

Figure 2.1: Classification of the power requirements of a device depending on its operation state.

usually waits for an event to wake up. This can be a user command over a remote control, a timeout or a measured parameter (e.g. temperature level). Therefore much more electronics have to be powered (e.g. remote receiver, transceiver, temperature sensor, microcontroller) which will consume more power. However, the standby consumption is usually way under the power consumption for normal operation. Additionally the appliance may start up faster from standby than from cold power up.

During idle mode or during normal operation the device can consume up to its maximum rated power. Usually the power consumption is lower in idle mode but the power consumption in idle mode is typically in the same magnitude than the power consumption in normal operating mode. However, in some cases the power consumption in normal operating mode can be much higher (e.g. motor under heavy load).

When an appliance is malfunctioning the power intake often changes. This has to be considered when designing the power supply for this device. Depending on the device the supply has to withstand no load conditions (e.g. bulb or other lighting device broken) or heavy load conditions (e.g. a motor that is stuck). Usually a safety mechanism is implemented to switch off the appliance in case of a failure. The user must then resolve the error and restart the device.

2.2 Power supply concepts

When selecting the proper power supply concept for a device a lot of different parameters have to be considered. Power and voltage requirements, reliability, costs, mobility and maintenance requirements are the most important. Depending on the application there may be more than one suitable solution to power a device. The basic supply options the designer usually faces are a battery based supply, a supply from the high voltage mains, a power supply utilizing local energy harvesting or a low voltage supply bus. Figure 2.2 shows a mindmap of the most common supply types. The supply concepts that are covered by this work are highlighted.

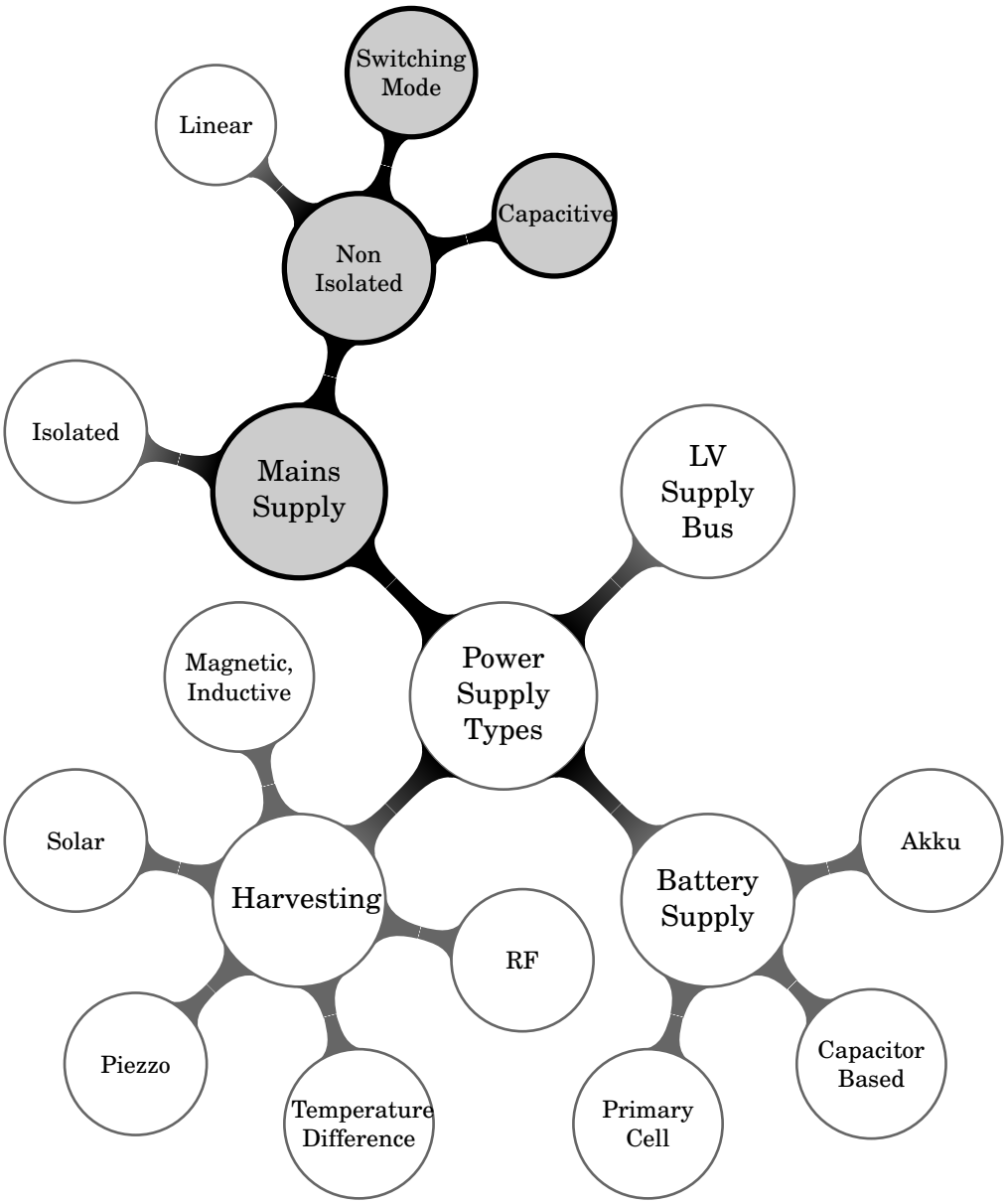

Figure 2.2: Power supply types.

Battery powered supply : A battery power supply is usually used when high mobility and availability is required or no general mains is available. A battery power supply can be realized using a primary cell or a rechargeable battery. A primary cell is typically used for devices with lower power requirements (e.g. clock) whereas rechargeable batteries are usually utilized for devices with higher power requirements (e.g. mobile phone) to minimize maintenance costs. When rechargeable batteries are used, the charging circuit can be integrated into the device to load the battery inside the device thereby reducing maintenance effort. The battery itself can be integrated into the device which gives a size advantage but may limit the lifetime of the device. Additionally, a battery-based power supply can be used to support a regular mains supply in order to bridge power outages. Some devices utilize a battery supply to completely take over the mains supply (e.g. notebook) in case the mains fails. Other devices use the battery backup only to retain memory or maintain some basic functions (e.g. alarm clock) whereas the main device function is discontinued. The main advantages of battery supplies are mobility and reduced converter costs whereas the main disadvantages are the limited energy and the increased weight due to the battery.

Energy harvesting : Energy harvesting is typically used for devices used on remote locations which are hard to reach for maintenance. Harvesting supplies are typically combined with battery supplies to bridge cycles with no energy harvesting output (e.g. solar supply). Hence this supply type is an extreme low maintenance supply. The disadvantages are the increased size and costs of the device. The application area of energy harvesting supplies range from a measuring station offside in the woods to a energy harvesting wireless light switch in office applications.

Low voltage supply bus : A local low voltage supply bus is typically used when a lot of devices with similar voltage requirements have to be supplied. Then a central power supply is more power and cost efficient and the power is distributed through a local bus. Typical examples are automotive or home automation applications.

Mains power supply : A mains based power supply is typically used for high power applications (e.g. heating) or when mobility is not an issue and the mains is easily accessible. Some appliances don't need a dedicated supply for the high power parts as they may be connected directly to the mains. A typical mains voltage is 230 V in Europe or 115 V in America. This supply type will be covered in greater detail in section 2.4.

2.3 Power saving concepts

Although the efficiency of the used power supply itself plays an important role for the total power efficiency of the device, there are additional parameters that have to be considered. When looking at a typical appliance (e.g. washing machine) there are phases with high power consumption and phases with low power consumption. When the machine is working,

the motor is spinning and the heating element may be on. This is a common high power scenario. On the other hand when the machine is finished or waiting to be refilled only the control electronic is drawing power as all the major power consumers are off. Although the control electronic consumes comparatively low energy when compared with the motors or the heating element, it has to be supplied all the time. This is particularly true when the machine enables time scheduled washing or similar services. The influence of the control logic on the total consumption becomes more substantial for appliances with lower power consumption when active (e.g. TV set, monitor, Blu-ray player). The worst case is, when the power consumption of the device in active mode is similar to its consumption in standby mode as the energy efficiency is very low for these devices.

A first approach to minimize standby power consumption is to switch off all unnecessary parts. The control circuits usually can be divided in a part that is only used when the device is active and a general part that always has to stay on. The part that actually controls the operation of the device (e.g. revolution counter, fill level measurement,...) can be switched off when the device is not active. The power gating and the clock gating technique [LCN11] is commonly used in integrated circuit design and has to be utilized at the PCB level too in order to create appliances with low standby power consumption.

Additional to turning off the unnecessary parts power consumption of the remaining parts has to be minimized. This is done first of all trough careful design of the control circuits and proper selection of the used components. Besides the usage of ultra low power active components the selection of the used microcontroller, if one is necessary, deserves special attention. A good choice strongly depends on the application but various sleep states, low power consumption when running and software selectable variable clock sources usually are a good start. Issuing a sleep state whenever the controller has nothing to do can save a lot of power. Also the clock speed has to be considered carefully. The power consumption as well as the performance of the controller depend greatly on the clock speed. When the microcontroller only has to perform simple tasks a clock that is always very low can be utilized. However, when the controller has to do more complex computations in active mode the clock has to be switched in order to save power. In this usage scenarios the high frequency main clock may be used to do the computations and when the controller enters sleep mode a low frequency clock may service a timer so that the main oscillator can be switched off in order to save power. Fully grown DVFS (Dynamic Voltage and Frequency Scaling) processors are usually too overpowered for this application. Additional external components such as pull-up or pull-down resistors or measuring networks have to be considered carefully as they may be responsible for a major power leak in a poor design.

The user interface is another part to consider. This can range from a simple led to display an operation state over a graphical display to a wireless transceiver. Power saving efforts in this area can easily affect the comfort level. Easy ways are to flash a led instead of constantly having it on, or to dim the display or allow less current for leds. This can be done dynamically depending on the last user interaction. Also the receiver can be power cycled in order to save power but that may increase the response time of the system. The usage

of special wakeup receivers [HMH11] may also be an advantage. The used software also affects the power consumption if a microcontroller is used. In particular when a transceiver is used and the device is part of a larger network the used protocol has a great influence on the power consumption [CTSBD13, KVMJ06].

2.4 Mains power supply

A mains power supply is providing energy for the appliance directly from the mains grid. For simple appliances no dedicated supply is needed as the load within the appliance is connected directly to the mains voltage. When a dedicated supply is needed either an isolated or a non-isolated supply can be used. An isolated supply has to be used when the user can get in contact with the secondary part of the supply. This may be the case through metal parts or controls of the device or trough signal outputs. A non-isolated supply can be used whenever a device has no signal outputs and no user touchable metal parts. Also a galvanically isolated supply makes it a lot easier to interconnect different devices through wires.

2.4.1 Isolated mains power supplies

There are plenty of options to transfer energy from the mains to a load in a galvanically isolated way (e.g. magnetically, optically, mechanically,...) but mainly transformer based designs are of importance in typical a power supply. Early designs used a simple mains transformer as power supply but this supply type has become obsolete mainly due to the size of the transformer. Newer designs use a switching mode supply topology, depending on the actual power requirements. While forward- or push-pull converters are used in the medium and high power range, flyback converters are used in the lower power range of up to 200 W.

Simple mains transformer : One approach is to use a simple low frequency (e.g. 50 Hz) mains transformer. When operated in the medium or high power range (> 10 W), these mains transformers have an efficiency of typically < 90 % for E-I type transformers and of 90 - 95 % for toroidal types [TG94]. Although this sounds promising, these transformer types have considerable size and relatively high no load losses, hence reducing efficiency dramatically when operated in the low power range. They are typically not used in new designs as main power supply. When used as standby power supply, not only their size as well as the no load losses are considerably lower because of their lower power rating. The suitability of small (up to 1 W) low power mains transformers in standby power supplies has been researched with special aspect on the no load losses [Nie04a]. While off the shelf low power transformers reach no load losses of 0.5 to 1.5 W, special optimized transformers reach 0.15 to 1.1 W. Additional the whole power supply has been considered, consisting of not only the mains transformer but also a rectifier.

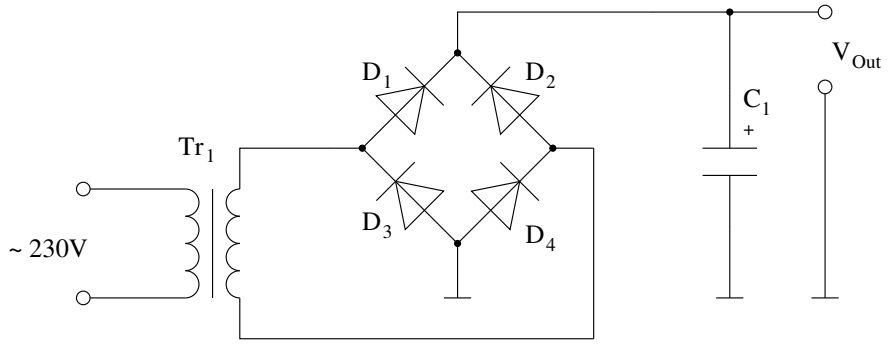

Figure 2.3: Simple unregulated transformer based mains supply. If the output has to be precise a second converter stage has to be added.

Figure 2.3 shows an unregulated transformer based mains supply. If the supply is regulated a second stage which may be a linear regulator or an additional buck converter has to be added which generates additional losses [Nie04b].

Results show that the efficiency is very low (5 - 14 %) at light loads of about 10 mA and reaches 59 % at a load current of 200 mA in the best case. Because of its size this power supply type is nearly impossible to integrate.

Flyback converter : The flyback converter is the most commonly used converter type for mains isolated low power supply applications. The converter typically reaches an efficiency of well over 90 % [HDY$^+$10]. It can operate in buck or boost mode which makes this converter topology also suitable for generating high voltages.

Figure 2.4 shows a simplified schematic of a flyback converter. The used transformer is not a conventional transformer but can be seen as coupled inductivities as the transformer utilizes an air gap. The energy is stored in the air gap during the conduction period of T_1 and is transfered to the secondary side while T_1 is off.

For higher output power levels the air gap has to be bigger to store more energy which also increases the leakage inductance which leads to more losses. This converter type is therefore only suitable for up to about 200 W [RLR97]. For higher output power levels the push-pull or full bridge converter is more applicable.

Because the flyback converter is typically used in isolated power supplies the control circuit also has to be isolated. The supply typically needs regulation feedback from the secondary side which also has to be provided in an isolated way, usually utilizing an optocoupler. Also an auxiliary winding at the transformer may be used to provide the necessary feedback or even to power the control logic [MYGW11].

Hence the power supply is more complex, harder to integrate but most efficient. The flyback converter is well known but to further boost its efficiency is still an active research area [HDY$^+$10, MYGW11, LS08].

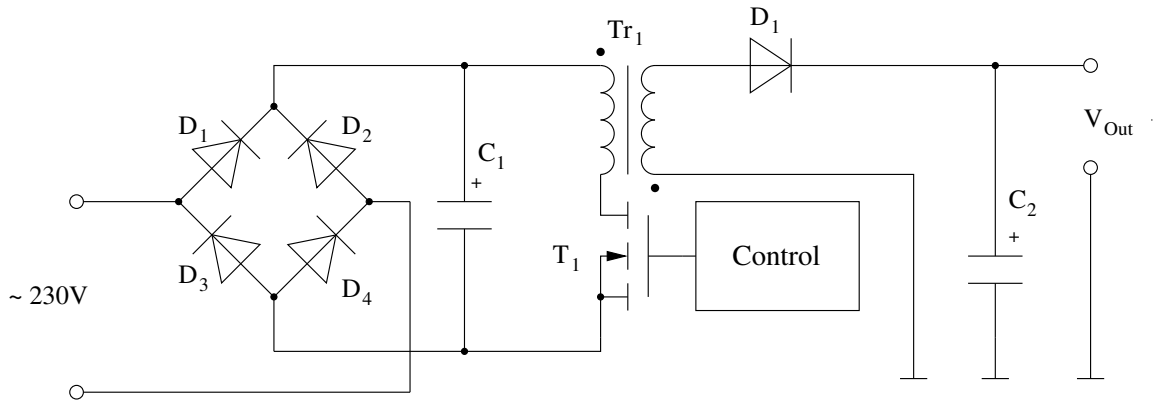

Figure 2.4: Principal schematic of a flyback converter. The transformer Tr_1 utilizes an air gap to store energy during the conduction period of T_1 and transfers it to the secondary side at the off-time of T_1.

2.4.2 Non-isolated mains power supplies

Whenever galvanic isolation is not necessary, a non-isolated power supply can be used. Typically a non-isolated supply can be built much smaller because a transformer is not needed. In principal the non-isolated power supplies can be divided into linear supplies and switching-mode supplies.

Linear non-isolated supplies : Figure 2.5 shows the principal structure of linear shunt supplies. X_1 acts as a current limiter and can be a simple resistor or a capacitor. X_2 is used to control the output voltage and acts as a voltage regulator. In a very simple supply X_2 can be left out. This leaves the supply unregulated which is only suitable for constant loads and a constant input voltage. If the supply has to be regulated because the load or the input may change, X_2 is typically a shunt regulator or a Zener diode. Hence the complete output power has to be dissipated in X_2 when the load stops to draw power. X_1 can be a simple resistor which is cheap but also very inefficient or a capacitor which builds the basis for a capacitive power supply. Hence the resistive version of X_1 can only be used for a very low power output.

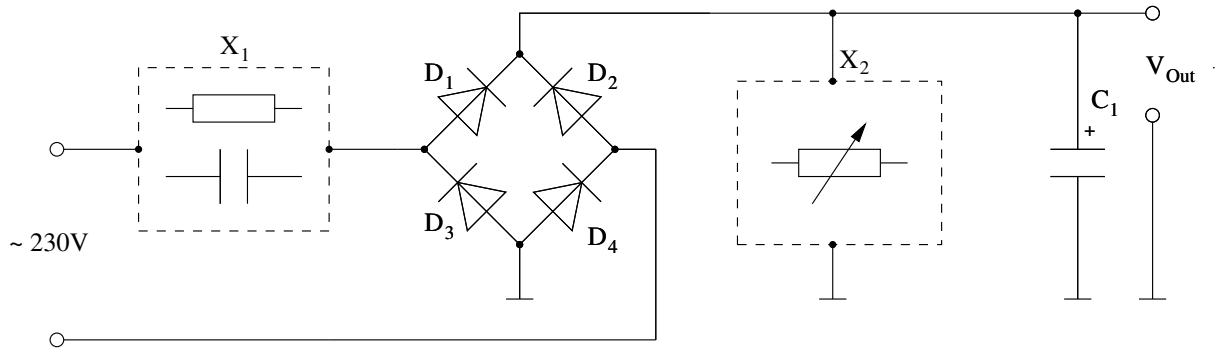

Figure 2.5: Principal structure of a non-isolated linear power supply. X_1 acts as a current limiting device which is either a resistor or a capacitor. X_2 acts as a voltage limiter which has to dissipate power in case the load draws not the full current.

The capacitive supply is more efficient but draws a significant amount of reactive power and has a relatively big capacitor. In either way X_1 has to sustain nearly the full mains voltage. The diodes D_1-D_4 are the rectifiers necessary to get DC. If necessary the full bridge rectifier can be replaced by a single rectifier diode to save money. The effects of the rectification on this supply type will be discussed in a later chapter.

Non-isolated switching mode power supplies : Besides the linear supplies the switching mode supplies are the second big supply group for non-isolated supplies. Typically a buck converter is used as the output voltage is lower than the input voltage in most cases. Figure 2.6 shows a basic structure of a simple buck converter. After rectification power is stored in the storage capacitor C_1. The switches S_1 and S_2 are needed to control the current flow through the inductor L_1. The timing of both switches has to be very precise otherwise the power dissipation in the switches will increase and the converter may be destroyed. The detailed operation principle of this supply type is described in a later chapter in this work.

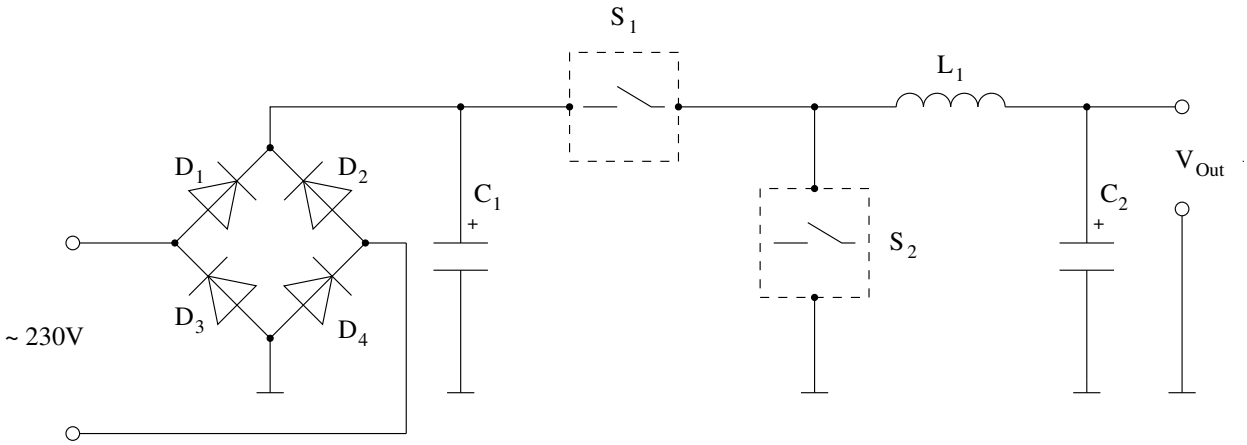

Figure 2.6: Basic structure of the non-isolated buck converter. D_1-D_4 form the rectification bridge, C_1 is the input storage capacitor, S_1 controls the current flow through the inductor L_1, S_2 has to take over the current when S_1 switches off and C_2 is the output storage capacitor.

3 State of the art and related work

This section gives an overview of the supply topologies that are currently in use as non-isolated standby power supplies in smart appliances. First the two most common capacitive supply topologies are generally discussed. The design process as well as the critical components are then described in greater detail. Various existing enhancements are presented that are partially used in state-of-the-art capacitive supplies. Then simple non-isolated SMPS converter topologies are discussed. The basic operation principle is explained and various topologies are introduced. Different operation modes and regulation strategies are outlined as they are important for further analysis.

3.1 Capacitive power supply topologies

The capacitive power supply is only suitable for AC voltage as the used current limiting capacitor in this supply type will block DC. The input current is limited by a capacitor and rectified afterwards. A Zener diode limits the output voltage which is buffered by an output capacitor.

This simple solution brings several advantages as reliability, small component costs, an easy design process and good efficiency for matched and constant loads. Some disadvantages of this supply concept are the big current limiting capacitor which makes it hard to design an integrated supply solution, a high reactive input current in relation to to the output, and low efficiency for varying or unmatched loads [Con04], [ST 04].

The capacitive power supply is usually galvanically not isolated which brings several limitations to the usage areas. On the other hand this supply concept brings the possibility to use a common system ground if needed, or a separated ground in a more efficient design variant. A typical application field for a common line capacitive power supply is energy metering [Max11], [Man10]. The supply type with a common ground uses a single rectifier and is introduced in section 3.1.2, while the more efficient bridge rectifier design variant is introduced in section 3.1.1.

The state-of-the-art capacitive supply includes a current limiting capacitor, a Zener diode, a rectifier circuit and a buffer capacitor for the output voltage as well as some resistors. Although the basic idea behind the supply is simple, there are a lot of potential design errors that can lead to serious safety issues, reduced reliability or accelerated aging.

Part selection deserves special attention since it has a fundamental relevance for safety and the reliability of the power supply. The utilization of a special capacitor of safety class X2 is mandatory for the current limiting capacitor to ensure power supply safety, as an X2-type capacitor has clearly defined requirements on voltage surges and inflammability [CEN05]. On the other hand, these X2-type capacitors may lose capacitance over time through voltage induced flash-over events which will limit the expected life span. The used X2-type current limiting capacitor will be discussed further in section 3.1.3. An X2-type capacitor refers to the X2 safety class and not to the part designator X_2 in figure 2.5.

Also other component types have to be considered carefully because they may have to withstand a high inrush current or high voltage peaks. Another safety consideration is the charge which is stored in the current limiting capacitance. Since the capacitor may be charged up to the full rectified input voltage when the device is disconnected, the charge might be accessible to the user over the plug. Precautionary measures have to been taken to ensure user safety [CEN06]. The startup of the supply which is initiated with the initial connection to the mains voltage as well as current and voltage surges during normal operation may additionally stress several components. They have to be selected to handle such events properly and without taking damage.

The basic operation principle induces a constant input current, which in combination with an usually constant Zener voltage will lead to a constant input power. Whenever no load is present, the power is dissipated within the supply, more precisely within the Zener diode. Hence the best efficiency can be obtained when the average absolute value of the input current equals the output current. In that case the supply is matched to the load which is connected to the output. Whenever the load draws less average power than the power limit of the supply, the efficiency drops. This may lead to difficulties at efficiency calculations because the typical load is not constant. Also the startup has to be considered carefully not only for safety, but also for functional reasons. During startup, when the buffer capacitor has not reached its nominal voltage, the power supply cannot supply the nominal power. This may lead to problems when the load draws power during startup.

The overall efficiency for this supply topology is not only highly dependent on the load, but also on the output and input current. Basically because of the parasitic losses in the supply, the efficiency is higher for lower currents. Therefore it is more efficient to build a supply with a higher output voltage for the same output power. This has also the advantage that the buffer capacitor can be smaller as energy can be stored better in capacitors at a higher voltage level.

This chapter addresses the state of the art for capacitive power supplies and provides all necessary analyses necessary to design one of the basic topologies. Several known enhancements to the basic single rectifier topology and the full bridge rectifier topology are discussed.

Although the basic function of the capacitive supply is well known, the capacitive supply is often poorly designed and dimensioned. Therefore this chapter not only gives an overview of the state of the art, but also gives a detailed analysis of the supply focusing on design parameters allowing the designer to select a suitable component with the help of the given figures. A detailed efficiency and usability analysis with respect to the application field of ultra low power supplies for smart appliances is not given in this part as this is discussed in section 4.1.

The basic operation principle is described and the key parameters as well as advantages and disadvantages are discussed. Alternative but also commonly used topologies are presented and explained. Detailed information on some key components is included as it is necessary to consider and select the proper component family.

The most important applicable standards are introduced because the compliance to these standards is relevant for safe and reliable device operation. Detailed design instructions are given to help a designer to understand and dimension a conventional capacitive power supply. Additionally several known enhancements are presented to increase efficiency. This section outlines the foundation for the detailed analysis of this power supply type with special attention to the desired application field.

3.1.1 Basic operation principle of the bridge rectifier topology

Figure 3.1 shows the circuit of the bridge rectifier topology of the well known capacitive power supply. The current limiting capacitor C_1 acts as a reactance to the mains and is used to define the input current. Hence, the input current is dependent not only on the mains voltage but also on its frequency. The output voltage of the supply is determined by the Zener diode D_2. The Zener voltage in combination with the input current, which equals the maximum continuous output current, outline the maximum output power of the power supply. The input current I_{in}, the apparent input power S_{in} and the output power P_{out} calculate to :

$$I_{in} = V_{mains} \cdot C_1 \cdot 2 \cdot \pi \cdot f_{mains} \tag{1}$$

$$I_{in} = I_{out} \cdot \frac{\pi}{2 \cdot \sqrt{2}} \approx I_{out} \cdot 1.11 \rightarrow I_{out} \approx I_{in} \cdot 0.9 \tag{2}$$

$$S_{in} = V_{mains}^2 \cdot C_1 \cdot 2 \cdot \pi \cdot f_{mains} \tag{3}$$

$$P_{out} \approx V_{mains} \cdot V_{out} \cdot C_1 \cdot 2 \cdot \pi \cdot f_{mains} \cdot 0.9 = I_{in} \cdot 0.9 \cdot V_{out} \approx I_{out} \cdot V_{out} \tag{4}$$

V_{mains} is the effective mains voltage and f_{mains} the mains frequency.

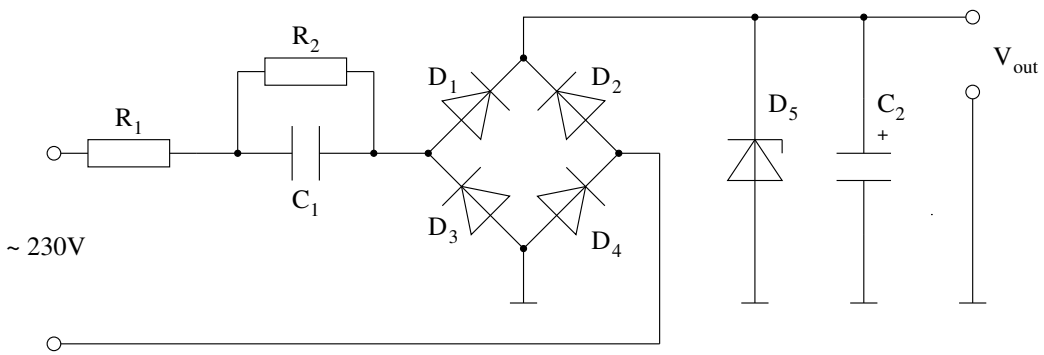

Figure 3.1: Conventional capacitive power supply utilizing a current limiting capacitor (C_1) and a bridge rectifier (D_1-D_4) for rectification. The output voltage is limited by D_5 and buffered with C_2. R_1 limits the inrush current and R_2 discharges the capacitor after the supply is unplugged.

The fact that the input current I_{in} is almost equal to the output current I_{out} leads to two important disadvantages of the capacitive power supply. Because the mains input voltage is usually much higher than the output voltage, the apparent input power is very high. Although most of the input power is reactive, this may lead to excessive line stress when lots of supplies are operated in parallel. Another disadvantage is the constant input power which will produce high losses in the Zener diode whenever no load is connected. The conventional capacitive power supply draws always the same power independent of the load. Hence this supply type reaches best efficiency for constant and matched loads only, which is not the typical case in combination with an RF transceiver used in smart appliances. The diodes D_1 - D_4 work as a rectifier bridge and the capacitor C_2 is used as a ripple filter and buffer capacitor. R_1 and R_2 are not necessary for principal operation, but are needed for safety and reliability of the supply. R_1 is necessary to limit the potential inrush current during the initial plug-in of the supply. Furthermore, R_1 is often used as a fuse resistor in order to prevent the supply from overheating in case the current limiting capacitor C_1 shorts. The purpose of R_2 is to discharge the current limiting capacitor C_1 after the supply has been plugged off.

This operation principle has another severe disadvantage. Phase detection of the mains voltage is not possible after the current limiting capacitor C_1. This is often necessary when zero voltage switching is required by the device and therefore a zero crossing detector has to be implemented. Through the phase shift this is not possible after the capacitor C_1. Compensating the phase error by recalculating the phase using the capacitor value and the output voltage is not very accurate due to component tolerances and therefore hardly done.

When the mains voltage is bad shaped or more rectangular than sinusoidal as some electronic inverters generate them, this could lead to various problems ranging from decreased efficiency to serious safety issues. This operation scenarios have to be considered carefully when designing a capacitive supply.

3.1.2 Basic operation principle of the single rectifier topology

Besides the classic approach shown in figure 3.1, there are numerous similar topologies. Another important variant is the single rectifier capacitive supply shown in figure 3.2. This topology has the main advantage that there is a common ground for the input and output which is required by some applications. Another advantage is that there are fewer components and the system gets cheaper. The main disadvantage is that only half of the input sine wave is used and therefore to reach the same output power the capacitance of C_1 has to be doubled to reach the same output current as in the full bridge rectifier topology. This leads to a higher input current which increases the loss in R_1. Also the loss in R_2 is increased because R_2 has to become smaller in order to discharge the bigger C_1 in the same time as in the variant with the bridge rectifier. Also the Zener diode D_5 is now before the rectifier D_1 which is necessary to establish alternating current trough the capacitor C_1. Hence the output voltage is the Zener voltage of D_5 diminished by the forward voltage of D_1.

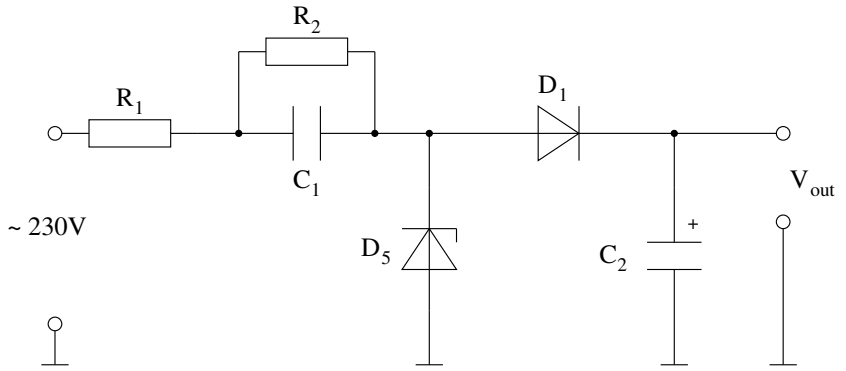

Figure 3.2: Single rectifier (D_1) capacitive supply topology. C_1 is the current limiting capacitor, D_5 limits the output voltage and is part of the current return path of C_1. C_2 is used to buffer the output voltage. R_1 limits the inrush current and R_2 discharges C_1 after the supply is unplugged.

3.1.3 The Current Limiting Capacitor

The current limiting capacitor (C_1) of a capacitive power supply has to fulfill specific requirements if it is to be used in an actual application outside the laboratory. The European norm EN60384-14 [CEN05] categorizes capacitors which are applied to a mains voltage < 1 kV in several X and Y classes with different requirements. Figure 3.3 shows the specified capacitor classes in their designated operation area. The class X capacitor is used between the power wires of the mains where the failure of the capacitor cannot lead to an electrical shock of the user. The class Y capacitor has higher requirements and is used between the power wires and the earth potential which is connected to a potential metal case that is accessible trough the user. If a class Y capacitor fails the user is in risk of taking an electrical shock. X and Y class capacitors are usually used for EMI repression or in capacitive power supplies.

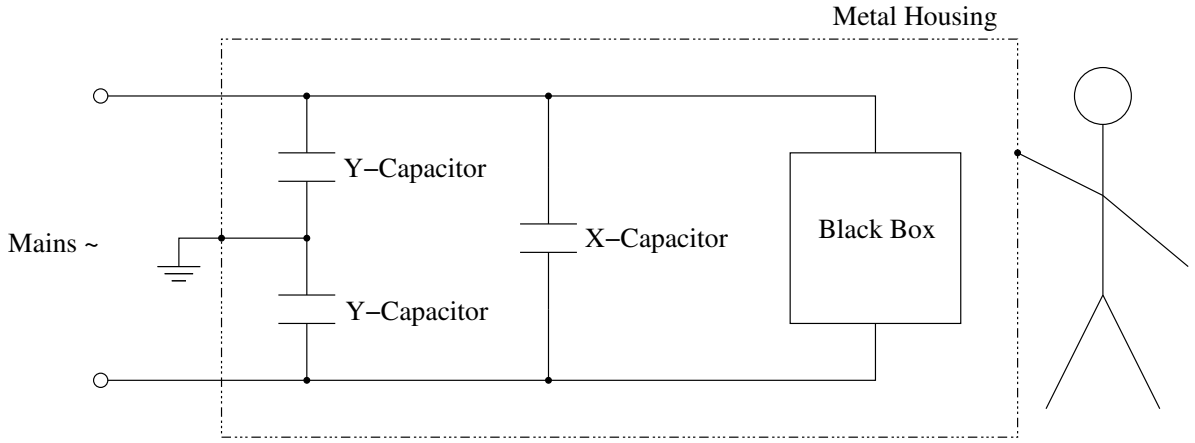

Figure 3.3: Typical operation of class X and Y capacitors. An X class capacitor is switched between the lines of the mains, an Y class capacitor is between one line and the ground connection. A faulty Y class capacitor can lead to an electrical shock of the user.

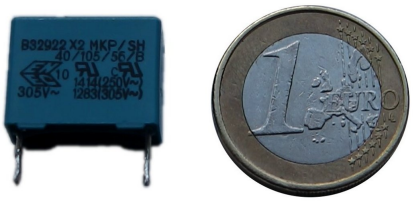

Figure 3.4: Typical 330 nF MKP (polypropylene dielectric) type X2 capacitor used for EMI repression between the lines of the mains or as current limiting capacitor in a capacitive power supply.

If a capacitor is to be rated class X or Y it has to pass several tests involving but not limited to active and passive flammability tests and impulse peak voltage tests [CEN05]. In a capacitive power supply the current limiting capacitor has to be at least an X type capacitor. In order to meet the specified requirements X and Y capacitors are relatively big and expensive. Figure 3.4 shows a typical X2-type capacitor used in a capacitive power supply. Common types for X or Y rated capacitors are plastic film capacitors or metalized paper capacitors. These capacitor types are self healing which means they remain functional after a voltage induced flash-over. However, because they heal by vaporizing the metalization at the flash-over point, they reduce their effective surface which means they loose capacitance. This has to be considered when this capacitor type is used in a power supply especial in regions with more transients on the mains supply. Other than that this capacitor type has little significant aging.

The capacitor manufacturer WIMA has studied the effects of cumulated flash overs for plastic film and metalized paper capacitors. They stated that a flash over of a polyester or polypropylene capacitor causes the previously bound carbon from the dielectric to condense as conductive graphite sediment in the insulation area of the capacitor. This will reduce the insulation resistance which can increase the capacitor current and therefore the thermal stress on the capacitor up to a point where the capacitor may ignite. The metalized paper capacitor on the other hand didn't suffer from this problem [WIM13].

3.1.4 Design of a conventional capacitive power supply

This chapter gives an overview of the design process and completes the available design guidelines [Con04, ST 04] with a detailed analysis and corresponding selection sheets. The first step in dimensioning the capacitive power supply is to determine the supply topology in order to meet the load requirements. In most cases the designer has to choose between the bridge rectifier variant and the single rectifier variant. While the bridge rectifier variant is more efficient, the single rectifier variant brings the common ground which means one wire of the mains can be directly connected to the load. The bigger and more expensive capacitor used in the single rectifier variant usually outweighs the cost reduction in the rectifier. Also the higher reactive input power of the single rectifier variant has to be considered. After the topology decision has been made, the output voltage has to be defined and the average output power has to be estimated. Although small power peaks can be compensated by the

buffer capacitor C_2, the supply has to be designed to handle the maximum load current if it exceeds the buffer capabilities of C_2.

The current limiting capacitor C_1defines the average output current : In the next step the current limiting capacitor C_1 has to be dimensioned to meet the required output current. As stated in section 3.1.3, it is important to use an X class capacitor for this application field. For the bridge rectifier variant C_1 calculates to :

$$C_{1(min)} = \frac{I_{out} \cdot 1.1}{(V_{AC_{RMS}(min)} - V_{DC} - V_{loss(max)}) \cdot 2 \cdot \pi \cdot f_{mains(min)}} \tag{5}$$

This is the minimum capacitance value for C_1 where the supply still provides its designated power. For the alternative single rectifier topology the value of $C_{1(min)}$ has to be doubled as only one half wave is used. $V_{AC_{RMS}(min)}$ is the minimum effective mains RMS voltage. As the effective mains RMS voltage is not the same around the world, the minimum effective mains RMS voltage has to be considered in order to ensure operation in all intended areas. The same applies to the minimum mains frequency $f_{mains(min)}$. V_{DC} is the DC output voltage which is set by the Zener diode and I_{out} is the required DC output current. V_{loss} represents the voltage losses in the resistors R_1 and R_2 as well as in the rectifier diodes D_1 - D_4. When designing an actual power supply, the capacitor values are only available in discrete steps. Hence the next higher capacitance value has to be chosen. Figure 3.5 offers a selection sheet for the current limiting capacitor C_1dependent on the output current for the bridge rectifier version (left) and the single rectifier version (right). As the figure shows, the dependency of the capacitance from the output voltage is within narrow limits.

Equation 5 shows also a dependency on V_{loss} which represents the voltage drop due to the losses in the resistor R_1 and the rectifiers D_1 - D_4. In typical designs V_{loss} is in the order of a few volts and therefore usually negligible for the capacitor selection process.

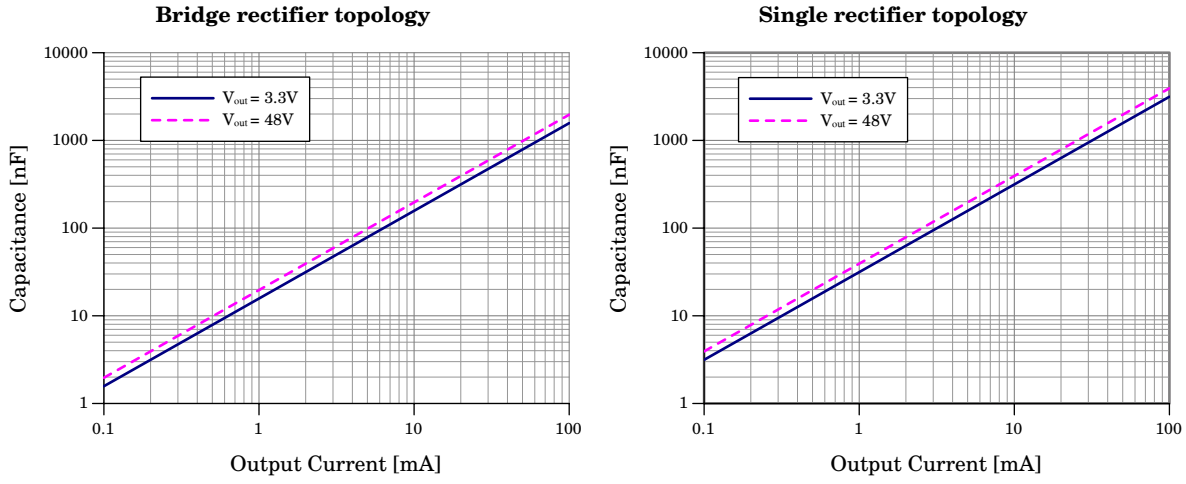

Figure 3.5: Selection sheet for the current limiting capacitor C_1 as a function of the required output current for the bridge rectifier version (left) and the single rectifier version (right).

When designing an actual supply, the tolerance of the selected capacitor has to be considered in a way that the supply can still deliver the designated current when the capacitor exploits the minimum tolerance limit. Also the aging due to high voltage transients has to be considered. The used capacitor must still have the calculated minimum capacitance $C_{1(min)}$ at the end of its designated lifetime.

The bridge rectifier D_1 - D_4, or D_1 for the single rectifier variant : Besides for input voltage surge protection the rectifier diodes don't have to handle the full mains voltage but only the output voltage. However, the rectifier diodes have another important requirement for this circuit. Because the inrush current which is limited trough R_1 is flowing through the rectifier, it has to be robust enough to sustain an inrush event. A typical I_{FSM} (maximum non-repetitive forward surge current) value for a 1N4007 standard rectifier is about 30 A. A small signal diode like the 1N4148 which may be enough when considering only the voltage rating, has an I_{FSM} value of only about 4 A. This value has to be taken into consideration when dimensioning R_1, and constitutes a compromise between efficiency and component cost. By increasing the inrush current limiting resistor R_1 the maximum inrush current is decreased and therefore a diode with a smaller I_{FSM} rating can be selected. On the other hand a larger value for R_1 decreases efficiency. The same considerations apply for the rectifier D_1 in the single rectifier variant in figure 3.2. The duration of an inrush event is discussed when dimensioning R_1 and has to be considered using the rectifier datasheet as well.

The Zener diode D_5 : The Zener diode has to be dimensioned according to the output voltage and the designated output power. The Zener voltage of D_5 will determine the output voltage. Note that the output voltage of the single rectifier version in figure 3.2 suffers an additional diode forward voltage drop because of D_1.

The input current of the capacitive supply is constant and independent of the load. Hence the current has to flow trough the Zener diode D_5 when no load is connected to the supply. Therefore the Zener diode has to be rated to handle at least the output power or the load has to ensure to draw a minimum power.

The buffer capacitor C_2 : The buffer capacitor C_2 has two main functions. The first is the smoothening of the mains frequency input ripples. Depending on the average load current it has to be dimensioned in a way that the resulting ripple is within acceptable limits. The second function is to compensate power consumption peaks of the load. When the load is not linear but a digital circuit, power peaks can occur during switching. Also it is possible to compensate planned short cycles of transmitter activity when C_2 is dimensioned accordingly. During each used input voltage half wave the capacitor C_2 is recharged up to a certain point where the Zener diode caps the voltage. When the Zener diode caps the voltage, the current from that moment on to the end of the half wave flows trough the Zener diode, which dissipates power in the Zener diode. Therefore a too small dimensioned output

capacitor C_2 would not only increase the ripple voltage but also decrease efficiency which may lead to insufficient output current capabilities of the supply. On the other hand, a too large output capacitor C_2 would lead to a longer startup time and increase component cost. The problem is to find the minimum capacitor to meet the efficiency and ripple criteria. To do that the recharging process has to be analyzed in greater detail.

Previous work formulates the time domain equations for a slightly modified capacitive single rectifier supply. [RJ11] This paragraph analyses the practical impacts of the capacitor C_2 from the single rectifier supply in figure 3.2.

Figure 3.6 shows simulation results of a single rectifier supply which V_{mains} = 230 V, f_{mains} = 50 Hz, C_1= 1 μF, $V_{Z(D5)}$ = 15 V, C_2=330 μF, R_{load}= 430 Ω. $V_{Z(D5)}$ is the Zener voltage of the Zener diode D_5 and R_{load} is a resistive load at the output of the supply. The supply was dimensioned for 30 mA output current. The waveforms show the currents in the supply during the recharge of the capacitor C_2 after the supply reached steady state. When a reload period begins at about 1.217s, the load current commutates from the capacitor to the input which leaves the capacitor current at 0 mA. The load current is nearly constant at 30mA. Now the charging process begins and lasts until the current trough D_1 , which is shared between the capacitor C_2 and the load, goes lower than the load current I_{load}which is at about 1.225s. Because I_{D1} is lower than the load current and decreasing, the capacitor C_2 has to take over the load current successively and hold it until the next charging period.

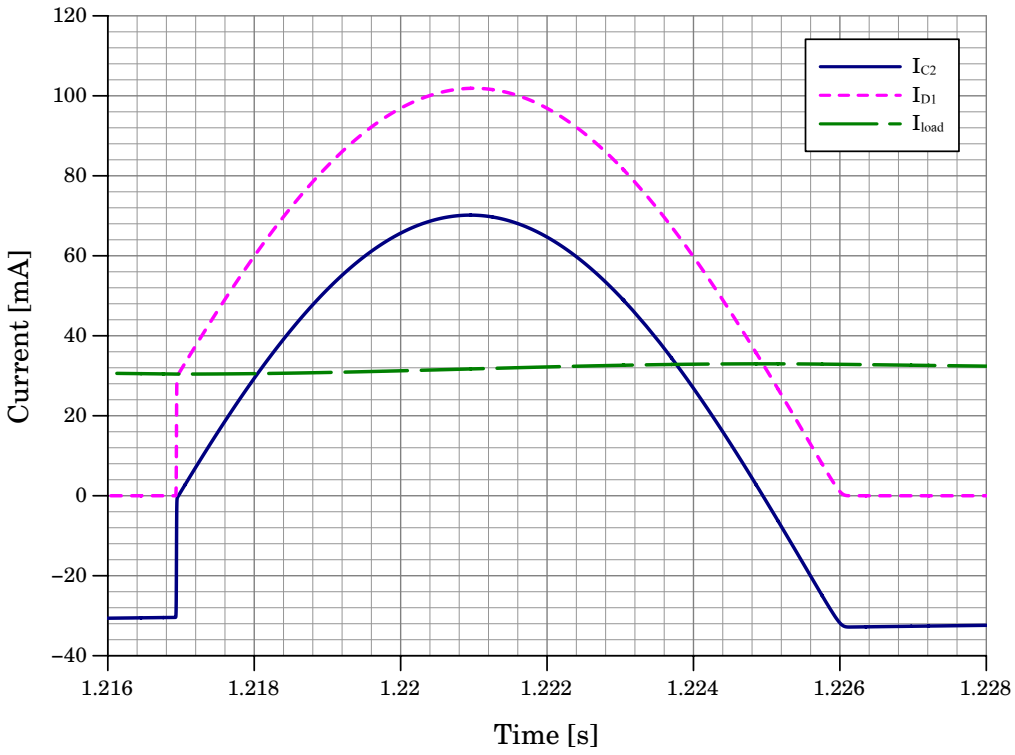

Figure 3.6: Simulation of a capacitive supply with a single rectifier. I_{C2} is the current trough the output capacitor C_2, I_{D1} is the current trough the rectifier diode D_1 and I_{load} is the load current trough a resistor R_{Load} that is connected to the output of the supply.

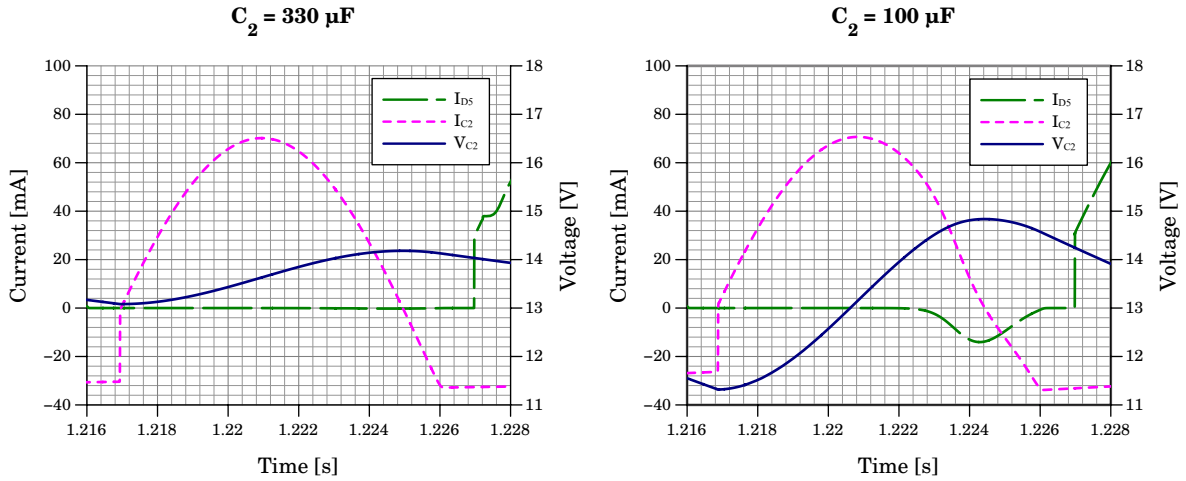

Figure 3.7: Simulation of the supply with a single rectifier in figure 3.2 for two different output capacitors (C_2). The right picture shows a higher voltage ripple and decreased efficiency due to the voltage limitation of the Zener diode D_5 caused by a too small output capacitor.

Figure 3.7 shows the difference between an output capacitor value of 330 μF (left) which is sufficient and an output capacitor value of 100 μF (right) which is slightly to small dimensioned. The used circuit is that of figure 3.2. As expected, the voltage ripple for the 100 μF capacitor (11.4 V - 14.8 V) is higher than the ripple for the 330μF capacitor (13 V - 14.2 V), but there is another important difference. The Zener diode starts to cap the output voltage at about 14.4 V by diverting the charging current to ground. Therefore the current trough the Zener diode D_5 is not zero during the charging phase but peaks to about -15 mA. This means that power is dissipated in the Zener diode and therefore the efficiency decreases. The current through the Zener diode during the non-charging phase can be neglected because it is induced during the forward time of the Zener diode as the Zener diode is also used as rectifier in forward direction.

This leads to a minimum output capacitance C_2, where no power is dissipated in the Zener diode during the charging phase of the capacitor when the load is matched and not changing. Figure 3.8 offers a selection sheet for the output capacitor C_2 based on simulation results with a single rectifier (left) and with the full bridge rectifier (right). While the lower capacitance level meets the efficiency criteria where the capacitance C_2 is big enough that no heat is dissipated in the Zener diode, a significant ripple of about 1.5V for the single rectifier version and of about 3V for the bridge rectifier version is remaining. The ripple for the bridge rectifier version is higher because a much smaller capacitor is required to meet the efficiency criteria. When comparing the upper lines in figure 3.8 which represent the required capacitance for a given output current to reach an output voltage ripple of about 150mV, the required capacitance value of C_2 to meet this ripple criteria, is about 5 times higher for the single rectifier version (left) than for the bridge rectifier version (right). The startup time of the capacitive power supply is directly proportional to the value of the output capacitance C_2 and inversely proportional to the rated output current.

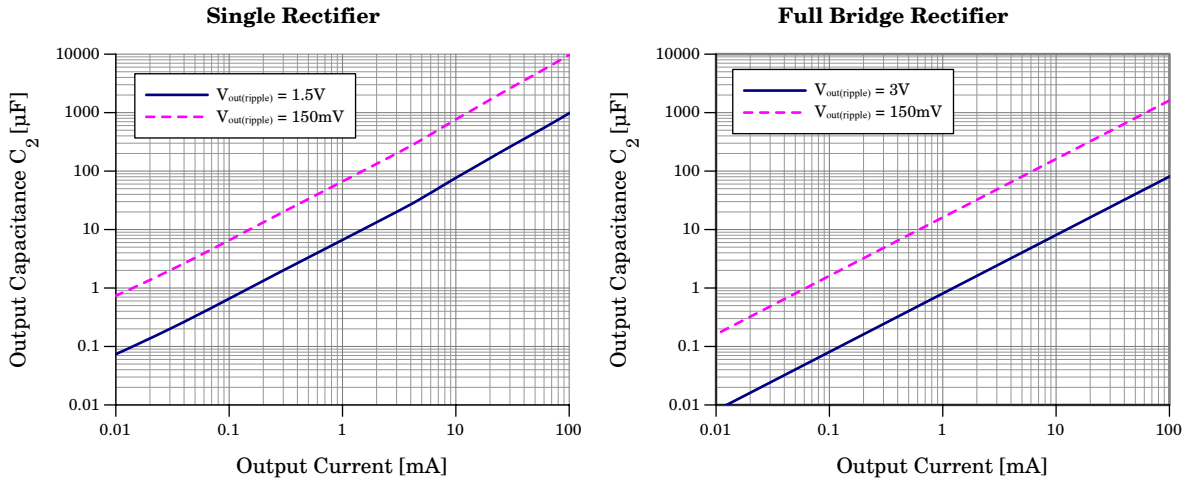

Figure 3.8: Selection sheet for the output capacitor C_2 in the single rectifier topology (left) and the full bridge rectifier topology (right). The lower capacitance lines represent the minimum capacitor size that will not cause heat dissipation in the Zener diode. The upper capacitance lines represent an output voltage ripple of 150 mV.

Figure 3.9 shows the simulated startup of the two capacitive power supply topologies. Both were dimensioned for 30mA output current and have been dimensioned for an output voltage of V_{out} = 15 V to supply a resistive load of R_{load} = 430 Ω. $C_2$was dimensioned to meet the efficiency criteria not to dissipate power in the Zener diode. Clearly evident is the longer startup time of about 0.5 seconds for the single rectifier topology (left) in this configuration which is caused by the large output capacitor which is necessary to meet the efficiency criteria. When the output voltage ripple is decreased by choosing a larger output capacitance C_2 this effect is even amplified. The output ripple is linearly dependent on the output capacitance and therefore also linearly dependent on the startup time.

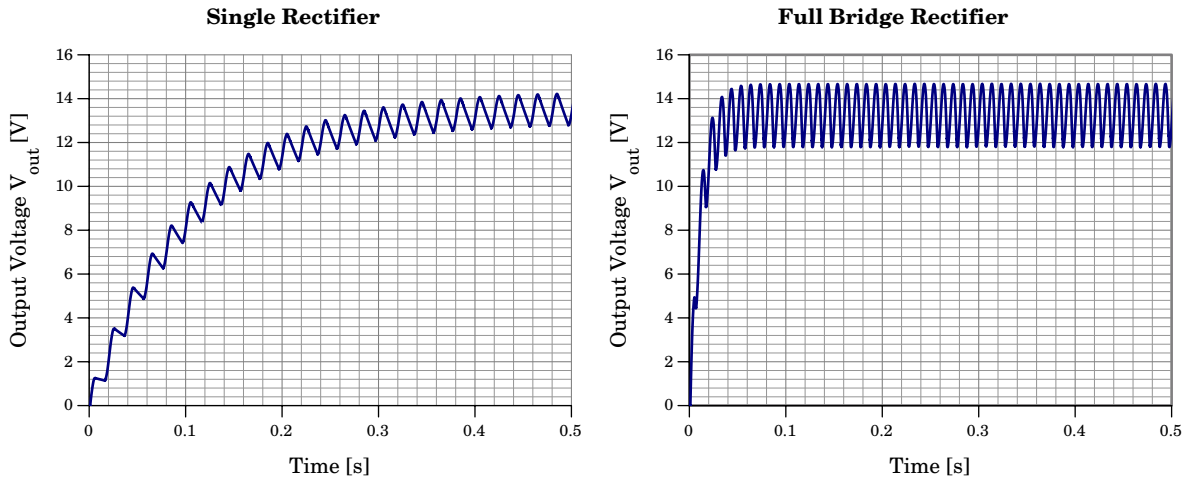

Figure 3.9: Simulated startup of the capacitive power supply with a single rectifier (left) and a full bridge rectifier (right). Single rectifier topology dimensioning: C_1 = 1 μF, C_2 = 250 μF. Bridge rectifier topology dimensioning : C_1 = 500 nF, C_2 = 25 μF.

Which output capacitor dimensioning is best is depending on the actual application. Usually a simulator is used to optimize the output capacitance and to consider additional parameters. When using an aluminum electrolytic capacitor the limited lifetime of the selected capacitor has to be considered.

The Inrush limiting resistor R_1 : The inrush limiting resistor R_1 has to be considered very carefully. It is often a subject to wrong dimensioning because not all important parameters are taken into account.

The first and also most important step is to determine the maximum allowed inrush current. A high current event can occur when the capacitive supply is initially plugged into the mains and the current limiting capacitor is not yet charged. The worst case which should be used for this calculation is when the supply is plugged in at the maximum of the input voltage sine wave. In this case the full 325 V (considering 230 V as effective mains voltage) is applied to the capacitor, which itself poses as a short in this moment because he is not charged.

The inrush current itself travels through the rectifier in both variants but can also travel through the Zener diode in the single rectifier version, depending on the implementation details. This gives a first idea of the maximum allowable current.

Not only the rectifier has to tolerate the inrush current, but also the current limiting capacitor C_1 and the inrush current limiting resistor R_1 itself. While the current limiting capacitor usually has no problem with the inrush current, the inrush current limiting resistor R_1 eventually has. Dimensioning of R_1 to a maximum allowable current of about 32 A which the rectifiers would sustain would lead to a resistor value of about 10 Ω (considering a maximum mains voltage of 325 V) which would lead to a peak power dissipation of about 10 kW at the resistor. That would destroy most usable resistor types.

This is still not the worst case when designing a reliable circuit. When the device is plugged in, the physical connections of the plug are not immediate and continuous. The contact will most likely bounce, which does not matter when the capacitor is discharged. But when the connection gets lost again when the capacitor is charged to the mains voltage maximum, it is likely that the connection is reestablished when the mains voltage is near it's minimum which is -325 V because that would result in a much higher voltage difference. That may cause a little flash-over at the plug and would result in a charging voltage of 650 V. Using the 10 Ω resistor from above would result in an inrush current of 65 A which would probably destroy the rectifier and the resistor. The worst case of an initial inrush event calculates to :

$$I_{max} = \frac{V_{mains(eff)} \cdot 2 \cdot \sqrt{2}}{R_1} \tag{6}$$

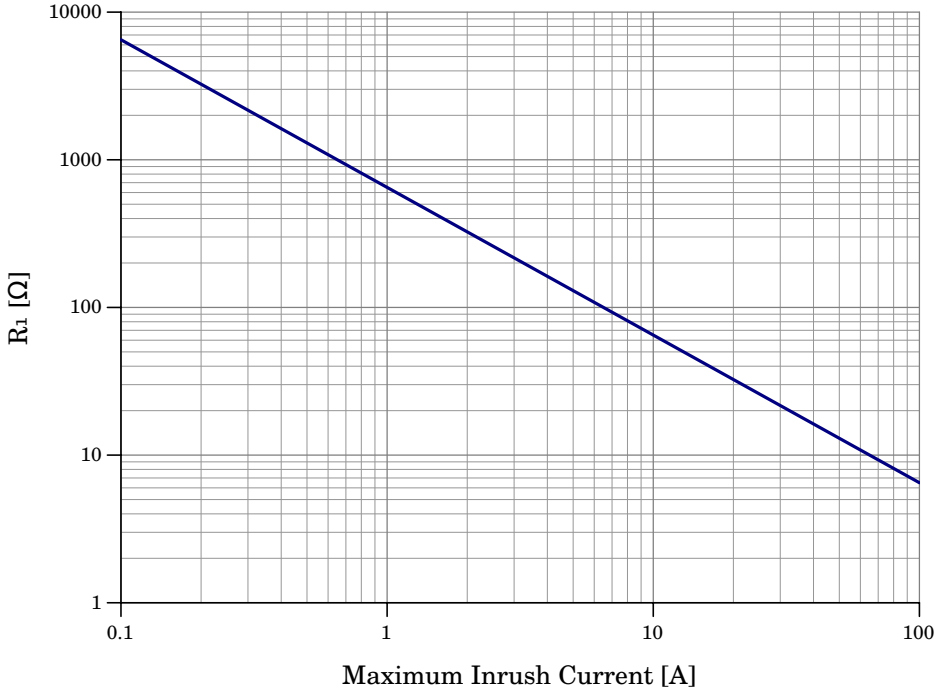

Figure 3.10: Selection of the inrush current limiting resistor R_1 depending on the maximum allowed inrush current for an effective mains voltage of 230 V.

With a given effective mains voltage of 230 V, the minimum resistance of the inrush current resistor R_1 calculates to :

$$R_{1(min)} = \frac{650V}{I_{max}} \tag{7}$$

Figure 3.10 offers a selection sheet for the inrush current resistor R_1. Note that this is a minimal value that may have to be increased as described in the next paragraph.

After the maximum inrush current has been determined and a minimum inrush current limiting resistor R_1 has been selected, the pulse duration of the inrush current has to be considered, as it may require further increase of R_1. The energy in which is dissipated in R_1during such an inrush event calculates to :

$$E_{inrush(R_1)} = \int i^2_{inrush}(t)\, dt \cdot R_1 \tag{8}$$

The inrush current pulse for a single inrush event calculates to:

$$i_{inrush}(t) = I_{max} \cdot e^{-\frac{1}{R_1 \cdot C_1} \cdot t} \tag{9}$$

Usually a quick simulation gives good information about the inrush event and if the pulse duration combined with the pulse height is compliant with the corresponding datasheet parameters of the resistor and the rectifiers.

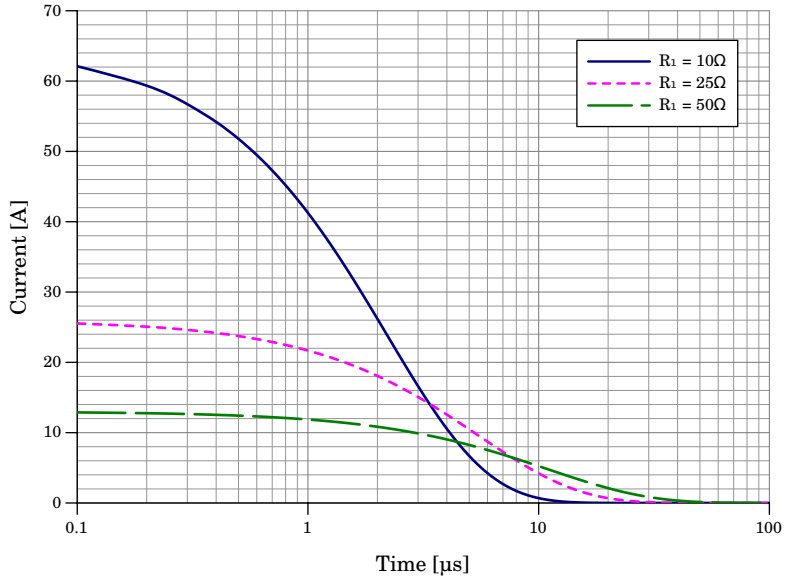

Figure 3.11: Worst case plug-in inrush event for different values of R_1 (10 Ω, 25 Ω, 50 Ω) for a current limiting capacitor C_1 = 220 nF and an effective mains voltage of 230 V.

Figure 3.11 shows the worst case inrush event during the initial connection of the supply to the mains for different values of R_1. Lower values of R_1 lead to higher and shorter inrush pulses, while larger values of R_1 lead to lower but longer inrush events. One may argue that the line impedance prohibits such high and short current pulses. This may be the case but if the supply is connected to the mains near another device that is utilizing a capacitor in parallel of the mains for filtering purposes short high current peaks are possible. Using a high pulse load MELF type resistor is strongly recommended as inrush current limiting resistor when working with SMD elements. Depending on the type they can handle single pulses of about 10 kW. Considering the pulse duration and the pulse repetition trough the contact bouncing, R_1 should be dimensioned with enough margin.

The discharge resistor R_2 : R_2 is responsible for discharging the current limiting capacitor C_1 after the supply is disconnected from the mains. The European norm EN60204-1 [CEN06] states in section 6.2.4 (Protection against residual voltages) that after a device is unplugged and the plug pins are touchable by a user the voltage must be discharged to 60 V or below within 1 second. When no live parts are touchable, the time can be 5 s. All devices having a stored charge of 60 μC or less are excluded from this regulation. A special exception can be made when the discharging process would interfere with the normal operation of the device. In this case a warning sign is required.

Hence the actual application area of the device in question has fundamental influence on the required discharge resistor R_2. Usually a discharge time of 1 second for mobile equipment and 5 seconds for fix installed applications can be assumed.

Starting from a maximum allowed charge of 60 μC the highest capacitance that can be used without a discharge resistor at 230 V mains would be :

$$C_{1(max)} = \frac{Q}{U} = \frac{60\mu C}{325V} = 184\,nF \tag{10}$$

If the capacitive power supply is designed to deliver more current a bigger capacitance has to be used and therefore a discharge resistor is needed. The voltage at the capacitor which is estimated the voltage on the plug calculates to :

$$U_c(t) = 325 \cdot e^{\frac{-t}{\tau}}, \tau = R_2 \cdot C_1 \tag{11}$$

This leads to the equations to calculate the maximum resistance value of the discharge resistor R_2 for a given discharge time $t_{discharge}$ and a given capacitance value of the current limiting capacitor C_1. Note that this calculations assume an effective mains voltage of 230 V which leads to a maximum mains voltage of 325 V.

$$U_{C(1s)} = 60V = 325V \cdot e^{-\frac{1s}{R_2 \cdot C_1}}, \qquad R_{2(max)} = \frac{t_{discharge}}{C_1 \cdot 1.69} \tag{12}$$

Figure 3.12 shows the dependency of the discharge resistor R_2 from the capacitance C_2which is shown in equation 10 as a selection guide for R_2. Typical values of R_2 are in the range of a few MΩ. Although R_2 does not need to sustain the inrush current, it must handle the mains voltage and may be exposed to high voltage peaks. The average power dissipation requirements of R_2 usually is met through the physically bigger size which is necessary to withstand the full mains voltage.

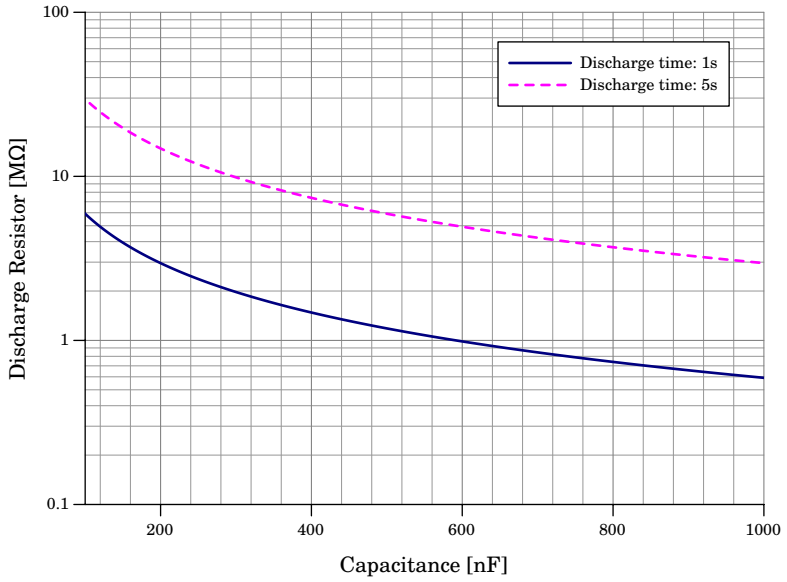

Figure 3.12: Selection of a discharge resistor R_2 depending on the current limiting capacitor C_1 for discharge times of 1 second and 5 seconds.

3.1.5 Various existing enhancements

Besides the well known basic operational principle, the field of capacitive power supply circuits is a wide research area because there is still much room for enhancement. There has been made a lot effort to eliminate some weak points of the supply circuit. One weak point is the constant effective power dissipation which is independent of the load. A way to circumvent this problem is to detach the buffer capacitor and short circuit the Zener diode using a transistor. This is easy for the single rectifier version as the buffer capacitor is automatically detached trough D_1 when the Zener diode D_5 is shortened by the transistor T_1. Figure 3.13 is showing the suitable circuit. The control logic which is attached to transistor T_1 is monitoring the output voltage. When the output voltage reaches its designated value, the transistor T_1 is switched on and the Zener diode is shortened. This shifts the input voltage-current phase so that almost no effective power is consumed. Hence the losses in the Zener diode cease to exist in this operating state. When the output voltage drops to a certain level, the transistor is switched off again and the supply is entering normal operation to refill the buffer capacitor C_2. This enhancement is very effective for loads that consume power only for a short period of time and are in a standby mode the rest of the time. An US patent [Ben09] describes the basic concept of shorting the Zener diode in greater detail.

Shorting the Zener diode to reduce effective input power is a little more complicated for the full rectifier version which was introduced in figure 3.1. The output capacitor has to be detached before the Zener diode is shorted, otherwise the output capacitor C_2 would be discharged. Figure 3.14 is showing a possible circuit. Transistor T_2 has to detach the capacitor before transistor T_1 shortens the Zener diode. Transistor T_2 could be replaced by a simple diode which would bring an additional diode forward voltage into the path which would slightly decrease efficiency. The supply in figure 3.14 would have better efficiency for changing loads but the rectifier bridge D_1 - D_4 is still in the current path in standby operation when T_1 is shortened.

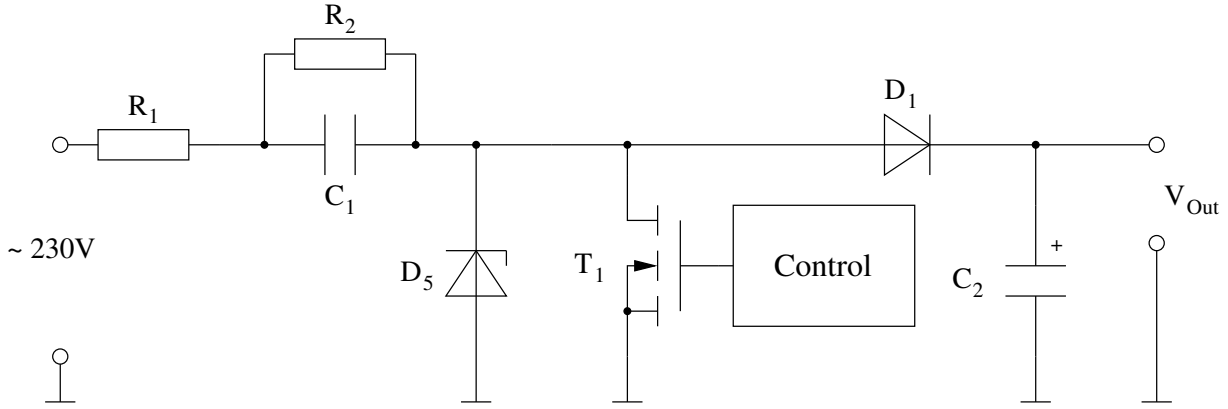

Figure 3.13: Capacitive Power Supply with enhanced efficiency for changing loads. The transistor T_1 shortens the Zener diode D_5 when the output voltage reaches its designated value. In this state the supply draws almost no effective power.

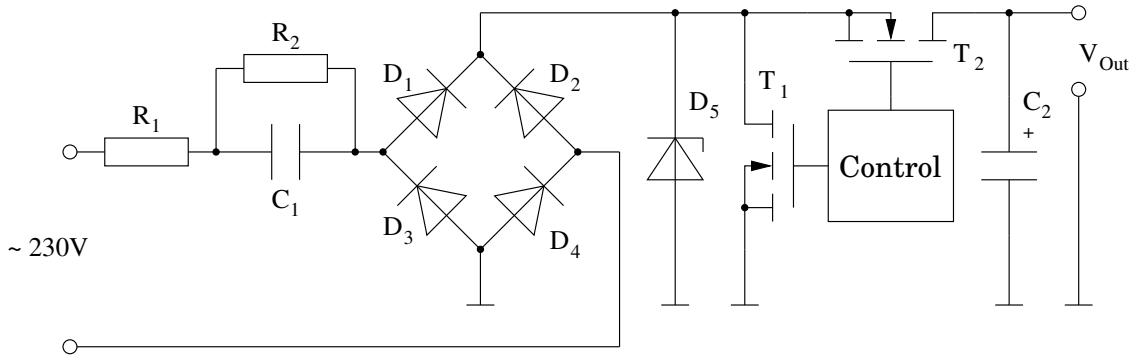

Figure 3.14: Capacitive Power supply with a full rectifier bridge and enhanced efficiency for changing loads. When the output voltage reaches a certain level, the output capacitor C_2 is detached by transistor T_2 and the Zener diode D_5 is shortened by transistor T_1.

Another way to improve efficiency for changing loads was used earlier because it can work without an integrated control logic. Depending on the current consumption of the load, the supply is switched from full way rectification to half way rectification. Figure 3.15 is showing a suitable circuit which is described in more detail in patent [Hei01].

Switching to half way rectification would halve the effective power consumption of the supply which translates to half of the effective output power. This operation principle can be very useful when the output voltage shall not drop too fast and too low when the supply is turned down and the load is requesting power again.

When the Zener diode is shortened completely, the voltage on the buffer capacitor C_2 will drop to a point where the supply is reactivated again. By switching to half wave rectification the supply can still provide power to the load and when the voltage on the buffer capacitor begins to drop which means that the load is requesting more power, the supply is turned to full rectification again.

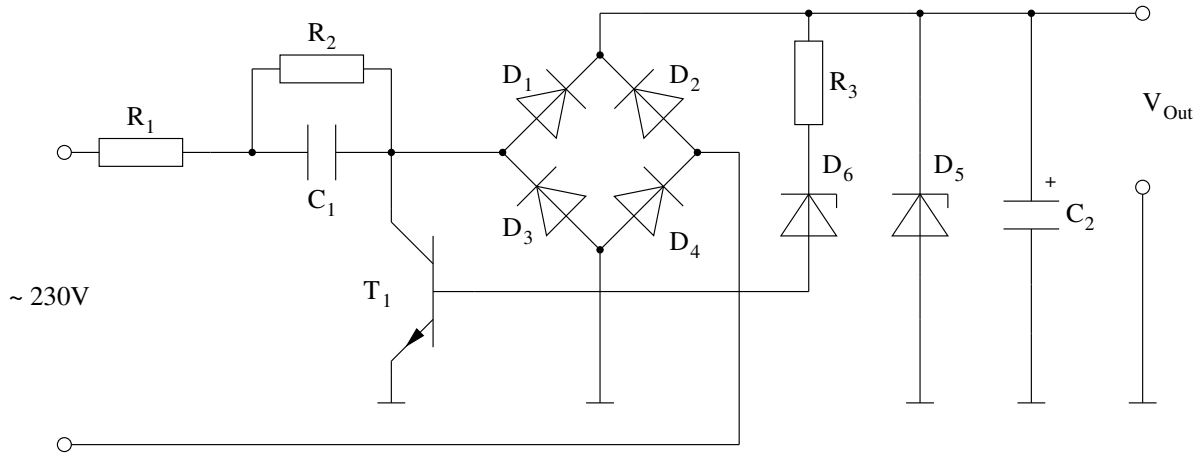

Figure 3.15: Load dependent full bridge to half wave rectifier switchover. Whenever the output voltage reaches a certain level, which is defined by the Zener voltage of D_6, current can flow trough T_1 which will shorten one rectifier pair of the bridge rectifier D_1 - D_4.

Patent [Ste07] is describing another way of enhancing the efficiency for changing loads. In principal the concept operates by utilizing two capacitive supply voltage sources that are connected in series. If the load doesn't need full power, one of the voltage sources is switched off by shorting the Zener diode.

Besides the work on enhancing the supply by shorting the Zener diode, designers have tried to enhance the supply by finding a more efficient way of inrush current limitation. The obvious idea is to short circuit the inrush current limiting resistor of the supply after the startup to make the supply more efficient. Patent [Gon12] describes doing so with a TRIAC. Another idea is to use two depletion type transistors that can operate in current limiting mode connected anti-serial instead of the inrush limiting transistor as patent [Car11] describes. However, these advancements are not suitable for the investigated application field as they would require additional high voltage components.

3.2 Switching mode power supply topologies

The second candidate to implement a suitable standby power supply for a smart appliance is an SMPS-based topology. Unlike linear supply types the SMPS utilizes a power switch that is either completely on or completely off to control the current flow through an inductor. The output voltage is regulated by the duty cycle of the power switch. This supply type is usually more efficient but also more complex to design. On the other hand this topology needs at least one high voltage switch and in case of a simple SMPS approach lots of other components that have to sustain the rectified mains voltage. This chapter first gives an overview of state-of-the-art SMPS converters that can be used in a non-isolated standby power supply for smart appliances.

Depending on the application field several SMPS topologies are available. The most basic topologies are the buck or step-down converter and the boost or step-up converter. The buck converter converts a higher input voltage into a lower output voltage while the boost converter on the contrary converts a lower input voltage to a higher output voltage. Additionally there are several hybrid topologies that offer buck/boost mode to handle a wider input voltage range. Some topologies can also be used to act as voltage inverters which means the output voltage is negative. Depending on the actual application the converter can utilize just one power switch, a half bridge configuration or a full bridge configuration. It is also popular to use multiple switches and multiple inductors to work in a multi-phase mode to reduce stress on the input. This is done especially for high power converters.

To describe every possible converter topology would clearly go beyond the scope of this work, therefore only topologies that are relevant for non-isolated standby supplies in smart appliances are described in this section. Converter topologies with more than one inductor are discarded with respect to higher costs and reduced integration possibilities, as they have no significant advantage for the target application area. Furthermore isolated topologies are left out too due to the size and the high cost of the necessary transformer.

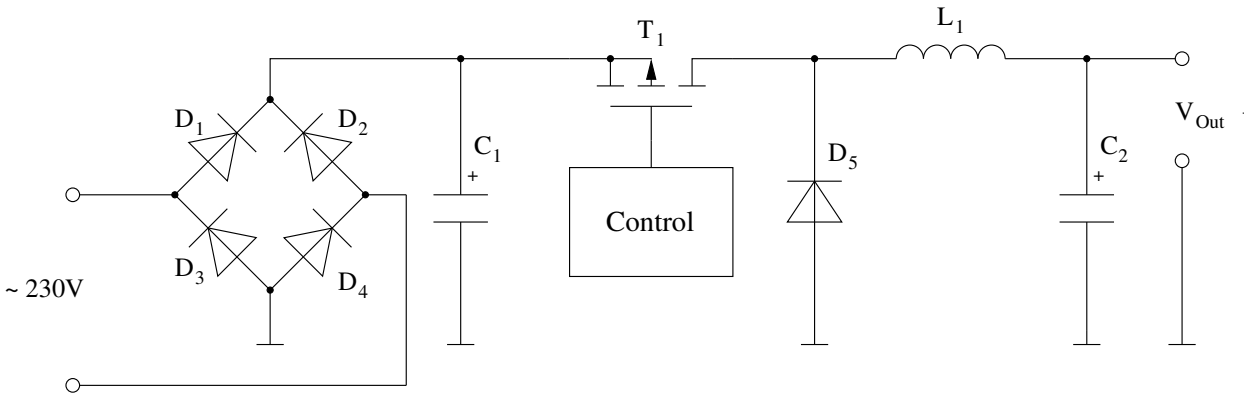

Figure 3.16: Principal schematic of a simple buck converter operating directly from the mains. D_1- D_4 are the rectification bridge, C_1 is the input storage capacitor and C_2 is the output buffer capacitor. T_1 is used to control the current through the inductor L_1 while D_5 automatically takes over the current when T_1 is switched off.

3.2.1 Simple buck converter

The buck converter is a widely used and efficient converter topology to convert a high input voltage to a lower output voltage. Figure 3.16 shows the buck converter topology which was introduced in figure 2.6 in greater detail.

The converter in figure 3.16 is operated directly from the 230 V mains. The mains voltage is rectified through the rectification bridge (D_1- D_4) and stored in the input storage capacitor C_1. During the on-phase of transistor T_1, current is flowing from the input over the inductor L_1 into the output capacitor C_2 while storing energy in the inductance L_1. During the off-phase of transistor T_1 current is still flowing through the inductance into the output capacitor but flowing through D_5 instead of coming from the input. Note that in both phases power is transfered to the output.

The inductor L_1 acts as an energy storage element used to transfer energy from the input to the output. During the on-time of the transistor T_1 the current through L_1 is rising and therefore energy is stored in L_1. The energy stored in L_1 calculates to :

$$E_L = \frac{L_1 \cdot I_L^2}{2} \tag{13}$$

During the off-time of the transistor T_1 the energy that is stored in L_1 is transfered to the output while the current is flowing through D_5 if the converter operates in discontinuous conduction mode (DCM).

When the buck regulator operates in continuous conduction mode (CCM) the inductor current has the shape of a triangle which never reaches zero in steady state. Whenever the current in L_1 however reaches zero during the off-time of T_1, the buck regulator operates in discontinuous conduction mode (DCM).

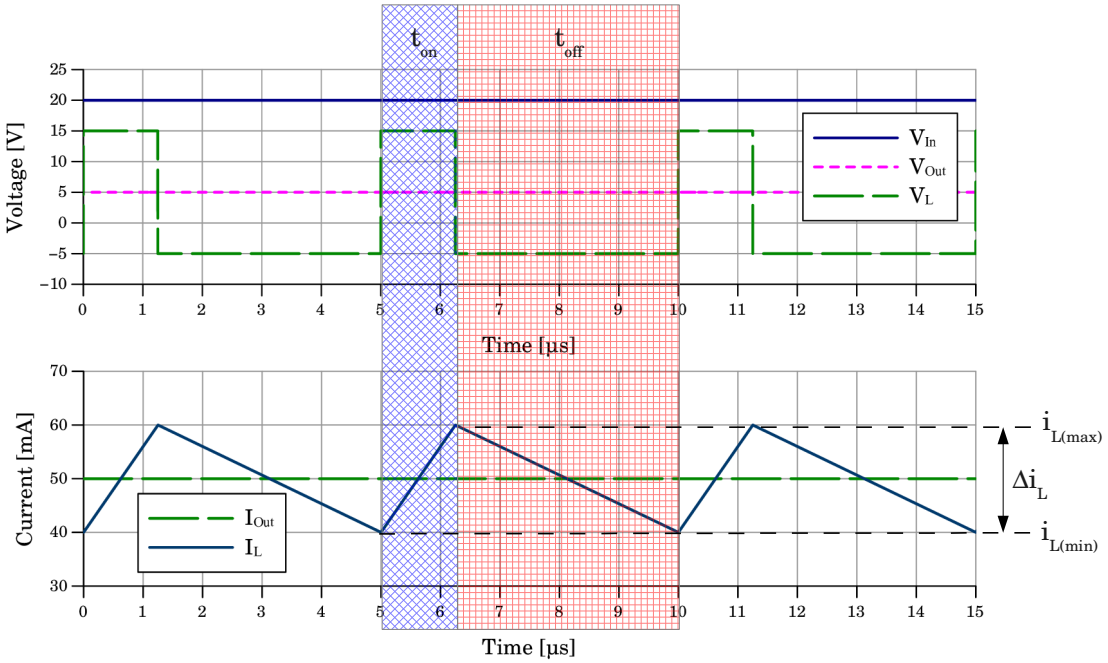

Figure 3.17: Buck converter from figure 3.16 operating in continuous conduction mode. V_{in} = 20 V, V_{out} = 5 V, I_{out} = 50 mA. The inductor current I_L doesn't reach zero during the off-time of transistor T_1.

Continuous conduction mode Figure 3.17 shows typical steady state current and voltage curves for a buck converter operating in CCM. The input voltage V_{in} at the input storage capacitor $C_1$is 20 V. The supply is configured for an output voltage V_{out} of 5 V which is the voltage at the output buffer capacitor C_2. The output current of the supply is 50 mA. For a first characterization no losses are considered. During the on-time t_{on} of the transistor $T_1$the inductor voltage V_L is V_{In}- V_{Out} and the inductor current I_L is rising from 40 mA to 60 mA. During the off-time of the transistor T_1 the inductor voltage is -$V_{Out}$and the inductor current I_L is falling from 60 mA to 40 mA. The current is flowing through the diode D_5 during this time. The inductor current doesn't reach zero during the off-time.

The switching cycle t_{cycle} is started with the on-time t_{on} of the transistor T_1 which is followed by the off-time t_{off} of the transistor T_1. This leads to :

$$t_{cycle} = t_{on} + t_{off} \tag{14}$$

The inductor voltage during the on-time of transistor T_1 $V_{L_{ON}}$ and the inductor voltage during the off-time of transistor T_1 $V_{L_{OFF}}$ therefore calculate to :

$$V_{L_{ON}} = V_{in} - V_{out} \tag{15}$$

$$V_{L_{OFF}} = -V_{out} \tag{16}$$

This leads to the calculation of the inductor current change ΔI_L which has to be zero when observed over an entire switching cycle t_{cycle} because the converter is in steady state :

$$\Delta I_{L_{ON}} = \frac{1}{L} \int_0^{t_{on}} (V_{in} - V_{out}) dt = \frac{V_{in} - V_{out}}{L} \cdot t_{on} \tag{17}$$

$$\Delta I_{L_{OFF}} = \frac{1}{L} \int_{t_{on}}^{t_{cycle}} (-V_{out}) dt = \frac{-V_{out}}{L} (t_{cycle} - t_{on}) \tag{18}$$

$$\Delta I_{L_{cycle}} = \frac{1}{L} (\int_0^{t_{on}} (V_{in} - V_{out}) dt + \int_{t_{on}}^{t_{cycle}} (-V_{out}) dt) = 0 \tag{19}$$

$$\Delta I_{L_{ON}} = \Delta I_{L_{OFF}} = \Delta I_L \tag{20}$$

Equation 17 can be further simplified to :

$$(V_{in} - V_{out}) \cdot t_{on} - V_{out} \cdot (t_{cycle} - t_{on}) = 0 \tag{21}$$

$$V_{in} \cdot t_{on} - V_{out} \cdot t_{cycle} = 0 \tag{22}$$

$$\frac{t_{on}}{t_{cycle}} = \frac{V_{out}}{V_{in}} = D \tag{23}$$

This leads to the duty cycle D which is determined only by the ratio of the output voltage and the input voltage and is independent of the inductor L_1 and the switching frequency f_s. ΔI_L on the other hand is dependent on the inductor L_1, the output current which is the average inductor current and the switching frequency. The output current of the supply equals the average inductor current I_L which is 50 mA in figure 3.17. CCM designs have the advantage of a low inductor peak current compared to its average current. Therefore the ripple at the output capacitor is lower compared to other designs. Typically CCM designs use a fixed switching frequency. The main disadvantages are the relatively big inductor compared to other design types and the losses through the reverse recovery current of the diode D_5 in figure 3.16. These losses can be decreased by the utilization of a Schottky diode if the input voltage is low enough. A higher inductance value leads to a lower peak inductor current and allows for a smaller switching frequency which leads to fewer switching losses. On the other hand the conduction losses are typically increased as a result of the higher current. Therefore there is always a tradeoff between the switching losses and the conduction losses.

When the output current ls lowered through a lighter load, the supply reaches a point where the inductor current reaches zero during the off-phase. This critical output current calculates to $\Delta I_L/2$ and marks the transition to the discontinuous conduction mode (DCM). When the supply is operated at that exact point, the supply is in critical conduction mode which is sometimes also referred to as transition mode or boundary conduction mode.

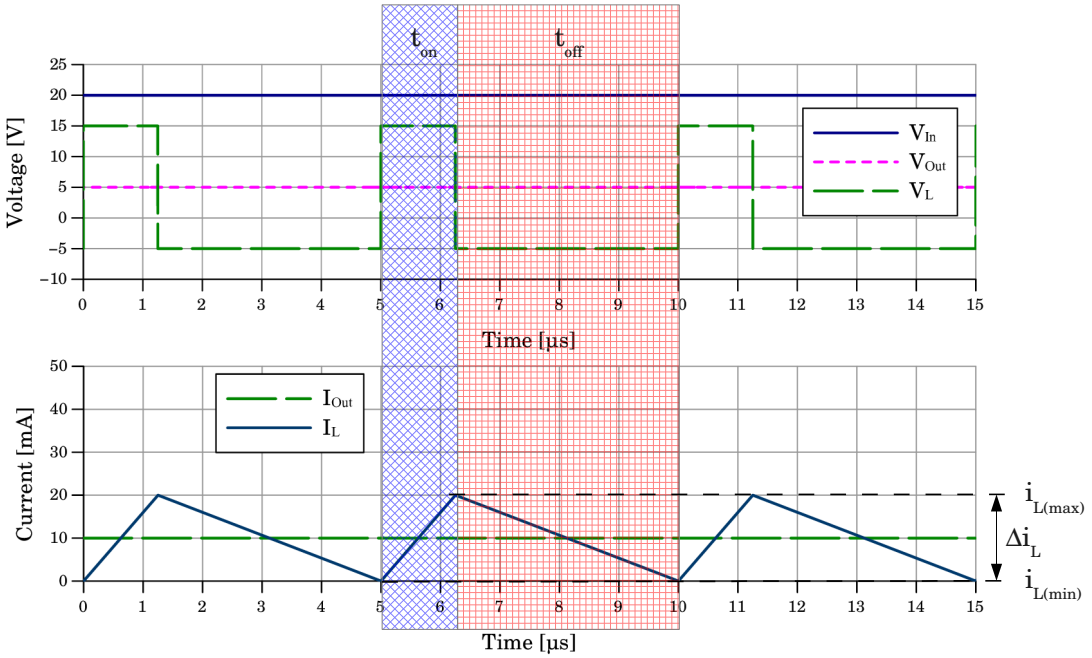

Figure 3.18: Buck converter from figure 3.16 operating in critical conduction mode. V_{in} = 20 V, V_{out} = 5 V, I_{out} = 10 mA. When the inductor current reaches zero the transistor is switched on again and a new switching cycle begins.

Critical conduction mode When the output current of the converter that operated in CCM in figure3.17 is lowered to $\Delta I_L/2$, while the other parameters are kept constant, it reaches the transition from CCM to DCM. Some regulator concepts are even designed to work exact in the transition between the continuous conduction mode and the discontinuous conduction mode by adjusting their switching frequency. This operation mode is called critical conduction mode (CRM). Figure 3.18 shows typical steady state voltage and current curves of a buck converter in CRM mode. The input voltage V_{In} is 20 V and the output voltage V_{Out} is 5 V. The output current of the supply is now 10 mA. During the on-time t_{on} of the transistor $T_1$the inductor voltage V_L is V_{In}- $V_{Out}$and the inductor current I_L is rising from 0 mA to 20 mA. During the off-time of the transistor T_1 the inductor voltage is -$V_{Out}$and the inductor current I_L is falling from 20 mA to exactly zero. Immediately after the inductor current reaches zero the transistor is switched on again and the next switching cycle begins. Hence a higher output current automatically leads to a smaller switching frequency.

Depending on the output current the switching frequency is changed so that the inductor current reaches zero in every switching cycle. Hence CRM operation has some advantages due to its zero current switching character. There is no hard reverse recovery current in D_5 during the switch-on of transistor T_1 which reduces losses and EMI. Also the inductance is smaller compared to the CCM design which makes it easier to integrate. A disadvantage of the CRM mode is the higher inductor peak current when it is compared to a CCM design with the same output current. This will cause additional losses in the power switch and the inductor but the overall efficiency and usability depends on the actual application and

may be better for a CRM design. Some solutions were found to minimize losses in CRM designs [PC05]. When the CRM converter is operated with a variable switching frequency to compensate for changing loads or a variable input voltage and the output current is falling, the switching frequency is increased to hold CRM operation. This may be limited through the determined maximum switching frequency of the converter with respect to admissible switching losses. When the output current is further falling, the design enters DCM.

Discontinuous conduction mode DCM operation is reached whenever the output current is smaller than $\Delta I_L/2$ compared to the CCM. This is usually happening in light load conditions of a CCM design when the output current falls under $\Delta I_L/2$. Figure 3.19 shows typical steady state voltage and current waveforms of a buck converter in DCM. The input voltage V_{In} is 20 V, the output voltage V_{Out} is 5 V and the output current I_{Out} is 2.5 mA. During the on-time t_{on} of transistor T_1 the inductor current increases from 0 to 10 mA. The inductor voltage V_L which is in combination with the inductance L_1 determining the slope of the inductor current is V_{Out} - V_{In} during this period. During the off-time t_{off} of transistor T_1 the inductor current I_L is first falling from 10 mA to 0 mA. During this time the inductor voltage V_L is -V_{Out}. After the inductor current I_L reached zero, the inductor voltage V_L jumps to zero too and stays there until the next on-period.

The discontinuous conduction mode is usually characterized by a high inductor peak-to-average current ratio which may lead to higher losses compared with CCM or CRM operation depending on the contribution of the reverse recovery losses of the used diode and the distribution of the switching and conduction losses.

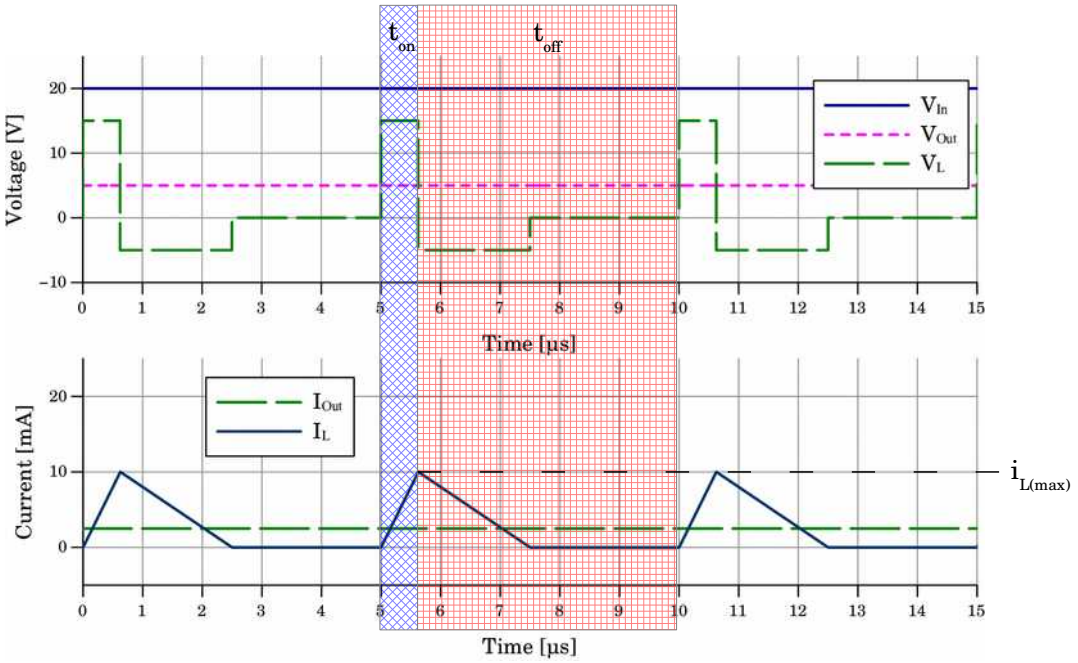

Figure 3.19: Example waveforms for a buck converter in DCM operation. V_{in} = 20 V, V_{out} = 5 V, I_{out} = 2.5 mA. The inductor current reaches zero during each switching cycle.

Although a smaller inductor can be used for the same output current and the same switching frequency which makes integration easier, the high peak inductor current may result in problems with core saturation. Like the CRM this operation mode has no reverse recovery losses in D_5. DCM is typically used in converters that have to operate over a wide output current range where the output current can vary in order of magnitudes. The converter is then designed for CCM operation for the higher output current region and switches to DCM for the low output current region or for standby operation. This leads to poor light load efficiency due to the high losses compared to the output power in this operation mode. A solution to this problem is the burst mode [JMXX08] or skip-cycle mode [LWLX09]. This operation mode utilizes CCM bursts to avoid DCM operation. Between the bursts the control IC can go to standby which further decreases losses. Through this technique the efficiency for light loads can be dramatically increased.

Synchronous rectification SMPS topologies require a free-wheeling diode (D_5 in figure 3.16) to operate. Its purpose was to takeover the inductor current when the transistor T_1 switches off. This diode causes several losses during circuit operation. Losses in the diode D_5 can be divided into conduction losses caused by its forward voltage and switching losses caused by its reverse recovery charge. The forward voltage of the diode as well as its reverse recovery charge are therefore of great importance. A Schottky diode utilizes a metal-semiconductor junction and brings a lower forward voltage as well as a smaller capacitance resulting in a shorter recovery time compared to a standard bipolar diode. Hence the switching diodes in SMPS topologies are typically Schottky diodes. To further increase efficiency, the diode can be replaced by a properly controlled transistor. This gives an advantage in the low voltage range, because the constant diode forward voltage is replaced by a smaller voltage drop caused by the on-resistance of a MOSFET transistor. For high current converters the voltage drop at the on-resistance of the MOSFET may exceed the forward voltage of a simple Schottky diode which would give the Schottky diode the efficiency advantage. Additionally the MOSFET has a much larger reverse recovery charge due to its big body diode which would increase the switching losses when a MOSFET is used as rectifier. The rectifying transistor has to be controlled synchronously to the other transistor which gives this topology the name synchronous buck converter. Figure 3.20 shows the principal schematic of a synchronous buck converter.

Synchronous converter topologies have a more complex control system because the two transistors have to be switched almost simultaneously, but not entire simultaneously to avoid a current shoot-through of both transistors and the resulting efficiency decrease. To evaluate the overall efficiency, including the losses in the control logic, the actual application parameters (e.g. input voltage, output voltage, output current, switching frequency...) have to be considered. Depending on the actual application both topologies are still used in state-of-the-art designs. Synchronous rectification is not limited to the buck converter design but can be used in any other SMPS converter topology too.

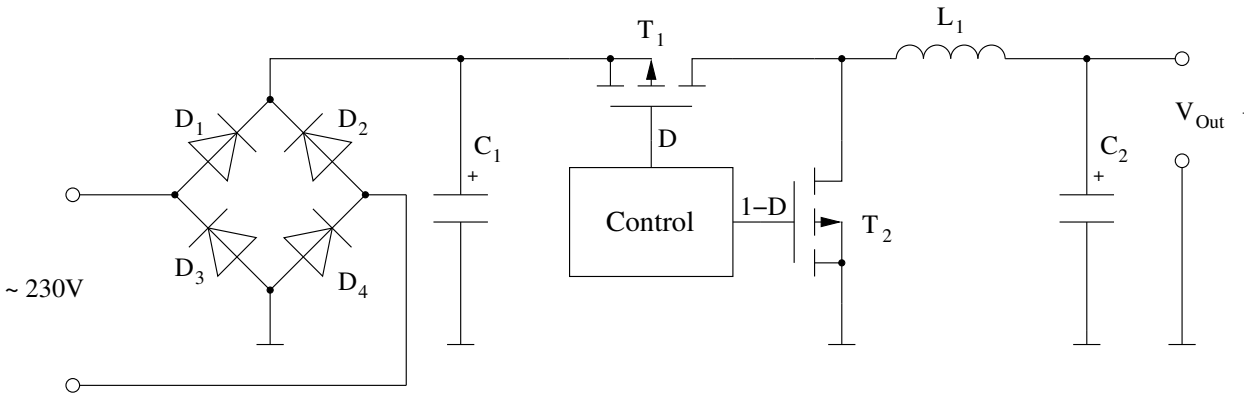

Figure 3.20: Principal schematic of a synchronous buck converter. The rectifier is replaced by the synchronous controlled transistor T_2. Due to the high switching losses of the MOSFETs this circuit variant is typically not efficient for a small output voltage.

3.2.2 Boost converter

A boost converter is used to convert a lower input voltage to a higher output voltage. It is often used in battery powered applications when there is not enough physical space to stack the battery cells to reach the target voltage. In that case a boost converter can generate the higher target voltage from fewer cells or even only one. In its simplest form, besides the input and output buffer capacitors, it needs only one switch, a diode and the inductor as energy storage element. Figure 3.21 shows the principal schematic of a simple boost converter topology. In case the converter is turned off, the output is still connected to the input over the diode D_1 and the inductor L_1. This may be a problem as the output can still draw power from the input even if the converter is turned off. During the on-phase of transistor T_1 current is flowing from the input through L_1 and T_1. No power is transfered to the output at that time. During the off-phase of transistor T_1 the current through L_1 will continue to flow from the input through T_1 but now has to flow to the output capacitor C_2 over diode D_1. This will allow the output voltage V_{Out} to reach higher levels than the input voltage V_{In}.

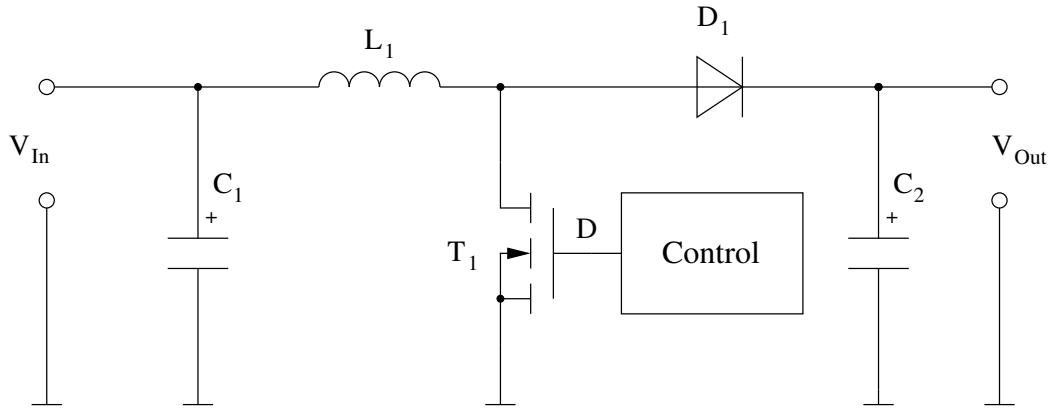

Figure 3.21: Principal schematic of a simple boost converter.

The boost converter can operate in the same operation modes as the buck converter. In CCM operation the current through the inductor never reaches zero. In CRM operation the inductor current reaches zero during the off-phase of transistor T_1 but immediately after that the transistor is turned on again which makes the inductor current triangular shaped as in CCM. Hence the switching frequency is variable during CRM operation. In DCM operation the inductor current reaches zero during the off-phase of T_1 and stays zero for the rest of the constant switching period. During DCM and CCM operation the switching frequency is fixed.

For CCM operation the output voltage is defined by :

$$V_{Out} = \frac{V_{In}}{1 - D} \tag{24}$$

$$D = \frac{t_{on}}{t_{cycle}} \tag{25}$$

$$t_{cycle} = t_{on} + t_{off} = \frac{1}{f_s} \tag{26}$$

The duty cycle D and the time of a switching cycle t_{cycle} is defined the same manner as for the buck converter during CCM operation. These equations apply for an ideal boost converter in CCM and suggest that the ratio of V_{Out} / V_{In} can be very high with the corresponding duty cycle D near one. Unfortunately, the losses increase significantly when the duty cycle reaches one which makes this topology less efficient for very high V_{Out} / V_{In} ratios. When estimating the possible output current I_{Out} of this converter type, the fact that power is transfered only during the off-phase of transistor T_1 has to be considered. The output current equals therefore the average of the diode current I_{D1} which is the current flowing during the off-phase of transistor T_1.

Figure 3.22 shows typical current and voltage waveforms for the boost converter in figure 3.21 operating in CCM with a constant duty cycle D of 0.5. The input voltage is 5 V, the output voltage is 10 V. During the on-phase t_{on} of transistor T_1 current is flowing from the input through the inductor L_1 and the transistor T_1. The inductor current is rising but no power is transfered to the output during t_{on}. During the off-phase t_{off} of transistor T_1 current is flowing from the input through the inductor L_1 and the diode D_1 into the output buffer capacitor. The inductor current I_L is falling during this period and power is transfered to the output. Because power is transfered only in the off-phase, the output current of the converter is not the average inductor current as it was for the buck converter but the average off-phase current which equals the diode current I_{D1}. Because the duty cycle D is exactly 0.5 in this example, the output current equals half of the average inductor current and therefore is 10 mA.

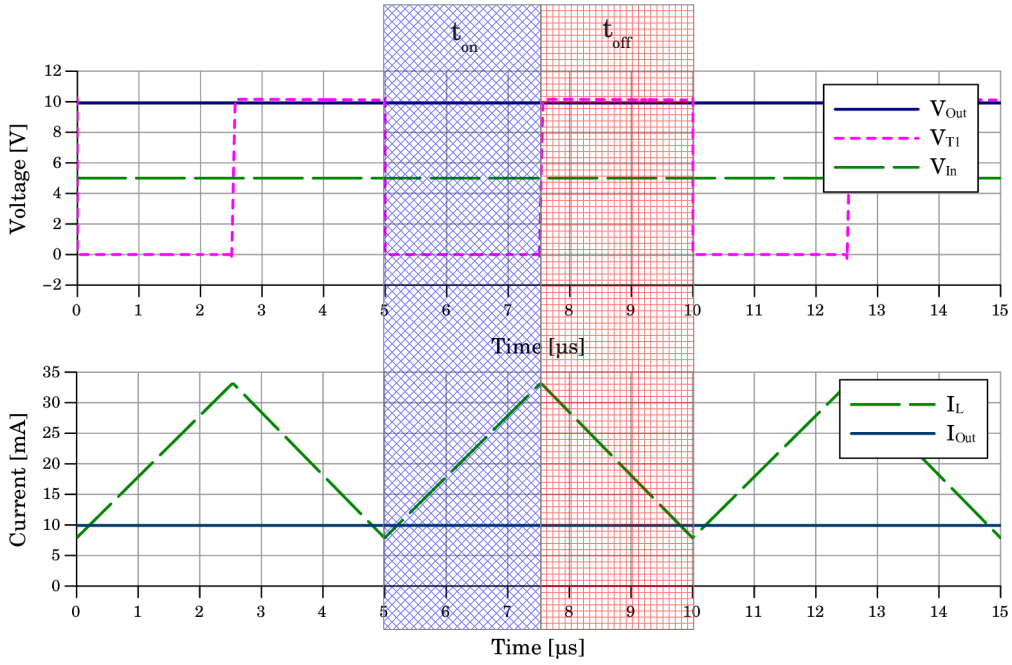

Figure 3.22: Typical voltage and current waveforms of the boost converter topology from figure 3.21 with a constant duty cycle D of 0.5 operating in CCM. V_{in} = 5 V, V_{out} = 10 V, I_{out} = 10 mA. Power is transfered to the output only during the off-time of transistor T_1.

3.2.3 Simple buck/boost converter

The buck/boost converter can convert an arbitrary input voltage into a higher or lower output voltage. Figure 3.23 shows a simple form of the buck/boost converter with one switch and one diode. By replacing the diode with a proper controlled transistor the circuit can be transformed into a synchronous buck/boost converter. A very important detail of the converter in figure 3.23 is that the output voltage has inverted polarity compared to the input voltage. This may be desirable when a negative voltage is needed but may also pose a problem. Like other SMPS topologies the buck/boost converter in figure 3.23 can operate in CCM or DCM. The power is transfered to the output only during the off-phase of transistor T_1.

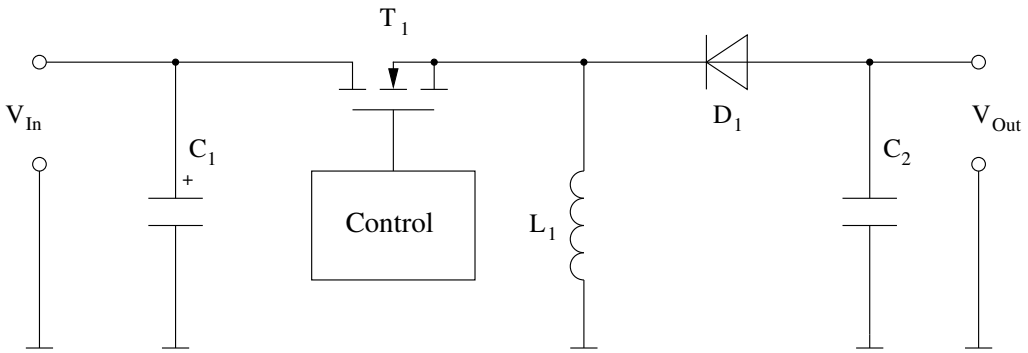

Figure 3.23: Simple buck/boost converter with an inverted output. This converter can convert an arbitrary input voltage to a higher or lower output voltage but has an inverted voltage polarity.

A typical application field of buck/boost converter topologies is battery driven equipment. That way the battery charge can be utilized over the whole voltage range even if the battery voltage drops below the operation voltage of the device (e.g. lithium ion accumulator voltage 2.8 V to 4.2 V - operation voltage 3.3 V)

Other buck/boost topologies don't have an inverted output but need a greater number of components. The SEPIC (single ended primary inductance converter) circuit uses two inductors and a capacitor as energy storage but only needs one switch and a diode. Its output is disconnected from the input when the converter is turned off and its output voltage has the same polarity as the input voltage. Similar topologies are the Ćuk converter [ST06] which has also an inverted output voltage and the Zeta converter [VB10]. The advantage of the Ćuk converter is that the input and the output current are continuous which may result in smaller input and output capacitors. A simple buck converter needs a bigger input capacitor because the circuit is drawing power from the input only during the on-phase of the transistor. A simple boost converter needs a bigger output capacitor because it's delivering power to the output only during the off-phase of the transistor. This advantage is paid for with a higher component count.

Another possibility to build a buck/boost converter is to combine a buck converter with a boost converter which basically increases the number of needed switches.

3.2.4 Full bridge buck/boost converter

A buck/boost converter can also be designed from a combination of a buck circuit and a boost circuit. Although the inductor can be shared, the so designed buck/boost converter has at least two switches and two diodes. If the diodes are replaced by switches as well to avoid the diode forward voltage and the affiliated losses, the design is a synchronous buck/boost converter. Figure 3.24 shows the principal schematic of the full bridge synchronous buck/boost converter. The blue (left) part is responsible for buck operation and the red (right) part is responsible for boost operation.

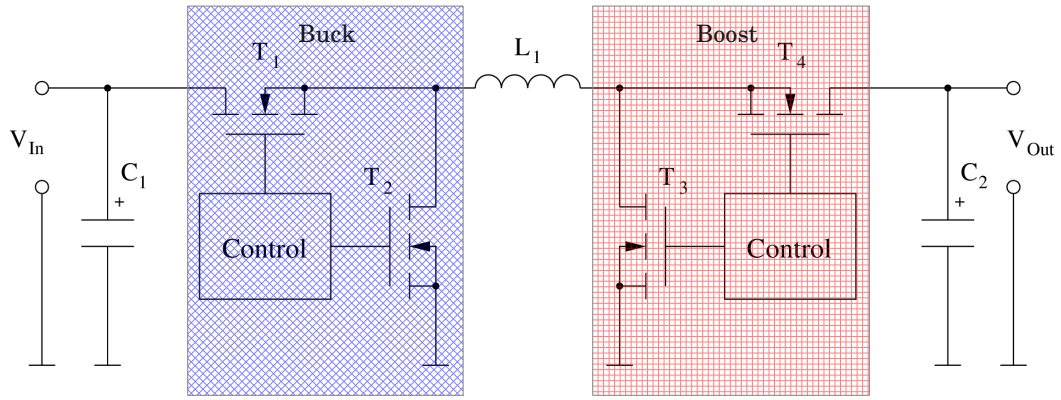

Figure 3.24: Principal schematic of a H-bridge buck/boost converter topology. This topology is a combination of the simple buck converter and the simple boost converter sharing a single inductor.

Because the control logic and the transistors can be integrated the full bridge buck/boost converter can operate with just an external inductor and the input buffer as well as the output buffer capacitor. This makes this converter not only versatile but also small. Because of the synchronous nature of this topology, it is suitable for medium output currents while offering very good efficiency. The actual implementation of the control logic defines the transition between buck and boost mode of the converter whenever necessary. State-of-the-art full bridge controller ICs offer a fluent transition without influencing the output voltage [GN04], while offering a good overall efficiency [ONS+11]. When the input voltage is much higher than the output voltage the converter operates in buck mode which means that T_1 and T_2 are switching alternately. T_3 is always off and T_4 is always on in this mode. When the input voltage is much smaller than the output voltage the converter operates in boost mode. In this mode the transistor T_1 is always on and T_2 is always off. T_3 and T_4 are switching alternately.

To avoid a short circuit of the output or the input the transistors T_1 and T_2 as well as the transistors T_3 and T_4 are considered pairs that are always switched together to opposing switching states. To prevent a current peak during the state transition of a transistor pair and the so resulting efficiency decrease, the conducting transistor is always switched off first, followed by a short dead-time before the other transistor pair is turned on.

When the input voltage is near the output voltage the converter operates in buck/boost mode. This operation mode is implementation dependent as there are different control methods. Some implementations always toggle both transistor pairs which charges the inductance in one cycle and discharges it in the next without respect to the actual voltage difference. This method has a higher ripple current and usually higher losses but ensures constant energy transfer from the input to the output even if the voltage levels are equal. Other implementation forms use this form of control only in the buck/boost region where the input and the output voltage are similar. There are also implementations that use both methods consequently in every cycle which ensures a smooth transition of the modes. The actual voltage difference between input and output is then determining the time each mode is active in each cycle [Max09].

3.2.5 Converter regulation

The control section of a SMPS has not been discussed yet. It derives the intended transistor states from different parameters and generates the corresponding gate voltages. It ensures proper load regulation as well as proper line regulation. Load regulation means that the supply can adapt do different loads whereas line regulation means that the supply can adapt to different input voltage levels. The switching frequency and the regulation type is also defined through the control section of the converter. There are two well known basic control principles for converter regulation as well as some newer variations. The voltage mode control was used in early converter designs. This control principle compares the output voltage to a reference voltage and adjusts the duty cycle accordingly.

To avoid instability a compensation network is necessary. Alternatively, the current mode control principle regulates the output voltage and the inductor current in an inner control loop to adjust the duty cycle. Both control principles as well as some variations are still used in modern converter designs.

Voltage mode control (VMC) The voltage mode control principle adjusts the duty cycle depending only on the output voltage. This control principle was used in the first converter designs and is still used as it has several advantages over other regulation variants. Figure 3.25 shows the principal schematic of a buck converter using voltage mode control. The output voltage V_{Out} is lowered by the feedback voltage divider consisting of R_1 and R_2. An error amplifier compares it to a reference voltage and gives an analog voltage as output which is proportional to the duty cycle which has to be set. The PWM modulator compares this output voltage to a sawtooth voltage which is oscillating with the switching frequency hereby generating the control PWM with the proper duty cycle.

Because this regulation has only the output voltage as parameter it is relatively slow. When the input voltage changes the converter cannot react immediately but has to wait for the output voltage to change in order to compensate. To avoid instability a compensation network has to be used with the error amplifier. For simple designs a PI-type compensator may be sufficient but usually a compensation network of higher order is used. This is especially necessary when using low ESR output capacitors (e.g. MLCC ceramic) [RPA]. Voltage mode control is not limited to buck converters but may be used on other SMPS topologies too. However, compensation may be more difficult.

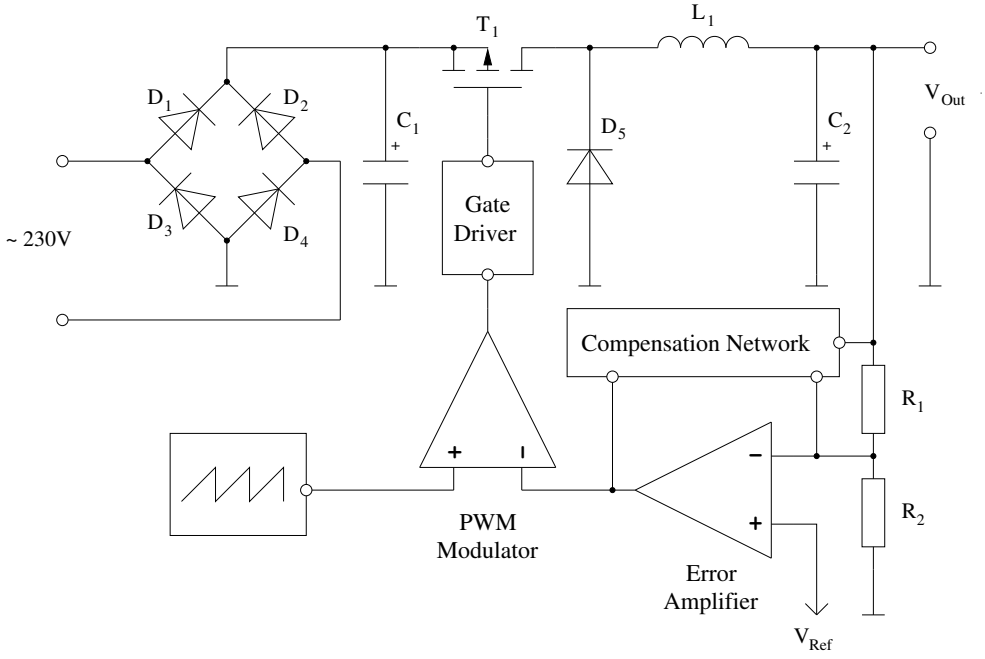

Figure 3.25: Principal schematic of a buck converter with voltage mode control. The output voltage is used as input for the regulator feedback loop.

The right half plane zero (RHPZ) problem is well known to occur in boost, flyback or Ćuk topologies in CCM operation but does not occur in buck converters. This is due to the indirect power transfer of the susceptible topologies [Tex01]. When the boost converter in figure 3.21 is regulated through voltage mode control the RHPZ problem occurs. When the load current is increased the output voltage will go down slightly. In order to compensate this the regulator is increasing the duty cycle. During the on-phase which is increased, the current is loaded into the inductor. This will compensate for the increased output current in the long run and the output voltage should go back to its nominal value. Unfortunately power is transfered to the output only during the off-phase of the transistor T_1, which has been decreased through the higher duty cycle. The reduced output power will immediately cause the output voltage to drop further before it is restored through the higher inductor current in the long run. A possibility to compensate this is to reduce the dynamic of the controller preventing it to go too far in the wrong direction.

Current mode Control (CMC) Current mode control not only takes the output voltage as parameter for converter regulation but the inductor current too. This will add an inner regulation loop to the converter which makes it much faster. There are several different current regulation techniques (peak current, average current, valley current) but the most common one is the peak current regulation principle. The basic idea is to measure the inductor current and when it reaches a predefined maximum level during the on-phase of the transistor the switch is turned off.

This control principle is stable for a duty cycle of < 50 % but inherently unstable for a duty cycle > 50 %. A small deviation in the inductor current would grow bigger over time and possibly lead to subharmonic oscillation of the inductor current. Slope compensation is a way to make the converter stable for all duty cycles. The actual inductor current is not compared to the output of the voltage error amplifier but an additional linear slope signal is subtracted. If the linear slope signal has the same amplitude as the down slope of the inductor current then the inductor current error is corrected within one switching cycle. Because the downward slope of the inductor varies with the output voltage and the inductance this can only be achieved within narrow parameters. Nonlinear slope compensation can ensure this for a wider output voltage and inductance range [SS07].

A disadvantage of CMC is the high noise sensitivity. To reduce losses the current sensing resistor R_{Sense} is usually very small which makes the sensed voltage very small too. This small voltage can be influenced by the switching of the transistor which then triggers a false off signal for the transistor. Therefore many designs have implemented a minimum on-time where the current is not evaluated since it may be disturbed by the switching transistor.

Figure 3.26 shows the principal schematic of a buck converter using current mode control. The inductor current is measured through the resistor R_{Sense} and amplified with the current sense amplifier. The output voltage is measured the same way as with voltage mode control. The output signal of the voltage error amplifier is then compared to the output signal of the current sense amplifier. This generates an off-signal for the switch when the maximum inductor current is reached for a certain output voltage [Tex99, She07].

Both control principles, CMC and VMC are used in state-of-the-art converters. The actual application as well as the actual control details determine the best choice.

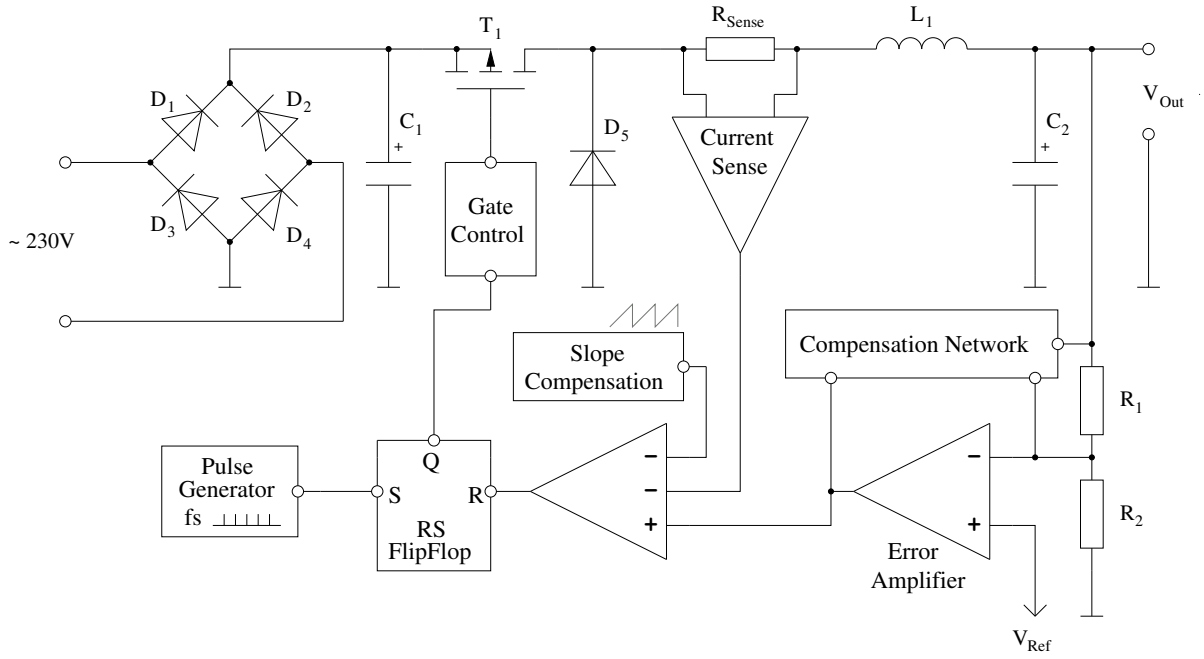

Figure 3.26: Principal schematic of a buck converter with current mode control. The output voltage is the parameter for the outer regulation loop while the inductor current is used as input for an inner regulation loop which makes this regulation faster than VMC.

4 Design space evaluation for smart appliances

This section investigates the design space of the different standby power supply topologies for smart appliances in great detail. First the capacitive supply is analyzed in order to find the optimum operation point. A two stage capacitive supply concept is introduced based on the findings of this analysis.

Then the design space of a conventional buck converter for the desired application field is outlined based on a simple model that was created for this purpose. Based on the results the dimensioning of the converter as well as its operation mode can be optimized. The findings in this section are the foundation for further topology enhancements leading to the new topology design in the next section.

4.1 Design space and loss analysis for the capacitive supply

This section analyzes the capacitive power supply in greater detail and investigates its usability in the area of wireless sensor nodes and standby power supplies for smart appliances. These nodes usually operate at a power level of about 100 mW or below for an output voltage level of a few volts [KKWK10].

First the total losses and the contribution of each component are discussed, then the efficiency for various operation scenarios is analyzed. This will then lead to a new multi stage concept which will be introduced and discussed.

Although for this analysis an effective mains voltage of 230 V at a frequency of 50 Hz was assumed, the principal effects are similar for other mains configurations. The figures within this section emerge from basic specially built models of the discussed capacitive supply topologies, which were created to allow various parameter sweeps in order to facilitate an extensive analysis.

Before efficiency estimations can be addressed, the component losses and their contribution to the total losses have to be found. This individual losses are depending on a lot of additional parameters like the design topology, output voltage or output power. This analysis is based on the dimensioning rules from the previous chapter, the single rectifier capacitive supply of figure 3.1 and the full bridge rectifier version of figure 3.2.

The investigated supplies are dimensioned for a constant load and the output capacitor is big enough to prevent losses in the Zener diode. From the remaining components the primary sources of losses are the inrush current limiting resistor R_1, the discharging resistor R_2 and the rectifiers. The rectifiers in the single rectifier version are D_1 and the forward path of D_5, the rectifiers of the full bridge version are D_1 - D_4.

4.1.1 Losses in the current limiting resistor R_1

R_1 has been dimensioned following the selection chart in figure 3.10 to a typical maximum inrush current of 10 A which gives a resistance value of about 68 Ω. Figure 4.1 illustrates the power losses in R_1 with respect to the output power of the capacitive power supply for the full bridge rectifier topology (left) and the single rectifier topology (right).

The input and output current follow from the given output power and output voltage. As is clearly evident when observing figure 4.1, the losses in R_1 are twice as high in the single rectifier topology for the same output voltage and the same output power. This is because the input current in the single rectifier topology is twice the current of the full bridge rectifier version because only one half wave can be used. When staying in the same topology and comparing the losses for a given output voltage depending on the output power for the same output voltage, the losses in R_1 increase quadratic with the output power. This relation results due to :

$$P_{out} = I_{out} \cdot U_{out}, \qquad I_{R1} = I_{in} \approx I_{out} \cdot 1.11, \qquad P_{R1} = I_{R1}^2 \cdot R_1 \tag{27}$$

This indicates that when considering only the losses in R_1, the supply is significantly more efficient at lower output power and that the full bridge rectifier topology is more efficient than the single rectifier version. Another observation can be made from figure 4.1. The losses in R_1 are much higher for a lower output voltage when compared at the same output power. Figure 4.2 shows the correlation between the output voltage and the loses in R_1 for an output power of 100 mW. The losses in R_1 decrease quadratically with increasing output voltage compared at the same output power.

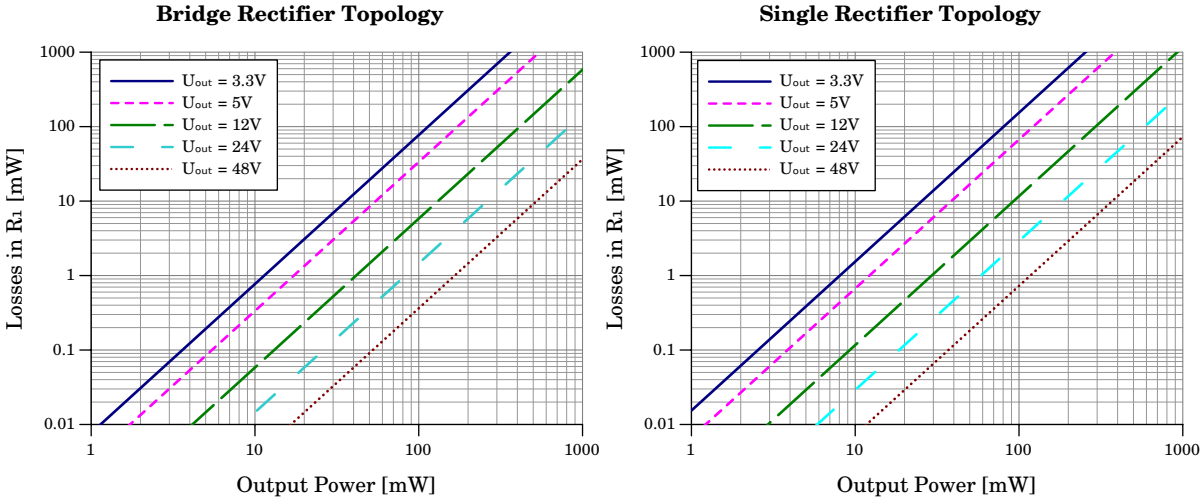

Figure 4.1: Power losses in R_1 depending on the output power for the bridge rectifier topology (left) and the single rectifier topology (right). Losses in R_1 are smaller for lower output power levels and higher output voltage levels for both topologies. Losses in R_1 of the single rectifier topology are twice the losses in R_1 of the full bridge topology.

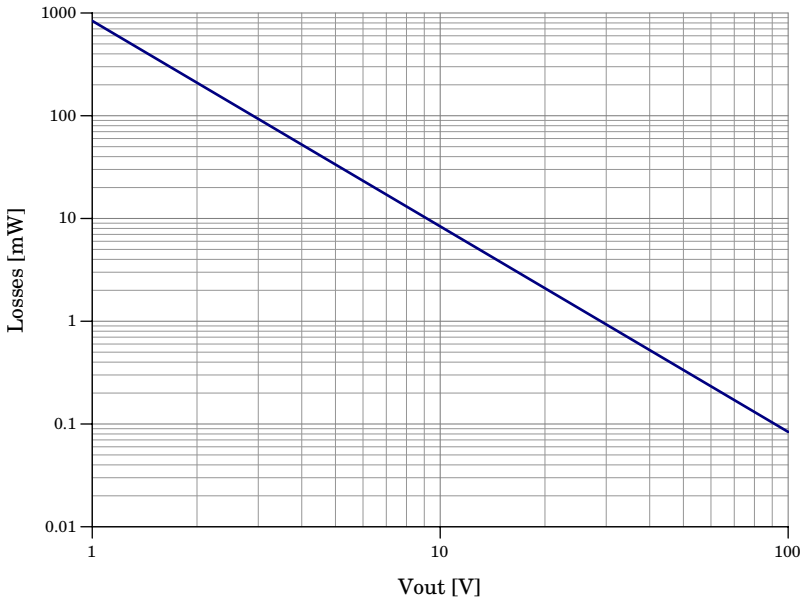

Figure 4.2: Losses in R_1 depending on the output voltage of the supply at a fixed output power of 100 mW. The losses in R_1 decrease quadratically with a rising output voltage level for the same output power.

4.1.2 Losses in the discharge resistor R_2

The discharge resistor R_2 has to be dimensioned to reach a given discharge time of the current limiting capacitor C_1 as described in equation 12. Therefore the resistance of the discharge resistor is inversely proportional to the capacitance of the current limiting capacitor C_1 which on his turn is depending on the supply current. Hence the losses in the discharge resistor R_2 are again depending on the output voltage and the output power of the supply as figure 4.3 shows.

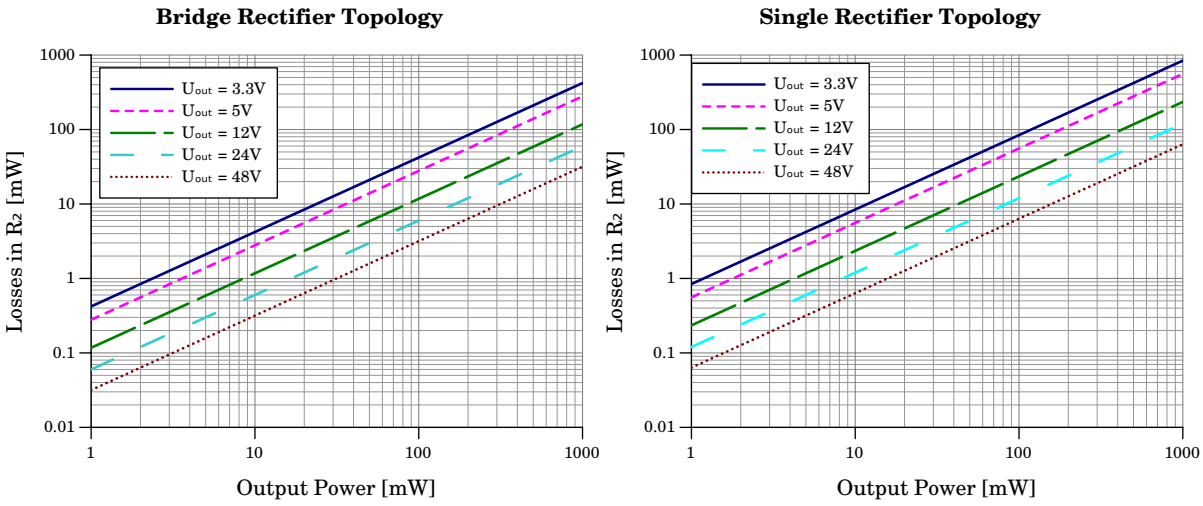

Figure 4.3: Power losses in R_2 depending on the output power for the bridge rectifier topology (left) and the single rectifier topology (right). Losses in R_2 are lower for higher output voltage levels and lower output power levels. The dependency is not as high as for R_1.

When investigating the losses in R_2 in greater detail, it is apparent that the output voltage of the supply not only affects the supply current and therefore the capacitance of C_1 but also affects the effective voltage on R_2 which is also noticeable in the capacitor selection process for extremely high output voltage levels as equation 5 shows. However, this supplementary dependency from the output voltage is much lesser then the main dependency deducing from the output power. The power losses in R_2 can be estimated through the voltage on R_2 and would then for a single rectifier topology calculate to:

$$P_{R_2} = \frac{U_{R_2}^2}{R_2} \tag{28}$$

$$U_{R_2} \approx \sqrt{\left(\frac{\hat{U}_{mains} - \frac{U_{out}}{2}}{\sqrt{2}}\right)^2 + \left(\frac{U_{out}}{2}\right)^2} \tag{29}$$

$$P_{R_2} \approx \frac{\frac{U_{out}^2}{4} + \left(\frac{\hat{U}_{mains} - \frac{U_{out}}{2}}{\sqrt{2}}\right)^2}{R_2} \tag{30}$$

The approximation of U_{R2} is achieved through the superposition of a reduced and displaced mains voltage. Unfortunately the real voltage at R_2 deviates from an ideal sine wave which introduces an error. A better approximation of U_{R2} that has been extrapolated from simulations can be achieved through:

$$U_{R_2} \approx \left(\frac{\hat{U}_{mains} - \frac{U_{out}}{2}}{\sqrt{2}}\right) + \left(\frac{U_{out}}{4}\right) \tag{31}$$

A simpler way to estimate the power losses in R_2 is to neglect the output voltage and calculate only with the effective mains voltage and the value of R_2 which provides usually sufficient accuracy especially for low output voltage levels.

When comparing figure 4.3 with figure 4.1 it is clearly evident that the dependency of the losses from the output power is quadratic for R_1 and linear for R_2which means that :

$$\frac{dP_{R_1}}{dP_{out}} > \frac{dP_{R_2}}{dP_{out}} \tag{32}$$

However, in the range of 100mW which is typical for wireless sensor and control nodes, the contribution to the total losses is much higher for R_1 for low output voltage levels. The losses in R_2 in the single rectifier topology are twice the losses in R_2 in the full bridge rectifier topology. Hence the influence of the topology on the losses in R_2 is identically to it's influence on the losses in R_1. When looking at the influence of the output voltage to the losses in R_2, then the losses in R_2 are linearly dependent on the output voltage.

4.1.3 Losses in the rectifiers

When looking at the losses of the rectifiers, one may think that there are big differences between the single rectifier topology and the full bridge rectifier topology. Looking at the single rectifier variant in figure 3.2 in comparison to the full bridge rectifier variant in figure 3.1 shows that the current, which is two times the current of the full bridge rectifier variant, has to flow trough only one diode, D_1. But additionally the forward path of the Zener diode D_5 is used to have a current return path to the capacitor C_1 during the other half wave. Therefore two diode paths are used in the single rectifier variant that produce losses, one for each half wave, each of them handling twice the current of the full bridge variant. When looking at the full bridge rectifier variant, there are two diode paths each of them consisting of two diodes, which swap for each half wave. When multiplying the amount of diodes in each path for each half wave with the current that flows through them, the results are exactly the same for the single rectifier variant and the full bridge rectifier topology. Figure 4.4 shows that the losses in the rectifiers for both topologies go linear with output power and output voltage.

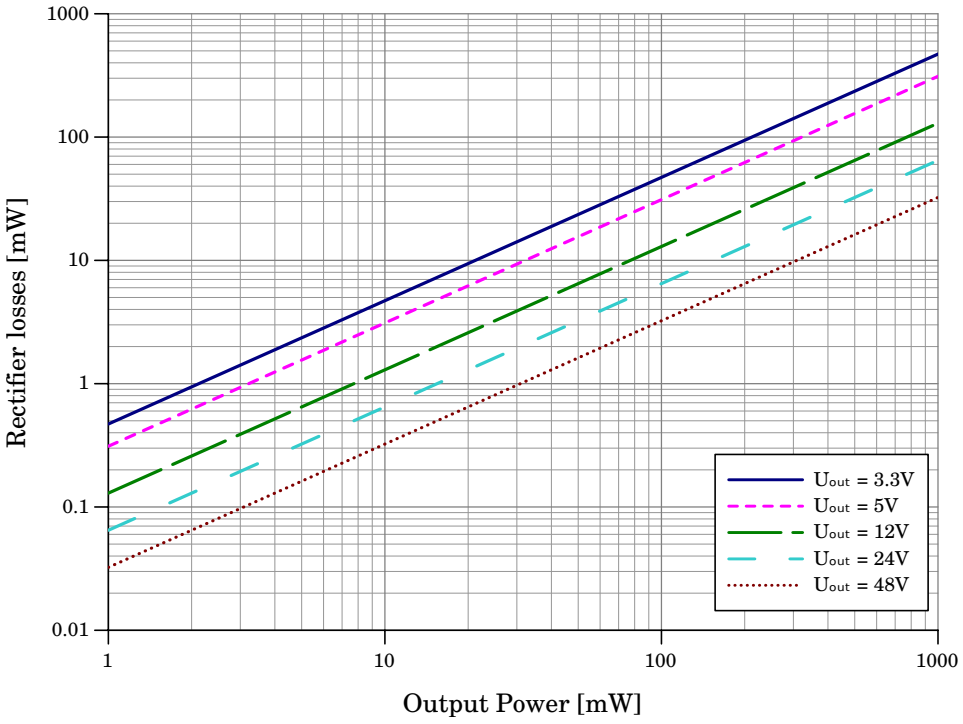

Figure 4.4: Power losses in the rectifier elements for both topologies (single rectifier and full bridge rectifier). The losses are higher for lower output voltage levels and higher output power levels.

4.1.4 Total losses and efficiency

After evaluating the losses of each individual relevant component the combined losses of the circuit are analyzed. Figure 4.5 shows the total losses of a capacitive supply circuit for the bridge rectifier variant (left) and the single rectifier variant (right).

Although the curve shapes are similar, the losses of the single rectifier topology are slightly fewer than twice the losses of the full bridge rectifier topology. This is because the losses of the single rectifier topology in R_1 and R_2 are twice the losses of the bridge topology but the losses in the rectifier itself are identical.

Another characteristic of figure 4.5 is the higher growth of the total losses for higher output powers of over 100 mW, which bends the curves for all voltages and both topologies slightly upwards. An explanation for this gives equation 32 in combination with figure 4.6. Figure 4.6 shows the contribution of each element to the total losses at 100 mW output power depending on the output voltage.

Because the losses in R_1 depend quadratically on the output power they have a greater influence on the total losses from a certain output power on. This happens at over 100 mW in the used dimensioning where $R_1 = 68\Omega$. Hence the growth of the losses is higher from that point on. Apparently the losses in R_1 are way below the losses in the other components for lower output power levels because the current is lower for a lower output power level. At lower output voltage levels the contribution of the losses in R_1 to the total losses is significant higher, because the current has to be significant higher. An increase of the output voltage reduces the current for the same output power and therefore reduces the losses in R_1 and the contribution of the losses in R_1 to the total losses. Hence the knees in the total losses in figure 4.5 can be shifted to a higher output power level by increasing the output voltage. When designing a capacitive power supply, it therefore is preferable to keep with the output power below the described knee.

Figure 4.7 shows the total efficiency for the capacitive power supply for both topologies and different output voltage levels. Figure 4.7 makes it obvious that the capacitive supply has better efficiency for higher output voltage levels whereas the efficiency drops rapidly after a certain output power level. Also the base efficiency is poor and the efficiency drop starts early for a low output voltage.

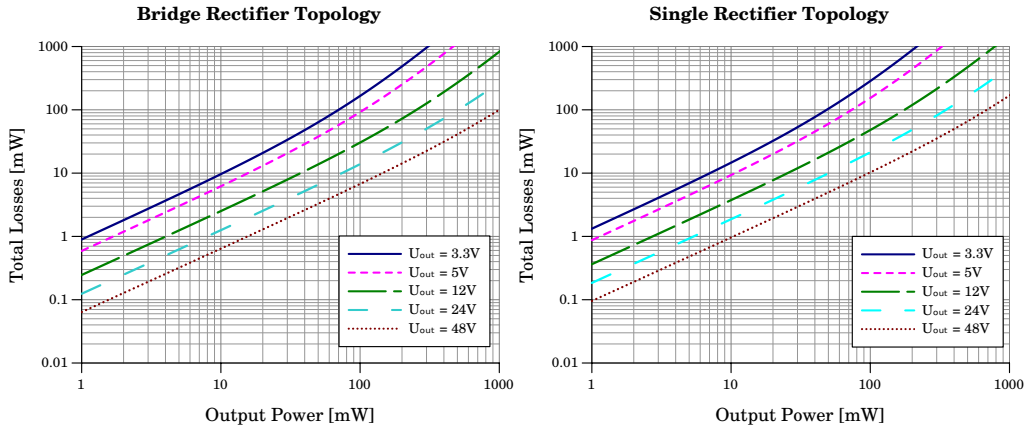

Figure 4.5: Total losses of the capacitive supply with bridge rectifier topology (left) and single rectifier topology (right).

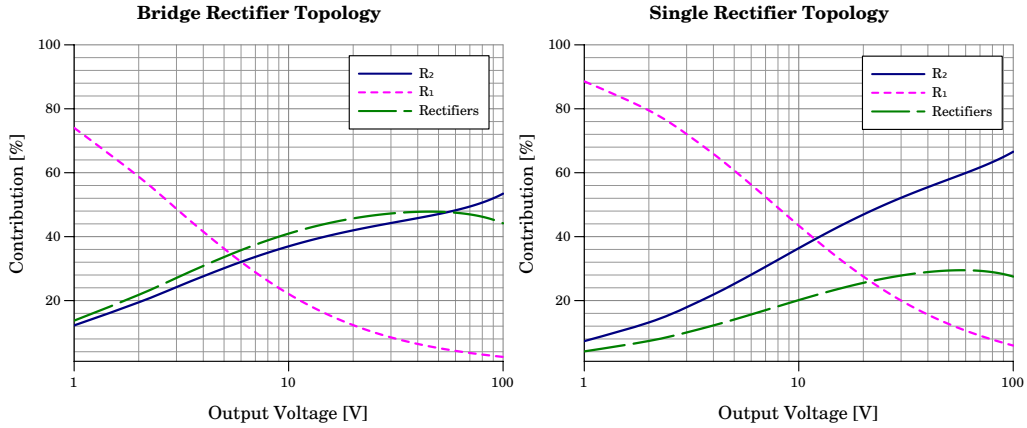

Figure 4.6: Contribution of each component to the total losses for the bridge rectifier topology (left) and the single rectifier topology (right) for an output power of 100 mW. The contribution of R_1 to the total losses dominates the total losses for low output voltage levels.

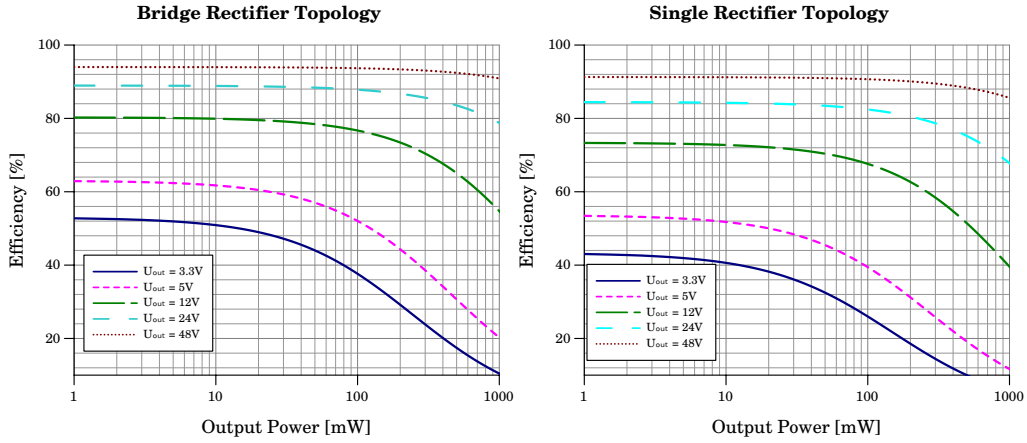

Figure 4.7: Total efficiency of the capacitive power supply for the bridge rectifier topology (left) and the single rectifier topology (right) for different output voltage levels depending on the output power.

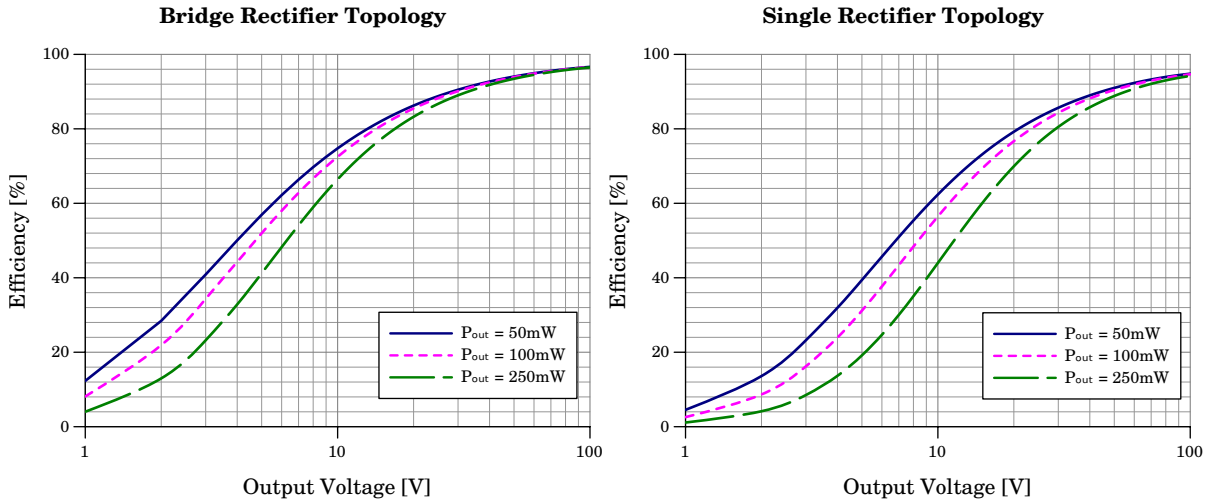

Figure 4.8: Total efficiency versus output voltage for the different output power levels 50 mW, 100 mW and 250 mW for the bridge rectifier topology (left) and the single rectifier topology (right).

Figure 4.8 shows the total efficiency depending on the output voltage for different output power levels. Whereas for low output voltage levels the efficiency is depending on the output power, this effect shrinks for higher output voltage levels. The difference between the full bridge rectifier topology and the single rectifier variant is not very distinct for this comparison.

After comparing different output power levels, figure 4.9 shows the direct comparison between the bridge rectifier variant and the single rectifier variant in terms of efficiency at an output power level of 100 mW. As expected, the efficiency for both topologies is low for low output voltage levels. The difference between the topologies has its maximum at about 6 V which gives just under 40 % efficiency for the single rectifier variant and just under 60 % for the full bridge rectifier topology. At an output voltage over 30 V the efficiency difference is only about 5 % and decreasing which is the result of the lower output current. At an output voltage of 30 V the efficiency reaches about 90 %.

4.1.5 Reactive input power

An important parameter when evaluating the supply for the application area of wireless sensor and control nodes is the reactive input current. It's important because in a larger network the reactive input power can sum up to a substantial amount which will stress the supply net. Figure 4.10 shows the dependency of the reactive input power from the output power for various output voltage levels. When studying figure 4.10 it becomes obvious that this concept draws a serious amount of reactive current under any operating condition, which may disqualify this concept for high output power levels, especially for low output voltage levels. This is the main disadvantage besides the big X2-type capacitor. Anyway, this effect can be minimized by choosing a higher output voltage and going with lower output power levels when possible. This would be the best strategy to increase total efficiency too.

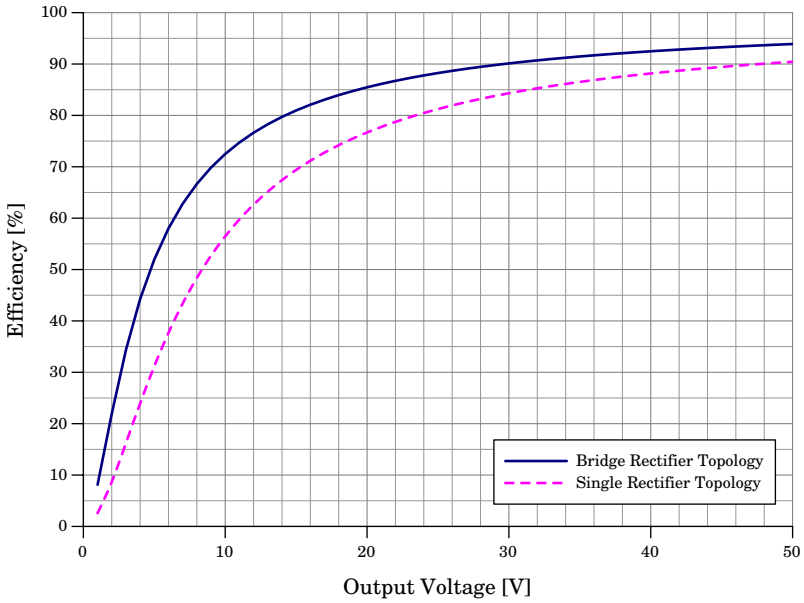

Figure 4.9: Efficiency comparison of the bridge rectifier topology and the single rectifier topology depending on the output voltage for an output power of 100 mW.

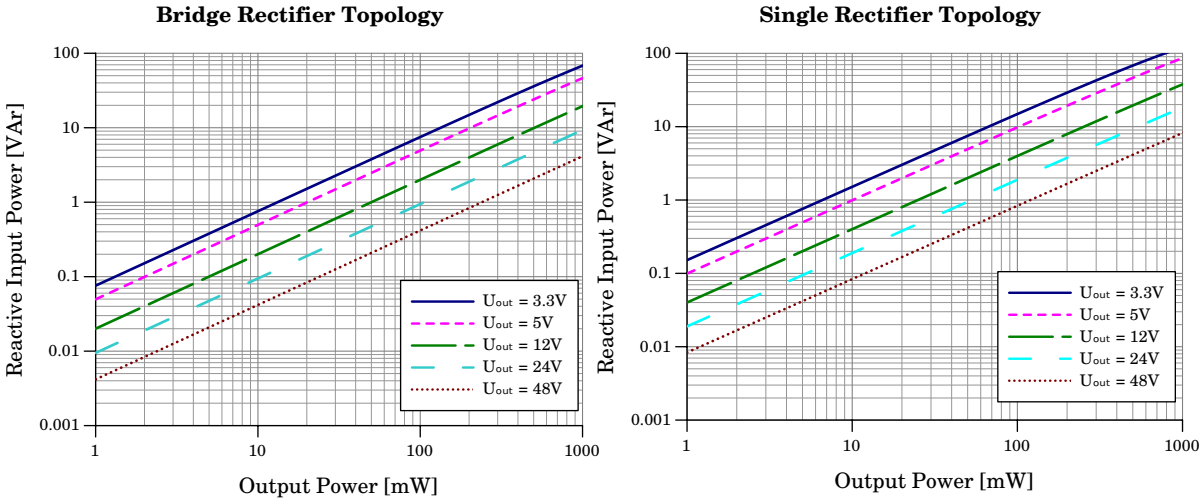

Figure 4.10: Reactive input power depending on the output power for various output voltage levels.

4.1.6 Two stage concept

The typical power requirements of wireless sensor and control nodes are at about 100 mW for a supply voltage of 3.3 to 5 V. As analyzed in the last chapter, the simple capacitive power supply has a lot of disadvantages in this operating area which apply for booth supply topologies. The high current which is needed for the low output voltage to meet the output power produces a massive amount of reactive input power which is stressing the supply lines especially when many nodes are used as part of a larger network. Also the losses for lower output voltage levels are relatively high which decreases efficiency of the supply. Also the used capacitors C_1 and C_2 have to be bigger as explained earlier. This makes the use of the simple capacitive supply uneconomic if not impossible. A solution to this problem may be the utilization of a two stage supply concept. The first stage is a capacitive supply stage, preferably the full bridge rectifier topology, which generates a relatively high auxiliary voltage. The higher the auxiliary voltage, the better for the characteristics of the first stage. The second stage is a high efficient SMPS DC-DC converter that converts the auxiliary voltage into the target voltage. Figure 4.11 shows a simplified schematic of this concept.

The characteristics of the secondary SMPS will determine the level of the auxiliary voltage. A typical high voltage and low power SMPS that can be used in this application area is the LTC3642 from Linear Technology [Lin08]. This SMPS can operate up to 45 V input voltage for an output current of 50 mA and is available at an output voltage of 3.3 V or 5 V. This makes this SMPS suitable for output power levels up to 165 mW for 3.3 V. Unfortunately but expectable this SMPS has lower efficiency for higher input voltage levels as figure 4.12 shows. Additionally the efficiency is depending on the output power level. Due to the static losses of the power converter IC the efficiency is low for low output power levels. To estimate the total efficiency the second stage has to be considered accordingly.

Figure 4.13 shows the efficiency of the combined capacitive power supply in comparison with single stage capacitive supply at an output voltage of 5 V. The first stage is a standard capacitive supply which is delivering the auxiliary voltage V_{aux}.

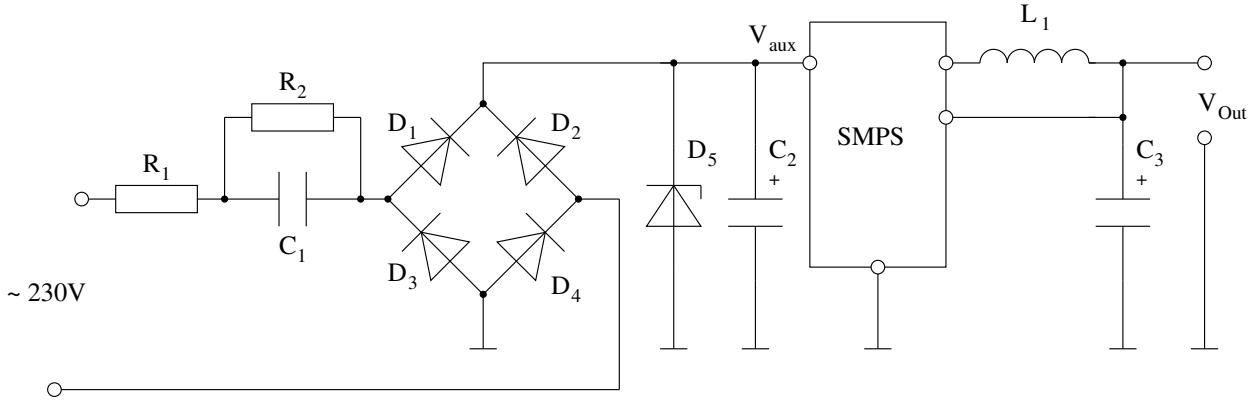

Figure 4.11: Two stage capacitive supply concept utilizing an SMPS as second stage.

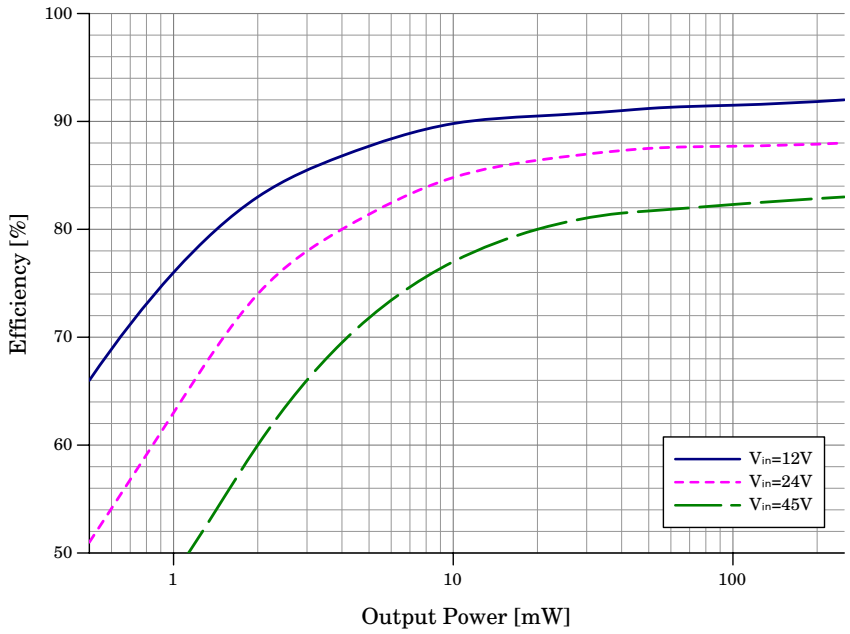

Figure 4.12: LTC3642 - Efficiency depending on the output power for different input voltage levels at 5 V output voltage.

The second stage utilizes the LTC3642 SMPS controller to convert the auxiliary voltage into the target voltage of 5 V. A lower auxiliary voltage is better for the efficiency of the secondary SMPS which can bee seen in the low output power region of figure 4.13. For a higher output power level the efficiency loss in the first stage compensates the efficiency gain in the second stage and the total efficiency drops for lower auxiliary voltage levels. This can be clearly seen at an auxiliary voltage of 12 V, but this trend is also noticeable for an auxiliary voltage of 24 V in the concrete example in figure 4.13.

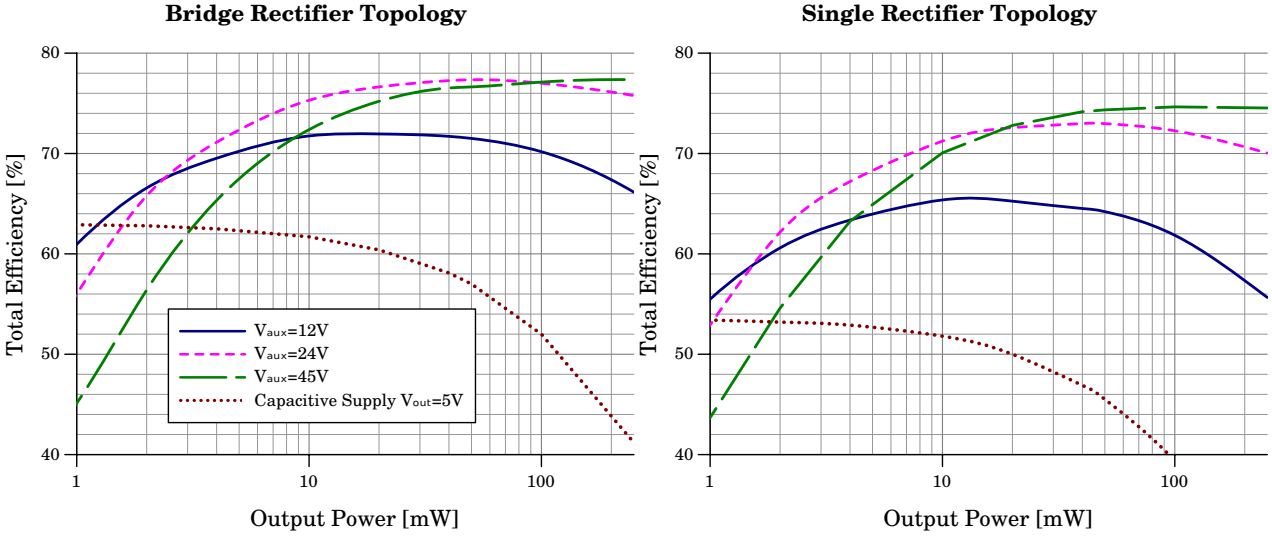

Figure 4.13: Total efficiency of the combined two stage capacitive supply depending on the output power for different auxiliary voltage levels compared to a single stage capacitive supply with 5 V output voltage.

Also this trend is amplified when the single rectifier topology is used because the losses of the primary stage are higher especially for higher output power levels. In terms of efficiency the combined solution has little difference between an auxiliary voltage of 24 or 45 V. But the reactive input current for the higher auxiliary voltage is still an important factor when designing a power supply for wireless sensor and control nodes which makes the usage of the higher auxiliary voltage desirable when it brings no other disadvantages. When comparing the efficiency of the two stage supply concept to the single stage capacitive supply with an output voltage of 5 V the two stage variant is clearly superior as can be seen in figure 4.13.

4.2 Causes of losses in SMPS-based topologies

To understand the basic deliberations in the next chapter and the motivation to create a new topology the basic losses occurring in an SMPS have to be analyzed. Generally the losses can be categorized into conduction losses and switching losses. Conduction losses are caused through the current during the conduction period of an element and vary with the square of that current. Switching losses on the other hand are caused through the charge of parasitic capacitances and therefore vary with the switching frequency and the involved voltages. They are usually harder to estimate as various effects play a role in switching losses. Additionally the parasitic capacitances are strong nonlinear depending on the used voltage. The converter control algorithms determine the actual voltage and current levels on a given converter topology. Hence the losses not only depend on the actual application field and the converter topology but also on the converter control algorithms.

This section gives an overview of the main losses that can occur in a converter. The MOSFET as the switching element is subject to conduction losses during the on-time and switching losses during the on-off and off-on transitions. The leakage losses during the off-time of the MOSFET are neglected as they are an order of magnitude smaller in the researched application field. The rectifier is also subject to conduction and switching losses. Its conduction losses are dependent on the forward voltage of the rectifier. In case a synchronous rectifier is used it is depending on the on-state resistance of the MOSFET and the used dead time in combination with the forward voltage of the body diode of that transistor. The switching losses of the rectifier are caused by its reverse recovery charge. The output capacitor is also subject to losses that are mainly dependent on its current ripple in combination with its ESR. The leakage current is usually neglectable. The inductor also suffers from conduction and switching losses, mainly due to the conductor material and the core material. Additional losses can occur due to the construction and the layout of the converter. Furthermore the control logic will need some energy to ensure converter operation. These losses are highly dependent on the actual converter implementation.

4.2.1 MOSFET conduction losses

MOSFET conduction losses occur as the name suggests in the on-phase of the MOSFET. During the on-phase the current flow is dependent on the drain source on-resistance $R_{DSon}$of the transistor. R_{DSon} can be seen as an equivalent resistance of the transistor in on-state. The conduction losses in the transistor $P_{loss(MC)}$ therefore are dependent on the drain current $i_D(t)$ which is variable over time and calculate to:

$$p_{loss(MC)}(t) = i_D^2(t) \cdot R_{DSon} \tag{33}$$

The actual average losses then calculate to:

$$P_{LOSS(MC)} = \frac{1}{T} \int_0^T (i_D^2(t) \cdot R_{DSon}) dt = R_{DSon} \cdot I_{D(rms)}^2 \tag{34}$$

Hence the conduction losses of the MOSFET grow quadratic with the RMS value of the drain current I_D. Therefore conduction losses are also referred to as I^2R losses. To decrease the I^2R losses, either the R_{DSon} value, or the drain current $I_{D(rms)}$ has to be decreased. A lower R_{DSon} value requires a transistor of higher chip size which on the other hand has higher parasitic capacitance values which increases the switching losses. A lower $I_{D(rms)}$ value can sometimes also be achieved by a higher switching frequency which will reduce the current ripple. Unfortunately this also leads to higher switching losses so that conduction and switching losses in a MOSFET are always a tradeoff.

The used inductance also influences the MOSFET conduction losses as a bigger inductance value leads to a smaller current ripple and therefore to a smaller RMS current value. Additionally the current ripple and therefore the conduction losses are influenced by the converter operation mode (CCM, CRM, DCM). CCM offers the fewest conduction losses as the RMS value of the current is lowest in this mode. The input to output voltage ratio influences the duty cycle which influences the operation mode of the converter in combination with the inductance value. Hence the input to output voltage ratio also influences the conduction losses.

4.2.2 MOSFET switching losses

The switching losses of a MOSFET are caused through different effects. To better understand these effects the equivalent circuit of a MOSFET has to be considered. Figure 4.14 shows a simplified form of an equivalent MOSFET circuit. The main reason for MOSFET switching losses are the parasitic capacitances C_{GS}, C_{GD} and C_{DS}.

MOSFET parasitic capacitances There are three important intrinsic capacitances which are the gate-source capacitance C_{GS}, the gate-drain capacitance C_{GD} and the drain source capacitance C_{DS}. The actual values of these capacitances are strongly dependent on the structure of the MOSFET as well as the voltage across them and are highly nonlinear.

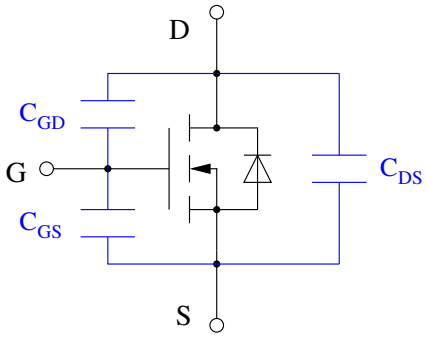

Figure 4.14: Simplified equivalent circuit of an N-channel MOSFET. C_{GS} represents the gate source capacitance, C_{GD} represents the gate drain capacitance and C_{DS} represents the drain source capacitance.

When working with the parasitic capacitances of a MOSFET another categorization is often used because its parameters are easier to measure. The input capacitance C_{iss} is the capacitance between the gate and the source of the transistor while drain is connected to source. The output capacitance C_{oss} is the capacitance between drain and source of the transistor while the gate is connected to source. The reverse transfer capacitance C_{rss} is the capacitance between gate and drain while source is connected to ground. This three parameters are usually found in MOSFET datasheets and are highly dependent on the voltage. This leads to the following equations :

$$C_{iss} = C_{GS} + C_{GD} \tag{35}$$

$$C_{oss} = C_{DS} + C_{GD} \tag{36}$$

$$C_{rss} = C_{GD} \tag{37}$$

Gate charge When looking at the input capacitance another model is often used to describe the switching behavior of the MOSFET. Because the gate-drain capacitance is highly voltage dependent the gate charge is used to design the driver circuit because it takes voltage into account. Figure 4.15 shows the gate voltage V_G and the drain current I_D while an N-channel MOSFET switches on a resistive load. At the time of 0 ns the gate driver tries to switch on the transistor. First the gate voltage rises till it reaches the miller plateau voltage, which is at a time of 25 ns in figure 4.15. During that time the gate-source charge Q_{GS} is charged. After that the gate voltage stays at the miller plateau voltage while the miller charge which is also called gate-drain charge Q_{GD} is charged. During this time the drain current starts to rise till it reaches its designated maximum. Simultaneously the drain-source voltage decreases until it reaches the on-state value. The total gate charge Q_G is the charge that is necessary till the gate voltage reaches the value which is defined through the gate driver.

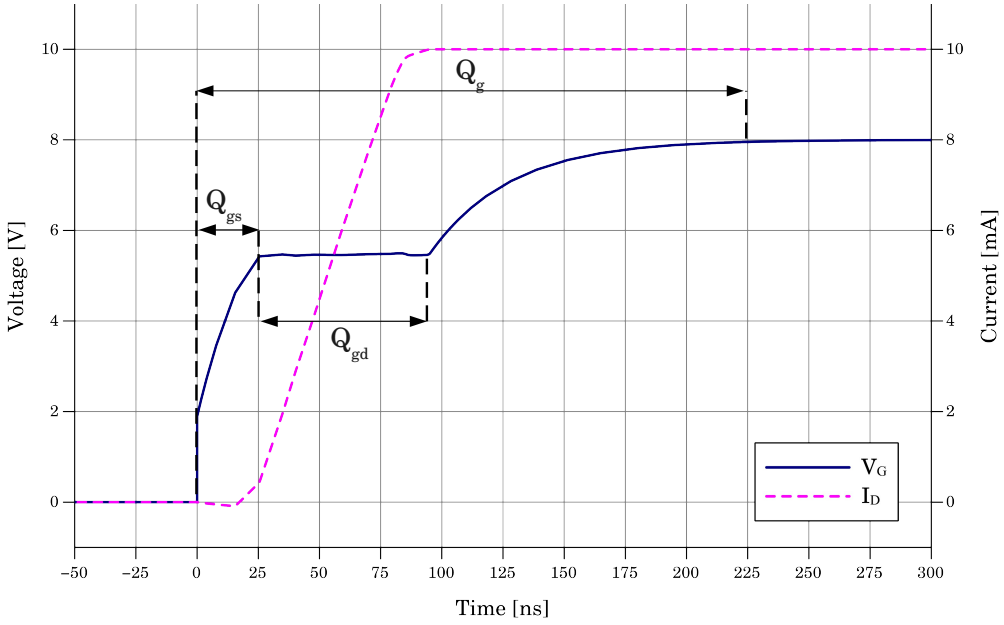

Figure 4.15: Charging the gate of an N-channel MOSFET. First the gate source charge is charged. After the gate voltage reached the plateau voltage the gate drain charge is charged. During that time the actual switching of the device occurs.

Gate charge losses The actual switching losses are a combination of three different effects. The first effect is the loss originating from charging and discharging the gate itself which has to be done every switching cycle. When calculating the gate charge losses the total gate charge Q_G is the relevant parameter. The losses due to the gate charge calculate to:

$$P_{loss(MSgate)} = Q_G \cdot V_G \cdot f_s \tag{38}$$

V_G is the output voltage of the gate driver and therefore the gate voltage when the transistor is switched on, and f_s is the switching frequency. Note that half of the energy is lost during the switch-on phase through the combination of the parasitic gate resistor, an optional external gate resistor and the gate driver output impedance. The other half is stored as gate charge Q_G and dissipated during the switch-off phase. Through resonant gate driving circuits the gate charge can be recovered and these losses can be diminished substantially [Fuj10]. Unfortunately an additional inductor is necessary to achieve this. To decrease the gate charge losses the gate voltage has to be low. Unfortunately the gate voltage influences the switching times that are another origin of switching losses.

MOSFET dV/dt rating One parameter that is determined by the parasitic capacitances is the maximum dV/dt rating of the transistor. This means that the slope of the drain voltage has to be limited in order prevent an unintentional turn-on of the device. The gate-source voltage V_{GS} is controlling the state of the transistor.

Simplified can be said that whenever it rises over the threshold voltage V_{th} the transistor is turned on. During normal operation the gate of the transistor is controlled through the gate driver of a preceding circuit. The maximum current that can be utilized to control the gate is determined by this gate driver and the used gate resistor. C_{GD} and C_{GS} act as a capacitive voltage divider. If a sudden change of the drain voltage occurs, the gate-source voltage goes along depending on the ratio of C_{GD} and C_{GS} before it is compensated through the gate driver. If the gate-source voltage rises over the threshold voltage, the transistor will turn on unintentionally. Even when the gate is connected to source there is a maximum dV/dt rating for the drain voltage because of the internal parasitic gate resistor.

Transition losses During the switching transition the drain current I_D and the drain source voltage V_{DS} of the transistor are both greater than zero during the same time. This is another origin of switching losses in MOSFETs. The voltage and current waveforms during switching are dependent on the actual application and in particular the switched load. Figure 4.16 shows the voltage and current waveforms V_G, V_{DS} and I_D during the switch-on of a MOSFET. The left side of figure 4.16 shows the waveforms for a resistive load and the right side shows the waveforms of a diode clamped inductive load.

The switch-off event has similar waveforms and therefore similar losses. Figure 4.17 shows the voltage and current waveforms V_G, V_{DS} and I_D during the switch-off phase of a MOSFET. The actual switch-on and switch-off time can be different and therefore cause different losses during switch-on and switch-off. This depends on the difference of the miller plateau voltage and the actual gate driver voltage that will define the gate current and therefore the switching times. If equal switching times are intended then the gate current for both switching events have to be equal which leads to the conclusion that the gate driver voltage has to be twice the miller plateau voltage.

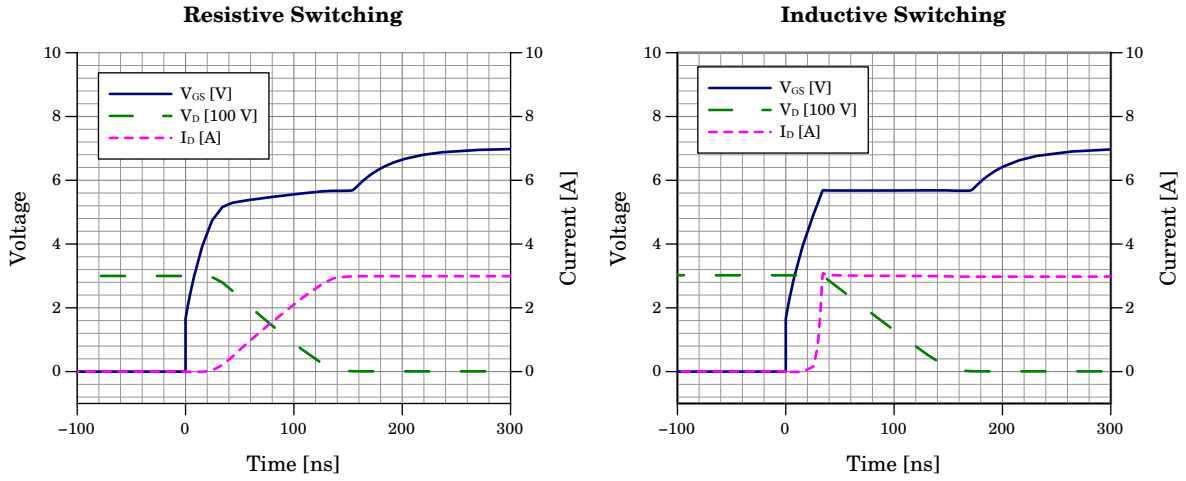

Figure 4.16: Switching waveforms during the switch-on of a resistive load (left) and a diode clamped inductive load (right) of a MOSFET.

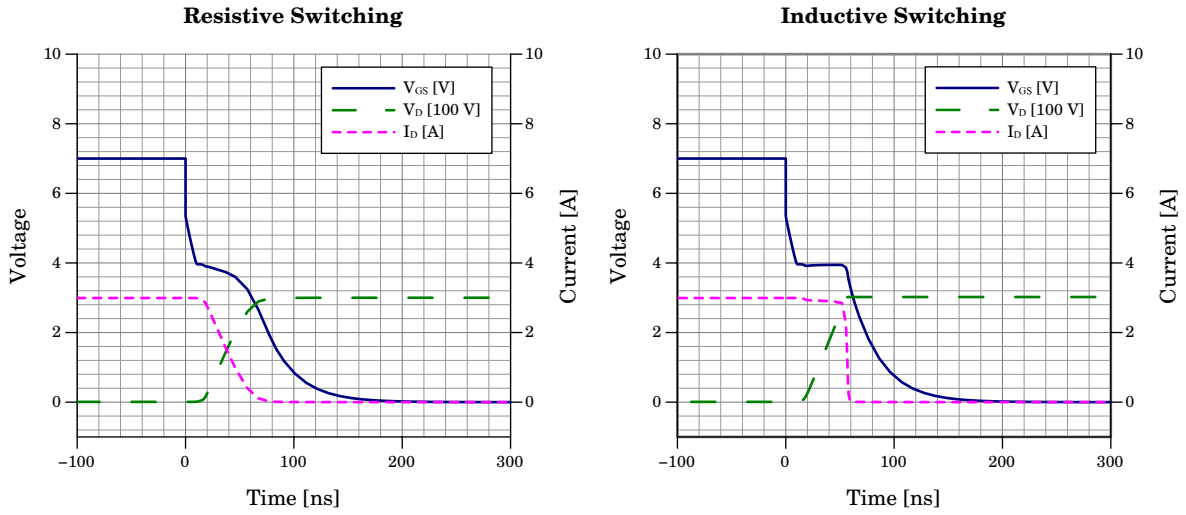

Figure 4.17: Switching waveforms during the switch-off of a resistive load (left) and a diode clamped inductive load (right) of a MOSFET.

The transition losses that are caused through a single switching then calculate to :

$$P_{loss(MStran)} = \frac{1}{T}\int_{t_1}^{t_2}(i_D(t)\cdot u_{DS}(t))dt \tag{39}$$

The switching event is defined by its starting time t_1 where the gate driver switches and its end time t_2 where the gate voltage reaches its designated value while T is the switching time. This time can be different for switch-on and switch-off events. The most crucial part when calculating the switching losses is the estimation of the turn-on time and the turn-off time. A first start is the gate-source-charge Q_{GS} and the miller charge Q_G with a linear approximation of U_{DS} and I_D. A more realistic approach would be the charge from when the gate voltage reaches the threshold voltage to when the drain-source voltage reaches a defined voltage level near its end value [XSJ+09]. This is due to the nonlinearity of U_{DS} over the switching cycle which often leads to an overestimation of the switching losses. Unfortunately this charge is usually not available from MOSFET datasheets. A reasonable good estimation of the switching times can be given by the utilization of Q_{GS} and Q_{GD} in combination with the gate current I_G ($Q = I \cdot t$) which is defined by the gate driver and the external gate resistor.

When the load is inductive which is typical for an SMPS converter then a simplification can be used as the current commutes almost immediately from the rectifier device to the switching transistor. When the switching times t_{on} and t_{off} are known then an estimation for the switching losses for an inductive load calculates to:

$$P_{loss(MStrans)} = \frac{I_D \cdot U_{DS}}{2}\cdot(t_{on}+t_{off})\cdot f_s \tag{40}$$

When t_{on} and t_{off} are equal (t_{on} = t_{off} = t_{switch}) then the transition losses calculate to:

$$P_{loss(MStrans)} = I_D \cdot U_{DS} \cdot t_{switch} \cdot f_s \tag{41}$$

Till now only the losses through the MOSFET itself have been considered for the switching losses. In a real converter application the reverse recovery current of the rectifier causes additional losses in the MOSFET. This has to be considered when estimating a power budget for the MOSFET but will be discussed later with the rectifier switching losses. Note that this effect occurs for simple rectifiers as well as for synchronous rectifiers.

[XSJ+09] states that the output capacitance C_{OSS} of the MOSFET does not have an additional influence on the switching losses as its influence is included in the losses caused by the voltage and current turnover. The losses during the switch-on are therefore overestimated while the losses during the switch-off are equally underestimated.

4.2.3 Rectifier conduction losses

The rectifier in a converter also causes conduction and switching losses. If a diode is used as rectifier, the conduction losses are determined by the forward voltage V_f of that diode and the average current I_D through it. The losses then calculate to $I_D \cdot V_f$. The actual diode current is dependent on the architecture of the converter and the duty cycle. When using a simple buck converter with a low duty cycle the conduction losses of the rectifier may be significant because it is conducting most of the time and I_D is therefore higher. As the rectifier conduction losses are highly depending on the converter topology and the application area it will be discussed later in the detailed application specific analysis.

The usage of a synchronous rectifier in form of a MOSFET can greatly diminish the rectifier conduction losses when it is controlled correctly. The actual energy savings again depend on the architecture and the application field. When a synchronous rectifier is used a dead time has to be introduced that prevents both devices from being “on” at the same time. This would be the case in a short time window during the switching period of the device and cause a current shoot-through without a dead time. As a result the losses would be high and possibly destroy the switching devices. The dead time switches the rectifier on later and off earlier. During the dead time the body diode of the synchronous rectifier is carrying the current and therefore the forward voltage of the body diode is responsible for the losses. During the on time of the synchronous rectifier the losses are MOSFET conduction losses which are I^2R losses that have been described earlier leading to equation 33 and 34. Depending on the duty cycle and the actual dead time the dead time losses may be neglected in some cases.

4.2.4 Rectifier switching losses

Unfortunately the usage of a synchronous rectifier can’t avoid the switching losses. These losses occur because of the reverse recovery current of the diode or the synchronous rectifier.

When compared to a synchronous rectifier, a Schottky diode has usually a smaller reverse recovery and therefore smaller losses. This is because the body diode of the synchronous rectifier MOSFET is typically slow. Hence Schottky diodes are sometimes switched in parallel to synchronous rectifier transistors. This effect is limited as the connection between the body diode and the Schottky diode suffers from parasitic inductance. Some devices therefore have an integrated Schottky diode in parallel. The easiest way to determine the reverse recovery losses is to use the reverse recovery charge Q_{rr} of the used rectifier. The reverse recovery losses then calculate to :

$$P_{loss(RS)} = Q_{rr} \cdot V_D \cdot f_s \tag{42}$$

In case a synchronous rectifier is used, the reverse recovery charge of the body diode has to be used to calculate the losses. The involved reverse diode voltage V_D is dependent on the architecture. For a buck converter V_D can be assumed V_{IN} while for a boost converter the diode voltage can be assumed V_{OUT}. The actual power dissipation of the reverse recovery charge is divided mainly between the main switching transistor and the synchronous rectifier.

4.2.5 Inductor losses

The inductor losses can be divided into copper losses and core losses. The copper losses can be divided into low frequency copper losses and high frequency copper losses. The low frequency copper losses originate from the DC resistance of the inductor wire and calculate to $I^2_{L(rms)} \cdot R_L$. They are independent of the used converter frequency. The high frequency copper losses originate from eddy currents due to the skin and the proximity effect [KK10]. The skin effect describes the limitation of the maximum skin depth of the current. The proximity effect describes the influence of the current in one winding on the current in a nearby winding of the inductor. Both effects cause an increase of the effective winding resistance which is greater for higher frequencies. Using litz wire may reduce these losses through the increase of the effective surface. Another possibility to reduce these effects through increasing the surface is to use planar inductors.

Because air coils have typically too low inductance values, core inductors with different core materials are used in SMPS converters. These inductor cores are subject to core losses due to the hysteresis of the magnetic field change in the core (B-H loop hysteresis) and due to eddy currents within the core material of the inductor. Because modern core materials have a high resistance, the hysteresis losses typically far dominate the core losses. The hysteresis losses are defined through the area within the B-H hysteresis loop where B is the flux density and H is the magnetic field strength. In modern core materials the relation between B and H is approximately linear when the core is not saturated [EPC13]. Hence the area within the B-H loop depends quadratically with H. Because H is proportional with the inductor current I_L the power losses due to the hysteresis are quadratically dependent on the inductor current.

On the other hand the core has to run through the hysteresis loop once every switching cycle which makes the hysteresis losses linear with the switching frequency. Hence to decrease inductor losses it is more important to decrease the inductor current even if the frequency is increased. This has the additional advantage that the inductor size can be decreased which gives a cost advantage since the inductor nowadays is probably the most expensive part in a converter. On the other hand an increase of the switching frequency will increase the switching losses in the power switch and the rectifier. This leads to a tradeoff between switching frequency and inductor current.

Because magnetic core materials show saturation the core has a maximum flux density B_{sat}. A further increase of the H-field which is proportional to an increase of the inductor current will not further increase the flux density. This is the motivation for the maximum current peak parameter of the inductor in datasheets. If the current is increased over the maximum allowed current and the core saturates the effective inductance is decreased and the current slope therefore increased for the same voltage. This leads to a even faster current increase which can in the end destroy the circuit. When selecting a core material for an inductor there is a tradeoff between B_{sat} and the losses due to eddy currents. A core material with low losses which is therefore usable for higher frequencies has a smaller B_{sat}. Determining the inductor losses is a major issue in designing a converter and is subject to recent research [UKG06, ML11]. Simulations are often used to estimate the actual inductor losses.

4.2.6 Capacitor ESR losses

Power losses in a capacitor can be divided mainly into dielectric leakage losses, dielectric hysteresis losses and connection losses. The total capacitor losses are summarized in an equivalent series resistance (ESR). Depending on the capacitor type the ESR is dominated from the connections and the electrodes or the electrolyte. Usually electrolyte capacitors have a much higher ESR than ceramic capacitors. The ESR of electrolytic capacitors is increasing over time due to aging and for higher frequencies. This can lead to circuit malfunction when the ESR exceeds tolerable limits and the capacitor heats up too much.

The ESR of the capacitor causes losses due to the RMS capacitor current I_C which will heat up the capacitor. The losses will then calculate to $I_C^2 \cdot R_{ESR}$. Hence the losses are also proportional to the ripple of the capacitor voltage. The actual losses are again highly dependent on the architecture and the used parameters. In general a bigger capacitor may reduce the voltage ripple and therefore reduce the losses. Also a higher frequency will reduce the voltage ripple and therefore the losses. Therefore a higher switching frequency may allow smaller capacitor values for the same capacitor losses and the same voltage ripple.

4.3 Design space for SMPS-based standby power supplies for smart appliances

As described earlier, a mains driven power supply for a wireless sensor node has to deliver a relatively low output voltage at a relatively low output power. In this chapter the conventional non-isolated buck topology is analyzed for usability in this application field, as it is a simple and low cost converter topology. The basic structure of this topology which was introduced in section 3.2.1 can be seen in figure 3.16. For all calculations and simulations in this section a rectified mains input voltage of 325 V has been considered, as well as an output voltage of 3.3 V and an output power of 100 mW.

The main goal is to trim the supply parameters in a way that reduce costs and provide good integration probabilities while sustaining acceptable efficiency. The most expensive part of the supply which is also hard to integrate is the inductor. Therefore the inductor size and with it the inductance has to be minimized. This leads to a higher converter frequency and up to a certain point to fewer losses in the inductor as described in section 4.2.5. As smaller energy packets are transfered with each cycle the output voltage ripple will decrease which allows the usage of a smaller output capacitor which will also promote integration efforts as described in section 4.2.6. Unfortunately the usage of a higher converter frequency will increase the losses in the power switch and the rectifier as described in section 4.2.2 and section 4.2.4. This section will illustrate the problems and boundaries of the conventional converter and explain the motivation for a new converter topology that brings certain advantages in size, costs and integration possibilities.

4.3.1 Converter frequency limitation due to minimum on-time

When designing a buck converter for wireless sensor and control nodes, the first problem lies in the high voltage ratio of the input and the output voltage. This would require a duty cycle of about 1% as described in equation 23 in section 3.2.1. The maximum switching frequency is therefore limited through the minimal on-time of the converter regulation as well as the transistor.

A first limitation is made through the dead-time of the current mode regulation to avoid a false turn-off triggering of the transistor due to switching noise in the current sense resistor or the reverse recovery current as described in section 3.2.5. This may be circumvented through the usage of the emulated current mode control [KD08] which is an improved version of the simple peak current mode control. The elimination of the current sense resistor eliminates the need of a dedicated dead-time and leaves the propagation delay of the controller.

The usage of the necessary high voltage MOSFET however leads to significant parasitic capacitances that will limit switching times. This is especially a problem when dealing with very small duty cycles as it leads to a minimum on-time. During the switch-off of the transistor the output capacitance C_{oss} of the transistor has to be recharged.

During that time the drain source voltage of the transistor rises till it reaches the input

voltage. Unfortunately to charge C_{oss} the current is still present and rising depending on the inductor L_1. The effective on-time therefore can be much greater than the intended on-time which is controlled through the gate especially in low duty cycle operation. Hence the minimum on-time is limited by the output capacitance C_{oss} of the MOSFET and the inductor current at the time of the off-switching. Figure 4.18 shows a simulation of this effect in detail. A simple buck converter was used to convert a 325 V input voltage to a 3.3 V output voltage while drawing 100 mW of output power. An inductor of 100 μH was used in this simulation which leads to DCM operation in combination with the switching frequency of 200 kHz. The used transistor was a 01N60C3 super-junction type MOSFET [Inf08] from Infineon with very low parasitic capacitances but capable of handling the rectified mains input voltage of 325V.

The gate of the transistor was driven to 7V for 10ns. Figure 4.18 shows a minor spike of the drain current during the switch-on phase which discharges parasitic capacitances. Note that the converter is in DCM operation and therefore no reverse recovery current is present. This spike would be much higher in CCM because of the reverse recovery of the used rectifier. After that the current starts to rise and the drain-source voltage drops to almost zero. The used transistor has an R_{DSon} resistance of 6 Ω. After the gate voltage drops back to zero because the controller wants to switch off the transistor, the drain-source voltage starts to rise again. During that time the current is still increasing and its slope is limited by the inductor. When the output capacitance C_{oss} of the transistor is fully charged the drain-source voltage reaches the input voltage of 325V and the drain current drops to zero as it commutes to the rectifier. When looking at the losses it is obvious that the output capacitance has influence on the switching losses. However, the calculation of the losses can

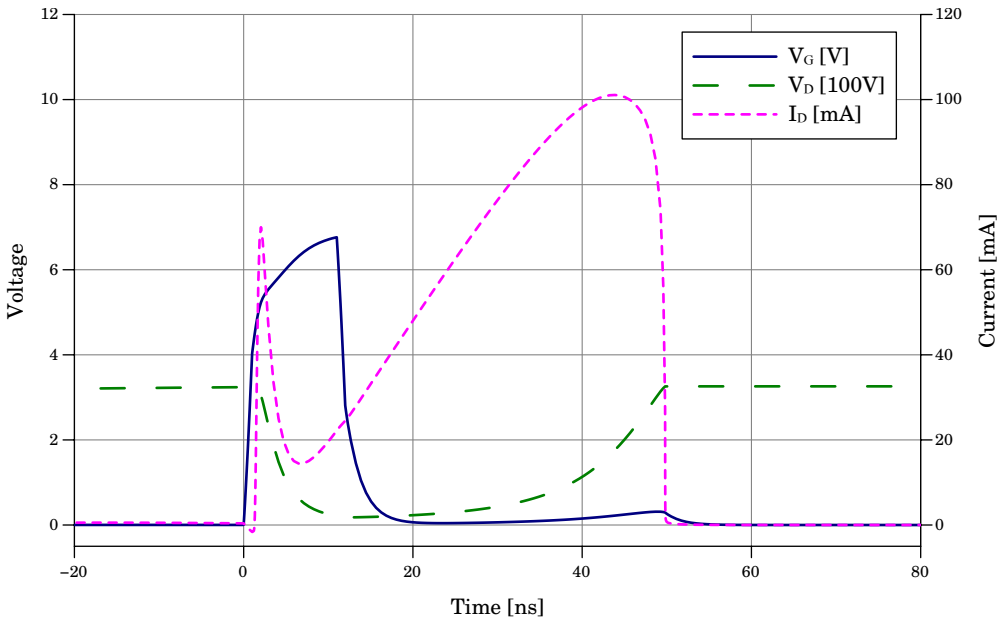

Figure 4.18: Extreme low duty cycle in a buck converter. The parasitic capacitances of the transistor dominate the on-time.

be done through the switching times that are influenced by the output capacitance C_{oss} as [XSJ+09] suggested. Depending on the calculation method of the switching times, the losses of the output capacitance can be introduced by an additional term. When looking at figure 4.18 it is clearly evident that the MOSFET is effectively on much longer as the controller intended, which may result in serious regulation issues. Additionally the gate voltage did not reach its designated value during the on-time which indicates a insufficient on-time. The practically usable switching frequency is therefore much lower. When operating the transistor with the minimum on-time during nominal converter operation the converter regulation may run into troubles as it cannot compensate for load jumps that would require a temporarily shorter on-time. Hence the practical nominal on-time in a converter should be considerably higher to add proper margin for the converter regulation.

4.3.2 Frequency limitation due to excessive losses

Figure 4.19 shows the generic correlation of the converter switching frequency, the input to output voltage ratio and the efficiency. The used simulation is based on an output voltage of 3.3 V, an output power of 100 mW, an inductance value of 100 μH (Coilcraft MSS1038-104NB), the 01N60C3 switching transistor and the SiC Schottky diode UPSC600 as rectifier. Note that the same components were used for the whole operating range to facilitate comparison. Hence component selection is not optimal for all operating areas. While P_{loss} is the sum of all losses within the circuit that have been extracted from simulation data, the efficiency calculates to :

$$\eta = \frac{P_{out}}{P_{out} + P_{loss}} \tag{43}$$

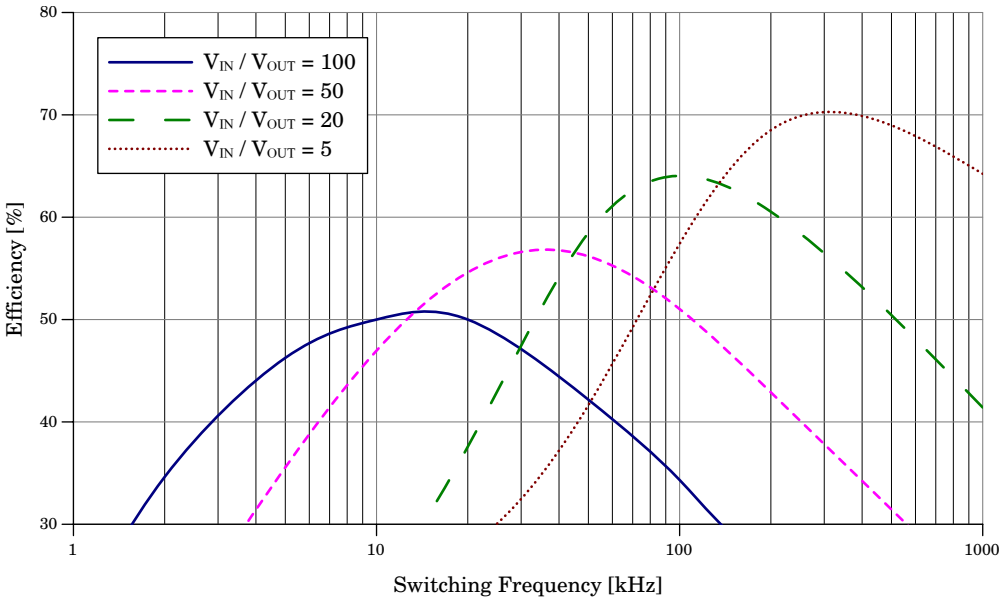

Figure 4.19: Correlation of the switching frequency and the input to output voltage ratio with the buck converter efficiency.

The first effect that can be observed is that the optimum efficiency is higher for a smaller input to output voltage ratio. The second effect is that the efficiency optimum is at a higher switching frequency for a smaller input to output voltage ratio. When the simulation data is observed in greater detail this characteristic is caused by the losses of the MOSFET and the rectifier as the losses of the other components are considerably smaller. Hence the losses of the MOSFET and the rectifier dominate the total losses. Note that the converter was switching between DCM and CCM depending on the actual setting. Only DCM operation allows reasonable efficiency for a high input to output voltage ratio as the switching losses of the rectifier due to its reverse recovery charge are avoided.

To further improve efficiency a synchronous rectifier can be used. The efficiency gain in this case depends on the used MOSFETs. Especially the low duty cycle operation and the high input voltage pose a considerable problem when optimizing this converter. To identify the key points in greater detail the converter losses were modeled and analyzed.

4.3.3 Detailed application specific analysis

A simple converter model was created exactly for the desired operation point to investigate the losses that occur in each component during operation. The converter model uses an input voltage of 325 V, an output voltage of 3.3 V and an output power of 100 mW. The model includes an inductor range of 50 μH to 1 mH and a switching frequency range of 50 kHz to 1 MHz. The inductor loss model is based on the specifications of the Coiltronics DR125 series inductors[Coi07]. More information on the used loss model can be found in the following subsection.

Depending on these values either DCM or CCM operation is used. The model can estimate the losses in the inductor due to conduction and core losses, the losses in the switching MOSFET and the losses in the rectifier. Losses in the output capacitor as well as losses due to parasitic circuit layout are not considered in this model as these losses have a minor contribution to the total losses.

At first the general converter behavior is analyzed. Figure 4.20 shows the dependency of the switching frequency and the value of the used inductance on the inductor current ripple. As expected the current ripple rises for smaller inductance values and lower switching frequencies. Note that the output power is constant at 100 mW in this model.

Furthermore the right side of figure 4.20 shows the transition between DCM and CCM operation of the converter. DCM operation is entered for small switching frequencies and small inductance values. As a consequence the inductor ripple current rises to maintain energy transfer to the output. For an output current of about 30 mA which corresponds to 100 mW the ripple current can go up to 250 mA within the specified frequency and inductance range. DCM operation is entered at an output current of 30 mA which corresponds to an inductor ripple current of 60 mA.

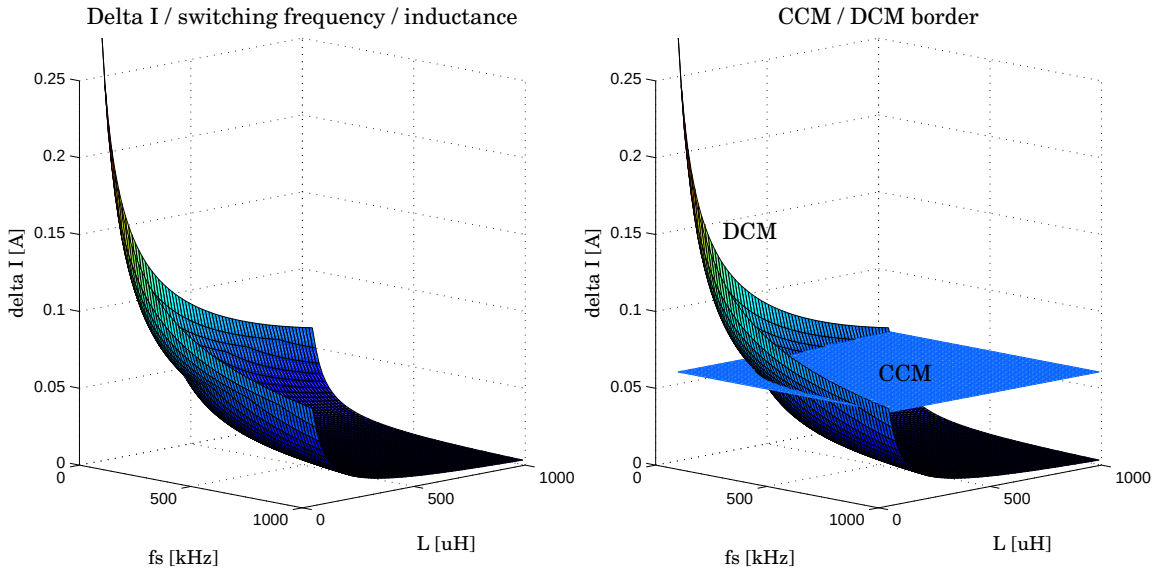

Figure 4.20: Dependency of the switching frequency and the inductance on the inductor ripple current at a constant output power of 100 mW at an output voltage of 3.3 V. The input voltage is considered 325 V.

Rectifier losses The rectifier has major contributions to the total losses. Its losses can be divided into switching losses that are caused by the reverse recovery of the rectifier and conduction losses that are caused by the its forward voltage. When modeling the switching losses a rectifier that has high voltage capabilities has to be used. A normal Schottky diode would have a small recovery charge but would not sustain the rectified mains voltage. One possibility is to use a normal silicon diode as rectifier. Unfortunately such rectifiers usually have a high recovery charge and therefore very high switching losses. Another possibility is the usage of a SiC (silicon carbide) Schottky diode. These diodes have a very small reverse recovery charge and can sustain the mains voltage. Unfortunately the forward voltage is very high for these diodes which would increase the conduction losses. The switching losses of the SiC diode are an order of magnitude smaller that the switching losses of a normal silicon diode. However, both diode types suffer significant switching losses that can reach several watts in CCM operation. Therefore the conventional buck converter cannot be used in CCM within this application field, even if a SiC diode is used as the losses would be intolerable. A solution to this problem may be to avoid CCM operation which would eliminate the reverse recovery losses of the rectifier.

The conduction losses of the rectifier are determined by its forward voltage. During CCM operation the duty cycle is independent of the switching frequency and the inductance. This leads to a constant off-time of the MOSFET and therefore a constant on-time of the rectifier. This leads with a constant $\frac{\Delta I_L}{2} + I_{L(DC)}$ to constant losses in CCM operation. In DCM operation the model shows a decrease of the off-time for falling switching frequencies and falling inductance levels. Furthermore $\frac{\Delta I_L}{2} + I_{L(DC)}$ rises with falling switching frequencies and falling inductance levels which again leads to constant rectifier conduction losses in DCM

operation that equal the constant losses in CCM operation. The model showed constant rectifier conduction losses of 25.5 mW for the silicon rectifier and 63 mW for the SiC rectifier due to its higher forward voltage.

These losses can be reduced further by the usage of a synchronous rectifier. The switching losses of a synchronous rectifier would be an order of magnitude higher than the switching losses of a silicon rectifier as the bulk diode of a MOSFET is very slow. Entering CCM would immediately destroy the rectifier as a result of the excessive losses. Therefore only DCM would be usable. The total losses of the rectifier at DCM operation are the constant conduction losses of 25.5mW for the used silicon rectifier (MUR460) and 63mW for the used SiC rectifier (C3D03060F).

Inductor losses Modeling the inductor losses was tricky especially for the core losses as they depend on many different parameters. The inductor losses were described in general in section 4.2.5. The created inductor model is based on the Coiltronics DR125 series [Coi07]. Various parameters and dependencies have been extrapolated from the corresponding datasheet. The DC resistance of the inductor has been considered 1.7 mΩ per μH and is linear dependent on the inductance. Without knowledge of the core geometry and the core material the core losses have been modeled using the given V·μs parameter for the DR125 series that correspond to a certain ΔI for a given inductance L and produce a given core loss. This parameter is depending on $\sqrt{L}$. The base value used was 4.75 V·μs per $\sqrt{L\,[\mu H]}$. The core losses itself are then quadratically dependent on the inductor ripple current as explained in section 4.2.5. Additionally the losses are linear dependent on the switching frequency which has also been included in the model. Core saturation effects as a result of excessive inductor current have not been modeled as the inductor current levels in this application field and for the investigated parameter range are way below the saturation current.

Figure 4.21 shows the copper losses (left) and the core losses (right) in the inductor . The copper losses scale mainly linear with the inductance value which seems reasonable as the DC resistance is depending on the inductance value [Coi07]. A stronger increase can be observed at small switching frequencies which is caused by the higher current peaks that are leading to a higher RMS value of the inductor current. With a maximum of 2 mW in the observed operation boundaries the inductor copper losses are relatively small for this application field.

The inductor core losses are pictured on the right side of figure 4.21. In general the inductor core losses decrease when the frequency increases which seems to be strange at a first look. This behavior is caused by the linear dependency of the losses on the frequency and the quadratic dependency on the current. As the switching frequency rises, the inductor current ripple that is the dominant factor for the inductor core losses falls. Additionally when the inductance value rises, the inductor current ripple falls which leads to decreased core losses. As the converter enters DCM operation the inductor core losses stay almost constant as the inductor has no DC current component which means that the energy which

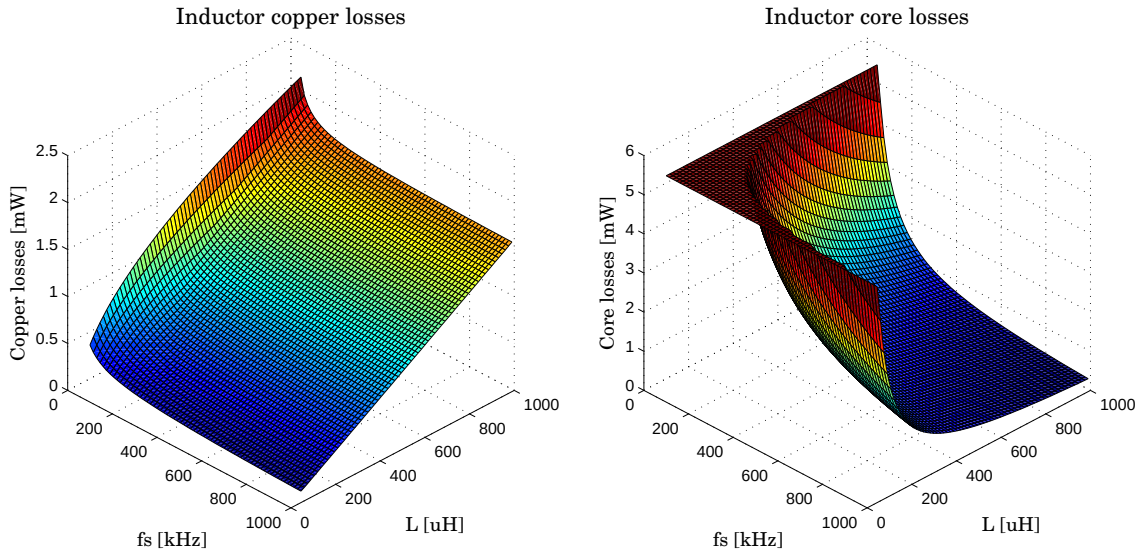

Figure 4.21: Core and copper losses of the used inductor for a conventional mains driven buck converter at an output voltage of 3.3 V and an output power of 100 mW.

is loaded into the inductor is entirely transfered to the output in each switching cycle. This is valid as long as the core is not near saturation. Again, the inductor core losses are relatively small for this application.

Figure 4.22 shows the comparison of the inductor core losses and the inductor copper losses (left) as well as the resulting total inductor losses (right). Depending on the operation parameters of the converter the inductor losses contribute maximum 8 mW to the total converter losses.

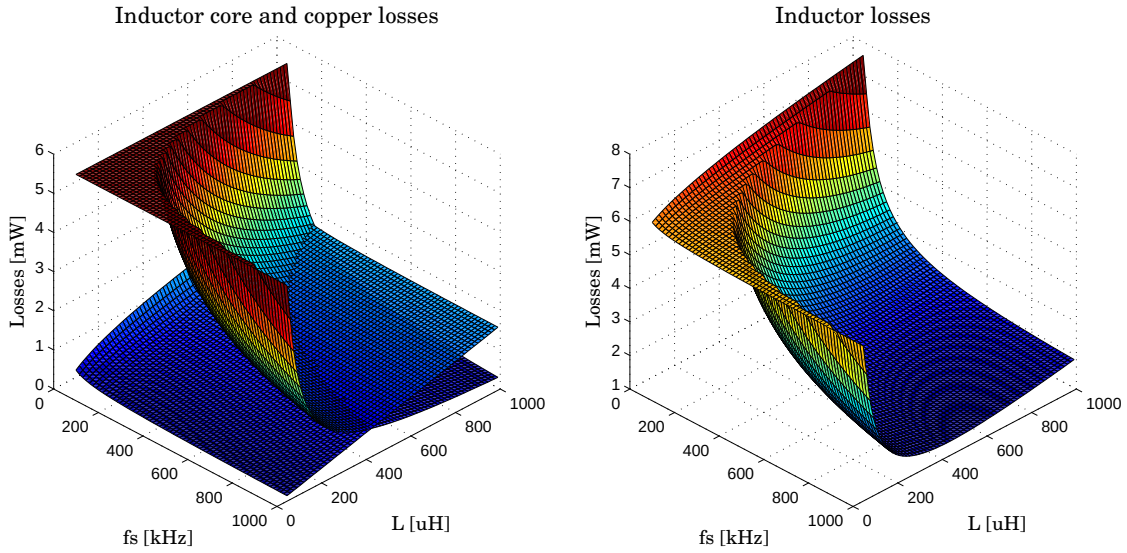

Figure 4.22: Comparison of the individual core and copper losses (left) and the combined total inductor losses (right) of the used inductor for a conventional mains driven buck converter at an output voltage of 3.3 V and an output power of 100 mW.

MOSFET losses The MOSFET losses can also be divided into conduction and switching losses as was explained in section 4.2.1 and 4.2.2. The base of the MOSFET loss model was the 01N60C3 transistor [Inf08] which is suitable for this application. The conduction losses were modeled using the on-state resistance of the transistor (R_{DSon}) and the RMS drain current. The switching losses were modeled using a fixed switching time of 50 ns which were controlled using a fixed gate resistor. The transition losses then depend on the inductor current by the time of the switching. The losses due to the output capacitance C_{oss} were included in the linear approximation of the transition losses. The gate charge losses were also included in the model but their contribution to the total switching losses is neglectable for this application field and the used transistor. Figure 4.23 shows the conduction losses (left) and the switching losses (right) of the used MOSFET.

The conduction losses are relatively small as the on-time of the transistor is short because of the high input voltage and the resulting low duty cycle. They are lower for higher switching frequencies and higher inductance values because the current ripple is lower. Because of the low duty cycle even a transistor with a high R_{DSon} value of 6Ω produces insignificant losses. The switching losses on the other hand are significant higher. As expected they rise linearly with the switching frequency. The dominant losses in this application field are the transition losses. Because the switching times are equal for the switch-on and the switch-off and the corresponding losses are proportional to the drain current in the switching moment, the switching losses are independent of the used inductance during CCM operation. In DCM operation the switch-off losses are dominant as a relatively high current has to be switched off.

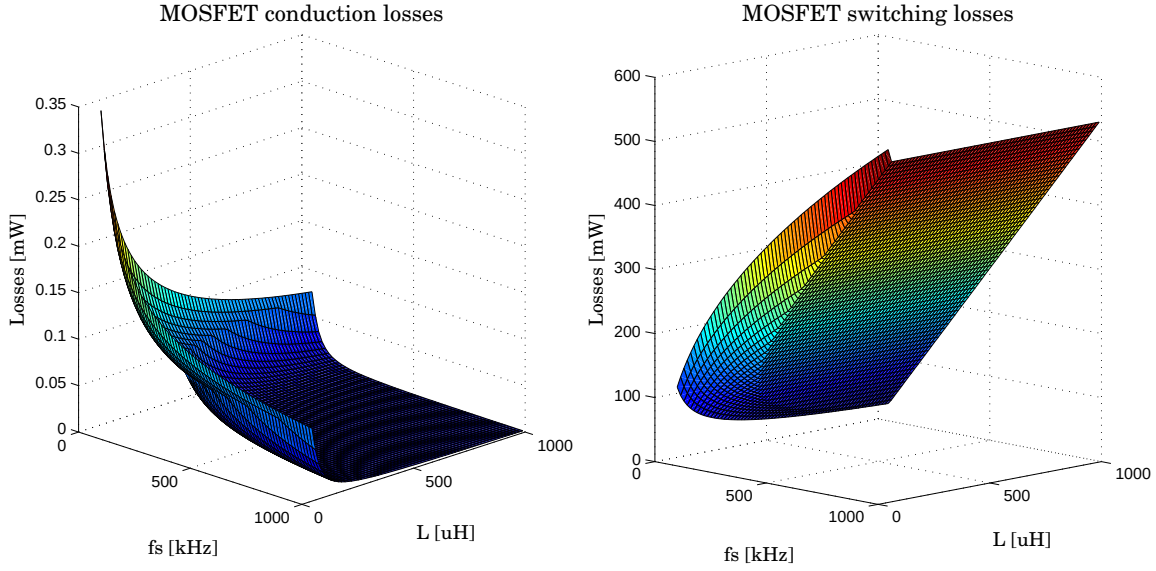

Figure 4.23: Switching and conduction losses of the used MOSFET for a conventional mains driven buck converter at an output voltage of 3.3 V and an output power of 100 mW.

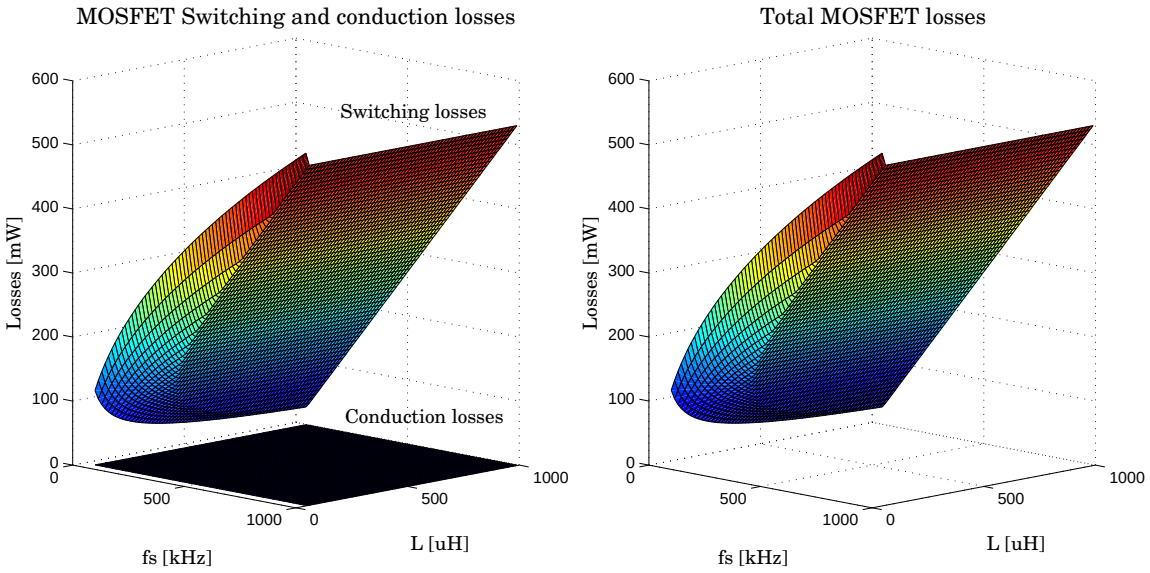

Figure 4.24: Comparison of the switching and conduction losses (left) and total MOSFET losses (right) of the used MOSFET (01N60C3) for a conventional mains driven buck converter at an output voltage of 3.3 V and an output power of 100 mW.

Figure 4.24 shows the comparison of the MOSFET switching and conduction losses (left) and the total MOSFET losses (right). It is clearly evident that the conduction losses are neglectable and the switching losses dominate the total losses. Normally this indicates that the wrong transistor is used for this application as with a type of increased R_{DSon} the parasitic capacitances would be reduced and the overall losses would be smaller. Unfortunately the 01N60C3 type transistor [Inf08] has already a resistance of 6 Ω and a further increase would not significantly decrease the parasitic capacitances. This is due to the fact that the transistor has to have high voltage capabilities for this application field that go along with increased parasitic capacitances.

Total converter losses For the total converter losses only DCM operation is investigated as CCM operation would lead to excessive losses in the rectifier. Figure 4.25 shows the modeled total losses of the converter during DCM operation. The DCM demand limits the usable frequency and inductance range dramatically. The converter has the best efficiency for lower switching frequencies and medium inductance values. As can be seen from figure 4.25 the efficiency ranges from about 15% to 50%. The efficiency may be increased by further reducing the switching frequency in DCM which will lead to a much higher ΔI_L as can be seen in figure 4.20. This will inevitable lead to a bigger inductor which makes integration harder.

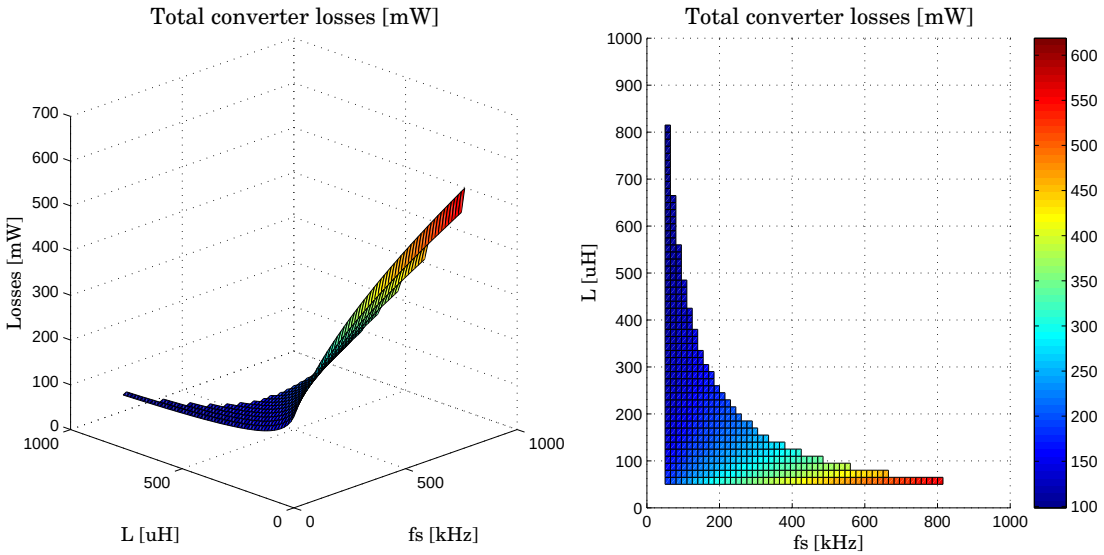

Figure 4.25: Total converter losses in DCM operation at an output power of 100 mW. The efficiency ranges from about 15% to 50%.

Conclusion In this section the simple buck converter design was evaluated for the usage to power wireless sensor and control nodes. On a first approach this conventional converter design can work in DCM with reasonable efficiency as figure 4.25 suggested. This converter would require a high voltage switching transistor, a high voltage switching rectifier and a relatively big inductor. As the switching frequency falls to stay at a reasonable efficiency the inductor peak current rises. This requires an inductor that has a relatively high saturation current which requires a physically bigger inductor. As the inductor is already the most expensive part of the supply this would further increase the costs and decrease the chance of a reasonable converter integration. Also the usage of higher inductance levels would increase the inductor cost. The main goal is therefore to decrease the inductance value and increase the switching frequency. Unfortunately this is the point where the converter gets incredibly inefficient, mainly due to the switching losses of the MOSFET. Furthermore the integration possibilities of this converter are very limited, as a large number of high voltage parts have to be used, and a physically big inductor is necessary. Hence this conventional converter type is not suitable to power wireless sensor and control nodes as it is either expensive and big or inefficient. This gives motivation to develop a new converter concept that can utilize a smaller inductor by increasing the switching frequency without loosing too much efficiency. Furthermore the usage of high voltage components has to be minimized to allow reasonable converter integration.

5 New SMPS-based phase controlled converter concept

As explained in section 4.3 the high input-to-output voltage ratio is one of the problems of mains driven standby power supplies for smart appliances. In combination with the necessary physically big high voltage transistor this leads to high switching losses especially for higher switching frequencies. An idea to circumvent this problem is to utilize the slope of the input voltage sine wave. This way, it may be possible to use a significant lower voltage as input voltage for the subsequent converter. This brings several advantages for the design of the subsequent converter. As the subsequent converter switches have to operate at a smaller voltage they can be built smaller which brings several advantages mainly in their switching characteristics.

5.1 Figure of merit

Because the switching transistors of the converter don't have to sustain the full mains voltage they can be built smaller. There are several figure of merits involving of the on state resistance R_{DSon} of a MOSFET and its parasitic capacitances. This figure of merits can be approximated constant for a specific MOSFET technology and describe the performance of a given MOSFET technology. The most commonly used figure of merit describes the dependency of the on state resistance R_{DSon} of a MOSFET from its gate charge Q_G. For a lower R_{DSon} value the transistor needs to be of larger chip size which results in a greater gate charge. The resulting FOM_{QG} parameter is generated by the multiplication of the gate charge Q_G and the on state resistance R_{DSon}. Another figure of merit describes the dependency of the on state resistance R_{DSon} and the output capacitance C_{OSS} of the transistor (FOM_{COSS}).

Additionally these figure of merits depend on the maximum drain source blocking voltage of the MOSFET. Because this parameter is technology dependent the FOM allows a good comparison between transistor technologies with different blocking voltages. [Bal11] (p. 551, fig 10.16) compares the blocking voltage to the figure of merit for different MOSFET technologies. A power law relationship was found between these two parameters. A short survey of suitable MOSFETs and a comparison of the blocking voltage with the figure of merit came to a similar conclusion. While the Infineon transistor IPT004N03L has a blocking voltage of only 30 V it has a FOM_{QG} of 101 $m\Omega{\cdot}nC$ and a FOM_{COSS} of 141 $m\Omega{\cdot}nC$. The SPP11N60C3 transistor as an example for the CoolMOS technology that is used for mains applications on the other hand has a blocking voltage of 650 V and a FOM_{QG} of 19000 $m\Omega{\cdot}nC$ and a FOM_{COSS} of 50000 $m\Omega{\cdot}nC$.

This means that the losses can be greatly reduced when a transistor with a lower blocking voltage could be used. This is only possible if the converter input voltage can be reduced accordingly. The rectifier will benefit from this too because now a simple low voltage Schottky diode is possible or even a synchronous rectifier can be used without producing too much switching losses. Because the whole converter can operate with a lower voltage the components including the inductor don't have to be high voltage resistant.

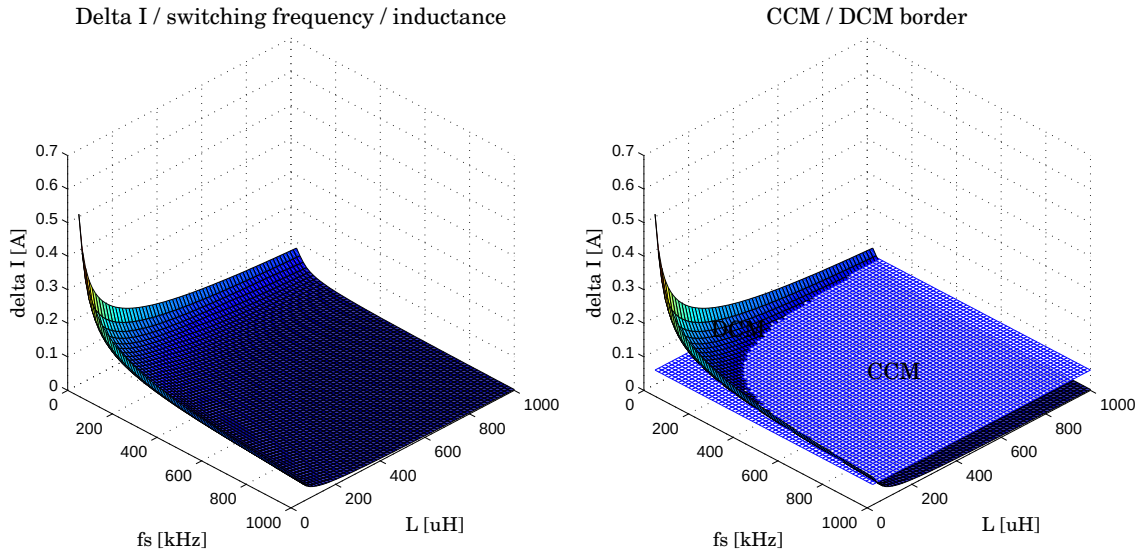

Figure 5.1: Dependency of the switching frequency and the inductance on the inductor ripple current at a constant output power of 100 mW at an output voltage of 3.3 V. The input voltage is considered 24 V.

5.2 Effects of the reduced input voltage

To investigate the effects of the reduced input voltage on the operation mode and the inductor size the model that was created earlier was reused to predict the converter behavior. The input voltage was lowered to 24 V and the parameters of the transistor (IPP065N03L) and the rectifier have been adapted accordingly. A synchronous rectifier was modeled including a parallel Schottky diode. Figure 5.1 shows the dependency of the switching frequency and the value of the used inductance on the inductor current ripple for the described converter concept. In DCM the ripple current is quite high which will stress the components. In the straight forward concept the high converter input voltage produced very high switching losses in the rectifier in CCM which pretty much disqualified CCM operation.

With the now lowered input voltage these switching losses decrease dramatically as figure 5.2 shows. On the contrary, CCM operation is the better choice for this converter as a much lower inductor peak current leads to reduced stress on the components and a smaller inductor. Even at extremely high switching frequencies the converter offers decent efficiency. Overall the reduced input voltage offers great advantages to the converter in terms of efficiency, size and integration efforts. On the other hand an additional first stage will be necessary to reduce the input voltage accordingly. The main question that will be investigated in the subsequent sections is if the first converter stage can be implemented in a way to retain most of the advantages of the low voltage converter stage without adding further problems.

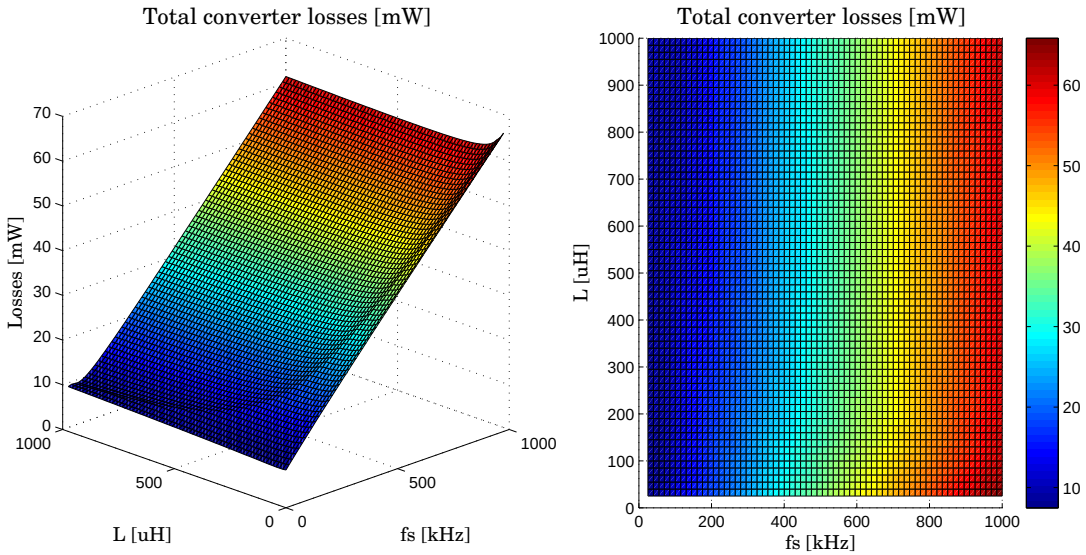

Figure 5.2: Total converter losses of the converter. The output power has been considered 100 mW at an input voltage of 24 V. The converter was modeled with ideal dead times and a synchronous rectifier with a Schottky diode in parallel.

5.3 First converter stage - principle of operation

As explained earlier the main problem in designing an efficient, small and easy to integrate SMPS power supply for wireless sensor and control nodes is the high input voltage in combination with a duty cycle of about 1 %. This requires a high voltage switch and a high voltage rectifier that will produce considerable switching losses and thus limit the switching frequency. A possible way to face this problem is to lower the input voltage to the SMPS through a preceding first stage that is described here.

The simplest way of voltage limitation could be achieved by a linear regulator which on the other hand would dramatically increase the losses. If a linear regulator is used to lower the input voltage from 325 V, which is the rectified mains voltage, directly to the target voltage of 3.3 V, the input power would be about 10 W. If a linear regulator is used to lower the rectified mains voltage to about 33 V, and a subsequent high efficiency SMPS (e.g. LTC3642 [Lin08]) is used to generate 3.3 V then the input power would be about 1.3 W which is considerably lower but still too high for the target application. Therefore a simple linear regulator is not suitable if the output is drawing power constantly.

As published in [Luk11] and [GHW+12] a solution to this may be the utilization of the input voltage sine wave. The converter can draw power from the mains only when the input voltage is under a certain level. The usable voltage region therefore is around the zero crossing of the mains voltage. Hence the converter could operate at a lower input voltage and therefore use smaller switching transistors that can operate at a higher switching frequency without producing excessive switching losses. The drawback would be the short time the first stage can operate as a result of the short time the input voltage is in the required range which would require an increase of the input current into the first stage for that small

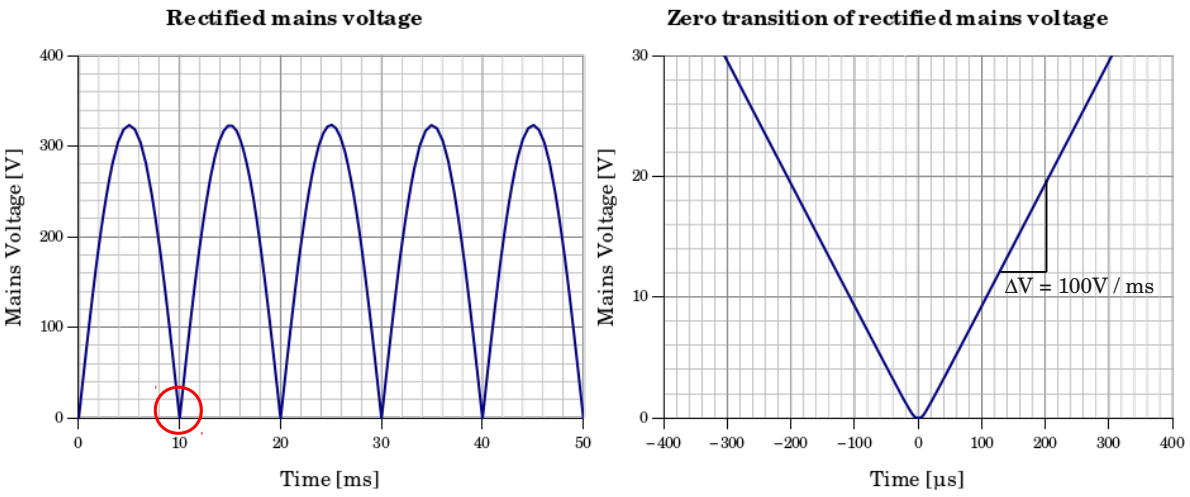

Figure 5.3: Usable fraction of the mains input voltage sine wave in a phase controlled SMPS design. The converter only operates near the zero crossing of the mains voltage when the mains voltage is under a certain level.

time period to have the same mean output power. A high voltage switch is still necessary but doesn't have to operate at the full switching frequency as it only have to connect the supply to the mains twice every mains cycle.

Figure 5.3 shows the mains region that could be utilized for this concept. The left side of figure 5.3 shows the rectified mains voltage that is not buffered with a capacitor. The usable region is marked with a red circle. The right side of figure 5.3 shows the mains voltage around the zero crossing. At an effective mains voltage of 230 V and a mains frequency of 50 Hz the mains voltage slope dV_{mains} / dt at the zero crossing is about 100 V / ms. When a voltage window of up to 24 V is used which is a decent intermediate auxiliary voltage the usable time window would be about 235 μs before and after the zero crossing which would lead to a total time window of 470 μs. This time window is relatively small compared to the periodic time of 10 ms of the rectified mains voltage. Because only about 5 % of the mains cycle can be used all the necessary power has to be concentrated within that time. Presuming a maximum allowable input voltage to the second stage of 24 V and a constant power requirement of 100 mW the input power within the time window would be about 2 W. The mean voltage during the time window is 12 V and therefore the theoretical mean input current calculates to about 170 mA. That is true only if the full time window can be used.

Figure 5.4 shows a simplified block diagram of the proposed converter topology. After rectification the input is controlled through a high voltage switch T_1. This high voltage switch is still necessary but does not suffer the high switching losses as it is not operated with the converter switching frequency but the mains frequency. Simplified this topology connects the subsequent converter stage to the mains whenever the mains input voltage is within the allowed voltage range. The Zener diode D_5 is a protection diode for the subsequent converter. Unfortunately this converter concept brings several problems.

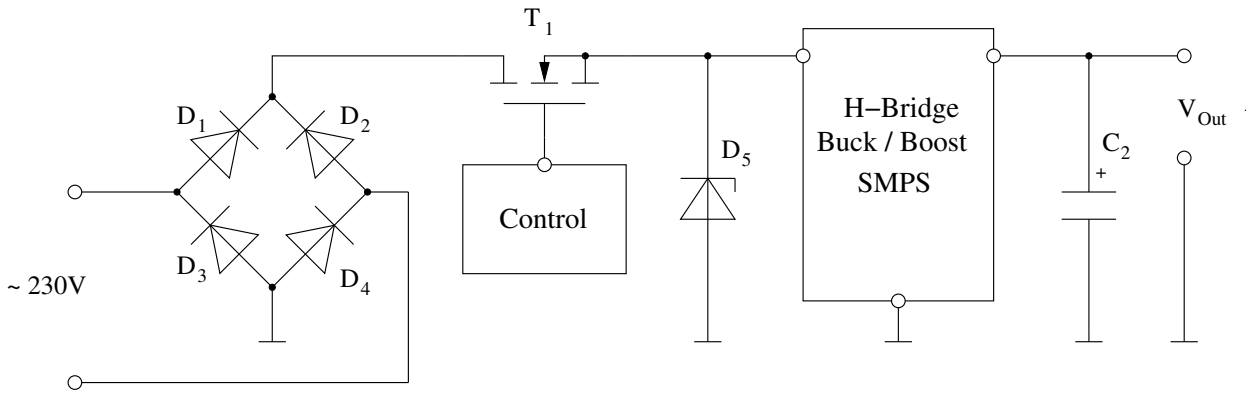

Figure 5.4: Simplified block diagram of the proposed converter. The high voltage transistor T_1 connects the mains to the subsequent SMPS only when the mains voltage is under the maximum allowed converter input voltage.

A first problem is the necessary input capacitor of the SMPS. When it is not present the high frequency current path of the converter would run over the mains which would produce excessive EMI and additional losses. When this capacitor is used and the switch is turned on at 24 V during the falling mains slope, a current peak would instantaneously reload the capacitor which again would lead to higher EMI and losses. Depending on the size of the used capacitor this may or may not be tolerable. Another problem is the time window detector. Because it is working with the input voltage sine wave, parts of the detector have to be in the high voltage path which makes integration harder and will produce additional losses. The startup of this supply is also a significant problem. The control logic and the detector have to be powered in order to operate the supply. This may require an additional regulator that is powered from the mains which will again produce additional losses and makes integration harder because of the high voltage. The output capacitor C_2 may also be problematic as it has to be very big to buffer the load during a mains cycle in case the input capacitor of the converter is not present or is very small to just provide a HF current path. Also a minimum voltage ripple is intended which further increases the output capacitor.

These problems will be addressed during the next sections of this work. Possible solutions will be presented, simulated and some of them will be verified in hardware. All of the solutions mainly use a high voltage switch to limit the input voltage. The main difference lies in the control mechanisms of the high voltage transistor and the subsequent converter stage. The most promising control options will be discussed now.

5.3.1 Simple capacitor reload

A simple solution is to use only the second half of the time window where the input voltage sine wave rises from zero to the designated maximum allowed voltage. In this case an input capacitor for the SMPS is no problem as this capacitor would be reloaded through the rising voltage slope of the input voltage sine wave. This input capacitor would be used to store the energy between the usable time windows of the mains voltage.

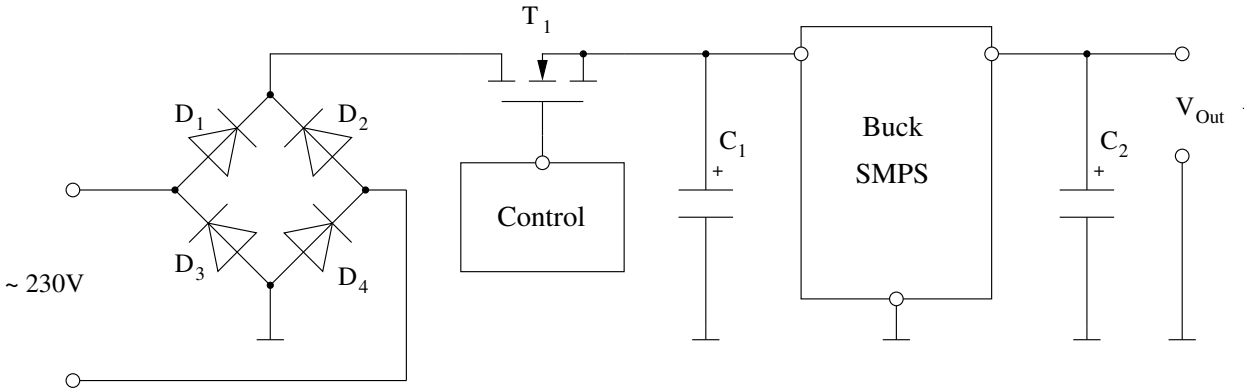

Figure 5.5: Block diagram of a power supply with a simple reload of the input buffer capacitor C_1. The transistor T_1 is switched on at the zero crossing of the mains input voltage and stays on until the voltage at C_1 reaches its designated value.

Figure 5.5 shows a block diagram of the converter. The transistor T_1 is switched on at the zero crossing of the input voltage sine wave and remains on until the voltage at C_1 reaches the maximum allowed input voltage of the subsequent converter. Because the voltage slope is linear near the zero crossing of the mains voltage the reload current of the capacitor C_1 is depending on the capacitance and is theoretically constant within the used time window. However, several parasitic effects cause a slower rise of the reload current.

Figure 5.6 shows the reload of the input buffer capacitor C_1. For this simulation the supply was equipped with a 5 μF input buffer capacitor C_1 that was providing power to a constant load of 100 mW. Hence the lower the voltage at C_1 drops during the discharge process of C_1, the higher rises the output current to maintain a constant output power. The left side of figure 5.6 shows the voltage at the capacitor C_1. During the discharge process of C_1 outside the usable mains time window the capacitor voltage drops drastically.

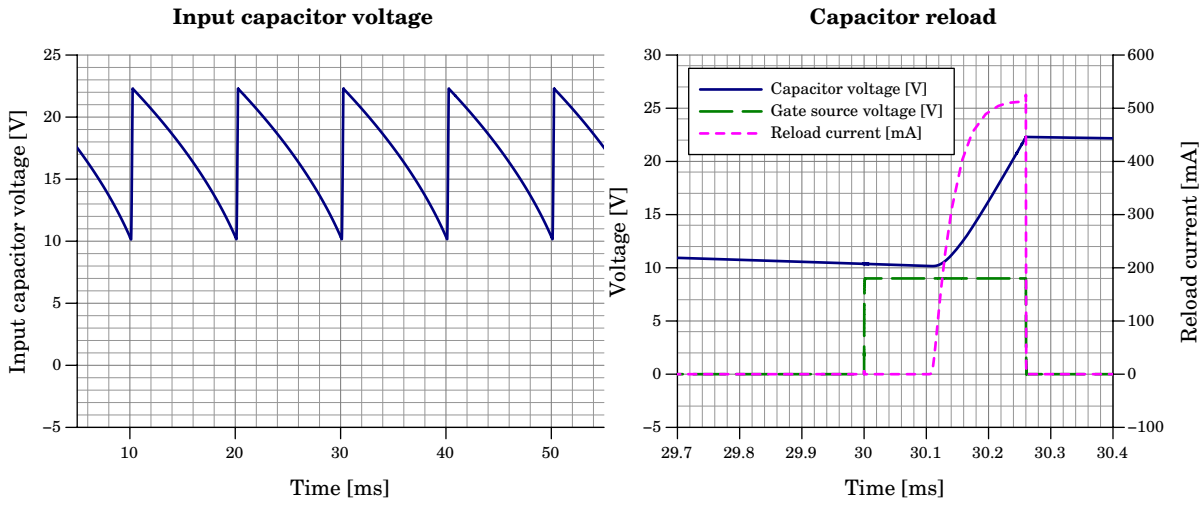

Figure 5.6: Voltage at the input buffer capacitor C_1 (left) and the reload procedure of the input buffer capacitor C_1 (right). A higher capacitance value would result in a higher reload current for a shorter time providing the output power is the same.

If a bigger capacitor is used the voltage ripple would be smaller what would seem to be a good thing at first. But the capacitor is reloaded only during the time the mains voltage is higher than the actual capacitor voltage and lower then the maximum allowed voltage. Therefore a bigger capacitor with the resulting smaller voltage ripple would have fewer time to reload. That would concentrate the reload current and increase EMI and losses. Therefore the capacitor has to be chosen with respect to the load as he should be discharged as much as possible but with a sufficient margin. Note that the energy stored in the capacitor decreases quadratic with the capacitor voltage which results in a very high voltage slope at low capacitor voltage levels which requires a higher voltage margin.

The right side of figure 5.6 shows the reload process of the capacitor C_1. The transistor is switched on at the zero crossing but the reload process starts only after the mains input voltage rises over the capacitor voltage. The reload current is higher and shorter for a higher capacitance value. Therefore it is desirable to select the smallest capacitor that is possible. The simulation showed a reload current spike of about 500 mA which is considerable and usually not acceptable for a larger number of nodes. Unfortunately the current cannot be better distributed over time with this control method which is its main disadvantage. If the relatively high current spike can be tolerated this is a very efficient primary stage as the control method is very simple and the additional losses are small as the reload current is shaped and limited by the mains input voltage sine wave.

5.3.2 Energy storage

All concepts that use a small time window to draw energy from the mains have to buffer the energy during the rest to ensure constant power delivery to the load. The necessary storage capacitor therefore has to buffer enough energy to bridge half a mains cycle. If this capacitor is at the output it additionally has to ensure a minimum voltage ripple that is defined by the used load.

If the supply is designed to power a 100 mW load at 3.3 V and a maximum allowed output voltage ripple is 50 mV then the necessary output capacitor would be about 6000 μF. This is a quite big capacitor and is not suitable in terms of size and cost efficiency. When the energy is stored at the input of the second stage at an auxiliary voltage of 24 V then the necessary output capacitor decreases dramatically as the energy storage capacitor that has to buffer between the mains cycles doesn't have a voltage ripple limitation and the output capacitor only has to filter the output of the secondary SMPS.

Additionally the energy that is stored in a capacitor increases quadratically with its voltage. This fact further decreases the necessary size of the energy storage capacitor. Hence a higher auxiliary voltage dramatically decreases the size of the energy storage capacitor.

The necessary storage capacitor calculates to :

$$C_s = \frac{2 \cdot E_{buff}}{V_{max}^2 - V_{min}^2} \tag{44}$$

$$E_{buff} = \frac{P_{out}}{2 \cdot f_{mains}} \tag{45}$$

The necessary buffer energy E_{buff} depends on the output power and the time the capacitor has to bridge which in this case because of the full bridge rectifier is half a mains cycle. At an auxiliary voltage of 24 V and an output power of 100 mW at an allowed voltage ripple at the energy storage capacitor of 12 V which leaves V_{min} at 12 V and V_{max} at 24 V the necessary capacitance size would be 4.63 μF. Note that because of the losses in the secondary stage its input power is higher that its output power which also has to be considered when an energy storage capacitor is selected. Also note that as explained earlier a suitable minimum voltage margin has to be considered that involves the minimum converter operation voltage and the fact that the stored energy decreases quadratically with the capacitor voltage.

5.3.3 SMPS controlled capacitor reload

As explained earlier the disadvantage of a simple transistor control that simply reloads the capacitor at the start of each mains cycle is the high current concentration near the zero crossing and the dependency of the reload current on the input capacitor. Depending on the remaining capacitor voltage at the start of the reload cycle only a small part of the total time window can be used. This problem can be solved by inserting an additional SMPS stage into the converter that charges the input capacitance. Figure 5.7 shows a block diagram of the described converter. The first stage consists of the high voltage switch and its control logic, the second stage is the buck/boost SMPS and the third stage is the final buck SMPS stage. At the zero crossing of the mains voltage sine wave the transistor T_1 is turned on. After the mains voltage reaches the maximum input voltage the transistor is switched off again. This will load the capacitor C_1 that was entirely empty to the maximum input voltage. In contrast to the simple approach the reload time of capacitor C_1 is extended over the entire time window from the zero crossing till the transistor is switched off again. Depending on the size of C_1, the needed energy and the accepted ripple current load on the mains, the first SMPS stage can be turned on during that time or immediately after the time window to transfer the energy to the energy storage capacitor C_S. The second stage is turned off again when the energy in C_1 is entirely depleted to ensure proper reload starting at the zero crossing of the next mains cycle. The third stage is running continuously to ensure a constant voltage at the load.

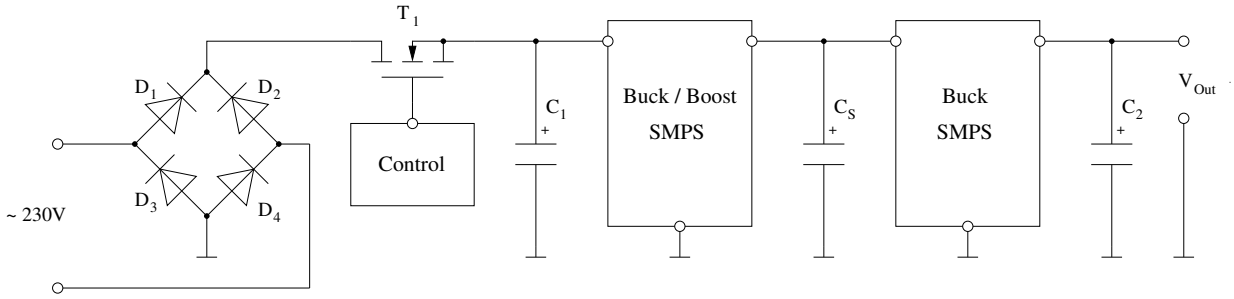

Figure 5.7: Three stage power supply with enhanced reload of the input buffer capacitor C_1. The transistor T_1 is switched on at the zero crossing of the mains input voltage and stays on until the mains voltage reaches the maximum allowed value. The second stage depletes the capacitor C_1 entirely so the next reload phase starts in the zero crossing again.

The advantage of this concept is the better utilization of the time window which reduces the peak current. Unfortunately a second SMPS stage is necessary to achieve this goal. In terms of cost efficiency and integration possibilities this may only be suitable if the two SMPS stages can be combined and share the same inductor which would result in an entirely new SMPS topology. Hence the simple approach which was described in section 3.2 cannot be implemented as this would require at least two inductors. This matter is addressed in a later section of this work.

On its own the advantage of this concept possibly would not justify the additional SMPS stage and with it the increased complexity but it dramatically increases the flexibility of the design. With this stage it is possible to utilize not only the time after the zero crossing but also the time before the zero crossing which doubles the usable time window. Additional the time window could be further increased while the excess voltage is dissipated in the transistor.

5.3.4 Symmetric time window control

The maximum allowed converter input voltage is determined by the maximum ratings of the subsequent second stage converter. When the maximum allowed input voltage is increased, the time window is automatically expanded. Because of the increased voltage and the expanded time window the mean input current during the time window decreases quadratically with the maximum allowed voltage of the second stage.

This is valid only to a certain voltage as the mains voltage slope can only be linearly approximated near the zero crossing. Because the increase of the maximum input voltage of the second stage requires physically bigger switching transistors with higher blocking capabilities the parasitic capacitances and with them the switching losses will also increase. Therefore it may be desirable to limit the converter input voltage while simultaneously increasing the time window.

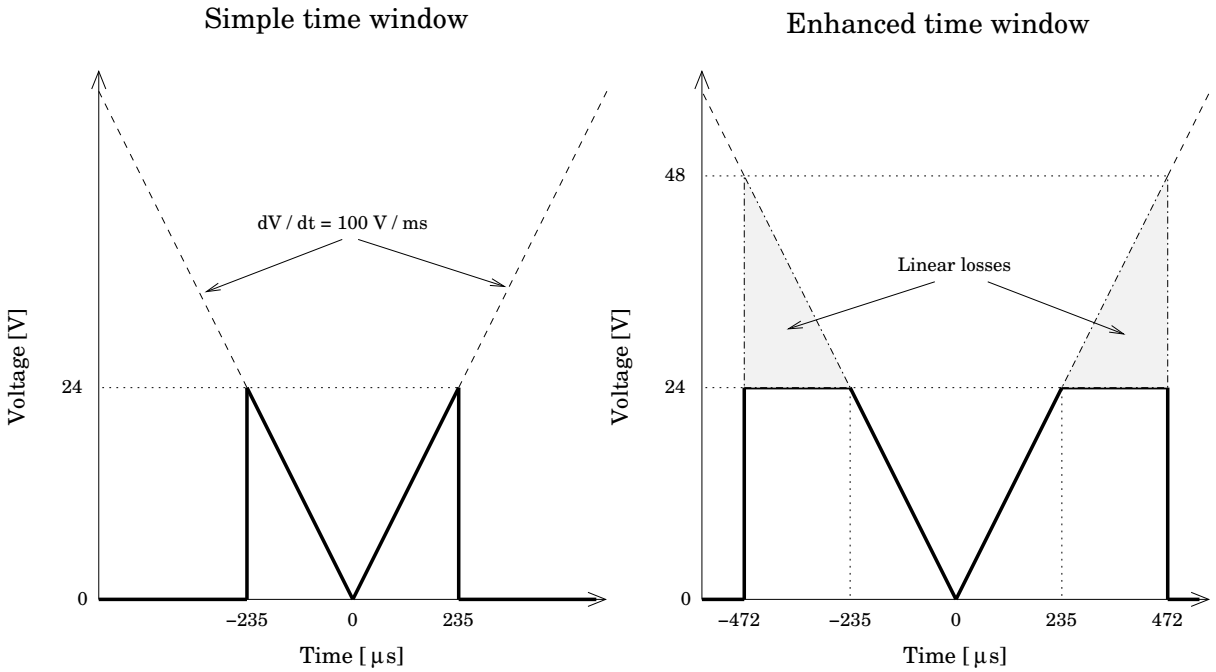

Figure 5.8: Usable time window of the input voltage sine wave for a maximum converter input voltage of 24 V. The left side shows the simple time window. The right side shows an enhanced time window where the excessive voltage is linearly dissipated in the transistor.

Figure 5.8 shows the usable voltage and time window of the mains input sine wave. The maximum input voltage to the subsequent converter is considered 24 V for the moment. The left side of figure 5.8 shows the simple time window that could be used to directly power the converter. When the time window is doubled (right side) then the input voltage would rise to about 48 V. The excessive voltage has to be linearly dissipated in order to ensure the maximum converter input voltage of 24 V. As can be seen on the right side of figure 5.8 the usable mean voltage over the time window would be 18 V which would result for the same mean current within the time window in an output power that is 3 times the output power of the simple time window on the left side. Hence for the same output power the mean current would be only a third of the original which may bring some advantages in EMI and the transistor selection. Unfortunately the enhanced time window suffers additional linear losses for the input voltage levels over 24 V. These additional losses will be a third of the used power in this example. Depending on the acceptable input current peaks during the time window, it can be expanded at the cost of efficiency. Also the allowable converter input voltage may be increased by changing the subsequent converter technology.

The control circuit for the high voltage transistor T_1 is dependent on the actual used concept. The first idea is to switch the transistor hard at a specific time of the mains input voltage. This is suitable when only the time after the zero crossing is used as the capacitor C_1 would suffer a high current peak when the transistor is switched on earlier. Even if the capacitor C_1 is held small a considerable current peak would occur that would produce EMI and corresponding losses. In the moment an enhanced time window is used as shown on the

right side of figure 5.8 a hard switching of transistor T_1 is out of the question as this would result in an overvoltage at the secondary converter stage. A solution to this problem is to control the transistor T_1 as a simple linear regulator.

5.4 HV transistor control

There are several possibilities to control the high voltage transistor and with it the input behavior of the supply. A common problem is that the transistor has to be controlled over the gate source voltage while the source potential is not connected to ground. A bootstrap circuit could be used to control the MOSFET accordingly but the slow switching frequency may be problematic. Additional an independent charge pump could generate a voltage that is accordingly higher than the source voltage to control the gate of the high voltage MOSFET. This solution would add additional complexity to the supply and may increase the losses. Additionally this solution would not allow the utilization of a symmetrical time window. Therefore the transistor T_1 is controlled as linear regulator to generate a constant output voltage of the first stage of 24 V. As linear operation would generate considerable losses when the input voltage sine wave is over the output voltage of 24 V the subsequent second stage has to make sure only to draw power during its designated time window.

The simplest way to implement a linear regulation is to apply a constant voltage to the gate of transistor T_1. The source would have to follow this voltage reduced by the threshold voltage of the transistor. This regulation may reduce the usable voltage range as the source voltage of transistor T_1 is the gate voltage reduced by the threshold voltage of the transistor. When the gate of the transistor is at a constant voltage of 24 V and the mains voltage reached the 24 V which will signal the second stage to draw power the voltage at the source of T_1 is already at about 20 V depending on the threshold voltage of the transistor. Alternatively, the source voltage can be integrated in a regulation loop of the linear regulator. This would result in a higher gate voltage which is a good thing when the circuit is implemented discrete. If the supply is integrated this may not be possible as the secondary stage would preferably be designed to work with the maximum voltage possible for that technology which would prevent the gate voltage of T_1 to be higher when implemented in the same technology.

Figure 5.9 shows a block diagram of a possible supply with a preceding linear stage. The first linear stage of this supply consists of the transistor T_1 in combination with R_1, C_3 and D_5 to generate a constant gate voltage. To compensate the impact of the threshold voltage of the transistor T_1 the source voltage can be included in a regulation loop. Alternatively, an ultra low power shunt regulator can be used to power the gate. The needed current for the gate voltage reference regulator is critical as only 100 μA would generate around 23 mW of losses as a result of the high input voltage which is considerable in comparison to an output power of 100 mW. If these losses are not acceptable then an alternative current limiter has to be found to replace R_1. A miniature capacitive supply could be used to achieve this goal. Depending on the actual needed current which is depending on the regulator

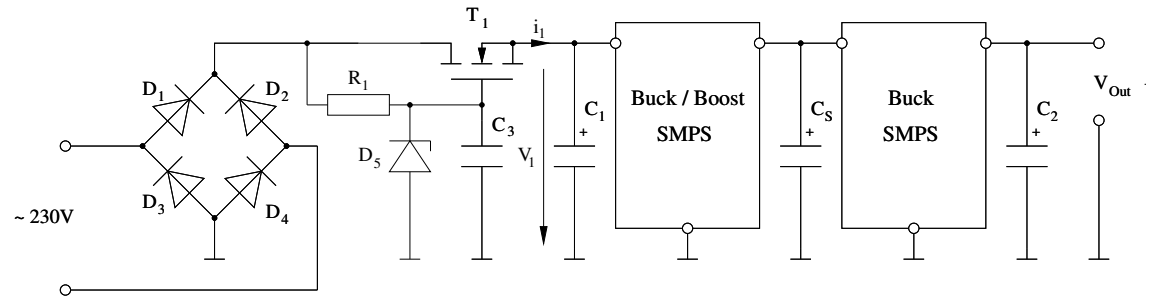

Figure 5.9: Block diagram of the proposed supply that is able to utilize a symmetrical time window. The first stage is a simplified linear regulator through a constant gate voltage of transistor T_1. A more advanced design could include the source voltage of T_1 in a regulation loop.

design and after consulting figure 3.5 a current limiting capacitor of a few nF or even less could be sufficient. If an external component has to be avoided the parasitic capacitance of HV semiconductor devices like the needed high voltage transistor T_1 could be utilized and integrated together with T_1. The actual device parameters and the implementation costs will define if this is a viable solution. Another approach is to power the gate directly from the input only during startup and then switch to an alternative voltage control which is powered from C_S. This would add further complexity but also reduce losses. The capacitor C_1 has to be considered carefully as it has to attenuate the high frequency strain on the mains. Although for this reason a bigger capacitor might be better, this would lead to larger time window displacement as well as a higher input current when the capacitor is recharged from the mains shortly after its zero-crossing.

Figure 5.10 shows a simulation of the first supply stage of the proposed converter when a resistive load is applied. The resistive load has been chosen to dissipate a mean power of 100 mW for the left and the right side. A constant gate voltage of 24 V has been chosen to operate the first stage in linear mode. The control circuit in this simulation is operated with a miniature capacitive supply and a rudimentary shunt regulator. On both sides the source voltage is therefore reduced by the threshold voltage of the transistor and reaches 20 V. On the left side of figure 5.10 the load is switched on exactly at the border of the 24 V time window. The current follows the voltage level and almost no power is dissipated in the high voltage transistor. On the right side of figure 5.10 the load is switched on at the 48 V time window. This effectively doubles the usable operating time. The output voltage of the first stage stays constant at 24 V during the time, the mains voltage is between 24 V and 48 V. Because the load is drawing power during that time the excess voltage is limited by the transistor which generates losses in the transistor.

The simple time window utilized a load of about 48 Ω to produce a mean output power of about 100 mW. The enhanced time window utilized a resistor of 240 Ω to achieve the same mean output power. Simulations showed a maximum current peak of about 400 mA for the simple time window and 80 mA for the enhanced time window. For the simple time window the first stage shows total losses of 30 mW. Of these losses are 16 mW in the rectifier bridge, 6 mW in the high voltage transistor and 8 mW in an additional diode between source of the

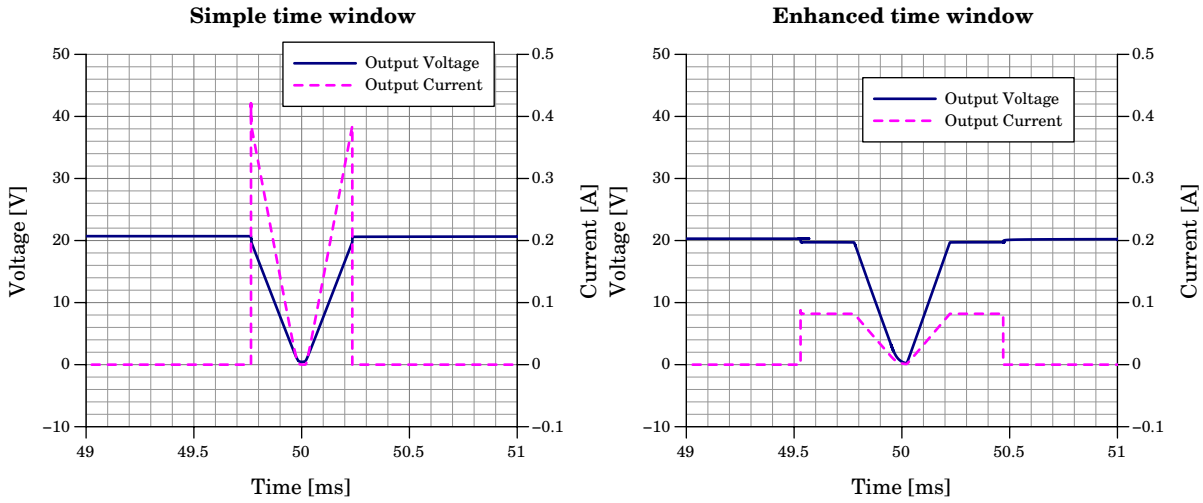

Figure 5.10: Simulation of the first stage operating in linear mode. The left side shows the exact 24 V time window while the right side shows the enhanced 48 V time window. While the output power is the same, the peak current is considerably lower for the enhanced time window.

high voltage transistor and the storage capacitor. This diode is part of the detector circuit that will be investigated later. The used transistor was a Infineon SPA11N60C3 [Inf09]. When a 01N60C3 type with much lower parasitic capacitances is used the losses in the high voltage transistor increase to about 24 mW. For the enhanced time window the total losses are about 75 mW. Of these losses 10 mW are dissipated in the rectifier bridge, 60 mW are dissipated in the high voltage transistor and 10 mW are dissipated in the additional diode. If a 01N60C3 type transistor is used instead of a SPA11N60C3 then the transistor losses increase to 70 mW.

These simulations show that the losses in the first stage are not neglectable. Especially when the enhanced time window is used the losses are considerably higher because of the linear mode of the high voltage transistor. These additional losses may be accepted because of the much lower input current peak. When the simple time window is used a transistor change to a transistor with lower parasitic capacitances has high influence on the losses. If the enhanced time window is used this influence is still there but considerably lower. Figure 5.11 shows the losses that are dissipated in the high voltage transistor during the enhanced time window. While the mains voltage is between 48 V and 24 V the high voltage transistor suffers losses from limiting the voltage. During the time between 24 V and 0 V no losses are dissipated in the high voltage transistor. When the high voltage transistor is controlled as linear regulator, the time window can be configured on demand depending on the power requirements of the load. During standby operation the simple time window can be used while during normal operation the time window could be extended. The limits are given by the power dissipation capabilities of the high voltage switch. This gives the supply the possibility to deliver higher power at the cost of efficiency. This way power peaks of the load that are too big for the storage capacitor could be compensated.

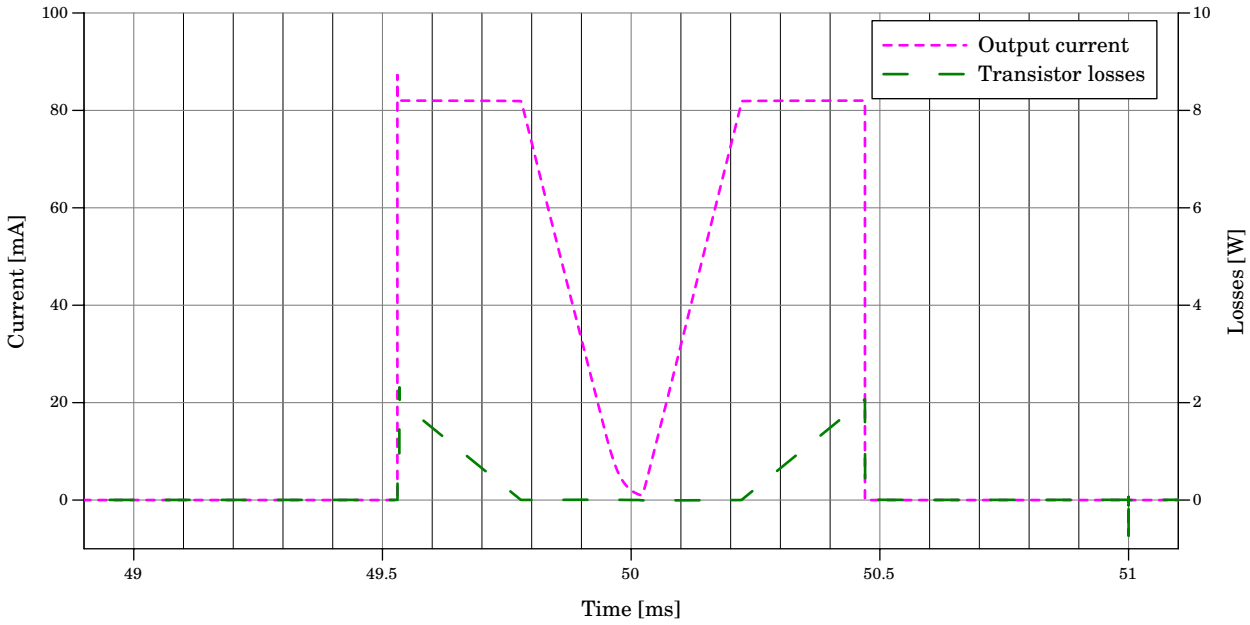

Figure 5.11: Simulation of the losses in the high voltage switch during the enhanced time window. While the mains voltage is between 24 V and 48 V the transistor suffers losses because of tis linear voltage reduction. Within the voltage range of 0 V to 24 V almost no losses are dissipated.

5.5 Detector circuit

The detection of the exact 24 V border of the input voltage sine wave is not trivial for the proposed converter concept. While state-of-the-art zero crossing detection circuits use additional high voltage components to limit the current, the proposed detector has to operate without high voltage components to make integration easier. Additionally the accuracy of the time window is important as the total time window length is only about 235 μs on each side of the zero crossing.

5.5.1 State of the art

There are numerous well known concepts for the detection of the zero crossing of the mains voltage. One of the most important concepts is the concept in figure 5.12.

The resistors R_1 and R_2 are relatively large and limit the input current into the circuit. The bridge rectifier D_1 - D_4 rectifies the mains voltage while the Zener diode D_5 limits the output voltage of the rectifier bridge. The capacitor C_1 is charged up to the Zener voltage of D_5 through the diode D_6. When the mains voltage decreases below the voltage of capacitor C_1, current will flow from C_1 into the emitter of T_1 and out of the base of T_1 through the resistor R_3 into ground. This will cause the transistor T_1 to conduct and the output voltage V_{Det} will be the voltage of capacitor C_1. Hence this circuit will generate a symmetrical time window around the zero crossing that is determined by the Zener voltage of D_5. The power consumption of this circuit depends on the dimensioning of the resistors but usually is about 100 mW.

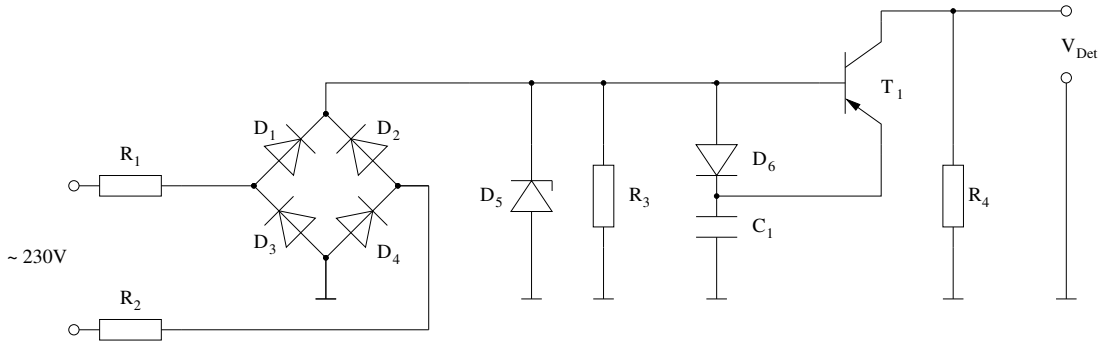

Figure 5.12: State-of-the-art zero crossing detector for mains voltage. The input current is limited through the large resistors R_1 and R_2. This circuit generates a symmetrical time window around the zero crossing.

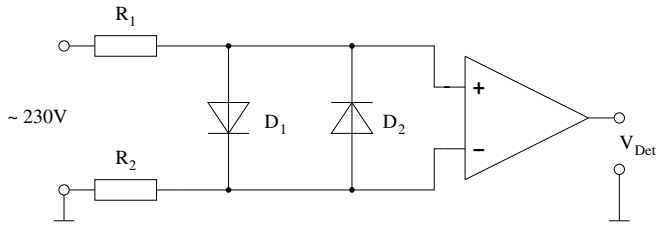

Figure 5.13: Alternative state-of-the-art zero crossing detector. The input current is limited through the resistors R_1 and R_2 while the input voltage into the OPA is limited through the diodes D_1 and D_2 to the forward voltage of these diodes. The output is a rectangular signal with the same frequency as the mains. The mains zero crossing is at the edges of the output signal.

Another highly used concept can be seen in figure 5.13. The relatively large resistors R_1 and R_2 limit the input current into the circuit while the diodes D_1 and D_2 limit the input voltage into the OPA. Sometimes the OPA is even operated with a single not symmetrical supply as the input voltage is not exceeding the forward voltage of the diodes D_1 and D_2. Alternatively, the input pin of a microcontroller may be used in a similar way while one mains line is connected to ground. This zero crossing detector will produce a rectangular signal with the same frequency as the mains while the signal edge is at the zero crossing. Its power consumption is determined by the resistors R_1 and R_2.

5.5.2 Specific problems

The described state-of-the-art detectors have a typical power consumption that is too high for the proposed converter topology. Additionally high voltage components shall be avoided. When the bridge rectifier and the subsequent transistor in figure 5.9 is not connected to a load the parasitic capacitances will make zero crossing detection hard. A major problem for the detector are therefore the parasitic capacitances in the first stage. No power is drawn from the input during most of the mains input voltage cycle. The rectifier diodes as well as the high voltage switching transistor T_1 have parasitic capacitances that are charged up to the maximum rectified mains voltage of 325 V. Through leakage in the circuit this parasitic capacitances are discharged partially but not entirely. The impact of this effect is depending

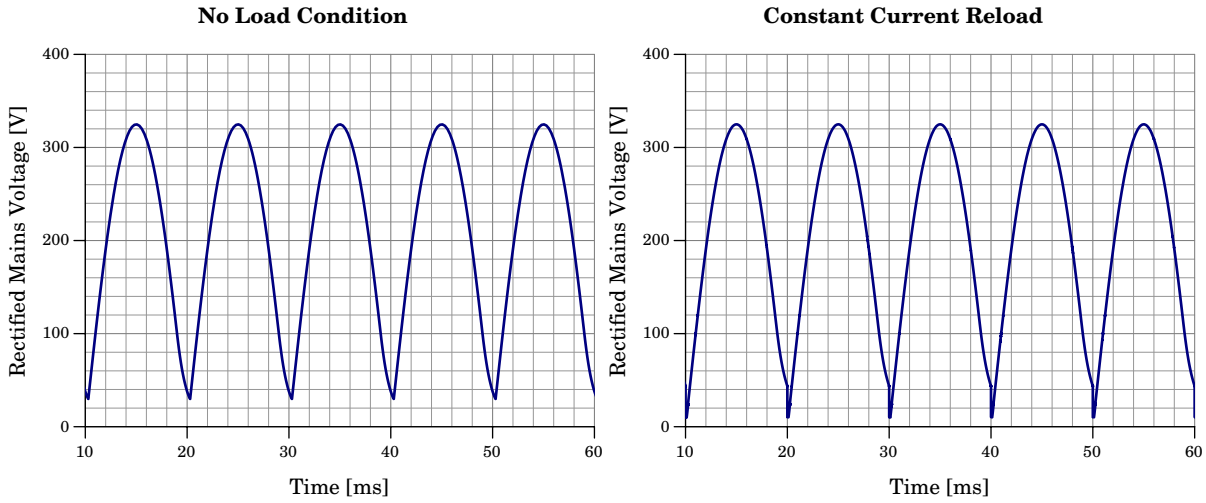

Figure 5.14: Rectified mains input voltage sine wave with a constantly switched off transistor (left) and normal converter operation (right). The parasitic capacitances of the transistor and the rectifiers prevent exact zero crossing detection.

on the used components but a detection of the 24 V border or a simple voltage zero crossing detection for the capacitor reload converter is not trivial and poses some problems when energy efficiency is considered. Figure 5.14 shows this problem in greater detail. The left side of figure 5.14 shows a simulation of the rectified input voltage sine wave while the transistor T_1 is constantly off. Components with low parasitic capacitances were used in this simulation. Because the transistor was off all the time the capacitor voltage was zero. As can be clearly seen the rectified input voltage does not reach the capacitor voltage at any time. The right side of figure 5.14 shows the rectified input voltage when the converter is operating properly. When the transistor is switched on at the zero crossing of the mains voltage the rectified input voltage drops immediately to the capacitor value because the parasitic capacitances are discharged. The zero crossing detector that was used in this simulation uses much power to compensate for the parasitic capacitances and is therefore not suitable for this supply concept.

5.5.3 Proposed detector

The detector of the proposed supply has specific requirements regarding energy efficiency, accuracy and integration efforts. Figure 5.15 shows a first simplified block diagram of the proposed detector. The capacitor C_1 that will be the input capacitor for the second stage is separated from the source of the high voltage transistor T_1 through the diode D_5. The transistor T_1 is operating in linear mode as described in section 5.4. During most of the mains cycle almost no power is drawn from the second stage which allows the capacitor C_1 to stay charged at the designated operating voltage. This voltage at the input capacitor for the second stage is called V_2 for the rest of this work. The voltage directly at the source of the high voltage transistor is called V_1. During most of the mains cycle the source of T_1 and with it V_1 is at about 24 V. V_2 follows V_1 but is reduced by the forward voltage of D_5.

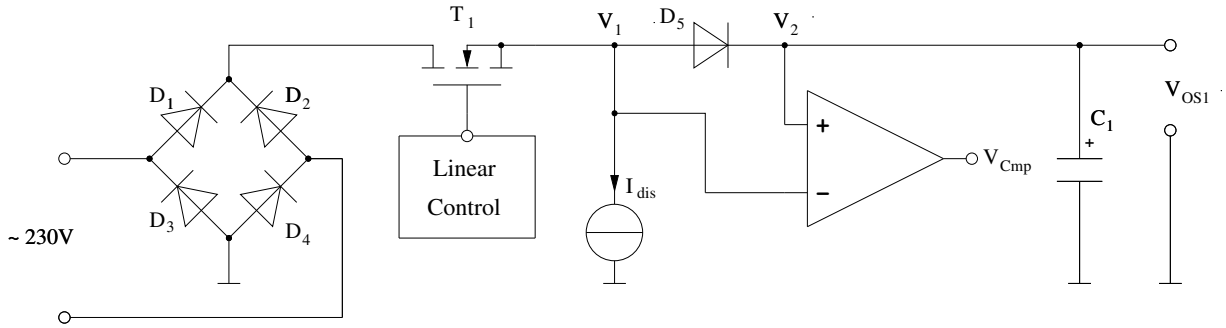

Figure 5.15: Simplified block diagram of the proposed detector circuit. When the voltage V_1 falls below the voltage V_2 the start of the time window is detected. A discharge current I_{dis} is necessary to compensate for parasitic capacitances.

When the input voltage sine wave falls below 24 V, V_1 will fall too but V_2 will stay at 24 V because it is buffered by the capacitor C_1. This will be detected by a comparator that issues a window detect signal V_{Cmp}. So far the operation principle of this detector is very similar to state-of-the-art detector circuits but it can operate without the input resistors. On the other hand the transistor T_1 makes detection hard because of its parasitic capacitances.

The general problem with this detector concept are the parasitic capacitances of the components before the diode D_5. Without countering measures V_1 will not drop enough to ensure detection of the time window. Therefore a discharge current I_{dis} for the parasitic capacitances is necessary. Its magnitude is strongly dependent on the used transistor that has the greatest effect on the parasitic capacitances. Additionally, the discharge current is dependent on the required time window accuracy. Unfortunately the discharge current has to flow through the high voltage transistor and therefore causes linear losses. Figure 5.16 shows a simulation of the detector circuit for different discharge currents and the transistor 01N60C3 [Inf08] that is characterized by low parasitic capacitances.

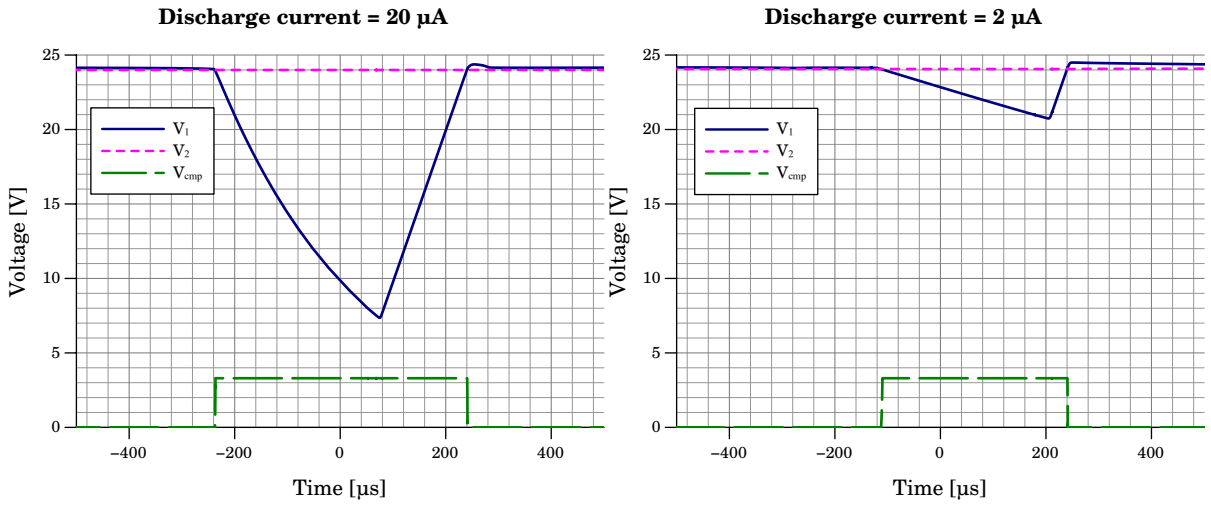

Figure 5.16: Simulation of the time window detection for a discharge current I_{dis} of 20 μA (left) and a discharge current of 2 μA (right). When the discharge current is too low the detected start of the time window suffers a significant delay to the optimum time window start time.

While a discharge current of 20 μA allows a very exact time window detection (left side), a discharge current of only 2 μA leads to a significant smaller time window (right side). The time window is only cut off at the beginning because of the detector delay for a smaller discharge current. The end of the time window is detected exact as the voltage V_1 is rising above the capacitor voltage again. Hence the time window is asymmetrical for a small discharge current.

This effect requires additional enhancements of the detector. When the beginning of a time window is detected the discharge current could be increased to a point where a safe zero crossing detection is possible. This detected zero crossing could then be used for the target application if zero voltage switching is required by the target device the supply is powering. Additional the time from the zero crossing to the end of the time window could be measured. Then a running average could be formed and the discharge current could be adjusted accordingly. This way the discharge current is only significant during the low voltage sections of the mains input voltage which will reduce the detector losses significantly. This especially is important when transistors with a lower on state resistance are used because the parasitic capacitances are accordingly higher. Additional the discharge current I_{dis} could be dynamically adjusted depending not only on the phase of the mains input voltage but also depending on the used high voltage transistor. This would make this detector usable even for larger transistors. The 01N60C3 type transistor would require a static discharge current of 20 μA to allow a very exact time window detection. This would lead to linear losses in T_1 of under 5 mW. This small losses would not require a dynamic discharge current control. The larger transistor SPA11N60C3 that has a considerably lower on state resistance would require a static discharge current of about 300 μA to achieve an accurate time window detection. This would lead to linear losses of about 70 mW only for the detector circuit which is not acceptable. Therefore dynamic discharge control is beneficial especially for bigger transistors as most of the losses in the proposed detector circuit can be prevented.

Alternatively to the OPA concept, the concept with a bipolar transistor can be investigated. Unfortunately this concept has the same problems regarding the discharge current. The accordingly adapted concept can be seen in figure 5.17. It uses the PNP transistor T_2 to detect the time window. Because it is current based and not voltage based as the detector in figure 5.15 it may be less susceptible to EMI noise that could unintentionally trigger the comparator. Additional the comparator circuit itself could be dropped which makes the design simpler. A disadvantage is the additional detector delay as a result of the additional base emitter forward voltage that has to be bridged. The losses due to the current itself are neglectable as they only occur when the mains input is below the operation threshold. Which detector is better suitable for the actual supply design has to be determined through implementation specific simulations.

A detector circuit in this simple configuration is only suitable when no load is switched based on the result of the detector. The detector works by detecting the voltage difference between V_1 and V_2. Whenever the subsequent supply is off V_2 is allowed to fall below V_1, when the mains input voltage falls below a defined border. When a load is then switched on

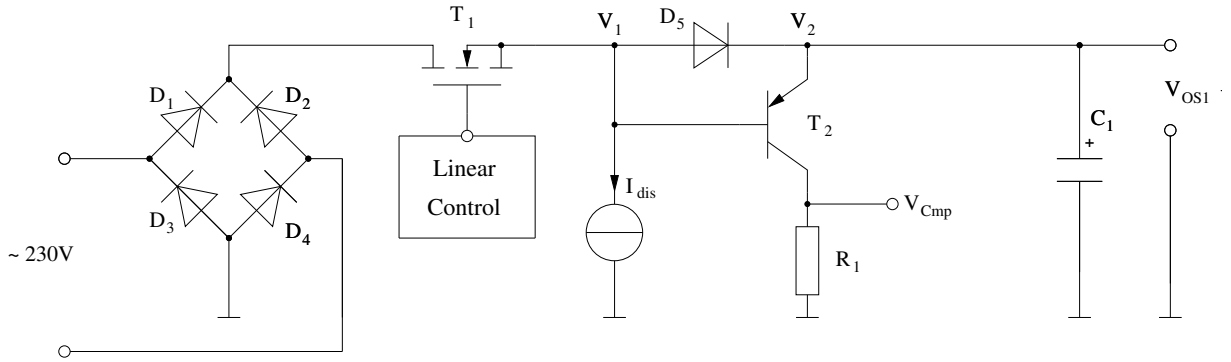

Figure 5.17: Alternative detector circuit utilizing a PNP transistor. When V_1 drops below V_2 the transistor allows current flow and the time window is detected. This design suffers an additional base emitter forward voltage delay but may proof more resistant to EMI.

the capacitor C_1 is immediately discharged to the actual mains voltage minus the forward voltage of D_5. The value of C_1 has to be small in order to avoid a phase delay of the input current to the intended input current. This will cause the detector to switch off the load again and the voltage at C_1 will stabilize at a lower voltage. As soon as the mains voltage falls below this voltage the load is switched on again. This leads to an oscillation which prevents proper time window control of the second stage. The simple detector circuits that are described in figure 5.15 and figure 5.17 are therefore not suitable for the desired application. If an independent high voltage path is used for the detector including the rectifier bridge and input resistors, the detector would work but that is not desired.

To solve this problem another signal has to be generated that can be used to switch off the second stage. Figure 5.18 shows a possible schematic to generate the second control signal. The voltage V_1 is monitored and whenever it is over a specific value the stop signal is triggered. While the activation signal for the second stage is generated by the comparison of V_1 and V_2, the deactivation signal is generated through a fixed voltage level.

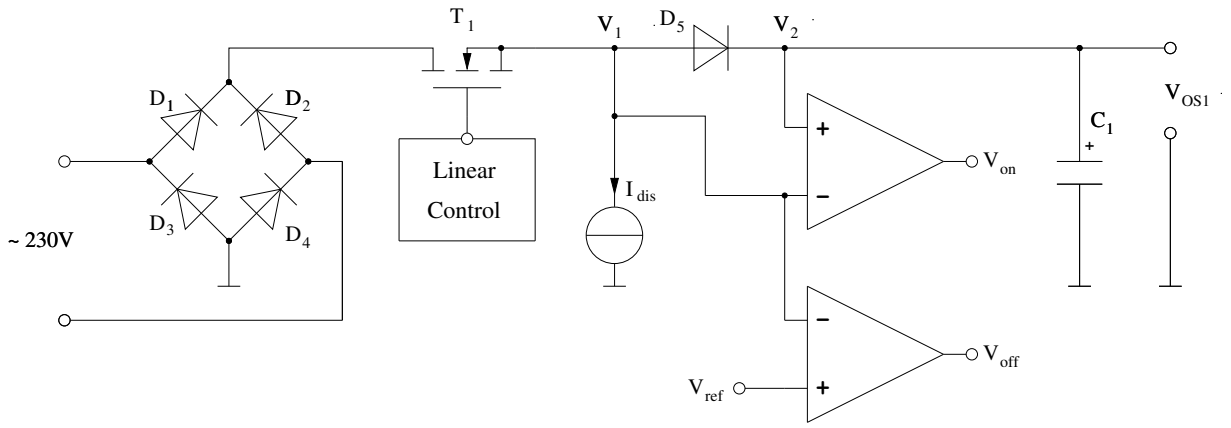

Figure 5.18: Supply with a time window detector utilizing the proposed comparator section. This design can work independent of the load as the start and stop signal for the time window are generated separately. An additional control logic section is necessary to generate the control signal for the second stage.

This deactivation signal brings several disadvantages as a complex control logic is necessary to control the secondary stage. Additional the fixed level has to provide enough margin to use different transistor types as T_1 as the on state resistance may produce an additional voltage drop that has to be considered for the reference level when the supply is running. The switch-on trigger has to be on the rising edge of the signal V_{on} while the switch-off trigger has to be at the falling edge of the control signal V_{off}. This requires at least two storage elements. To ensure reliable and efficient supply operation a subsequent supply control logic section is therefore necessary.

5.6 Control logic for time window control

As described in section 5.5.1 the control signals V_{on} and V_{off} have to be processed by a control logic in order to generate a proper time window control for the second stage. Figure 5.19 shows a control logic that can be used to achieve this task. Two asynchronous RS flip-flops have been used in combination with a few AND gates. The control logic is simple enough to stay asynchronous which brings an advantage in speed and power consumption. Additional the utilization of a dedicated logic section brings further possibilities to extend the time window control and therefore to build a more flexible design.

Figure 5.20 shows a simulation of the proposed detector in combination with the proposed control logic. When the start of a time window is detected through the signal V_{on} the control logic switches on the second stage by activating the signal V_{Ctrl}. This causes the voltage at the input capacitor C_1 to almost immediately drop to the actual mains voltage (reduced by the forward voltage of D_5) which is as a consequence of the detector delay a little lower than the initial capacitor voltage. At the same time the V_{on}-signal is reset to zero so that its only task is to switch on the supply before it is reset again. Shortly after that the V_{off}-signal goes high and the supply is in the designated operating area. The control logic still leaves the subsequent stage enabled. When V_{off} goes back to zero to signal that the mains voltage leaves the safe area the control logic switches V_{ctrl} and with it the second stage off again. The signal V_{off} cannot be used solely to control the second stage as it may not be generated in time without an excessive discharge current I_{dis}which was explained

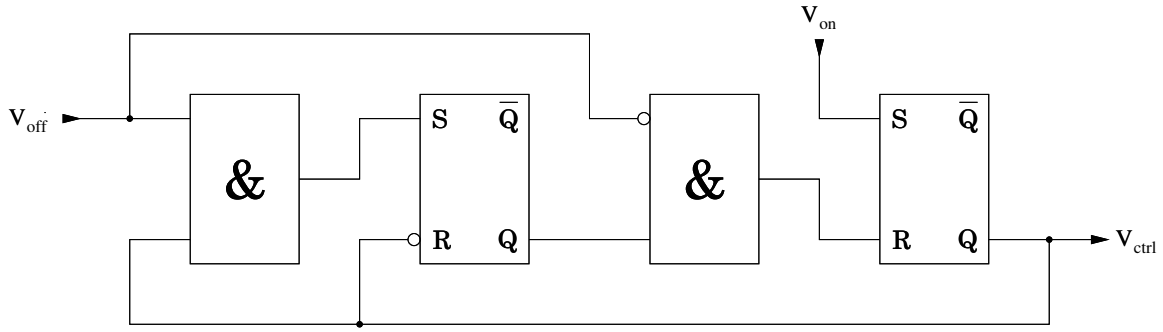

Figure 5.19: Simple control logic for the proposed detector circuit. The control signal V_{ctrl} is generated from the input signals V_{on} and V_{off} that are generated in the comparator section of the detector. Additional logic stages may be added to further enhance supply flexibility.

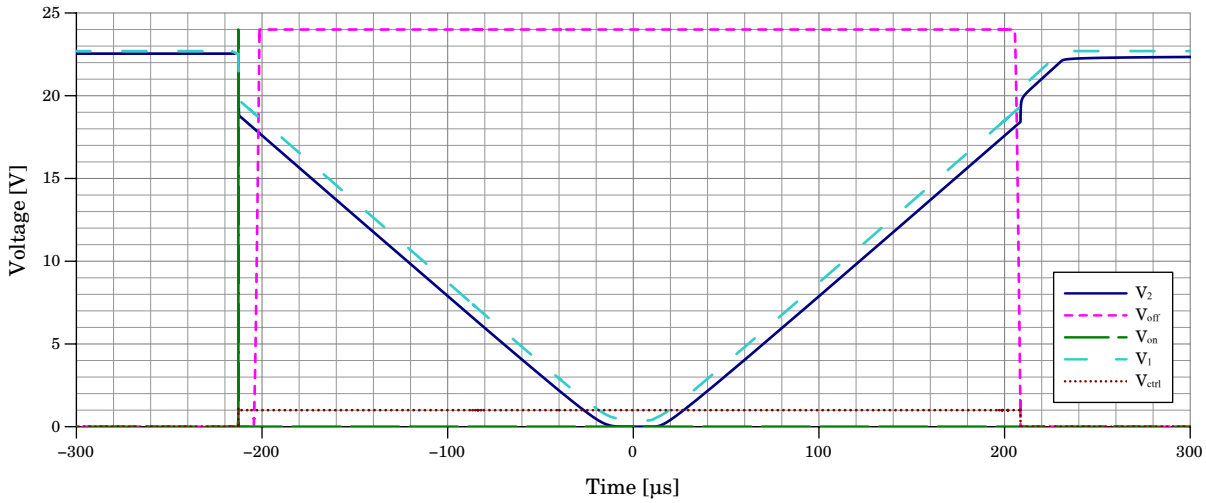

Figure 5.20: Simulation of the proposed supply including the introduced detector and logic section. A short spike of V_{on} brings the control logic to enable the second stage with V_{ctrl} as soon as V_1 drops below V_2. The second stage is switched off again induced by the falling edge of V_{off}.

earlier. After the activation of the secondary supply the discharge current is not necessary any more as the second stage will draw enough power to discharge all parasitic capacitances. What remains, is the voltage step at the switch-off point of the second stage that makes it difficult to define a switch-off voltage level as there are differences depending on the used components. Therefore a margin is necessary to allow for different voltage drops.

Additionally, this gives possibility to enhance the supply for practical use. A first item that could be optimized is the dynamic time window control depending on the load. When the load is greater for a short time interval, the time window has to be enhanced to meet its power requirement. The simplest way to do this is to extend the time window to the right which means to let the supply work for a longer period and dissipate some energy in the high voltage transistor. This could be achieved by monitoring the output voltage of the second stage where the storage capacitor is located. When this storage capacitor reaches its designated voltage level, it is fully charged and the second stage can be disabled. As this can also happen before the time window is over, a fully charged storage capacitor is therefore an additional switch-off condition. A problem would be if the load draws excessive power or the second stage is short circuited. In that case the supply would not switch off as the voltage at the storage capacitor never reaches its designated level. That would destroy the high voltage transistor as a result of excessive linear losses. Therefore an additional safety switch-off mechanism has to be implemented to avoid the destruction of the supply. This is done by a maximum on-time of the second stage which is independent of the actual voltage levels. The logic section can be easily supplemented with the necessary signals. At last the time window that is not symmetric anymore at this time can be shifted to the left to minimize losses by making it symmetric. The actual implementation of the control logic is dependent on the requirements of the second and the third stage as well as the load but a combination of the mentioned control mechanisms has proven successfully.

5.7 Second and third supply stage

After the first stage the subsequent SMPS stages have very specific requirements. On one hand the input to the second stage can be anywhere between 0 and 24 V. Because the capacitor C_S acts as an energy storage capacitor the output of the second stage which is the input of the third stage as well has a very high voltage dynamic ranging from about 12 V to 24 V during normal operation. This requires the second stage to be implemented as a buck/boost stage. The third stage has to deliver a constant output voltage of 3.3 V and can therefore be implemented as a simple buck stage. Figure 5.21 shows the principal schematic of the second and the third stage.

Especially the second stage needs careful consideration as it is operating only for a short period of time with a highly variable input and output voltage. Figure 5.22 shows the typical inductor current near and during the zero crossing of the mains. The supply in this simulation utilizes a rudimentary peak current mode control and operates in critical conduction mode as described in section 3.2.1. Hence the switching frequency decreases for a lower value of V_{OS1}which is the output voltage of the first stage. The second stage stops operation during the zero crossing and restarts when the minimum operation voltage has reached again. Note that the reaction time to the start and stop signals has to be relatively short as the usable time window of the mains input voltage is relatively small. Tests that have been conducted on commercially available state-of-the-art SMPS controllers show various problems when they are operated in the described way. Section 7.2 describes these problems in greater detail.

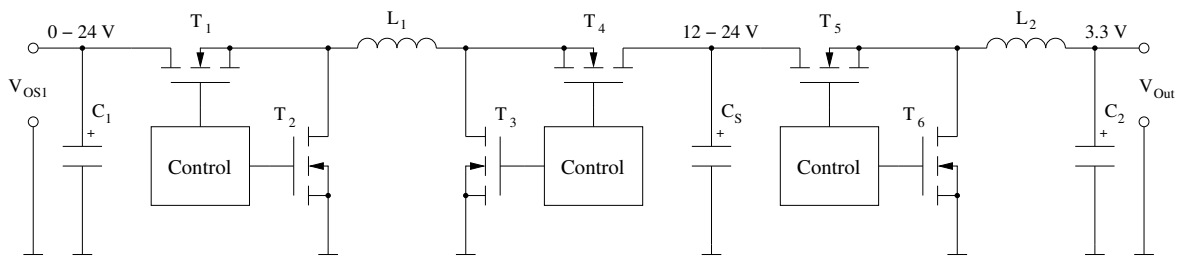

Figure 5.21: The second stage of the proposed power supply consists of the full bridge buck/boost converter (T_1-T_4) and the inductor L_1. The third stage consists of the subsequent buck converter (T_5 and T_6) as well as the inductor L_2.

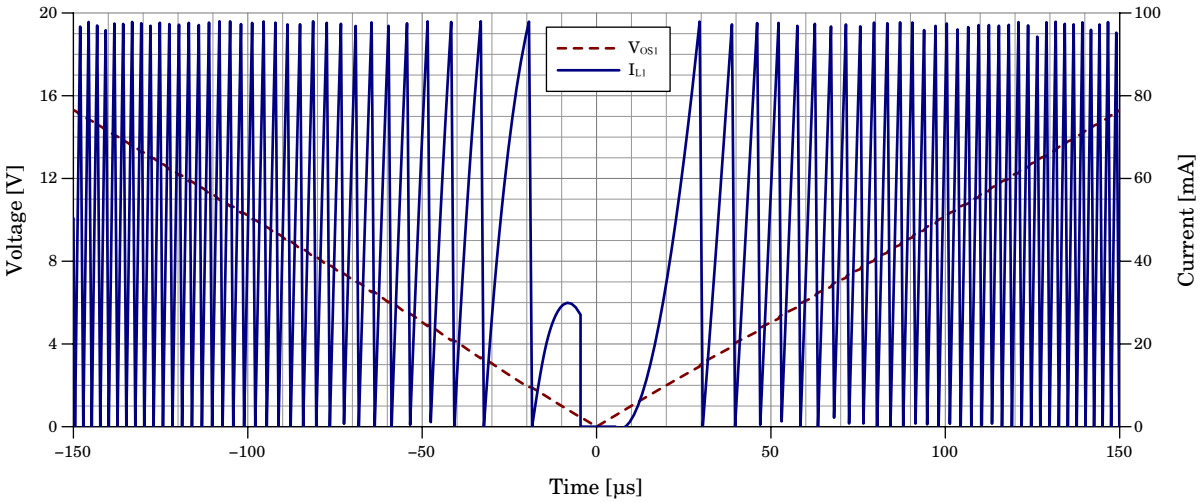

Figure 5.22: Typical inductor current near the zero crossing of the mains voltage. The switching frequency of the converter is smaller near the zero crossing as a result of the decreased voltage which leads to an increased time to reach a fixed inductor current.

6 Supply integration

The goal to finding a cost efficient supply solution can only be achieved by a high integration density. The high-efficient capacitive two stage concept can work as a mostly discrete supply as suitable components are available. However, an integrated version may prove much more cost-efficient when dealing with greater volumes of supplies. Some components as the current limiting X2-type capacitor, the inrush current limiting resistor and the discharge resistor have to sustain the maximum mains voltage which makes integration hard. Other parts as the bridge rectifier, the Zener diode and a sophisticated control circuit to improve efficiency for changing loads can directly be integrated as active parts with the subsequent SMPS control IC. The remaining components can be encapsulated within a system-in-package (SiP). The subsequent section describes a possible integrated capacitive supply solution and presents some simulation results.

While the capacitive approach can work efficiently as a discrete version, the phase controlled SMPS concept has too many drawbacks when it's implemented only discretely. Not only the additional components like the second inductor and the second SMPS control IC make the discrete construction uneconomic but also the control ICs themselves are not designed to work in the necessary operation area. However, a discrete functional demonstrator that can verify the operation principle is possible although it cannot remotely reach the efficiency of an integrated version. This demonstrator is discussed in a later section of this work. This section deals with the possibilities of an integrated version of the phase controlled SMPS concept. A new topology is introduced that is constructed precisely for this application field and can work with a single inductor for both supply stages. Simulation results of this supply topology are presented to show and demonstrate its capabilities.

6.1 Integration possibilities for the capacitive approach

The integration potential of the capacitive supply starts mainly after the current limiting capacitor C_1. The current limiting capacitor itself as well as the current limiting resistor R_1 and the discharge resistor R_2 may be uneconomic to integrate because of their high voltage rating as well as the safety regulations regarding the X2-type capacitor. Fortunately all other parts of the supply are low voltage parts during normal operation. Figure 6.1 shows the block diagram of the proposed integrated capacitive power supply controller. C_1 is the current limiting X2-type type capacitor and R_2 its discharge resistor. R_1 is the inrush current limiting resistor. D_5 is only necessary to protect the IC against overvoltage peaks during operation and to protect the IC during the initial startup. T_1-T_4 is a self driven synchronous rectifier circuit which replaces D_1-D_4 in the discrete version. Note that this self driven synchronous rectifier topology was specifically designed to work with the rest of this capacitive supply control IC and cannot charge a buffer capacitor directly. T_5 and its control logic operate as configurable shunt regulator in order to replace the Zener diode D_5 of the discrete version. Hence T_5 regulates the auxiliary voltage V_{aux} steplessly with respect to the needed power and limits the voltage to a maximum. This operation gives an efficiency

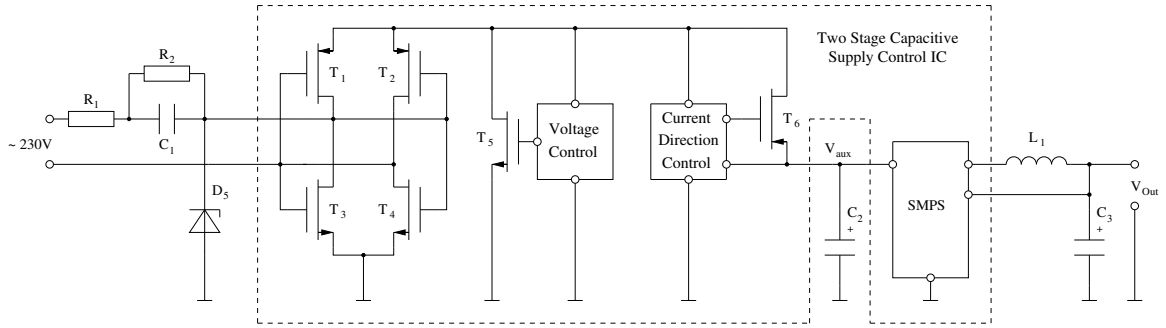

Figure 6.1: Proposed power supply IC for a two stage capacitive supply suitable to power wireless sensor and control nodes consisting of the self driven synchronous rectifier T_1 - T_4, the auxiliary power control T_5 and a decoupling circuit for the buffer capacitor C_2.

advantage as the auxiliary voltage can be lowered when the load is not drawing maximum power which results in a better efficiency in the second stage SMPS. Precautions have to be taken that when the load draws maximum power after a long sleep period, enough power is left in the buffer capacitor that the supply can switch back to high power mode. This is also an issue during the startup of the supply which will be handled later. T_6 and its control logic has the responsibility to decouple the auxiliary buffer capacitor C_2 from the first stage. This is necessary because of the transistor T_5 which can lower the voltage or even short it to switch the supply into a lower power or standby mode. If the capacitor C_2 is not decoupled it would be discharged. It is also necessary because of the special self driven synchronous rectifier which is used in the first stage. Current would flow back to the bulk diodes of the used transistors when the capacitor C_2 is not decoupled accordingly. The second stage is a standard SMPS buck controller which can be integrated into the same IC.

The startup of this supply has to be considered carefully. During the initial startup the control logic of the supply is not powered and therefore not operational. During normal operation the control logic is powered from the auxiliary voltage. Because the used synchronous rectifier is self driven, it will work during startup. The control logic of T_5 has to come up in a way that the gate of T_5 is low when the control logic is not powered which is usually no big problem. The control logic of transistor T_6 on the other hand would have to hold the gate of T_6 at its source potential during startup to switch it off and prevent current backflow into the bridge. The current can flow into the buffer capacitor C_2 through the body diode of T_6 during startup. However, it is possible to hold the gate of T6 at ground during startup if the control logic reliably starts to work before V_{aux} reaches the threshold voltage of T_6. Because the threshold voltage is variable with various parameters, it is usually not a good idea to rely on a specific value as this may result in an unstable design. Another point has to be considered when designing the control logic of T_6. Simply drive the gate voltage to ground when the transistor has to switch on may exceed the maximum allowed gate-source voltage when the auxiliary voltage is chosen too high. Figure 6.2 shows the simulated startup of the first stage of the supply in figure 6.1.

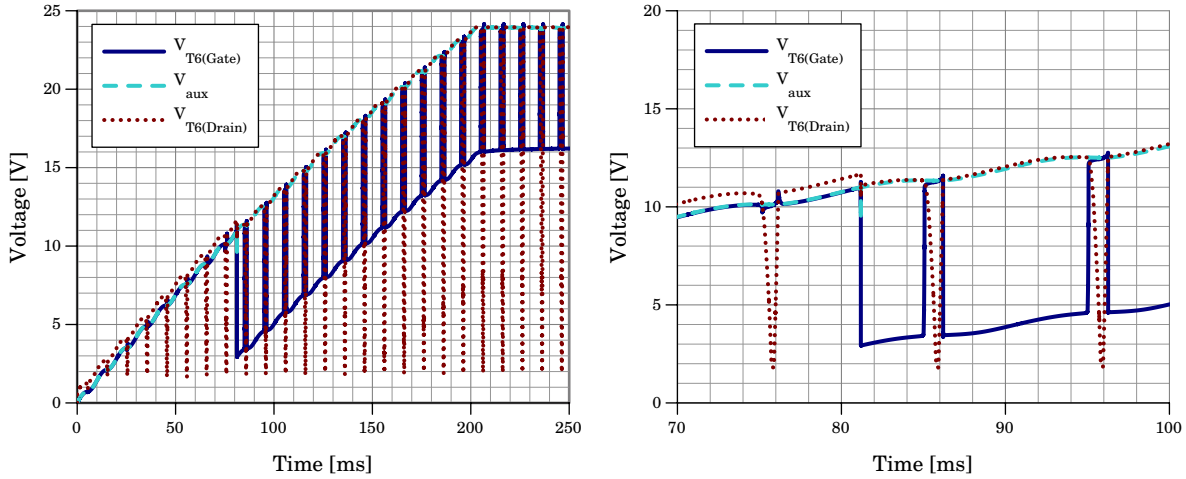

Figure 6.2: Simulation of the startup of the proposed circuit in figure 6.1.

The supply is dimensioned for an auxiliary voltage of 24V and an auxiliary output current of 10 mA. The left diagram in figure 6.2 is showing the whole startup procedure. The level of V_{aux} is reaching its designated value about 200 ms after the supply is switched on. The control logic starts about 80 ms after the supply is switched on. The gate voltage on transistor T_6 is generated with respect to the actual auxiliary voltage level. The right diagram in figure 6.2 is showing the startup of the control logic in greater detail. The voltage after the self driven synchronous rectifier bridge $V_{T6(Drain)}$ is falling down periodically with the mains frequency. During the startup when the control logic is off, the current flows through the body diode of T_6 into the buffer capacitor C_2, raising the auxiliary voltage. The forward voltage of the body diode can clearly be seen in the right part of figure 6.2 as the difference between $V_{T6(Drain)}$ and V_{aux} during the time the control logic is still off. This would produce power loss of about 70 mW. After the control logic is powered and active, transistor T_6 is switched on and the forward voltage drop disappears. Every time $V_{T6(Drain)}$ drops below the auxiliary voltage V_{aux}, transistor T_6 is switched off again to prevent current backflow through the bridge.

When dimensioning the startup behavior of the second stage one have to keep in mind that the first stage is powered by a current source. That means that the power the primary stage can deliver depends on the actual auxiliary voltage level. During startup and after a restart when the supply was in standby mode, the auxiliary voltage rises and with that the maximum power output capability. When the secondary stage starts too early to draw power, the auxiliary voltage can not rise because the current that should be used to charge the capacitor C_2 is used by the second stage. Additionally the second stage will draw even more current in order to meet the output power requirement because of the low auxiliary voltage. This may lead to a breakdown of the auxiliary voltage to a point where the second stage can no longer operate. Then the whole process starts again. To prevent this, the second stage has to make sure not to draw any power till the auxiliary voltage is at a certain level. Also when the primary stage is switched off temporarily to save power and the energy in the

buffer capacitor C_2 is used, the auxiliary voltage cannot drop below a certain point because the supply would not be able to recharge the capacitor C_2 again. A temporary interruption of the target supply would occur till C_2 is recharged which would probably reset the target system.

6.2 Integration possibilities for the SMPS-based approach

The main drawback of the described new phase-controlled SMPS converter topology are the two inductors that make integration harder. Additionally, state-of-the-art buck/boost control ICs are typically not constructed to operate within the needed operation parameters. Especially the startup behavior as well as the startup time, the off-state current and the minimum operation voltage which is caused by the integrated direct supply of the control logic are a big issue. Therefore a new converter topology is proposed that can solve this issues and can work with a single inductor for its two SMPS stages. This new topology is then simulated and evaluated for the utilization in standby power supplies for smart appliances.

6.2.1 Power feedback SMPS

As explained in section 5.7 the necessary second and third stage in the proposed phase-controlled SMPS topology requires an individual inductor which makes integration more difficult. A solution to this problem is the proposed new power feedback SMPS topology that combines the second and the third stage by creating a power feedback loop through the storage capacitor C_S. The energy storage capacitor therefore can act as an energy source or an energy sink depending on the actual operation state of the supply. Energy packets can be loaded into the inductor either from the output of the first stage or the energy storage capacitor. The inductor can transfer its energy either directly to the output or to the energy storage capacitor. The decision of the proper source and destination of the energy packet can be made for each energy packet independently and can even be changed during the energy transfer process. Figure 6.3 shows the schematic of the proposed supply.

By utilization off a full bridge the design is most flexible. While T_1 is the input transistor from the first supply stage, T_2 is the input transistor from the storage capacitor. T_5 is the output transistor to the energy storage capacitor C_S while T_6 is the output transistor to the load. C_1 is a very small input capacitor and poses as a filter for the HF. The capacitor C_2 is the buffer capacitor for the load and can be relatively small as the energy is stored in the energy storage capacitor C_S. The energy transfer speed from the input to the output is critical as the usable time window is limited and the supply has to transfer as much energy as possible as constant as possible. This is especially a problem as the inductor is time shared between two inputs and two outputs. A similar problem occurs in the normal full bridge converter. Whenever the input and the output voltage are similar the current slope in the inductor will be smaller as the voltage difference will be smaller. Therefore it takes longer to load an energy packet into the inductor. This effect was described in section 3.2.4 in

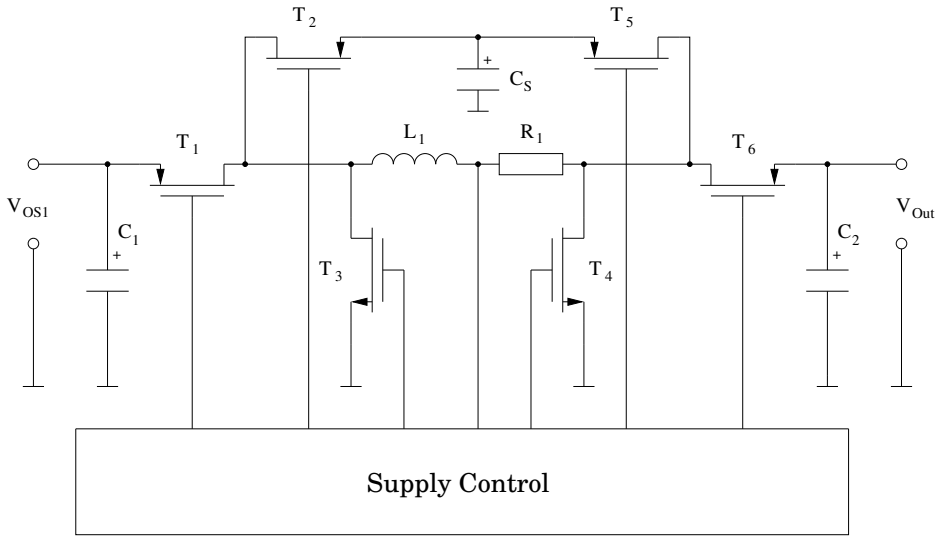

Figure 6.3: Principal schematic of the proposed power feedback SMPS topology. Energy is stored in an energy storage capacitor C_S during the usable mains time windows and is used to reload the output capacitor C_2 outside the time windows to ensure a constant output voltage.

greater detail as it marks the transition from buck to boost mode. State-of-the-art controller ICs overcome this problem by special control algorithms [GN04, ONS+11]. The controller IC that was used in the discrete HW prototype had such mode transitions but they may have been not very efficient for the fast changing input voltage. This supply topology could also benefit from these control algorithms making it more efficient. For the basic simulations in this section a relatively simple diagonal transistor control was utilized as the main focus was the energy packet distribution control. The diagonal transistor control that was used in this simulation will ensure a good power transfer ratio without first determining the necessary supply mode which may cost time. There are four main operation states of the supply as well as a standby state.

The first operation state marks the energy transfer from the output of the first stage V_{OS1} into the inductor. This operation state is initiated whenever the mains input voltage is within the usable voltage range and the control logic issues an energy request for either the output capacitor C_2 or the energy storage capacitor C_S. The current is flowing from the input and the input capacitor C_1 through the transistor T_1 into the inductor L_1 and from there over the current sense resistor R_1 over the transistor T_4 into ground. Figure 6.4 shows the current path during this operation state. The transistor T_1 and T_4 are turned on, all other transistors are off. After the inductor reaches the designated maximum current the transistors T_1 and T_4 are switched off and the energy is transfered either into the output capacitor or the energy storage capacitor.

The energy storage capacitor is the alternative energy source for the supply. Another operation state marks the transfer of an energy packet from the energy storage capacitor to the inductor. This operation state is issued by the control logic whenever the output capacitor has to be reloaded and no mains voltage is available which is most of the time.

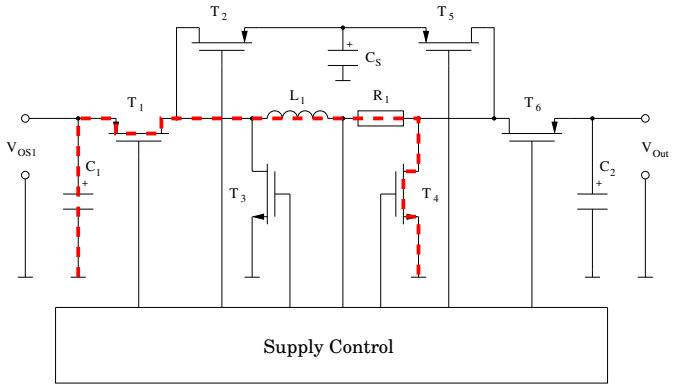

Figure 6.4: Current path for the load phase of the inductor from the mains. The current is flowing from the input over the transistor T_1 into the inductor L_1 and from there over the current sense resistor R_1 and the transistor T_4 into ground. The inductor current is increasing in this operation state.

The transistors T_2 and T_4 are turned on which allows the current to flow from the energy storage capacitor C_S through the transistor T_2 into the inductor and from there over the current sense resistor and the transistor T_4 into ground. Figure 6.5 shows the current path for this operation state. After the inductor reaches the designated maximum current the transistors T_2 and T_4 are switched off and the energy is transfered into the output capacitor. An energy transfer back to the energy storage capacitor is possible too but makes no sense unless the output voltage reaches the maximum value during the energy transfer. In that case the energy is diverted back to the energy storage capacitor.

The next operation status marks the energy transfer into the output capacitor C_2. Whenever the supply has loaded energy into the inductor and the control logic determines the output capacitor requires reloading this operation state is entered. Current flows from ground via the transistor T_3, the inductor and the current sense resistor R_1 through transistor T_6 into the output capacitor C_2. Figure 6.6 shows the current path for this operation state. The transistors T_3 and T_6 are switched on until the current in the inductor reaches its minimum

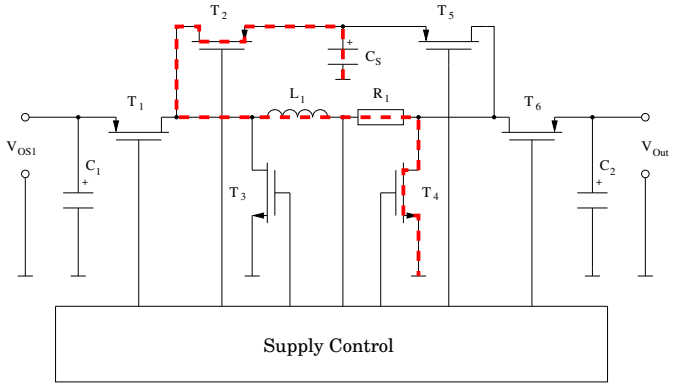

Figure 6.5: Current path for the load phase of the inductor from the energy storage capacitor C_S. The current is flowing from C_S over the transistor T_2 into the inductor L_1 and from there over the current sense resistor R_1 and the transistor T_4 into ground. The inductor current is increasing in this operation state.

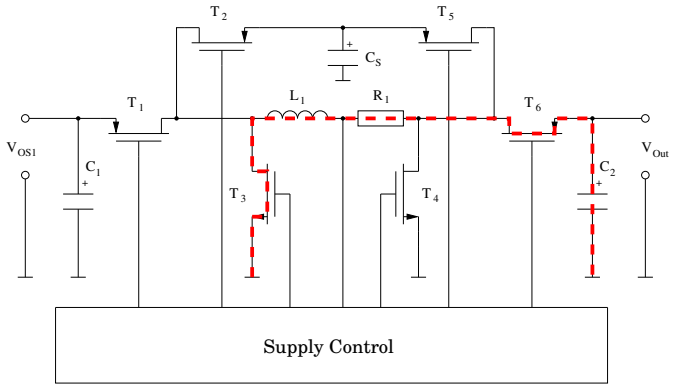

Figure 6.6: Current path for the unload phase of the inductor into the output capacitor C_2. The current is flowing from ground over the transistor T_3 into the inductor L_1 and from there over the current sense resistor R_1 and the transistor T_6 into the output capacitor C_2. The inductor current is decreasing in this operation state.

value. When more energy is required, another energy packet is loaded into the inductor.

Another operation state marks the energy transfer from the inductor into the energy storage capacitor C_S. This operation state is entered whenever energy is stored in the inductor and the output capacitor C_2 is fully loaded. Current flows from ground through transistor T_3 over the inductor and the current sense resistor R_1 through the transistor T_5 into the energy storage capacitor C_S. Figure 6.7 shows the current path for this operation state. The transistors T_3 and T_5 remain on until the current in the inductor reaches its designated minimum. When more energy is requested for the output or the energy storage capacitor another packet is loaded into the inductor. If no more energy is requested, the switches T_3 and T_5 stay on until the inductor current reaches zero and then they are turned off.

The final operation state during normal operation is standby. When no energy is requested for the output capacitor or the energy storage capacitor the supply is in standby mode. Additionally the supply is in standby mode when energy is requested for the en-

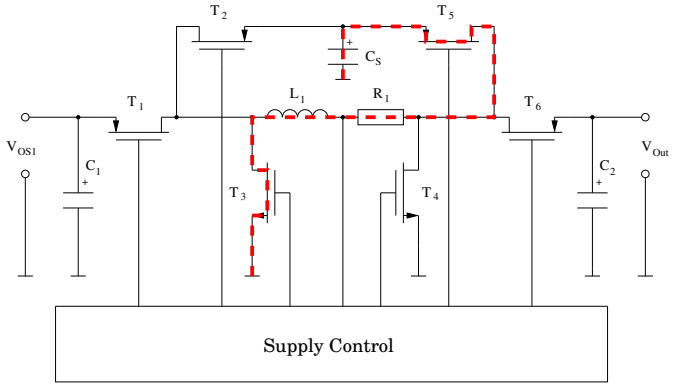

Figure 6.7: Current path for the unload phase of the inductor into the energy storage capacitor C_S. The current is flowing from ground over the transistor T_3 into the inductor L_1 and from there over the current sense resistor R_1 and the transistor T_5 into the energy storage capacitor C_S. The inductor current is decreasing in this operation state.

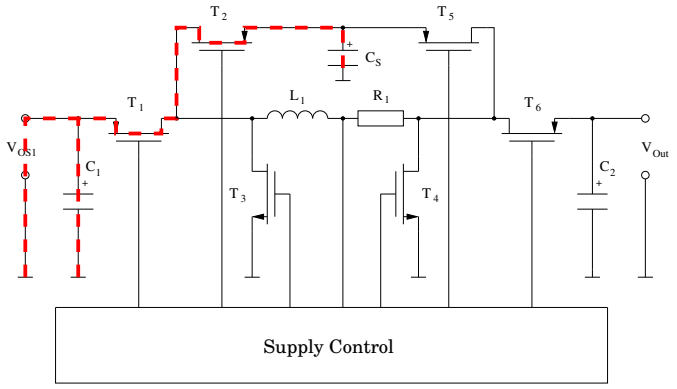

Figure 6.8: Current path for the direct capacitor reload configuration. The transistors T_1 and T_2 are switched on during the zero crossing of the mains and the capacitor C_S is reloaded during the rising voltage slope of the mains to the designated maximum voltage.

ergy storage capacitor C_S but no energy is available from the output of the first stage as the mains voltage is out of the time window. In standby mode all transistors are off as no current is stored in the inductor and no energy is requested.

The proposed supply structure can also be used for a simple capacitor reload control mode. In this case the input capacitor C_1 is removed or reduced to a minimum. Energy is taken from the storage capacitor to reload the output capacitor C_2 during normal operation. During the zero crossing of the mains the transistor T_1 and T_2 are switched on which connects the energy storage capacitor C_S directly to the mains while it is reloaded through the mains voltage slope. After C_S reaches its designated voltage level T_1 and T_2 are turned off again and normal supply operation continues. Note that C_1 is connected to C_S during this state which will produce additional losses if C_1 is present. Figure 6.8 shows the current path for this additional operation state.

The power-feedback SMPS concept shares a single inductor to short-term store energy within a higher voltage energy storage capacitor when input energy is available, while simultaneously maintaining a constant load voltage. While a dedicated second and third stage can work independent of each other and therefore theoretically operate continuous, the power-feedback SMPS has to alternate between the two tasks which leads to a time scheduled operation. Figure 6.9 shows the current budget of the energy storage capacitor C_S and the output capacitor C_2 depending on the usable mains time window. Positive current means the capacitor is charged and its voltage is increased while negative current means that the capacitor is discharged.

As the output capacitor provides a constant output power of 100 mW at a nearly constant output voltage of 3.3 V an output current of about 30 mA is required. This output current can be seen as negative current offset of I_{C2} in figure 6.9. Whenever the output voltage drops below a predefined value the supply has to replenish the output capacitor. This task has the highest priority as the supply has to guarantee a constant output voltage for the load. Outside the usable mains time window this is the only task as the energy to recharge the output capacitor C_2 comes from the energy storage capacitor C_S. The recharge process of C_2

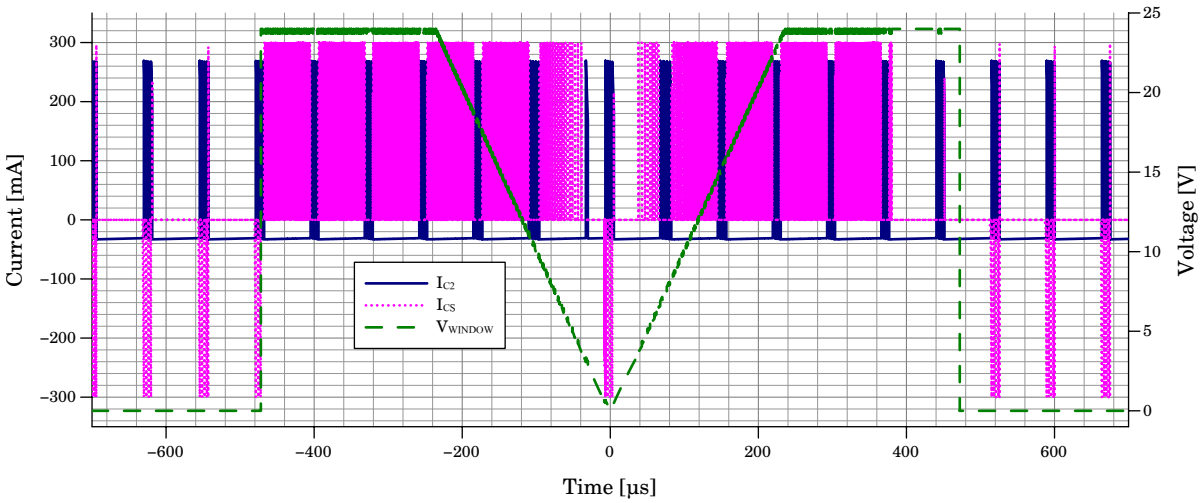

Figure 6.9: Current budget of the proposed power feedback SMPS topology. Outside the time window the output capacitor C_2 is reloaded from the energy storage capacitor C_S. During the time window both capacitors are recharged from the mains while C_2 has higher priority.

can be seen in figure 6.9 as small positive bursts of I_{C2}. As the energy to recharge C_2 comes from C_S outside the usable mains time window the recharge bursts of C_2 go along with negative discharge current bursts I_{CS} of the energy storage capacitor C_S. Between these bursts the supply is inactive. The time window in figure 6.9 starts during a recharge burst of C_2 at about 470 μs before the zero crossing at 0 μs. During the ongoing recharge burst the energy source is switched from the energy storage capacitor to the mains input which can be seen in figure 6.9 as the discharge burst of C_S stops immediately at the begin of the time window while the recharge process of C_2 is still ongoing. After C_2 is replenished the supply starts to recharge the energy storage capacitor C_S from the mains as now is the usable time window which can be seen as longer positive current bursts of I_{CS} in figure 6.9. The recharge process of C_S is interrupted by an energy request signal for the output capacitor C_2 which has a higher priority as the output voltage has to stay constant at all time. This fact is the reason why the whole time window cannot be used to replenish C_S as C_2 also has to be recharged repeatedly during the time window. Because the time window has to be longer for a higher output power as more energy is needed within the energy storage capacitor, additional time is lost because of the necessary recharge of C_2 which is also longer for a higher output power. Therefore the length of the time window goes quadratic with the output power for the power feedback SMPS design. This can be compensated on the other hand by allowing a higher peak current which will shorten the necessary current bursts. At the zero crossing of the mains there is no mains energy available and therefore if the output capacitor C_2 has to be recharged during the zero crossing the energy source has to be again the energy storage capacitor which can be seen in figure 6.9 at 0 μs. After the mains voltage reaches a minimum again the recharging process of C_S continuous. When the energy storage capacitor is fully recharged (which has to happen during the time window otherwise the supply cannot work for long) the only remaining task is the frequently recharge of C_2.

The energy for this comes again from the mains during the remaining time window which conserves power in the energy storage capacitor. After the end of the time window C_2 is recharged from the energy storage capacitor again. Note that it is important to select a time window length and a recharge current that allows a complete recharge of the energy storage capacitor during the time window at maximum load with a sufficient margin. In an advanced design the time window can be re-centered for the next cycle which will increase efficiency. Additional the end of the time window may be adjusted dynamically dependent on the energy state of the energy storage capacitor. In other words the time window will be cut off when the energy storage capacitor is replenished and centered over the zero crossing at the next cycle. This will allow most efficiency while maintaining good flexibility.

A problem that has to be properly managed by the supply control is when the control logic requests energy for the output capacitor C_2 during the time window while the mains voltage is relatively low or at the zero crossing. As the time window is active the energy should come from the mains. Because the mains voltage is low, the phase that loads current into the inductor is longer which leads to a lower switching frequency. This can (especially in combination with the further falling mains voltage) lead to an output voltage drop. To prevent this, the energy source has to be switched to the storage capacitor whenever the inductor current load time is too long which is the case near the zero crossing. The proper reaction of the supply can be seen in figure 6.10 at the inductor current I_L and the output voltage V_{C2}. .An energy request for the output capacitor is issued about 20 μs before the zero crossing. The inductor current cannot reach the defined peak value in time as the mains voltage drops further. This will cause the supply to recharge the output capacitor C_2 with a burst from C_S before it switches back to the mains. After the output voltage is back in a safe area but the output capacitor C_2 is still not fully recharged the supply switches back to the mains and tries to draw power from there. As can be seen in figure 6.10 the

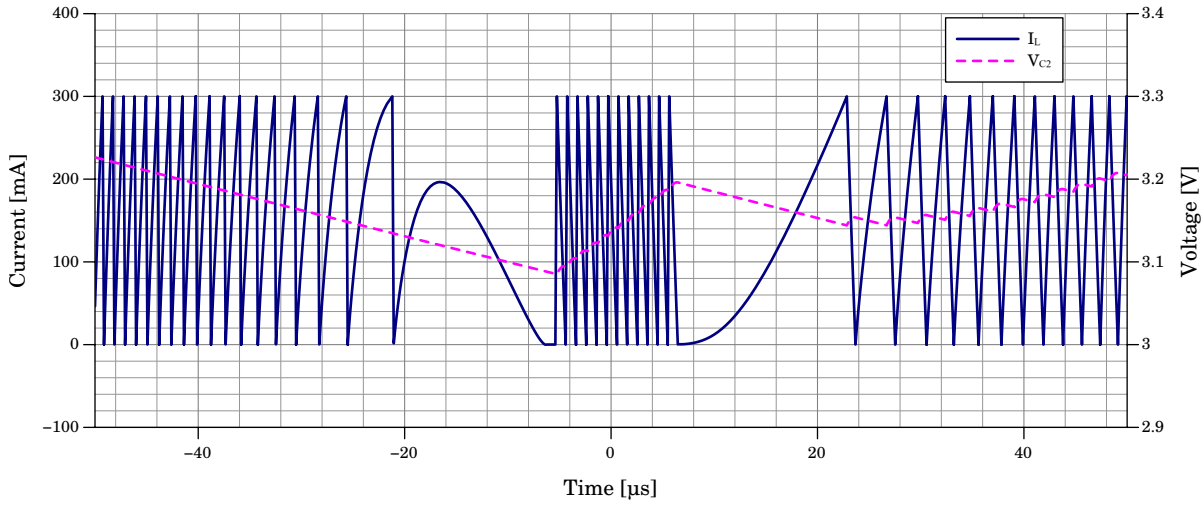

Figure 6.10: Recharge of the output capacitor C_2 during the zero crossing. When the mains voltage is near the zero crossing and C_2 needs to be reloaded the energy is taken from the energy storage capacitor C_S even if the time window is still active.

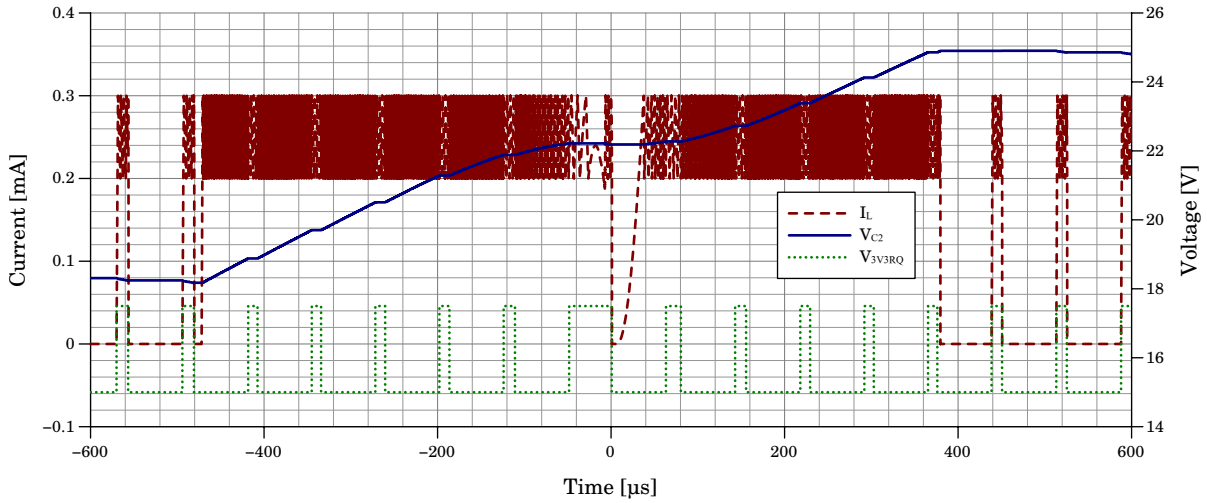

Figure 6.11: Recharge process of the energy storage capacitor C_S during the time window. The recharge process is interrupted by energy demand signals for the output capacitor which has higher priority. The supply is configured for CCM operation in this simulation.

output voltage drops again after the recharge burst during the zero crossing because the current reload phase into the inductor still takes very long as a result of the still low mains voltage. But the output voltage doesn't drop so far that another recharge burst from C_S is issued. As the mains voltage rises again the current reload into the inductor gets faster and the switching frequency increases, which allows the supply to replenish C_2 from the mains.

Figure 6.11 shows the recharge process of the energy storage capacitor $C_S$with a different current setup. The supply is setup to have a minimum inductor current of 200 mA and a maximum inductor current of 300 mA during operation which increases the energy transfer ratio. When the supply is in standby mode the inductor current drops back to zero. The voltage signal V_{3V3RQ} is the recharge request signal for the output capacitor C_2. Whenever this signal is present the supply stops recharging the energy storage capacitor because it has to recharge the output capacitor C_2 which can be seen as a short period of constant voltage at the energy storage capacitor (V_{CS}) in figure 6.11.

The proposed supply topology including the proposed control principles could be used in an integrated supply. To further improve the efficiency potential enhanced control algorithms could be used that further differentiate the supply states. For example at a momentary input voltage of 20 V the transistors T_1 and T_2 could switch on to load energy into the inductor as well as into the output capacitor the same time. These operation states can be entered whenever the input and the output voltage are not close. Additionally an advanced time window control as described earlier is probably necessary in an actual supply.

The delay between the enable signal and the begin of the switching operation that has been found in the discrete HW demonstrator is mainly caused by some parts of the SMPS control IC that are powered down during standby to save power. While this is normally a good idea it poses a problem in the proposed supply topology. As the integrated version of the supply has to operate all the time to ensure proper output voltage and the internal

supply control is powered from the energy storage capacitor the proposed integrated version will not have this delay problem as no circuitry has to be powered up prior to the recharge phase of the energy storage capacitor C_S.

6.2.2 System in package integration

Figure 6.12 shows a block diagram of a possible integrated variant of the proposed supply. It consists of a high voltage section which holds all high voltage parts and a low voltage section for the rest. In this case the high voltage section consists of the bridge rectifier, the high voltage transistor and an additional diode for an integrated capacitive startup circuit to supply voltage to the gate of the high voltage transistor. The current limiting capacitor that would otherwise be necessary within this startup circuit was substituted with a diode circuit which may simplify integration. The low voltage section holds the proposed detector, the proposed power feedback SMPS as well as a reset circuit and a linear internal power supply to ensure proper operation.

This new approach may be a possibility to power smart appliances during standby. The design has the potential to reach higher efficiencies than normal designs as smaller switching transistors and therefore higher switching frequencies could be used. This advantage can be seen especially for the simple capacitor reload method as no combined second and third stage is necessary and the current requirements on the inductor are relatively low. The disadvantage of relatively high pulsed input current is also the highest for the simple capacitor reload method. Through the usage of a symmetrically controlled time window this disadvantage can be minimized. However the design gets more complex and depending on the actual control method the losses increase. The practical usage of this supply in the field may be very limited as a result of the relatively high current peaks.

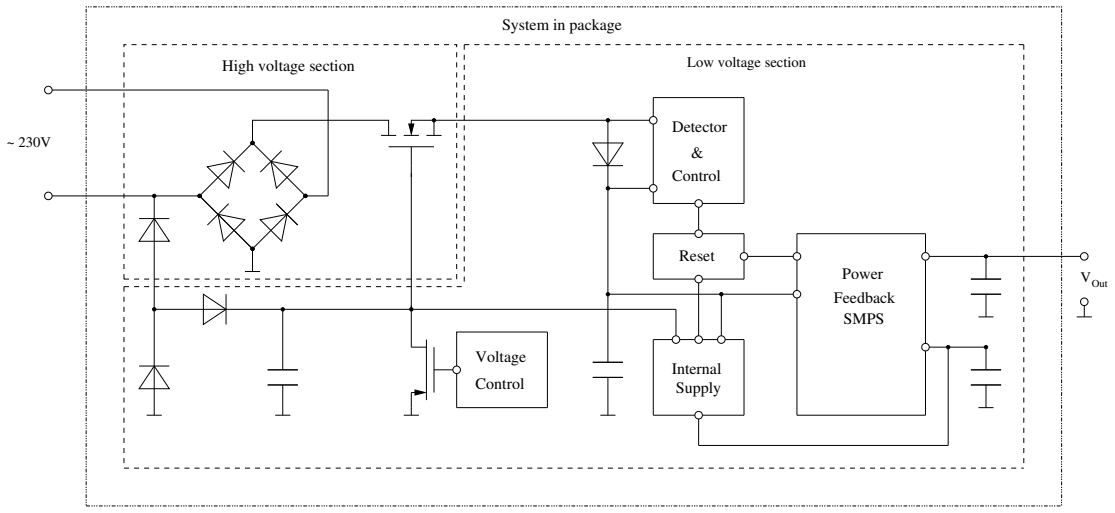

Figure 6.12: Block diagram of a possible integrated version of the proposed power supply. The high voltage section houses the bridge rectifier as well as the high voltage transistor while the low voltage section houses the detector, the power feedback SMPS as well as some auxiliary blocks.

7 Experimental supply demonstrators

After extensive analysis and simulations this section deals with the practical evaluation of the described supply types. For that purpose a discrete two stage capacitive supply was integrated into the SmartCoDe nodes as part of the SmartCoDe project. These nodes have power requirements that are similar to a typical wireless sensor node or a smart appliance in standby mode. These nodes were then deployed at a remote test site as part of a wireless sensor network. This section discusses the experience from this test.

As the phase controlled SMPS concept is not operating efficient without the described integrated power feedback SMPS it was not included in practical field tests. However, a functional HW prototype was created to validate the design idea and to further investigate this supply concept. This prototype uses state-of-the-art available SMPS control ICs to construct the second and the third stage. The results and measurements are then discussed within this section.

7.1 Practical evaluation of the two stage capacitive supply

After the two stage concept with a high voltage primary capacitive supply and a succeeding SMPS converter has been identified as the most promising candidate out of the capacitive supply concepts a labor prototype was built to verify this supply topology. Following the successful prototype tests, a field test was planned to evaluate the practical applicability of this supply concept in a wireless sensor and control node. This field test was done within the SmartCoDe project.

7.1.1 Evaluation setup

After careful simulations and a labor prototype that approved the principal two stage capacitive supply concept, the supply was integrated into the functional discrete PCB prototype of a SmartCoDe node. This SmartCoDe node was then switched in between the mains supply and selected household appliances like freezers or washing machines. Several of this nodes were deployed at a special test site. Every node had to monitor the energy consumption of its load and report it back to a base station over a ZigBee network. Additionally every node had to switch the load on or off with respect to various parameters such as the actual energy price, with the goal to save energy and therefore money. Figure 7.1 shows the functional overview of a SmartCoDe node. Figure 7.2 shows a picture SmartCoDe node that was deployed on the test site.

The power supply of the described SmartCoDe node was built as a single rectifier version because the used power meter had to operate from the same ground as one of the mains lines. The supply was designed for an auxiliary voltage of 44 V and an output power of about 100 mW. The output power was increased to about 200 mW during the test period. The second stage of the supply was designed for an output voltage of 3.3 V. Additional voltage levels were needed for the power meter (5 V) and the DALI bus interface (12 V).

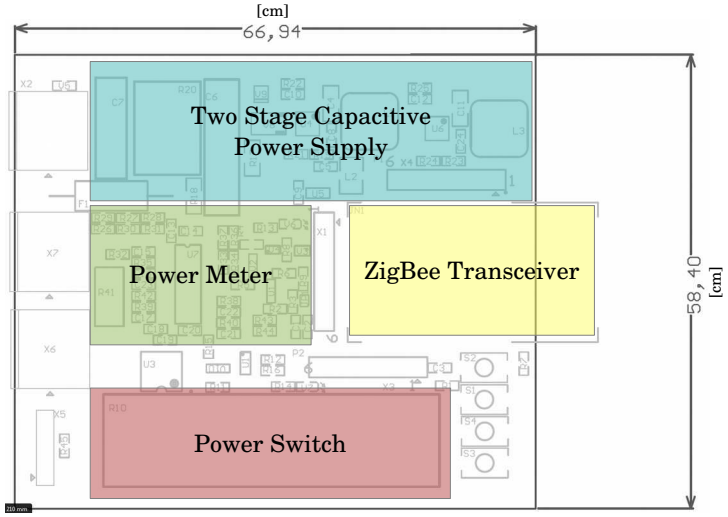

Figure 7.1: Functional Overview of a SmartCoDe Node. The power supply block provides the power for the node and is connected to the mains. In this case a two stage capacitive power supply was used. The ZigBee transceiver is responsible for the communication of the node. The power meter measures the power consumption of the attached household appliances and the power switch can switch the connected appliances on or off.

Figure 7.2: Picture of a SmartCoDe node and its casing.

7.1.2 Results of the evaluation

During the activation and the maintenance of the nodes over a period of a few months at the test site, know-how regarding the operation of the used supply type was acquired.

Flexibility Over the course of the test, the application was extended and new features were added to the system. This had influence on the power requirements and required an update of the power supply in order to deliver more power. An update was easily possible by changing the main X2-type capacitor to a higher value without changing the rest of the supply. This change had no influence on the auxiliary voltage or the rest of the supply.

Power fluctuations Short power fluctuations were observed at the test site that caused the SmartCoDe node to reset. In the first run the auxiliary buffer capacitor was too small to handle this small blackouts. After the buffer capacitor size was increased, the node could handle power failures of up to 1 s.

EMI Some of the nodes were switching old and power demanding freezers. After the switching of this inductive load, some nodes sometimes experienced a reset that was caused by a failure of the second supply stage. After recreating this situation in the laboratory the reason for the power failure could be found. A voltage peak of about 55 V at the input of the second stage triggered the over voltage lockout function of the used SMPS controller (LTC3642). To resolve this problem a few strategies were pursued. The first step was to enhance the layout of the SMPS circuit to reduce EMI vulnerability. Additionally the auxiliary voltage was lowered to have a greater buffer for overvoltage peaks at the second stage. Finally additional line filtering was applied to ensure reliable operation of the supply even in rough operation scenarios.

System stability Because of unannounced power failures in connection with the described problems in an early test phase, some nodes became unstable and stopped to work. Some nodes lost the connection to the network and were unreachable, others completely stopped operation. Hence the software was adapted to handle and log unannounced power failures that can even occur during normal operation when the user unplugs a device.

7.1.3 Conclusion

After taking care of the problems mentioned above, the supply worked as expected. Anyway when designing a capacitive two staged supply for a wireless sensor and control node, the environment has to be considered. For an actual field deployment sufficient margins have to be considered to ensure the reliable operation of the supply under any circumstances. In case power fails for any reason, even if the user unplugs the device unannounced, the system has to startup in a clear defined way when power comes back.

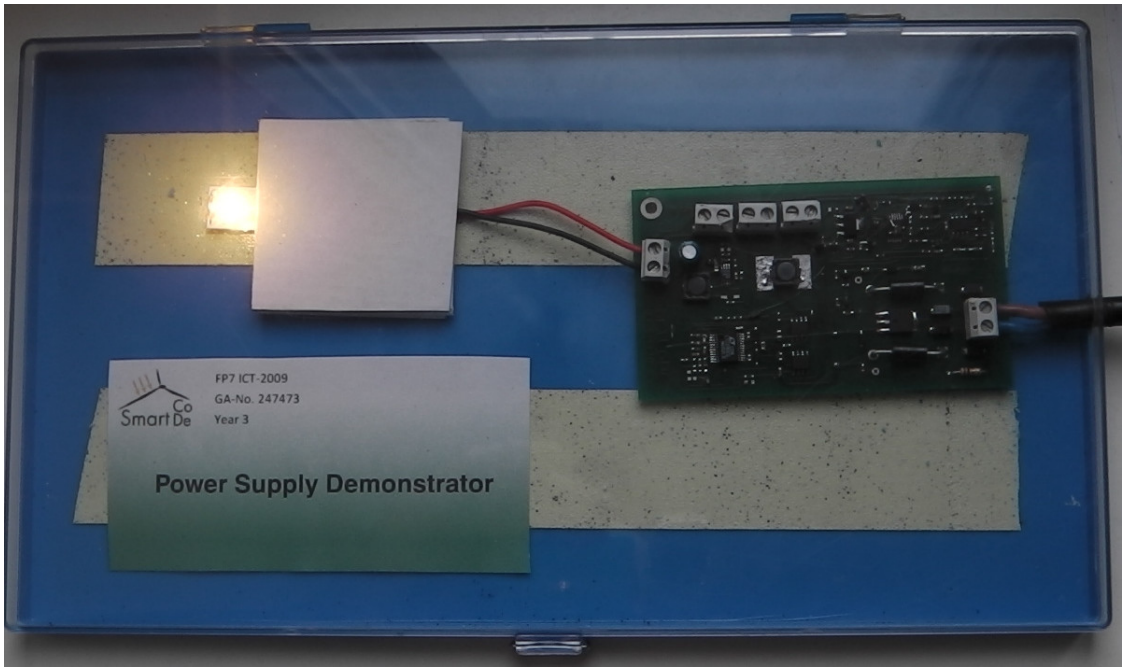

Figure 7.3: Functional HW demonstrator of the proposed power supply operating a LED at 100 mW output power.

7.2 Discrete hardware demonstrator for the new phase-controlled SMPS concept

After theoretical considerations and simulations a functional HW demonstrator was designed to further investigate the proposed supply concept. The main goal behind this demonstrator was to identify possible problems with the supply concept in general, to verify the time window detector, to identify a reasonable time window control algorithm, to determine a proper startup circuit and to investigate if state-of-the-art SMPS control ICs could be used as second and third stage. Figure 7.3 shows a picture of the working HW demonstrator while supplying 100 mW of output power to a LED. Figure 7.4 shows the prototype in greater detail while dividing it into subsections.

7.2.1 High voltage section

The high voltage section is the primary stage of the supply. When looking at the circuit in figure 5.18 the high voltage section consists of the bridge rectifier (D_1 - D_4), the high voltage transistor T_1, the diode D_5 and the small capacitor C_1. The gate of T_1 is supplied by a small and simple ultra low power shunt regulator that is powered from the input. No efforts were made to shift the gate power source to the output after startup to further save power. Additionally the functional demonstrator has been equipped with two big TVS (transient voltage suppressor) diodes to protect the supply during commissioning and during experiments with the control circuit. Also a 1 Ω shunt resistor was included for measuring purposes and as an intentional weak link that is destroyed in case of a supply failure. When experiments

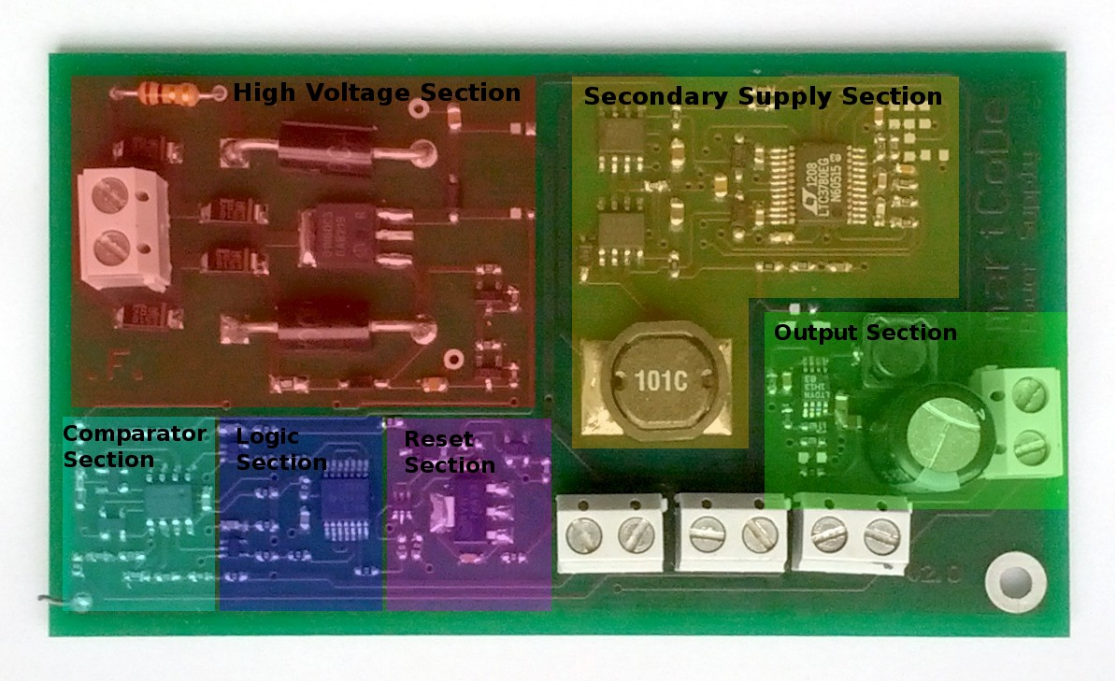

Figure 7.4: Functional HW demonstrator divided into the main sections. The high voltage section is the first stage of the supply. The comparator and the logic section house the detector and the time window control. The reset section ensures proper startup. The secondary supply section is a full bridge buck/boost converter while the output section is the third supply stage which is a simple buck converter.

with the control circuit cause an overload of the transistor T_1 the typical failure scenario is a short between drain and source of T_1. In that case the TVS diodes limit the output voltage of the first stage till the shunt resistor blows. Hence in case of an error only the HV transistor and the shunt resistor have to be replaced instead of every semiconductor on the PCB. The only outputs of the high voltage section are the voltages V_1 and V_2 (compare figure 5.18). The implementation of the high voltage section in the functional HW demonstrator was straight forward and did not require any special measurements.

7.2.2 Comparator and logic section

The next sections that were implemented were the comparator section in combination with the logic section. These two sections are responsible for the time window detector and the generation of the control signal for the next supply stage. The comparator section consists mainly of the circuit that was introduced in figure 5.18 but with additional voltage dividers at the input of the comparator to limit the input voltage to under 3.3 V and to add some flexibility for experiments. The logic section was first implemented as described in figure 5.19. Unfortunately this logic section was unable to adapt the time window in order to react on different output power requirements of the supply. Therefore first the voltage at the energy storage capacitor was included as input into the control logic. Hence, the switch-off event was generated depending only on the output voltage of the capacitor C_S (compare

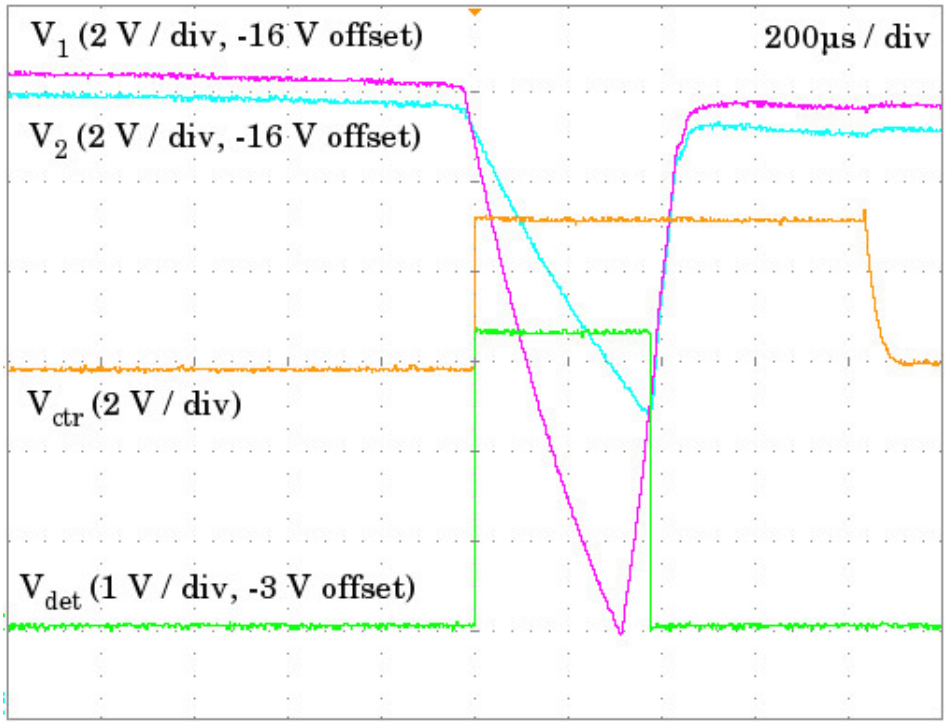

Figure 7.5: Oscilloscope measurement of the detector and the time window control during no-load operation of the functional HW demonstrator. The control signal V_{ctr} that controls the second stage is active longer than the detected time window to ensure a complete reload of the energy storage capacitor.

figure 5.21). This led to a highly flexible operation as the supply was generating longer time windows for a higher output power level and shorter time windows for a lower output power. Unfortunately this led to an overload of T_1 when the power requirements were too high or the output was shorted. Additionally this overload occurred when bigger energy storage capacitors were used at the first startup as the capacitor is completely empty. To solve this issue an additional maximum time window length was introduced into the control logic. Figure 7.5 shows a measurement of the detector operation on the functional HW demonstrator at no-load operation. V_1 and V_2 come from the high voltage section (compare figure 5.18). As soon as V_1 goes under V_2 the start of the time window is detected. V_{det} represents the detected time window while V_{ctrl} is the actual control signal to the second stage. After the time window is detected the control signal V_{ctr} goes high and stays high even after the end of the regular time window. That is because the second stage is disconnected and therefore the energy storage capacitor is empty. The length of the actual time window is limited through the maximum time window length which forces V_{ctr} down after about 850 μs to avoid a potential overload of T_1 even if the energy storage capacitor still needs energy.

Figure 7.6 shows the functional HW prototype under normal operation at full load. V_{out} is the output voltage of the supply which is at 3.3 V. V_{ctr} is the control voltage for the second stage converter. V_{CS} is the voltage at the energy storage capacitor. Figure 7.6 is not showing any irregularities.

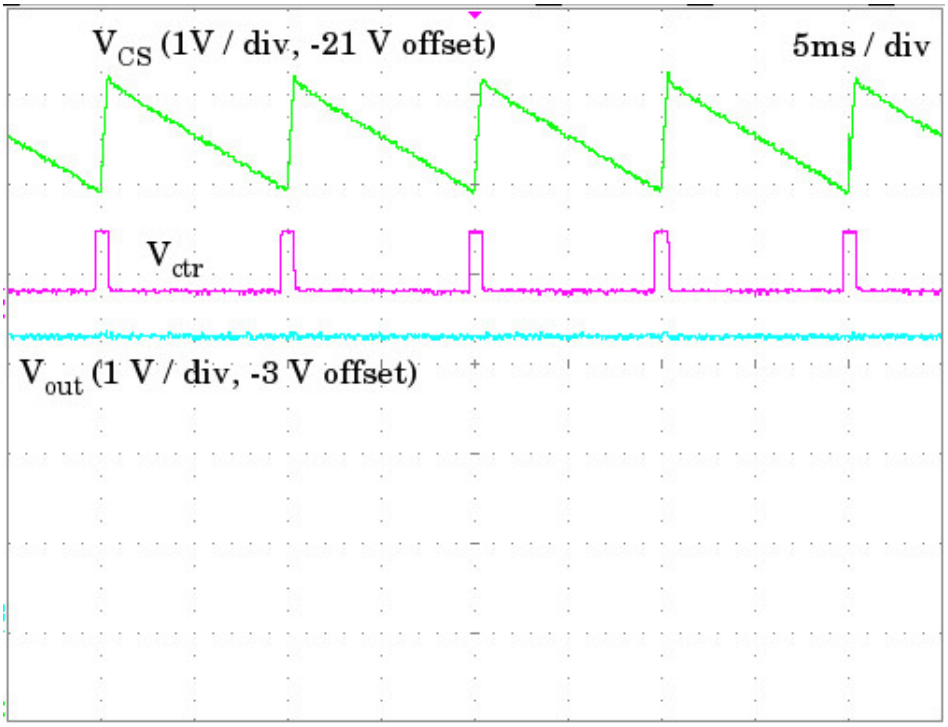

Figure 7.6: Normal operation of the functional HW demonstrator of the proposed supply at an output power of 100 mW at an output voltage of 3.3 V.

In figure 7.7 the input current of the discrete HW demonstrator can be investigated. As the mains zero crossing is at the center it is clearly evident that the time window is not symmetric and that almost all of the input power is drawn after the zero crossing. As the detector works perfectly, the reason for this behavior has to be related to the second stage as well as its input voltage which will be investigated next.

7.2.3 Second converter stage

To further investigate this behavior figure 7.8 shows the reload of the energy storage capacitor C_S after the second stage is enabled. Additional the inductor voltage is shown. As expected the reload procedure is happening only in the second half of the time window which is after the zero crossing. The first reason for this is the delay between the enable signal for the second stage and the begin of its actual switching operation. Figure 7.8 shows a delay of about 60 μs which has also been measured at numerous other setups. A few full bridge buck/boost converter ICs have been investigated on their startup time. Unfortunately this parameter is not a standard parameter in converter IC datasheets. The used LTC3780 had the fastest reaction time to the enable signal. Unfortunately these 60 μs still cost about 6 V of the usable time window. This fact substantiates the need of a new control IC for this application that can react faster. The next problem that is related to the control IC is its integrated soft start. The datasheet recommends a minimum soft start capacitor of 6.8 nF which would lead to a startup of 1.5 ms in which the supply gradually drawing more power

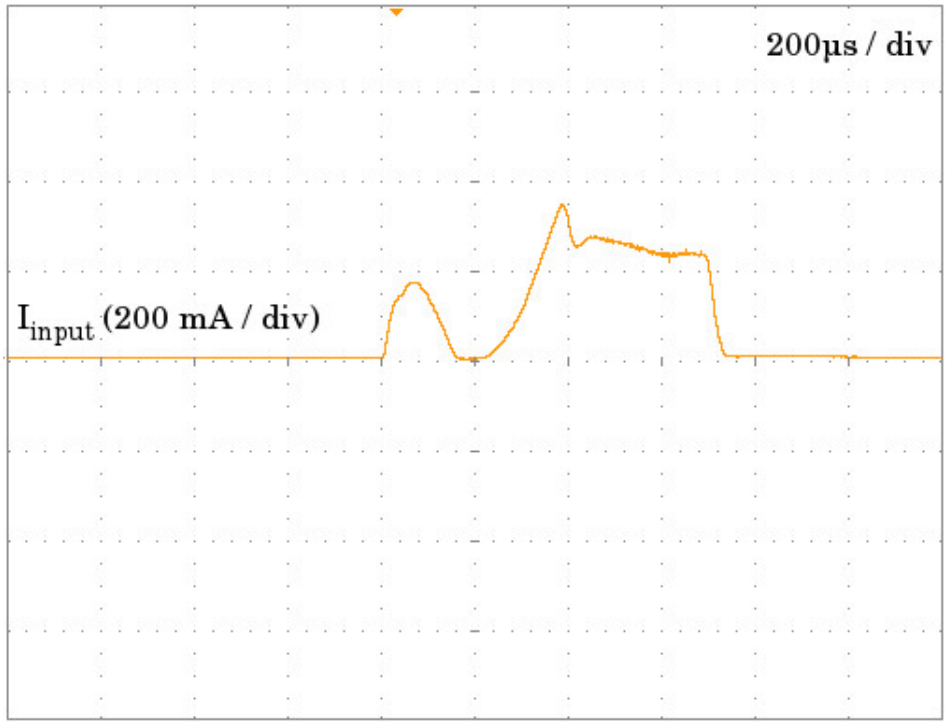

Figure 7.7: Input current of the functional HW demonstrator. The time window is asymmetric and most of the power is transfered after the zero crossing. This is caused through various effects originating mainly in the second supply stage.

up to its designated operating point. As the time window is considerably shorter this is a serious problem. Even when the soft start capacitor is completely removed which is not recommended, the supply has a considerable soft start which leads to further delay. Another problem could be circumvented by the selection of a bigger energy storage capacitor. To limit the current at a short circuit of the output the supply limits the inductor current progressively to up to 30 % of its designated maximum. This limitation starts if the output of the supply that is powering the energy storage capacitor is falling 30 % of its nominal value. To avoid this the capacitor voltage cannot drop 30 % of its designated value which makes the usage of a bigger capacitor necessary. The last problem that is related to the control IC of the second stage is the minimum input voltage. Whenever the input voltage drops below 4 V the supply is reset and a new soft start event is initiated. An external power supply for the control IC could not significantly lower this limit. Although the used control IC for the second stage is far from optimum it still was a good choice as other state-of-the-art control ICs have even worse characteristics. Especially the turn-on delay is a problem with most converters. These problems could be eliminated and additionally the second and third stage could be combined with a specialized control IC solution.

In the end there is only a small voltage region left that can be utilized at the falling slope of the mains voltage. Unfortunately even this small voltage region cannot be used properly in the used setup configuration for the discrete HW demonstrator. For safety reasons the supply was connected to the mains over an isolation transformer that has considerable in-

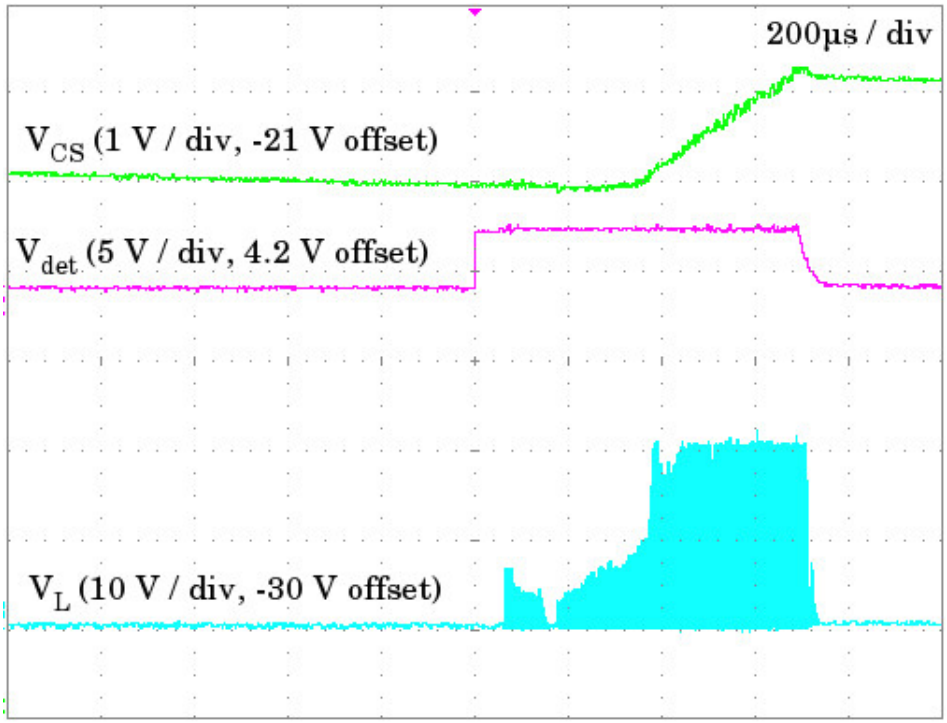

Figure 7.8: The reload of the energy storage capacitor is done in the second half of the time window. A 60 μs delay after the edge of the enable signal to the begin of the switching operation as well as a low inductor voltage are two reasons. An additional reason is the soft start circuit that is included in the used SMPS control IC.

ternal resistance (about 4 Ω on the secondary side and about the same at the primary side) as well as considerable leakage inductance. This causes a small voltage breakdown of the mains voltage when the second stage starts to draw power that partially recovers. In figure 7.9 this effect is marked with a red circle. Note that no filter capacitors are used for this measurements. Filter capacitors could eliminate the mains disturbance at the second half of the time window but could not counter the partial voltage breakdown. On the other hand, the standard IEC60725 [CEN] states that the public supply net is considered to have an impedance of 0.4 + 0.25j at 50 Hz in the worst case, which would be a resistor of 0.4 Ω and a series inductance of about 800 μH. That would dramatically lower the voltage breakdown in comparison to the utilization of the isolation transformer, but a similar breakdown could be caused by a large number of parallel nodes. A more realistic estimation of the public supply net can be made by looking at the used mains power transformers. A typical energy distribution transformer has a power rating of about 500 kVA which means about 750 A rated current per phase. The typical leakage inductance is about 5 %. This would lead to a maximum short circuit current of about 15 kA. With respect to the 230 V mains voltage at 50 Hz this leads to a mains impedance of about 15 mΩ which translates to an inductivity of about 50 μH. Because this parameter is depending not only on the used energy distribution transformer, but is also influenced by the distance to the feed point it is highly variable with the location. Anyhow, the typical public mains is much better than the worst case that is

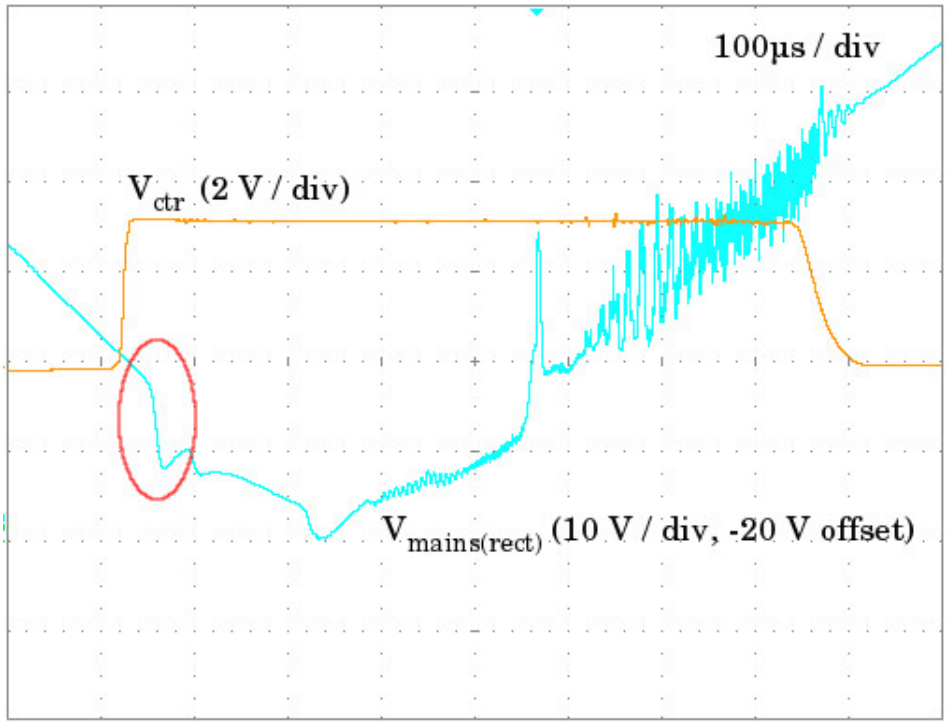

Figure 7.9: Partly temporal mains voltage drop caused mainly by the high impedance of the isolation transformer. This effect decreases the usable voltage range of the input mains voltage.

stated in the standard IEC60725, let alone the used isolation transformer. This leads to the conclusion that the supply will have a much better performance when used without an isolation transformer. Future tests will have to clarify possible conducted EMI on the mains as well as an efficiency reduction due to the described voltage breakdown.

Figure 7.10 shows in addition to figure 7.9 the output voltage of the first stage V_{OS1} which is also the input voltage to the second stage. As expected the voltage drop of the mains also occurs for V_{OS1}. Additional because of the bridge rectifier and the diode in the detector another 2.1 V are lost. When starting from 24 V and considering a loss of about 4 V from the threshold voltage of the transistor, additional 6 V for the input delay, at least temporary 8 V from the partial voltage breakdown, while 4 V is the minimum input voltage and another 2.1 V are lost in the used diodes the entire first half of the time window is lost. After the zero crossing the input voltage has to reach its minimum value and the soft start circuit has to power up. Then the supply starts operation and the energy storage capacitor is recharged.

A proper designed control IC would get rid of most of the described problems. Furthermore specialized mode transitions could be implemented to optimize the energy transfer time as the development of the input voltage is known. Additionally a symmetric time window that is placed over the zero crossing would further increase efficiency. This cannot be achieved through the used discrete HW demonstrator as this would require a more sophisticated time window calculation.

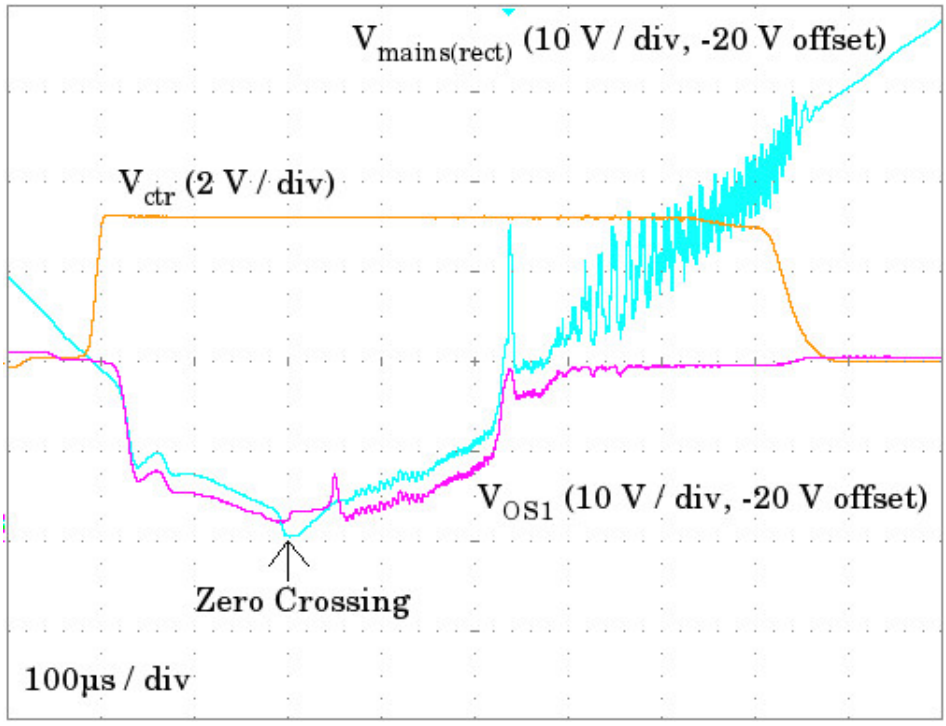

Figure 7.10: The input voltage into the second stage V_{OS1} has the same voltage drop as the mains. Additional three diode forward voltages are lost. The actual energy transfer occurs only at the end of the time window mainly due to the SMPS control IC that is not optimal and the high impedance of the isolation transformer.

7.2.4 Third converter stage and reset circuit

The third converter stage in the functional HW demonstrator generates the 3.3 V output voltage. This is a simple and straight forward buck SMPS that is powered from the energy storage capacitor and is running all the time to ensure a constant output voltage. The third converter stage didn't cause any problems in the functional HW demonstrator.

The reset circuit on the other hand had to be designed very carefully as an unintentional switch-on signal to the second stage caused by a improper powered logic could destroy the supply. An ultra low power linear regulator is used to power the logic circuits and the comparator. Additional a power- good reset circuit connects the logic and the comparator to the internal voltage only after it reached its designated value after startup to avoid uncontrolled oscillations and potential high currents. Additionally the control signal for the second stage is connected to the second stage after a delay that is generated by the power-good circuit. In a first approach the linear regulator for the internal voltage was powered from the energy storage capacitor only. The second stage was activated by default to charge the energy storage capacitor up to a point where the internal linear regulator is working. This causes high linear losses only during startup. The average energy would have been no problem for the transistor but unfortunately the peak current was. Some transistor types (e.g. 01N60C3) could not handle the peak current of the second stage at full mains voltage and have been destroyed. As a solution the internal linear regulator was supplied directly from the output

of the first stage. As the logic and the comparator section are extremely low power this is no problem for the transistor even at the maximum mains voltage. The second stage is now off by default and only activated when a valid time window is detected. When enough energy is in the energy storage capacitor the supply of the internal linear regulator is switched back.

7.2.5 Conclusion for the functional HW demonstrator

The functional HW demonstrator offered numerous problems that have to be addressed when designing such a supply topology. The second and third stage were separated and therefore two inductors were needed. Additionally the used SMPS control IC had a considerable reaction time to the enable signal and utilized a small but still noticeable soft start time. Although the state-of-the-art buck/boost full bridge control IC that was used in the second stage was carefully selected the reaction time as well as the control algorithms were not suitable for this supply type. The also included short circuit protection decreased the converter current during low output voltage levels when the storage capacitor was almost empty which made the usage of a bigger capacitor necessary. The supply control had a hard time adapting to the fast changing input voltage which may have resulted in an inefficient operation mode during the low voltage periods. The supply control IC had a relatively high minimum input voltage which further took some of the time window away. Additional to hold complexity of the discrete prototype manageable the time window was kept asymmetrically which further decreased performance.

Although the discrete version has a lot of troubles most due to the control IC of the second stage the demonstrator supply works reliable but not at maximum efficiency. The discrete HW demonstrator reached an efficiency of about 45% during tests which is remarkable considering the circumstances. A special designed integrated control IC may solve a lot of these issues and should be able to significantly increacse efficiency.

A remaining problem are the high current peaks near the zero crossing. While the public mains has better impedance characteristics as the used isolation transformer a larger number of nodes could cause a small voltage breakdown near the zero crossing that causes conducted EMI and decreases the efficiency of the supply. Therefore extensive filtering may be necessary which would make the supply bigger and make integration harder. If the concept is still feasible is depending on the actual supply configuration and the application parameters.

8 Conclusion

This thesis compares concepts for a non-isolated mains-powered power supply as standby power supply for smart appliances or as dedicated power supply for a wireless sensor node. The typical power requirements for the application field have been considered 100 mW at about 3.3 V. Basically two supply concepts have been investigated in greater detail. The capacitive based power supply utilizes an X2-type capacitor to limit the input current while the SMPS concepts use a high voltage transistor.

8.1 Evaluation of capacitive supply solutions

The capacitive power supply as described in section 3.1 is based around a current limiting X2-type capacitor. This capacitor limits the input current while a voltage limiting device which is a Zener diode in the simplest case limits the output voltage. A fundamental principle of the simple supply version is therefore that the input current of the supply equals the maximum output current. This leads to a relatively big X2-type capacitor and a relatively high apparent input power. The simple single stage version can be constructed very straight forward and the costs are comparatively low. However the efficiency is not the best and the reactive input power is high. This applies for the single rectifier version as well as for the full bridge version. When operating a large network of nodes especially the total reactive input power can be a big problem as it stresses the supply lines. As described in section 4.1 the supply can be much more efficient by simultaneously reducing the reactive input power and the capacitor size if the design is based on a higher rectifier output voltage level. For this, a two stage concept has been proposed that can reach very good efficiency with a decent sized X2-type capacitor. The second stage is a state-of-the-art high efficiency SMPS stage. The usage of a second stage requires an additional inductor but without a second stage this supply concept would not be applicable for practical use as the reactive input power would be too high.

However the practical usability of this supply principle may still be limited by the high reactive input current and the resulting low power factor. A supply with 100 mW output power would have a reactive input power of about 1 W even when a decent auxiliary voltage and a second stage is used. While this is absolutely no problem for a few nodes this can be not allowed if thousands of these nodes are used within a big network. Further reduction of the necessary power output and an increase of the auxiliary voltage can attenuate this problem. On the other hand [Dwy12] states that most commercial and industrial buildings are likely to have an overall inductive load profile. This means that the proposed capacitive supply concept can even compensate for a part of this inductive load balance. Hence, depending on the circumstances and the actual size of the network the proposed supply has a good chance to be utilized in a wireless sensor and control node. The only component of bigger size is the X2-type current limiting capacitor that is representative for the power output capabilities of the supply.

8.1.1 Methodology for the creation of automated design algorithms

Although designing a capacitive power supply seems simple on first sight, a lot of different scenarios have to be considered to design a reliable and safe power supply. Therefore section 3.1 not only gives an overview over existing capacitive supply topologies and their basic dimensioning but also gives a detailed description of additional design parameters that have to be considered for designing reliable supply solutions. These additional parameters that are not or only inadequately found in corresponding literature include component stress and compliance to safety regulations. This section builds the methodical foundation for future design automation for capacitive standby supplies. While it is theoretically possible to further simplify the presented designs or to soften their safety margins this may in the long therm lead to an unreliable or unsafe supply.

While section 3.1 delivers the basic coherences that have to be implemented in an automated design algorithm for capacitive-based standby power supplies, section 4.1 provides the necessary evaluation of this supply type in order to select the right design parameters as input for an automated algorithm for the dedicated application field. While the actual design parameters are more complex there is a tradeoff between the supply cost and its efficiency and its reactive input. Generally and for a first version of an automated design algorithm the two stage topology which was introduced in section 4.1.6 as a result of the evaluation is a good starting point especial when more supplies are straining the mains with the disadvantage that the second stage adds additional costs. The maximum auxiliary voltage will depend on the technology of the used second supply stage.

The enhanced integrated version of the two stage capacitive supply that is introduced in section 6.1 can further reduce costs. While this integrated supply looks promising, the detailed performance of this integrated topology still has to be evaluated before it can be included in an automated design algorithm.

8.2 A new SMPS-based supply topology

A direct straight forward SMPS topology for standby power supplies has to use a lot of high voltage components including a high voltage semiconductor switch and a relatively big inductor. Because of the high switching losses in the rectifier only DCM operation is applicable. An interesting enhancement was discussed in section 5 where only a small voltage window of the mains voltage is used. This leads to a highly reduced input voltage to the subsequent stages and results in the reduction of the necessary blocking voltage of the switching transistors which in further consequence reduces the parasitic capacitances and increases the possible switching frequency. The potential higher switching frequency makes the usage of a smaller inductor possible.

On the other hand because only a small time window of the mains voltage is available for the power conversion, the input current during this time window is relatively high. Hence the main drawback of this supply concept are short and relatively high bursts of input current. This means that the size can potentially be reduced or the efficiency potentially

increased when high input current peaks don't matter. By the usage of a more advanced time window control the current peaks can be attenuated by increasing the time window which on the other hand will decrease efficiency and increase the size and complexity of the design.

The main design problem for this supply solution is to find a tradeoff between the input current peaks, the maximum input voltage, the length of the time window and energy efficiency. Small current peaks make integration easier as the size of the inductor can be reduced. To decrease the input current peaks the time window can be enhanced in two ways. One way is to simply increase the time window but not the maximum input voltage. This would result in decreased current peaks and decreased EMI but would also lead to decreased efficiency because of linear losses in the high voltage transistor. Another way is to allow a higher input voltage which will increase the length of the time window automatically. This will require physically bigger transistors with a higher blocking voltage which will produce more switching losses and therefore limit the maximum switching frequency.

All the described solutions require a properly designed time window detector and a corresponding supply control. The main problem with these parts is energy efficiency and integration efforts. On one hand the circuits should not require additional high voltage components to make integration easier. On the other hand the detector and the control logic have to be fast enough to utilize most of the usable time window while not drawing too much power. While the detector and the control logic has been described and simulated, their proper function in a real supply had to be verified. This is done through the discrete hardware functional demonstrator.

The applicability of this concept depends on a number of issues. The European norm EN61000-3-2 [CEN02] defines limits for harmonic current emissions that stress the mains. That among other guidelines resulted in the breakthrough of active power factor correction (PFC) that is highly used in commercial power supplies. This norm regulates equipment over 75 W excluding lighting equipment, for which PFC is required typically for devices with a total power consumption greater than 25 W. However, for lighting equipment the supply may be usable as the power consumption of the node is very small compared to the power consumption of the lighting equipment. While the utilization of this supply may be possible theoretically, the practical consequences have to be considered. As these nodes are powered all the time the mains is stressed all the time and not only during the actual operation of the equipment. While this is acceptable for a few nodes it may be problematic for a larger number of nodes. This could go as far as the mains voltage could suffer a local voltage breakdown during the time window for a very large number of nodes which would produce serious EMC disturbances. Additional this will disturb supply operation as the time window has to be increased to ensure a constant output power. The actual application field and the size of the network will in combination with the time window control define if this supply is a viable solution. Because of its far smaller disadvantages the proposed two stage capacitive supply concept is likely to be the better choice for a standby power supply.

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Abbreviations

AC	alternating current
CCM	continuous conduction mode
CMC	current mode control
CRM	critical conduction mode
DC	direct current
DCM	discontinuous conduction mode
DVFS	dynamic voltage and frequency scaling
EMC	electromagnetic compatibility
EMI	electromagnetic interference
ESR	equivalent series resistance
EU	European Union
FOM	figure of merit
HV	high voltage
IC	integrated circuit
IEA	International Energy Agency
LED	light emmiting diode
MELF	metal electrode leadless faces
MLCC	multi layer ceramic capacitor
MOSFET	metal oxide semiconductor field effect transistor
OPA	operational amplifier
PCB	printed circuit board
PFC	power factor correction
PI	proportional integral
PNP	positive negative positive
RF	radio frequency

RHPZ	right half plane zero
RS	reset set
SEPIC	single ended primary inductance converter
SiC	silicon carbide
SiP	System in Package
TRIAC	triode for alternating current
TVS	transient voltage supressor
VMC	voltage mode control

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