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DISSERTATION

Behavior of Silicon and Gallium Nitride devices under electrical overstress conditions

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“There is no need to ask the question ”Is the model true?”. If ”truth” is to be the ”whole truth” the answer must be ”No”. The only question of interest is ”Is the model illuminating and useful?”.”, George Box, 1978.

Abstract

The miniaturization of integrated circuits has made microelectronics devices better and better whether in terms of integrability, speed or cost. One of the drawbacks of this trend is that the devices are more and more prone to failure caused by unwanted electrical stresses, as power density increases. This has gone to the point where half of the available area is sometimes used for protecting the active device. In general, the protection also hinder the performance of the device.

The first type of unwanted stress whose effects have been studied in this thesis is electrostatic discharge (ESD).

ESD effects on Silicon-Germanium hetero-junction bipolar transistors (SiGe HBT) used in low noise amplifiers have been studied. Two different types of athermal failure behaviors have been identified and explained in terms of silicon breakdown for long rise time and transistor parasitic action for short rise time and/or substrate coupling.

Two types of Silicon controlled rectifiers (SCR) used as ESD protection were studied. The SCR action was studied in terms of initial triggering, on-state spreading (OSS) in one finger, and sequential finger triggering was studied using Transient Interferometric Mapping (TIM). The role of trigger taps was investigated in breakdown with Emission Microscopy (EMMI) and during triggering using TIM.

The reliability of Gallium Nitride High Electron Mobility Transistors (GaN HEMTs) has been investigated in terms of vertical breakdown, degradation of the conducting and blocking performance at high temperature and short circuit load conditions. The behavior of HEMT devices under pulsed stress conditions (ESD and short circuit load) was studied with the TIM technique, which allows to probe the heat dissipation and the free carrier concentration through their effect on the refractive index of the material. New methods to analyze of the phase shift were developed, also enabling to work with distorted signal, or indirect probing outside the active region.

Kurzfassung

Durch die Miniaturisierung von integrierten Schaltkreisen sind mikroelektronische Vorrichtungen hinsichtlich deren Integrierbarkeit als auch deren Leistung und Preisverhältnis immer besser geworden. Ein Nachteil bei diesem Trend stellt jedoch die Tatsache dar, dass diese Geräte auf Grund von unvorhergesehenen, von steigender Energiedichte verursachten Spannungsdurchschlägen immer mehr zum Durchbruch neigen.

So wird manchmal bis zu der Hälfte der verfügbaren Fläche als Schutz für die aktiven Vorrichtungen eingesetzt. Somit wird übrigens die Leistungsfähigkeit der Vorrichtungen beeinträchtigt.

Diese Arbeit befasst sich zuerst mit elektrostatischer Entladung (ESD) als erste Ursache eines unvorhergesehenen Spannungsdurchschlags.

Dabei wurden die Effekte der ESD auf Silizium-Germanium-Heterobipolartransistoren (SiGe HBT) in rauscharmen Verstärkern erforscht. Es konnten zwei verschiedene Arten athermalen Spannungsdurchschlags bemerkt und analysiert werden, d.h. der Durchbruch von Silizium für lange Anstiegszeiten und die parasitäre Transistorwirkung für kurze Anstiegszeiten und/oder Substratkopplungen.

Es wurden zwei Typen von gesteuerten Silizium-Gleichtrichtern (SCR) mittels transienten interferometrischen Abbildungverfahren beobachtet, welche als ESD-Schutz benutzt wurden. Besondere Aufmerksamkeit wurde auf deren Wirkung bei der Auslösung der Triggerspannung sowie bei der Ausbreitung in einem und in den darauffolgenden Fingern während der Durchlassphase geschenkt. Die Rolle von Abgriffen wurde in Durchbruchsituationen durch Emissionsmikroskopie, bei der Auslösung durch TIM analysiert.

Darüber hinaus wurde die Beständigkeit von Galliumnitrid-Transistoren mit hoher Elektronenbeweglichkeit gegen vertikalen Durchbruch, Funktionsbeeinträchtigung im Sperr- und Durchlasszustand bei höheren Temperaturen und Kurzschluss getestet. Das Verhalten von HEMTs unter gepulster Belastung (ESD und Kurzschluss) wurde mit der TIM-Technik untersucht, welche es ermöglicht, die Wärmeabfuhr und die freie Ladungsträgerkonzentration durch deren Wirkung auf den Brechungsindex vom Material zu beweisen. Dabei wurden neue Techniken zur Analyse der Phasenverschiebung – etwa Datengewinnung aus dem verzerrten Signal oder der indirekten Beobachtung außerhalb des aktiven Bereichs – entwickelt.

Acknowledgement

I would like to thank all the people that have made this thesis a pleasant and fruitful period, which is both the end of my student life and the start of my professional carrier.

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Finally I would like to thank my family and friends for their support and patience.

Contents

Chapter 1

Introduction

1.1 Motivation

From smart phones to autonomous cars, microelectronics devices are more and more central to modern society. Since its beginning, microelectronics industry has been in a continuous process of diversification and improvement. The strength of microelectronics lies in the lithographic processes, that have allowed a mass production. The progress of the lithography has allowed to reach smaller and smaller feature size, thus improving the density of the devices on the wafer, which reduces their fabrication cost. In parallel, the fabrication on larger and larger silicon wafers has allowed to produce more and more devices on one wafer.

The miniaturization has not only been interesting for questions of cost, but also for the performances of the devices. The miniaturization of field effect transistors has enabled processors to reach higher speeds by reducing the switching time, and has allowed multi-core designs with billions of transistors. The reduction of the size of bipolar junction transistors allows to decrease the base transit time, and therefore improve their cut-off frequency.

Nowadays, the reduction has reached critical points for some of the silicon devices. The blocking capabilities of the devices are constrained by the breakdown electric field of silicon. The use of other materials having higher breakdown electric fields while still having other interesting properties has been developed in the last decades, such as silicon carbide, or ultimately gallium nitride. These materials are more expensive than silicon, and growing them on silicon substrates to reduce the costs has been a very active field of research.

Independently of the material, the miniaturization of the active region leads to an increase of the power density. This leads in turn to self heating, which can in the best cases be a source of performance degradation, and in the worst case lead to catastrophic failure due to thermal instability. This makes the devices very sensitive to certain types of stress that their bulky ancestors would have sustained without difficulty, and other new

types of stress that they would never have encountered in their use - even by accident.

1.2 ESD

Electrostatic discharges are produced when an object who has gathered charges by triboelectric or electrostatic induction effect discharges to another object due to a contact or a dielectric breakdown [1]. The energy of the discharge is low, but as the microelectronic circuit are small, the dissipated power density might be high enough to damage the components. Difference in objects capacitance and resistivity result in different density and duration of the current flow. As the microelectronic circuit should encounter various type of object in their production and their use, the industry has defined standardized models that define several types of ESD. The Human Body Model (HBM) of ESD aims to capture the ESD that is produced when a human being touches a pin and discharges in it. The model is essentially a capacitive discharge. The standardized test is made with an ESD gun, whose charging voltage is chosen according to the requirements of the situation in which the device will be placed. The device will then be called "robust" to a precise charging voltage if it sustains an ESD discharge at this charging voltage.

1.2.1 Silicon germanium HBT reliability

1.2.1.1 Silicon germanium HBT concept and use as a low-noise amplifier

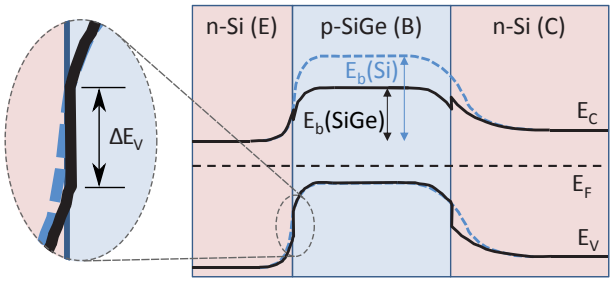


Figure 1.1: Schematics band diagram of a SiGe HBT, with silicon BJT in dashed line for comparison.[2]

Silicon germanium (SiGe) base hetero-junction bipolar transistor (HBT) are widely used in RF circuits due to several interesting properties, that we will shortly detail before discussing reliability issues. SiGe HBTs are made on silicon wafers. The silicon serves as collector, and is generally accessed by a burried layer. Then a p-doped noncrystalline SiGe layer that will be used as the base is grown, and a growth of silicon on top of the SiGe, or poly-silicon in some cases, makes the emitter on top of the base. The use of a silicon wafer enable SiGe HBT technology to inherit some of the advantages of silicon, for example in terms of thermal conduction, but also in terms of technological developments for large

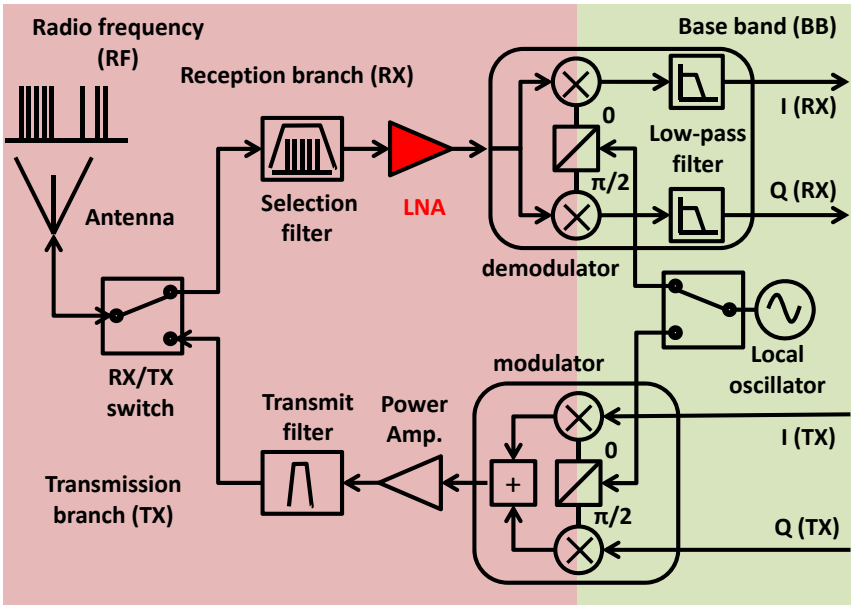


Figure 1.2: Position of the HBT as a low noise amplifier (LNA) in a reception branch of a mobile phone

crystal growth and doping, which makes them an affordable solution. Another advantage of using a silicon wafer is that a silicon CMOS circuitry can be included on the same chip to be used in BCMOS technology, or for a separate logic circuitry. The added value of the SiGe compared to pure silicon is the possibility of band gap engineering. The band gap of SiGe ranges between the band gap of silicon (1.14 eV at 273K) and germanium (0.67 eV at 273K). The alloy stoichiometry is typically in the range of 12 % germanium in the base of the HBT, which provides a band gap shrinkage of 50 meV [3]. The device that will be studied here have a $Si_{.85}Ge_{.15}$ base. Figure 1.1 shows the comparison between a SiGe HBT and a Si BJT band diagram at equilibrium. One can see that the valence bandgap discontinuity ΔE_V allows to keep a barrier for holes from base to emitter that is very similar as for the Si BJT, as seen in the zoom. This helps maintaining a low base leakage current. The main effect of the band gap engineering is seen in at the conduction band where the built-in potential of the base-emitter junction is lower in the case of the SiGe HBT compared to its silicon counterpart.

This allows to increase the doping in the base and reduce the base width to minimize the transit time of electrons to increase the speed of the device, while still avoiding punch-through and gain loss. The cut-off frequency is roughly five times higher than with Si BJT [2, 4, 5]. Another key aspect is the lattice constant that varies according to the stoichiometry of the alloy. At 300 K, the lattice constant of $Si_{.85}Ge_{.15}$ (5.47 Å[6]) is larger than the lattice constant of pure Si (5.43 Å[6]), and the SiGe is therefore compressively strained. This opens the possibility of strain engineering but also gives constraints to the largest achievable mono-crystal that can be grown on a silicon substrate at a given

thickness. The devices under study will have a maximum emitter window length of 10 μm and 2 μm width, or will have several fingers in parallel to achieve the desired collector current.

The HBT that has been studied here is used as a low noise amplifier. Figure 1.2 shows a possible architecture for the hardware of a general RF communication device, such as a mobile phone. For transmission, the RX/TX switch is set to connect the transmission branch to the antenna. The signal is mixed with the signal of a local oscillator to reach the desired RF frequency. For reception purposes, the RX/TX switch is set to connect the reception branch to the antenna (as in the schematics). The signal is filtered by the selection filter, amplified by the low noise amplifier and the IQ frequency demodulator brings the signal to the base band. As its name suggests, the LNA device amplifies with minimal increase of the signal to noise ratio from the input (filtered signal from the antenna) to the output (mixer). More than noise, the major concern of nowadays' design is linearity. The generation of harmonics that could cause intermodulation distortion in the mixing, as well as a noise for other reception channel (e.g GPS), should be minimized.

The devices under study are derived from the base technology presented in [4, 5] but with modified collector and base for higher breakdown voltage. Nevertheless, this modification also results in a lower cut-off frequency. The goal of this study is therefore to find how to get an improved ESD robustness of the device without giving up on the performance.

Part 2.1.2 will present the robustness of all junctions of the device. Section 2.1.3.1 will show the study of a high current, long rise time failure of the base-collector, whereas section 2.1.3.2 will show the causes of a low current/short rise time failure of the base-collector.

1.2.2 SCR as ESD protection

1.2.2.1 A general presentation of ESD protections

Many devices are nowadays equipped with USB ports, one function of whose is to transmit data through wire with a high rate - in 2017, 10 Gb/s has already been achieved. The devices that are directly on the interface between the system and the external world are subject to electrostatic discharges (ESD), that have become more and more dangerous for them as the miniaturization has concentrated the same electrical currents into a smaller and smaller area. These devices therefore need to be protected against ESD with protection devices that cannot be scaled down with the same factor, as they are bounded by the hard constraint of the electrical current value of the discharge. Although technological progress has been achieved with ESD protection, the protection takes more and more space on the die, which limits the yield, and sometimes the performance. Protection devices can be quite complex structures on the inside, but from the outside they are mere

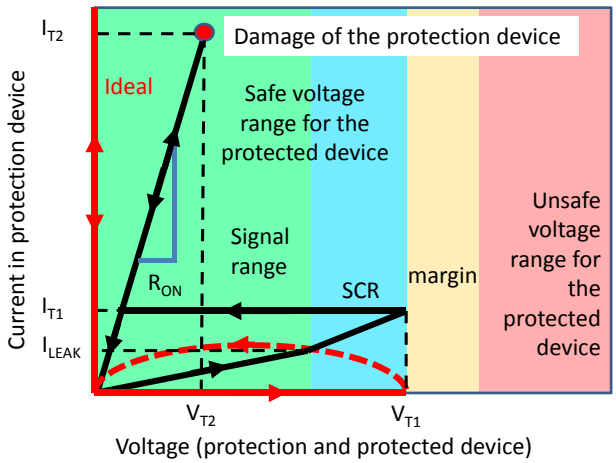


Figure 1.3: IV characteristics of an ideal ESD protection and a realistic SCR

two port devices that need to be connected in parallel to the protected USB port. This simplicity of the connections allows them to be placed in the third dimension as discrete components, which make their market one of the few microelectronics areas where the discrete component approach is still preferred to the integration. Several technologies of ESD protection are available on the market against different kinds of ESD and for different kinds of protected devices. Here we will focus on the Silicon Controlled Rectifier (SCR) for the protection of USB ports.

Ideally the protection is invisible to the rest of the system until it is needed to protect it. Figure 1.3 shows with red lines the current intensity-voltage characteristics (IV) of an ideal protection. Note that the protection device is in parallel with the protected device, so they share the same voltage. The ideal device is an open circuit when the voltage is safe (green and blue voltage range), and turns instantaneously into a short circuit if - and only if - the voltage ever goes beyond a given triggering voltage that is chosen from the designer at a margin of the unsafe voltage range for the protected device (the red area). The triggering voltage is noted V_{T1}.

The protection should also be able to go back to its dormant state once the ESD is over. Since the current is the only variable when the protection device is triggered, the protection has to be designed to turn off when the current value corresponds to a safe voltage in the characteristics of the protected device. This current is called the holding current I_H.

In practice, the device is not a perfect open circuit in its dormant state, because it has a leakage current (marked I_{LEAK} on figure 1.3), but also a capacitance, which is a source of attenuation and distortion for the useful signal. For high data rate USB purpose, the capacitance has to be less than 0.25 pF in the useful voltage range according to the IEC 61000-4-2 standard [7].

In its active state a real device does not feature a zero voltage, but is clamped below a voltage that should be safe for the protected device (green and blue area in figure 1.3). As

the device should stay in the safe zone independently of the current value in the protection, the slope of the IV curve in the triggered state should be as vertical as possible. The device should therefore have a large ON-conductance, or a small ON-resistance R_{ON}. A large R_{ON} also generates a power dissipation which can be a source of failure for the protection device itself at high current. The destruction current and voltage are called I_{T2} and V_{T2}, respectively. Last but not least, a real device takes a non zero time to react to the high voltage at its ports. This is referred as triggering time.

Shunting high currents is demanding in terms of space as the current needs to be spread to a large width so that the protection itself stays safe. Devices are therefore usually composed of several fingers in parallel, which divide the R_{ON} by as many folds.

1.2.2.2 Silicon Controlled Rectifiers (SCR)

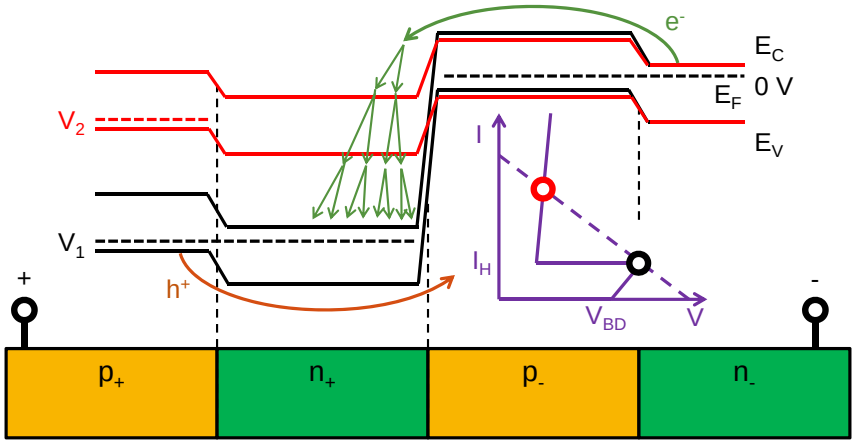


Figure 1.4: SCR structure and band diagram in blocking and triggered configurations

SCRs are PNPN structures [8] such as described in figure 1.4, which also shows the band diagram of the structure under blocking condition at voltage V1 (black) and triggered conditions at voltage V2 (red). The IV characteristics of the SCR in inset show the IV points in corresponding colors. SCR are used as ESD protection due to their S-shaped characteristics. For voltage V1 below the triggering voltage, the SCR presents a band structure such as presented in black in figure 1.4. At such voltage levels, both p^+/n^+ and p^-/n^- junctions are forward biased, and the n^+/p^- junction is reverse biased, which is the cause of the blocking state. This allows an SCR in parallel of a protected device to have a low leakage. The breakdown voltage V_{BD} corresponds to the voltage at which the n^+/p^- junction starts its avalanche breakdown represented by the arrows above the conduction band. The avalanche multiplication factor is voltage dependent, and is represented schematically by the 8 arrows that reach conduction band for V=V1 (against 2 for V=V2). At higher and higher voltage, the current flow increases, and the injections of electrons from the n^- through the p^- and holes from the p^+ through the n^+

provide more and more carriers to feed the avalanche process. Provided enough current, the device will "trigger". This means that the voltage that is needed to maintain the current level by means of carrier multiplication drops, as the avalanche current is fed by the injection. This state is represented by the red band diagram, where the multiplication is schematically represented as 2 arrows reaching the conduction band for V=V2. In practice, the device has to follow a load line, so the current increases as the voltage drops. From the triggered condition, the device can only be brought back to a breakdown condition by having a current flowing that is smaller than the holding current I_H.

1.2.2.3 State of the art

The SCR scheme that has been presented in the previous part can be applied in several ways to achieve the desired parameters for V_{T1}, I_H, Capacitance, R_{ON}, and leakage current, although there are tradeoffs to be made. First of all, in some applications, another connection can be made to the p^- to be used as a gate. A pulsed current can serve as triggering current instead of the breakdown current. This is not used for ESD protection, where the p^- is connected to the n^-.

The n^+ and p^- can be widened, and less doped to lower the leakage current and diminish the capacitance by spreading the depletion width. In the SCR that will be presented in this part, the p^- length is largely composed of the low p-doped substrate itself. In turn this approach gives a much larger triggering voltage (up to 80 V), that can be unsuitable to the use of the SCR as an ESD protection. The way around this problem is to insert trigger taps [9]. The trigger taps are narrow regions of p implants in the p^- region in the device width to achieve the desired low triggering voltage. Their role is to start the injection that can trigger the rest of the device. On the one hand, the trigger taps have a high contribution to the overall capacitance and to the leakage, and their number should therefore be minimized. On the other hand, the process of propagation of the ON-state (On-state spreading) has a finite speed along the width, which imposes a large enough number of these trigger taps to start the mechanism at several places. The R_{ON} of the device depends on the resistance of the structure, which is dominated by the low p-doped p^- region, and the total width of the device. This width can be the combined width of several fingers that are independent SCRs. If the fingers are isolated, one should not expect that they all trigger, as the first finger to trigger will make the voltage drop and prevent the current to flow in the other ones. Making all fingers of the device trigger simultaneously requires either that the voltage goes temporarily higher than the triggering voltage, or that a parasitic current (e.g to the substrate [10] or a displacement current [11]) initiates the triggering in all fingers, in a similar way as when the gate is used.

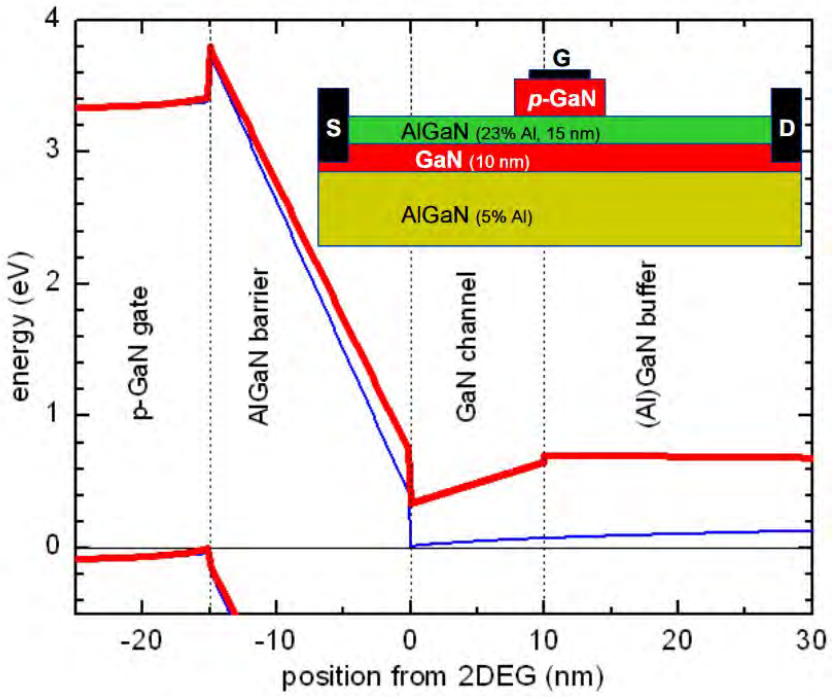


Figure 1.5: Simulated band structure at the gate position for a device with GaN buffer (thin, blue) and a device with Al 0.05 Ga 0.95 N buffer (bold, red). Inset: schematic cross section of the p-GaN gate GaN transistor. [12]

1.2.2.4 Outline of the section

Section 2.2.2 will show the behavior of the trigger taps in blocking and triggered state using EMMI and TIM. In the next part (2.2.3) the ON-state spreading will be measured with TIM and compared to simulations. The time-to-triggering at low voltage will be analyzed in part 2.2.4. In part 2.2.5, the focus will be made on how the fingers of the open base SCR share the power during the pulse depending on the pulse rise time, also using TIM at different current levels. Finally in part 2.2.6 the power dissipation at very high current will be analyzed to see the origin of the high current failure of the device.

1.3 GaN HEMTs reliability

Gallium nitride (GaN) is a III-V semiconductor with a 3.4 eV direct band gap. Although the 2014 Nobel prize for Physics has been awarded to Isamu Akasaki, Hiroshi Amano and Shuji Nakamura for their research on GaN to produce blue and white light by making a electroluminescent diode out of it [14, 15], large band gap semiconductors are also suitable for other purposes, in particular for the design of high voltage devices, thanks to their high blocking capability. GaN features a relatively high thermal conductivity of 250 W/mK at room temperature [16], which can be used to evacuate the dissipated heat

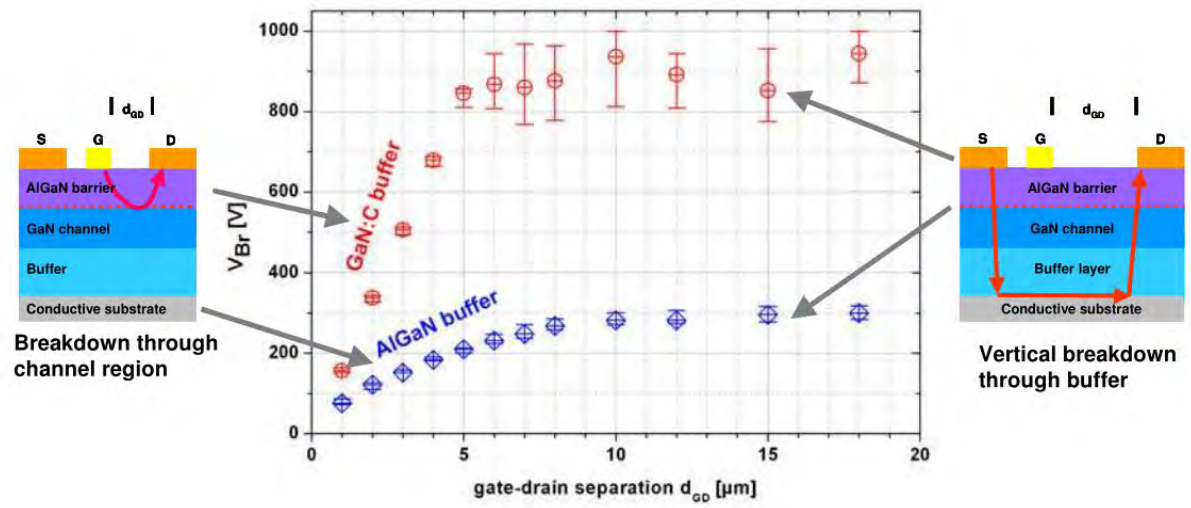


Figure 1.6: Median value of device breakdown in dependence on gate-to-drain distance (d_{GD}) for different buffer designs. The insets on the left and right side are highlighting the proposed breakdown mechanisms in the respective regions of the IV-characteristic. [13]

in a device. It also features a spontaneous polarization [17], that provides additional possibilities for the design of devices. The material capabilities of GaN also give hope that these devices be able to operate at high temperatures whether due to self- or external heating conditions [18, 19].

Numerous designs of GaN power devices have been demonstrated, such as vertical power transistors [20] or MOSFETs [21]. In this part, the focus will be made on AlGaN/GaN high electron mobility transistors (HEMTs) [22].

High electron mobility transistors Figure 1.5 shows the schematics cross-section of a transistor made with a GaN channel [12] and the associated simulated band diagram under the gate. The channel presents a triangular well that is created by polarization charges at the barrier/channel interface [23] (hence the electrical field discontinuity). In absence of a p-GaN gate, as in the access region, the triangular well is partially under the Fermi level, which allows conduction. The confinement of the electrons in a 2-dimensional electron gas (2DEG) gives them a high mobility [24]. The additional growth of a p-GaN gate on top of a part of the 2DEG is used to lift the triangular well above the Fermi level as in figure 1.5, which depletes it. This area is called the channel of the transistor, and the area between the channel and the drain/source contacts where the 2DEG is present is called the access region. To operate the transistor, the triangular well can be brought down under the Fermi level by applying a positive voltage on the p-GaN gate. This brings the transistor in ON state. For safety reasons, the transistor should have a high enough threshold voltage. In OFF state, when a high voltage is set on the drain and the gate is grounded, the access region gets depleted as well and the whole access

region sustains the electric field. The use of an AlGaN buffer allows to have an insulated buffer to limit the punch-through under the gate. This is made at the expense of the thermal conductivity [25]. Carbon or iron doping of a GaN buffer can also be used to the same purpose. As bulk GaN is expensive, the buffer is grown on a SiC substrate, with a final goal to have GaN on silicon devices [26]. Gallium nitride HEMTs face several reliability issues, such as charge trapping [27], or dynamic ON-resistance due to virtual gate effect [28].

Vertical breakdown The first part of this study will focus on the high voltage breakdown. The breakdown voltage V_{BD} of HEMTs has been proved to linearly increase with the gate to drain distance L_{GD}, as a critical electric field needs to be reached in the gate-to-drain area, see figure 1.6 on the left. Beyond a critical voltage, V_{BD} becomes independent of L_{GD} [13, 29]. The explanation involves a parasitic current path through the substrate as depicted in figure 1.6 on the right. To enable this path, the voltage should be high enough to breakdown the vertical stack in one direction and the other [13, 29]. The high spreading in the V_{BD} data in vertical mode might indicate that the vertical current conduction is related to extended defects. Trap-mediated transport [30, 31] was hypothesized by several groups, and the failure was located by conventional microscopy [31]. These studies have led to the optimization of the contact areas. [32]. However, more understanding of the vertical breakdown is necessary to produce devices that can be reliable at high voltage. In section 3.1, a statistical analysis that can extract useful information from vertical DC-IV measurements at the wafer level will be shown. The time dependence of the vertical breakdown will be demonstrated and explained in section 3.1.4. The vertical breakdown will also be analyzed by the failure analysis of purposely damaged device using infrared microscopy in section 3.1.4.

High temperature behavior As a strong point of GaN devices should be their high temperature operation, reliability of GaN HEMTs under high temperature conditions need to be studied. The variations of the threshold voltage, and the decrease of the transconductance and the maximum drain current will be shown in section 3.2.2 in DC operation. The blocking capabilities of the GaN HEMT at high temperature will be shown in section 3.2.3 and the hypothesis that the lowering of the breakdown is due to vertical breakdown will be discussed using high temperature vertical breakdown measurement in section 3.2.4.

Short circuit load operation The self-heating effect is one of the main limiting factors for the performance and reliability of these devices. Liquid crystal thermography [33], micro-Raman thermography [34] or scanning thermal microscopy [35], have been used to map the temperature distribution in GaN-based devices. Section 3.3 will show the thermal analysis and the reliability of HEMT devices by the TIM technique (see section 1.4.2.1)

under short circuit load operation, where the drain voltage is nearly fixed due to the short circuit like load line and the gate is open during 10 μs. By nowadays' standards, The HEMTs should be robust to this conditions during few microseconds [36, 37].

TIM on GaN HEMTs Section 3.3.2 will present a new post-processing method for TIM data evaluation, enabling temperature extraction in the whole heated region from the limited TIM data outside the active region utilizing the 2-dimensional nature of the power dissipation source located in the two-dimensional electron gas (2DEG).

1.4 Methods

1.4.1 Electrical stressing

1.4.1.1 Transmission Line Pulser (TLP)

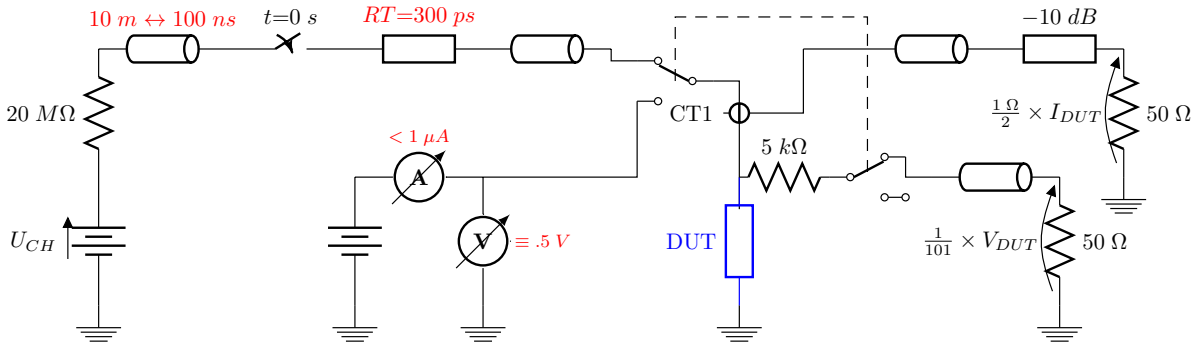


Figure 1.7: Schematics of a 4-point-probe TLP system, adjustable parameters are shown in red.

The Transmission Line Pulser (TLP) is an instrument that allows to provide a wide range of electrical pulses. As figure 1.7 shows, a coaxial cable is charged at a defined charging voltage (between -1.5 kV and +1.5 kV for this HPPI model). The opening of a relay (REED, or mercury relay) then discharges the line into the device under test [38, 39]. The width of the pulse (PW) is equal to the time that the pulse needs to travel twice the length of the charged line, which makes 10 ns/m. In the following study, we used line lengths that provide pulses from 10 ns up to 450 ns. Rise Time (RT) filters can be connected between the end of the charged transmission line and the output of the relay that low-pass filter the pulse, hence smoothing the edges, so that the pulse RT is fixed at a specified value. The user can choose between values of 100 ps (no filter), 300 ps, 1 ns, 5 ns, 10 ns, and 50 ns. The main inconvenient of the TLP for some purposes is its large jitter, i.e the precision on the time at which the pulse starts. This means that the TLP has to be the trigger source for all other instruments in the measurement. This for

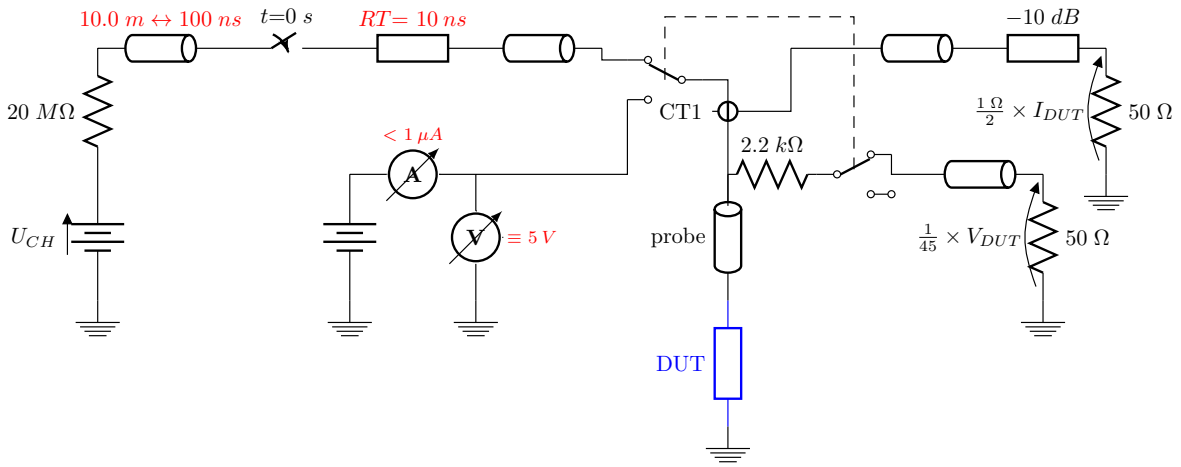


Figure 1.8: Schematics of a 2-point-probe TLP system, adjustable parameters are shown in red.

example excludes the TLP as a stress for the 2D-TIM setup, where a pulsed laser has to be synchronized to the electrical stress.

The pulse parameters that correspond best to the HBM model are $PW = 100\ ns$ and $RT = 10\ ns$ [1]. This approximation is valid mostly from the energy point of view and not necessarily for all the transient voltage or current, to which a device can also be sensitive, as it will be shown with the HBT devices in part 2.1 and with the SCR in part 2.2.

Two ways have been used to probe the voltage at the device. The 4-point-probe configuration is shown in figure 1.7, where the voltage is probed at the device with a 5kΩprobe needle. This configuration allows to cancel the contact resistance due to the force probe. The setup shown in figure 1.8 is a two point probe setup. The measured voltage should be corrected for the contact resistance, but its compactness makes it a more convenient tool for stressing during TIM.

1.4.1.2 Solid State Pulser (SSP)

The solid state pulser uses a solid state switch. The interest of the SSP is a low jitter in the ns range that allows synchronization with other instruments, pulses of arbitrary lengths, and the possibility of using a repetitive mode, which can be useful for techniques such as EMMI where a single pulse does not produce a detectable response. A baseline can also be used. The limitations of the SSP are the minimum rise time of 5 ns, and the maximum charging voltage of 100 V, which provides 2 A under 50 Ω load line.

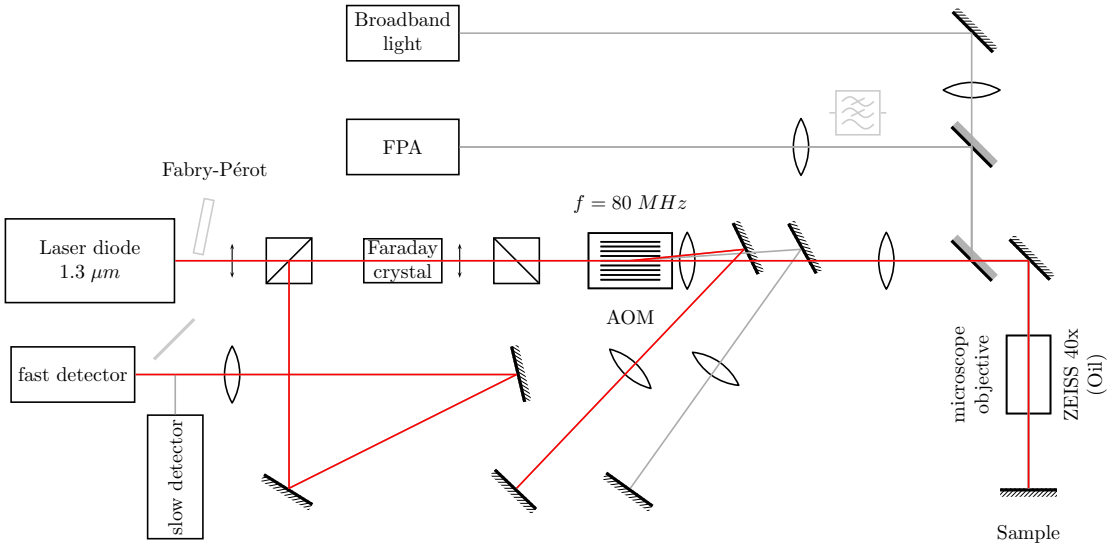


Figure 1.9: Schematics of the TIM setup in fast heterodyne configuration

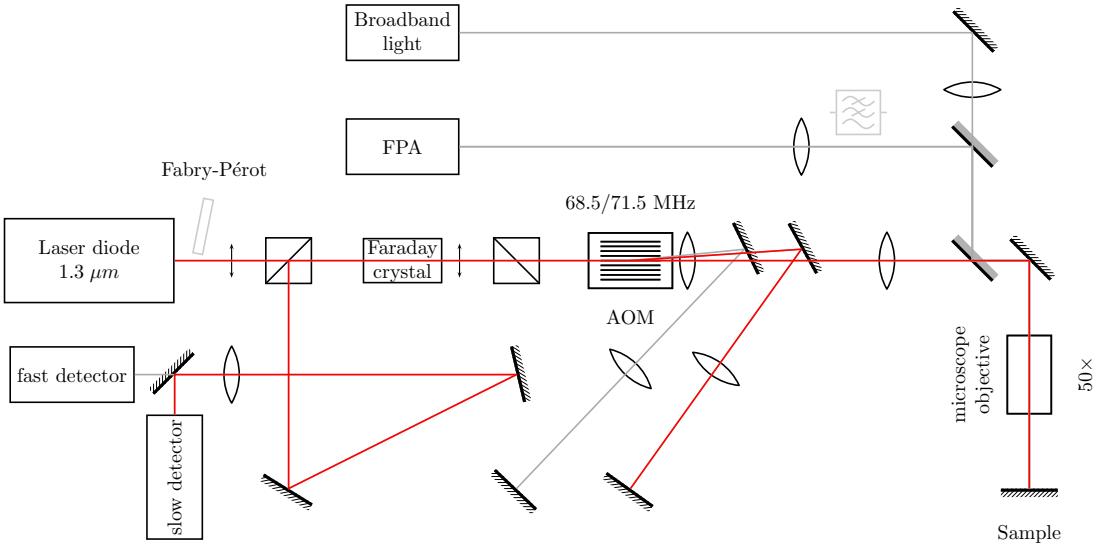


Figure 1.10: Schematics of the TIM setup in slow heterodyne configuration

1.4.2 Optical methods

1.4.2.1 Transient Interferometric Mapping (TIM)

The TIM technique is based on the measurement of the change of refractive index due to temperature or free carrier concentration (FC) change during an electrical stress (e.g under TLP stress). The measurement is performed with an interferometer shown schematically in figure 1.9 and 1.10, where the probe beam probes the device from the polished backside. The wavelength of the laser is λ=1.3 μm, so semiconductors with a band gap larger than 0.95 eV (including silicon with 1.1 eV and GaN with 3.4 eV) are transparent to the probe

beam, provided they are low-doped.

The change of the index of refraction with the density of the free carrier plasma can be explained in terms of the Drude model for the photons going through the medium, where they can scatter with the free carriers, hence decreasing their group velocity. [40]

The change of the index of refraction with temperature has been measured for several materials by [41]. In general the change of the refractive index with temperature or FC will be described with a linear model around a fixed condition, where the coefficient will only be material dependent.

The effect of the refractive index change on the phase of the probe beam depends on the behavior of the light in the device. The light can be scattered, in which case the effect is unpredictable without accurate 3D optical modeling, so this case will be left apart.

The simplest case is the single reflection, where the phase shift is due to the lengthening or shortening of the optical distance. As the beam is reflected on the metal or on the top interface with air, it goes twice through the device. We note z the direction of the beam in the device and λ the wavelength of the light in vacuum (here 1.3 μm). Provided a field of refractive index change $\Delta n(x, y, z, t)$, the phase shift $\Delta\phi(x, y, t)$ of the probed beam will therefore be given by:

$$\Delta\varphi(x, y, t) = 2 \times \frac{2\pi}{\lambda} \int_{bottom}^{top} \Delta n(x, y, z, t)\, dz \tag{1.1}$$

In this case the reflectivity of the device will change very little during the pulse.

If there are reflections at other interfaces, as in the case of a SOI substrate or a GaN heterostructure, the dependence on the phase shift is more complicated and the reflectivity is likely to change due to constructive and destructive interferences. One way to compute the phase shift response to a given refractive index change at a given vertical position is to use the transfer matrix method [42], where a complex valued transfer matrix is computed for each layer using its thickness and refractive index (plus the refractive index variation for the active layer). After the multiplication of all matrices corresponding to each layer, the complex reflection coefficient of the whole stack is extracted. The complex argument of the reflection coefficient is the phase of the beam, and its squared modulus is the reflectivity.

This computation can give the phase associated to any field of refractive index, but it suffers some issues when applied to practical cases. The computation requires a level of precision on the thicknesses of the layers that is small compared to $\lambda/2n$, i.e tens of nanometers. As the process is not always able to reach this precision in all layers (particularly for the passivation layer), the best course of action is to FIB-cut the device along the scan path after the TIM scan and measure the layer, which is still quite an investment to make.

Note that these simulation techniques compute the response from a given refractive index change, whereas we are actually much more interested by the inverse problem. This will be discussed in a few paragraphs.

The measurement of the phase shift is performed with a heterodyne interferometer. The word "'heterodyne"' indicates that there is a mixing to an intermediate frequency. The fast heterodyne configuration shown in figure 1.9 is suitable for short stress in the order of 100 ns. The mixing is made through a Acoustical-Optical Modulator (AOM) fed with a 80 MHz signal, that shifts the frequency of the probe beam by 160 MHz compared to the reference beam. The interference of these two beams at the detector creates a 160MHz beating signal with a phase that is equal to the phase of the probe beam.

The slow heterodyne configuration shown in figure 1.10 uses a a frequency for the probe beam and a second frequency for the reference beam. The beating frequency is then half the difference between both. The heterodyne signal will typically be at 71.5-68.5=3 MHz. This allows using a slower, more precise detector and record the response to longer stress.

The device positioning is performed by a stage with 100 nm step. The device is contacted on the stage with the appropriate circuitry. Every step of the scan consists in displacing the device to a new position, enabling the stress a chosen number of time while recording the electrical waveforms and the signal from the detector (the oscilloscope is triggered on the current or the voltage), and performing a leakage check to control whether the device suffers cumulative damage. The leakage check uses relays to switch the connection of the device to a SMU.

The post-processing of the TIM signal is done numerically by phase demodulation of the recorded signal for the phase shift [43]. The amplitude can be extracted as well, for example using Hilbert transform. The averaging is done after the extraction on individual waveforms. Filtering of the signal can be needed in some cases, at the expense of the high frequency features of the signal.

The interpretation of the phase shift should be made using different approaches, depending on the optical response discussed earlier and the nature of the optical phenomenon (FC or temperature). In the case of a single reflection and when only one material is heated, a purely thermal signal is proportional to the integral of the heat along the z axis. As long as the diffusion length of the heat is smaller than the resolution of the scan, the time derivative of phase shift corresponds to the integral of the power dissipation. As the phase shift starts at zero by definition, the derivative is proportional to the phase shift itself at low time, provided that the power dissipation be constant during this interval, which provides yet another simplification of the phase shift interpretation,

at the cost of one more hypothesis. This hypothesis will be unsafe to use in the case of filaments that move faster than the diffusion allows, for example, and the derivative needs to be used even for time below the diffusion time corresponding to the scan step or the required precision [44]. As time goes, the diffusion spreads the heat and the phase shift distribution is no longer representative of the instantaneous power dissipation. Furthermore, additional heat is dissipated during the pulse. To compute the power dissipation, or rather its horizontal projection P_{2D}, one should integrate the heat diffusion equation including the diffusion term along the z direction [43]. The resulting equation (1.2) shows the relation between the 2D power dissipation P_{2D} and the phase shift $\Delta\varphi$, where μ is the thermo-optical coefficient, C_V is the thermal capacitance of the material of the active layer, and γ its thermal conductivity.

$$P_{2D} = \mu^{-1} \times \left[C_V \frac{\partial}{\partial t} - \gamma \left(\frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2} \right) \right] \Delta\varphi + J_z^{th} \tag{1.2}$$

This method only requires a local measurement of the device (at least 5 points to be able to compute second derivatives in both direction) to extract the local power dissipation. However, there are a few difficulties to overcome when applying it to experimental data. One remarks that the z-component of the thermal current density J_z^{th} cannot be solved. This is due to the projection that the TIM operates on the z-axis. The vertical heat flow cannot be sensed and the numerical extraction method is best when this component can be neglected. This is not always an issue, as microelectronic devices mostly have their active region in the first few micrometer of the top side. The equation also features a first derivative with time and two second derivatives with space. The numerical derivation is in general very sensitive to noise, and this can be a major issue in some cases. The phase shift distortion due to multiple reflection can also be problematic.

This method will also suffer some issues when dealing with a device using several materials that do not feature the same thermo-optical response, such as GaN on SiC. The heat flow from one to the other material will increase or decrease the phase shift without needing any heat input, and yet this effect will be interpreted as power dissipation.

In part 3.3.2 a new method will be presented that can avoid the problem of multiple materials by making a linear thermo-optical model of the whole device. This approach will also enable to deal with the uncertainty of the optical response by using indirect probing.

1.4.2.2 Backside Infrared Microscopy

The backside infrared microscopy uses partly the TIM setup, as shown in figure 1.11. The device is lit from the backside and an infrared camera looks at it. This allows to align the device with the laser beam for TIM, and can also be used to identify damage signatures on a damaged device, in particular when metal hides the active region from the top. The camera that is used for this purpose is either a Vidicon camera, or a InGaAs

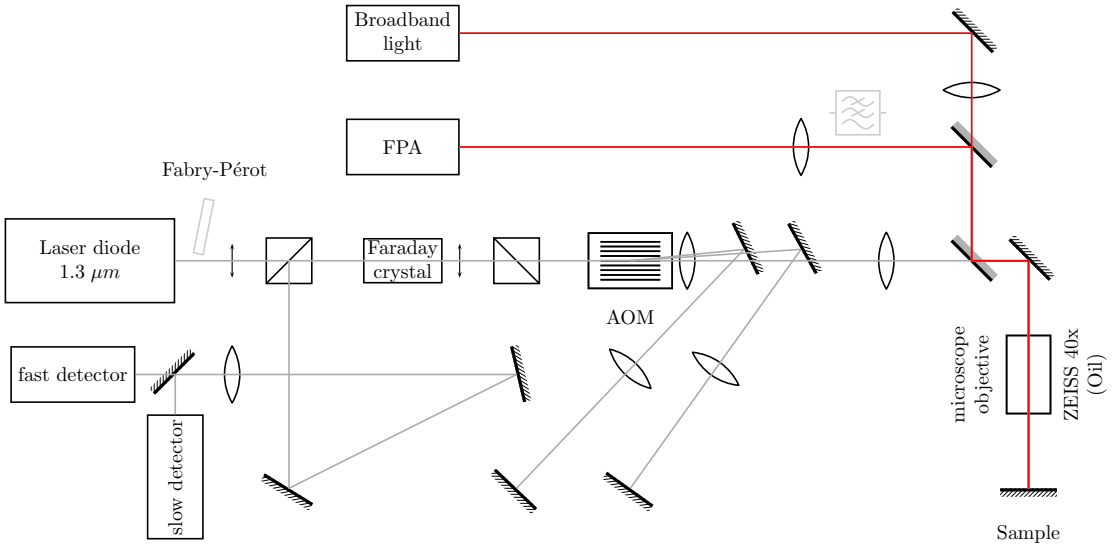


Figure 1.11: Schematics of the TIM setup used for imaging devices from the backside.

Focal Plane Array (FPA). Several objectives have been used, depending on the device, including oil-immersion objectives.

1.4.2.3 Emission microscopy (EMMI)

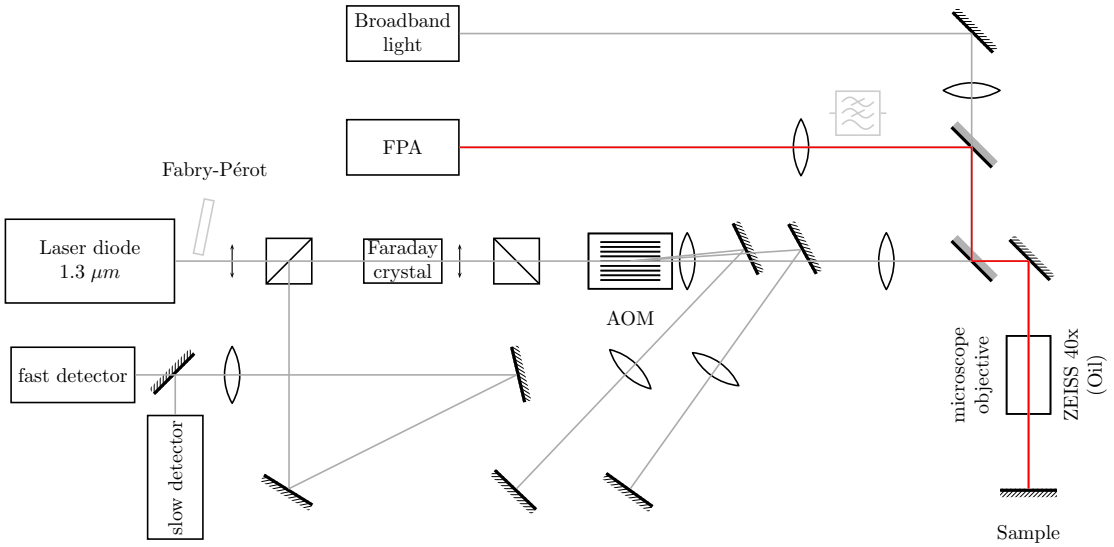


Figure 1.12: Schematics of the TIM setup used to perform EMMI

EMMI consists in stressing a device electrically and simultaneously looking at the device with a camera, as shown in figure 1.12. The stress that have been used are DC and repetitive pulses. In our case, as the TIM setup is used, the device is imaged from the

back side. The microscope objective is a 50x oil-immersion and the camera is a InGaAs Focal plane array. Filters can be used to identify the emitted wavelength.

1.4.2.4 Optical Beam Induced Current (OBIC)

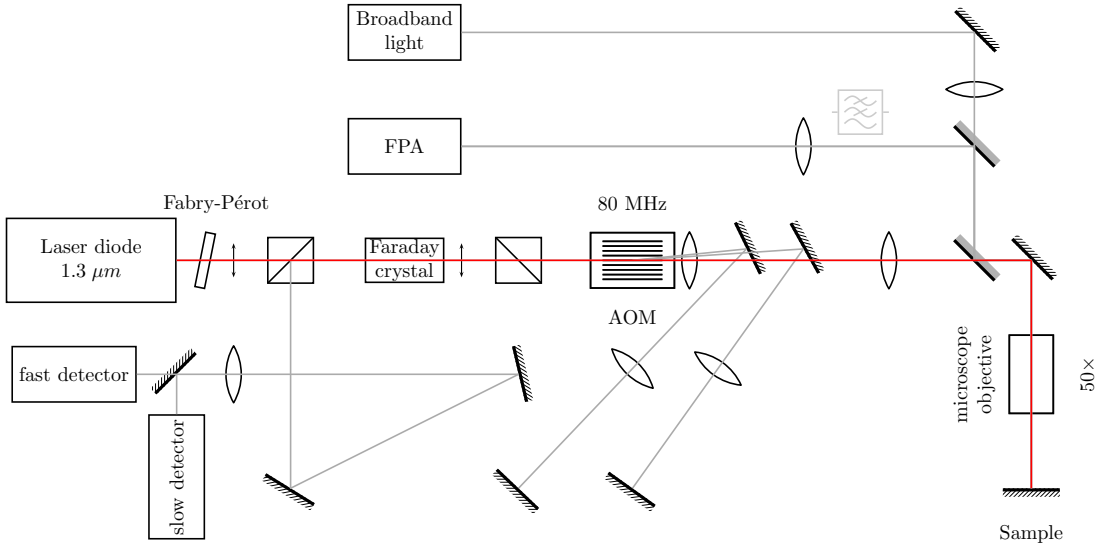


Figure 1.13: Schematics of the TIM setup used to perform OBIC

The OBIC technique is the only technique that has been used in this thesis that uses the laser beam in an invasive way. As figure 1.13 shows, the device is biased at a fixed DC voltage or current and the probe beam scans the device. The leakage level for each position of the beam is recorded and a map of the leakage current under light is drawn. The high current position are parts of the device that are light sensitive, as forward pn junctions. The damage signature of a damaged device might respond to light in some case, depending on the nature of the damage and the wavelength of the laser beam, which makes it an interesting tool for failure analysis. The setup that is used for OBIC is the TIM setup where an additional Fabry-Pérot is set at the output of the laser to shape the laser spot.

Chapter 2

ESD self-protected HBT devices and discrete SCR protection

2.1 ESD self protected Silicon-Germanium base HBT as low noise amplifiers

2.1.1 Devices under study

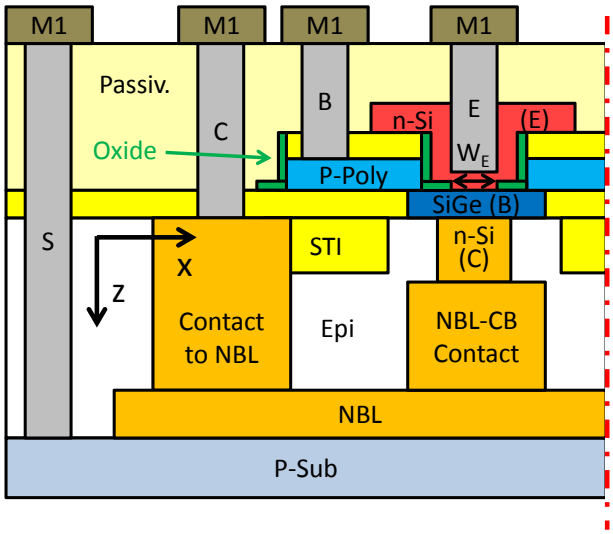


Figure 2.1: Schematic cross-section of a single finger device. The dashed line on the right shows the symmetry for the double finger device.

The devices under study are npn HBTs with a $Si_{.85}Ge_{.15}$ base. The devices structure is shown in figure 2.1 for a single finger HBT, and should be mirrored with respect to the dashed line to obtain the structure of a double finger device. The collector is brought from the n-doped buried layer (NBL) through n-implantation. The NBL is connected to the collector metal by the n-implantation contact marked as "contact to NBL" and

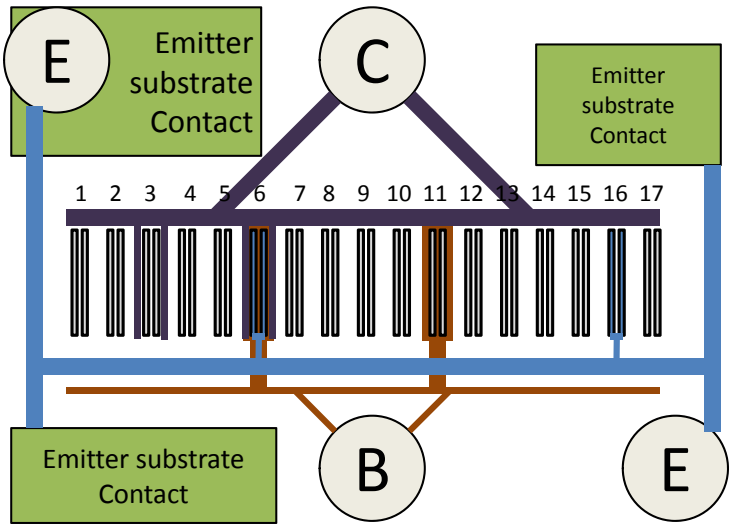


Figure 2.2: Schematic layout of the multifinger HBT device

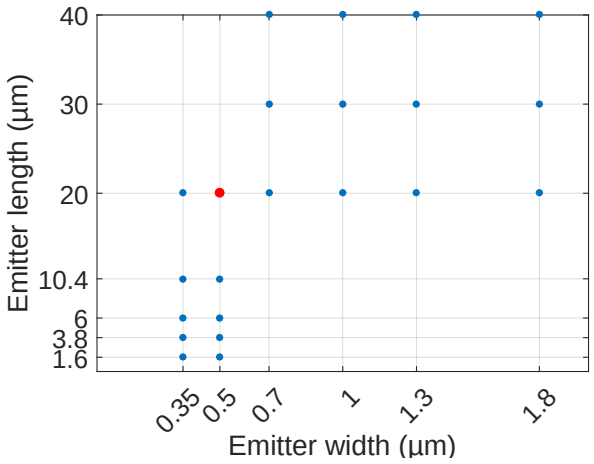


Figure 2.3: Available width and length combinations for the emitter window of test structures. The red dot at (W_E=0.5 μm, L_E= 20 μm) indicates the dimensions of one finger of the multifinger device

the collector of the device is connected to the NBL by the n-implant contact marked as "NBL-CB contact". The SiGe base is contacted with a p-poly-silicon layer that accesses the finger from all around the emitter window. The emitter n-Si is separated from the p-poly by a SiO_2 deposited layer marked with the arrow and the "oxide" label. The size of the base emitter junction, or emitter window, in the x (resp. y) dimension will be referred as emitter width (resp. length) and noted W_E (resp. L_E). The two types of devices that were studied are:

- Multifinger devices, that consist of 16 blocks of double finger HBTs, where the width of each finger is 0.50 μm and the 20 μm length is divided into two 10 μm SiGe islands. In these devices, the substrate is connected to the emitter with a via and a

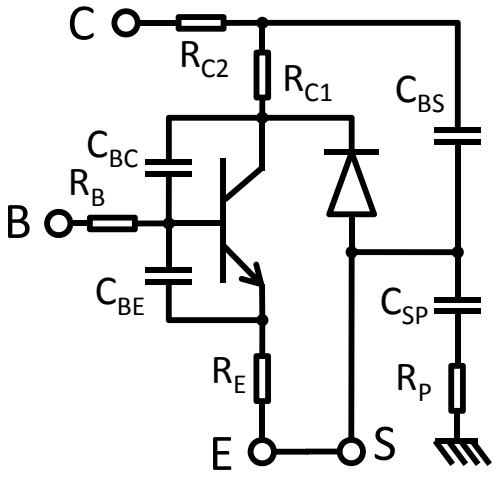


Figure 2.4: Device with its main parasitic elements. The ground symbol shows the shield of the probe needle, wherever the ground contact is placed.

metal. This connection scheme is used because the amplifier is operated in common emitter mode, and the substrate is chosen to be the ground of the circuit. Figure 2.2 shows the layout of the multifinger device that was analyzed in this study. The collector and base pads and the two emitter-substrate pads are shown. All fingers are shown as gray rectangles in the center, corresponding to their emitter contour. The collector, base and emitter-substrate metals are shown in dark purple, brown and blue, respectively. Finger 9 is not connected. On finger 3, the collector metal M2 is shown, which is connected to the collector M1 that is shown in figure 2.1. In finger 11, the base connections are shown in brown: the M1 is used to go underneath the M2 of the emitter metal in blue. Inside the transistor block the base contact is made with poly-silicon, as shown in figure 2.1. On finger 16 are shown the emitter contacts with the M2 metal. The M1 shown in figure 2.1 is connected by vias to the emitter M2. In finger 6, all connections are shown at once.

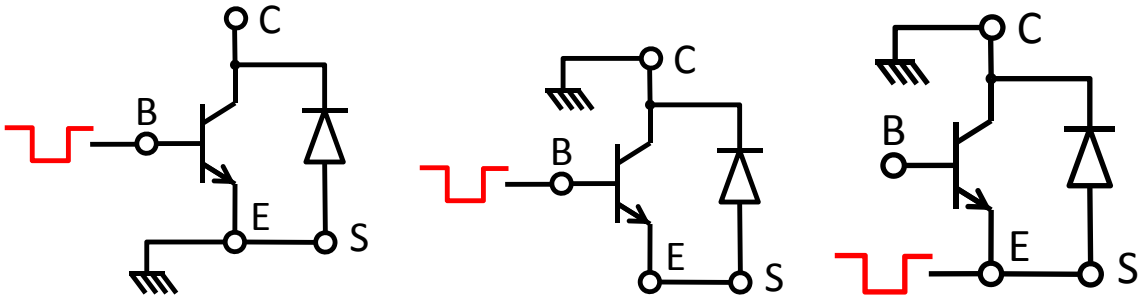
The layout in figure 2.2 also shows the location of the main substrate contact to the emitter.

- Test structures (TS), which consists of a double-finger and single-finger HBTs with independent substrate contacts. They have emitter width values W_E=0.35, 0.5, 0.7, 1, 1.3 and 1.8 μm and emitter length L_E=1.6, 3.8, 6, 10.4, 20, 30, and 40 μm. All available combinations are shown in figure 2.3. Notably, all the emitter width values are available for L_E=20 μm, as double finger structures with W=0.50 μm, and L=20 μm are the building blocks from which the multifinger devices are made.

The parasitic elements of the device are shown in figure 2.4. The diode between the p-substrate and the n-collector is due to the pn junction. C_{BC} and C_{BE} and C_{CS} are the three junction capacitance. C_{BE} is large as it also includes the thin oxide capacitance.

R_B and R_E are respectively the base and emitter series resistance. R_{C1} is the resistance to the substrate/NBL junction and R_{C2} is the contact from the NBL to the collector pad. To explain the substrate coupling, C_{SP} and R_P are introduced. The reduced form of the HBT schematics (whether test structure or multifinger) will keep the substrate diode as a convenient notation to explicit the substrate connection.

2.1.2 ESD robustness of the HBT in different combinations



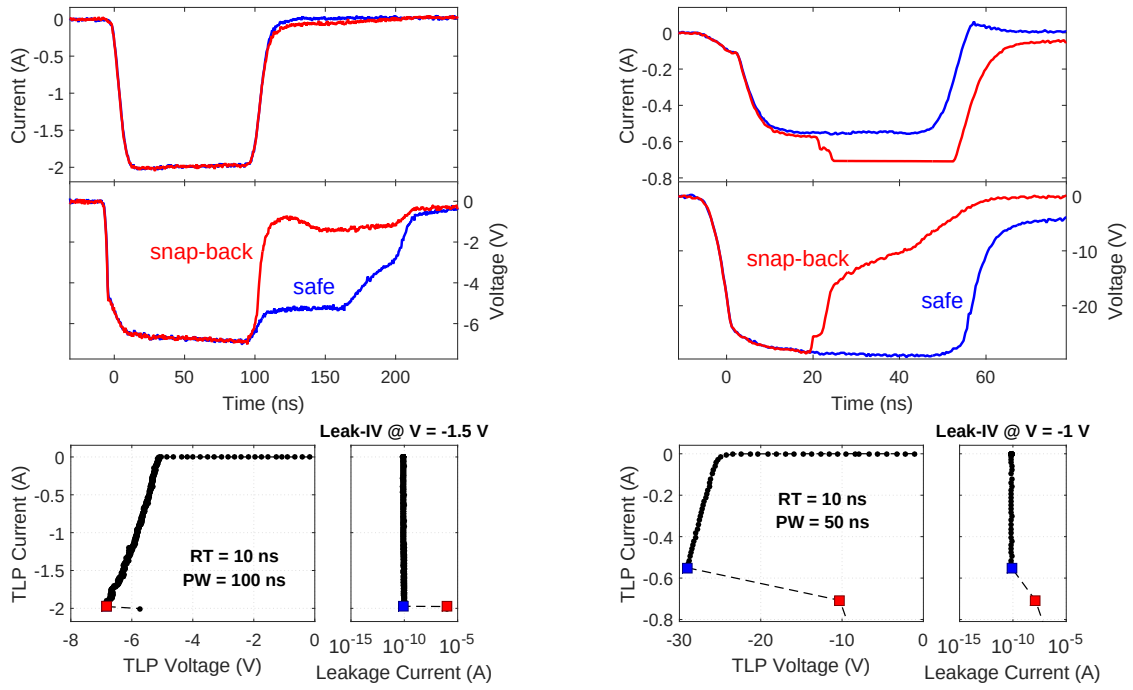
(a) B^-vsE **(b)** B^-vsC **(c)** E^-vsC

Figure 2.5: Stressing conditions for HBT multifinger device

The robustness of the multifinger device was studied by making the TLP-IV of all possible pairs of pads. In the following we show the reverse base-emitter (B^-vsE), the emitter-collector (E^-vsC) and the reverse base-collector stressing (B^-vsC) that are represented in figure 2.5.

2.1.2.1 Base-emitter characterization

The reverse base-emitter TLP-IV for a rise time of 10 ns and a pulse width of 100 ns is shown in figure 2.6a (bottom). As long as the voltage is below the breakdown voltage of 5 V, the current is negligible and the voltage is equal to the charging voltage of the pulser (see part 1.4.1.2). Beyond the breakdown voltage, the device shows a breakdown, which is a rise of the reverse current. The ON-resistance, i.e the differential resistance of the device in breakdown is roughly 1 Ω. This corresponds to the intrinsic base and emitter resistance, plus the access resistance to the base emitter junction from the pads, most of which should be due to the base resistance, as it includes the poly-silicon, and narrower metal lines. The contact resistance of the probe is not affecting the voltage measurement, as the measurement is done in 4 point mode (see part 1.4.1.2). In the blue waveform, where the device is safe, one can see that the voltage is rising during the pulse. This is typical of avalanche breakdown, which is caused by the impact ionization of the lattice that leads to carrier multiplication. The temperature increase due to self heating during the pulse shortens the mean free path of the electrons, thus diminishing



(a) B^- vs E **(b)** B^- vs C

Figure 2.6: TLP IV of the multifinger device under B^-vsE and B^-vsC conditions (described in figure 2.5) and post stress leakage. Waveforms corresponding to the cursors in the TLP-IV and leakage are shown in corresponding colors. The TLP-IV values correspond to a 70-90 ns averaging window.

their impact energy, and therefore the multiplication that drives the current. As the value of the current/voltage follow the load line, where the load resistance is the characteristic impedance of the transmission line (50 Ω), the decrease in the current is accompanied by an increase of the voltage. The "safe" waveform also shows that the device voltage stays at the breakdown voltage after the end of the pulse during about 60 ns and then decreases. This is probably due to a reflected pulse that that is attenuated in the pulser so that its effective charging voltage is hardly above 5 V.

When the charging voltage is set to 100 V, the device is damaged, which can first be seen in the increase of the leakage current in figure 2.6a. There is no visible snap-back during the pulse (see red waveform in figure 2.6a), but the low value of the voltage for the reflected pulse (at 150 ns) and the slightly higher current show that the device now features low impedance. The voltage drops as fast as the incident pulse, and the current is slightly higher than for the safe pulse, which corresponds to the increase of the conductance of the discharge path. After the pulse it can be seen that the DC leakage value at $V_{BE} = -1.5\,V$ has rose to 1 μA, which is also the sign of a damage of the transistor. The snap-back at the end of the pulse for a small charging voltage increase is

evidence for a thermal damage.

The I_{T2} value of the base-emitter stressing under 100 ns and 10 ns is 2 A. This shows that the device should be robust to 3 kV HBM testing.

2.1.2.2 Base-collector characterization

The stressing of the base-collector junction is shown in figure 2.6b for a pulse width of 50 ns and rise time of 10 ns. The shape of the IV (bottom) is similar to the base emitter IV for low charging voltage up to the breakdown voltage. The breakdown voltage is -24 V which is much higher than for the base emitter due to the much lower doping of the collector. The ON-resistance is 7 Ω, which is due to the high resistance of the electrical path corresponding to the contact to the buried layer and to the collector pad (see figure 2.1). Figure 2.6b shows a safe waveform in blue and a destructive waveform featuring a snap-back in red. Despite a larger resistance, the safe waveform does not show a clamping of the voltage at the end of the pulse as in the BE case, which probably means that the parasitic capacitance is much smaller. In these measurement conditions, the I_{T2} of this device is 550 mA, which is low. Furthermore, looking at the red snap-back waveform in figure 2.6b, one can see that the device enters in snap-back in the middle of the pulse. The dissipated energy up to the snap-back is therefore less than the dissipated energy during the whole safe pulse. This rules out the hypothesis of a thermal damage. The snap-back is likely due to a purely electrical phenomenon, such as a parasitic BJT triggering or damage due to concentration of the current into one finger of the transistor.

2.1.2.3 Emitter-collector characterization

To complete the characterization of the transistor as concerns HBM type ESD between pairs of pins, a device was stressed in negative emitter versus collector. In the TLP-IV presented in figure 2.7, one sees a breakdown voltage of 7 V. This breakdown is smaller than the base-collector breakdown. This means that a transistor action takes place. The breakdown could be due to open base breakdown where the emitter triggers the BC breakdown by providing carriers [45, 46]. Alternatively the breakdown might be due to a punch-through phenomenon, in particular the base depletion region at the BC junction extends across the whole base to the emitter. This hypothesis is supported by the observation of an Early effect in DC. With further increase of the charging voltage, a non destructive snap-back is visible at V=11 V. It can be that the increased current makes a stronger injection from the emitter that provide the electrons for initiating the avalanche in the base collector junction. This is a feature of open-base breakdown.

With increasing current, the device builds a voltage until the second snap-back at V=11 V and I=1.63 A. Beyond the second snap-back the device degrades. As it can be seen in the green waveforms, the snap-back happens at the end of the pulse and has no visible effect on the leakage measurement. At slightly higher charging voltage, the device

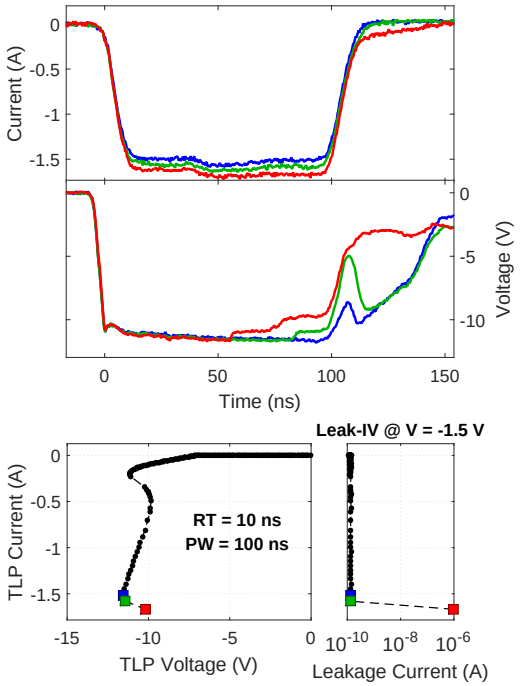


Figure 2.7: TLP IV of device A13 under E-vsC (negative stressing of the emitter versus grounded collector)

has an earlier snap-back and gets damaged. This is probably due to a thermal instability similarly as in [47] that concentrates the whole power into one finger, thus starting the thermal runaway in this finger. Given enough time in this inhomogenous configuration, this finger gets damaged. In any case the I_{T2} value for this device is more than 1.5 A.

2.1.2.4 Summary of the multifinger device ESD robustness and choice of study

Stress conditions	I_{T2}	type of breakdown	type of failure
B^- vs E	2 A	avalanche	thermal runaway
B^- vs C	600 mA	avalanche	electrical - unknown
E^- vs C	1.6 A	punch-through/open-base BD	thermal instability

Table 2.1: Summary table of the different junctions

Table 2.1 summarizes the TLP measurements of the HBT for all three configurations and the conclusions that were drawn from the analysis of the TLP-IV, the waveforms and the leakage measurements. The base collector stressing shows that this configuration is the least robust one for this transistor, and might be considered too low for some applications. This problem needs to be solved and will be investigated in details in the following.

2.1.3 Intrinsic and extrinsic Base-Collector failure modes

The first measurements of the base-collector junction in reverse by means of the TLP depending on pulse width, rise time, and substrate capacitive coupling to the probe station (or TIM setup), reveal a clear separation of two failure modes in the multifinger devices.

- One of these modes has a high value for I_{T2} ($\approx$ 1 A). This mode will be called "intrinsic". It takes place for long rise times ($\geq$ 10 ns).
- The other presents low I_{T2} failures that can be problematic for the use of the device, as it has been shown in the previous part. This mode will be called "extrinsic". It takes place for low rise times ($\leq$ 10 ns) or substrate coupling with the probe shield or a metallic sample holder. The failure example given in figure 2.6b is due to substrate coupling.

Stress conditions	$RT < 10ns$	$RT \geq 10ns$
Weak substrate coupling	extrinsic	intrinsic
Strong substrate coupling	extrinsic	extrinsic

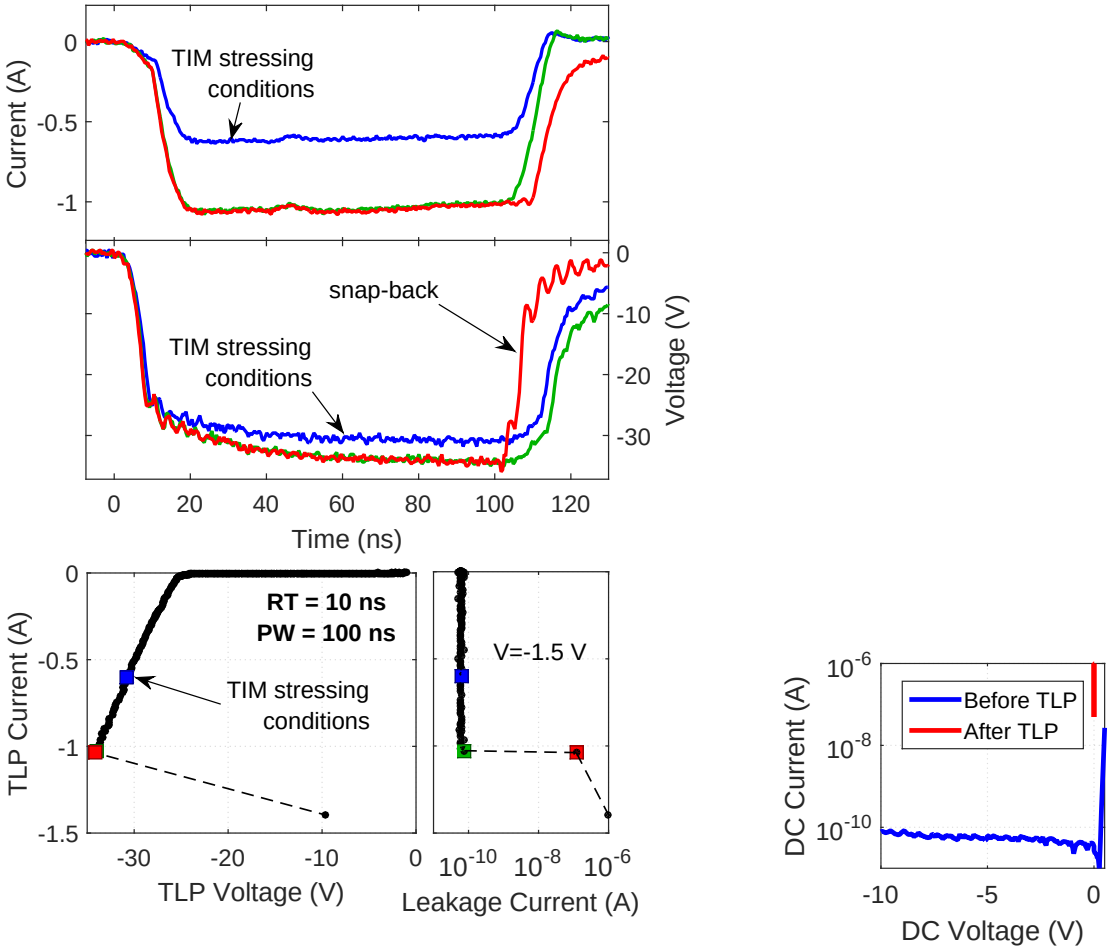
Table 2.2: BC failure observed modes

The differences between the intrinsic and extrinsic failure modes and the stressing conditions that are required to achieve each of them are summarized in table 2.2. The experimental conditions for each mode will be detailed in their dedicated part. For simplicity, the conditions themselves will sometimes be called "intrinsic" or "extrinsic", depending on the failure mode that is observed in this conditions, given high enough charging voltage of the TLP for the failure to occur.

2.1.3.1 Intrinsic mode

Figure 2.8a shows a negative base versus collector (B^-vsC) TLP-IV of the multifinger device for 10 ns rise time and 100 ns pulse width measured on an insulating holder. The I_{T2} value is 1 A. As the red waveforms in figure 2.8a show, the snap-back occurs at the end of the pulse, which is typically the sign of a thermal failure. The leakage IV characteristics of the base-collector has been measured before and after the TLP stress, and is shown in figure 2.8b. Figure 2.8b shows that where the virgin base collector junction shows little leakage current in reverse, the measurement after the stress shows a very low ohmic characteristics.

Pulse width scaling in intrinsic conditions The goal of the pulse width scaling is to determine whether the snap-back is thermal by using a Wunsch-Bell methodology [48].



(a) TLP IV **(b)** Leakage IV

Figure 2.8: TLP IV and leakage IV of device A13 under reverse base collector conditions for RT=10 ns, PW=100 ns. The averaging window is 70-90 ns.

Figure 2.9 shows in the same picture the TLP-IV and the destructive waveforms for the multifinger device in floating substrate configuration under 10 ns rise time and various pulse widths and figure 2.10 presents the extracted parameters of these TLP-IVs. In the waveforms, one can see that the devices fail at the end of the pulse for all pulse widths. The relevant parameter to describe this failure is V_{T2}, as its value of 33 V seems independent of the pulse width, as it is shown in the TLP-IVs and in the summary figure 2.10b. The variation in I_{T2} with pulse width (figure 2.10a) is due to the breakdown current power dissipation that heats the junction, decreasing the efficiency of the avalanche breakdown, and thus leading to an increase of the on-resistance, which is shown in figure 2.10c. The I_{T2} value is therefore the consequence of the fixed V_{T2} value and the R_{ON} increase with time. This is seen in the power fit of the R_{ON} and the I_{T2} values versus pulse width that show opposite values (± 0.26). The breakdown voltage does not seem to be affected

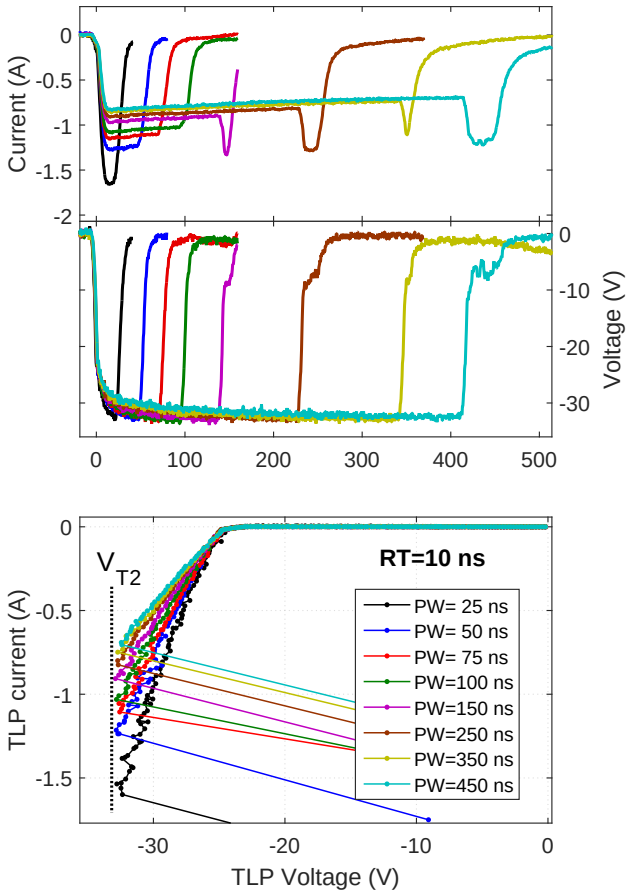


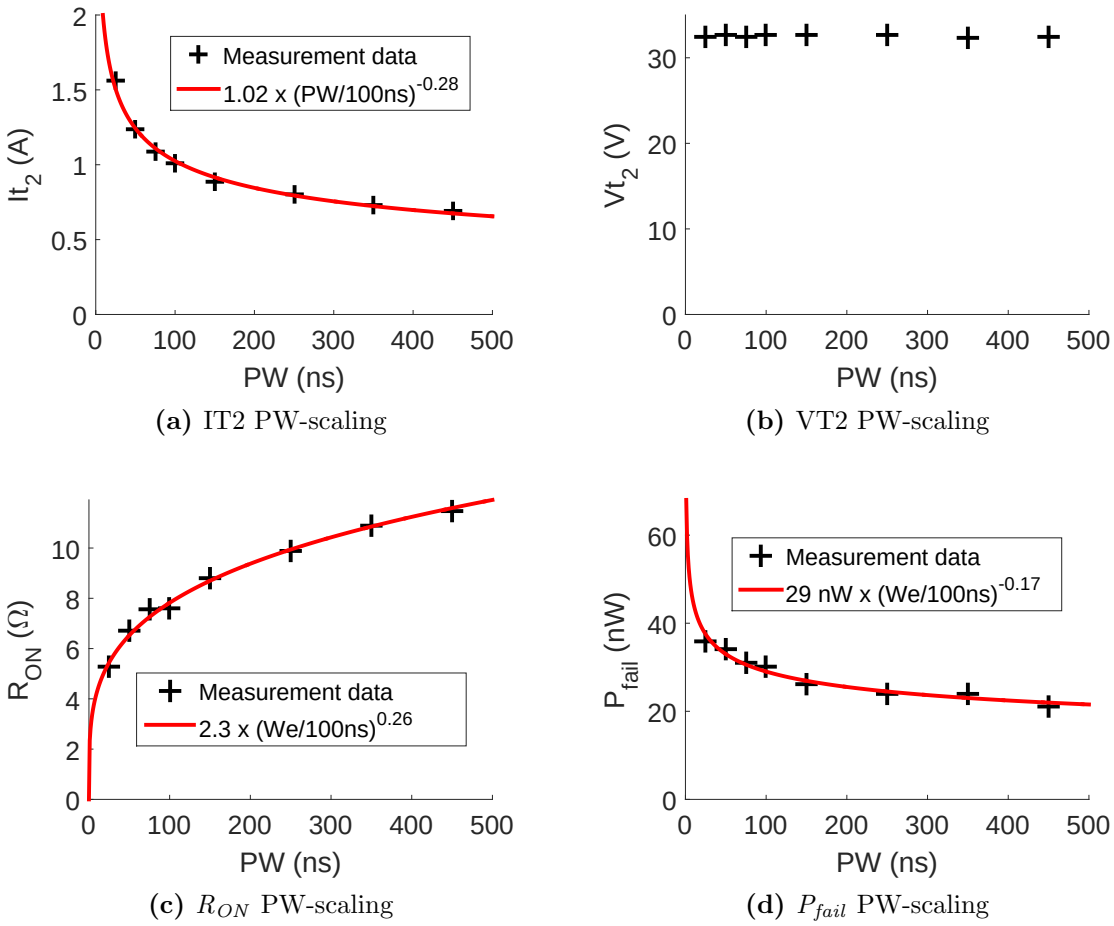
Figure 2.9: TLP IV and destructive waveforms for multifinger devices under $B^+ vs C$ conditions for 10 ns rise time and different pulse widths. The averaging window is 70-90% of the pulse width for all TLP-IVs.

significantly by the self heating.

Figure 2.10d shows the average dissipated power versus the time-to-failure, i.e the pulse width in this case. As the pulse width is increased, the decrease of the power is too weak to support the hypothesis of a thermal process in the time domain that is relevant to the HBM type of ESD. This means that identifying and solving the problem that causes the intrinsic failure could lead to a much robust device.

To summarize, the intrinsic mode is a purely electrically-caused snap-back which leads to a failure of the device as the voltage reaches a critical value. As the voltage increases during the pulse for thermal reasons, the snap-back always happens at the very end of the pulse (as showed for example in figure 2.8a), but it is not thermally driven.

TIM characterization of multifinger devices in intrinsic conditions The multifinger devices were submitted to the TIM experiments under the conditions that correspond to the intrinsic mode (10 ns rise time performed on insulating holder). The chosen current was 600 mA which is at a safe margin from the intrinsic $I_{T2}(\approx 1\ A)$. The point on the



(a) IT2 PW-scaling

(b) VT2 PW-scaling

(c) R_{ON} PW-scaling

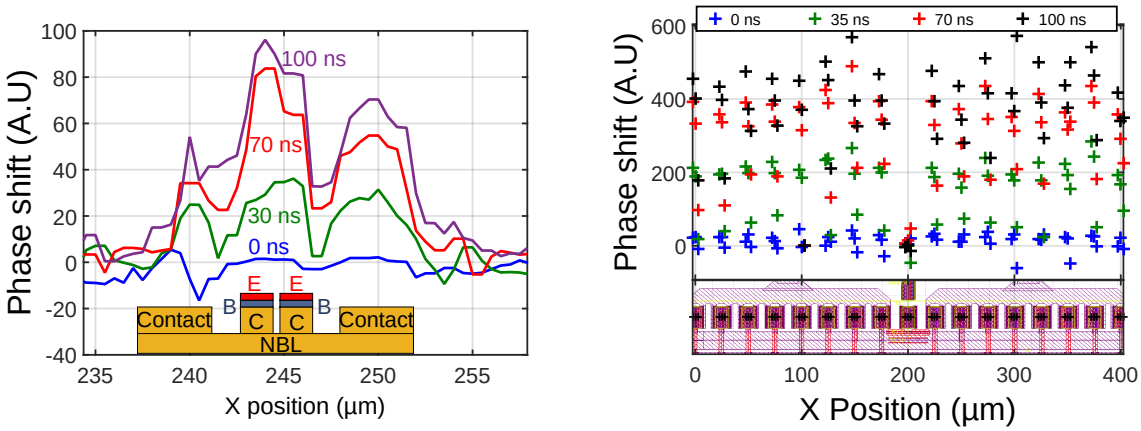
(d) P_{fail} PW-scaling

Figure 2.10: PW-scaling of TLP extracted parameters on multifinger devices

TLPIV and the waveforms are presented in blue in figure 2.8a.

The TIM data that is presented in figure 2.11a is the result of a scan that has been performed across the width of a double finger block of the multifinger device. At all time instants, there are 3 peaks in along the width direction of the device, at positions 240, 245 and 250 μm. The two external peaks are at the position of the connection to the NBL, whereas the central peak is at the position of both base collector junctions. The positive phase shift indicates that the change of the index of refraction is due to heat dissipation.

The phase shift is proportional to the integrated heat over the beam path (see part 1.4.2.1 for more details). The drawing at the bottom of figure 2.11a schematically shows the parts of the device where the current flows (more details in figure 2.1). As the contacts (n-doped silicon) are vertical, the beam probes a heated region for a longer part of its path, thus making one peak for each contact. Indeed, two peaks are counted for the external contacts (marked as "contacts to NBL" in figure 2.1), and two peaks that are merged into a larger one for the contacts to the active region (marked as C in the drawing at the bottom of figure 2.11a and as "NBL-CB contacts" in figure 2.1). The merging of the peaks corres-



(a) Detailed scan on one of the 16 double finger blocks of the multifinger device

(b) Scan featuring three points for each block

Figure 2.11: TIM scans in device A13 for PW=100 ns and RT=10 ns (intrinsic conditions), I=600 mA

ponding to the active regions is due to the small separation between the two fingers of about 3 μm, which is the thermal diffusion length value at 100 ns in silicon [49]. Between the peaks (at positions 243 and 247 μm), the phase shift signal is weaker because the part of the optical path that is dissipating heat is only the NBL itself.

From this analysis it can be deduced that the heat dissipation is roughly homogeneous in all the collector and sub-collector regions, i.e the NBL and the n+ contacts, and the collector n-silicon itself.

Figure 2.11b shows the TIM phase shift in few points in every double finger block of the multifinger device, namely the three peaks positions from figure 2.11a. Except for the central block, which is not contacted, the height of the peaks of the blocks are roughly similar, so it is deduced that all blocks share the power dissipation equally. This is expected, as the heat dissipation has a negative feedback on the current inhomogeneity under avalanche breakdown conditions [50].

Emitter width scaling in intrinsic conditions To further collect evidence on the intrinsic failure mode, it was chosen to perform TLP stressing of single-fingered test structures with different emitter widths. The device substrate was externally connected to the emitter with a flexible pitch set to mimic the connection scheme of the multifinger devices. The results are presented in figure 2.12. It can be seen on the TLP-IV that the breakdown voltage has a very low dependence on the emitter width. The waveforms show that the snap-back happens at the end of the pulse, although for the narrower width devices the snap-back occurs around 80 ns. This is compatible with the hypothesis of the critical voltage, considering that the voltage at the end of the waveform is quite flat with time. The charging voltage step that was used for the pulser is therefore larger than the increase

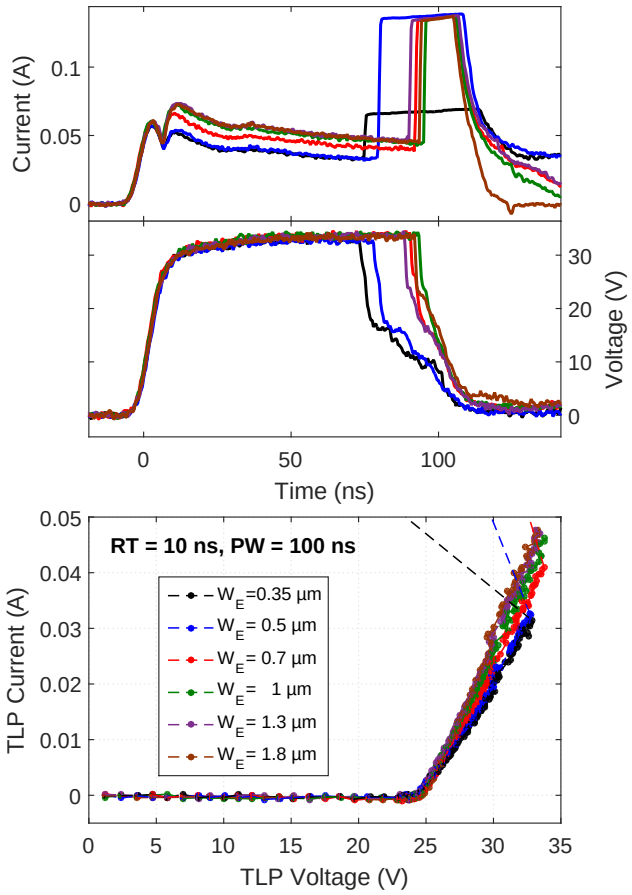
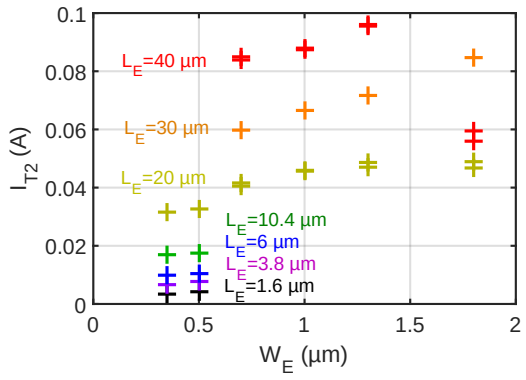
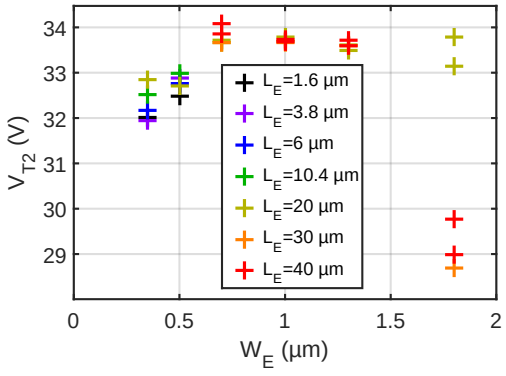


Figure 2.12: TLP IV and destructive waveforms for test structure devices with 20-μm-long emitter and various emitter widths under C^+vsB conditions for 10 ns rise time and 100 ns pulse width. The averaging window is 70-90 ns.

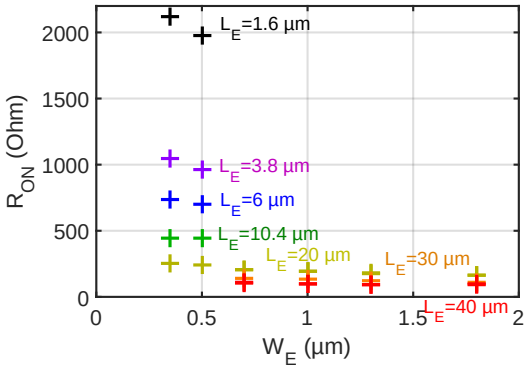
of the voltage in the last 20 ns of the last safe charging voltage. This makes the snap-back voltage the highest voltage that is reached in the whole series of pulses. Furthermore, the device has much higher impedance than the multifinger device and therefore creates positive voltage reflections in the transmission line that can be reflected back to the device, thus overcoming the snap-back voltage of the device before the end of the pulse. The possibility of having an extrinsic failure mode at the end of the pulse in the test structure is not completely excluded, as the test structure devices may be subject to very different parasitics as the multifinger devices. However, the TLP-IV of the single finger test structure with W_E=0.5 μm is almost exactly identical to the multifinger device when the current is rescaled to the total number of fingers (2 $\times$ 16 fingers), and in particular the V_{T2} of this test structure is also 33 V. This gives strong evidence that the breakdown and the snap-backs in the test structures and in the multifinger devices are due to the same mechanism. This, in turn, shows that this mechanism does not require the presence of several fingers to take place, as for thermal instability [51]. Figure 2.13 shows the extracted parameters for the structures whose TLP IVs and waveforms are presented in



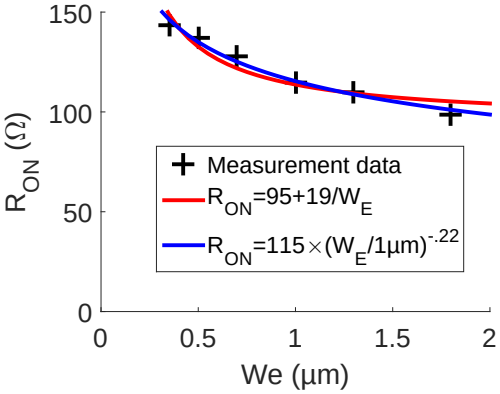
(a) IT2 W_E-scaling



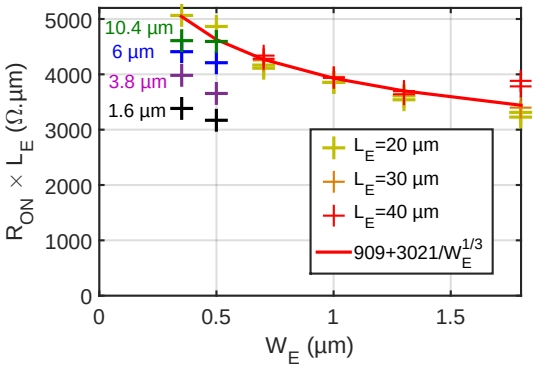
(b) VT2 W_E-scaling



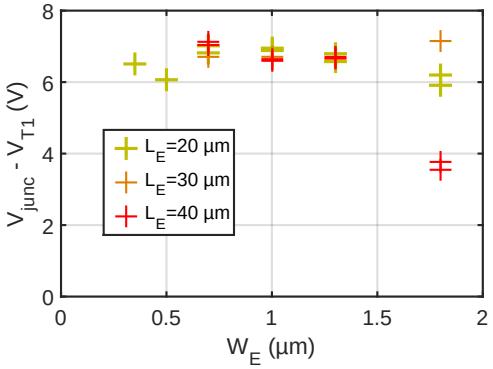
(c) R_{ON} W_E-scaling



(d) R_{ON} W_E-scaling for $L_E = 20\ \mu m$



(e) $R_{ON} \times L_E$ W_E-scaling



(f) Extracted junction voltage W_E-scaling

Figure 2.13: W_E-scaling of extracted parameters on TS devices with L=20 μm

figure 2.12, alongside the parameters for the test structures of other available emitter length.

Figure 2.13b shows the emitter width dependence of the V_{T2} for all transistor length. Notice that the voltage scale covers few volts around 33 V. At first glance, there is no clear trend for the relation between V_{T2} and the emitter length that works for all emitter

width values. However, it seems that the V_{T2} increases with the emitter width, at least up to 0.7 μm(see figure 2.13b). There are 3 devices with long and wide emitter that have a relatively low V_{T2} (see the three points on the bottom right of figure 2.13b). For the devices with L_E=30 μm, this low V_{T2} is also correlated with a lower ON-conductance.

The dependance of the ON-resistance is shown in figure 2.13c. The ON-resistance of the device is roughly inversely proportional to the device length, but depends very little on the device width. This can be explained by considering that most of the resistance of the base-collector breakdown comes from the contact to the collector. This is shown by the TIM scan in the single block, where most of the power dissipation is found in the collector contacts (see part 2.1.3.1). By design, the dimension of this contacts are scaled with the device length, but not with the width. The size of the BC junction itself, however, is the emitter length and width. Equation 2.1 describes a proposed model for the dependence of the ON-resistance with the dimensions of the device. The first term corresponds to the contacts and is inversely proportional to the emitter length. The second term describes the junction and is inversely proportional to its area. The emitter length can be factorized.

$$R_{ON} = R_{cont} + R_{junc} = \frac{r_{cont}}{L_E} + \frac{r_{junc}}{L_E \times W_E} = \frac{1}{L_E} \times (r_{cont} + \frac{r_{junc}}{W_E}) \tag{2.1}$$

and:

$$V_{junc} = V_{T1} + R_{junc} \times I \tag{2.2}$$

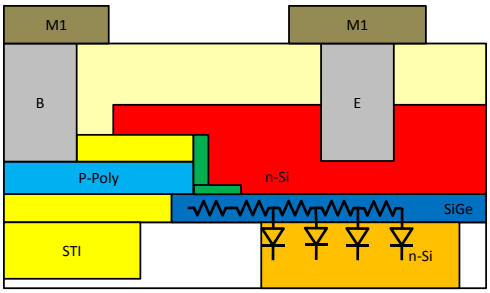


Figure 2.14: Schematics of the device in the width direction with distributed base resistance

Figure 2.13e shows the ON-resistance rescaled to the emitter length. For low emitter lengths, one can see that the R_{ON} values do not collapse, and the device have lower resistance than the model predicts. When the emitter length becomes small, the value of the perimeter of the junction becomes increasingly different from the value corresponding to twice the length. This dependence of the resistance on the length could therefore be the sign that the device mostly conducts at the edges of the base. This can be explained by the effect of a distributed base resistance in the thin SiGe layer, which is represented in the schematics in figure 2.14. Due to the flow of the current in the base resistance,

the voltage is larger at the edge of the junction than in the center. As the differential resistance of the junction itself is very low, this results in the concentration of the current at the edge of the junction. As a consequence, having a larger width does not allow more current in breakdown as it only adds a central region where the current cannot flow. This makes the perimeter a relevant scaling factor for low emitter length. This also explains why in figure 2.13d, the dependance of the junction resistance with the emitter width is better fitted by a sub-linear term than by a model corresponding to equation 2.1.

Figure 2.13e shows that for the large value of L_E, an inverse cubic root term inserted in the model at the place of a inverse linear dependence on the emitter width of the junction resistance ($R_{junc} = r_{junc}/W^{1/3}$) fits fairly well the data. By computing the junction voltage according to equation 2.2 using I_{T2} as a current, a junction failure voltage is obtained and plotted against the width in figure 2.13f. The failure voltage of the junction is roughly equal to $V_{junc}(I_{T2})=V_{T1}+R_{junc} \times I_{T2}=30$ V for all devices, without much dependence on the emitter width. This shows that there is a critical junction voltage that is independent on the length and width. The increase of the V_{T2} with W_E observed in figure 2.13b is due to the slight decrease of the junction resistance with the emitter width, which causes an increased current flow in the contact resistance, whose value depends solely on L_E. This critical junction voltage should drop between two points on each side of the base collector junction.

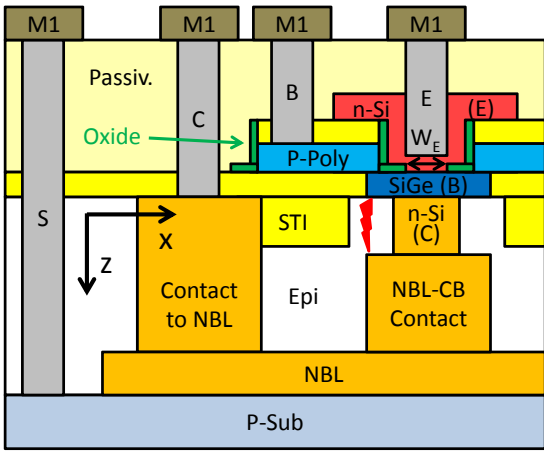


Figure 2.15: Schematics presenting the hypothesis for intrinsic mode failure

Figure 2.15 presents the hypothesis that is made to link all these pieces of evidence. The failure is likely due to the breakdown of the silicon between the edge of the base and the corner of the contact marked as NBL-CB in figure 2.15, where the electrical arc is schematically drawn. This breakdown would start at a precise voltage near 30 V. V_{junc} is identified to the collector n-Si and the SiGe (i.e the part that the arc short-circuits), and V_{cont} is identified with all the rest of the base-top-collector path (i.e p-poly, sub-collector regions and contacts).

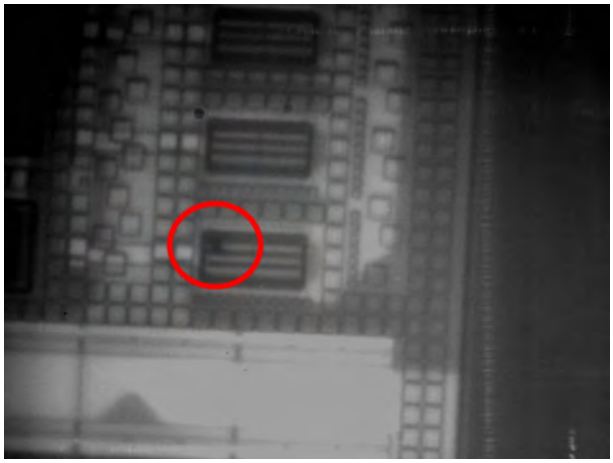
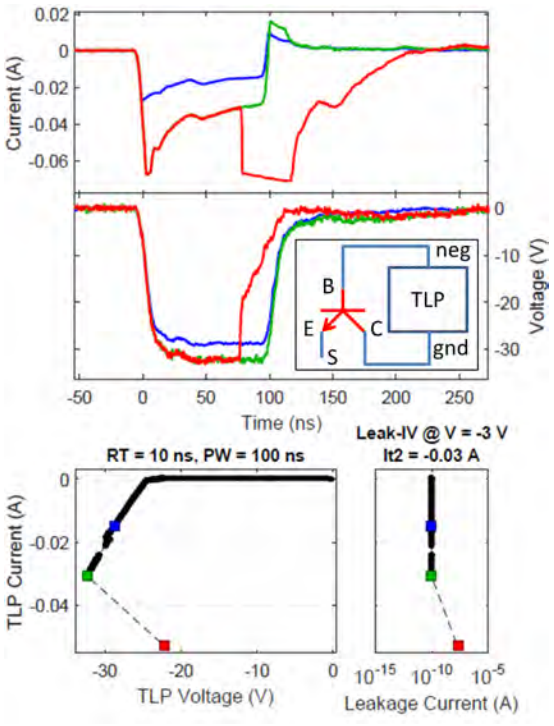
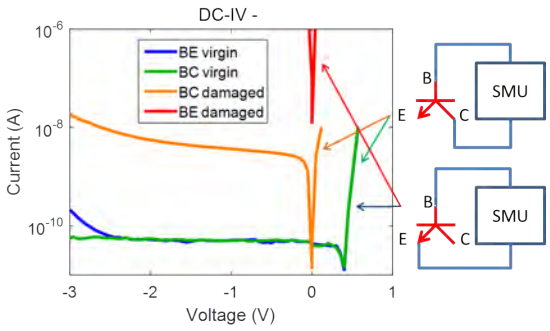


Figure 2.16: Damage signature for a intrinsic mode damage in the multifinger device seen with backside infrared microscopy



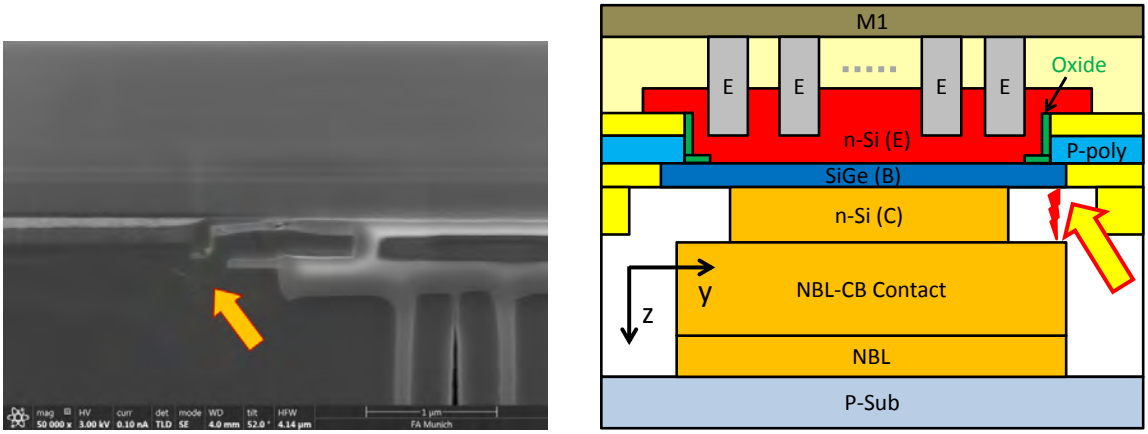
(a) TLP IV and damaging pulse



(b) Leakage of both junctions before and after low energy damage

Figure 2.17: Stressing conditions for the intrinsic low energy damage

Failure analysis of the intrinsic failure With measurements of the leakage DC-IV of both base-emitter and base-collector junctions before and after TLP stressing of the devices, it has been found that both intrinsic and extrinsic failure modes lead to an increased leakage in both junctions, as shown in figure 2.17b, where both junctions are leaky after the stress of the base collector. This could be due to the very low thickness



(a) SEM picture of the damaged device

(b) Schematics of the test stucture along the length (YZ plane)

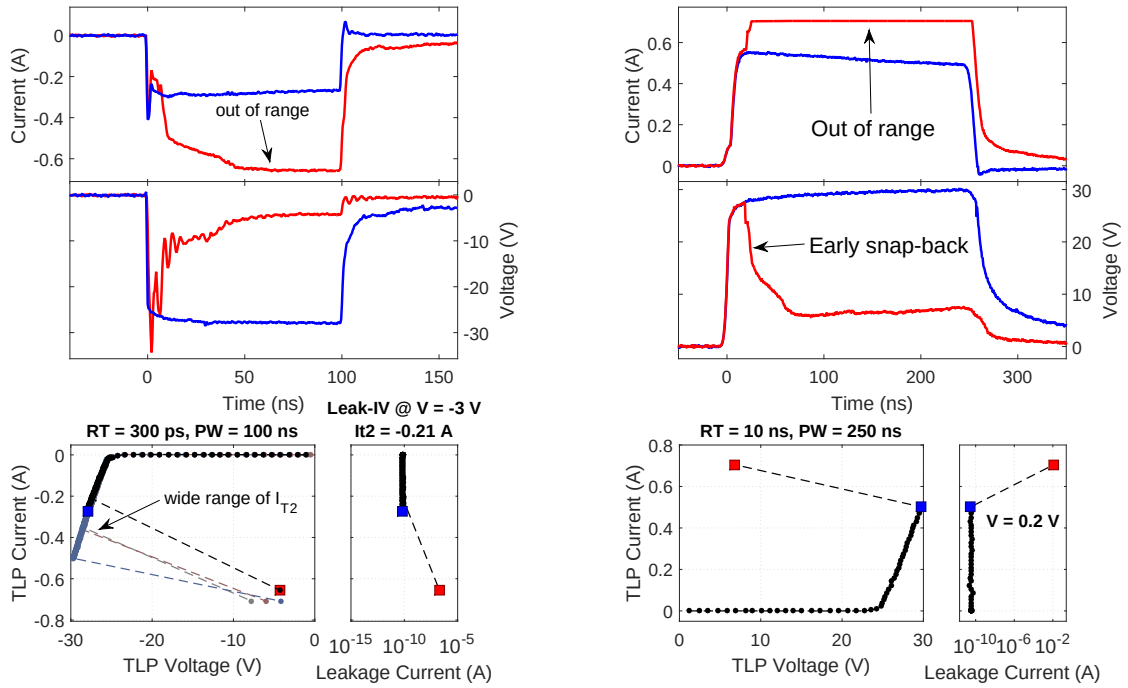
Figure 2.18: SEM image of the damaged device and schematics of the device along the length

of the base SiGe, which would enable a damage signature covering both junction, independently on which of the BC or the BE junction originally failed. Alternatively, it could be that both junctions suffer from a parasitic BJT triggering with a large current flowing from emitter to collector.

For the intrinsic failure mode in the multifinger devices, backside infrared microscopy (described in part 1.4.2.2) was used to analyze failed devices. Figure 2.16 shows a double finger block where a black spot is visible on one of the junctions in the middle of the red circle. The two junction areas are the two dark stripes in the middle of the blocks. This black spot is the sign of metal melting. This damage is too extended to be useful for a failure analysis. As the large current flow creating this damage is probably due to the discharge of the parasitic capacitance of all the combined parallel fingers, a single finger test structure device was used so that the damage signature be less extended, and leave evidence of the root cause of the failure.

The stressing of the device is presented in figure 2.17a, where it can be seen that the snap-back conditions at the end of the pulse and at high voltage correspond to an intrinsic mode. The device was sent for failure analysis in an industrial center where the location of the damage was first found with EMMI and Thermally Induced Voltage Alteration techniques (TIVA) [52]. The position of the damage was then imaged by a scanning electron microscopy on the deprocessed and FIB-cut device. The results are shown in figure 2.18. Figure 2.18a shows the SEM image where the arrow points on the damage that can be seen as a clearer mark on the background of the dark silicon. Figure 2.18b shows a schematics of the device along the length of the device (YZ plane) with the position of the damage. The position of the damage signature is marked by the arrow in figure 2.18b.

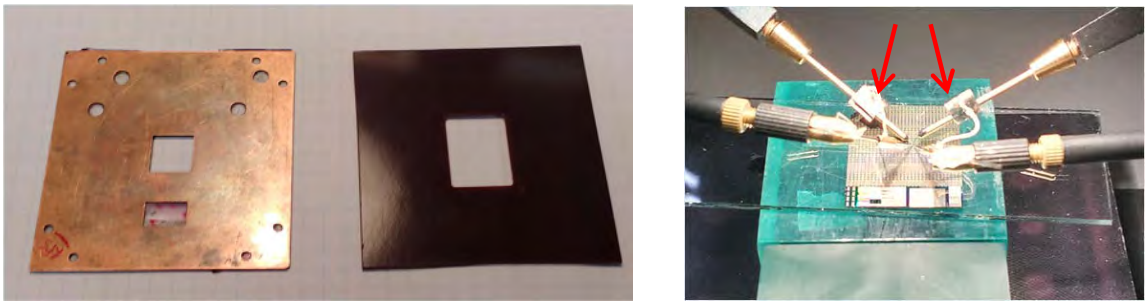
2.1.3.2 Extrinsic mode



(a) 300 ps rise time, insulated holder

(b) 10 ns rise time, coupled substrate to flexible pitch

Figure 2.19: Base-Collector TLP IV in multifinger device for two extrinsic conditions



(a) holders

(b) flexible pitch

Figure 2.20: Possible sources of substrate coupling leading to early failures

Extrinsic conditions Figure 2.19a shows typical extrinsic failures of the base collector. The I_{T2} is random and lower than the value of the intrinsic I_{T2} (1 A for the multifinger device). The other characteristics of the extrinsic mode is that the destructive snap-back occurs in the first nanoseconds of the pulse, as seen on the voltage and current

waveforms in figure 2.19a. In the multifinger devices, this type of failure happens in several configurations:

- When the rise time of the pulse is less than 10 ns. This is the case for the measurements presented in figure 2.19a
- when there is a large enough capacitive coupling of the substrate with the probe station. For example if the device under study is measured on a electrically floating metal holder instead of one made of an insulator, as shown in figure 2.20a for the TIM holders. The insulating holder on the right was made on purpose for these devices to avoid the coupling that was seen with the metalic holder on the left. Figure 2.20b shows a stress mode where needles connected to the shield of the probe using a flexible pitch clamp (marked by red arrow on the photograph) were used to connect the base. The TLP-IV in figure 2.19b shows that the device suffered from early failure in this conditions. We attribute this early failure to the additional stray capacitance between the substrate-emitter and these needles (C_{SP} in figure 2.4), since the mode that is observed using coaxial RF probe in the very same conditions of rise time and pulse width is intrinsic.

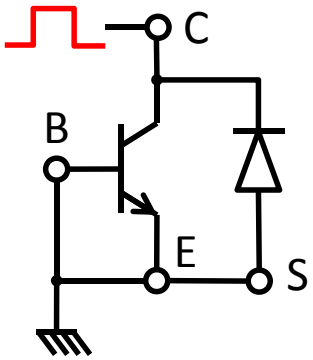
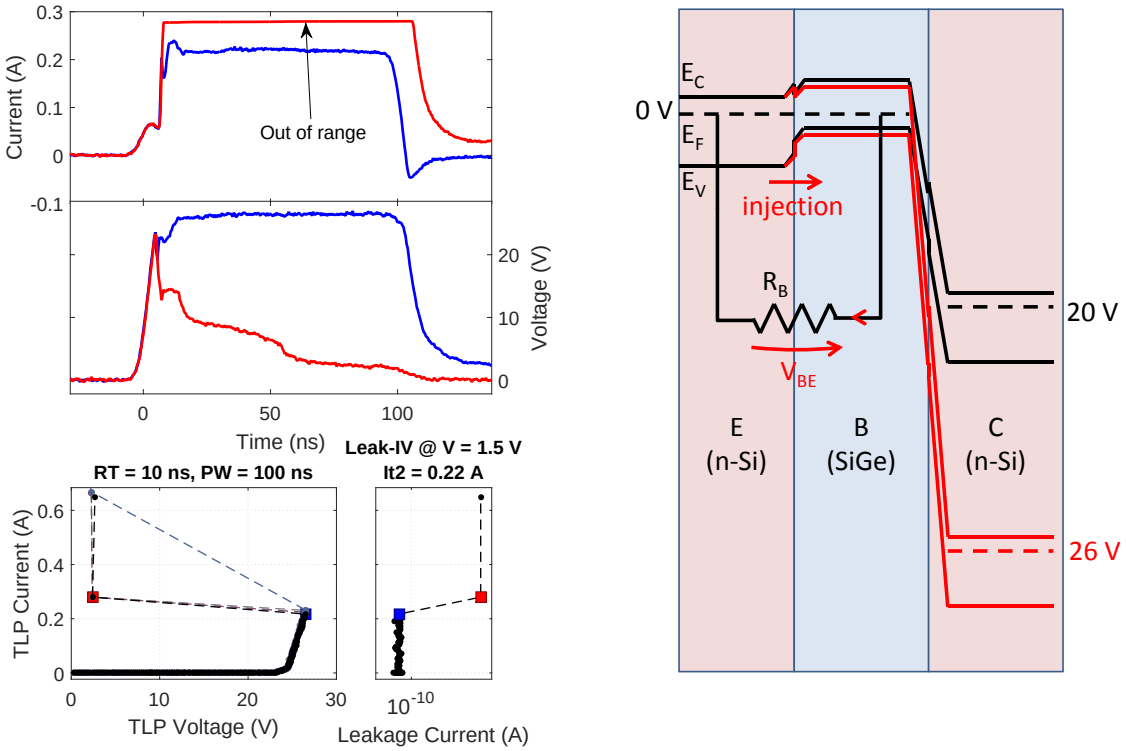


Figure 2.21: C^+ vs BE configuration

Grounding of the emitter during BC measurements As the substrate-emitter grounding conditions seem to be critical in the extrinsic failure mode, it was chosen to perform a TLP-IV of the C^+ vs B configuration while also grounding the emitter of the device as shown in figure 2.21. This condition is achieved by grounding the emitter with a needle that is connected to the shield (ground) of the RF coaxial needle. This condition will be referred as C^+ vs BE.

Figure 2.22a shows the TLP IV and the highest current waveforms of the multifinger device in this configuration. The TLP-IV plot shows the TLP-IVs of several devices in the same plot, demonstrating that the destructive snap-back conditions are reproducible within a very small window of I_{T2}/V_{T2}. The waveforms of the destructive pulse show a similarity with the waveforms of the extrinsic mode of the base-collector shown



(a) Last safe and damaging pulse, TLP-IV for averaging window 70-90 ns

(b) Band diagram of the device at below breakdown voltage (black) and in breakdown (red)

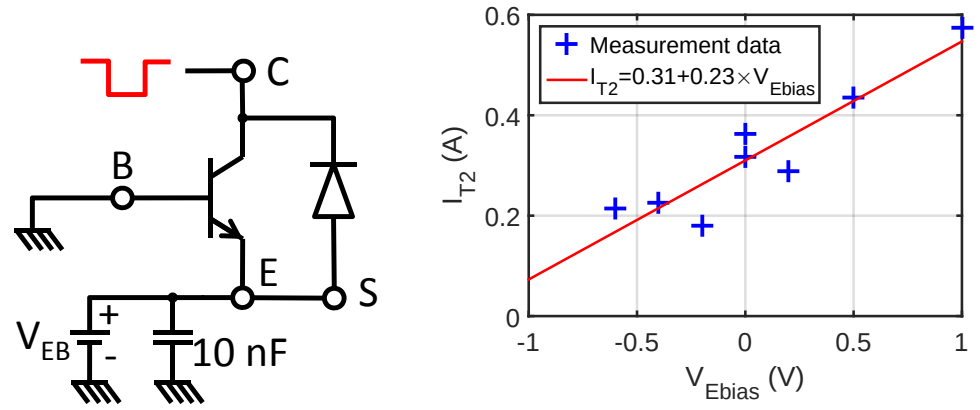
Figure 2.22: TLP IV and band diagram of the device under CvsBE conditions

in figure 2.19a, as in both cases the snap-back occurs at the beginning of the pulse. Furthermore, given the values of the I_{T2} for the C^+vsBE condition, and the values of I_{T2} on extrinsic failures (presented in figure 2.19a), it can be said that the grounded emitter mode is the worst case scenario (i.e lowest I_{T2}) of the extrinsic failures.

This triggering effect can be explained by taking into account the base series resistance to the ground (SiGe, P-poly and metals). When the base-collector voltage is below the breakdown voltage of 24 V, the current flow in the base is negligible, and the voltage drop between base and emitter is zero. Figure 2.22b shows the band diagram of the device in this condition in black with a voltage drop of 20 V.

At voltages higher than the base collector breakdown voltage, as the current is flowing in the base contacts, the voltage at the SiGe base rises, until the point where the base-emitter junction becomes forwardly biased so a snapback due to parasitic BJT occurs. This situation is shown in the red band diagram in figure 2.22b. At this voltage, the base-emitter starts to inject in the base-collector junction, thus triggering the parasitic BJT. This effect is very fast, as the base is very thin. The ON-resistance of the BE breakdown (figure 2.6a) gives an estimation of the base resistance of 1 Ω. The base emitter voltage

at the snap-back current is therefore roughly 300 mV. However, contacts resistance of 0.5 Ω with at the base and at the flexible pitch clamp bring an additional voltage to the BE junction of the order of 150 mV.



(a) Biasing circuit for the emitter **(b)** I_{T2} vs emitter bias

Figure 2.23: Biasing circuit for the emitter biasing during C^+ vs B stressing and I_{T2} dependence on the emitter bias.

Biasing of the emitter during BC measurements The experiment where the emitter is grounded was extended to a more general case where the emitter is biased at a fixed voltage. The biasing circuit is presented in figure 2.23a, where the 10 nF capacitor are included inside the custom made RF probe, whose shield is connected to the shield of the force probe of the TLP that pulses the collector and grounds the base. The I_{T2} dependence on the emitter bias is shown in figure 2.23b. The value at 0 V is the one that has been observed for the C^+ vs BE condition. The data shows that a negative bias of the emitter lowers the I_{T2}, which is consistent with the model that has been proposed to explain the triggering in the C^+ vs BE conditions. The resistance that is given by the linear fit is about 1/0.23=4.3 Ω. However, this low value should include the contact resistance of the base probe needle, the emitter probe needle and the clamp of the flexible pitch setup. The intrinsic base base resistance of the device might play little role, and this value might depend for a large part on the parasitics of the measurement setup.

Parasitics Figure 2.4 shows the parasitics of the device that could play a role in the extrinsic failure. All the conditions where the device fails in extrinsic mode could be linked to the extreme condition of the grounded emitter. Assuming a C^+ vs B condition:

- For short rise time (i.e high frequency), the large parasitic capacitance C_{BE} will behave as a short-circuit and clamp the emitter voltage to the ground during few nanoseconds, thus creating the conditions similar to a shorted base-emitter conditions.

- The clamping of the emitter to the ground can also happen for long rise time (i.e low frequency), given high enough parasitic capacitance C_{SP} from the substrate to the ground (i.e shield of the probe, or needle).

Depending on the rise time and the value of the stray capacitance C_{SP}, the emitter-base voltage could take a wide range of values, which can lead to a wide range of I_{T2} values, as the emitter bias dependence shown in figure 2.23b suggests. This could be the cause of the apparent randomness of the I_{T2} values that are observed for the extrinsic conditions.

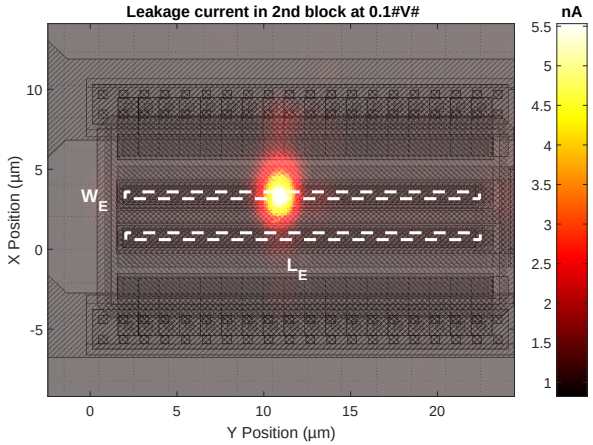


Figure 2.24: Example OBIC signal for an extrinsic mode damage in a multifinger device, aligned with the device layout. The dashed line shows the position of the emitter junction

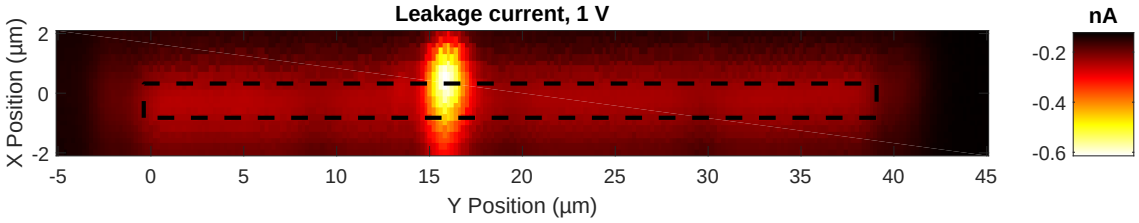


Figure 2.25: OBIC signal for an extrinsic mode damage in a test structure with W_E= 1.3 μm and L_E= 40 μm. The dashed line shows the position of the emitter junction

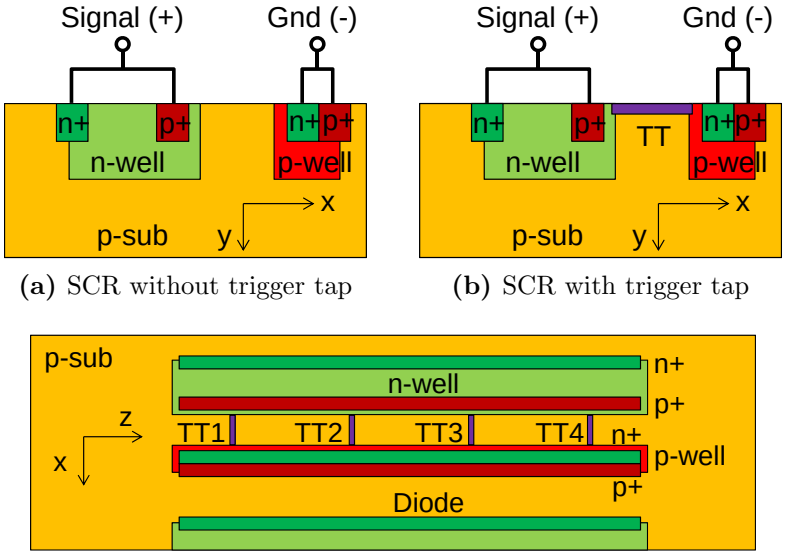
Failure analysis of the HBT in extrinsic mode The OBIC technique presented in part 1.4.2.4 has been used to characterize the multifinger devices damaged in C^+ vs BE, i.e the devices whose TLP-IV is shown in figure 2.22a. Figure 2.24 shows the OBIC image of the device. It can be seen that the damage signature is in the center of a finger. However the OBIC resolution is not enough to locate the damage in the width dimension. In the multifinger device, the damage has been located in different fingers and at different positions for each measurement.

In order to see the location of the damage in the width, a single test structure 1.3 μm-wide test structure that displayed extrinsic damage was analyzed with OBIC. The result is shown in figure 2.25 where it can be seen that the damage is located at one side of the width. To gather more evidence on the failure signature, failure analysis should be applied.

2.2 SCRs as external ESD protections

2.2.1 Devices under study

The SCR devices that have been studied have been presented in [9]. They are shown in figure 2.26a for the SCR without trigger tap and figure 2.26b for the SCR with trigger tap. A top view of the device with trigger taps is shown in figure 2.26c. The trigger taps are four p implants in the 45 μm width of the device, that have been placed so that every one of them is in the center of its 11.25 μm-wide region of the SCR width. The devices with trigger taps have 10 fingers in parallel, whereas the device without trigger taps are single finger test structures. The side where the tap is located is called the "SCR side", as the PNPN structure is on this side. The other side will be called the "diode side" as its function is to block the current when the voltage is positive, and to let the current flow when the voltage is negative, as there will be no useful negative voltage signal for the protected device (typically USB uses 0 to 5 V).



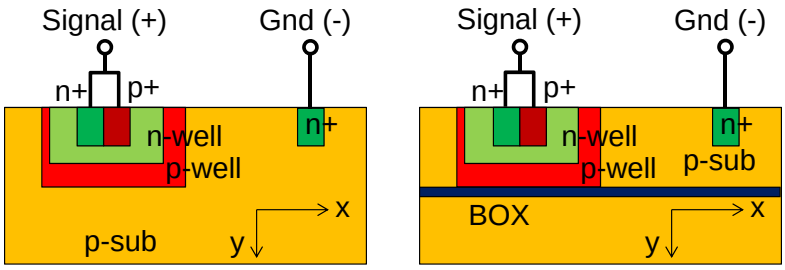
(a) SCR without trigger tap

(b) SCR with trigger tap

(c) SCR with trigger tap, top view

Figure 2.26: Schematic view of SCRs without and with trigger tap

The open base SCR device (ob-SCR) concept is shown in figure 2.27a for the bulk technology and in figure 2.27b for the SOI technology. The "open base" is the base of the PNP transistor, i.e the p-well, which is floating as shown in figure 2.27, contrary to the standard design where the bases of both transistors are contacted, as shown in figure 2.26.



(a) Bulk **(b)** SOI

Figure 2.27: Schematic view of open base SCRs on Bulk and SOI

2.2.2 Study of the trigger taps behavior in breakdown and triggered modes in SCRs

The study presented in this part has been published in [53] and presented in [54].

2.2.2.1 DC EMMI analysis of the SCR

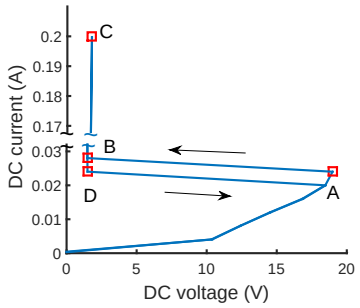
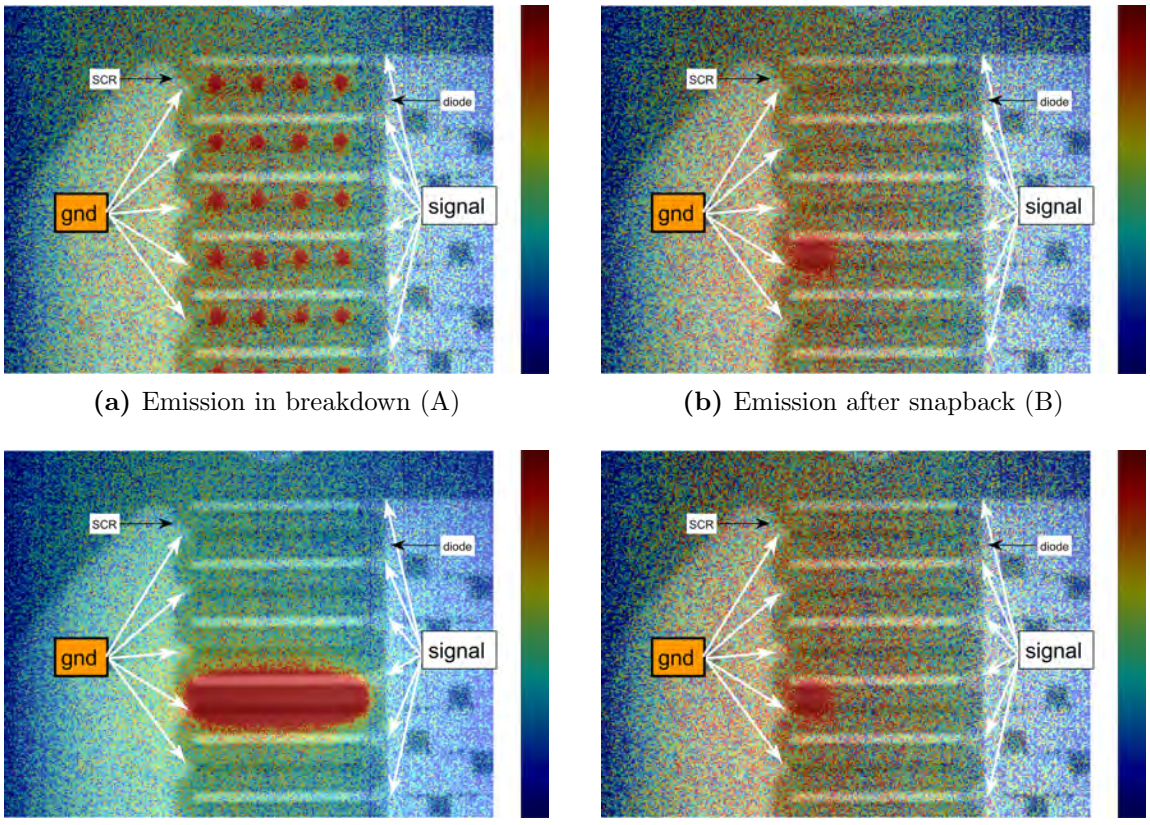


Figure 2.28: DC-IV of the SCR device in current controlled mode

The DC EMMI technique (shown in part 1.4.2.3) has been used to see the action of the trigger taps in breakdown mode and to look at the finger activation in DC current-controlled mode. Figure 2.28 presents the results of the EMMI by overlapping two pictures: one is the backside image of the device lit by a broadband infrared light shown with a back and white color map, and the other is the emission signal given with a "Jet" color map, as the color bar on the side of the pictures indicates. Both pictures have been taken at the same position with the same focus settings, so they are perfectly aligned. As seen in figure 2.28 the DC current was swept from 0 to 200 mA and back with a step of 2 mA. The device shows an hysteretic behavior which is typical for devices with negative differential resistance [55]. Following the value of the current with time, the measurement starts with a low current condition where the device is in breakdown, i.e the current is forced through the reversed junction of the nwell/trigger tap. This mode lasts until the current reaches 26 mA, and marked as A in figure 2.28. At this point the EMMI pattern



(a) Emission in breakdown (A)

(b) Emission after snapback (B)

(c) Emission at high current (C)

(d) Emission at holding current (D)

Figure 2.29: Emission patterns depending on the IV-conditions.[53]

is as shown in figure 2.29a. This pattern shows a strong emission from the trigger taps, in particular on the cathode (gnd) side. This could mean that the trigger taps are depleted along their whole length.

It is therefore shown that all the current flows in the taps in breakdown, which means that a sufficient number of trigger taps are needed to sustain the high current before the triggering of the device. The highest current (resp. voltage) in breakdown is called the triggering current I_{T1} (resp. voltage V_{T1}). Here I_{T1}/V_{T1} is 26 mA/18 V.

Slightly beyond the triggering current (28 mA, point B in figure 2.28), the emission pattern is as shown in figure 2.29b. The trigger taps do not emit anymore, and only one finger is emitting, although partially. The emission is due both to the forward current in the pn junction in the pwell and pn junction in the nwell, as the emission pattern is spread in the length of the finger ($\vec{x}$ direction). This experiment shows the inhomogeneity of the current density in triggered mode, which is a well known phenomenon in spatially extended systems with a negative differential resistance [56, 57].

With increasing current in snap-back regime, the emitting region spreads. Figure 2.29c shows the emission pattern corresponding to 200 mA (point C in figure 2.28). The emitting region now covers most of the finger that was already emitting at 28 mA. Attempts to

further increase the current level have lead to the damage of the device, so it seems that a transient voltage (e.g TLP or HBM pulse) is necessary to trigger more fingers. When lowering the current, the emission region shrinks, until the lowest current that can be sustained in snapback called the holding current I_h, which is 24 mA for this device (point D in figure 2.28). The corresponding emission pattern is shown in figure 2.29d, where the emission width is slightly smaller than the emission corresponding to B. The holding current is therefore flowing only in one finger, and only in one part of it, which means that it will not be possible to scale it by having less fingers. The width of the emission at I_h in this device is the maximum width where the I_H can be constrained for this technology. This tool can be applied to other technologies to assess the value of this critical width, and be inserted in the development loop of SCRs technology.

2.2.2.2 TIM analysis of the SCR with trigger taps

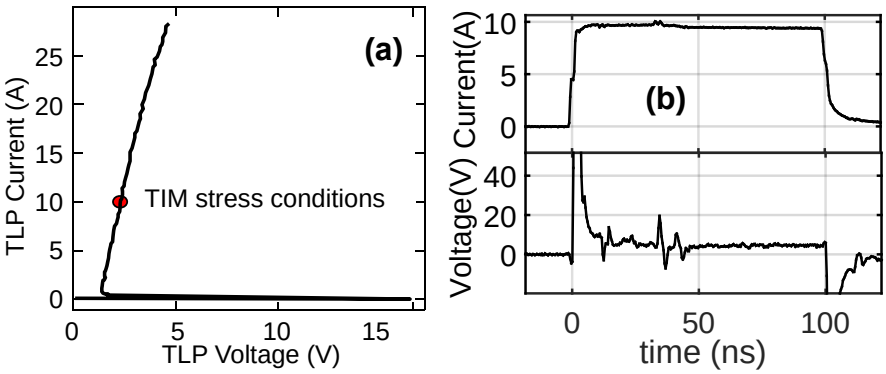


Figure 2.30: TLP IV of the SCR device with trigger taps (a) and waveforms from the TIM experiment (b).[53]

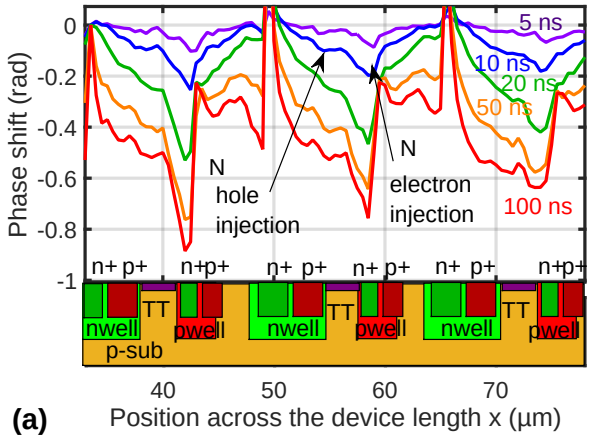


Figure 2.31: Phase shift profile along the length of the device [53]

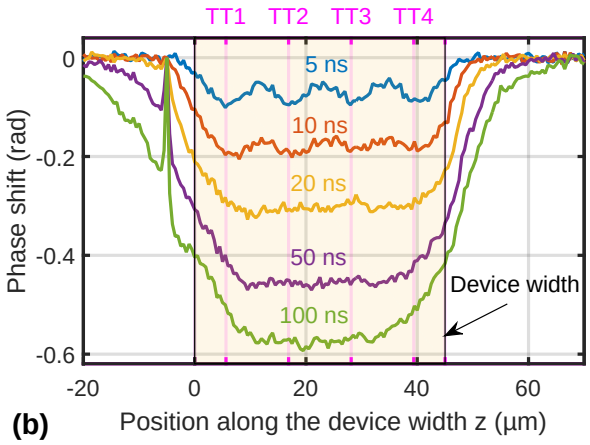


Figure 2.32: Phase shift profile along the width of the device [53]

The role of the trigger tap has been studied using the TIM method described in part 1.4.2.1. The device was stressed by a TLP pulse with 500 V charging voltage, 100 ns pulse and 300 ps rise time. The pulse waveforms are given in figure 2.30, along with the TLP-IV of the device. The voltage peak at the beginning of the voltage waveform is due to the incident pulse, as the the measurement has been performed on the TIM setup with 2-point probes. The I_{T2} of the device is not reached at 30 A.

Two scans have been performed, along the length of the device across 3 fingers in the middle of the width, and along the width of the device across the four trigger taps.

Figure 2.31 shows the phase shift versus the position along the path for several time instants during the pulse. The diodes are marked with the N. The negative phase shift shows that the probed signal is the integral of the free carrier density along the beam path. We can see that the main negative peaks are aligned with the n+ contacts of the signal pad which is the sign of an electron injection in the p-well and the p-substrate. There is a second peak that is mostly visible at 5 ns, which is aligned with the p+ contact in the n-well. From previous studies in the diffusion of carriers and heat [43], we can say that these two injection sources are the only ones and the widening of the peaks is mostly due to the diffusion. The diode side is therefore inactive. As the holes are majority carriers in the p-substrate, the TIM technique will not probe them there (see part 1.4.2.1), but only in the n-well. On the oposite, the electrons are probed much further in the substrate where they diffuse. This explains why the peaks at the n+ contacts are larger.

Along the width of one finger (at $X = 56\ \mu m$ on the axis of figure 2.31), the phase shift profile is as shown in figure 2.32. At 5 ns after the pulse beginning, one can see the injection of free carriers by all four of the trigger taps in the form of small negative peaks on the width of the SCR. This shows that the trigger taps have to sustain quite a lot of current on their own at the beginning of the pulse, which is the reason why they are so numerous, despite their contribution to the capacitance of the device [9]. At 10 ns, we see that the peak get smaller whereas the background free carrier signal still increase. At 20

ns the taps are not injecting anymore. Although the measurement is able to detect the activation of a trigger tap, the measurement of the on state spreading on a such a short distance is not very precise.

2.2.3 On-state spreading in SCR devices

The study presented in this part has been published in [53].

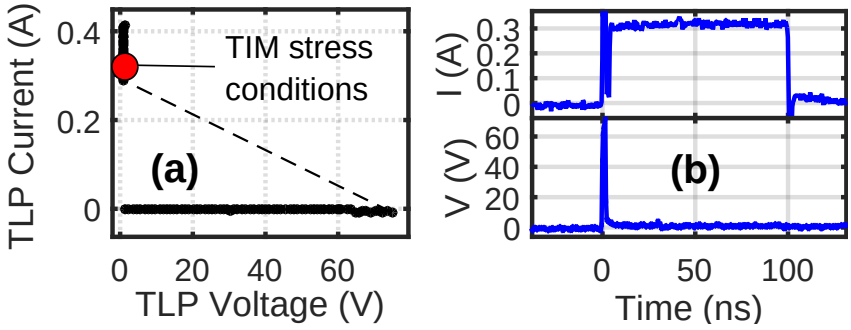


Figure 2.33: TLP-IV of the test structure without trigger tap and waveform at the current level used for the TIM scan. [53]

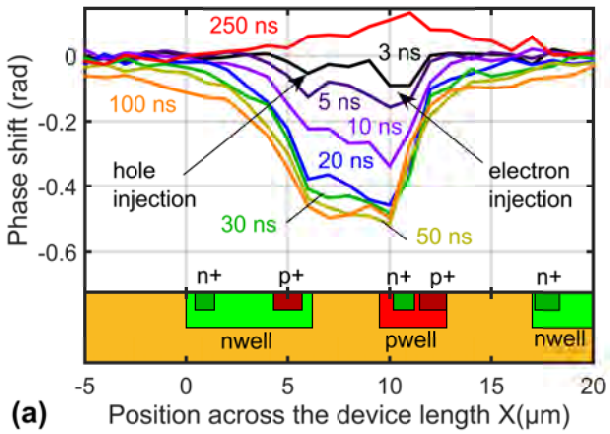
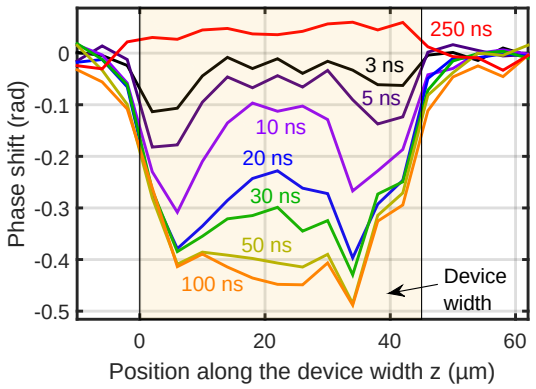
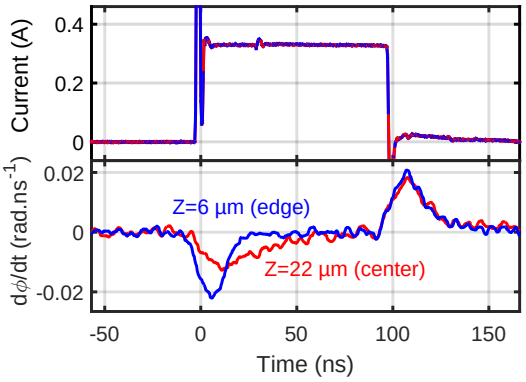


Figure 2.34: Phase shift profile along the length of the device. [53]

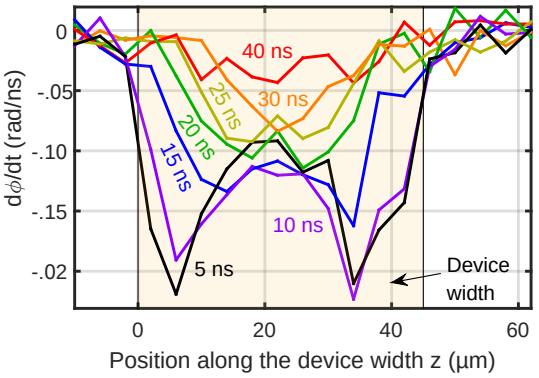
The experiment that was carried out to see the on state spreading in a SCR was performed on a SCR device without trigger tap to have a large enough width to be able to see it and measure its speed. This device is depicted in figure 2.26a. It has a V_{T1} of 70 V, which means that the minimum achievable current in snap-back with a 50 Ωload line is 1.4 A. As the device is a test structure with only one finger, it is necessary to have a large resistance in series with the device to be able to access the low current part of the device IV that would correspond to the same current density in a 10 finger device. The High Impedance Transformer is limited in term of rise time by its distance to the device. Instead, a 300 Ω resistor was brought by replacing the standard 50 Ω probe needle with



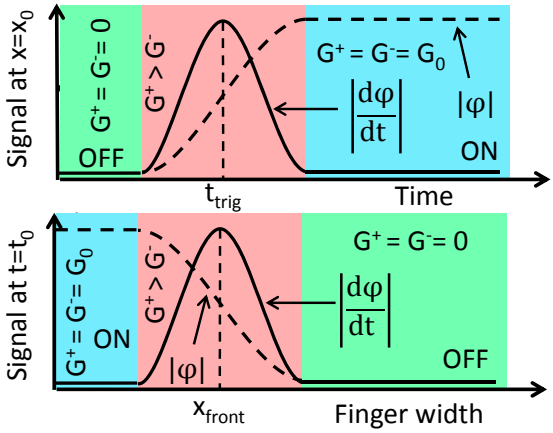
(a) Phase shift profile along the width



(b) $\frac{d\phi}{dt}(t)$ waveform (edge and center)



(c) $\frac{d\phi}{dt}$ profile along the width

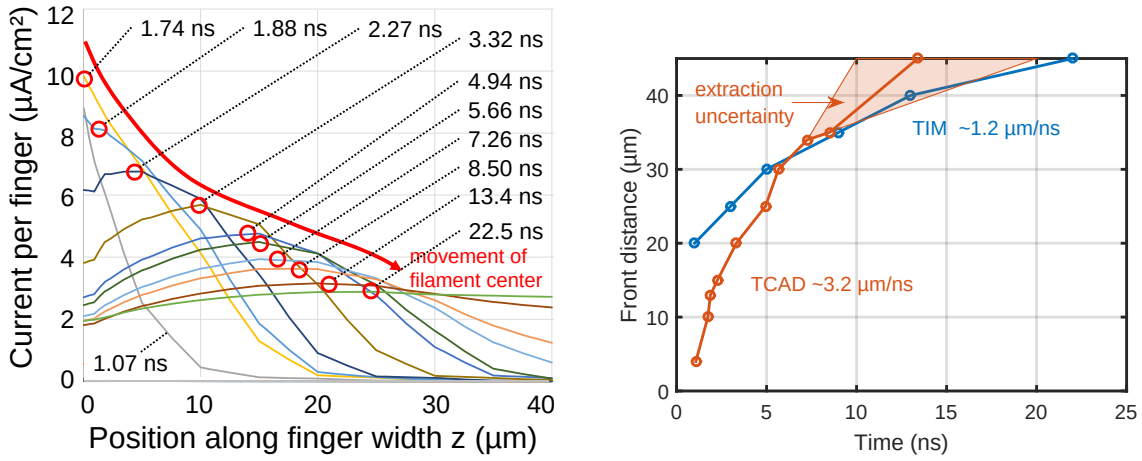


(d) Schematic view of $\frac{d\phi}{dt}_{z=z_0}(t)$ (top) and $\frac{d\phi}{dt}_{t=t_0}(z)$ (bottom)

Figure 2.35: Measured phase shift versus position along the width (a), time derivative of he phase shift versus position (b) and time (c) for the SCR device under 300 mA, schematics at fixed position and fixed time (only in case of OSS for the latter) (d). [53]

a high impedance needle, which is normally used for voltage sensing. In 4 point probe mode, the voltage can directly be measured at the device pads with a 5 kΩ probe, so the current and voltage are well measured. Figure 2.33 shows the 4 point probe TLP-IV of this test structure, along with a waveform that corresponds to the conditions in which the TIM scan was performed, i.e at 300 mA.

One TIM scan was performed across the length of the device and another across the width. Across the length we see the injection peaks at the n+ contact in the pwell and the p+ contact in the nwell. This is quite similar to what is observed in the device with trigger taps, see part 2.2.2. The phase shift distribution between and outside these contacts, corrected for the vertical integration that the TIM technique introduces, is compatible with a diffusion profile of electrons, where the diffusion length corresponding to 100 ns is calculated as $\sqrt{\mu_n V_t/100\ ns} = 16\ \mu$m for a electron mobility $\mu_n = 1000\ \text{cm}^2/\text{s}$ in the



(a) 3D TCAD current flow

(b) Front speed versus time

Figure 2.36: Results of 3D TCAD simulations and comparison with the TIM results. [53]

p-substrate.

Along the width of the device (figure 2.35a), one can see with the phase shift distribution at 3 ns, that the injection starts at both edges of the device width, and the peaks then move to cover the whole device width. The initial injection at the edges of the width is attributed to the high electric fields at the corners [58], and the spreading of the free carrier is a sign of ON-state spreading. In order to analyze the ON-state spreading in the conditions of this experiment, a methodology has been developed, which is inspired by the power dissipation extraction method described in [43].

$$\frac{\mathrm{d}n}{\mathrm{d}t} = D\nabla^2 n + G^+ - G^- \text{ where } \quad G^- = n \times \tau(\vec{r}, I, V)^{-1} \tag{2.3}$$

As the TIM signal is a measurement of the carrier concentration (as detailed in part 1.4.2.1), the time derivative of the signal, which is plotted in figure 2.35c, can intuitively be thought of as a value proportional to the increase of the concentration of carriers, with a negative proportionality constant. A change of the carrier concentration $n(x, y, z, t)$ can be due to diffusion, injection and recombination, which is expressed in equation 2.3, D is the carrier diffusivity, G^+ is the injection and G^- is the recombination.

This model neglects the diffusion. The literature values for the electron diffusion constant in silicon of 36 cm^2/s at 300 K [59] and the measurement of the diffusion tails that are seen in the scan along the length of the device in figure 2.34 show that diffusion alone cannot reach the 45 μm of device width that the OSS phenomenon has to cover in about 30 ns. The recombination term G^- is assumed to be an increasing function of the carrier concentration of the type n/τ. The recombination lifetime is assumed to be very small, because the device is in ON-state. This means that the carriers are driven by drift to the opposite contacts where they are collected. This drift consideration the recombination lifetime voltage/current dependent. Furthermore, as it can be seen by the

two peaks at the contacts in figure 2.34, the diffusion is ambipolar, which might also affect the recombination lifetime.

Let us consider a fixed position in the width of the device as in figure 2.35d(top) and look at the behavior with time. At this position, the value of the time derivative of the phase shift is 0 as long as the device is in the OFF-state, which correspond to the blue area in figure 2.35d. Let us introduce a triggering event at this point. With a fast responding recombination source and no diffusion, it is expected that the free carrier density reaches a steady state soon after the triggering of the device, as the injection is quickly compensated by the recombination ($G^+ = G^- = G^0$). The time derivative of the phase shift in this ON steady state is therefore also zero, as in the green region in figure 2.35d. This means that the time derivative of the phase shift of any steady state - whether ON or OFF - is zero. During the transition (red region in figure 2.35d), as the recombination process reacts to the increase with a delay described by the carrier lifetime, there is a transient excess injection term, which can be seen as a negative value in the time derivative of the phase shift. Therefore, at any point of the width, a peak in the $\frac{\mathrm{d}\phi}{\mathrm{dt}}$ can be seen at the moment of the triggering at this point. In figure 2.35b are presented the measured waveforms of the time derivative of the phase shift at the left edge and at the center of the device width. One can see that both waveforms exhibit a negative peak of $\frac{\mathrm{d}\phi}{\mathrm{dt}}$ at the beginning of the pulse, with a slight delay and spreading of the peak for the waveform at the center, corresponding to the triggering of the device at these positions.

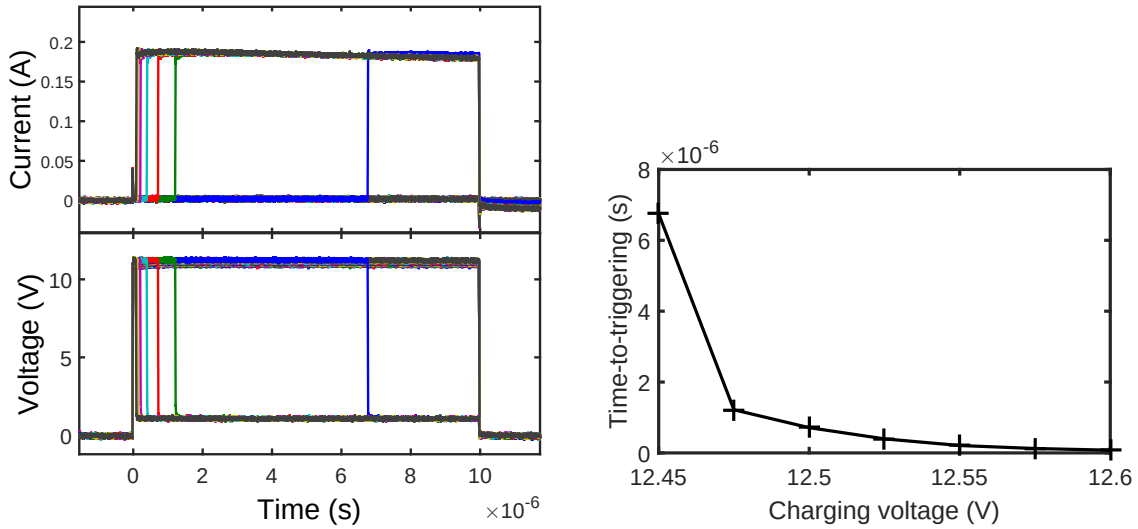
Now let us consider the width of the device as in figure 2.35d(bottom). From the previous conclusions one can can derive that the on-state spreading should look like a moving peak in the $d\phi/dt$ signal, as shows figure 2.35d when the time axis is replaced by the position along the width. Indeed, with increasing time, the peak corresponding to the triggering event is expected to travel the width of the device, having ahead of it an off-state region, and behind it an on-state region. This is what figure 2.35c shows, where two peaks start at the corner of the device, and meet at around 30 ns at the center. The decrease of the peaks during their travel to the center can be linked to the decreasing current density in the ON-state region and therefore the lowering of the injection G^+ at the front of the on-state spreading, due to the increase of ON-state width [60]. The spreading of the peak both in space and time could be due to the increase of the free carrier lifetime, as the current density and the voltage drop.

Notice that for both waveforms in figure 2.35b, at the end of the pulse, the time derivative of the phase shift also features a peak with a positive value on the same time and amplitude scale, which is the sign of an excess recombination. However, this time, there is no significant difference between the edge of the device and its center.

This results have been compared to the results of a 3D TCAD simulation performed by the company producing the device (Nexperia). In this simulation, the total current in the finger was 1 A. A trigger tap has been introduced at one edge of the device to force the triggering at this position. The current density distribution along the width for

several time instants in the pulse is shown in figure 2.36a. From these distributions, a front position was extracted for every time instant by taking the position of the full width at half maximum. The values are plotted in figure 2.36b, along with the data extracted from the TIM experiment. The estimated front of the simulated ON-state spreading has a speed of 3.2 μm/ns, wheras the TIM experiment gives about 3.2 μm/ns. Considering that the simulated current is more than 3 times more than in the TIM experiment, and that the TIM experiment shows an ON-state spreading from both edges of the devices, the values for the speed are in relatively good agreement.

2.2.4 Time-to-triggering in open base SCRs



(a) Waveforms **(b)** Time-to-triggering versus charging voltage

Figure 2.37: Waveforms and extracted time-to-triggering for the ob-SCR under 10 μs-long pulse near triggering voltage

The time-to-triggering was studied by applying long pulses to the ob-SCR device near the triggering conditions using a solid state pulser. The resulting waveforms are shown in figure 2.37a. For very small increase in the TLP charging voltage, the device triggering can be delayed quite a lot. This part shows how this behavior can be explained by a conductivity and electric field modulation of the p-sub part due to the injection from the contacts. First of all, since the device resistance in OFF-state is much higher than the TLP internal resistance, the device sees a constant voltage. The voltage across the device in the off-state is divided between the p-sub region, and the voltage across the n-well/p-well voltage, which needs to enter in avalanche breakdown to provoke an SCR triggering. As the voltage is fixed, the voltage divider between the p-sub and the junction can be affected by the modulation of the conductance of the p-sub. An injection of carriers in the p-sub will lead to such a modulation, which will increase the voltage on the junction

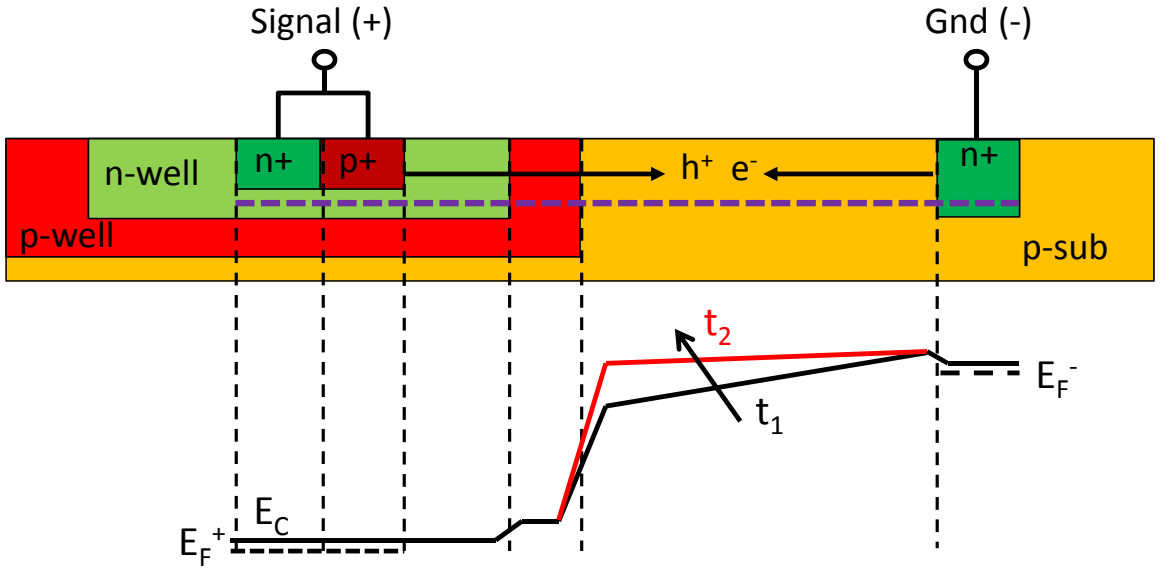


Figure 2.38: Schematic band diagram of an SCR in breakdown

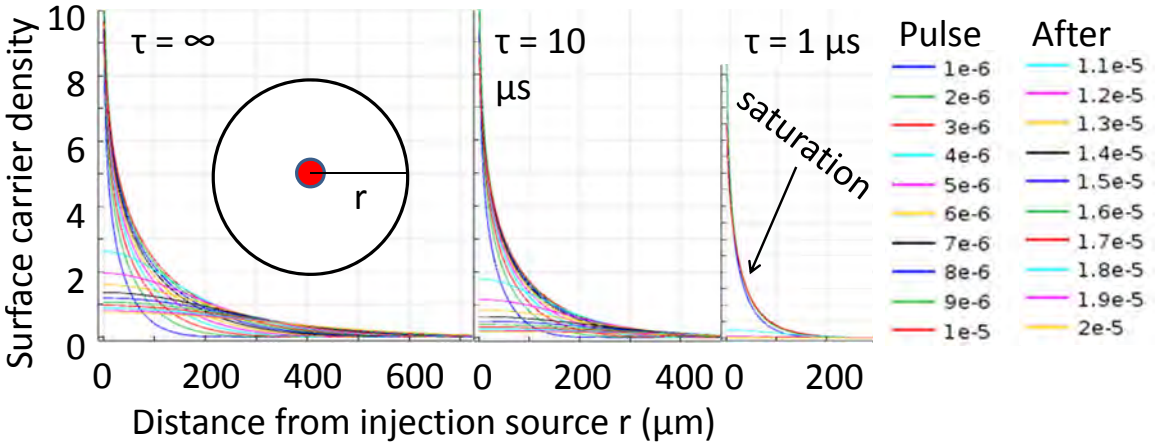


Figure 2.39: Simulated free carrier distribution at the surface over 20 μs for a pulsed injection

beyond the threshold for the SCR triggering. Provided that the value of the critical conductivity only depends on the free carrier density, the question then reduces to the analysis of the following problem: depending on the injection level, how much time is needed to reach a given concentration?

Simulations with COMSOL have been performed using a diffusion model where a linear term has been introduced to take the recombination into account, as in equation 2.4, where n is the electron density, $D = \mu k_B T/q = 36\ cm^2/s$ is the diffusion constant of the electron in silicon, τ is the recombination time, and G is a source of electron that models the injection at the n+ contact. The model is different as the model presented in part 2.2.3 because the time scale is much longer, and the process of carrier collection described in part 2.2.3 is in steady state. Here the diffusion term is taken into account, and the free-carriers that are probed are far deeper in the substrate or laterally further

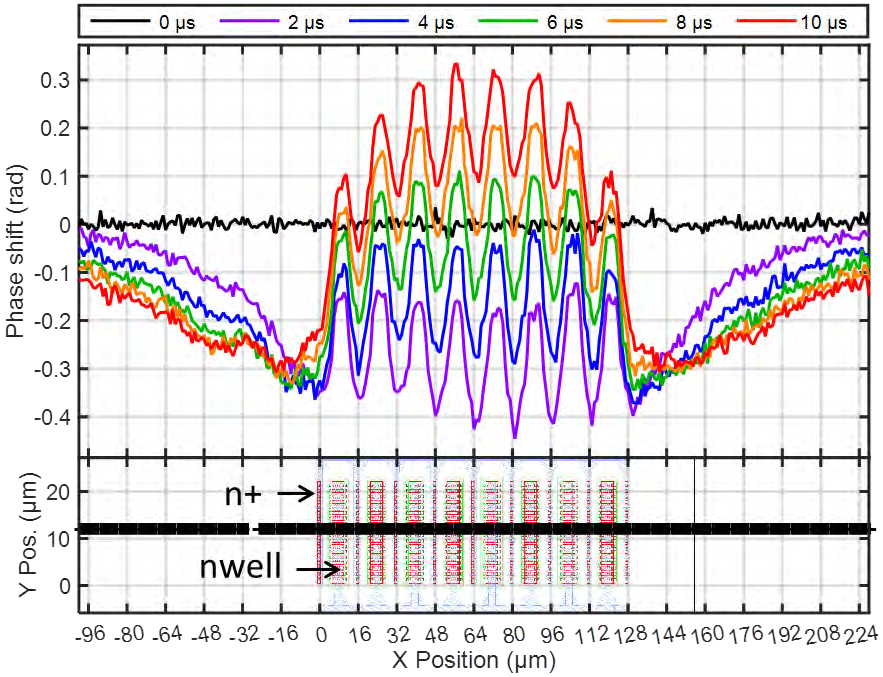


Figure 2.40: Measured TIM signal versus position for the ob-SCR for a 10 μs-long pulse in triggered mode, with three different values for the carrier lifetime

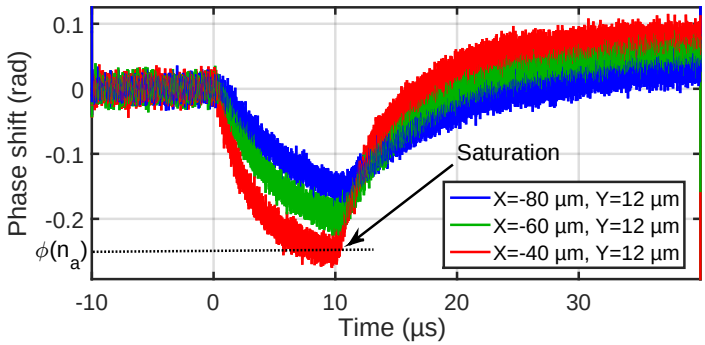


Figure 2.41: TIM phase shift waveforms of the ob-SCR under 10 μs-long pulse in triggered mode

from the device where they have time to diffuse, and thus the value that is measured for the carrier life-time is not related to the collection of the carriers by the collectors of the transistors, but rather to the spontaneous recombination of the free electrons in the p-sub. The results of the simulation are given in figure 2.39 as the carrier concentration distribution for several value of the carrier life time. It can be seen that the carrier life time sets the order of magnitude for the time to reach the steady state.

$$\frac{\mathrm{d}n}{\mathrm{d}t} = D\nabla^2 n - n/\tau + G \tag{2.4}$$

The solution to equation 2.4 is linear with the injection source (it can be rewritten

as $f(n) = G$, where f is a sum of linear operators), provided linear boundary conditions (here dn/dx=0 at all boundaries). In particular, for a step function at the n+ contact as the injection function, the equilibrium distribution will be proportional to the step amplitude G_0. For a given critical concentration that is needed for triggering, the concentration will take an arbitrarily long time as the step amplitude is reduced. If the injection source amplitude is reduced to the point where the equilibrium value is under the critical concentration the device will stay in breakdown, and never trigger. This explains qualitatively the large increase of the time-to-triggering as the voltage increases by small steps in figure 2.37a. Nevertheless, the dependence between injection (i.e current) and time-to-triggering is dependent on the value of the carrier lifetime, as the simulation show. For this model to be plausible the carrier lifetime should be at least in the μs range.

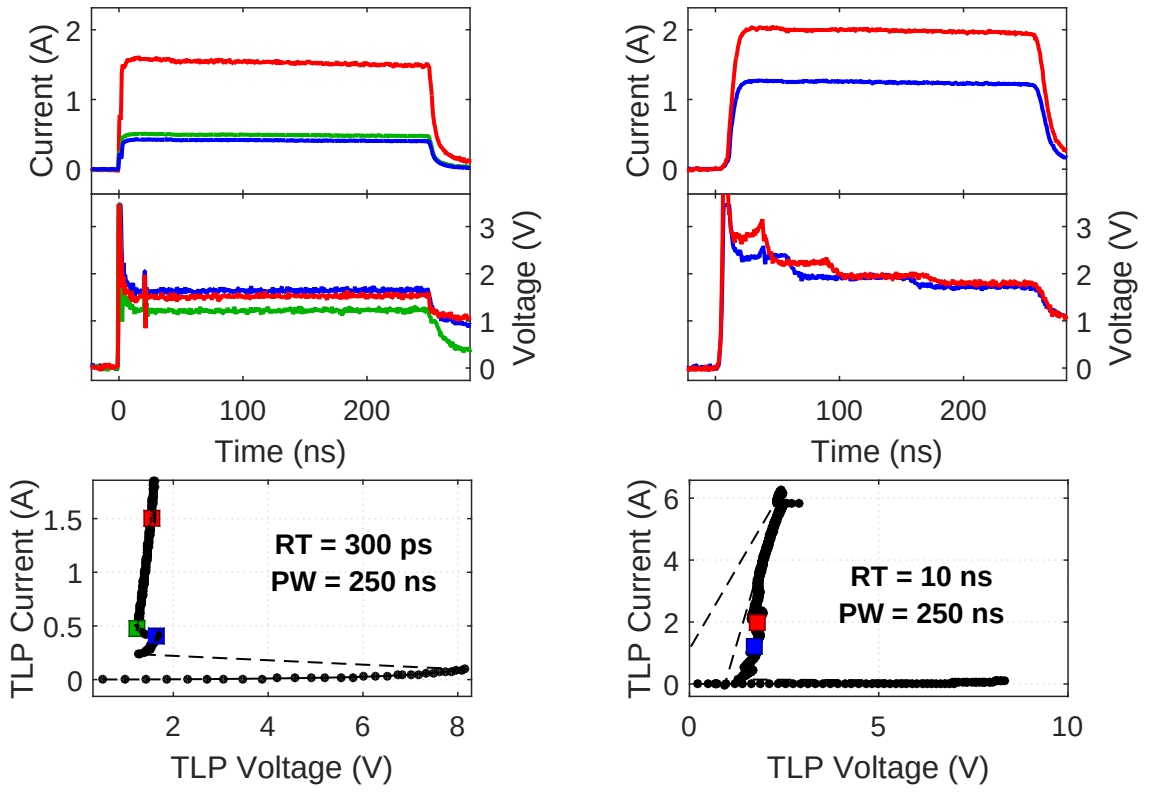
The carrier lifetime has been studied on the basis of TIM measurements using long pulse width up to 10 μs in triggered conditions using a Solid State Pulser. The result of the TIM experiment are shown in figure 2.40 for the phase shift distribution at different time instant, and figure 2.41 for waveforms at chosen positions. As it can be seen in figure 2.40, the signal in the active region of the SCR is a superposition of the negative free carrier signal and the positive heat signal. Therefore, the extraction has to be made far enough from the device in order not to have heat signal overlapped with the free carrier signal.Figure 2.41 shows that at 40 μm from the first finger, the TIM signal starts to saturate at the end of the pulse. This corresponds to a recombination lifetime in the range of the μs. The conductance modulation model for the time to triggering near the triggering voltage is therefore compatible with the extracted range for time the recombination lifetime.

2.2.5 Rise time effect and sequential finger triggering in SOI open base SCR

To see the rise time influence on the triggering behavior, TLP-IV measurements have been performed with RT=300 ps and RT=10 ns on a 16 finger ob-SCR on SOI. The TLP-IV of the SOI ob-SCR device is shown in figure 2.42a with chosen waveforms. The triggering voltage is roughly 8 V. At 400 mA we see another little snap-back that is marked with the blue cursor on the IV in figure 2.42a. The hypothesis that we make is that the part between the main snap-back and the little snap-back (200 mA to 400 mA) is a state of the device where only a certain number of fingers are triggered and the part of the IV above the additional little snap-back (more than 400 mA) corresponds to a state where all fingers are triggered. The partially triggered part of the IV has a differential resistance of roughly 1.2 Ω, whereas the the fully triggered part has a differential resistance of roughly 0.25 Ω, which makes a factor 5. This could mean that only 3 or 4 fingers are active in this state. Figure 2.42a shows that the voltage waveforms at all current levels are flat after 20 ns in the pulse, so the number of triggered fingers is determined at the initial

triggering event and not during the pulse. This is likely due to a du/dt triggering, or a voltage overshoot.

As seen figure 2.43, the TIM scan of the SOI ob-SCR device at 1.5 A for 300 ps rise time shows that after 1 ns all the fingers are already triggered. The signal is saturated in a time that is not resolvable by the TIM technique, i.e less than 3 ns. The device can therefore be considered fully triggered after less than 3 ns.



(a) RT=300 ps **(b)** RT=10 ns

Figure 2.42: TLP-IV of obSCR on SOI for different rise time values

The TLP measurement for 10 ns rise time gives voltage waveforms as in figure 2.44 on the right. These waveforms show several snap-backs during the pulse at times that depend on the current level. This makes the standard method of TLP-IV plotting, as described in part 1.4.1.2, inefficient, as a fixed averaging window will not always cover a meaningful part of the waveform.

To improve the visualization of the phenomenon, an algorithm was written in MATLAB to find the significant falling edges in all voltage waveforms by finding the local maxima of the cross-correlation of each waveform with a normalized falling edge pattern. From this information, it is possible to separate each waveform in flat parts, or plateaus, to each one of which a custom averaging windows is associated. For example in figure 2.44 on the right, one can see five averaging windows in color, that are bounded by 6 falling

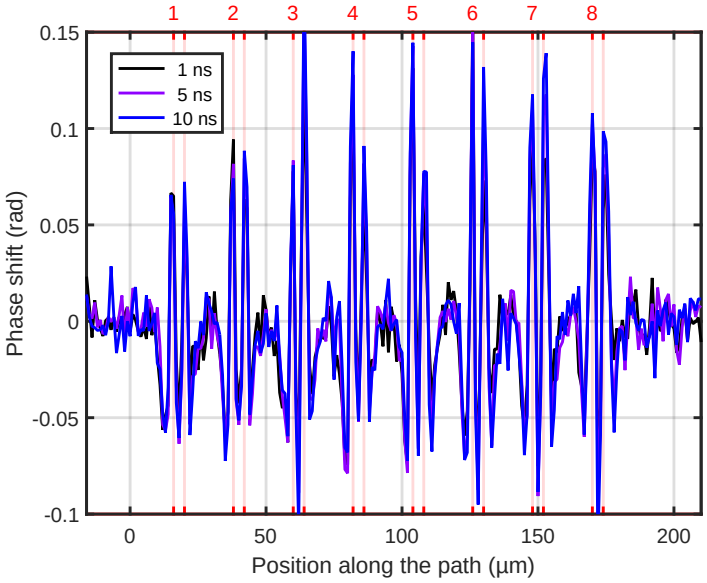


Figure 2.43: Phase shift in the ob-SCR device under 1.5 A, 300 ps rise time pulses

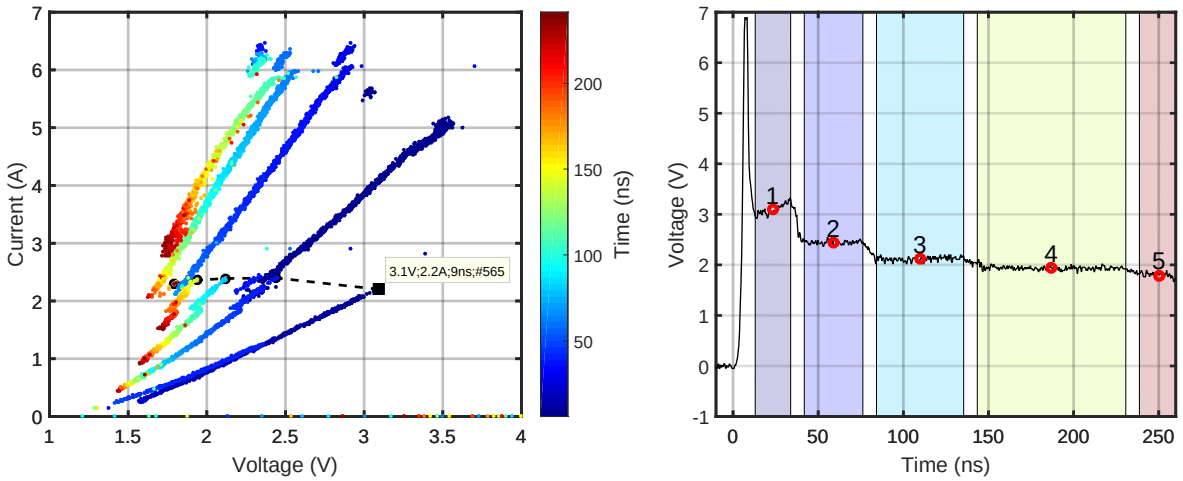


Figure 2.44: TLP-IV with adaptive average windows of the SOI ob-SCR device (left), with a mode 1 waveform (right). The TLP shows the sequence of plateaus in the waveform with a dashed line.

edges, including the initial voltage drop of the triggering event and the falling edge of the pulse itself. After analyzing all the pulses and creating a map of the falling edges and averaging windows, they are used to produce a TLP IV that maps all the flat states. The information of the preceding falling edge time is also displayed as a color code on the scatter plot. The result is shown in figure 2.44 on the left. In this IV plot, the dashed line represents the averaged values of the voltage waveform on the right in the different averaging windows against which is plotted the corresponding values for the current.

At first glance, this method generates points that can be grouped into lines that

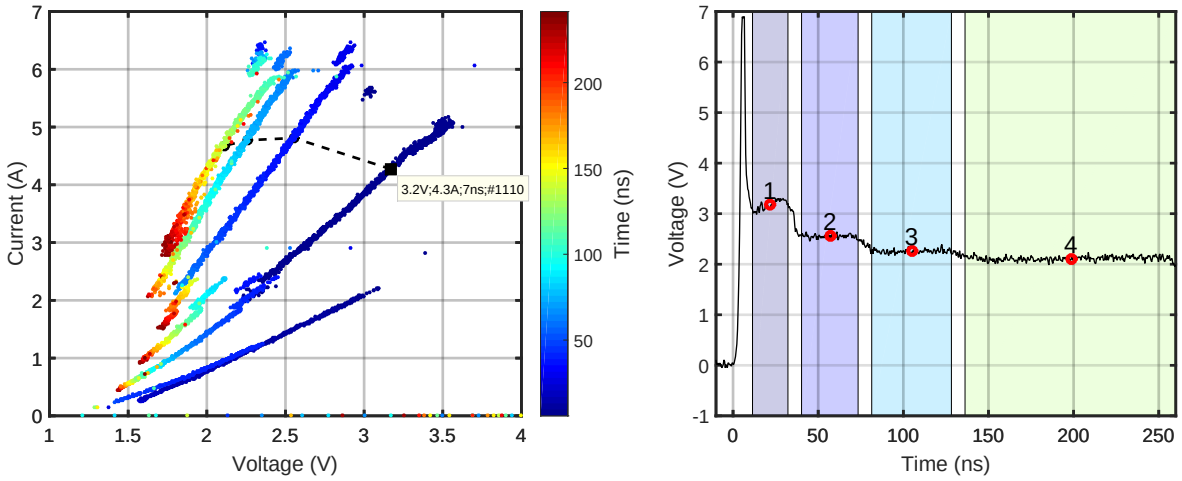


Figure 2.45: TLP-IV with adaptive average windows of the SOI ob-SCR device (left), with a mode 2 waveform (right). The TLP shows the sequence of plateaus in the waveform with a dashed line.

roughly converge into one point on the voltage axis at around 1.1 V. The IV plot can be separated in two parts, from each side of the $I = 2.2\ A$ line, where the lines underneath stop abruptly and other start. Each line can be interpreted as the IV of the device with a particular configuration of active fingers, that will be referred as "state" in the following. The lower resistance states are the ones with more active fingers. As it has been seen with the example in figure 2.44, as time goes on, states are likely to be switched for another state with more active fingers without going through the triggering voltage of 8 V. The duration of a state is a decreasing function of the current/voltage that flows in the device, as the colors indicate. The first state on the bottom right of the IV where the cursor is located on figure 2.44 cannot be reached for current higher than 2.2 A. We define mode 1 as the sequence of states that start with this state. The direct triggering of a lower resistance state could be explained by a multiple finger triggering by du/dt effect that would also explain the 300 ps rise time behavior of the device. A waveform at higher current of 4 A is shown in figure 2.45. The first state that is reached with current larger than 2.2 A is the state where the cursor is placed. Waveforms that start with this state define mode 2 and this state will be referred as the state 1 of mode 2, or M2S1. Figure 2.46 shows the adaptive averaging window-TLP IV of the device with indicated modes and states. This figure shows that mode 1 and 2 are not only different on the initial state that is reached, but also on the next states that follow. If one trusts the apparent alignment of the lines, one could say that the triggering sequence of mode 2 jumps over the odd steps of mode 1. Furthermore, it seems that the state M2S2 is the state where all fingers are triggered. This hypothesis is supported by the fact that its R_{ON} value is comparable to the value for 300 ps, where we know by TIM that the device is fully triggered.

A mechanism that would explain this behavior would be the sequential triggering of

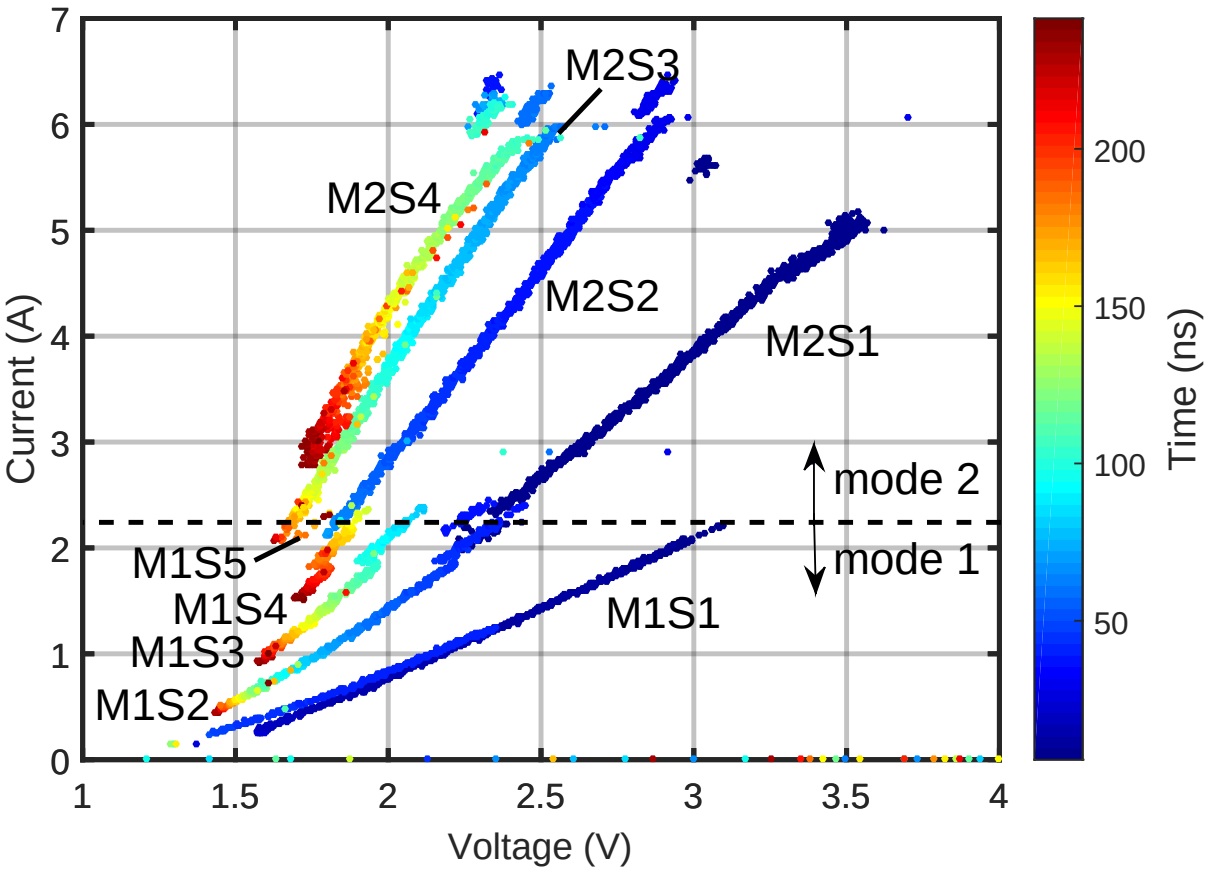


Figure 2.46: TLP-IV of the SOI ob-SCR device with adaptive averaging windows, modes and states are indicated

the fingers from neighbor to neighbor. A good candidate for the underlying phenomenon would be the injection of carriers to the reverse junction of the next finger through the nwell or the p-sub, depending on which one they share. It would explain that an increased current value decreases the time needed to propagate the triggering. When a larger number of triggered fingers, there is less current in each of them, and therefore less injection towards the non triggered neighbors. This results in a longer time for the following triggering event.

Considering that mode 2 has four states, it is possible that the device triggers from the pairs of fingers of both edges, and then propagate the on-state to the central pairs of fingers from both sides. Mode 1 would be the same but with only one pair of finger at the edge, propagating in only one direction.

However this analysis relies on how figure 2.46 looks to the eye. Table 2.3 shows the extracted on-resistance and V_{T1} of each state of both modes, i.e the fitting parameters for the equation $V = V_{T1} + R_{ON} \times I$. From these values, it looks like the ON-resistance of state M2S1 is closer to the one of the state M1S3 as to the one of state M1S2, although

the combination of R_{ON} and V_{T1} makes it seem like state M2S1 is in line with state M1S2 on the figure 2.46. The correspondence between the states of both modes to particular configurations of active fingers and between them have been investigated with TIM.

State	R_{ON} (Ω)	V_{T1} (V)
1	.76	1.40
2	.54	1.23
3	.43	1.16
4	.38	1.03

(a) Mode 1

State	R_{ON} (Ω)	V_{T1} (V)
1	.41	1.41
2	.28	1.20
3	.23	1.16
4	.21	1.11

(b) Mode 2

Table 2.3: R_{ON} and V_{T1} of the different states in the SOI ob-SCR device with $PW = 250\ ns$ and $RT = 10\ ns$

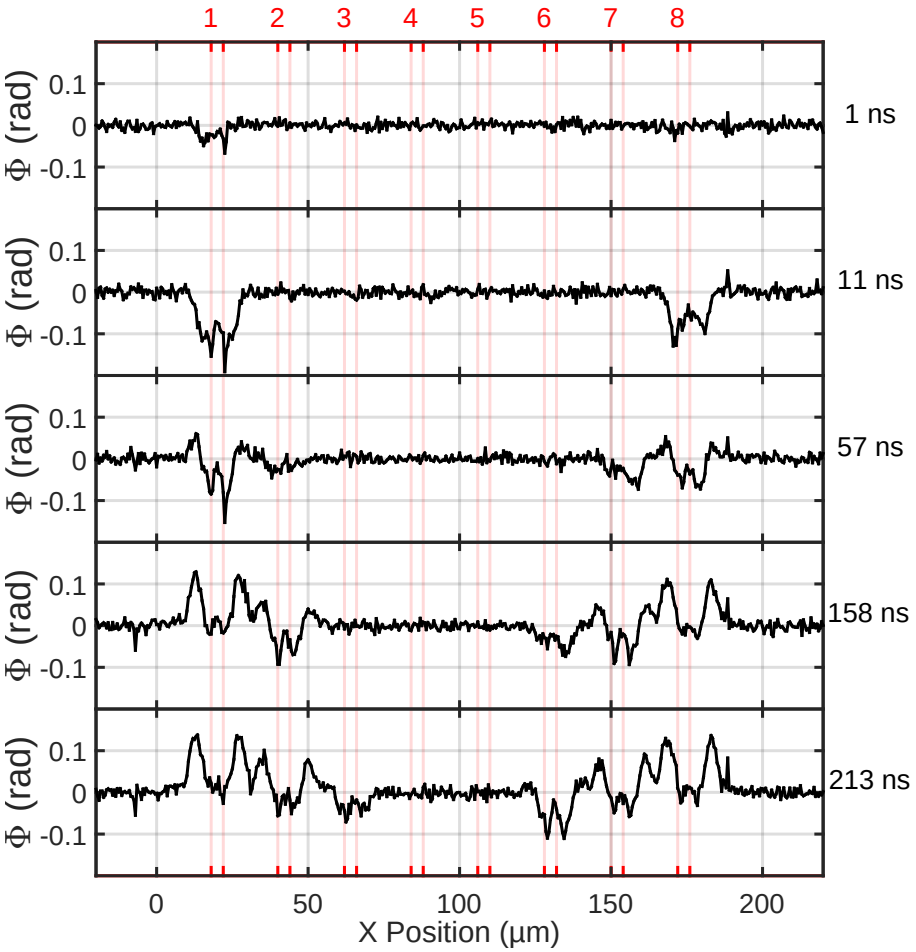


Figure 2.47: TIM of obSCR on SOI for different current value for RT=10 ns, I=2 A

To test the different hypotheses that have previously been formulated regarding the sequential finger triggering, a TIM scan was performed on the SOI-ob-SCR under 10 ns

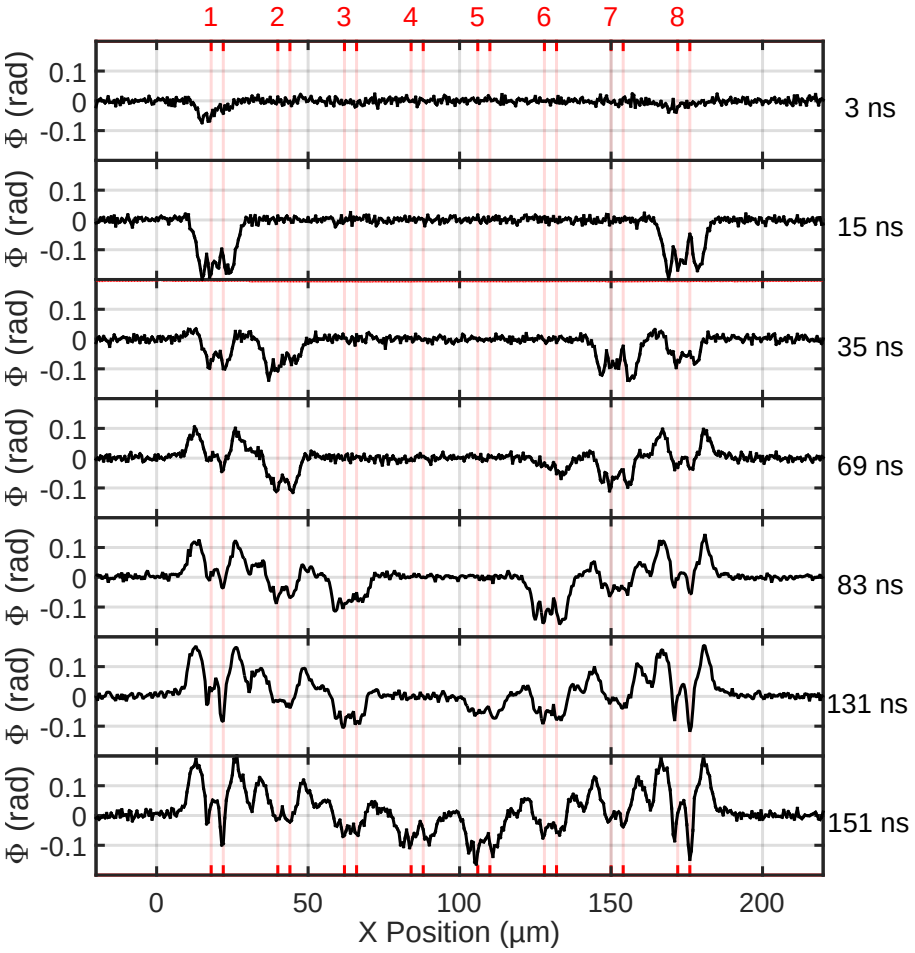
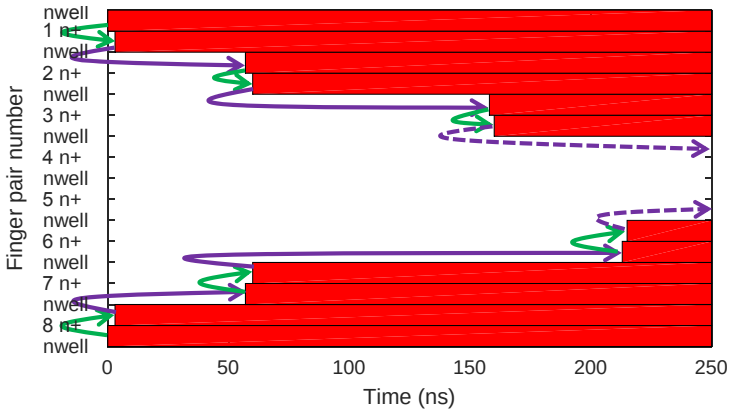


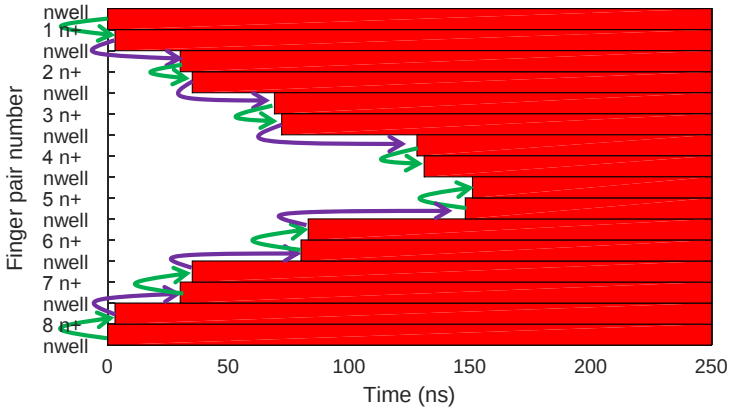
Figure 2.48: TIM of obSCR on SOI for different current value for RT=10 ns, I=4 A

rise time and 250 ns pulse width to see what fingers are active and when.

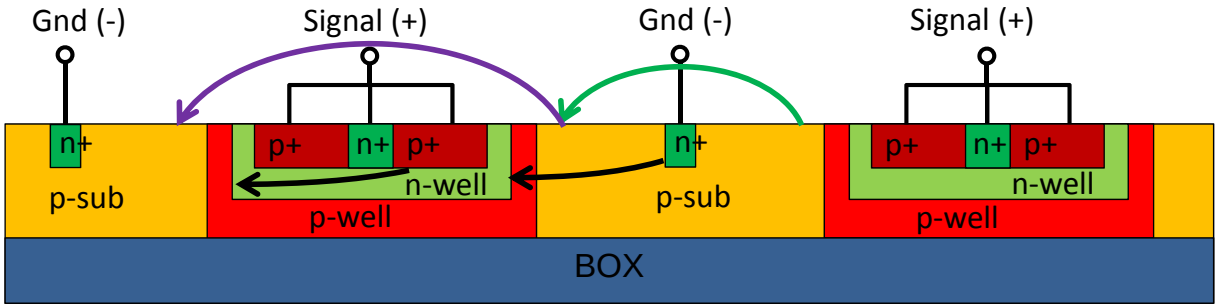
The result for the 2 A scan is shown in figure 2.47. The pair of fingers are numbered 1 to 8 on the top axis. The red lines correspond to the width of the gnd n+ implants that each pair of fingers shares. One can see that there is a sequential triggering, which propagates from finger to finger. The data show that the triggering of one finger results quickly in the triggering of the next finger when they share the n+ gnd contact, which are shown by the green arrows in figure 2.49a (this is why it has been chosen to pair these fingers to simplify the description). For example, it can be seen with the triggering of the 7th pair at t=57 ns that the first finger of the pair to trigger is the one closest to the 8th pair, which is quickly followed by the other finger of the pair with a delay of few nanoseconds. On the contrary, it seems that the propagation of the ON-state from one finger to the other when they share the p+ contact and the nwell is much longer, as the purple arrows in figure 2.49a show. This might be linked to a lower free carrier life time in the nwell as in the p-sub. However there is no visible signal associated to the carrier diffusion to support the hypothesis of the triggering by injection from finger to finger.



(a) 2A



(b) 4A



(c) Multifinger device cross section, with indicated transition types.

Figure 2.49: Schematics showing the finger activity versus time extracted for the TIM data shown in figures 2.47 and 2.48, green (resp. purple) arrows indicate sequential triggering of fingers sharing ground (resp. signal) contact.

The needed concentration might be below the sensitivity of the TIM setup.

There is a clear relation between the voltage drops and the finger activation monitored by TIM. At 2 A, the two first pairs of finger to trigger are the external pairs of fingers numbered 1 and 8, although the 8th pair seems slightly late. The resulting state could corresponds to state M1S1. After that, one can see the simultaneous triggering of the pairs 2 and 7 at t=57 ns, which corresponds to state M1S2. The triggering of the 6th

finger pair follows at t=158 ns which corresponds to the transition to state M1S3. This is the first time in the sequence that only one finger pair triggers. At t=213 ns the 3rd finger pair triggers, which corresponds to the transition to state M1S4. The dashed purple arrow in figure 2.49a indicated that the triggering of a new finger might happen, provided a longer pulse width.

The result for the 4 A scan is shown in figure 2.48. At 3 ns, the first fingers to trigger are the two pairs of fingers at the edge of the device. This should therefore correspond to state M2S1. At 35, 69, and 83 ns there are each time two additional pairs of triggered fingers, one at each side. The two last pairs of fingers to trigger are at 131 and 151 ns, respectively. The corresponding voltage falling edges are probably too close to each other, and not sharp enough to be separated by the falling edge detector. This means that the state M2S4 is in fact two states corresponding to 7 and 8 pairs of triggered fingers, respectively.

In both cases, each rise of the free carrier signal at a finger can be associated to a drop of the voltage, and the fingers trigger in order from the external to the internal. The TIM experiment therefore confirmed the mechanism of the sequential finger triggering. The question of the difference between mode 1 and 2 is still open, as there is no visible difference in the TIM signature. It could be that in the case of mode 1, the signal coming from pairs of fingers is not the sign of two fingers being actually triggered. In this case, mode 1 would be the mode where the sequential triggering operates on only one finger per pair, whereas mode 2 triggers two of them, at least for the two external finger pairs. Another hypothesis would be that due to the difference between the parasitics on the 2 point probe TIM setup and on the 4-point probe TLP probe station, the device triggers in another mode on the TIM setup. The DC leakage measurement during the TLP measurement might also influence the sequential triggering of the device. Indeed slight shift of about 500 mV has been observed in the triggering voltage after DC measurement. It is attributed to trapping at the passivation oxide interface due to hot carrier degradation. This effect might also be determinant on the order of the triggering sequence as in [61]. In this case, the sequence of stresses should be adjusted to match in both measurements, so that the same sequence be observed.

2.2.6 High current regime in open base SCR

The goal of this study was to locate the critical heat dissipation location at high current levels in order to assess the cause of the device destruction at I_{T2}. The current that was used for the stress of the devices is 6 A, as it is the maximum current that the TLP can provide with a 13dB attenuator on the output. The role of the attenuator is to attenuate the reflections of the pulse that can destroy the device when they come back with a negative amplitude after reflecting on the end of the transmission line inside the pulser. Indeed, these test structures do not have diodes in parallel to protect them like the SCRs

that have been studied for the ON-state spreading, and some of them have been destroyed during preliminary measurements at high current.

2.2.6.1 High current regime in bulk open base SCR

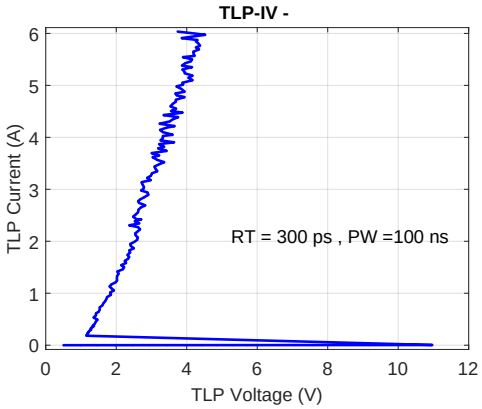


Figure 2.50: 2-point-probe TLP-IV up to 6 A

The device that was chosen to characterize the ob-SCR bulk technology at high current is a 8 finger device, where each finger is 25 μm-wide. The configuration of the contacts is $G|S|G|S|G|S|G|S|G$, where S and G are signal (anode) and gnd (cathode) contacts. Figure 2.27a gives a schematic view of one finger of this device. Figure 2.50 gives the TLPIV of the device measured in 2-point-probe configuration on the TIM setup for 100 ns pulse width and 300 ps rise time.

The scan path that was analyzed is a three line scan along the length of all eight fingers that is shown in figure 2.51. Typical waveforms can be seen in figure 2.52.

As it can be seen in figure 2.51 and 2.52, this scan features positive and negative phase shift values at various time instants and positions. This means that the effects of the free-carrier signal and the thermal signal are both significant at this current level. To distinguish the free carrier and thermal signals, it is useful to perform simulations to see what the effect of each one of them is.

Using COMSOL, 2D simulation of the phase shift has been made by simulating independently the heat diffusion in the structure, and the free carrier diffusion with a fixed free carrier life time constant of 20 ns that emulates the carrier collection. Figure 2.53 shows the result of such a simulation. The source of both heat and free carrier has been placed at the n+ contact to match the main peaks of the phase shift in figure 2.51 and are marked with a red area on the figure. The phase shift corresponding to the simulated heat (resp. free carrier) is shown in figure 2.53a (resp. figure 2.53b). The sum of these two phase shift components fit the experimental main feature during the pulse.

One can see that at t=200 ns, the phase shift peaks still have a fair contrast against the background of diffused heat in the device, with a contrast $(max - min)/min$ of roughly

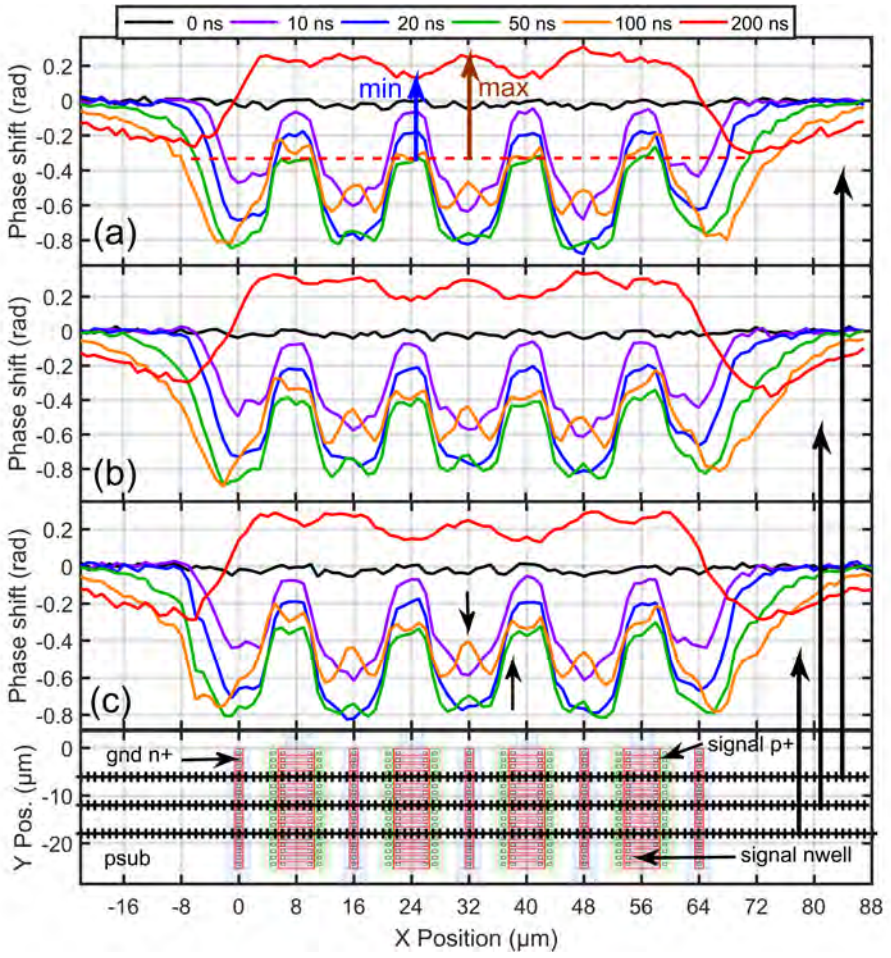


Figure 2.51: Phase shift versus position at chosen time instants for all three scan lines (TIM scan on bulk ob-SCR device, $I = 6A$)

1/3.

The simulated free carrier distribution at 200 ns is negligible, and leads to no phase shift. This is not what the experiment shows, for example in the diffusion tails outside of the device (see at X= -16 μm in figure 2.51). This is probably due to the simplified model of the simulation that keeps collecting the carriers even when the pulse is over, which is not realistic. The model would need to be adapted to change the recombination constant in function of the triggering state of the device, to take into account that the collection of carriers decreases as the device returns to the off-state. Alternatively, some negative carrier source should be introduced with a delay. However, this situation is hard to describe in both terms, as the collection allows the device to stay in a state that can be considered ON even with a current level below I_H, which allows it not to switch back to breakdown mode. To simplify the study, the assumption that is made is that the diffusion of the free carriers makes a quasi flat distribution at t=200 ns, shown as a red dashed line at -0.35 rad in figure 2.51.

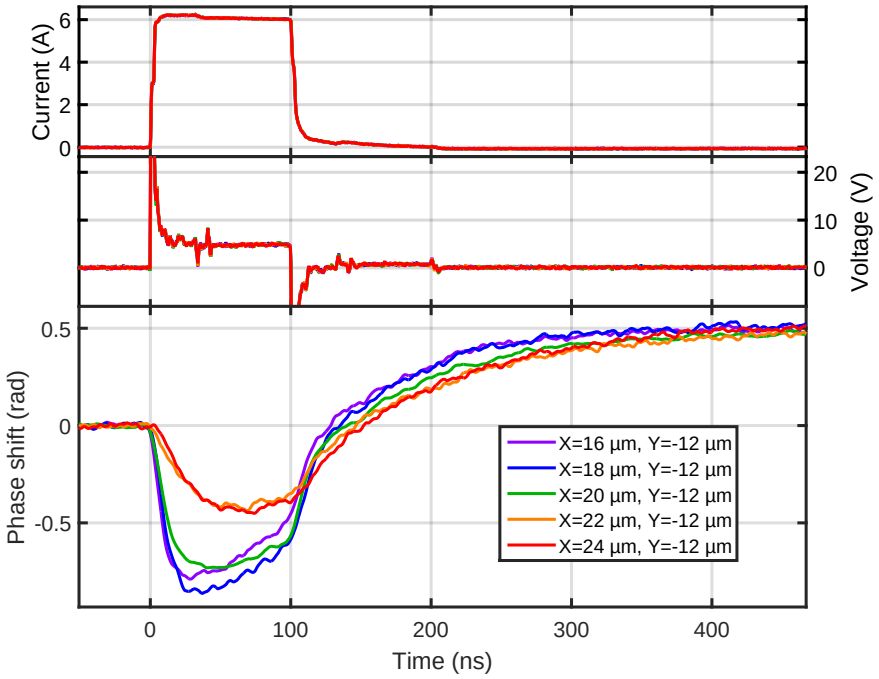


Figure 2.52: Voltage, current and phase shift waveforms at chosen positions (TIM scan on ob-SCR device, $I = 6A$).

Taking this value as baseline for the heat signal, the contrast of the peaks is much weaker ($(max - min)/min = 0.15$ for the central finger) than the simulated values (0.33), where max and min values are indicated in figure 2.51a for the experiment and figure 2.53a for the simulation. This means that the actual heat source are more spread than in the simulation, covering the whole p-sub region until the p+ contact. This locates the power dissipation along the current path in the device from the p+ contact to the n+ contact.

Now let us look at intermediate time instants to be more precise. At 50 ns, both in the simulation and the experimental data, one can see that there is a positive peak appearing inside the negative peak at the gnd n+ location (arrow at X=32 μm in figure 2.51c). This can be expected, as the heat diffusivity is lower than the free-carrier diffusivity, therefore creating sharper peaks, but it shows that the n+ pad itself exhibits a large power dissipation. Other positive peaks can be found at the p+ pad, as marked by the arrow at X=37 μm in figure 2.51c. However, the corresponding power, which can be seen from the area inside these peaks, is not enough to match the heat signal that is seen at 200 ns. It is therefore likely that most of the heat is dissipated homogeneously along the length of the finger, with a slight concentration at the n+ gnd and p+ signal pads.

The analysis therefore shows that the highest temperature at high current is reached at the gnd n+ pad. This might be caused by the single row of contacts here, as opposed to the double row at the signal side. This could be helped by separating the n+ pads of two adjacent fingers in the same way as the signal pads, which seem to have less power dissipation. However, as it has been seen in part 2.2.5, the sequential finger triggering

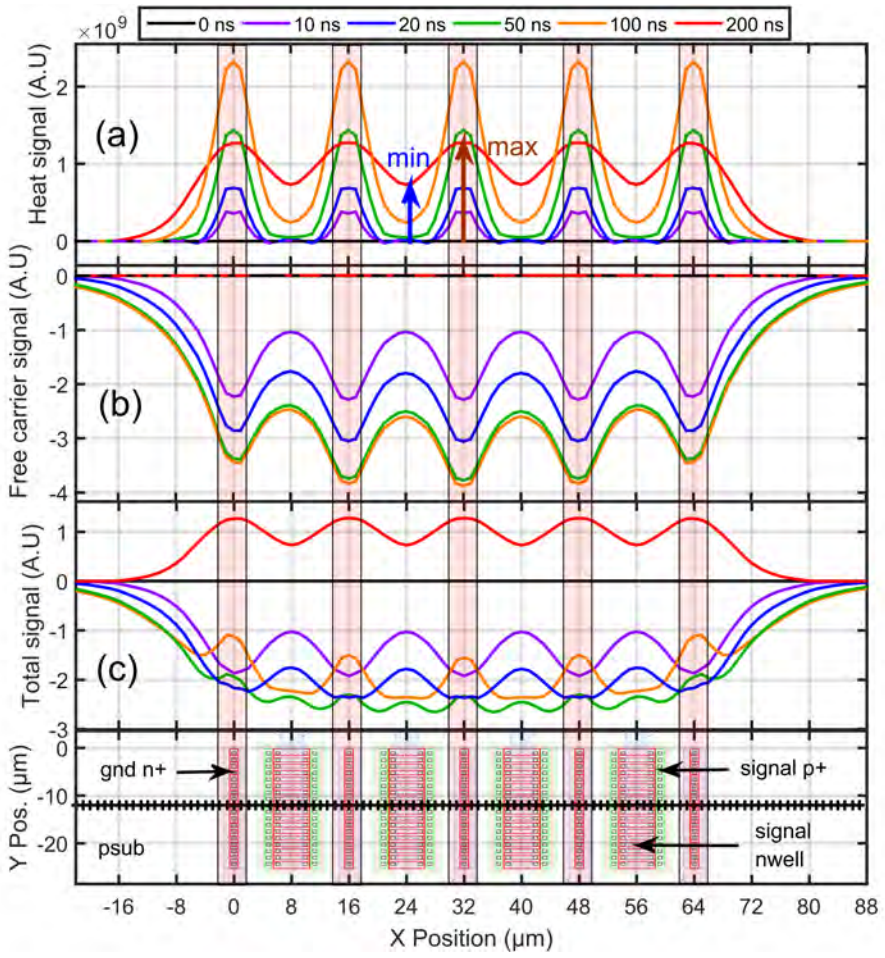


Figure 2.53: Simulated phase shift versus position at chosen time instants. Injection and heat sources are marked by the red areas.

might be affected by such modifications.

2.2.6.2 High current regime in SOI open base SCR

The device that was chosen to characterize this ob-SCR SOI technology at high current is a 8 finger device, where each finger is 25 μm-wide. The configuration of the contacts is $S|G|S|G|S|G|S|G|S$, where S and G are signal (anode) and gnd (cathode) contacts. Figure 2.27b gives a schematic view of one finger of this device. Figure 2.54 gives the TLP-IV of the device measured in 2-point-probe configuration on the TIM setup.

Figure 2.57a shows that the amplitude of the signal in these SOI devices changes during and after the pulse, unlike in the bulk devices. This is an indication that multiple reflections take place at the buried oxide/semiconductor and passivation layer/semiconductor interfaces. The consequence of this phenomenon is a nonlinear phase distortion that makes the thermal energy/free carrier evaluation from the phase shift complicated [62], although the change of the amplitude contains valuable information. The problem is that

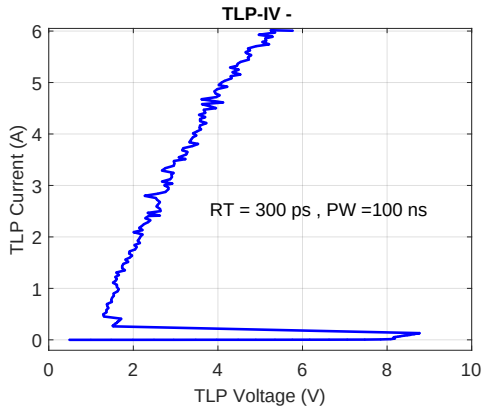


Figure 2.54: 2-point-probe TLP-IV up to 6 A

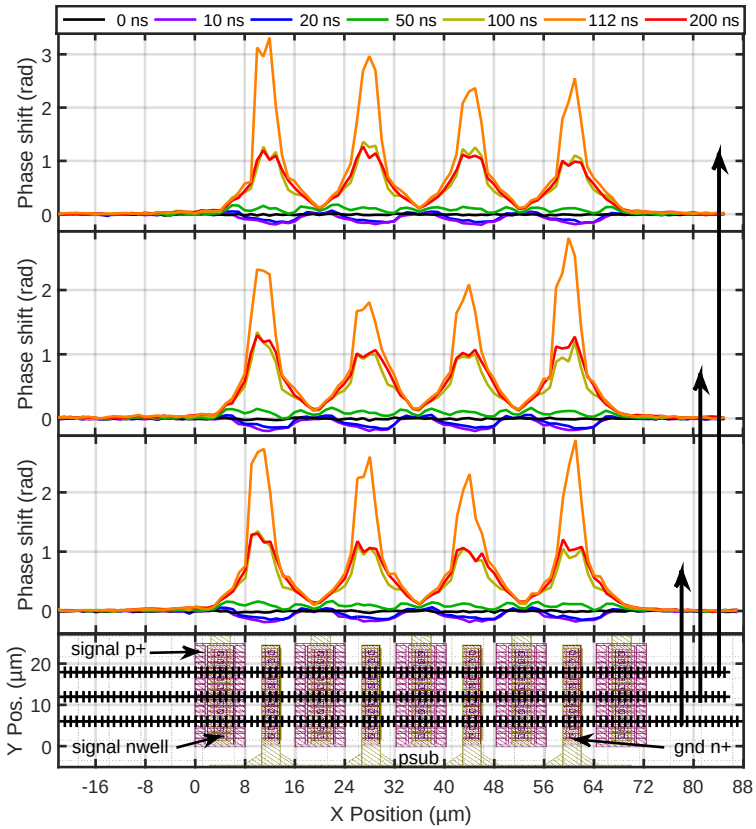


Figure 2.55: Phase shift versus position at chosen time instants (TIM scan on SOI ob-SCR device, $I = 6A$)

depending on the exact thicknesses and optical parameters of the layers, the measured phase shift gain $\mathrm{d}\phi/\mathrm{d}n$ can take a wide range of positive, but also negative values. In the case of a bulk device, the gain can only be positive and roughly independent of the distribution of the refractive index change along the beam path. Due to this variable gain, one could misinterpret thermal and free carrier signals. If the thicknesses of buried oxide, active Si layer and passivation layers are known with high accuracy (much smaller

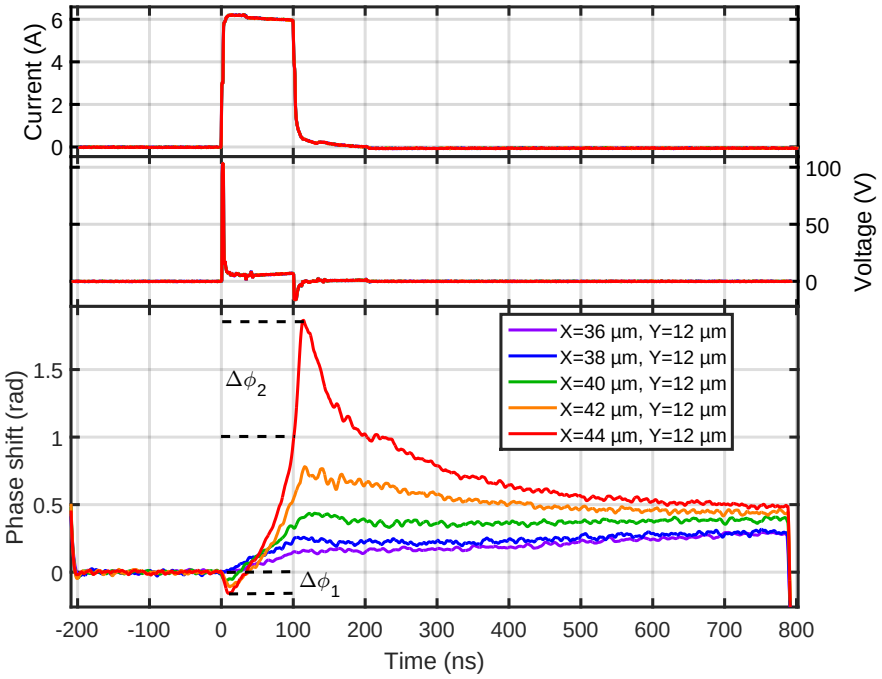
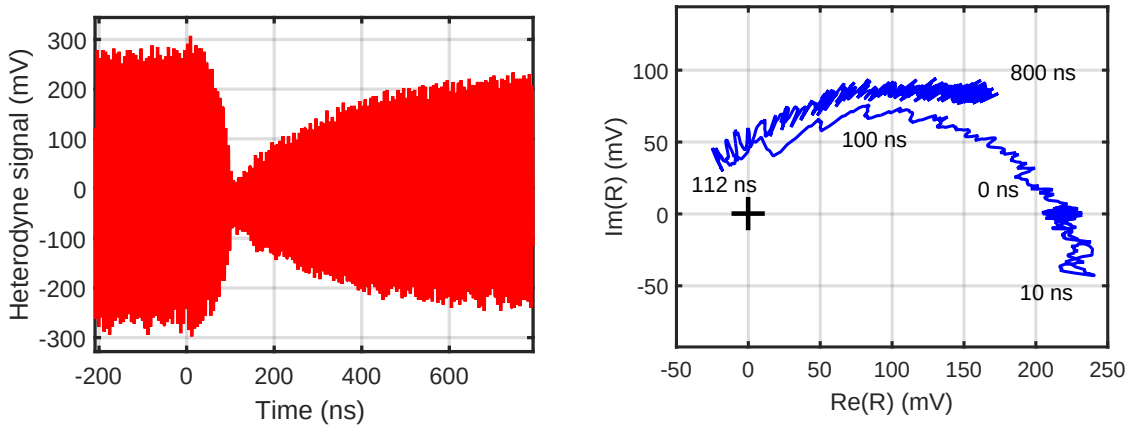


Figure 2.56: Voltage, current and phase shift waveforms at chosen positions (TIM scan on SOI ob-SCR device, $I = 6A$)

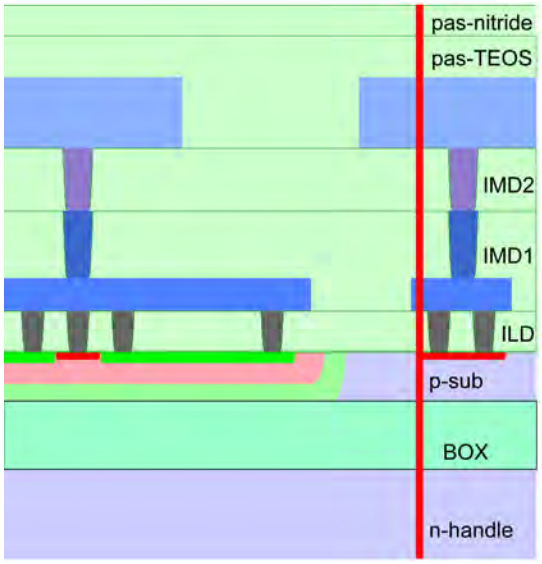


(a) Heterodyne signal.

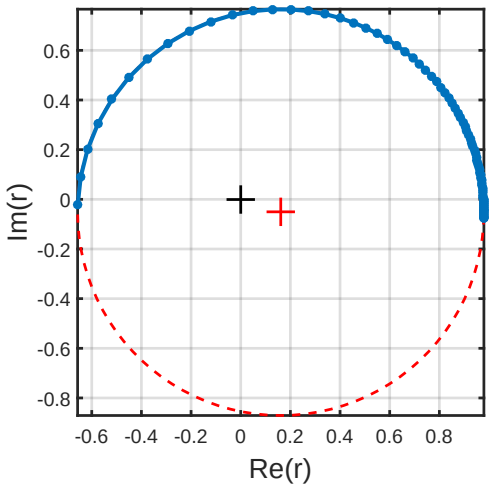
(b) Complex reflectivity.

Figure 2.57: Example of signal distortion at position X = 44 μm, Y = 12 μm (TIM scan on SOI ob-SCR, I=6 A).

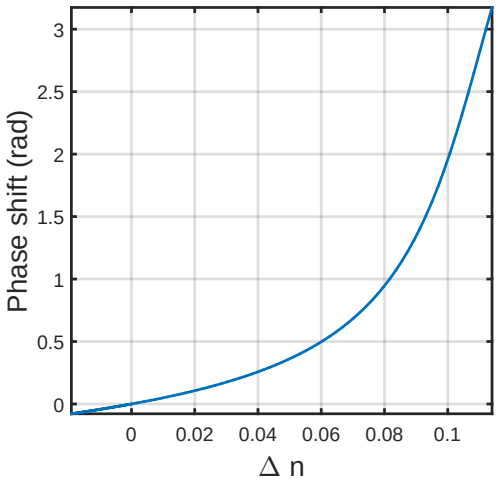
than $\lambda/(2n)$, where λ is the laser wavelength in vacuum and n is the refractive index of the layer), as well as the value of refractive index of the passivation layer and the BOX, then using optical simulation it would be possible to extract the variation of index of refraction from the phase data, and then extract the heat energy and the free carrier concentration from this variation as in the simple reflection case, as in the bulk case in part 2.2.6.1. As the thicknesses of SOI layers have some tolerance, a FIB cut over the



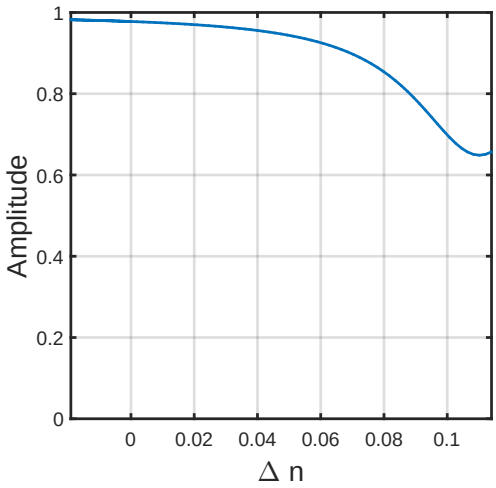
(a) Cross section schematics with optical path for the simulation indicated in red.



(b) Complex reflectivity.



(c) Phase shift.



(d) Amplitude.

Figure 2.58: Simulated optical response versus refractive index change of the active layer p-sub

particular investigated device after its TIM analysis is needed to get the highest accuracy.

To explain what is seen in this scan, optical simulations of the device under study was performed using a optical transfer matrix approach, within $\lambda/(2n)$ thickness tolerances and literature values of 1.447 for the refractive index value of SiO_2 [63] and 1.97 for SiN [64]. The results are presented in figure 2.58. The optical stack that was simulated is indicated in red in the cross section schematics (figure 2.58a) provided by the device designers. The contours of the complex reflectivity form a circle in the complex plane. The result is similar but not identical to the experimental data in terms of complex reflectivity (figure 2.58b to be compared with figure 2.57b), as the circle center is shifted in the same

direction. This translation changes the amplitude of the signal if the p-sub refractive index is modified due to free carriers or thermal effects (figure 2.58d). More importantly, the phase shift gain $\mathrm{d}\phi/\mathrm{d}n$ is positive and increases with the index of refraction, as shown in figure 2.58c where the slope of the phase shift response increases with the value of n. Consequently, the phase shift signal will be more sensitive to the change of refractive index if the p-sub refractive index is already high, as in the case of high temperature.

In figure 2.56, the negative signal at the positions around the n+ gnd (X=12 μm) at the beginning of the pulse corresponds to the injection of free carriers, which seems to saturate after 10-15 ns, due to the mechanism of carrier collection described in part 2.2.3. Due to the low thickness of the p-sub (SOI), there is no effect of the diffusion like in the bulk devices, where the carriers can diffuse deep in the substrate. After the end of the pulse, an increase of phase shift is observed, which also takes 10-15 ns and corresponds to the recombination of the carriers. Thanks to the simulation results, the difference between the phase shift increase due to the recollection after the end of the pulse $\delta\Phi_2$ and the initial decrease $\delta\Phi_1$ can be attributed to the gain $\mathrm{d}\phi/\mathrm{d}n$ difference due to different optical working points. The change in refractive index, and therefore in carrier density is the same in absolute value.

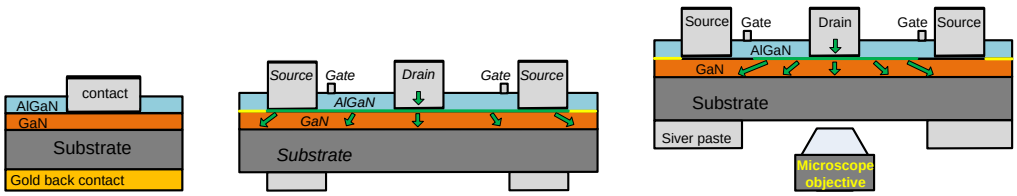
As the carriers are fast collected or recombined after the end of the pulse, whereas the heat is blocked in the silicon by the buried oxide, the phase shift at 200 ns is representative of the heat distribution in the device. However, the peaks in figure 2.55 are sharper than the temperature peak that causes them, due to the distortion caused by the multiple reflections effect. The device is still particularly hot at the gnd n+ pad which could be the cause of the damage at $\mathrm{I_{T2}}$. Again, separating the n+ pads from neighboring fingers could be tried to improve the thermal behavior of the SCR.

Chapter 3

Gallium nitride HEMTs

3.1 Study of the vertical breakdown

3.1.1 Devices under study



(a) Structure **(b)** Normally ON (A) **(c)** Normally OFF (B)

Figure 3.1: Schematics of circular test structure dedicated to vertical breakdown measurements (a), and normally-on (b) and normally-off (c) HEMTs (2DEG is indicated by green, arrows show the current flow from the drain to the substrate).[65]

Table 3.1 and figure 3.1 present the devices that were investigated in this study. There are four different structures, each having HEMTs and ohmic contacts. Device A is a HEMT featuring a negative threshold voltage of $V_{th} \approx -2.5\ V$ (i.e normally ON). It has a Schottky-gate (Ir/Ti/Au) with a 25-nm-thick $Al_{0.25}Ga_{0.75}N$ barrier, and a 2-μm-thick $Al_{0.8}Ga_{0.92}N$ buffer that is grown on a conductive Si substrate. The circular ohmic contacts on the same dice are done with Ti/Al/Ni/Au/Ti/Pt. Their area is 13105 μm^2. Device B has a threshold voltage $V_{th} \approx 0.5\ V$ ($I_{dmax} = 0.35\ A/mm$). It features a p-GaN gate on a 14-nm-thick $Al_{0.23}Ga_{0.77}N$ barrier. The GaN buffer is $\approx$ 3.1-μm-thick, and grown on a conductive n-type Silicon Carbide substrate [66]. The Ohmic contacts of the structure B are Ti/Al/Mo/Au. The area of the circular ohmic contact is 69746 μm^2 (i.e the diameter is 300 μm) Devices C and D are ohmic contact with a 13-nm-thick $Al_{0.23}Ga_{0.77}N$ barrier. Additionally, device C features a 3-nm-thick GaN cap layer. Both C and D have several available dimensions for these contacts: 4778 μm^2 ($\Phi = 80\ \mu m$),

Device	A		B		C		D	
Description								
Back contact	Pt/Au							
Substrate	n-Si		n-SiC					
Buffer	2 μm $Al_{0.08}Ga_{0.92}N$		3.1 μm GaN					
Barrier 25% Al	25 nm 25%		14 nm 23%		13 nm 23%		13 nm 23%	
GaN cap	-		-		3 nm		-	
Ω Contact	Ti/Al/Ni/Au/Ti/Pt		Ti/Al/Mo/Au					
Large structures contact area	13105 μm^2		69746 μm^2		4778 μm^2 17203 μm^2 69746 μm^2			
V_{TH}	-2.5 V		0.5 V		-		-	
Normal operation	ON		OFF					
Results								
Drain bias	-	+	-	+	-	+	-	+
V_{BD} stat. distr. - large structures	Normal		Weibull (or more complex)					
no. of modes	1	1	1	2	3	3	3	2
Failure signatures on small HEMTs	Channel area	Drain + contact pad	-	Drain + contact pad	-	-	-	-

Table 3.1: Summary table of the studied devices and the main results.[65]

17203 μm^2 ($\Phi = 150\ \mu m$), and 69746 μm^2 ($\Phi = 300\ \mu m$). All devices have Pt/Au back contact.

3.1.2 Statistical IV analysis

The results presented in this section were published in [65] and presented in [67].

The vertical leakage and vertical breakdown is first analyzed by the measurement of voltage-controlled DC-IV characteristics on few dozens of identical ohmic test structures for each technology. The measurement was performed in Berlin by our partners in FBH. The V_{BD} is defined as the voltage corresponding to a leakage current of 0.1 mA. For every structure of a fixed dimension on a wafer, the V_{BD} values are extracted and the empirical cumulative distribution function of these values is computed. The Cumulative Density Function (CDF) associates to any given voltage U the ratio of devices that have their

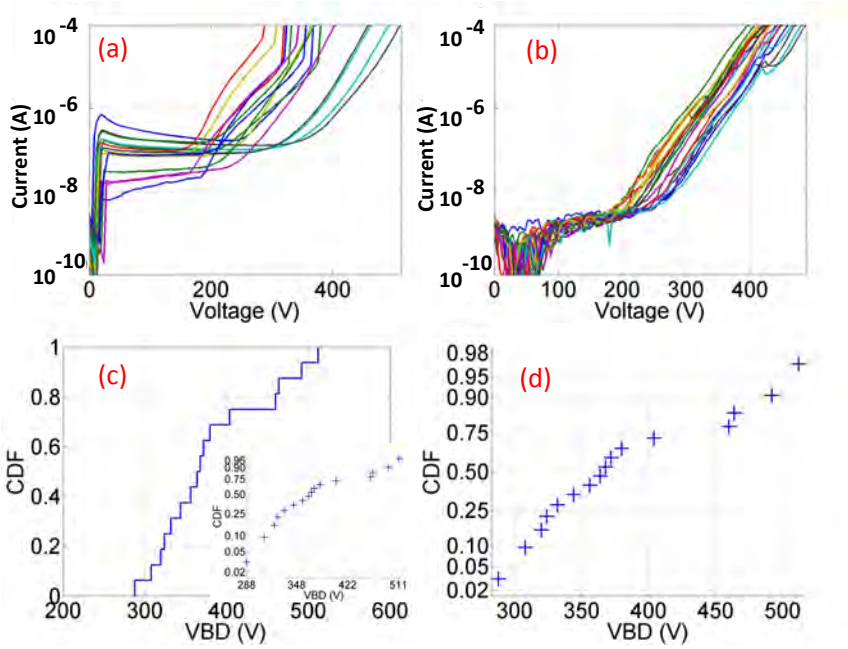


Figure 3.2: IV curves recorded under voltage-controlled mode for negative (a) and positive bias (b) on the top contact for device A. CDF of V_{BD} values for negative bias in linear scale (c) and in normal coordinates (d).[65]

previously defined breakdown voltage below U, or equivalently a leakage current superior to 0.1 mA at this voltage U.

Figure 3.2a-b, 3.3a and 3.5a-b show the DC-IV curves of the devices for negative and positive bias at the top contact. Most of the devices feature a low leakage up to few hundred volts, and an exponential or over-exponential dependence at high voltage.

The potential energy barrier at the 2DEG/GaN buffer interface and nucleation layer / substrate are the cause of the blocking behavior of the structure in negative and positive polarity, respectively. The leakage can be due to phenomenon involving traps in the bulk GaN. Hopping current, space charge limited current (injection from the contact, with V^2 dependence [68]), and Poole-Frenkel field-assisted conduction (electrons from traps are thermally excited to the conduction band, as the electric field lowers the barrier they have to overcome [69]) have been considered to explain the dependence of the vertical leakage current on the bias [30, 31].

In devices A and D (figures 3.2a-b and 3.4a-b) one can notice two main breakdown types. Some devices have their breakdown at high voltage with a small spreading of breakdown voltage values. The other type concerns devices that only feature similar low leakage current characteristics up to a random voltage value, beyond which the current rises abruptly. By analogy with the time dependent dielectric breakdown (TDDB) terminology [70], these two breakdown types will be called intrinsic for the high voltage ones and extrinsic for the type featuring random and premature vertical breakdown. It is to

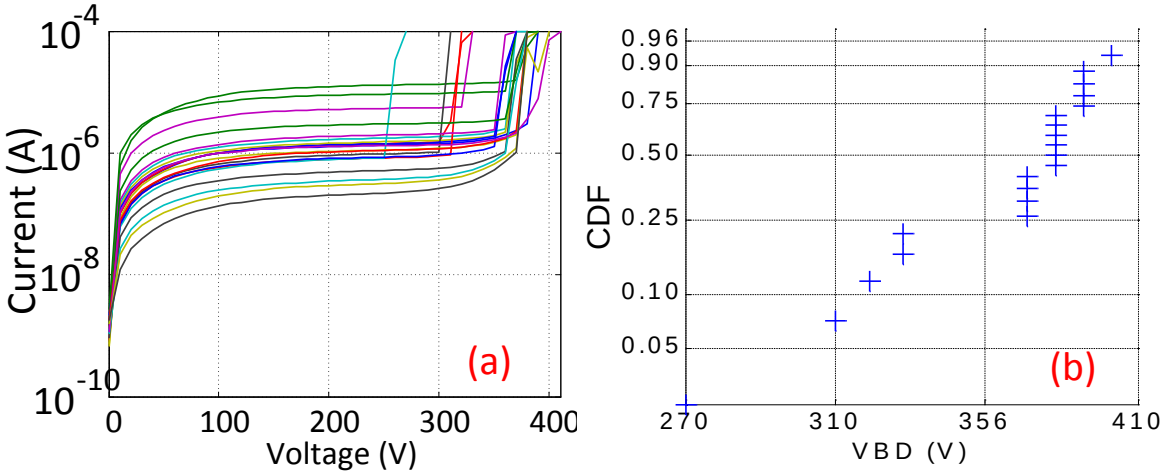


Figure 3.3: IVs (a) and CDF of V_{BD} values for positive bias in Weibull coordinates (b) in Dev. B.[65]

be noted that for device B in negative bias (figure 3.3a), the intrinsic breakdown mode is not easy to define as there is no large group of device that feature a high breakdown voltage. One can argue that all devices in B feature extrinsic breakdown mode.

In device C and D, it is possible to compare the V_{BD} statistical distributions of three size of devices on the same wafer. One remarks that the devices with larger area tend to have more early failures. This can be explained considering a quasi uniform random distribution in space of large extended defects that favor the conduction at high enough voltage, such as dislocations in the GaN buffer, or percolation path that are statistically unlikely enough to have a low density. The probability of having such a defect in the device is proportional to the area of the structure, resulting in a larger number of extrinsic breakdown mode for large area, similarly as in the time dependent dielectric breakdown of the gate oxide[70]. The intrinsic breakdown is likely due to smaller point defects that are much more common, so that their density is not dependent on the size of the contact.

Figure 3.2c shows the CDF of the vertical breakdown in device A for negative bias. The resulting curve can be divided in the intrinsic and extrinsic modes. From 300 to 400 V the CDF is increasing and slightly convex. From 450 to 550 V the five devices with intrinsic breakdown are found. The distribution of the V_{BD} were fitted to known distributions. Figure 3.2d shows the CDF in normal coordinates, i.e coordinates where normal distributions appear as straight lines. In the normal distribution plot, the points divide in two lines, one under 400 V and one above 450 V that correspond to the extrinsic and intrinsic modes, respectively. The inset of figure 3.2c shows the data in Weibull coordinates (where Weibull distribution form lines). One can see that this coordinates system does not allow to collapse the data on a line as well as for the normal coordinates, because the distribution is left skewed compared to a Weibull distribution (i.e too many low V_{BD} values).

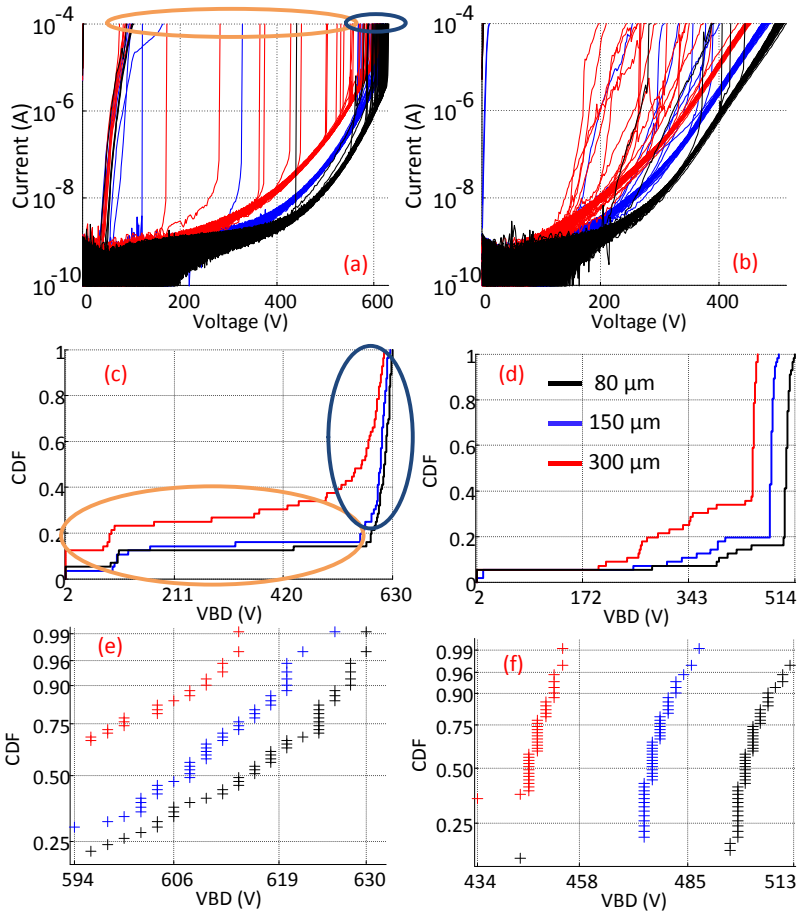


Figure 3.4: IV curves recorded under voltage-controlled mode for negative (a) and positive bias (b) on the top contact in Dev. D, for the three diameter values. CDF of V_{BD} values for negative (c) and positive (d) bias in linear scale and in Weibull coordinates (e and f). The data in the Weibull coordinates shows an area scaling coefficient [i.e. $ln(area2/area1)$, $area2 > area1$] in Weibull coordinates in the $0.6 - 1$ range instead of theoretical value of $ln(4) = 1.4$. The blue and orange ellipses indicate the intrinsic and extrinsic VB regions, respectively.[65]

For device B, on can see on figure 3.3d that the Weibull coordinates allow to gather all the data in one line, showing that the V_{BD} values are Weibull distributed. This single-moded distribution reflects that all devices display an extrinsic breakdown, as we remarked previously from the sudden increase of the leakage current for all devices.

Figure 3.5c shows that for negative voltage, device D features a number of early failures at 100 V that seem not to depend much on the area. This could be due to a particular region of the wafer that suffers from a high density of extended defects. Device C and D seem to present several modes that can individually be fitted to one distribution or the other with moderate success. Table 3.1 shows the number of modes and the closest distribution that was found.

The collapsing of the V_{BD} values on known distribution could be the sign that the

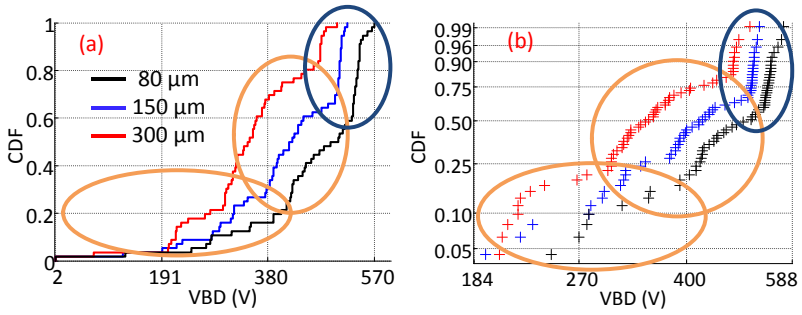


Figure 3.5: CDF of V_{BD} values for positive bias in linear scale (a) and in Weibull coordinates (b) in Dev. C, for the three diameter values. The blue and orange ellipses indicate the intrinsic and extrinsic VB regions, respectively.[65]

mechanism leading to these values are the same, but involving a different size of defects. The Weibull distribution has been used in TDDB for describing the distribution of time to breakdown. It emerges from the creation of percolation paths when the creation of defects is random in the dielectric [70, 71]. The activation of a possible percolation path that is already present depends on the voltage and on the distance between the traps. The information provided by the statistical distribution of the V_{BD} values is therefore linked to the statistical distribution of defects in the nucleation layer. Nevertheless, the effect of inhomogeneities in the wafer and other types of extended defects should be taken into account. This could only be possible by performing statistical analysis on a much larger sample set.

3.1.3 Time dependent vertical breakdown

The results presented in this section were published in [65] and presented in [67].

Time dependent measurements were performed on HEMTs in device B from drain to substrate. The gate and source of the device were left floating. The drain-to-substrate DC-IV of the HEMT device is shown on figure 3.6a. The two arrows at V=250 V and 500 V indicate the biasing points that were used for the time dependent measurements. By comparison to figure 3.3a, which represent the equivalent DC-IV for the vertical test structure, the HEMT device has a higher V_{BD}than any ,test structure, which shows that all measurements in the test structures displayed extrinsic breakdown, whereas the HEMT displays an intrinsic breakdown. This is likely due to the low size of the drain contact compared to the test structures contact.

Figure 3.6b shows the evolution of the leakage current with time for V=250 V and V=500 V. A schematic band diagram showing the conduction band is shown in inset. For both devices the current drops during the first hours, and then becomes noisy. For the device biased at 500 V the current starts to rise to a plateau. This evolution is very similar to what is observed for the degradation of AlGaN barriers in reverse bias stress

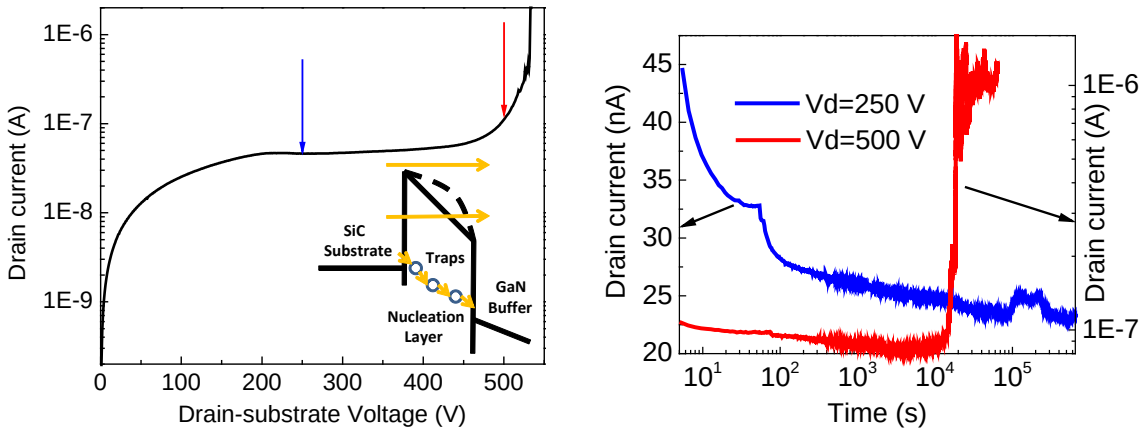


Figure 3.6: (a) Vertical IV of HEMTs under voltage-controlled mode. The arrow indicates the initial points of the TTB measurement. (b) Evolution of the vertical leakage current at 500 V. Inset: Band diagram for a positive drain-to-substrate bias, with negative charging of traps and creation of new defects, eventually leading to the creation of a percolation path.[65]

experiments [72–74]. The initial lowering of the current is due to the charging of the traps in the GaN buffer that enlarges the potential barrier. This is shown in the inset of figure 3.6a by the dashed line. After few minutes of stress, one can see that the current becomes noisy. This is associated to the creation of new traps [72, 73, 75], shown on the schematics as circles in the potential barrier. After 6 hours of random trap creation for the device under 500 V, a percolation path is formed and the leakage currents rise to 1 μA where it stabilizes. For the device under 250 V, no significant increase of the current was seen during the whole experiment (one week). That data gathered from time experiments on four samples seem to indicate that the rise of the current occurs in less than one day when the device is biased above 400 V which corresponds to the rise of the breakdown current (see figure 3.6a). Nevertheless more experiments are needed to take into account the initial randomness of the traps and defects to analyze the dependence between the voltage, the current and the time to breakdown.

3.1.4 Failure analysis using backside infrared microscopy

The results presented in this section were published in [65] and presented in [67].

The backside of dices of device A and B was polished with an angle so that some metal (and therefore an ohmic contact) was left in a corner of the dice. The dices were mounted on a PCB with a hole. To connect the backside, a silver paste was used to contact the remaining gold, and a wire was soldered. The dice of device A was placed on the probe station of the TIM setup for the drain to be contacted with probe needles whereas the drain of device B was wire-bonded to a track of the PCB, due to its small size.

It is worth noticing that device A is a normally ON device, so the 2 dimensional

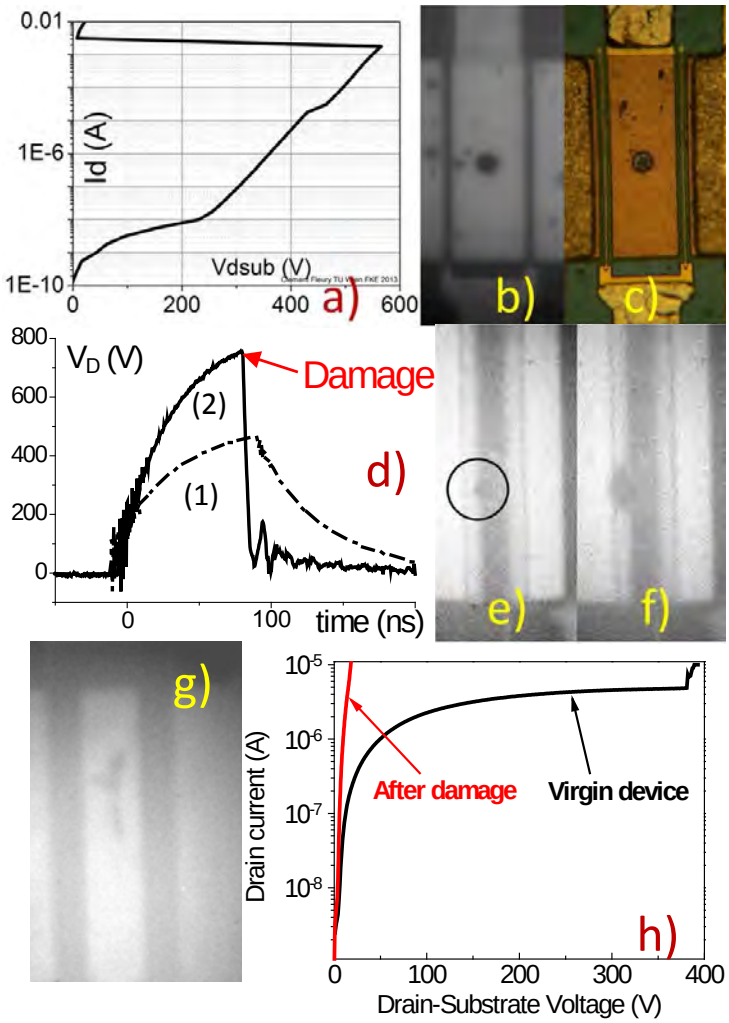


Figure 3.7: DC IV on silicon substrate (device A) in current-controlled mode (a) and resulting damage from bottom (b) and top (c). TLP voltage waveform for a non-destructive pulse (1) and during the destruction (2) of device B (SiC substrate) (d) and resulting damage from backside before (e) and after (f) additional DC stress.[65]

electron gas extends in the whole mesa (see Fig.3.1b, leading to a much wider area for the vertical conduction as device B where the gate limits the extent of the vertical conduction to the drain ohmic contact and the drain to gate area (see Fig.3.1c).

The original intent was to use EMMI under DC-IV (see part 1.4.2.3), but no light was detected until the damage of the device. The constant current DC-IV characteristics for device A are shown in figure 3.7a, where one can see the snap back at 2 mA that shows the creation of a leakage path. Even if the total current is relatively low, the current density in snap back can be large, as the device follows a negative differential resistance path, where the current tends to concentrate in filaments [55, 76]. In figure 3.7h, one can see from the post stress constant voltage DC-IV that the device is leaky.

The devices were imaged with standard visible light microscopy and backside infrared

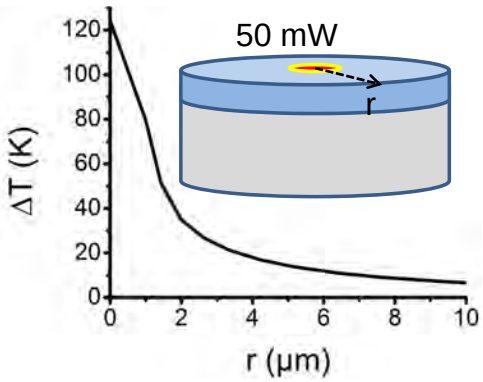


Figure 3.8: Simulated surface temperature distribution for a 50 mW input power at the surface of the GaN buffer.

microscopy (see section 1.4.2.2). Figure 3.7b and 3.7c that show the resulting damage on device A from the top and from the back, respectively. The position of the signature is located at the center of the drain. Figure 3.7g show the backside infrared picture of device B. In this case one can see that due to the discharge of the coax cables in the device, the current filament lasts long enough to extend the damage signature on the metalization, similarly as in [31].

To minimize the spreading of the signature, one can minimize the input energy by applying a short voltage pulse at the drain. For the pulsed stressing of device B, a transmission line pulser with 100 ns pulse width was used with a 5 kΩ load line (see section 1.4.1.2 and [77]). A voltage waveform is shown in dotted line in figure 3.7d, marked as (1). The long rise time and fall time of the pulse is due to the load line, the high impedance of the device and its parasitic capacitance. On the same figure, the pulse marked as (2) is the damaging pulse, with a maximum voltage of 750 V. One can see that the voltage suddenly drops, as the leakage path is created. This breakdown voltage is much higher than the intrinsic breakdown voltage of the device in DC, which could mean that the DC intrinsic breakdown is in fact the result of a time dependent breakdown that acts on a sub-milliseconds timescale (the minimum integration time of the SMU is 2 ms).

The device is then imaged with infrared microscopy, showed in figure 3.7e. The damage signature indicated with the circle is much smaller than the damage signatures obtained with DC-IV stress, as the input energy is smaller. To image this signature, backside infrared microscopy is necessary, as it is not visible from the top. Figure 3.7f shows that the damage signature can be enlarge by subsequent stress in DC.

The results have been extracted in HEMTs where the breakdown mode is intrinsic. It is not sure that these results extend to the cases where the breakdown is extrinsic, as in all the circular test structures of wafer B.

To evaluate the role of the self heating effect in the damaging, a thermal finite element modeling of the HEMT was performed using COMSOL in cylindrical coordinates. A cir-

cular heat source with no thickness and 1 μm radius was placed at the top of a 3 μm-thick GaN layer, under which was set a 600 μm-thick SiC substrate. The thermal parameters of GaN, SiC and the thermal boundary resistance of $4 \times 10^{-8} m^2 K/W$ are taken from [78]. Figure 3.8 shows the surface temperature distribution for an input power of 50mW (i.e. 0.1 mA x 500 V). In particular, the computed temperature rise at the center of the source is 130 $^\circ C$. Such a temperature could accelerate the vertical breakdown process in DC. For better temperature estimation the vertical extent of the heat dissipation needs to be known with better accuracy. The horizontal extent can be studied by looking at low energy damage signatures.

3.2 Degradation of GaN HEMTs in high temperature conditions

The results presented in this section were published in [79] and presented in [80].

3.2.1 Devices under study

The devices under study were p-GaN gate HEMTs with 2×125 μm gate width and 6 μm gate-to-drain distance fabricated on the heterostructures descibed in table 3.2. Three of the four heterostructures are grown on a SiC substrate and the fourth is grown on silicon. Several strategies for avoiding the punch-through breakdown is the GaN buffer are tested, such as the carbon, or iron dopping [81] and a back barrier using a double heterostructure [82]. The device technology is similar to [83]. To enable vertical measurements, the dices had a backside Ni-Au contact.

Device	A	B	C	D
Substrate	n-SiC +Ar[1]	n-SiC +Ar[1]	s.i[2]-SiC	p-Si (111)
AlN (nm)	50	70	50	200
Buffer	GaN:Fe	DH[3]:C	GaN:Fe	GaN
Doping	2e18	5e18	2e18	UID[4]
Thickn. (nm)	2000	3060 +560	2000	4500
Channel layer (nm)	850	40	810	-
AlGaN Barrier (nm)	9	14	10	15
% Al	24	24	24	25

Table 3.2: Description of the devices under study

[1] SiC surface was Ar-implanted before GaN growth [83]
[2] Semi-insulating substrate
[3] Double heterostructure with AlGaN back barrier (7...2% Al content)
[4] unintentionally doped buffer

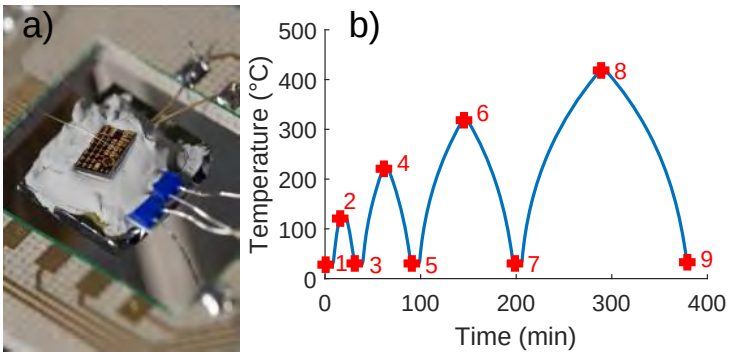


Figure 3.9: a) Detailed photo of a suspended heater module with bonded device. b) Temperature vs. time during measurement with indicated measurements points.[79]

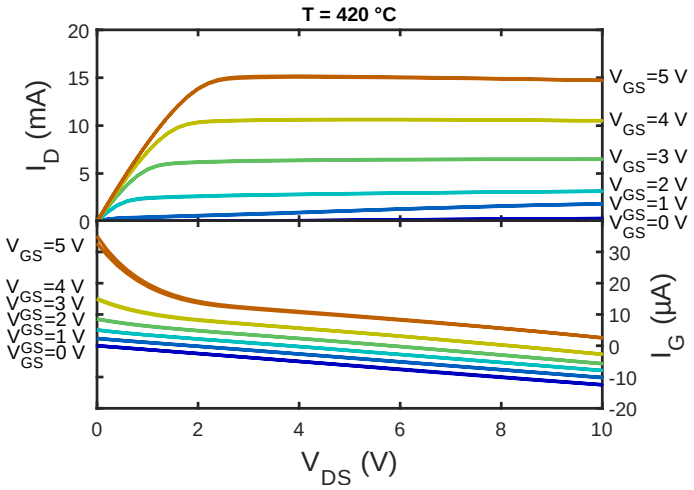


Figure 3.10: 3-terminal DC output characteristics of device D at 420 $°C$.[79]

3.2.2 High temperature DC performance

For the temperature measurements, each die was glued on a silicon substrate together with two resistive heater and a Pt100 sensor using a glue that isolates the device electrically while still conducting heat, similarly as in [84]. The heaters and the Pt100 were then soldered to a PCB. The device was then connected through wire bonding to the same PCB. Figure 3.9a shows the module soldered with the wire-bonded device. One can see that the main conductive paths for the heat are the soldering of the resistance and the Pt100. The position of the Pt100 near the device ensures that the temperature of the Pt100 is equal to the device temperature. The PCB was placed on a holder and its pins were connected to a ohmmeter for the pt100, to a voltage source for the heater, and to two SMUs for the gate-source and the drain-source measurements. A automated controller was programmed in Matlab for this setup. It was chosen to perform a long measurement overnight to check the response of these devices to a prolonged exposition to a high temperature environment. The temperature profile that was chosen is shown

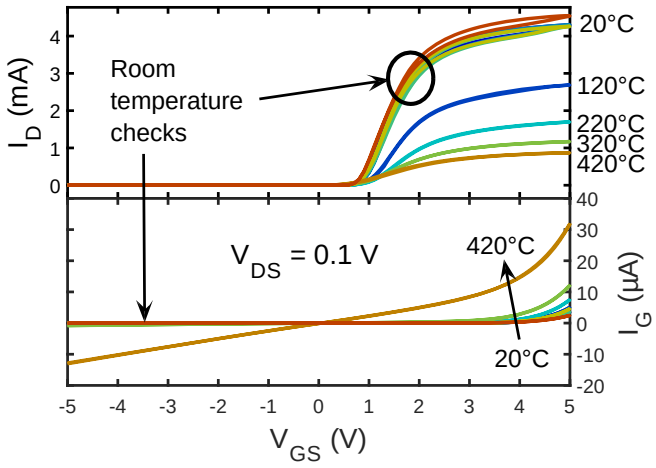


Figure 3.11: Transfer characteristics of device D at VDS=100 mV, for all steps of the measurement.[79]

in figure 3.9b. At each point the transfer, output, forward and reverse gate leakage IV was measured. The virgin device was measured first at room temperature, and then at 120, 220, 320 and 420 $°C$. Between each high temperature measurement, the device was brought down to room temperature to check its characteristics against the virgin characteristics.

The output characteristics of device D at 420 $°C$ is shown in figure 3.10, and figure 3.11 shows the transfer characteristics of device D for V_{DS}=100 mV for all temperature steps of the measurement.

The procedure for the extraction of the parameters is the following: the threshold voltage is first extracted from the transfer characteristics with V_{DS}=100 mV by using the method of the maximum transconductance [85]. The maximum drain current $I_{DMAX}$and the ON-resistance R_{ON} are extracted at fixed overdrive voltage (V_{GS}-V_{TH}) to exclude the effect of the change of threshold voltage with temperature from their extraction. The extracted parameters are shown versus temperature in figure 3.12.

Figure 3.12a shows that the general trend for the threshold voltage is to decrease with temperature. Up to 200 $°C$ the threshold voltage of devices A and D increase by a few hundred millivolts. This correlates with a large variation of their threshold voltage at room temperature between the high temperature measurements, showing that the degradation lasts at least for few hours. It also correlates with the initial value of the threshold voltage, as the devices featuring the increase both have high RT threshold voltage to begin with. The ionization of acceptor impurity in the p-GaN gate and donor in the GaN buffer at high temperature could explain the initial increase of the threshold voltage. The decrease of the threshold voltage for all devices for temperatures higher than 200 $°C$ might be caused by the increase of intrinsic carrier concentration in the p-GaN. The Fermi level in the p-GaN getting closer to the center of its band gap shifts the whole conduction band

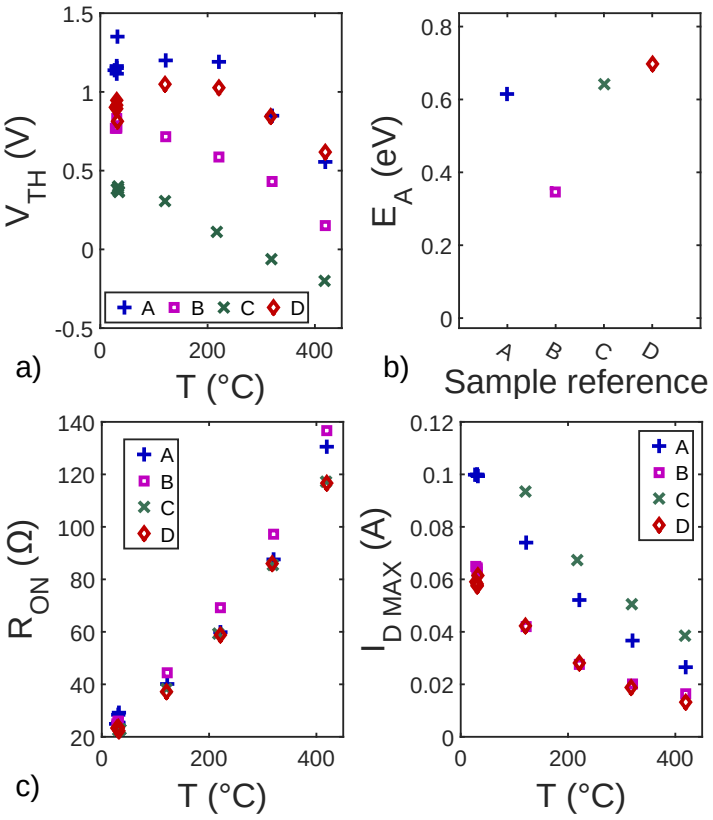


Figure 3.12: Extracted threshold voltage (a), activation energy for the forward gate leakage (saturation) current (b), ON-state resistance (c), and maximum drain current (d) in function of temperature.[79]

down. As the down shifting of the conduction band in the channel is equivalent to a decrease of threshold voltage, this effect would indeed tend to lower it. Nevertheless the effect is too weak to explain such a drop of threshold voltage of the order of -150 V/100K as observed at high temperature. The ionization of deeper residual donors in the p-GaN and residual acceptors in the GaN buffer, or other mechanisms need to be considered.

Figure 3.12d shows that the maximum drain current decreases with the temperature for all devices. Fitting the logarithm of the I_{DMAX} versus the logarithm of the temperature in Kelvin gives power law exponents in the range of 1.55 to 1.7. The model considering pure mobility degradation in long channel devices give a factor of 1.5 [86]. The difference could be explained by the temperature dependence of the access resistance. Transmission Line Matrix (TLM) structure have been measured at the same temperature as the devices and their access resistance varies with the square of the temperature up to 420 $°C$, which could be due to a decrease of the 2DEG concentration due to surface potential variations. The combination of the power 1.5 for the channel and the power 2 for the access resistance would explain the final exponents in the range of 1.55 to 1.7.

Figure 3.12c shows that the degradation of the ON-resistance with temperature is

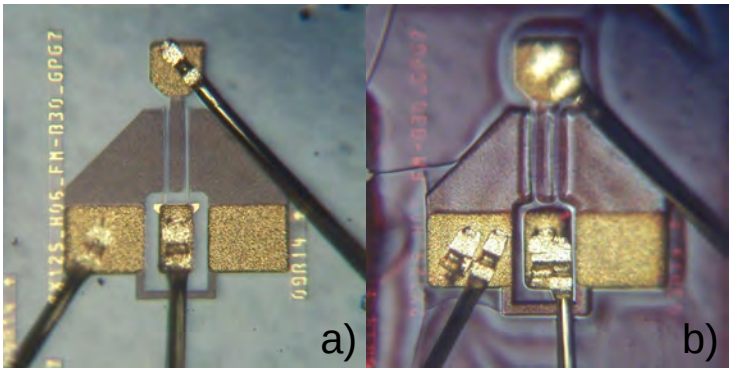


Figure 3.13: a) Virgin device. b) Device after temperature cycling, with cracked BCB passivation.[79]

quadratic, which is consistent with the square access region resistance that was measured on the TLM.

Figure 3.12b shows that the temperature dependence of the gate leakage current extracted from the forward bias saturation current, features an activation energy of 600 meV for all devices, except for device B where the activation energy is closer to 350 meV.

The devices suffered some degradation at high temperature, but the measurements at room temperature indicate that they are recoverable. Some effects such as the threshold voltage shift can be seen several hours after the measurement. Figure 3.13a and b show the device before and after the temperature measurements. The change of color is due to a reaction of polymerization of the benzocyclobutene used as passivation layer, which also expands and cracks. The material is not guaranteed to be stable at temperatures higher than 300 $^{\circ}C$.

3.2.3 High temperature blocking capabilities

The setup described in part 3.2.2 was used to measure high voltage blocking capability of device D (Gan on Si) by the step-stress methodology [74, 87] at high temperature. The step stress consists in applying a gate voltage under the threshold voltage of the device, and increase the drain voltage step by step with a fixed time for each step. In this case, the gate voltage was -4 V, and the drain voltage was increased by 20 V every 30 s. Between every step, the DC-IV output, transfer and gate leakage characteristics were performed, and the threshold voltage, ON-resistance and maximum drain current were extracted similarly as in part 3.2.2.

Figure 3.14 shows the evolution of the drain voltage in black, and the evolution of the drain current and gate current during the stresses. The axis underneath present the evolution of the threshold voltage and the maximum drain current, extracted at the end of the corresponding stress. The critical voltage for this conditions at room temperature is 360 V, where the drain current rises up to the compliance and the gate leakage rises.

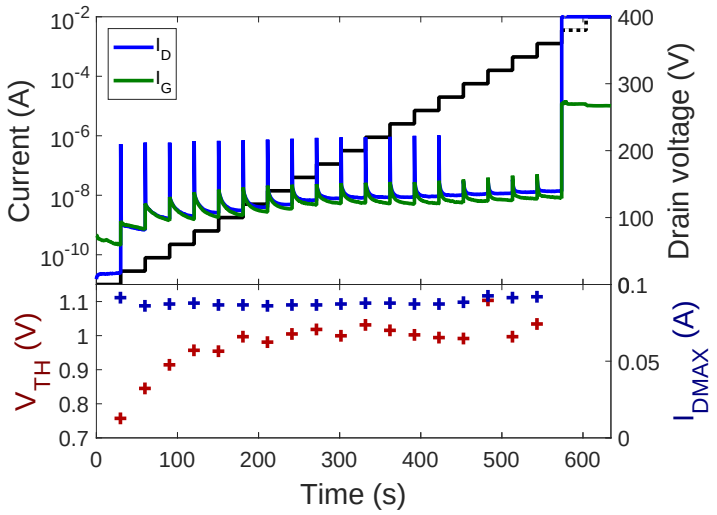


Figure 3.14: Step stress experiment on device D at 20 $°C$ and monitored post-stress threshold voltage and maximum drain current. The gate-drain separation is 6 μm.[79]

This indicates that the damage is at the gate stack, probably due to the AlGaN barrier degradation at the drain edge of the gate[88, 89]. Figure 3.15 shows the voltage and currents during the step stress experiment at 420 $°C$ and the threshold voltage and maximum drain current after every step. The critical drain voltage at 420 $°C$ is 160 V. In this case, at the critical voltage, the drain current increases, while the gate current decreases. The gate current decrease is due to the SMU reducing the voltage, as the drain current has reach compliance. The gate can therefore be considered safe during this breakdown. This indicates that at the critical voltage, the drain current flows either through the buffer under the gate (punch-through) or through the substrate. In this case, as the substrate is floating, the drain voltage needs to be high enough to provoke the break down of the drain to substrate, and the substrate to source, so it should not depend of the gate-to-drain distance [13]. Two devices with 10 and 15 μm as gate to drain distance were measured in the same way showing the same critical drain voltage, and no damage to the gate. This supports the hypothesis of the vertical breakdown as cause of the low blocking capabilities at high temperature.

One can notice that during all the step, gate and drain currents decrease with time at room temperature (see figure 3.14), while they increase at 420 $°C$ (see inset of figure 3.15). This phenomenon is correlated with the variation of threshold voltage at the end of these pulses, increasing for room temperature, and decreasing for high temperature. The drain current decrease can be explained by the trapping of electrons in the barrier[73, 90] or in the bulk [91] whereas the current rise could be explained by the creation of defects in the AlGaN barrier [72, 73, 89, 92].

Similar results have been obtained in device B.

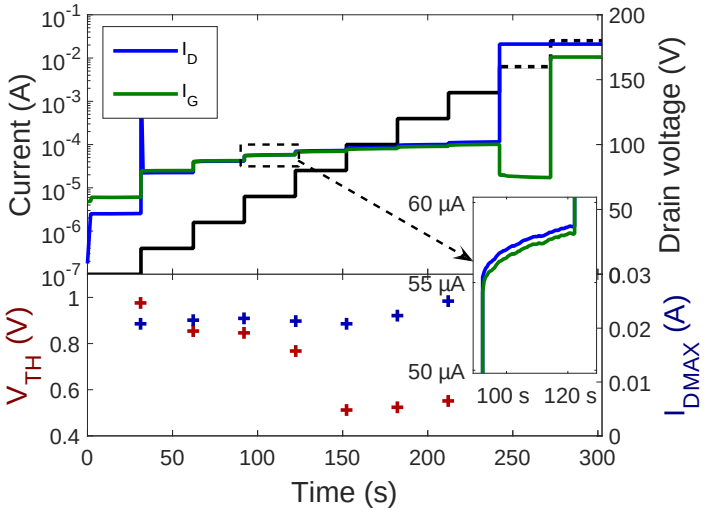


Figure 3.15: Step stress experiment of device D at 420 °C and monitored post-stress threshold voltage and maximum drain current. Inset: Zoom (linear scale) on 60 V stress.[79]

3.2.4 Vertical leakage current dependence on temperature

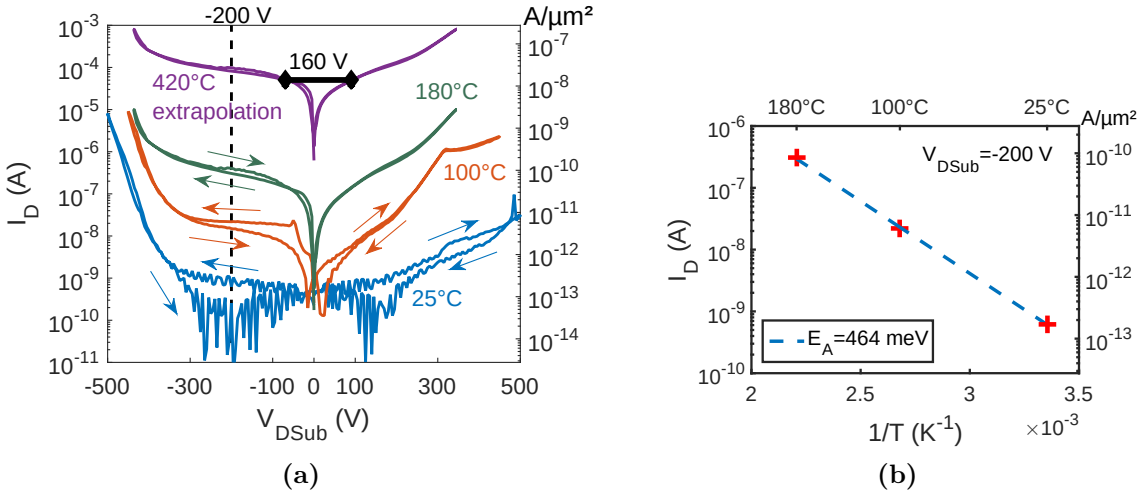


Figure 3.16: (a) Vertical breakdown IVs and corresponding current density at 25 °C, 100 °C and 180 °C on device D, and extrapolation to 420 °C (b) Arrhenius plot of vertical leakage on device D at $V_{DSub} = -200\ V$.[79]

To characterize the devices vertically and assess the role of vertical breakdown in the high temperature breakdown that has been shown in part 3.2.3, the chips corresponding to devices B and D were mounted on a copper tape with siver paste on the backside, and a wire was soldered to the copper. The device was then placed on a heater with a thermostat, which in turn was placed on a needle probe station. The drain of the devices was contacted using a DC probe needle and the substrate was grounded through the wire connected to the copper tape. This setup does not allow for temperature as high as the

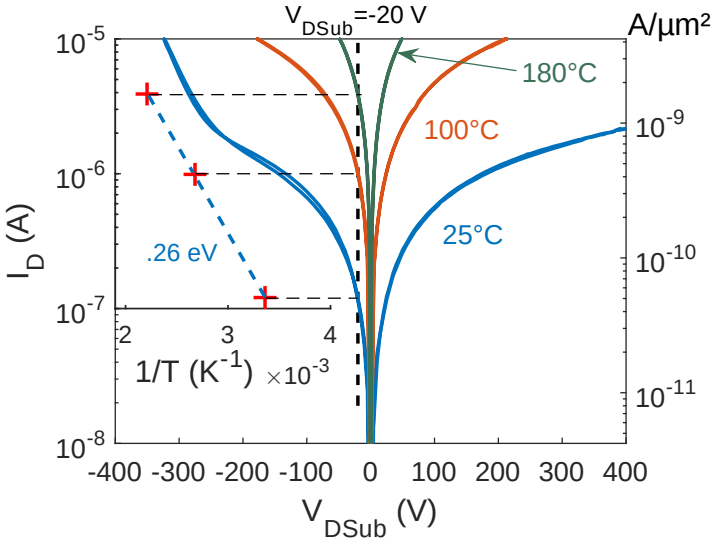


Figure 3.17: Vertical leakage IVs and corresponding current density at 25 $°C$, 100 $°C$ and 180 $°C$ on device B. Inset: Arrhenius plot of the vertical leakage on device B at $V_{DSub} = -20\ V$.[79]

setup described in part 3.2.2, but the latter is not suitable for vertical measurement, as the dices are contained in the glue from all sides. For this setup, vertical measurement would only be possible with a top contact for the substrate.

The DC vertical leakage was measured at 25, 100, and 180 $°C$. The voltage was swept from 0 to -500 V and back, and from 0 to +500 V and back. The current compliance was set to 10 μA. Figure 3.16a and figure 3.17 show the vertical leakage IV of device D and B, respectively. At room temperature, device D presents sub-nA leakage up to 300 V at both polarity whereas device B shows an ohmic behavior in this range. Both devices show an exponential increase of the current beyond -300 V. At 180 $°C$ device D feature a ohmic behavior up to 300 V in both polarity.

To evaluate what the role of the vertical breakdown would be in the case of the step-stress at 420 $°C$ in device D, the ohmic dependence on the temperature was analyzed by plotting the leakage current at -200 V in an arrhenius plot. The results is shown in figure 3.16b. The activation energy was extracted and used to provide an extrapolation of the vertical leakage at 420 $°C$, which is represented in figure 3.16a. To assess the current that would be flowing provided a 160 V drain voltage, one should find the current value where the sum of the voltage for drain to substrate and substrate to drain (here the drain and the source are considered the same) is 160 V. Graphically, this is equivalent to find the current at which the positive voltage and negative voltage curves are separated by 160 V. On the extrapolation curve in figure 3.16a, one can see that the current would be close to 50μA. The drain current before failure in device D during the step-stress was of this order of magnitude. Considering that part of this current flows in the gate, the vertical leakage might be the main component of the source current. The high vertical current density

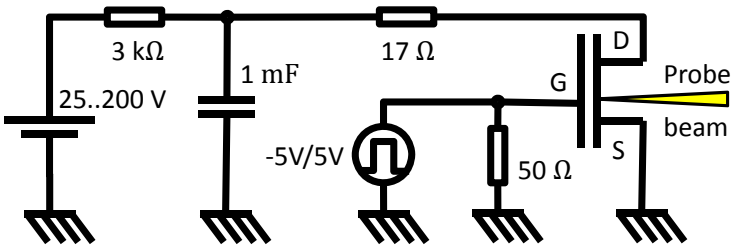
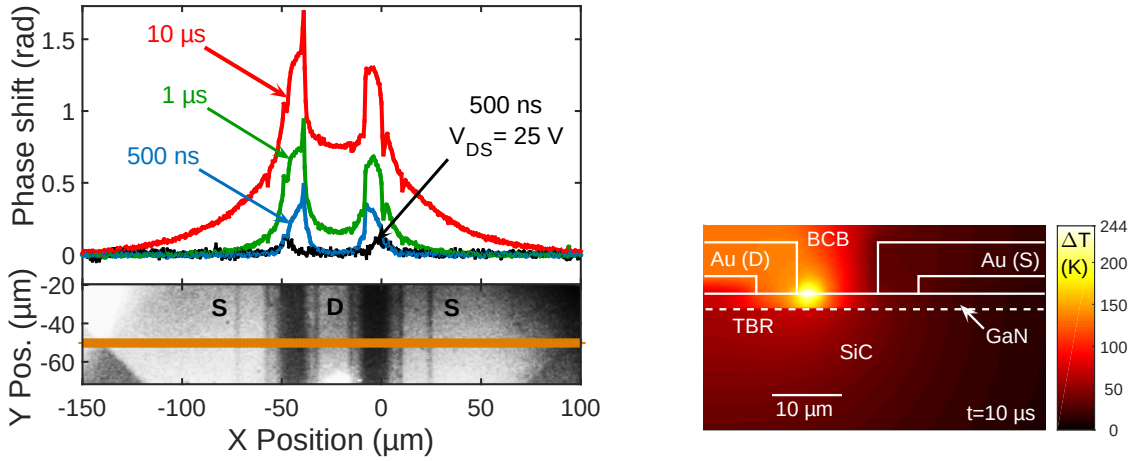


Figure 3.18: Electrical connections for the TIM measurements in short circuit load conditions

of 10 $nA/\mu m^2$ associated to the time dependence of the vertical breakdown described in part 3.1.4 may explain the vertical failure of the device.

3.3 Short circuit conditions

3.3.1 Power dissipation and reliability

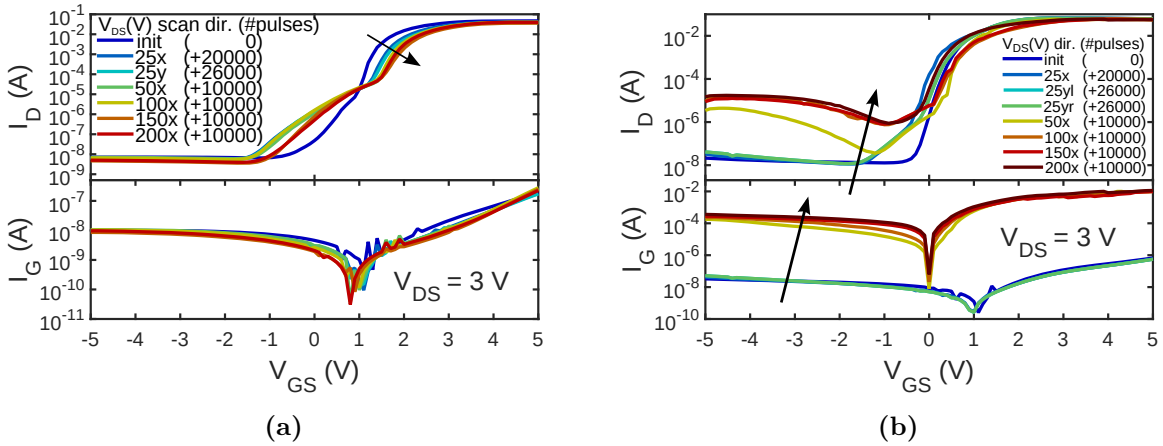


(a) (b)

Figure 3.19: (a) Top: Phase distribution across the two fingers at different time instants; V_{DS}=200 V. Average current = 80 mA. The device gate width is 0.25 mm and L_{GD}=10 μm. Bottom: backside infrared picture of the middle part of the device where the scan was performed. [93] (b) Temperature simulation results at the end of 10 μs long pulse at V_{DS}=200 V stress. Only half of the structure was simulated. [93]

The results presented in this section were published in [93].

The TIM technique described in part 1.4.2.1 was used to characterize the p-GaN gate HEMTs devices in a situation close to short circuit load conditions. Figure 3.18 shows the electrical connections for the TIM measurements. The HEMTs were biased with a constant drain to source and the gate to source voltage was pulsed from -5 V to +5 V for 10 μs using the solid state pulser with a baseline of -5 V and a pulse amplitude of 10 V.



(a) **(b)**

Figure 3.20: (a) 3-terminal DC transfer characteristics of the device from figure 3.19a monitored after each TIM scan. The legend lists the TIM scans applied to the device, with VDS and number of pulses; "+" means cumulative stress.[93] (b) 3-terminal DC transfer characteristics monitored after each TIM scan of a device with early cumulative damage.[93]

This results in the opening of the channel during 10 μs. The load of the device was a 17 Ω resistance, that was also used to measure the current by placing the oscilloscope probe at its pins. The SMU that was used to bias the drain was connected in parallel to a 1 mF capacitor, that was used as a buffer to provide a constant voltage during the pulse. Scans were performed for V_{DS}values of 25, 50, 100, 150 and 200 V. Between two scans, DC-IV transfer and output characteristics were performed to measure the degradation of the device due to the cumulative stress. Additionally, the access region of the device was imaged by making a reflectivity map using the TIM probe beam.

The main result of the TIM are presented in figure 3.19a. The black curve shows the TIM phase shift at 500 ns for V_{DS}=25 V. It indicates that the power dissipation is located at the gate. By comparison the blue curve shows the same measurement at V_{DS}=200 V, showing that the power is mainly dissipated in the access region towards the drain. These results support the observations from other groups in various time domains [35, 94, 95]. Thermal simulations have been performed to estimate the absolute temperature distribution of the device from the power dissipation location indicated by the TIM results and thermal parameters from [96], including a thermal boundary resistance at the GaN/SiC interface. Figure 3.19b shows the simulated temperature distribution in the device for the power dissipation distribution extracted from V_{DS}=200 V. The maximum temperature increase of 244 K is reached at 10 μs.

Figure 3.20a shows the transfer characteristics of the device measured after each scan. The legend indicates the number of pulses that stressed the device and the V_{DS} bias during these pulses. This device has not suffered a major degradation during the experiment. Figure 3.20b shows the post-stress transfer characteristics of a device that has

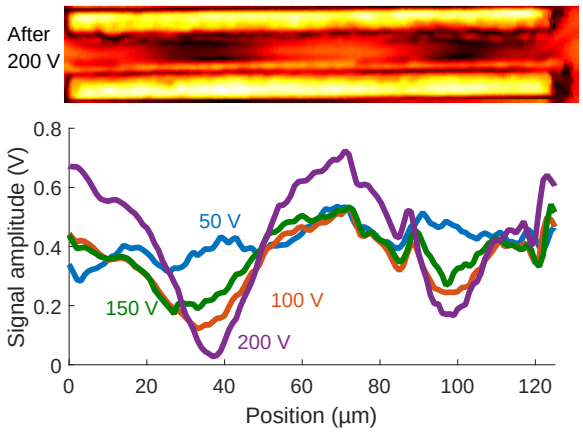
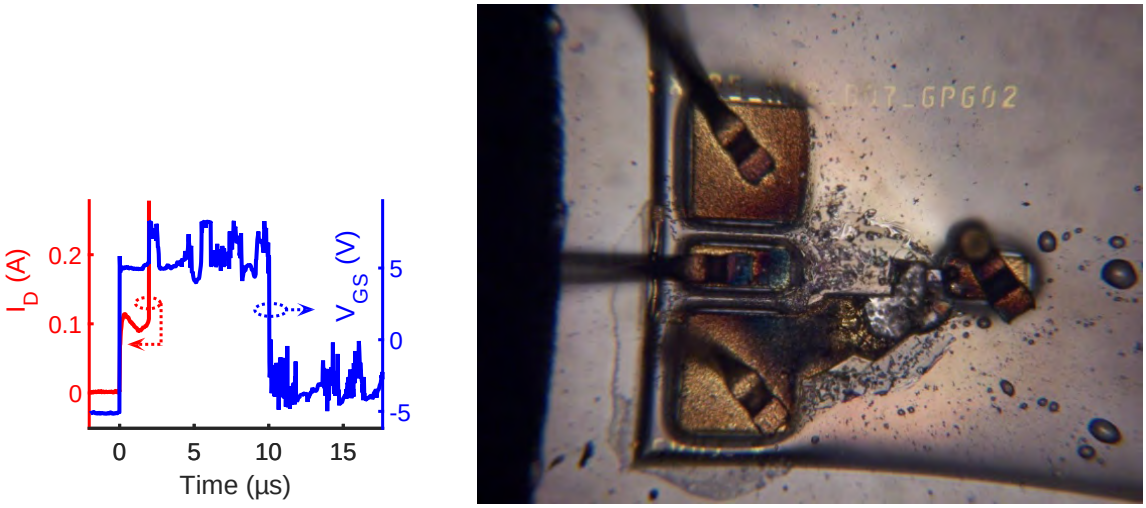


Figure 3.21: Top: 2D reflectivity scan after cumulative damage after TIM scan at V_{DS}=200 V. The yellow parts are the high reflecting source and drain contacts. Bottom: Line reflectivity scan after TIM scans at different V_{DS}, showing the evolution of the cumulative damage of the passivation layer (delamination). [93]



(a) (b)

Figure 3.22: (a) Drain current and gate voltage waveform during single shot damage of a device (V_{DS}=200 V) [93] (b) Top-side view of a typical single shot damage of a device. [93]

been degraded by the cumulative stressing of the TIM experiment. One can see that the effect of the first stress at V_{DS}=25 V is to rise the sub-threshold-voltage drain current, which was also observed in figure 3.20a. After the stress at V_{DS}=50 V, one can see that the gate leakage is increased, as well as the drain current in off-state. Figure 3.21 shows the reflectivity scan of the channel and the access region. One can see that two regions around 40 μm and at around 100 μm in the gate width optically change, as their reflectivity is reduced throughout the experiment. After the stress at V_{DS}=200 V, one can see that the reflectivity in the central region has increased. This effect can be explained in

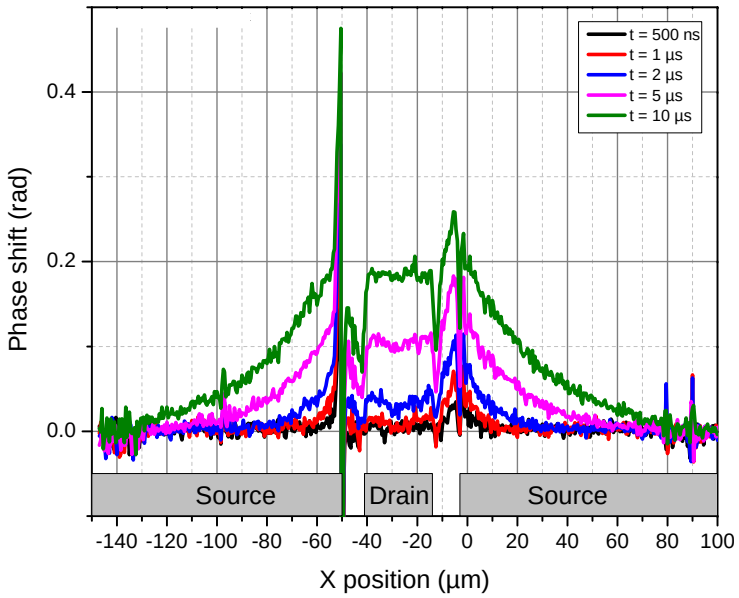


Figure 3.23: Phase shift extracted from a TIM scan across the channel of a HEMT

terms of delamination of the polymeric passivation due to the mechanical stress induced by the thermal dilatation, similarly to the cracking that have been seen after the high temperature measurement in part 3.2.2, with the added effect of a temperature gradient. The delamination might cause the change of the reflectivity by causing a change of the thickness of the existing layers of the passivation, and by creating new interfaces. Both of these change would have an effect on the multiple reflection constructive and destructive interference. This would also explain why the reflectivity that is measured with a single wavelength coherent source can feature such reflectivity change, whereas the backside infrared microscopy using a broadband light does not allow to see these features. In general this change of reflectivity may have a large impact on the phase shift dependence on the temperature. The scans that are shown in this part are performed in the area that suffers the least from this effect (at Y=60 μm along the width, see figure 3.21). The degradation of the optical properties has not been found to correlate with the electrical damage measured by the transfer characteristics. Some device have suffered a destructive thermal breakdown during the first pulse of the TIM scan at high voltage. Figure 3.22a shows the measured drain current and the gate voltage during such an event at V_{DS}=200 V. The failure occurs at $t = 2\ \mu s$ where it can be seen that the drain current rises. Figure 3.22b shows the device after this destructive pulse, showing metal burnout. Notice the melting of the drain and source bonding wires, which might have reduced the damage by acting like a fusible.

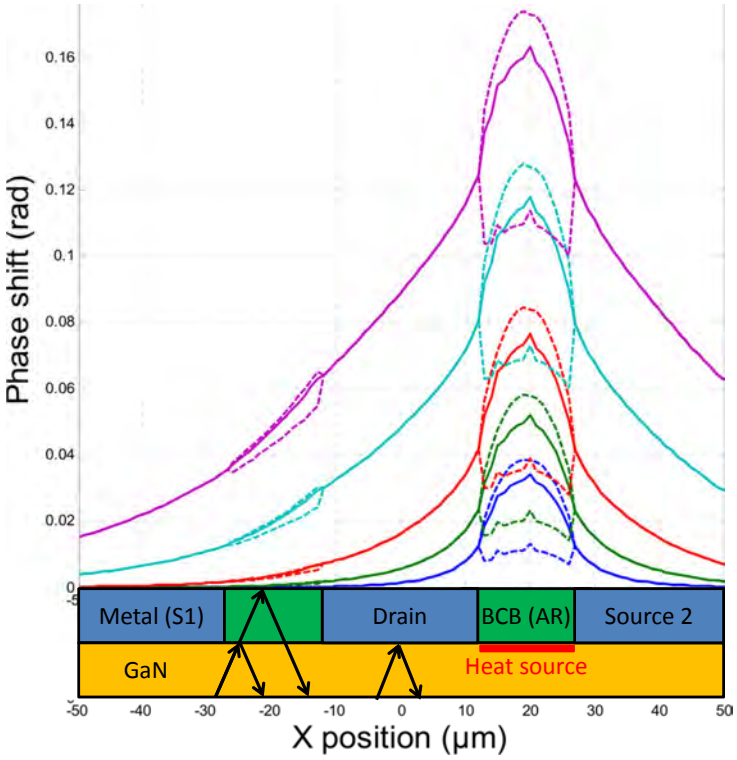


Figure 3.24: Simulated range of phase shift for BCB thickness variation in the access region area computed with transfer matrices applied to thermal simulation data using a uniform heat source (in red) in the right access region (AR). The multiple reflections of the beams are shown with arrows.

3.3.2 A new method for power dissipation and temperature extraction from TIM data

The results presented in this section were presented in [97].

3.3.2.1 Optical artifacts in the access region.

Figure 3.23 shows the TIM phase shift in a p-GaN HEMT device with a gate to drain distance L_{DG}= 10 μm under the previously described short circuit load like conditions, with V_{DS}=25 V. This device features a 14-nm-thick Al0.23Ga0.77N barrier and a 3.2-μm thick GaN buffer layer grown on a SiC substrate[83].

The measured current was 80 mA, so the total dissipated power in the two 125-μm-wide channels was 2 W.

On figure 3.23, one can see that the left finger features a weaker phase shift than the right finger. If one trusts the value of the phase shift in the access region, one should conclude that twice as less heat is dissipated in the left finger. In contrast, the value of the phase shift outside of the access region (marked as source and drain) shows a perfect symmetry with respect to the center of the drain contact (X=-25 μm), which indicates

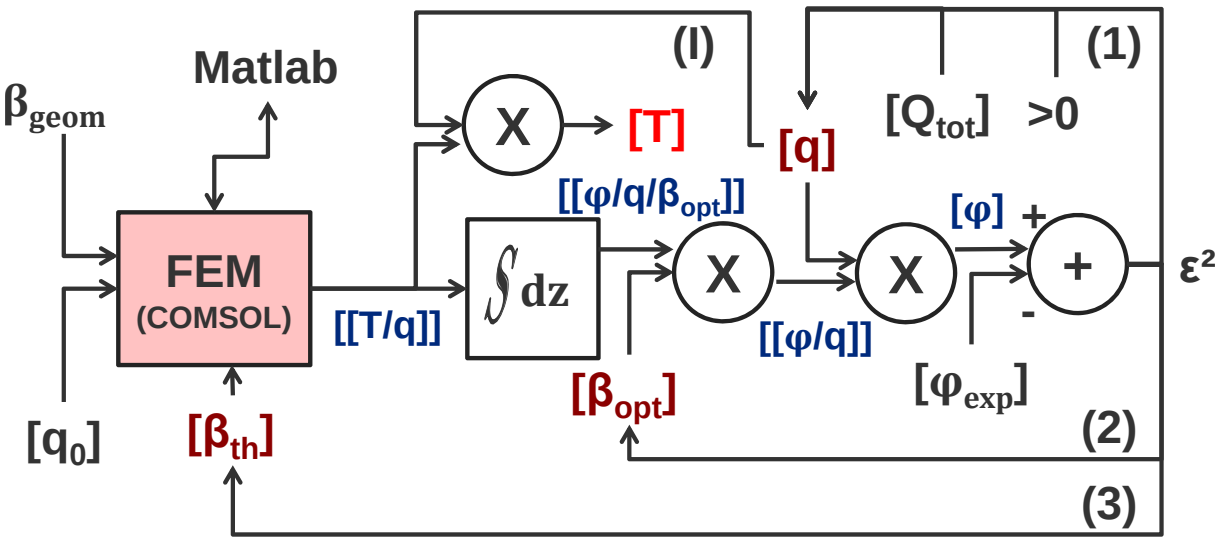


Figure 3.25: Block diagram describing the algorithm for temperature extraction from the TIM data

that the heat distribution is symmetrical. Furthermore the value in the left source area is higher than in the left channel, showing that if the heat that is measured in the left access region cannot be originated in the left channel, as heat flows from warm to cold areas. The right finger displays a phase shift that can be interpreted as the heat signal without problems but it seems that the phase shift in the left finger is distorted.

The reason for the distortion could be the multiple interference due to BCB thickness variation, possibly due to delamination. Contrary to the case showed previously where the passivation layer was degraded by the cumulative stressing of the device, the TIM scan is performed on a virgin device, so the thickness variation is process related.

To assess the effect of a variation of the passivation layer on the phase shift, a transient thermal simulation was performed in COMSOL, with only one homogeneously active finger on the right. The resulting distribution was fed to a Matlab program that computes the phase shift using the transfer matrix approach. Additionally the program performed 100 different variation of the thickness of the passivation within half wavelength. Figure 3.24 shows the simulated phase shift in the device. The plain lines correspond to the single reflection case, and the dashed line show the maximum and minimum phase shift values computed from the multiple reflection model when varying the passivation thickness. This variation explains well the experimental results shown in figure 3.23 and why the phase shift in the access region can be unreliable. Any power dissipation that relies on a linear response of the phase shift to the refractive index variation, like [43] will suffer from this distortion (see more in section 1.4.2.1). The simulation also shows that the data from the area under the source and the drain is reliable. The next part will show an attempt to use this data to recover the power dissipation and temperature in the device.

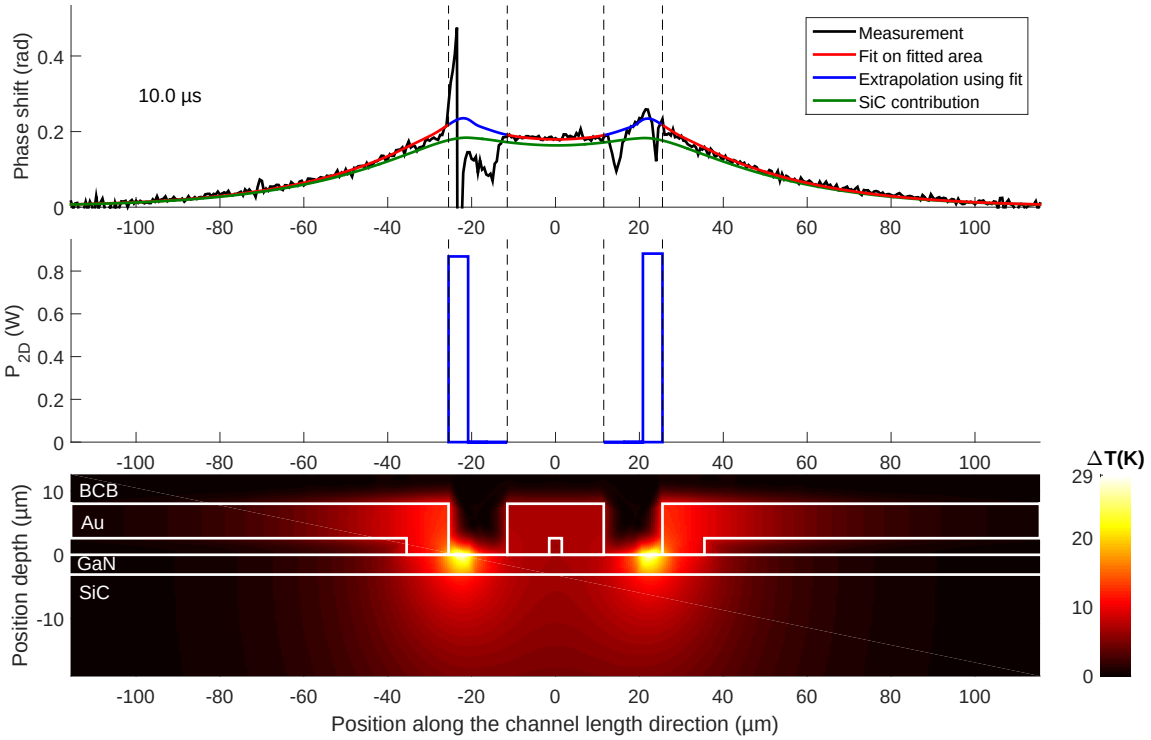


Figure 3.26: Phase signal and fitted phase signal, extracted power and extracted temperature of the top GaN layer at t = 10 μs.

3.3.2.2 Use of optical and thermal simulation for data analysis

The solution that is proposed is to use the thermal model coupled to the phase shift computation that has been introduced in the previous paragraph. If one computes the phase shift distribution that corresponds to the activation of both fingers independently with a 1 W power source, one can fit the experimental phase shift distribution with the simulation in the drain and source contact areas, where the fitting parameters are the power in each channel. This gives a power dissipation that is based only on the data of the drain and source contact areas, and does not take into account the unreliable data of the access region. From there it is possible to recover the temperature in the channel by multiplying the simulated thermal distributions by the fitted powers in the fingers. Note that the temperature distribution that corresponds to the activation of the right finger only requires mirroring the distribution for the left finger, so in total only one transient thermal simulation is needed. Also note that this process is used because the thermal diffusion equation is assumed linear with the heat source distribution, and the phase shift is assumed linear with the heat distribution in the single reflection model that is implemented for the computation of the phase shift.

This idea can be taken further by dividing each access region into several regions

along the length of the fingers, and several time intervals, that constitute independent heat sources in the access regions and during the pulse width. For n_x regions per finger and n_t intervals in time, only n_x thermal simulations need to be performed. The temperature distribution corresponding the the same source in the opposite finger can be obtained by mirroring and the same heat source at a later time by introducing a delay in the data. The $2 \times n_x \times n_t$ resulting phase shift distributions are fitted against the experimental phase shift, giving the power dissipation for all the heat sources. These sources constitute the power dissipation P_{2D}.

Figure 3.25 shows a block diagram describing the algorithm. The sequence starts on the left with COMSOL computing the temperature distribution for several unitary (1 W) heat sources (noted $[q_0]$) in the device and at different times (the symmetry and delaying by Matlab is not shown). The results are named $[[T/q]]$ as it can be multiplied by a matrix of values representing the heat sources to obtain a transient temperature distribution. Integrating in every layer gives a matrix $[[\varphi/q/\beta_{opt}]]$, where $\beta_{opt} = \frac{4\times\pi}{\lambda}\left[\frac{dn}{dT}\right]_{300K}$ is the matrix that contains the thermooptical coefficients for each layer (initially literature values). By multiplication with β_{opt}, the phase distribution matrix $[[\varphi/q]]$ is obtained. At this stage, one can associate a transient phase shift distribution to a transient power distribution by multiplication. The uniform constant distribution will be used as a first guess. The following block compares the simulated phase shift $[\varphi]$ to the experimental data $[\varphi_{exp}]$ and gives the sum of the residuals ϵ^2. The loop (1) will then perform a least square fitting of the experimental phase shift, where $[q]$ is the fitting parameter. Once $[q]$ is found, it can be multiplied by $[[T/q]]$ to find the transient temperature distribution [T].

The size of the heat sources in space and time mostly depend on the dimensions of the device and the pulse width. As the diffusion tends to filter the high spatial and time frequency components, having more sources is not useful if the difference between the signal coming two of them is smaller than the noise of the experimental signal when they arrive at the contact region. This is linked to the ill-posed nature of the inverse thermal conduction problem [98]. Feeding simulated data to the algorithm works fine, but there is generally a problem of over-fitting with this method when applied to real data. One of the way to correct it is to apply constraints to the optimization algorithm that fits the data. To this purpose, the total power, i.e the sum of the powers at the same time instant, is fixed to the power that was measured during the TIM experiment at that instant. The second condition is that the power for every source at any time should be positive. This prevents the algorithm to over-fit the data with the equivalent of dipolar field for heat distribution. This two conditions are noted in loop (1) in the block diagram in figure 3.25. Note that this algorithm mainly fits the difference in the phase shift nearby the active region between the homogenous case and the measured case. If the homogenous case is not well modeled, the difference will not only be due to an inhomogeneity, but partially to this error. The Lagrangian parameters of the results, that can be understood as the "'reaction force"' that the constraints put on the solution,

are good indications of the matching between the model and the reality, as with a model that uses the right thermal and optical parameters, the constraints should play a minimal role. The thermal and optical parameters of the model should therefore be optimized on the tail of the experimental phase shift distribution (i.e far from the device, or after the end of the pulse) before using the algorithm, but can also be tuned further in the active region by looking at the outputs of the algorithm. The data of several scans on the same device at different voltage can be combined for this purpose. These are loops (2) and (3) in the block diagram in figure 3.25.

Figure 3.26 shows the result of this algorithm applied to the TIM results that have been presented in figure 3.23. On the top window, one can see the experimental phase shift in black. The phase shift represented in red and blue is the simulated phase shift corresponding to the best fit of the power source. Only the red part of the phase shift is compared to the experimental data, as the data in the access region is not trusted. Nevertheless, in the center of the right finger region, the simulated and experimental values match quite well. In contrast, in the left finger, the simulated phase shift indicates much higher value than the experimental data. The algorithm was therefore able to predict the value of the phase shift in the right finger, that has not suffered delamination, with a good precision. The green curve shows the contribution of the silicon carbide substrate to the phase shift. This is important to take into account in the model, especially if the thermo-optical parameters of the two layers are different, as the same total heat produces different phase shift depending on its distribution in the layers. The differentiation method [99] is not able to face this problem. The second window indicates the power distribution in the last microsecond at the end of the pulse. The power dissipation still appear at the gate side of the finger, as at the beginning of the pulse. The bottom window shows the simulated temperature distribution at the end of the pulse (t = 10 μs), that corresponds to the fitted power dissipation transient distribution. The maximum temperature increase is 29 K at both gates positions.

Chapter 4

Conclusion and prospects

Through various types of characterization techniques, the behavior of devices under various types of electrical overstress has been studied.

The robustness of Hetero-junction Bipolar Transistors with a Silicon-Germanium base has been studied using a transmission line pulser and optical techniques. The intrinsic (high current, voltage limited) and extrinsic (low current, du/dt limited) failure modes have been identified and analyzed using TLP, TIM and failure analysis on multifinger devices and test structures.

The favored hypothesis for the intrinsic high current failure is the breakdown of the silicon in the sub-collector region. Adjusting the geometry of the base contact of the sub-collector region could lead to an increased ESD protection.

The favored hypothesis for the extrinsic low I_{T2} mode is the triggering of the transistor due to parasitic clamping the emitter voltage, thus having electrons injection from the emitter in the base. The solution would either involve a decrease of the base series resistance, or the tuning of the parasitic capacitance. These are however important for the RF performance of the transistor.

This study shows that ESD should be considered very early in the device development to optimize the ESD self protection performance.

Standard and open-base Silicon Controlled Rectifiers were analyzed using EMMI, and TIM under TLP. In standard SCR with trigger taps, the trigger taps have been identified as the main source of leakage in breakdown, and the holding current flow location has been identified using EMMI. The standard SCRs were measured with TIM while triggered, showing injection peaks at the two forward-biased junctions. The trigger taps were shown to be the initial triggering position. The ON-state spreading has been measured at roughly 1 μm/ns, which is compatible with the results of TCAD simulations.

Measurements on the open base SCRs showed that the time-to-breakdown could be linked to conductance modulation in the p-sub. A low rise time was found to be critical

to trigger all finger at the beginning of the pulse due to dU/dt effect. For long rise times, a triggering propagation from finger to finger was found using TLP, and confirmed with TIM.

At high current the whole current path from the signal p+ to the ground n+ has been found to dissipate heat, with a peak of heat at the ground n+ which might be the cause of the thermal damage at higher current. These measurements show that there is a trade-off to be made between triggering and heat management. Further iteration of design and measurements could enable a better performance of these devices .

Gallium Nitride High Electron Mobility Transistors were characterized electrically and optically under various electrical overstress.

The vertical breakdown study showed that fitting cumulative density function with known distributions can give an insight to the diversity of the mechanisms taking place. The time to breakdown behavior was evidenced for vertical breakdown. These results have lead to deeper research on the topic in the last years. [100] The filamentary nature of the vertical breakdown was observed by using infrared microscopy as a failure analysis method. This methodology can be used to see weak points in the vertical breakdown in future designs.

The high temperature performance of GaN HEMTs has been quantified in DC, and the blocking capabilities have been shown to decrease at 420°C. Evidence has been shown that vertical breakdown is most likely the cause of the degradation of the blocking capabilities. This could lead to further optimization of the buffer hetero-epitaxy to minimize the vertical leakage at high temperature.

In short circuit load conditions, TIM proved that the HEMTs have their power dissipation on the gate side at low voltage, and at the drain side for high voltage. The reliability was analyzed and various outcomes were observed from low degradation to hard damage. The delamination of the passivation was observed.

A new analysis technique of TIM data has been developed, allowing the extraction of the power dissipation using only the phase shift under the metalizations. The main advantages and defects of this technique have been discussed. In the specific case of GaN HEMTs, this technique has been proven immune to the some of the optical artifacts. The technique should soon be applied on other devices suffering similar artifacts.

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Abbreviations

Symbol	Meaning
AlGaN	**Al**uminum **Ga**llium **N**itride
AR	**A**ctive **r**egion
BJT	**B**ipolar **J**unction **T**ransistor
BCB	**B**enzo**c**yclo**b**utene
BOX	**B**urried **O**xide
DC	**D**irect **C**urrent
DC-IV	**D**irect **C**urrent **I**ntensity **V**oltage characteristics
EMMI	**Em**ission **Mi**croscopy
ESD	**E**lectro**s**tatic **d**ischarge
FIB	**F**ocused **I**on **B**eam
FP	**F**abry **P**érot or **F**ield **P**late
FPA	**F**ocal **P**lane **A**rray
GaN	**Ga**llium **N**itride
HBM	**H**uman **B**ody **M**odel
HBT	**H**etero-junction **B**ipolar **T**ransistor
HEMT	**H**igh **E**lectron **M**obility **T**ransistor
InGaAs	**In**dium **Ga**llium **Ars**enide
IR	**I**nfra**r**ed
OBIC	**O**ptical **B**eam **I**nduced **C**urrent
ob-SCR	**o**pen-**b**ase **S**ilicon **C**ontrolled **R**ectifier
OSS	**O**N **S**tate **S**preading
RF	**R**adio **F**requency
SCR	**S**ilicon **C**ontrolled **R**ectifier
SEM	**S**canning **E**lectron **M**icroscope
Si	**Si**licon
SiGe	**Si**licon-**Ge**rmanium
TIM	**T**ransient **I**nterferometry **M**apping
TLP	**T**ransmission **L**ine **P**ulser
TLP-IV	**T**ransmission **L**ine **P**ulser **I**ntensity **V**oltage characteristics
USB	**U**niversal **S**erial **B**us

Curriculum vitae

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Electro-optical characterization of Gallium-Nitride-based power switches, Silicon-Germanium Heterojunction Bipolar Transistors for RF low noise amplification, and Silicon Controlled Rectifiers as external ESD protection under EOS/ESD events. Measurements of GaN, Ge, InN, ZnO devices. Programing of measurement setup and post-processing for emission microscopy and transient interferometric mapping.

Partners Infineon Austria, Infineon Germany, Nexperia

2012 **Intern**, *STMicroelectronics*, Crolles, France.

(Micro-)optical study and design, mechanical study and CMOS detector bending processes for a curved detector camera using optical and mechanical simulation.

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Institut f. Sensor- und Aktuatorsysteme, Vienna, Austria

Design and characterization of piezoelectrically actuated resonant microstructures for measurements in fluidic media.

2011 **Intern**, *EADS – Defence and Security Systems*, Paris, France.

Measurement tools maintaining in a research and development laboratory.

Education

2012–Present **PhD in technical Sciences**, *TU Wien*, Vienna, Austria.
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thesis Behavior of Silicon and Gallium Nitride devices under electrical overstress conditions

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teaching Electrical measurements of RF devices

2011/2012 **Dipl.Ing./Master of Science**, *Grenoble INP*, France.
MSc in Microelectronics

thesis Study of the optical interest and mechanical feasibility of an imaging sensor implemented in a flexible and deformable silicon membrane.

2010/2012 **Master NANOTECH**, *Grenoble INP (France), Politecnico di Torino (Italy), EPF Lausanne (Switzerland).*

Specialized international Master in nanotechnology.

Languages

French	Mother tongue
English	Fluent
German	B2
Italian	B2
Spanish	B1

Technical skills and competences

Programing	C, assembler, VHDL, Python
Computer	AutoCAD, CADence, COMSOL, Matlab, Eagle, Zemax
Characterization	Clean room tools, transmission line pulser, optical setups

Interests and activities

Acting	Les Médusés du Radeau (MDR), in Vienna
Scuba diving	lately in Teneriffe and Corsica (FFESSM P3 - CMAS ⋆⋆⋆)
Cycling	Experienced tandem pilot with visually impaired partners

List of publications

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