Diplomarbeit

Monolithic Integrated RF Power Amplifier for GSM 2+

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Abstract

This work presents the design and characterization of a monilithic integrated 1.75 GHz RF power amplifier for an EDGE mobile phone. The two-stage differential design was fabricated in *austriamicrosystems*' 0.8 μm SiGe BiCMOS process. Transistors for both amplifier stages were designed, along with the integrated input balun and the integrated interstage transformer. An off-chip harmonic matching network and balun was also designed. The power transistors were characterized. While the amplifier did not live up to expectations, a model for the parasitics of the power transistors was developed and recommendations can be given regarding power amplifier design and the selection of a fabrication process

Zusammenfassung

Gegenstand dieser Arbeit ist das Design und die Charakterisierung eines monolithisch integrierten 1.75 GHz Hochfrequenz-Leistungsverstärkers für ein EDGE-Mobiltelefon. Der zweistufige, differentielle Verstärker wurde bei *austriamicrosystems* in einem 0.8 μm BiCMOS Prozess gefertigt. Die Transistoren für beide Verstärkerstufen, sowie der integrierte Eingangsbalun und der integrierte Transformator zwischen Treiber- und Leistungsstufe wurden entworfen und simuliert. Die Leistungstransistoren wurden charakterisiert. Obwohl der Verstärker hinsichtlich Ausgangsleistung und Linearität weit hinter den Simulationsergebnissen zurückbleibt, konnten Modelle für parasitäre Elemente der Leistungstransistoren entwickelt werden und Empfehlungen für die weitere Vorgangsweise und die Auswahl eines Fertigungsprozesses gegeben werden.

Acknowledgements

My thanks go out to the many people who provided generous help during my thesis work. The colleagues at the Institute of Electrical Measurements and Circuit Design, first and foremost my advisor Markus Mayer, helped me master the black magic of RF design and provided immeasurable guidance during measurements (and much-needed encouragement after looking at some of the results). I am also indebted to the fine people at the radio-frequency design group at *austriamicrosystems*, who introduced me to the art of integrated circuit design and ever had a watchful eye on my creations. Special thanks are due to Martin Dechant for many insightful discussions. This work was supported by *austriamicrosystems* AG, Unterpremstätten.

T. D.

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List of Abbreviations

ACPR	Adjacent Channel Power Ratio
ASITIC	Analysis and Simulation of Spiral Inductors and Transformers for ICs [simulation software]
BJT	Bipolar Junction Transistor
BiCMOS	[combination of] Bipolar and CMOS
CAD	Computer-Aided Design
CMOS	Complementary Metal Oxide Semiconductor
DC	Direct Current
EDGE	Enhanced Data Rates for GSM Evolution
EM	Electromagnetic [Simulation]
FET	Field-Effect Transistor
GMSK	Gaussian Minimum-Shift Keying [modulation scheme]
GPRS	General Packet Radio Service
GSM	Global System for Mobile Communications
HBT	Heterojunction Bipolar Transistor
HSCSD	High-Speed Circuit Switched Data
IMD3	Third-order Intermodulation Distance
IP3	Third-order intercept point
MS	Mobile Station
PA	Power Amplifier
PAE	Power-added Efficiency
PCB	Printed Circuit Board
PSK	Phase-Shift Keying [modulation scheme]
RF	Radio Frequency
RFC	RF Choke
RMS	Root Mean Square
UMTS	Universal Mobile Telephone Service
VBIC	Vertical Bipolar Inter-Company Model
VSWR	Voltage Standing-Wave Ratio

Chapter 1

Introduction

Since its humble and analog beginnings in the 1940s, mobile telephony has steadily improved, both in utility and in cost. This is owed not in the least to the advances made in RF engineering in the past decades.

State of the art for mobile handset power amplifiers are gallium-arsenide (GaAs) heterojunction bipolar transistors (HBTs), which are assembled into hybrid modules. In recent years, interest in silicon-germanium (SiGe) monolithic integrated circuits for radio-frequency applications up to several GHz has sprung up. Monolithic integration offers small device size combined with low cost per unit for high quantities, which are highly desirable traits for circuits used in mobile phones. The challenges the designer of such a monolithic integrated circuit is confronted with include only limited power capability and noticeable changes of the device parameters due to process variations.

SiGe is the preferred material for mass applications due to its significantly lower price (compared to GaAs). Additional benefits are its higher thermal conductivity, and the possibility of integrating digital circuits on the chip in the same process as the RF components. The downsides of SiGe devices are their low breakdown voltage, which is typically only some volts, and the fact that silicon is a relatively bad insulator, which limits the quality factors attainable with on-chip inductors and transformers, although quality factors higher than 10 can be reached with thick metal and high-resistivity substrates [14].

The present work is a feasibility study, aimed at the EDGE mobile station specification in the 1.8 GHz band. Chapter 2 starts with a discussion of classic power amplifier concepts (classes A through C) and goes on to describe the concepts of harmonic control amplifiers (classes D through F), along with the push-pull technique and discusses the linearity of amplifiers. Chapter 3 is dedicated to the design of on-chip transformers, while chapter 4 is a short overview of SiGe heterojunction bipolar transistors. In chapter 5, the EDGE

norm, which prescribes the amplifier characteristics, is presented and the amplifier schematic design and layout are described. A description of the measurements on the power amplifier and the results is given in chapter 6, chapter 7 finally sums up the results and offers an outlook and some suggestions for further research.

Chapter 2

High-Efficiency Amplifiers

The most important characteristics of a radio-frequency power amplifier are the output power P_{out} it can deliver to its load impedance and, especially for power amplifiers in battery-powered devices, the consumed (DC) supply power P_{DC} and the power-added efficiency

$$\text{PAE} = \frac{P_{\text{out}} - P_{\text{in}}}{P_{\text{DC}}} \tag{2.1}$$

with the input power P_{in}. For $P_{\text{in}} \ll P_{\text{out}}$ (i. e., high amplifier gain), PAE and efficiency

$$\eta = \frac{P_{\text{out}}}{P_{\text{DC}} + P_{\text{in}}} \tag{2.2}$$

are equal to the collector efficiency

$$\eta_{\text{C}} = \frac{P_{\text{out}}}{P_{\text{DC}}} \ . \tag{2.3}$$

Input power P_{in} and gain G are generally regarded as of only minor importantance, since the designer is always free to add a another amplifier stage at the input, while the output power and efficiency of a multi-stage amplifier are largely determined by the last stage.

2.1 Classical RF Amplifiers

Power amplifiers are classified according to their mode of operation into classes A, AB, B, and C. These classes are distinguished by the conduction angle Θ. The conduction angle is defined as half the angle per (RF signal) period during which the transistor is conducting (the collector current I_{C} in Fig. 2.1 is non-zero). Figure 2.2 shows the conduction angle Θ

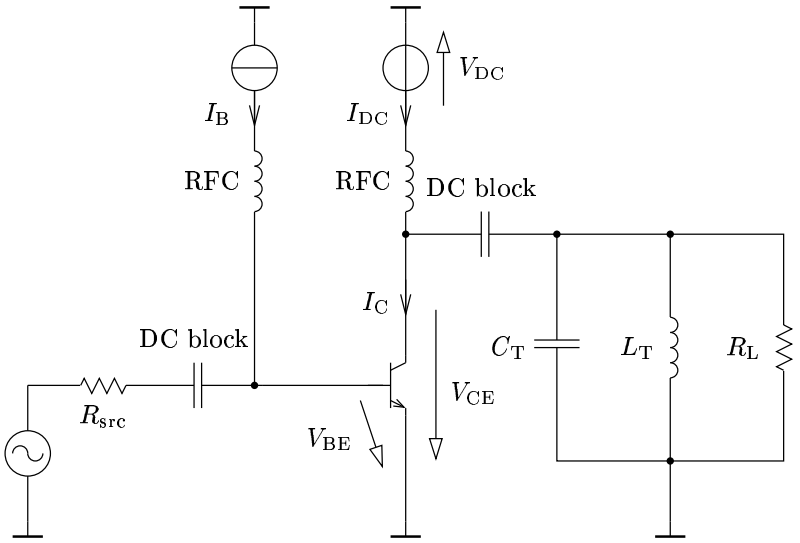


Figure 2.1: Simple amplifier circuit

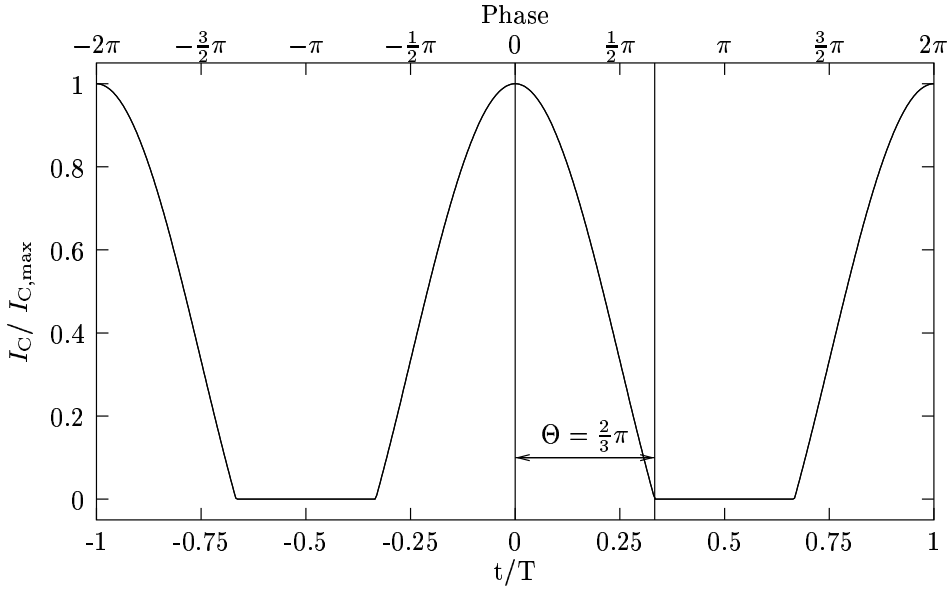


Figure 2.2: Conduction angle Θ for a clipped sinusoidal collector current. T is the cycle duration

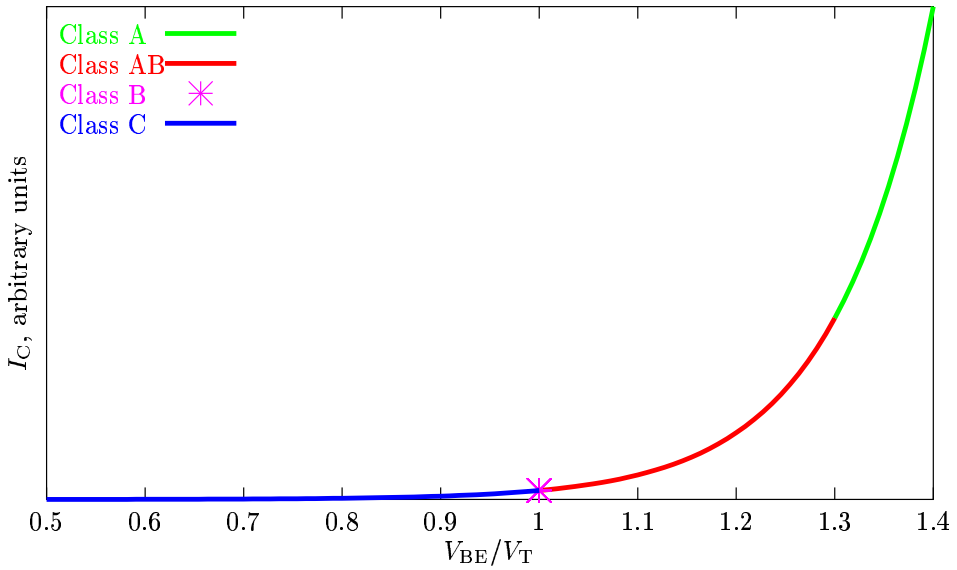


Figure 2.3: Operating points for classes A, AB, B, and C

Class	Conduction angle Θ
A	$\Theta = \pi$
AB	$\frac{\pi}{2} < \Theta < \pi$
B	$\Theta = \frac{\pi}{2}$
C	$\Theta < \frac{\pi}{2}$

Table 2.1: Conduction angles of class A, AB, B, and C amplifiers

for a clipped sinusoidal collector current. Figure 2.3 shows the DC operating regions and Table 2.1 gives the conduction angles for class A through C. Class B amplifiers are biased to the threshold voltage V_T of the V_{BE}/I_C characteristic, class C amplifiers are biased below the threshold voltage, while A and AB are biased above the threshold voltage. The difference between classes A and AB is that in class A operation the DC bias current is high enough to sustain collector current throughout the whole RF signal period. The "Class A" curve in Fig. 2.4 shows the collector current at maximum RF current amplitude.

Class A amplifiers operate in the linear region of the DC I_C/V_{CE} characteristic. They feature a high quiescent current (and thus generally low efficiency), due to the requirement that a positive overall collector current must be present even when its RF component is at its negative peak value.

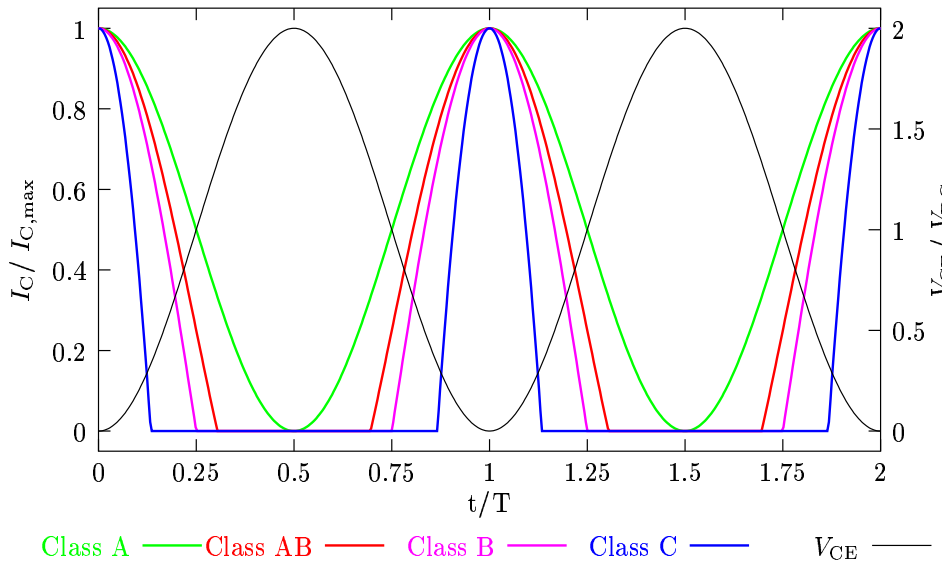


Figure 2.4: I_C and V_{CE} for a class A, B, AB, and C amplifiers

Class AB amplifiers have a lower (but still non-zero) quiescent current. No quiescent current is present in Class B and C amplifiers, which tend to have high efficiency. The properties of these amplifiers will be examined in the following sections.

2.1.1 Class A

Class A amplfiers combine excellent linearity with low efficiency. A typical loadline for a class A amplifier in the DC I_C/V_{CE} plane of an idealized transistor (a transistor with zero collector-emitter saturation voltage $V_{CE\ sat}$) is shown in Fig. 2.5. If the amplifier shown in Fig. 2.1 is biased to a class A operating point, the DC supply voltage V_{DC} must be larger than the peak value of the output voltage. The tank circuit L_T, C_T is assumed to be ideal and to be tuned to the fundamental frequency and presents a short to all harmonics. Thus, the output voltage is forced to be sinusoidal with the fundamental frequency and no power is dissipated in the load resistor at any harmonic frequency. The maximum output power is reached when the output current alternates between zero and the maximum collector current of the transistor $I_{C,max}$, i. e., the amplitude of the RF current is $\frac{1}{2}I_{C,max} = I_{DC}$. The output power for a harmonic constant-envelope signal is then (see Fig. 2.4)

$$P_{out} = \frac{1}{2} V_{DC} \frac{I_{C,max}}{2} \ , \tag{2.4}$$

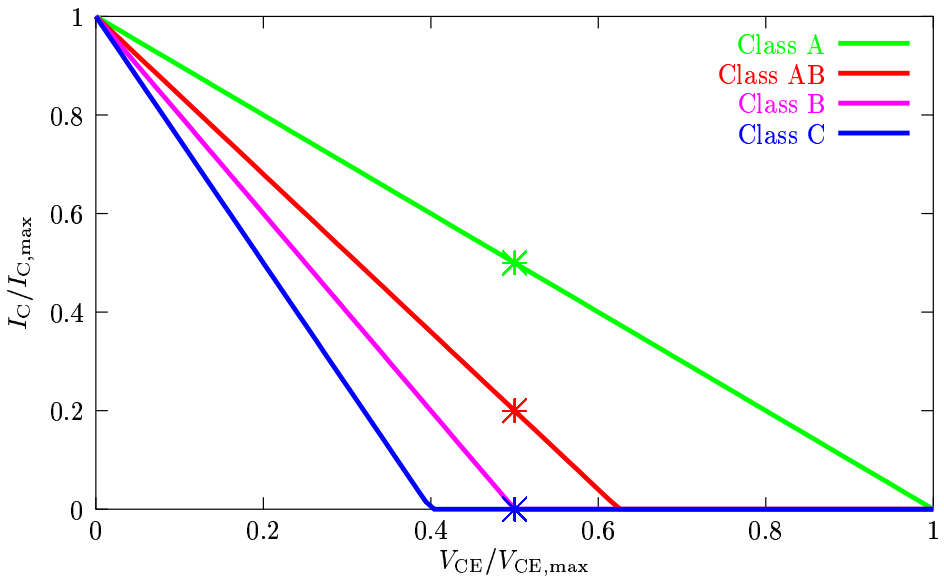


Figure 2.5: Operating points and loadlines for classes A, AB, B, and C

while the battery power consumed is

$$P_{DC} = V_{DC}\frac{I_{C,max}}{2} , \tag{2.5}$$

which is independent of the RF signal. The collector efficiency (2.3) is thus limited to

$$\eta_C \leq \frac{1}{2} , \tag{2.6}$$

even under ideal conditions. Efficiency is much worse if signals with large crest factors are to be amplified, since the bias conditions and the consumed DC power are determined by the peak value of the signal. The crest factor is the ratio of peak voltage $\hat{V}$ to the RMS value of the voltage V,

$$C = \frac{\hat{V}}{\sqrt{\lim_{T\to\infty}\frac{1}{2T}\int_{-T}^{T} V^2(t)\,\mathrm{d}t}} . \tag{2.7}$$

2.1.2 Class B

Class B amplifiers are biased at the threshold of the I_B/V_{BE} characteristic. No quiescent current in present, and the collector current waveform is exactly a half-wave rectified sinusoidal, as shown in Fig. 2.4. The following calculation

of the upper bound for the emitter efficiency is again based on the schematic in Fig. 2.1. The DC power provided by the source is

$$P_{\mathrm{DC}} = V_{\mathrm{DC}} I_{\mathrm{DC}} \ . \tag{2.8}$$

The DC current delivered by the collector bias source must necessarily be equal to the the mean value of the collector current $I_{\mathrm{C}}(\phi)$:

$$I_{\mathrm{DC}} = \frac{1}{2\pi} \int_0^{2\pi} I_{\mathrm{C}}(\phi)\, \mathrm{d}\phi = \frac{I_{\mathrm{C,max}}}{\pi} \int_0^{\pi/2} \cos\phi\, \mathrm{d}\phi = \frac{I_{\mathrm{C,max}}}{\pi} \tag{2.9}$$

where $\phi = 2\pi \frac{t}{T}$ is the phase. The RF power delivered to the load resistor is

$$P_{\mathrm{out}} = \frac{1}{2} V_{\mathrm{DC}} I_{\mathrm{C1}} \ , \tag{2.10}$$

where I_{C1} is the amplitude of the fundamental component of the collector current which can be calculated to be

$$I_{\mathrm{C1}} = \frac{1}{\pi} \int_0^{2\pi} I_{\mathrm{C}}(\phi) \cos\phi\, \mathrm{d}\phi = \frac{2 I_{\mathrm{C,max}}}{\pi} \int_0^{\pi/2} \cos^2\phi\, \mathrm{d}\phi = \frac{I_{\mathrm{C,max}}}{2} \ . \tag{2.11}$$

The efficiency of the class B amplifier for a harmonic constant-envelope signals is thus bounded by

$$\eta_{\mathrm{C}} \leq \frac{\pi}{4} \approx 0.785 \ . \tag{2.12}$$

2.1.3 Class AB

Class AB amplifiers are the "middle ground" between classes A and B, both in linearity and efficiency. The attainable collector efficiency of class AB amplifiers depends on the operating point. It varies from 50 % (near class A) to 78.5 % (near class B). Class AB amplifiers are often used in complementary or push-pull configuration. If biased near the class B operating point in complementary configuration, the efficiency approaches the value for class B, while crossover distortions are relatively small.

2.1.4 Class C

If the conduction angle is decreased beyond the class B operating point to a class C condition, the collector efficiency is increased further and can, for vanishing conduction angle Θ, approach 100 percent. Class C amplifiers with small conduction angles, however, have two great disadvantages. They are highly nonlinear and thus only useful for narrowband applications. Second,

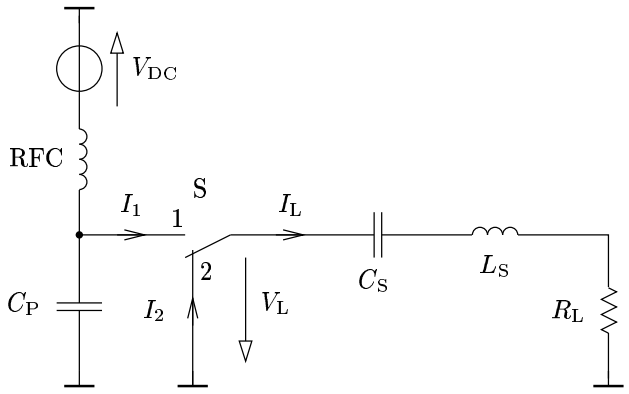


Figure 2.6: Schematic of a switching class D amplifier

the output power for a given device size (which entails a fixed $I_{C,max}$) diminishes rapidly for decreasing conduction angles, since the transistor is driving current for ever shorter periods of time [20], as can be seen by comparing the class B and C current waveforms in Fig. 2.4.

2.2 Harmonic Control Amplifiers

While class C amplifiers can in theory reach 100 % efficiency when operated at very low conduction angles, this not feasible in practice due to

- large device size compared to the attainable output power
- bad linearity
- losses due to imperfect device characteristics (non-zero collector-emitter saturation voltage)

To build high-efficiency RF amplifiers in real life, the designer has to resort to switching-mode amplifiers of the classes D, E, and F, which all have 100 % efficiency in theory. There are also amplifiers with harmonic control output networks in which the transistor is acting as a controlled current source, not as a switch.

2.2.1 Switching Class D

The schematic of a switching Class D amplifier is shown in Fig. 2.6. The switch S is operated at the fundamental RF frequency, with 50 % duty cycle.

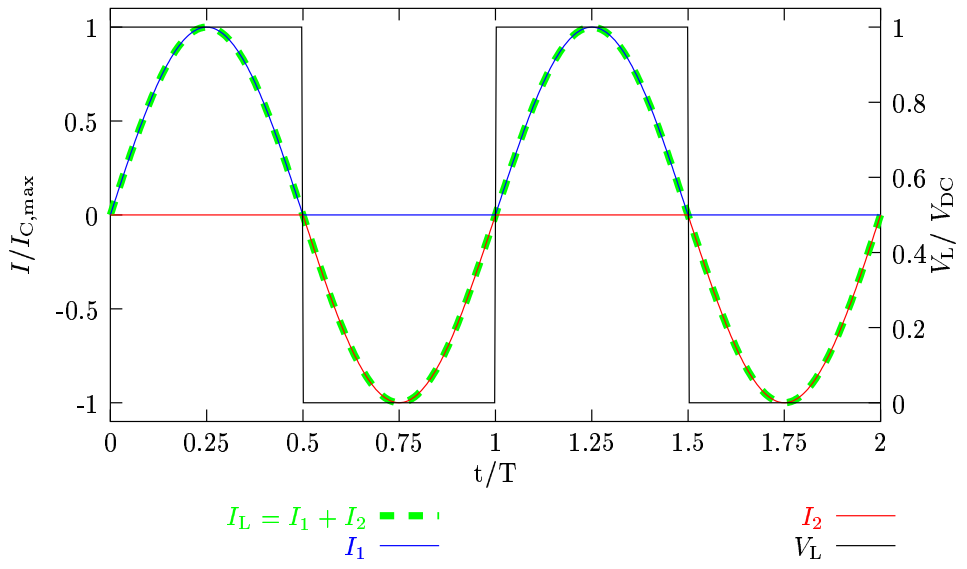


Figure 2.7: Switching class D waveforms

If the series resonant circuit L_S, C_S is ideal and tuned to the fundamental frequency (it has zero conductance for all other frequencies), the load current I_L must be sinusoidal with the fundamental frequency, and power can only be dissipated in the load resistor R_L at the fundamental frequecy Furthermore, the load current I_L cannot have a DC offset due to the series capacitor C_S. The sinusoidal load current must be in phase with the fundamental component of the voltage V_L, which is switched between V_{DC} and zero. The voltage and current waveforms are shown in Fig. 2.7. The main shortcoming of class D is the difficulty to build a switch that can be switched to position "1" in Fig. 2.6, which essentially requires two transistors which must be driven with inverted signals, as sketched in Fig. 2.8.

2.2.2 Class D

There is also an amplifier in which the transistor is operated in its linear region which is also termed "class D" [7]. This "RF class D" amplifier is a class AB or B amplifier where all odd harmonics are terminated with an open-circuit, while all even harmonics are shorted (with a shorted $\frac{\lambda}{4}$ microstrip stub, for example). The schematic of such an amplifier is shown in Fig. 2.9. Due to this particular load resistance, the collector current can only contain even-order harmonics, which coincides with the clipped sinusoidal waveform of the collector current expected from a class AB or B amplifier. The collec-

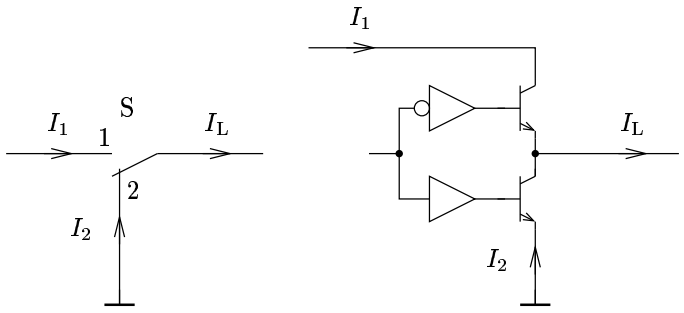


Figure 2.8: Realization of the switch in a switching class D amplifier

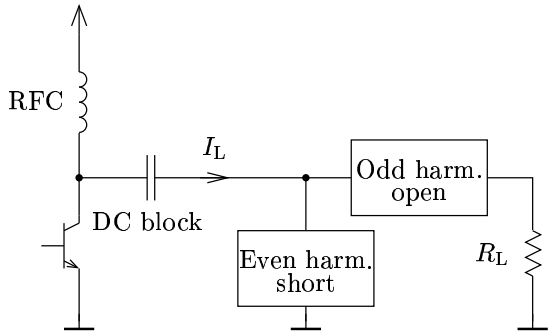


Figure 2.9: Schematic of a class D amplifier

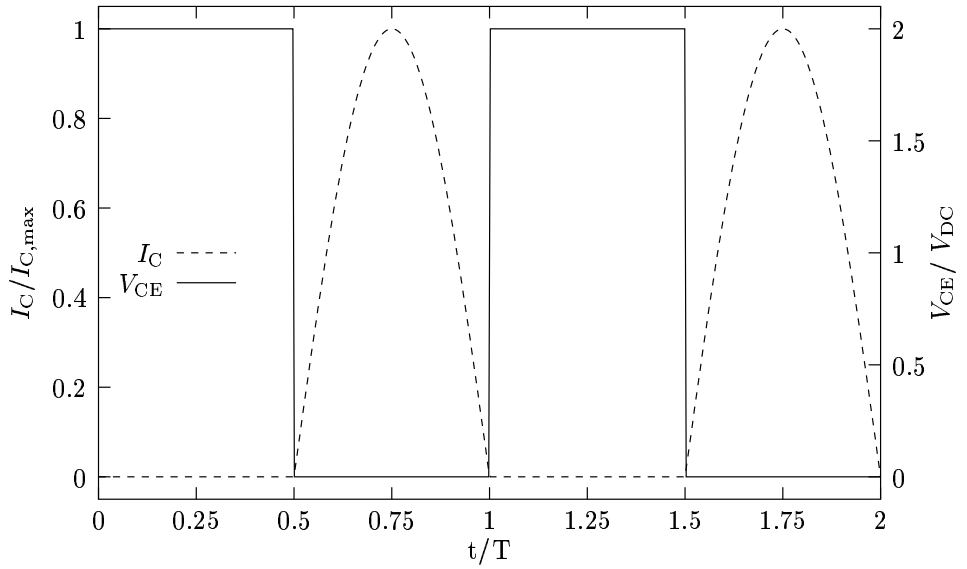


Figure 2.10: Class D waveforms

tor voltage, on the other hand, can only contain odd-order harmonics, The collector voltage is a square wave, the output current is a halfwave rectified sinewave as shown in Fig. 2.10. The voltage swing is $2V_{\mathrm{DC}}$ (as opposed to V_{DC} for the switching class D amplifier), and peak-to-peak RF current is the peak current of the switch (as opposed to twice the peak current of the switch for the switching class D amplifier)

2.2.3 Class E

Class E is another example of a switching amplifier, with the advantage over class D that the switch S in the schematic of a class E amplifier (Fig. 2.11) can be realized with a single bipolar or field-effect transistor and no couple of inverted drive signals is needed. Again, the resonant circuit C_{S}, L_{S} is assumed to be ideal and tuned to the fundamental frequency. Thus, the load current I_{L} must be sinusoidal. If we apply Kirchhoff's Current Law in Fig. 2.11, we get

$$I_{\mathrm{DC}} - I_{\mathrm{L}} = I_{\mathrm{S}} + I_{\mathrm{P}} \ . \tag{2.13}$$

Since the left side of (2.13) is a current sinewave with amplitude I_{L} and DC offset I_{DC}, this must hold for the right side as well. Furthermore, if the amplifier is in a steady state, the capacitor current I_{P} cannot have a DC component, which leads to the current waveforms shown in Fig. 2.12. The voltage across the switch is easily obtained by integration of the collector

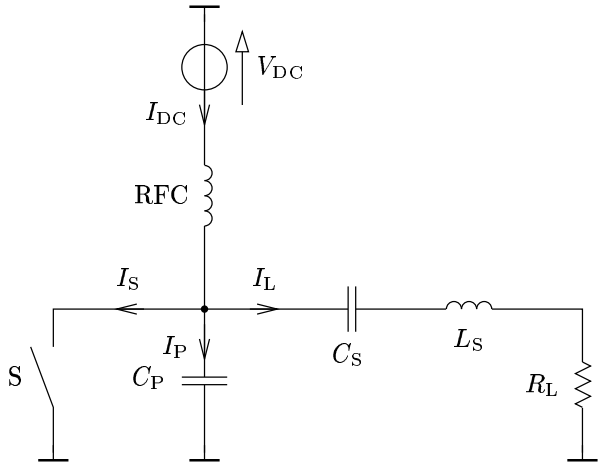


Figure 2.11: Schematic of a class E amplifier

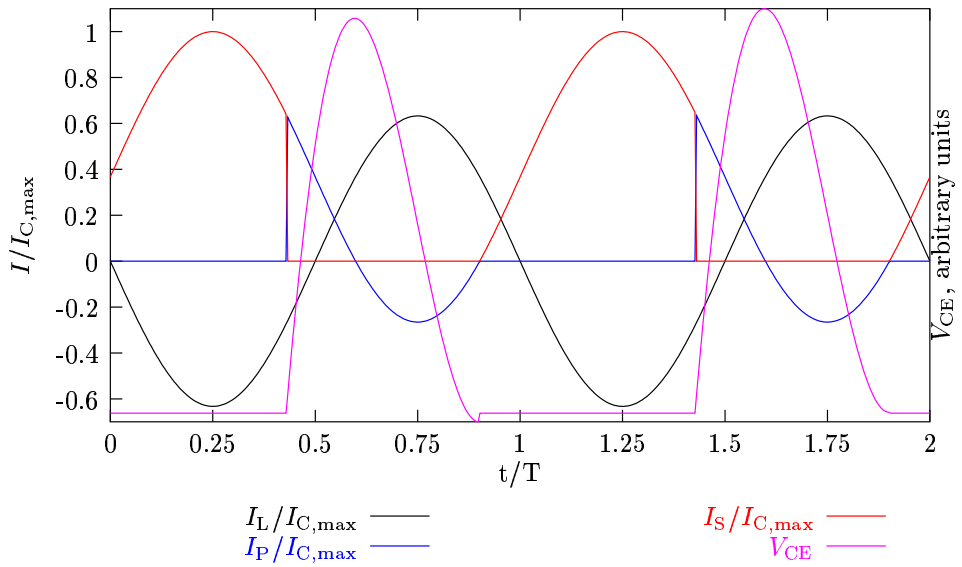


Figure 2.12: Class E waveforms

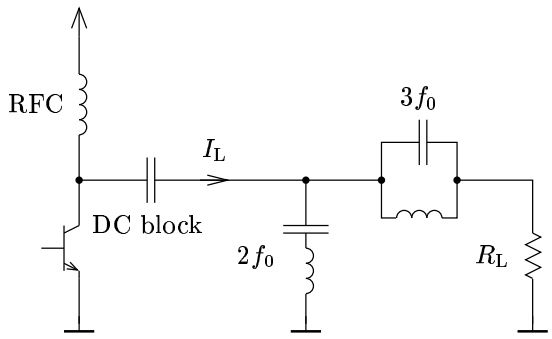


Figure 2.13: Schematic of a class F amplifier

current during the time the switch S is open. The high peak voltage across the switch is a problem if the switch is a transistor which should be exposed to limited collector-emitter voltages only. The peak voltage increases if the class E amplifier is driven to high power utilization factors [7]. The power utilization factor is the ratio of the output power of a certain amplifier to the output power that could be obtained from a class A amplifier using the same transistor. Class E is nonlinear: variations in input power will not be reproduced at the output in any acceptable form.

2.2.4 Class F

Similar to the class D RF amplifier presented in section 2.2.2, there exist class F ampifiers with a multiple-resonator output network. The schematic of one example is presented in Fig. 2.13. The series resonant circuit is tuned to $2f_0$ and presents a short to the collector at this frequency, while the parallel LC combination is tuned to $3f_0$ and presents an open to the collector at the third harmonic. The collector current contains a second harmonic component which, if suitably dimensioned, makes the collector current similar to a half-wave rectified sinewave. A perfect half-wave rectified sinewave could be obtained if all even-order harmonics were shorted. The third harmonic component of the collector-emitter voltage serves to lower the peak voltage. The peak of the fundamental component can be higher than the actual peak voltage. The benefit is increased output power when the peak voltage is limited. A maximally flat collector voltage is obtained if the ratio of the amplitude of the third harmonic V_3 to the amplitude of the fundamental component V_1 is

$$V_3 = \frac{1}{9} V_1 \ , \tag{2.14}$$

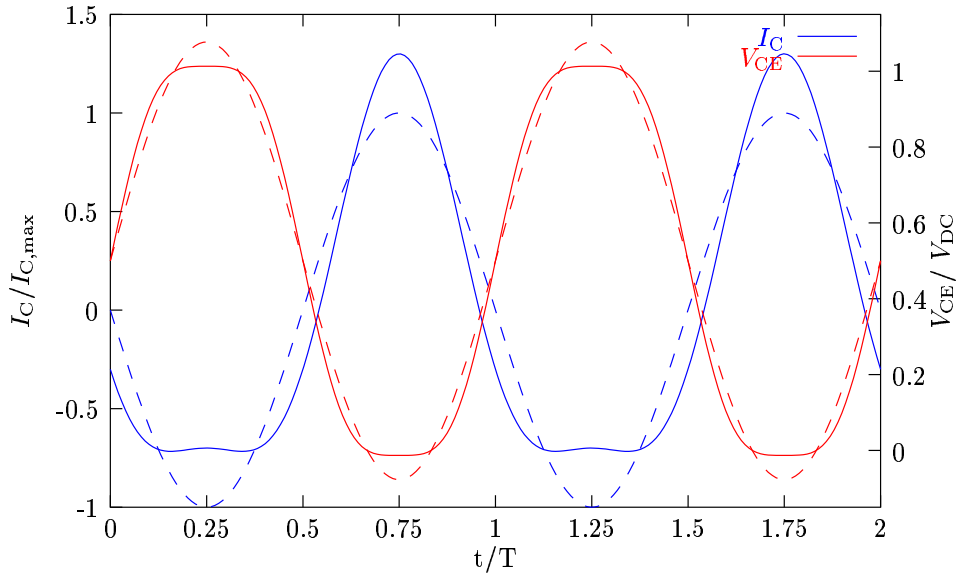


Figure 2.14: Class F waveforms. Dashed lines are the respective fundamental components.

which is the case in Fig. 2.14. The minimum peak value of the output voltage (relative to the amplitude of the fundamental component V_1) is obtained for

$$V_3 = \frac{1}{6} V_1 \ . \tag{2.15}$$

2.3 Push-pull Amplifiers

The combination of two power transistors shown in Fig. 2.15 is a push-pull amplifier. The transistors Q1 and Q2 are driven differentially, and are both biased to a class B operating point. Each transistor contributes a half-wave to the (sinusoidal) load current I_L. As stated before, the half-wave rectified sinusoidal collector current of each of the transistors can be composed of the DC current $\frac{1}{2} I_{DC}$ and suitable even-order harmonics, which are shorted by the $\lambda/4$ stubs. Both collector currents are summed up in the output balun to form the sinusoidal load current I_L.

The push-pull techniqe offers some key advantages over single-ended designs.

- If the output power of a single-ended amplifier is given, and the voltage amplitude is limited (as is the case for SiGe HBTs), the only way to achieve the desired power is to increase the RF load current. High RF

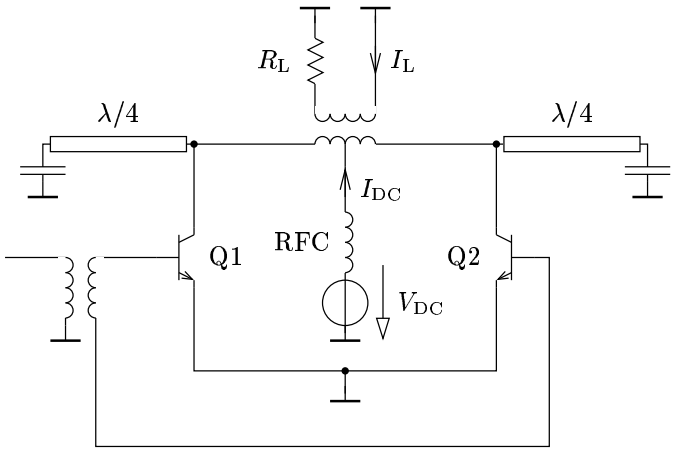


Figure 2.15: Schematic of a push-pull amplifier

load currents mean small load impedances, which makes the design of matching networks complicated and fabrication expensive. The most significant benefit of the push-pull technique for RF power amplifiers is that the peak-to-peak voltage swing at the load can be double the peak collector voltage at one device of the push-pull pair. If one transistor in single-ended configuration is replaced by two transistors, each of them half the size of the single-ended transistor and thus capable of half the output RF current, the overall device size stays the same, as does the RF output power. The load impedance, however, is quadrupled, since the load current is halved and the load voltage swing is doubled. This fourfold increase of the load impedance *while maintaining constant output power and overall transistor size* makes designing the matching networks much easier, since optimum loads of RF power transistors tend to be in the range of a few ohms and load resistances smaller than 1 Ω are quite hard to realize.

- A consequence of class B operation is that DC consumption will rise and fall with varying RF power levels [7], which makes efficient amplification of signals with large envelope variations possible.

- Another benefit is the cancellation of common lead effects [7]. The voltage along the connection from emitter to ground (possibly a bondwire) diminishes the available collector-emitter voltage, which reduces the attainable output power. In the push-pull circuit shown in Fig. 2.16, the emitters are connected on-chip (with low parasitic inductances), and the RF output current I_L does not traverse the bondwire, and no

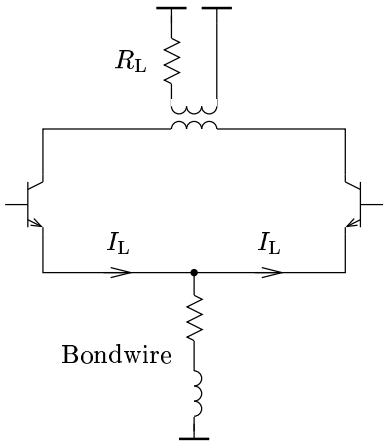


Figure 2.16: Cancellation of common-lead effects in a push-pull amplifier

voltage (at least at the fundamental frequency) is developed across the bondwire connecting both emiters to ground. This beneficial effect is diluted at high frequencies, when the RF power transistors start to behave as distributed devices.

- For an ideally symmetric amplifier, the output does not contain even-order harmonics [3].

2.4 Linearity

Linearity is the ability of an amplifier to sustain a constant input to output voltage (or, equivalently, current) ratio over its entire operating range. The transfer characteristic of an RF amplifier usually shows some sort of clipping of the output voltage at high drive levels, which leads to decreased gain as well as signal distortions at high output power levels. Ususally, the maximum power (or minimum transistor size) for which some linearity figure of merit limit can be attained is sought. Some figures of merit are discussed below in this chapter.

Generally, the transfer function $V_{\text{out}}(V_{\text{in}})$ of the amplifier can be expressed as a Taylor series

$$V_{\text{out}} = k_1 V_{\text{in}} + k_2 V_{\text{in}}^2 + k_3 V_{\text{in}}^3 + k_4 V_{\text{in}}^4 + \cdots \ . \tag{2.16}$$

For the following deliberations, the third-order approximation

$$V_{\text{out}} = k_1 V_{\text{in}} + k_3 V_{\text{in}}^3 \ , k_1 > 0 \ , \ k_3 < 0 \tag{2.17}$$

is used to simulate some sort of symmetric "voltage clipping" at high input amplitudes. This simple approximation, however, is valid only for realitively small distortions. The second-order term $k_2 V_{\text{in}}^2$ has been omitted in (2.17), since the second-order intermodulation products are located near DC and near the double signal frequency and thus (usually) far outside the used frequency band. For a perfect harmonic input voltage

$$V_{\text{in}} = \hat{V}_{\text{in}} \cos(\omega t) \tag{2.18}$$

the output voltage is

$$\begin{aligned} V_{\text{out}} &= k_1 \hat{V}_{\text{in}} \cos(\omega t) + k_3 \left[\hat{V}_{\text{in}} \cos(\omega t)\right]^3 \\ &= \left[k_1 \hat{V}_{\text{in}} + \frac{3}{4} k_3 \hat{V}_{\text{in}}^3\right] \cos(\omega t) + \frac{1}{4} k_3 \hat{V}_{\text{in}}^3 \cos(3\omega t) \ . \end{aligned} \tag{2.19}$$

If we compare (2.19) with the output voltage of a perfectly linear amplifier

$$V_{\text{out}} = k_1 \hat{V}_{\text{in}} \cos(\omega t) \ , \tag{2.20}$$

two differences are evident: The amplitude of the fundamental component at ωt is smaller than that obtained from a perfectly linear amplifier. There is an additional third harmonic component in the output voltage, which grows not linearly with $\hat{V}_{\text{in}}$, but with its third power.

These two significant consequences of a nonlinear transfer characteristic can be observed even for more sophisticated approximations.

- Amplifier gain generally diminishes with increasing input amplitude and power. This "gain compression" (the difference between the small-signal gain and the gain observed at some higher input drive) increases with the input amplitude.

- For a harmonic input signal, additional signal components at multiples of the input frequency are introduced.

Real-world signals, of course, rarely consist of a single perfect sinewave. To mimic real-world signals which occupy some finite amount of bandwidth, we consider an input signal composed of two sinewaves (a so-called two-tone signal)

$$V_{\text{in}} = V_1 \cos(\omega_1 t) + V_2 \cos(\omega_2 t) \ , \tag{2.21}$$

where the relative difference of ω_1 and ω_2 is small:

$$\omega_2 - \omega_1 \ll \omega_1, \ \omega_2 \ . \tag{2.22}$$

Frequency	Amplitude
$2\omega_1 - \omega_2$	$k_3\left(\frac{3}{4}V_1^2V_2\right)$
ω_1	$k_1V_1 + k_3\left(\frac{3}{4}V_1^3 + \frac{3}{2}V_1V_2^2\right)$
ω_2	$k_2V_2 + k_3\left(\frac{3}{4}V_2^3 + \frac{3}{2}V_1^2V_2\right)$
$2\omega_2 - \omega_1$	$k_3\left(\frac{3}{4}V_1V_2^2\right)$
$3\omega_1$	$k_3\left(\frac{1}{4}V_1^3\right)$
$2\omega_1 + \omega_2$	$k_3\left(\frac{3}{4}V_1^2V_2\right)$
$2\omega_2 + \omega_1$	$k_3\left(\frac{3}{4}V_1V_2^2\right)$
$3\omega_2$	$k_3\left(\frac{1}{4}V_2^3\right)$

Table 2.2: Amplitudes of third-order intermodulation products

The output voltage of our amplifier, again using the third-order characteristic (2.17), is

$$V_{\text{out}} = k_1\left[V_1\cos\left(\omega_1 t\right) + V_2\cos\left(\omega_2 t\right)\right] + k_3\left[V_1\cos\left(\omega_1 t\right) + V_2\cos\left(\omega_2 t\right)\right]^3 \ . \tag{2.23}$$

After applying some trigonometric relations to (2.23) to obtain a weighted sum of $\cos\left(n\omega_1 t + m\omega_2 t\right)$, we get the amplitudes given in Tab. 2.2 at the respective frequencies $n\omega_1 t + m\omega_2 t$. The third-order intermodulation products (as, in fact, all odd-order intermodulation products) generate some signal power not only at the signal frequencies, but also at nearby frequencies. If we take ω_1 and ω_2 as the corner frequencies of one channel in a multi-carrier system, these intermodulation products distort signals in adjacent channels.

Based on the concepts and findings presented above, we can now present a number of figures of merit which are commonly used to judge the linearity, or the linear operating range, of an RF amplifier:

- 1 dB compression point: the output (or input) power where the gain compression reaches 1 dB. In Fig. 2.17, the 1 dB compression point is at 37.8 dBm output power (or 18.8 dBm input power)

- Third-order intercept point IP3: The curves of the output power at the fundamental frequency for a single-tone input signal and the third-order intermodulation products (IM3 in Fig. 2.18) obtained under two-tone excitation can both be extrapolated logarithmically (or linearly, if the amplitudes are given in dB), as shown in Fig. 2.17. The intersection point of both curves is the third-order intercept point. In Fig. 2.17, it is located at 49 dB output power (or 29 dB input power).

- Intermodulation distance: The ratio of the signal powers at ω_1 (or ω_2)

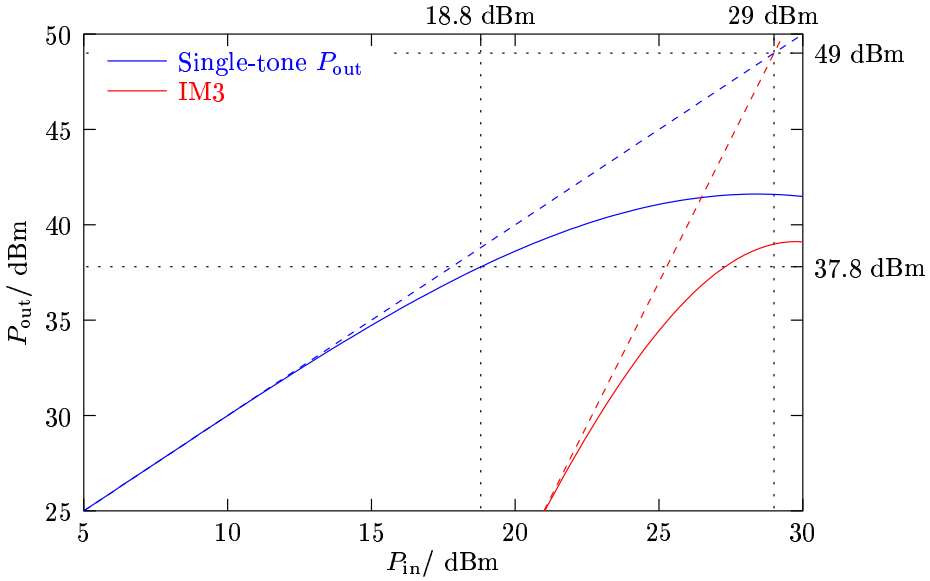


Figure 2.17: 1 dB compression point and third-order intercept point of a typical RF amplifier. Small-signal gain is 20 dB.

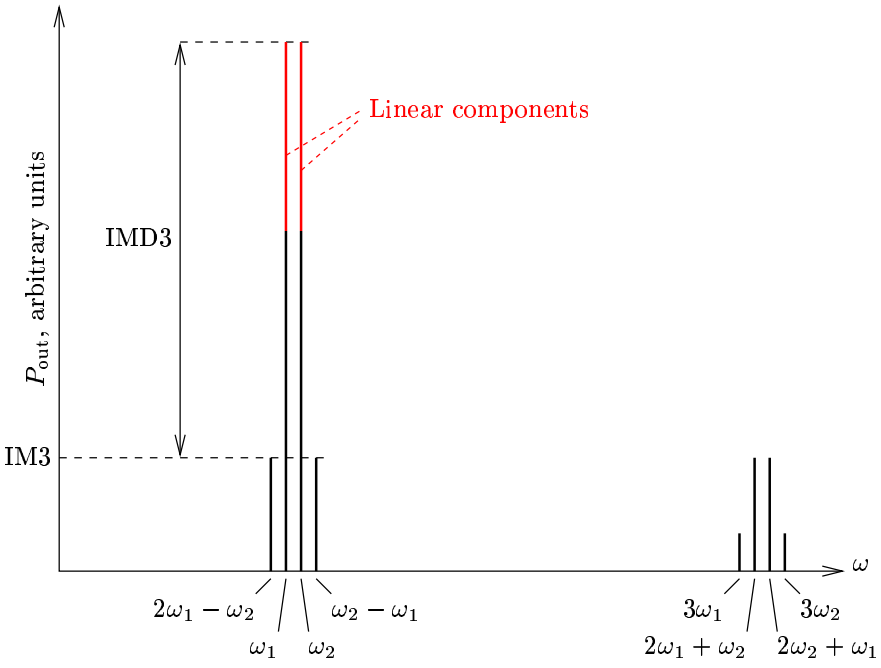


Figure 2.18: Spectrum of third-order intermodulation products

to the third-order intermodulation product at $(2\omega_2 - \omega_1)$ is called the (third-order) intermodulation distance IMD3 (see Fig. 2.18).

- Adjacent channel power ratio ACPR: This figure of merit is useful if the RF spectrum is divided into channels (as is the case in mobile telephony), each occupying some specified amount of bandwidth. The ratio of signal power in the channel occupied by the RF signal to that in one adjacent channel which is generated by amplifier nonlinearity is the adjacent channel power ratio.

Chapter 3

Integrated Inductors and Transformers

Integrating inductive components on a silicon chip along with active devices and other passives became feasible in the 1990s when higher frequencies (1 GHz and above) required typically smaller inductance values, while at the same time advances in semiconductor fabrication technology allowed for smaller metal width and pitch [12].

Silicon is a relatively bad insulator (typically 10 to 20 Ωcm for BiCMOS substrates, and 0.01 Ωcm for CMOS substrates), which leads to significant substrate losses.

Three major loss mechanisms can be distinguished:

- Electrical coupling to the substrate which causes displacement currents to flow to nearby grounds at the bottom of the chip or in substrate taps near the inductor.
- Eddy currents in the substrate, and electrically induced currents in the substrate which flow perpendicular to the spiral segments.
- Ohmic losses in the metallization, aggravated by the skin effect (current crowding) at high frequencies.

These factors limit the Q factors attainable on silicon to about 10, although Q factors as high as 12.3 have been reported [4] on high-resistivity substrate (150 to 200 Ωcm) with thick metallization (4.5 μm gold). Silicon RF inductive devices are generally limited by substrate losses while inductive devices on gallium arsenide (GaAs) are mostly limited by the finite metal conductivity, since the substrate resistivity of GaAs is significantly higher than that of silicon [13].

These problems nonwithstanding, integrated inductors and transformers are being increasingly used because they offer much smaller total circuit size and simplified assembly (at the price of increased chip size) when they replace off-chip (thin film or discrete) inductors. For RF applications, where very small inductances are needed, there is no possibility to realize some components off-chip, since the inductivity and resistance of the connections and bondwires alone would be prohibitively high.

To reduce the coupling to the substrate, a "ground shield" can be added (in a polysilicon or lower metal layer) between the inductor and the substrate. To avoid eddy currents, ground shields are always patterned in such a way that the conductive paths of the conductor and shield are perpendicular to each other. A typical example of a patterned ground shield is shown in Fig. 3.1. While such a shield can improve the Q factor below the self-resonant frequency, it always increases the capacitance to substrate and decreases the self-resonant frequency of the inductor. The larger substrate capacitance can furthermore lead to stronger coupling between inductors on the same die since all the substrate capacitances are not ideally grounded, but connected to ground by a common inductance which leads to "ground-bounce" [13]. Increasing the capacitance values C_{sub} in Fig. 3.2 actually increases the coupling between the circuits around L_1 and L_2 via R_{GND} and L_{GND}, which represent bondwires and lines connecting the substrate to the "true" ground, which is somewhere off the chip.

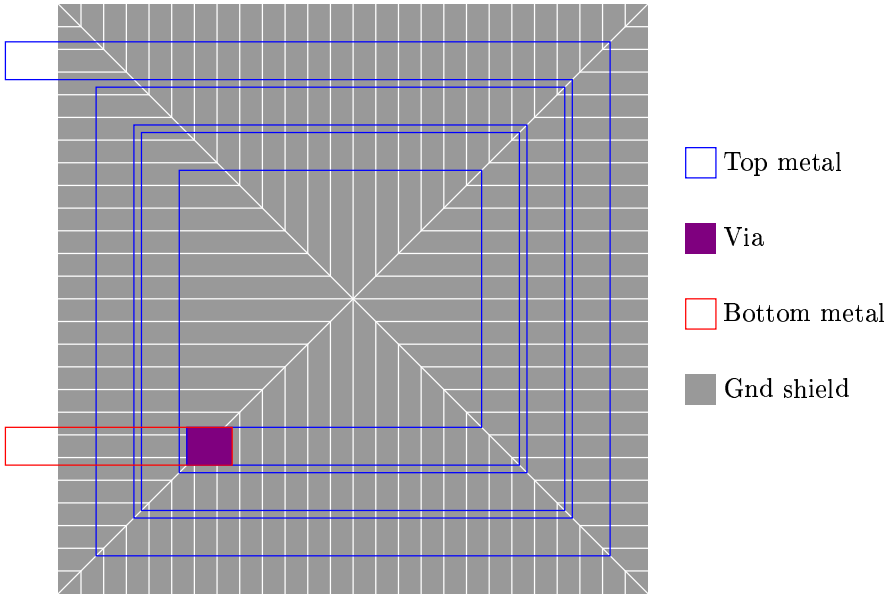


Figure 3.1: Layout of a typical spiral inductor with a patterned ground shield

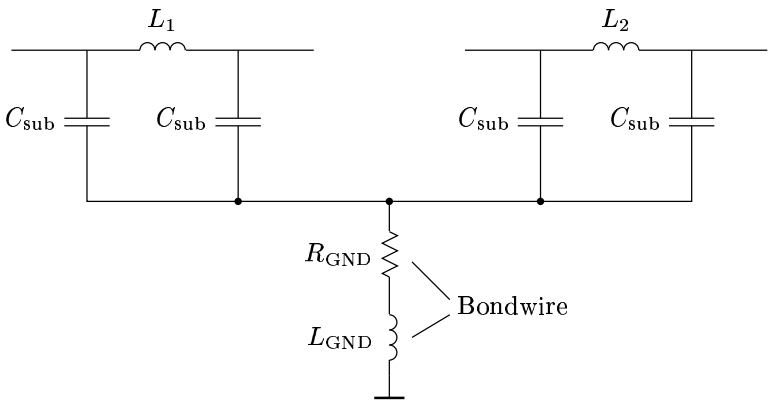


Figure 3.2: Ground bounce, coupling of two shielded inductors L_1 and L_2

Chapter 4

SiGe Transistors

SiGe transistors are an example of *bandgap engineering*, where a device is composed of materials with different band structures. The bases of SiGe transistors contain some fraction of germanium, typically about 10 to 20 percent, which narrows the bandgap ($E_\mathrm{C} - E_\mathrm{V}$) in the base region. The germanium can be distributed uniformly ("uniform base"), or the germanium content can vary along the base layer ("graded base"). The band diagrams of SiGe HBTs with uniform and graded bases are shown in Fig. 4.1. Figure 4.2 is a cross-section of a wafer containing a SiGe HBT.
The benefits of SiGe HBTs compared to plain silicon BJTs are:

- Increased emitter efficiency: In an *n-p-n* device, holes are blocked from entering the emitter by a high potential barrier in the valence band (see Fig. 4.1(a)), thus increasing the ratio of electron current to hole current in the emitter. This results in a higher emitter efficiency

$$\gamma = \frac{I_\mathrm{En}}{I_\mathrm{E}} \tag{4.1}$$

  where I_En is the injected electron current from the emitter (again for *n-p-n* devices), and I_E is the total emitter current (hole and electron current combined) [18]. The higher the share of electron current in the emitter current, the more electrons are injected into the base region and can drift to the collector, which results in better (higher) current gain.

- Lower base transit time: The graded germanium content in the base induces an additional drift field along the base, thus lowering base transit time which results in higher f_T [8].

- Lower base resistance: The base can be heavily doped (typically $6 \cdot 10^{18}$ [8]) without sacrificing significant amounts of emitter efficiency [18].

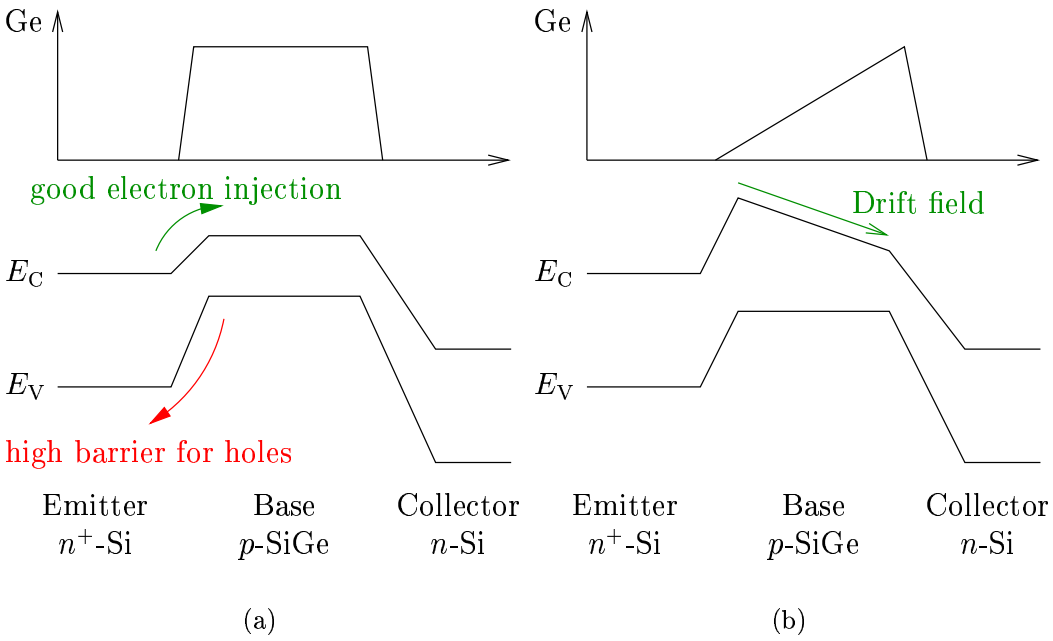


Figure 4.1: Band diagram of SiGe HBTs with uniform (a) and graded (b) base

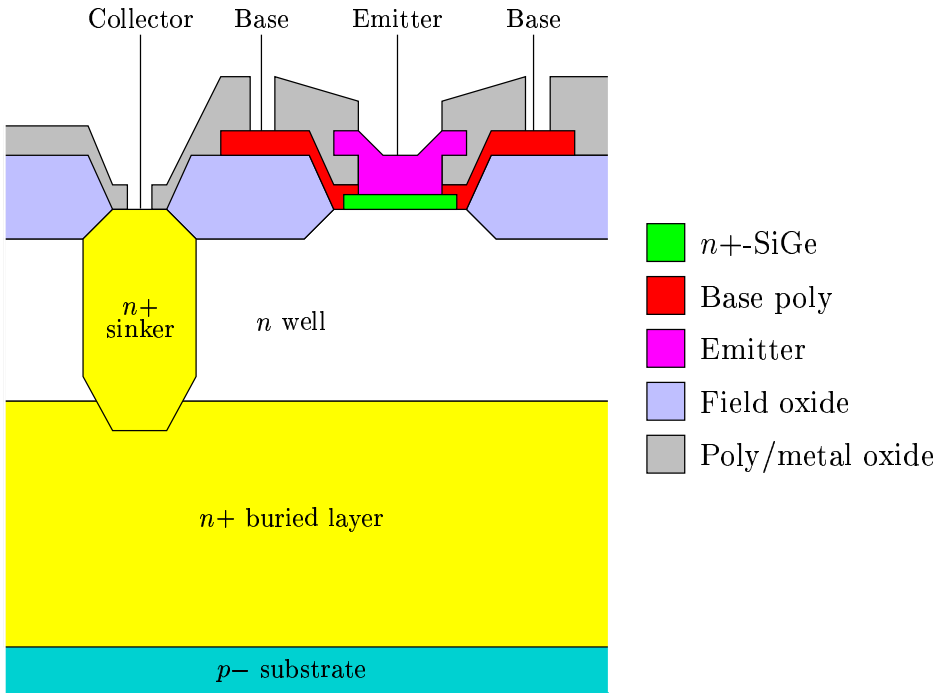


Figure 4.2: Wafer cross-section of a vertical n-p-n SiGe HBT with one collector finger, two base fingers and one emitter finger

The heavy base doping reduces resistance in the base region, and the decreased base resistance results in a higher $f_{\max}$ and low noise figure [8].

- Less emitter current crowding: In SiGe devices, less emitter current crowding occurs because of the lower voltage drop at the B-E junction [18].

The suitablility of SiGe transistors for high-freqency applications up to several GHz along with substantial cost benefits over GaAs will ensure their continued presence in RF amplifier construction.

Chapter 5

Amplifier Design

5.1 On the EDGE Signal

The digital cellular telephony standard GSM has been adopted world-wide since commercial service started in 1991 and has since then replaced many of the analog mobile phone systems previously used. Since GSM was intended to be a mostly-voice network, the channel coding was optimized for speech. Only circuit-switched data up to 9.6 kbit/s could be transmitted over the first GSM networks. Recent GSM additions improving its data transfer capabilities are

- High-speed circuit switched data (HSCSD) which increases the cannel bit rate to 14.4 kbit/s by introducing a new channel coding scheme and allows the user to use several GSM channels in parallel.
- General packet radio service (GPRS), which introduces packet-switched data to GSM.

Both HSCSD and GPRS use the same modulation format as "plain" GSM: Gaussian minimum-shift keying (GMSK) with 1 bit per symbol, and a channel bit rate of about 271 kbit per second. EDGE is intended as an intermediate step from phase 2 (GSM) to phase 3 (UMTS) mobile telephony systems (hence sometimes labelled "phase 2+") which introduces a new modulation scheme with triple the channel bit rate of "plain" GSM, while maintaining the same bandwidth requirements.

The EDGE signal is a $\frac{3\pi}{8}$-shifted 8-PSK signal. After each symbol, the signal constellation is rotated by $\frac{3\pi}{8}$. Three bits are transmitted per symbol, which results (with the same symbol rate of 271 kbaud as the GMSK modulation used in GSM) in a bit rate of 813 kbit per second.

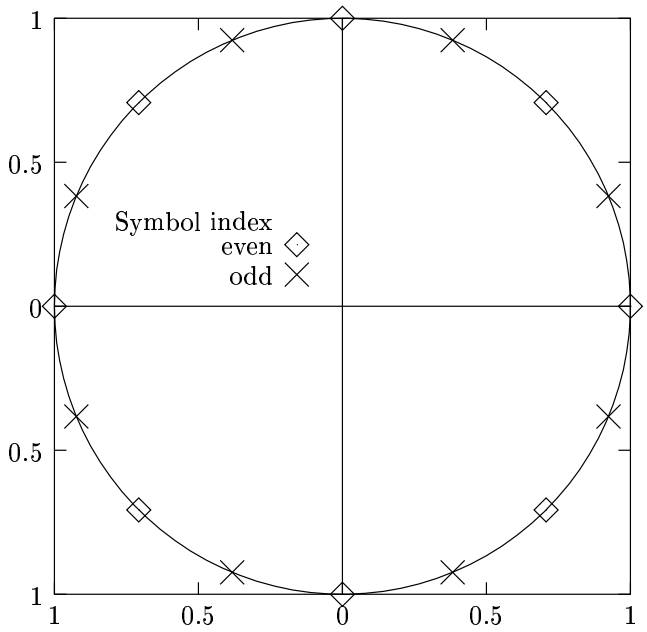


Figure 5.1: Signal constellation of the EDGE signal

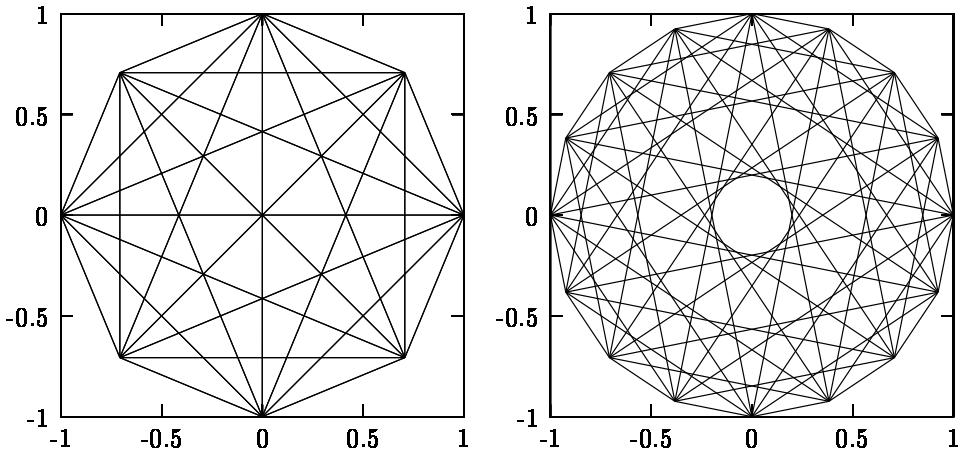
Figure 5.1 shows the two signal constellations for odd- and even-numbered symbols. Note that although the constellations of every other symbol comprise the same signal points, the constellation of the n-th symbol is actually the constellation of the $(n-2)$-th symbol rotated by $\frac{6\pi}{8}$.

The $\frac{3\pi}{8}$ rotation of the signal constellation between consecutive symbols prevents the envelope from reaching zero, as illustrated in Fig. 5.2, which shows the paths of the (unfiltered) complex baseband signal wandering through the complex plane. The envelope of the EDGE signal is nevertheless varying noticeably, with a crest factor (2.7) of 3.12 dB and an envelope dynamic range (the ratio of the maximum amplitude to the minimum amplitude of the signal envelope) of 17 dB [17]. The spectrum of an undistorted EDGE signal, along with the spectral mask allowed by the EDGE standard [10], is shown in Fig. 5.3.

The baseband pulse of an EDGE signal is defined in [10], an approximation is given in [17] as

$$p(t) \approx \exp\left(-1.045\left(\frac{t}{T}\right)^2 - 0.218\left(\frac{t}{T}\right)^4\right) \tag{5.1}$$

with the time t and the symbol period T. The maximum error of the approximation in (5.1) is about 0.25 % of the pulse peak value.



(a) 8-PSK constellation

(b) $\frac{3\pi}{8}$-shifted 8-PSK constellation

Figure 5.2: Comparison of 8-PSK (a) and its shifted variant (b). All possible transitions between consecutive signal points are plotted

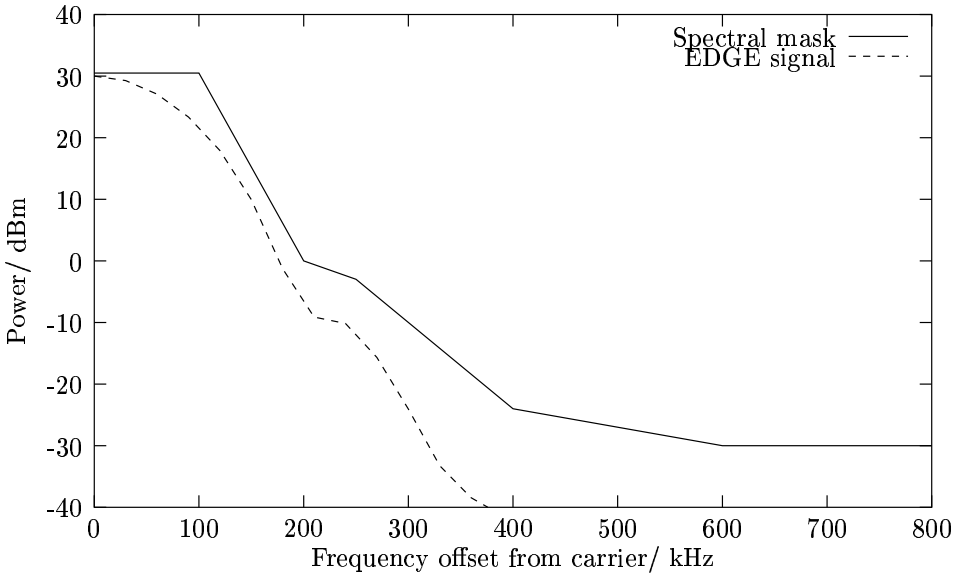


Figure 5.3: Spectrum of the EDGE signal

Output power	30 dBm (power class E1) 26 dBm (power class E2) 22 dBm (power class E3)
Frequency range	1.71 GHz – 1.785 GHz
Channel spacing	200 kHz

Table 5.1: EDGE mobile station transmitter specifications [10]

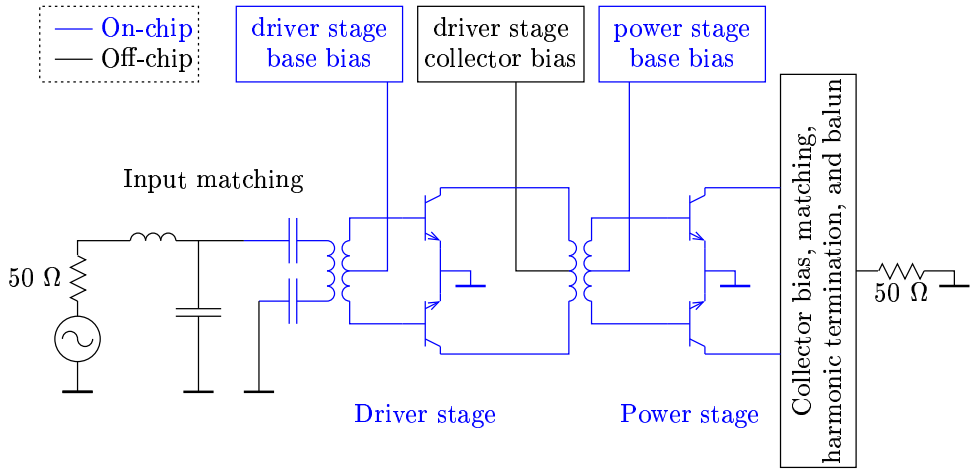


Figure 5.4: Schematic of the power amplifier

5.2 Amplifier Specifications

The RF characteristics of an 1800 MHz EDGE mobile station (MS), are specified in Tab. 5.1. The limits on the output RF spectrum are nearly the same as for GSM, but since the EDGE signal has (in contrast to the GSM signal) large envelope variations, the linearity requirements on the power amplifier are much tighter compared to the constant-envelope GSM signal.

5.3 Power Amplifier

The process used for fabrication of the amplifier was *austriamicrosystems*' 0.8 μm SiGe BiCMOS process. Its features include *n*-*p*-*n* HBT devices and FETs, as well as various capacitances and resistors. Two thin metal layers are available for interconnections and for constructing inductive components.

The largest devices available from *austriamicrosystems* are SiGe HBTs with an emitter area of 48 μm^2. 240 of these transistors were used as funda-

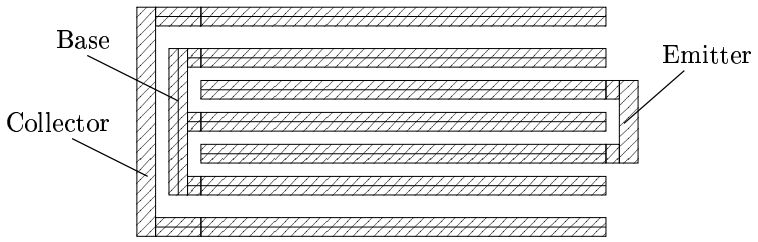


Figure 5.5: Layout of a unit transistor

mental cells and connected in parallel to yield a device capable of delivering an output power of above 30 dBm. Since the input and output impedance of such a large device are in the sub-ohm range, the power stage had to be a push-pull design (see section 2.3) with two devices of 120 building blocks each, which allowed for a load impedance of about 2 Ω. A push-pull driver stage was included on the chip to provide for an overall gain in excess of 20 dB. An 2:1 interstage balun was designed for DC isolation between driver and power stage and for matching the input impedance of the power stage (which is above 1 Ω) to the output impedance of the driver stage (in the 10 Ω range). To deliver enough power to drive the power transistors even through a lossy interstage balun, the driver transisitors are composed of 40 elementary cells. An 5:1 input balun was also needed to transform the 50 Ω source impedance at the input down to 2.5 Ω, which is a suitable source impedance for the driver stage. The only off-chip components in the design are an input match section (which was placed off-chip for tunability) and the output match and balun which had to be placed off-chip due to the limited current densities on-chip. The two amplifier stages, along with the input balun and the inter-stage matching network were integrated on a single chip. The base bias currents in both stages are fed through the center taps of the baluns by on-chip current mirrors connected to external current sources.

5.4 Transistor Design

An *n*-*p*-*n* SiGe HBT provided by *austriamicrosystems* was used as the basic building block for the power BJTs. This fundamental cell has two emitter fingers, each 30 μm long and 0.8 μm wide, and three base and two collector fingers with the same dimensions. Along with the layout, the VBIC model [11] used in the simulations was provided by *austriamicrosystems*. The layout of the metallization of one such unit transistor is presented in Fig. 5.5.

In order to verify the scaling of the transistor model, a device consisting

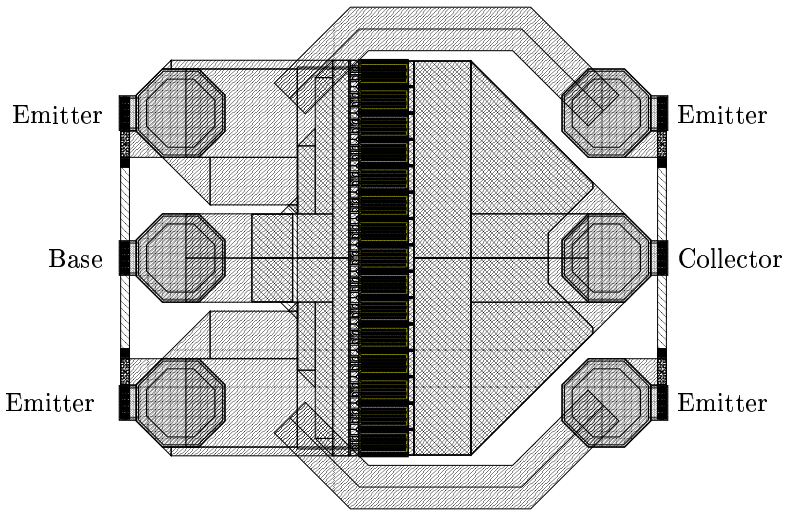


Figure 5.6: Layout of the scaling test with 15 unit cells

of fifteen unit transistors in parallel was fabricated and measured on-wafer. The Layout is shown in Fig. 5.6. The measured results (see Fig. 5.7) showed good agreement with simulation, bringing about some optimism regarding the function of the complete amplifier.

5.4.1 Driver Transistor

The transistors used in the driver stage were obtained by connecting 40 fundamental cells in parallel, resulting in a total emitter area of 1920 μm^2 per device. Figure 5.8 shows a layout detail; the collector is contacted at the bottom edge on both metal layers, base and emitter are contacted at the top edge on the bottom and top metal layer, respectively.

5.4.2 Power Transistor

The power transistors were constructed by connecting 120 fundamental cells in parallel, which gives a total emitter area of 5760 μm^2 per device. To achieve maximum power capability with a small-size device and to maintain constant bias conditions across all fundamental cells, the collector and emitter fingers are linearly tapered off, reflecting the decreasing current along the length of the finger. The layout of one such power device is sketched in Fig. 5.9. A detail of the layout of the actual device showing four fundamental cells is shown in Fig. 5.10.

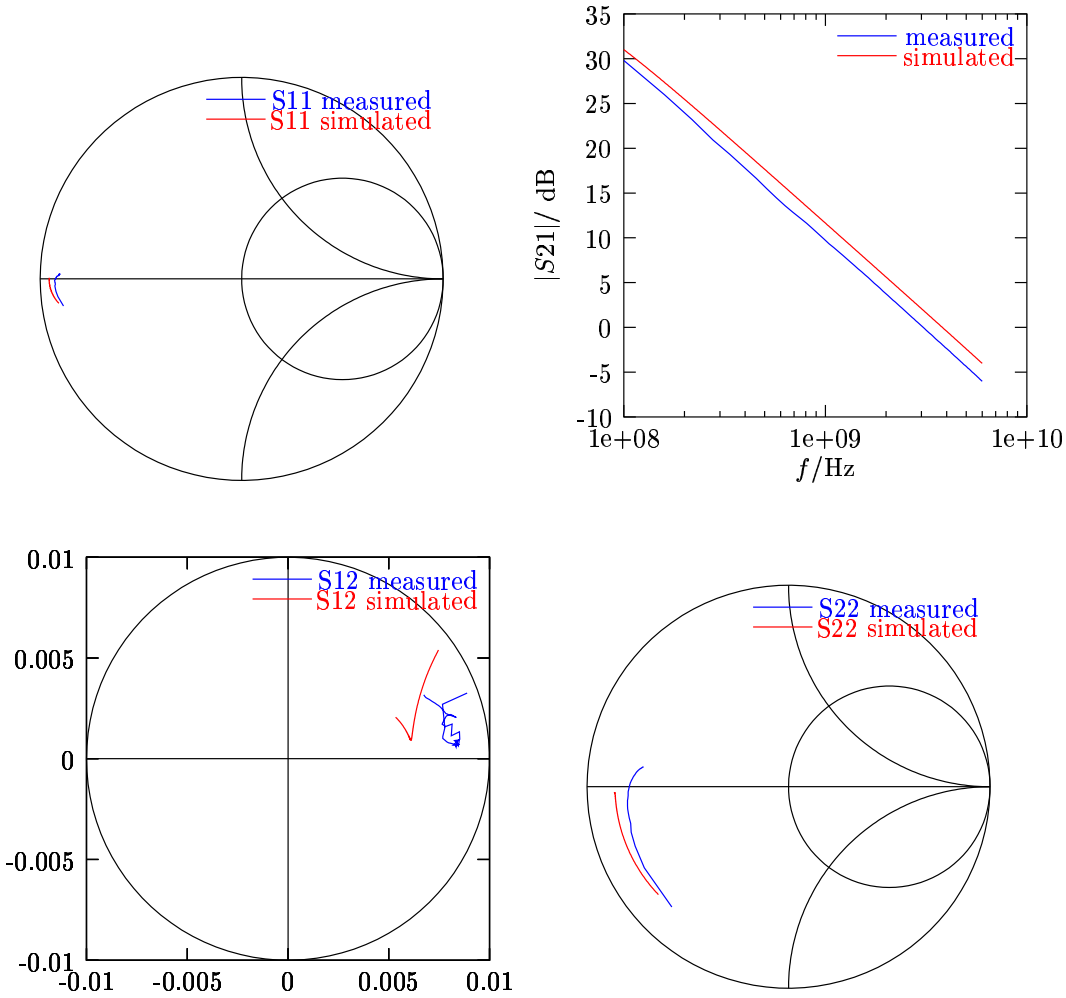


Figure 5.7: Scaling test with 15 unit cells, comparison of simulated and measured S-parameters. The device was biased with two voltage sources: $V_{\mathrm{BE}} = 0.9$ V, $V_{\mathrm{CE}} = 1.5$ V, the currents were $I_{\mathrm{B}} = 2.51$ mA and $I_{\mathrm{C}} = 150$ mA.

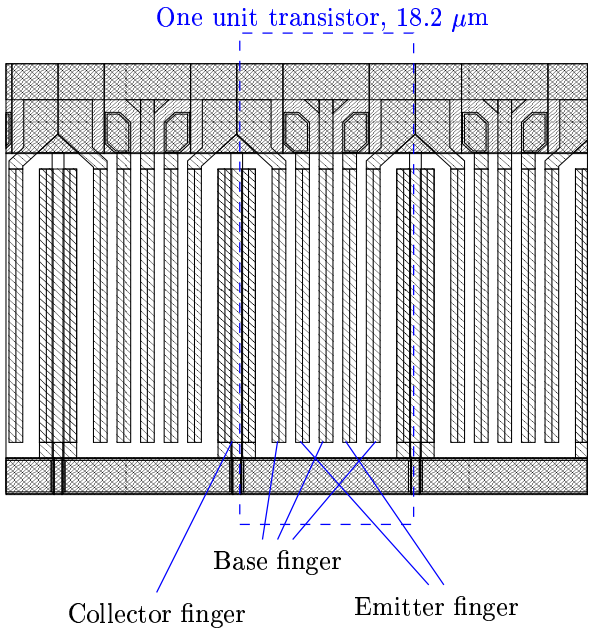


Figure 5.8: Layout detail of the driver transistor

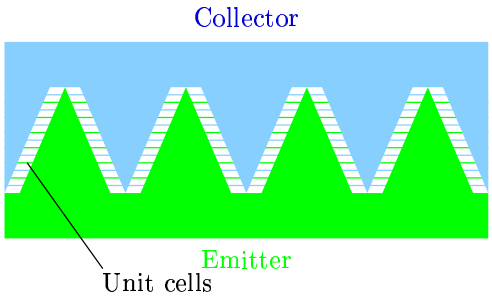


Figure 5.9: Collector and emitter contacting configuration

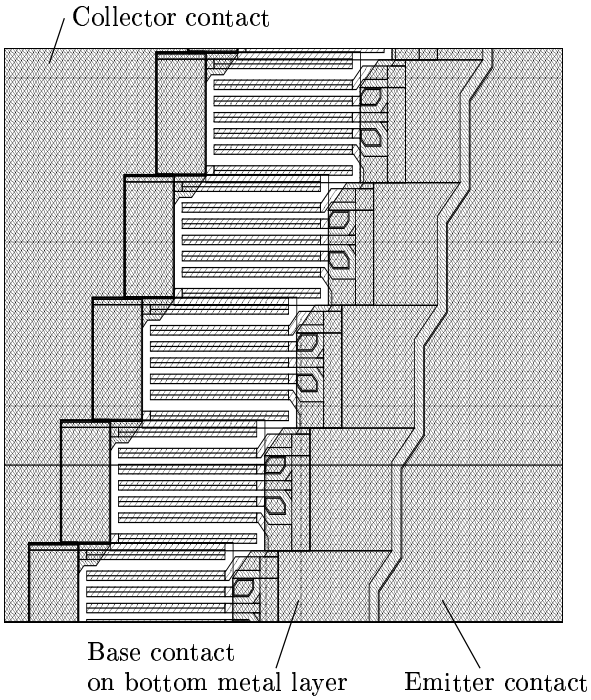


Figure 5.10: Layout detail of the power transistor

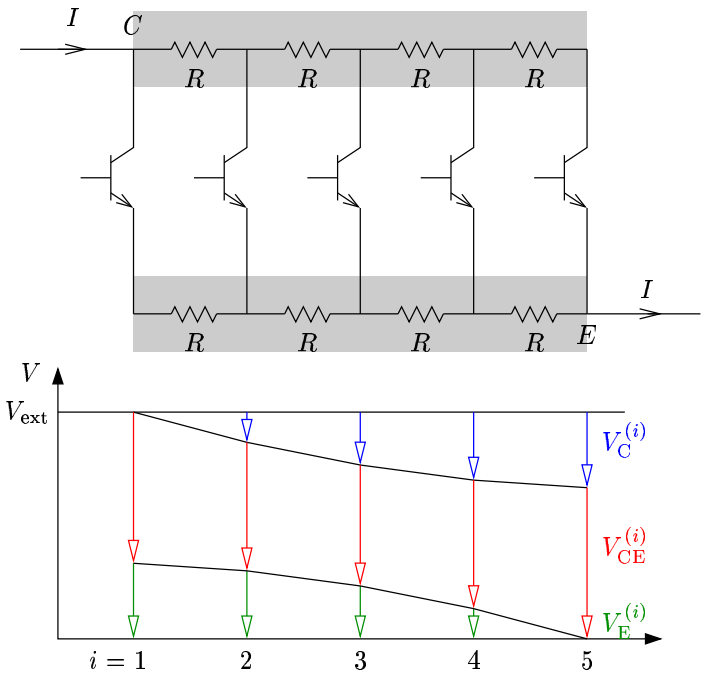


Figure 5.11: Rectangular collector and emitter finger

Figure 5.11 shows the voltages for a structure in which the five unit transistors are connected by a conventional rectangular finger. For the sake of simplicity, let us assume that the collector and emitter current of each unit cell is equal to $\frac{1}{5}I$. The collector current I enters the structure at the left edge of the finger and is divided equally among five fundamental cells. The constant voltage V_{ext} can be divided into the voltage drop along the collector finger from the common collector contact C to the collector of the unit cell $V_{\text{C}}^{(i)}$, the collector-emitter voltage at the unit cell $V_{\text{CE}}^{(i)}$, and the voltage drop along the emitter finger from the emitter of the unit cell to the common emitter contact E: $V_{\text{E}}^{(i)}$ Trivially,

$$V_{\text{ext}} = V_{\text{E}}^{(i)} + V_{\text{CE}}^{(i)} + V_{\text{C}}^{(i)} = const \tag{5.2}$$

holds for each unit transistor i. V_{CE} is smaller for the unit transistors near the center of the finger, which leads to current imbalances.

This effect can be avoided by tapering the collector and emitter fingers, as shown in Fig. 5.12. In the simplified layout in Fig. 5.12 the finger width at each point is proportional to the current traversing it. Thus the voltages across the resistors modelling the collector and emitter fingers are equal. In the case of increasingly many transistors distributed along the finger, the

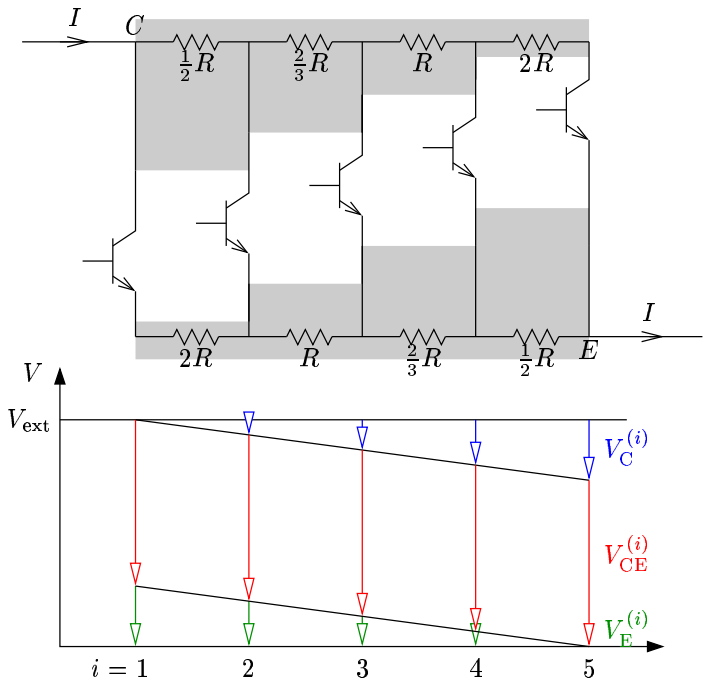
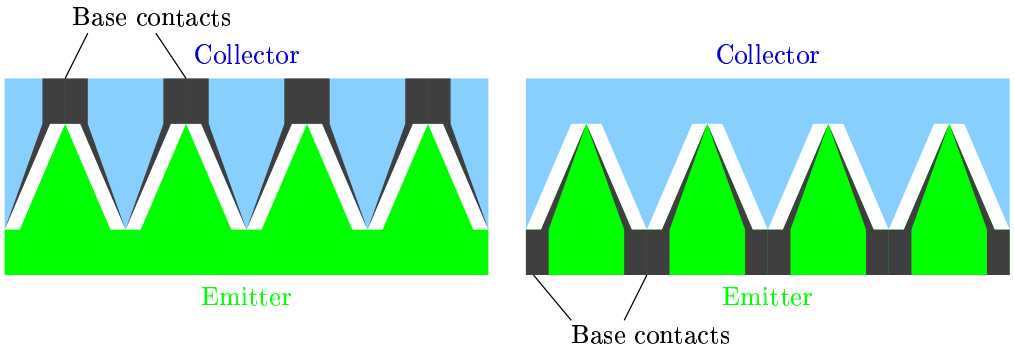


Figure 5.12: Tapered collector and emitter finger

gradients of V_{C} and V_{E} are constant along the finger length. In consequence, the collector-emitter voltage V_{CE} is equal for each unit transistor.

The tapered finger is also advantageous if the current density in the metallization is the (lower) limit for the device size because the current density is the same for each section of the tapered finger, and the finger needs to reach its maximum width (determined by the gross current I) only at its base.

It would of course be desirable to achieve the same effect for the base-emitter voltage as well by contacting the bases of the fundamental devices from the collector side as shown in Fig. 5.13(a) (although the voltage gradient along the base trace is much smaller). In the design presented here, the bases were, however, contacted from the emitter side as shown in Fig. 5.13(b), to minimize the Miller capacity which would have been undesirably high if large areas of collector and base metallization had been laid out above each other. Another advantage of the design in Fig. 5.13(b) is that the collectors could be placed as close to the edge of the chip as possible. Fig. 5.14 shows a photo of a single power transistor, mounted and bonded to a brass fixture for characterization.



(a) Bases contacted from the collector side

(b) Bases contacted from the emitter side

Figure 5.13: Base contact strategies

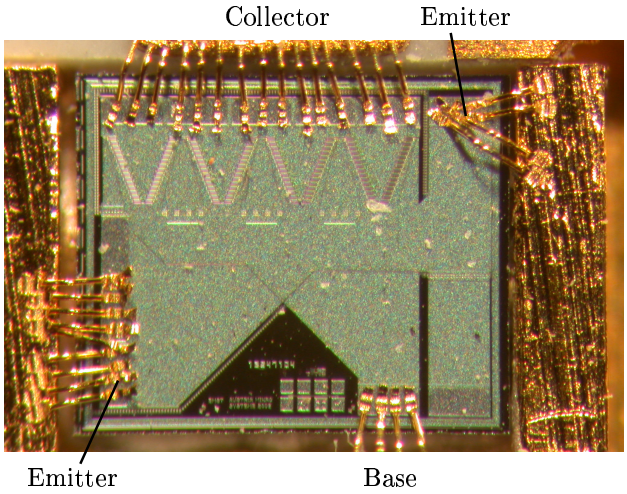


Figure 5.14: Chip photo of a power transistor

5.4.3 Thermal Considerations and Emitter Ballasting Resistance

In general, bipolar transistors with a positive temperature coefficient of the current gain β are, when connected in parallel, thermally unstable. An infinitesimal temperature difference between devices implicates a collector current imbalance, which in turn leads to higher power dissipation in the already warmer device. In the extreme case, this can result in the thermal destruction of all the involved devices. Sufficient thermal coupling of devices leads to a more uniform temperature and current distribution. If the thermal resistance between devices is not low enough, emitter ballasting resistors are needed as an additional feedback mechanism to stabilize the current distribution. Because some output power is lost in these emitter resistances, they should be kept as low as possible. A SiGe power amplifier without emitter ballasting resistors was reported [21] using SiGe HBTs with a uniform base, which have negative temperature coefficient of the current gain β.

The thermal conductivity of silicon at 300 K is $k = 1.5 \frac{\mathrm{W}}{\mathrm{cm\ K}}$. As a crude approximation, we calculate the thermal resistance of a piece of silicon of $\ell = 1$ mm length, and a cross-section area of $A = 300\ \mu\mathrm{m} \times 300\ \mu\mathrm{m}$ as

$$\theta_{\mathrm{th}} = \frac{1}{k}\frac{\ell}{A} = \frac{1}{1.5 \cdot 10^2}\frac{\mathrm{K\ m}}{\mathrm{W}} \cdot \frac{1\ \mathrm{mm}}{(300\ \mu\mathrm{m})^2} = 74\frac{\mathrm{K}}{\mathrm{W}}\ . \tag{5.3}$$

and take it as the worst case (i. e., the highest thermal resistance between any two fundamental cells).

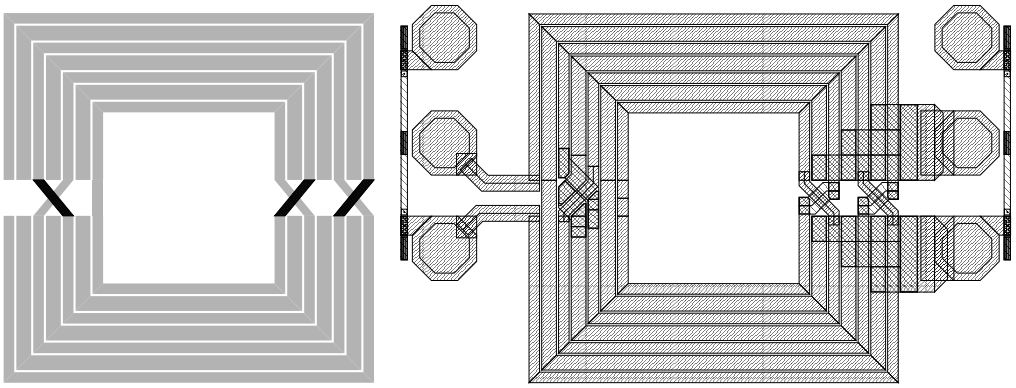
We can then proceed to calculate the required minimum value of the emitter ballasting resistor for stable current distribution, according to [1] (we set here $I_{\mathrm{C}} = I$ for simplicity): If a class A operating point at $V_{\mathrm{C}} = 2$ V, $I_{\mathrm{C}} = 1$ A is assumed, and with the thermal coefficient of the collector current $\alpha = 5 \cdot 10^{-2} I_{\mathrm{C}} \frac{1}{\mathrm{K}}$, and a temperature of 348 K (75 ° C, $\frac{kT}{e} = 30$ mV), we obtain a lower bound for the emitter ballasting resistance R_{E}:

$$R_{\mathrm{E}} \geq \frac{kT}{e}\frac{1}{I_{\mathrm{C}}}\left[\alpha\theta_{\mathrm{th}}V_{\mathrm{C}} - 1\right] = 192\ \mathrm{m\Omega}. \tag{5.4}$$

This condition was satisfied by the resistance of the aluminum layer connecting the devices, additional emitter ballasting resistances were not necessary.

5.5 On-chip Transformers

The on-chip transformers were simulated in ASITIC [5], a CAD tool for the synthesis and analysis of on-chip inductors and transformers. To verify the



(a) Layout used for ASITIC simulation

(b) Layout of the fabricated and measured transformer with probe pads

Figure 5.15: Layout of the test transformer

accuracy of the finite-elements simulation results from ASITIC, four transformers were fabricated and tested beforehand. Although only a simplified layout without most of the cross-over segments was simulated, the simulation agrees quite well with measurement results. Fig. 5.15 shows the layout used for simulation and the layout that was actually fabricated. Figure 5.16 shows simulated and measured S-parameters of one of these test transformers, a 4:1 transformer similar to the 5:1 input balun described in section 5.5.1.

5.5.1 Input Balun

The input balun (Fig. 5.17) is a 5:1 balun, with a center tap at the secondary winding for providing the driver stage base bias. To improve coupling, the secondary winding is divided into four individual traces connected in parallel, and situated between the turns of the primary winding. The trace that runs horizontally through the center of the balun is the center tap of the secondary winding. It is connected to the two innermost traces of the secondary winding at the left side of the balun, and can be accessed on the right edge of the balun just above and below the center. The input balun occupies a die area of approximately 450 μm by 450 μm. Each secondary trace is 10 μm wide, while the primary traces are 15 μm wide. All traces (except at cross-overs) reside on the topmost metal layer. Metal spacing is 2 μm.

The on-chip pre-match section consists of two 3.6 pF capacitors, one in series to each of the two input terminals of the input balun.

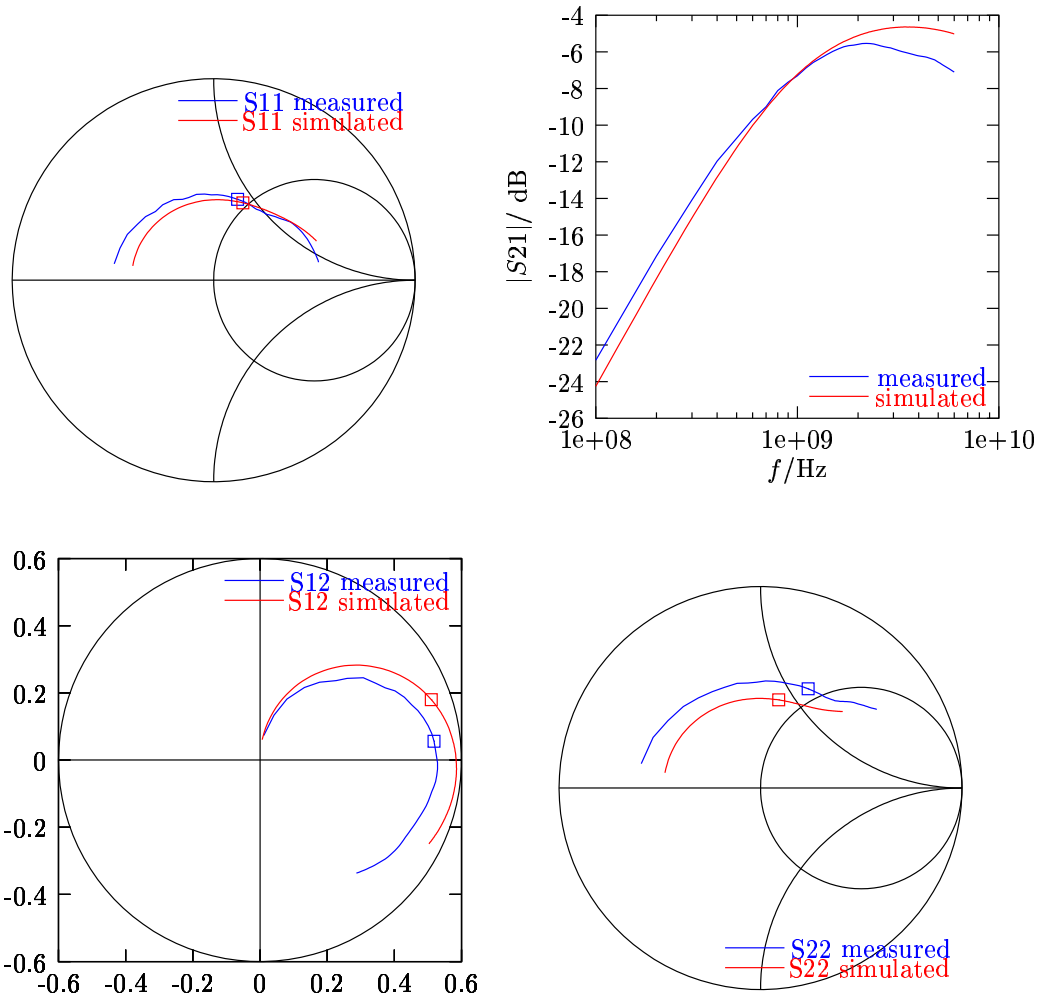


Figure 5.16: Test transformer S-parameters from 100 MHz to 6 GHz. Port impedances are $Z_1 = 50\ \Omega$ and $Z_2 = \frac{50}{16}\ \Omega = 3.125\ \Omega$. Values at 1.75 GHz are marked by a □.

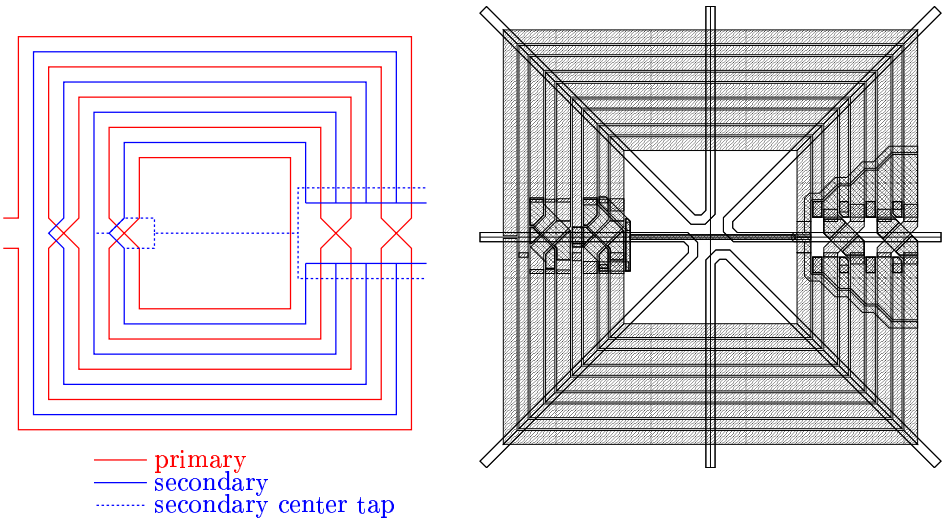


Figure 5.17: Layout of the input balun

5.5.2 Interstage Transformer

The interstage transformer (Fig. 5.18) features a turn ratio of 2:1, with center taps at both windings through which the driver stage collector bias and the power stage base bias are fed.

As with the input balun, the windings are split into parallel traces to improve coupling. Here, each of the two turns of the primary side are each split into two traces. Each trace occupies one of the gaps between the five parallel traces which make up the single turn of the secondary coil. The center tap of the secondary winding enters from the top and bottom. The two traces are connected in the center of the balun, and then run to the left to meet the three innermost of the five secondary traces. The high currents at the output of the driver stage necessitate quite a large balun: occupied die area is 1.66 mm by 1.66 mm; each trace of the primary winding is 70 μm, each secondary trace is 50 μm wide. Equal to the input balun, the spacing is 2 μm and all traces except cross-overs were placed in the top metal layer.

5.6 Driver Stage Bias

The driver stage RF transistors (Q3, Q4 in Fig. 5.19) are biased through an on-chip 1:100 current mirror consisting of Q1 and (Q3 || Q4) with base current compensation (Q2) through the center tap of the input balun. The reference current I_{ref} is provided off-chip (see section 6.1 for a description of

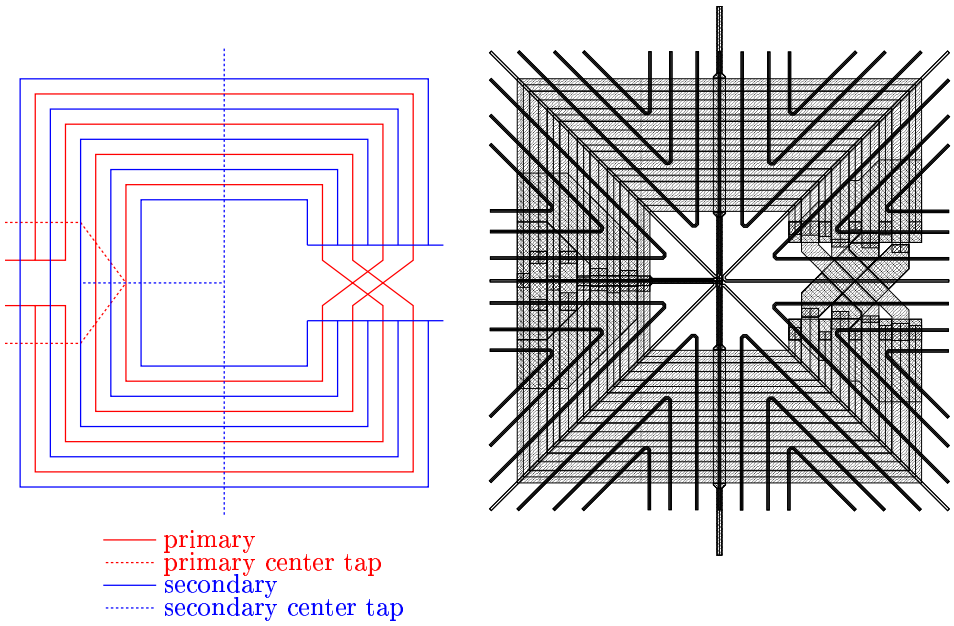


Figure 5.18: Layout of the interstage transformer

the DC supply circuits).

In order to obtain an exact 1:100 ratio of resistances, the 5 kΩ and 50 Ω resistors are composed from an array of 20 resistors (500 Ω each), shown in Fig. 5.20. Ten resistors are connected in series (between points "A"), the other ten are connected in parallel (between the bars "B"). Dummy resistors were added at both ends of the array to minimize edge effects.

5.7 Power Stage Bias and Protection

The on-chip base bias current mirror presented in Fig. 5.21 for the power stage is similar to the one for the driver stage presented above, with a current ratio of 1:120.

To prevent damage to the power devices due to high collector-emitter voltages (at load mismatch at the PA output), two VSWR protection circuits, one for each power transistor, were integrated on the die to detect potentially harmful peak voltages and turn down the amplifier.

Figure 5.22 shows the schematic of the VSWR protection circuit for one of the RF transistors in the power stage. The peak voltage at the PA output is detected by the peak detector Q1, C1, where Q1 acts as a diode. Resistor R1 limits the current through Q1. The discharge of C1 can be accelerated

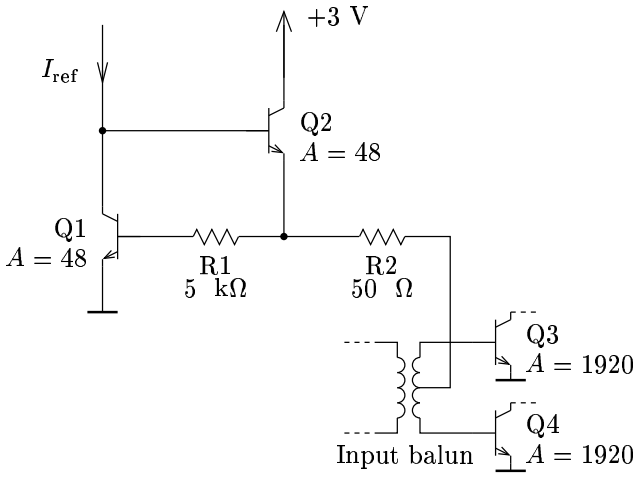


Figure 5.19: Schematic of the driver stage base bias

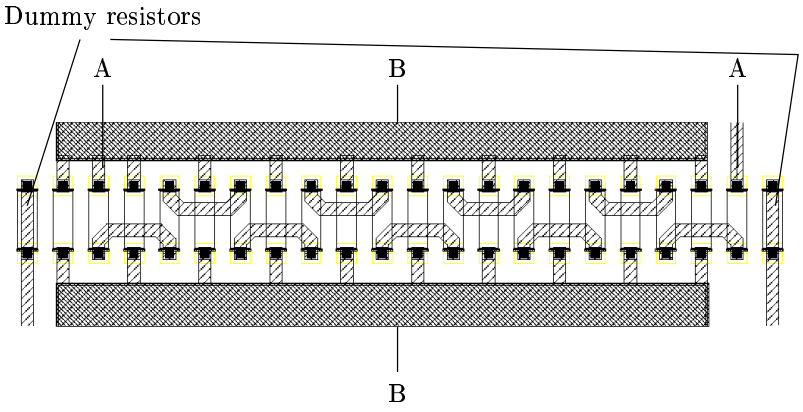


Figure 5.20: Layout of resistors in the driver stage base bias

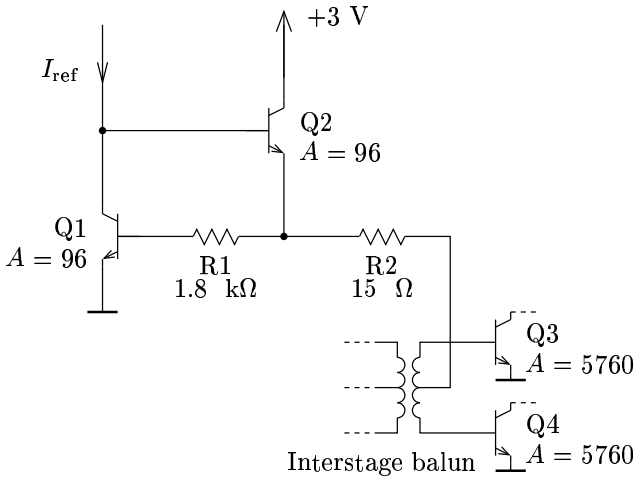


Figure 5.21: Schematic of the power stage base bias

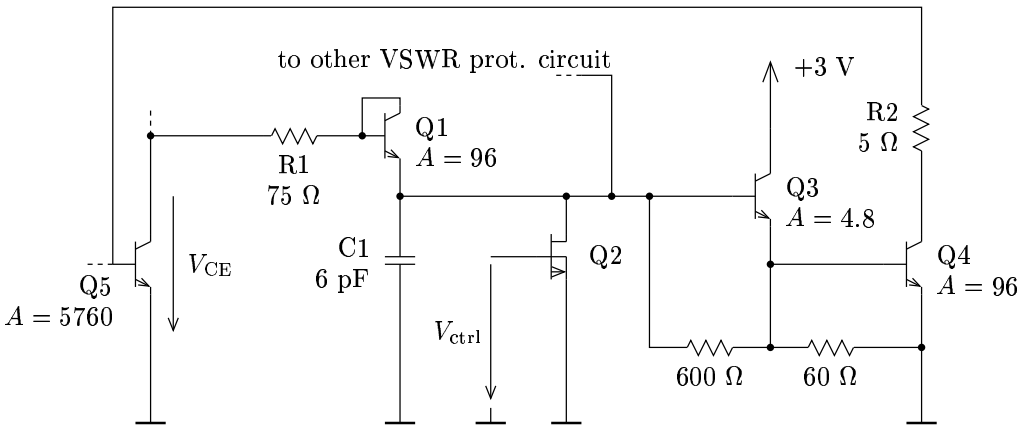


Figure 5.22: Schematic of the VSWR protection circuit

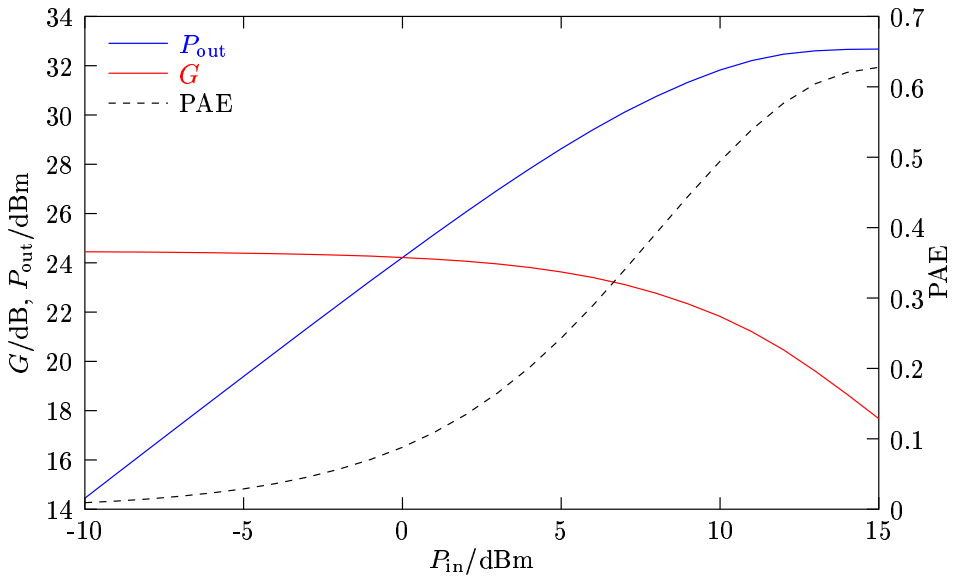


Figure 5.23: Single-tone power amplifier simulation results at 1.75 GHz

by applying a DC voltage V_{ctrl} to the gate of the FET Q2, which acts as a voltage-controlled resistor. Increasing V_{ctrl} increases the threshold for V_{CE}. If V_{CE} exceeds the threshold, the base current of the power device Q5 is diverted through the Darlington transistor Q3, Q4. Since the protection circuits of the two power transistors are connected at the base of Q3, the other power transistor is turned off as well. The resistor R2 isolates the VSWR protection circuit from the RF signal when the protection circuit is not active.

5.8 Simulation results

Simulation results for the whole PA chip are shown in Fig. 5.23 for single-tone excitation and 5.24 for a two-tone input signal.

5.9 Off-Chip Components

Figure 5.25 shows the RF PCB containing the input and output matching networks along with a tuning section and a lattice-type LC balun [6] at the output, in which the lumped elements except one capacitor are replaced by microstrip lines.

The substrate material used was Rogers RO 4003, 510 μm thick with 35 μm copper, gold-plated.

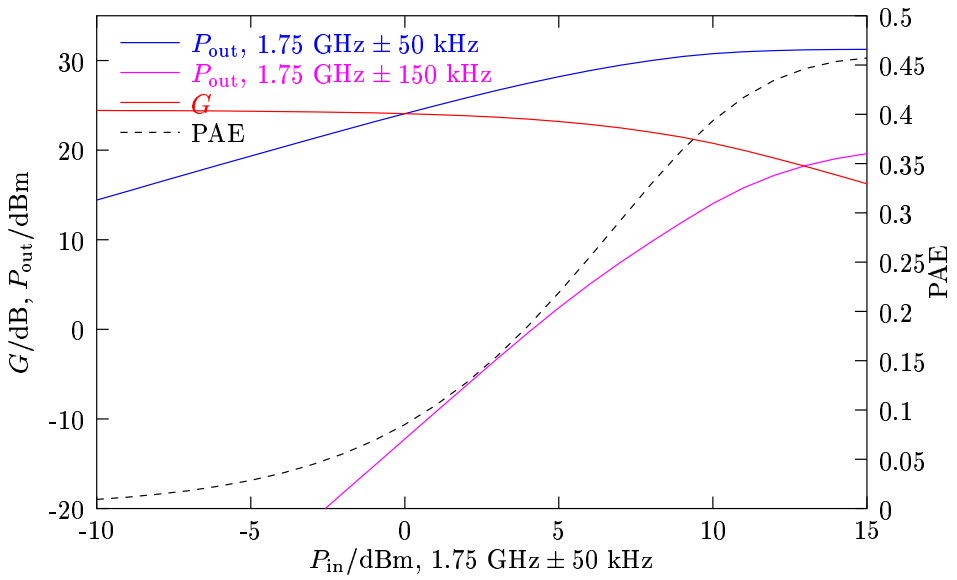


Figure 5.24: Two-tone power amplifier simulation results at 1.75 GHz ± 50 kHz

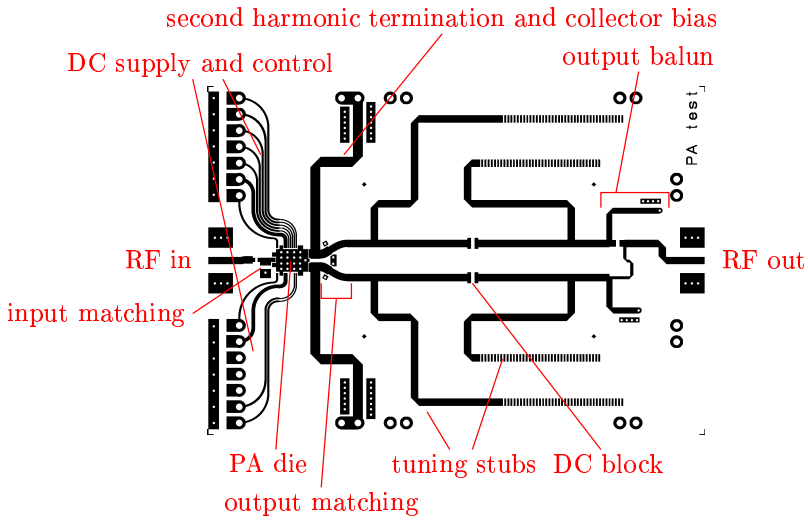


Figure 5.25: Layout of the PA test RF PCB

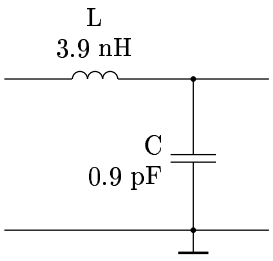


Figure 5.26: Schematic of the input matching

Frequency	Γ_{in}		Z_{in}	
1.75 GHz	0.937	-179 °	1.66 Ω	-12.8 °
3.50 GHz	1.0	-180 °	0.0 Ω	
5.25 GHz	0.948	130 °	23.6 Ω	86.1 °

Table 5.2: Optimum load impedance, simulated

5.9.1 Input Matching

The off-chip input matching section is a simple LC match. Fig. 5.26 shows the schematic. L is a Coilcraft CC04CS3N9 3.9 nH inductance, while C is an ATC 500S0R9A 0.9 pF capacitor.

5.9.2 Output Matching

The power stage was implemented as a class F amplifier of the type presented in section 2.2.4. The optimum load impedances from simulations are given in Table 5.2 and Figure 5.28. The matching at the fundamental frequency was done by means of the circuit in Fig. 5.27. The matching is illustrated in the smith chart in Fig. 5.28. C was realized with two single-layer capacitors (Tecdia AMS3R9J1H) with 3.9 pF each, one at each side of the microstrip line (see Fig. 6.3). The short at $2f_0$ was produced by a $\frac{\lambda}{4}$ shorted stub ("second harmonic termination" in Fig. 5.25), which was also used as a DC feed for supplying the bias voltage to the collectors of the power transistors. The third harmonic impedance of the given matching network was satisfying.

5.9.3 Tuning

Two open-ended stubs were placed between the output matching and the output balun on each of the differential paths to tune the output resistance

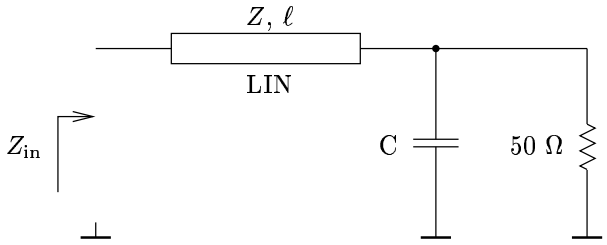


Figure 5.27: Output matching network for the fundamental frequency

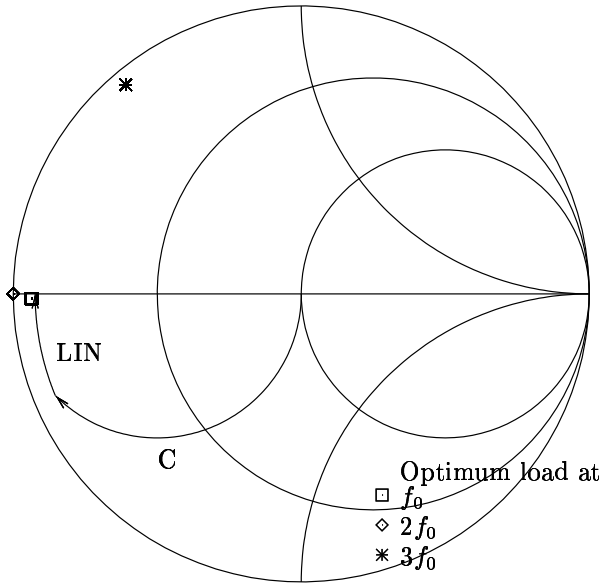


Figure 5.28: Optimum load impedances and matching at the fundamental frequency $f_0 = 1.75$ GHz

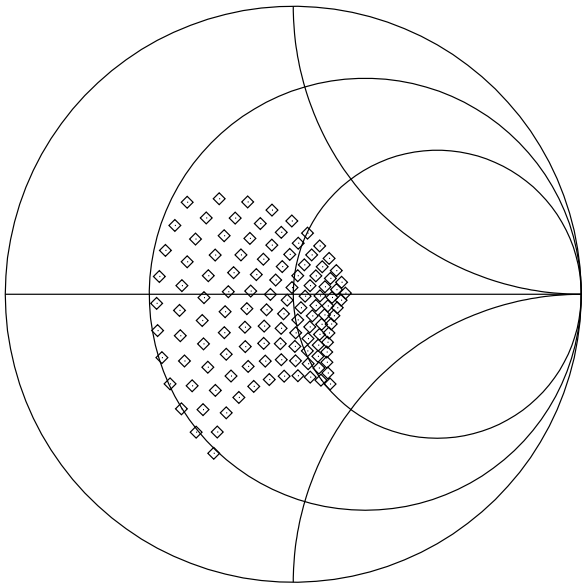


Figure 5.29: Input reflection coefficient of the tunable load impedance, $Z_0 = 1\ \Omega$. Only one branch of the symmetric matching and tuning networks was simulated

during measurements. The stubs were lengthened and shortened by moving copper strips the width of the microstrip line which were soldered to the end of the microstrip line. The DC block capacitor was a 33 pF capacitor (ATC 100A330J), with a series resonant frequency of 1.70 GHz, which is sufficiently near the freqency of operation.

Figure 5.29 shows the load impedance for various combinations of stub lengths at 1.75 GHz. Each stub length was varied by ± 5 mm around its nominal length.

5.9.4 Output Balun

The output balun was designed following the procedure described by Bakalski et al. [6], where three of the elements (L1, L2, and C2) of a lattice-type LC balun (Fig. 5.30) are realized with microstrip lines. With $\omega_1 = 2\pi 1.75$ GHz, the differential input resistance $R_1 = 100\ \Omega$, and the load resistance $R_\mathrm{L} = 50\ \Omega$, we get the characteristic impedance $Z_1 = \sqrt{50\ \Omega \cdot 100\ \Omega} = 70.71\ \Omega$. and with equation (1) from [6] we get

$$L_1 = L_2 = 6.43 \text{ nH} \tag{5.5}$$

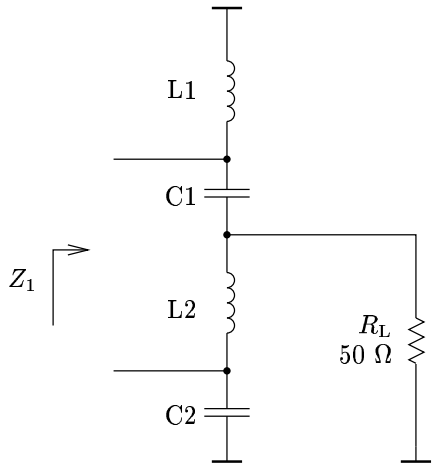


Figure 5.30: Schematic of the output balun

and with equation (2) from [6]

$$C_1 = C_2 = 1.29 \text{ pF} . \tag{5.6}$$

The electrical length of the microstrip lines substituting L_1, L_2, and C_2, was $\theta = 0.7$ (40.11 °), with the respective line impedances

$$Z_{L1} = 83.94 \ \Omega , \tag{5.7}$$

$$Z_{L2} = 109.75 \ \Omega \text{ , and} \tag{5.8}$$

$$Z_{C2} = 59.38 \ \Omega . \tag{5.9}$$

Fig. 5.31 shows the measured and simulated S-parameters of the output balun.

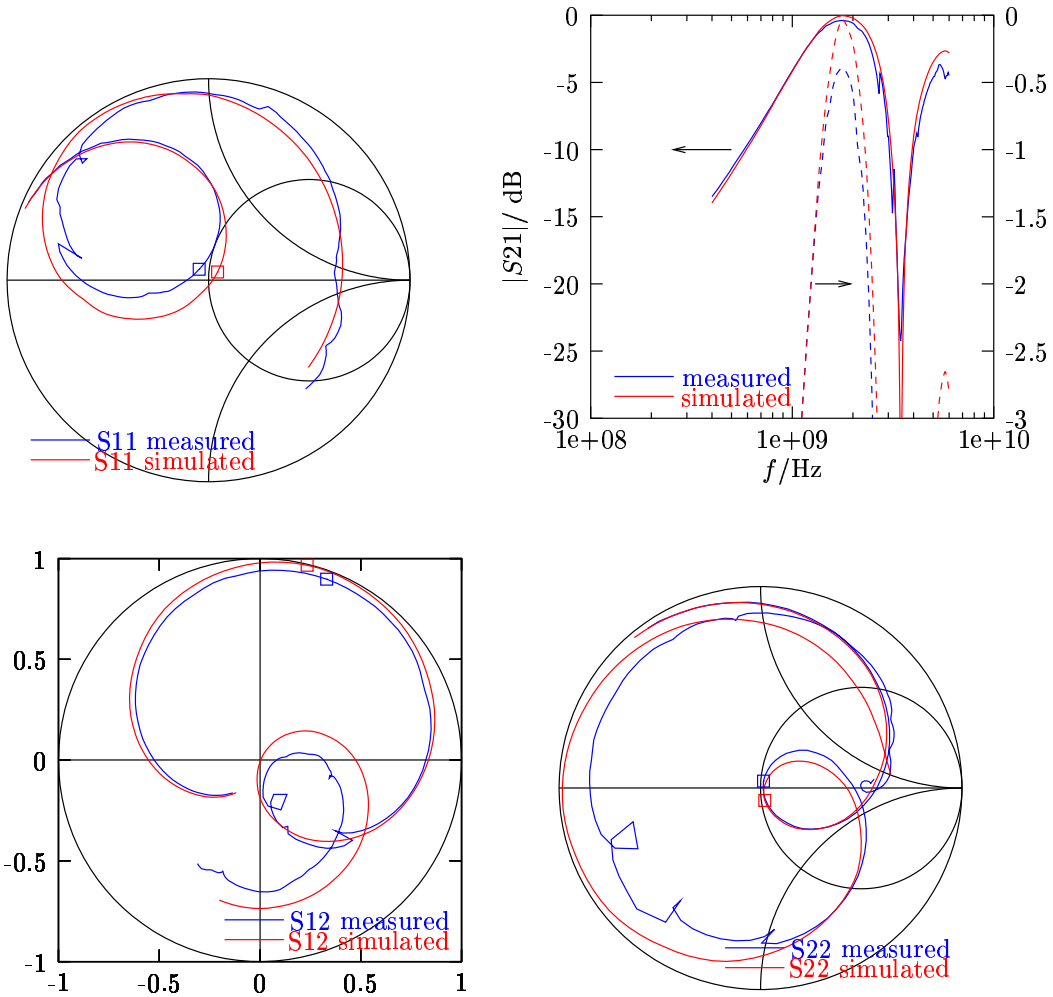


Figure 5.31: S-parameters of the output balun from 500 MHz to 6 GHz. Values at 1.75 GHz are marked by a □. Port 1: 100 Ohm differential, Port 2: 50 Ohm single-ended

Chapter 6

Evaluation

In addition to the power amplifier, some dies which contain only power HBTs, with pads suitably placed for both bonding and on-wafer tests, were fabricated at *austriamicrosystems*. Two types of mounts were produced for each of these die types: first, the devices were mounted on a printed circuit board, with a brass block as a heatsink at the bottom of the (RF) PCB, and second, a brass fixture to which the chips were mounted directly. Fig.6.1 shows a schematic cross-section of such a fixture. The brass rails that stick up next to the chip provide good RF ground that can be accessed with very short bondwires. In addition to the RF print containing the input and output networks described in section 5.9, a DC print was fabricated for the power amplifier which contains a voltage regulator for the 3 V DC supply and two current sources for the collector bias of the driver and power stage. Figure 6.2 shows the complete measurement assembly for the power amplifier, and Fig. 6.3 is a detail view of the mounted power amplifier chip.

6.1 DC Supply Board

The DC supply board for the power amplifier contains two current sources for the reference currents of the base bias circuits, and a 3 V supply for the on-chip protection and bias circuitry. The current sources for the driver and power stage base bias differ only in one resistance value. Their schematic is shown in Fig. 6.4. Approximate values for the load currents I_{ref} are 6 mA for the driver stage and 20 mA for the power stage. The schematic of the 3 V supply is shown in Fig. 6.5.

For monitoring purposes, some DC lines were connected to a DSUB9 connector on the DC board (at the left edge in Fig. 6.2) Table 6.1 shows the allocation of the DSUB9 connector pins. All signals are “sense”-only signals.

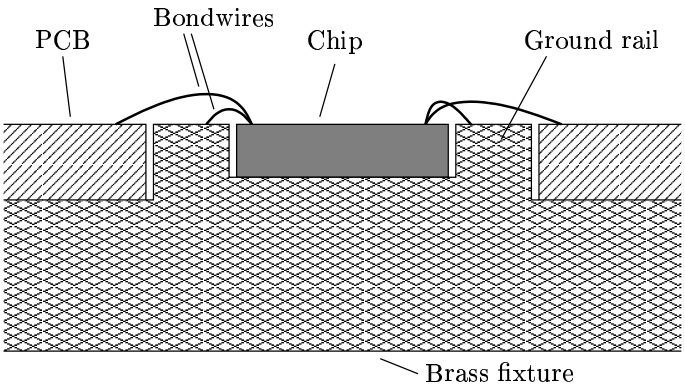


Figure 6.1: Schematic cross-section of a brass fixture

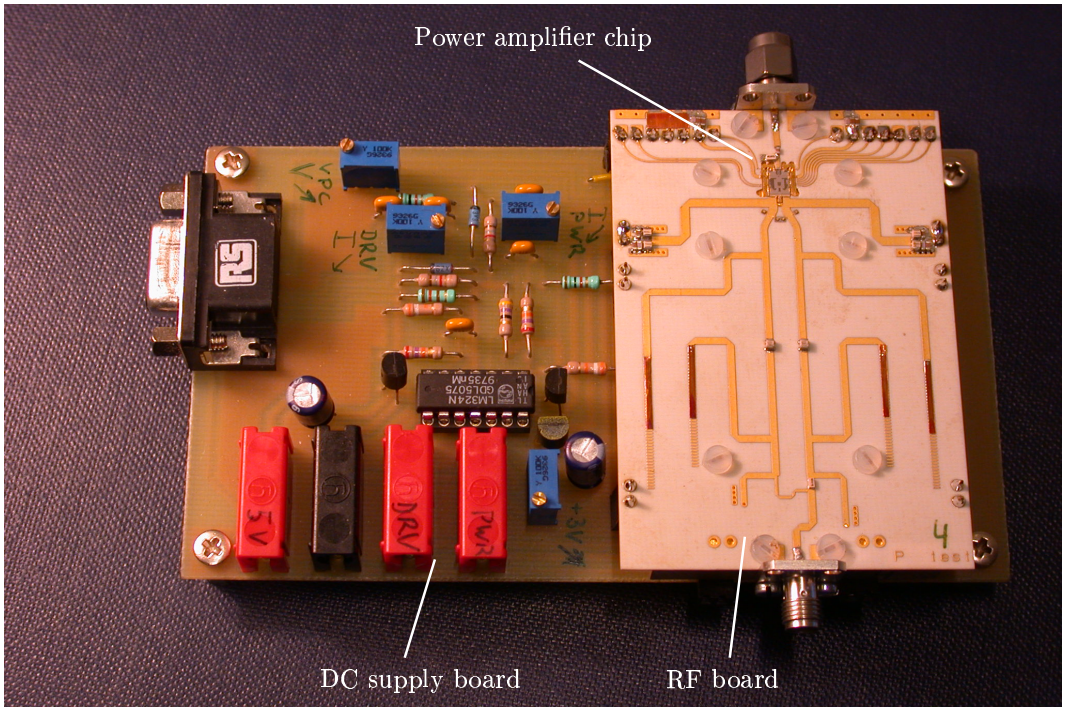


Figure 6.2: Photo of the power amplifier measurement assembly

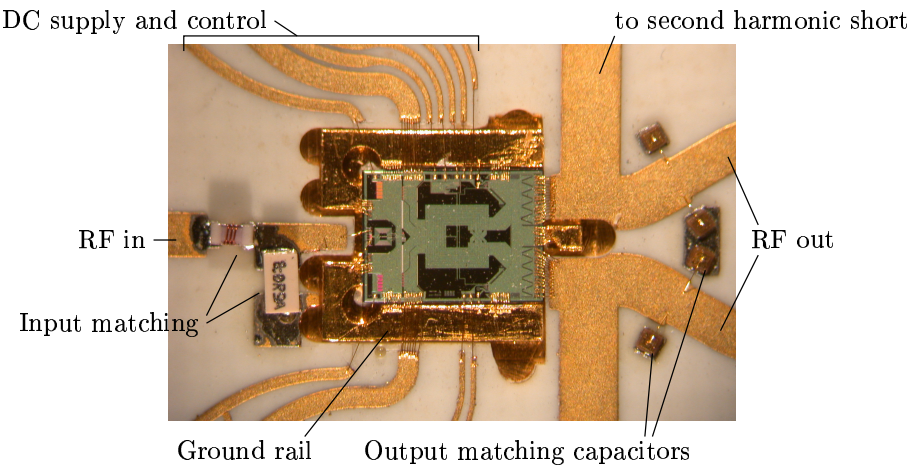


Figure 6.3: Photo of the mounted power amplifier chip

The base bias currents I_{ref} in Fig. 6.4 were not measured directly. The voltage along the resistor R1 was measured instead (pins 6 and 1 for the driver stage, pins 6 and 2 for the power stage in Tab. 6.1), via sense contacts and the current approximated as

$$I_{\mathrm{ref}} \approx \frac{V_{\mathrm{S}}}{\mathrm{R1}} \ . \tag{6.1}$$

This equation was tested by measuring I_{ref} and V_{S} on the DC board alone. The load were three diodes (1N4148) in series. The results (Tab. 6.2 and 6.3) were used to calculate the more accurate resistance values of $\mathrm{R1_D} = 121.7\ \Omega$ for the driver stage and $\mathrm{R1_P} = 47.5\ \Omega$ for the power stage. The collector bias voltages for both stages were fed from external sources.

6.2 Calibration Kit

For the HBT evaluation, a calibration kit was built to allow for the reference planes to be at the PCB-sided end of the bondwires. The contacts and microstrip lines of the calibration kit elements shown in Fig. 6.6 were identical to those of the power amplifier test PCBs, with the reference plane 5 mm from the board edge. The TRL method [9] was chosen because it can easily be implemented in a microstrip PCB design.

The calibration kit consists of the following elements:

- Through

Pin number	Signal
1	Driver stage base bias sense
2	Power stage base bias sense
3	Ground
4	+3 V
5	Driver stage V_{CC}
6	+5 V
7	Power stage protection control (V_{ctrl} in Fig. 5.22)
8	Ground
9	Power stage V_{CC}

Table 6.1: DC board, DSUB9 connector pins

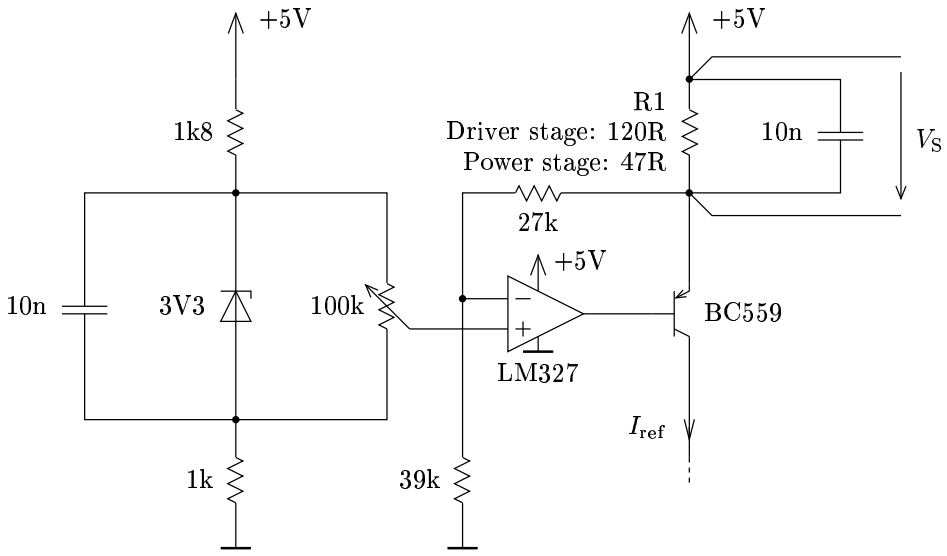


Figure 6.4: Schematic of a bias current source

I_{ref}	V_S	V_S/I_{ref}
6 mA	730 mV	121.67 Ω
12 mA	1461 mV	121.75 Ω

Table 6.2: V_S, I_{ref} results, driver stage

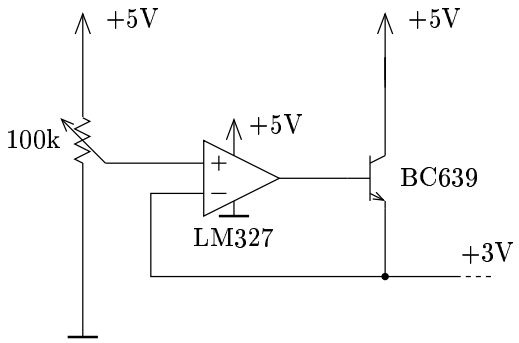


Figure 6.5: Schematic of the bias voltage source

I_{ref}	V_{S}	$V_{\text{S}}/I_{\text{ref}}$
10.5 mA	500 mV	47.62 Ω
20.0 mA	948 mV	47.4 Ω

Table 6.3: V_{S}, I_{ref} results, power stage

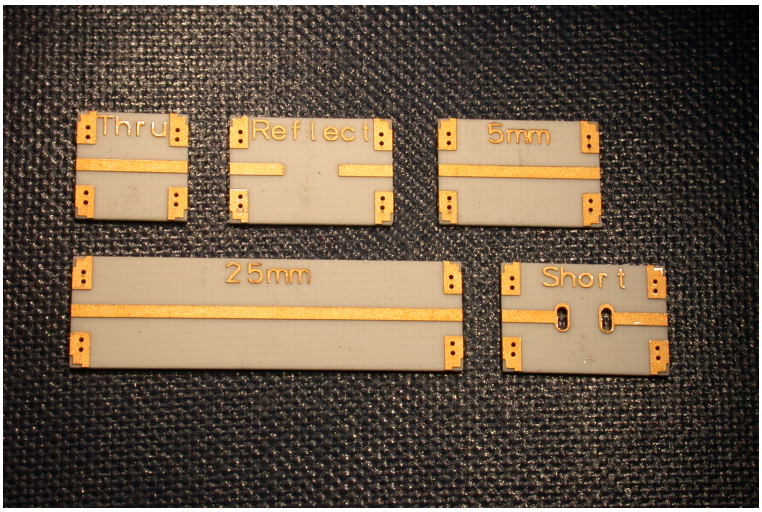


Figure 6.6: Photo of the calibration kit elements

- Reflect (open-ended stubs)
- Line, length $\ell_1 = 25$ mm
- Line, length $\ell_2 = 5$ mm
- Short (shorted stubs). The "Short" elements were used to determine the DC resistance of the setup up to the reference plane during DC measurements.

The phase offset between a "Line" element and the "Through" element must be between 20 ° and 160 ° for useful calibration in the associated freqency range [2], optimum accuracy is reached at 90 °. The ratio of the upper corner freqency of the i-th "Line" element $\overline{f}_i$ to the lower corner frequency of the same element $\underline{f}_i$ is thus bounded by

$$\frac{\overline{f}_i}{\underline{f}_i} < \frac{160\ ^\circ}{20\ ^\circ} = 8\ . \tag{6.2}$$

For calibrated measurements from 500 MHz to 6 GHz (a freqency ratio of 12, or $(3.46)^2$), *two* line elements were needed. The effective dielectric constant of the Rogers RO4003 substrate ($\epsilon_\mathrm{r} = 3.38$) is $\epsilon_\mathrm{eff} = 2.7$ for 50 Ω microstrip lines. The longer line should have an electrical length of more than 20 ° at 500 MHz, which leads to a minimum length of

$$\ell_{1\mathrm{min}} = \frac{20\ ^\circ}{360\ ^\circ}\frac{c}{500\ \mathrm{MHz}\sqrt{2.7}} = 20.2\ \mathrm{mm}\ , \tag{6.3}$$

where $\frac{c}{500\ \mathrm{MHz}\sqrt{2.7}}$ is the wavelength at 500 MHz. The associated upper corner frequency is $8 \cdot 500$ MHz = 4 GHz. Since the desired frequency range could easily be covered with two line elements, the length ℓ_1 was chosen to be well above this minimum value. For $\ell_1 = 25$ mm, the corners of the usable frequency range can be calculated as

$$\underline{\lambda}_1 = 25\ \mathrm{mm} \cdot \frac{360\ ^\circ}{20\ ^\circ} = 450\ \mathrm{mm}\ ; \quad \underline{f}_1 = \frac{c}{\underline{\lambda}_1\sqrt{\epsilon_\mathrm{eff}}} = 408\ \mathrm{MHz} \tag{6.4}$$

and

$$\overline{\lambda}_1 = 25\ \mathrm{mm} \cdot \frac{360\ ^\circ}{160\ ^\circ} = 56.25\ \mathrm{mm}\ ; \quad \overline{f}_1 = \frac{c}{\overline{\lambda}_1\sqrt{\epsilon_\mathrm{eff}}} = 3.26\ \mathrm{GHz}\ . \tag{6.5}$$

To have some overlap between the line elements, the length of the second line element was not chosen to be $\frac{1}{8} \cdot 25$ mm, but rather $\ell_2 = 5\ \mathrm{mm} = \frac{1}{5} \cdot 25$ mm. The corner frequencies of the second line element can easily be calculated as

$$\underline{f}_2 = \frac{\ell_1}{\ell_2}\underline{f}_1 = 2.04\ \mathrm{GHz} \tag{6.6}$$

and

$$\overline{f}_2 = \frac{\ell_1}{\ell_2}\overline{f}_1 = 16.3 \text{ GHz} . \tag{6.7}$$

The calibration kit used in evaluating the PA and power transistor performance allows calibrated measurements from 408 MHz to 16.3 GHz.

The time delay τ_i of a line element of length ℓ_i can be calculated as

$$\tau_i = \frac{\ell_i}{\frac{c}{\sqrt{\epsilon_{\text{eff}}}}} . \tag{6.8}$$

For the lengths from above, the delay times are

$$\tau_1 = \frac{\ell_1}{\frac{c}{\sqrt{\epsilon_{\text{eff}}}}} = 137 \text{ ps} \tag{6.9}$$

and

$$\tau_2 = \frac{\ell_2}{\ell_1}\tau_1 = 27.4 \text{ ps} . \tag{6.10}$$

6.3 Power Transistor Performance

In addition to the power amplifier, the transistors used in the power stage were fabricated separately to make device characterization possible. The first tests were carried out with the power HBTs glued and bonded to a small PCB (approx. 12 mm by 12 mm) in a test fixture, with a brass block at the bottom of the PCB to provide some cooling.

Measurements of the DC I_C/V_{CE} curves at constant V_{BE} values (Fig. 6.7) showed that the device was not thermally stable as a whole. During on-wafer tests, however, when the devices were on a whole wafer which was directly placed on a large metal block in the wafer prober, no such thermal runaway was observed. Figure 6.7 compares the DC I_C/V_{CE} curves of on-wafer to on-PCB measurements, as well as the curves of devices mounted directly on a gold-plated brass block (see below). Figure 6.8 compares the DC I_C/V_{CE} curves of the devices measured on PCB with on-wafer measurements at constant I_B.

RF tests of the PCB-mounted devices were not satisfying, either: The S-parameters did not match well and G_{max} was far below the simulated values, as shown in Fig. 6.9 and 6.10. Subsequent simulations with various combinations of parasitics added to the circuit revealed that the inductivity and resistance of the emitter bondwires and PCB vias were at least partially responsible for the low performance.

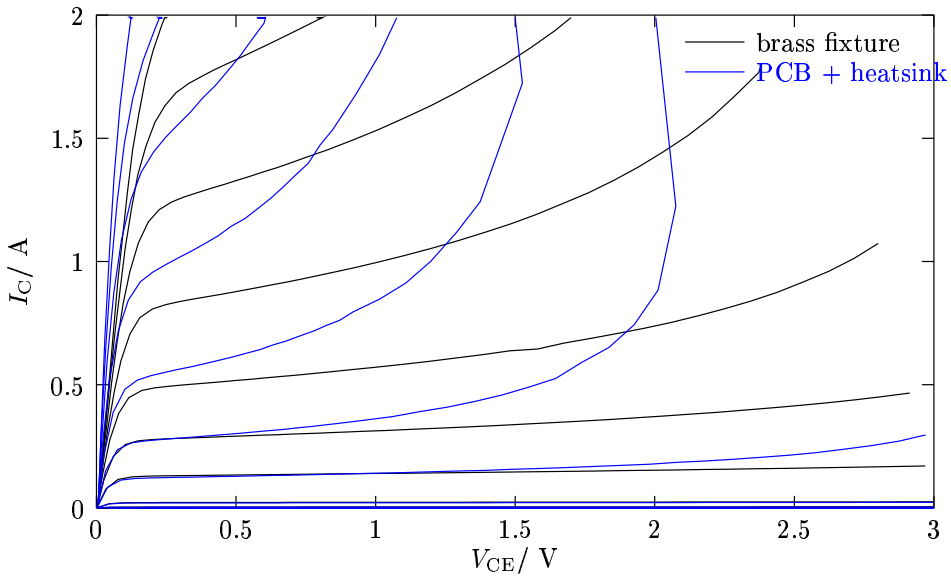


Figure 6.7: Power HBT, comparison of DC I_C/V_{CE} curves for constant V_{BE} of the device mounted on a PCB + heatsink, in the fixture, and measured on-wafer. V_{BE} values are 950 mV, 925 mV, 900 mV, 875 mV, 850 mV, 825 mV, 800 mV, 750 mV, 700 mV.

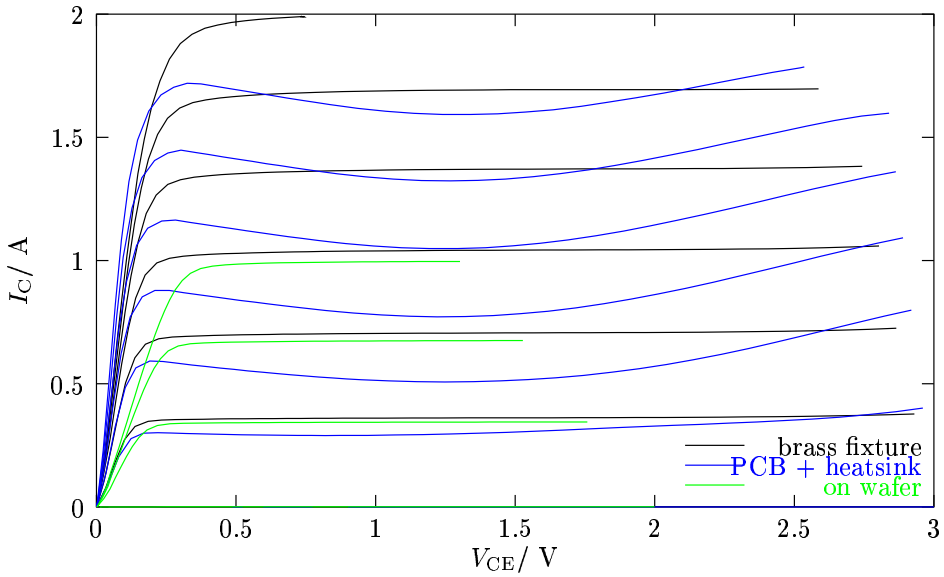


Figure 6.8: Power HBT, comparison of DC I_C/V_{CE} curves for constant I_B of the device mounted on a PCB, PCB + heatsink, in the fixture, and measured on-wafer. I_B values are 30 mA, 25 mA, 20 mA, 15 mA, 10 mA, 5 mA, 0 mA (only up to 15 mA for the on-wafer curves)

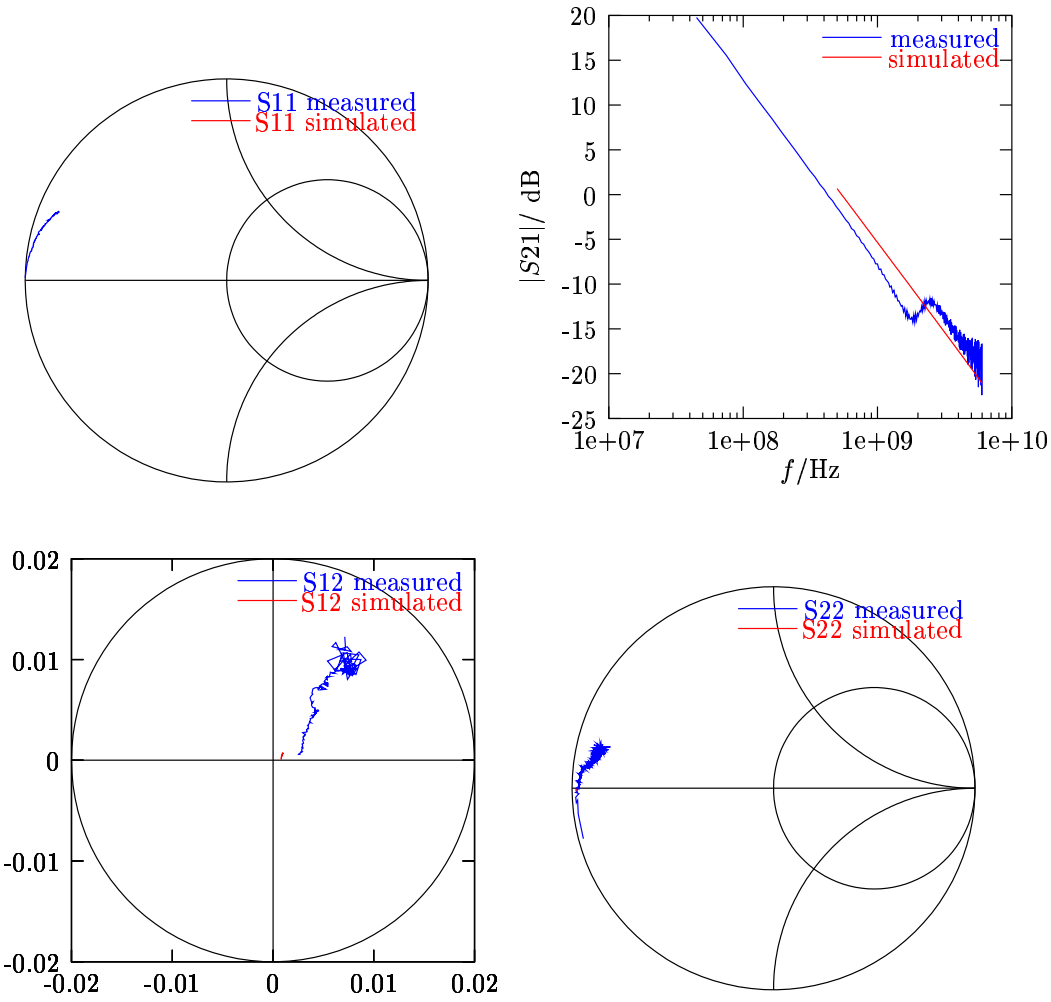


Figure 6.9: Simulated and (on-wafer) measured S-parameters for the power HBT device. Bias conditions: $I_{\mathrm{B}} = 20$ mA, $V_{\mathrm{CE}} = 1.5$ V

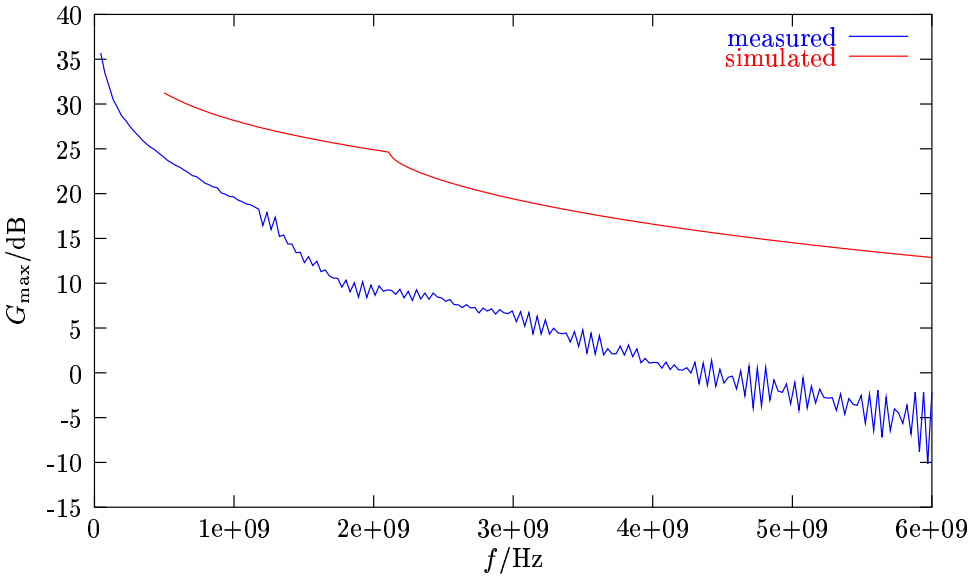


Figure 6.10: Simulated and (on-wafer) measured $G_{\max}$ for the power HBT device. Bias conditions: $I_{\mathrm{B}} = 20$ mA, $V_{\mathrm{CE}} = 1.5$ V

A brass fixture was fabricated to allow for much shorter bondwires at the emitter (bondwire length was only about 200–300 μm), and furthermore allowed to connect the bondwires not to a PCB, but to a massive brass block, thus eliminiating the resistance and inductivity of the PCB vias, and reducing the inductivity and resistance introduced by the bondwires. The cooling of the device was also much improved, since the thermal resistances of the PCB vias and of the PCB/brass block interface were eliminated. A schematic cross-section of the assembly is shown in Fig. 6.1.

6.3.1 Lumped-element Model for on-wafer Parasitics

The lumped-element model shown in Fig. 6.11 for the on-wafer parasitics of the power HBT was developed. R_{BS}, C_{BS}, R_{CS}, and C_{CS} represent the substrate losses. A comparison of the S-parameters and $G_{\max}$ from simulations of the above model compared to on-wafer measurements is shown in Fig. 6.12 and Fig. 6.13. The ability of this simple lumped-element model to emulate the layered structure of the substrate (the silicon and metal are separated by a thin insulating silicon oxide layer) and the complex geometry is, unfortunately, limited.

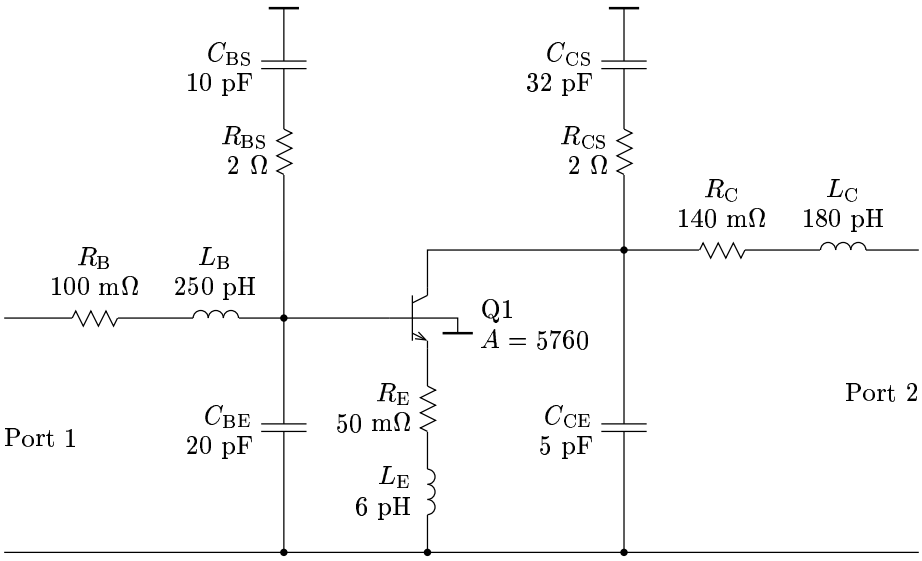


Figure 6.11: Lumped-element model of the on-wafer parasitics

6.3.2 EM Simulation of on-wafer Parasitics

A better match was achieved with EM simulations of the metallization, even with the coarse approximation of the layout shown in Fig. 6.14. To emulate the situation during on-wafer tests, the collector was only contacted at the bottom pad, and the emitter was contacted at the two pads adjacent to base and collector. The respective reference planes of the ports are the dotted lines in Fig. 6.14. Compare this to Fig. 6.15 which shows the placement of the on-wafer probes on the power transistors.

Internal ports were set to connect the HBTs to the metallization. The S-parameters obtained from the EM simulation were thereafter used in a simulation of the ideal transistor with the parasitics, as shown in Fig. 6.16. The results of these simulations are shown in Fig. 6.17 and 6.18. EM simulations were also carried out for an "empty" chip which consisted of the metallization and pads, but without the actual transistors, again with very good agreement between measured and simulated S-parameters.

6.3.3 Off-wafer Parasitics

The only notable off-wafer parasitics of the power HBTs when mounted in the brass fixture were the inductances of the bondwires. These were determined by adding lumped inductances to the S-parameters from the on-wafer tests, and by varying the inductivity values in this setup to fit the S-

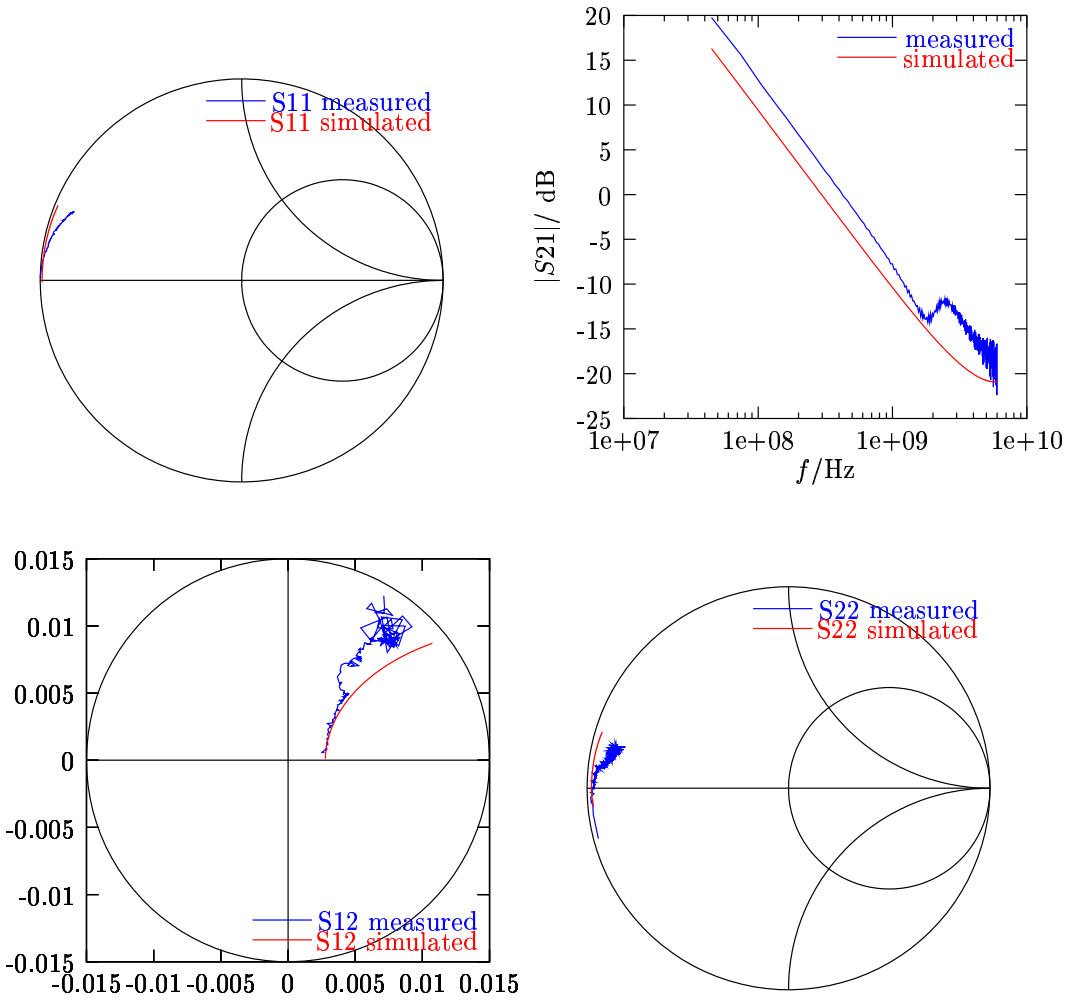


Figure 6.12: S-parameters of the lumped-element model for the on-wafer parasitics. $V_{\mathrm{CE}} = 1.5$ V, $I_{\mathrm{B}} = 20$ mA

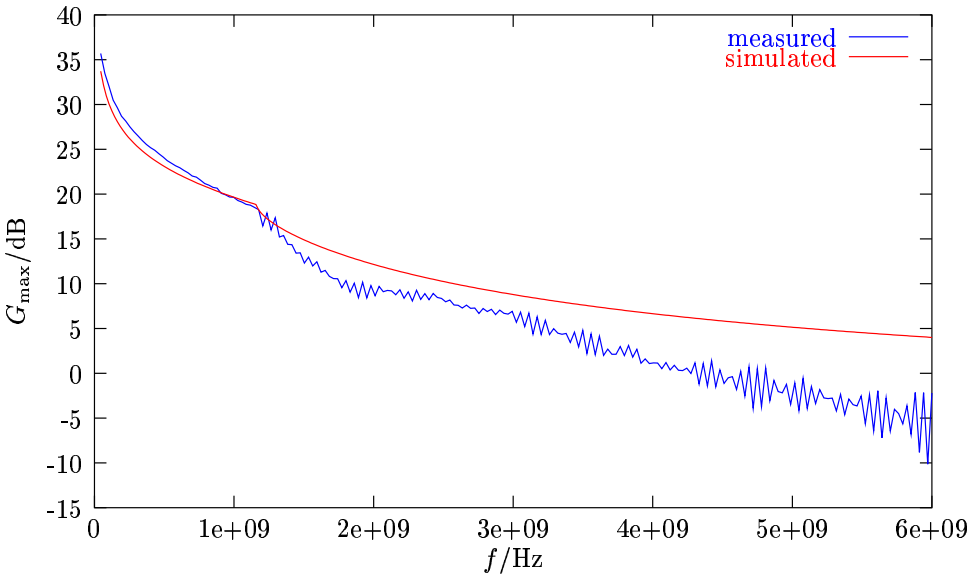


Figure 6.13: Maximum available gain G_{max} of the lumped-element model for the on-wafer parasitics. $I_B = 20$ mA, $V_{CE} = 1.5$ V

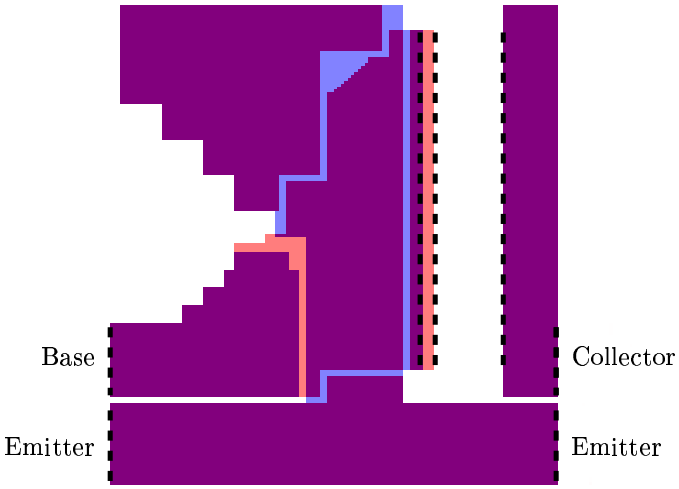


Figure 6.14: Power transistor layout used for EM simulations

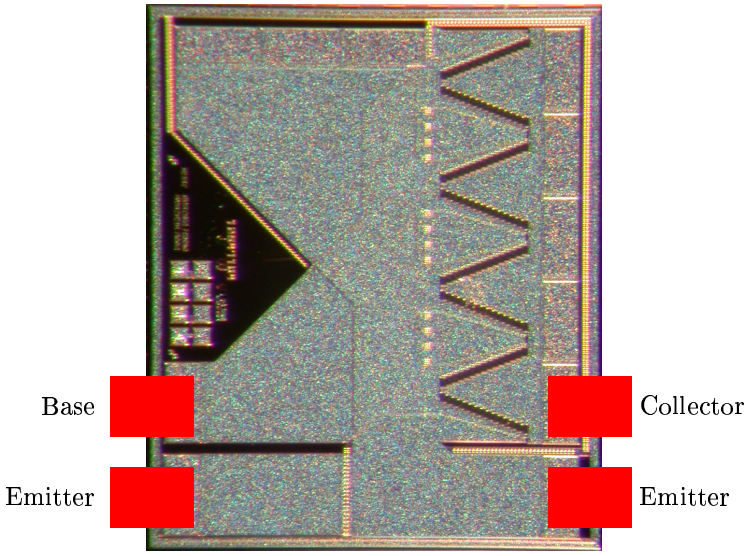


Figure 6.15: Placement of the probes during on-wafer tests of the power transsitor

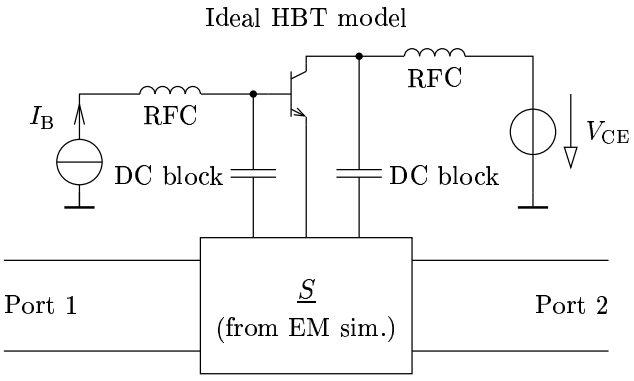


Figure 6.16: Combination of EM simulated parasitics and an ideal HBT model

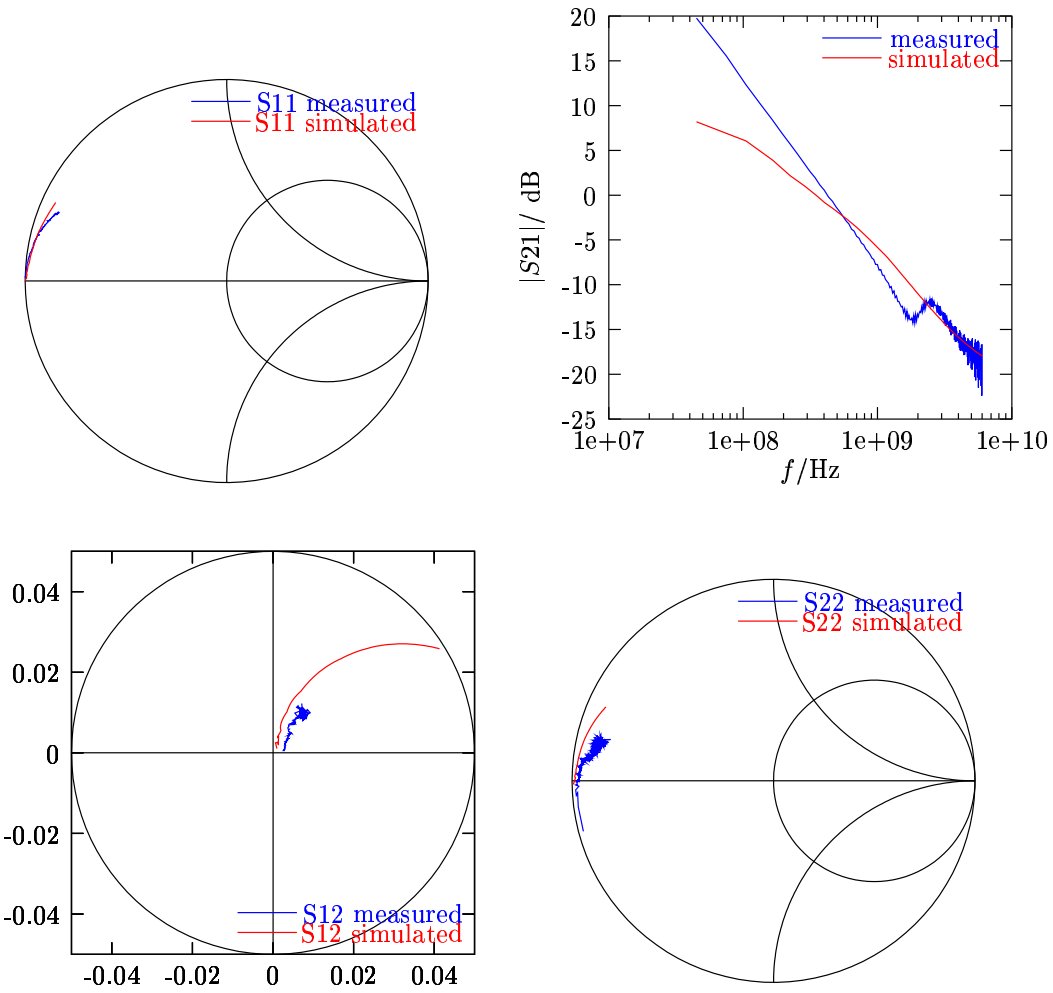


Figure 6.17: Comparison of S-parameters: On-wafer measurements and EM simulation of on-wafer parasitics, from 45 MHz to 6 GHz. $I_{\mathrm{B}} = 20$ mA, $V_{\mathrm{CE}} = 1.5$ V

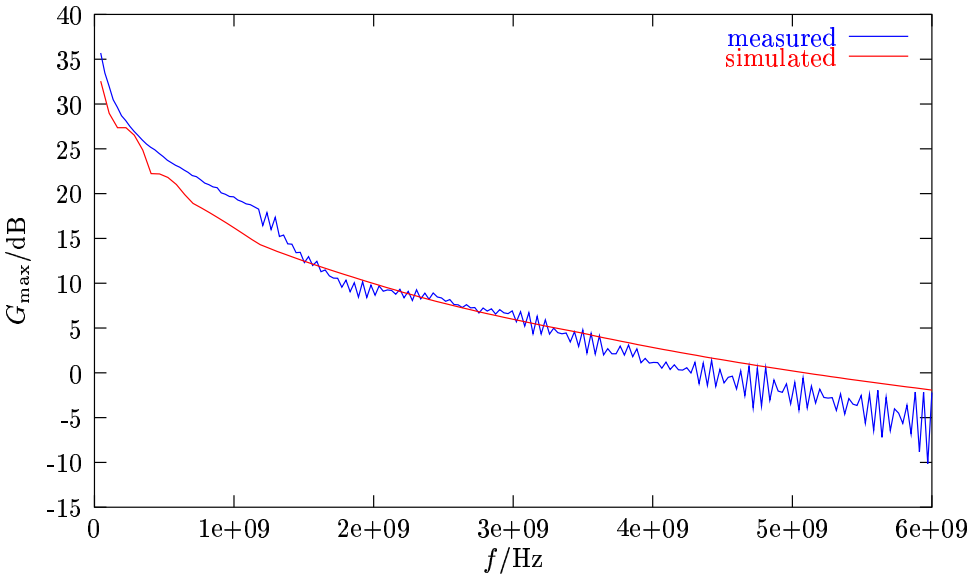


Figure 6.18: Comparison of $G_{\max}$: On-wafer measurements and EM simulation of on-wafer parasitics, $I_B = 20$ mA, $V_{CE} = 1.5$ V

parameters measured for the brass fixture-mounted device. Figure 6.19 shows the schematic of this lumped-element model, where $\underline{S}_{\text{int}}$ is the (measured) scattering matrix of the device including on-wafer parasitics. Figure 6.20 shows the S-parameters for this setup.

The impressive detrimental effect of the emitter inductivity on $G_{\max}$ is illustrated in Fig. 6.21. All other parasitics were set to their "normal" values (shown in Fig. 6.11 and 6.19), only the value of $L_{\text{E ext}}$ was varied. For the emitter inductivity of the transistor mounted in the brass fixture $L_{\text{E ext}} =$ 65 pH, the maximum available gain is reduced by about 4 dB. For realistic

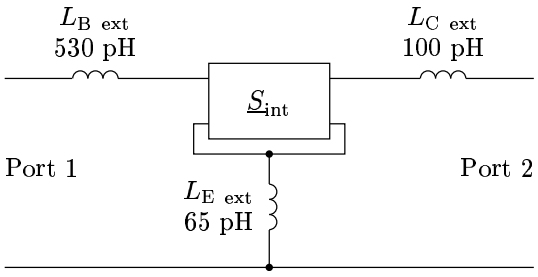


Figure 6.19: Lumped-element model of the off-wafer parasitics

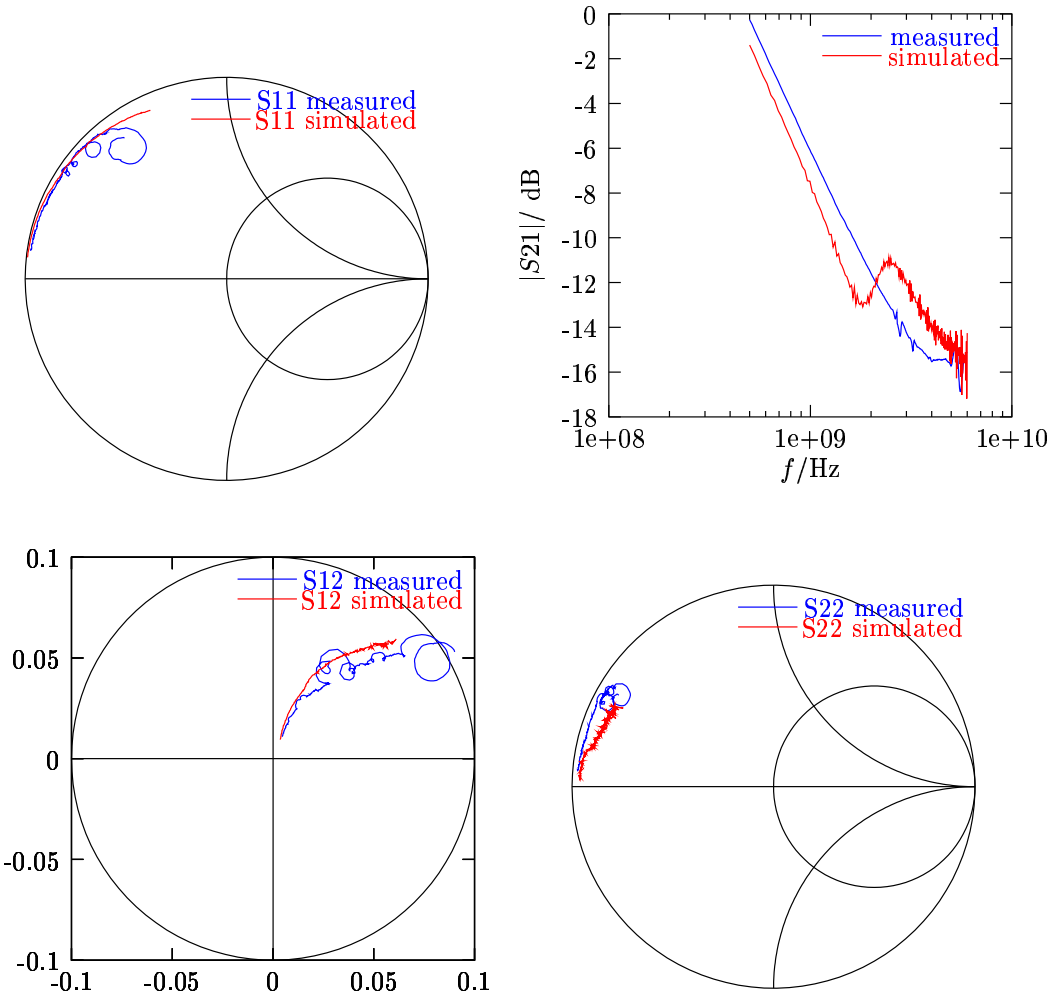


Figure 6.20: S-parameters of the lumped-element model for the off-wafer parasitics of the power HBT mounted on the brass fixture. $V_{\mathrm{CE}} = 1.5$ V, $I_{\mathrm{B}} = 20$ mA

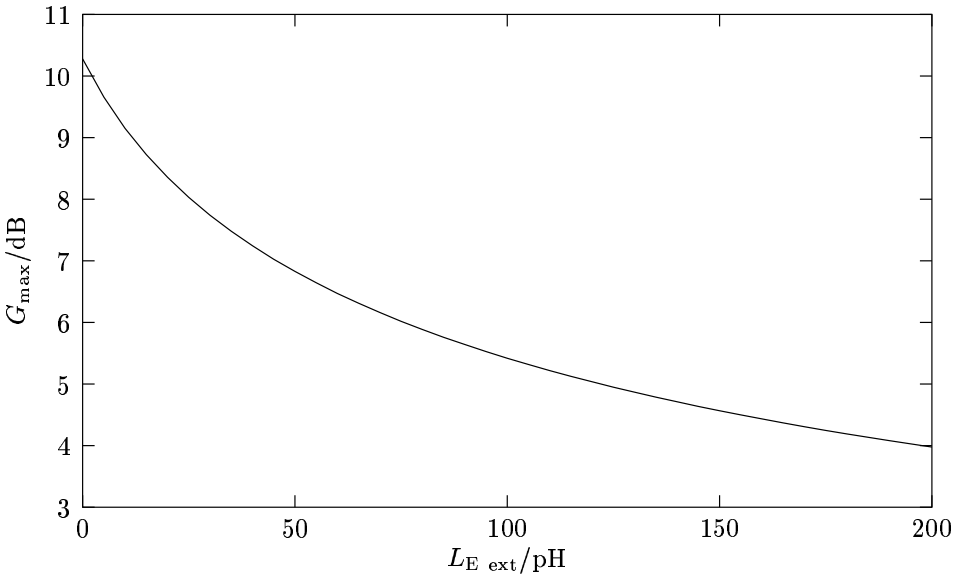


Figure 6.21: G_{max} vs. off-wafer emitter inductivity at 1.75 GHz, $I_B = 20$ mA, $V_{CE} = 1.5$ V

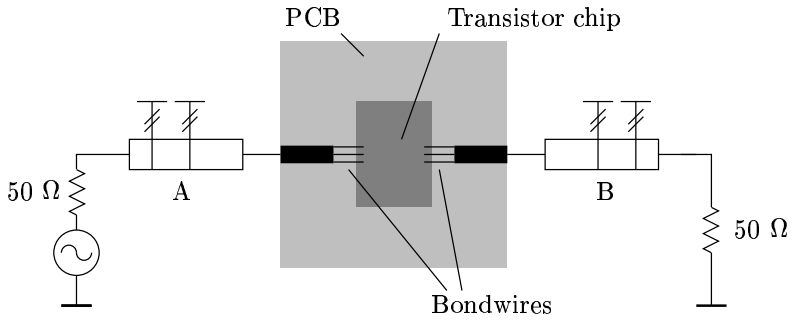
off-wafer emitter resistances, the G_{max} deterioration is not quite as bad: G_{max} is reduced by 1 dB for a resistance of 185 mΩ.

6.3.4 Optimum Source and Load Impedance

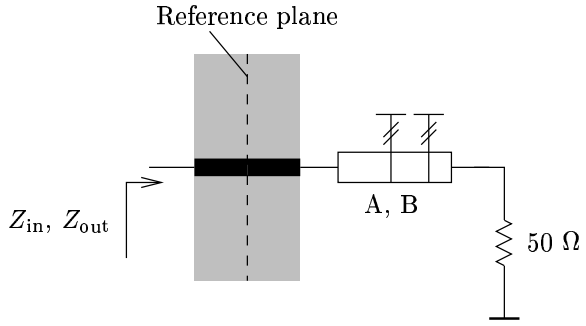
The optimum source and load impedances of the device were measured by attaching tuners to its input and output ports in the test fixture, tuning for maximum output power (as usual, at $I_B = 20$ mA, $V_{CE} = 1.5$ V) as shown in Fig. 6.22(a) and then measuring the respective impedances of the tuners. For this measurement, the PCBs carrying the transistors were replaced with the "Through" element from the calibration kit (see Fig. 6.22(b)), thus the reference planes for the impedance measurements were at the PCB-sided ends of the respective bondwires. The measured impedances are shown in Fig. 6.23.

Assuming that the optimum source and load impedances *at the device* are real-valued, we can get an estimate of the inductance of the bondwires and metallization on the chip at the base L_{src} and collector L_{load}. If an inductance (representing the bondwires) is added in series to the measured impedance Z_{in} to obtain a real-valued impedance,

$$\mathrm{Im}\{Z_{in}\} + \omega L_{src} = 0 \ , \tag{6.11}$$



(a) Tuning for maximum output power



(b) Measurement of the impedances

Figure 6.22: Measurement setup for optimum source and load impedances

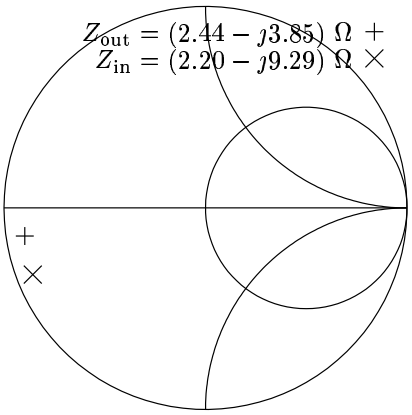


Figure 6.23: Optimum input and output impedances of a power HBT. $V_{\text{CE}} = 1.5$ V, $I_{\text{B}} = 20$ mA, at 1.75 GHz.

we can calculate (with Z_{in} from Fig. 6.23 and $\omega = 2\pi 1.75$ GHz) $L_{\text{src}} = 845$ pH, and similarly $L_{\text{load}} = 350$ pH. The deviation from the values of on- and off-chip inductances from the lumped-element models Fig. 6.11 and 6.19 combined ($L_{\text{B}} + L_{\text{B ext}} = 780$ pH, $L_{\text{C}} + L_{\text{C ext}} = 280$ pH) can be attributed to small shifts in line length during mounting and unmounting the tuners from the fixture.

6.4 Power Amplifier Performance

The power amplifier chips were mounted on a similar brass fixture as the HBT chips (Fig. 6.3 shows a photo of the mounted and bonded power amplifier chip) to have the emitter bondwires as short as possible.

Figure 6.24 shows a single-tone power sweep of the PA with both stages biased to a class A operating point. Gain and output power were improved by increasing V_{CE} in both stages to 2.5 V. The result of a power sweep at this operating point is depicted in Fig. 6.25.

Compared to the simulation results without parasitics the measurement results are disappointing. To verify the parasitics extracted in section 6.3, a simulation with the parasitics shown in Fig. 6.26 was carried out. For the following simulations, parasitics were only added to the power stage. The elements R_{E1}, L_{E1}, R_{E2}, and L_{E2} representing the metallization and bondwires from the emitters to ground were assumed to be equal to the emitter resistances and inductances, respectively, of the HBT mounted to the brass fixture (see Fig. 6.19). R_{E12}, L_{E12} representing the connection

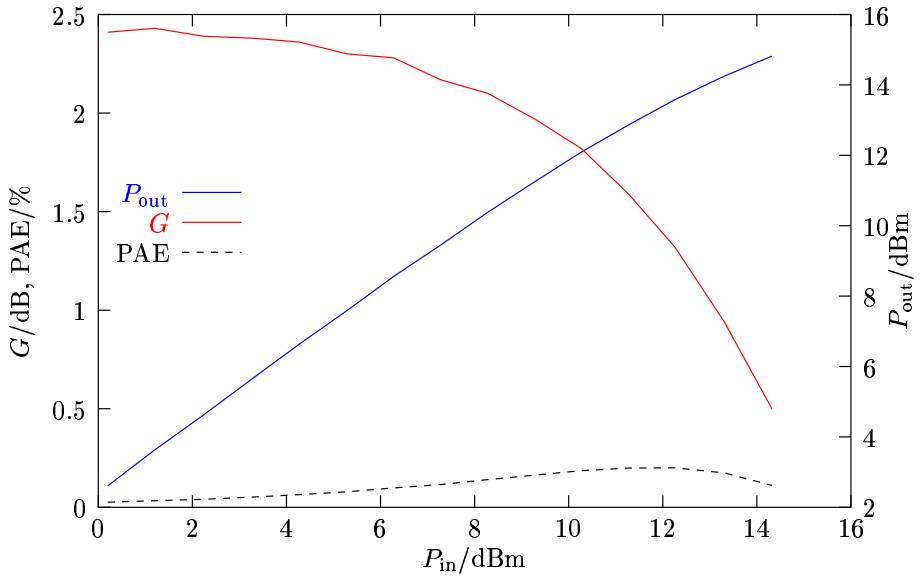


Figure 6.24: PA Power sweep, measured at 1.75 GHz. Driver stage bias: $V_{\text{CE}} = 1.5$ V, $I_{\text{C}} = 0.5A$, power stage bias: $V_{\text{CE}} = 1.5$ V, $I_{\text{C}} = 1.5$ A

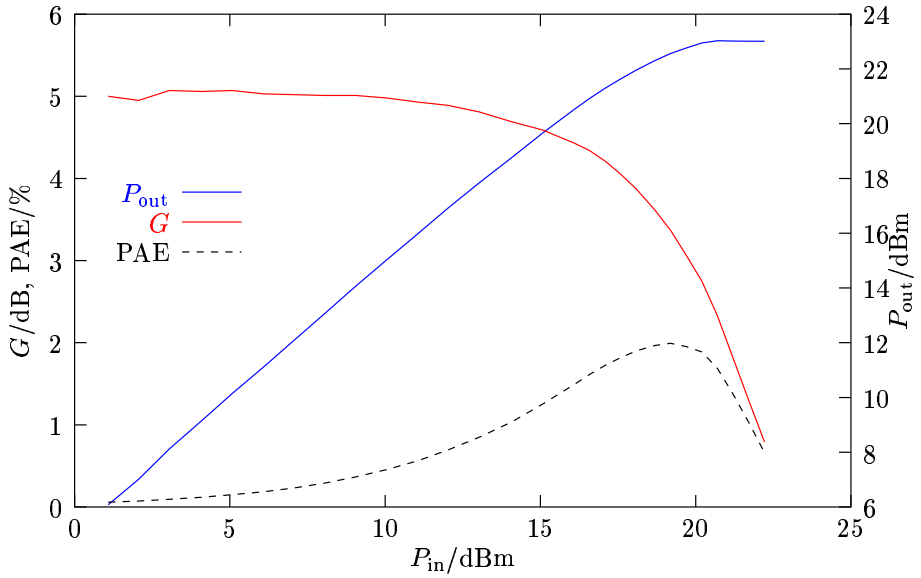


Figure 6.25: PA Power sweep, measured at 1.75 GHz. Driver stage bias: $V_{\text{CE}} = 2.5$ V, $I_{\text{C}} = 0.4$ A, power stage bias: $V_{\text{CE}} = 2.5$ V, $I_{\text{C}} = 1.5$ A

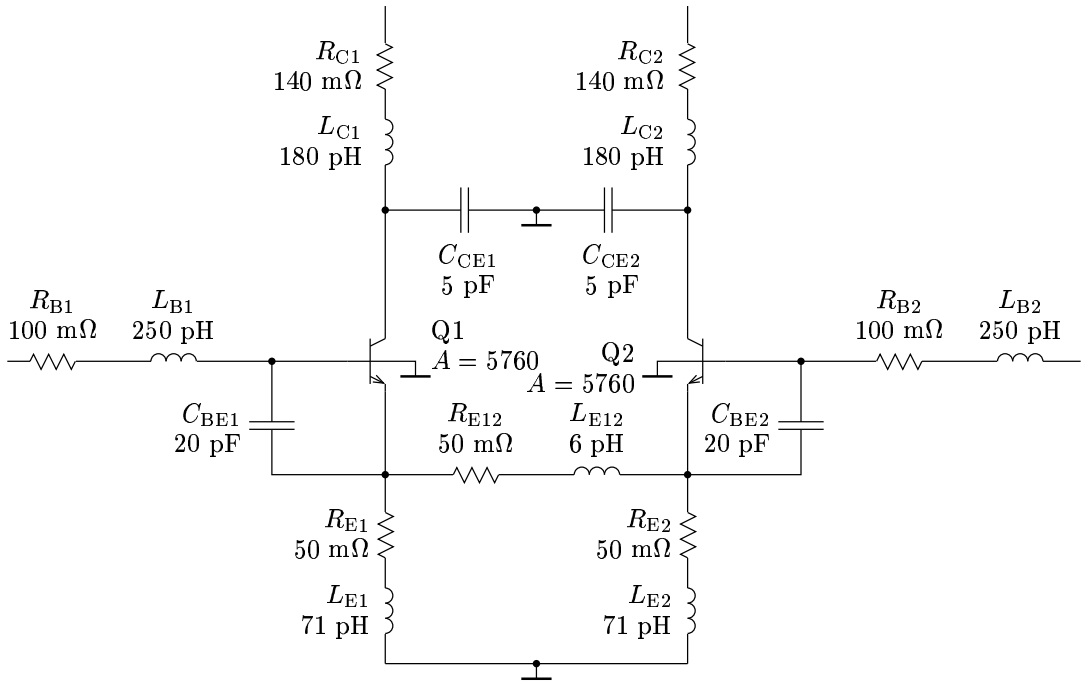


Figure 6.26: Schematic of the lumped-element model of PA parasitics

of the emitters on the chip were modeled as equal to the on-wafer emitter parasitics from on-chip tests (see Fig. 6.11). Simulation results without and with parasitics are shown in Fig. 6.27. In addition, the curves for the PA with only the inductive parasitics, and curves with only the base inductances L_{B1} and L_{B2} are plotted. It can readily be seen that resistances and capacitances have only moderate impact on performance compared to inductivities, and among the inductivities, the base inductivities L_{B1} and L_{B2} have the largest single impact on gain and output power. Fig. 6.28 shows how the output power increases when the base inductances vary. All other parasitics were set to the values given in Fig. 6.26 for this simulation.

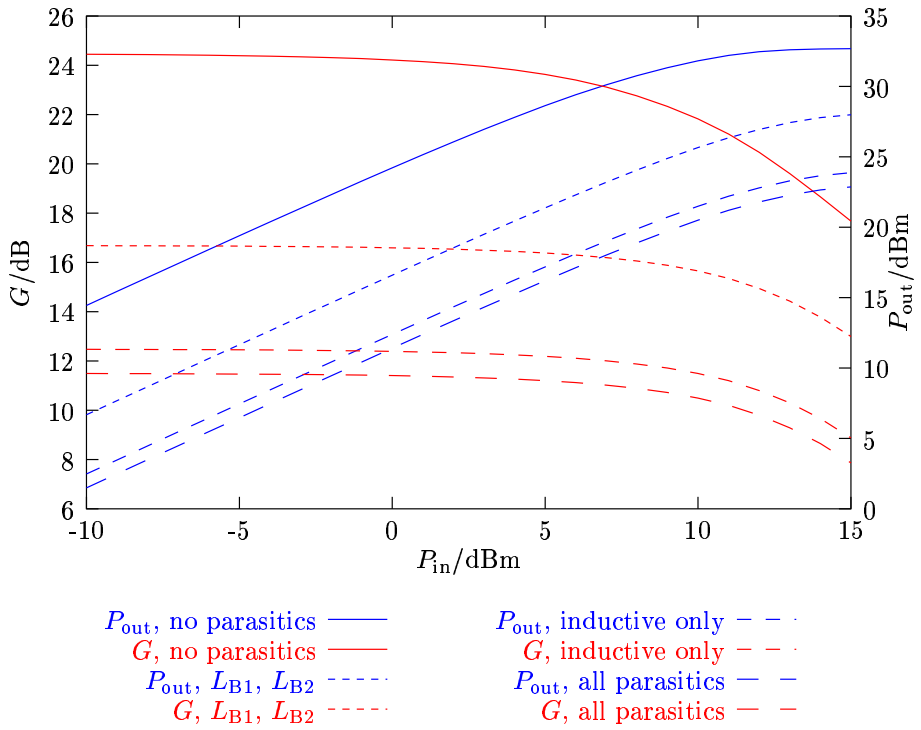


Figure 6.27: PA power sweep, simulation with parasitics

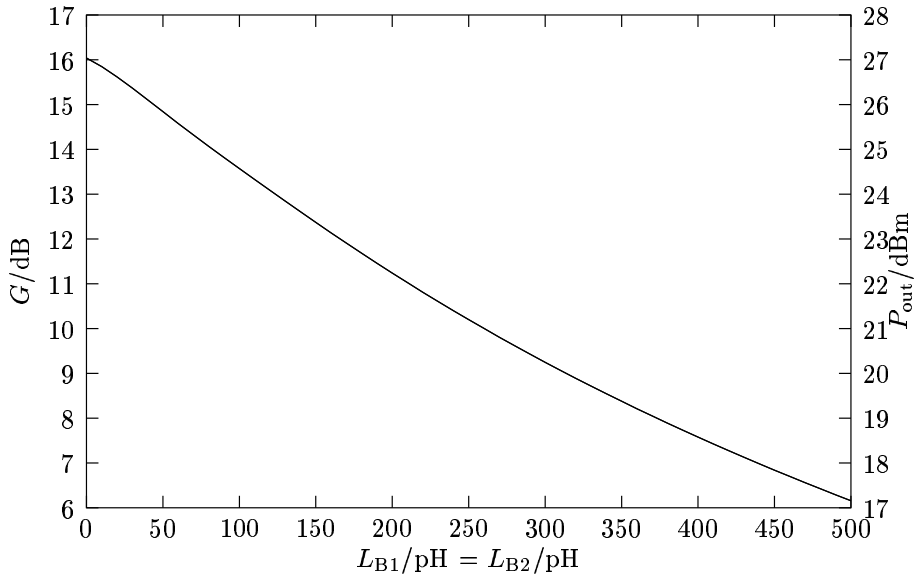


Figure 6.28: PA output power and gain vs. base inductance, at 11 dBm input power

Chapter 7

Outlook and Conclusion

It has been shown that a monolithic integrated power amplifier for EDGE is not feasible with the given fabrication process. The main obstacle was certainly the non-availability of a thick metal layer.

- Some smaller stand-alone HBT devices should be built and characterized. A scalable model for n parallel fundamental cells could then be developed.
- Package selection: Good ground is needed for low-impedance devices. Especially the inductances hurt performance. Another criterion for package selection is the thermal conductivity. The package must have solid metal at its bottom.
- Use thick metal layers to improve the Q of the baluns [16], [15] and significantly reduce the occupied die area. Use only the top metal layer to remove the inductors as far as possible from the substrate.
- Re-assess some design rules, especially the maximum current densities in the metal layers. Experience from some tests shows that the metallization can (at least locally) handle much higher current densities when mounted on a substrate with low thermal resistivity.
- Wafer thinning: Use of an even thinner wafer would be beneficial for the thermal resistance and the length of the emitter bondwires. When inductive components are integrated, a thin wafer can, however, lead to "image currents" in the (highly conductive) package ground under the wafer [13].
- Use a smaller transistor: a smaller device would have input and output impedances which are a bit higher. Parasitic inductances would have

less impact, which would surely be desirable, while the greater impact of parasitic capacitances would be tolerable.

- Significant improvements in the RF performance of HBTs have been obtained by varying the DC resistance of the base bias source [19]. The influence of the DC resistance of the bias current or voltage source should be examined.

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