DISSERTATION

Heterogeneously Integrated 8×10 Gbps Optical Receiver

ausgeführt zum Zwecke der Erlangung des akademischen Grades
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Kurzfassung

Die vorliegende Dissertation beschreibt die Entwicklung eines 8×10 Gbps optischen Empfängers, der für die Verwendung von heterogen integrierten Ge und InP/GaAs Photodioden optimiert wurde. Der Empfänger basiert auf einer 0.35 μm SiGe BiCMOS Technologie von Austriamicrosystems. Der Vorteil der heterogenen Integration optischer Komponenten gegenüber herkömmlichen Verbindungstechniken (Bonden mit dünnen Golddrähten) liegt vor allem in kleineren parasitären Kapazitäten bzw. Induktivitäten. Um die heterogen integrierten Photodetektoren mit konventionell gebondeten Photodioden vergleichen zu können, wurde eine Empfängerversion produziert deren Verstärkung einstellbar ist. Damit ist es möglich den Empfänger an verschiedene Diodentypen anzupassen. Die verwendeten Photodioden wurden von CEA-LETI und IMEC, zwei Projektpartnern des HELIOS Projekts der Europäischen Gemeinschaft (FP7 224312), zur Verfügung gestellt. Die Detektoren von CEA-LETI basieren auf Ge und werden mit dem CMOS Chip in einem Verfahren das 'wafer-to-wafer bonding' genannt wird verbunden. Dabei werden, nachdem der optische Wafer mit dem CMOS Wafer verbunden wurde, durch den optischen Wafer Durchkontaktierungen erzeugt die bis zum CMOS Wafer reichen. Diese Durchkontaktierungen stellen die Verbindung zwischen optischen und CMOS Wafer her. Im Gegensatz dazu basieren die von IMEC produzierten Dioden auf InP/GaAs. Diese Dioden werden mittels eines Verfahrens, das sich 'die-to-wafer bonding' nennt, mit dem CMOS Wafer verbunden. In diesem Verfahren ist der optische Wafer deutlich dicker und beinhaltet schon vor der Verbindung mit dem CMOS Wafer Durchkontaktierungen aus Kupfer ("copper nails"). Der optische Wafer wird dann mit kleinen Indium-Kupferkugeln an jeder Verbindungsstelle mit dem CMOS Wafer verbunden. Das optische Signal wird bei beiden Diodentypen mittels Gitterkoppler und Wellenleiter in die Diode eingekoppelt. Um die heterogen integrierten Photodioden mit herkömmlich gebondeten Dioden vergleichen zu können, wurden von CEA-LETI auch verschiedenste vertikale Ge Photodioden zur Verfügung gestellt. Diese wurden mittels konventioneller Verbindungstechnik (Drahtbonden) mit der CMOS Schaltung verbunden.

Im ersten Schritt wurden die unterschiedlichen Photodioden charakterisiert. Danach wurden basierend auf den Messdaten Simulationsmodelle der einzelnen Dioden und ihrer Verbindungsstrukturen entwickelt. Diese Modelle bilden die Grundlage der Entwicklung und Optimierung der Eingangsstufe des Empfängers. Der Empfänger ist für eine Versorgungsspannung von 3.3 V ausgelegt und besteht aus acht identen Kanälen von denen jeder eine maximale Datenrate von 10 Gbps besitzt. Jeder Kanal des Empfängers ist differenziell aufgebaut und besteht aus einem Transimpedanzverstärker (TIA) gefolgt

von zwei limitierenden Verstärkerstufen und einer 50 Ω CML Ausgangstreiberstufe. Erst der differenzielle Aufbau ermöglicht eine optimale Gleichtaktunterdrückung, garantiert eine hohe Immunität gegen Versorgungsspannungsschwankungen und hilft Temperaturschwankungen und Prozesstoleranzen zu minimieren. Im Detail basiert die Eingangsstufe auf einem einfachen Transimpedanzverstärker ("single-ended") der mit Hilfe eines weiteren Transimpedanzverstärkers ('dummy TIA') zu einem differenziellen System erweitert wird. Zusammen mit einem Operationsverstärker zur Offset-Kompensation, erzeugt die kombinierte Eingangsstufe das differenzielle Signal für die nachfolgenden Schaltungsteile. Um den Verstärker mit den verschiedenen Diodenarten verwenden zu können, wurden zwei verschiedene Versionen realisiert. Eine Version wurde für heterogen integrierte Photodioden optimiert während die zweite Version für die Verwendung mit konventionell gebondeten Photodioden angepasst wurde.

Unglücklicher Weise hatten sowohl CEA-LETI als auch IMEC schwerwiegende Probleme mit der heterogenen Integration der optischen Bauteile. Daher konnte keiner der Projektpartner einen heterogen integrierten Testchip herstellen. Der Empfänger wurde deshalb nur mit herkömmlich gebondeten Photodioden vermessen. In Kombination mit einer externen Photodiode mit 300 fF Kapazität erreicht der Verstärker eine Transimpedanz von 125 kΩ bei einer maximalen Bitrate von 10 Gbps. Bei einer Versorgungsspannung von 3.3 V verbraucht der Empfänger 1,29 W und der differenzielle Ausgangsspannungshub beträgt 800 mVpp an einer 50 Ω Last. Mit einem PRBS31 Bitmuster und einer Photodiodenempfindlichkeit von 0,5 A/W weist der Verstärker eine Empfindlichkeit von -20 dBm bei einer Bitfehlerrate von 10^{-9} beziehungsweise -18.8 dBm bei einer Bitfehlerrate von 10^{-12} auf. Zieht man dabei die relativ niedrige Photodiodenempfindlichkeit von nur 0,5 A/W in Betracht, so könnte die Empfindlichkeit des Verstärkers durch Verwendung eines dem Stand der Technik entsprechenden Photodetektors mit einer Empfindlichkeit von 1 A/W um -3 dB verbessert werden. Zusätzlich ließe sich die Verstärkerempfindlichkeit durch die heterogene Integration der Photodiode um weitere -3 dB vergrößern. Insgesamt könnte dadurch die Empfindlichkeit des Verstärkers auf bis zu -26 dBm gesteigert werden.

Abstract

This PhD thesis focuses on the development of an 8×10 Gbps optical receiver, fabricated in austriamicrosystems 0.35 μm SiGe BiCMOS technology for use with heterogeneously integrated Ge and InP/GaAs photodiodes on top of the CMOS wafer. The heterogeneous integration of the photodetectors promises lower parasitic capacitances and inductances than conventional wire bonding. To compare this novel interconnection method with conventional wire bonded photodetectors the receiver was designed with variable transimpedance to make the usage of various external photodiode types also possible. The photodetectors are fabricated by CEA-LETI and IMEC, two project partners of the European Community project HELIOS (FP7 224312). The photodiodes fabricated by CEA-LETI are based on Ge and integrated on top of the CMOS chip by wafer-to-wafer bonding using subsequent through silicon vias (TSV). The detectors fabricated by IMEC are based on InP/GaAs and use die-to-wafer bonding and Cu filled TSVs to connect the photonic die to the CMOS wafer. Both detector types use grating couplers and waveguides to couple the optical signal into the diode. To compare the heterogeneous integration of the photodetectors with conventional wire bonding CEA-LETI also provided various vertical Ge photodiodes with bond pads.

The different diode types are characterized and based on the measurement results models of the various detectors and connection structures are developed. These models are used for all simulations during the design of the receiver. The receiver itself is designed for a supply voltage of 3.3 V and consists of eight identical amplifier channels, each capable of 10 Gbps maximum data rate. It is based on a fully differential structure and is built up of a transimpedance amplifier (TIA) followed by two limiting amplifier stages and a 50 Ω CML-style output buffer. The fully differential structure is chosen to minimize the influence of common mode disturbances, temperature effects and process tolerances. Due to the fact that the TIA itself is single-ended while the following stages are built up fully differential, a dummy TIA and an operational amplifier, which works as offset compensation, are used to provide the differential input signal for the following limiting amplifier. To adapt the amplifier to the different photodiode types, two different versions were fabricated. One version that is optimized to take full advantage of the heterogeneous integrated photodetectors and a second version which was optimized for use with various wire bonded photodiode types.

Unfortunately CEA-LETI as well as IMEC had substantial problems with the heterogeneous integration of the photodiodes on top of the CMOS wafer. Therefore no het-

erogeneous integrated demonstrator chips were available for characterization. Together with a conventional wire bonded vertical Ge photodiode with a capacitance of 300 fF the achievable total transimpedance is 125 kΩ at a bit rate of 10 Gbps. The total power consumption is 1.39 W at a supply voltage of 3.3 V. The measured differential output voltage swing is 800 mVpp at a load of 50 Ω. At a data rate of 10 Gbps, a PRBS31 test pattern and a photodiode responsivity of 0.5 A/W a sensitivity of −20 dBm (BER = 10^{-9}), respectively −18.8 dBm (BER = 10^{-12}) is reached. Taking into account the relative low responsivity of the used photodetector, a sensitivity improvement of −3 dB can be expected if a photodiode with a state-of-the-art responsivity of around 1 A/W would be used. In addition simulations showed that the heterogeneous integration of the photodetector would increase the receiver sensitivity by further −3 dB. Therefore sensitivities of around −26 dBm would be reached by using heterogeneously integrated photodiodes with state-of-the-art responsivities of 1 A/W.

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Last but not least, I would express my gratitude to my parents for their support and patience.

Contents

Abbreviations

Abbreviation	Description
AC	Alternate current
Al	Aluminum
ARC	Anti reflection coating
Au	Gold
AWG	Arrayed waveguide grating
BCB	Benzocyclobutene
BER	Bit error rate
BiCMOS	Bipolar complementary metal oxide semiconductor
CEA	Commissariat à l'énergie atomique et aux énergies alternatives
CML	Current mode logic
CMOS	Complementary metal oxide semiconductor
CMP	Chemical mechanical polishing
Cu	Copper
CW	Continuous wave
DSA	Digital signal analyzer
DC	Direct current
DUT	Device under test
FOM	Figure of Merit
GaAlAs	Gallium-Aluminum-Arsenide
GaAs	Gallium-Arsenide
Gbps	Gigabits per second
Ge	Germanium
GSG	Ground-signal-ground
HBT	Heterojunction bipolar transistor
HELIOS	pHotonics ELectronics functional Integration on CMOS
IC	Integrated circuit
III–V	Group III–V compound semiconductors
IMEC	Interuniversity microelectronics centre
InAs	Indium-Arsenide
InGaAs	Indium-Gallium-Arsenide
InP	Indium-Phosphide
LED	Light emitting diode
LETI	Laboratoire d'electronique des technologies de l'information

Abbreviation	Description
MOS	Metal oxide semiconductor
MOSFET	Metal oxide semiconductor field effect transistor
OEIC	Optoelectronic integrated circuit
OP-AMP	Operational amplifier
PCB	Printed circuit board
PD	Photodiode
PIN diode	Positive intrinsic negative diode
PM	Polarization maintaining
PRBS	Pseudo-random bit stream
S11	Scatter parameter: Input return loss
S21	Scatter parameter: Gain
SCR	Space-charge region
SiC	Silicon-Carbide
SiGe	Silicon-Germanium
SiO_2	Silicondioxide
SMA connector	SubMiniature version A connector
SNR	Signal-to-noise ratio
SOI	Silicon on insulator
TE mode	Transversal electric mode
TM mode	Transversal magnetic mode
TIA	Transimpedance amplifier
TSV	Through silicon via
VNA	Vector network analyzer
WDM	Wavelength division multiplexing

List of Symbols

Symbol	Description	Units
A	Area	μm
$A(\omega)$	Frequency dependent gain	
A_0	Low-frequency open-loop gain	
B	Bit rate	bit/s
BW	Bandwidth	Hz
c	Speed of light in a medium	m/s
c_0	Speed of light in vacuum	m/s
C_{con}	Connection structure capacitance	F
C_{fb}	Feedback capacitance	F
C_{limit}	Limiting capacitance	F
C_p	Photodiode capacitance	F
C_{pad}	Pad capacitance	F
$C_{parasitic}$	Parasitic capacitance	F
C_T	Input node capacitance	F
C_{TSV}	TSV capacitance	F
C_π	Base-emitter capacitance	F
d_1	Inner diameter of TSV	μm
d_2	Outer diameter of TSV	μm
d_{ARC}	Thickness of antireflecting coating	μm
d_g	Pitch of arrayed waveguide grating	nm
d_I	Thickness of intrinsic region	μm
D_n	Diffusion coefficient of electrons	cm^2/s
D_p	Diffusion coefficient of holes	cm^2/s
D_t	Decision threshold of photocurrent	A
E	Photon energy	eV
$\boldsymbol{E}$	Electric field	eV
E_g	Bandgap Energy	eV
f_{-3dB}	-3 dB cutoff frequency	Hz
g_m	Transconductance	A/V
G	Generation rate	cm^{-3}
h	Planck constant	6.626×10^{-34} Js
$\langle i_0 \rangle$	Discrete photocurrent representing logical zero	A

Symbol	Description	Units
$\langle i_1 \rangle$	Discrete photocurrent representing logical one	A
i^2	Noise current spectral density	A^2/Hz
$\overline{i^2}$	Mean-square noise current	A^2
$\overline{i_{amp}^2}$	Mean-square equivalent amplifier input noise current	A^2
$\overline{i_b^2}$	Mean-square base noise current	A^2
i_{bn}^2	Mean-square burst noise current density	A^2/Hz
$\overline{i_{bn}^2}$	Mean-square burst noise current	A^2
$\overline{i_c^2}$	Mean-square collector noise current	A^2
$\overline{i_{in}^2}$	Mean-square equivalent input noise current	A^2
i_{fn}^2	Flicker noise current density	A^2/Hz
$\overline{i_R^2}$	Mean-square feedback resistor noise current	A^2
i_{sn}^2	Shot noise current density	A^2/Hz
$\overline{i_{sn}^2}$	Mean-square shot noise current	A^2
i_{th}^2	Thermal noise current density	A^2/Hz
$\overline{i_{th}^2}$	Mean-square thermal noise current	A^2
in^+	+ input differential amplifer	
in^-	− input differential amplifer	
I	Current	A
I_B	Base current	A
I_C	Collector current	A
I_D	Drain current	A
I_{dark}	Dark current	A
I_{diff}	Output buffer current	A
I_{ph}	Photocurrent	A
k_B	Boltzmann constant	1.381×10^{-23}
L	Length	μm
L_{bond}	Bond wire inductance	H
$L_{parasitic}$	Parasitic inductance	H
m	Order of diffraction	
$\overline{n}$	Refractive index	
$\overline{n_{ARC}}$	Refractive index of antireflecting coating	
$\overline{n_c}$	Refractive index of star coupler	
$\overline{n_g}$	Refractive index of arrayed grating waveguide	
$\overline{n_s}$	Refractive index of surroundings	
$\overline{n_{sc}}$	Refractive index of semiconductor	
N_A	Acceptor concentration	cm^{-3}
N_D	Donor concentration	cm^{-3}
$N_{A/D}$	Doping concentration low dopded side of pn junction	cm^{-3}
$p_0(i)$	Probability density for a logical zero	

Symbol	Description	Units
$p_1(i)$	Probability density for a logical one	
P_{opt}	Incident optical power	W
q	Elementary charge	1.602×10^{-19} As
Q	Q-factor	
R	Responsivity	A/W
$\overline{R}$	Reflectivity	
r_b	Base series resistance	Ω
r_o	Small signal output resistance	Ω
r_{pi}	Base-emitter resistance	Ω
R_c	Load resistance	Ω
R_{fb}	Feedback resistance	Ω
R_{in}	Input resistance	Ω
R_{load}	Output load resistance	Ω
R_p	Parallel resistance	Ω
R_s	Series resistance	Ω
R_{Si}	Series resistance of Si substrate	Ω
R_{term}	Termination resistance	Ω
RF_{in}	RF input signal	
t_f	Fall time	s
t_r	Rise time	s
T	Absolute temperature	K
$T_1 - T_8$	Bipolar transistor	
$T_{I1} - T_{I7}$	MOSFET	
T_{Iref}	Current reference MOSFET	
$T(j\omega)$	Frequency-dependent transimpedance of a TIA	Ω
T_t	Time slot	s
$\overline{v_{amp}^2}$	Mean-square equivalent amplifier input noise voltage	V^2
$\overline{v_b^2}$	Mean-square base noise voltage	V^2
$\overline{v_{in}^2}$	Mean-square equivalent input noise voltage	V^2
v_{th}^2	Thermal noise voltage density	V^2/Hz
$\overline{v_{th}^2}$	Mean-square thermal noise voltage	V^2
v_n	Electron velocity	cm^{-2}
v_p	Hole velocity	cm^{-2}
V	Voltage	V
V_+	Supply voltage	V
V_{bias}	Bias voltage	V
V_{gc}	Gain control voltage	V
V_{pp}	Peak-to-peak voltage	V
x	x-coordinate	μm
y	y-coordinate	μm

Symbol	Description	Units
z	z-coordinate	μm
α	Absorption coefficient	μm^{-1}
α_{Ge}	Thermal expansion coefficient of Ge	K^{-1}
α_{Si}	Thermal expansion coefficient of Si	K^{-1}
β	Common-emitter current gain	
ϵ_0	Vacuum permittivity	F/m
ϵ_r	Relative permittivity	
η	External quantum efficiency	%
η_i	Internal quantum efficiency	%
η_o	Optical quantum efficiency	%
Φ	Photon flux density	$\text{cm}^{-2}\text{s}^{-1}$
$\overline{\kappa}$	Extinction coefficient	
λ	Wavelength in a medium	nm
λ_0	Wavelength in vacuum	nm
λ_c	Wavelength corresponding to E_g	nm
μ	Mobility	cm^2/Vs
μ_n	Electron mobility	cm^2/Vs
μ_p	Hole mobility	cm^2/Vs
ν	Frequency of light	Hz
τ_n	Electron lifetime	s
τ_p	Hole lifetime	s
ω	Angular frequency	s^{-1}
ω	$2{\cdot}\pi \cdot f_{-3dB}$	s^{-1}
Θ_{in}	Couple angle	$^\circ$

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1 Introduction

1.1 Motivation

Optical interconnection technology is a fast growing sector in the global economy. Optical data transmission, optical storage, imaging, optical sensors and lightning are only a few samples. High bandwidth, low propagation losses, immunity to electromagnetic fields, wavelength multiplexing and reduced crosstalk are just a few benefits of optical interconnects. Even if photonics offers a wide range of new functionalities to electronic components the high costs of fast photonic components and their assembly are major obstacles to their deployment in most application fields.

Classic approaches to solve this problem are the monolithic integration of III–V photonic devices (e.g. photodetectors, sources, modulators, ...) together with electronic circuits based on GaAs substrate [13] or the use of cheap, standard CMOS electronics with external, wire bonded III–V or Ge photonic devices [14]. III–V photonic components and electronic circuits which are implemented on GaAs are fast but their high costs are major obstacles for mass production. The use of standard CMOS circuits together with external wire bonded Ge or III–V photonic components is cheaper but has significant disadvantages concerning mechanical and electrical performance. On one hand the thin bond wires are sensitive to mechanical stress and on the other hand the bandwidth is limited by the additional pad capacitances and the bond wire inductances. Other problems are the increased cross talk between neighboring channels [15] and the additional die area needed by the bond pads.

Nevertheless it is important to develop fast optical components in a much more compact and cost-effective way by integrating photonic and electronic components into a single chip. Till now the cost-effective photonic-electronic integration is hindered by the large amount of different photonic devices and technologies and the fact that most integration technologies are application specific. Thus the market for integrated photonics is too fragmented to justify the investments for designing one integration technology to a level which really leads to substantial cost reductions.

One way to solve this problem is to combine cost-effective standard CMOS technology with heterogeneously mounted photonics directly on the CMOS wafer using microelectronics fabrication processes. The aim is to develop a small set of elementary components with a level of functionality that covers a wide range of applications and opens new opportunities

for a much larger deployment of photonic ICs. Due to the fact that single components (e.g. source, receiver, modulator, ...) will have negligible costs, the desired functionality can be realized by using as many components as needed. Another benefit of co-integrating photonics and electronics on a single chip is the option of fabricating high functionality, high performance and highly integrated devices using a well mastered microelectronic fabrication process.

Nevertheless there are still many challenges and issues to be considered until heterogeneous mounted photonics on standard CMOS can be brought at a mature industrial level [16]:

- The performance of optical functions has to comply with the application requirements.
- The structure of costs of photonic and electronic components has to be similar (e.g. packaging costs lower than chip costs).
- Photonics integration has to be straightforward for IC designers and manufacturers. CMOS compatibility is mandatory as well as the creation of design tools and libraries compatible with IC standards.

Consequently an integrated design and a fabrication chain using standard and generic processes has to be developed.

1.2 Problem Definition and Objectives

This PhD thesis focuses on the design of an 8×10 Gbps transimpedance amplifier, fabricated in a standard 0.35 μm SiGe BiCMOS process for use with conventional wire bonded photodiodes on one hand and heterogeneously integrated photodiodes on the other hand. The used photodiodes are provided by IMEC and CEA-LETI, two project partners of the European Community project HELIOS (FP7 224312). The photodetectors developed by IMEC are based on InP/InGaAs and use Cu filled through silicon vias (TSV) and die-to-wafer bonding for the integration on the CMOS wafer. The diodes manufactured by CEA-LETI are based on Ge and are integrated on the CMOS wafer using wafer-to-wafer bonding with subsequent TSVs and photonic processing. To compare these novel integration strategies with conventional wire bonding, standard Ge photodiodes are also connected by conventional wire bonding to the CMOS wafer.

The aim of this work is to design a high sensitivity 8×10 Gbps parallel optical receiver which can be used with different kinds of photodiodes and integration strategies. Therefore in a first step the photodiodes have to be characterized and models of the relevant parasitics of the photodetectors itself and the different connection types (wire bonding, die-to-wafer bonding and wafer-to-wafer bonding) have to be developed. Based on these models a parallel 8-channel optical receiver with maximum sensitivity shall be designed. Each channel should be capable to drive a differential 100 Ω load or respectively two 50 Ω

loads at a data rate of 10 Gbps. To adapt the receiver to the different photodiodes and connection structures, the gain of the TIA stage has to be variable. In a last step the whole receiver chain (photodetector, connection structure and transimpedance amplifier) will be characterized and the different realization strategies will be compared.

2 Optical Fiber Receiver

In general optical fiber receivers are used to convert the light-wave signal, coming from an optical fiber, from the optical to the electrical domain. A block diagram of a typical optical fiber receiver is shown in Fig. 2.1.

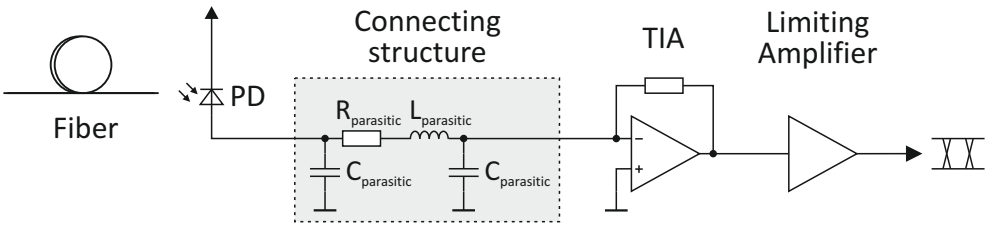


Figure 2.1: Block diagram of optical fiber receiver

The photodiode (PD) collects the light leaving the fiber and generates a photocurrent in response to the optical excitation. Depending on the used wavelength Si, Ge or III–V photodetectors are used. Typically the generated electrical signal is low-level and needs amplification and signal processing to recover the transmitted information. The connection between the photodiode and the amplifier is established either by bond wires, heterogeneous integration or monolithic integration. To reach high bandwidth and high sensitivity it is important to keep the parasitics of the connection structure as small as possible. Then the generated photocurrent is amplified and converted into a voltage by the preamplifier, which is usually realized by a transimpedance amplifier (TIA). In the next step the voltage signal is amplified further by the limiting amplifier. The limiting amplifier typically consists of one or more gain stages and an output driver stage which is capable of driving the following clock and data recovery circuits.

In the following sections each part of the optical fiber receiver, shown in fig. 2.1, is described in detail.

2.1 Photodetectors

The first element of an optical fiber receiver is the photodetector. It converts the optical signal into a photocurrent. Thus the performance of the optical receiver depends strongly

on the characteristics of the used photodiode. Its main properties are quantum efficiency, speed, capacitance and leakage current. This chapter starts with a brief introduction to the basics of optical absorption, discusses the main photodetector properties, describes the functionality of the PIN photodiode and closes with a selection of semiconductor materials used for typical telecom applications. Further literature concerning fundamental semiconductor theory and optoelectronics can be found in [1, 3, 8].

2.1.1 Basics of Optical Absorption

The smallest known unit of light is called photon. It is a massless quantum-mechanical particle which is used to characterize electromagnetic radiation from the far infrared to the extreme ultraviolet spectrum. The velocity c and the wavelength λ of a photon depend on the optical index of refraction $\overline{n}$ of the ambient medium (2.1) [3].

$$c = \frac{c_0}{\overline{n}} \tag{2.1}$$

$$\lambda = \frac{c}{\nu} = \frac{c_0}{\overline{n}\nu} \tag{2.2}$$

On the other hand the frequency ν of a photon is the same in vacuum ($\overline{n} = 1$) and in a medium ($\overline{n} > 1$). Thus the wavelength λ in a medium is shorter than the vacuum wavelength λ_0. As consequence light emitting diodes (LED) or laser sources are characterized by their vacuum wavelength (2.2).

Another way to characterize photons is to describe them by their energy E. The energy E of a photon only depends on its vacuum wavelength λ_0 (2.3) [3].

$$E = \frac{h}{\nu} = \frac{hc}{\lambda} = \frac{hc_0}{\lambda_0} \tag{2.3}$$

(2.3) allows to calculate the boundary wavelength of semiconductor materials. If the photon energy E is larger than the bandgap energy E_g of the semiconductor material, the photon energy E can be transferred to an electron in the valence band and the electron moves to the conduction band. The photon is absorbed and an electron-hole pair is generated. If the energy of the photon is smaller than E_g it cannot be absorbed and no electron-hole pair is generated. Therefore the semiconductor material is transparent for light with wavelengths longer than the boundary wavelength λ_c (2.4) [3].

$$\lambda_c = \frac{hc_0}{Eg} \tag{2.4}$$

The absorption process of light in a semiconductor material can be described by Lambert-Beer's law (2.5).

$$P_{opt}(z) = P_{opt}(0)e^{-\alpha z} \tag{2.5}$$

In (2.5) the z-axis describes the vertical penetration depth into the semiconductor material having its origin at the semiconductor surface. The absorption coefficient α is the most important optical constant for semiconductor photodetectors. It determines how far light of a particular wavelength penetrates into a semiconductor until it is absorbed. Fig. 2.2 shows the absorption coefficient of the most important semiconductor materials [17]. The absorption coefficient α strongly depends on the semiconductor material and the

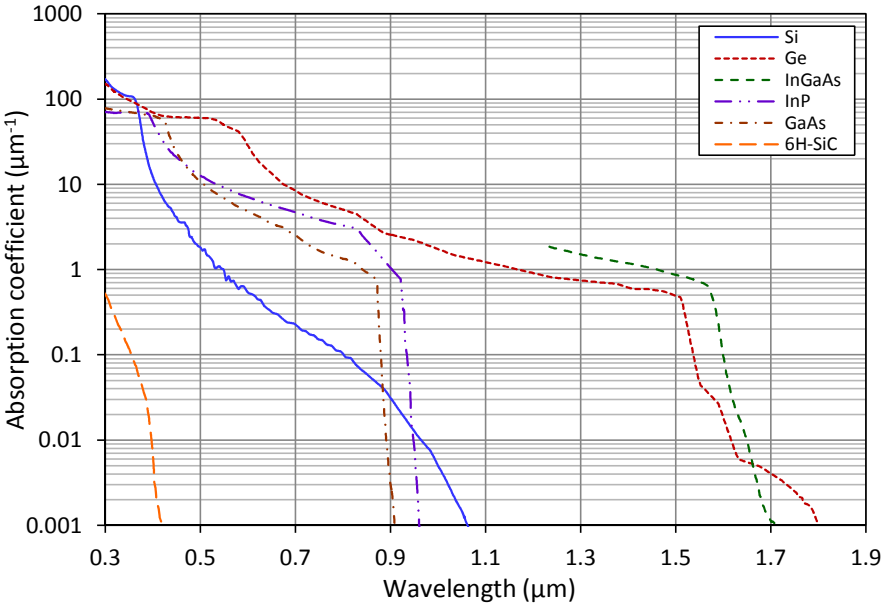


Figure 2.2: Absorption coefficient of important semiconductor materials

wavelength. Light with wavelengths longer than the boundary wavelength λ_c has not sufficient energy to move an electron from the valence band to the conduction band. Thus the absorption coefficient is zero for wavelengths longer than λ_c. For wavelengths shorter than λ_c the absorption coefficient increases rapidly to the so-called *fundamental absorption*.

The direct semiconductors GaAs and InP have high absorption coefficients in the visible and near infrared spectrum. Silicon, on the other hand, is an indirect semiconductor and its absorption coefficient is one to two magnitudes lower in this range. Nevertheless Si is the economically most important semiconductor and thus it is worth to investigate in Si photodetectors in spite of the non-optimum optical properties. The widest wavelength range is covered by Ge and InGaAs including the wavelengths 1.3 μm and 1.55 μm which are used widely for long distance optical data transmission over glass fiber.

2.1.2 Carrier Drift and Minority Carrier Diffusion

One of the main properties of photodetectors, their speed, depends strongly on carrier drift and minority carrier diffusion. As mentioned before the absorbed light generates electron-hole pairs inside the semiconductor if the photon energy E of the incident light is larger than the bandgap energy E_g of the semiconductor material. The generation rate per volume $G(z)$ can be calculated by equation (2.6) [3].

$$G(z) = \frac{\alpha P_{opt}(0)}{Ahc} e^{-\alpha z} \tag{2.6}$$

The simplest photodiode is a reverse biased pn junction. It consists of a heavily doped p^+ region below the surface and a lower doped n region in the depth of the semiconductor. Due to the reverse biasing a space-charge region (SCR) with a considerable electric field is formed while there is no electric field in the regions outside the space-charge region (fig. 2.3). If light penetrates the semiconductor, electron-hole pairs are generated in all depths of the semiconductor dependent on the wavelength of the incident light.

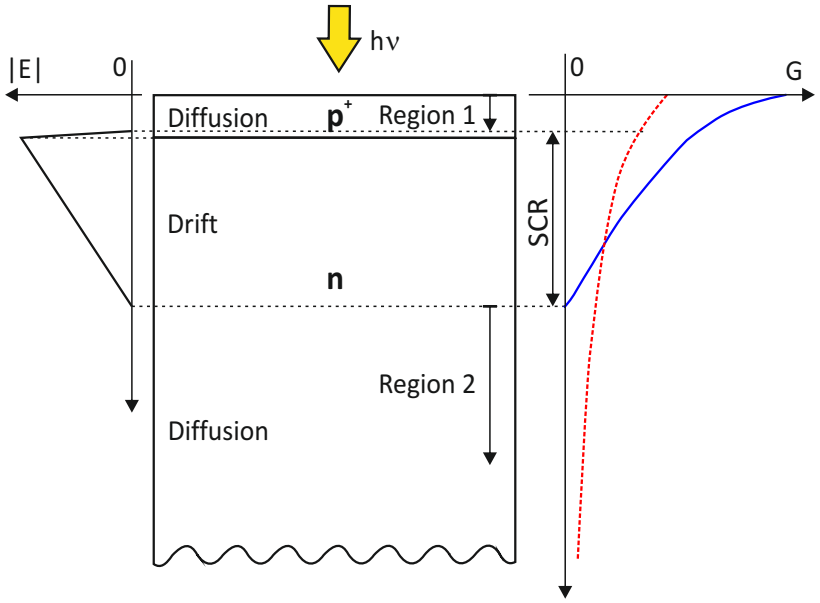


Figure 2.3: Drift and diffusion regions in a photodiode [1]

Carrier drift occurs if the electron-hole pairs are generated inside the space-charge region (drift region) (fig. 2.3). Due to the electric field inside the SCR the electrons are drifting towards the cathode with the velocity v_n while the holes are drifting towards the anode with the velocity v_p. On one hand their velocities depend on the carrier mobilities of the

electrons μ_n and the holes μ_p and on the other hand on the electric field $\boldsymbol{E}$ inside the space-charge region (2.7).

$$v_n = \mu_n \boldsymbol{E}, \qquad v_p = \mu_p \boldsymbol{E} \tag{2.7}$$

The carrier mobilities depend on the semiconductor material, the doping concentration and the electric field. Tab. 2.1 shows the electron and hole mobilities of different semiconductors [18].

Table 2.1: Electron and hole mobilities of different semiconductors

Semiconductor		Mobility at 300 K (cm^2/Vs)	
		μ_n	μ_p
Si	Silicon	1450	500
Ge	Germanium	3900	1900
GaAs	Gallium arsenide	8000	400
InAs	Indium arsenide	33000	460
InP	Indium phosphide	4600	150

Minority carrier diffusion occurs if the electron-hole pairs are generated outside the space-charge region (diffusion zones). In a typical photodiode there are two such regions. The first region is the heavily doped surface region (p^+ in fig. 2.3) which is usually rather thin. A more critical region, where no electric field is present, is located deeper inside the semiconductor below the space-charge region (fig. 2.3). This region is much thicker than the surface region and thus many electron-hole pairs might be generated inside it. The carrier diffusion in this two regions depends on the carrier mobilities and is characterized by the Einstein relation (2.8) [18].

$$D_n = \mu_n \frac{k_B T}{q}, \qquad D_p = \mu_p \frac{k_B T}{q} \tag{2.8}$$

Due to the fact that there is no electric field in these regions the generated charge carriers only move at random due to the thermal energy and do not contribute to the photocurrent immediately. Instead of that there are two possible scenarios. The carriers either reach the SCR by chance within their lifetimes τ_n and τ_p or they recombine after τ_n and τ_p. Carriers which reach the drift region are accelerated towards the anode or the cathode respectively and generate a photocurrent. The remaining carriers recombine and do not contribute to the photocurrent at all.

The statistical distribution of the carriers generated either in the diffusion or the drift region, causes a certain delay between the light incidence and the resulting photocurrent (see fig. 2.4). Summarizing it can be concluded that it is necessary to minimize carrier diffusion to design fast photodetectors. This can be either achieved by using semiconductor materials with higher absorption coefficients or by increasing the width of the space-charge

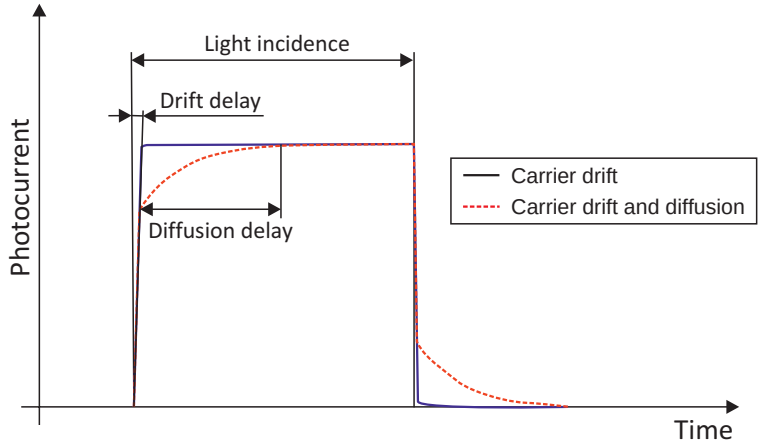


Figure 2.4: Photocurrent for carrier drift and diffusion [1]

region. The latter can be reached by three factors: the use of a PIN photodiode with a thick intrinsic zone, a reduced intrinsic zone doping or a larger reverse voltage.

2.1.3 Quantum Efficiency and Responsivity

The external, total or overall quantum efficiency η is defined as the number of generated charge carriers per incident photon

$$\eta = \frac{I_{ph}}{q\Phi} = \frac{I_{ph}}{q}\left(\frac{h\nu}{P_{opt}}\right) \tag{2.9}$$

with the photocurrent I_{ph}, the photon flux $\Phi = P_{opt}/h\nu$ and the optical power P_{opt} [18]. The ideal quantum efficiency is unity, but reflection at the semiconductor surface, incomplete absorption or recombination in the field free regions reduce the quantum efficiency of a real photodetector. Thus the external quantum efficiency η can be divided into the optical quantum efficiency η_o and the internal quantum efficiency η_i (2.10).

$$\eta = \eta_o \eta_i \tag{2.10}$$

The **optical quantum efficiency** describes the losses due to the partial reflection of the incident light at the semiconductor surface. The reflection occurs due to the different indices of refraction of the surrounding air $\overline{n}_s$ (air: $\overline{n}_s = 1.0$) and the semiconductor material $\overline{n}_{sc}$ (e.g. Si: $\overline{n}_{sc} \approx 3.5$)(see fig. 2.5). The reflectivity $\overline{R}$ of the transition between air ($\overline{n}_s = 1.0$) and the semiconductor depends on the index of refraction $\overline{n}_{sc}$ and on the extinction coefficient $\overline{\kappa}$ of the absorbing material (2.11) [3].

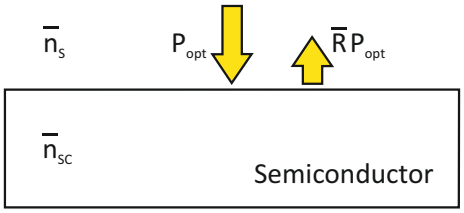


Figure 2.5: Reflection at the semiconductor surface [1]

$$\overline{R} = \frac{(1-\overline{n}_{sc})^2 + \overline{\kappa}^2}{1+\overline{n}_{sc})^2 + \overline{\kappa}^2}, \qquad \overline{\kappa} = \frac{\alpha\lambda_0}{4\pi} \tag{2.11}$$

The partial reflection at the semiconductor surface is described by the optical quantum efficiency η_0 (2.12).

$$\eta_o = 1 - \overline{R} \tag{2.12}$$

The optical quantum efficiency can be increased by introducing an anti reflection coating (ARC) at the semiconductor surface. For a certain wavelength the index of refraction $\overline{n}_{ARC}$ and the optimum thickness d_{ARC} of the ARC layer can by calculated by [1]

$$\overline{n}_{ARC} = \sqrt{\overline{n}_s \overline{n}_{sc}}, \qquad d_{ARC} = \frac{\lambda_0}{4\overline{n}_{ARC}}. \tag{2.13}$$

Nevertheless a complete suppression of the partial reflection at the semiconductor surface is not possible in practice.

The **internal quantum efficiency** is defined as the number of photo generated electron-hole pairs, which contribute to the photocurrent, divided by the number of photons which penetrate into the semiconductor. Exactly speaking η_i has to be sub classified into the stationary and the dynamical internal quantum efficiency.

In the stationary case light intensity and therefore the photocurrent are constant with time. Carriers generated in the SCR are accelerated by the electric field towards the anode or the cathode respectively and generate a photocurrent. Electron-hole pairs which are generated in the field free diffusion zones (Region 1 and 2 in fig. 2.3) only contribute to the photocurrent if they can reach the drift zone within their lifetimes. Carriers which cannot reach the SCR within their lifetimes recombine and thus the internal quantum efficiency is reduced.

In the dynamical case, light intensity and photocurrent change with time. Alike in the stationary case, electron-hole pairs generated in the SCR are drifting to the anode or cathode and contribute to the photocurrent. However, carriers that are generated in the diffusion zones do not have enough time to diffuse to the drift region until the light intensity is reduced again. Thus the diffusion tails of the photocurrent of sequenced light pulses overlap and the internal quantum efficiency is additionally reduced (fig. 2.6). The

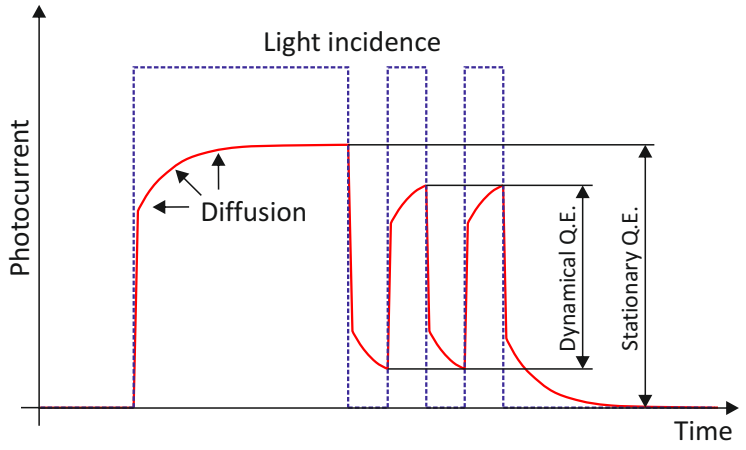


Figure 2.6: Influence of carrier diffusion on the internal quantum efficiency [1]

higher the data rate or the frequency of the signal, the smaller becomes the dynamical quantum efficiency. Therefore the dynamical quantum efficiency is usually lower than the stationary one.

Another useful figure of merit for the design of optical receivers is the responsivity of a photodiode. The responsivity R is the ratio of the generated photocurrent I_{ph} to the incident optical power P_{opt} at a certain wavelength λ_0 (2.14) [1].

$$R = \frac{I_{ph}}{P_{opt}} = \frac{q\lambda_0}{hc}\eta = \frac{\lambda_0\eta}{1.243} AW^{-1} \tag{2.14}$$

The responsivities of important real photodetectors are shown in fig. 2.7. The dashed line represents the maximum responsivity of an ideal photodetector with $\eta = 100\%$. Due to partial reflection at the semiconductor surface, incomplete absorption or recombination in the field free regions, the responsivity of real detectors is always lower than shown in (2.14).

2.1.4 Equivalent Circuit

The equivalent circuit of a photodiode consists of a current source I_{ph}, which represents the generated photocurrent, the capacitance of the space-charge region C_p, a parallel resistor R_p and a serial resistor R_s (2.8). C_p depends on the doping concentration of the p and n zone and on the area and the thickness of the SCR. For a reverse-biased abrupt pn junction C_p is given by [3]

$$C_p = A\sqrt{\frac{q\epsilon_r\epsilon_0 N_{A/D}}{2}} \frac{1}{\sqrt{U_D - U - (2k_BT/q)}}, \qquad U_D = \frac{k_BT}{q} \ln \frac{N_A N_D}{n_i^2} \tag{2.15}$$

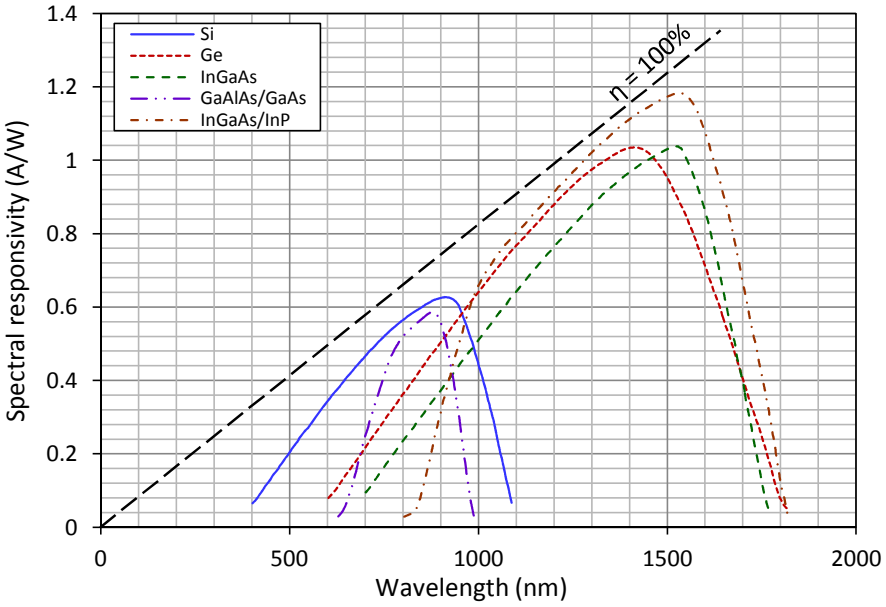


Figure 2.7: Responsivity comparison of real photodetectors [2]

where $N_{A/D}$ represents the doping concentration of the low doped side of the pn junction. The capacitance of a PIN photodiode with a low doped intrinsic zone with the thickness d_I between the high doped p and n regions, can be approximated by

$$C_p = A\frac{\epsilon_r \epsilon_0}{d_I}. \tag{2.16}$$

The parallel resistor R_p models the leakage, the dark or the reverse current of the photodiode. In most cases R_p is very high and can be neglected. The resistance of the low doped zones of the photodiode through which the photocurrent I_{ph} traverses, is modeled by the serial resistance R_s. For PIN photodiodes with high doped p and n zones R_s can be neglected if the intrinsic zone is fully depleted and carrier drift dominates.

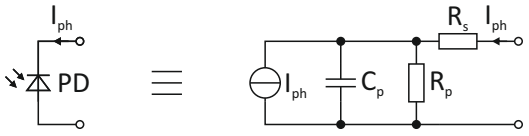


Figure 2.8: Equivalent circuit of a photodiode

2.1.5 PIN Photodiode

A PIN photodiode consists of heavily doped p^+ and n^+ zones with a low doped 'intrinsic' zone in between. If the pn junction is reverse biased, the intrinsic zone is easily depleted due to the low doping concentration and a space-charge region is generated inside the intrinsic region. With further increasing bias voltage the SCR cannot extend further into the high doped p^+ and n^+ regions and thus the electric field increases inside the intrinsic zone. The result is an electric field that is strong and nearly constant within the intrinsic zone (see fig. 2.9). Electron-hole pairs, which are generated inside the intrinsic zone,

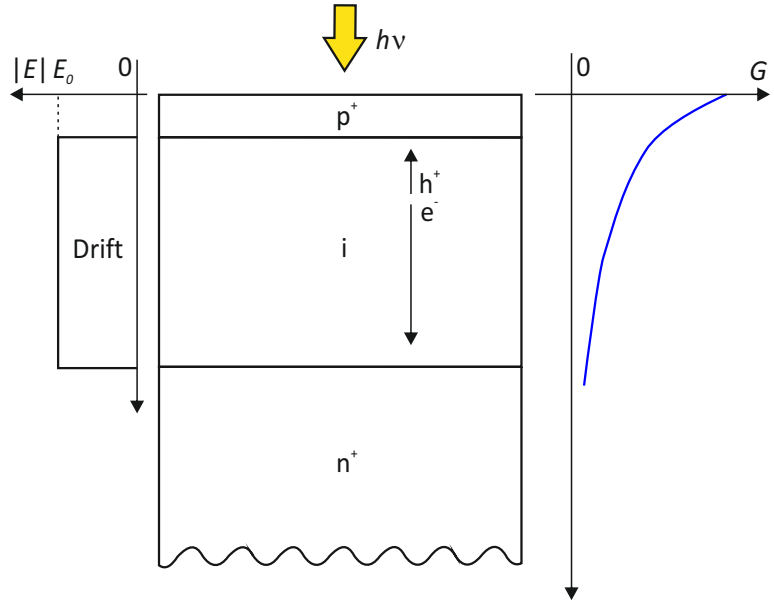


Figure 2.9: Distribution of the electric field in a reverse biased PIN photodiode [3]

are immediately separated and accelerated towards the anode or the cathode respectively by the strong electric field. To maximize the responsivity of the diode it is important to generate as many electron-hole pairs as possible inside the intrinsic zone. Thus the thickness d_I of the i-zone must be increased for high efficiency. On the other hand, a thicker i-zone increases the time which is needed by the carriers to move through the diode. Therefore a tradeoff between speed and efficiency has to be found. The use of semiconductor materials with high absorption coefficients α, like Ge or InGaAs, addresses this problem. Another benefit is the higher electron mobility, which increases the speed even further, and the ability to detect light with wavelengths up to 1.6 μm, which are typical for telecom applications.

2.1.6 Semiconductor Materials

Fibers for optical data transmission have been developed over years in a series of generations which are closely tied to the wavelength of the transmitted light. Fig. 2.10 shows the attenuation of the different fiber generations. The dashed line represents a fiber of the early 1980's, the dotted line a late 1980's fiber and the solid line a modern fiber. It can be seen that there are three regions with low optical losses and that the attenuation was reduced from generation to generation.

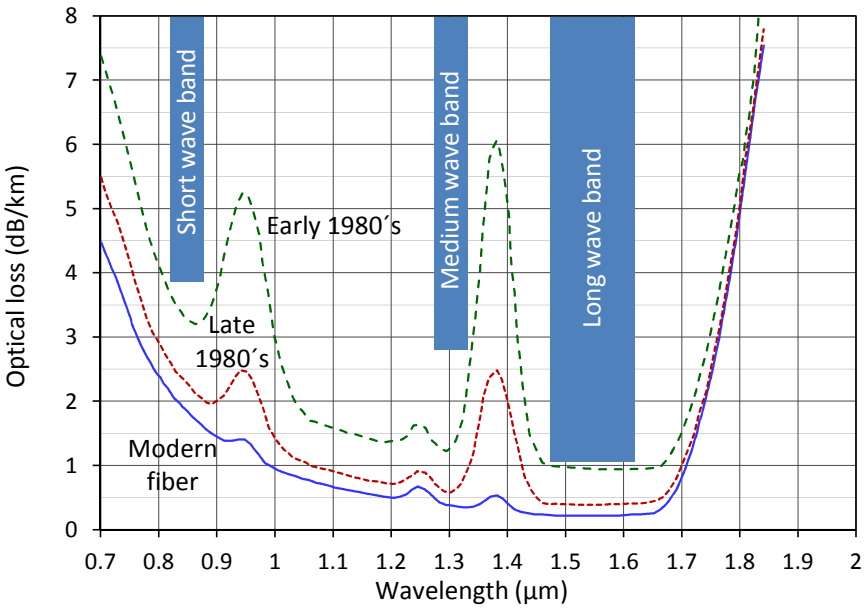


Figure 2.10: Attenuation of different fiber generations [4]

The earliest fiber optic systems were driven at a wavelength of about 850 nm, the so-called 'short wave band'. This window was chosen due to the local dip in the attenuation profile and the availability of low cost optical sources and cheap silicon detectors for these wavelengths. A drawback of this wavelength region was the relatively high 3 dB/km loss limit. Therefore the development of optical systems concentrated to the 'medium wave band' which offers a lower attenuation of about 0.4 dB/km. To minimize the optical losses the wavelength was further increased and the so-called 'long wave band' with losses of only 0.2 dB/km at around 1550 nm became standard for telecom applications [19].

As silicon is transparent for wavelengths longer than 1.1 μm it can only be used as detector material for wavelengths in the short wave band. To obtain efficient photodetection at the typical telecom wavelengths 1.31 μm and 1.55 μm other materials have to be used. Possible approaches are the use of Ge or InGaAs as photodetector material. The lower

bandgap energy, the higher absorption coefficient α and the higher mobility, compared to Si, qualify them as detector materials for fast telecom applications in the long wave band. Another alternative is the use of Ge photodetectors on Si substrates. The lower bandgap of Ge makes the Si-based detector capable of wavelengths up to 1.55 μm [20, 21, 22]. One challenge of the fabrication of Ge-on-Si photodiodes is the large lattice mismatch of about 4% between Si and Ge. Therefore it is necessary to implement graded composition buffer layers to produce high quality Ge layers on Si substrate [23, 24]. However, the high absorption index, the high carrier mobility, the large responsivity and the ability to detect light with wavelengths up to 1.55 μm justify the high effort.

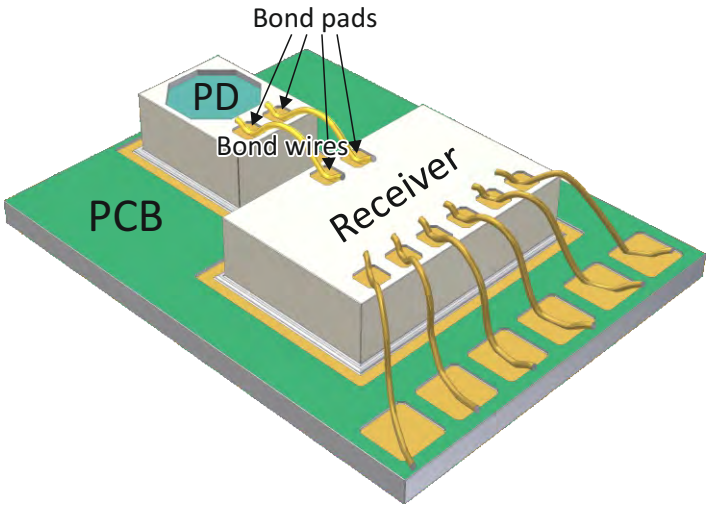
2.2 Connection Structures

The connection between the photodiode and the amplifier can be realized by different methods. To reach high bandwidth and high sensitivity it is important to keep the parasitics of the connection structure as small as possible. Typical connection methods are the use of bond wires, heterogeneous integration or monolithic integration. Each of these connection methods has advantages and disadvantages. The connection via bond wires and bond pads for instance has large parasitic capacitances and inductances but is easy to realize. Monolithic integration on the other hand minimizes the parasitics but is limited by the lattice mismatch of different semiconductor materials. Heterogeneous integration combines the photonic layer with the CMOS wafer using microelectronic fabrication processes at wafer level. This overcomes the problem concerning the lattice mismatch and the parasitics are minimized as well. On the other hand the used technology is still in the fledgling stages. Therefore it is important to choose the best solution for the particular application.

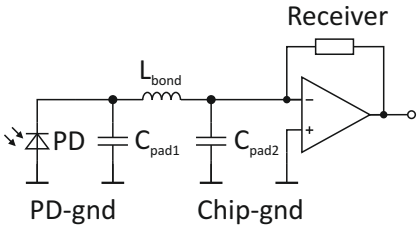
2.2.1 Wire Bonded Photodiode

Traditionally optical receivers consist of a die with the integrated amplifier circuit and an external, wire bonded photodiode. The electronic chip and the photodiode are clued on a printed circuit board (PCB) or inside a chip package and the bond pads of the chips are interconnected via bond wires. The bond wire is usually made either of gold (Au), aluminium (Al) or copper (Cu) and has diameters from 15 μm up to several hundred μm for high-power applications [25]. Generally speaking wire bonding is the most cost-effective and flexible interconnection technology and therefore it is used to assemble the vast majority of semiconductor packages [26]. Especially important for optical receivers at telecom wavelengths is the possibility to easily connect an amplifier, fabricated in cheap CMOS technology, with a Ge or III–V photodiode. But wire bonding also has several disadvantages. The bond pads and the bond wires cause large parasitic capacitances and inductances that significantly reduce the bandwidth of fast optical receivers. Other

drawbacks are the increased package size needed by the receiver chip and the external photodiode as well as the sensitivity of the bond wires to mechanical stress. A typical optical receiver with an external wire bonded photodiode built up on a PCB is shown in fig. 2.11(a).



(a) Optical receiver with external wire bonded photodiode



(b) Equivalent circuit of the wire bonded connection between photodiode and receiver

Figure 2.11: Optical receiver with external wire bonded photodiode and equivalent circuit of the connection structure

Fig. 2.11(b) shows the equivalent circuit and the relevant parasitic components of the connection between photodiode and receiver chip. C_{pad1} represents the capacitance of the photodiode pad and is referenced to the ground of the photodiode die. The photodiode ground and the receiver chip ground can be interconnected either with bond wires or via the PCB using a conductive glue and suitable backside contacts. The inductance of the bond wire between the receiver and the photodiode is represented by L_{bond}. C_{pad2} is the capacitance of the bond pad of the receiver chip. Additional coupling capacitances between

the bond pads and surroundings or mutual inductances between neighboring bond wires are neglected in fig. 2.11(b).

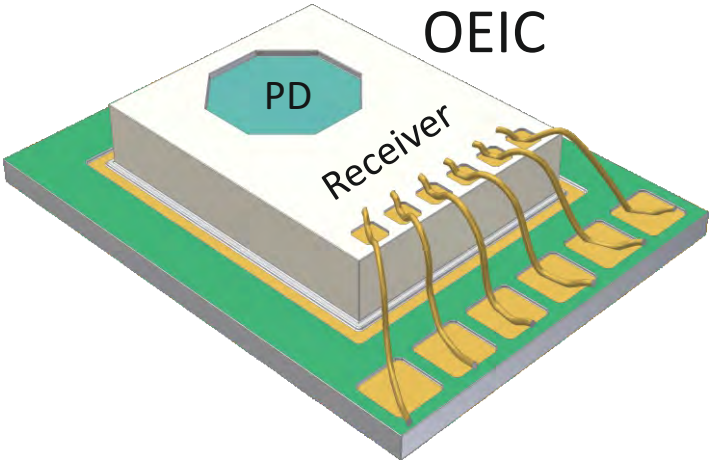
Due to the fact that the receiver bandwidth and sensitivity essentially depend on the capacitance at the input node, it is necessary to keep the parasitic capacitances as low as possible. The parasitic inductances, on the other hand, may lead to unwanted gain-peaking of the receiver input stage.

2.2.2 Monolithic Integrated Photodiode

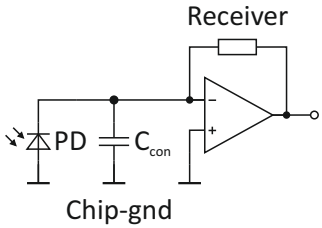
In general a monolithic integrated circuit is an integrated circuit in which substantially all active, passive and interconnection elements are disposed on a single substrate [27]. An integrated circuit with a monolithically integrated photodiode is called optoelectronic integrated circuit (OEIC). The monolithic integration of the photodetector has economical as well as technical advantages compared to the solution with an external photodiode. The economical advantages are basically the reduced production costs due to the use of only one single chip instead of two chips. The single chip solution needs no bondpads for the connection of the photodiode and additional parts of the receiver circuit can be placed space saving around the integrated photodiode. This reduces the required chip size and the production costs as well. Additionally one single chip needs less space than two chips and therefore a smaller and cheaper package for the receiver can be used. A monolithic integrated optical receiver is shown in fig. 2.12(a).

The technical advantages of the monolithic integration are mainly the reduced parasitic components. Due to the fact that neither bond pads nor bond wires are needed almost all parasitic components at the input node of the receiver input stage are avoided. Only the capacitance of the interconnection between the integrated photodiode and the receiver circuit C_{con} is remaining. This interconnection is established by a short on-chip metal path and thus its capacitance is usually negligibly small. Therefore neither the bandwidth nor the sensitivity of the optical receiver is affected by the connection structure between photodiode and receiver. Fig. 2.12(b) shows the parasitic components of a monolithic integrated photodiode.

Nevertheless the monolithic integration of optical components and integrated circuits also has some disadvantages. As silicon is the most common used material for integrated circuits, it is obvious to fabricate optical receivers with monolithically integrated Si photodiodes. However, due to the absorption coefficient of silicon (fig. 2.2) it is not possible to design fast and efficient photodiodes for light with wavelengths larger than 850 nm in standard CMOS or BiCMOS technologies. Therefore at typical telecom wavelengths at 1.31 μm and 1.55 μm materials with high absorption coefficients, like Ge or III–V semiconductors, are used as detector material. The lower bandgap energy and the high mobility make them a good choice for fast telecom applications. InGaAs/InP based integrated circuits are fast and the monolithic integration of fast photodetectors is possible. These



(a) Optoelectronic integrated circuit (OEIC)



(b) Equivalent circuit OEIC

Figure 2.12: Optoelectronic integrated circuit with monolithic integrated photodiode

integration technologies are very expensive and thus the material is not suitable for cheap mass production.

One solution to overcome the before mentioned problems is to combine cheap, mature silicon CMOS technology with monolithic integrated Ge or III–V photodetectors. Therefore high-quality Ge layers must be grown epitaxial on Si substrates. High quality Ge on Si can also act as virtual substrate for the epitaxial growth of GaAs layers. A challenge is the large lattice mismatch between Si and Ge of about 4% which leads to the formation of a huge number of threading dislocations. A way to tackle this problem is to implement graded SiGe composition buffer layers between the Si substrate and the 100% Ge layer. However, with the increase of the Ge composition the surface roughness increases as well due to the influence of strain and the mismatch of the thermal expansion coefficients of Si and Ge ($\alpha_{Si} = 3.55 \times 10^{-6}\mathrm{K}^{-1}$, $\alpha_{Ge} = 7.66 \times 10^{-6}\mathrm{K}^{-1}$ at 750°C) [1].

This effect can be avoided by introducing an intermediate chemical mechanical polishing (CMP) step at a composition of $Si_{0.5}Ge_{0.5}$ [28]. The planarization of the surface allows the dislocations to relieve the strain introduced by the subsequent growth to eliminate the

driving forces for the nucleation of additional threading dislocations. Fig. 2.13 shows a Ge mesa photodiode on top of the graded SiGe structure with CMP step at $Si_{0.5}Ge_{0.5}$.

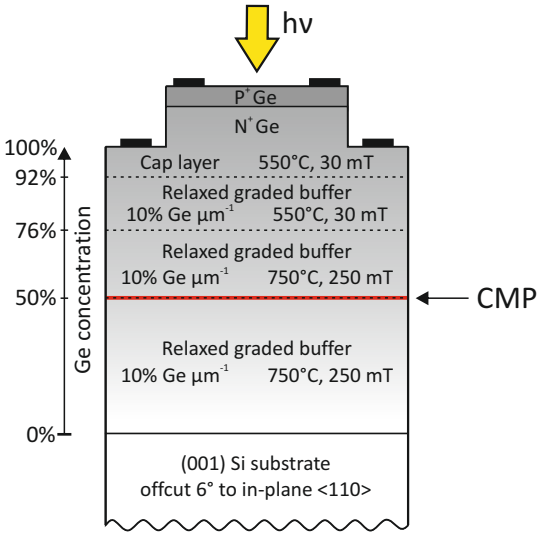


Figure 2.13: Ge PD on SiGe/Si [5]

In conclusion it can be stated that the monolithic integration of photodiode and receiver on the same die has many advantages concerning the reduced paracitic components between the photodiode and the receiver input node. This leads to significantly increased sensitivity and bandwidth of the optical receiver. On the other hand the monolithic integration of photodetectors that are capable of the typical telecom wavelengths 1.31 μm and 1.55 μm, is hindered by the large lattice mismatch between Ge or III–V semiconductor materials and Si.

2.2.3 Heterogeneous Integrated Photodiode

Heterogeneous integration is defined as the integration of different functionalities such as signal processing, photonics, or sensors at wafer level. The idea is to integrate high-performance optical, electrical or mechanical materials such as mono crystalline silicon, Ge or III–V materials with standard Si CMOS circuits. Compared to the monolithic integration the different devices are not disposed on a single substrate but manufactured on separate substrates with dedicated technologies. In a next step the different devices are joined together by wafer-to-wafer or die-to-wafer bonding. The electrical interconnection between the different dies is established by subsequent through silicon vias (TSV) or Cu TSVs and micro bumps [29].

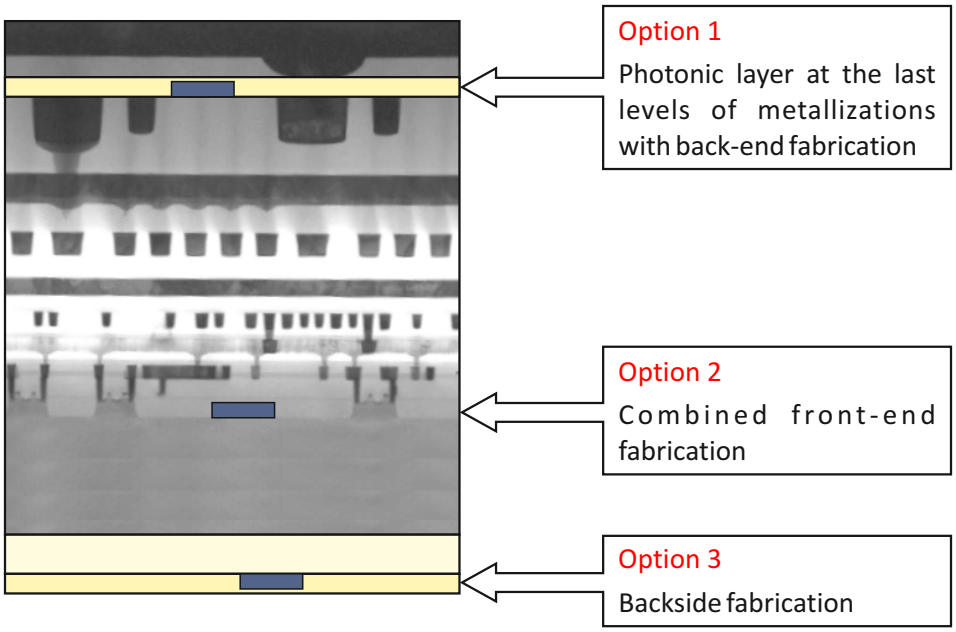


Figure 2.14: Ge PD on SiGe/Si [6]

Fig. 2.14 presents different integration technology routes for the heterogeneous integration of photonic components.

Option 1: The photonic components are built on the top of the CMOS chip at the uppermost levels of metallization. This approach allows the use of any standard CMOS technology and the full heterogeneous integration of III–V based photonic components which results in a high integration density. Depending on the photonic components to be processed two sub-options can be considered [16]:

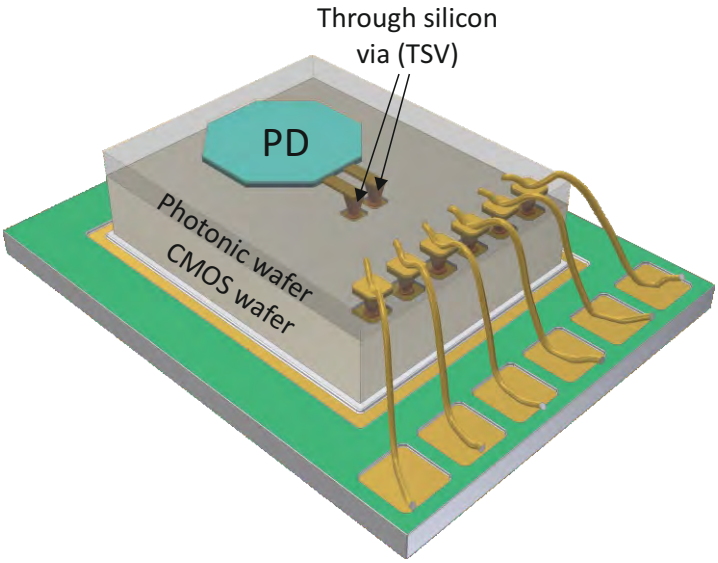
(a) The photonic layers are fabricated by using only low temperature production steps ($< 400°C$) as low temperature deposition or molecular die-to-wafer bonding.
(b) The electronic and the photonic components are fabricated on two separate substrates. In the next step the planarized surfaces of both wafers are coated with deposited oxide. After chemical mechanical polishing (CMP) and perfect cleaning, the oxide surfaces of both wafers are molecular wafer-to-wafer bonded at room temperature. In a last step holes are etched through the top layer and the electrical and the photonic part are connected electrically by TSVs. This approach allows the use of high temperature processes for the fabrication of the photonic components (e.g. Si based modulators or Ge based photodetectors).

Option 2: The processing steps for photonic and electronic devices are combined by using a specific front-end technology using customized design libraries. The areas for photonic and electronic components are separated while the metallizations are designed as

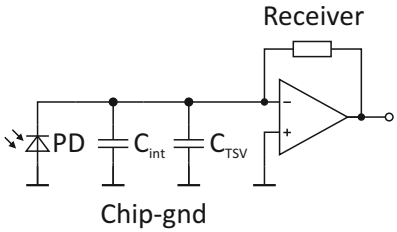
an interconnection network between the electronic and the photonic components. Photonic devices based on III–V semiconductor materials can only be integrated using flip-chip technology which leads to moderate integration density only.

Option 3: The photonic layer is mounted on the rear side of the electronic wafer using either die-to-wafer or wafer-to-wafer bonding. This leads to a high integration density like as shown in option 1. Through wafer contacts build up the electrical interconnections between the photonic and the electronic components.

Heterogeneous integration technologies combine the advantages of both, wire bonding and monolithic integration. Compared to wire bonding the parasitic components of the interconnection structures are rather small. In comparison to monolithic integration technologies there is no problem concerning material or process incompatibilities as lattice mismatch and different thermal expansion coefficients. An optical CMOS receiver with heterogeneous integrated photodiode, electrical connected with through silicon vias, is shown in fig. 2.15(a).



(a) CMOS wafer with photonic wafer and TSVs



(b) Equivalent circuit heterogeneous integrated photodiode

Figure 2.15: CMOS wafer with heterogeneous integrated photodiode

Fig. 2.15(b) shows the equivalent circuit of the heterogeneous integrated photodiode. Due to the fact that the interconnection between the photonic layer and the CMOS wafer is established by TSVs instead of bond wires, the parasitic components are reduced to the capacitance C_{int} of the short on-chip metal path between photodiode and TSV and the capacitance C_{TSV} of the TSV itself. The capacitance C_{int} is usually negligibly small and thus C_{TSV} is the only parasitic component of the heterogeneous interconnection which cannot be neglected.

However, compared to an external wire bonded photodiode the influence of the parasitic components on the bandwidth and the sensitivity of the optical receiver is rather small. Compared to a receiver with monolithic integrated photodiode the parasitic components are a little bit higher but the possibility to use III–V semiconductors as photodetector materials together with standard Si CMOS circuits compensates for this drawback.

2.3 Transimpedance Amplifier

A transimpedance amplifier is a current/voltage (I/V) converter which generates an output voltage being proportional to the input current similarly to an impedance. In an optical receiver it is used to convert the photocurrent generated by the photodiode into an output voltage which is further amplified by the subsequent amplifier stages. The simplest way to do this conversion is to apply a resistor in series to the photodiode and to amplify the voltage across the resistor as shown in fig. 2.16 [1].

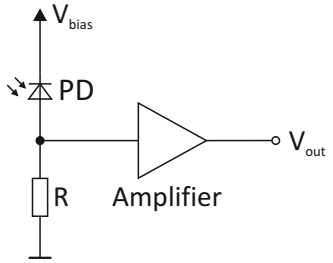


Figure 2.16: Simplest current/voltage converter

The most interesting characteristics of an optical receiver are its bandwidth and sensitivity. The sensitivity basically depends on the responsivity of the photodiode and the input referred noise current of the receiver. Due to the fact that the photocurrent is the smallest signal in the whole receiver circuit, the signal-to-noise ratio (SNR) is most critical at the input node of the transimpedance amplifier. Therefore the input referred noise current is dominated by the noise of the transimpedance amplifier. For the simple receiver shown in fig. 2.16 the noise of the resistor R and the noise of the amplifier are the crucial factors.

The bandwidth of the simple receiver circuit shown in fig. 2.16 depends on the resistor R and on the capacitance of the input node C_T, which is the sum of the photodiode capacitance C_p and the amplifier input capacitance C_{in} (2.17).

$$f_{-3dB} = \frac{1}{2\pi R C_T} \tag{2.17}$$

Thus the resistance R and as well the capacitance C_T have to be small to achieve a high bandwidth. On the other hand the noise of the circuit also depends on the resistor R, the input node capacitance C_T and the first amplifier stage. The mean-square thermal noise current $\overline{i_{th}^2}$ of the resistor R can be calculated by (2.18) [1].

$$\overline{i_{th}^2} = \frac{4k_B T \Delta f}{R} \tag{2.18}$$

Consequently, decreasing the resistor R increases the bandwidth of the receiver on one hand, but on the other hand the noise current of R also increases. This results in a decreasing sensitivity of the whole receiver.

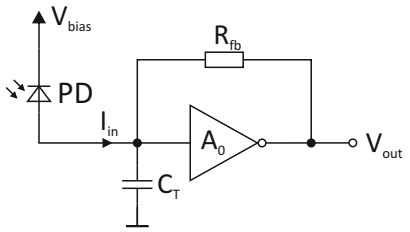


Figure 2.17: Basic circuit of a TIA as preamplifier

These drawbacks can be overcome by using a transimpedance amplifier as shown in fig. 2.17. The input referred noise of this circuit again depends on the resistor R_{fb}, the input node capacitance C_T and the noise of the first amplifier stage. The input node capacitance C_T consists of the photodiode capacitance C_p and the input capacitance of the TIA. The main advantage of using a TIA as preamplifier compared to the simple receiver circuit shown in fig. 2.16 is the fact that the bandwidth is indirectly related to R_{fb} divided by the open-loop gain A_0 of the amplifier (2.19) while the thermal noise current density of R_{fb} stays direct proportional to the value of the resistor [1].

$$f_{-3dB} = \frac{A_0 + 1}{2\pi R_{fb} C_T} \tag{2.19}$$

Thus it is possible to decrease the input referred noise for a given bandwidth of the receiver.

To sum it up, the smaller C_T and the larger R_{fb}, the higher is the sensitivity of the receiver. On the other hand a high bandwidth can be only achieved with small C_T and small R_{fb}. Therefore the design of an optical receiver is always a tradeoff between bandwidth and sensitivity.

2.3.1 Frequency Response

The bandwidth of a TIA, consisting of an operational amplifier with a frequency dependent open-loop gain, a feedback network and a total input node capacitance C_T, not only depends on C_T and the feedback network but also on the frequency response of the operational amplifier. The equivalent circuit of an transimpedance amplifier front-end is shown in fig. 2.18. The serial resistance of the photodiode R_s is neglected and therefore the equivalent circuit of the photodiode consists of an ideal current source I_{ph}, the photodiode capacitance C_p and the parallel resistor R_p. The capacitance C_{con} represents the summarized parasitic capacitances of the connection between photodiode and amplifier input while C_{in} is the capacitance of the input transistor of the amplifier. The feedback network is formed by the feedback resistor R_{fb} and the compensation capacitance C_{fb}. The compensation capacitance C_{fb} is needed to guarantee stability as well as to avoid gain-peaking.

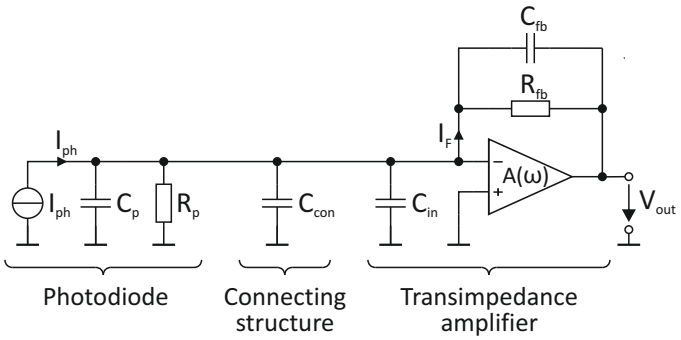


Figure 2.18: Equivalent circuit of a TIA front-end

The total input node capacitance C_T of the circuit shown in fig. 2.18 consists of the photodiode capacitance C_p, the paracitic capacitance C_{con} of the connection structures between photodetector and transimpedance amplifier and the capacitance C_{in} of the input stage of the amplifier (2.20).

$$C_T = C_p + C_{con} + C_{in} \tag{2.20}$$

The frequency-dependent transimpedance $T(\omega)$ of the transimpedance amplifier has the dimension Ω and can be calculated by:

$$T(j\omega) = -\frac{U_{out}}{I_{ph}} = -\frac{R_{fb}/(1+j\omega R_{fb}C_{fb})}{1+\frac{1}{A(j\omega)}\left(1+\frac{R_{fb}/(1+j\omega R_{fb}C_{fb})}{R_p/(1+j\omega R_p C_p)}\right)} \tag{2.21}$$

Substituting the frequency-dependent transfer function of the operational amplifier

$$A(j\omega) = \frac{A_0}{1+j\omega/\omega_c}, \tag{2.22}$$

where ω_c is the transit frequency and A_0 is the open-loop gain ($A_0 \gg 1$) of the operational amplifier, into (2.21) and neglecting the term $1/(R_p \omega_c A_0)$ leads to [30]

$$T(j\omega) = -\frac{R_{fb}}{1 + j\omega\frac{1}{\omega_0 Q} - \frac{\omega^2}{\omega_0^2}}, \tag{2.23}$$

with the following abbreviations ($C_T \gg C_{fb}$):

$$Q \equiv \frac{\sqrt{\frac{R_{fb}(C_{fb}+C_T)}{\omega_c}}}{\frac{1}{\omega_c A_0} + R_{fb}\left(C_{fb} + \frac{C_T + C_{fb}}{A_0}\right)} \approx \frac{\sqrt{\frac{R_{fb}C_T}{\omega_c A_0}}}{\frac{1}{\omega_c A_0} + R_{fb}\left(C_{fb} + \frac{C_T}{A_0}\right)} \tag{2.24}$$

$$\omega_0 \equiv \sqrt{\frac{\omega_c A_0}{R_{fb}(C_{fb} + C_T)}} \approx \sqrt{\frac{\omega_c A_0}{R_{fb} C_T}} \tag{2.25}$$

For an ideal operational amplifier with a frequency-independent amplification ($A_0 = \infty$ and $\omega_c = \infty$) equation (2.23) can be simplified to

$$T(j\omega) = -\frac{R_{fb}}{1 + j\omega R_{fb} C_{fb}} \tag{2.26}$$

which is clearly the transfer function of a first order low pass filter with a -3 dB cutoff frequency of

$$f_{-3dB} = \frac{1}{2\pi R_{fb} C_{fb}}. \tag{2.27}$$

However, the assumption of an ideal operational amplifier is a too simple approximation of the real behavior of a transimpedance amplifier. In particular for large input node capacitances C_T the term ω^2 in equation (2.23) leads to the so-called gain-peaking, an overshoot in the frequency response at high frequencies, which reduces the bandwidth and causes stability problems. Fig. 2.19 shows the influence of the total input node capacitance C_T on the frequency response of an operational amplifier in transimpedance configuration. The gain-peak disappears if the input node capacitance is reduced from 1 pF to 100 fF. On the other hand the -3 dB bandwidth increases from 120 MHz to 180 MHz. Therefore it can be concluded that the total input node capacitance, consisting of the photodiode capacitance, the capacitance of the connecting structures and the capacitance of the amplifier input stage (2.20), has to be kept as small as possible for building fast optical receivers.

2.3.2 Stability and Compensation

The transfer function of the transimpedance amplifier shown in (2.23) obviously is a function with two poles. As mentioned above large values of C_T may lead to a gain peak

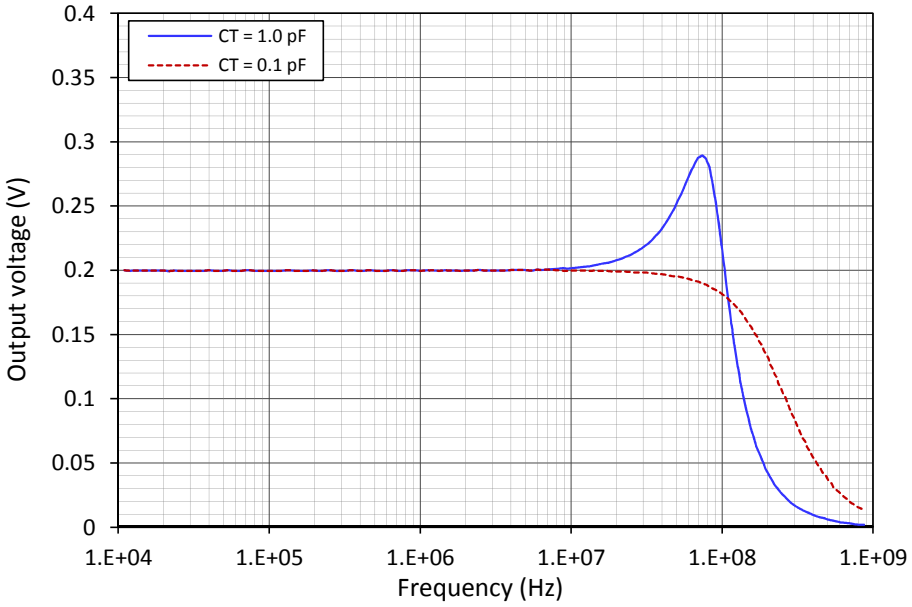


Figure 2.19: Frequency response of an operational amplifier in transimpedance configuration for two different values of the input node capacitance C_T ($I_{ph} = 10$ μA, $R_{fb} = 20$ kΩ, $R_p = 10^9$ Ω, $\omega_c = 6.28$ s^{-1}, $C_{fb} = 50$ fF, $A_0 = 100$) calculated with (2.23) [3]

in the frequency response curve of the transimpedance amplifier at high frequencies. The consequence is at least an overshoot in the time domain. A strong gain-peaking may cause oscillations and the amplifier gets unstable. The gain-peaking can be avoided by either decreasing the total input node capacitance C_T or by increasing the feedback capacitance C_{fb}. Due to the fact that C_T cannot be minimized at will it makes sense to compensate the gain-peaking by choosing suitable values for C_{fb}.

If the gain-peak should be suppressed completely (i.e. the frequency response should be maximally flat), $Q = 1/\sqrt{2}$ must be chosen (Butterworth filter). Inserting $Q = 1/\sqrt{2}$ into (2.24) and solving for C_{fb} leads to a value of [31]

$$C_{fb} = \frac{\sqrt{2A_0 R_{fb} C_T \omega_c} - (1 + \omega_c R_{fb} C_{fb})}{R_{fb}\omega_c A_0} \approx \sqrt{\frac{2C_T}{R_{fb}\omega_c A_0}} - \frac{C_T}{A_0}. \tag{2.28}$$

However, this elimination of the gain-peaking is at the expense of a reduced -3 dB bandwidth [3]. Although equation (2.28) guarantees a maximum flat response, C_{fb} may be lower in order to achieve dynamic stability [32]. An alternative solution is to choose a smaller value of C_{fb} than calculated in (2.28) and, therefore, reach a higher bandwidth at the cost of some gain-peaking. If C_{fb} is chosen to reach a phase margin of 45° the system

still remains stable and it follows that $Q = \sqrt[4]{2}$ [32]. Inserting this value into equation (2.24) and solving for C_{fb} leads to

$$C_{fb} = \frac{\sqrt{\frac{1}{\sqrt{2}} A_0 R_{fb} C_T \omega_c} - (1 + \omega_c R_{fb} C_T)}{R_{fb} \omega_c A_0} \approx \sqrt{\frac{C_T}{\sqrt{2} R_{fb} \omega_c A_0}} - \frac{C_T}{A_0}. \tag{2.29}$$

For practical implementation of a transimpedance amplifier the value of C_{fb} should be chosen between the values specified by 2.28 and 2.29.

2.3.3 Noise

Noise in integrated circuits is generated basically due to the fact that the electrical charge is not continuous but is carried in discrete amounts equal to the elementary charge $q = 1.602 \times 10^{-19}\ C$. Therefore noise is caused by small current and voltage fluctuations which are associated with fundamental processes in the integrated circuit devices. Due to the fact that noise limits the sensitivity and the bit error rate of an optical receiver it is important to analyze the different noise sources.

Sources of Noise

Shot noise is always associated with a direct current flow and appears in diodes, bipolar and MOS transistors. Its origin is the passage of the charge carriers across the pn junction. The passage of the carriers depends on their energy and their velocity towards the junction. Due to the fact that each carrier has a different energy and a different velocity the external current I through the junction is not a steady current but, in fact, the sum of a large number of independent current pulses. This current fluctuation is termed shot noise and is specified in terms of its mean-square variation $\overline{i_{sn}^2}$ about the average value I_D [7]. It can be calculated by

$$\overline{i_{sn}^2} = \overline{(I - I_D)^2} = \lim_{T \to \infty} \frac{1}{T} \int_0^T (I - I_D)^2 dt = \int_0^{BW} i_{sn}^2 df, \tag{2.30}$$

where i_{sn}^2 is the shot noise current spectral density in A^2/Hz and BW the bandwidth in Hertz. The noise current spectral density i_{sn}^2 of a current I that is composed of random independent current pulses with an average value I_D is defined by

$$i_{sn}^2 = 2qI_D, \tag{2.31}$$

where q is the elementary charge (1.602×10^{-19} As). As shown in (2.31) it is frequency independent and therefore is a source of white noise [7].

Thermal Noise results from the random thermal movement of the electrons in a conventional resistor. Due to the fact that the drift velocities of electrons in a conductor are much slower than than the thermal velocities, it is unaffected by the presence or absence of direct current. Since the thermal noise is caused by the thermal movement of the electrons it is proportional to the absolute temperature T. If the absolute temperature approaches zero, the thermal noise also approaches zero.

Monolithic and thin-film resistors show thermal noise which can be represented either by a series voltage generator $\overline{v_{th}^2}$ as shown in fig. 2.20(a) or by a shunt current generator $\overline{i_{th}^2}$ as shown in fig. 2.20(b). These two representations are equivalent and the thermal noise spectral densities can be calculated by

$$v_{th}^2 = 4k_B T R \tag{2.32}$$

and

$$i_{th}^2 = 4k_B T \frac{1}{R}, \tag{2.33}$$

where k_B is the Boltzmann constant (1.38×10^{-23} J/K) [7].

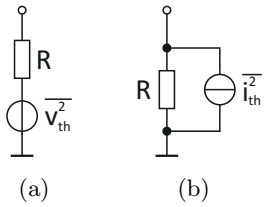


Figure 2.20: Thermal noise voltage source (a) and thermal noise current source (b)

Due to the fact that the thermal noise spectral densities v_{th}^2 and i_{th}^2 are frequency-independent, the thermal noise is also a source of white noise [1].

Flicker Noise (1/f Noise) occurs in all active devices and also in some passive components such as carbon resistors [7]. It has different reasons, but mainly it is caused by traps associated with crystal defects or contaminations of the material. Electrons are captured and released by these traps in a random process and cause a noise signal with its energy concentrated at low frequencies. It is always bound to a direct current flow and its noise current spectral density shows a $1/f$ dependence

$$i_{fn}^2 = K_1 \frac{I^a}{f^b}, \tag{2.34}$$

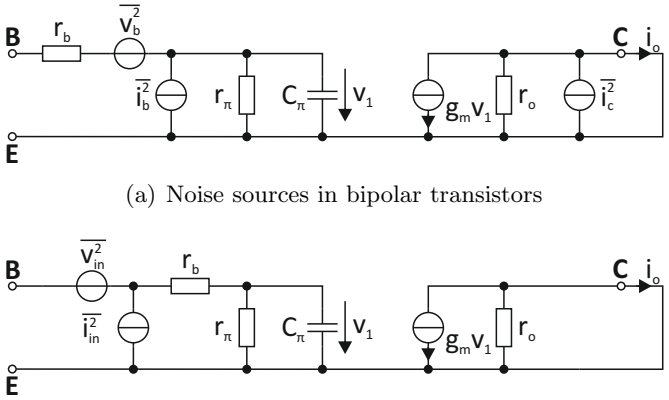
where K_1 is a constant for a particular device, I the direct current through the device, a constant a between 0.5 and 2 and a constant b around unity. The values of the constants depend on the different technologies and devices [7].

Burst Noise (Popcorn Noise) is another low-frequency noise which appears in integrated circuits as well as in discrete transistors. The origin of this noise is not fully clarified but experiments showed that it is bound to the presence of heavy-metal ions. Gold-doped devices, for instance, show a very high burst noise [7]. One characteristic of burst noise is that its waveform consists only of noise pulses of a number (two or more) of certain discrete levels. These noise bursts have a repetition rate of few kilohertz or less and can be heard as a popping sound when played through a loudspeaker (popcorn noise) [33]. The burst noise current spectral density can be calculated by

$$i_{bn}^2 = K_2 \frac{I^c}{1 + \left(\frac{f}{f_c}\right)^2}, \tag{2.35}$$

where K_2 is a constant for a particular device, I the direct current through the device, c a constant between 0.5 and 2 and f_c a certain frequency for a given noise process [7].

Bipolar Transistor Noise Model



(a) Noise sources in bipolar transistors

(b) Equivalent transistor input noise sources

Figure 2.21: Equivalent circuits of noise sources in a bipolar transistor [7]

In an active-forward biased bipolar transistor the minority carriers diffuse and drift across the base region towards the collector-base junction. As soon as they reach the collector-base space-charge region they are accelerated by the electric field existing there and are swept to the collector. Due to the fact that the time of arrival of the diffusing and drifting carriers at the collector-base junction is a random process, the resulting collector current I_C consists of a series of random current pulses. These fluctuations are represented in the equivalent circuit of the noise sources (fig. 2.21(a)) by a shot noise current generator $\overline{i_c^2}$

between collector and emitter and their mean-square value can be calculated by

$$\overline{i_c^2} = \int_0^{BW} 2qI_C df. \tag{2.36}$$

The base current I_B in a bipolar transistor results from carrier injection from the base into the emitter and the recombination of carriers in the base and the base-emitter depletion region. Due to the fact that these are all random processes, I_B also shows full shot noise. Additional flicker noise and burst noise have been found experimentally across the internal base-emitter junction [1]. In the equivalent circuit (fig. 2.21(a)) these three noise sources are combined and represented by the noise generator $\overline{i_b^2}$ (2.37).

$$\overline{i_b^2} = \underbrace{\int_0^{BW} 2qI_B df}_{Shot\ noise} + \underbrace{\int_0^{BW} K_1 \frac{I_B^a}{f} df}_{Flicker\ noise} + \underbrace{\int_0^{BW} K_2 \frac{I_B^c}{1+\left(\frac{f}{f_c}\right)^2} df}_{Burst\ noise} \tag{2.37}$$

The collector series resistor r_c shows thermal noise but is neglected in fig. 2.21(a) since it is in series with the high-impedance collector node. The resistance r_b represents the lateral connection between the base contact and the emitter. The thermal noise caused by r_b is represented by the noise source $\overline{v_b^2}$ (2.38).

$$\overline{v_b^2} = \int_0^{BW} 4k_B T r_b df \tag{2.38}$$

The resistors r_π and r_o in the equivalent circuit are virtual resistors used for modeling purposes only and thus they do not show thermal noise. The noise sources defined by (2.36)–(2.38) of the circuit shown in fig. 2.21(a) can be also represented by an equivalent input noise voltage source $\overline{v_i^2}$ and an equivalent input noise current source $\overline{i_i^2}$ as shown in fig. 2.21(b) [1]:

$$\overline{v_{in}^2} = \int_0^{BW} 4k_B T \left(r_b + \frac{1}{2g_m}\right) df \tag{2.39}$$

$$\overline{i_{in}^2} = \int_0^{BW} 2q \left(I_B + \frac{K_1}{2q}\frac{I_B^a}{f} + \frac{I_C}{|\beta(jf)|^2}\right) df \tag{2.40}$$

Fig. 2.22 shows the equivalent input noise current density of a bipolar transistor with a collector current $I_C = 100\ \mu$A, a gain $\beta = 80$ and a -3 dB cutoff frequency $f_{-3dB} = 500$ MHz. At low frequencies the equivalent input noise current density is dominated by flicker noise. The flicker noise can be neglected for high bandwidths of more than several

hundred MHz since the equivalent input noise density is increasing with the square of the frequency [1].

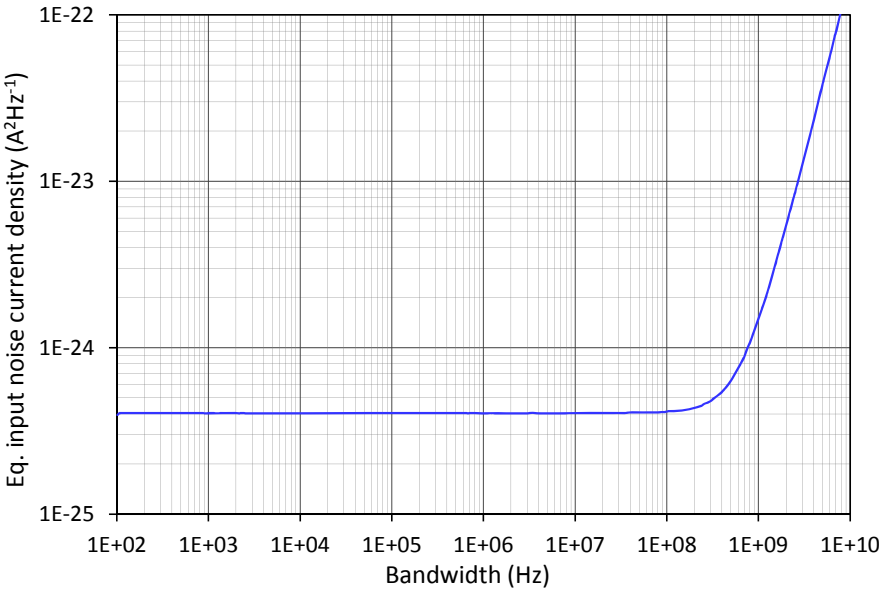


Figure 2.22: Equivalent input noise current density of a bipolar transistor, $I_C = 100\ \mu$A, $\beta = 80$, $f_{-3dB} = 500$ MHz, flicker noise neglected [1]

Noise Model of a TIA with Bipolar Input Stage

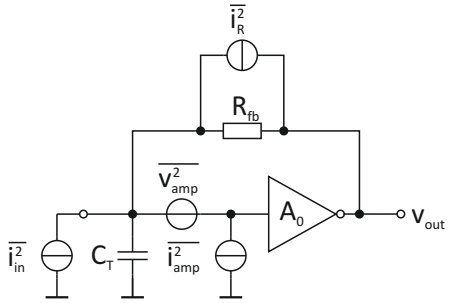


Figure 2.23: Basic TIA circuit including general noise sources

Fig. 2.23 shows a basic TIA circuit including the general noise sources of the individual TIA components. The main noise sources are the input noise sources of the first amplifier

stage $\overline{i_{amp}^2}$ and $\overline{v_{amp}^2}$ and the thermal noise generated by the feedback resistor $\overline{i_R^2}$. Therefore the mean-square input noise current of the circuit shown in fig. 2.23 is given by

$$\overline{i_{in}^2} = \overline{i_{amp}^2} + \frac{\overline{v_{amp}^2}}{\left|\frac{R_{fb}}{1+j\omega C_T R_{fb}}\right|^2} + \overline{i_R^2}, \tag{2.41}$$

which leads to

$$\overline{i_{in}^2} = \overline{i_{amp}^2} + \overline{v_{amp}^2}\ \frac{1+4\pi^2 f^2 C_T^2 R_{fb}^2}{R_{fb}^2} + \overline{i_R^2}. \tag{2.42}$$

For a bipolar transistor input stage, as shown in fig. 2.24, the mean-square input noise

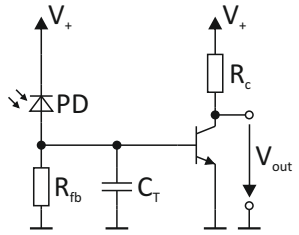


Figure 2.24: Simplified TIA circuit for noise analysis

current $\overline{i_{in}^2}$ depends mainly on the noise generated by the input transistor of the first amplifier stage and the noise of the feedback resistor R_{fb}. The noise of the load resistor R_c can be neglected in a first approximation because it is attenuated by the gain of the input transistor. Therefore equation 2.42 together with the equivalent input noise sources of the bipolar transistor (2.39) and (2.40) leads to the equivalent input noise current of the bipolar transimpedance amplifier [1]

$$\begin{aligned}\overline{i_{in}^2} \;=\; & \int_0^{BW} \frac{4k_BT}{R_{fb}} df + \int_0^{BW} 2q\left(\frac{I_C}{\beta} + \frac{K_1}{2qf}\left(\frac{I_C}{\beta}\right)^a + \frac{I_C}{\left|\frac{\beta}{1+jf/f_\beta}\right|^2}\right) df + \\ & + \int_0^{BW} \frac{4(1+4\pi^2 f^2 C_T^2 R_{fb}^2) k_B T \left(r_B + \frac{1}{2g_m}\right)}{R_{fb}^2} df. \end{aligned} \tag{2.43}$$

2.3.4 Sensitivity and Bit Error Rate

The sensitivity of an optical receiver is defined as the minimal average optical signal power level required at the receiver input to achieve a certain bit-error rate BER [34]. If, for

instance, a specific optical receiver reaches a BER of 10^{-12} at a minimal average signal optical power of -25 dBm its sensitivity is -25 dBm. Therefore the definition of the receiver sensitivity always depends on the targeted bit-error rate. In a typical optical receiver the responsivity of the used photodetector and the noise generated in the receiver are the major limiting factors to reach a high sensitivity.

In general optical data transmission uses binary optical signals with two discrete states (no light = "0", light = "1"). These two states lead to two discrete photocurrents $\langle i_0 \rangle$ and $\langle i_1 \rangle$ which again represent the logical zero ($\langle i_0 \rangle$) and the logical one ($\langle i_1 \rangle$). Due to noise the generated photocurrent has a certain distribution around the expected values $\langle i_0 \rangle$ and $\langle i_1 \rangle$ as shown in fig. 2.25. The bit rate B is defined by the time slot T_t. For simplicity an amplifier with an ideal low-pass characteristic and a bandwidth of $B/2$ is assumed [8].

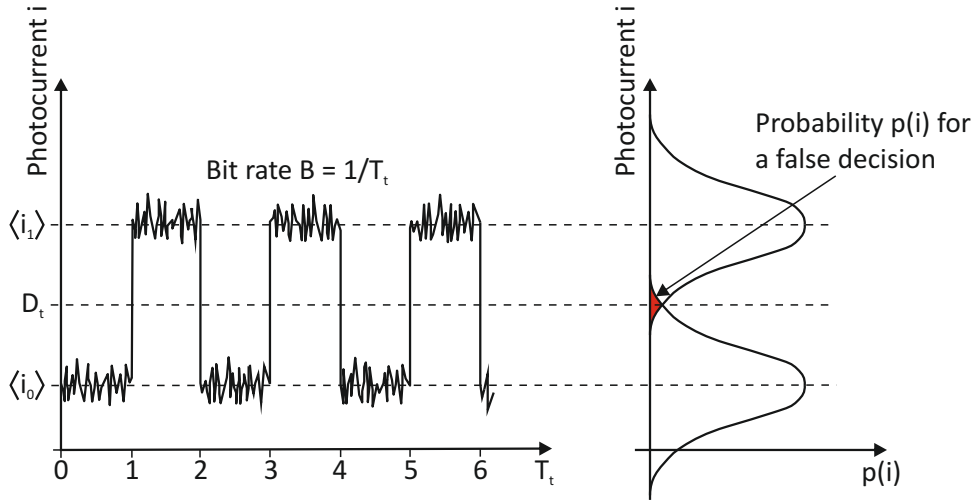


Figure 2.25: Noisy photocurrent with bit rate B and corresponding distribution $p(i)$ of the instant i values around the logic levels $\langle i_0 \rangle$ and $\langle i_1 \rangle$ [8]

Integrating the equivalent input noise spectral density i_{in}^2 over the bandwidth of the amplifier $B/2$ gives the variance of the equivalent input noise current $\overline{i_{in}^2}$ [8]:

$$\overline{i_{in}^2} = \int_0^{B/2} i_{in}^2 df \tag{2.44}$$

If a gaussian distribution of the instant current values around the expected values $\langle i_0 \rangle$ and $\langle i_1 \rangle$ is assumed, the probability density for a logical zero is

$$p_0(i) = \frac{1}{\sqrt{2\pi \overline{i_{in}^2}}} \, e^{-\frac{(i-\langle i_0 \rangle)^2}{2\overline{i_{in}^2}}} \tag{2.45}$$

and for a logical one

$$p_1(i) = \frac{1}{\sqrt{2\pi\overline{i_{in}^2}}}\, e^{-\frac{(i-\langle i_1\rangle)^2}{2\overline{i_{in}^2}}}. \tag{2.46}$$

Furthermore it is assumed that the distribution of the logical zeros and the logical ones of the input pattern is equally distributed in respect to time. The mean value of the gaussian current distribution around $\langle i_0\rangle$ and $\langle i_1\rangle$ is the so-called decision threshold D_t.

$$D_t = (\langle i_1\rangle + \langle i_0\rangle)/2 \tag{2.47}$$

A current $i \leq D_t$ is considered as a logical zero while a current $i \geq D_t$ is considered as a logical one. The probability of a wrong decision concerning the logical zero can be calculated by the bit error rate for the logical zero

$$BER_0 = \int_{D_t}^{\infty} p_0(i)di = \frac{1}{\sqrt{2\pi}}\int_{Q}^{\infty} e^{\frac{-u^2}{2}}du, \tag{2.48}$$

with

$$u = \frac{i - \langle i_0\rangle}{\sqrt{\overline{i_{in}^2}}} \tag{2.49}$$

and the Q-factor

$$Q = \frac{\langle i_1\rangle - \langle i_0\rangle}{2\sqrt{\overline{i_{in}^2}}}. \tag{2.50}$$

Under the applied assumptions the same is also valid for the bit error rate of the logical one

$$BER_1 = \int_{\infty}^{D_t} p_1(i)di = BER_0 \tag{2.51}$$

Hence it follows the bit error rate BER in general

$$BER = \frac{1}{\sqrt{2\pi}}\int_{Q}^{\infty} e^{\frac{-u^2}{2}}du \approx \frac{1}{\sqrt{2\pi}Q}\, e^{-\frac{Q^2}{2}} \tag{2.52}$$

where the useful approximation is valid for $Q > 1$ [35]. Fig. 2.26 shows the relationship of the bit error rate and the Q-factor. This relationship can be useful for a fast estimation of the BER of an optical receiver when using a communication analyzer or a digital sampling oscilloscope which are able to calculate the Q-factor from the eye diagram. For instance $Q = 6$ complies to $BER = 10^{-9}$ and $Q = 7$ complies to $BER = 1.3 \times 10^{-12}$.

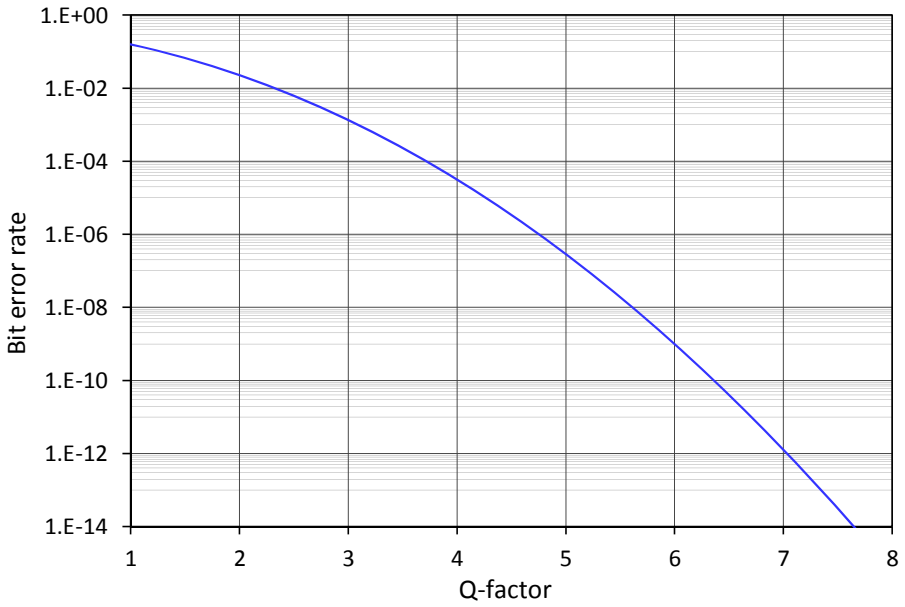


Figure 2.26: Relationship between bit error rate and Q-factor

3 Photodiode Characterization

The first part of an optical receiver chain is the photodiode (see fig. 2.1). The characteristics of the used photodiode are crucial for the performance of the whole receiver. Important parameters for a good receiver performance are the bandwidth, the responsivity, the capacitance and the dark current of the photodiode. The diodes used in this work are provided by IMEC and CEA-LETI, two project partners of the European Community project HELIOS (FP7 224312). The diodes manufactured by CEA-LETI are based on Ge while the diodes developed by IMEC are based on InP/InGaAs.

This chapter starts with an overview of the characterized photodiode types, describes the measurement setups used to determine the different diode parameters and concludes with a summary of the diodes which are suitable for the optical receiver developed in this work.

3.1 CEA-LETI Photodetectors

CEA-LETI provided two different types of Ge photodetectors – vertical ones, where the light is directly coupled from the fiber into the diode, and lateral ones, where the light is coupled into the diode via a grating coupler and an on-chip waveguide. The connection of the vertical diodes to the CMOS chip is realized by conventional wire bonding while the lateral diode is designed for heterogeneous integration by flip-chip wafer-to-wafer bonding the photonic wafer on top of the CMOS wafer using subsequent through silicon vias (TSV) [36].

3.1.1 Vertical Photodiodes (T559A P23)

CEA-LETI provided seven different vertical photodiode types. All diodes have a PIN structure, are based on Ge and use conventional bond pads and bond wires to connect the diode to the CMOS wafer. The light is coupled directly from the fiber into the diode. The main differences between the various types are the diode diameter and the geometrical dimensions of the contacts between metal and diode. The diodes have bond pads for conventional wire bonding which are used as test pads for the characterization. Fig. 3.1 shows the crosscut of the vertical photodiode from CEA-LETI.

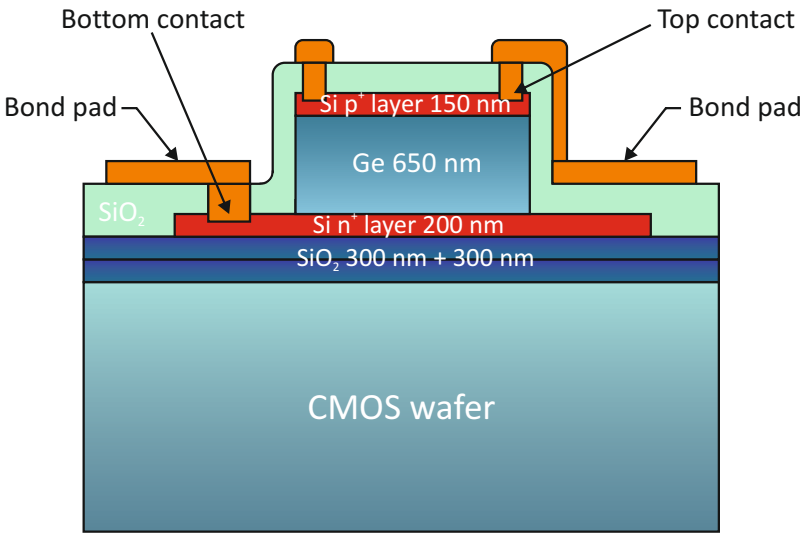


Figure 3.1: Crosscut CEA-LETI vertical photodiode [9]

The diode itself consists of a highly doped 150 nm thick Si p^+ layer, a highly doped 200 nm thick Si n^+ layer and a 650 nm thick Ge intrinsic layer in between. The crystalline quality of the Ge layer, which is grown epitaxially on silicon, has to be as high as possible to reduce the photodiode dark current. The electrical connection of the diode to the test pads is realized by the diode contacts and metal layers to the bond pads. Fig. 3.2 shows a photomicrograph of the vertical photodiode with the pads for wire bonding. As mentioned above seven different diode types, which differ in diode size and width of the top contact metal ring, were characterized. Tab. 3.1 gives an overview of the different photodiode layouts.

Table 3.1: Vertical photodiode layouts

	PIN1	PIN2	PIN3	PIN4	PIN5	PIN6	PIN7
Photodiode ⌀ (μm)	30	50	70	30	50	70	10
Top contact ring width (μm)	1.4	1.4	1.4	2.4	2.4	2.4	1.4

3.1.2 Lateral Photodiodes (V985H)

The lateral photodiodes fabricated by CEA-LETI are based on Ge and have a PIN structure. In contrast to the vertical diode, which uses Ge only as intrinsic layer (see fig. 3.1) between the p^+ and n^+ Si layers, the lateral photodiode is entirely based on Ge. Another

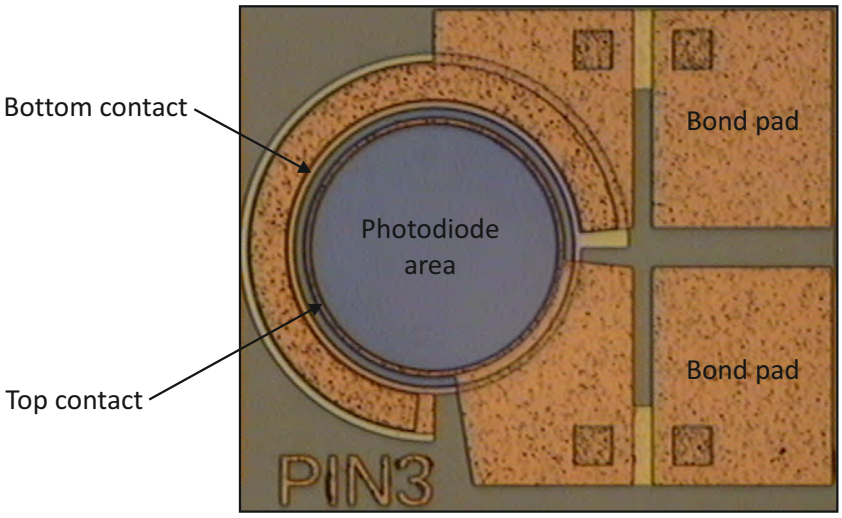


Figure 3.2: Photomicrograph CEA-LETI vertical photodiode

difference is the way to couple the light into the detector. Instead of coupling the light directly from the fiber into the diode, a grating coupler and a Si rib waveguide is used. The waveguide is 400 nm high, 660 nm wide and the etching depth is 130 nm. The diode itself consists of laterally arranged p-doped and n-doped Ge layers with an intrinsic Ge layer between them. The light, guided by the waveguide, is coupled into the diode using a direct butt coupling configuration. In this configuration the epitaxial growth of the Ge is done in a silicon recess at the end of the waveguide [37]. A schematic view of the lateral germanium photodetector integrated at the end of the waveguide is shown in fig. 3.3.

The working principle of grating coupler and waveguide is shown in fig. 3.4. The light, coming from the fiber, is coupled into the grating under the angle Θ_{in} in the yz-plane and is reflected by the grating into the waveguide to the photodiode. The angle Θ_{in} depends on the wavelength of the incident light and the geometrical dimensions of the grating coupler. In the particular case it is in the range of $7° - 10°$.

At first glance the use of grating couplers and waveguides seems to be much more complex than coupling the optical signal directly into the diode. However, the main advantage of this configuration is the possibility of integrating arrayed waveguide gratings (AWG), which work as an optical wavelength (de)multiplexer. Together with an array of e.g. eight photodiodes an 8-channel wavelength division multiplexed (WDM) system can be realized directly on the photonic wafer [38].

In general an AWG consists of input and output waveguides, two star couplers and the grating waveguides (see fig. 3.5). The grating itself is built up by a number of waveguides which have length differences of ΔL between any two neighboring channels. The length differences of the photonic paths lead to phase shifts of $2\pi\overline{n_g}\Delta L/\lambda$ between the channels,

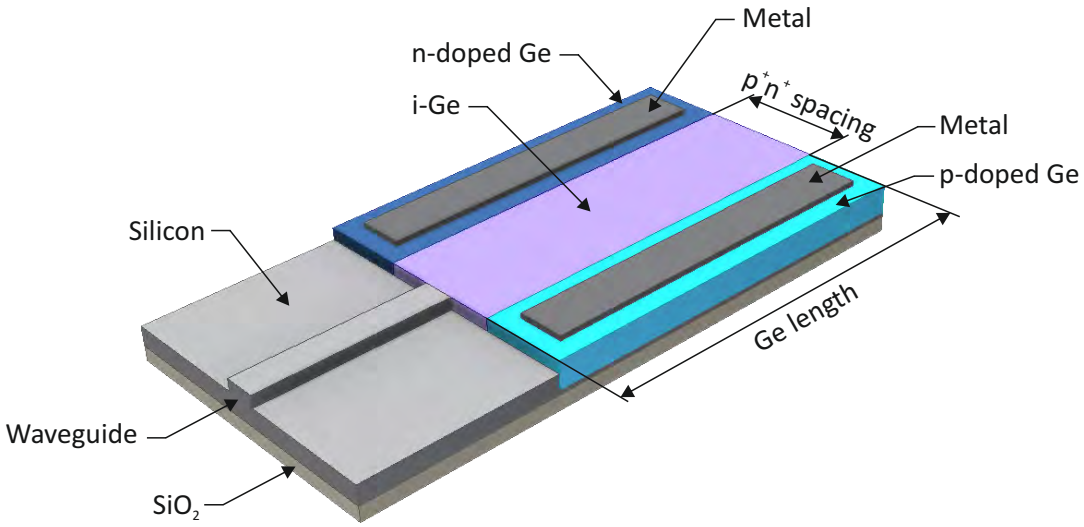


Figure 3.3: Schematic view of lateral Ge photodetector integrated at the end of the waveguide [10]

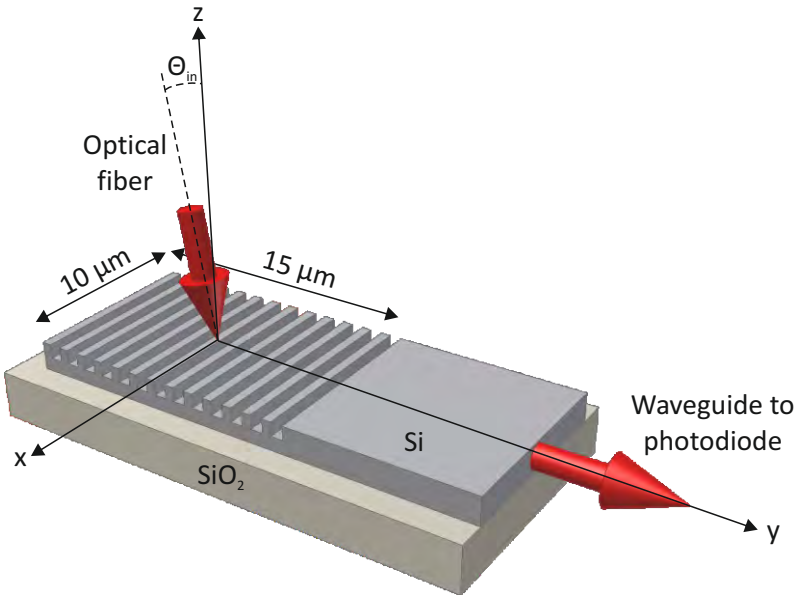


Figure 3.4: Working principle of grating coupler and waveguide

where $\overline{n_g}$ is the refractive index of the grating waveguide. Light emitted from the grating

waveguide is diffracted at a wavelength dependent angle Θ_i

$$\Theta_i = \arcsin\left(\frac{m\lambda_i - \overline{n_g}\Delta L}{\overline{n_c} d_g}\right), \tag{3.1}$$

where $\overline{n_c}$ is the refractive index of the star coupler, d_g the pitch between two neighboring grating waveguides and m the diffraction order. If ΔL and d_g are chosen according to the wavelength spacing of the multiplexed input signal, the diffracted light from each grating waveguide interferes constructively in the output star coupler and is wavelength dependent focused at the different output waveguides [39].

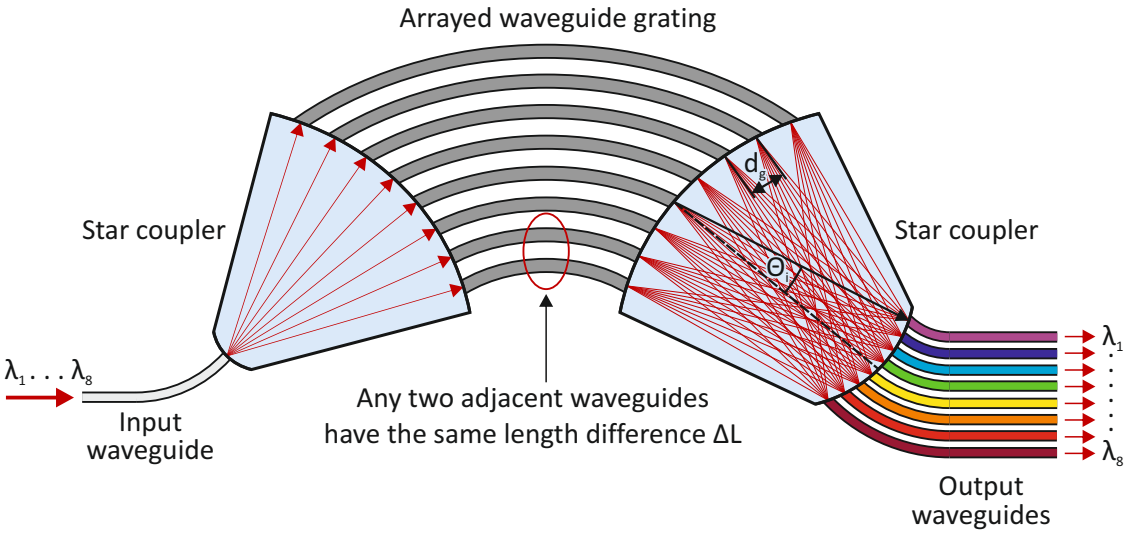


Figure 3.5: Working principle of the arrayed waveguide grating demultiplexer

The main electrical parameters as capacitance, dark current and carrier transit time depend highly on the geometrical dimensions of the detector. For instance the carrier transit time and the capacitance value per length unit mainly depend on the thickness of the intrinsic zone while the dark current and the capacitance are directly linked to the device length. Therefore CEA-LETI provided nine different lateral photodiode types, which differ in device length and spacing between p^+ and n^+ layer (see tab. 3.2).

Table 3.2: Lateral photodiode layouts

	10E05	10E07	10E1	15E05	15E07	15E1	25E07	25E1	50E1
Photodiode length (μm)	10	10	10	15	15	15	25	25	50
p^+n^+ spacing (μm)	0.5	0.7	1.0	0.5	0.7	1.0	0.7	1.0	1.0

Contrary to the vertical photodiodes provided by CEA-LETI, the lateral diodes are designed for heterogeneous integration on top of the CMOS wafer. The photonic wafer is wafer-to-wafer bonded on the CMOS wafer and the electrical connection to the CMOS circuits is established by TSVs. However, the devices used for characterization of the diode parameters came on a separate wafer without TSVs. Instead conventional ground-signal-ground (GSG) test pads were used to connect the measurement equipment. Fig. 3.6 shows the photodetector with the waveguide and the test pad structure.

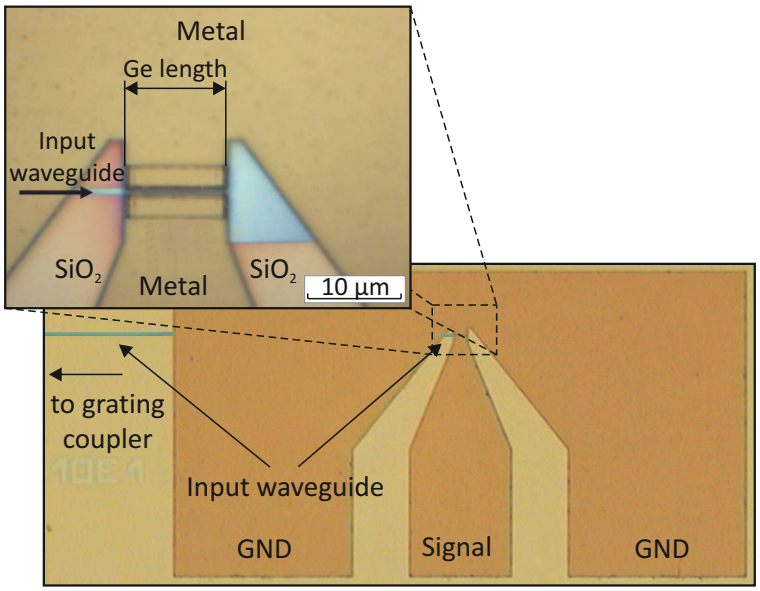


Figure 3.6: Photomicrograph CEA-LETI lateral photodetector with GSG test pads

3.2 IMEC Photodetectors

The photodetectors fabricated by IMEC are based on InP/InGaAs and use a vertical PIN structure. In contrast to the lateral Ge detectors, which are grown epitaxially in Si cavities at the end of the waveguide (see fig. 3.3), the III–V photodetectors are heterogeneously integrated on Silicon-on-Isolator (SOI) waveguide components using benzocyclobutene (BCB) die-to-wafer bonding. The heterogeneous integration is necessary to overcome the large lattice mismatch between silicon and the III–V semiconductor materials. Therefore the SOI wafer, containing the waveguide circuitry, is processed first. In a next step the unprocessed photonic dies are bonded to the SOI wafer using a BCB layer as bonding layer. After removing the III–V substrate the optical components are processed in the III–V epitaxial layer stack [40].

The diode itself consists of a 400 nm thick n-doped (10^{18} cm^{-3}) InP bottom layer, a 2 μm thick intrinsic InGaAs layer and a 100 nm thick p-doped (10^{19} cm^{-3}) InGaAs top layer. It is placed on top of the SOI waveguide wafer using a BCB polymer bonding layer. Due to the fact that there is the BCB layer between the photodiode and the SOI waveguide structure, a grating coupler, lying under the detector, is needed to diffract the light, coming from the SOI waveguide, into the photodetector. The silicon waveguide is 220 nm thick and the grating coupler uses a second order grating with a periode of 610 nm, a duty cyle of 50 % and an etch depth of 50 nm [40]. A schematic cross-section of the coupling scheme is shown in fig. 3.7.

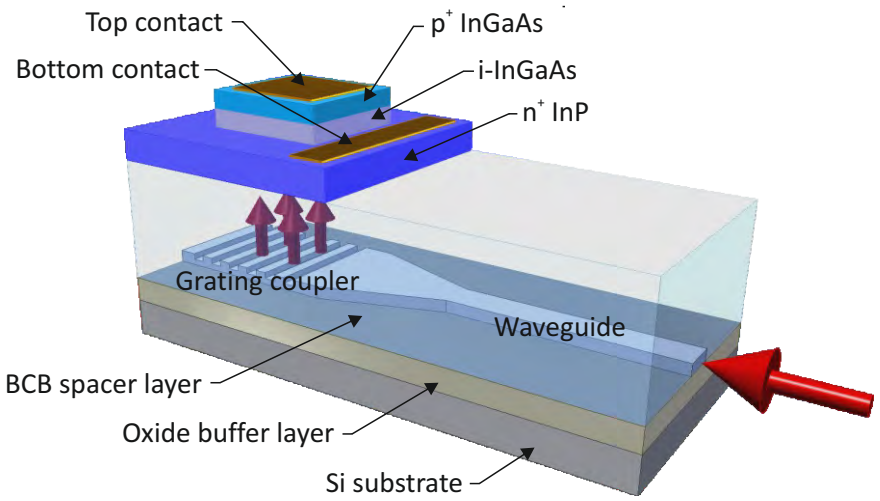


Figure 3.7: Coupling scheme of the InP/InGaAs photodetector

Like the Ge photodetectors, the III–V detectors are also designed for heterogeneous integration on top of a CMOS wafer. Instead of using flip-chip wafer-to-wafer bonding and removing the substrate by mechanical grinding and chemical etching [36], the III–V photonic wafer is cut into dies and die-to-wafer bonded on top of the CMOS wafer. The substrate of the dies is not removed and thus the thickness of the photonic die is in the range of 20 μm. In contrast to short TSVs, long Cu nails through the photonic substrate are used. These nails are isolated to the surrounding substrate by an oxide layer. The interconnection between the CMOS pads and the Cu nails is established by InCu bumps. A crosscut of the interconnection between the photonic die and the CMOS wafer is shown in fig. 3.8.

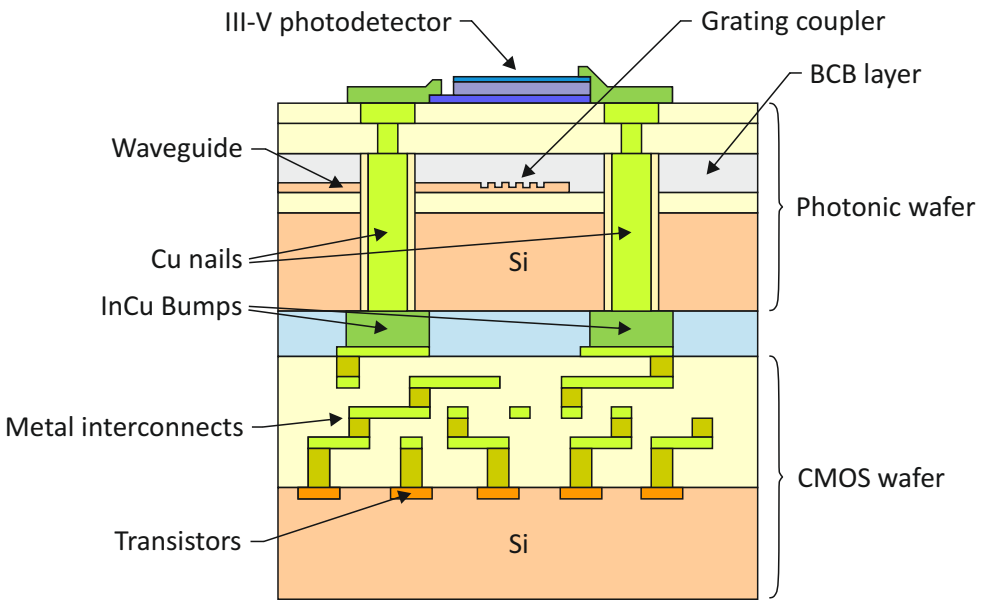


Figure 3.8: Connection structure between III–V photodetector and CMOS wafer

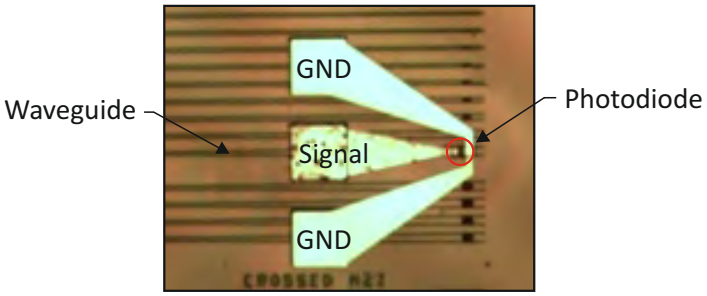


Figure 3.9: Photomicrograph of III–V photodetector with GSG test pads

Fig. 3.9 shows a photomicrograph of the III–V photodetector with GSG test pads. These test pads were only used for the characterization of the detector and will be removed on the final detector.

3.3 Measurement Setup

For the characterization of the different photodetector parameters several measurements have been made. In a first step the DC parameters as dark current, the capacitance and

the responsivity of the detectors were determined. Afterwards the AC performance of each detector was quantified by recording the AC response and the eye diagrams at different bit rates. A main issue for all measurements with exception of dark current and capacitance gauging, is the coupling of the optical signal into the detector. Due to the fact that all diodes are prototypes all measurements were carried out directly on the wafer using a SUSS PA200 semiautomatic probe system.

3.3.1 Light Coupling

Depending on the photodiode type two different coupling configurations were used. The vertical Ge diodes do not use waveguide structures and therefore the optical signal can be coupled directly from the fiber into the diode. To achieve a good coupling efficiency a tapered single mode fiber with a core diameter of 8 μm and a cladding diameter of 125 μm is used. The vertical working distance from the diode to the tip of the fiber is chosen as 20 μm which results in a light spot diameter of approximately 5 μm on the detector surface. This spot size is selected to ensure that the whole light beam which leaves the fiber is focused within the active area of the diode. This is crucial because a light spot larger than the size of the active area can result in incorrect responsivity and AC measurements. Another important factor for a good coupling efficiency is the correct beam position in the horizontal plane. An optical alignment using the microscope of the probe system is impossible due to the fact that the thick fiber cladding obscures the vision to the diode and the tapered fiber tip. Thus a photocurrent measurement is used to align the fiber. In a first step a 1550 nm laser source with constant output power is connected to the fiber and the fiber is placed coarsely over the diode. In the next step the x and y position of the fiber are varied until the photocurrent is maximized and thus the optimal fiber position is found.

For the diodes with grating coupler and waveguide a different coupling configuration was used. Since the used grating coupler is a so-called 1-D coupler only one polarization plane (e.g. TE) is coupled from the fiber into the waveguide [41]. Therefore a polarization maintaining (PM) Panda fiber is used to couple the optical signal into the grating coupler (see fig. 3.10). The maximum coupling efficiency is reached when the slow axis (TE) of the Panda fiber is aligned parallel to the grating structure. Furthermore the longitudinal axis of the fiber has to be tilted $7^\circ - 10^\circ$ in respect to the vertical axis to avoid second order reflection at the grating [42].

Beside the correct axis alignment of the fiber, a accurate fiber position in the horizontal plane is necessary to achieve an optimal coupling efficiency. Due to the fact that the grating coupler, which is only 10×15 μm^2, is entirely covered by the fiber (125 μm in diameter) it is impossible to align the fiber using the prober microscope. Therefore again the photocurrent for a constant optical power is used to find out the optimal fiber position.

Compared to the diodes without waveguide the fiber alignment for the grating coupler is

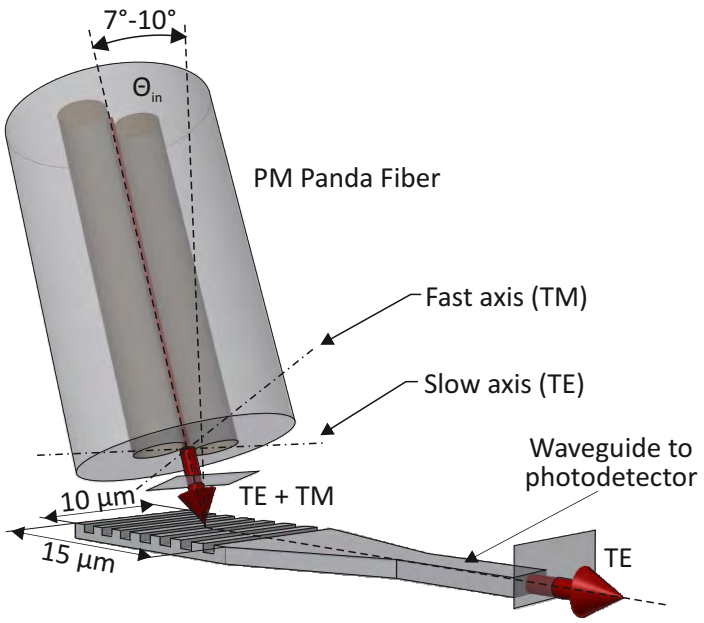


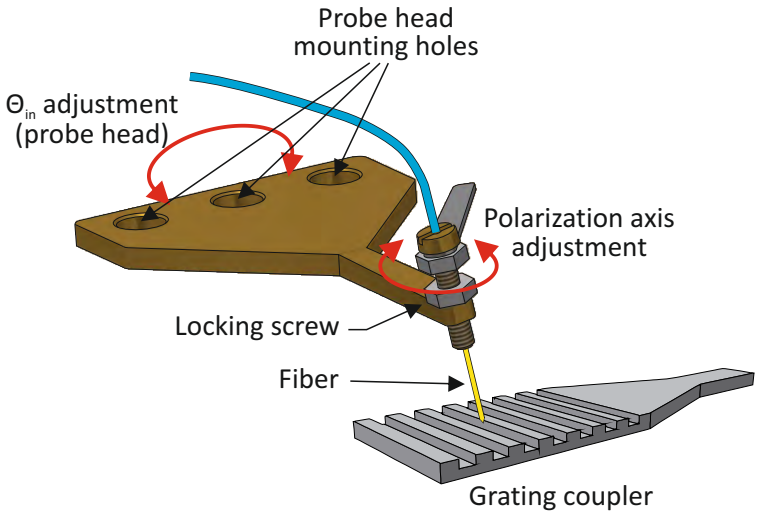
Figure 3.10: Coupling configuration of 1-D grating coupler

much more complicated due to the fact that five parameters (distance between fiber and grating, angle between fiber and vertical axis, polarization axis, x and y position) must be considered. Therefore a special fiber holder was developed (see fig. 3.11(a)). The fiber holder is designed to be mounted on a SUSS PH120 manual probe head instead of a GSG Z-Probe. The polarization axis of the fiber is adjusted on the fiber holder itself while the probe head is used to adjust the angle Θ_{in} and the x, y and z position of the fiber. A photograph of the fiber holder mounted on the SUSS PH120 probe head is shown in fig. 3.11(b).

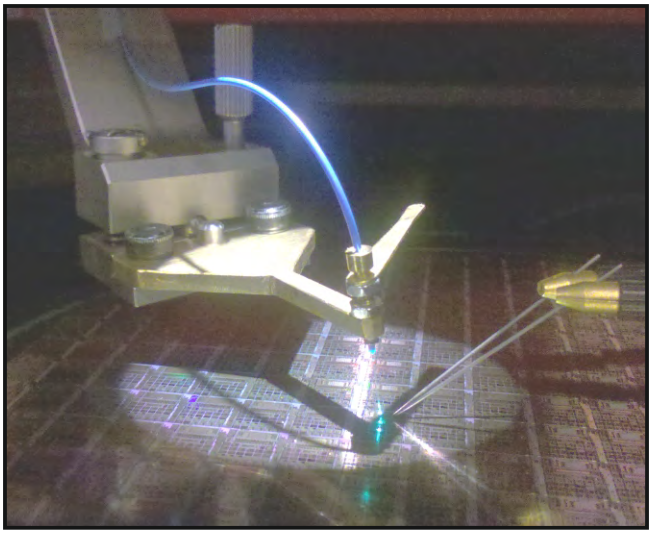
3.3.2 Responsivity Measurement

The responsivity R of a photodiode is defind as the ratio of the photocurrent I_{ph} to the incident optical power P_{opt} at a certain wavelength (2.14). A high responsivity of the photodetector is crucial for building an optical receiver with high sensitivity.

The principle of the responsivity measurement is shown in fig. 3.12. As light source a continuous wave (CW) laser source with a wavelength of 1550 nm is used. The light coming from the laser source is split by a 50:50 optical splitter into two optical signals with identical optical power. From the splitter one output fiber leads to a Ophir Nova laser power meter which determines the optical power of the light beam. The second output fiber from the splitter leads to the photodiode (DUT). Due to the use of a splitter with a



(a)



(b)

Figure 3.11: 3-D model (a) and photograph of mounted fiber holder (b)

ratio of 50:50 light with the same optical power as determined by the optical power meter irradiates into the photodiode. The diode itself is reverse biased (2.0 V for the Ge diodes and 6.0V for the InP/InGaAs diodes) and the photocurrent generated by the incident light is measured. In a last step the responsivity of the photodetector is calculated using (2.14).

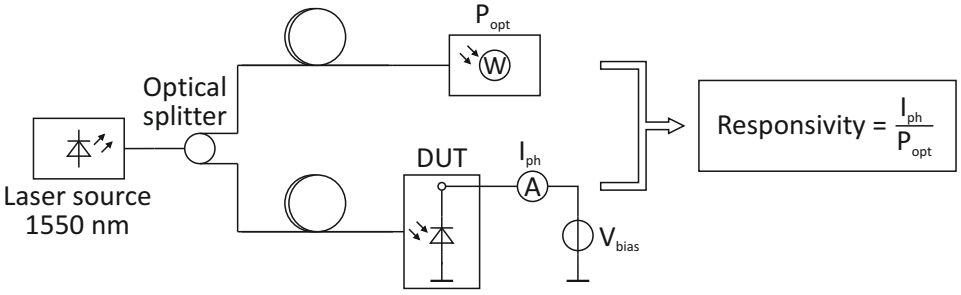


Figure 3.12: Responsivity measurement principle

3.3.3 Dark Current Measurement

The dark current I_{dark} is defined as the current that flows through the reverse biased photodiode in the absence of light. It is a combination of bulk leakage and surface currents and increases with the applied bias voltage V_{bias}. On the other hand it strongly depends on the used semiconductor material and the geometrical dimensions of the diode. The slope of the dark current curve at small reverse bias voltages is represented by R_p in the photodiode model (see fig. 2.8).

In a typical optical receiver the photodiode is DC coupled to the amplifier input stage. Therefore the operating point of the input stage is influenced strongly by the dark current of the photodiode. Another problem is the shot noise which is generated in the photodiode due to the dark current. It is also amplified and contributes to the overall noise of the optical receiver. Therefore the dark current is a critical parameter for the design of an optical receiver and should be kept as low as possible. On the other hand the speed of a typical photodiode strongly depends on the applied bias voltage. If the applied bias voltage increases, the electric field inside the SCR of the diode also increases. The charge carriers are increasingly accelerated and the diode gets faster. Therefore the value of the applied bias voltage is always a tradeoff between dark current and photodetector speed.

The principle of the dark current measurement is shown in fig. 3.13. The photodiode

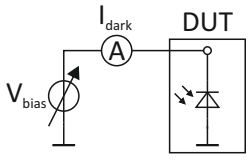


Figure 3.13: Principle of dark current measurement

(DUT) is reverse biased and the dark current is measured in the absence of light. As

bias voltage source and as ampere meter a Keithley 2612 dual-channel system source meter, which is controlled by a short LabVIEW application, was used. Depending on the photodiode type V_{bias} was increased from $0-2$ V for the Ge diodes and from $0-7$ V for the InP/InGaAs diodes in 0.1 V steps and the corresponding dark current was metered.

3.3.4 Capacitance Measurement

The performance of an optical receiver also depends strongly on the capacitance of the used photodiode. A large capacitance limits the -3 dB cutoff frequency of the receiver (2.27) and can lead to gain-peaking which can cause stability problems (see fig. 2.19). Therefore it is necessary for the design of a fast optical receiver to choose a photodiode with a low capacitance.

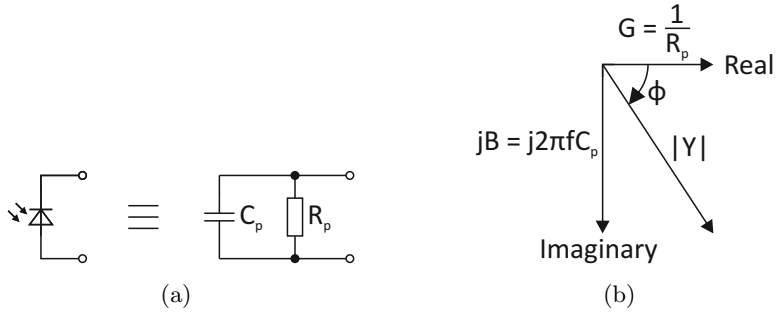
The capacitance of the photodiode was measured using an Agilent HP4284A LCR meter. The capacitance measurement is based on the determination of the admittance Y of the diode at a certain frequency f in the absence of light. The admittance Y contains a real and an imaginary part, which can be either expressed in rectangular form as conductance G and susceptance B, or in polar form as magnitude of admittance $|Y|$ and phase ϕ:

$$Y = G + jB \tag{3.2}$$

$$|Y| = \sqrt{G^2 + B^2} \tag{3.3}$$

$$\phi = arctan\left(\frac{|B|}{G}\right) \tag{3.4}$$

For the measurement of the photodiode capacitance the serial resistor R_s in fig. 2.8 is neglected and the equivalent circuit shown in fig. 3.14(a) is used. The corresponding vector representation of the admittance is shown in fig. 3.14(b).



(a) (b)

Figure 3.14: Equivalent circuit (a) and admittance vector representation (b) of a photodiode

Together with the known test frequency f the photodiode capacitance C_p can be calculated directly by

$$C_p = \frac{B}{2\pi f}. \tag{3.5}$$

To avoid any mutual inductance, interference of the measurement signals and unwanted residual factors of the connection method which may effect the measurements, a four-terminal pair measurement configuration as shown in fig. 3.15 was used.

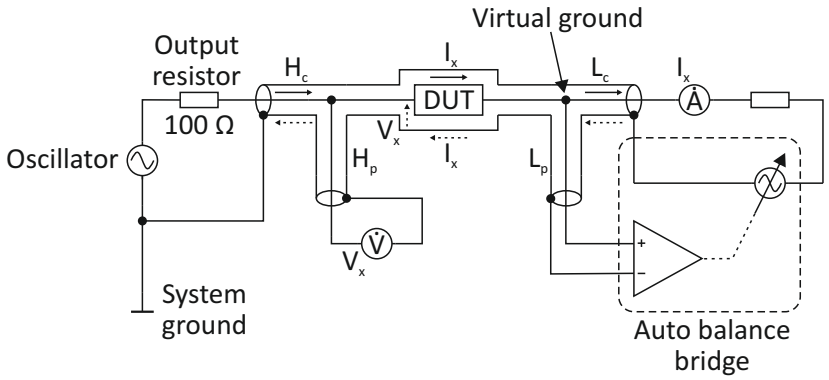


Figure 3.15: Four-terminal pair capacitance measurement principle

The photodiode (DUT) is reverse biased and an AC signal with an amplitude of 10 mV and a frequency of 1 MHz is applied. To calculate the admittance of the photodiode the amplitude of V_x and I_x and the phase between them are determined. The outer shield conductors work as return path for the measurement signal current. The same current flows through the center conductors and the outer shield conductors in opposite directions. The magnetic fields produced by the inner and outer currents cancel out each other and no external magnetic fields are generated around the conductors. Thus the measurement signal current does not produce an inductive magnetic field and the test leads do not contribute additional errors.

Depending on the diode type the bias voltage was increased in 0.25 V steps for the vertical Ge diodes from $0-2$ V and for the InP/InGaAs diodes in 0.5 V steps from $0-4$ V. Due to the large dark current, caused by the low parallel resistance R_p of the lateral Ge diodes, the bias voltage was only increased in 50 mV steps from $0-0.25$ V in this case.

Due to the fact that the lateral Ge diodes as well as the InP/InGaAs diodes will be heterogeneously integrated in the final version, the GSG test pads will be replaced by TSVs. TSVs have much lower parasitic capacitances than GSG test pads and therefore the capacitance of the test pads was nulled out by calibration to measure only the capacitance which will be effective at the TIA input node. On the other hand the capacitance of the vertical Ge diodes, which will be wire bonded, was measured together with the bond pads

because in this case the effective capacitance at the TIA input node is the sum of the pad and the diode capacitance.

3.3.5 Serial Resistance Measurement

The serial resistance of a photodiode consists of the anode and cathode contact resistances and the resistance of the undepleted low doped zones of the diode. Normally it can be neglected for PIN photodiodes if the intrinsic zone is fully depleted and carrier drift dominates. Therefore the serial resistance of the lateral Ge 10E1 diode was measured only exemplarily.

The serial resistance of the photodiode is determined by recording the Smith diagram of the S11 parameter in the frequency range from 45 MHz − 50 GHz and calculating R_s by coefficient extraction. Fig. 3.16 shows the measurement principle and the equivalent circuit used for the coefficient extraction. The coefficient extraction itself was performed with MICROWAVE OFFICE®, a RF/microwave design software, and the known values of C_p and R_p.

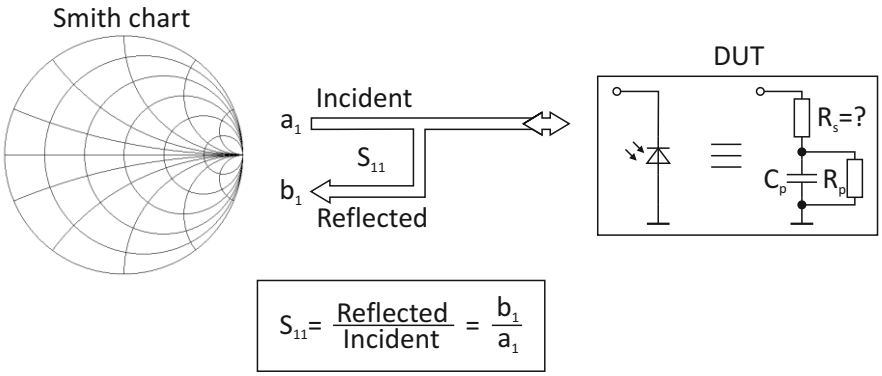


Figure 3.16: Block diagram of serial resistance measurement

3.3.6 AC Response

The speed of the photodetectors was measured by determining their AC response using an vector network analyzer (VNA). A block diagram of the measurement setup is shown in fig. 3.17. The frequency response of the photodiode is determined by measuring the S21 parameter in the frequency range 45 MHz − 50 GHz with an Agilent E8364A PNA vector network analyzer. Port a of the VNA is connected to a Photline DR-DG-40-MO 40 GHz modulator driver module which drives a Photline MX-LN-40 40 GHz Mach-Zehnder modulator. The light from the 1550 nm CW laser source is modulated by the

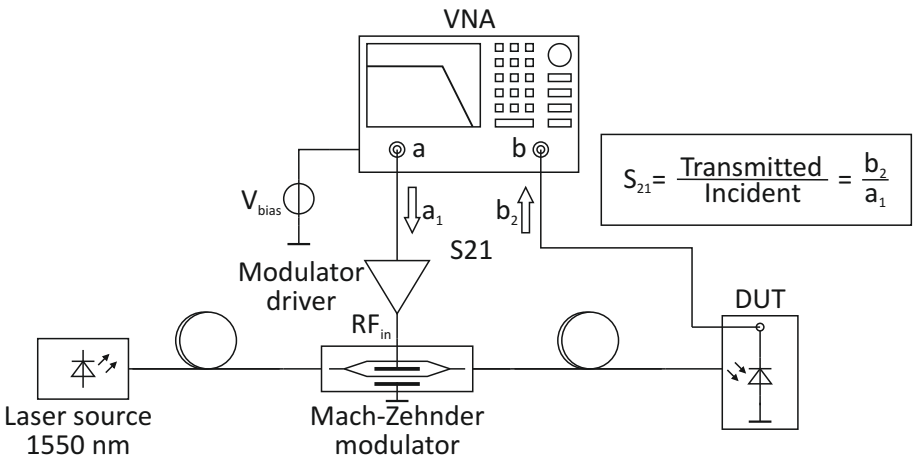


Figure 3.17: Block diagram of AC response measurement

RF-signal RF_{in} and irradiates into the photodiode (DUT). The photodiode is reverse biased by the VNA and the photocurrent generated by the modulated light is detected at port b. To determine the frequency response of the photodiode RF_{in} is swept from 45 MHz up to 50 GHz and the S21 parameter is plotted over the input frequency RF_{in}.

To eliminate the influence of the frequency response of the used cables, the modulator driver, the Mach-Zehnder modulator and the network analyzer itself an ultrafast InGaAs PIN DSC10ER photodiode from Discovery Semiconductors, Inc. with a flat frequency response up to 60 GHz was used as reference detector. For the calibration the DUT was replaced by the reference diode and the network analyzer was used to null out the frequency responses of all components in the measurement setup. After successful calibration the frequency response shown on the VNA is a flat line at 0 dB over the entire frequency range. In the next step the reference diode is replaced with the DUT again and the AC response of the photodiode can now be measured without the influence of other components.

Depending on the photodiode type the AC response was measured at reverse bias voltages V_{bias} from $0 - 2$ V for the Ge diodes and from $0 - 7$ V for the InP/InGaAs diodes.

3.3.7 Eye Diagram Measurement

The eye diagrams of the photodiodes were recorded to verify the results of the frequency response measurement and to determine other diode parameters as SNR or raise and fall times. A block diagram of the measurement setup is shown in fig. 3.18.

A 40 GHz Sympuls BPG bit pattern generator is used to generate a PRBS31 bit pattern which is used to modulate a 1550 nm CW laser by a Mach-Zehnder modulator. To

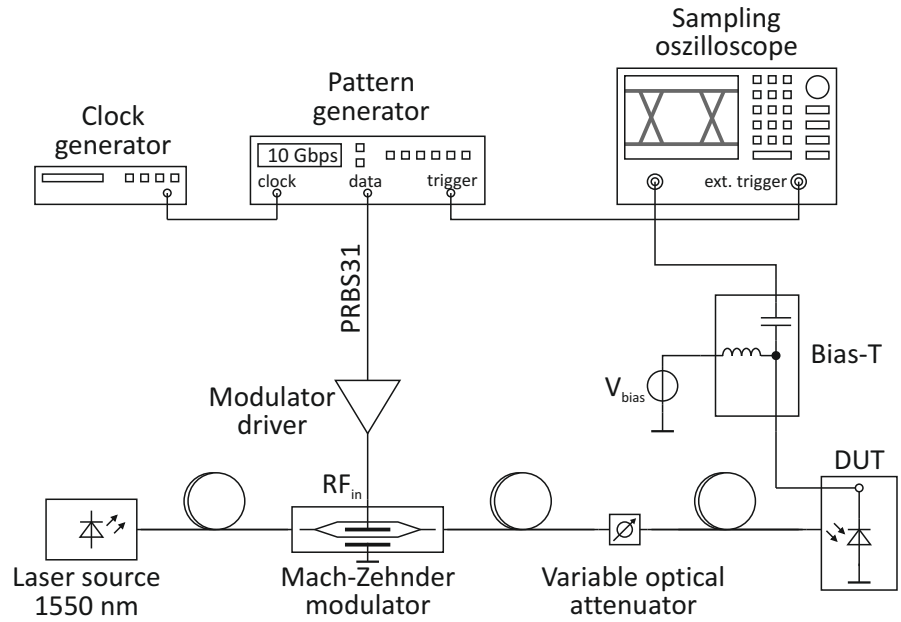


Figure 3.18: Block diagram eye diagram measurement

determine the SNR of the photodiode an optical attenuator is used to adjust the light power. Due to the fact that the input of the used Tektronix DSA 8200 digital sampling oscilloscope is very sensitive to DC voltages, a Bias-T is used to reverse bias the photodiodes. The incident optical PRBS31 signal leads to a photocurrent that is detected by the sampling oscilloscope and due to the external triggering by the pattern generator a standing eye is created on the screen.

For the measurement of the eye diagram following bias voltages were used for the different photodiode types:

Table 3.3: Bias voltages of eye diagram measurement

	vertical Ge (T559A P23)	lateral Ge (V985H)	InP/InGaAs (IMEC)
Bias voltage (V)	2.0	1.0	6.0

3.4 Measurement Results

3.4.1 CEA-LETI T559A Vertical Ge Photodetectors

Responsivity

The responsivity of the different vertical Ge photodiode types measured at a wavelength of 1550 nm is in the range of 0.5 A/W (see tab. 3.4). These results are not really astonishing due to the fact that the diameter of the active diode area is the only difference between the various detector types. Furthermore it can be concluded that the scattering losses caused by the light coupling from the fiber into the diode are constant even at the smallest diode. Nevertheless the measured responsivities are only moderate compared to other state-of-the-art vertically illuminated Ge photodiodes [43].

Table 3.4: Responsivity of CEA-LETI vertical Ge photodetectors

	PIN1	PIN2	PIN3	PIN4	PIN5	PIN6	PIN7
Responsivity (A/W)	0.50	0.49	0.49	0.51	0.49	0.49	0.50

Dark Current

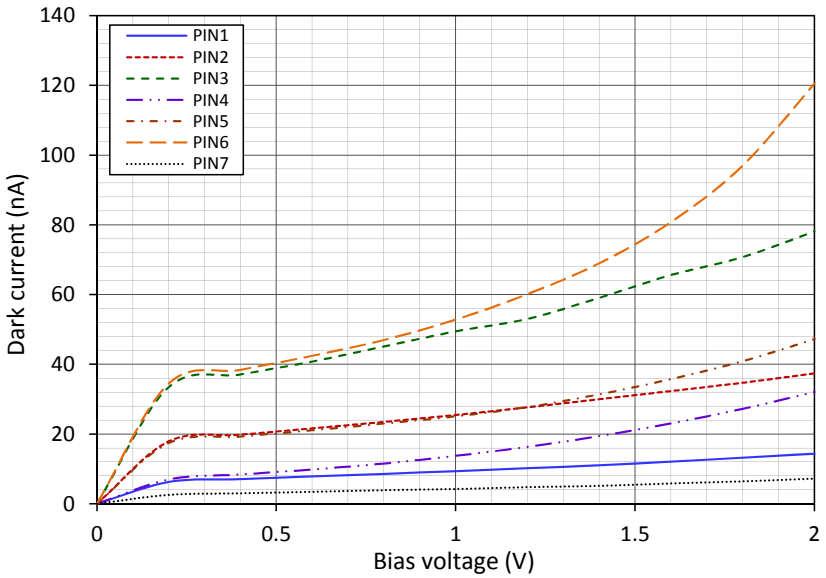


Figure 3.19: Dark current of CEA-LETI vertical Ge photodetectors

Fig. 3.19 shows the dark current measurement results of the different vertical Ge photodiodes. It can be seen that the dark current depends mainly on the detector size – the smaller the diode, the lower the dark current. This can be explained by the fact that the thicknesses of the p^+, the n^+ and the intrinsic Ge layer are the same for all diode types. At increasing reverse bias voltage there seems to be an additional influence caused by the different top contact ring widths of the diodes. Diodes with a thicker contact ring show a higher dark current than diodes with a thinner contact ring.

Capacitance

The capacitance measurement results show a direct relation between the photodiode area and its capacitance. The measured capacitances remain nearly constant for increasing bias voltages above 0.5 V. This effect can be explained by the thickness of the SCR. The depletion region gets thicker with increasing bias voltage until the intrinsic zone of the diode is fully depleted (in this case above 0.5 V). Due to the fact that the depletion region cannot expand further into the high doped p^+ and n^+ regions the thickness of the SCR (and thus the capacitance) stays nearly constant at further increasing bias voltages. The capacitances of the different diode types in dependence on the applied bias voltage are shown in fig. 3.20.

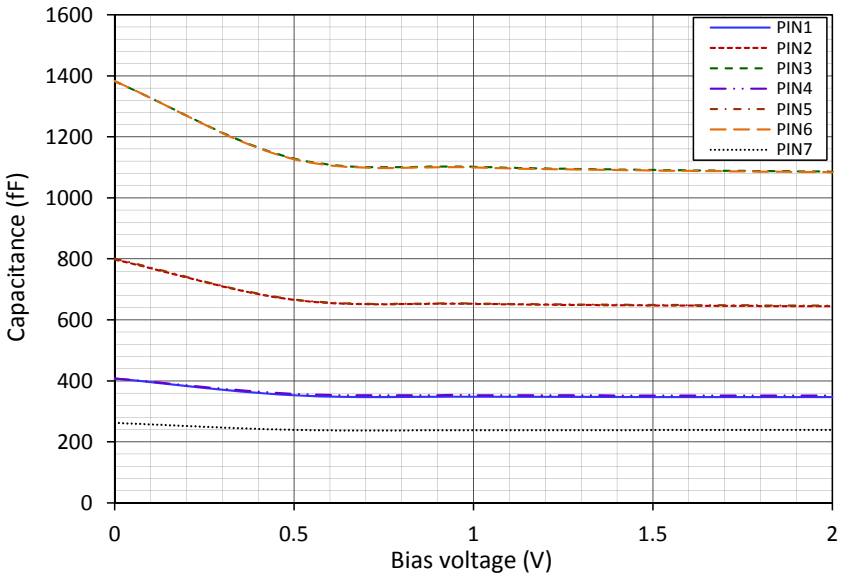


Figure 3.20: Capacitance of CEA-LETI vertical Ge photodetectors

AC Response

Fig. 3.21 – 3.27 show the AC responses of the various photodiodes at different bias voltages. The bandwidths of all diode types increase strongly in the voltage range $0 - 0.5$ V while they stay nearly constant at higher bias voltages. This behavior can be explained by the dependence between diode capacitance and applied reverse voltage (see fig. 3.20). The bias voltage dependent capacitance of the photodiode forms together with the impedance of the measuring equipment a low pass. Therefore the AC responses of the characterized Ge photodiodes show the behavior of a first order low pass filter. Only the AC response of diode PIN7 shows the behavior of a high-order low-pass filter for frequencies above 20 GHz which is caused by calibration artifacts (see fig. 3.27).

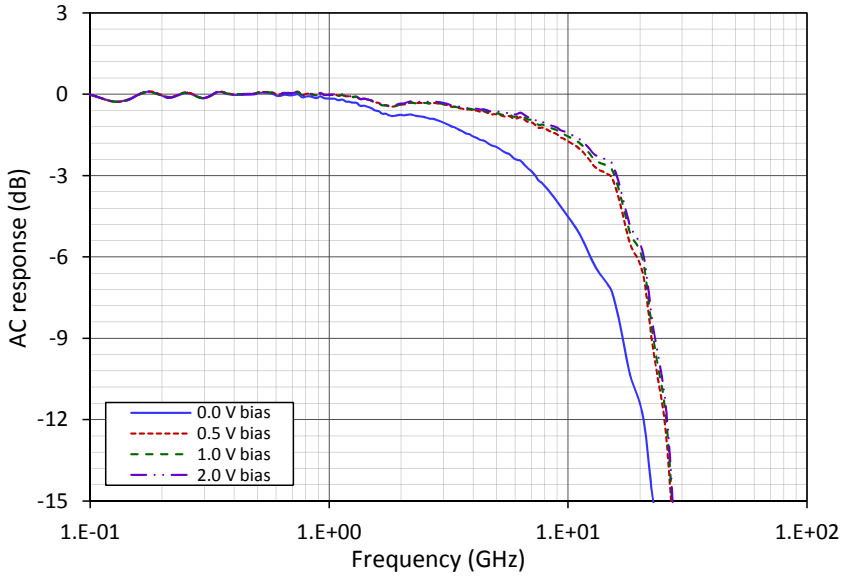


Figure 3.21: AC response of CEA-LETI PIN1 Ge photodetector at different bias voltages

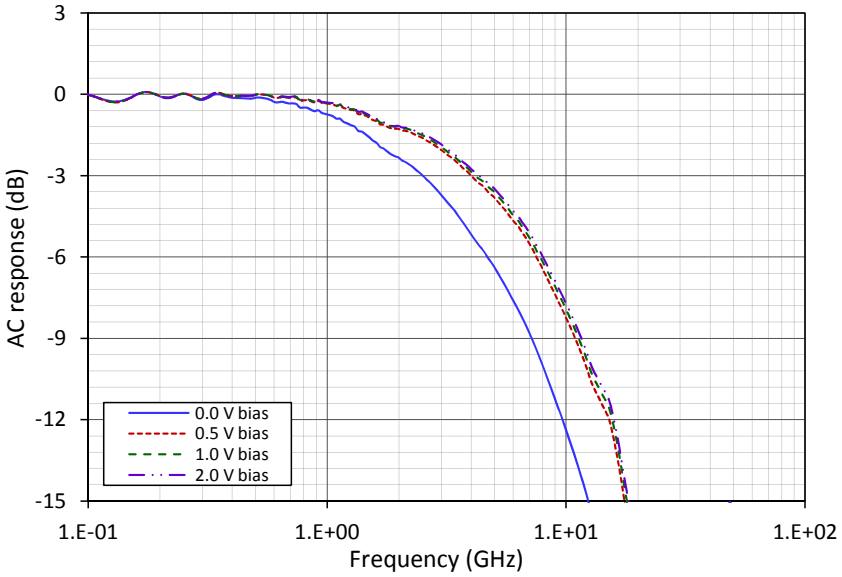


Figure 3.22: AC response of CEA-LETI PIN2 Ge photodetector at different bias voltages

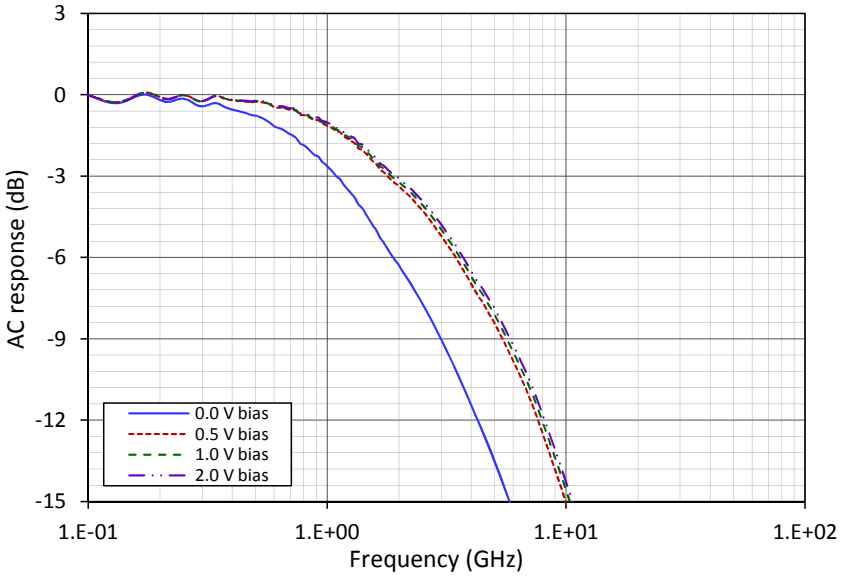


Figure 3.23: AC response of CEA-LETI PIN3 Ge photodetector at different bias voltages

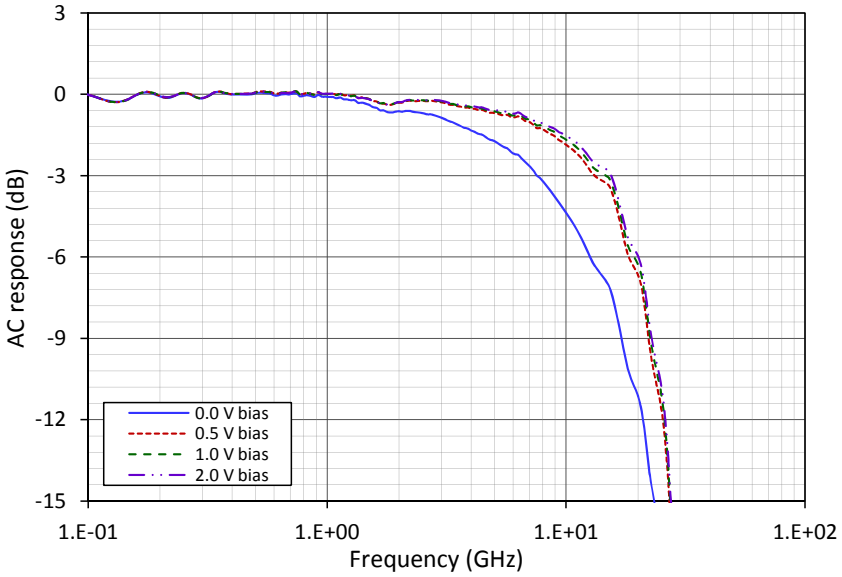


Figure 3.24: AC response of CEA-LETI PIN4 Ge photodetector at different bias voltages

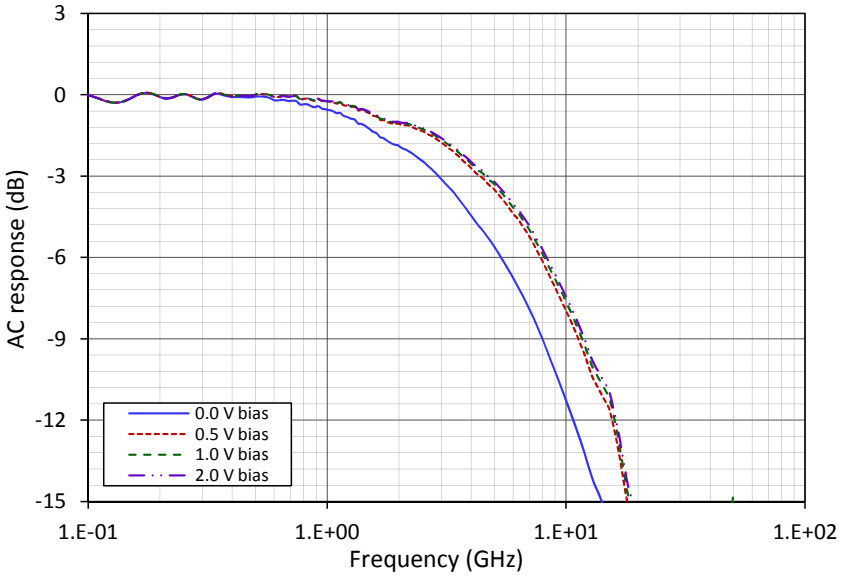


Figure 3.25: AC response of CEA-LETI PIN5 Ge photodetector at different bias voltages

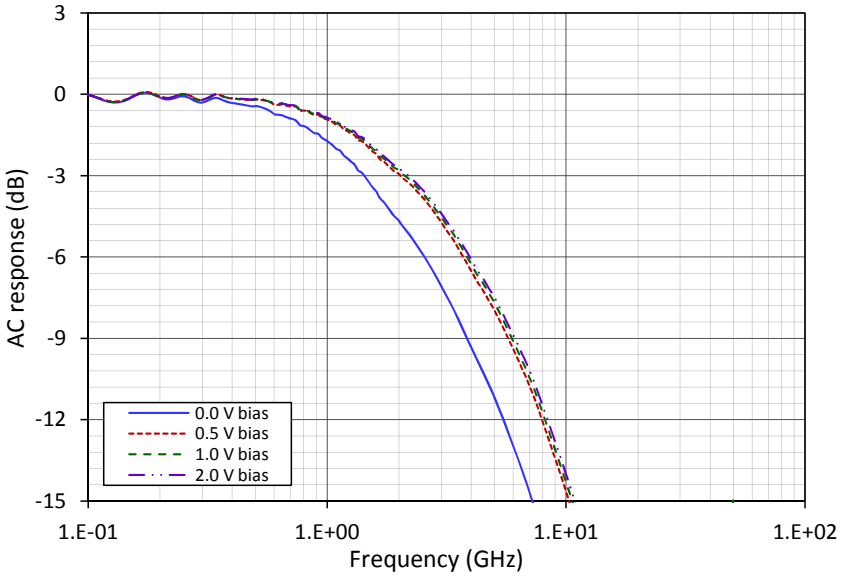


Figure 3.26: AC response of CEA-LETI PIN6 Ge photodetector at different bias voltages

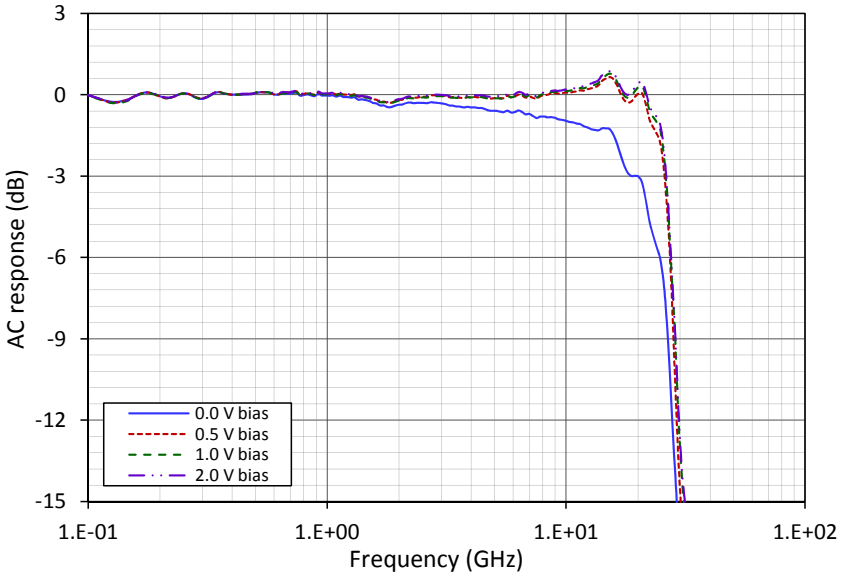
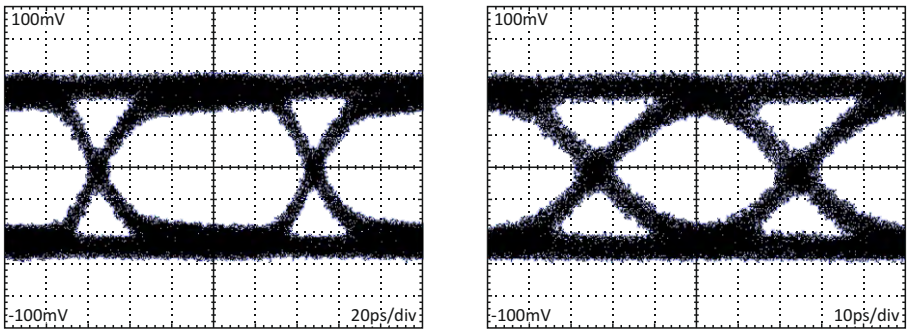


Figure 3.27: AC response of CEA-LETI PIN7 Ge photodetector at different bias voltages

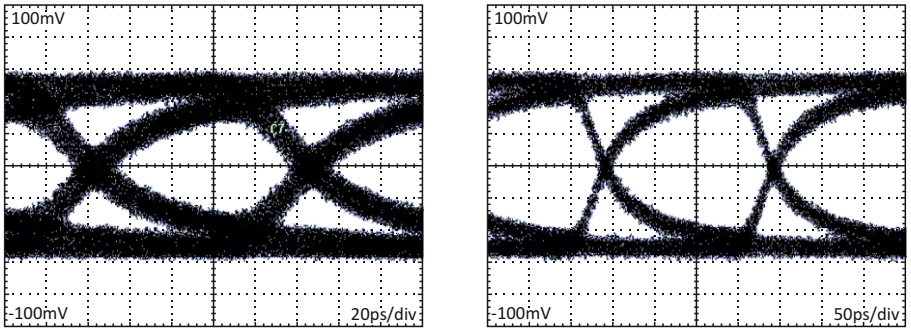
Eye Diagram

The eye diagrams recorded at different data rates confirm in general the results of the AC response measurement. The photodiode types PIN2, PIN3, PIN5 and PIN6 having a -3 dB cutoff frequency smaller than 7 GHz are not capable of a data rate of 10 Gbps (see fig. 3.29, 3.30, 3.32 and 3.33) while the photodiodes PIN1, PIN4 and PIN7 are fast enough to obtain the required data rate (see fig. 3.28, 3.31 and 3.34).



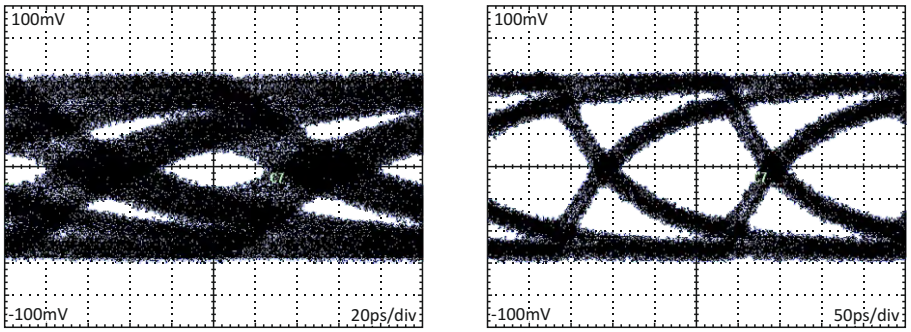
(a) (b)

Figure 3.28: Eye diagram of PIN1 photodetector at 10 Gbps (a) and at 20 Gbps (b)



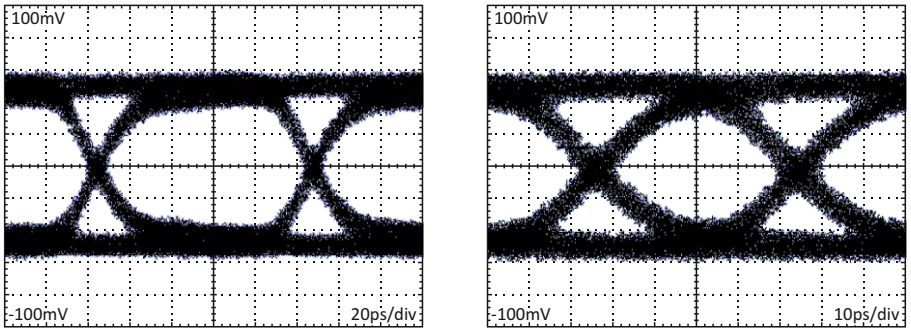
(a) (b)

Figure 3.29: Eye diagram of PIN2 photodetector at 10 Gbps (a) and at 5 Gbps (b)



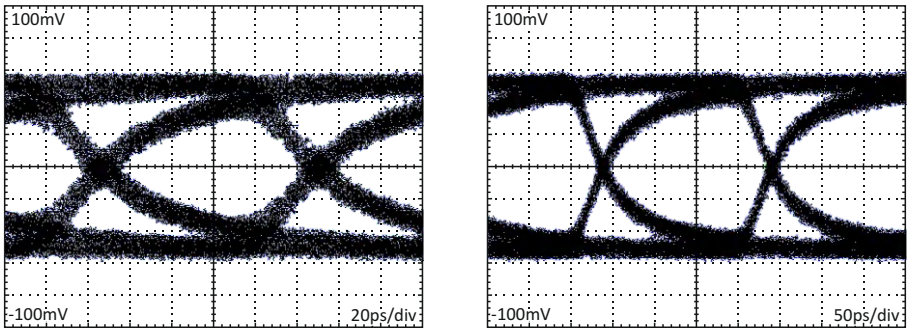
(a) (b)

Figure 3.30: Eye diagram of PIN3 photodetector at 10 Gbps (a) and at 5 Gbps (b)



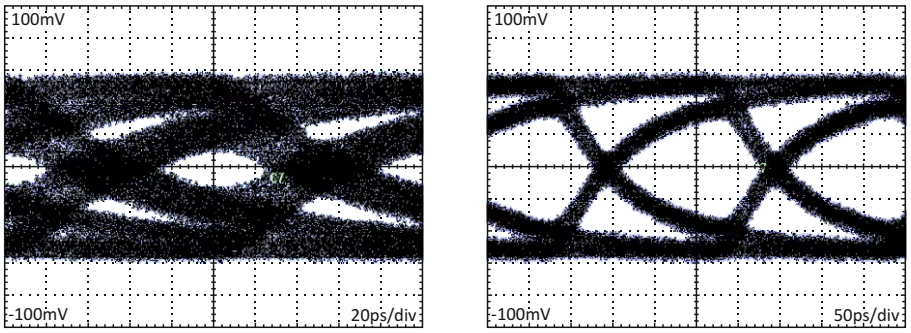
(a) (b)

Figure 3.31: Eye diagram of PIN4 photodetector at 10 Gbps (a) and at 20 Gbps (b)



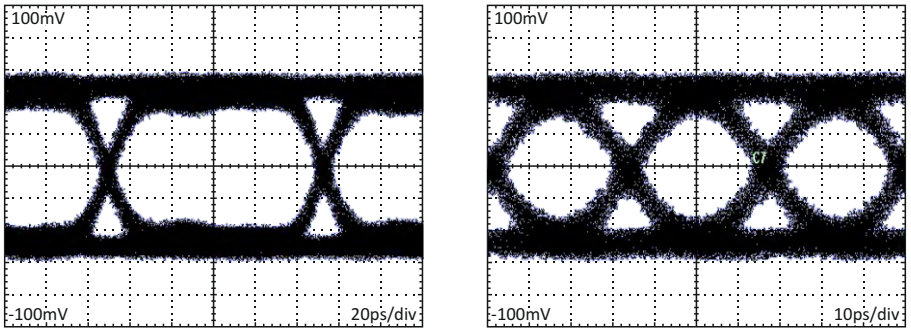
(a) (b)

Figure 3.32: Eye diagram of PIN5 photodetector at 10 Gbps (a) and at 5 Gbps (b)



(a) (b)

Figure 3.33: Eye diagram of PIN6 photodetector at 10 Gbps (a) and at 5 Gbps (b)



(a) (b)

Figure 3.34: Eye diagram of PIN7 photodetector at 10 Gbps (a) and at 30 Gbps (b)

3.4.2 CEA-LETI V985H Lateral Ge Photodetectors

Responsivity

The responsivity measurement results of the lateral Ge photodetectors show a strong dependence on the geometrical dimensions of the different photodiodes (fig. 3.5). The responsivity rises at increasing p^+n^+ spacing and increasing diode length. This dependence can be explained on one hand by the varying coupling efficiency between the waveguide and the intrinsic zone for different p^+n^+ spacing and on the other hand by the relation between diode length and penetration depth $1/\alpha$ (see fig. 2.2). Nevertheless the responsivities of all photodiode types are poor compared to state-of-the-art waveguide Ge detectors [44], [45].

Table 3.5: Responsivity of CEA-LETI lateral Ge photodetectors

	10E05	10E07	10E1	15E05	15E07	15E1	25E07	25E1	50E1
Responsivity (A/W)	0.08	0.11	0.15	0.09	0.13	0.19	0.19	0.24	0.26

Serial Resistance

Normally the serial resistance of PIN photodiodes can be neglected, if the intrinsic zone is fully depleted and carrier drift is dominating. Therefore only the serial resistance of the lateral Ge 10E1 photodetector was measured exemplarily (tab. 3.6).

Table 3.6: Serial resistance of lateral 10E1 Ge photodetector

R_s	R_p	C_p
30 Ω	1 MΩ	20 fF

Dark Current

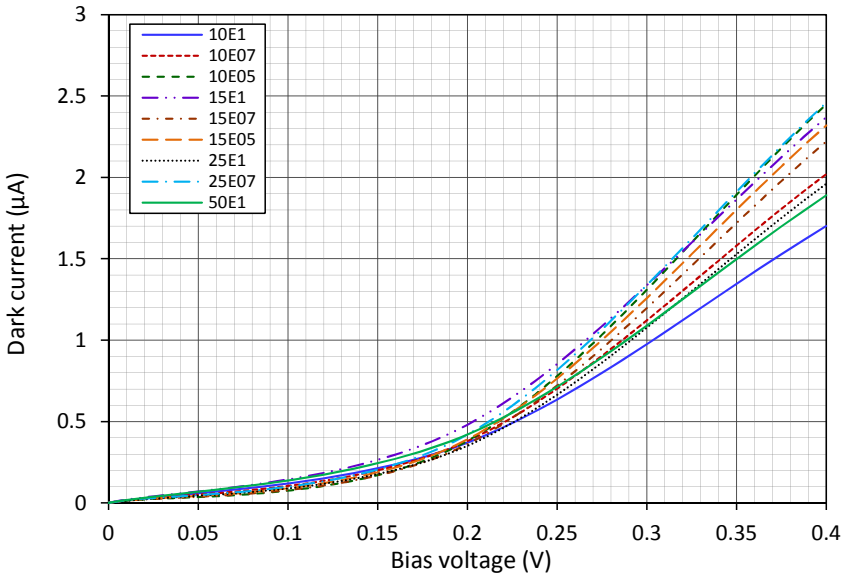


Figure 3.35: Dark current of CEA-LETI lateral Ge photodetectors

Fig. 3.35 shows the measured dark current of the different lateral Ge photodiodes in dependence on the applied bias voltage. The dark current increases strongly for bias

voltages larger than 0.25 V for all diode types. The relatively large dark current shows a dependence on the p^+n^+ spacing – the larger the p^+n^+ spacing, the smaller the dark current.

Capacitance

Fig. 3.36 shows the capacitances of the various lateral Ge photodiodes in dependence on the applied bias voltage. Due to the above mentioned high dark current it was only possible to measure the diode capacitances at low bias voltages. In general, it can be stated that the capacitance depends mainly on the length (size) of the diode while the thickness of the intrinsic zone influences the capacitance only minor.

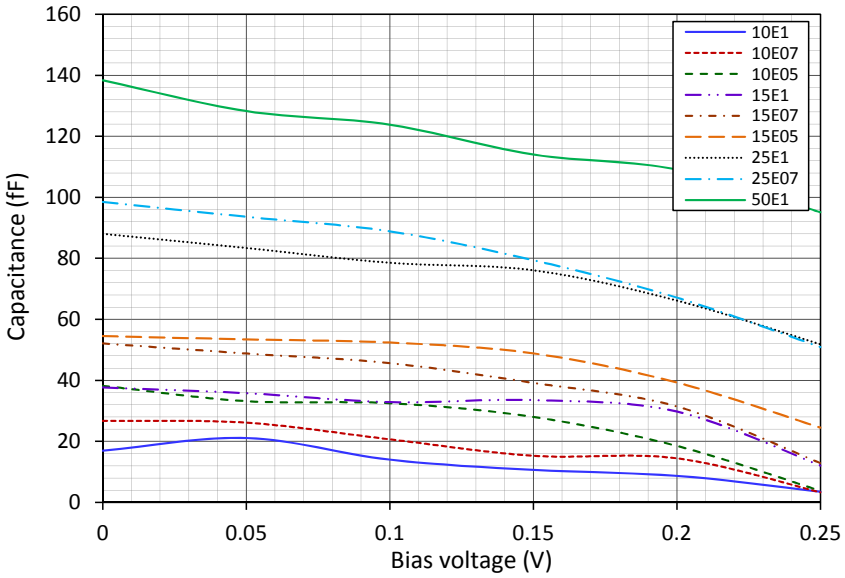


Figure 3.36: Capacitance of CEA-LETI lateral Ge photodetectors

AC Response

The frequency responses of the different lateral photodiode types in dependence on the applied bias voltages are shown in fig. 3.37 – 3.45. The −3 dB cutoff frequencies of the various diodes show a dependence on the diode lengths and the thicknesses of the p^+n^+ spacing. In general it can be stated that the smaller and thinner the diode, the larger the bandwidth. For instance, the small and thin diode type 10E05 reaches −3 dB cutoff frequencies around 50 GHz even without biasing (fig. 3.37) while the large diode 50E1 has a bandwidth of only 20 GHz at 2.0 V bias voltage (fig. 3.45).

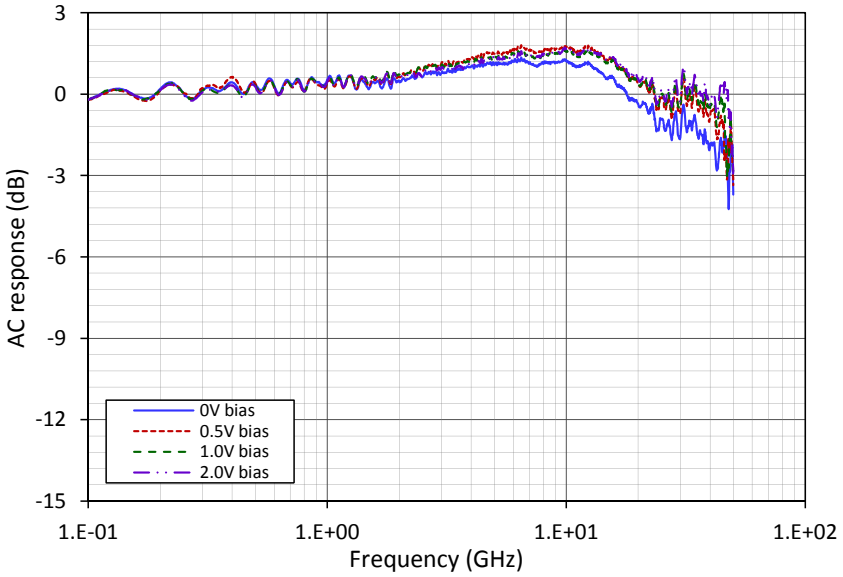


Figure 3.37: AC response of CEA-LETI 10E05 Ge photodetector at different bias voltages

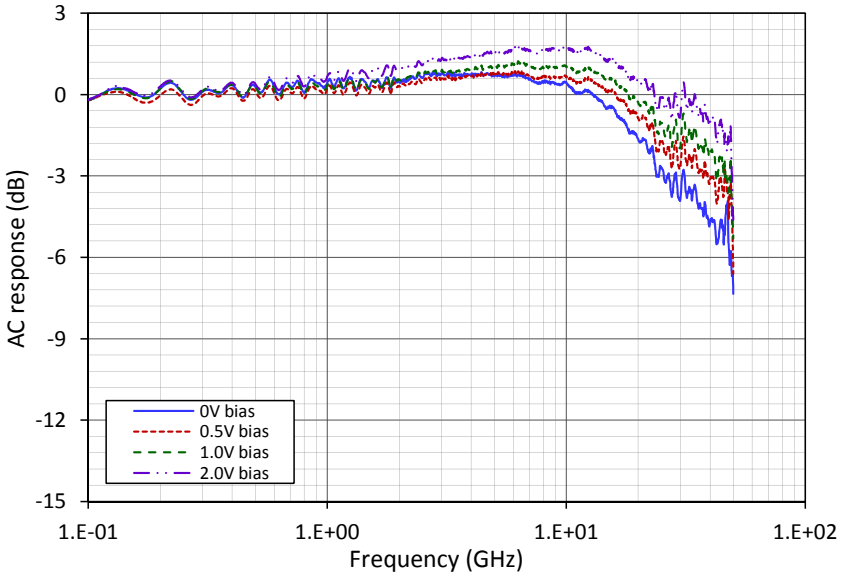


Figure 3.38: AC response of CEA-LETI 10E07 Ge photodetector at different bias voltages

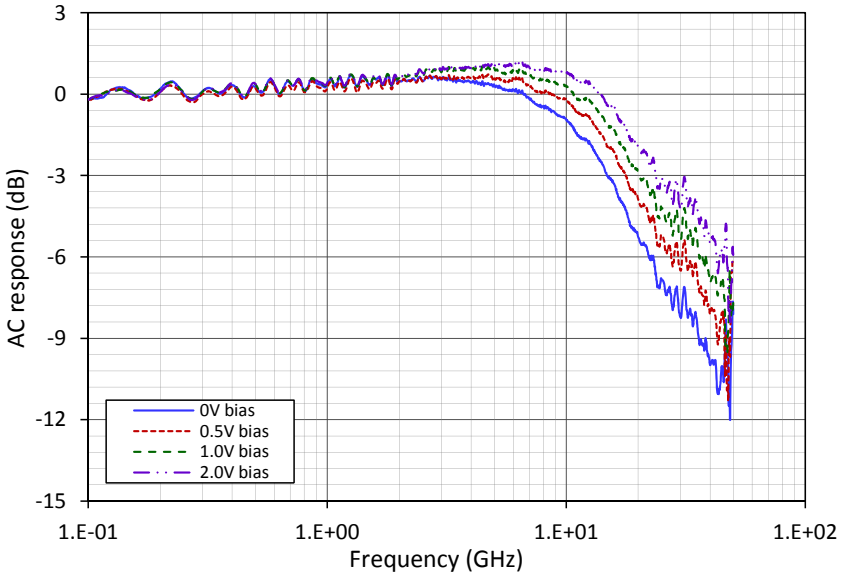


Figure 3.39: AC response of CEA-LETI 10E1 Ge photodetector at different bias voltages

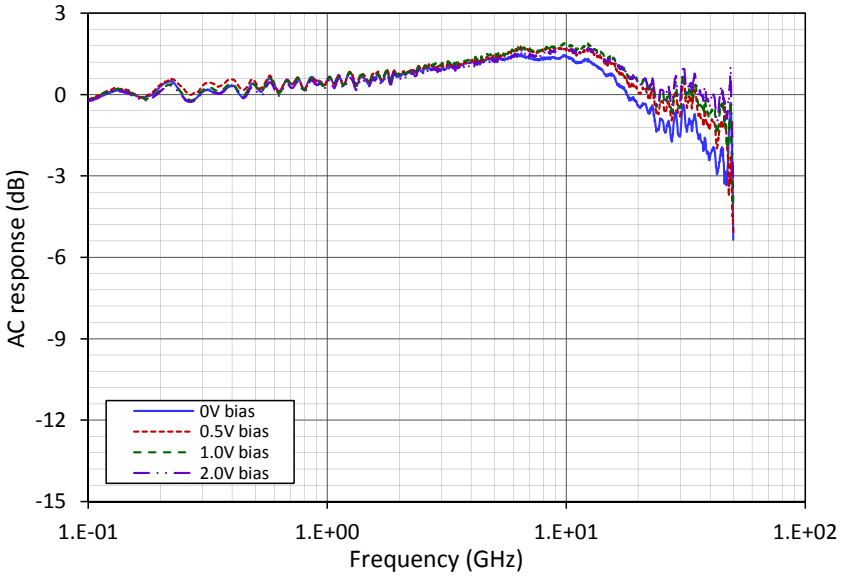


Figure 3.40: AC response of CEA-LETI 15E05 Ge photodetector at different bias voltages

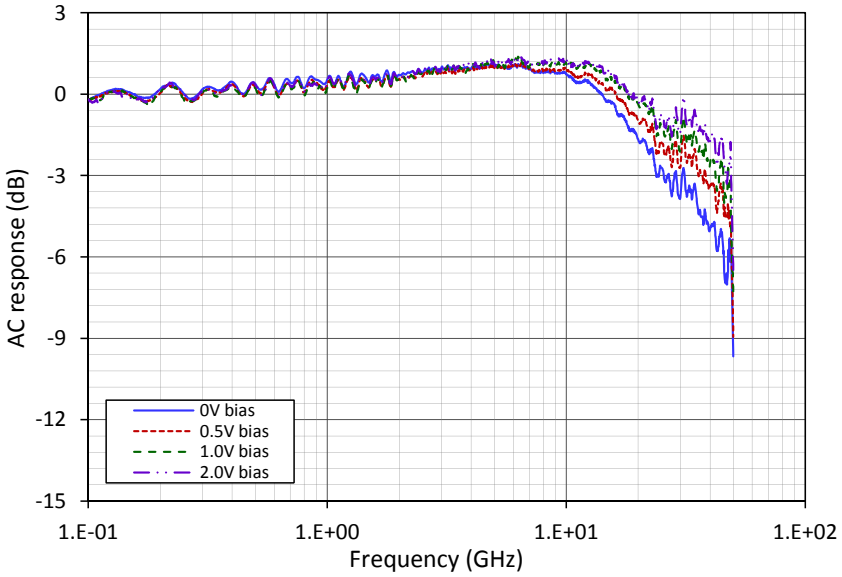


Figure 3.41: AC response of CEA-LETI 15E07 Ge photodetector at different bias voltages

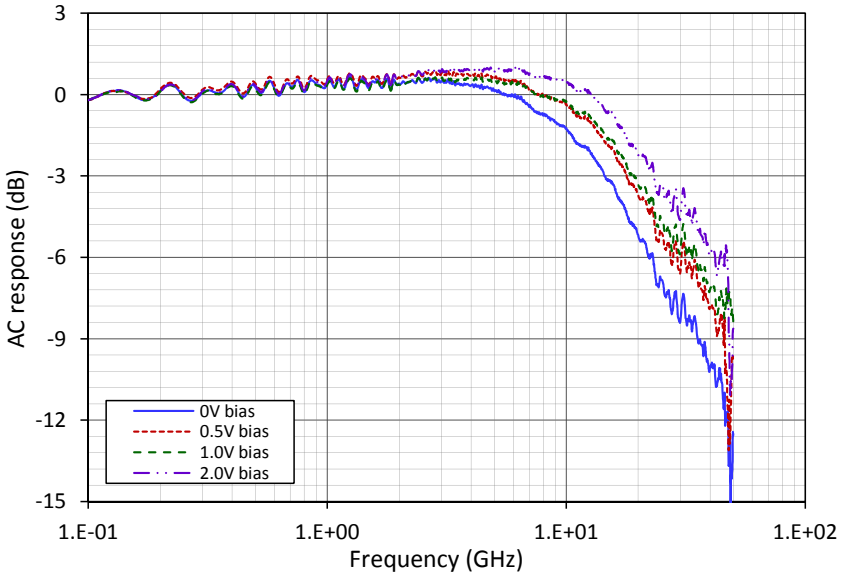


Figure 3.42: AC response of CEA-LETI 15E1 Ge photodetector at different bias voltages

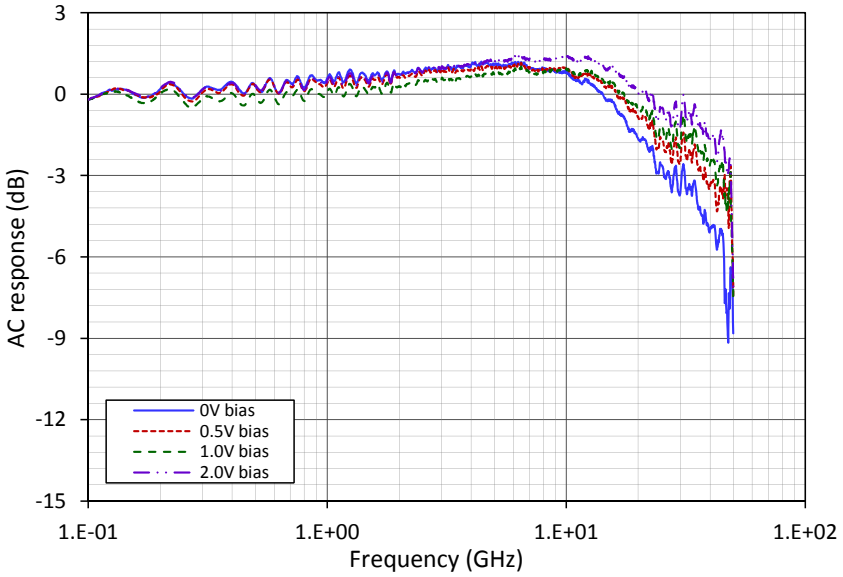


Figure 3.43: AC response of CEA-LETI 25E07 Ge photodetector at different bias voltages

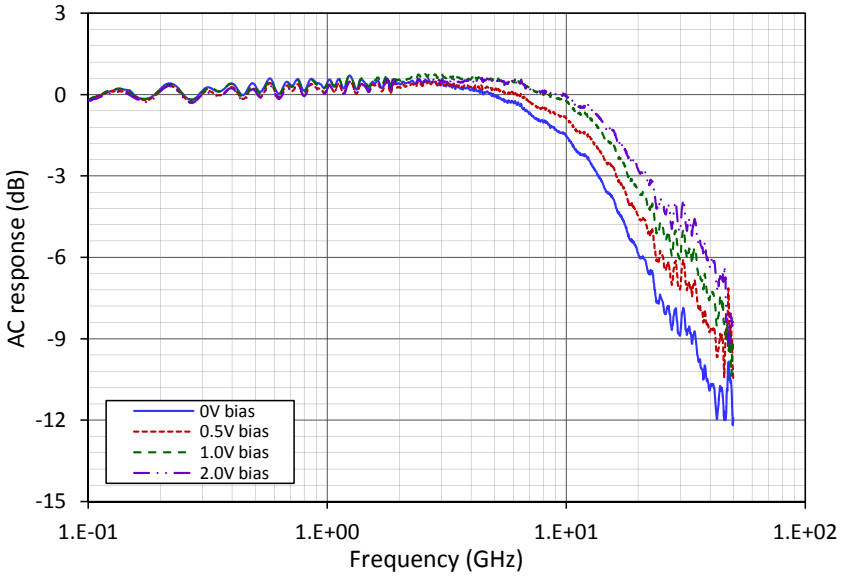


Figure 3.44: AC response of CEA-LETI 25E1 Ge photodetector at different bias voltages

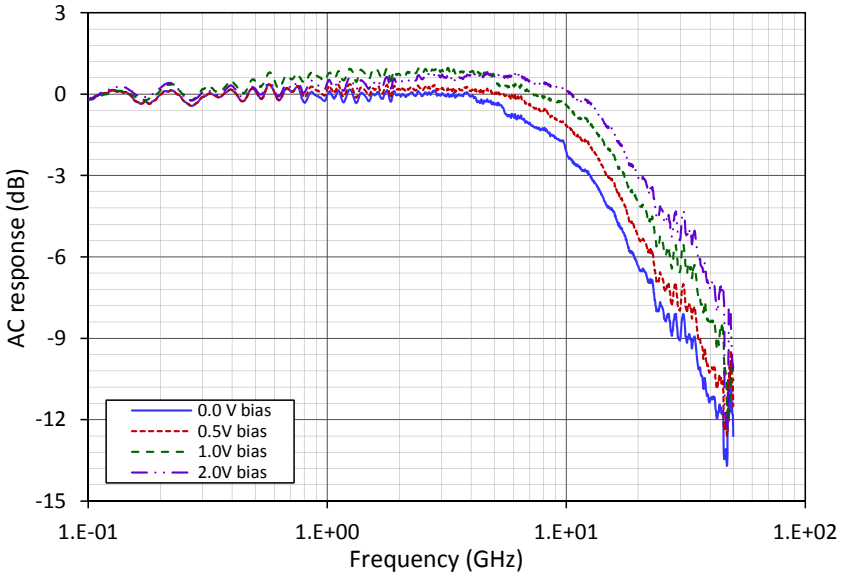
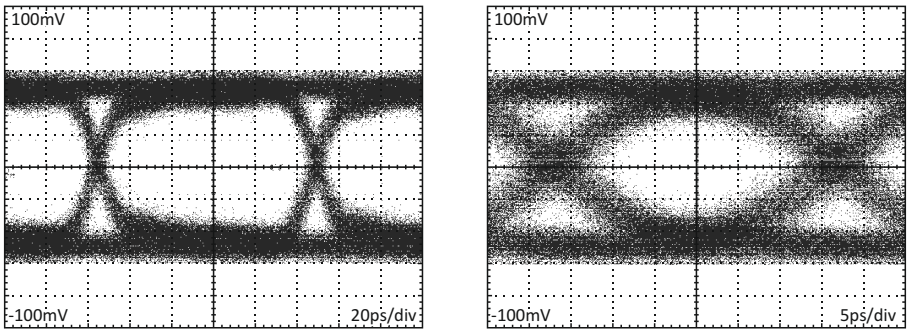


Figure 3.45: AC response of CEA-LETI 50E1 Ge photodetector at different bias voltages

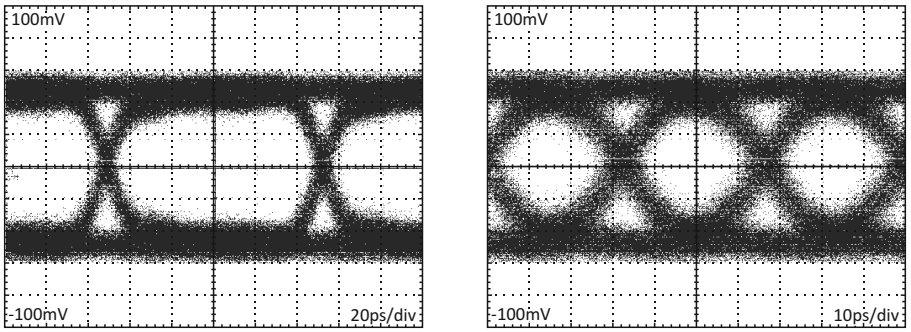
Eye Diagram

The eye diagrams of the different lateral Ge photodiodes recorded at different data rates are shown in fig. 3.46 – 3.54. The eye diagrams confirm the frequency response measurements – each photodetector is capable of a data rate of at least 10 Gbps.



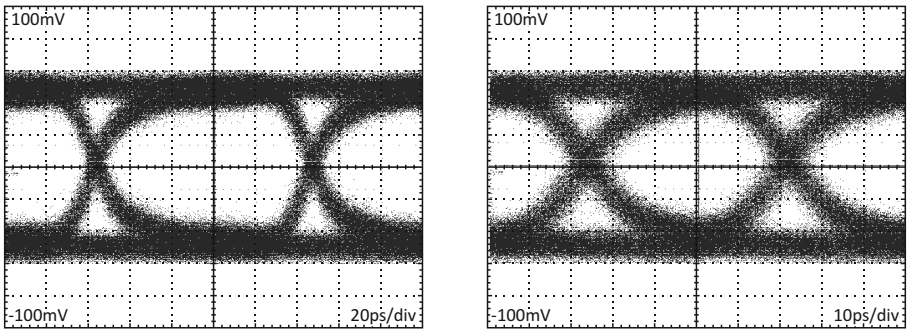
(a) (b)

Figure 3.46: Eye diagram of 10E05 photodetector at 10 Gbps (a) and at 30 Gbps (b)



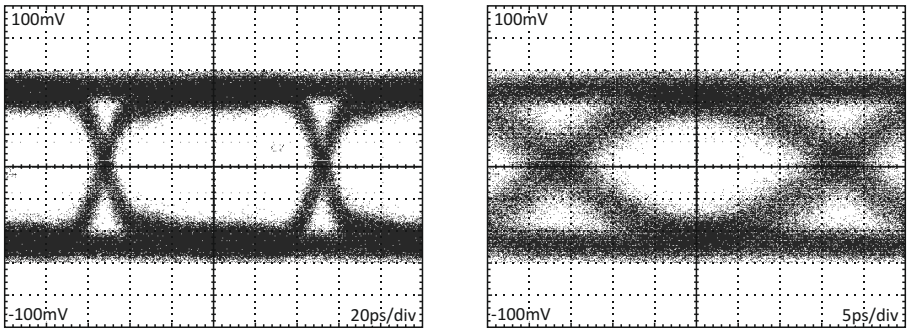
(a) (b)

Figure 3.47: Eye diagram of 10E07 photodetector at 10 Gbps (a) and at 30 Gbps (b)



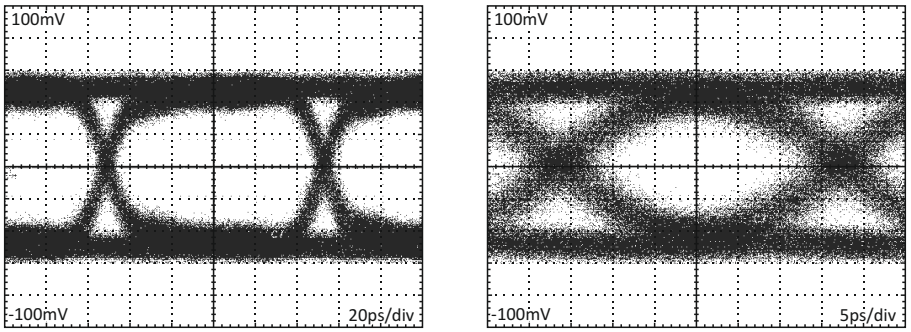
(a) (b)

Figure 3.48: Eye diagram of 10E1 photodetector at 10 Gbps (a) and at 20 Gbps (b)



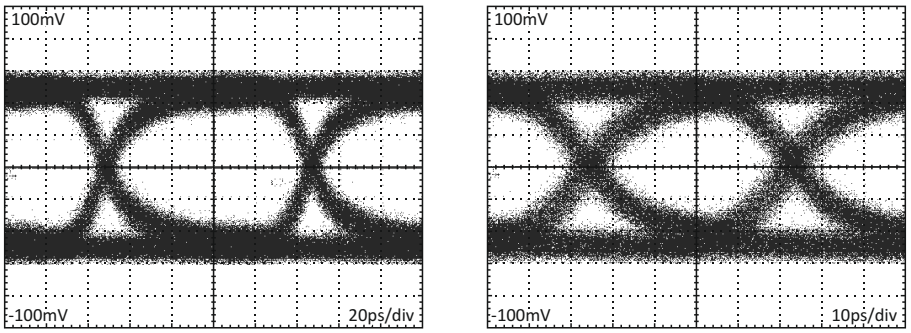
(a) (b)

Figure 3.49: Eye diagram of 15E05 photodetector at 10 Gbps (a) and at 30 Gbps (b)



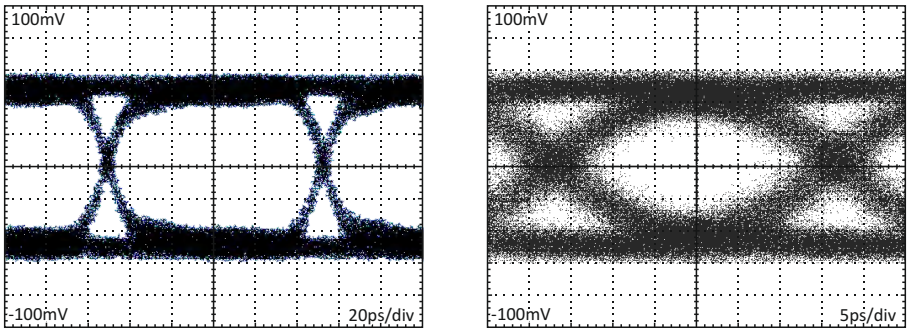
(a) (b)

Figure 3.50: Eye diagram of 15E07 photodetector at 10 Gbps (a) and at 30 Gbps (b)



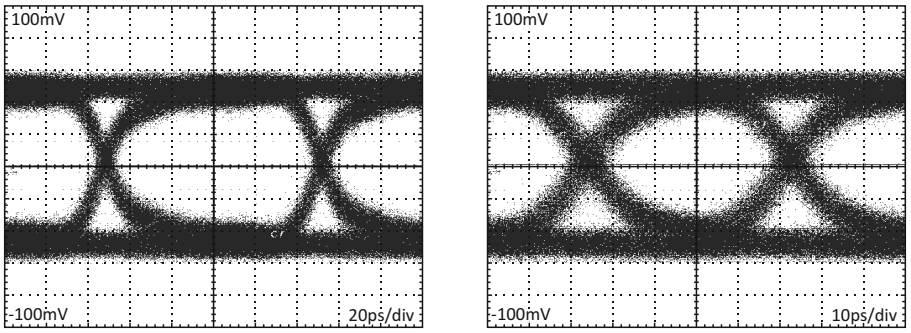
(a) (b)

Figure 3.51: Eye diagram of 15E1 photodetector at 10 Gbps (a) and at 20 Gbps (b)



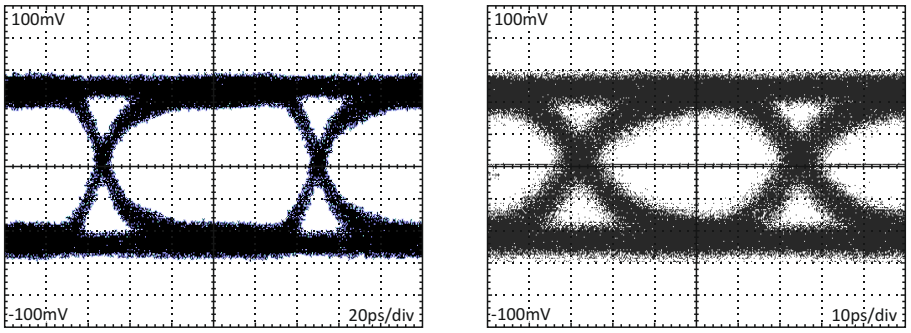
(a) (b)

Figure 3.52: Eye diagram of 25E07 photodetector at 10 Gbps (a) and at 30 Gbps (b)



(a) (b)

Figure 3.53: Eye diagram of 25E1 photodetector at 10 Gbps (a) and at 20 Gbps (b)



(a) (b)

Figure 3.54: Eye diagram of 50E1 photodetector at 10 Gbps (a) and at 20 Gbps (b)

3.4.3 IMEC InP/InGaAs Photodetector

Responsivity

The responsivity of the waveguide InP/InGaAs photodiode is also relatively low compared to state-of-the-art photodetectors [46]. Together with the coupling losses of the grating coupler and the waveguide losses the measured responsivity is only 0.14 A/W (tab. 3.7).

Table 3.7: Responsivity of IMEC InP/InGaAs photodetector

	IMEC InP/InGaAs
Responsivity (A/W)	0.14

Dark Current

Fig. 3.55 shows the dark current of the InP/InGaAs photodiode in dependence on the applied bias voltage. Compared to the Ge photodiodes (see chapters 3.4.1 and 3.4.2) the InP/InGaAs photodetector has a relative low dark current for bias voltages below 3.0 V. At higher bias voltages the dark current increases faster and reaches 330 nA at a bias voltage of 7.0 V. Such high bias voltages are needed by the InP/InGaAs photodiode to obtain a high bandwidth (see chapter 3.4.3).

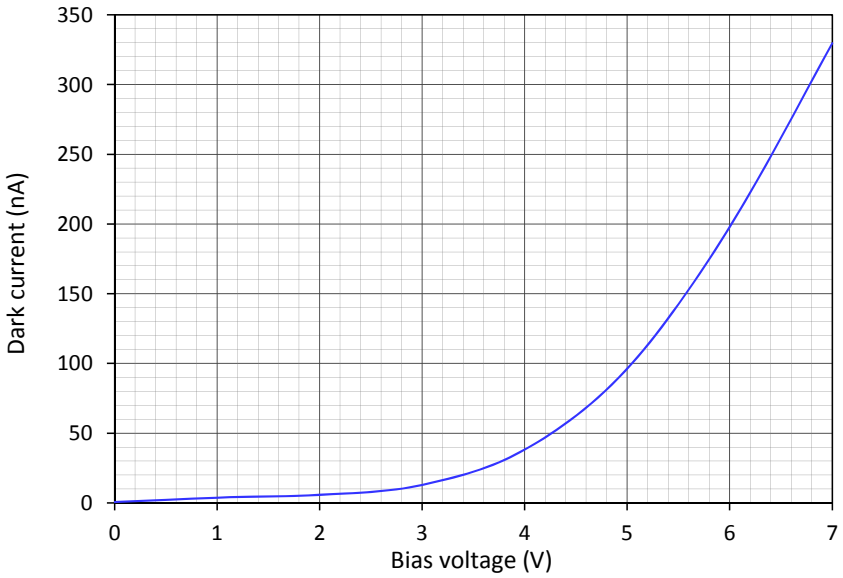


Figure 3.55: Dark current of IMEC InP/InGaAs photodetector

Capacitance

Fig. 3.56 shows the capacitance of the InP/InGaAs photodetector as a function of the applied bias voltage. It can be seen that the capacitance stays nearly constant in the voltage range $0 - 4.0$ V.

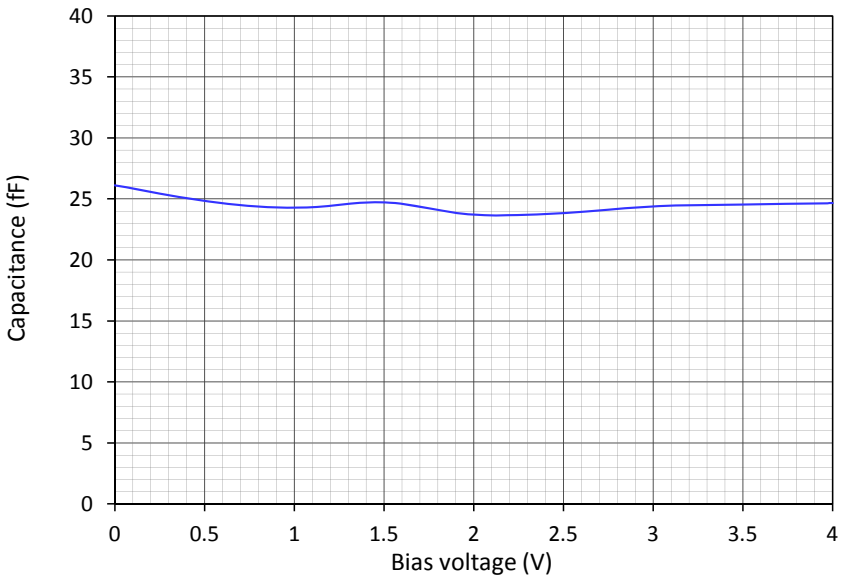


Figure 3.56: Capacitance of IMEC InP/InGaAs photodetector

AC Response

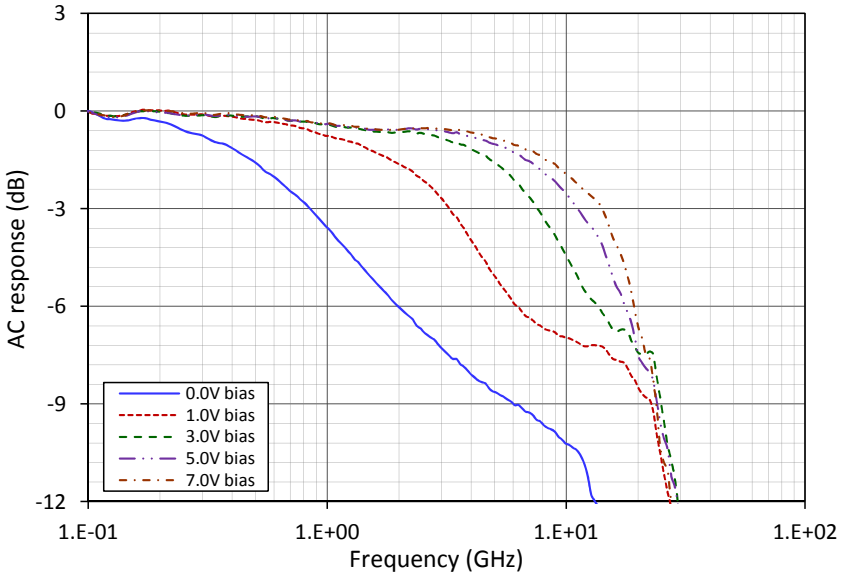
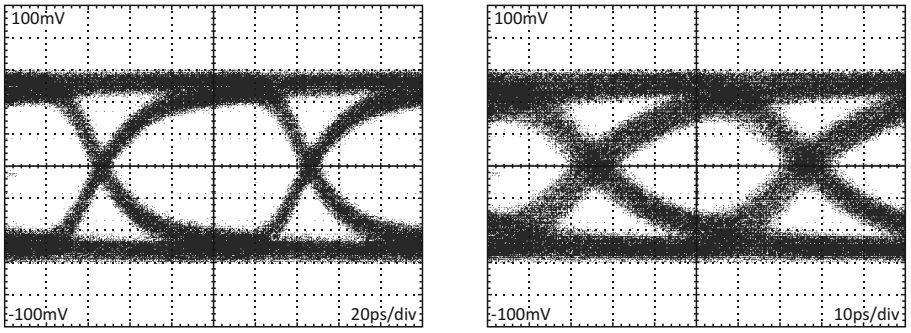


Figure 3.57: AC response of IMEC InP/InGaAs photodetector at different bias voltages

The −3 dB cutoff frequency of the InP/InGaAs photodetector shows a strong dependence on the bias voltage (fig. 3.57). The speed of the photodiode increases strongly with rising bias voltage and reaches its maximum at 7.0 V.

Eye Diagram



(a) (b)

Figure 3.58: Eye diagram of InP/InGaAs photodiode at 10 Gbps (a) and at 20 Gbps (b)

3.5 Conclusion

The measurement results show that not all characterized photodiodes are suitable as photodetector for a 10 Gbps receiver. The crucial diode parameter for designing a fast optical receiver is the −3 dB cutoff frequency. Tab. 3.8 gives an overview of the −3 dB cutoff frequencies of the different characterized diode types in dependence on the applied reverse bias voltage.

Table 3.8: −3 dB cutoff frequency of characterized photodiodes

	−3 dB cutoff frequency (GHz)						
Reverse bias voltage (V)	0.0 V	0.5 V	1.0 V	2.0 V	3.0 V	5.0 V	7.0 V
PIN1	7.53	15.18	15.72	16.28			
PIN2	2.54	4.00	4.30	4.45			
PIN3	1.09	1.79	1.85	1.99			
PIN4	7.53	13.19	14.65	15.72			
PIN5	3.03	4.45	4.61	4.77			
PIN6	1.45	2.06	2.13	2.21			
PIN7	20.09	26.60	26.60	26.60			
10E05	47.41	>50.00	>50.00	>50.00			
10E07	26.32	38.96	46.63	49.86			
10E1	15.74	18.24	21.68	23.87			
15E05	42.92	49.63	>50.00	>50.00			
15E07	26.11	37.12	42.39	46.43			
15E1	14.85	18.25	19.91	23.59			
25E07	27.36	38.96	39.17	46.58			
25E1	14.18	16.52	19.14	22.00			
50E1	12.84	15.84	17.74	20.64			
IMEC	0.86		3.24		7.56	11.2	14.2

Tab. 3.8 shows that the vertical Ge photodiode types PIN2, PIN3, PIN5 and PIN6 are too slow, even at high bias voltages and thus are not suitable as detector. Only the vertical Ge types PIN1, PIN4 and PIN7 offer a −3dB cutoff frequency which is high enough for reaching data rates up to 10 Gbps. In contrast all lateral Ge diodes offer a suitable bandwidth even without biasing. The vertical InP/InGaAs photodetector needs high bias voltages up to 7.0 V, but is also fast enough for achieving a data rate of 10 Gbps.

Other important photodiode parameters are the responsivity R, which should be as huge as possible to reach a high receiver sensitivity, and the capacitance C_p which should be as low as possible to keep the capacitance at the receiver input node small. The responsivities and the capacitances of the different photodetector types are shown in tab. 3.9.

To make the comparison of the different photodetector types easier their performance parameters as bandwidth, responsivity and junction capacitance were combined in a figure of Merit (FOM). Due to the fact that a higher bandwidth and a larger responsivity are

Table 3.9: Responsivity and capacitance of characterized photodiodes

Photodiode type	Responsivity (A/W)	Capacitance (pF)
PIN1	0.50	348
PIN2	0.49	653
PIN3	0.49	1102
PIN4	0.51	353
PIN5	0.49	654
PIN6	0.49	1100
PIN7	0.50	238
10E05	0.08	33
10E07	0.11	21
10E1	0.15	14
15E05	0.09	52
15E07	0.13	46
15E1	0.19	33
25E07	0.19	89
25E1	0.24	79
50E1	0.26	124
IMEC	0.14	24

advantageous while a huge photodiode capacitance is bad, the FOM can be defined as [47]:

$$FOM = BW\frac{R}{C_p}\ \frac{\mathrm{A/W}}{\mathrm{nF}}\mathrm{GHz} \tag{3.6}$$

Fig. 3.59 shows the FOM of the different photodetectors. The vertical Ge diodes (red) have a good responsivity on one hand, but due to their size (see tab. 3.1) and the large bond pads a high capacitance on the other hand. Furthermore only the diode types PIN1, PIN4 and PIN7 offer a high bandwidth while the other vertical Ge diodes types are rather slow. In contrast the lateral Ge detectors (blue) offer only bad responsivities but have very low parasitic capacitances and are quite fast. The same is also valid for the InP/InGaAs diodes (green).

Due to the fact that the impact of different photodetector types and connection structures on the performance of the optical receiver should be examined within the HELIOS project, one diode from each detector type was chosen for the design of the receiver. The selection is based on the -3 dB cutoff frequency and on the FOM (3.6). Tab. 3.10 gives an overview of the selected diodes, the used connection structures and the light coupling.

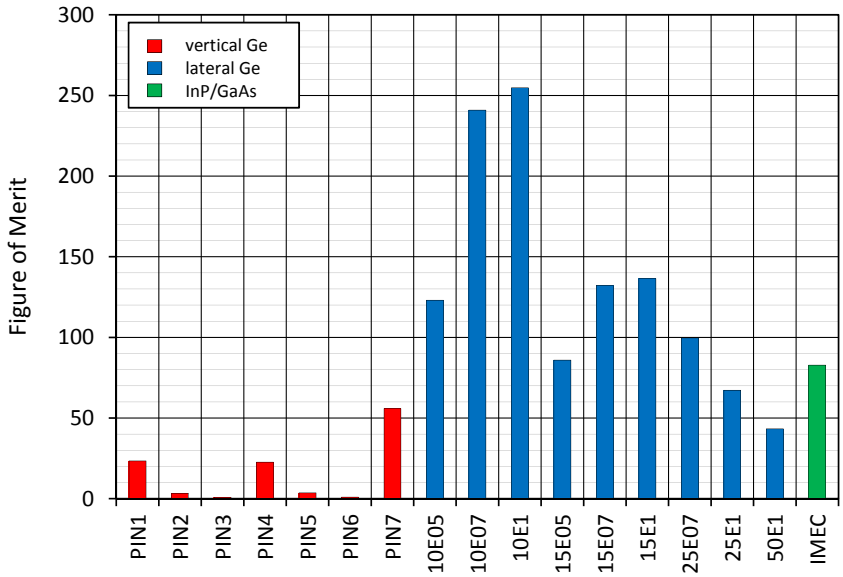


Figure 3.59: Figure of Merit = $(BW \cdot R)/C$

Table 3.10: Overview of selected photodiodes

Diode type	Connection structure	Light coupling	Selected diode
Vertical Ge	Wire bonded	Direct	PIN7
Lateral Ge	Subsequent through silicon vias	Grating coupler, waveguide	10E1
Vertical InP/InGaAs	Copper through silicon vias	Grating coupler, waveguide	IMEC

4 Photodetector Model

For the design of an optical receiver the performance as well as the parasitics of the used photodetector are essential. Thus models of the used photodiodes and their connection to the amplifier were developed. The models consider the main parasitics as junction capacitances, pad capacitances or bond wire inductances. All models are based on the measurement results of chapter 3 on one hand and on the geometric dimensions of the connection structures on the other hand.

4.1 PIN7 Vertical Ge Photodetector

The vertical Ge PIN7 detector is conventionally wire bonded to the amplifier chip. Both chips are clued on a PCB and the connection between them is established with Au bond wires. A cross section of the wire bonded Ge photodiode and the receiver chip together with the main parasitic components is shown in fig. 4.1.

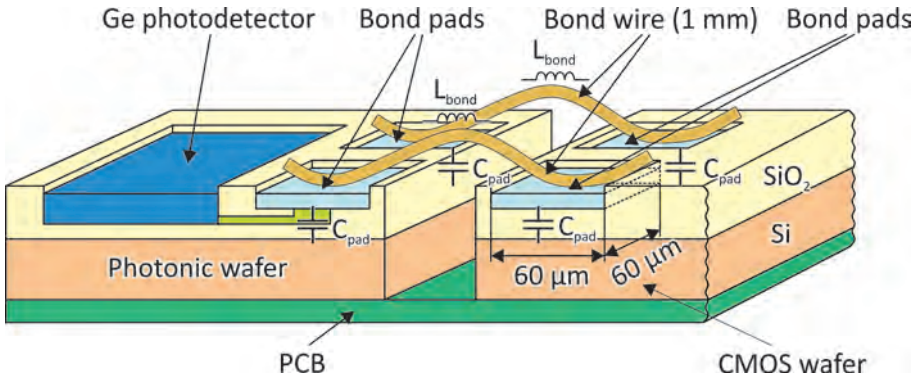


Figure 4.1: Crosscut of wire bonded connection between CMOS and photonic wafer

The main parasitic components of the wire bonded connection are the bond pad capacitances C_{pad} and the bond wire inductances L_{bond}. The used pads are special RF pads which consist of only one metal layer to minimize the parasitic pad capacitances. Nevertheless the bond pad capacitances are relatively large compared to the photodiode junction capacitance. The pads on the photonic chip have a calculated capacitance of approximately

80 fF while the RF pads on the CMOS wafer with a size of 80×80 μm^2 have a capacitance of 70 fF. The bond wire itself has an inductance of approximately 1 nH per 1 mm length.

Together with the measured pn junction capacitance C_p, the estimated photodiode serial resistance R_s and the photodiode parallel resistance R_p, which can be calculated by

$$R_p = \frac{\Delta V_{bias}}{\Delta I_d}, \tag{4.1}$$

follows the equivalent circuit shown in fig. 4.2.

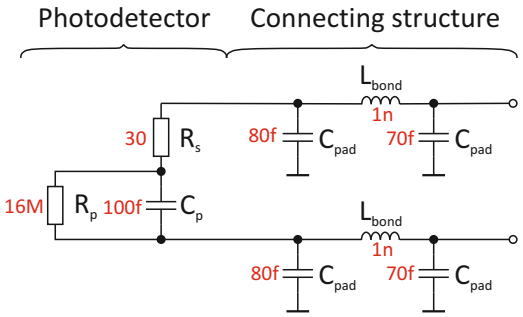


Figure 4.2: Equivalent circuit of vertical Ge photodetector PIN7

4.2 10E1 Lateral Ge Photodetector

In contrast to the vertical Ge detector the lateral Ge photodiode 10E1 is designed for heterogeneous integration. The photonic wafer is flip-chip wafer-to-wafer bonded on top of the CMOS wafer and its sacrificial Si handle part is removed by mechanical grinding and chemical etching [36]. The result is a SiO_2 photonic wafer on top of the CMOS wafer with only 3 μm thickness. In a last production step the holes for the TSVs are etched and the subsequent vias are processed. The TSVs are 5 μm in diameter, only 3 μm long and contact the electronic wafer at special pads with a size of only 10×10 μm^2. Thus the parasitics of the interconnection between photodiode and amplifier are reduced dramatically.

Fig. 4.3 shows the crosscut of the only 3 μm thick photonic wafer, which contains the optical waveguide and the lateral Ge photodetector, flip-chip wafer-to-wafer bonded on top of the CMOS wafer. The main parasitic capacitances are the pad capacitances C_{pad} and the capacitance C_{TSV} between the two TSVs. The geometrical dimensions of the connection structure composed of TSVs and pads were used to calculate the values of the parasitic capacitances $C_{pad} = 3$ fF and $C_{TSV} = 0.3$ fF. The parasitic capacitances and

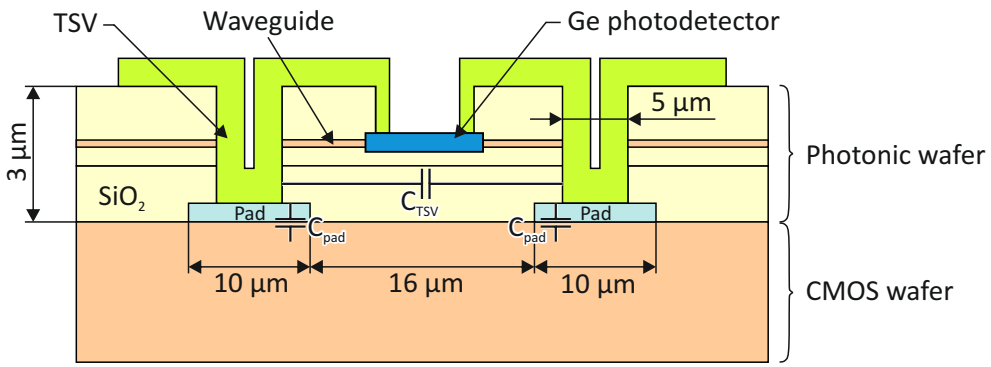


Figure 4.3: Cross section heterogeneous integration 10E1 lateral Ge photodiode using subsequent TSVs

resistances of the lateral Ge photodetector 10E1 itself are $C_p = 14$ fF, $R_p = 1\text{M}\Omega$ and $R_s = 30\ \Omega$ (see chapter 3). The equivalent circuit of the photodiode together with the interconnection to the CMOS wafer is shown in fig. 4.4.

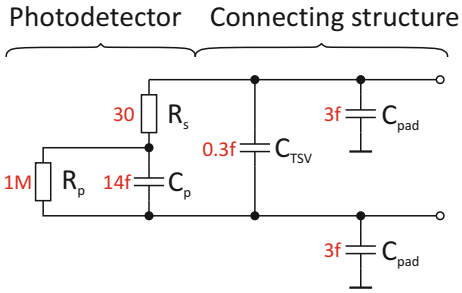


Figure 4.4: Equivalent circuit of vertical Ge photodetector 10E1

4.3 IMEC Vertical InP/InGaAs Photodetector

The vertical InP/InGaAs photodetector from IMEC is also designed for heterogeneous integration on top of the CMOS wafer. In contrast to the lateral Ge detectors from LETI, which are flip-chip wafer-to-wafer bonded, the III–V wafer is cut into dies and die-to-wafer bonded on top of the CMOS wafer. Due to the fact that the dies are mounted with their backside on top of the CMOS chip it is not possible to remove the Si substrate of the dies like it is done at the LETI Ge diodes. Thus the photonic dies are much thicker than the SiO_2 photonic wafer used for the lateral Ge diodes. The thicker photonic wafer necessitates

the use of long Cu nails (TSVs) to establish the electric interconnection between diode and CMOS wafer. Due to the fact that the Cu nails penetrate the Si substrate it is necessary to isolate them by a thin SiO_2 layer. In contrast to the use of subsequent TSVs (fig. 4.3), which are processed after the wafer-to-wafer bonding, the Cu nails are processed before the die-to-wafer bonding. Therefore InCu bumps between the Cu nails and the pads of the CMOS wafer are used to compensate surface roughness of the CMOS wafer respectively the photonic wafer. Fig. 4.5 shows a crosscut of the interconnection with its geometric dimensions and the main parasitics.

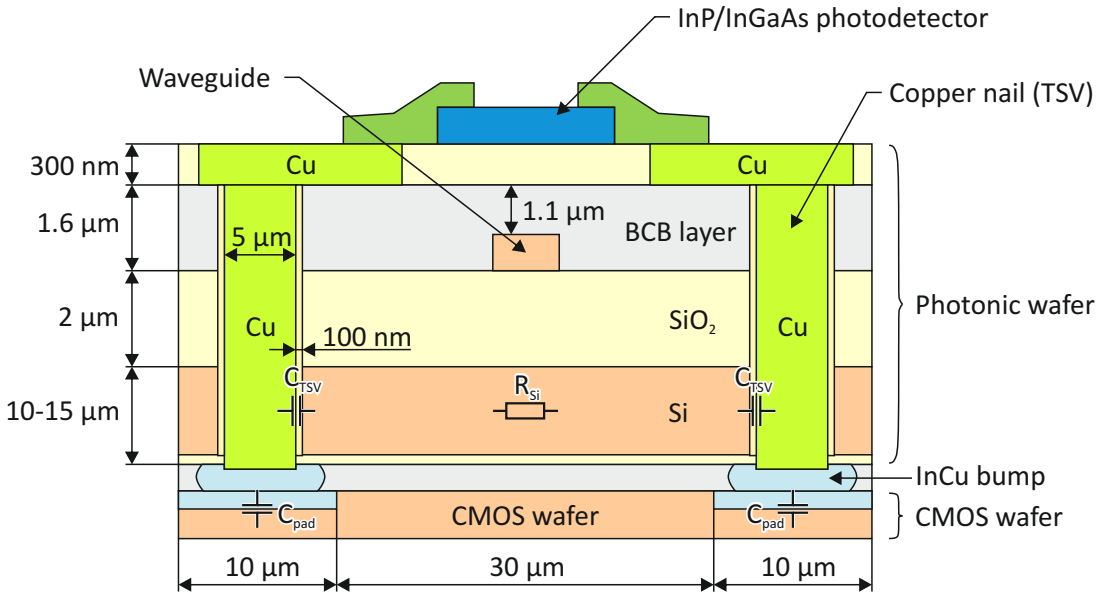


Figure 4.5: Cross section heterogeneous integration IMEC InP/InGaAs photodiode

C_{pad} is the capacitance of the connection pad on the CMOS wafer and its simulated value is $C_{pad} = 3$ fF. The capacitance C_{TSV} describes the capacitance between the Cu nails, isolated by the 100 nm thick SiO_2 layer and the Si substrate of the photonic wafer. Its value can be calculated by

$$C_{TSV} = 2\pi\epsilon_0\epsilon_r \frac{l}{\ln(\frac{d_2}{d_1})}, \tag{4.2}$$

where ϵ_r is the relative permeability of SiO_2, l the thickness of the Si substrate, d_1 the diameter of the TSV and d_2 the diameter of the TSV plus the SiO_2 isolation layer. R_{Si} is the resistance of the Si substrate between the two TSVs. Its simulated value is $R_{Si} = 25$ kΩ.

The InP/InGaAs photodetector itself has a junction capacitance of $C_p = 24$ fF and a parallel resistance of $R_p = 20$ MΩ (see chapter 3). Fig. 4.6 shows the equivalent circuit of

the InP/InGaAs photodiode and the connection elements.

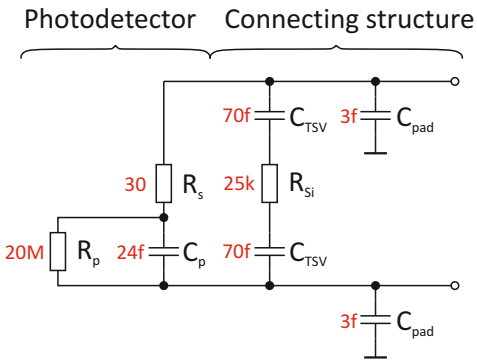


Figure 4.6: Equivalent circuit vertical InP/InGaAs photodetector

5 Amplifier Design

This chapter describes the development of a highly sensitive 8×10 Gbps optical receiver, which can be used together with different photodiode types and integration strategies discussed in chapter 3. In particular the wire bonded vertical Ge photodiode PIN7, the heterogeneously integrated Ge photodiode 10E1 and the heterogeneously integrated InP/InGaAs diode from IMEC were used as photodetector. For all simulations which were necessary during the circuit design the photodiode models, discussed in chapter 4, were used.

The amplifier itself is designed for a supply voltage of 3.3 V and is fabricated in austriamicrosystems noise optimized 0.35 μm SiGe HBT BiCMOS process, which is a modular enhancement of industry standard 0.35 μm CMOS technology [48]. This advanced RF-process offers high performance analog oriented SiGe HBT transistors as well as standard CMOS transistors which makes it ideally suitable for high performance RF applications.

5.1 Circuit Overview

The amplifier consists of eight identical channels, each capable of 10 Gbps maximum data rate. Each channel is based on a differential receiver structure and consists of a TIA followed by two limiting amplifiers and a 50 Ω CML-style output buffer. The differential receiver structure is chosen to minimize the influence of common mode disturbances, temperature effects and process tolerances. Due to the fact that the TIA itself is only single-ended while the following stages have a fully differential structure, a dummy TIA and an operational amplifier, which works as offset compensation, are necessary to provide the differential input signal for the following limiting amplifier. The operational amplifier compares the DC offset voltage between the differential inputs of the output buffer and generates an adequate input signal for the dummy TIA to compensate this DC offset voltage. The extra noise caused by the dummy TIA, compared to a single-ended structure, is suppressed by an additional RC low-pass filter which is implemented inside the dummy TIA. The offset compensation at the input of the output driver was chosen since this feedback loop indicated the most stable behavior among all simulations. Fig. 5.1 shows the block diagram of one receiver channel.

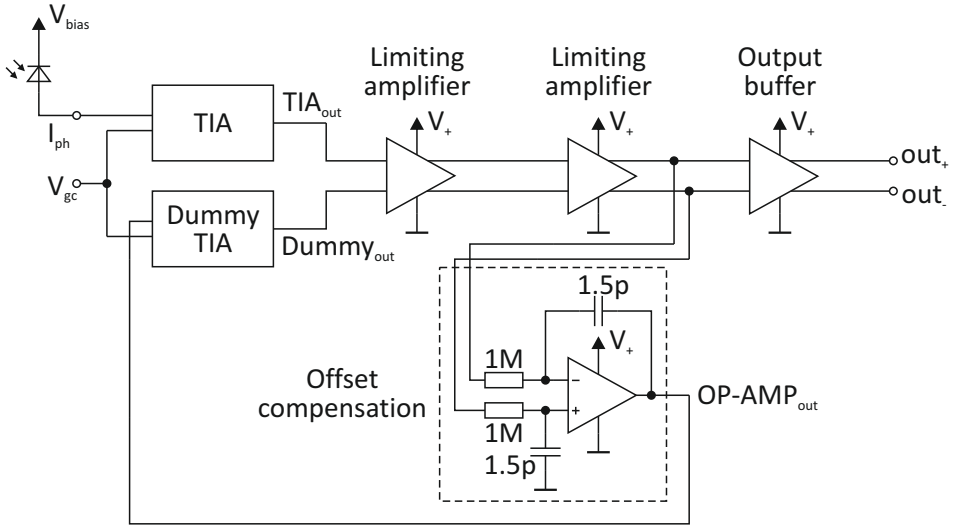


Figure 5.1: Block diagram of one receiver channel

5.1.1 TIA Circuit

The transimpedance amplifier is based on an input transistor in common-emitter configuration, the feedback network and two emitter followers (fig. 5.2). The common-emitter amplifier consists of the bipolar transistor T_1 and the load resistor R_c. Due to the fact that the noise generated by the first amplifier stage is the largest contributor to the overall noise of the whole receiver, it is crucial to optimize the input stage for a minimal equivalent input noise current. For a bipolar transistor input stage the equivalent mean-square input noise current $\overline{i_{in}^2}$ mainly depends on the noise generated by the input transistor and the noise of the feedback resistor R_{fb} (2.43). The noise of the load resistor R_c can be neglected in a first approximation because it is attenuated by the gain of the input transistor. To find the optimal working point and the proper size of the input transistor T_1 excessive simulations on a simplified TIA circuit (fig. 2.24) were carried out. The feedback network is formed by the feedback resistor R_{fb}, the feedback capacitance C_{fb} and the gain control MOSFET T_{gc}. Applying a positive voltage V_{gc} decreases the gain of the feedback network and the gain of the amplifier is reduced. The resistance R_{gc} is implemented to avoid floating of the gate of T_{gc} if V_{gc} is left unconnected. The feedback resistor defines the transimpedance of the amplifier while C_{fb} is used to compensate for the gain peaking of the frequency response which may appear at large values of the input node capacitance C_T. The input node capacitance C_T of a bipolar input stage can be calculated by

$$C_T = C_p + C_{con} + (1 + g_{m1}R_c)C_{\mu 1} + C_{\pi 1} \tag{5.1}$$

where C_p is the photodiode capacitance, C_{con} the capacitance of the connection structures, $C_{\pi 1}$ the base-emitter capacitance and $C_{\mu 1}$ the base collector capacitance of T_1 which has

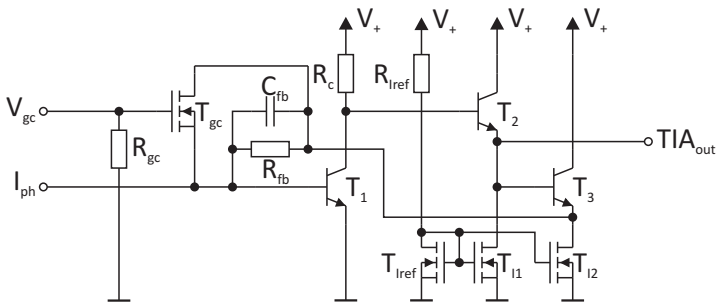


Figure 5.2: Schematic of TIA

to be multiplied according to Miller's theorem. For a given input node capacitance the value of C_{fb} can be calculated by the equations (2.28) and (2.29). On the other hand the feedback network also determines the bandwidth of the amplifier (2.26). Thus excessive simulations with different values of R_{fb} and C_{fb} and the three different photodiode models were done to optimize the feedback network. Finally it turned out that it is not possible to use the same feedback network for all three photodetector types. While it is possible to use the same value of R_{fb} for all three photodiode types, C_{fb} has to be larger for the use of the conventional wire bonded photodetector to avoid gain peaking due to the large photodiode capacitance. Unfortunately a larger value of C_{fb} reduces the bandwidth of the receiver. This bandwidth loss can be compensated by reducing the transimpedance via the gain control at the cost of receiver sensitivity. As compromise three different feedback configurations were implemented, two versions for use with heterogeneously integrated diodes (gain peak completely suppressed and higher bandwidth at the cost of some gain-peaking) and one version with a larger feedback capacitance for use with the wire bonded diode. The first two versions are designed to take full advantage of the heterogeneous integrated photodiodes. In contrast the version with the large feedback capacitor can be adapted to work with various diode types with the help of the gain control. Tab. 5.1 gives an overview of the different feedback configurations and their simulated bandwidths for the different diode types.

Table 5.1: Overview of feedback network configurations of TIA

	Feedback configuration		
	Conservative	Progressive	External PD
R_{fb}	4.2 kΩ	4.2 kΩ	4.2 kΩ
C_{fb}	5 fF	4 fF	20 fF
Connection	TSV	TSV	bond wire
Diode type	10E1/IMEC	10E1/IMEC	PIN7
Transimpedance	4.2 kΩ	4.2 kΩ	2.0 kΩ (gain control)
Bandwidth	9.2 GHZ/8.8 GHz	8.8 GHz/8.5 GHz	7.8 GHz

The two emitter followers are realized by T_2 and the current source T_{I1}, respectively T_3 and T_{I2}. T_{Iref} works as current mirror for T_{I1} and T_{I2}. The noise of the two emitter followers is not critical, because they are not connected directly to the input node and thus the generated noise is attenuated by the gain of the first stage. The whole transimpedance amplifier has a power consumption of 8 mW at a supply voltage of 3.3 V. Tab. 5.2 gives an overview of type, value and geometrical dimensions of the used resistors and capacitors, type and emitter area of the bipolar transistors and type, number of gates, width and length of the used MOSFETs.

Table 5.2: Component values and sizes of TIA

		Component properties		
Component	Value	Width (μm)	Length (μm)	Type
R_{gc}	1.0 kΩ	0.65	8.00	rpoly2
R_{fb}	4.2 kΩ	0.65	33.60	rpoly2
R_c	2.5 kΩ	1.00	37.50	rpoly2
R_{Iref}	780 Ω	3.00	42.85	rpoly2
	4 fF	1.65	2.35	cpoly
C_{fb}	5 fF	1.90	2.6	cpoly
	20 fF	4.25	5.0	cpoly
T_1		0.4	2.2	npn121
T_2		0.4	1.2	npn121
T_3		0.4	15.0	npn121
T_{gc}		1×0.4	0.35	modn
T_{I1}		4×3.0	2.00	modn
T_{I2}		4×3.0	2.00	modn
T_{Iref}		4×2.5	2.00	modn

5.1.2 Dummy TIA

Since the TIA itself is only single-ended while the following amplifier stages are fully differential, a dummy TIA is needed to provide a differential input signal for the limiting amplifiers. Due to the fact that the limiting amplifiers are based on DC coupled differential amplifiers it is necessary to avoid DC offset voltages between the differential inputs in^+ and in^-. In order to achieve this the basic idea was to apply a DC voltage to the differential input in^- which fulfills this. One possibility to generate such a DC voltage is to use two identical single-ended TIAs. The first TIA is connected to the photodiode while the second TIA is connected to an identical photodiode which is covered and therefore generates no photocurrent. The first TIA generates an output voltage which consists of a DC and an AC part which is proportional to the photocurrent generated by the photodiode. The second TIA only generates a DC voltage on its output due to the fact that the second diode is covered. These two signals together form the differential input signal for the

following amplifier stages. The drawbacks of this configuration are the required second photodiode and the additional noise caused by the dark diode and the second TIA.

These problems can be resolved by using a dummy TIA and an operational amplifier which generates the input signal of the TIA according to the DC voltage offset between the differential amplifier inputs (fig. 5.1). The used dummy TIA is identical to the photodiode TIA except the additional capacitor C_{limit} which limits the bandwidth of the amplifier to 40 MHz and thus suppresses the additional noise caused by the dummy TIA compared to a single-ended structure. Fig. 5.3 shows the schematic of the dummy TIA. The parameters of the used components are the same as used for the photodiode TIA (tab. 5.2) except the additional capacitor C_{limit}. Its value, dimensions and type are listed in tab. 5.3.

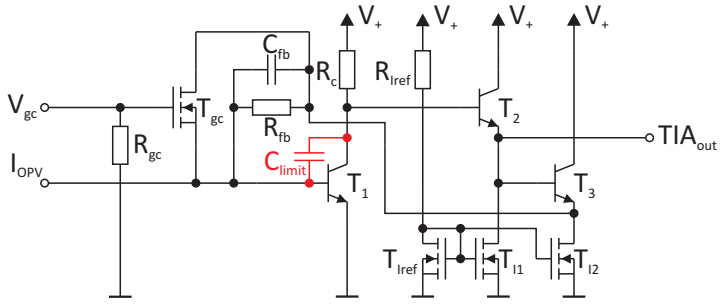


Figure 5.3: Schematic of dummy TIA

Table 5.3: Parameters of C_{limit}

		Component properties		
Component	Value	Width (μm)	Length (μm)	Type
C_{fb}	1.85 pF	5.2	39.9	cstack

5.1.3 First Limiting Amplifier Stage

The first limiting amplifier stage is realized as differential amplifier with emitter followers (fig. 5.4). The differential amplifier is built up of the bipolar transistors T_1 and T_2, the load resistors R_{c1} and R_{c2} and the MOSFET T_{I1} which interact with T_{Iref} and R_{Iref} as current source. The emitter followers consist of T_3 and T_{I2}, respectively T_4 and T_{I3}. T_{I2} and T_{I3} work together with T_{Iref} as current mirror. The first limiting amplifier stage offers a bandwidth of 10.2 GHz and its power consumption is 30 mW at a supply voltage of 3.3 V. The component parameters as value, size and type are listed in tab. 5.4.

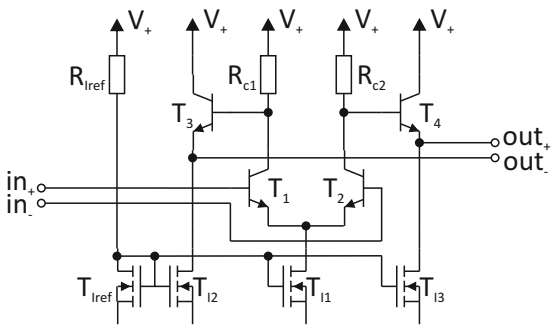


Figure 5.4: Schematic of first limiting amplifier stage

Table 5.4: Component values and sizes of first limiting amplifier

		Component properties		
Component	Value	Width (μm)	Length (μm)	Type
R_{c1}	120 Ω	2.00	29.25	rpoly1
R_{c2}	120 Ω	2.00	29.25	rpoly1
R_{Iref}	780 Ω	3.00	42.85	rpolyc
T_1		0.4	3.0	npn121
T_2		0.4	3.0	npn121
T_3		0.4	10.0	npn121
T_4		0.4	10.0	npn121
T_{I1}		6×2.85	2.00	modn
T_{I2}		12×3.35	2.00	modn
T_{I3}		12×3.35	2.00	modn
T_{Iref}		4×2.5	2.00	modn

5.1.4 Second Limiting Amplifier Stage

The second limiting amplifier also is realized as differential amplifier with emitter followers. In contrast to the first limiting amplifier an additional voltage level shifter is implemented to ensure the appropriate input DC voltage level for the following output buffer (fig. 5.5).

The differential amplifier is formed by T_1 and T_2, the load resistors R_{c1} and R_{c2} and the current source T_{I1}. T_3 and T_{I2}, respectively T_4 and T_{I3} form the subsequent emitter followers. Simulations showed that additional emitter followers with larger transistor sizes are necessary to drive the subsequent output buffer with its large input transistors. These output emitter followers are formed by T_7 and T_8 and the current sources T_{I6} and T_{I7}. Due to the additional emitter followers the output DC voltage level of the amplifier stage gets too low for the following output buffer. Therefore T_5, R_1 and T_{I4}, respectively T_6, R_2 and T_{I5} are used as voltage level shifters between the two emitter follower stages to raise

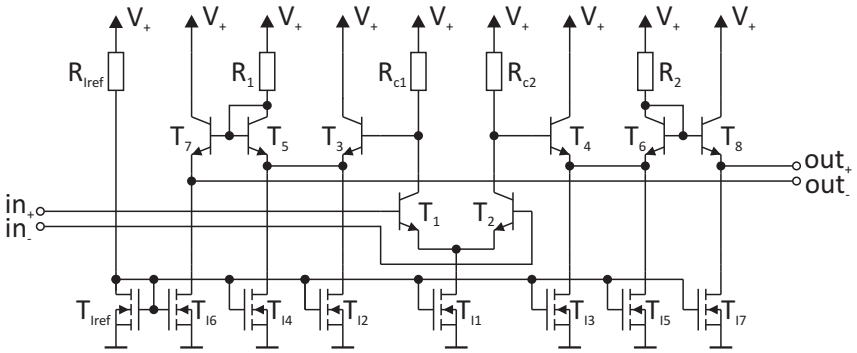


Figure 5.5: Schematic of second limiting amplifier stage

the DC voltage level to an appropriate value. Due to the short-circuited base-collector diodes T_5 and T_6 are working as normal diodes and thus the output DC voltage level is increased by the forward voltages of the base-emitter diodes. T_{Iref} and R_{Iref} are used to generate the reference current for $T_{I_1} - T_{I7}$. The second limiting amplifier stage is designed for a supply voltage of 3.3 V, has a power consumption of 58 mW and a bandwidth of 9.25 GHz. Tab. 5.5 lists the parameters of the used components.

Table 5.5: Component values and sizes of second limiting amplifier

		Component properties		
Component	Value	Width (μm)	Length (μm)	Type
R_1	110 Ω	5.00	68.10	rpoly1
R_2	110 Ω	5.00	68.10	rpoly1
R_{c1}	400 Ω	4.00	30.00	rpoly2
R_{c2}	400 Ω	4.00	30.00	rpoly2
R_{Iref}	780 Ω	3.00	42.85	rpolyc
T_1		0.4	7.0	npn121
T_2		0.4	7.0	npn121
T_3		0.4	2.0	npn121
T_4		0.4	2.0	npn121
T_5		0.4	2.0	npn121
T_6		0.4	2.0	npn121
T_7		0.4	10.0	npn121
T_8		0.4	10.0	npn121
T_{I1}		16×3.10	2.00	modn
T_{I2}		4×3.00	2.00	modn
T_{I3}		4×3.00	2.00	modn
T_{I4}		4×3.00	2.00	modn
T_{I5}		4×3.00	2.00	modn
T_{I6}		12×3.35	2.00	modn
T_{I7}		12×3.35	2.00	modn
T_{Iref}		4×2.5	2.00	modn

5.1.5 50 Ω CML-style Output Buffer

The output buffer stage is implemented as differential cascode amplifier. It is capable of driving a differential 100 Ω output load with a simulated voltage swing of 800 mVpp. The cascode circuit is chosen to overcome the Miller capacitance limitations of common-emitter amplifiers by using two additional transistors as common-base buffers [49]. The result is a higher input-node impedance and a higher bandwidth compared to a common-emitter amplifier. The schematic of the differential cascode output buffer is shown in fig. 5.6.

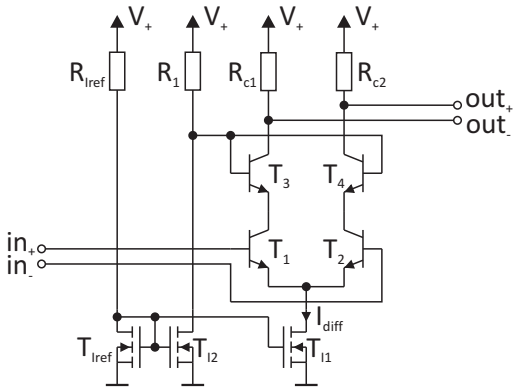


Figure 5.6: Schematic of cascode output buffer

The advantage of the cascode circuit in contrast to a common-emitter amplifier is the use of the cascode transistors T_3 and T_4 as load of the input transistors T_1 and T_2. The bases of the cascode transistors T_3 and T_4 are biased by a constant voltage generated by R_1 and T_{I2}. Therefore the emitters of T_3 and T_4 are also held at a nearly constant voltage level during operation. In other words, the cascode transistors T_3 and T_4 present low load resistances to the input transistors T_1 and T_2. Thus the gain of the input transistors is very small, which reduces the Miller feedback capacitances of T_1 and T_2. The resulting voltage gain loss of the input stage is recovered by the cascode transistors which work as common-base buffer. Therefore T_1 and T_2 can be operated with minimum negative feedback improving their bandwidth [50]. T_{Iref} and R_{Iref} are used as current mirror for T_{I_1} and T_{I2}. The current I_{diff} = 19 mA, the output buffer has a power consumption of 65 mW and its bandwidth is 9.65 GHz. The properties of the used components are summarized in tab. 5.6.

Table 5.6: Component values and sizes of output driver

Component	Value	Component properties Width (μm)	Length (μm)	Type
R_1	600 Ω	3.40	37.80	rpoly2
R_{c1}	50 Ω	20.00	124.70	rpoly1
R_{c2}	50 Ω	20.00	124.70	rpoly1
R_{Iref}	780 Ω	3.00	42.85	rpolyc
T_1		0.4	40.0	npn121
T_2		0.4	40.0	npn121
T_3		0.4	40.0	npn121
T_4		0.4	40.0	npn121
T_{I1}		64×3.10	2.00	modn
T_{I2}		4×2.50	2.00	modn
T_{Iref}		4×2.5	2.00	modn

5.1.6 Offset Compensation

The intention of the offset compensation is to generate an adequate input current for the dummy TIA, which compensates the offset voltage between the differential inputs of the following amplifier stages. The offset compensation is formed by a RC network and an operational amplifier (fig. 5.1). The operational amplifier is used to generate the input signal for the dummy TIA in dependence on the offset voltage between the differential inputs of the output buffer. This configuration was chosen since the feedback loop over the whole receiver chain indicated the most stable behavior among all simulations.

The operational amplifier itself is based on a differential amplifier, which consists of the MOSFETs T_1 and T_2, followed by an output buffer formed by T_5 and T_6. The reference current for the current sources $T_{I1} - T_{I5}$ is generated by the reference resistance R_{Iref} and T_{Iref}. The capacitances C_1 and C_2 are used to ensure stability under all circumstances. Fig. 5.7 shows the schematic of the operational amplifier and the component properties are listed in tab. 5.7.

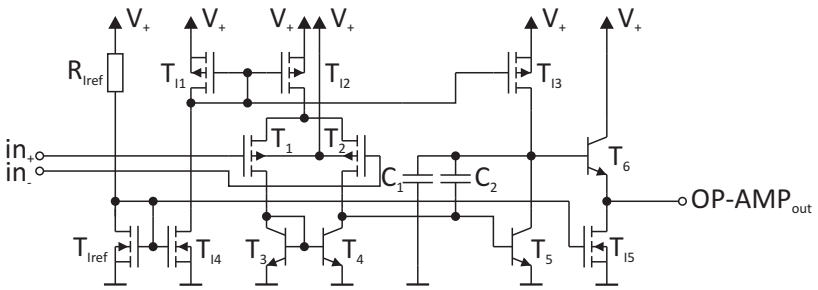


Figure 5.7: Schematic of operational amplifier

Table 5.7: Component values and sizes of operational amplifier

Component	Value	Component properties Width (μm)	Length (μm)	Type
R_{Iref}	780 Ω	3.00	42.85	rpolyc
C_1	340 fF	19.30	20.10	cpoly
C_2	1.35 pF	25.00	62.20	cpoly
T_3		0.4	4×7.5	npn254h5
T_4		0.4	4×7.5	npn254h5
T_5		0.4	4×15.0	npn254h5
T_6		0.4	1.0	npn111h5
T_1		6×26.65	2.00	modp
T_2		6×26.65	2.00	modp
T_{I1}		2×12.50	5.00	modp
T_{I2}		6×12.50	5.00	modp
T_{I3}		6×12.50	5.00	modp
T_{I4}		1×10.00	2.00	modn
T_{I5}		3×10.00	2.00	modn
T_{Iref}		4×2.5	2.00	modn

5.2 Layout

As mentioned above three different 8-channel receiver versions with minor adaptions for the different photodiode and connection types were designed. The first and the second version are designed for use with heterogeneously integrated photodetectors directly on top of the receiver chip and differ only in the size of the used feedback capacitor C_{fb} (4 fF vs. 5 fF). In contrast the third version is designed for use with external wire bonded photodiodes. Therefore large bond pads for wire bonding are necessary instead of the small pads of the two other versions. The larger capacitances of the pads and the external diode also necessitate a larger feedback capacitor $C_{fb} = 20$ fF to avoid gain peaking. The gain control is used to adapt the transimpedance (and therefore the bandwidth also) of the TIA to the wire bonded photodiodes.

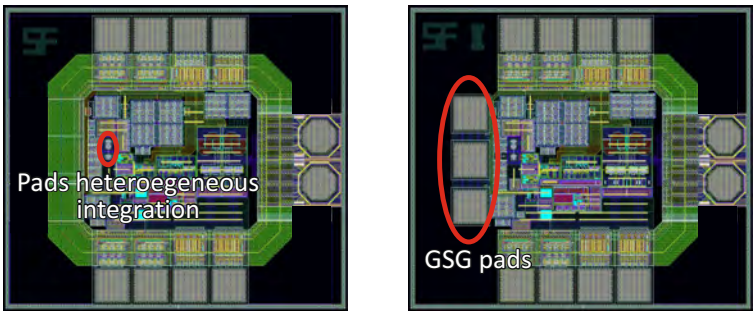
In addition to the three 8-channel receiver version also three 1-channel receiver versions were designed for test purposes. Two versions which differ only in the size of the feedback capacitor C_{fb} (4 fF vs. 5 fF) and a third version with a voltage input for electrical characterization of the receiver without the use of a photodiode. The voltage input consists of additional GSG pads and an integrated 10 kΩ resistor R_{in} in series to the current input of the TIA. The series resistor simulates a photocurrent at the TIA input when a voltage is applied at the GSG pads. Therefore a voltage data signal (eg. PRBS31) can be applied directly to the GSG pads for the electrical characterization of the amplifier. To minimize the influence of the parasitic capacitance of the serial resistor on the receiver properties a

high resistive poly resistor with a size of $0.8 \times 5.0\ \mu m^2$ (width $\times$ length) and a parasitic capacitance of only 1 fF was used. Due to the fact that this value is very small compared to the parasitic capacitances of the used heterogeneously integrated photodiodes of several fF, it can be concluded that the 10 kΩ serial resistance has no influence on the electrical properties of the amplifier. Overall, six different receiver versions were put into layout (see tab. 5.8).

Table 5.8: Different receiver versions

	1-channel receiver			8-channel receiver		
R_{fb}	4.2 kΩ	4.2 kΩ	4.2 kΩ	4.2 kΩ	4.2 kΩ	4.2 kΩ
C_{fb}	4 fF	5 fF	5 fF	4 fF	5 fF	20 fF
Connection type	TSV	TSV	GSG	TSV	TSV	bond wire
Diode type	10E1/IMEC	10E1/IMEC	-	10E1/IMEC	10E1/IMEC	PIN7

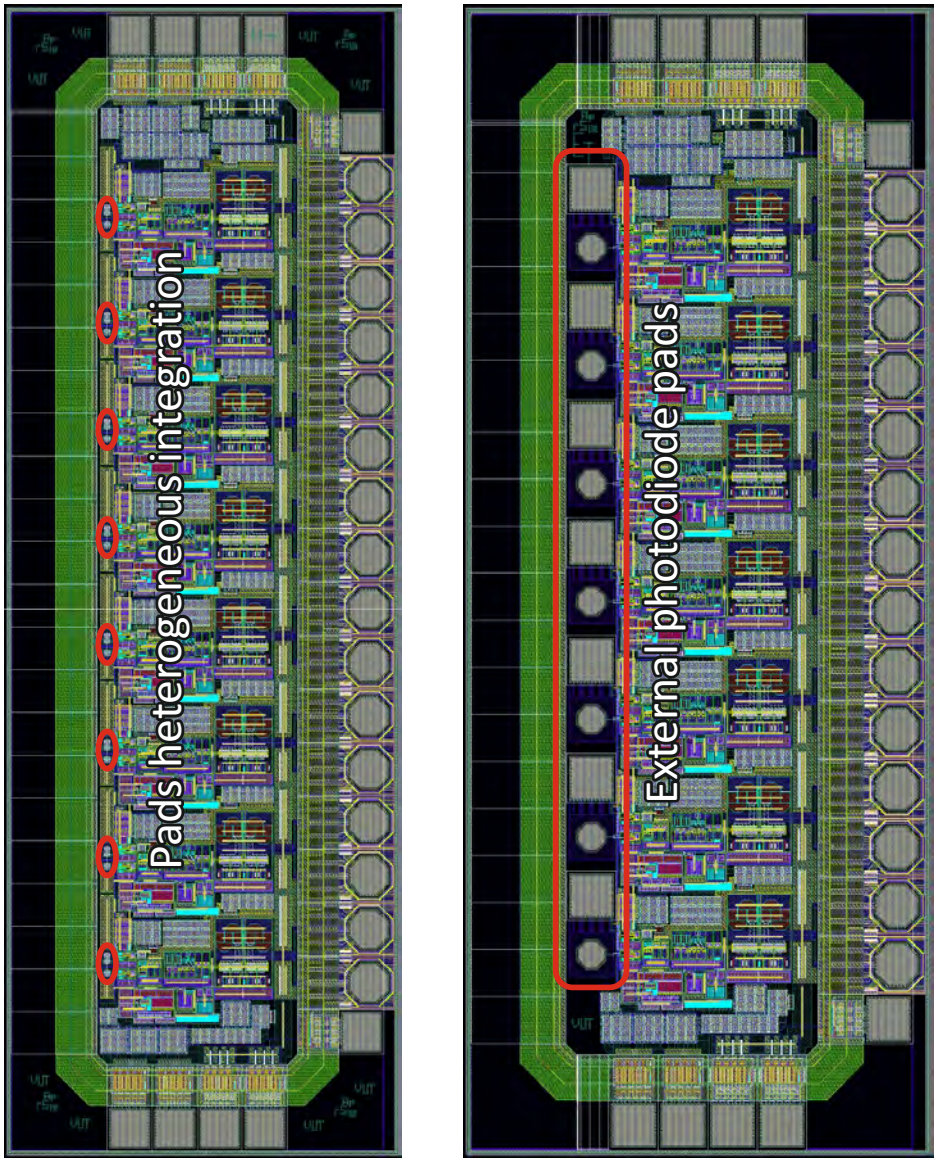
The different layout versions of the 1-channel receiver are shown in fig. 5.8. The input pads for heterogeneous integration of the photodetector (fig. 5.8(a)) and the GSG pads for electrical characterization (fig. 5.8(b)) can be seen on the left side of each picture (marked red) while the differential output pins are located on the right side. The remaining pins on top and bottom of each chip are used for supply voltages, GND, photodiode biasing and gain control.



(a) (b)

Figure 5.8: Layout 1-channel receiver for heterogeneously integrated photodiode (a) and GSG voltage inputs for electrical characterization (b)

Fig. 5.9 shows the different layout versions of the 8-channel receiver. Fig. 5.9(a) is designed for heterogeneous integration of the photodetectors and fig. 5.9(b) shows the receiver version with bond pads for wire bonded photodiodes.



(a) (b)

Figure 5.9: Layout 8-channel receiver for heterogeneously integrated (a) and external wire bonded (b) photodiode

The layout of the whole module with all six receiver versions is shown in fig. 5.10.

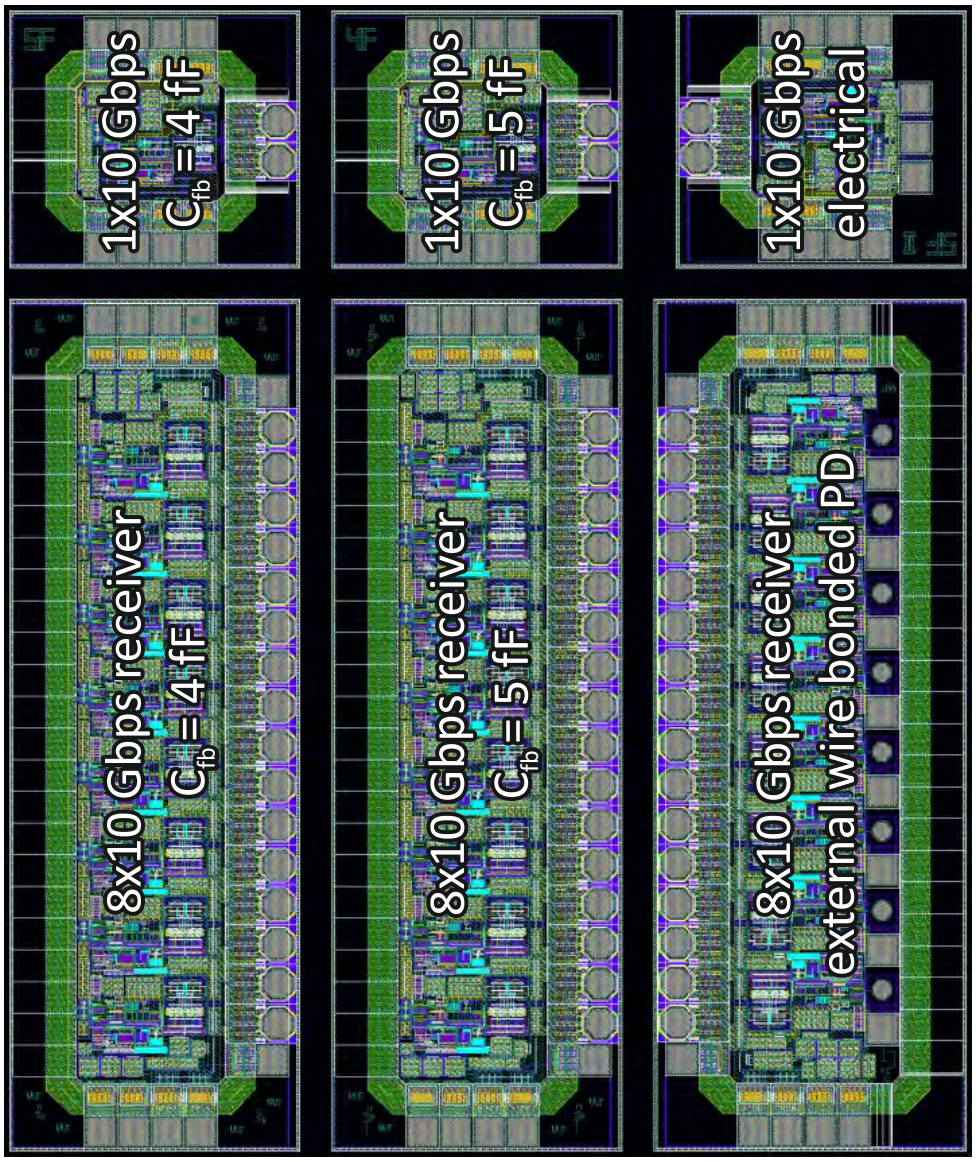


Figure 5.10: Module layout with all six receiver versions

5.3 Postlayout Simulation

After the layout of the whole receiver chip was finished, the components and the parasitic capacitances were extracted from the layout. For the postlayout simulations the extracted view of the layout was completed with the various photodiode models, the 100 Ω differential

load R_{load} and the bond wire inductances L_{bond}. Then the postlayout simulation was accomplished with each of the three photodetector models (PIN7, 10E1 and IMEC) and the 10 kΩ resistor R_{in} for electrical characterization. Fig. 5.11 shows the setup of the postlayout simulation.

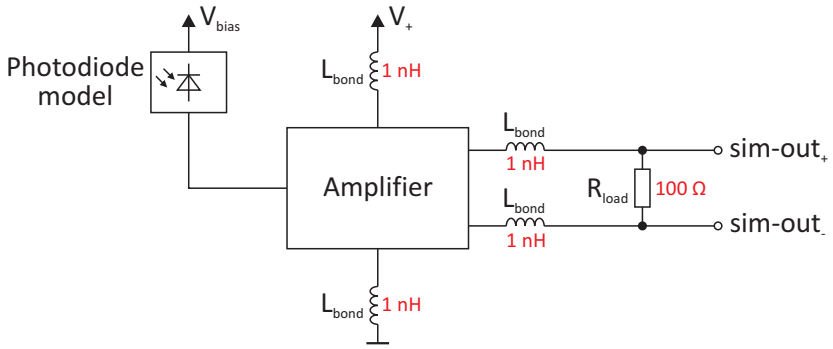


Figure 5.11: Setup postlayout simulation

5.3.1 Simulation Results with Vertical Ge PIN7 Photodetector

As already mentioned the wire bonded PIN7 photodiode can only be used in combination of a larger feedback capacitance $C_{fb} = 20$ fF and a reduced transimpedance. The reduction of the transimpedance was done via the integrated gain control by applying a positive voltage V_{gc} at the gain control pin. To find a appropriate value for the transimpedance, V_{gc} was increased until a receiver bandwidth of around 6.5 GHz was reached. This bandwidth value was finally reached at an transimpedance of 2.0 kΩ and at $V_{gc} = 2.4\ V$ which results in an total transimpedance of the whole receiver chain of 130 kΩ. These values were used for the following postlayout simulations with the vertical Ge PIN7 photodetector.

Receiver Gain

Fig. 5.12 shows the simulated gain of the receiver in combination with the PIN7 photodetector in dependence on the frequency. As mentioned above the total transimpedance of the whole receiver chain was reduced by the gain control to 130 kΩ to reach the required bandwidth for a data rate of 10 Gbps.

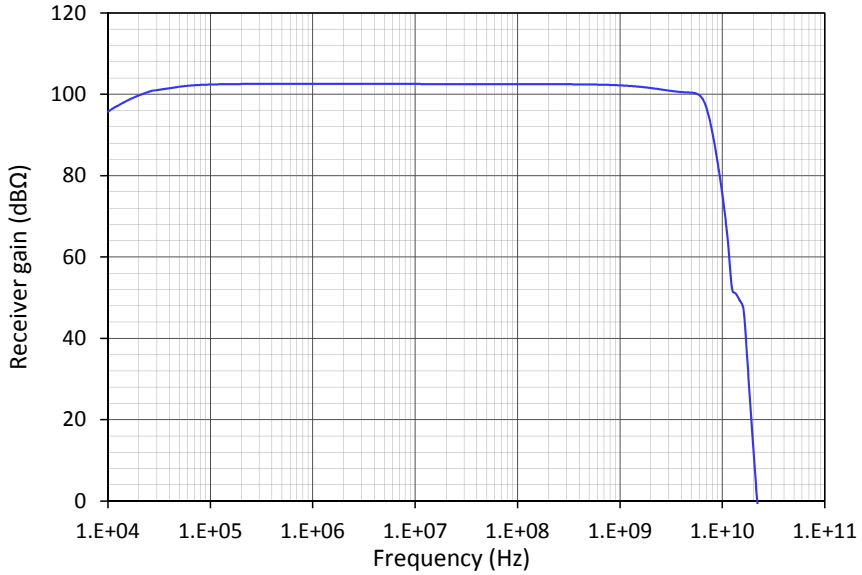


Figure 5.12: Receiver gain with vertical Ge PIN7 photodetector

Transient Response

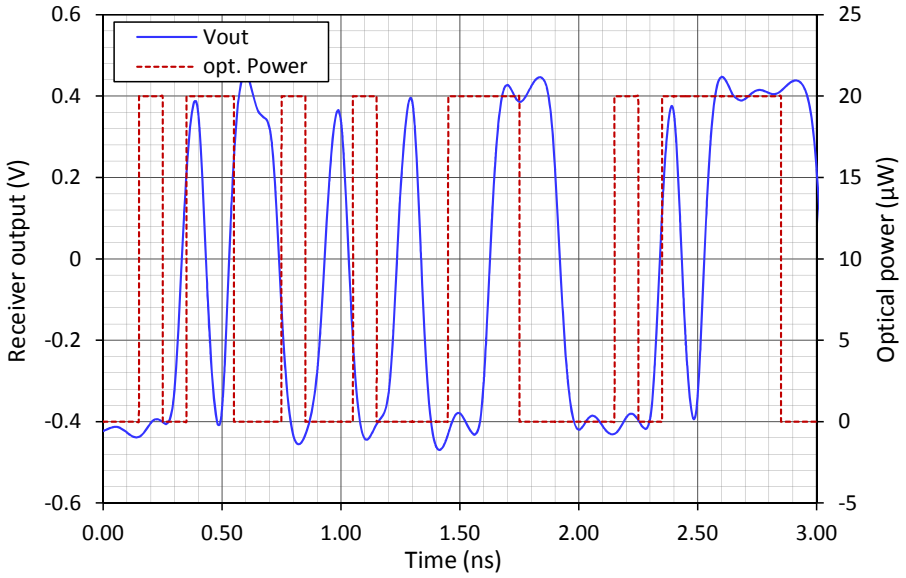


Figure 5.13: Transient response with vertical Ge PIN7 photodetector

Fig. 5.13 shows the simulated transient response of the receiver in combination with the vertical Ge PIN7 photodiode at a data rate of 10 Gbps and a PRBS31 signal. The transient overshoot is only minor and the receiver output signal nearly reaches the full amplitude even at short pulses.

Eye Diagram

The simulated eye diagram shown in fig. 5.14 was recorded using a 10 Gbps PRBS31 data signal at a simulated optical power of 10.8 μW. This optical power was chosen to reach a Q-factor of $Q = 6$ ($BER = 10^{-9}$) together with the measured photodiode responsivity of 0.5 A/W (tab. 3.9). Therefore a simulated sensitivity of -19.7 dBm ($BER = 10^{-9}$) at 10 Gbps is reached.

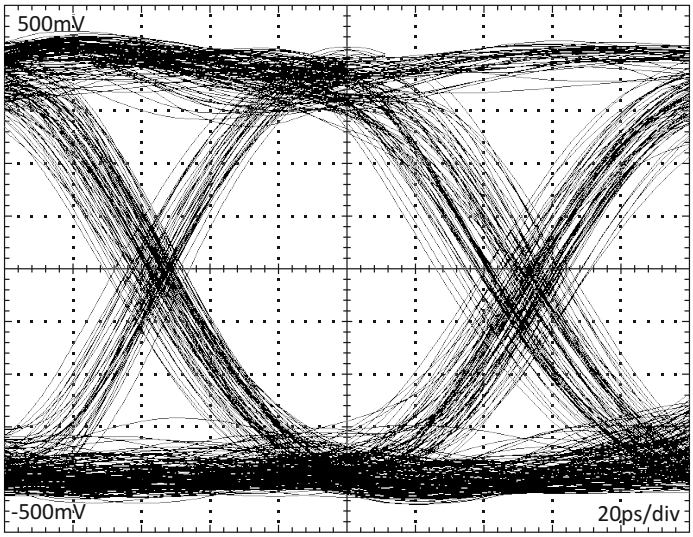


Figure 5.14: Eye diagram of 10 Gbps receiver with Ge PIN7 photodiode @ 10 Gbps, $P_{opt} = 10.8$ μW ($Q = 6$)

Equivalent Input Noise Current

Tab. 5.9 lists the main equivalent input noise current sources. It can be clearly seen that the input transistor of the transimpedance amplifier is the largest noise source followed by the feedback resistor. Thus the design of the first amplifier stage is crucial for the overall performance of the optical receiver.

Table 5.9: Equivalent input noise current contribution with vertical Ge PIN7 photodetector

Device	Equivalent input noise current (nA)	Percent of total %
TIA/$T1$	648.4	72.12
TIA/R_{fb}	60.7	6.75
Diode/R_s	23.7	2.64
Dummy/T_2	22.7	2.52
TIA/T_2	17.4	1.93
Other	126.2	14.04
Total	899.1	100.00

5.3.2 Simulation Results with Lateral Ge 10E1 Photodetector

In contrast to the wire bonded PIN7 photodiode the heterogeneously integrated 10E1 Ge photodetector allows the usage of the receiver without gain reduction. Therefore the transimpedance of the first amplifier stage was increased to 4.2 kΩ for the following simulations which results in a total transimpedance of 275 kΩ for the whole receiver chain.

Receiver Gain

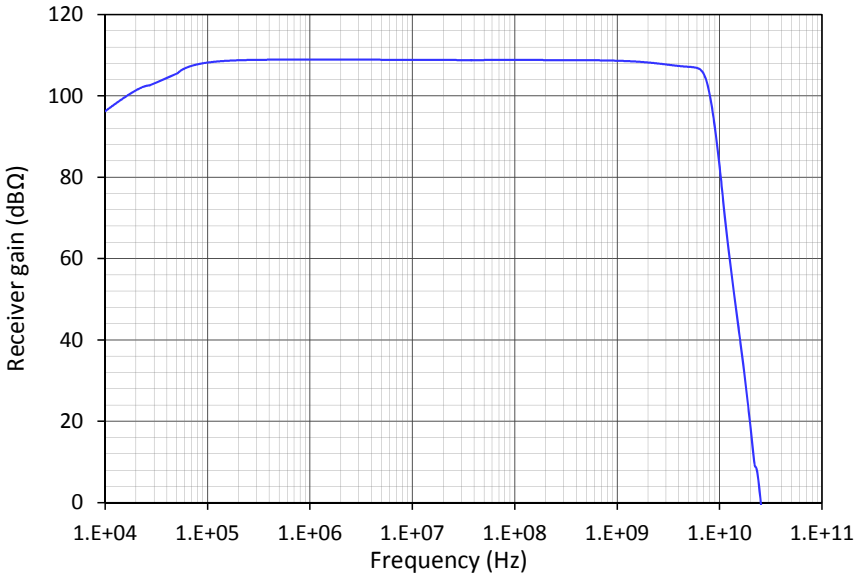


Figure 5.15: Receiver gain with lateral Ge 10E1 photodetector

Fig. 5.15 shows the simulated gain of the receiver in combination with the heterogeneously integrated 10E1 Ge photodetector. In contrast to the usage of the PIN7 photodiode the gain has not to be reduced to reach the required bandwidth of around 7 GHz.

Transient Response

The simulated transient response of the receiver in combination with the heterogeneously integrated Ge 10E1 photodetector at a data rate of 10 Gbps and a PRBS31 signal is shown in fig. 5.16. The transient overshoot is minor and even at short pulses the full voltage swing is nearly reached. Therefore it can be concluded that the receiver in combination with the 10E1 photodiode is capable of a data rate of 10 Gbps even without gain reduction.

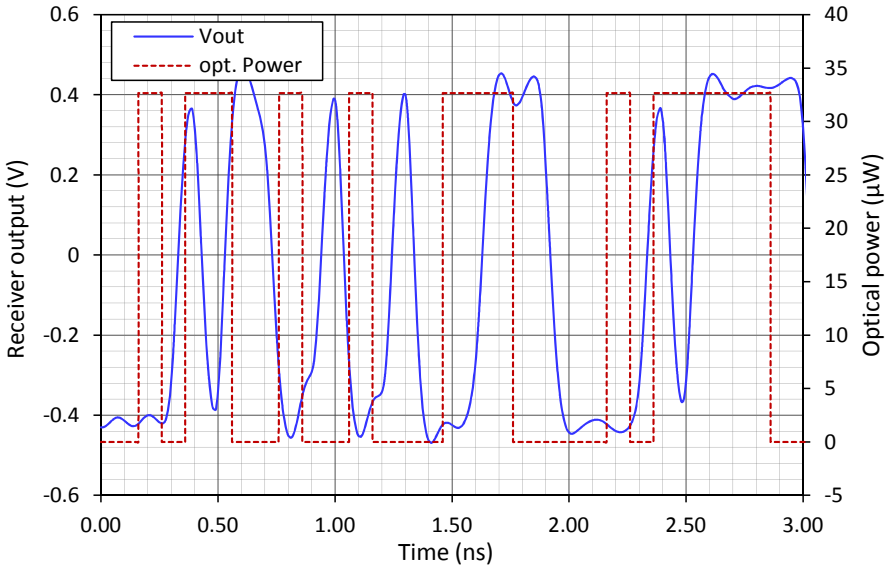


Figure 5.16: Transient response with lateral Ge 10E1 photodetector

Eye Diagram

Fig. 5.17 shows the eye diagram of the receiver together with the 10E1 photodiode at a 10 Gbps PRBS31 data signal and a Q-factor of $Q = 6$ ($BER = 10^{-9}$). To reach $Q = 6$ a simulated optical input power of 14.6 μW was needed. This relative high input power is a result of the low photodiode responsivity $R = 0.15$ (tab. 3.9). Although the gain of the receiver is more than doubled compared to the receiver with the PIN7 photodiode only a lower sensitivity of -18.3 dBm ($BER = 10^{-9}$) is reached due to the poor responsivity of the 10E1 photodetector.

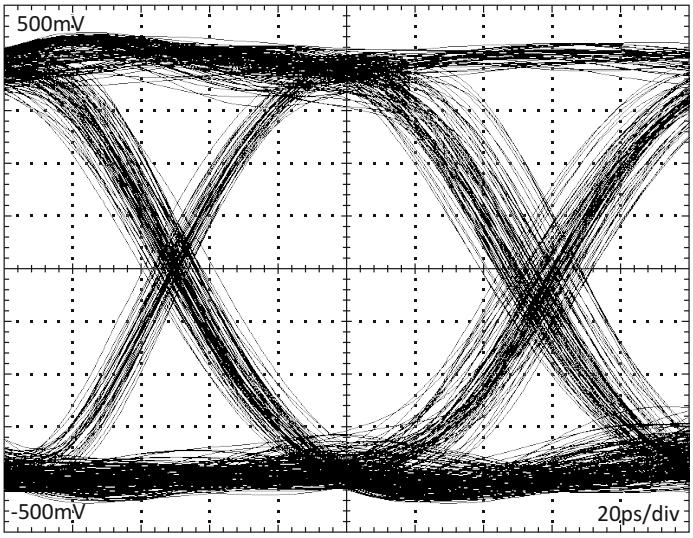


Figure 5.17: Eye diagram of 10 Gbps receiver with Ge 10E1 photodiode @ 10 Gbps, $P_{opt} = 14.6\ \mu$W ($Q = 6$)

Equivalent Input Noise Current

The main equivalent input noise current sources are listed in tab. 5.10. The input transistor of the transimpedance amplifier is once again the largest noise source followed by the feedback resistor R_{fb}. Nevertheless is the noise generated by the input transistor only on-third compared to the receiver configuration with the wire bonded PIN7 photodetector. This can be explained by the smaller parasitic components of the heterogeneously integrated 10E1 photodiode and by the doubled transimpedance compared to the receiver with the PIN7 photodetector.

Table 5.10: Equivalent input noise current contribution with lateral Ge 10E1 photodetector

Device	Equivalent input noise current (nA)	Percent of total %
TIA/$T1$	228.6	62.45
TIA/R_{fb}	65.7	17.95
TIA/T_2	15.4	4.21
Dummy/T_2	7.6	2.09
Dummy/T_1	5.5	1.51
Other	43.6	11.79
Total	366.4	100.00

5.3.3 Simulation Results with Vertical InP/InGaAs Photodetector

The InP/InGaAs photodetector is as already mentioned also heterogeneously integrated to minimize the parasitic components of the connection between photodiode and receiver. Therefore the following simulations were accomplished without reducing the receiver gain.

Receiver Gain

The simulated gain of the receiver in combination with the heterogeneously integrated InP/InGaAs photodiode at a total transimpedance of 275 kΩ is shown in fig. 5.18. Like as at the other receiver photodiode combinations the bandwidth is in the range of 7 GHz and thus is also high enough for a data rate of 10 Gbps.

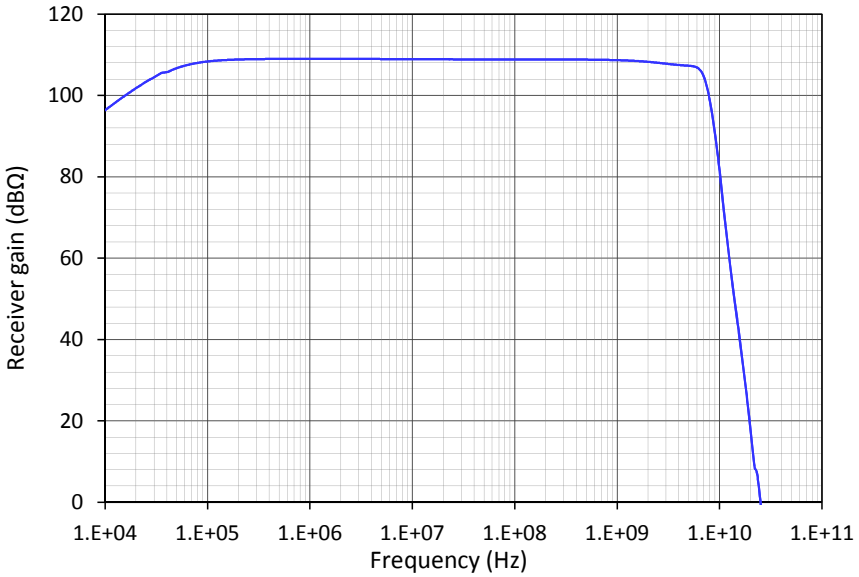


Figure 5.18: Receiver gain with vertical InP/InGaAs photodetector

Transient Response

The transient response of the receiver/photodetector combination simulated at a data rate of 10 Gbps using a PRBS31 signal is shown in fig. 5.19. The full voltage swing is nearly reached even at short pulses and the overshoot is minor. Therefore it can be concluded that the receiver together with the InP/InGaAs photodiode is fast enough to transmit a 10 Gbps data signal even without gain reduction.

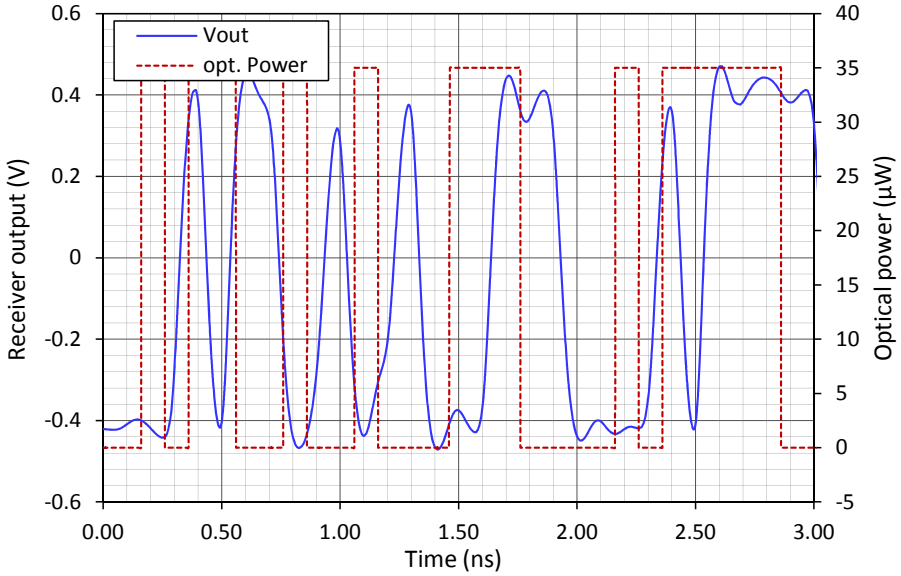


Figure 5.19: Transient response with vertical InP/InGaAs photodetector

Eye Diagram

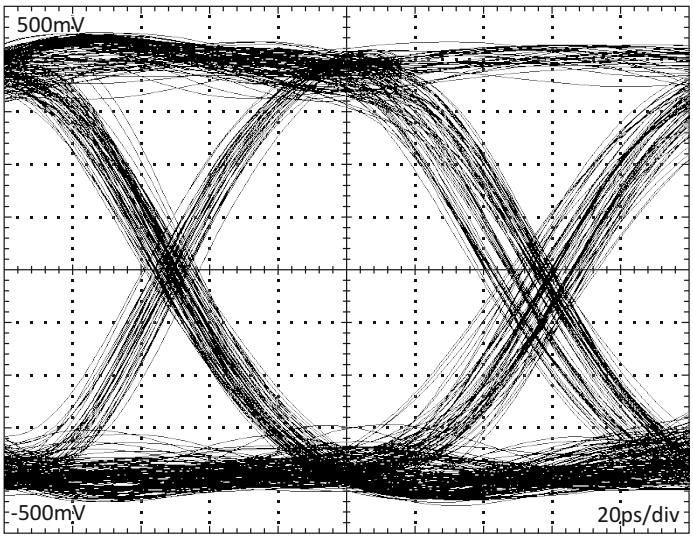


Figure 5.20: Eye diagram of 10 Gbps receiver with InP/InGaAs photodiode @ 10 Gbps, $P_{opt} = 16.7\ \mu W$ ($Q = 6$)

Fig. 5.20 shows the simulated eye diagram of the receiver in combination with the heterogeneously integrated InP/InGaAs photodiode. The eye diagram was recorded at a 10 Gbps PRBS31 data signal and a Q-factor of $Q = 6$ ($BER = 12^{-9}$). Due to the poor photodiode responsivity of $R = 0.14$ (tab. 3.9) an optical power of 16.7 μW is necessary to reach $Q = 6$. This results in a sensitivity of -17.8 dBm ($BER = 10^{-9}$) which is lower than the responsivity of the receiver with the wire bonded PIN7 photodiode.

Equivalent Input Noise Current

The main noise sources of the receiver in combination with the InP/InGaAs photodetector are summarized in tab. 5.11. The noise level and the noise distribution is similar to the receiver with the 10E1 Ge photodiode. The input transistor of the transimpedance amplifier again generates the largest part of the overall noise followed by the feedback resistor R_{fb} while all other parts of the receiver contribute only 20 % to the equivalent input noise current.

Table 5.11: Equivalent input noise current contribution with vertical InP/InGaAs photodetector

Device	Equivalent input noise current (nA)	Percent of total %
TIA/$T1$	247.9	63.47
TIA/R_{fb}	61.0	15.68
TIA/T_2	15.8	4.06
Diode/R_{Si}	9.9	2.54
Dummy/T_2	7.1	1.82
Other	47.5	12.43
Total	389.2	100.00

5.3.4 Simulation Results of the Receiver with Voltage Input

As mentioned in section 5.2 also a receiver with voltage input for electrical characterization without the use of a photodiode was brought to layout. The voltage input consists of an integrated high resistive poly resistor $R_{in} = 10$ kΩ in series to the TIA input node. This series resistor is used to generate an adequate input current at the TIA input if a voltage signal (i.e. a PRBS31 signal from a pattern generator) is applied. Unfortunately this series resistance also has a parasitic capacitance of around 1 fF which influences the characteristics of the receiver. Therefore the following postlayout simulations were carried out to verify the performance of the receiver with voltage input.

Receiver Gain

Fig. 5.21 shows the simulated gain in dependence of the frequency of the receiver with voltage input. Compared to the receivers with photodiodes the bandwidth of around 7 GHz is not reduced by the parasitics of the input series resistor. Therefore the receiver for electrical characterization should be also fast enough to transmit a 10 Gbps data signal.

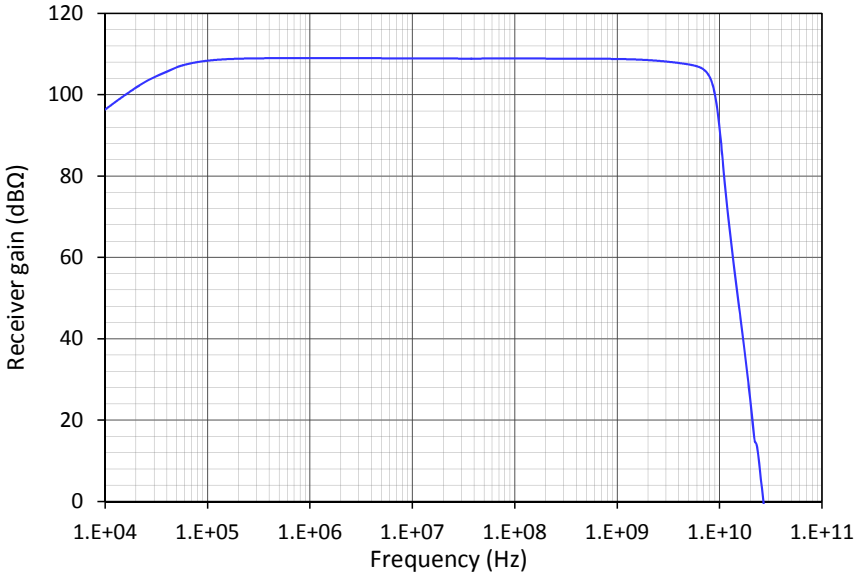


Figure 5.21: Gain of receiver with voltage input

Transient Response

The transient response of the receiver with voltage input simulated at a data rate of 10 Gbps using a PRBS31 signal is shown in fig. 5.22. The amplitude of the voltage input signal is 35 mVpp which corresponds to a photocurrent of 1.75 μA. The transient response looks similar to the transient responses of the receivers with photodiodes and thus the influence of the series resistance seems to be negligible.

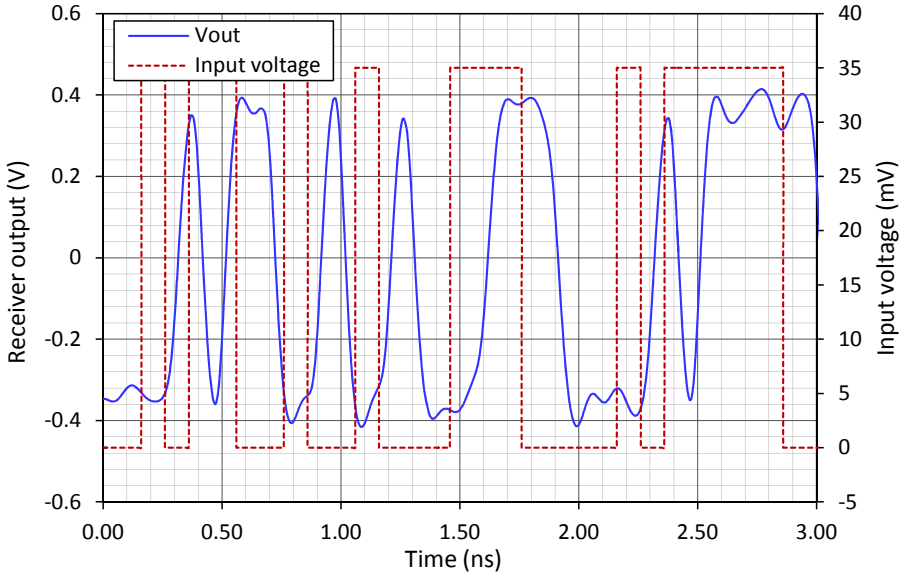


Figure 5.22: Transient response of receiver with voltage input

Eye Diagram

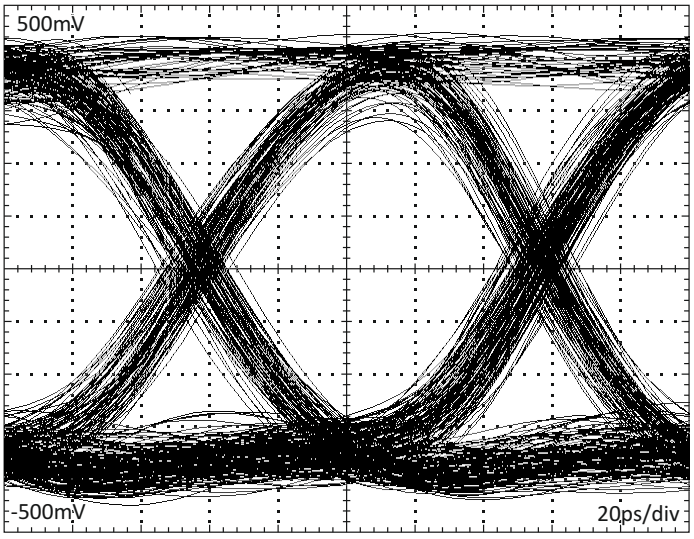


Figure 5.23: Eye diagram of 10 Gbps receiver with voltage input @ 10 Gbps, $V_{in} = 17.5\ \mu V$ ($Q = 6$)

Fig. 5.23 shows the simulated eye diagram of the receiver with voltage input. The eye diagram was recorded at a 10 Gbps PRBS31 data signal and a Q-factor of $Q = 6$ which was reached at an input voltage of 17.5 mV. Considering the 10 kΩ input series resistance, this input voltage value is equal to a photocurrent of 1.75 μA which corresponds to a receiver sensitivity of −27.6 dBm. Comparing this value with the sensitivities of the receivers with heterogeneously integrated photodiodes and considering the sensitivity losses of more than 8 dBm due to the poor photodiode responsivities shows a good accordance of the electrical receiver characteristics.

Equivalent Input Noise Current

Tab. 5.12 shows the main noise sources of the receiver with voltage input. The input transistor of the transimpedance amplifier and the feedback resistor R_{fb} are again the largest noise sources followed by the series input resistor R_{in} of the voltage input. Nevertheless the equivalent input noise current is only insignificantly larger than the noise generated by the receivers with heterogeneously integrated photodiodes. This explains also the similar sensitivity values of the different receiver configurations (10E1 photodiode, InP/InGaAs photodetector and voltage input) if the sensitivity losses due to the poor photodiode responsivities are considered.

Table 5.12: Equivalent input noise current contribution of receiver with voltage input

Device	Equivalent input noise current (nA)	Percent of total %
TIA/$T1$	141.8	35.94
TIA/R_{fb}	76.7	18.67
TIA/R_{in}	70.9	17.97
Dummy/T_2	24.4	6.19
TIA/T_2	23.4	5.93
Other	57.3	15.30
Total	394.5	100.00

5.3.5 Summary Postlayout Simulation

The postlayout simulation results of the relevant receiver parameters for the three used photodetector models (PIN7, 10E1, IMEC) and the receiver with voltage input for electrical characterization are summarized in tab. 5.13.

The simulation results show that there are only minor differences between the receiver performance of the lateral Ge 10E1 and the InP/InGaAs photodetector of IMEC. The vertically, wire bonded PIN7 photodiode has large parasitic capacitances and thus the transimpedance of the TIA had to be reduced to achieve the required bandwidth. Another drawback of the PIN7 photodetector is the large equivalent input noise current which

Table 5.13: Postlayout simulation results for the different used photodetectors models

	Parameter	Simulated values PIN7	10E1	IMEC	V input
TIA	Transimpedance	2.0 kΩ	4.2 kΩ	4.2 kΩ	4.2 kΩ
	Bandwidth	7.88 GHz	8.76 GHz	8.41 GHz	9.46 GHz
First limiting amplifier	Gain	2.2			
	Bandwidth	9.88 GHz			
Second limiting amplifier	Gain	5.3			
	Bandwidth	8.85 GHz			
50 Ω output driver	Gain	5.8			
	Bandwidth	8.66 GHz			
Complete receiver (with bond wires)	Supply voltage	3.3 V			
	Power consumption	175 mW			
	Total transimpedance	130 kΩ	275 kΩ	275 kΩ	275 kΩ
	Bandwidth	6.39 GHz	6.81 GHz	6.59 GHz	7.17 GHz
	Lower cutoff frequency	19.01 kHz	52.24 kHz	41.87 kHz	40.15 kHz
	Output swing @ 50 Ω	800 mVpp			
	Equivalent input noise current	899 nA	366 nA	389 nA	395 nA
	Input signal (10 Gbps, $BER = 10^{-9}$)	10.8 μW	14.6 μW	16.7 μW	1.75 μA
	Photodiode responsivity ($\lambda = 1550$ nm)	0.50 A/W	0.15 A/W	0.14 A/W	1.00 A/W
	Sensitivity (10 Gbps, BER=10^{-9})	−19.7 dBm	−18.3 dBm	−17.8 dBm	−27.6 dBm
	Sensitivity (1 A/W) (10 Gbps, $BER = 10^{-9}$)	−22.7 dBm	−26.6 dBm	−26.3 dBm	−27.6 dBm

reduces the sensitivity of the receiver. However, another important parameter of an optical receiver is the responsivity of the used photodiode. Unfortunately the responsivities of the two waveguide photodetectors, provided by CEA-LETI and IMEC, are very low compared to state-of-the-art detectors [37], [44], [45], [51]. Thus the sensitivities of the receivers, using waveguide photodiodes, are lower than the sensitivity of the receiver with conventional wire bonded photodiodes. It can be concluded that the higher parasitics of conventional wire bonded photodiodes have less effect on the receiver sensitivities than the low responsivities of the waveguide photodiodes.

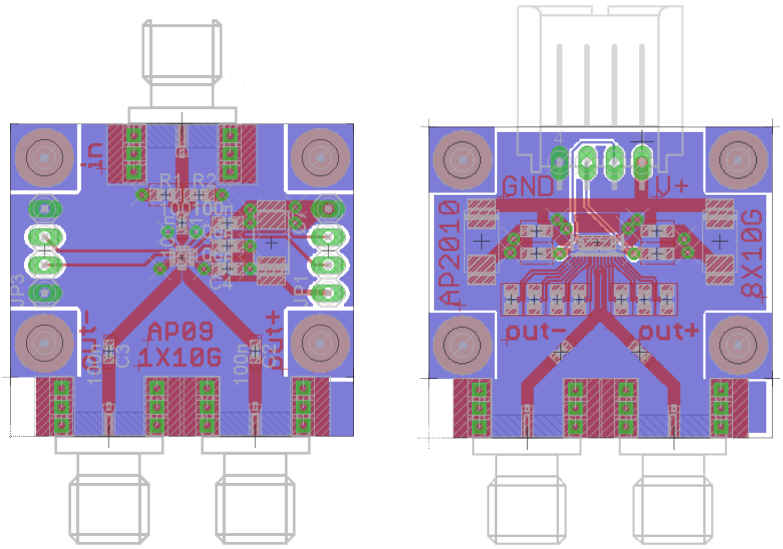
To compare the influence of the different connection structures on the receiver performance, the calculated sensitivities for a photodiode responsivity of 1 A/W are presented in the last row of tab. 5.13. It can be concluded that the novel heterogeneous integration of the photonic wafer on top of the CMOS wafer doubles the sensitivity of the receiver. Nevertheless it is necessary to improve the responsivity of the used waveguide photodetectors to take full advantage of the heterogeneous photodiode integration.

6 Receiver Characterization

To verify the performance of the fabricated receiver several measurements were carried out. To get reliable measurement results all metered receiver chips were bonded together with the used photodetectors on especially designed printed circuit boards (PCB). The test PCBs contain connectors for power supply, bias voltage, gain control, signal input (version for electrical characterization) and signal output. The supply voltage is stabilized by the use of several back-up capacitors. The RF in- and outputs are AC coupled and implemented as SMA connectors. In addition the RF input is terminated with a 50 Ω resistance to avoid reflections caused by impedance mismatch. Depending on the receiver type two different PCB versions were developed – one version for the single channel and another version for the 8-channel receiver. The single-channel PCB can be equipped either with a photodiode or a RF input connector for electrical characterization purposes. The 8-channel version is designed for use with photodiodes exclusively. To save costs only one differential output of the 8-channel receiver is connected to SMA connectors. The other seven differential outputs are terminated by 100 Ω resistances directly on the PCB. The layout of both PCB versions is shown in fig. 6.1.

In a first step the electrical performance of the fabricated receiver lacking a photodiode was measured. As mentioned in chapter 5.2 one version of the single-channel receiver was designed especially for this purpose. The difference to the other receiver versions is the voltage input instead of a current input. The voltage input consists of additional GSG pads and an integrated 10 kΩ resistor in series to the current input of the TIA. The series resistor simulates a photocurrent at the TIA input when a voltage is applied at the GSG pads. Therefore a voltage data signal (eg. PRBS31) can be applied directly to the GSG pads for the electrical characterization of the amplifier.

In a second step the receiver performance together with the three different photodiode types (vertical Ge PIN7, lateral Ge waveguide 10E1 and vertical InP/InGaAs waveguide built by IMEC) was measured. Unfortunately CEA-LETI and IMEC had massive problems with the heterogeneous integration of the waveguide photodetectors on top of the receiver chip. Therefore no heterogeneous integrated demonstrator chips were available until this PhD thesis had to be finished. Instead of working heterogeneous integrated demonstrator chips CEA-LETI and IMEC provided 8-fold arrays of the 10E1, respectively the InP/InGaAs photodiode, for conventional wire bonding. Each array consists of eight waveguide diodes, a grating coupler and an arrayed waveguide grating (AWG). The AWG is fabricated by IMEC and works as wavelength demultiplexer in the wavelength



(a) (b)

Figure 6.1: PCB 1-channel receiver for electrical characterization (a) and PCB 8-channel receiver (b)

range of $1530 - 1560$ nm. Depending on the wavelength of the optical signal only one of the eight diodes is illuminated and generates an electrical signal. Thus it is possible to convert eight data streams of different wavelengths at the same time. Fig. 6.2 shows the InP/InGaAs photodiode array from IMEC.

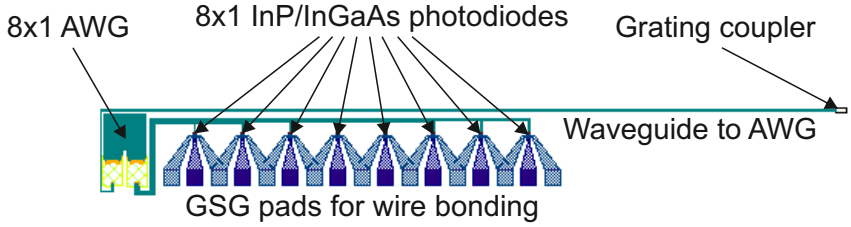


Figure 6.2: 8x1 InP/InGaAs AWG photodiode array for conventional wire bonding [11]

The optical output power of the eight AWG channels in dependence of light wavelength is shown in fig. 6.3.

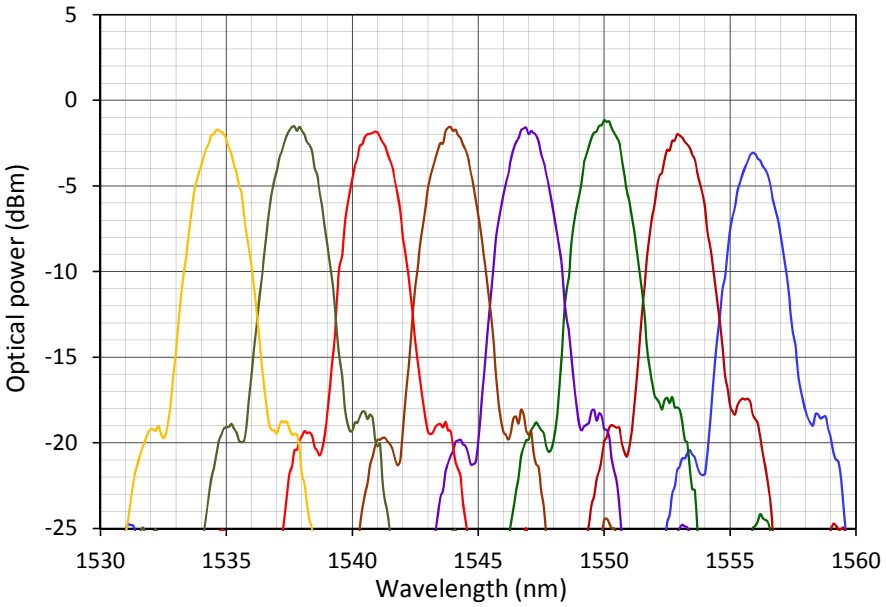


Figure 6.3: AWG optical output power in dependence of light wavelength [12]

6.1 Measurement Setup

To verify the performance of the receiver several measurements were carried out. In a first step the AC response and the transient response of the different receiver configurations were measured. The results were verified by recording the eye diagrams at different data rates and varying input power levels. Afterwards the sensitivity of the receiver was determined by a bit-error rate measurement. In a last step the crosstalk between the different receiver channels was measured to estimate the influence of the AWG crosstalk on the receiver performance.

6.1.1 AC Response

The speed of the different receiver/photodiode combinations was measured by recording their AC response in the frequency range from 10 MHz – 20 GHz using a Rhode&Schwarz ZVR vector network analyzer. As light source a Tunics 1550 wavelength tunable laser source with a wavelength range from $1480 - 1580$ nm and variable output power was used. The tunable laser source is necessary due to the AWGs which are used to demultiplex the optical input signal of the waveguide photodiodes. To measure the AC response of a distinct receiver channel, the wavelength of the light source has to be tuned to the AWG wavelength of the correspondent photodiode (fig. 6.2). The light of the laser source,

modulated by the network analyzer via a Photline DR-DG-40-MO 40 GHz modulator driver and a Photline MX-LN 40 GHz Mach-Zehnder modulator, is used as optical input signal for the receiver (DUT). The AC response of the receiver is determined by sweeping the input frequency RF_{in} from 10 MHz – 20 GHz and plotting the S21 parameter over the frequency. The block diagram of the measurement setup is shown in fig. 6.4.

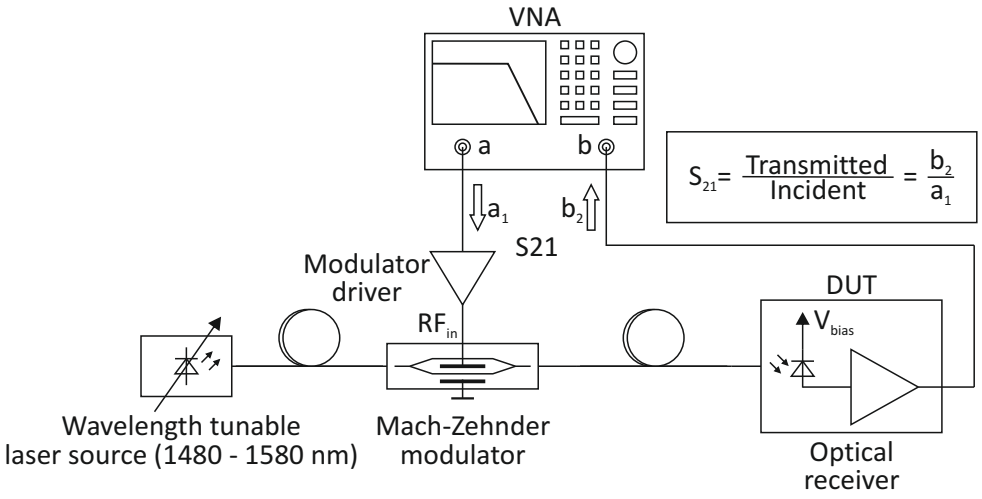


Figure 6.4: Block diagram AC response measurement

The influence of the used cables, the modulator driver, the modulator and the network analyzer itself is eliminated by calibrating the whole measurement setup with a fast reference detector as mentioned in section 3.3.6.

6.1.2 Eye Diagram

The eye diagram is used to verify the transmission performance of the receiver and can also be used to determine other receiver parameters as Q-factor or rise and fall times. Again the tunable laser source Tunis 1550 is used as light source. The optical PRBS31 input signal for the receiver is generated by a 40 GHz Sympuls BPG bit pattern generator which modulates a Mach-Zehnder modulator via a DR-DG-40-MO 40 GHz modulator driver. A optical splitter with a ratio of 50:50 and an optical powermeter were used to determine the power of the incident light. The output signal of the optical receiver is recorded by a Tektronix DSA 8200 sampling oscilloscope and due to the external triggering by the pattern generator a standing eye is generated. The block diagram of the measurement setup is shown in fig. 6.5.

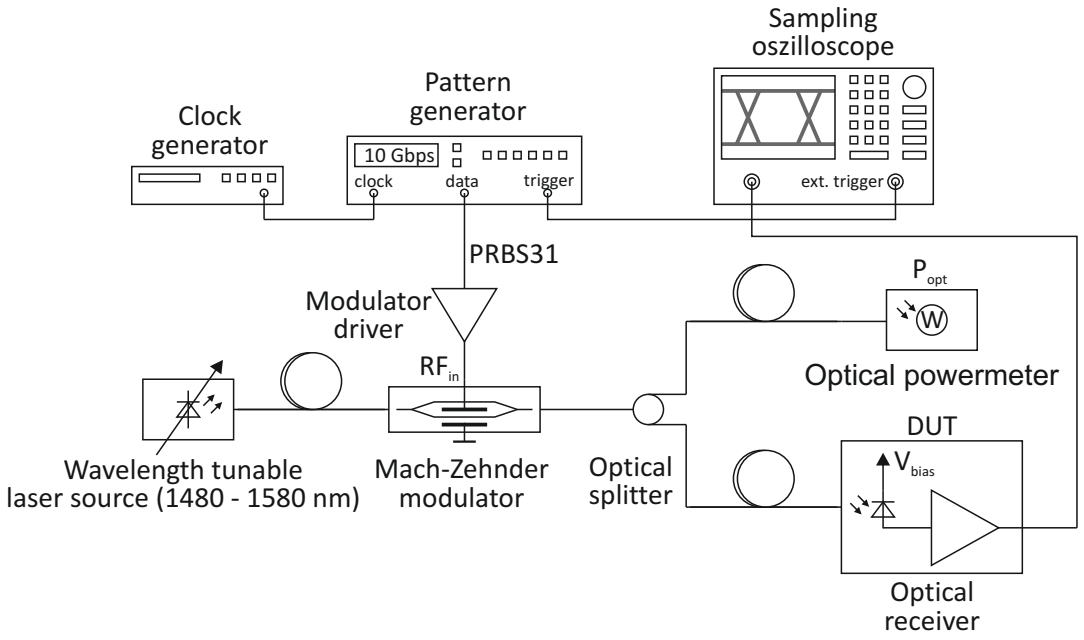


Figure 6.5: Eye diagram measurement

6.1.3 Transient Response

The transient response is recorded to measure the rise time t_r and the fall time t_f of the receiver output signal. The rise and fall times can be used to estimate the maximum possible bit rate B_{max} (6.1) [3].

$$B_{max} = \frac{2}{3(t_r + t_f)} \tag{6.1}$$

Furthermore the transient response can be used to determine a possible transient overshoot. For recording the transient response the same measurement setup as for the eye diagram measurement is used. The only difference is the used bit pattern and the different triggering mode of the sampling oscilloscope.

6.1.4 Sensitivity and Bit-Error Rate

The sensitivity of an optical receiver is defined as the minimum optical input power which is required to achieve a certain bit-error rate. It can be determined by varying the optical input power and counting the occurring bit errors. The bit-error rate is the number of bit errors divided by the total number of transferred bits. For the measurement of the bit-error

rate again a pattern generator with a PRBS31 bit pattern is used to modulate the optical signal. The receiver output is connected to a bit-error rate tester which compares the original bit pattern with the bit pattern at the receiver output. The optical powermeter is used to determine the sensitivity of the receiver at a certain bit-error rate. Fig. 6.6 shows the measurement setup.

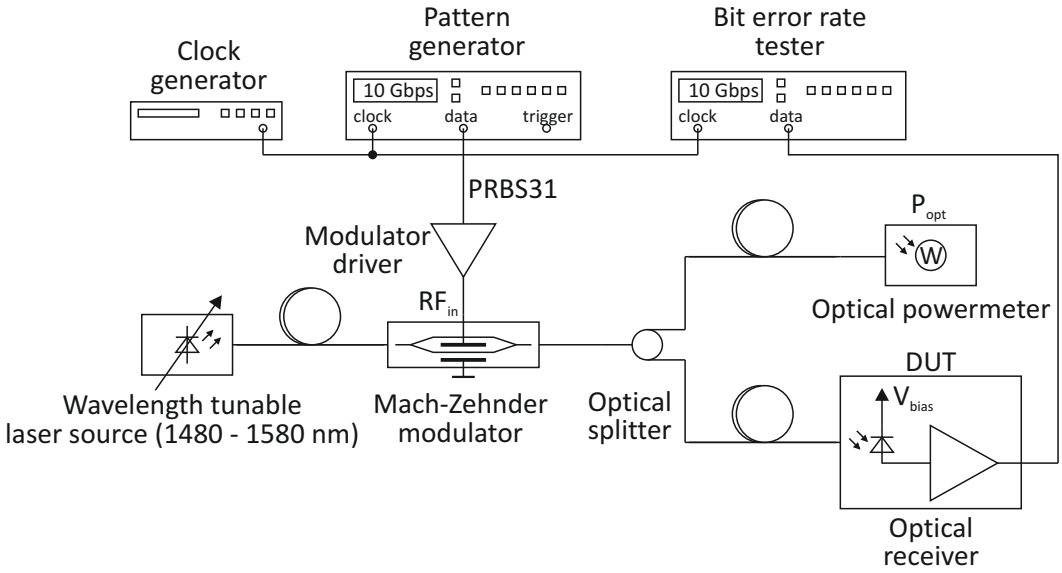


Figure 6.6: Sensitivity and bit-error measurement

6.1.5 Crosstalk

The crosstalk between the different receiver channels is measured by stepping the wavelength of the optical input signal according to fig. 6.3 from $1530 - 1650$ nm and recording the output signal amplitude of one distinct receiver channel. The amplitude reaches its maximum value when the wavelength of the incident optical signal corresponds to the AWG wavelength of the measured channel. The measurement process is controlled by a short LabVIEW program which adjusts the wavelength of the light source, reads the corresponding amplitude value out of the sampling oscilloscope and writes the result into an Excel file. The measurement setup is shown in fig. 6.7.

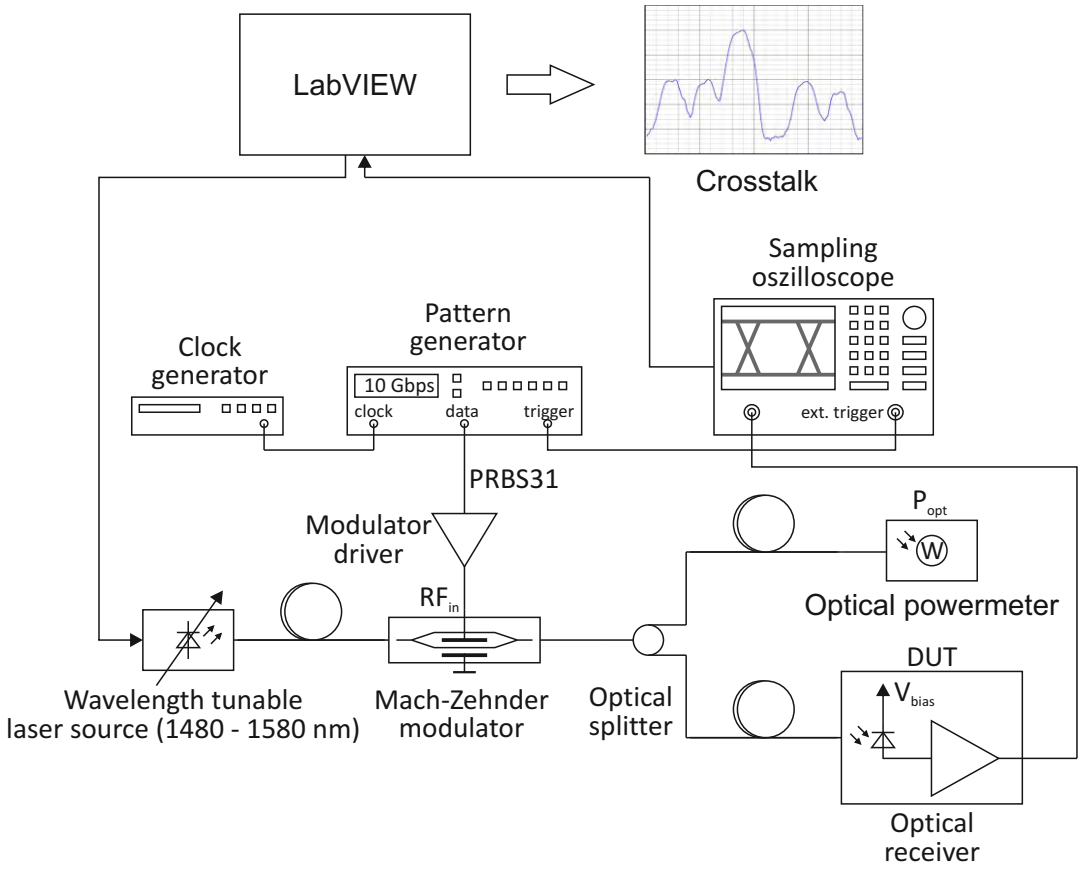


Figure 6.7: Crosstalk measurement

6.2 Electrical Characterization

For the electrical characterization without photodiode a special version of the single channel receiver with additional GSG input pads is used (see section 5.2). As already mentioned the input GSG pads are connected by an on-chip 10 kΩ high resistive poly resistor R_{in} to the TIA input. The high resistive poly material was chosen to minimize the resistor size and thus the parasitic capacitance of the resistor. Nevertheless excessive simulations were performed to evaluate the influence of the additional resistor on the receiver parameters (see section 5.3.4). Together with the coupling capacitor and the 50 Ω termination resistor R_{term}, implemented on the PCB, the receiver can be connected directly to the VNA or the pattern generator. The output power of the VNA P_{dBm} can be adjusted in the range from −20 dBm to +10 dBm. In contrast the output voltage level of the pattern generator is fixed to 1 Vpp. Thus an electrical attenuator is necessary to adjust the PCB input voltage V_{in}. The equivalent current I_{ph} into the TIA input for a given power, respectively

voltage can be calculated by (6.2).

$$I_{ph} = \frac{1}{R_{in}} \sqrt{10^{-3} \cdot 10^{\frac{P_{dBm}}{10}} (R_{term} || R_{in})}, \qquad I_{ph} = \frac{V_{in}}{R_{in}} \tag{6.2}$$

A photomicrograph of the bonded 1-channel receiver chip used for electrical characterization is shown in fig. 6.8.

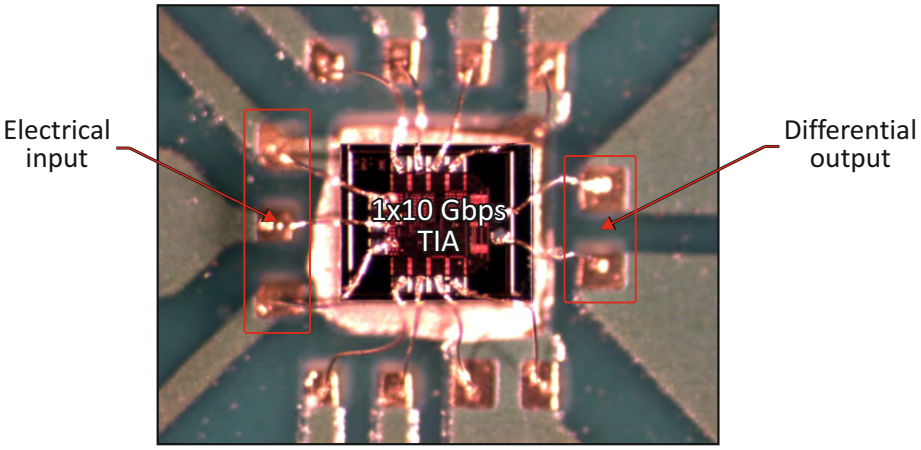


Figure 6.8: Photomicrograph of bonded 1-channel receiver for electrical characterization

As already mentioned the 1-channel receiver version designed for electrical characterization without photodetector has an additional input resistor $R_{in} = 10$ kΩ connected to the TIA input node. Therefore it is possible to connect a voltage input signal directly to the receiver. As already shown in the postlayout simulations (see section 5.3.4) the transimpedance of this receiver configuration has not to be reduced for reaching a data rate of 10 Gbps. Thus the following measurements were performed at a total receiver transimpedance of 275 kΩ.

AC Response

The AC response of the 1-channel receiver without photodiode is shown in fig. 6.9. Despite of the additional parasitic capacitance of R_{in} a bandwidth of 7.59 GHz is reached. The AC response shows, similar to the simulations (see fig. 5.21), a steep gain drop for frequencies above the −3 dB cutoff frequency. The steep gain drop is caused by the fact that the different amplifier stages have nearly the same −3 dB cutoff frequency. Therefore the

whole amplifier shows a behavior similar to a high-order low-pass filter.

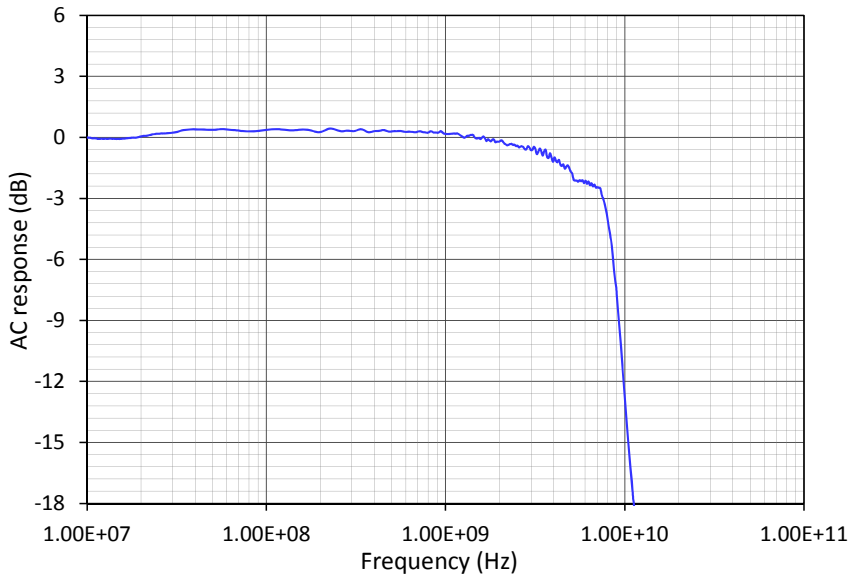


Figure 6.9: AC response of 1-channel receiver without photodiode

Transient Response

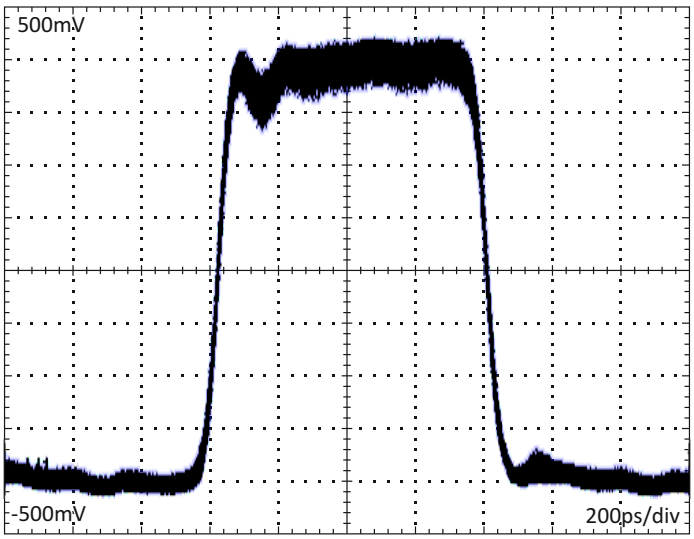


Figure 6.10: Transient response of 1-channel receiver without photodiode @ 1 Gbps

Fig. 6.10 shows the transient response of the electrical characterized 1-channel receiver. The transient response recorded at a data rate of 1 Gbps shows practically no overshoot and only a minor ringing. The rise time of the output signal is $t_r = 55$ ps while the fall time is $t_f = 51$ ps.

Eye Diagram

The eye diagram of the receiver with electrical input shown in fig. 6.11 was recorded at a data rate of 10 Gbps and an input voltage $V_{in} = 50$ mV. This input voltage value leads to a photocurrent of $I_{ph} = 5$ μA at the TIA input node which results in a measured Q-factor of $Q = 11.8$.

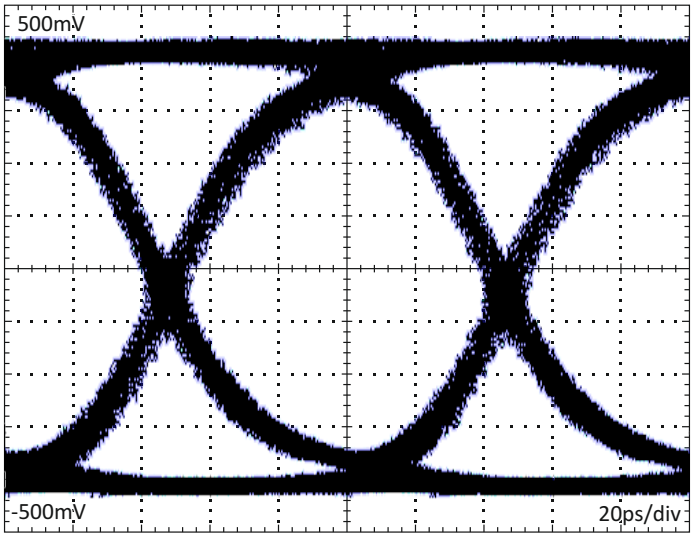


Figure 6.11: Eye diagram of 1-channel receiver without photodiode @ 10 Gbps, $V_{in} = 50$ mV

Sensitivity and Bit-Error Rate

Fig. 6.12 shows the measured bit-error rate of the electrical characterized 1-channel receiver for an electrical 10 Gbps PRBS31 input signal. The receiver reaches a sensitivity of -28.13 dBm at $BER = 10^{-9}$ and -27.52 dBm at $BER = 10^{-12}$. Thus the measured sensitivity at $BER = 10^{-9}$ is slightly higher than the simulated value (see tab. 5.13).

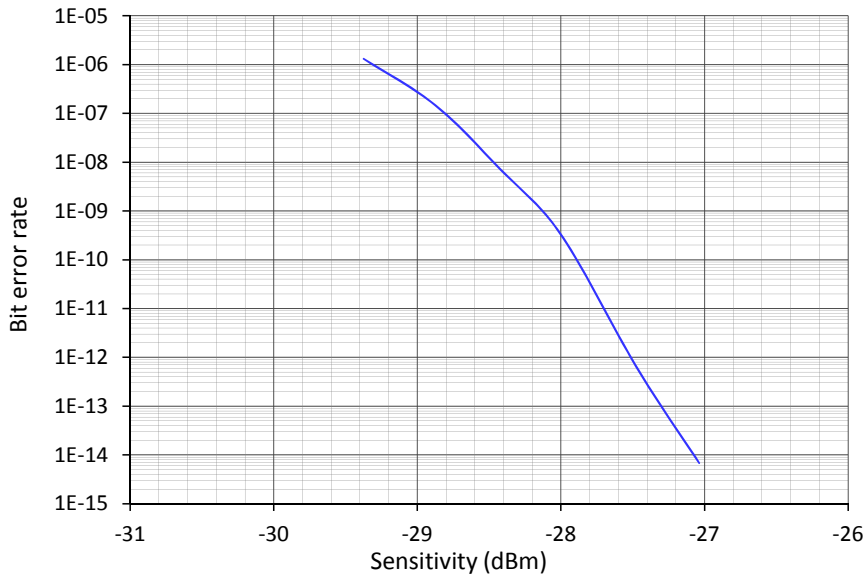


Figure 6.12: Sensitivity of 1-channel receiver without photodiode @ 10 Gbps, PRBS31

6.3 8-channel Receiver with PIN7 Vertical Ge Photodetector

For the characterization of the 8-channel receiver together with the PIN7 vertical Ge photodetectors the receiver version with bond pads for conventional wire bonded photodiodes was used. Due to the large parasitics of the wire bonded photodiodes the total

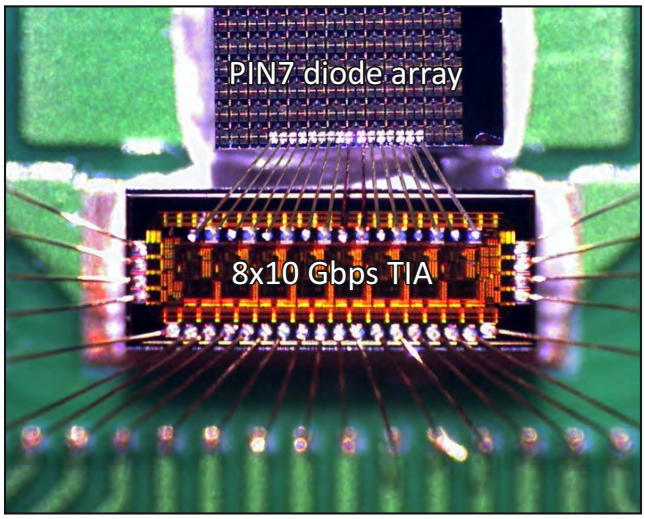


Figure 6.13: Photomicrograph of the 8-channel receiver with wire bonded PIN7 photodiodes

transimpedance of the receiver had to be reduced to 125 kΩ as already shown in the postlayout simulations. The receiver chip and the diode array are clued on the test PCB side by side as near as possible to avoid long bond wires between photodiode and receiver chip. The optical input signal is coupled directly from the fiber into the photodetector. A photomicrograph of the 8-channel receiver chip with the conventional wire bonded PIN7 photodiodes is shown in fig. 6.13.

In contrast to the electrical measurements described in section 6.2 an optical input signal was used instead of an electrical input signal for the following measurements. The optical data signal was coupled directly from the fiber into the wire bonded photodiode which was reverse biased by $V_{bias} = 2.0$ V.

AC Response

Fig. 6.14 shows the measured AC response of the 8-channel receiver together with the wire bonded PIN7 Ge photodiodes at a bias voltage $V_{bias} = 2.0$ V. This receiver photodiode/combination has a bandwidth of 7.89 GHz and shows no gain peaking. The frequency response also shows a steep gain drop for frequencies higher than the −3 dB cutoff frequency. Compared to the simulation results the measured AC response shows a slightly higher bandwidth than the simulated frequency response.

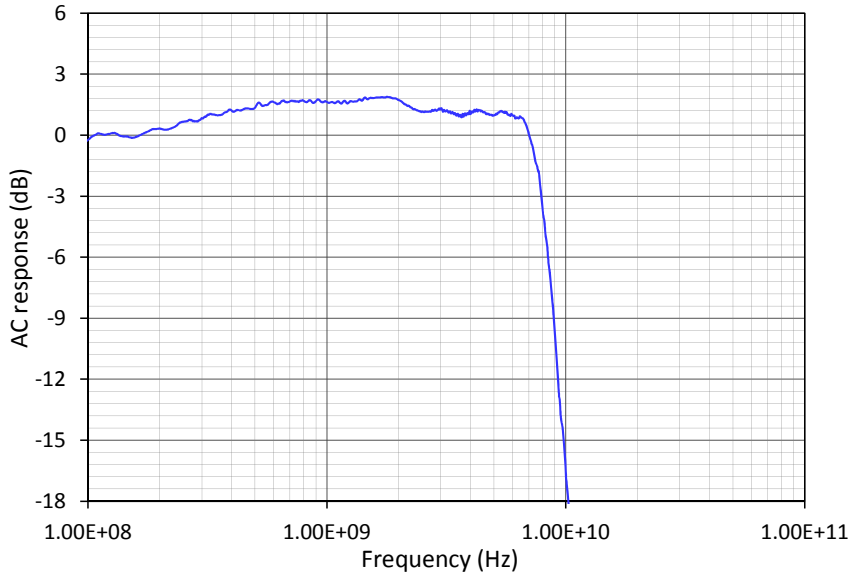


Figure 6.14: AC response of 8-channel receiver with PIN7 photodiode

Transient Response

The transient response of the 8-channel receiver with PIN7 photodiodes is shown in fig. 6.15. The transient response recorded at a data rate of 1 Gbps shows no overshoot or ringing. The analysis of the transient leads to a rise time $t_r = 63$ ps and a fall time $t_f = 61$ ps.

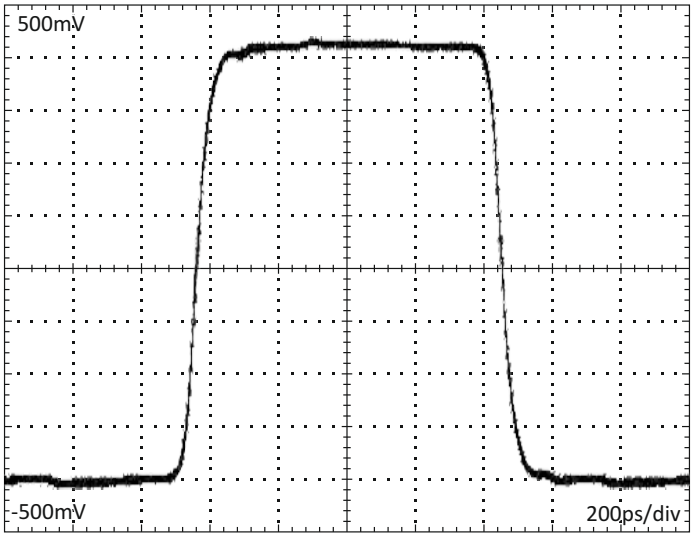


Figure 6.15: Transient response of 8-channel receiver with PIN7 photodiode @ 1 Gbps

Eye Diagram

The eye diagram of the receiver with the wire bonded PIN7 photodiodes shown in fig. 6.16 was recorded using an optical 10 Gbps PRBS31 input signal. To reach a Q-factor of $Q = 6$ an optical input power of $P_{opt} = 10$ μW is necessary.

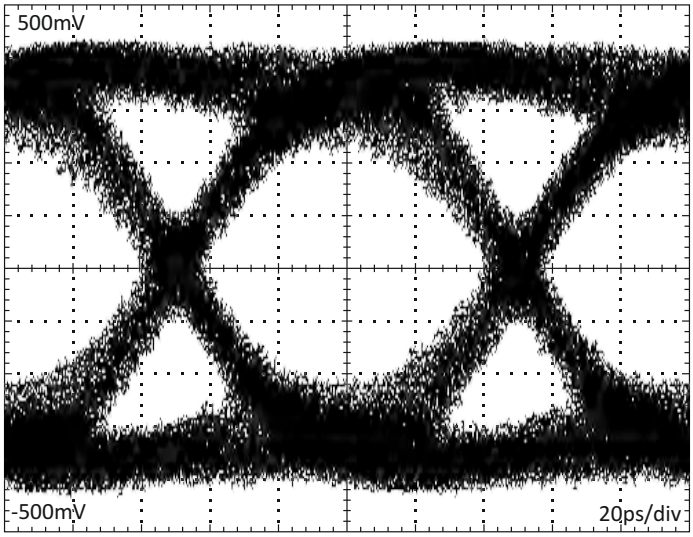


Figure 6.16: Eye diagram 8-channel of receiver with PIN7 photodiode @ 10 Gbps, $P_{opt} = 10\ \mu\text{W}$ ($Q = 6$)

Sensitivity and Bit-Error Rate

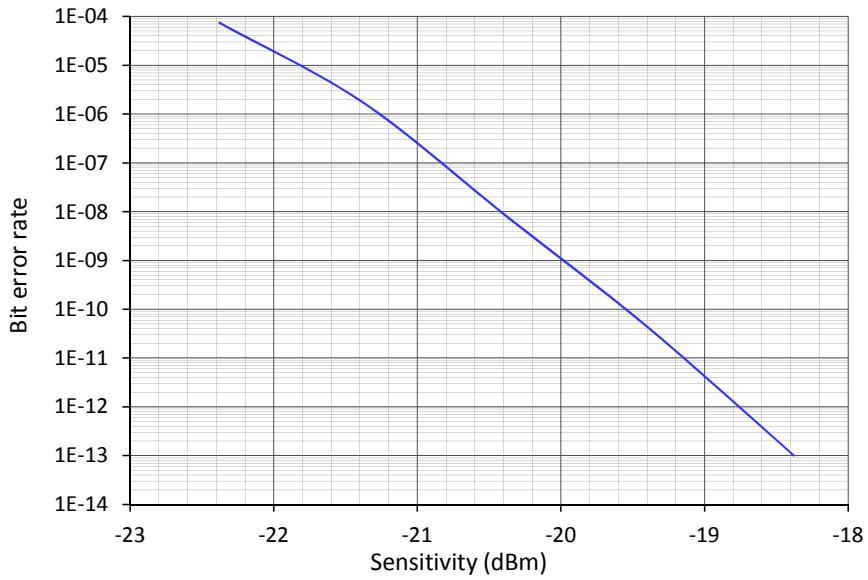


Figure 6.17: Sensitivity of 8-channel receiver with PIN7 photodiode @ 10 Gbps, PRBS31

Fig. 6.17 shows the measured bit-error rate of the 8-channel receiver with the wire bonded PIN7 photodetector array in dependence on the optical input power. The receiver reaches a sensitivity of -20.00 dBm at $BER = 10^{-9}$ and -18.75 dBm at $BER = 10^{-12}$ which confirms the simulation results (see tab. 5.13).

6.4 8-Channel Receiver with IMEC Vertical InP/InGaAs Photodetector

Originally the vertical InP/InGaAs waveguide photodetector, fabricated by IMEC, was designed for heterogeneous integration on top of the CMOS chip, but due to massive problems with the heterogeneous integration no heterogeneously integrated demonstrators were available. Therefore a photodetector version with GSG pads for conventional wire bonding was used for the characterization. The used diodes are combined in an array and connected by waveguides to an AWG. The AWG distributes the optical signal depending on its wavelength to the individual diodes. Fig. 6.2 shows the layout of the photodiodes and the waveguide structures.

For the characterization the diode chip was also clued on the test PCB beside the receiver chip and connected with the amplifier by conventional wire bonding. During the bonding process it turned out that the quality of the GSG bond pads on the diode chip was very bad. The pads are highly sensitive to mechanical stress and thus it is impossible to wire bond the photodiodes conventionally to the receiver chip. However, after some unsuccessful bonding attempts an unconventional method was found to establish an electrical connection between the diodes and the receiver chip. The 'Use bond wire as spring' bonding process is illustrated in fig. 6.18. In a first step the bond wire is bonded conventionally to the TIA input pad (1). Then the wire is bended sharp (2) and cut off (3). In a last step the loose bond wire end is moved to the photodiode pad (4). The sharp bend in the bond wire works as spring (5) and presses the loose bond wire end onto the diode pad (6).

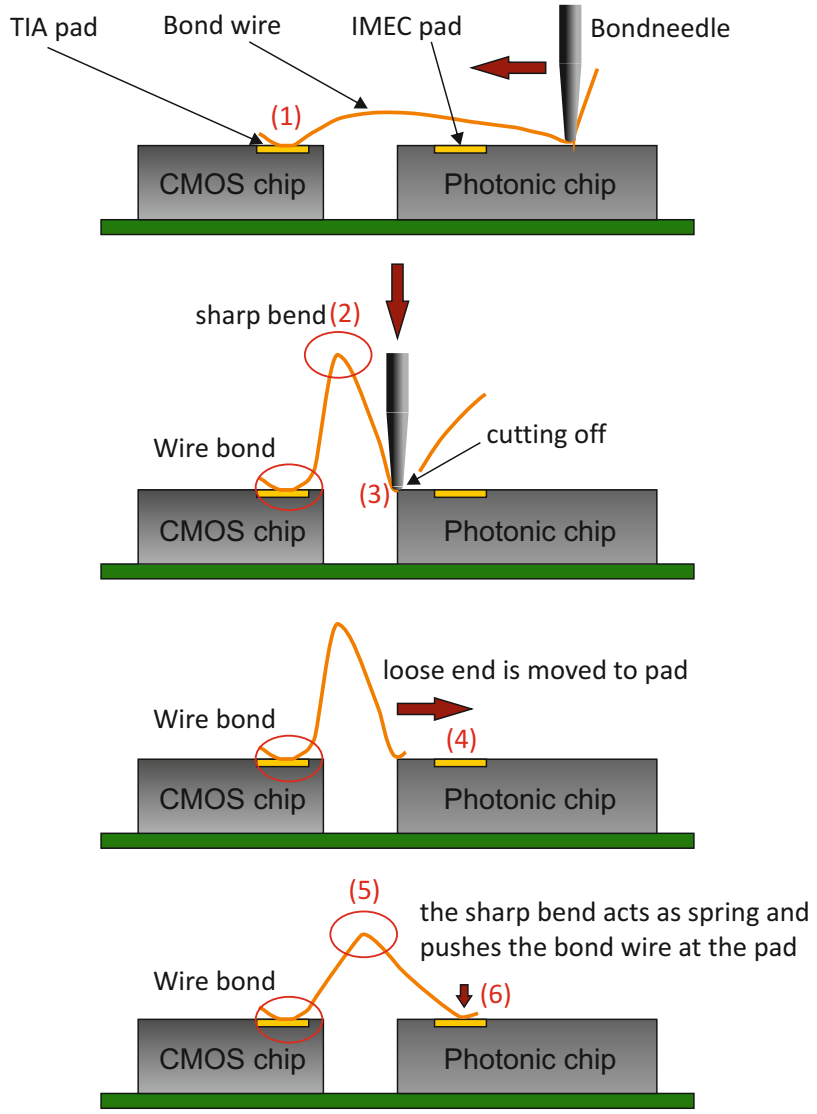


Figure 6.18: Unconventional 'Use bond wire as spring' bonding technique©R. Enne

Nevertheless the pad of one photodiode was destroyed during the unsuccessful bonding attempts and thus only seven photodetectors could be connected to the receiver. A photomicrograph of the 8-channel receiver chip with the unconventional wire bonded photodiode array is shown in fig. 6.19.

As already mentioned the InP/InGaAs photodetectors are arranged in an 8-fold array. The diode array consists of eight waveguide photodiodes, a grating coupler and an AWG which is used as wavelength dependent demultiplexer in the wavelength range of 1530 – 1560 nm.

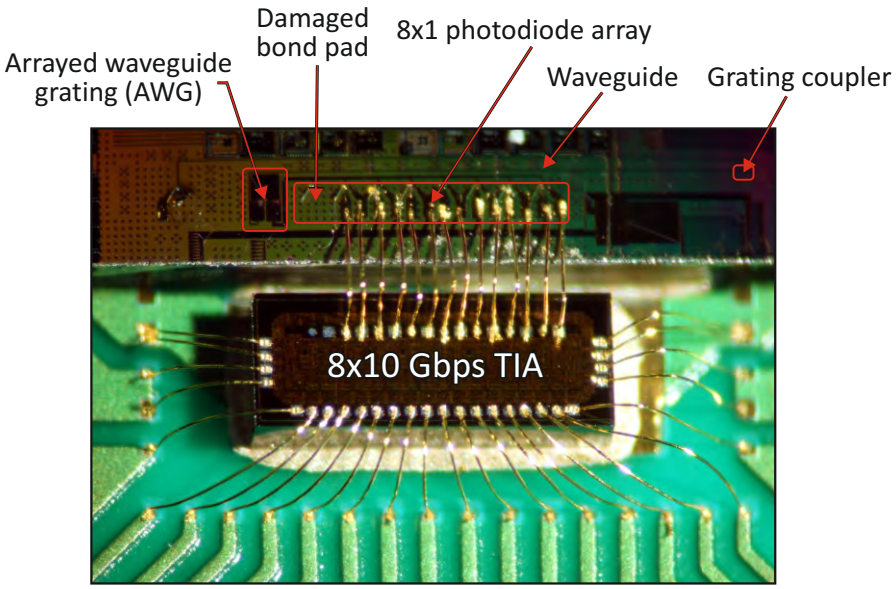


Figure 6.19: Photomicrograph of the 8-channel receiver with unconventional bonded InP/InGaAs photodiode array

The light coming from the fiber is coupled into the AWG via the grating coupler, is demultiplexed and depending on its wavelength only one of the eight diodes is illuminated. Therefore it is necessary for the following measurements to tune the wavelength of the optical input signal to the AWG wavelength of the receiver channel to be measured. Due to the fact that the diode array is wire bonded instead of being heterogeneously integrated on top of the CMOS chip the parasitics of the connection structure are higher than estimated in the simulations. Therefore the total transimpedance of the receiver had to be reduced to 100 kΩ to reach the requested data rate of 10 Gbps.

AC Response

Fig. 6.20 shows the measured frequency response of the 8-channel receiver together with the 8-fold InP/InGaAs photodiode array at a bias voltage $V_{bias} = 7.0$ V. The −3 dB cutoff frequency is reached at 7.03 GHz. The AC response is flat up to 5 GHz, has a gain peak of about 1.5 dB at a frequency of 6 GHz and shows also a steep gain drop at frequencies higher than the −3 dB cutoff frequency. As already mentioned the steep gain drop is caused by the fact that the different receiver stages have similar −3 dB cutoff frequencies. Therefore the whole receiver shows a frequency behavior like a high-order low-pass filter.

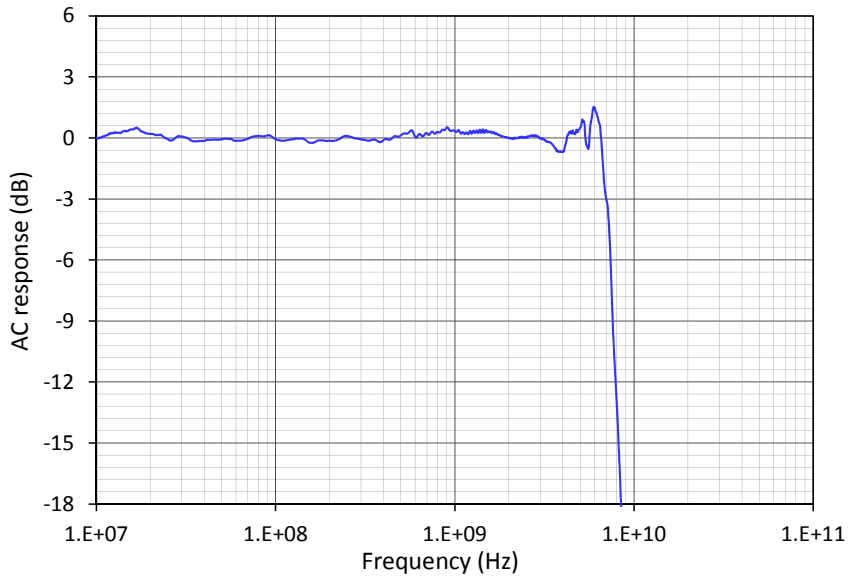


Figure 6.20: AC response of 8-channel receiver with InP/InGaAs waveguide photodiode

Transient Response

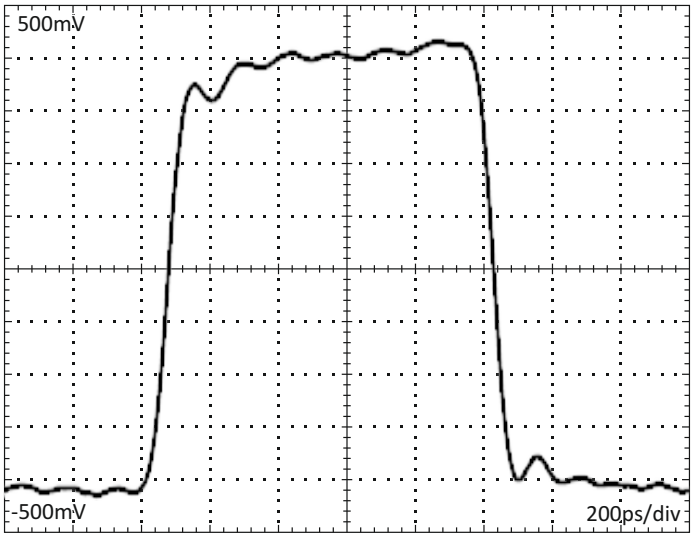


Figure 6.21: Transient response of 8-channel receiver with InP/InGaAs waveguide photodiode @ 1 Gbps

Fig. 6.21 shows the transient response of the 8-channel receiver together with the wire bonded InP/InGaAs photodiode array. The relative large rise- and fall times of $t_r = 73$ ps and $t_f = 67$ ps are caused by the large parasitics of the wire bonded photodetector array.

Eye Diagram

The eye diagram of the receiver in combination with the wire bonded InP/InGaAs photodetector array shown in fig. 6.22 was recorded using a 10 Gbps PRBS31 data signal at a bias voltage $V_{bias} = 7.0$ V. Due to the poor photodiode responsivity of only 0.14 A/W (tab. 3.9) and the reduced receiver transimpedance of 100 kΩ an optical input power $P_{opt} = 60$ μW is required to reach a Q-factor $Q = 6$.

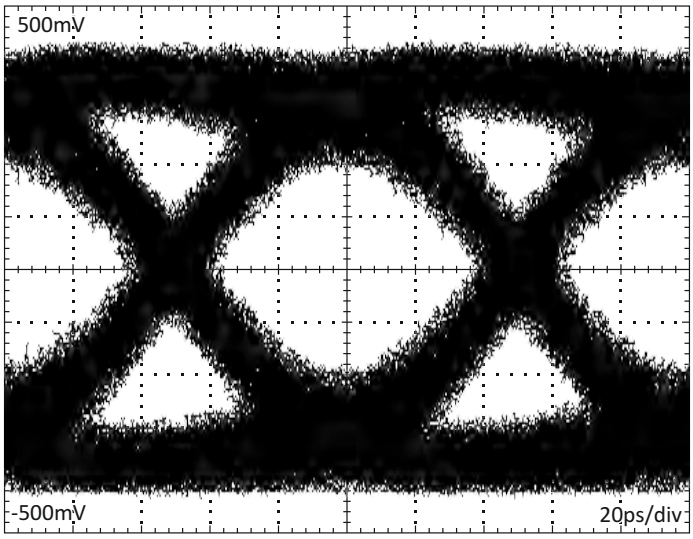


Figure 6.22: Eye diagram of 8-channel receiver with InP/InGaAs waveguide photodiode @ 10 Gbps, $P_{opt} = 60$ μW ($Q = 6$)

Sensitivity and Bit-Error Rate

The bit-error rate of the receiver with the InP/InGaAs photodiode array was recorded using an optical 10 Gbps PRBS31 input signal at a bias voltage $V_{bias} = 7.0$ V. As shown in fig. 6.23 the receiver has a sensitivity of only -12.60 dBm at $BER = 10^{-9}$ and -11.33 dBm at $BER = 10^{-12}$. These low responsivity values are not really surprising if the poor photodiode responsivity of 0.14 A/W and the reduced receiver transimpedance of only 100 kΩ are considered.

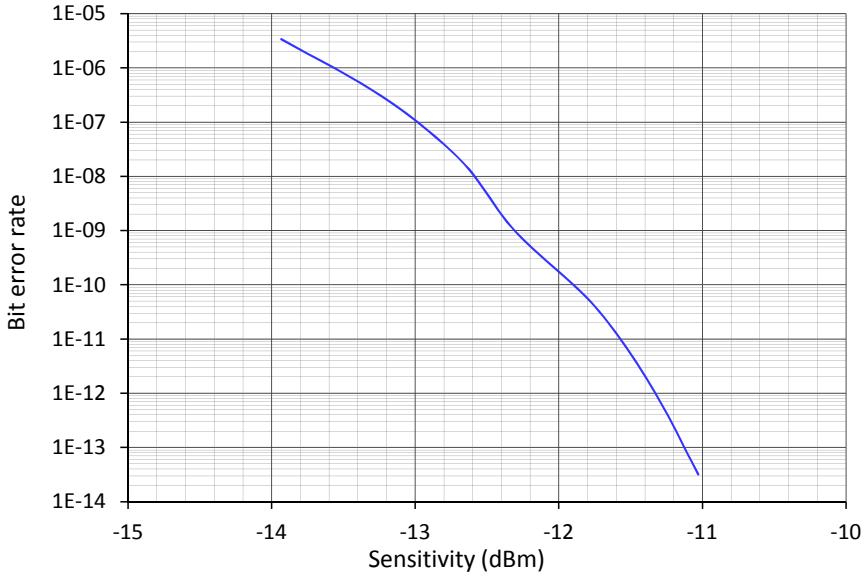


Figure 6.23: Sensitivity of 8-channel receiver with InP/InGaAs waveguide photodiode @ 10 Gbps, PRBS31

Crosstalk

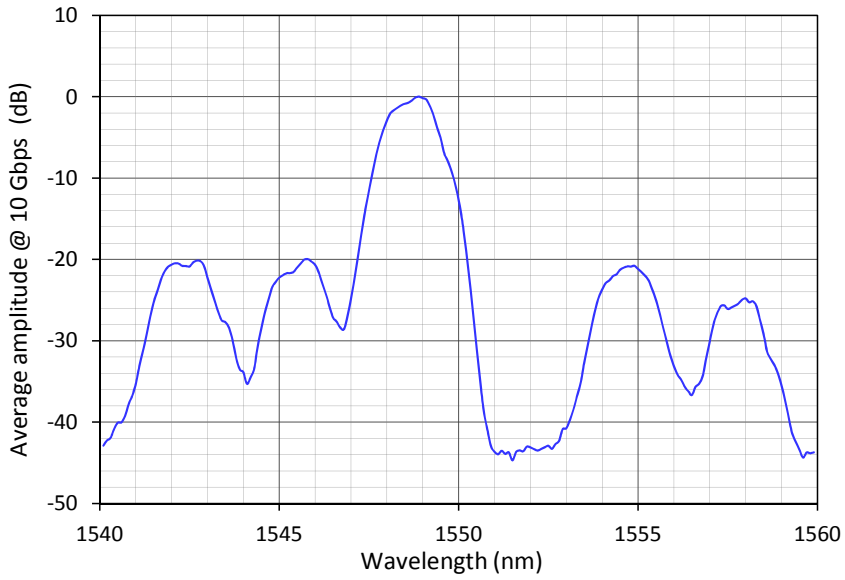


Figure 6.24: Crosstalk of 8-channel receiver with InP/InGaAs waveguide photodiode

Fig. 6.24 shows the crosstalk between the different receiver channels of the receiver together with the InP/InGaAs photodetector array. The crosstalk between the different receiver channels was recorded by stepping the wavelength of the optical 10 Gbps input signal from 1530 – 1560 nm and recording the output signal amplitude of one distinct receiver channel. The graph in fig. 6.24 shows that the crosstalk between two neighboring receiver channels is in the range of −20 dBm. If this result is compared with the optical crosstalk between the neighboring AWG channels (see fig. 6.3) it can be concluded that the measured crosstalk shown in fig. 6.24 is caused mainly by the optical properties of the AWG.

6.5 8-Channel Receiver with LETI 10E1 Ge Photodetector

The lateral Ge waveguide photodetector 10E1 fabricated by CEA-LETI is originally designed for heterogeneous integration on top of the CMOS wafer, but like IMEC CEA-LETI also had massive problems with the heterogeneous integration of the photodiodes. Thus no heterogeneous integrated demonstrators were available for characterization. Instead the photonic chip was clued on a PCB beside the CMOS chip and the photodetectors were conventionally wire bonded to the receiver chip. Similar to the InP/InGaAs photodetectors the lateral Ge diodes are optically connected by waveguides and use an AWG as wavelength demultiplexer. Fig. 6.25 shows a photomicrograph of the 8-channel receiver with the wire bonded photonic chip.

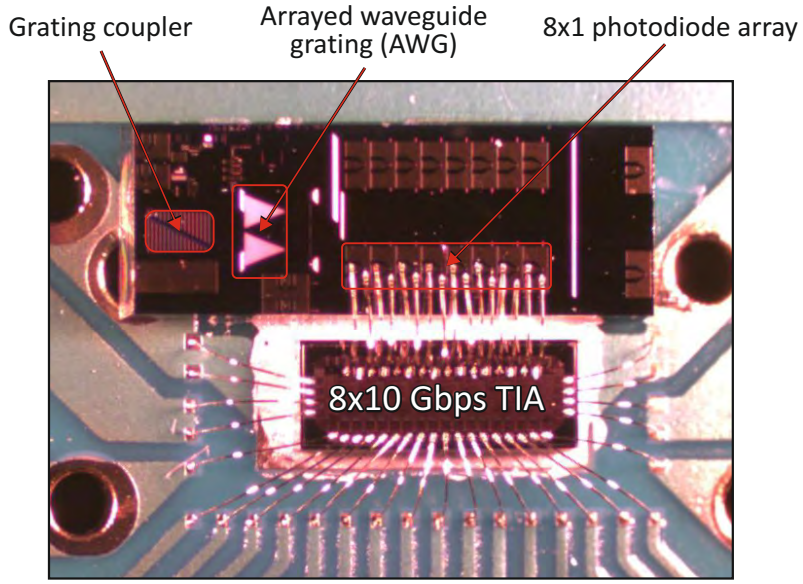


Figure 6.25: Photomicrograph of the 8-channel receiver with wire bonded Ge 10E1 photodiode array

AC Response

The frequency response of the 8-channel receiver in combination with the wire bonded Ge 10E1 waveguide photodetector array at a reverse bias voltage $V_{bias} = 2.0$ V is shown in fig. 6.26. The bandwidth of the receiver together with the Ge photodiodes is around 7 GHz and the AC response also shows a steep gain drop for frequencies above the -3 dB cutoff frequency. The steep gain drop arises due to the combination of a slight gain peak at around 6 GHz and the high-order low-pass characteristic of the amplifier.

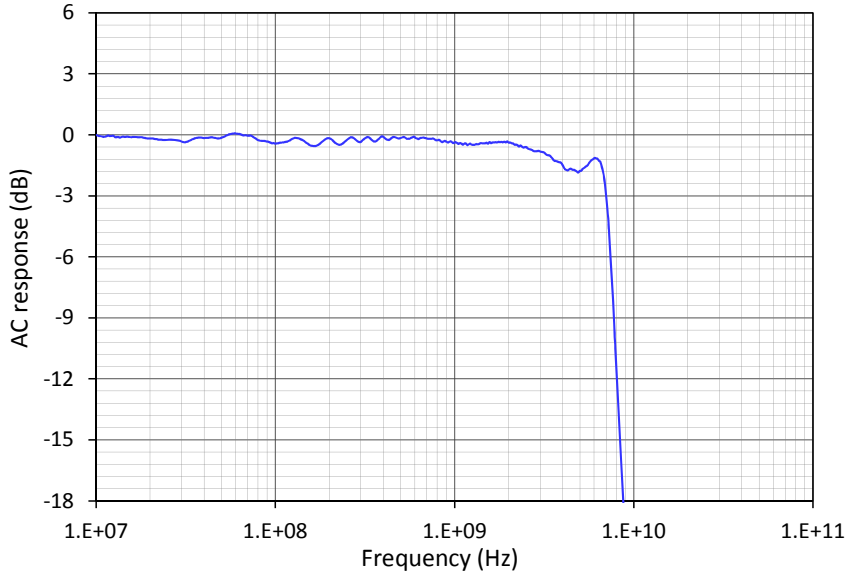


Figure 6.26: AC response of 8-channel receiver with Ge 10E1 waveguide photodiode

Transient Response

The transient response of the 8-channel receiver together with the wire bonded Ge 10E1 photodiode array recorded at a data rate of 1 Gbps and a bias voltage $V_{bias} = 2.0$ V is shown in fig. 6.27. The transient response shows neither overshooting nor ringing and has a rise time of $t_r = 71$ ps and a fall time of $t_f = 66$ ps.

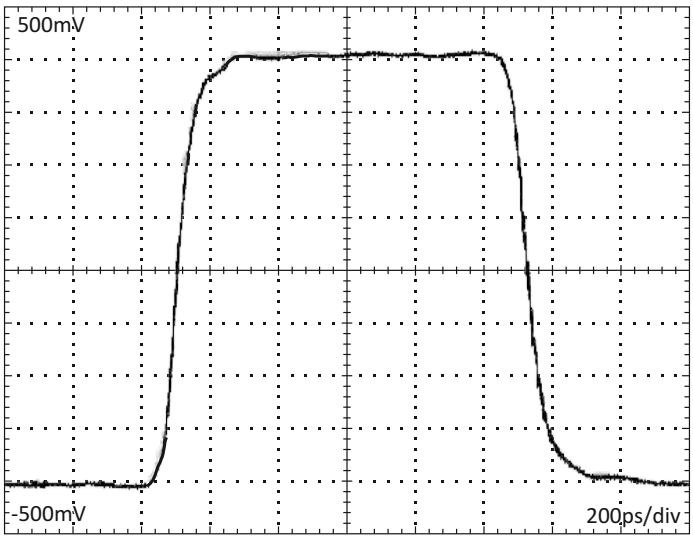


Figure 6.27: Transient response of 8-channel receiver with 10E1 Ge waveguide photodiode @ 1 Gbps

Eye Diagram

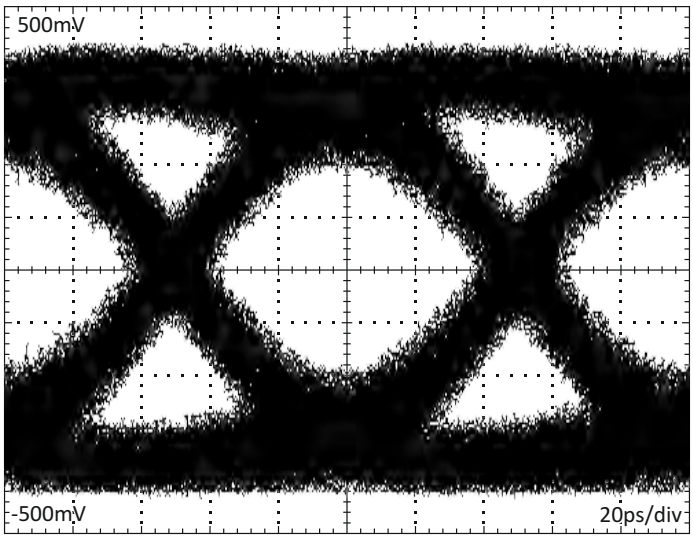


Figure 6.28: Eye diagram of 8-channel receiver with Ge 10E1 waveguide photodiode @ 10 Gbps, $P_{opt} = 55\ \mu$W ($Q = 6$)

Fig. 6.28 shows the eye diagram of the receiver with the wire bonded Ge 10E1 waveguide photodiode array at a Q-factor $Q = 6$. The eye diagram was recorded by using a 10 Gbps PRBS31 data signal with an optical power $P_{opt} = 55\ \mu$W. The resulting poor sensitivity in the range of -12.5 dBm is caused by the low photodiode responsivity of only 0.15 A/W (tab. 3.9) and the lowering of the receiver transimpedance to 100 kΩ necessary for reaching the required bandwidth.

Sensitivity and Bit-Error Rate

To record the bit-error rate of the receiver with the wire bonded Ge 10E1 photodiode array in dependence on the optical power a PRBS31 input signal with a data rate of 10 Gbps was used. As shown in fig. 6.29 only a relatively low sensitivity of -12.65 dBm at $BER = 10^{-9}$ and -11.65 dBm at $BER = 10^{-12}$ was reached. As mentioned above these low values can be explained by the low photodiode responsivity and the reduced receiver transimpedance.

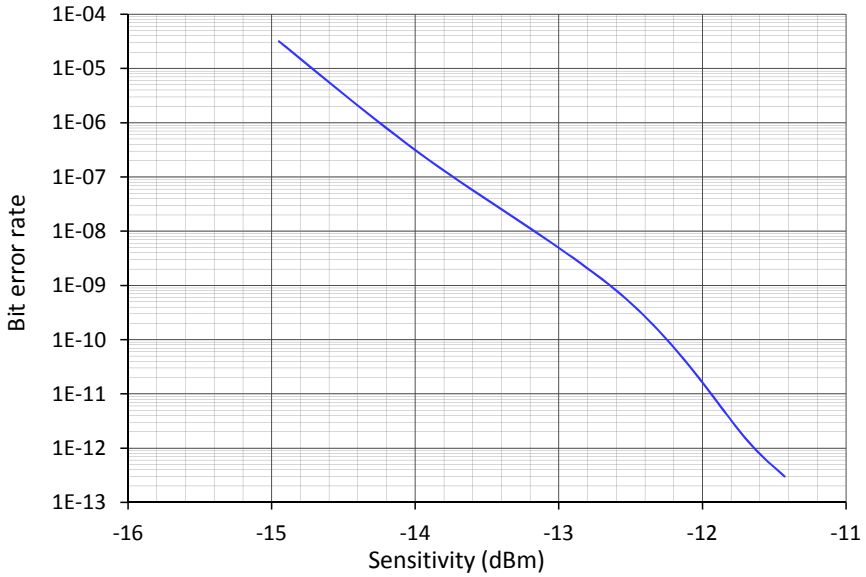


Figure 6.29: Sensitivity of 8-channel receiver with Ge 10E1 waveguide photodiode @ 10 Gbps, PRBS31

Crosstalk

The crosstalk between the different receiver channels of the receiver with the wire bonded Ge photodetector array was recorded by stepping the wavelength of the optical 10 Gbps

input signal from 1530 – 1560 nm and recording the output signal amplitude of one distinct receiver channel. Fig. 6.30 shows that the crosstalk between two neighboring receiver channels is in the range of −20 dBm. Comparing this value with the optical crosstalk between two AWG channels of the waveguide photodiode array (see fig. 6.3) it can be concluded that the crosstalk shown in fig. 6.30 is caused again mainly by the optical properties of the AWG.

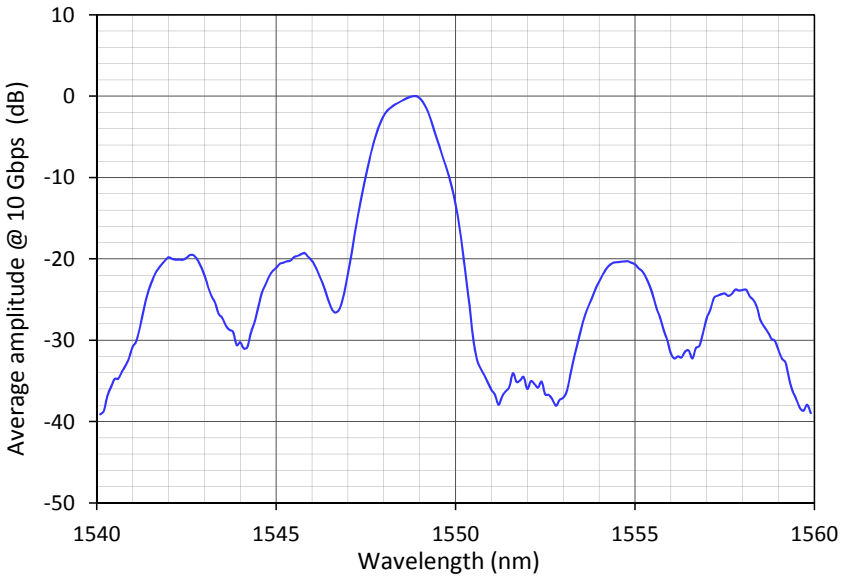


Figure 6.30: Crosstalk of 8-channel receiver with Ge 10E1 waveguide photodiode

6.6 Summary of Characterization Results

The measurement results of the relevant receiver parameters depending on the used photodiodes (no photodiode, PIN7, 10E1, IMEC) are summarized in tab. 6.1. The first column in tab. 6.1 shows the measurement results of the electrical characterization of the stand-alone receiver without photodetector. The comparison of the measured receiver performance with the results of the postlayout simulation shows a good compliance (see tab. 5.13). The characterization results of the receiver with the PIN7 photodiodes are also in good accordance to the postlayout simulation results (see tab. 5.13). On the other hand the receiver performance leaves a lot to desire if wire bonded 10E1 or InP/InGaAs photodiodes are used as detectors. The combination of poor responsivity and wire bonding diodes, which were designed for heterogeneous integration originally, inhibits a good performance. Thus the low sensitivity of only −12.6 dBm ($BER = 10^{-9}$) is not astonishing for those configurations.

Table 6.1: Characterization results of 8-channel receiver with different photodetectors ($\lambda = 1550$ nm)

Parameter	Measured values			
	electrical	PIN7	10E1	IMEC
Photodiode bias voltage	–	2.0 V	2.0 V	7.0 V
Supply voltage		3.3 V		
Power consumption		1.39 W		
Output swing @ 50 Ω		800 mVpp		
Total transimpedance	270 kΩ	125 kΩ	100 kΩ	100 kΩ
−3 dB cutoff frequency	7.59 GHz	7.89 GHz	7.05 GHz	7.03 GHz
Rise time	55 ps	63 ps	71 ps	73 ps
Fall time	51 ps	61 ps	66 ps	67 ps
Optical input power (Q = 6)	1.6 μW	10.0 μW	55.0 μW	60.0 μW
Photodiode responsivity	1.0 A/W	0.5 A/W	0.15 A/W	0.14 A/W
Sensitivity ($BER = 10^{-9}$)	−28.13 dBm	−20.00 dBm	−12.65 dBm	−12.60 dBm
Sensitivity ($BER = 10^{-12}$)	−27.52 dBm	−18.75 dBm	−11.65 dBm	−11.33 dBm
Crosstalk	–	–	−20 dB	−20 dB

However, the receiver was originally designed for use with heterogeneous integrated photodiodes on top of the receiver chip. As mentioned in chapter 4 the main advantages of the heterogeneous integration are the minimized parasitics of the interconnection between receiver and diode. Unfortunately CEA-LETI as well as IMEC had substantial problems with the heterogeneous integration of the photodetectors on top of the receiver chip. Thus the lateral Ge 10E1 and the vertical InP/InGaAs photodiodes with GSG pads, originally designed for the detector characterization only, were wire bonded to the receiver. The consequences are undesired large parasitic capacitances and inductances. Therefore it is necessary to reduce the total transimpedance of the receiver from 270 kΩ to 100 kΩ to achieve the required data rate of 10 Gbps. This gain reduction is equivalent to a sensitivity loss of 4.3 dBm. If the sensitivity loss due to the conventional wire bonding instead of heterogeneous integration is considered, the measurement results are again in good accordance with the postlayout simulation results.

Nevertheless all receiver/photodiode combinations reach a −3 dB cutoff bandwidth of more than 7 GHz and thus are capable of data rates up to 10 Gbps. The maximum data rate is also confirmed by the eye diagrams. The eye diagrams of the different receiver configurations are recorded at 10 Gbps data rate and at an optical input power which is equivalent to a BER of 10^{-9} ($Q = 6$).

To make sure that the influence of the neighboring channels of the 8-fold receiver together with waveguides and AWGs is not a crucial factor for the receiver performance the crosstalk between the different receiver channels was measured. It turned out that the crosstalk

between neighboring channels is in the range of −20 dB. A comparison of the crosstalk measurement results with the optical output power of the AWG in dependence on the wavelength (see fig. 6.3) shows that the crosstalk is mainly caused by the optical properties of the AWG. The crosstalk of the receiver with diodes from CEA-LETI and IMEC is similar due to the fact that both AWGs are fabricated by IMEC.

Concluding it can be said that the performance of the designed receiver strongly depends on the properties of the used photodetectors. For the sensitivity of the receiver the photodetector responsivity and the parasitic capacitances of the connection structures between diode and receiver are the crucial factors. Measurement results show that the receiver reaches a sensitivity of −20 dBm ($BER = 10^{-9}$) with the conventional wire bonded PIN7 photodiode (0.5 A/W). Simulation results (see tab. 5.13) show that using heterogeneous integrated photodetectors with a state-of-the-art responsivity of $0.8 - 1.0$ A/W ([37], [44], [45], [51]) would increase the sensitivity up to −26 dBm. Unfortunately no heterogeneous integrated demonstrators from CEA-LETI or IMEC are available on one hand and on the other hand the responsivity of the provided diodes is very low (0.15 A/W). The result is the poor sensitivity of only −12.6 dBm ($BER = 10^{-9}$). Finally it can be concluded that the photonic integration of waveguide photodiodes together with (de)multiplexing AWG structures on a photonic chip, which is mounted heterogeneously on top of the CMOS chip is a forward-looking integration technology. Nevertheless the responsivity of the used diodes and the optical attenuation of the waveguide and AWG structures have to be improved to be competitive with state-of-the-art waveguide photodiodes.

7 Conclusion

The focus of this PhD thesis was the design of an 8×10 Gbps optical receiver, fabricated in austriamicrosystems 0.35 μm SiGe BiCMOS process, for use with conventional wire bonded photodiodes on one hand and heterogeneously integrated photodiodes on the other hand. The used diodes were provided by CEA-LETI and IMEC, two project partners of the European Community project HELIOS (FP 224312). The photodetectors fabricated by IMEC are based on InP/InGaAs, have a vertical PIN structure and are designed for heterogeneous die-to-wafer bonding on top of the CMOS wafer. CEA-LETI provided lateral Ge PIN photodiodes for heterogeneous wafer-to-wafer bonding as well as vertical Ge PIN diodes for conventional wire bonding.

The characterization of the various photodiode types and connection structures indicated significant differences concerning the parasitic capacitances and the responsivities. The overall capacitances of the heterogeneously integrated diodes are in the range of 30 fF while the capacitances of the wire bonded diodes are in the range of 300 fF. In contrast the integrated diodes have poor responsivities of only 0.15 A/W compared to the wire bonded diodes with responsivities of 0.5 A/W. Simulations of the receiver circuitry together with the different detector parameters showed that it was impossible to design one receiver which works with all photodetector types. Thus two receiver versions were optimized for heterogeneously integrated photodiodes while a third version was designed for use with wire bonded diodes.

Postlayout simulation results show that the total transimpedance of the receiver used with heterogeneous integrated photodiodes of 275 kΩ has to be reduced to 130 kΩ for use with wire bonded diodes. At the same time the equivalent input noise current increases from below 400 nA (integrated detectors) up to 900 nA (wire bonded diodes). Nevertheless the simulation results indicated a sensitivity of -19.7 dBm ($BER = 10^{-9}$) for the wire bonded photodiode and a sensitivity ($BER = 10^{-9}$) of -17.9 dBm (CEA-LETI), respectively -17.6 dBm (IMEC) for the heterogeneously integrated detectors. These results show that the benefit of the heterogeneous detector integration (-3.3 dB sensitivity) is eliminated by the poor photodiode responsivity ($+5.3$ dB sensitivity).

Due to the fact that CEA-LETI as well as IMEC had substantial problems with the heterogeneous integration of the photonic chip on top of the CMOS chip, no demonstrators with heterogeneously integrated photodetectors were available for the final characterization. Therefore the photodiodes originally designed for heterogeneous integration were also conventionally wire bonded to the receiver chip. The final characterization

confirmed the postlayout simulation results widely. The receiver with the wire bonded vertical Ge photodiode PIN7 has a total transimpedance of 125 kΩ, a −3 dB cutoff frequency of 7.89 GHz and a measured sensitivity of −20 dBm ($BER = 10^{-9}$), respectively −18.75 dBm ($BER = 10^{-12}$). In contrast the receivers with the wire bonded diodes, originally designed for heterogeneous integration, reach a total transimpedance of 100 kΩ, a −3 dB cutoff frequency slightly above 7 GHz and sensitivities of −12.65 dBm (CEA-LETI) and −12.60 dBm (IMEC) at $BER = 10^{-9}$, respectively −11.65 dBm (CEA-LETI) and −11.33 dBm (IMEC) at $BER = 10^{-12}$. All receiver versions have a power consumption of 1.39 W at a supply voltage of 3.3 V and an output swing of 800 mVpp. The poor performance of the receiver chips with the wire bonded diodes which were originally designed for heterogeneous integration can be explained by the small responsivities on one hand and the large parasitics due to the wire bonding on the other hand.

A comparison of the various receiver parameters of the fabricated amplifier chips with some state-of-art 1550nm 10 Gbps optical front-ends that are based on Si-related technologies is shown in tab. 7.1. The direct comparison of the different front-ends shows that either photodiodes with responsivities larger than in this work were used [52], [53], [54], [55], [56] or the receiver was characterized only electrical without photodetector [57], [58]. The used photodiodes, with exception of the monolitically integrated Ge waveguide photodiode in [56], are wire bonded to the receiver chip and have responsivities in the range of 0.6 − 1.0 A/W. Nevertheless the receiver with the wire bonded PIN7 Ge photodiode reaches after [54] the second best sensitivity of all listed front-ends. The receiver described in [54] reaches a higher sensitivity due to the use of a photodiode with a responsivity of 0.85 A/W on one hand and a LC ladder input filter to compensate for the large photodetector capacitance on the other hand.

Taking into account the relatively low responsivity of 0.5 A/W ([37], [44], [45], [51]) of the PIN7 photodiode, a sensitivity improvement of around −3 dB can be expected if a photodiode with a state-of-art responsivity of around 1 A/W would be used. Simulations show that the heterogeneous integration of the photodetectors would increase the sensitivities by further −3 dB. Thus sensitivities of around −26 dBm ($BER = 10^{-9}$) could be achieved by using heterogeneously integrated photodetectors with responsivities of around 1 A/W.

Concluding it can be said that the heterogeneous integration of the photonic chip on top of the CMOS chip is a forward-looking way to improve the performance of optical receivers. Nevertheless this technology seems to be still in the fledgling states. Further research will be necessary to improve this novel interconnection method.

Table 7.1: Performance comparison of 10 Gbps optical receiver

	Technology	Connection type	Photodiode capacitance	Responsivity	−3 dB cutoff frequency	Data rate	Total trans-impedance	Sensitivity ($BER = 10^{-12}$)
This work (PIN7)	0.35 μm SiGe BiCMOS	wire bonded	0.25 pF	0.5 A/W	7.89 GHz	8×10 Gbps	125 kΩ	−18.8 dBm
This work (10E1)	0.35 μm SiGe BiCMOS	wire bonded	0.3 pF	0.15 A/W	7.05 GHz	8×10 Gbps	100 kΩ	−11.7 dBm
This work (IMEC)	0.35 μm SiGe BiCMOS	wire bonded	0.3 pF	0.14 A/W	7.03 GHz	8×10 Gbps	100 kΩ	−11.3 dBm
[52] PTL2012	SiGe BiCMOS	wire bonded	n. a.	0.9 A/W	n. a.	10×11.1 Gbps	n. a.	−14.0 dBm
[57] ISSSE2010	0.18 μm CMOS	no PD	0.5 pF	no PD	7.0 GHz	10 Gbps	100 kΩ	−14.6 dBm
[53] ICACT2009	0.13 μm CMOS	wire bonded	0.25 pF	0.7 A/W	8.2 GHz	10 Gbps	56 kΩ	−18.5 dBm
[54] SOPO2009	0.13 μm BiCMOS	wire bonded	0.6 pF	0.85 A/W	7.8 GHz	10 Gbps	62 kΩ	−22.0 dBm
[58] CICC2008	0.35 μm SiGe BiCMOS	no PD	1.1 pF	no PD	8.85 GHz	10 Gbps	232 kΩ	−16.4 dBm
[55] VLSI2007	0.18 μm CMOS	wire bonded	0.15 pF	1.0 A/W	7.86 GHz	10 Gbps	32 kΩ	−13.0 dBm
[56] GFP2007	0.13 μm CMOS	monolithic integrated	n. a.	0.6 A/W	7.86 GHz	10 Gbps	n. a.	−14.2 dBm

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